Semiconductor IC

Data Book 1992 Computer Audio/Video

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Computer Audio/Video

1992

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Computer Audio/Video Semiconductor Data Book 1992

Preface

The history of Sony Semiconductor began in 1954, with the first commercial introduction of the transistor in Japan. Since then, Sony has applied this leading edge, innovative technology in the development of the Semiconductors, currently used in most of its consumer and professional electronic products.

This Computer Audio/Video semiconductor data book has been compiled with the aim of providing the circuit designer with a reference guide describing Sony's presently available line, together with application information for each category of Computer Audio/Video Semiconductors.

Computer Audio/Video Numerical Index

Part Number	Application	Function	Voltage	Package	Page
CXA1145P/M	Color Encoding (Analog)	RGB input, NTSC/PAL Video out	5V	24P DIP/SOP	116
CXA1213AS	Color Decoding (Analog)	Chrominance Processor, RGB out	9V	48P SDIP	25
CXA1214P	Color Decoding (Analog)	SECAM, Video in, UV output	9V	24P DIP	51
CXA1218S CXA1228S	Color Decoding (Analog)	NTSC/PAL, Video in, YUV output	5V	28P SDIP	65
CXA1219P/M CXA1229P/M	Color Encoding (Analog)	YUV input, NTSC/PAL Video out	5V	24P DIP/SOP	131
CXA1236Q	Data Conversion; D/A	8bit 500MSPS Single VIDEO DAC (ECL input)	-4.5V	44P QFP	200
CXA1365S	Synchronization/ Timing	Sync Separator for CRT	9V	28P SDIP	156
CXA1385Q	Color Decoding (Analog)	NTSC, Video in, RGB output with BPF & DL	5V	32P QFP	80
CXA1387S	Miscellaneous	Aperture Corrector	9V	30P SDIP	272
CXA1451M	Miscellaneous	Video switch with 75ohm driver	±5V	16P SOP	290
CXA1496AQ	Data Conversion; A/D	10bit 20MSPS A/D	±5V	48P QFP	195
CXA1693Q	Data Conversion; A/D	Sample and Hold for A/D	±5V	32P QFP	196
CXD1030M	Synchronization/ Timing	NTSC/PAL Sync Generator	5V	28P SOP	167
CXD1160AP/AQ	Audio Processing	Digital Audio Signal Processor	5V	28P DIP 80P QFP	299
CXD1172AM/AP	Data Conversion: A/D	6bit 20MSPS Video A/D	5V	16P SOP/DIP	197
CXD1176Q	Data Conversion; A/D	8bit 20MSPS Video Low Power	5V	32P QFP	198
CXD1178Q	Data Conversion; D/A	8bit 40MSPS RGB 3-Channel D/A	5V	48P QFP	201
CXD1179Q	Data Conversion; A/D	8bit 35MSPS Video low-power	5V	32P QFP	199
CXD1185AQ	CD-ROM	SCSI Controller Direct interface w/CXD1186Q	5V	64P QFP	383
CXD1186Q	CD-ROM	CD-ROM Decoder (ECC, Buffer control)	5V	80P QFP	413
CXD1196R	CD-ROM	CD-ROM Decoder w/ADPCM, D/F	5V	80P VQFP	457
CXD1225M	Synchronization/ Timing	Frequency Synthesizer	5V	14P SOP	176
CXD1229Q	Synchronization/ Timing	NTSC Sync Processor	5V	48P QFP	187
CXD1244S	Audio Processing	100dB Attenuation Digital Filter	5V	40P SDIP	351
CXD2011Q	Digital Processing	Comb Filter	5V	80P QFP	202
CXD2500AQ/AQZ	CD-ROM	CD Digital Signal Processor	5V	80P QFP	460
CXD2552Q	Audio Processing	Pulse D/A Converter	5V	44P QFP	364
CXD2555Q	Audio Processing	Audio Delta Sigma Type A/D+D/A+D/F	5V	48P QFP	372
CXK1202Q	Digital Processing	Digital Delay Line Memory	5V	32P QFP	213
CXK1202S	Digital Processing	Digital Delay Line Memory	5V	28P SDIP	222
CXK1206M	Digital Processing	1Mbit, 3 port Video Memory	5V	38P SOP	232
V7021	Color Decoding (Analog)	NTSC/PAL, Video in, RGB output	5V	28P SDIP	99
V7040	Color Encoding (Analog)	RGB input, NTSC/PAL Video out, Superimpose	5V	28P SDIP	142

Functional Index

Video Processing

Color Decoding (Analog)

Part Number	Function	Voltage	Package	Page
CXA1213AS	Chrominance Processor, RGB out	9V	48P SDIP	25
CXA1214P	SECAM, Video in, UV output	9V	24P DIP	51
CXA1218S/1228S	NTSC/PAL, Video in, YUV output	5V	28P SDIP	65
CXA1385Q	NTSC, Video in, RGB output with BPF & DL	5V	32P QFP	80
V7021	NTSC/PAL, Video in, RGB output	5V	28P SDIP	99

Color Encoding (Analog)

CXA1145P/M	RGB input, NTSC/PAL Video out	5V	24P DIP/SOP	116
CXA1219/1229P/M	YUV input, NTSC/PAL Video out,	5V	24P DIP/SOP	131
V7040	RGB input, NTSC/PAL Video out, Superimpose	5V	28P SDIP	142

Synchronization/Timing

CXA1365S	Sync Separator for CRT	9V	28P SDIP	156
CXD1030M	NTSC/PAL Sync Generator	5V	28P SOP	167
CXD1225M	Frequency Synthesizer	5V	14P SOP	176
CXD1229Q	NTSC Sync Processor	5V	48P QFP	187

Analog to Digital Conversion (For more information refer to the Sony Converter Data Book)

CXA1496AQ	10-bit 20MSPS A/D Converter	±5V	48P QFP	195
CXA1693Q	High Speed Sample and Hold A/D Converter	±5V	32P QFP	196
CXA1172AM/AP	6bit 20MSPS Video A/D Converter	5V	16 SOP/DIP	197
CXD1176Q	8bit 20MSPS Video A/D Converter	5V	32P QFP	198
CXD1179Q	8bit 35MSPS Video A/D Converter	5V	32P QFP	199

Digital to Analog Conversion (For more information refer to the Sony Converter Data Book)

CXA1236Q	8bit 500MSPS Single Video DAC (ECL input)	-4.5V	44P QFP	200
CXD1178Q	8bit 40MSPS RGB 3-channel D/A Converter	5V	48P QFP	201

Digital Processing

CXD2011Q	Comb Filter	5V	80P QFP	202
CXK1202Q	Digital Delay Line Memory	5V	32P QFP	213
CXK1202S	Digital Delay Line Memory	5V	28P SDIP	222
CXK1206M	1Mbit, 3 port Video Memory	5V	38P SOP	232

Miscellaneous

CXA1387S	Aperture Corrector	9V	30P SDIP	272
CXA1451M	Video switch with 75ohm driver	±5V	16P SOP	290

Audio Processing

Part Number	Function	Voltage	Package	Page
CXD1160AP/AQ	Digital Audio Signal Processor	5V	28P DIP/ 80P QFP	299
CXD1244S	100dB Attenuation Digital Filter	5V	40P SDIP	351
CXD2552Q	Pulse D/A Converter	5V	44P QFP	364
CXD2555Q	Audio Delta Sigma Type A/D+D/A+D/F	5V	48P QFP	372

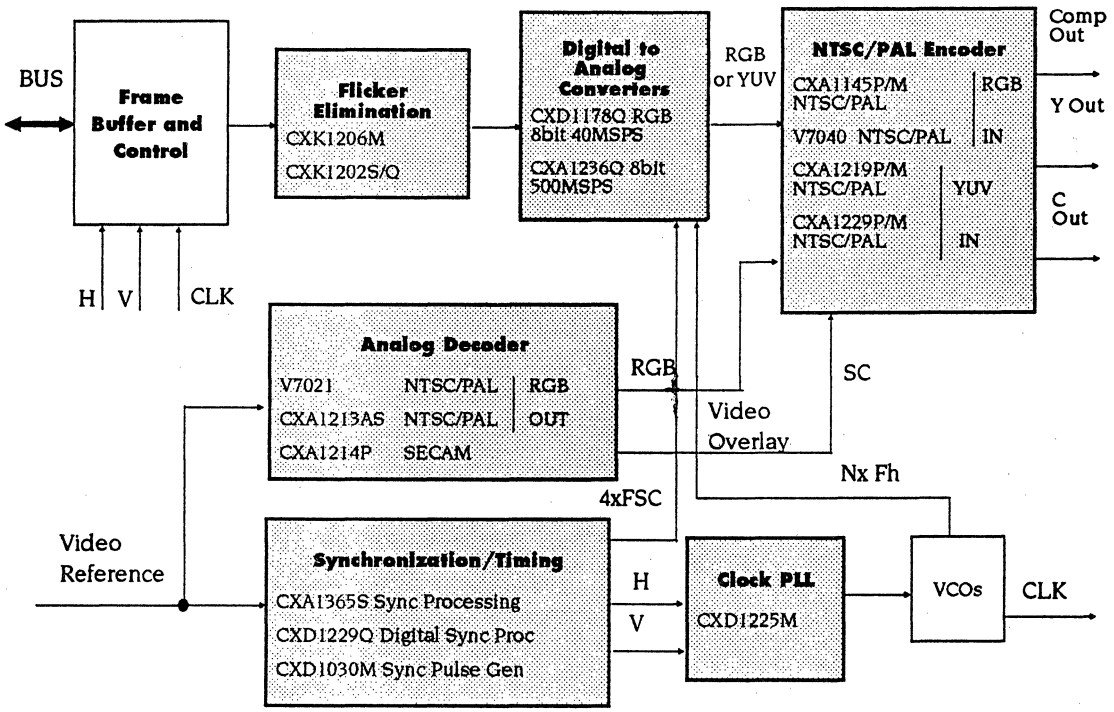
CD-ROM Processing

Part Number	Function	Voltage	Package	Page
CXD1185AQ	SCSI Controller Direct interface w/CXD1186Q	5V	64P QFP	383
CXD1186Q	CD-ROM Decoder (ECC, Buffer control)	5V	80P QFP	413
CXD1196R	CD-ROM Decoder with ADPCM, D/F	5V	80P VQFP	457
CXD2500AQ/AQZ	CD Digital Signal Processor	5V	80P QFP	460

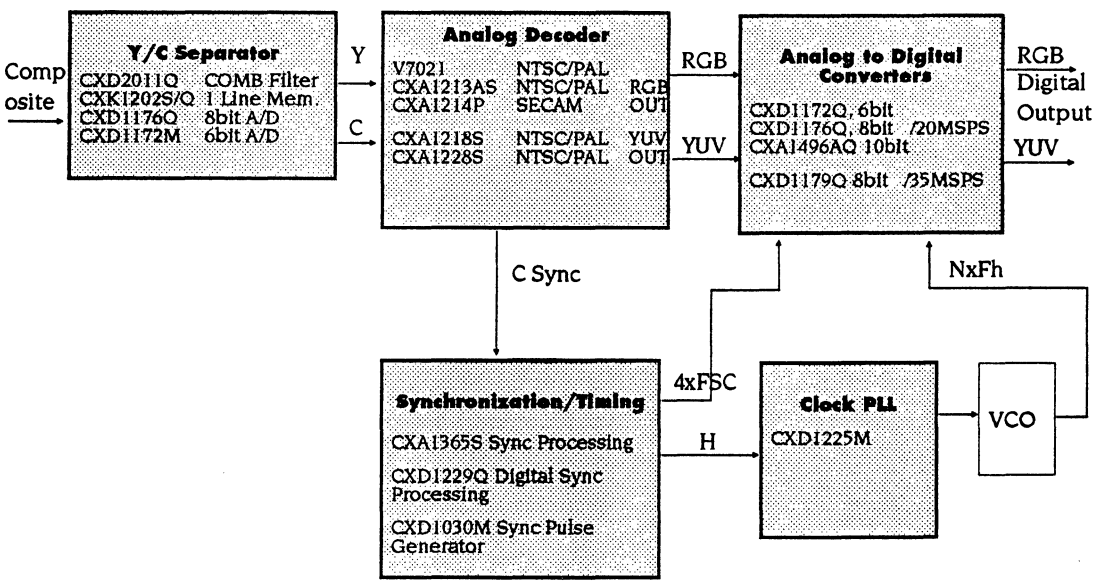
Application Notes

Reference Number	Description	Recommended IC's	Page
CAV01	Audio A/D + D/A interface	CXD2555Q	509
CAV02	NTSC/PAL encoder Y, C interface	CXA1145P/M	511
CAV03	NTSC/PAL decoder & Comb filter	CXA1228S, CXL5504M	512
CAV04	Digital comb filter interface	CXD2011Q, CXK1202S/Q, CXD1176Q, CXA1365S, CXD1030M	515
CAV05	NTSC/PAL Encoder, RAMDAC interface	CXA1145M, CXD1030M, CXK1202S/Q	517
CAV06	Gen Lock circuit	CXA1365S, CXD1030M	518
CAV07	NTSC/PAL Decoder digital interface	CXA1228S, CXD1179Q, V7021, CXD1172AM, CXD1030M, CXK1206M, CXA1365S	520
CAV08	New CD-ROM Decoder	CXD1196R, CXD2552Q	522

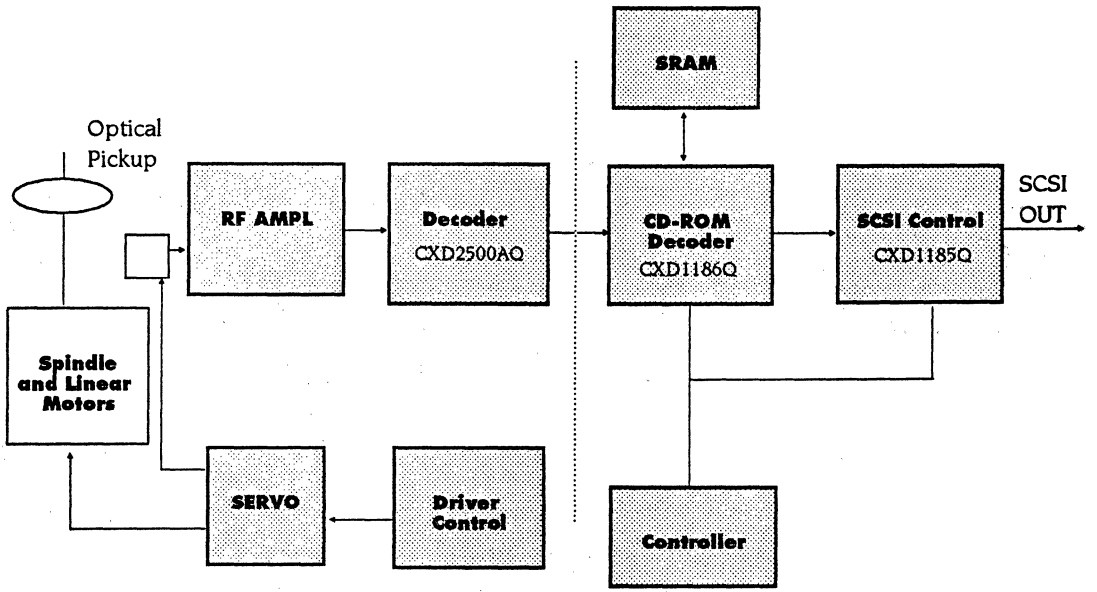
Video Output with Graphics Overlay



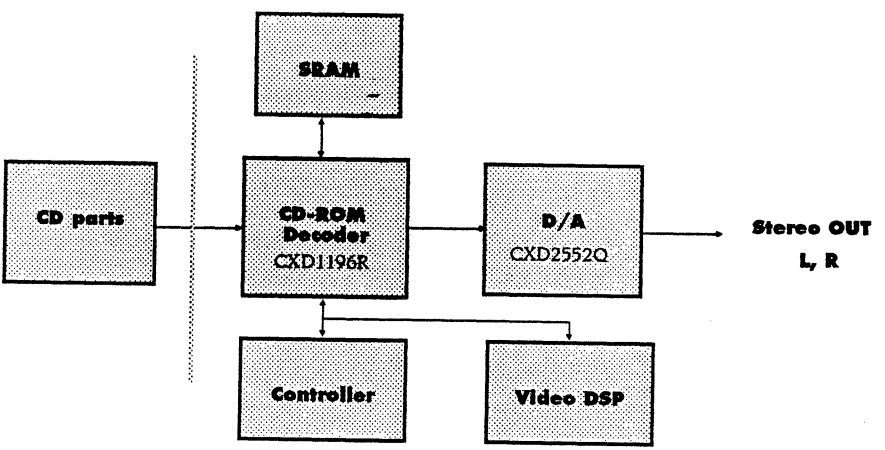
Video Input Digitizing



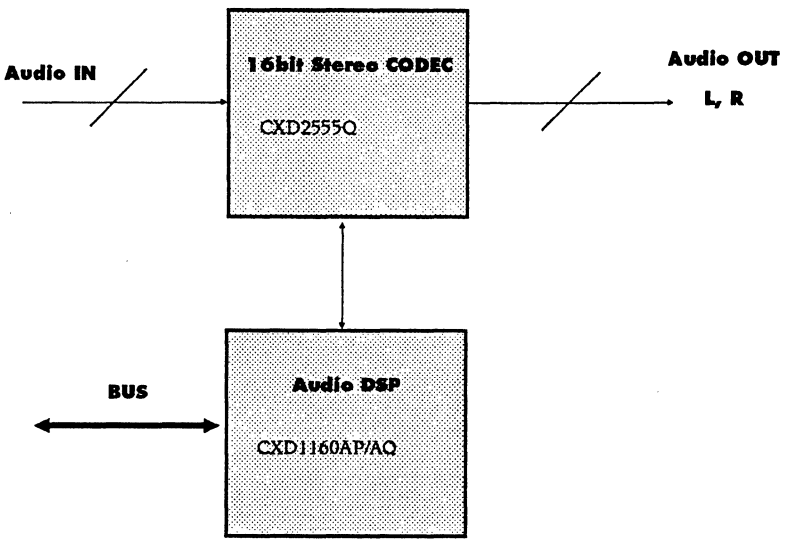
CD-ROM

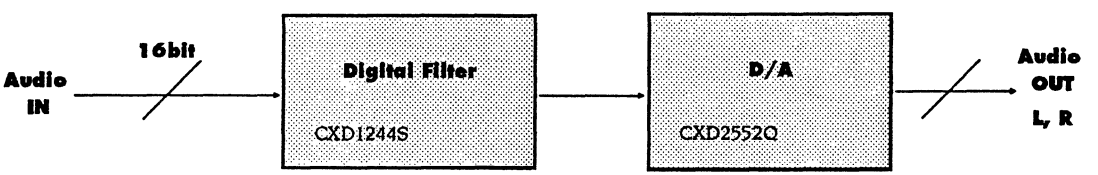


If CXD1196R is included,



Digital Audio





3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] C X 2 0 0 1 1 A

- Improvement mark
  - "A" is affixed when specifications are partially improved.
- Product number
  - Identifies individual product.
- Category number
  - Indicates the product category in one or two digits.
    - Bipolar IC: 0, 1, 8, 10, 20, 22
    - MOS IC: 5, 7, 23, 79
- Sony IC mark

b) New nomenclature

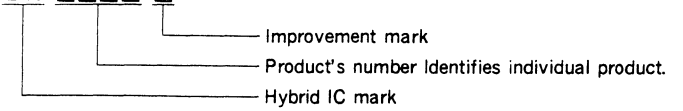
[Example] C X A 1 0 0 1 A P

- Package mark
  - P: Plastic Dual In-line Package
  - D: Ceramic Dual In-line Package
  - M: Small Outline L-Leaded Package
  - L: Single In-line Package
  - Q: Quad Flat L-Leaded Package
  - S: Shrink Dual In-line Package
  - N: Very Small Outline Package (SSOP)
  - R: Very Small Quad Flat Package
- Improvement mark
  - "A" is affixed when specifications are improved.
- Product number
  - Identifies the individual product.
- Product category mark
  - A: Bipolar IC
  - B: Bipolar digital IC
  - D: MOS logic IC
  - K: Memory, Mask ROM
  - P, Q: Microcomputer, Microprocessor
  - L: CCD signal processor
- Sony IC mark

2) Hybrids nomenclature

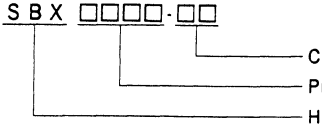
(1) Conventional nomenclature system

[Example] B X - □□□□ - □



(2) New nomenclature

[Example] S B X □□□□ - □□



Hybirds have carried SBX or BX prefix up to January 1987. i.e. BX-1452, Those developed after the above dute all stand by SBX. i.e. SBX1435/SBX1475.

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

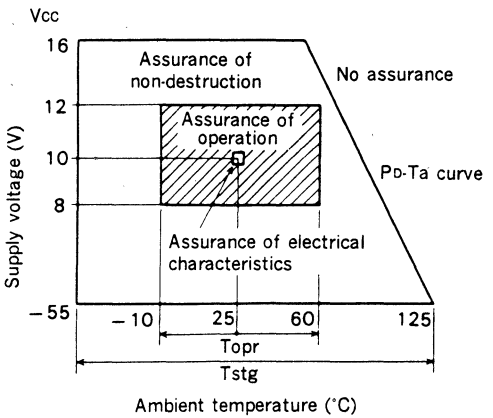
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

A general example on the relation with Absolute Maxium Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

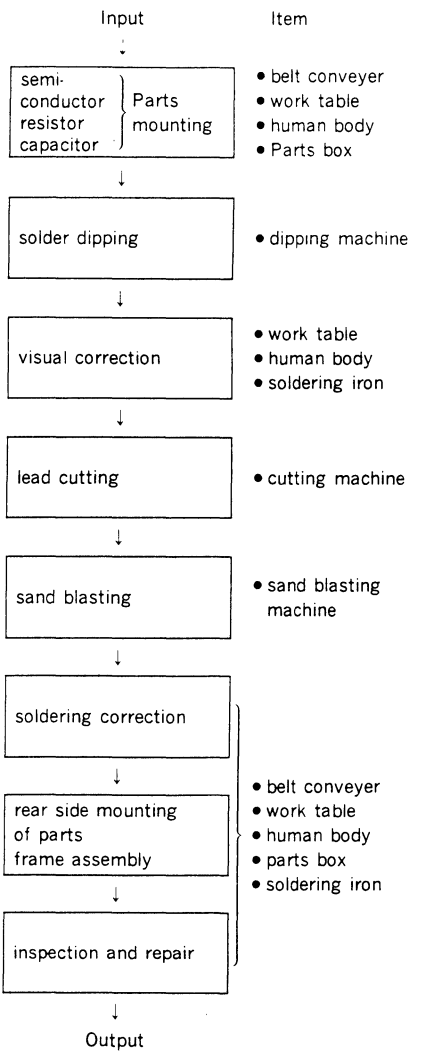
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room to about 50%.

Operator

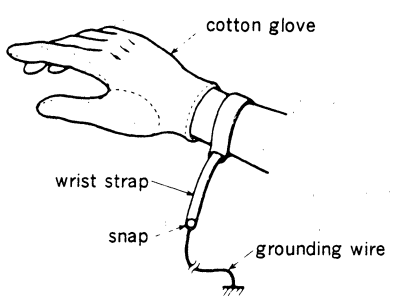
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

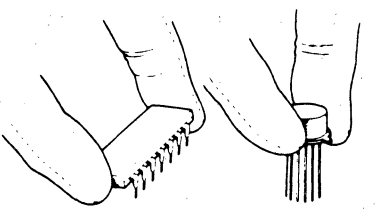


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

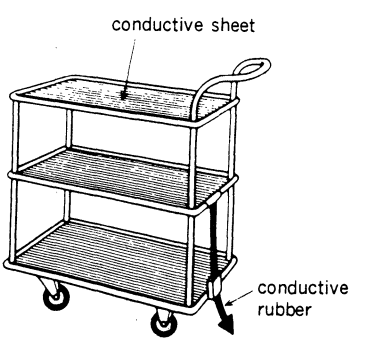
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

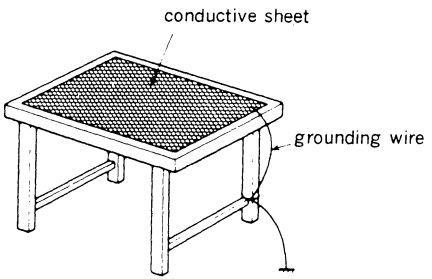
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

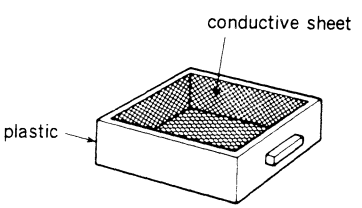
grounding of work table



(3) Semiconductor device case

Use a conductive case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

(5) Other points of caution

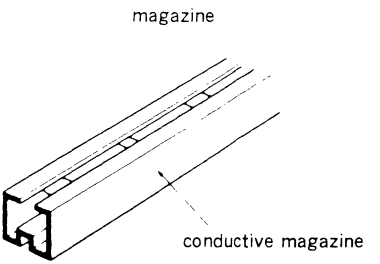
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

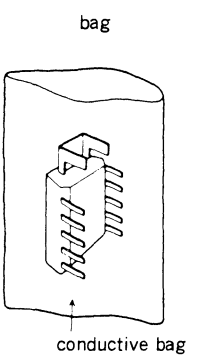
Use conductive, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

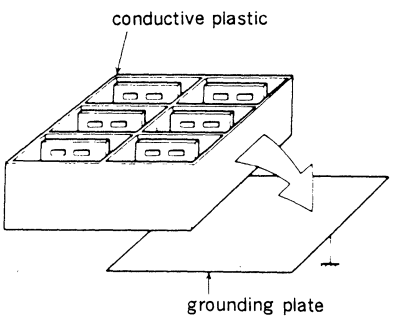
Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



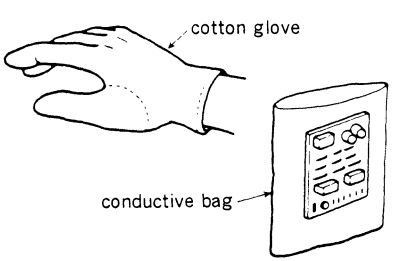
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

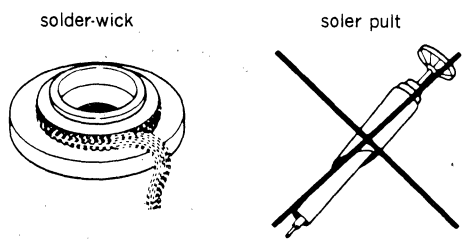
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table for soldering. Do not solder on foam styrol, vinyl, or melamine resin.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

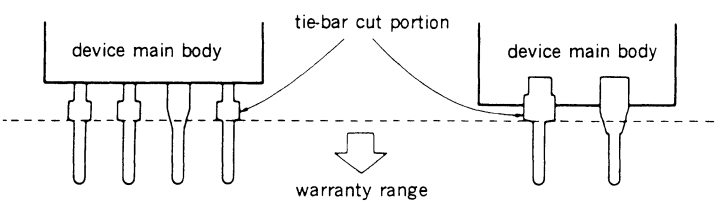
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

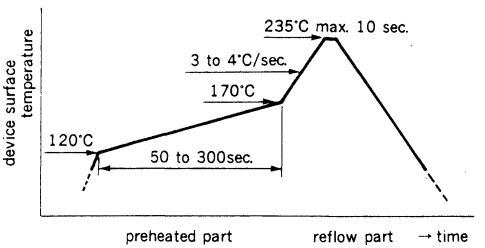
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

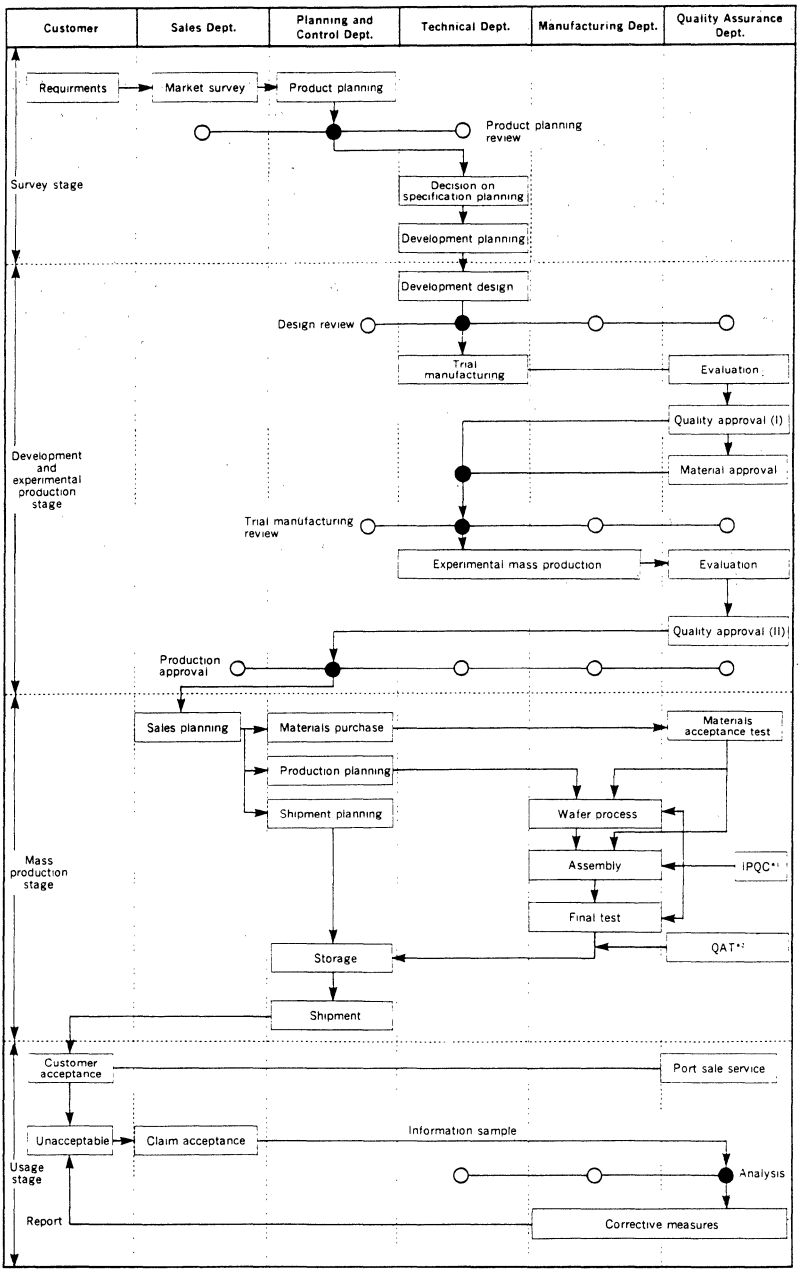
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

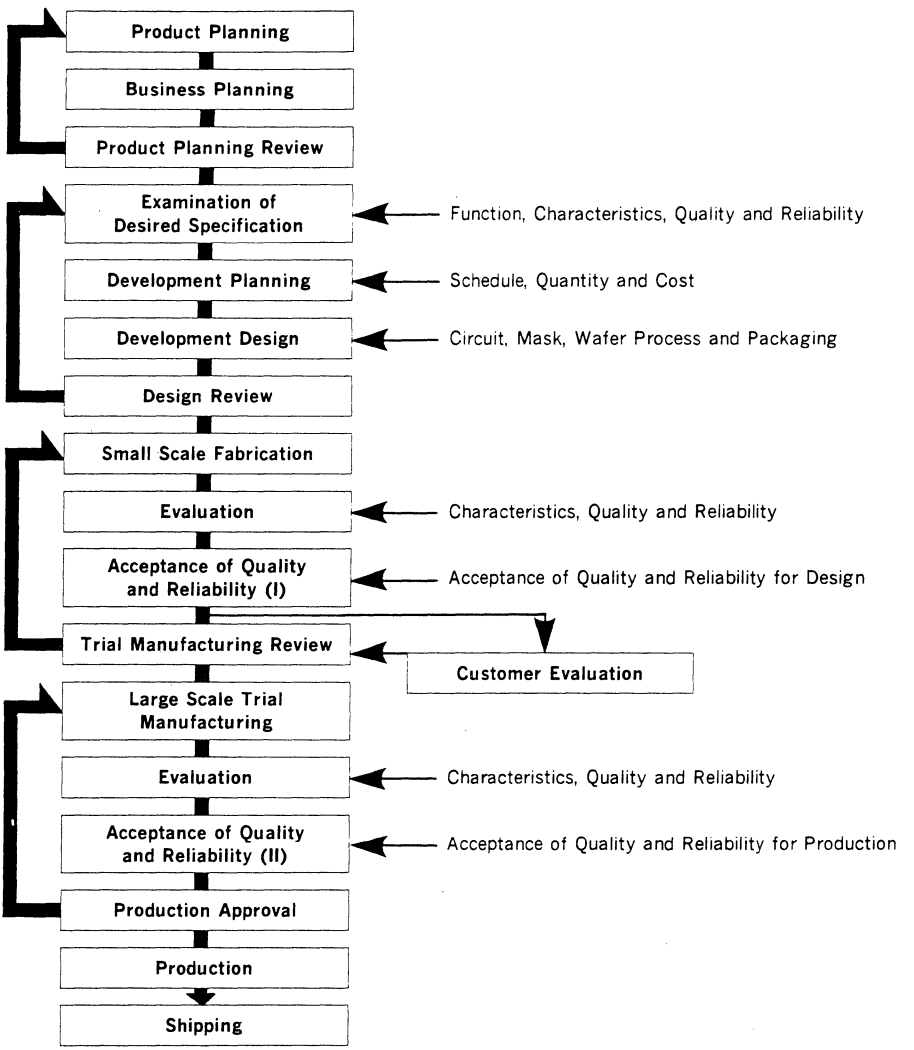
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

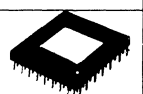
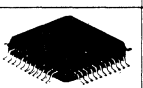
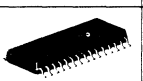
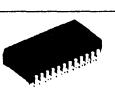
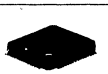
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole-Lead	1-direction
		Z I P	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	Q F J	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

* P·····Plastic, C·····Ceramic

Video Processing

Video Processing

Color Decoding (Analog)

Part Number	Function	Voltage	Package	Page
CXA1213AS	Chrominance Processor, RGB out	9V	48P SDIP	25
CXA1214P	SECAM, Video in, UV output	9V	24P DIP	51
CXA1218S/1228S	NTSC/PAL, Video in, YUV output	5V	28P SDIP	65
CXA1385Q	NTSC, Video in, RGB output with BPF & DL	5V	32P QFP	80
V7021	NTSC/PAL, Video in, RGB output	5V	28P SDIP	99

Color Encoding (Analog)

CXA1145P/M	RGB input, NTSC/PAL Video out	5V	24P DIP/SOP	116
CXA1219/1229P/M	YUV input, NTSC/PAL Video out,	5V	24P DIP/SOP	131
V7040	RGB input, NTSC/PAL Video out, Superimpose	5V	28P SDIP	142

Synchronization/Timing

CXA1365S	Sync Separator for CRT	9V	28P SDIP	156
CXD1030M	NTSC/PAL Sync Generator	5V	28P SOP	167
CXD1225M	Frequency Synthesizer	5V	14P SOP	176
CXD1229Q	NTSC Sync Processor	5V	48P QFP	187

Analog to Digital Conversion (For more information refer to the Sony Converter Data Book)

CXA1496AQ	10-bit 20MSPS A/D Converter	±5V	48P QFP	195
CXA1693Q	High Speed Sample and Hold A/D Converter	±5V	32P QFP	196
CXA1172AM/AP	6bit 20MSPS Video A/D Converter	5V	16 SOP/DIP	197
CXD1176Q	8bit 20MSPS Video A/D Converter	5V	32P QFP	198
CXD1179Q	8bit 35MSPS Video A/D Converter	5V	32P QFP	199

Digital to Analog Conversion (For more information refer to the Sony Converter Data Book)

CXA1236Q	8bit 500MSPS Single Video DAC (ECL input)	-4.5V	44P QFP	200
CXD1178Q	8bit 40MSPS RGB 3-channel D/A Converter	5V	48P QFP	201

Digital Processing

CXD2011Q	Comb Filter	5V	80P QFP	202
CXK1202Q	Digital Delay Line Memory	5V	32P QFP	213
CXK1202S	Digital Delay Line Memory	5V	28P SDIP	222
CXK1206M	1Mbit, 3 port Video Memory	5V	38P SOP	232

Miscellaneous

CXA1387S	Aperture Corrector	9V	30P SDIP	272
CXA1451M	Video switch with 75ohm driver	±5V	16P SOP	290

SONY CXA1213AS

Y/C/Jungle IC for PAL/NTSC

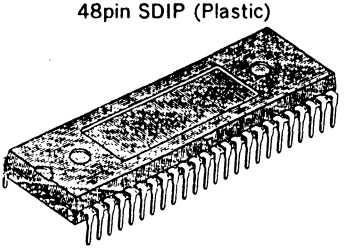
Description

The CXA1213AS is a Y/chroma/jungle signal processing IC of PAL, NTSC (4.43MHz, 3.58MHz) systems color TVs.

Features

- TV system is compatible with PAL,SECAM, and NTSC(4.43MHz,3.58MHz)through combination with the CXA1214P.
- No adjustment of H,V oscillation frequency by count down system.
- Built-in 50/60Hz automatic discrimination circuit and compulsory mode applicable.
- Built-in 3.58/4.43MHz color sub carrier oscillation frequency automatic discrimination circuit and compulsory mode applicable.
- Input prohibition gate function according to frequency of input vertical synchronization. (Noise elimination ability)
- Black expansion function. (New dynamic picture)
- High speed blanking function which blanks interval of characters.

48pin SDIP (Plastic)



- Built-in SHP circuit and OFF applicable.
- Auto white balance IC CXA1024S compatible.

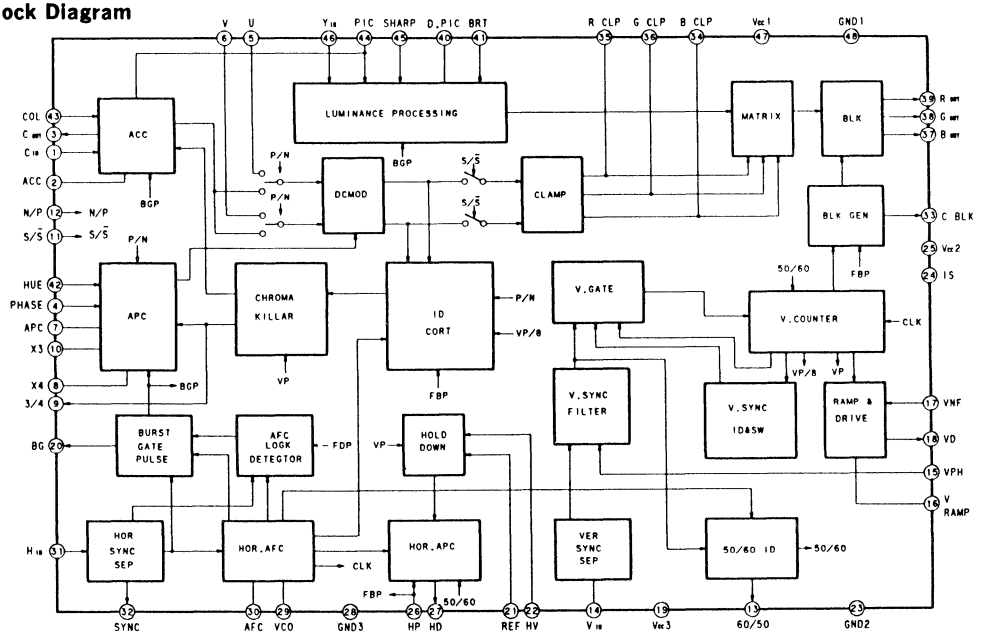
Applications

Color decoder for PAL/NTSC system

Structure

Bipolar silicon monolithic IC

Block Diagram



E90931-HP

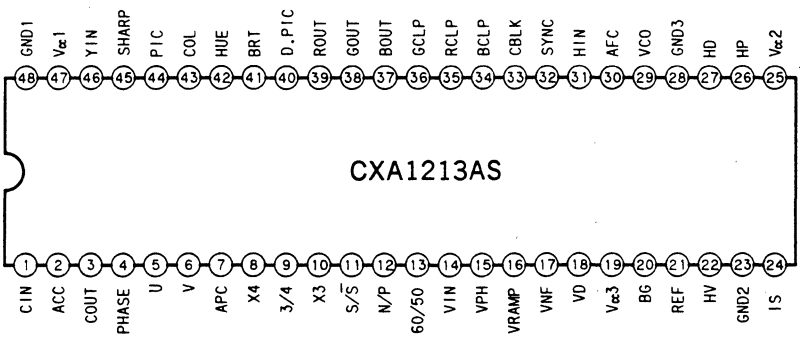
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	2.2	W

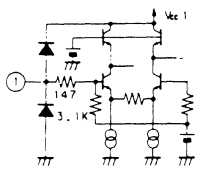
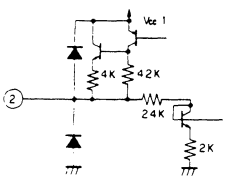
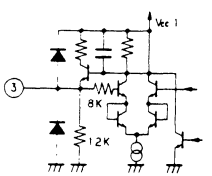
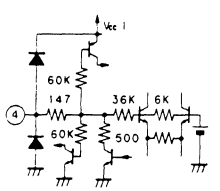
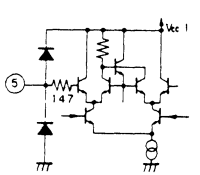
Recommended Operating Conditions

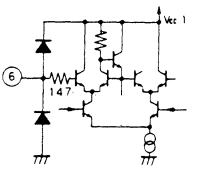
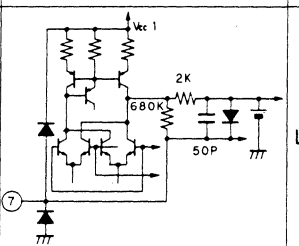
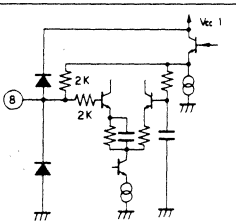
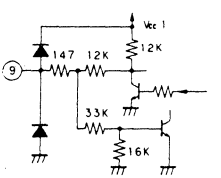
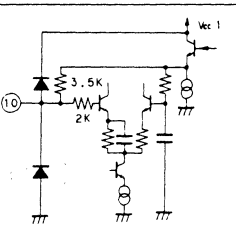
• Supply voltage	V_{CC}	9 ±1	V
• Operating temperature	T_{opr}	−20 to +75	°C

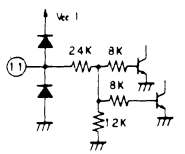
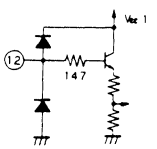
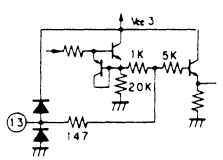
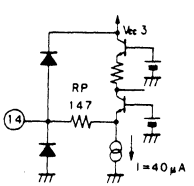
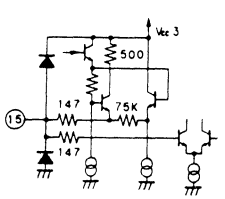
Pin Configuration

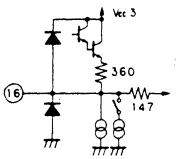
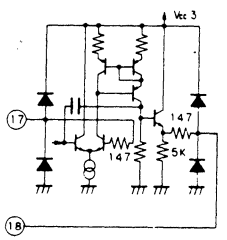
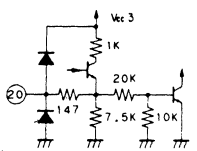
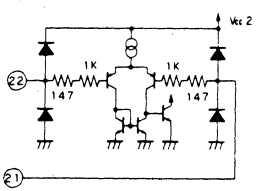
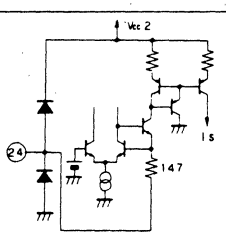


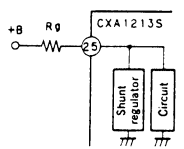
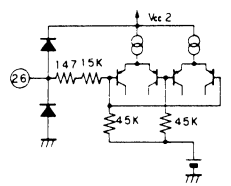
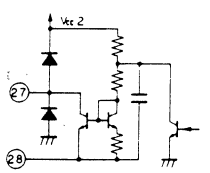
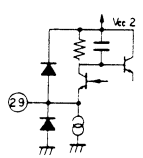
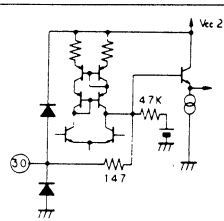
Pin Description

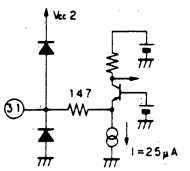
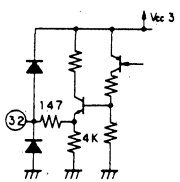
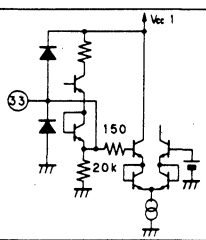
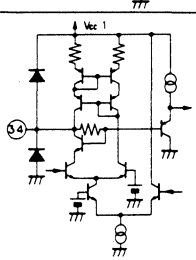
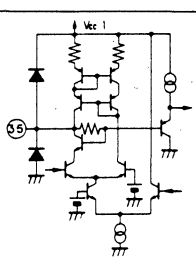
No.	Symbol	Voltage	Equivalent circuit	Description
1	C_{IN}	2.5V		Chroma input pin. Input signal after passing chroma B.P.F via capacitor.
2	ACC	Approx. 5.5V (At Typ. input)		External capacitance pin for ACC control. This pin voltage is to be ACC voltage.
3	C_{OUT}	$\overline{\text{SECAM}}$: 5.85V SECAM : 0V		ACC and chroma output pin after passing color control circuit. Pin voltage varies by SECAM/$\overline{\text{SECAM}}$. At $\overline{\text{SECAM}}$: $5.85V_{DC}$ At SECAM: $0V_{DC}$
4	PHASE	4.5V		Phase control voltage input pin for PAL. this pin is also applicable to forced killer input. killer output and f_{SC} free run adjustment mode. V_{DD} : Forced fsc free run adjustment 2 to 8V: Phase control GND : Forced killer input or killer output
5	U	—		U signal input pin after separating C_{OUT} signal at Pin 3 to U and V by using 1H Delay Line.

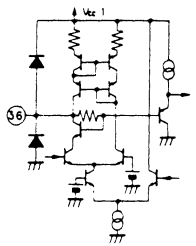
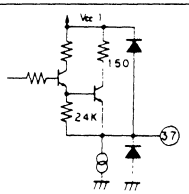
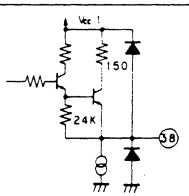
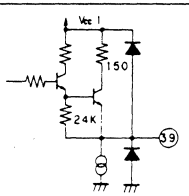
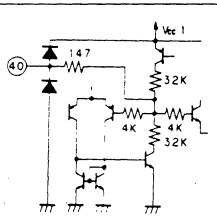
No.	Symbol	Voltage	Equivalent circuit	Description
6	V	—		V signal input pin after separating C_{OUT} signal at Pin 3 to U and V by using 1H Delay Line.
7	APC	6.7V		Lag lead filter pin for APC
8	X4			4.43MHz crystal pin for chroma VCO
9	3/4	At 3.58MHz output: 5.5V AT 4.43MHz output: GND		Discrimination output pin of VCO oscillation frequency. High level(5.5V) at oscillation frequency 3.58MHz, Low level at oscillation frequency 4.43MHz. Also input pin applicable: Forced 3.58MHz at mode H and 4.43MHz at mode L. Repeats H and L every 5 Vertical section at killer mode.
10	×3			3.58MHz crystal pin for chroma VCO.

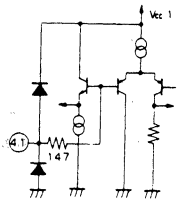
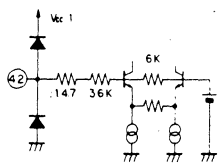
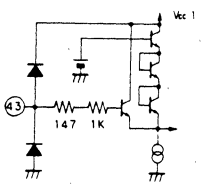
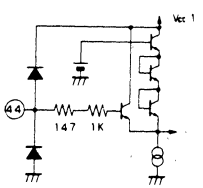
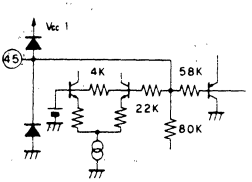
No.	Symbol	Voltage	Equivalent circuit	Description
11	S/$\overline{S}$	—		SECAM/$\overline{SECAM}$ input pin. Input high voltage over 2.7V at SECAM and low voltage under 0.3V at $\overline{SECAM}$.
12	N/P	—		NTSC/PAL input pin. Input low voltage under 0.3V at PAL and high voltage over 3.0V at NTSC.
13	60/50	At 50Hz: 0V At 60Hz: 4V		Discrimination output pin of vertical frequencies 50Hz and 60Hz. Also input pin applicable: Forced 60Hz mode at V_{CC}, Forced 50Hz mode at GND.
14	V_{IN}			Input pin for vertical sync separation. Slice level is decided by internal constant current of 40μA and protection resistance R_P and external resistance. Video signal is input at 2Vp-p.
15	VPH	3.35V		Pin to detect slice level to take out V.sync peak of sync separation output is detected at this pin. Connect Capacitor or Capacitor and Resistance between GNDs for external fixing.

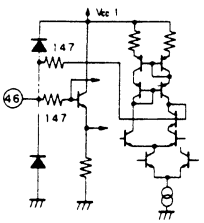
No.	Symbol	Voltage	Equivalent circuit	Description
16	VRAMP			Generates saw tooth wave for vertical deflection. Use the external capacitance which holds a stable temperature characteristics.
17	VNF	—		Feedback pin for vertical deflection. This is compared to saw tooth wave generated at Pin 16 with comparator and obtains almost the same waveform as internal saw tooth wave.
18	VD			Pin which outputs the difference of comparison between feedback waveform at Pin 17 and internal saw tooth wave.
19	V_{CC3}	9V		Power supply pin for vertical drive circuit. This supplies a stable 9V voltage.
20	BG			Burst gate pulse is output. Artificial H.sync is supplied instead of H.sync when AFC is not locked like at no signal. and it outputs approx. 4μs width pulse.
21	REF	—		Pins 21 and 22 are the pins to detect over voltage and to make it hold down. This supplies reference voltage to Pin 21 and high voltage detection output to Pin 22.
22	HV	—		
23	GND2	0V		GND pin for Jungle.
24	IS	2.1V		Pin to generate the reference current to be used at internal IC. Use the external resistance at 27kΩ which holds a stable temperature characteristics since the reference current is 80μA.

No.	Symbol	Voltage	Equivalent circuit	Description
25	V_{CC2}	9V		Power supply pin for horizontal drive circuit. Shunt regulator provided inside and it regulates to 9V. Since the current flowed into is approx. 15mA.the Rg value is obtained by the following formula when +B is +115V. $Rg=\frac{(115-9)V}{15mA}=7.07\rightarrow 6.8k\Omega$
26	HP	4.3V		FBP input pin and inputs it via capacitor.
27	HD			Horizontal drive output pin and open collector output. Drive pulse width is 24μs constant.
28	GND3	0V		Horizontal drive GND pin.
29	VCO			Connect ceramic oscillator for $32f_H$ VCO and dumping resistance. CSB500F2 for ceramic oscillator and 470Ω for dumping resistance are recommended.
30	AFC	5.2V		Pin that connects AFC loop filter.

No.	Symbol	Voltage	Equivalent circuit	Description
31	H_{IN}	2.3V		Input pin for H.sync separator. The form of circuit is the same as V.sync separator, however, set the slice level lower and time constant shorter than V.sync Separator when H. sync separator.
32	S_{sync}			Outputs sync pulled out in H.sync Separator circuit.
33	C BLK			C BLK output pin and BLK signal input pin. BLK input is ON : over 2.5V at H. OFF : under 0.3V at L Input in emitter follower circuit at input pin.
34	B CLP	6.2V		External Capacitor pin for B-Y signal color clamp. Also B-Y signal input pin of SECAM.
35	R CLP	6.2V		External Capacitor pin for R-Y signal color clamp. Also R-Y signal input pin of SECAM.

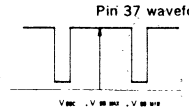
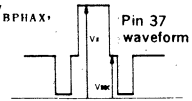
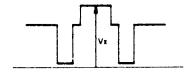
No.	Symbol	Voltage	Equivalent circuit	Description
36	G CLP	6.2V		External Capacitor pin for G-Y signal color clamp.
37	B_{OUT}			B signal output pin.
38	G_{OUT}			G signal output pin.
39	R_{OUT}			R signal output pin.
40	D. PIC	4V		External Resistance and Capacitor pin for black peak hold of New Dynamic Picture. Connect this pin to GND at 10kΩ when you want New Dynamic Picture OFF.

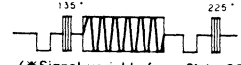
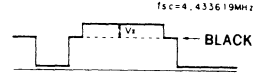
No.	Symbol	Voltage	Equivalent circuit	Description
41	BRT	—		Bright control voltage input pin. It is applicable for interface to auto white balance IC when BRT pin is to be V_{CC}.
42	HUE	4.5V		HUE control voltage input pin for NTSC.
43	COL	—		Color control voltage input pin.
44	PIC	—		Picture control voltage input pin.
45	SHARP	3.2V		Sharpness control voltage input pin. The sharpness circuit in IC dose not go through when this pin is connected to V_{CC}.

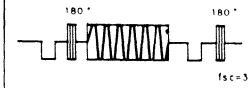
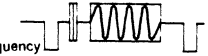
No.	Symbol	Voltage	Equivalent circuit	Description
46	V_{IN}	6.4V		Y signal input pin. 1Vp-p input.(Typ.)
47	V_{CC1}			V_{CC} pin (Y/C system)
48	GND1	0V		GND pin (Y/C system)

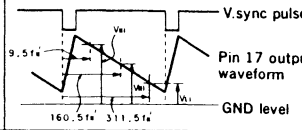
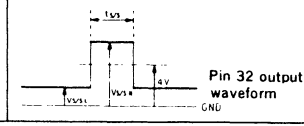
Electrical Characteristics

(Ta=25°C V_{CC}=9V See Electrical Characteristics Test Circuit)

No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
1	Current consumption	IV_{CC1}	a	a	a	a	a	a	a			20	9	5	3	0	SIG1	A1	Test current consumption at A1	24	39	57	mA
2	BRT Center black level DC (B)	V_{BBC}								ON									Input SIG2 to Input A. Test DC at Pin 37	1.6	1.8	2.0	
3	BRT MAX black level DC (B)	V_{BBMAX}		b														Pin 37	Pin 37 waveform 	3.4	3.6	3.8	V
4	BRT MIN black level DC (B)	V_{BBMIN}		c																0	0.45	0.75	
5	PIC Center (B)	V_{BPC}		a															Input SIG3 to Input A. Test DC value at Pin 37 on 3 SW conditions. The formula V_X-V_{BBC} is applied for the Specifications V_{BPC}, V_{BPHAX}, and V_{BPMIN}. Pin 37 waveform 	1.8	21	2.3	
6	PIC MAX (B)	V_{BPMAX}					b											Pin 37		2.55	2.85	3.1	V
7	PIC MIN (B)	V_{BPMIN}					c													0.25	0.5	0.75	
8	COLOR CONTROL Center	V_{CCBO}					a				ON								Input SIG4 to Input B. Test DC value at Pin 37 on 3SW conditions. The formula V_X-V_{BBC} is applied for the specifications V_{CCBO}, V_{CXBO}, and V_{CNBO}. 	0.6	0.9	1.2	V
9	MAX	V_{CXBO}				b	d											Pin 37		1.4	2.0	2.6	
10	MIN	V_{CNBO}				c	d													0	20	100	mV

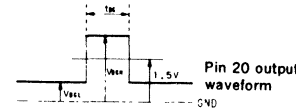
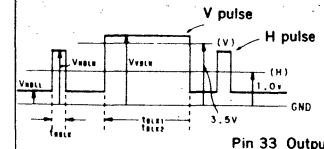
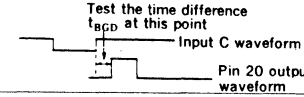
No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
11	Detection axis at PAL (B axis)	ϕ_{BP}				a	a											Pin 37 Pin 38 Pin 39	Input the signal as shown in Diagram 1 to Input B. R,G,and B outputs V_x are taken as V_R,V_G,and V_B respectively. At this time vary input signal from 0° to 360° and test maximum value V_{RMAX}, V_{GMAX},and V_{BMAX} of V_R,V_G,and V_B. Phase angles of each output at maximum value are taken as ϕ_{BP}',ϕ_{RP}',and ϕ_{GP}' respectively.(Get maximum value at each output.) At this time the following formulas are applied. $\Phi_{BP}=\phi_{BP}'$, $\Phi_{RP}=\phi_{RP}'-\phi_{BP}'$, $\Phi_{GP}=\phi_{GP}'-\phi_{BP}'$ And also, $(R/B)P=V_{RMAX}/V_{BMAX}$, $(G/B)P=V_{GMAX}/V_{BMAX}$.  (*Signal variable form 0° to 360° to phase of burst signal.) Diagram 1 Input signal  Diagram 2 RGB each output signal	−10	4	17	deg
12	Detection axis at PAL (R axis)	ϕ_{RP}																		82	90	98	
13	Detection axis at PAL (G axis)	ϕ_{GP}																		228	235	242	
14	Gain ratio (R/B)	(R/B)P																		0.43	0.5	0.57	
15	Gain ratio (G/B)	(G/B)P																		0.24	0.28	0.33	
16	KILLER POINT	D_{KILL}	e															Pin 37	Attennate SIG4 less then 300mVp-p and test amplitude of SIG4 when color killer operates. the following formula is applied for D_{KILL} when the value the is taken as V_x. $20 \log \frac{V_x}{300}$			−28	dB

No	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
17	4.43 f_O	ΔF_P	d	↓	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	Pin 37	Since APC circuit does not operate when Pin 4 is connected to 9V, the carrier frequency of SIG4 is varied and the frequency FP when the demodulation waveform occurs at Pin 37 is to be free run frequency. Then formula $\Delta F_P = F_P - 4433619Hz$ applies.	−220	0	210	Hz
18	APC pull-in (+)	ΔF_{CPU}	e	↓	↓	↓	↓	↓	↓	↓	ON	↓	↓	↓	↓	↓	↓	↓	The APC circuit operates when Pin 4 is opened and vary the subcarrier frequency as the killer circuit is operating.	240	420		
19	APC pull-in (−)	ΔF_{CDO}	e	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	The frequency when demodulation waveform occurs at Pin37 is to be pull-in range frequency. Then the following formulas are applied. $\Delta F_{CUP} = (f_x - F_P)$ (when f_x is $f_x > F_P$) $\Delta F_{CDO} = (f_x - F_P)$ (when f_x is $f_x < F_P$)		−870	−550	
20	Detection axis at NTSC (B axis)	Φ_{BN}	a	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	SIG5	Pin 37 Pin 38 Pin 39	The contents of test are the same as the Items 10 to 15, however, the signal input to Input B is as diagram below.  (*Signal variable from 0° to 360° to phase of burst signal.)	0	11	20	deg
21	Detection axis at NTSC (R axis)	Φ_{RN}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	93	99	105	↓
22	Detection axis at NTSC (G axis)	Φ_{GN}	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	234	240	246	↓
23	Gain ratio (G/B)	(R/B) N	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0.72	0.77	0.84	
24	Gain ratio (G/B)	(G/B) N	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0.26	0.3	0.34	
25	HUE characteristics 1	Φ_{BNMAX}	a	a	b	a	a	a	a		ON	20	9.0	5.0	3.0	0	↓	Pin 37 Pin 38 Pin 39	The contents of test are the same as the Items 10 to 15. Input signal is shown in the right diagram.  (Sub carrier frequency is to be free run frequency F_N.)		−18.5	−8	deg
26	HUE characteristics 2	Φ_{BNMIN}	↓	↓	c	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	18	30		↓

No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
27	3.58 f_O	ΔF_N	d		a														The contents of test are the same as the same as Items 17 to 19. $\Delta F_N = F_N - 3579545HZ$ F_N : Free run frequency $\Delta F_{CUP1} = f_x - F_N$ Hz (When fx is $fx > F_N$) $\Delta F_{DO1} = f_x - F_N$ Hz (when fx is $fx < F_N$)	−180	30	230	Hz
28	APC pull-in (+)	ΔF_{CPU1}	e								ON									210	410		
29	APC pull-in (−)	ΔF_{DO1}	e																		−1000	−600	
30	Horizontal power supply voltage	V_{CH}	a														SIG1	Pin 25	Test voltage at Pin 25 when current 15mA is flowed into Pin 25.	8.6	9.0	9.4	V
31	Vertical power supply inflow current	I_{CV}																A_2	Test the current flows into Pin 19	9.5	13.7	18	mA
32	Vertical triangle level (H) 1	V_{H1}																Pin 17	Test the voltages V_{H1}, V_{M1}, and V_{L1} at Pin 17 after 9.5fH', 160,5fH', and 311.5fH' from V_{SYNC} pulse rising. 	3.75	4.00	4.25	V
33	Level (M) 1	V_{M1}																		2.55	2.90	3.20	
34	Level (L) 1	V_{L1}																		1.35	1.80	2.40	
35	S/S output level (H)	$V_{S/SH}$																Pin 32	Test each level, $V_{S/SH}$ and $V_{S/SL}$, and pulse width $t_{S/S}$ from GND of Pin 32 output. 	7.5	7.85	8.2	V
36	S/S output level (L)	$V_{S/SL}$																		0	0.02	0.1	
37	S/S output pulse width	$t_{S/S}$																		4.4	4.8	5.2	μs

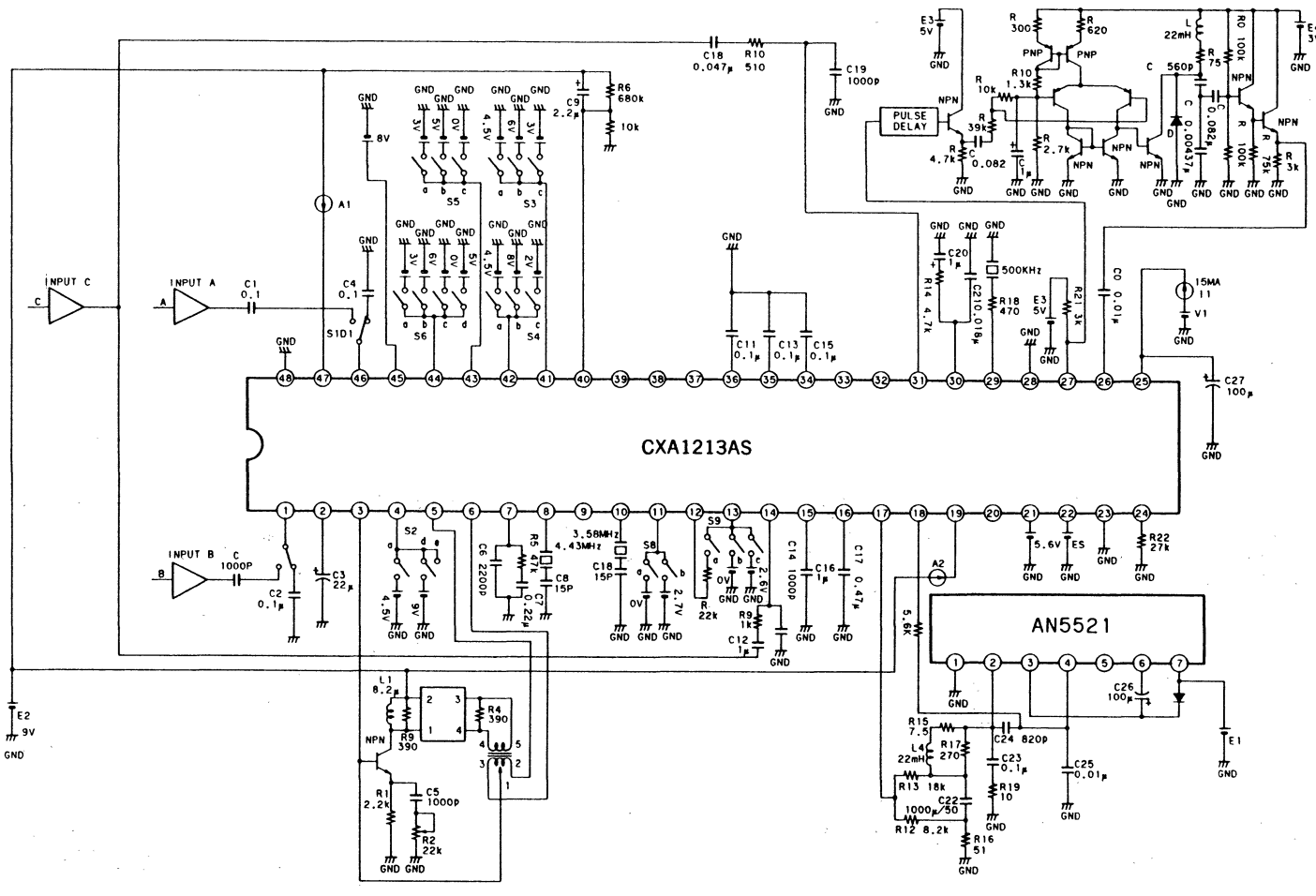
SONY

CXA1213AS

No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
38	BG OUT level (H)	V_{BGH}																Pin 20	Test each level, V_{BGL}, V_{BGH}, and pulse width t_{BG1} from GND of Pin 20 output. 	2.7	3.3	4.1	V
39	BG OUT level (L)	V_{BGL}																		0	0.01	0.1	
40	BG OUT pulse width	t_{BG1}																		2.9	3.4	3.9	μs
41	HBLK level (H)	V_{HBLH}																		1.8	2.2	2.6	V
42	HBLK level (L)	V_{HBLL}																		0	0.05	0.1	
43	H_{BLK} pulse width	t_{HBLK}																		10.8	11.7	12.5	μs
44	V_{BLK} level (H)	V_{VBLH}																	Test each level from GND of Pin33 output waveform and pulse width. Input SIG1 or SIG5 to Input C when t_{BLK1} and t_{BLK2} are tested.	4.2	4.8	5.4	V
45	V_{BLK} pulse width 1	t_{VBLK1}																		1.70	1.76	1.80	ms
46	V_{BLK} pulse width 2	t_{VBLK2}															SIG5			1.40	1.44	1.50	
47	BG OUT phase	t_{BGD}															SIG1		Pin 20 output waveform that tests the time difference t_{BGD} at this point. 	0.4	0.7	1.1	μs
48	HOLD DOWN operating voltage	V_{HOLD1}														※			※ Raise the voltage of E5 from 5.6V subsequently and test offset voltage from 5.6V of E5 when HD pulse of Pin 27 stops.	0	45	60	mV

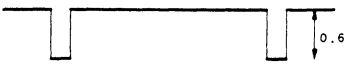
No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
49	Horizontal pull-in range 1	F_{H1}	a	a	a	a	a	a	a			20	9.0	5	3	0	SIG8	Pin 37 Input C	Confirm the output waveform Pin 37 agrees with f_H=16.075kHz and f_H=15.175kHz of SIG8 and SIG9 which are input to Input C. This range is to be pull-in range.			16.075	kHz
50	Horizontal pull-in range 2	F_{H2}															SIG9			15.175			
51	Vertical pull-in range 1	F_{V1}						b									SIG1	Pin 37 Input C	Pull-in frequency range which varies V frequency and synchronizes from asynchronism. ※ However, let f_H=15.625kHz. (Compulsion 50Hz mode)	42.1	50	72.6	Hz
52	Vertical pull-in range 2	F_{V2}						c											Pull-in frequency range which varies V frequency and synchronizes from asynchronism. ※ However, let f_H=15.625kHz (Compulsion 60Hz mode)	48.6	60	72.6	

Electrical Characteristics Test Circuit



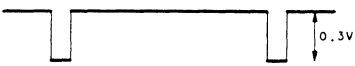
Input Signal

SIG1



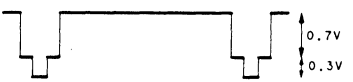
PAL V_{SYNC} available
f_H=15.625kHz

SIG2



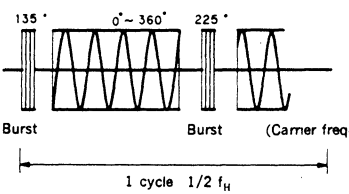
PAL V_{SYNC} available
f_H=15.625kHz

SIG3



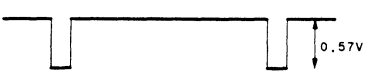
PAL V_{SYNC} available
f_H=15.625kHz

SIG4



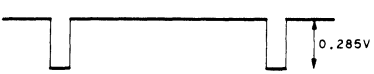
PAL V_{SYNC} available
f_H=15.625kHz
(Carrier frequency f=4.433619MHz, phase variation applicable)

SIG5



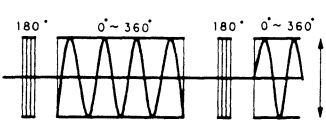
NTSC V_{sync} available
f_H=15.734kHz

SIG6



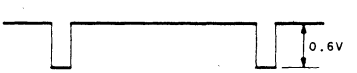
NTSC V_{sync} available
f_H=15.734kHz

SIG7



NTSC V_{sync} available
f_H=15.734kHz
(Carrier frequency f=3.579545MHz, phase variation applicable)

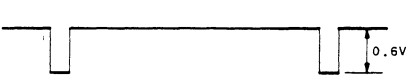
SIG8



f_H'=(15.625+0.45) kHz
(V_{sync} available)

f_H'=(15.625−0.45) kHz
(V_{sync} available)

SIG9



Operation Description

(1) Luminance signal system

(i) SHP circuit

The luminance signal that is input from Pin 46 is emphasized around 3.0 MHz of luminance signal by SHP circuit. Connect Pin 45 to V_{CC} so that SHP circuit gets OFF when it is not necessary.

(ii) BLK MUTE circuit

Connecting Pin 41 to V_{CC} replaces BLK section to black level and connection with auto white balance IC (CXA1024S) applicable.

(iii) Fast BLK circuit

Inputting the character signal etc. to CBLK pin makes the function that attenuates the character signal part of video signals available.

(iv) New Dynamic Picture circuit

The function to expand black operates in the signals under 50IRE of input signal. Connecting Pin 40 at around 10kΩ resistance makes the function cancelled.

(2) Chroma system

(i) ACC circuit

Detects the burst signal (that is demodulated by average level detection) by ACC DET and applies return to ACC amplifier according to the detection output to keep the demodulated burst level always stable.

(ii) APC circuit

The input chroma component from Pin 1 composes B-Y signal and R-Y signal by detecting to the external crystal at Pin 8 (3.58MHz) or Pin 10 (4.43MHz), which are output of VCO by APC circuit, after it is amplified via ACC and color amplifiers.

(iii) Matrix

Composes G-Y signal by mixing B-Y and R-Y signals. Then,outputs at R,G,and B orignal signal by these signals and the luminance signal Y.

(iv) ID correction

PAL system is sent after R-Y (V) component of the sygnal gets inverted every 1H. Due to this reason, the demodulation axis also needs to be inverted every 1H. The R-Y axis is inverted every 1H synchronizing with HP in this IC, however, the flip-flop corrects it if it is wrong according to R-Y burst detection output.

(v) SECAM system applicable (Combined with the CXA1214P)

The combination with the CXA1214P enables the SECAM signal demodulated. (See Application Circuit 2) Inputting the direct voltage of H level (over 2.5V) and R-Y and B-Y signals, which SECAM signal is demodulated to R CLP (Pin 35) and B CLP (Pin 34) via direct capacitor make the original signals R,G, and B output.

(3) Jungle system

The count down system is adopted. by the $32f_H$ ceramic oscillator.

Due to these reason, no adjustment of H and V free run frequency is realized and the number of pins and external parts get lesser.

The horizontal synchronization cicuit adopts double loops. The input, VCO frequency and phase are combined and the HD pulse is generated in the first loop and the phase with FBP of deflection is combined in the second loop.

The burst gate pulse is generated synchronizing with the input horizontal sync, however this generates a artifical pulse at no signal with a artifical horizontal sync from the horizontal count down circuit.

The vertical synchronization circuit varies the width of input prohibition gate according to input frequency and shortens the section that vertical sync passes throngh to improve the elimination capacity of the noises going into vertical sync. (See Diagram of (i) Vertical Synchronization Prohibition Gate)

At the same time, the elminated capacity of the noises are furthermore improved since the peak hold circuit is adopted at vertical sync separation circuit.

The auto discrimination circuit is built in when Switching 50 or 60Hz.

(i) Vertical synchronization prohibition gate

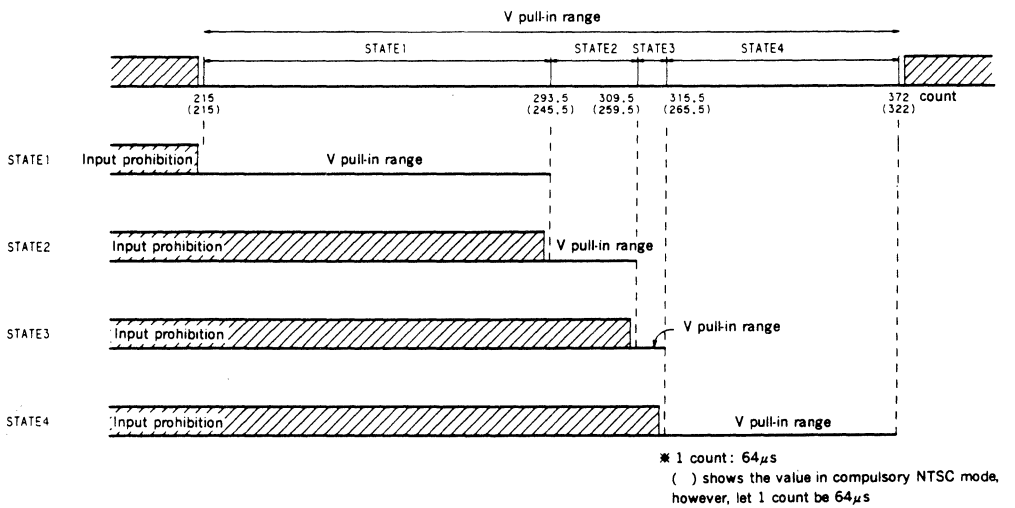
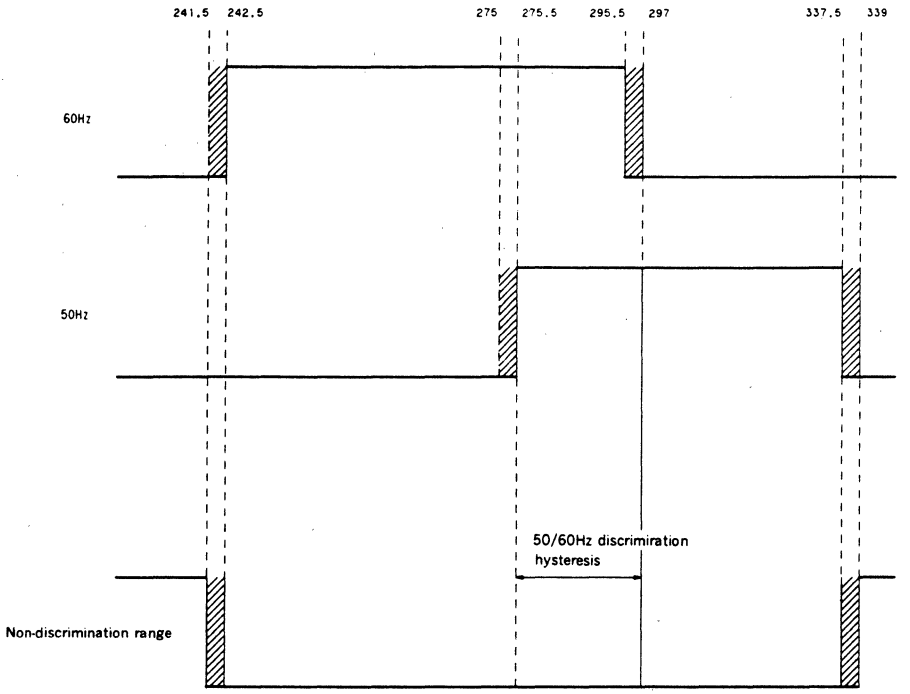


Diagram 1. Vertical pull-in range

This is synchronized in state 1 to 4 by vertical sync wavelength. The vertical pull-in range is composed as Diagram 1. Throngh this,the noise is eliminated as providing the input prohibition gate severely not to discriminate the non-continuous noise pulse besides vertical sync. (ex. VHS noise).

(ii) 50/60Hz Discrimination Operation



The count number is 64μs by a count ($=1/f_H$)

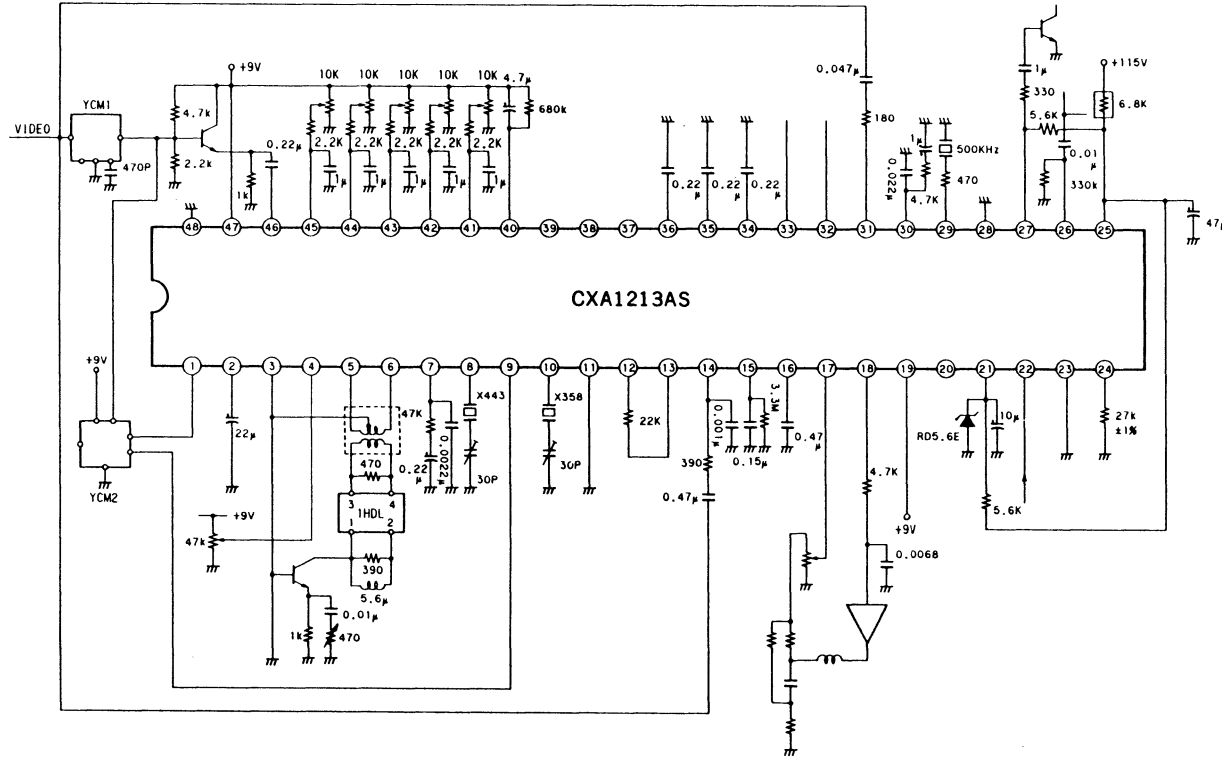
Diagram 2. 50/60Hz Discrimination Range

This IC automatically discriminates the discrimination of 50Hz and 60Hz from the input vertical sync. The 50Hz has priority when the power supply is on and discriminates as in Diagram 2 by vertical sync wavelength. The discrimination output pin is Pin 13 ,and outputs as 60Hz mode H and 50Hz mode L.

For example, this discriminates as 60Hz mode when the input signal is from 242.5 to 295.5 counts and 50Hz mode when the input signal is from 275.5 to 337.5 counts. And the hysteresis is provided between the count from 275.5 to 295.5. No discrimination occurs besides those so that the discrimination output of former state is held.

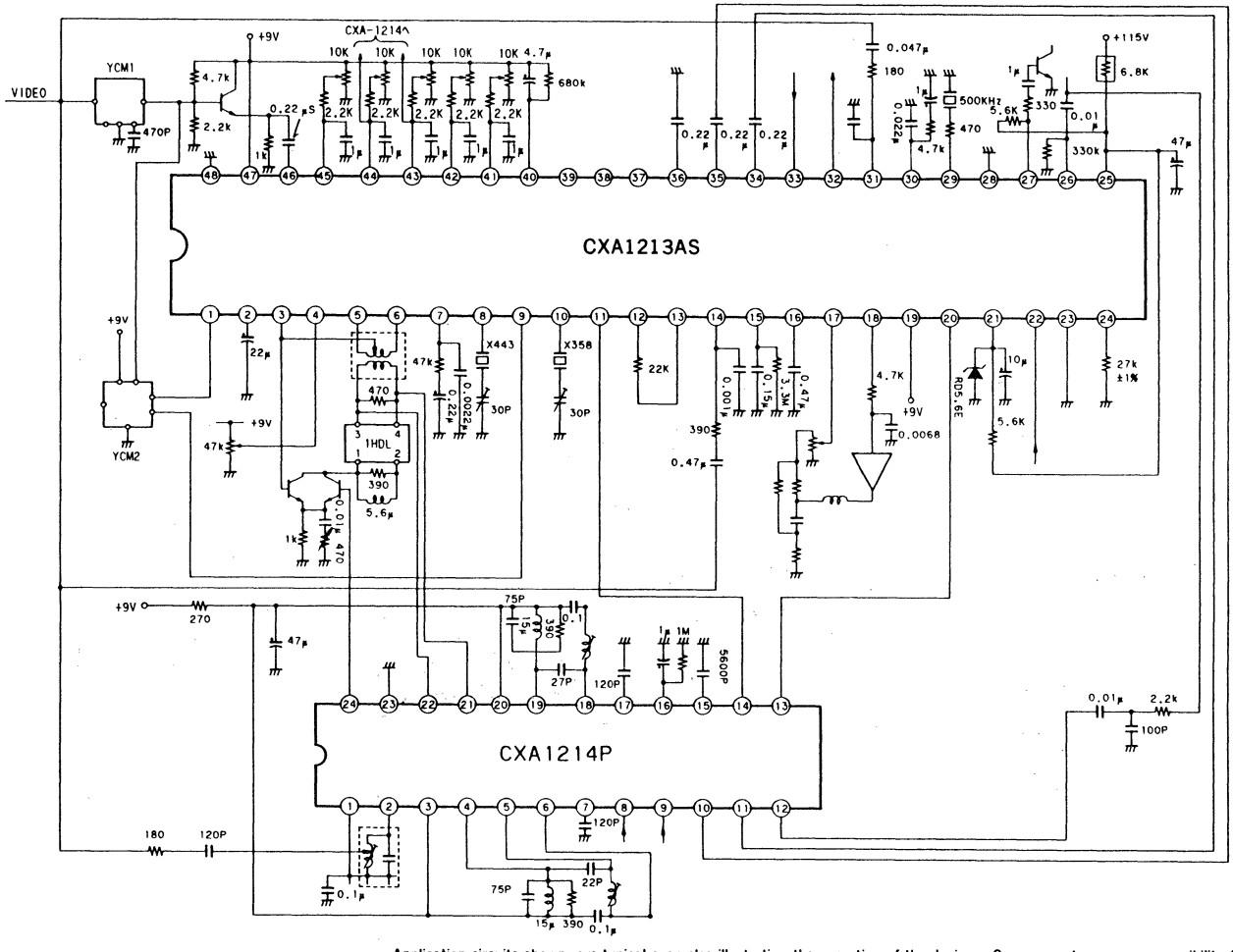
The mark ▨,which is a discrimination error occurs due to like an error of vertical sync separation circuit in this IC, is a state that discriminates as either 50Hz or 60Hz.

Application Circuit 1 PAL/3.58NTSC/4.43NTSC System



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 PAL/SECAM/3.58NTSC/4.43NTSC



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Bright Control Characteristics

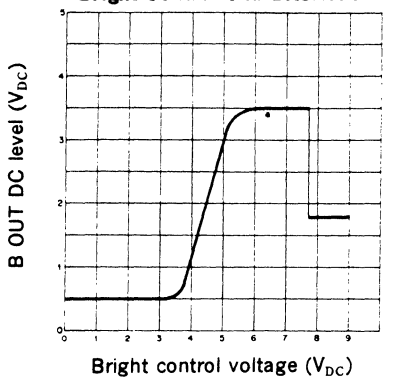


Fig. 1

Picture Control Characteristics

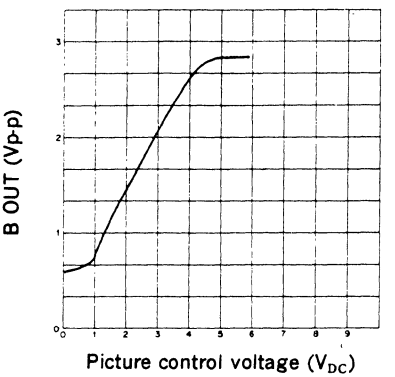


Fig. 2

New Dynamic Picture I/O Characteristics

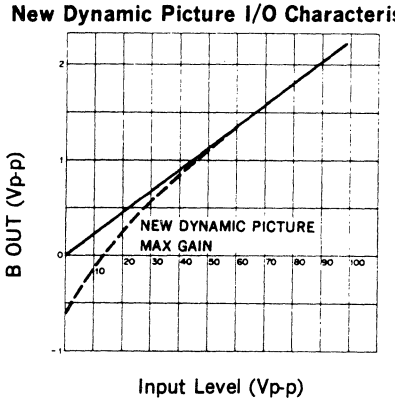


Fig. 3

Color Control Characteristics

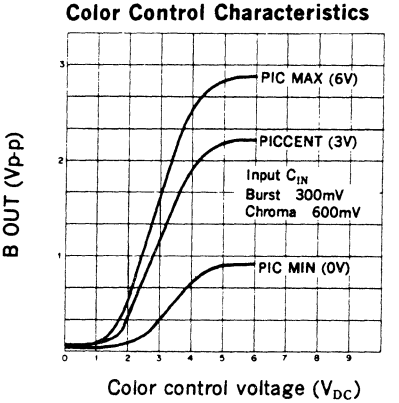


Fig. 4

ACC Characteristics

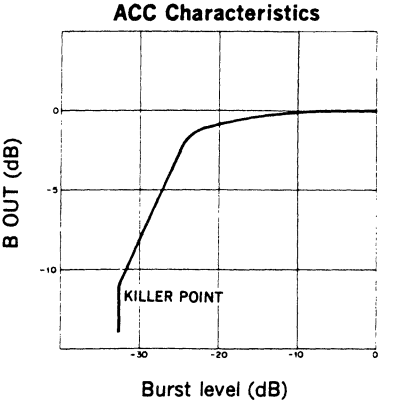


Fig. 5

Y. Signal Frequency Characteristics

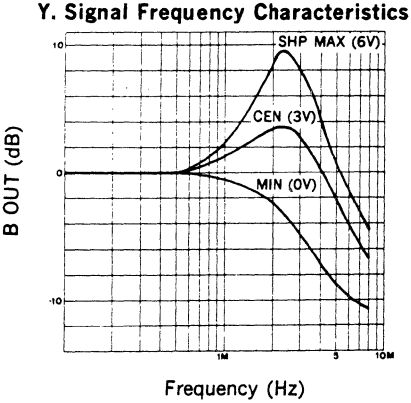
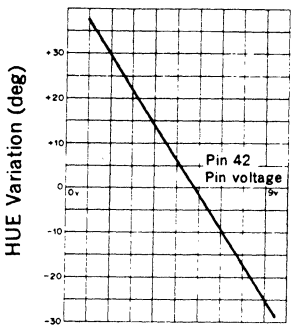


Fig. 6

HUE Control Characteristics



Pin voltage at pin 42

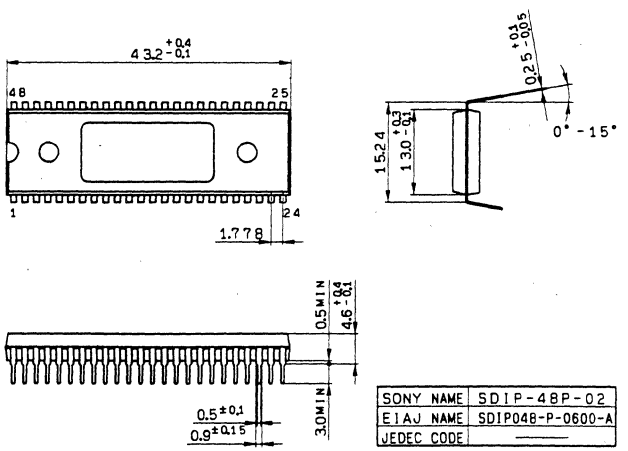
Fig. 7

Notes or Operation

(1) Recommend adjusting the free run frequency to 4.433619MHz and 3.579545MHz by using the trimmer capacitor.
(2) The HUE characteristics 1 and 2 are tested at HUE pin voltage 8V and 2V. The HUE center is about 6.0V.
(3) Adjust the detection axis of PAL mode B output to 0deg by contorolling Pin 4 (PHASE).
(4) Input the signal to Pin 33 in the emitter follower type when the high speed blanking function used.

Package Outline **Unit : mm**

48pin SDIP (Plastic) 600mil 5.1g



SONY® CXA1214P

SECAM Color Decoder

Description

The CXA1214P is a color signal processing IC for SECAM color television system. The IC has an ID determination circuit as well as the video processing circuits required for processing of color signals.

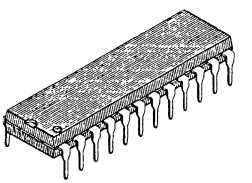
Features

- Combined use of the CXA1214P and CXA1213S makes it possible to configure a system compatible with all three systems, PAL, SECAM and NTSC.
- Has a self-contained automatic ID determination circuit.

Applications

- Color television
- SECAM color decoder

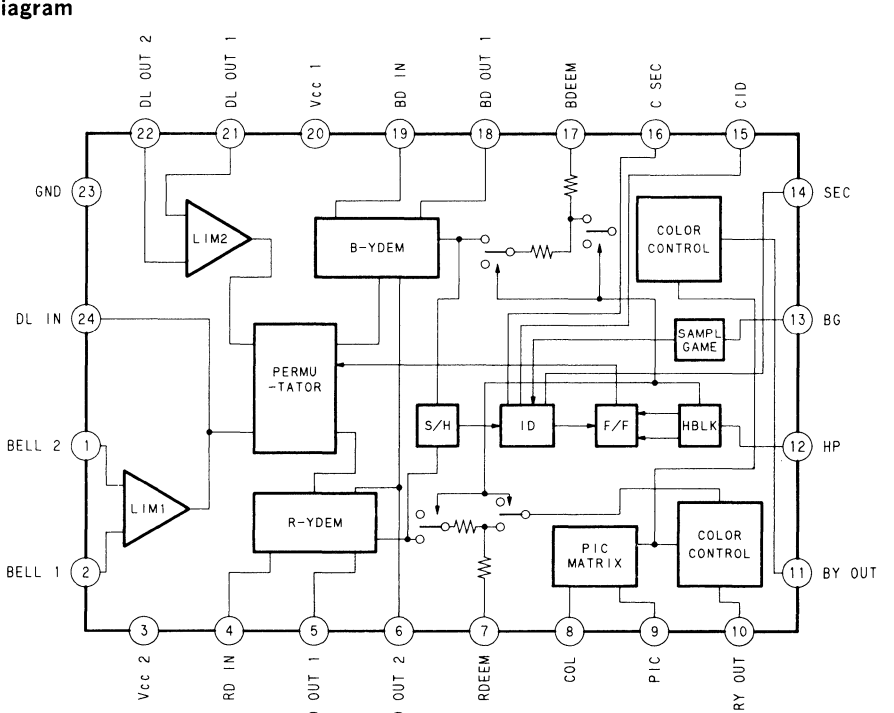
24pin DIP (Plastic)



Structure

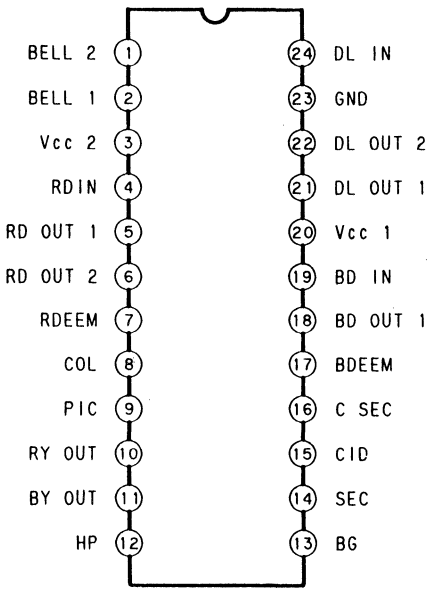
Bipolar silicon monolithic IC

Block Diagram



E89532-HP

Pin Configuration



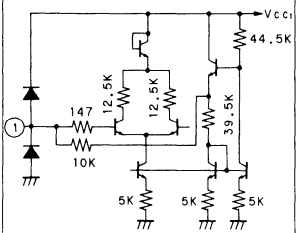
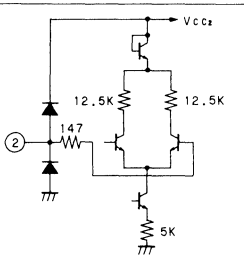
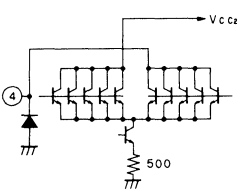
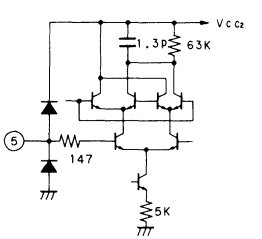
Operating Condition

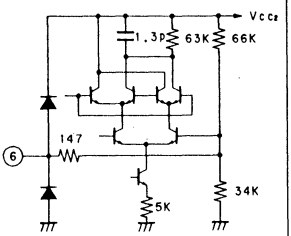
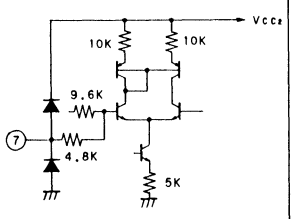
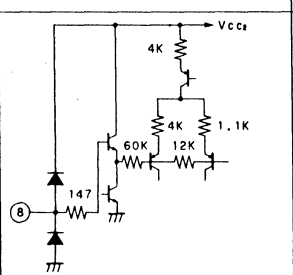
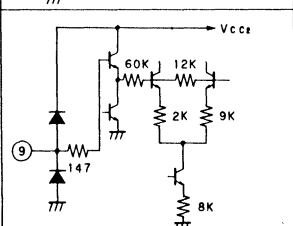
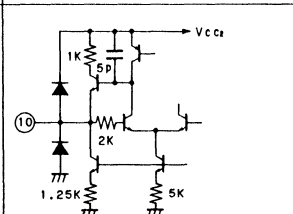
• Supply voltage	V_{CC}	8.5 to 9.5	V

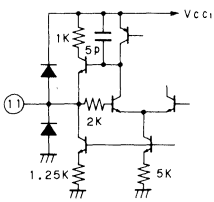
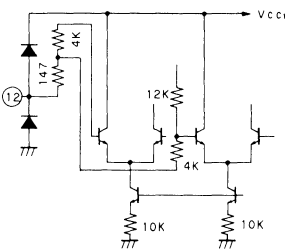
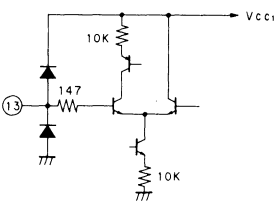
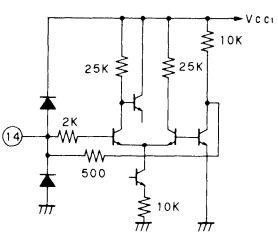
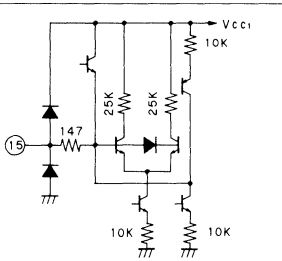
Absolute Maximum Ratings(Ta=25°C)

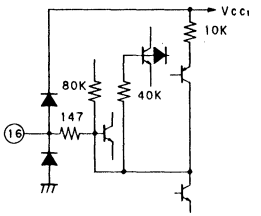
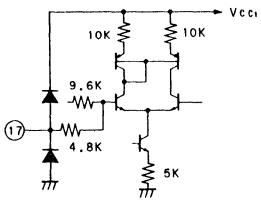
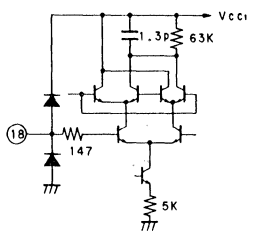
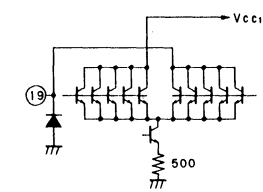
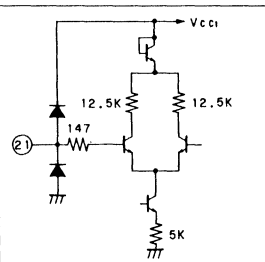
• Supply voltage	V_{CC1} V_{CC2}	7	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +125	°C
• Allowable power dissipation	P_D	1.3	W

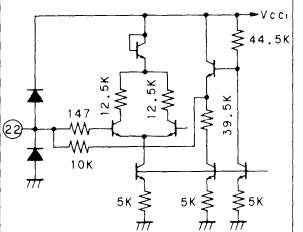
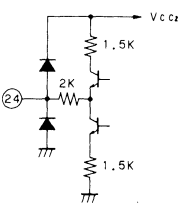
Pin Description

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
1	BELL2	2.5V		Chrominance signal bias pin.
2	BELL1	2.5V		SECAM Chrominance signal input pin.
3	V_{CC2}	5V		Stabilized power supply decoupling pin. Connected to Pin 20, it allows supply of current (15mA standard) from outside.
4	RDIN	4.9V		Use this pin to connect the R-Y discriminator.
5	RDOUT1	1.7V		The FM demodulator input pin.

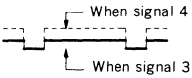
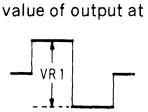
Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
6	RDOUT2	1.7V		FM demodulator bias pin.
7	RDEEM	2.5V		Use this pin to connect the de-emphasis capacitor.
8	COL	—		Color control pin.
9	PIC	—		Picture control pin.
10	RYOUT	2.5V		R-Y signal output pin.

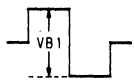
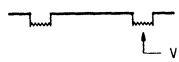
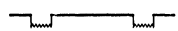
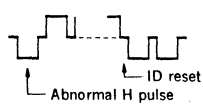
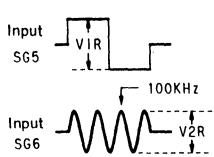
Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
11	BYOUT	2.5V		B-Y signal output pin.
12	HP	2.5V		Flyback pulse input pin. Input positive 3Vp-p flyback pulse via a capacitor.
13	BG	—		Burst gate pulse input pin.
14	SEC	—		SECAM/$\overline{\text{SECAM}}$ output pin. Forced grounding of this pin creates the forced $\overline{\text{SECAM}}$ mode.
15	CID	—		Use this pin to connect the ID sample hold capacitor.

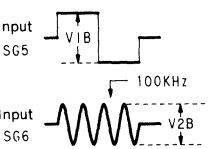
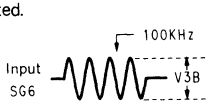
Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
16	CSEC	—		Time constant pin for identification of SECAM.
17	BDEEM	2.5V		Use this pin to connect the de-emphasis capacitor.
18	BDOUT1	1.7V		The FM demodulator input pin.
19	BDIN	4.9V		Use this pin to connect the B-Y discriminator.
20	V_{CC1}	5V		Connected to Pin 3, this pin allows supply of current (15mA Typ.) from outside.
21	DLOUT1	2.5V		Use this pin to input 1H delayed signal.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
22	DLOUT2	2.5V		Delay line bias pin.
23	GND	0V		GND pin.
24	DLIN	2.5V		Delay line bias pin.

Electrical Characteristics T_a=25°C, V_{CC}=9V, Refer to Electrical Chracteristics Test Circuit.

No.	Item	Symbol	SW condition	Bias condition	Condition	Min.	Typ.	Max.	Unit
1	Regulator voltage 1 V_{CC}=8	V_{CC1}	—	1	Voltage at Pin 3 tested.	4.65	5.0	5.35	V
2	Regulator voltage 2 V_{CC}=9V	V_{CC2}	—	2	Voltage at Pin 3 tested.	4.65	5.0	5.35	V
3	Regulator voltage difference 1	VD12	—	—	Difference between measurements of test No. 1 and 2.	—	—	30	mV
4	DEM difference R-Y	RDE	SW1 : OFF SW2 : OFF SW3 : OFF		Input signal : SG1, SG2 Difference in output DC level at Pin 10. 	−20	0	+20	mV
5	DEM difference B-Y	BDE	↓	↓	Input signal : SG1, SG2 Difference in output DC level at Pin 11.	−20	0	+20	mV
6	Output amplitude 1 R-Y	VR1	↓	↓	Input signal : SG3 p-p value of output at Pin 10 tested. 	0.73	0.899	1.14	Vp-p

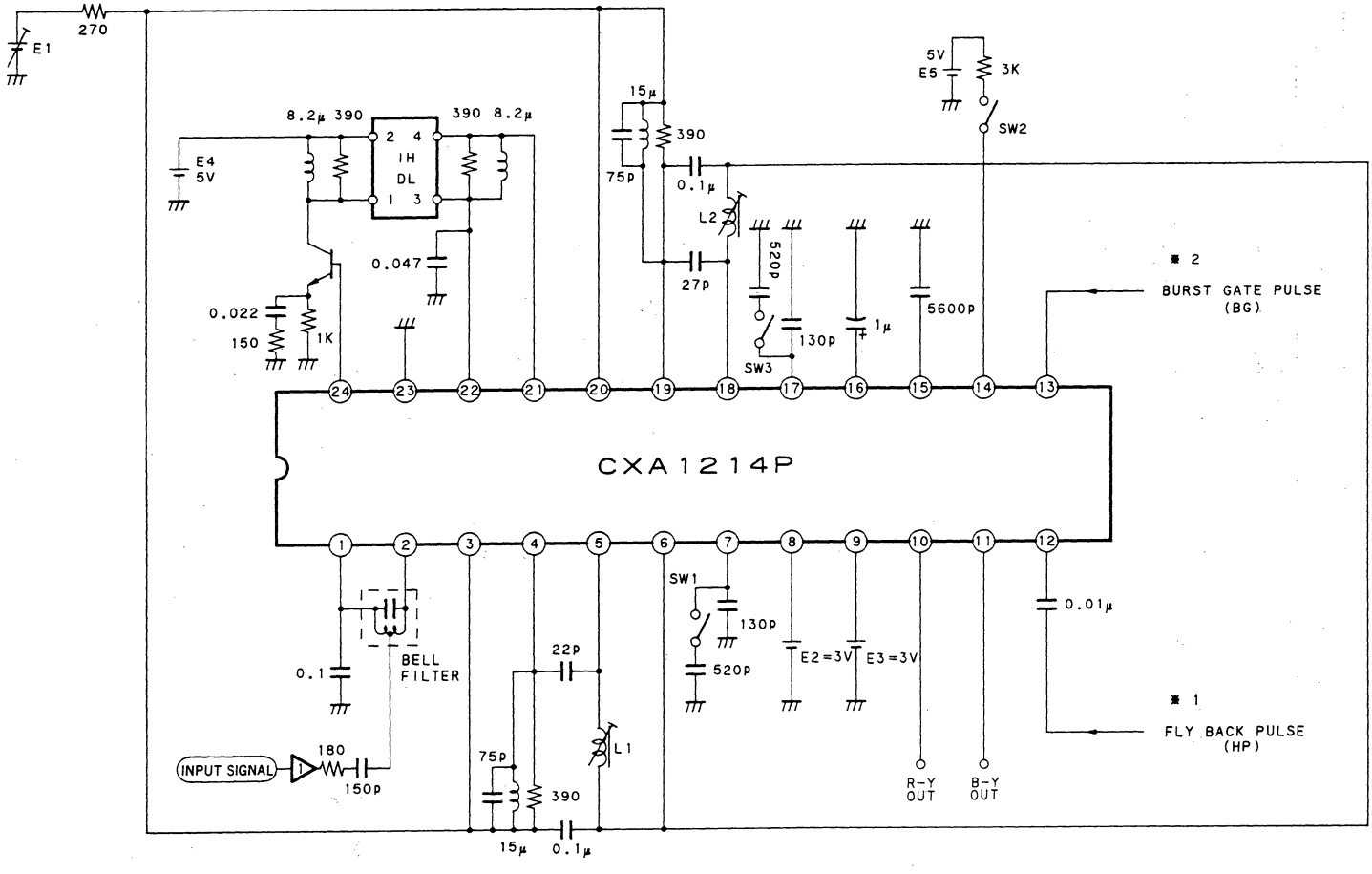
No.	Item	Symbol	SW condition	Bias condition	Condition	Min.	Typ.	Max.	Unit
7	Output amplitude 1 B-Y	VB1	↓	↓	Input signal : SG3 p-p value of output at Pin 11 tested. 	0.90	1.11	1.39	Vp-p
8	Output amplitude ratio R-Y/B-Y	VRB	—	—	Output amplitude ratio of above-mentioned Pins 6 and 7. $VRB=\frac{VR1}{VB1}$	0.75	0.813	0.87	
9	HBLK noise R-Y	VNR	↓	2	Input signal : SG1 Noise in BLK section of output at Pin 11 tested. 	—	—	10	mV_{rms}
10	HBLK noise B-Y	VNB	↓	↓	Input signal : SG1 Noise in BLK section of output at Pin 10 tested. 	—	—	10	mV_{rms}
11	ID reset R-Y	RID	↓	↓	Time from when abnormal pulse is forced into input signal (SG4HP) to when normal output is restored at Pin 11. 	0.15	0.303	0.43	mS_{ec}
12	ID reset B-Y	BID	↓	↓	Time from when abnormal pulse is forced into input signal (SG4HP) to when normal output is restored at Pin 10.	0.15	0.291	0.43	mS_{ec}
13	Deem characteristic R-Y 100kHz	DER2	SW1 : OFF SW2 : OFF SW3 : OFF	2	Input signal : SG5, SG6 Output level at Pin 11 tested.  $DER2=20\log\frac{V_2R}{V_1R}$ (dB)	−2.71	−1.71	−0.70	dB

No.	Item	Symbol	SW condition	Bias condition	Condition	Min.	Typ.	Max.	Unit
14	Deem characteristic R-Y 50kHz	DER3	SW1 : ON SW2 : OFF SW3 : ON	↓	Input signal: SG5, SG6 Difference in output level at Pin 11 tested.  $DER3=20\log\frac{V_3R}{V_1R}$ (dB)	−7.73	−6.73	−5.73	dB
15	Deem characteristic B-Y 100kHz	DEB2	SW1 : OFF SW2 : OFF SW3 : OFF	↓	Input signal: SG5, SG6 Difference in output level at Pin 10 tested.  $DEB2=20\log\frac{V_2B}{V_1B}$ (dB)	−3.19	−2.19	−1.19	dB
16	Deem characteristic B-Y 500kHz	DEB3	SW1 : ON SW2 : OFF SW3 : ON	↓	Input signal: SG5, SG6 Difference in output level at Pin 10 tested.  $DEB3=20\log\frac{V_3B}{V_1B}$ (dB)	−6.71	−5.71	−4.71	dB
17	Killer Point	KIL	SW1 : OFF SW2 : OFF SW3 : OFF	↓	Input signal: SG3 Input signal reduced to find the point where the Killer is caused to be ON. (Voltage at Pin 14···0.2V or less).	−65	−50	−35	dB
18	Killer drive	KILR	SW1 : OFF SW2 : OFF SW3 : OFF	↓	Input signal: SG3 Voltage at Pin 14 tested when input signal is reduced to 65dB.	—	—	1	V
19	Regulator voltage difference 2	VD23	—	3	Difference from testing 2 tested in voltage at Pin 3.	—	—	40	mV

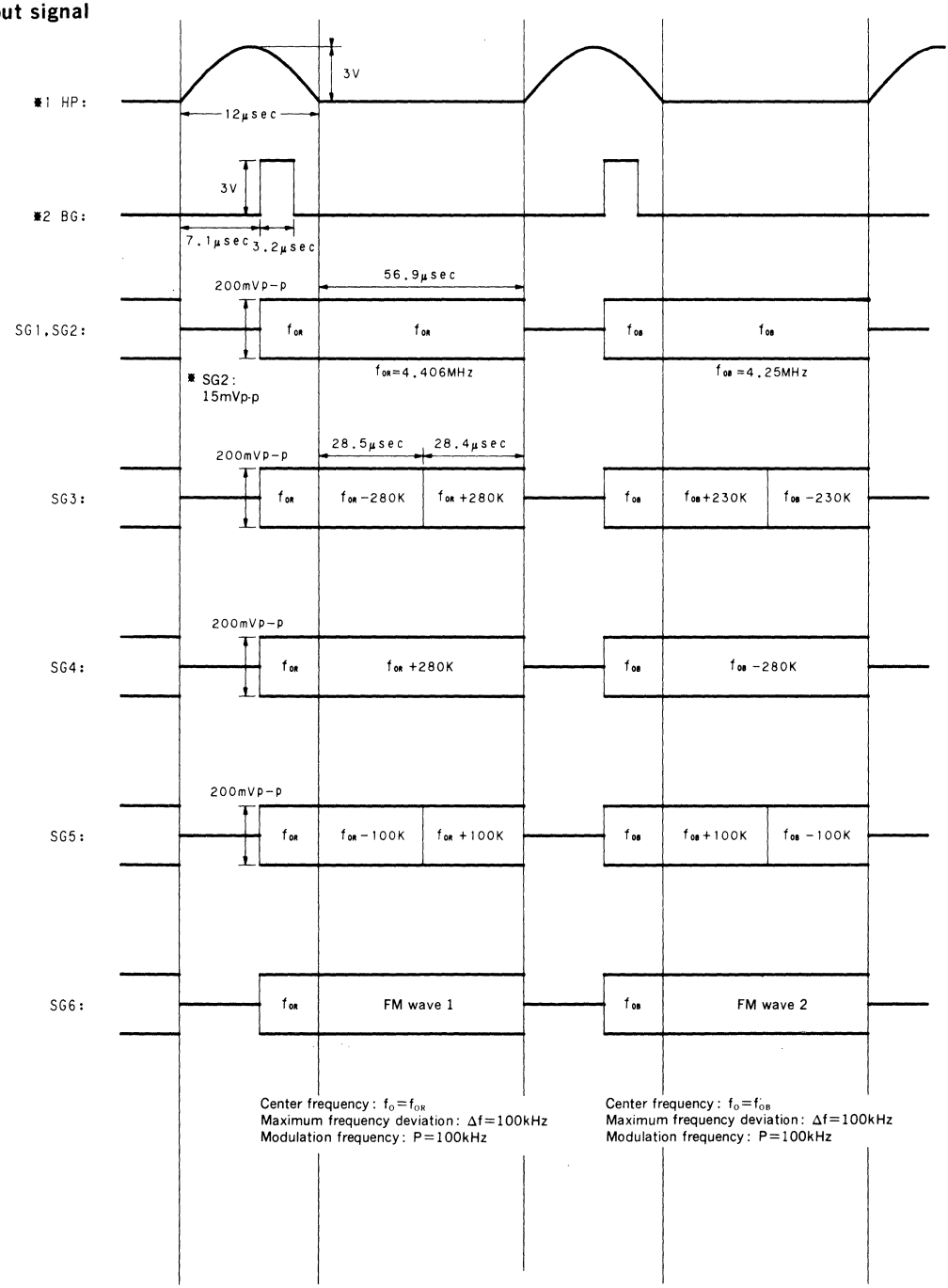
Bias Condition Table

Condition No. \ Power supply No.	E_1	E_2	E_3
1	8V	3V	3
2	9	3	3
3	10	3	3

Electrical Characteristics Test Circuit



Input signal



Operation

SECAM color signal is input from Pin 2 via the bell filter.

The signal is passed through the limiter from which it is directly routed to the permutator and is also output to Pin 24.

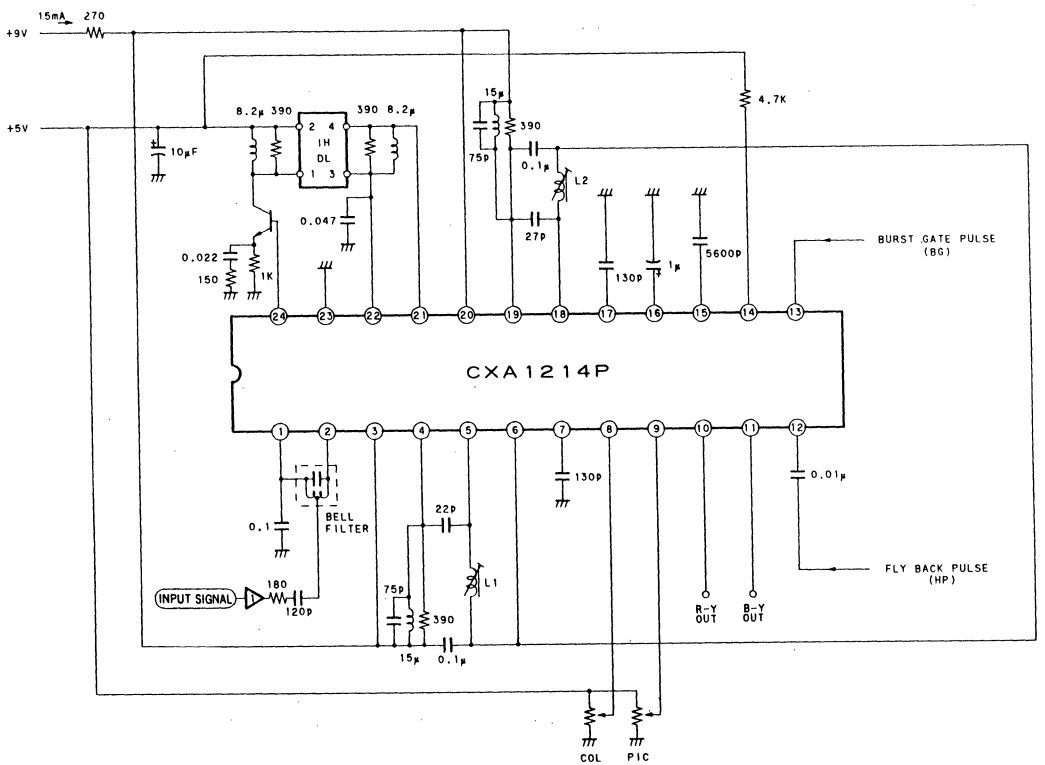
The signal output from Pin 24 passes through the 1H delay line and is re-input from Pin 21 and it is sent through the limiter to the permutator.

In response to a switching pulse from the determination system, the permutator sends either the signal directly input from the bell filter or the signal input via the 1H delay line to the R-Y or B-Y FM detector.

The color signals passed through the FM detectors are output through the respective de-emphasis circuits and color control circuits to Pins 10 (R-Y output) and 11 (B-Y output).

The determination system monitors the outputs from the FM detectors to check whether the permutator is correctly switching the signals, and provides controls to make sure that the permutator correctly switches the signals. When no SECAM signal is input, the forced killer is activated to block output of R-Y and B-Y signals. In addition, the output at Pin 14 is caused to be "Low".

Application Circuit



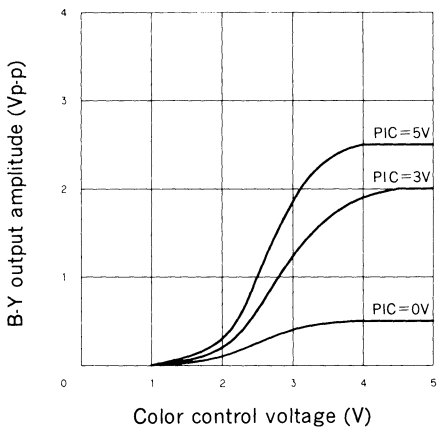
Adjustment procedure

Input SECAM color bar signal to Pin 2 via the bell filter. Adjust coil L1 so that the video section black level and BLK level will be in alignment in the output at Pin 10.

Similarly, adjust coil L2 so that the black level and BLK level will be in alignment in the output at Pin 11.

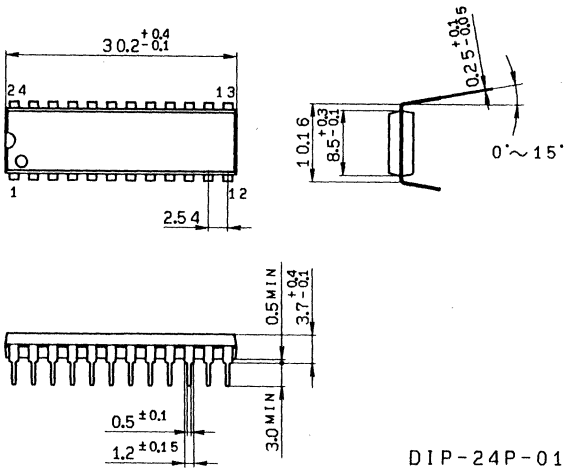
Example of characteristics

Color Control Characteristics (When color bar is input)



Package Outline **Unit : mm**

24pin DIP (Plastic) 400mil 2.0g



DIP-24P-01

SONY CXA1218S/CXA1228S

NTSC/PAL Decoder

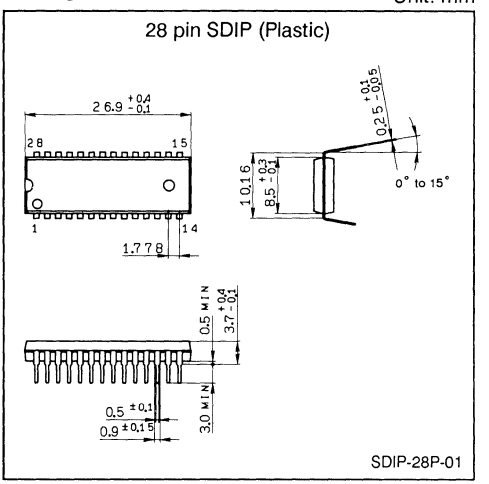
Description

CXA1218S and CXA1228S are decoder ICs used to convert composite video signals into color difference signals. They have signal outputs, such as composite sync, burst flag, subcarrier, and alternate signal outputs, necessary, for image processing. CXA1228S operates in both NTSC and PAL modes.

Ratio is R–Y : B–Y = 1.4 : 1.0 for CXA1218S
R–Y : B–Y = 1 : 1.27 for CXA1228S

Package Outline

Unit: mm



Features

- Single supply operation 5V
- Low power consumption (85 mW Typ.)
- Compatible with both NTSC and PAL modes
- Provides composite sync, burst flag, subcarrier, and line alternate signal output

Function

Synchronous separation, compostie sync output, burst flag output, ACC, ACK, APC, demodulator, DL amplifier, PAL ID, HUE control.

Structure

Bipolar silicon monolithic IC

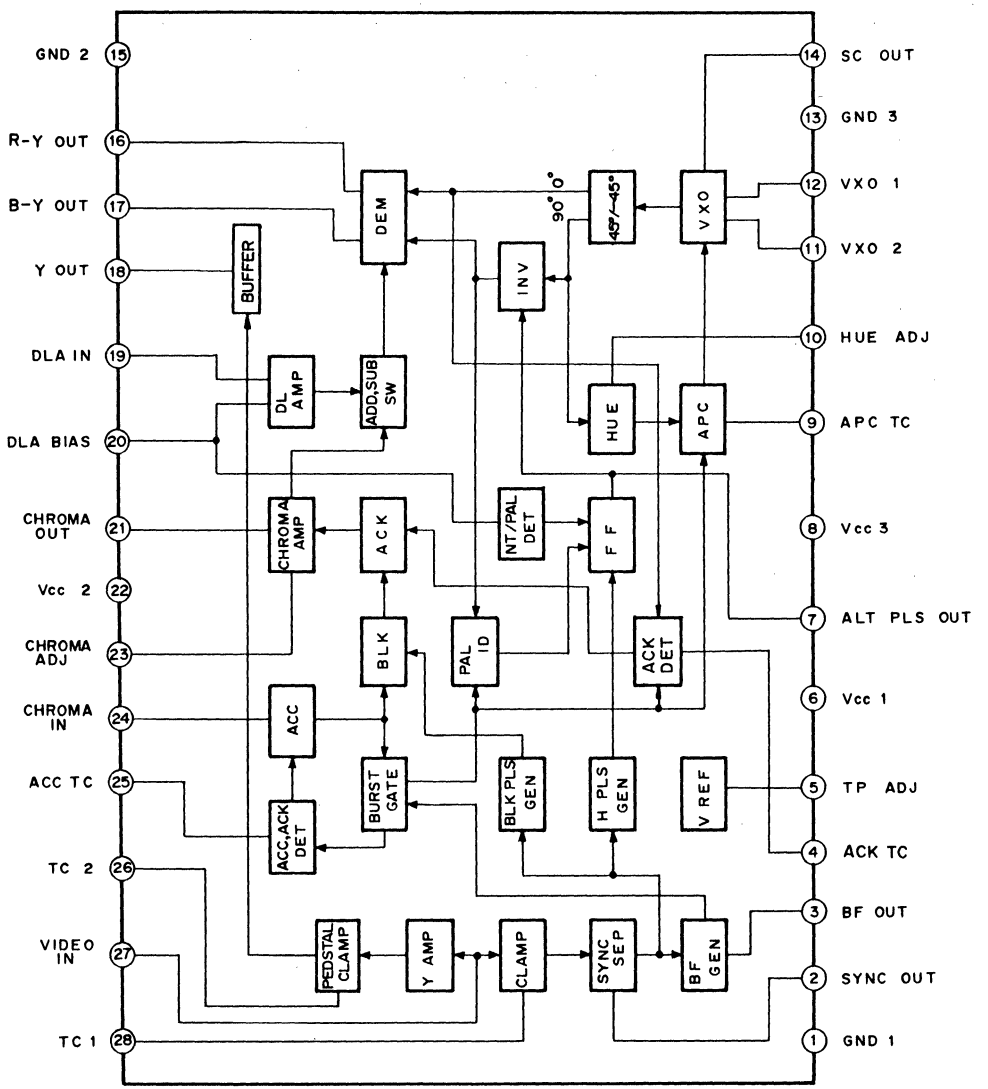
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc		10		V
• Operating temperature	Topr	−20	to	+75	°C
• Storage temperature	Tstg	−55	to	+150	°C
• Allowable power dissipation	PD		250		mW

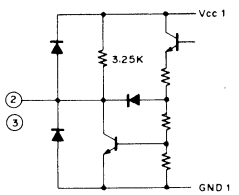
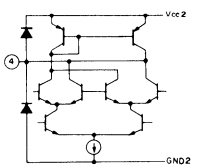
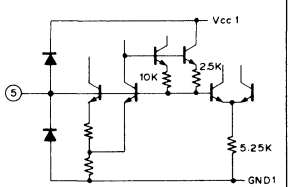
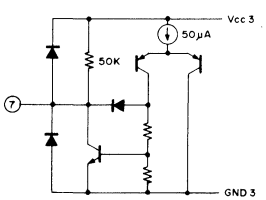
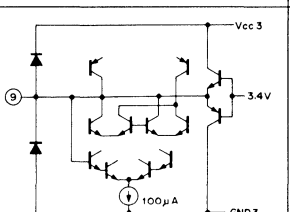
Recommended Operating Condition

• Supply voltage	Vcc	5	±	0.25	V

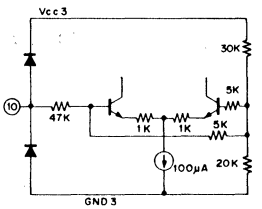
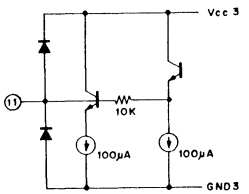
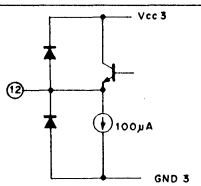
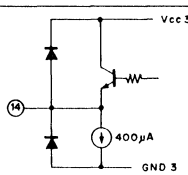
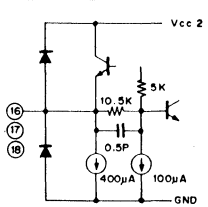
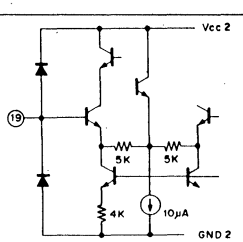
Block Diagram and Pin Configuration



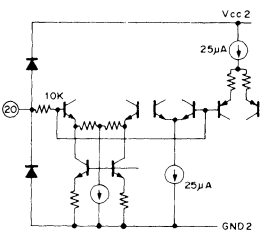
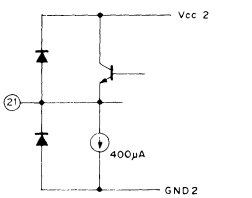
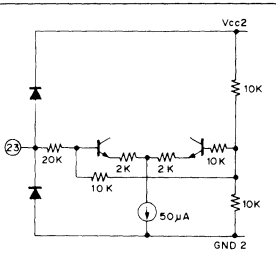
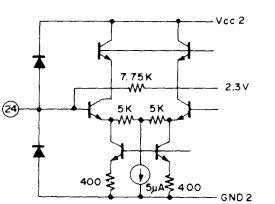
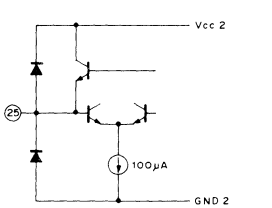
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	GND 1	0V		GND pin of Y AMP and SYNC SEP.
2	SYNC OUT	H; 2.4V Min. L; 0.4V Max.		Composite Sync output pin (TTL level)
3	BF OUT			Burst flag output pin (TTL level)
4	ACK TC	3.1V Typ.		ACK (Auto Color killer) time constant pin
5	TP ADJ	1.23V Typ.		Burst flag positional adjusting pin By changing the current from this pin burst flag position adjustment to tD (BF) = 5.6 μs can be performed.
6	Vcc 1	*5V		Supply pin of Y AMP and SYNC SEP.
7	ALT PLS OUT	H; 2.4V Min. L; 0.4V Max.		Line alternate pulse output pin NTSC mode; L PAL mode ; Alternate H and L every IH.
8	Vcc 3	*5V		Supply pin of APC, HUE, VXO and SYNC SEP.
9	APC TC	*3.4V		APC (Auto Phase Control) time constant and fo adjusting pin By varying the DC voltage to be applied to this pin, free running frequency of VXO adjustment can be performed.

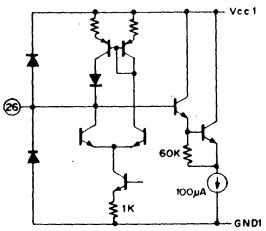
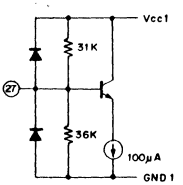
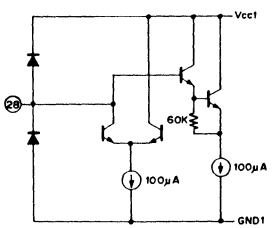
***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
10	HUE ADJ	*2.0V		HUE adjusting pin By applying voltage 0 to 5V to this pin, HUE adjustment at over ±30° can be performed. Ground with a capacitor at PAL mode.
11	VXO 2	3.1V Typ.		X' tal oscillation pin
12	VXO 1	3.3V Typ.		X' tal oscillation pin
13	GND 3	0V		GND pin of APC, HUE and VXO.
14	SC OUT	1.8V Typ.		Sub carrier output pin
15	GND 2	0V		GND pin of demodulator and Y/C mixer.
16	R-Y OUT	2.0V Typ.		R-Y output pin
17	B-Y OUT			B-Y output pin
18	Y OUT	2.0V Typ.		Y output pin
19	DLA IN	*2.3V (PAL) *0V (NTSC)		DL amplifier input pin Ground at NTSC mode. Connect with IHDL output during PAL mode.

***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
20	DLA BIAS	*2.3V (PAL) *0V (NTSC)		NTSC/PAL mode switching and DL amplifier gain adjusting pin. NTSC/PAL mode selection and DL amplifier gain adjustment in PAL mode are effected through application of voltage to this pin. $V_{20} \leq 0.8V$; NTSC mode $2.0V \leq V_{20} \leq 2.8V$; PAL mode Variable range over ±3dB
21	CHROMA OUT	3.7V Typ.		Chroma output pin Connect to Vcc 2 at NTSC mode. Connect to IHDL input at PAL mode.
22	Vcc 2	*5V		Supply pin of demodulator and Y/C mixer.
23	CHROMA ADJ	2.5V Typ.		Chroma amplifier gain adjusting pin Chroma amplifier adjustment can be performed by applying volage to this pin. $V_{23} \leq 0.8V$; B/W (Free run) mode $2.0V \leq V_{23} \leq 3.2V$; Color mode. Variable range –20 to 0dB.
24	CHROMA IN	2.3V Typ.		Chroma signal input pin Typical input level is burst amplitude 143mVp-p.
25	ACC TC			ACC (Auto Color Control) time constant pin

***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
26	TC 2			Pedestal clamp time constant pin
27	VIDEO IN	2.7V Typ.		Video signal (luminance + sync signal) input pin Standard input level is 0.36 Vp-p.
28	TC 1			Feed back clamp time constant pin for SYNC SEP.

Electrical Characteristics

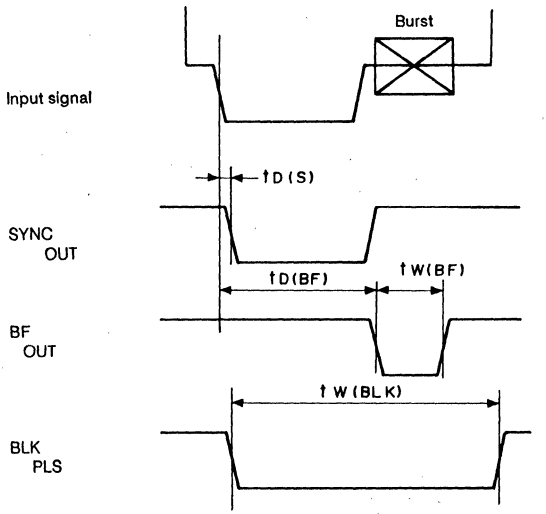
(See the Electrical Characteristics Test Circuit.)
Ta = 25°C, Vcc = 5V

Test item		Symbol	Condition	Input signal V	Input signal C	Test point	Min.	Typ.	Max.	Unit
Consumption current 1		Icc1	Chroma input no signal PAL mode	2	–	6	3.45	4.55	6.70	mA
Consumption current 2		Icc2				22	5.48	7.24	10.65	mA
Consumption current 3		Icc3				8	3.13	4.13	6.07	mA
Video amplifier voltage gain		$V_{O(Y)}$	V_{AC}=0.1Vp-p f=100kHz V_{DC}=0.125V Refer to test method detail-1	1	–	18	9 (11.5)	10 (12.5)	11 (13.5)	dB
Video amplifier frequency characteristics		$f_{O(Y)}$	Input frequency of –3dB with 100kHz output taken as 0dB	1	–	18	5.0			MHz
Video amplifier maximum output		$V_{OM(Y)}$	V_{AC}=0.32Vp-p f=100kHz V_{DC}=0.16V	1	–	18	0.7 (1.0)			Vp-p
Demodulation output DC voltage		$E_{O(R-Y)}$	Chroma input no signal	2	–	16	1.4	2.0	2.7	V
		$E_{O(B-Y)}$				17	1.4	2.0	2.7	
Video output pedestal voltage		$E_{O(Y)}$				18	1.6	2.0	2.3	
Color difference demodulation output voltage		$E_{O(R-Y)}$	Refer to test method detail-2	3	5/7	16	1.4 (1.0)			Vp-p
		$E_{O(B-Y)}$				17	1.0 (1.27)			
Demodulating output residual carrier		$CL_{(R-Y)}$	Chroma input no signal 3.58MHz component	2	–	16			40	mVp-p
		$CL_{(B-Y)}$				17				
ACC characteristics 1		ACC1	$ACC1 = \frac{Voc\ (Vin=-20dB)}{Voc\ (Vin=0dB)}$	3	5/7	21	–5.0	–2.0		dB
ACC characteristics 2		ACC2	$ACC2 = \frac{Voc(Vin=+6dB)}{Voc(Vin=0dB)}$	3	5/7	21		+1.0	+3.0	dB
Color killer level		ek	Chroma input level during color killer operation	3	5/7	24	–44	–38	–32	dB
APC pulling range		fp		2	6/8	14	±300			Hz
Synchronizing output	H level	$V_{OH(S)}$		2	–	2	2.4			V
	L level	$V_{OL(S)}$							0.4	
	Delay time	$t_{D(S)}$					0.4	0.5	0.6	μs
Burst flag output	H level	$V_{OH(BF)}$		2	–	3	2.4			V
	L level	$V_{OL(BF)}$		2	–	3			0.4	V
	Pulse width	$t_{W(BF)}$	when adjust to $t_{D(bf)}$=5.6μs	2	–	3	2.2	2.4	2.6	μs
Blanking pulse width		$t_{W(BLK)}$		2	4	18	9.0	10.0	11.0	μs
Sub carrier output voltage		$V_{O(SC)}$		3	5/7	14	400	500		mVp-p
Alternate pulse output	H level	$V_{OH(ALT)}$	PAL mode	3	5/7	7	2.4			V
	L level	$V_{OL(ALT)}$							0.4	

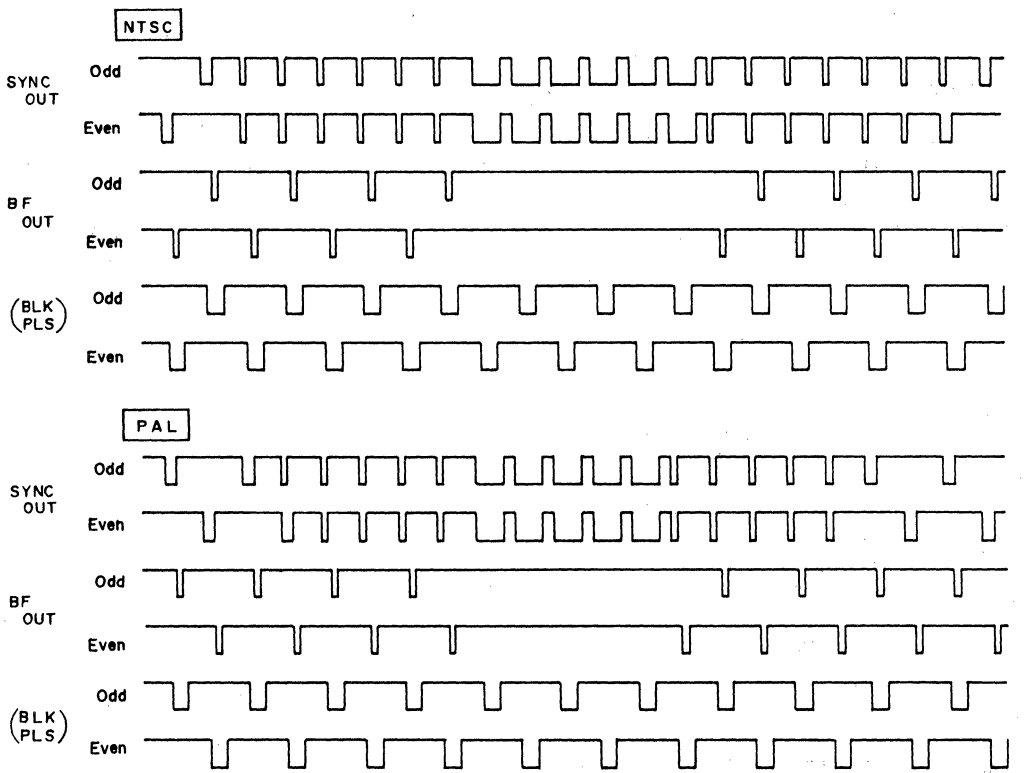
Note) The values in the parentheses are for CXA1228S.

Synchronous Timing Chart

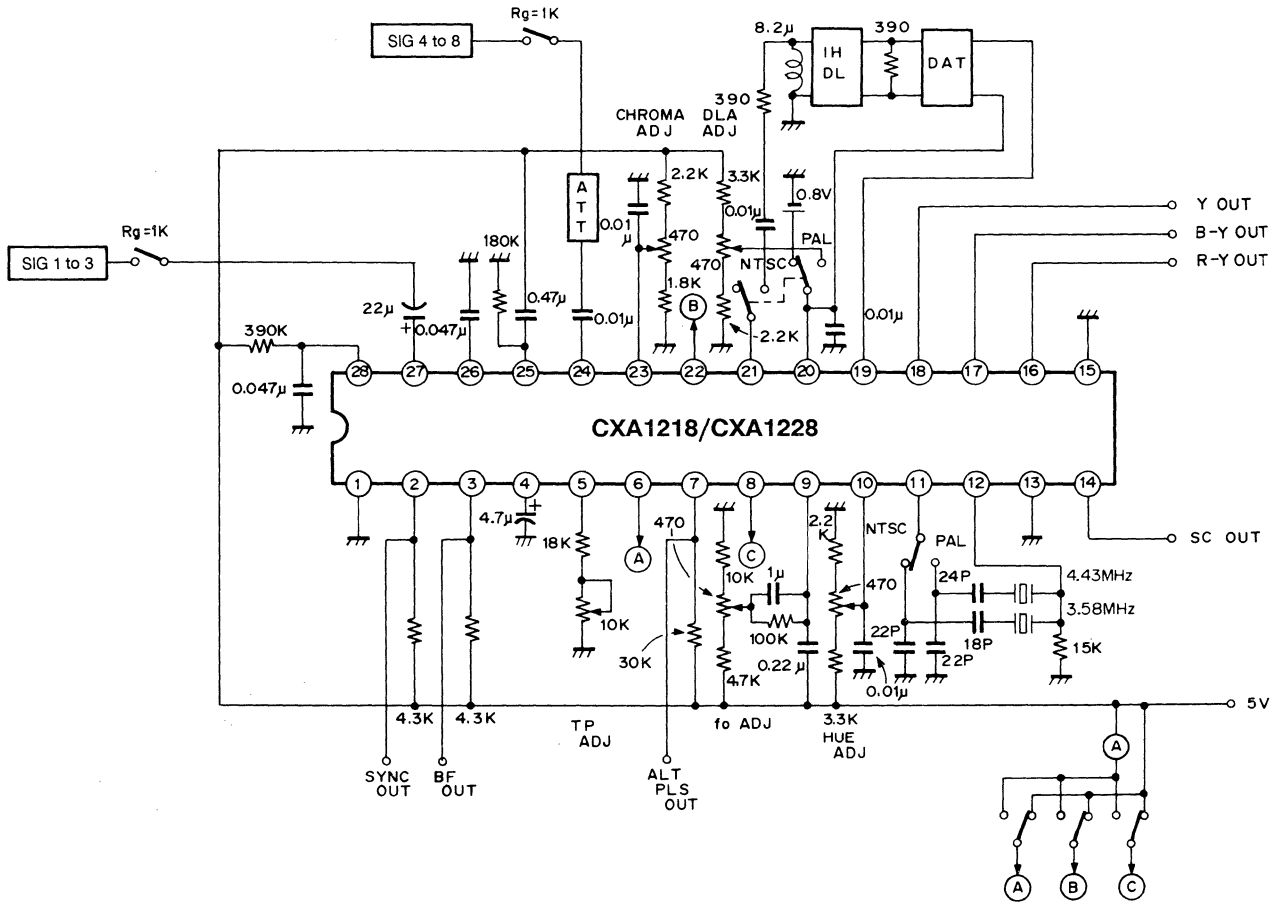
H Synchronizing



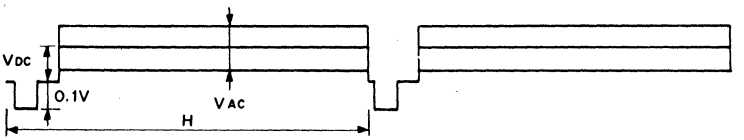
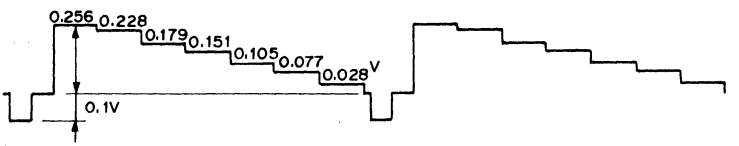
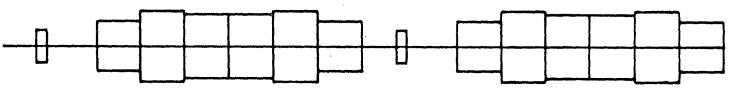
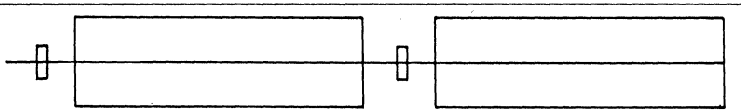
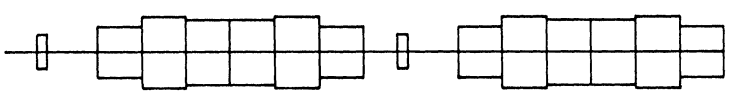
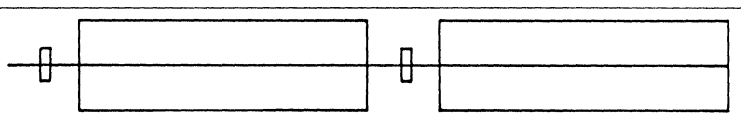
V Synchronizing



Electrical Characteristics Test Circuit

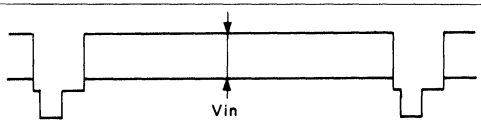
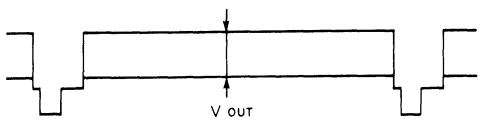


Input signal

V	SIG 1	
	SIG 2	
	SIG 3	
C	SIG 4	Sine wave Frequency 3.579545 MHz Amplitude 143 mVp-p
	SIG 5	 Amplitude 143 320 451 422 422 451 320 mVp-p Phase 180 168 284 241 61 104 348 deg Frequency 3.579545 MHz
	SIG 6	 Amplitude 143 436 mVp-p Phase 180 0 deg Frequency 3.579545 MHz ±300 Hz
	SIG 7	 Amplitude 143 320 451 422 422 451 320 143 320 451 422 422 451 320 mVp-p Phase 135 168 284 241 61 104 348 225 192 76 119 299 256 12 deg Frequency 4.433619 MHz
	SIG 8	 Amplitude 143 436 143 436 mVp-p Phase 135 0 225 0 deg Frequency 4.433619 MHz ±300 Hz

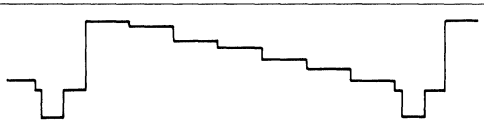
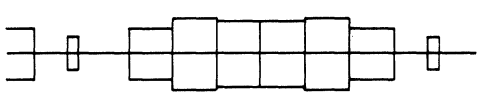
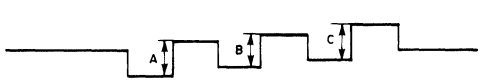
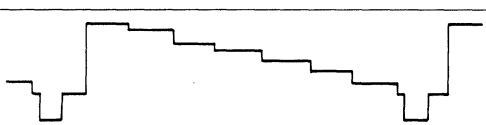
Details of Test Method

1. Video amplifier voltage gain

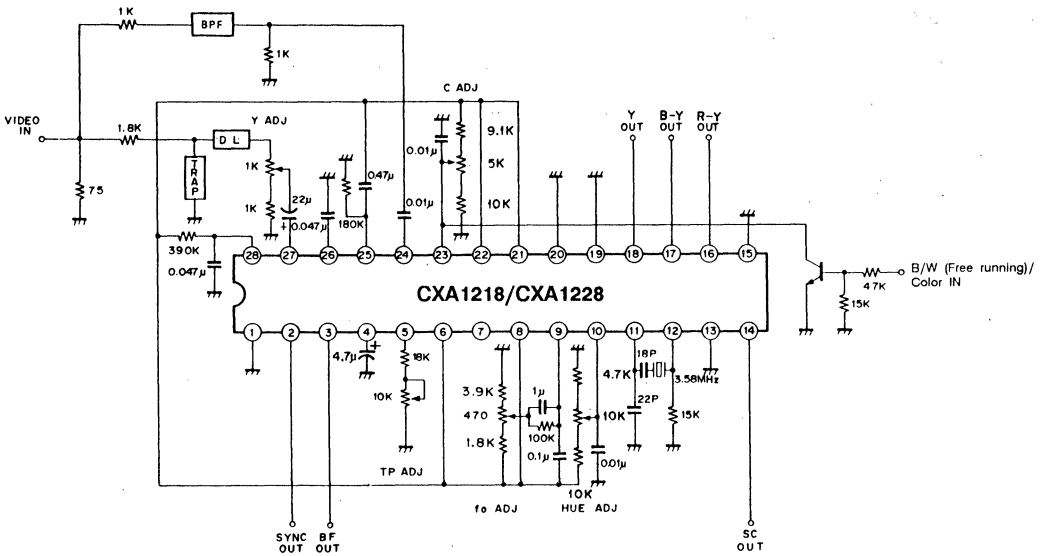
Input waveform	VIDEO IN	
	CHROMA IN	No signal input
Output waveform	Y OUT	

$$Gv = 20 \log \frac{Vout}{Vin} \quad (dB)$$

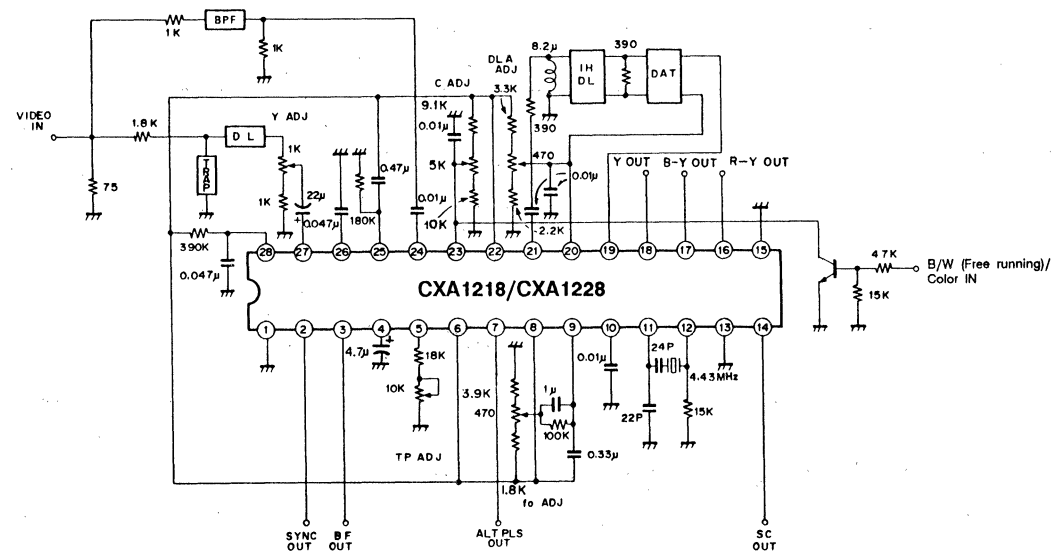
2. Primitive output voltage

Input waveform	VIDEO IN	
	CHROMA IN	
Output waveform	R-Y OUT	
	B-Y OUT	
	Y OUT	

Application Circuit (NTSC mode)



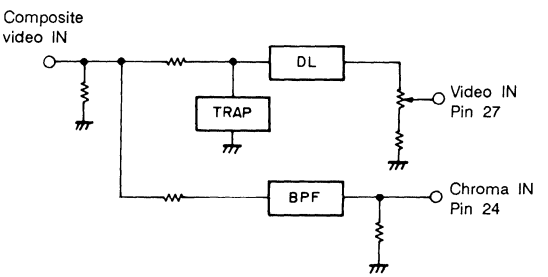
Application Circuit (PAL mode)



Applications

1. Input signals

Composite video signal input is separated into video signal (Y) and chroma signal (C) by band-pass filter, trap and delay line, Y is input to Pin 27 and C to Pin 24. While composite video signal is input at 1 Vp-p, the typical levels of the input signals are as shown in the table below.



		CXA1218S	CXA1228S
Composite video input (Synchronous negative polarity)		1.0Vp-p	1.0Vp-p
Video input	Luminance	0.256Vp-p	0.189Vp-p
	Sync	0.103Vp-p	0.076Vp-p
Chroma input	Burst	0.143Vp-p	0.143Vp-p

2. Time pulse adjustment

BF (Burst Flag) pulse positional adjustment can be performed by changing the current to be taken out from Pin 5. Setting tD (BF) at 5.6 μs by this adjustment results in that BF pulse width is set at approx. 2.4 μs and BLK (blanking) pulse width at 10 μs.

3. Monochrome (free-running)/color mode switching

If Pin 23 (CHROMA ADJ) is set to H (≧2.0 V), the color mode is established. Input chroma signal will be decoded and output in the form of color difference signal. If Pin 23 is set to L (≦0.8V), the monochrome (free-running) mode is established and the APC circuit is made to stop. As a result, VXO oscillates in the free-running mode.

4. NTSC/PAL mode switching

Setting Pin 20 (DL A BIAS) to H (≧2.0V), establishes the PAL mode, and setting the pin to L (≦0.8V).

5. Chroma output

Chroma signal subjected to ACC and blanking is output at Pin 21 (CHROMA OUT). Output amplitude is approx. 160mVp-p with typical input (75% color bar).
In the PAL mode, this output is to be input to 1 H DL. In the NTSC mode, connect Pin 21 to the power supply (Vcc).

6. DL (Delay Line) AMP

An amplifier for insertion of 1 H DL and matching loss compensation when in the PAL mode. Its gain is variable within 14 ± 4 dB to absorb DL dispersion.
Its input pin is Pin 19 (DL A IN); apply to this pin a bias voltage of the same potential as with Pin 20 (DL A BIAS). The signal having passed through 1 H DL is to be input to Pin 19 after adjusted at the delay adjusting transformer (DAT) so that the delay time is 1 H (64 μs).

In the NTSC mode, this amplifier is not used; set the levels of Pins 19 and 20 at L (≦0.8V).

7. VXO and APC
Pin 9 (APC TC) a time constant pin for APC. In the monochrome (free-running) mode in which the APC circuit does not operate, the free-running frequency depends on the DC voltage across this pin. VXO can operate either for NTSC or PAL by changing the quartz oscillator and series capacity.

8. Adjustment procedure
Input signal : 100% color bar

[NTSC mode]

1) BF positional adjustment
Adjust the resistance between Pin 5 and GND so that BF position t_D = 5.6 μs.
2) Video amplifier level adjustment
Adjust Y ADJ so that Y output white peak (100% white) is of 0.714 Vp-p.
3) fo adjustment
Establish the monochrome (free-running) mode, and adjust fo ADJ so that oscillation frequency (output subcarrier) frequency is fsc.
4) Hue adjustment
Establish the color mode, and adjust HUE ADJ so that output amplitudes A, B and C are all equal.
5) Chroma level adjustment
CXA1218S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.0 Vp-p.
CXA1228S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.27 Vp-p.

[PAL mode]

1) BF positional adjustment ..... Same as with NTSC mode.
2) Video amplifier level adjustment .. Same as with NTSC mode.
3) fo adjustment ..... Same as with NTSC mode.
4) DL amplifier adjustment
Establish the color mode, and adjust DLA ADJ so that the R output amplitude is the same for any adjacent two H intervals.
5) Chroma level adjustment
CXA1218S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.0 Vp-p.
CXA1228S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.27 Vp-p.

Description of Operation

1. Sync separation system
   The sync separation system clamps the sync tip of the video signal having been input from Pin 27 to separate the sync signal from the input video signal. Sync pulses are then processed to form BF, H, and BLK pulses, which are supplied to subsequent circuits. Of these pulses, sync and BF pulses are output at Pins 2 and 3, respectively, after transformed to TTL level via buffer.

2. Luminance signal regeneration system
   Video signal input from Pin 27 has its pedestal clamped, and amplified by the Y amplifier.

3. ACC system
   The burst component of the chroma signal having been input from Pin 24 is detected at ACC DET. Feedback to ACC AMP occurs depending on the detected output so that the burst level is kept constant.

4. APC system
   After the signal level is brought to the fixed value at ACC AMP, the burst component alone goes into the APC circuit via the BURST GATE circuit. Meanwhile, a 0° carrier and a 90° carrier are formed from VXO output, and the 90° carrier goes into APC via the HUE circuit. At APC, phase comparison is carried out between the 90° carrier and the input burst, and feedback to VXO is performed so that the phase difference is 90°. The 0° and 90° carriers thus formed are supplied to B-Y DEM and R-Y DEM, respectively. Therefore, demodulation axis can be changed by rotating the phase of the 90° carrier at the HUE circuit.

5. Color signal regeneration system
   1) NTSC system
      The chroma signal amplified at ACC AMP is amplified again at CHROMA AMP, then demodulated at B-Y DEM and R-Y DEM, and output at Pins 16 and 17 in the form of color difference signal.

   2) PAL system
      Processing is the same as with the NTSC system up to CHROMA AMP.
      The chroma signal output at Pin 21 goes into DL AMP at Pin 19 via 1 H DL and DAT, and then input to the ADD/SUB circuit after level-controlled. At the ADD/SUB circuit, the signal is subjected to addition and subtraction with respect to the original signal. The signals obtained by addition and subtraction are input to B-Y DEM and R-Y DEM, and demodulated by the 0° carrier and the 90° carrier inverted every H. After that, the signal is output in the form of color difference signal as with the NTSC system.

6. PAL ID
   The PAL signal is transmitted with its R-Y component inverted every H. It is therefore necessary to inverse the demodulation axis every H. In this IC, the 90° carrier is inverted in synchronization with H BLK pulses, and checking for correspondence with the input burst is performed by synchronous detection. If an error is detected, feedback to FF (Flip Flop) is performed for correction.

SONY

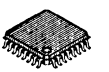
CXA1385Q

LCD TV YC Jungle

Description

The CXA1385Q is a LCD TV IC that converts the composite video signals to RGB equivalents. It is ideally suited for use in a 2- to 4-inch LCD TV set. It incorporates all filters necessary for signal processing.

32 pin QFP (Plastic)



Features

- Built-in delay line (Y/C delay alignment)
- Built-in TRAP, BPF, and SHARPNESS functions
- Built-in APL circuit
- Few number of parts (approximately 50 parts)
- Low power consumption 135mV (Vcc=5V).

Applications

Color LCD TV sets etc.

Structure

Bipolar silicon monolithic IC

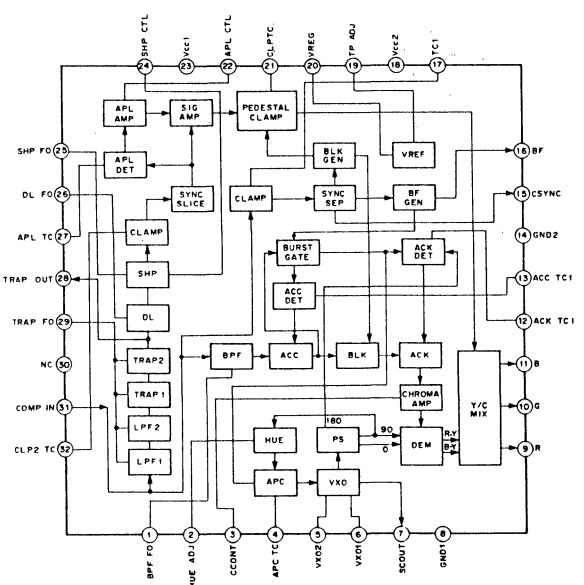
Absolute Maximum Ratings

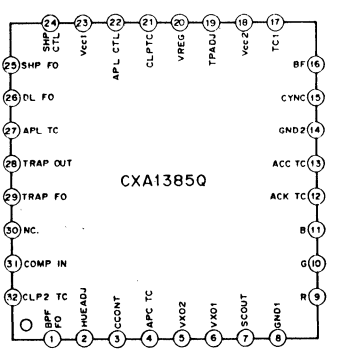
• Supply voltage	Vcc	14	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	500	mW

Operating Conditions

Supply voltage	Vcc	4.75 to 5.25	V

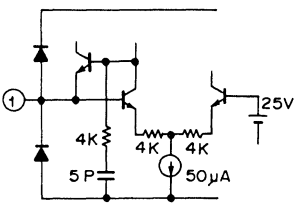
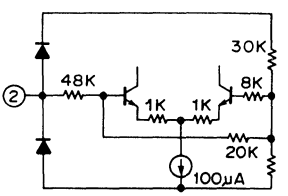
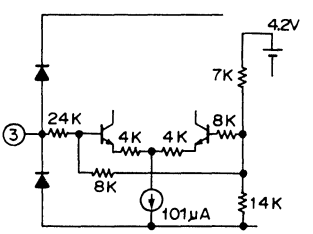
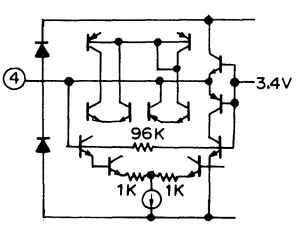
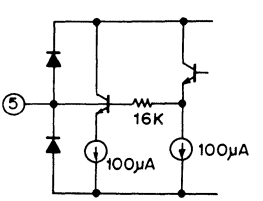
Block Diagram and Pin Configuration

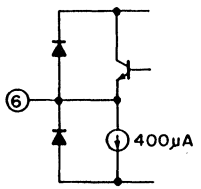
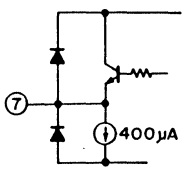
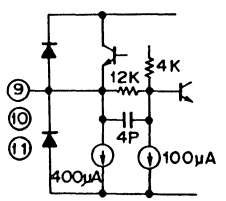
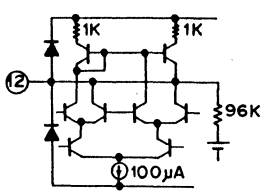
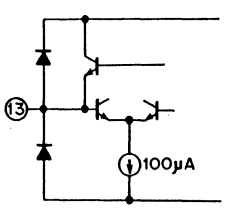


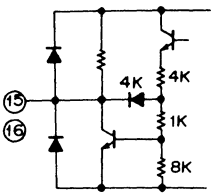
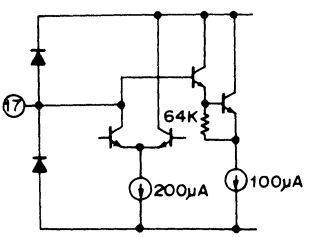
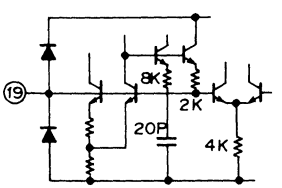
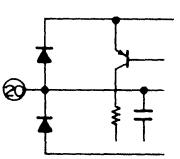
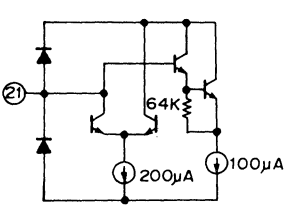


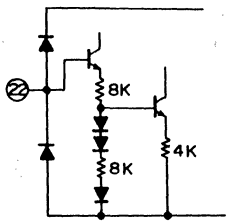
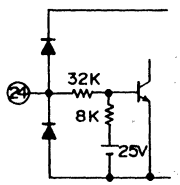
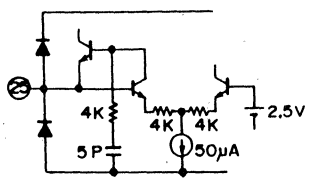
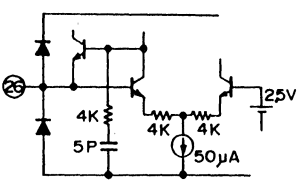
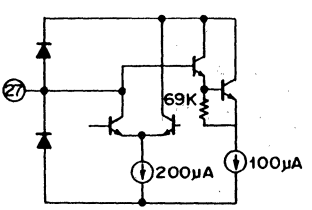
E91621 - ST

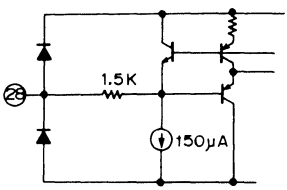
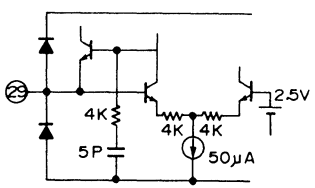
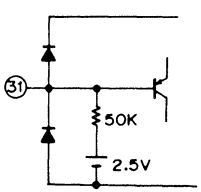
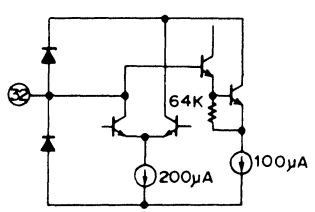
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	BPF F0	2.1V		Filter fo adjustment. The current derived from this pin is made variable for filter fo adjustment.
2	HUE ADJ	2.0V		Hue adjustment. Applying a voltage of 0 to 5V to this pin provides hue adjustment over ± 20°.
3	CCONT	2.8V typ.		Chroma amplifier gain adjustment. Chroma amplifier adjustment is made according to the voltage applied to this pin.
4	APC TC	3.4V		APC (color sync) time constant and free-running frequency adjustment. The VXO free-running frequency is adjusted by varying the DC voltage applied to this pin.
5	VXO2	2.8V		Crystal oscillation.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	VXO1	3.3V		Crystal oscillation.
7	SC OUT	1.3V		Subcarrier output.
8	GND1	0V		Filter/chroma GND.
9	R	2.0V		R output.
10	G			G output.
11	B			B output.
12	ACK TC	3.2V		ACK (automatic color killer) time constant.
13	ACC TC			ACC (automatic color control) time constant.
14	GND2	0V		Y GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	CSYNC	H; 2.4V min. L; 0.4V max.		Composite sync output (TTL level).
16	BF			Burst flag output (TTL level).
17	TC1			Feedback clamp time constant for SYNC SEP.
18	Vcc2	5V *		Y power supply.
19	TP ADJ	1.23V		Burst flag adjustment. The burst flag position to (BF) is adjusted to 5.6 µs by varying the current derived from this pin.
20	VREG	4.2V		4.2V regulator output. It provides a decoupling capacity.
21	CLP TC			Pedestal clamp time constant.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
22	APL CTL	2.5V		APL sensitivity adjustment. When the APL amplifier is not required, connect this pin to the GND.
23	Vcc1	5V		Filter/chroma power supply.
24	SHP CTL	2.5V		(1) Sharpness gain adjustment. (2) Variable range: –5dB to +5dB ($1.5 \leqq V_{24} \leqq 3.5$). (3) The fo band gain can be adjusted by varying the voltage applied to this pin.
25	SHP FO	2.1V		Filter frequency adjustment. Filter fo adjustment is made by varying the current derived from this pin.
26	DL FO	2.1V		Delay line delay amount adjustment. The delay amount is adjusted by varying the current derived from this pin.
27	APL TC	2.0V		Time constant for luminance signal APL (average picture level) detection.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	TRAP OUT	2.5V		The Y signal passing through the trap can be monitored at this pin. To obtain a deeper trap, connect the LC in series with the GND.
29	TRAP FO	2.1V		Filter fo adjustment. Filter fo adjustment is made by varying the current derived from this pin.
30	NC			
31	COMP IN	2.5V		Composite video signal input. Typical input is 0.56Vp-p.
32	CLP2 TC			Pedestal clamp time constant.

Electrical Characteristics

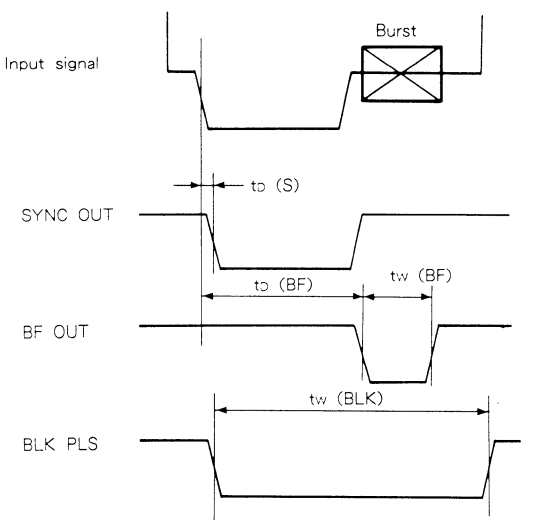
(Ta=25℃, Vcc=5V, See the electrical characteristics test circuit.)

Test item		Symbol	Conditions		Input signal	Test point	Min.	Typ.	Max.	Unit
Current consumption 1		Icc1			1	A1	17.0	26.5	36.5	mA
YAMP voltage gain		Vo (R)	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=300kHz See detailed test procedure 1.		2	V1	6.5	8	9.5	dB
		Vo (G)				V2				
		Vo (B)				V3				
YAMP frequency response characteristics		Fc (R)	Input frequency required for –3dB output generation when the output at 300kHz is 0dB SHP FO (external 39kΩ) SHP CTL=2.5V		2	V1	1.8			MHz
		Fc (G)				V2				
		Fc (B)				V3				
Trap attenuation		V_{TP}	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=3.58MHz * Ratio of the output at 3.58MHz to the 0dB output at 300kHz		2	V3			–30	dB
Sharpness characteristics	MAX	V_{SHP} (MAX)	V_{DC}=280mV V_{AC}=160mVp-p V_{FC}=1.5MHz * Ratio of the output at 1.5MHz to the 0dB output at 300kHz	SHP CTL =3.5V	2	V3	5.0			dB
	MIN	V_{SHP} (MIN)		SHP CTL =1.5V	2	V3			–5.0	dB
AGC characteristics	20% white	V_{AGC1}	V_{DC}=80mV V_{AC}=60mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	4.3	6	7.0	dB
	50% white	V_{AGC2}	V_{DC}=200mV V_{AC}=160mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	3.3	4.6	5.8	
	100% white	V_{AGC3}	V_{DC}=400mV V_{AC}=160mVp-p F_{AC}=300kHz APL CTL=2.5V		2	V3	1.3	2.5	3.5	
Demodulated output DC voltage		E_{ODC} (R)			1	V1	1.5		2.7	V
		E_{ODC} (G)				V2				
		E_{ODC} (B)				V3				
Primary color output voltage		Eo (R)	See detailed test procedure 2.		3	V1	1.1			Vp-p
		Eo (G)				V2				
		Eo (B)				V3				
Demodulated output residual carrier		C_L (R)	3.58MHz component of the output		1	V1			20	mV
		C_L (G)				V2				
		C_L(B)				V3				
ACC characteristic 1		Acc1	$Acc1=\frac{Voc(Vin=-14dB)}{Voc(Vin=0dB)}$		3	V3	–4			dB
ACC characteristic 2		Acc2	$Acc2=\frac{Voc(Vin=+6dB)}{Voc(Vin=0dB)}$		3	V3			3	dB
Color killer level		Ek	Chroma input level during color operation		3	V3	–55		–33	dB
APC pull-in		Fp			5	F1	±250			Hz

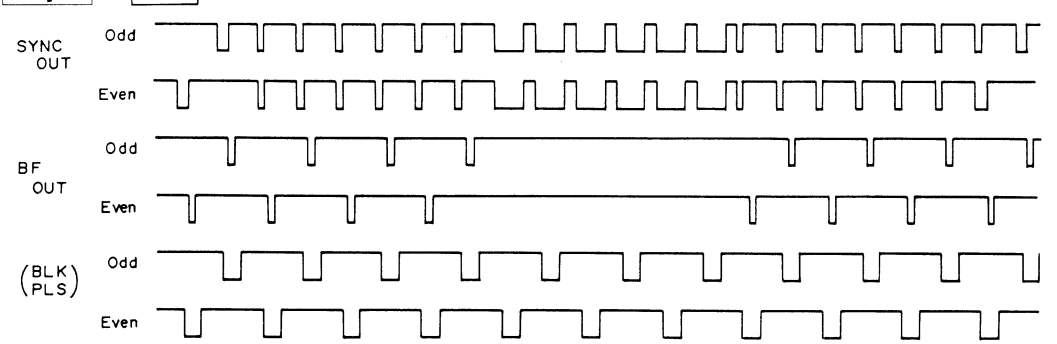
Test item		Symbol	Conditions	Input signal	Test point	Min.	Typ.	Max.	Unit
Sync output	H level	V_{OH} (S)		1	V4	2.4			V
	L level	V_{OL} (S)						0.4	
	Delay time	t_D (S)					0.5		µs
Burst flag output	H level	V_{OH} (BF)		1	V5	2.4			V
	L level	V_{OL} (BF)		1	V5			0.4	V
	Pulse width	tw (BF)	When the t_D (BF) value is adjusted to 5.6 µs	1	V5		2.4		µS
Blanking pulse width		tw (BLK)		4	V3	7.5	9.2	11.0	µS

Sync System Timing Chart

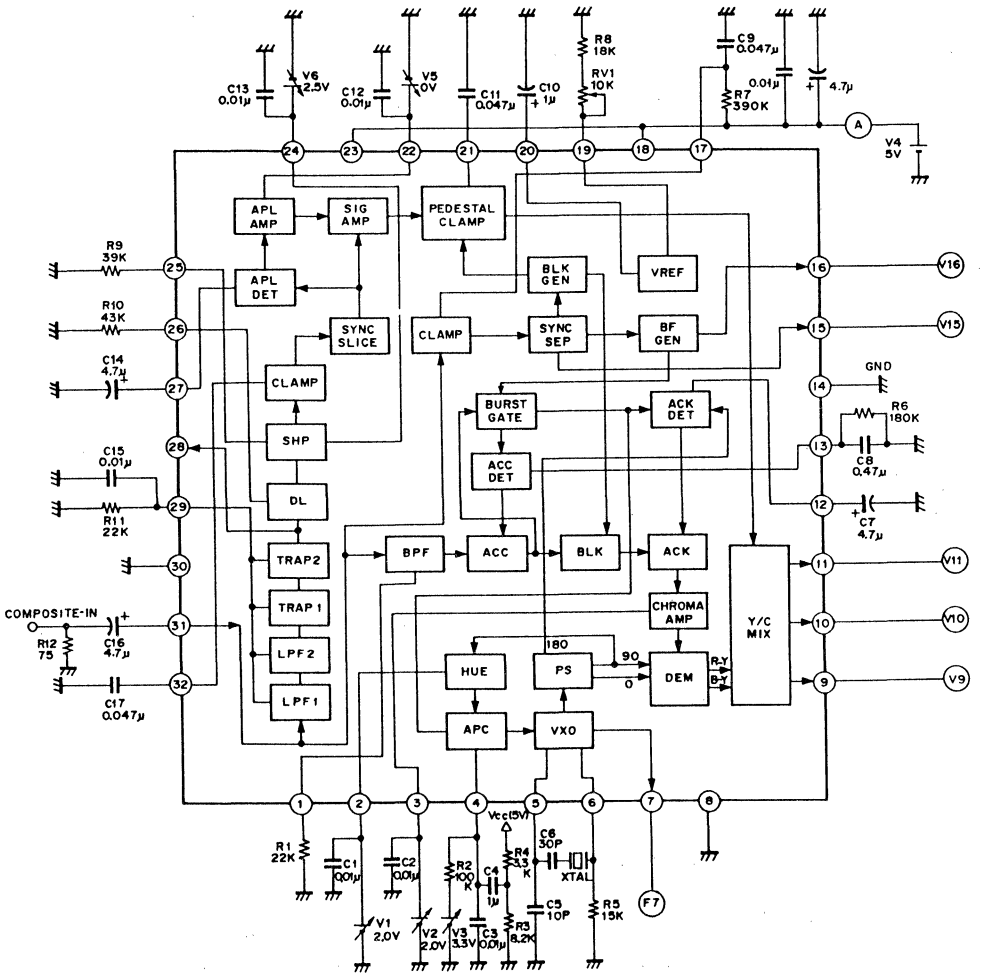
H sync



V sync NTSC



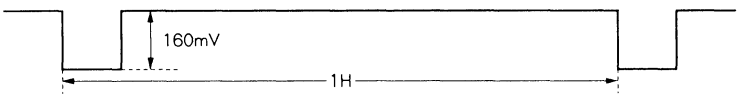
Electrical Characteristics Test Circuit



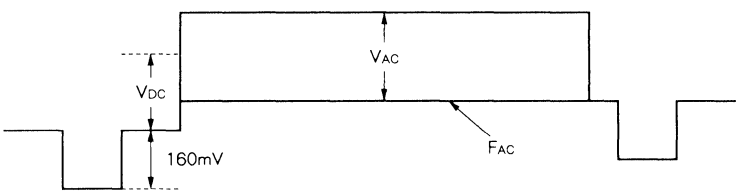
Note) Unless otherwise specified in the Conditions column of the electrical characteristics, the above indicated values are to be applied to V_1, V_2, V_3, V_5, and V_6.

Input Signals

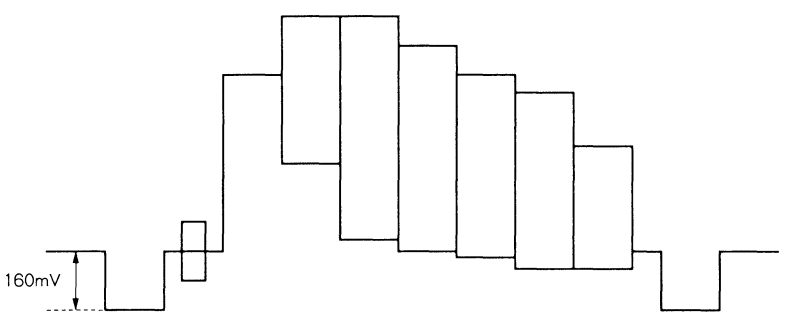
1



2

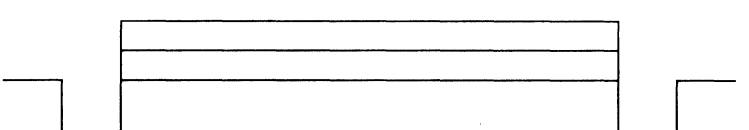


3



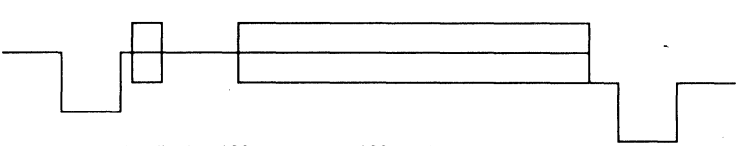
Luminance level	0,	300,	268,	212,	176,	124,	88,	32,	0, mV
Amplitude	160,	0,	264,	376,	352,	352,	376,	264,	0, mVp-p
Phase	180,	–	168,	284,	241,	61,	104,	348,	–, deg
Frequency	3.579545MHz								

4



3.579545MHz/160mVp-p

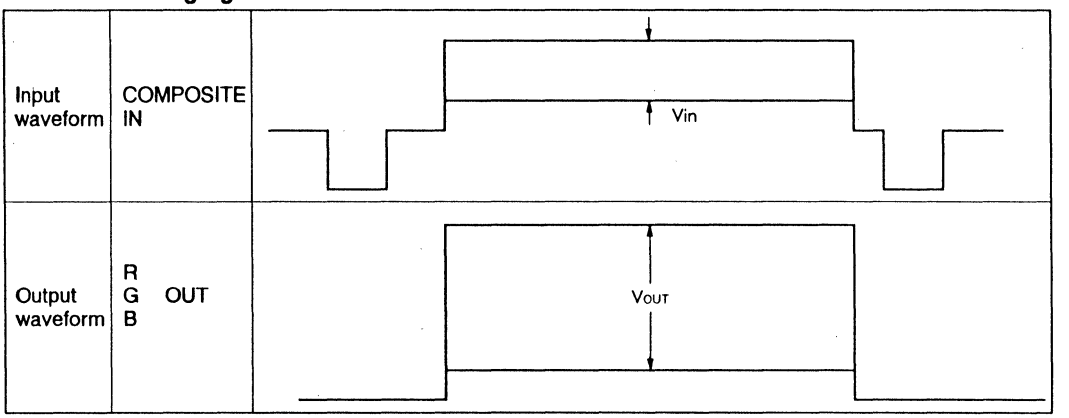
5



Amplitude	160	160	mVp-p
Phase	180	0	deg
Frequency	3.579545MHz ± 250Hz		

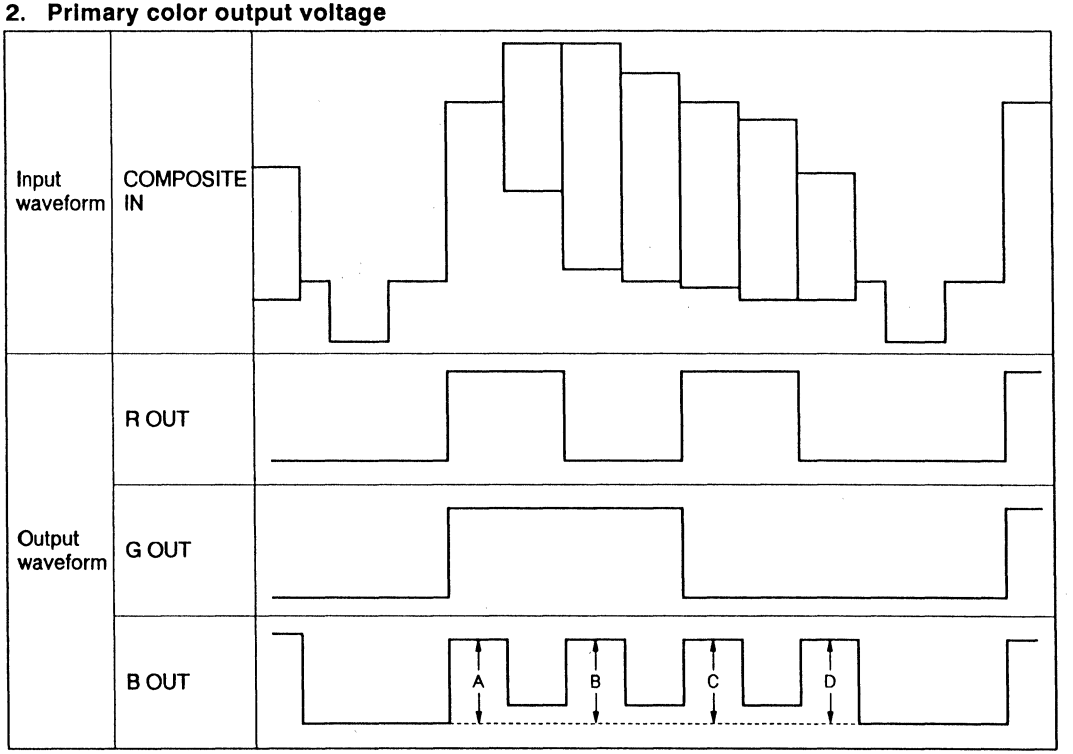
Detailed Test Procedures

1. YAMP voltage gain



G=20log $\frac{V_{OUT}}{Vin}$ (dB)

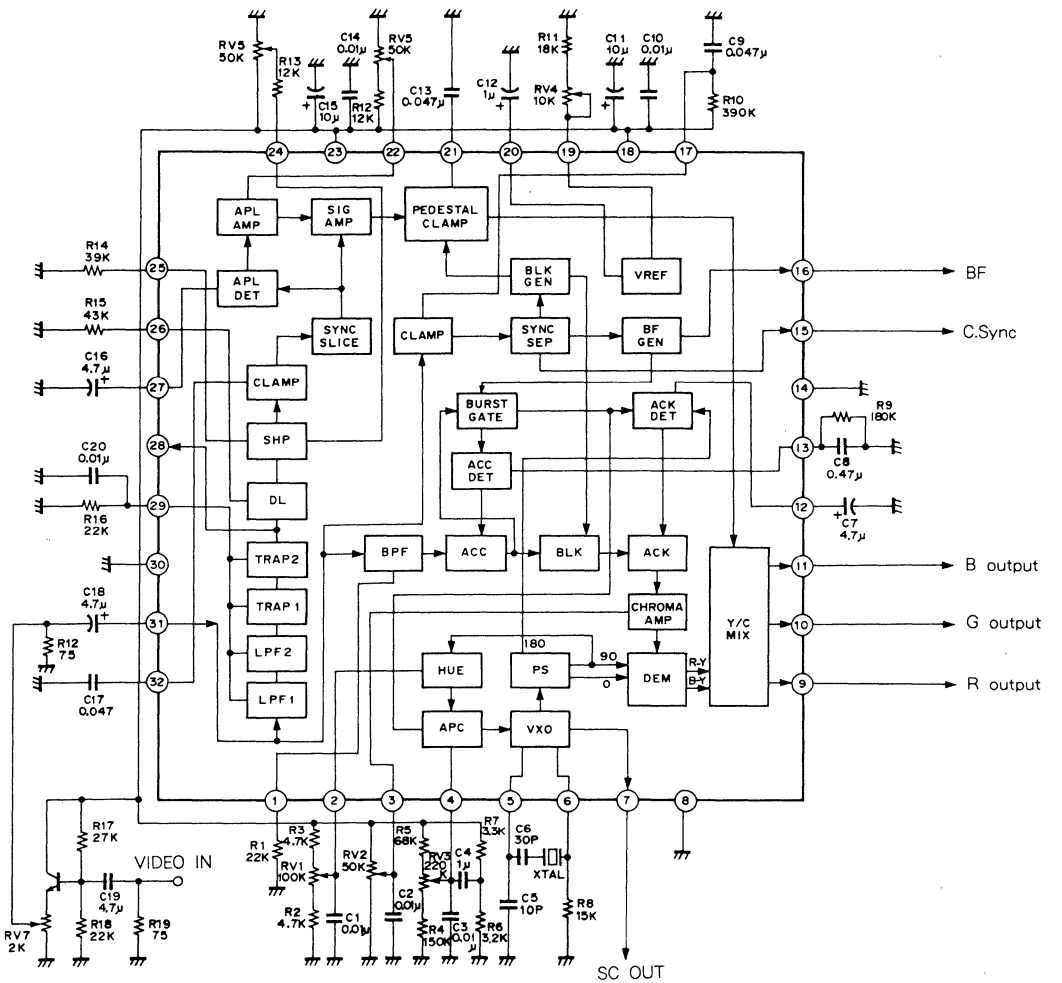
2. Primary color output voltage



Adjustment Procedure (Input signal: 75% color-bar)

1. Adjust the HUE ADJ and C CONT controls so that B output amplitudes A, B, C, and D are equal.

Application Circuit



* Change the C19 input capacitor polarity in accordance with the operating conditions.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

(1) Luminance Signal Regeneration System

i) Trap Filters
Two LPFs and two trap filters are used to derive the luminance signal from the composite signal.

ii) Delay Line Filter
Makes delay amount adjustment relative to the color signal.

iii) Sharpness Filter
Accentuates the 1.5MHz region of the luminance signal passing through the delay line. The voltage applied to Pin 24 (SHP CTL) varies the 1.5MHz component over the range from –5 to +5dB (with reference to 300kHz). When 2.5V is applied to Pin 24 (SHP CTL), the 0dB level (with reference to 300kHz) results.

iv) APL Circuit
The APL (average picture level) is used to control the YAMP gain. When the APL is low, the gain is increased. When the APL is high, on the other hand, the gain is decreased. The AGC turns ON when 2.5V is present at Pin 22 (APL CTL). If the AGC function is not needed, the AGC circuit is turned OFF by applying 0V to Pin 22.

(2) Color Signal Regeneration System

i) BPF
Derives the chroma signal from the composite signal.

ii) ACC Circuit
After the chroma signal is passed through the BPF, the burst signal is detected by the ACC DET. The feedback resulting from detection is then returned to the ACC AMP so as to maintain the burst level constant.

iii) APC Circuit
After being adjusted to a fixed level by the ACC AMP, the signal passes through the burst gate circuit so that only the burst signal enters the APC circuit. Meanwhile, the VXO output is fed to the phase circuit, where the 0 °, 90 °, and 180 ° signals are generated. These signals then go into the hue circuit, and the resultant synthesized signal (90 ° carrier) enters the APC circuit. The phase of this signal is compared against that of the burst signal, and a feedback signal is transmitted to the VXO so that a phase difference of 90 ° occurs. The 0 ° and 90 ° carriers generated in this manner are supplied to the B–Y and R–Y DEM sections. Therefore, the DC voltage applied to Pin 2 (HUE ADJ) controls the synthesized wave phase to vary the demodulation axis.

iv) DEM Circuit
After being adjusted to a fixed level by the ACC AMP, the chroma signal is amplified by the CHROMA AMP, demodulated by the B–Y DEM and R–Y DEM, fed to the Y/C MIX circuit together with the G–Y signal generated by the resistor matrix, and mixed with the luminance signal to generate the R, G, and B primary color outputs.

(3) Sync Separation System

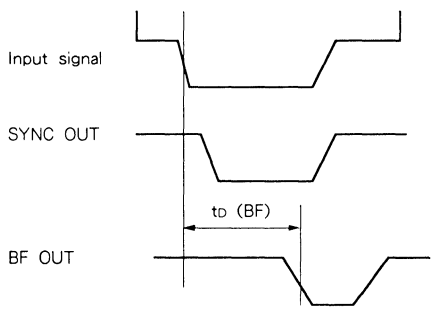
After the composite video signal is entered via Pin 31 (COMP IN), the sync tip is clamped so that sync separation occurs. The resulting SYNC pulse is used to generate the BF (burst flag), BLK, and other timing pulses to be supplied to various circuits. The SYNC and BF pulses are converted to TTL level through buffer, and transferred out.

Adjustment Procedures

Input signal: 75% color-bar (NTSC)

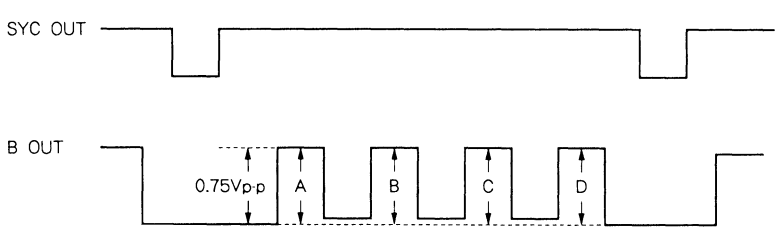
1) fo adjustment
Adjust the Pin 4 (APC TC) DC voltage so that the Pin 7 (SCOUT) oscillation frequency (subcarrier output) is within fsc (=3.579545MHz) ± 20Hz in a no-signal state (free-run).

2) BF position adjustment
Adjust the resistance between Pin 19 and GND to set the BF (burst flag) position t_D (BF) to 5.6 µs.



3) Input level adjustment
With Pin 22 (APL CTL) connected to the GND, adjust the input level so that the B output white peak (75% white) is 0.75Vp-p.

4) HUE ADJ and C CONT adjustments
Adjust the HUE ADJ and C CONT controls so that the amplitudes of all B output colors (A, B, C, and D below) are equal.



Application

1. The maximum input dynamic range is 0.56Vp-p.
   The details are given below.

Composite video signal	0.56Vp-p
Sync signal	0.16Vp-p
Luminance signal	0.40Vp-p (100% white)
Burst signal	0.16Vp-p

   The value 0.56Vp-p is measured from the sync tip to the white peak. Note that the output may be clipped and distorted if the input signal is greater than 0.56Vp-p.
   However, this applies when the AGC is OFF (Pin 22 [APL CTL]=0V).

2. Filter F0 pin
   The filter F0 sensitivities are as follows.

BPF F0	–150kHz/+kΩ
TRAP F0	–140kHz/+kΩ
SHARP F0	–40kHz/+kΩ
DELAY F0	+4nS/+kΩ

3. To obtain a deeper trap, connect the LC (100 μH, 20 pF) in series between Pin 28 (TRAP OUT) and GND. The trap is then rendered about 3dB deeper.

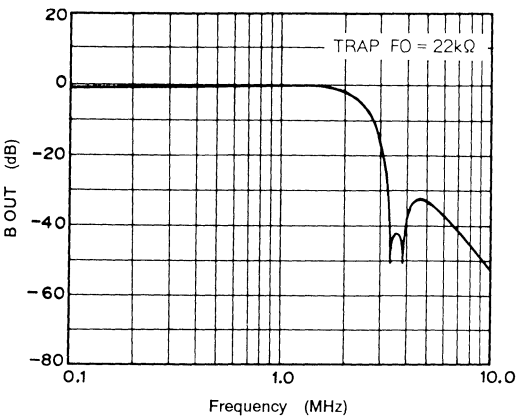
4. Notes on operation

   i) When making wiring connections, ensure that Pin 28 (TRAP OUT) is not affected by signal input or X'tal (crystal oscillator) oscillation frequency.

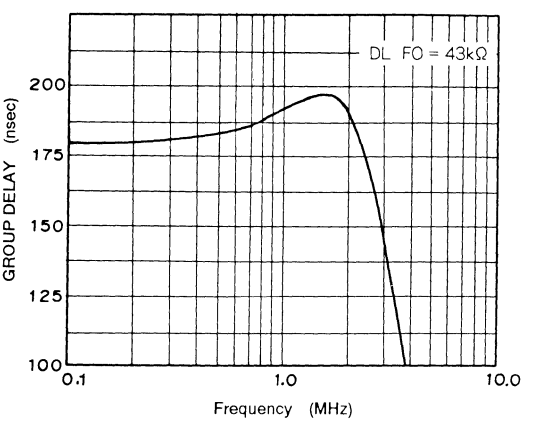
   ii) The fo value of the X'tal varies with the floating capacity and other factors. Therefore, mount the X'tal as close as possible to the IC using a minimum of connecting wiring.

Example of Representative Characteristics

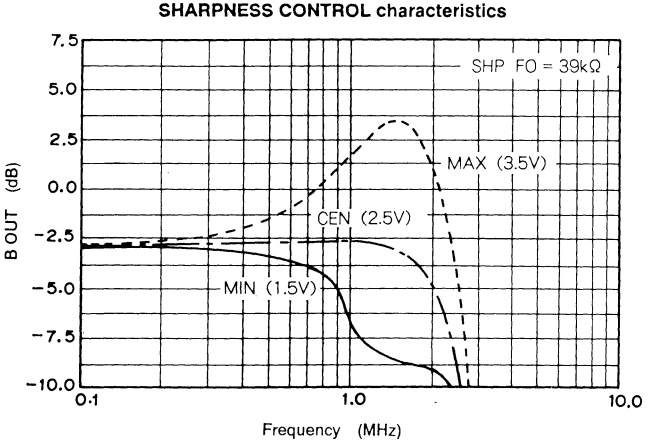
TRAP characteristics



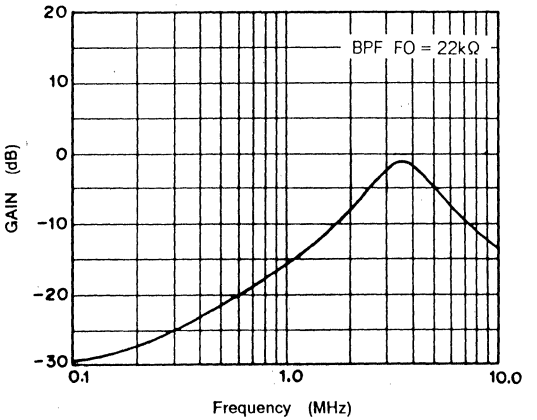
DELAY characteristics



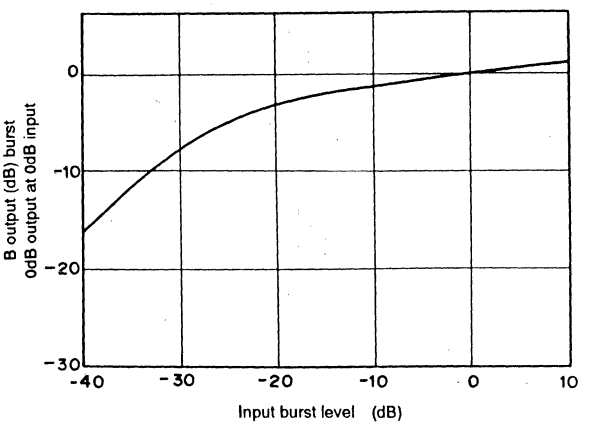
SHARPNESS CONTROL characteristics



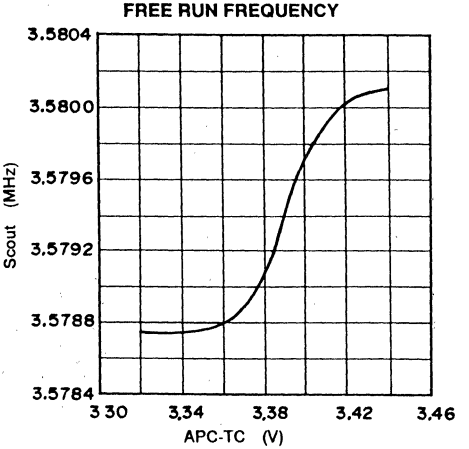
BPF characteristics



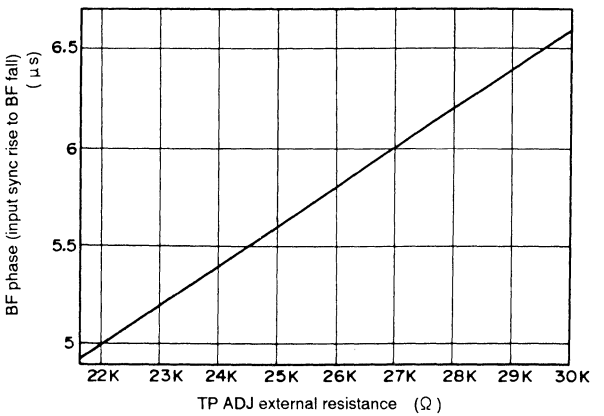
ACC characteristics



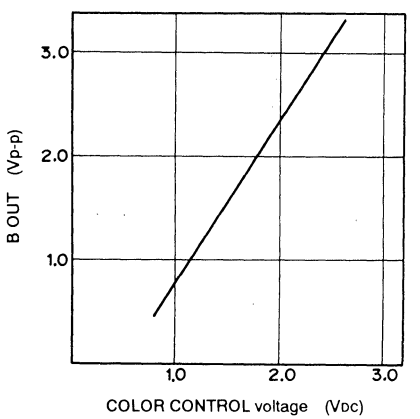
FREE RUN FREQUENCY



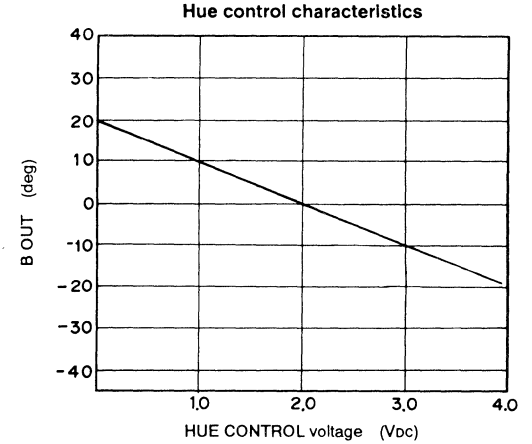
BF phase characteristics provided by TD ADJ (external resistor)



Color control characteristics

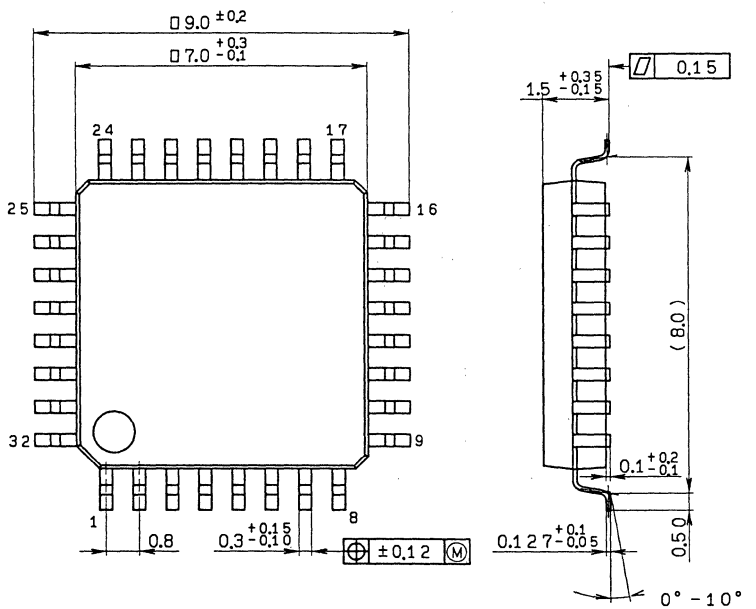


Hue control characteristics



Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

NTSC/PAL Decoder

Description

V7021 is a decoder IC used to convert composite video signals into analog RGB signals. It has signal outputs, such as composite sync, burst flag, sub-carrier, and alternate signal outputs, necessary for image processing. V7021 operates in both NTSC and PAL mode.

Features

- 5V single supply operation
- Low power consumption (about 85mW)
- Compatible with both NTSC and PAL modes.
- Provides composite sync, burst flag, sub-carrier, and line alternate signal outputs.

Function

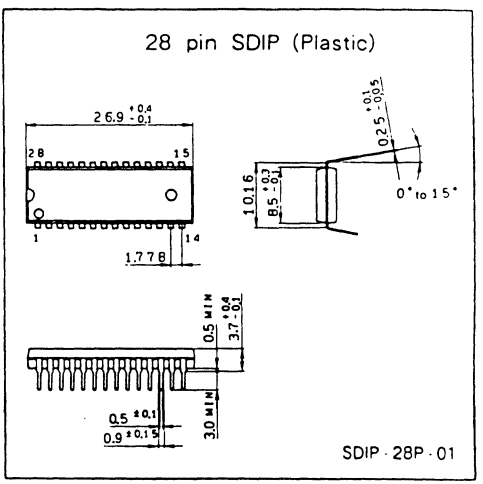
Synchronous separation, Composite sync output, burst flag output, ACC, ACK, APC, demodulator, Y/C mixer, DL amplifier, PAL ID, HUE control

Structure

Bipolar silicon monolithic IC

Package Outline

Unit : mm



Absolute Maximum Ratings

• Supply voltage	V_{CC}	10	V
• Operating temperature	Topr	−20 to +75	℃
• Storage temperature	Tstg	−55 to +150	℃
• Allowable power dissipation	P_D	1250	mW

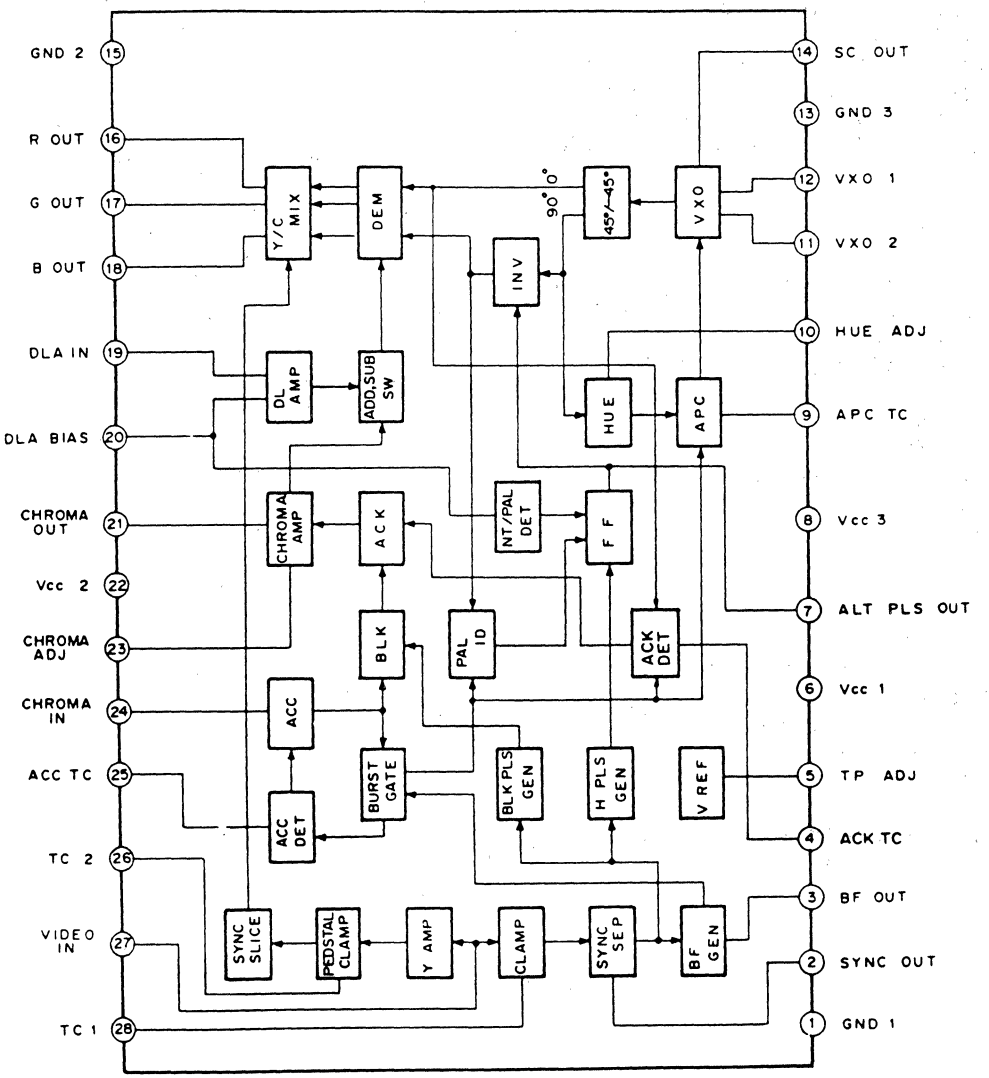
Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V

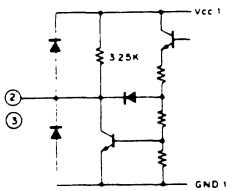
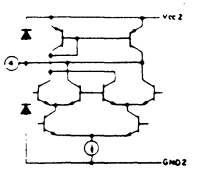
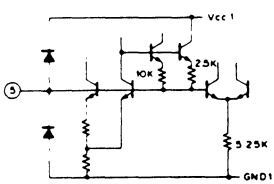
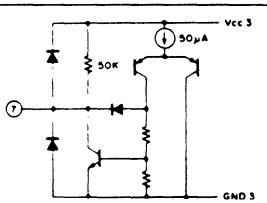
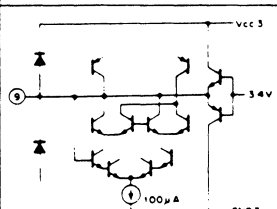
8/91 version

81118 - ST

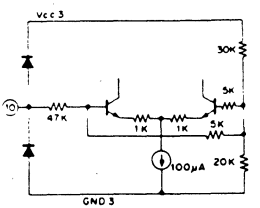
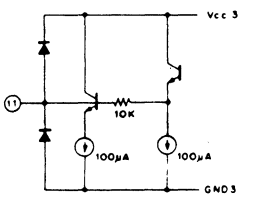
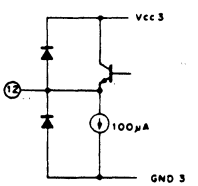
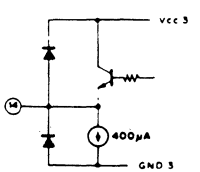
Block Diagram and Pin Configuration



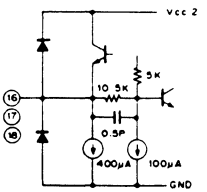
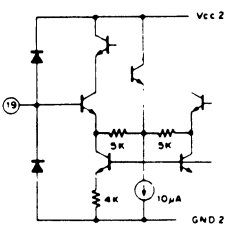
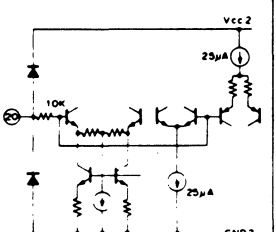
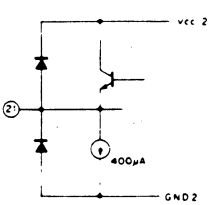
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	GND 1	0V		GND pin of Y AMP and SYNC SEP.
2	SYNC OUT	H ; 2.4V Min. L ; 0.4V Max.		Composite sync output pin (TTL level)
3	BF OUT			Burst flag output pin (TTL level)
4	ACK TC	3.1V Typ.		ACK (Auto Color Killer) time constant pin
5	TP ADJ	1.23V Typ.		Burst flag positional adjusting pin By changing the current from this pin burst flag position adjustment to tD (BF) = 5.6 µs can be performed.
6	Vcc 1	5V *		Supply pin of Y AMP and SYNC SEP.
7	ALT PLS OUT	H ; 2.4V Min. L ; 0.4V Max.		Line alternate pulse output pin NTSC mode ; L PAL mode ; Alternate H and L every 1H.
8	Vcc 3	5V *		Supply pin of APC, HUE, VXO and SYNC SEP.
9	APC TC	3.4V *		APC (Auto Phase Control) time constant and fo adjusting pin By varying the DC voltage to be applied to this pin, free running frequency of VXO adjustment can be performed.

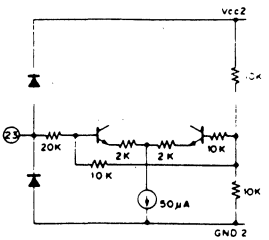
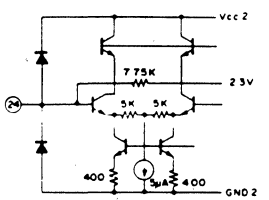
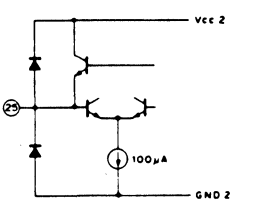
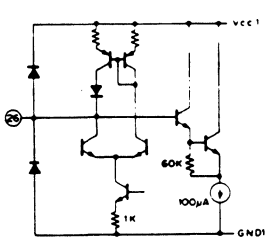
* **Note**) External apply voltage.

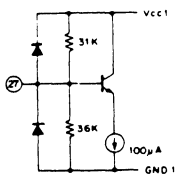
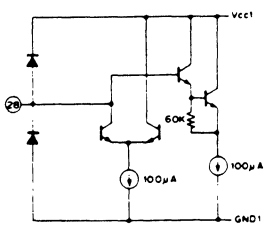
No.	Symbol	Voltage	Equivalent circuit	Description
10	HUE ADJ	2.0V *		Pin for adjusting HUE. By applying 0 to 5V to this pin, more than ±30° HUE can be adjusted. When in PAL mode, it is grounded by the capacitor.
11	VXO2	3.1V (Typ.)		Pin for crystal oscillator.
12	VXO1	3.3V (Typ.)		Pin for crystal oscillator.
13	GND3	0V		Ground pin for APC, HUE, and VXO
14	SC OUT	1.8V (Typ.)		Sub-carrier output pin
15	GND2	0V		Ground pin for demodulator and Y/C mixer.

* **Note**) External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
16	R OUT	2.0V (Typ.)		R output pin
17	G OUT			G output pin
18	B OUT			B output pin
19	DLA IN	2.3V * (PAL) 0V * (NTSC)		DL amplifier input pin. This must be grounded in NTSC mode. The 1HDL output must be connected in PAL mode.
20	DLA BIAS	2.3V * (PAL) 0V * (NTSC)		Selects NTSC or PAL mode, and adjusts DL amplifier again in PAL mode NTSC mode : V_{20} 0.8V max. PAL mode : V_{20} 1.8V min. 2.8V max. The variable range is ± 3dB min.
21	CHROMA OUT	3.7V (Typ.)		Chroma output pin. It is connected to V_{CC2} in NTSC mode, and to the 1HDL input in PAL mode.
22	V_{CC2}	5V		Power pin of demodulator and Y/C mixer.

* **Note**) External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
23	CHROMA ADJ	2.5V (Typ.)		The voltage applied to this pin selects monochrome (BW) or color mode. Monochrome mode : V_{23} 0.8V max. Color mode : V_{23} 2.0V min. 3.0V max. The variable range is −20dB to more than 0dB.
24	CHROMA IN	2.3V (Typ.)		Chroma signal input pin. The standard input level is burst amplitude 143mVp-p.
25	ACC TC			Pin for ACC time constant.
26	TC2			Pin for pedestal clamp time constant.

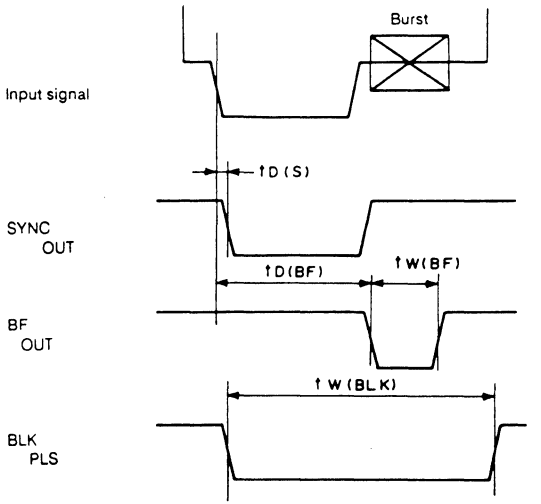
No.	Symbol	Voltage	Equivalent circuit	Description
27	VIDEO IN	2.7V (Typ.)		Input pin of video signal (luminance and SYNC). The standard input level is 0.36Vp-p.
28	TC1			Pin for feedback clamp time constant for SYNC SEP.

Electrical Characteristics (V_{CC} = 5V Ta = 25°C See the Electrical Characteristic Test Circuit.)

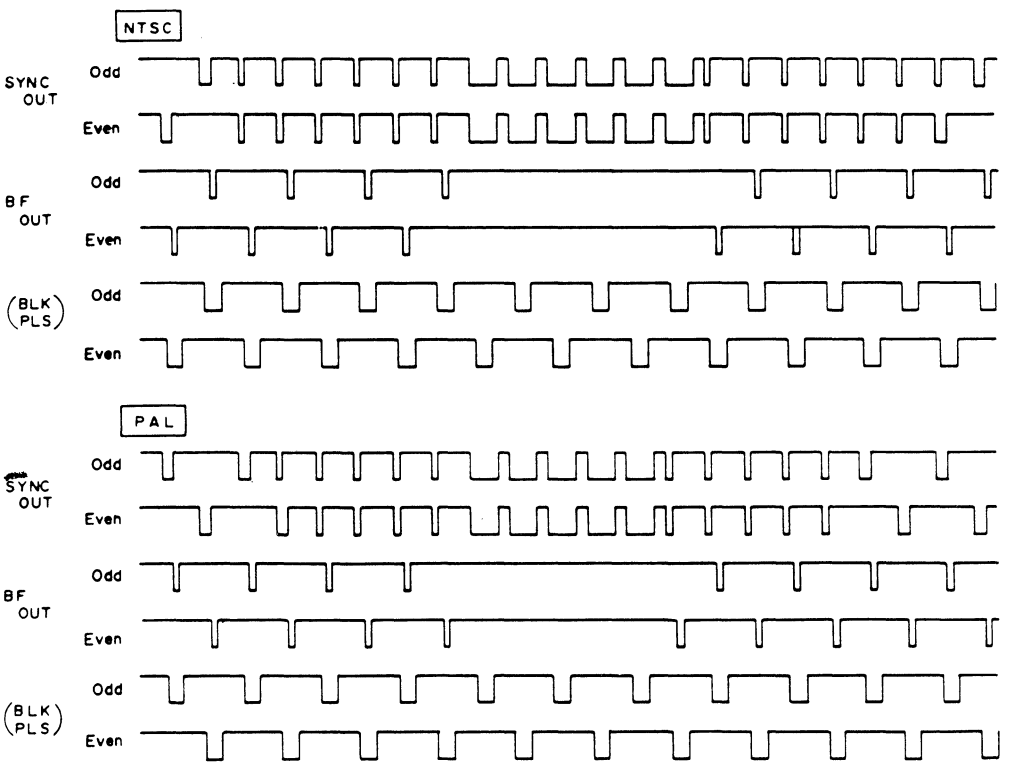
Item		Symbol	Conditions	Input signal V	Input signal C	Test point	Min.	Typ.	Max.	Unit
Supply current 1		I_{CC1}	Signal for no chroma input	2	–	6	3.45	4.55	6.70	mA
Supply current 2		I_{CC2}	PAL mode			22	5.48	7.24	10.65	mA
Supply current 3		I_{CC3}				8	3.13	4.13	6.07	mA
Video amplifier voltage gain		$V_{O(R)}$	V_{AC} = 0.1Vp-p f = 100kHz V_{DC} = 0.125V See test method 1 for details	1	–	16	10.8	11.8	12.8	dB
		$V_{O(G)}$				17				
		$V_{O(B)}$				18				
Video amplifier 3-dB bandwidth		$f_{C(R)}$	Input frequency which becomes – 3dB when 100kHz output is 0dB.	1	–	16	5.0			MHz
		$f_{C(G)}$				17				
		$f_{C(B)}$				18				
Video amplifier maximum output		$V_{OM(R)}$	V_{AC} = 0.32Vp-p f = 100kHz V_{DC} = 0.16V	1	–	16	1.1			Vp-p
		$V_{OM(G)}$				17				
		$V_{OM(B)}$				18				
Demodulation output DC voltage		$E_{ODC(R)}$	Signal for no chroma input	2	–	16	1.4	2.0	2.8	V
		$E_{ODC(G)}$				17				
		$E_{ODC(B)}$				18				
Original color output voltage		$E_{O(R)}$	See test method 2 for details	3	5/7	16	0.9	1.0	1.1	Vp-p
		$E_{O(G)}$				17				
		$E_{O(B)}$				18				
Demodulation output residual carrier		$C_{L(R)}$	Signal for no chroma input 3.58MHz component	2	–	16			40	mVp-p
		$C_{L(G)}$				17				
		$C_{L(B)}$				18				
ACC characteristic 1		ACC1	$ACC1 = \frac{V_{OC}\ (Vin = -14dB)}{V_{OC}\ (Vin = 0dB)}$	3	5/7	21	– 3.0	– 1.0		dB
ACC characteristic 2		ACC2	$ACC2 = \frac{V_{OC}\ (Vin = +6dB)}{V_{OC}\ (Vin = 0dB)}$	3	5/7	21		+ 1.0	+ 3.0	dB
Color killer level		e_k	Chroma input level during color killer operation	3	5/7	24	– 44	– 38	– 32	dB
APC lock in range		f_P		2	6/8	14	± 300			Hz
Sync output	H	$V_{OH(S)}$		2	–	2	2.4			V
	L	$V_{OL(S)}$							0.4	V
	Delay	$t_{D(S)}$					0.4	0.5	0.6	µs
Burst flag output	H	$V_{OH(BF)}$		2	–	3	2.4			V
	L	$V_{OL(BF)}$		2	–	3			0.4	V
	Pulse width	$t_{W(BF)}$	When adjusted to $t_{D(BF)}$ = 5.6 µs	2	–	3	2.2	2.4	2.6	µs
Blanking pulse width		$t_{W(BLK)}$		2	4	18	9.0	10.0	11.0	µs
Sub-carrier output		$V_{O(SC)}$		3	5/7	14	400	500		mVp-p
Alternate pulse output	H	$V_{OH(ALT)}$	PAL mode	3	5/7	7	2.4			V
	L	$V_{OL(ALT)}$							0.4	

Synchronization System Timing Chart

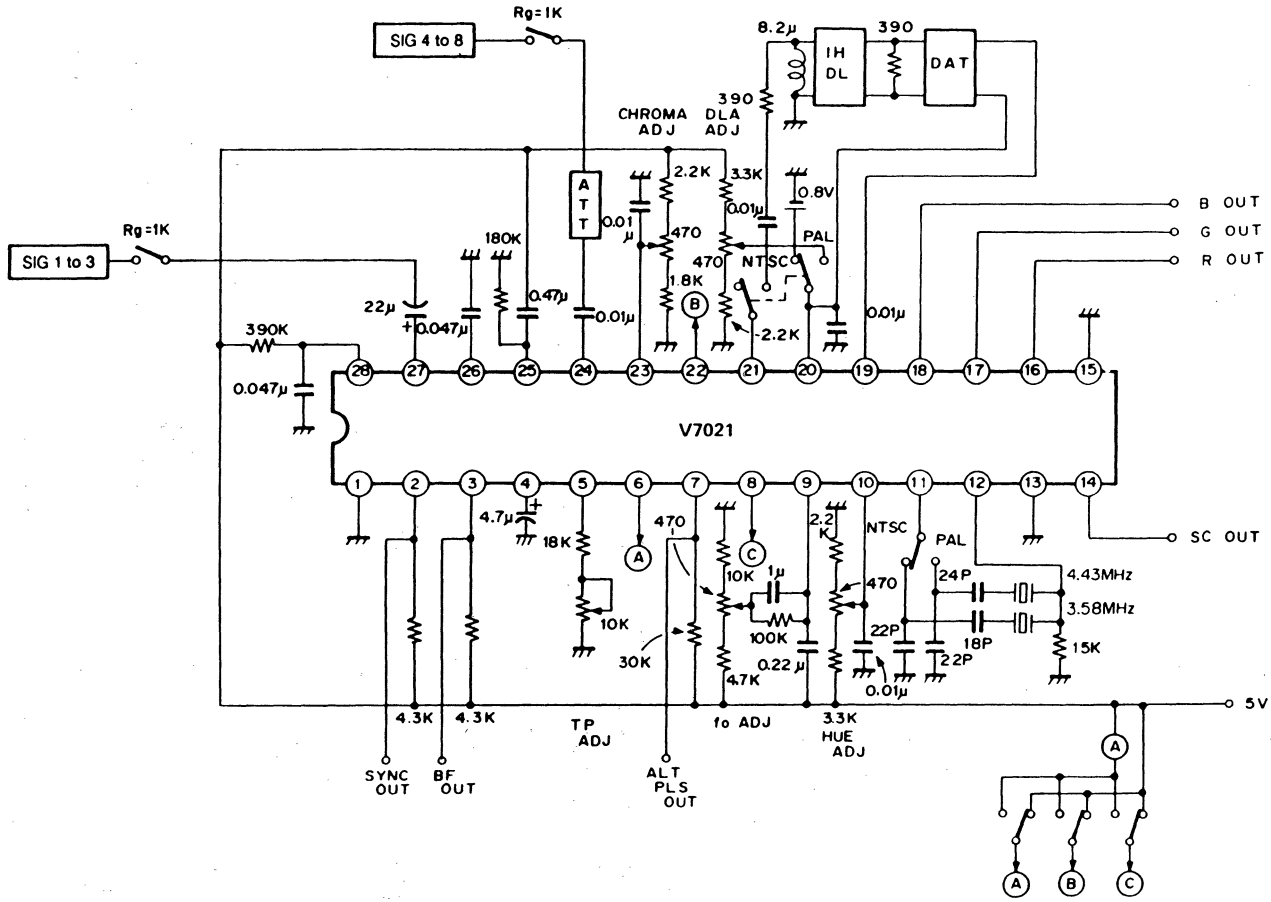
H SYNC



V SYNC



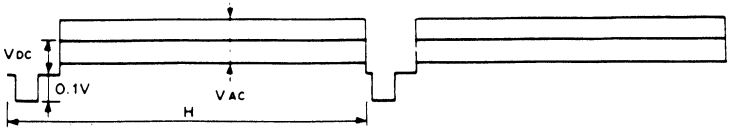
Electrical Characteristics Test Circuit



Input signal

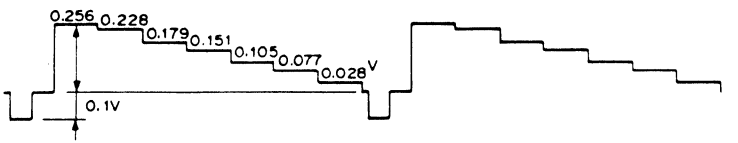
V

SIG 1



SIG 2

SIG 3

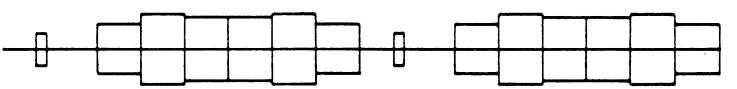


C

SIG 4

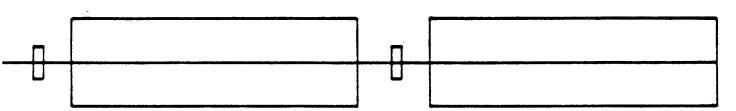
Sine wave Frequency 3.579545MHz
Amplitude 143mVp-p

SIG 5



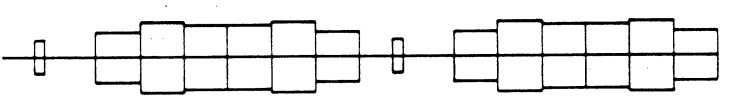
Amplitude	143	320	451	422	422	451	320	mVp-p
Phase	180	168	284	241	61	104	348	deg
Frequency		3.579545 MHz						

SIG 6



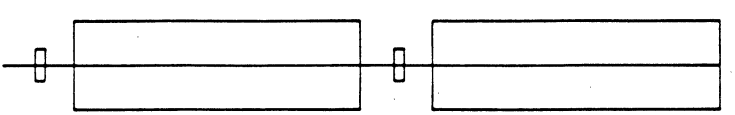
Amplitude	143	436	mVp-p
Phase	180	0	deg
Frequency		3.579545 MHz	±300 Hz

SIG 7



Amplitude	143	320	451	422	422	451	320	143	320	451	422	422	451	320	mVp-p
Phase	135	168	284	241	61	104	348	225	192	76	119	299	256	12	deg
Frequency		4.433619 MHz													

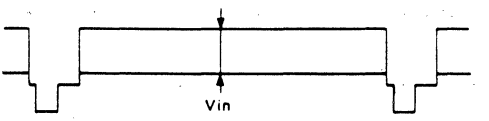
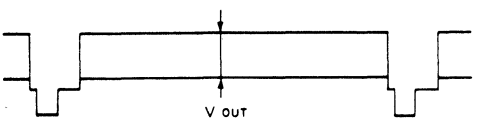
SIG 8



Amplitude	143	436	143	436	mVp-p
Phase	135	0	225	0	deg
Frequency		4.433619 MHz	±300 Hz		

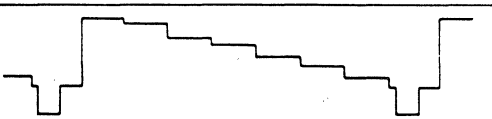
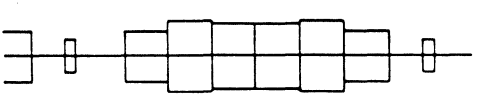
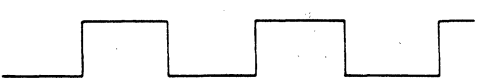
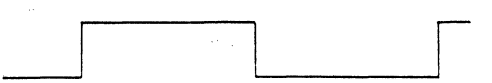
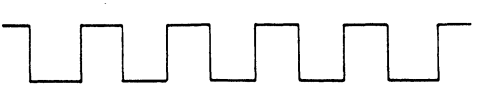
Test Method

1. Video amplifier voltage gain

Input waveform	VIDEO IN	
	CHROMA IN	Non-signal input
Output waveform	R G OUT B	

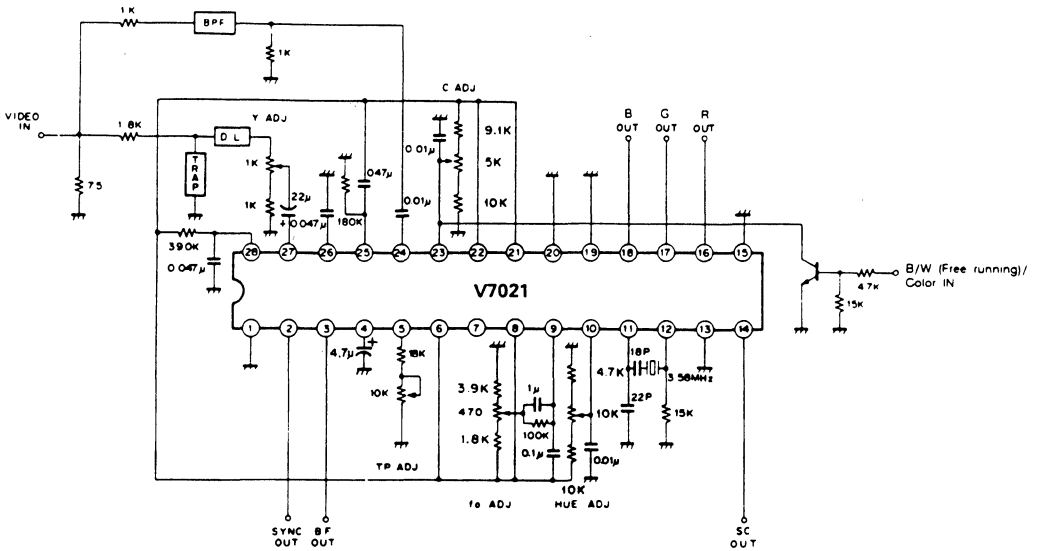
$$Gv = 20\log\frac{Vout}{Vin}\ (dB)$$

2. Original color output voltage

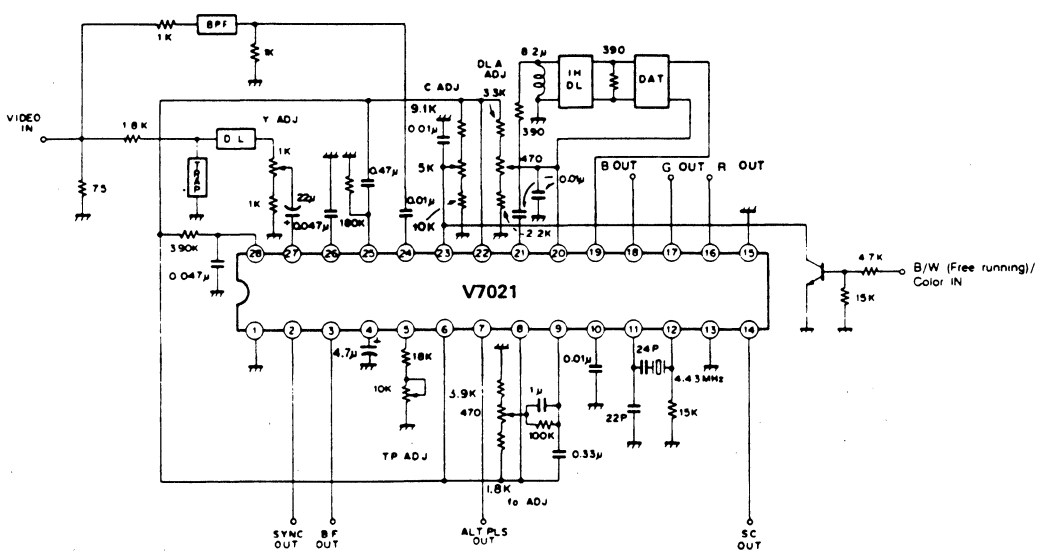
Input waveform	VIDEO IN	
	CHROMA IN	
Output waveform	R OUT	
	G OUT	
	B OUT	

Adjustment
1. Adjust HUE ADJ so that output B is the same amplitude.
2. Adjust CHROMA ADJ so that output B is 1Vp-p.

Application Circuit
(NTSC mode)

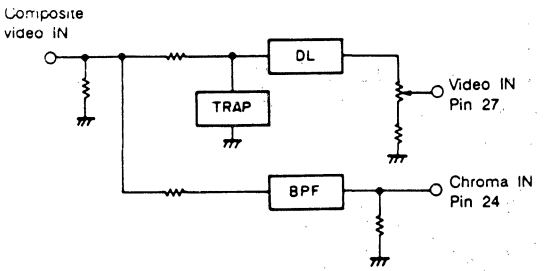


(PAL mode)



Applications

1. Input signals
   Composite video signal input is separated into video signal (Y) and chroma signal (C) by band-pass filter, trap and delay line, Y is input to pin 27 and C to pin 24. While composite video signal is input at 1Vp-p, the typical levels of the input signals are as shown in the table below.



Composite video input (Synchronous negative polarity)		1.0Vp-p
Video input	Luminance	0.256Vp-p
	Sync	0.103Vp-p
Chroma input	Burst	0.143Vp-p

2. Time pulse adjustment
   BF (Burst Flag) pulse positional adjustment can be performed by changing the current to be taken out from pin 5. Setting t_D (BF) at 5.6 µs by this adjustment results in that BF pulse width is set at approx. 2.4 µs and BLK (blanking) pulse width at 10 µs.

3. Monochrome (free-running) /color mode switching
   If pin 23 (CHROMA ADJ) is set to H (≧ 2.0V), the color mode is established. Input chroma signal will be decoded and output in the form of color difference signal. If pin 23 is set to L (≦ 0.8V), the monochrome (free-running) mode is established and the APC circuit is made to stop. As a result, VXO oscillates in the free-running mode.

4. NTSC/PAL mode switching
   Setting pin 20 (DL A BIAS) to H (≧ 2.0V), establishes the PAL mode, and setting the pin to L (≦ 0.8V).

5. Chroma output
   Chroma signal subjected to ACC and blanking is output at pin 21 (CHROMA OUT). Output amplitude is approx. 160mVp-p with typical input (75% color bar).
   In the PAL mode, this output is to be input to 1 H DL. In the NTSC mode, connect pin 21 to the power supply (Vcc).

6. DL (Delay Line) AMP
   An amplifier for insertion of 1 H DL and matching loss compensation when in the PAL mode. Its gain is variable within 14 ± 4dB to absorb DL dispersion.
   Its input pin is pin 19 (DL A IN) ; apply to this pin a bias voltage of the same potential as with pin 20 (DL A BIAS). The signal having passed through 1 H DL is to be input to pin 19 after adjusted at the delay adjusting transformer (DAT) so that the delay time is 1 H (64 µs).

   In the NTSC mode, this amplifier is not used ; set the levels of pins 19 and 20 at L (≦ 0.8V).

7. VXO, APC
   Pin 9 (APC TC) is the APC time constant pin. When APC circuit is not active in PC mode, free run frequency is determined by means of the DC voltage of this pin to compensate the free run frequency temperature characteristics execute temperature compensation as in the example for application circuits. VXO can be used to handle NTSC and PAL by changing the crystal oscillator and the linear capacitance.

8. Order of adjustment
   Input signal 100% Color bar
   [NTSC mode]
   1) BF (burst flag) position adjustment
      Adjusting the resistance between pin 5 and the ground, BF position is rendered $t_D = 5.6$ µs.
   2) Adjustment of video amplifier level
      Adjust YADJ with RGB output, so that white peak (100% white) becomes 1.0Vp-p.
   3) f_0 adjustment
      Adjustment f_0 ADJ, so that in PC mode oscillating frequency (subcarrier output) becomes fsc.
   4) HUE adjustment
      Adjust HUE ADJ so that in S1 mode, the amplitude be the same for the respective colors from B output amplitude.
   5) Chroma level adjustment
      Adjust C ADJ so that the respective colours of B output amplitude, become 0.75Vp-p.

   [PAL mode]
   1) BF position adjustment
   2) Adjustment of video amplifier level
   3) f_0 adjustment.

   } The same as for NTSC

   4) DL amplifier adjustment.
      Adjust DLA ADJ so that in SI mode, the R output amplitude former and latter parts, in H section, be equal.
   5) Chroma level adjustment
      Adjust C ADJ so that the respective colors from B output amplitude, become 0.75Vp-p.

Operation

1. Sync separation system
   The sync separation system clamps the sync tip of the video signal having been input from pin 27 to separate the sync signal from the input video signal. Sync pulses are then processed to form BF, H, and BLK pulses, which are supplied to subsequent circuits. Of these pulses, sync and BF pulses are output at pins 2 and 3, respectively, after transformed to TTL level via buffer.

2. Luminance signal regeneration system
   Video signal input from pin 27 has its pedestal clamped, and amplified by the Y amplifier.

3. ACC system
   The burst component of the chroma signal having been input from pin 24 is detected at ACC DET. Feedback to ACC AMP occurs depending on the detected output so that the burst level is kept constant.

4. APC system
   After the signal level is brought to the fixed value at ACC AMP, the burst component alone goes into the APC circuit via the BURST GATE circuit. Meanwhile, a 0° carrier and a 90° carrier are formed from VXO output, and the 90° carrier goes into APC via the HUE circuit. At APC, phase comparison is carried out between the 90° carrier and the input burst, and feedback to VXO is performed so that the phase difference is 90°. The 0° and 90° carriers thus formed are supplied to B-Y DEM and R-Y DEM, respectively. Therefore, demodulation axis can be changed by rotating the phase of the 90° carrier at the HUE circuit.

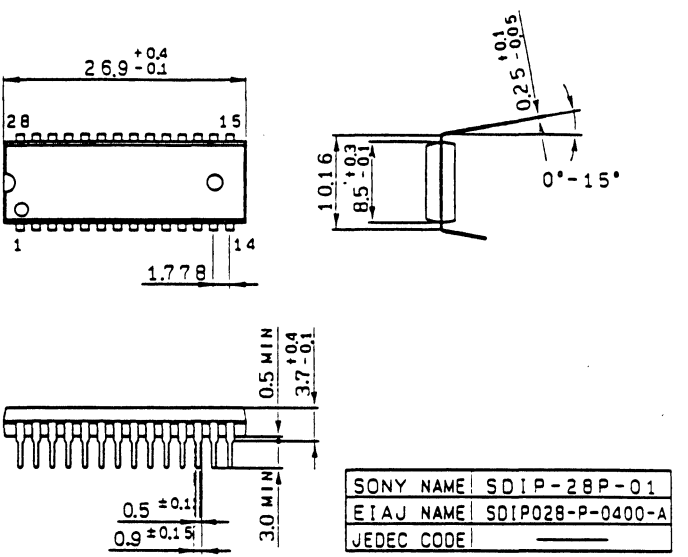
5. Color signal regeneration system
   1) NTSC system
      The chroma signal amplified at ACC AMP is amplified again at CHROMA AMP, then demodulated at B-Y DEM and R-Y DEM, and output at pins 16 and 17 in the form of color difference signal.

   2) PAL system
      Processing is the same as with the NTSC system up to CHROMA AMP.
      The chroma signal output at pin 21 goes into DL AMP at pin 19 via 1 H DL and DAT, and then input to the ADD/SUB circuit after level-controlled. At the ADD/SUB circuit, the signal is subjected to addition and subtraction with respect to the original signal. The signals obtained by addition and subtraction are input to B-Y DEM and R-Y DEM, and demodulated by the 0° carrier and the 90° carrier inverted every H. After that, the signal is output in the form of color difference signal as with the NTSC system.

6. PAL ID
   The PAL signal is transmitted with its R-Y component inverted every H. It is therefore necessary to inverse the demodulation axis every H. In this IC, the 90° carrier is inverted in synchronization with H BLK pulses, and checking for correspondence with the input burst is performed by synchronous detection. If an error is detected, feedback to FF (Flip Flop) is performed for correction.

Package Outline Unit : mm

28pin SDIP (Plastic) 400mil 1.7g



SONY NAME	SDIP-28P-01
EIAJ NAME	SDIP028-P-0400-A
JEDEC CODE	———

SONY CXA1145P/M

RGB Encoder

Description

The CXA1145P/M encoder converts an analog RGB signal to a composite video signal.

With its built-in circuit various pulses required for an encoder, composite video outputs are obtained just by inputting the composite sync and analog RGB signal.

Features

- Single power supply 5 V
- Low power consumption (110 mW)
- Compatible both with NTSC and PAL systems
- Built-in 75Ω driver (RGB output, composite video output, composite sync output)
- Built-in oscillator for subcarrier
- External input of subcarrier is also possible.
- Built-in audió buffer circuit

Functions

- MTX circuit
- R-Y, B-Y MOD circuit
- Y/C MIX circuit
- 75Ω driver for RGB, composite video and composite sync outputs
- PAL ALT circuit
- BF generator
- Half H killer circuit
- Subcarrier oscillator
- Audio buffer circuit

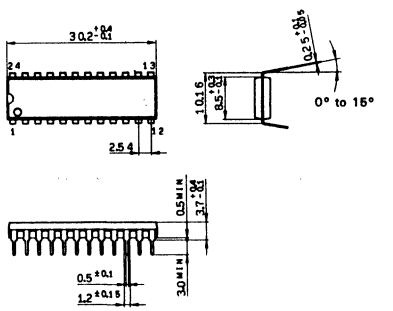
Structure

Bipolar silicon monolithic IC

Package Outline

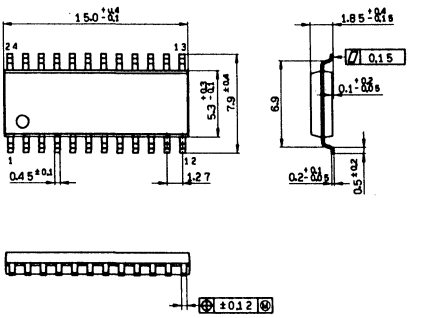
Unit: mm

CXA1145P 24 pin DIP



DIP-24P-01

CXA1145M 24 pin SOP



SOP-24P-L01

Absolute Maximum Ratings (Ta = 25°C)

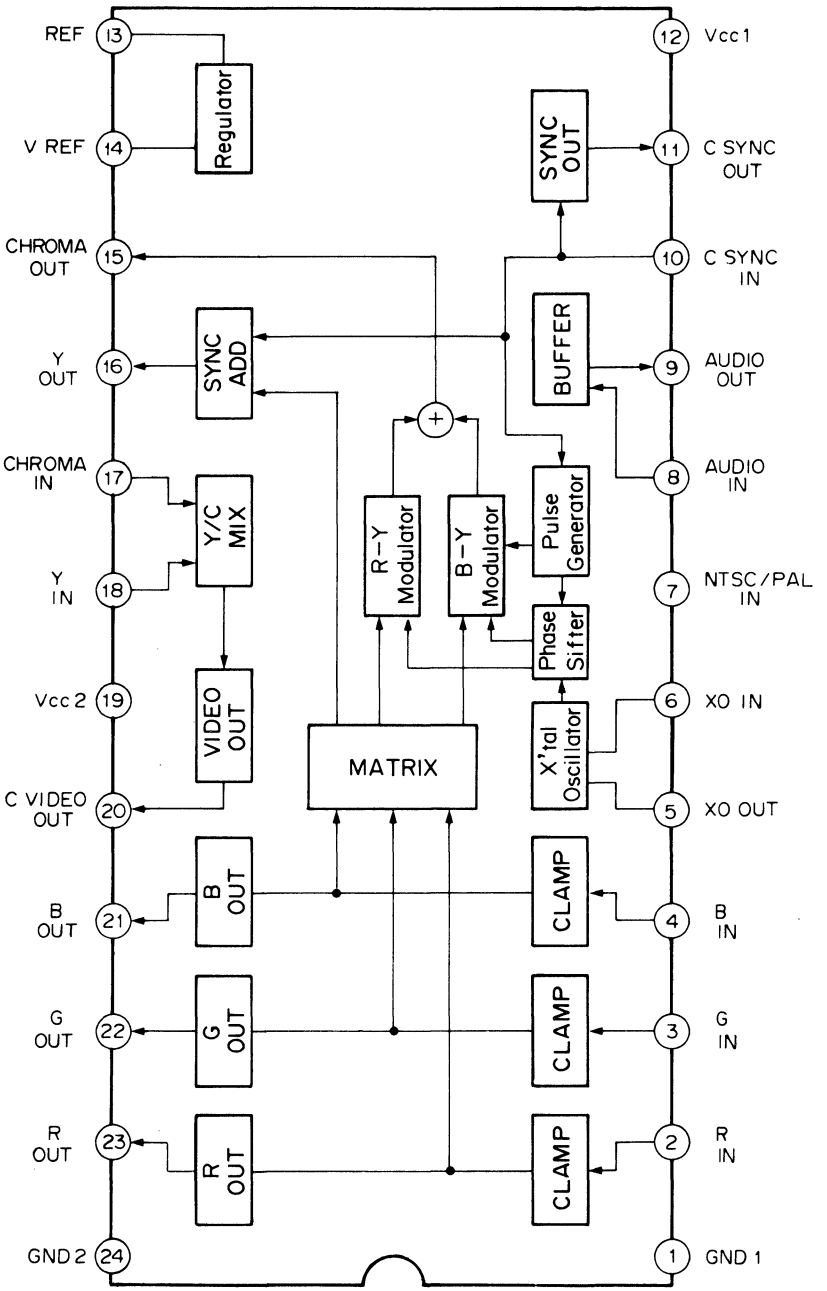
• Supply voltage	Vcc	10	V	
• Operating temperature	Topr	−20 to +75	°C	
• Storage temperature	Tstg	−55 to +150	°C	
• Allowable power dissipation	PD	1250	mW	(CXA1145P)
		780	mW	(CXA1145M)

Recommended Operating Condition

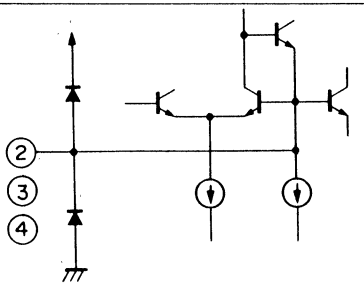
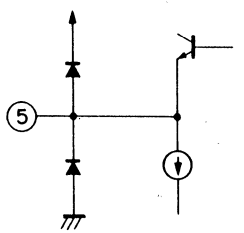
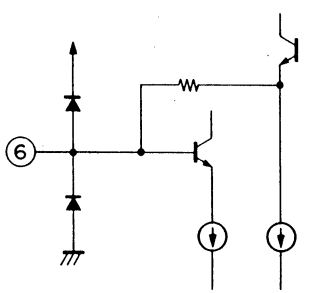
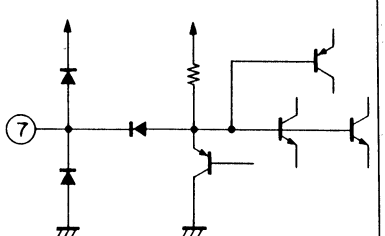
• Supply voltage	Vcc	5±0.25	V

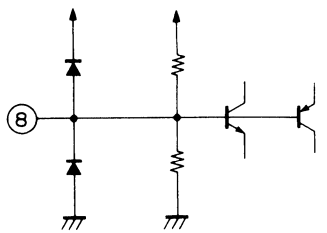
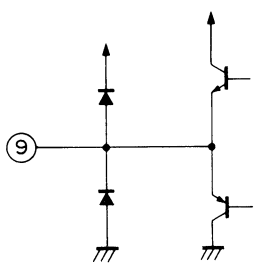
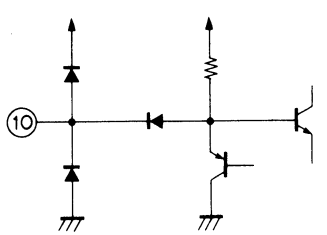
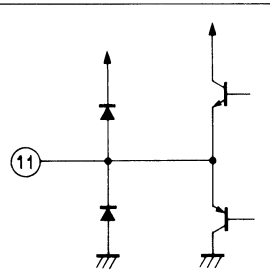
70945-TO

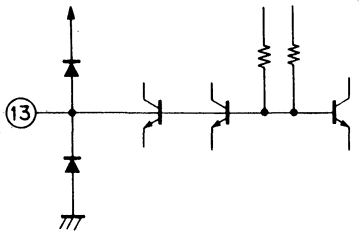
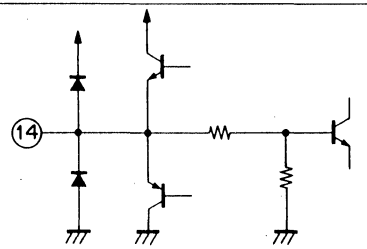
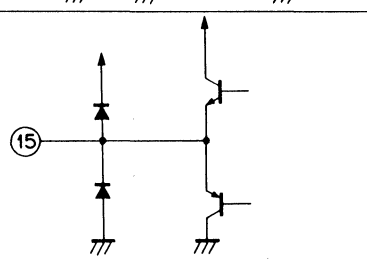
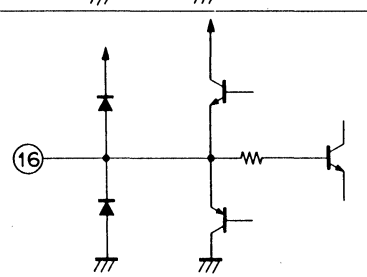
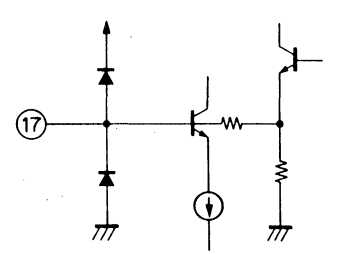
Block Diagram and Pin Configuration

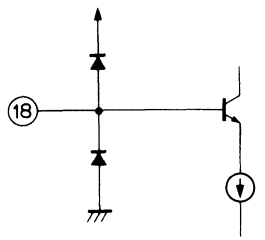
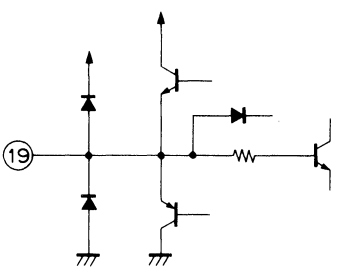
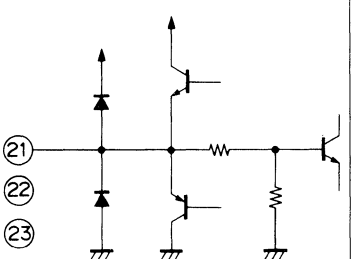


Pin Description

No.	Symbol	Equivalent circuit	Description
1	GND 1		GND pin for circuits other than outputs of RGB and composite video. Connect with GND 2 using an impedance as low as possible.
2 3 4	R IN G IN B IN		Input pin for the analog RGB signal. Input with 100% = 1 Vp-p. It is necessary to input with an impedance as low as possible to minimize the clamp error allowance.
5	XO OUT		Pin for the x'tal OSC. For inner oscillation, a crystal oscillator is connected. For external oscillation, input to pin 6 XO IN through a coupling capacitor. Input with the sub-carrier input level at 400 mVp-p to 1,000 mVp-p. For external oscillation, input a sine wave with enough less distortion. With much distortion, the chroma signal's phase property may deteriorate.
6	XO IN		
7	NTSC/PAL IN		Switching pin between NTSC and PAL mode. Vcc NTSC GND PAL

No.	Symbol	Equivalent circuit	Description
8	AUDIO IN		Input pin for the audio buffer circuit. The input impedance is about 25 kΩ
9	AUIO OUT		Output pin for the audio buffer circuit.
10	C SYNC IN		Input pin for the composite sync signal. Input with the TTL level. L (≦ 0.8 V): Sync. H (≧ 2.0 V)
11	C SYNC OUT		Output pin for the composite sync signal. Capable of driving a 75Ω load direct.
12	Vcc 1		Power supply pin for circuits other than RGB and composite video output circuits.

No.	Symbol	Equivalent circuit	Description
13	I REF		Pin to determine the inner reference current. Connect to GND via a 27 kΩ resistor.
14	V REF		Pin for the inner reference voltage. Connect to GND with 10 μF.
15	C OUT		Chroma signal output pin. Connect a Band Pass Filter (BPF) between this pin and pin 17 (C IN).
16	Y OUT		Y signal output pin. Connect a delay line between this pin and pin 18 (Y IN).
17	C IN		Input pin for the chroma signal without harmonic distortion after BPF.

No.	Symbol	Equivalent circuit	Description
18	Y IN		Input pin for the Y signal with delay after the delay line.
19	Vcc2		Power supply pin for RGB and composite video output circuits. Decouple with a large-enough capacity as a massive current flows.
20	C V OUT		Output pin for the Y/C MIX circuit. The composite video signal is output. This output can drive a 75Ω load direct.
21 22 23	B OUT G OUT R OUT		Output pin for the analog RGB signal. Capable of driving a 75Ω load drive.
24	GND2		GND pin for RGB and composite output circuits. Connect with GND 1 using low impedance as possible.

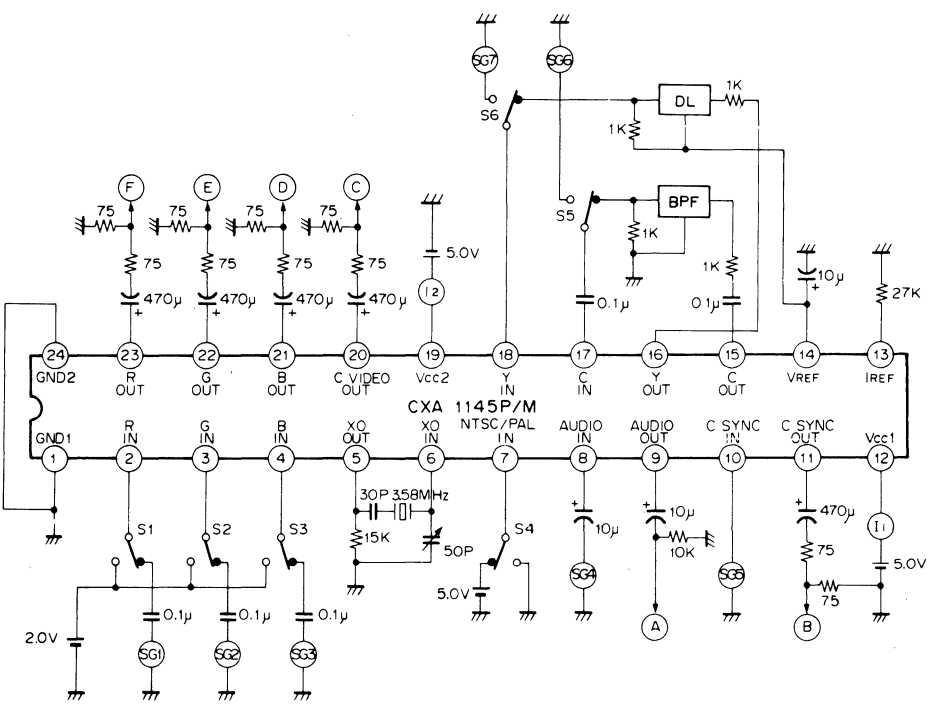
Electrical Characteristics

Ta = 25°C, Vcc = 5V, See the Electrical Characteristics Test Circuit

Item			Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
Consumption current 1			Icc1	S1 S2 S3 ON	I1	15.0	19.5	27.9	mA
Consumption current 2			Icc2	SG5 DC = 2. 0V	I2	6.3	8.2	11.7	mA
RGB output voltage			Vo(R)	RIN = 1Vp-p, f = 200 kHz, Fig. 1	F	0.64	0.71	0.78	Vp-p
			Vo(G)	GIN = 1Vp-p, f = 200kHz, Fig. 1	E				
			Vo(B)	BIN = 1Vp-p, f = 200kHz, Fig. 1	D				
RGB output frequency response			fc(R)	Frequency when an output becomes −3 dB with the output of f = 200 kHz in Fig. 1 set to 0 dB.	F	5.0			MHz
			fc(G)		E				
			fc(B)		D				
Composite video output: Sync level			Vo (CS)	S6 ON, Fig. 2	C	0.26	0.29	0.33	Vp-p
R 100%: Y level			Vo (YR)	S1 S6 ON, Fig. 2	C	0.189	0.21	0.245	V
G 100%: Y level			Vo (YG)	S2 S6 ON, Fig. 2	C	0.378	0.42	0.482	V
B 100%: Y level			Vo (YB)	S3 S6 ON, Fig. 2	C	0.072	0.08	0.092	V
White 100%: Y level			Vo (YW)	S1 S2 S3 S6 ON, Fig. 2	C	0.64	0.71	0.82	V
MIX AMP	Voltage gain	Y	Gv(Y)	S6 ON, Fig. 3	C	9	10	11	dB
		C	Gv(C)	S5 ON, Fig. 3	C				
	Frequency response	Y	fc(Y)	S6 ON, Fig. 3	C	5.0			MHz
		C	fc(C)	S5 ON, Fig. 3	C				
	Differential gain		DG	S5 S6 ON, Fig. 4	C			3.0	%
	Differential phase		DP	S5 S6 ON, Fig. 4	C			3.0	deg
Burst level			Vo (BN)	Fig. 5	C	0.26	0.29	0.32	Vp-p
R chroma ratio			R/BN	Level ratio between R and burst in Fig. 5	C	2.84	3.16	3.48	
R phase			θR	R phase in Fig. 5	C	94	104	114	deg
G chroma ratio			G/BN	Level ratio between G and burst in Fig. 5	C	2.65	2.95	3.25	
G phase			θG	G phase in Fig. 5	C	231	241	251	deg
B chroma ratio			B/BN	Level ratio between B and burst in Fig. 5	C	2.01	2.24	2.47	
B phase			θB	B phase in Fig. 5	C	337	347	357	deg
PAL burst level ratio			K(BP)	Burst level ratio between S4 ON, PAL and PAL in Fig. 5	C	0.9	1.0	1.1	

Item		Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
PAL burst phase		θ_{PAL}	Burst phase of S4 ON, PAL in Fig. 5	C	125	135	145	deg
		$\theta_{\overline{PAL}}$	Burst phase of S4 ON, $\overline{PAL}$ in Fig. 5	C	215	225	235	
Burst width		tW(B)	Fig. 5	C	2.5	2.75	3.6	μS
Burst position		tD(B)	Fig. 5	C	0.45	0.5	0.75	μS
Carrier leakage		VL	Fig. 5	C			20	mVp-p
Composite sync output voltage		VD(S)	Fig. 7	B	0.2	0.29	0.4	Vp-p
Audio buffer	Voltage gain	Gv(A)	VIN = 1.0Vp-p, f = 1kHz, Fig. 6	A	−1.0	0	1.0	dB
	Frequency response	fc(A)	Frequency when an output becomes −3 dB with the output of f = 1 kHz in Fig. 6 set to 0 dB.		30			kHz
	Distortion factor	THD	VIN = 1.0Vp-p, f = 1kHz, Fig. 6				1.0	%

Electrical Characteristics Test Circuit



Test Signal

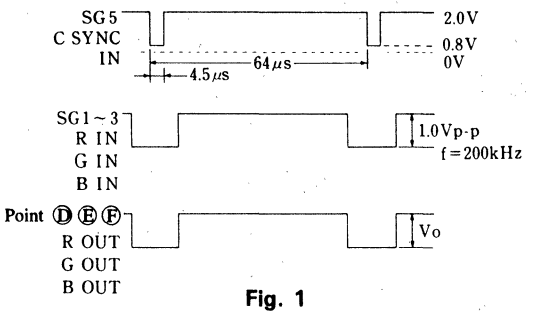


Fig. 1

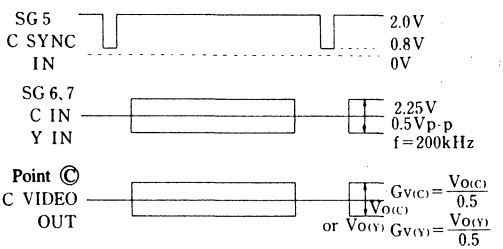


Fig. 3

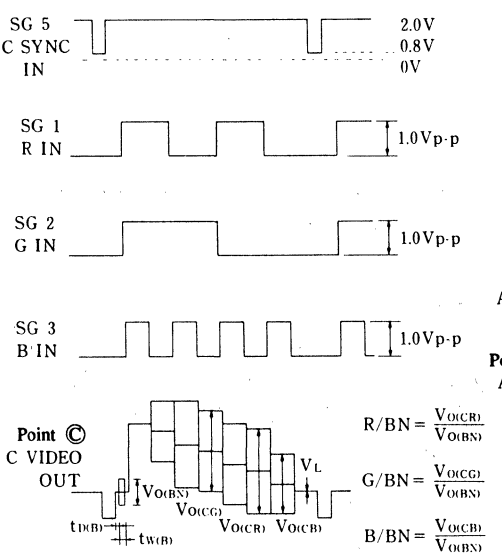


Fig. 5

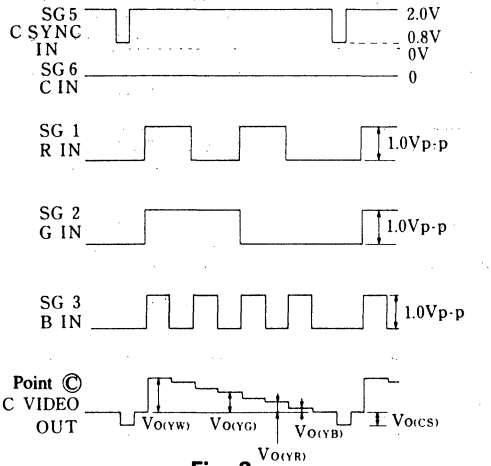
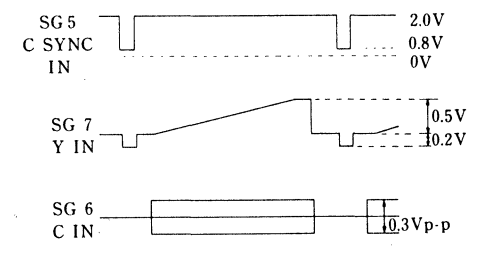


Fig. 2



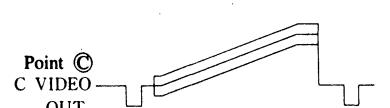


Fig. 4

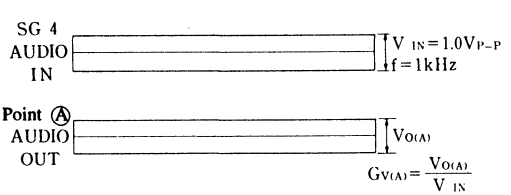


Fig. 6

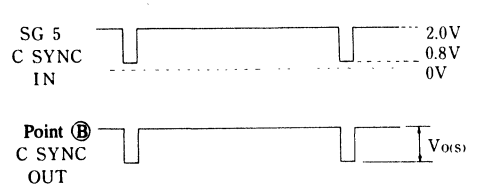
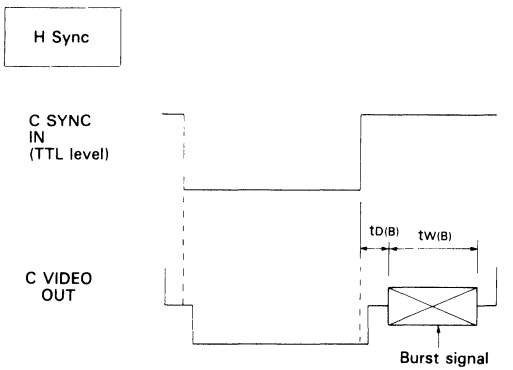
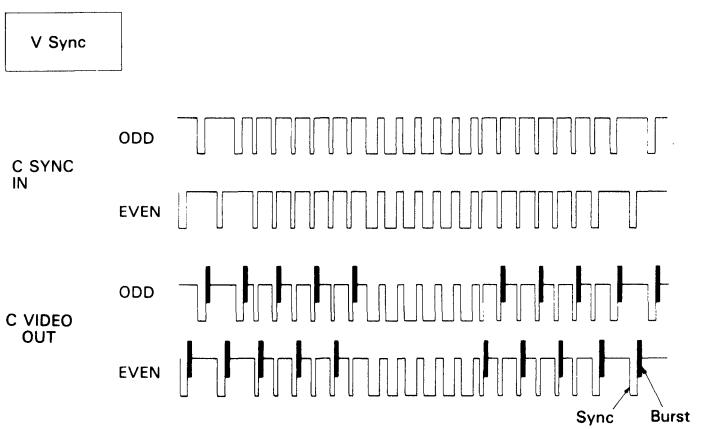


Fig. 7

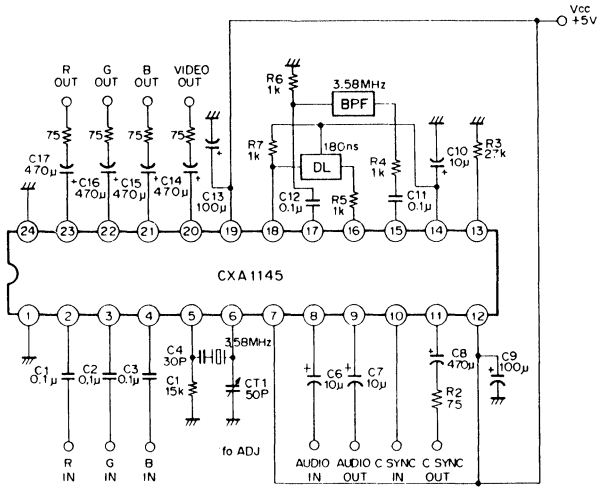
Burst Signal

CXA1145P/M generates the burst signal in the timings below following an input composite sync.



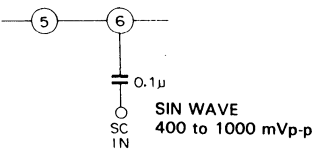


Application Circuit (NTSC mode)



<How to supply subcarrier externally>

When a subcarrier is added externally, this section will be as follows:



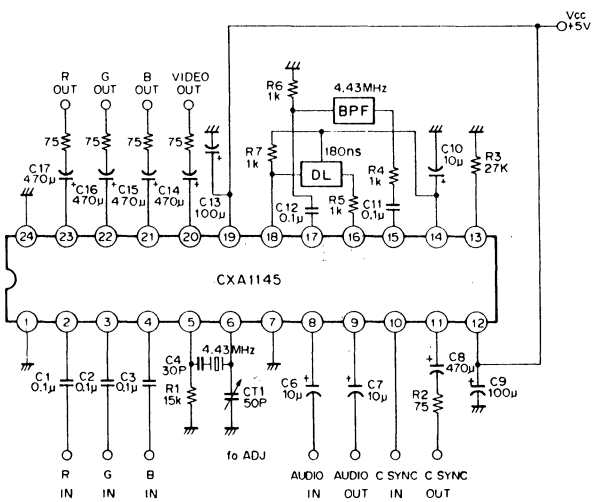
<How to adjust the oscillation level>

Regulating the trimmer capacitor, set XO out level between 400 to 1000 mVp-p.

* Metal film resistor ±1%

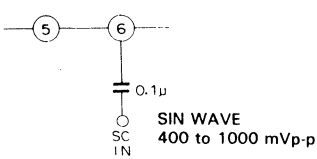
BPF: Toko H287BSJS-3108HWD
DL: Matsushita ELB-5F020N

Application Circuit (PAL mode)



<How to ...>

When a subcarrier is added externally, this section will be as follows:



<How to adjust the oscillation level>

Regulating the timmer capacitor, set XO out level between 400 to 1000 mVp-p.

* Metal film resistor ±1%

BPF: Toko H287BSJS-3108HWD
DL: Matsushita ELB-5F020N

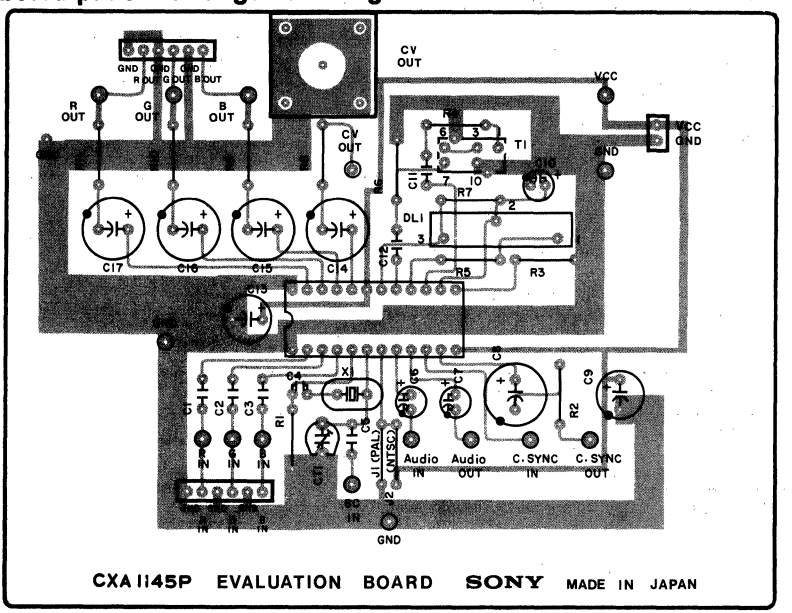
<How to set to NTSC/PAL modes>

To set to NTSC/PAL modes, connect CXA1145P's pin 7 to 9 either Vcc (supply pin) or GND. Connection to Vcc produces NTSC mode, and to GND PAL mode. This is executed by connecting the jumper line of the desired mode on the evaluation board.

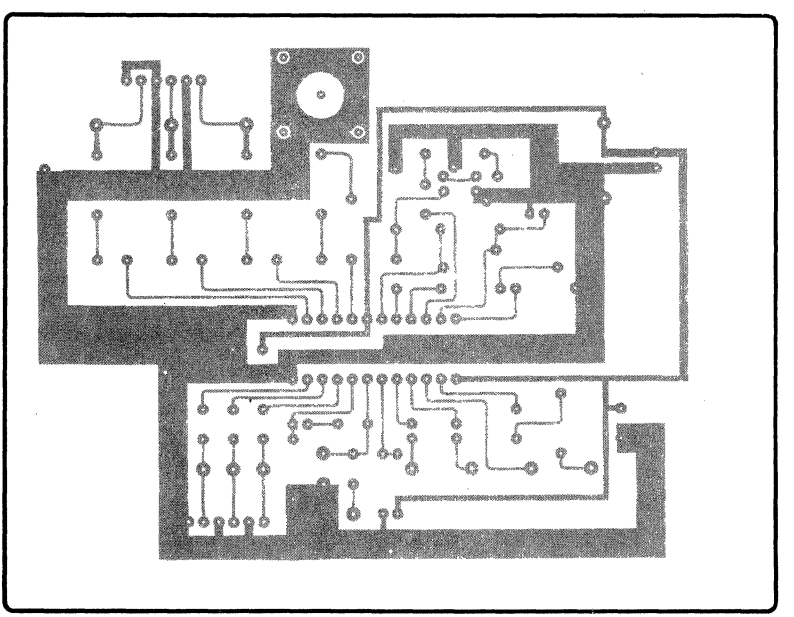
CXA1145P Evaluation Board Pins Description

Symbol	Description
R IN G IN B IN	Input pin of the analog RGB signal
SC IN	Pin for the external sypply of the subcarrier. For the connection in this case. See the subcarrier external supplying method. SC_{IN} = 400 mVp-p to 1000 mVp-p
AUDIO IN	Input pin of the audio buffer amplifier
AUDIO OUT	Output pin of the audio buffer amplifier
C SYNC IN	Input pin of the composite sync signal C $SYNC_{IN}$ = TTL level ($L \leq 0.8V$, $H \geq 2.0V$)
C SYNC OUT	Output pin of the composite sync signal
R OUT G OUT B OUT	Output pin of the analog RGM signal
VIDEO OUT	Output pin of the composite video signal
Vcc	Supply Vcc = 5V
GND	GND pin

Evaluation PC board pattern arrangement diagram

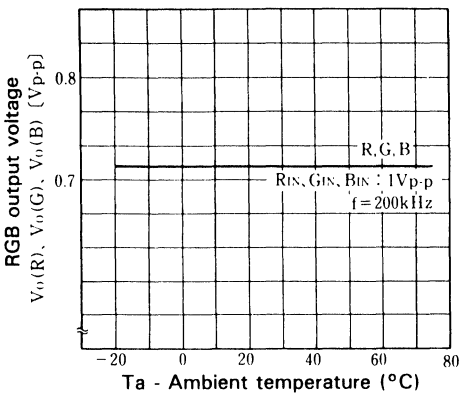


Parts arrangement diagram (parts side)

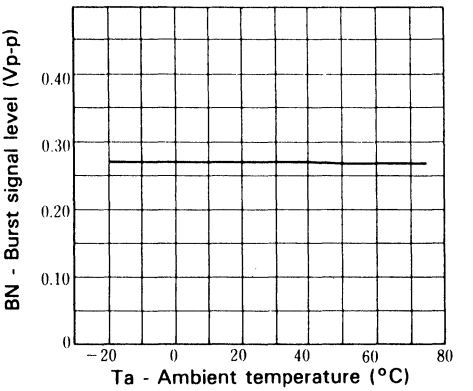


Pattern diagram (reverse side)

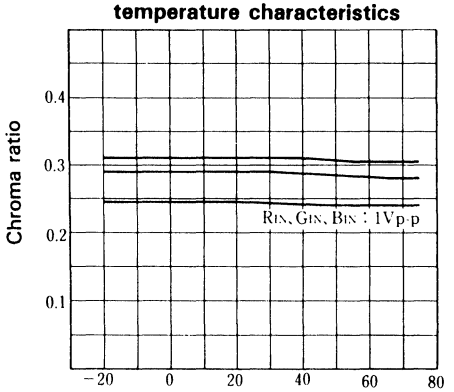
RGB output voltage temperature characteristics



Burst signal level temperature characteristics

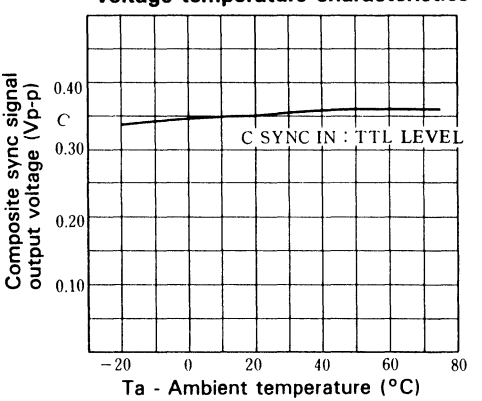


Chrome ratio temperature characteristics

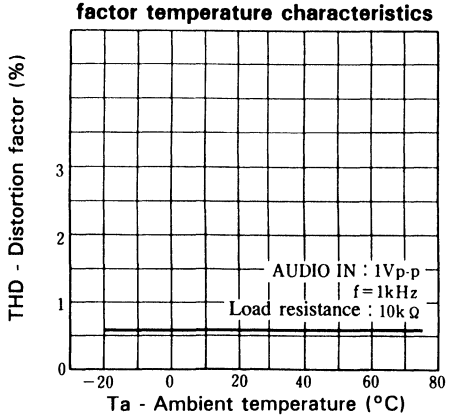


$$B/BN = \frac{Vo(CB)}{Vo(BN)} \quad R/BN = \frac{Vo(CR)}{Vo(BN)} \quad G/BN = \frac{Vo(CG)}{Vo(BN)}$$

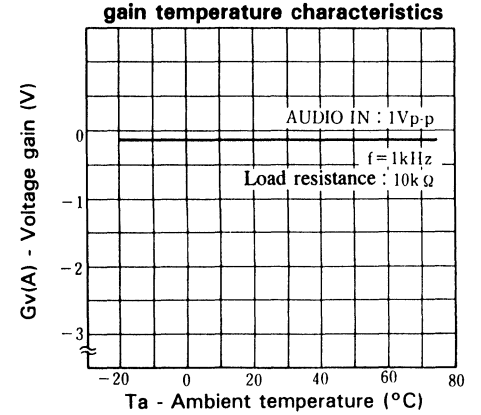
Composite sync signal output voltage temperature characteristics



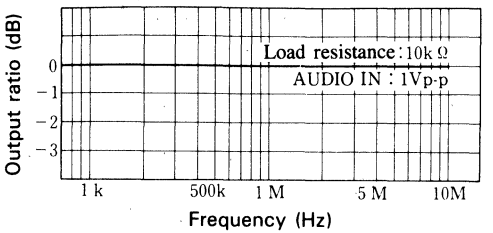
Audio buffer amplifier distortion factor temperature characteristics



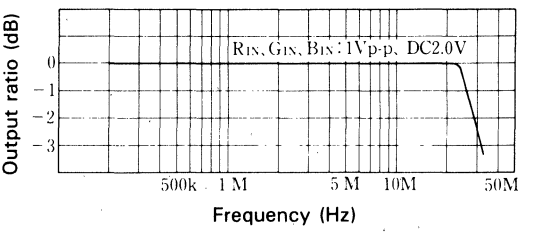
Audio buffer amplifier voltage gain temperature characteristics



Audio buffer amplifier frequency characteristics



RGB output frequency characteristics



Note) For details refer to the test signals in the Electrical Characteristics Test Circuits.

NTSC/PAL Encoder

Description

CXA1219P/M and CXA1229P/M are encoder ICs used to convert Y, R–Y, B–Y signals into composite video or RGB signals.

The composite sync can be separated from the incoming luminous of the signal, as well as the external sync.

With a ratio of R–Y : B–Y = 1.4 : 1 CXA1219P/M is ideally suited for still video floppy usage.
CXA1229P/M R–Y : B–Y = 1 : 1.27

Features

- Single power supply 5V
- Low power consumption (130 mW)
- Compatible with both NTSC and PAL mode
- Built-in 75 Ω driver (RGB output, composite video output, composite sync output)
- Built-in crystal oscillator for subcarrier
- External subcarrier input possible
- Audio buffer

Function

- Matrix circuit
- R–Y, B–Y modulator circuit
- Y/C mixer circuit
- 75 Ω driver for RGB, composite video and composite sync output.
- PAL alternate circuit
- Burst flag generator
- Half H killer circuit
- Oscillator for subcarrier
- Buffer amplifier circuit for audio's

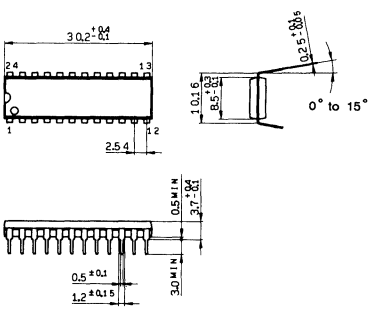
Structure

Bipolar silicon monolithic IC

Package Outline

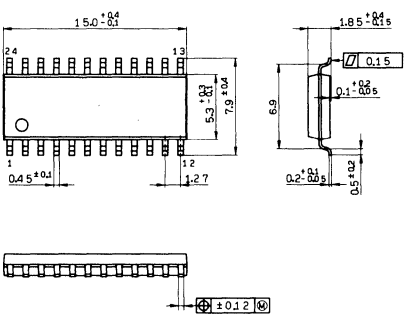
Unit: mm

CXA1219P 24 pin DIP (Plastic)
CXA1229P



DIP-24P-01

CXA1219M 24 pin SOP (Plastic)
CXA1229M



SOP-24P-L01

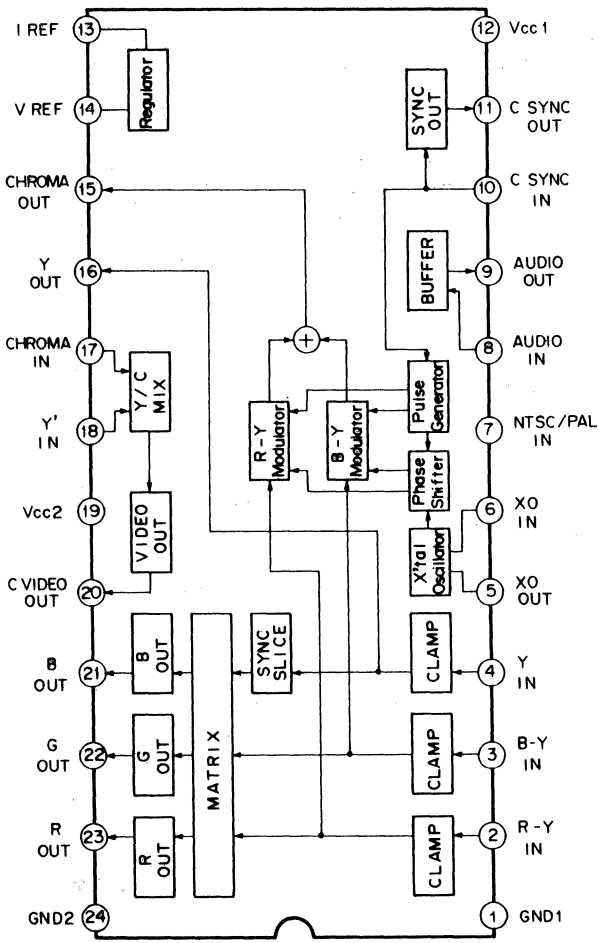
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc		10		V	
• Operating temperature	Topr	−20	to	+75	°C	
• Storage temperature	Tstg	−55	to	+150	°C	
• Allowable power dissipation	PD		1,250		mW	(CXA1219P, CXA1229P)
			780		mW	(CXA1219M, CXA1229M)

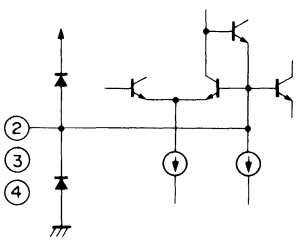
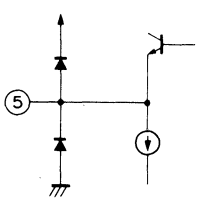
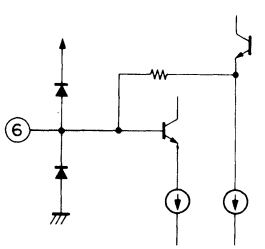
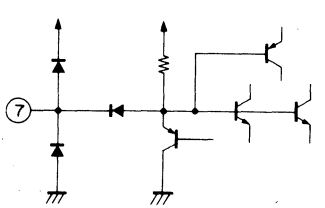
Recommended Operating Condition (Ta = 25°C)

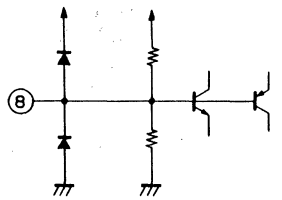
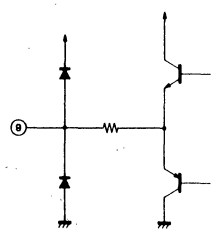
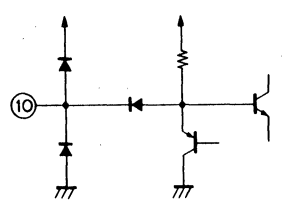
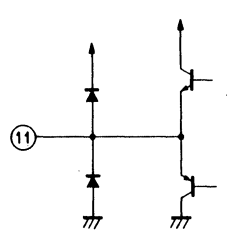
• Supply voltage	Vcc	5	±	0.25	V

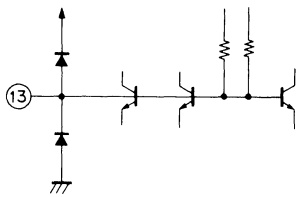
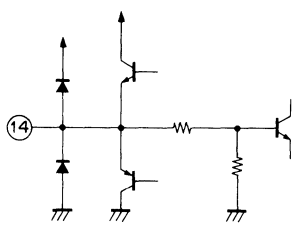
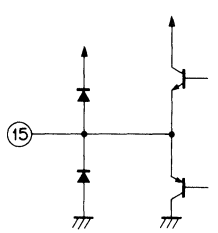
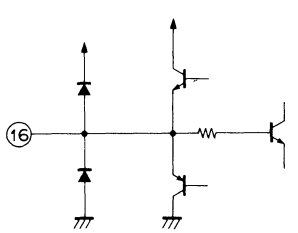
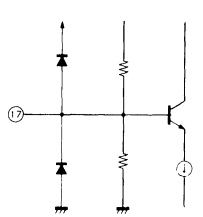
Block Diagram and Pin Configuration (Top View)

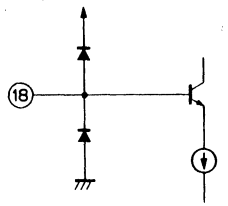
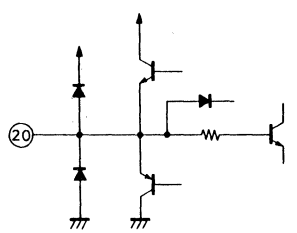
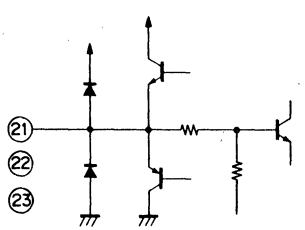


Pin Description and Equivalent Circuit

No.	Symbol	Equivalent Circuit	Description
1	GND 1		Ground pin for the circuits other than the RGB output and composite video output circuits. Must be connected to GND2 at as low impedance as possible.
2 3 4	R–Y IN B–Y IN Y IN		Input pins for Y and color difference signals. With CXA1219P/M, input requirements are: R–Y = 1.4 Vp-p, B–Y = 1 Vp-p, Y = 1 Vp-p. With CXA1229P/M, input requirements are: R–Y = 1 Vp-p, B–Y = 1.27 Vp-p, Y = 1 Vp-p. Y must be 1 Vp-p (with SET UP, SYNC). To minimize clamp error, input impedance must be as low as possible.
5	XO OUT		Pin for crystal oscillator. For internal oscillation, connect a crystal oscillator to this pin. For external oscillation, the signal must be input to pin 6 (XO IN) via coupling capacitor. Subcarrier input level must be 400 mVp-p to 1,000 mVp-p. For external oscillation, it is necessary to input sine waves of sufficiently low distortion. (High distortion may degrade the phase characteristics of chrominance signal.)
6	XO IN		
7	NTSC/PAL IN		Switching pin of NTSC and PAL mode. Vcc NTSC GND PAL

No.	Symbol	Equivalent Circuit	Description
8	AUDIO IN		Input pin of the audio buffer amplifier circuit. Input impedance about 25 kΩ.
9	AUDIO OUT		Output pin of the audio buffer amplifier circuit.
10	C SYNC IN		Input pin at the composite sync signal. Input at TTL level. "L" (≤0.8 V) Time: SYNC "H" (≥2.0 V)
11	C SYNC OUT		Output pin at the composite sync signal. Can drive directly a load of 75Ω.
12	Vcc1		Supply pin for the circuit other than the RGB output and composite video output circuits.

No.	Symbol	Equivalent Circuit	Description
13	IREF		Pin that determines internal reference current. Connect to GND through 27 kΩ.
14	VREF		Internal reference voltage pin. Ground with a capacitor about 10 μF.
15	C OUT		Chroma signal output pin. Connect BPF (Band Pass Filter) to pin 17 (CIN).
16	Y OUT		Y signal output pin. Connect DL (Delay Line) between pins 16 and 18.
17	C IN		Input a chroma signal excluded a high frequency at the BPF (Band Path Filter).

No.	Symbol	Equivalent Circuit	Description
18	Y' IN		Input Y signal delayed at DL (Delay Line).
19	VCC 2		Supply pin for the RGB output and composite video output circuits. Decoupling by a capacitor of sufficiently large capacity is needed because high current is to flow across this pin.
20	C VIDEO OUT		Output pin for the Y/C MIX circuit. Composite video signal is output. Can drive directly a load of 75Ω.
21 22 23	B OUT G OUT R OUT		Output pin at the analog RGB signal. Can drive directly a load of 75Ω.
24	GND2		Ground pin for the RGB output and composite video output circuits. Must be connected to GND1 at as low impedance as possible.

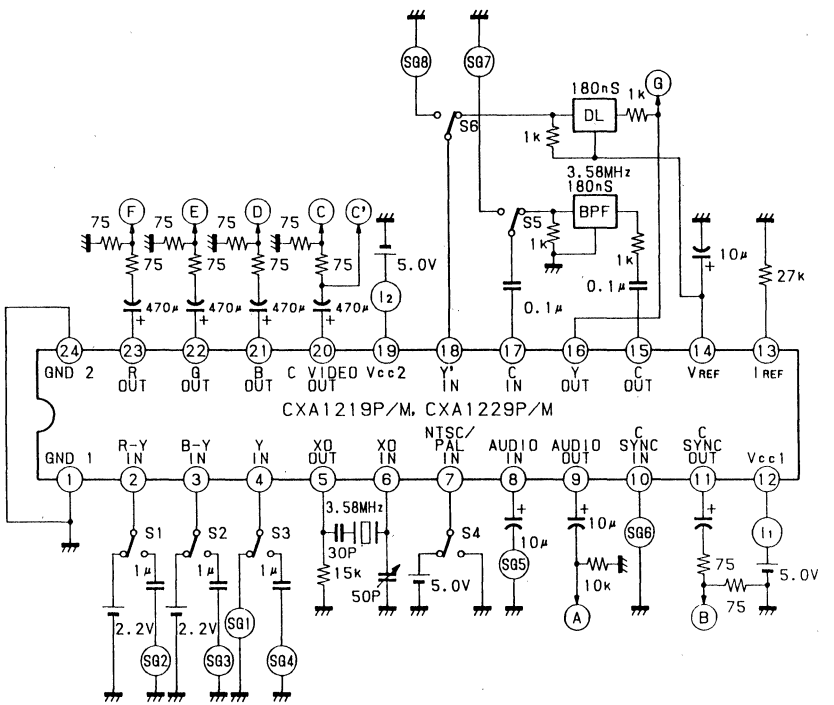
Electrical Characteristics

(See the Electrical Characteristics Test Circuit.)
Ta = 25°C, Vcc = 5V

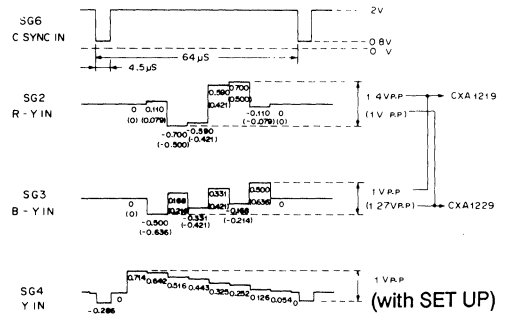
Test item			Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
Supply current 1			Icc1	SG1 DC=2.2V	I1	12.5	18.0	23.5	mA
Supply current 2			Icc2	SG6 DC=2V	I2	5.0	7.6	10.0	mA
RGB output voltage			Vo(R)	Fig. 1 S1 S2 S3 ON	F	0.65	0.71	0.78	Vp-p
			Vo(G)		E				
			Vo(B)		D				
RGB output frequency characteristics			fc(R)	Fig. 2 Frequency of −3dB with f=200 kHz output taken as 0 dB.	F	5			MHz
			fc(G)		E				
			fc(B)		D				
Y OUT	Voltage gain		Gv(Yo)	Fig. 3	G	−0.5	0	0.5	dB
Y OUT	Frequency characteristics		fc(Yo)	Frequency of −3dB with f=200kHz output taken as 0 dB.	G	5			MHz
MIX AMP	Voltage gain	Y	Gv(Y)	Fig. 4, S5 S6 ON	C'	11.2	12.2	13.2	dB
MIX AMP	Voltage gain	C	Gv(C)	Fig. 5, S5 S6 ON	C'	8.8	9.8	10.8	dB
MIX AMP	Frequency characteristics	Y	fc(Y)	Fig. 4, S5 S6 ON Frequency of −3dB with f=200kHz output taken as 0 dB.	C'	5			MHz
MIX AMP	Frequency characteristics	C	fc(C)	Fig. 5, S5 S6 ON	C'				
MIX AMP	Differential gain		DG	Fig. 6, S5 S6 ON	C			3	%
MIX AMP	Differential phase		DP	Fig. 6, S5 S6 ON	C			3	deg
Burst level			Vo(BN)	Fig. 7, S1 S2 S3 ON	C	257	286	314	mVp-p
R chroma ratio			R/BN	Fig. 7, level ratio between R and burst.	C	2.62	2.92	3.21	
R phase			θ_R	Fig. 7, phase of R	C	94	104	114	deg
G chroma ratio			G/BN	Fig. 7, level ratio between G and burst.	C	2.46	2.74	3.02	
G phase			θ_G	Fig. 7, phase of G	C	231	241	251	deg
B chroma ratio			B/BN	Fig. 7, level ratio between B and burst.	C	1.87	2.08	2.29	
B phase			θ_B	Fig. 7, phase of B	C	337	347	357	deg
PAL burst level ratio			K (BP)	Fig.7, S4 ON. level ratio between PAL and $\overline{PAL}$.	C	0.9	1.0	1.1	
PAL burst phase			θ_{PAL}	Fig.7, S4 ON. burst phase of PAL.	C	125	135	145	deg
PAL burst phase			$\theta_{\overline{PAL}}$	Fig.7, S4 ON. burst phase of $\overline{PAL}$.	C	215	225	235	deg

Test Item		Symbol	Conditions	Test point	Min.	Typ.	Max.	Unit
Burst cycle		tw(B)	Fig. 7	C	8	9.5	11	CYCLE
Breeze way		tD(B)	Fig. 7	C	0.38	0.47	0.65	μS
Carrier leak		VL	Fig. 7	C			30	mVp-p
Composite sync output voltage		Vo(S)	Fig. 8	B	0.25			Vp-p
Buffer amplifier audio	Voltage gain	Gv(A)	Fig. 9, VIN=1Vp-p, f=1kHz	A	−1	0	1	dB
	Frequency characteristics	fc (A)	Fig. 9, Frequency of −3dB with f=1kHz output taken as 0 dB.		30			kHz
	Distortion ratio	THD	Fig. 9, VIN=1 Vp-p, f=1kHz				1	%

Electrical Characteristics Test Circuit



Signals for Testing



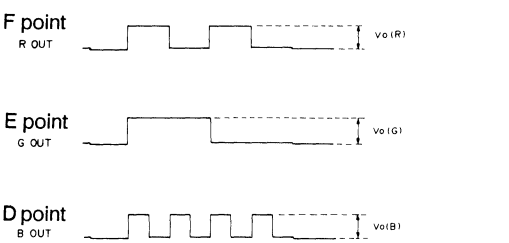
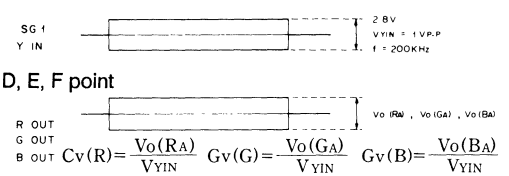


Fig.1



$$Cv(R)=\frac{Vo(R_A)}{V_{YIN}} \quad Gv(G)=\frac{Vo(G_A)}{V_{YIN}} \quad Gv(B)=\frac{Vo(B_A)}{V_{YIN}}$$

Fig.2

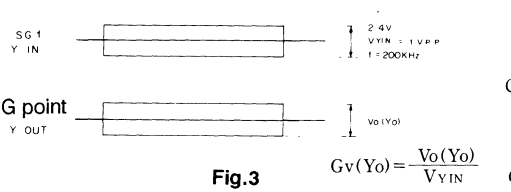


Fig.3

$$Gv(Y_O)=\frac{Vo(Y_O)}{V_{YIN}}$$

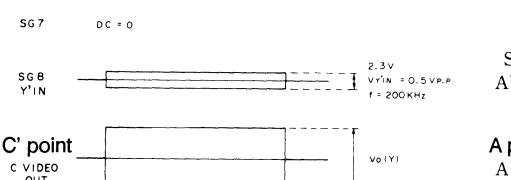


Fig.4

$$Gv(Y)=\frac{Vo(Y)}{V_{Y'IN}}$$

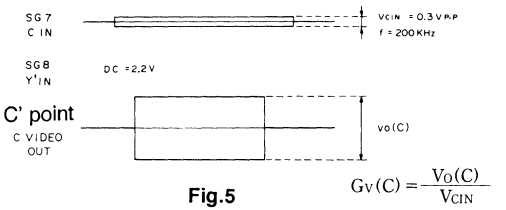


Fig.5

$$Gv(C)=\frac{Vo(C)}{V_{CIN}}$$

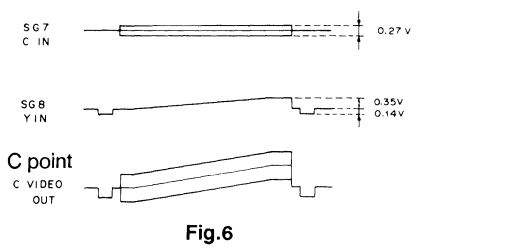
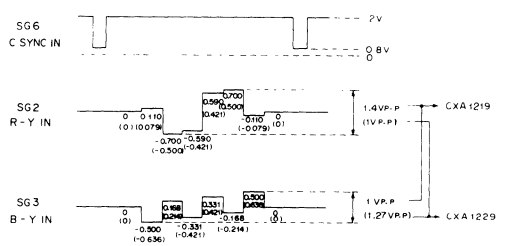
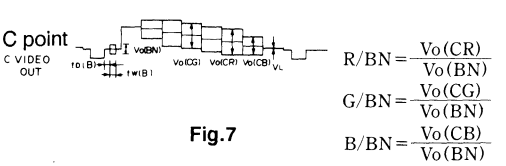


Fig.6





$$R/BN=\frac{Vo(CR)}{Vo(BN)} \quad G/BN=\frac{Vo(CG)}{Vo(BN)} \quad B/BN=\frac{Vo(CB)}{Vo(BN)}$$

Fig.7

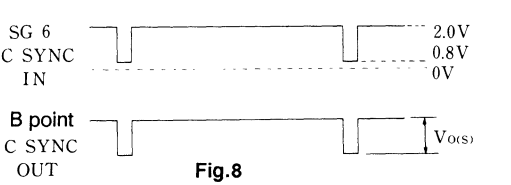
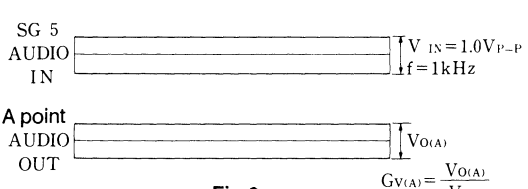


Fig.8

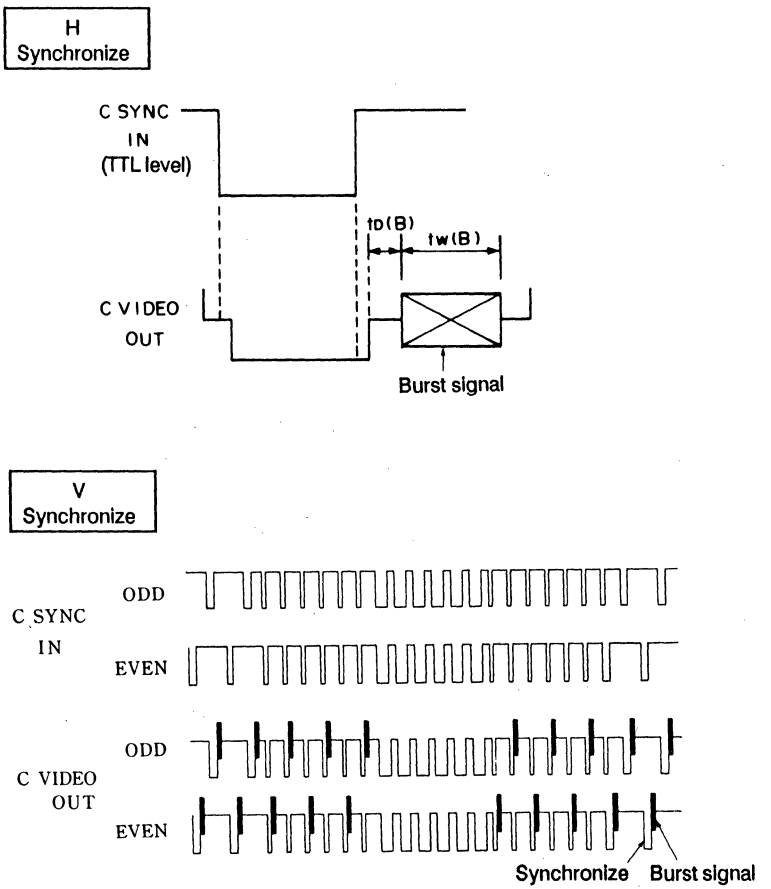


$$GV(A)=\frac{V_{O(A)}}{V_{IN}}$$

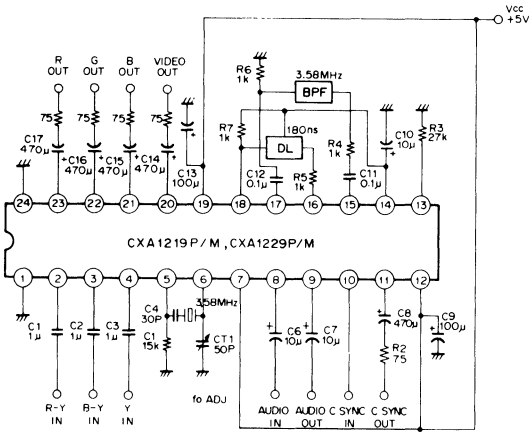
Fig.9

Burst Signal

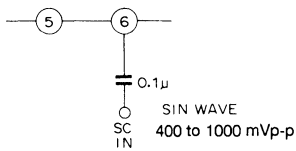
CXA1219P/M and CXA1229P/M generate burst signals with the timing indicated below and in accordance with the input composite sync.



Application Circuit
NTSC mode (Evaluation board)



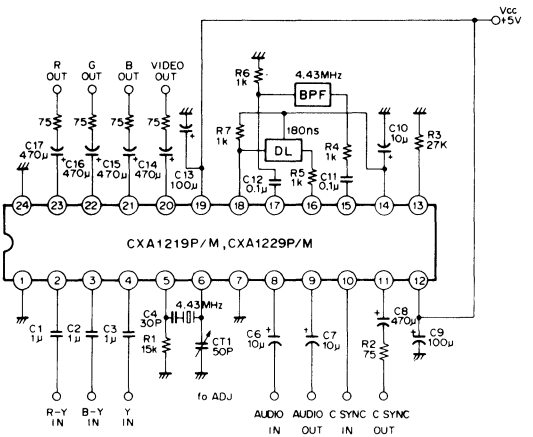
External supply to the subcarrier
To supply the subcarrier from the exterior connect as shown in Figure below.



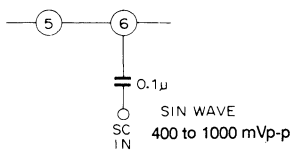
Adjusting the frequency level
Adjusting the trimmer capacitor, set XOOUT level to 400 through 1000 mVp-p.

* Metal film resistor ±1%
BPF Toko H287BSJS-3108HWD
DL Matsushita ELB-5F020N

PAL mode (Evaluation board)



External supply to the subcarrier
To supply the subcarrier from the exterior connect as shown in Figure below.



Adjusting the frequency level
Adjusting the trimmer capacitor, set XOOUT level to 400 through 1000 mVp-p.

* Metal film resistor ±1%
BPF Toko H287BSJS-3108HWD
DL Matsushita ELB-5F020N

Setting the NTSC/PAL mode
Setting the CXA1219P/M or CXA1229P/M to the NTSC or PAL mode is to be carried out by connecting pin 7 to the power supply pin (Vcc) or GND. Connecting pin 7 to Vcc sets the board to the NTSC mode, and connecting pin 7 to GND sets the board to the PAL mode. On the evaluation board, make connection by the jumper wire for the desired mode.

Notes on Use
When you connect C VIDEO OUT to TV and input characters from personal computer for example, you may notice rainbow-hued blurs along edges of characters displayed on the screen, or unevenness of color distribution. This phenomenon results from mixing of Y-signal's high-frequency components into chrominance components (cross-color interference), and does not represent a faulty operation of the board.

SONY **V7040**

NTSC/PAL Encoder

Description

The V7040 is an IC that can operate in both NTSC and PAL modes. It superimposes analog RGB signals and outputs them as such, or as composite video signals. Both types of output can drive the 75Ω load directly.

Features

- 5 V single supply operation
- Low power consumption (135 mW)
- Built-in 75Ω driver (RGB output, 2 systems of composite video output)
- Compatible with both NTSC and PAL modes
- Superimposition (MIX, half-tone functions)

Functions

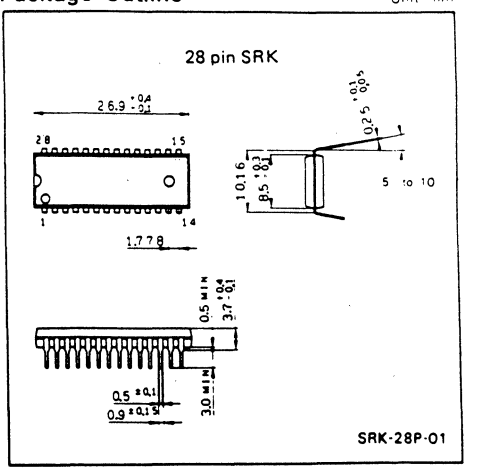
- SW circuit for superimposition
- MTX circuit
- R-Y, B-Y MOD circuit
- 75Ω driver for RGB and composite video outputs

Structure

Bipolar silicon monolithic IC

Package Outline

Unit mm



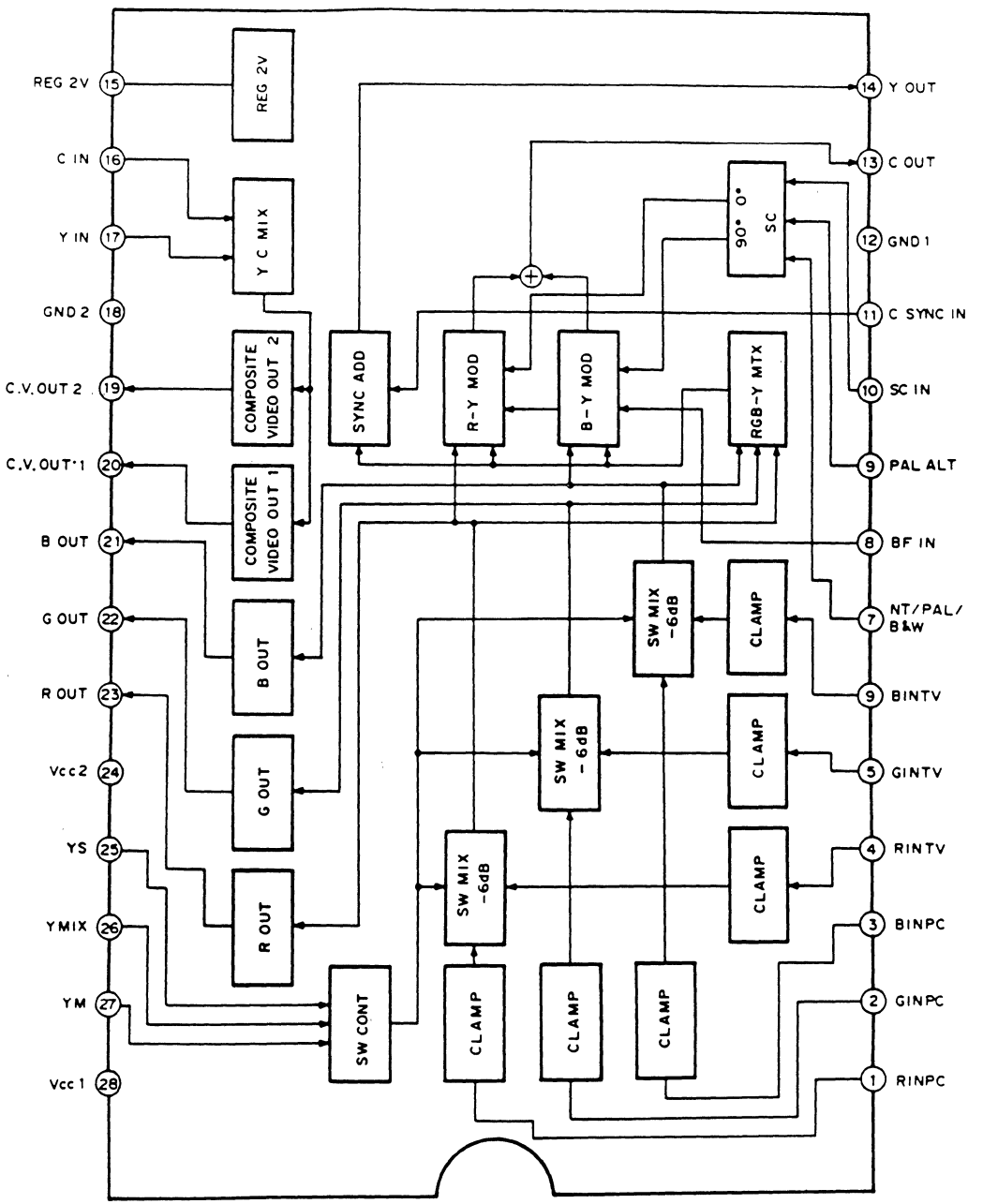
Absolute Maximum Ratings

• Supply voltage	V_{CC}	10	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	1250	mW

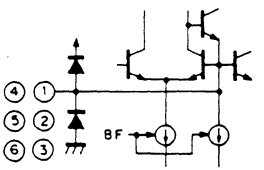
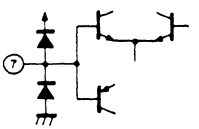
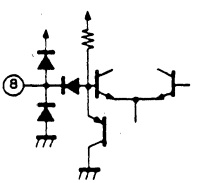
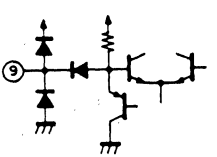
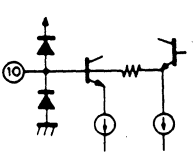
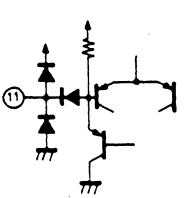
Recommended Operating Condition

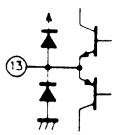
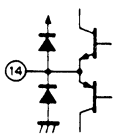
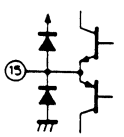
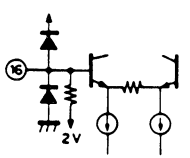
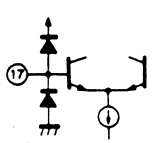
• Supply voltage	V_{CC}	5 ± 0.25	V

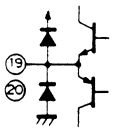
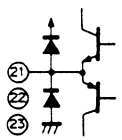
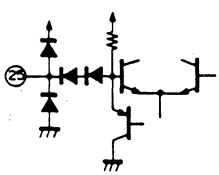
Block Diagram

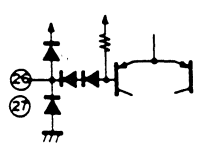


Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 3 4 5 6	RINPC GINPC BINPC RINTV GINTV BINTV		Inputs an RGB color signal from a PC or a TV. Input must be of sufficiently low impedance to clamp.
7	NT/PAL B&W		Switches the modes of NTSC, PAL, and B&W 4.0 v to V_{CC} NTSC mode 2.0 V to 3.0 V PAL mode 0 V to 0.8 V B&W mode
8	BF IN		Inputs burst flag signal. Clamp is performed by this burst flag signal. L: 0 V to 0.8 V H: 2.0 V to V_{CC} Burst at L.
9	PAL ALT		Inputs the PAL ALT signal and inverts the burst and chroma signal phases in every field in PAL mode. 0 V to 0.8 V Burst at 225° 2.0 V to V_{CC} Burst at 135°
10	SC IN		Inputs the sub-carrier. Input sine wave between 0.4 to 0.8 V_{P-P}.
11	C SYNC IN		Inputs composite SYNC signal. L: 0 V to 0.8 V H: 2.0 V to V_{CC} SYNC at L

No.	Symbol	Equivalent circuit	Description
12	GND1		Ground pin for circuits other than RGB OUT and C.V.OUT circuits. Connect with GND2 of pin 18 at the lowest impedance.
13	C OUT		Outputs chroma signal to BPF.
14	Y OUT		Outputs Y signal to delay line.
15	REG2V		For the inner reference voltage. Ground at 10 μF.
16	C IN		Inputs the chroma signal from which the harmonics are removed by BPF.
17	Y IN		Inputs Y signal which is delayed by delay line.

<table>
<tr><th>No.</th><th>Symbol</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>18</td><td>GND2</td><td></td><td>Ground pin for RGB OUT circuit and for C.V OUT circuit. Connect with GND1 of pin 12 at the lowest impedance.</td></tr>
<tr><td>19
20</td><td>C.V.OUT2
C.V.OUT1</td><td>  </td><td>Outputs a composite video signal encoded from switched RGB signals. The load of 75 Ω can be directly driven.</td></tr>
<tr><td>21
22
23</td><td>B OUT
G OUT
R OUT</td><td>  </td><td>Outputs a switched RGB signal as an RGB signal. The load of 75 Ω can be directly driven.</td></tr>
<tr><td>24</td><td>V_{CC2}</td><td></td><td>Power source for RGB OUT circuit and for C.V.OUT circuit. Decoupling should be performed with a very large capacity.</td></tr>
<tr><td>25</td><td>YS</td><td>  </td><td rowspan="2">Switches TV, PC, MIX and halftone modes. Input at TTL level.

SW mode<table><tr><th>YS</th><th>YMIX</th><th>YM</th><th>SW mode</th></tr><tr><td>0</td><td>0</td><td>0</td><td>TV</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Half-tone</td></tr><tr><td>0</td><td>1</td><td>0</td><td>TV</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Half-tone</td></tr><tr><td>1</td><td>0</td><td>0</td><td>PC</td></tr><tr><td>1</td><td>0</td><td>1</td><td>PC</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MIX</td></tr><tr><td>1</td><td>1</td><td>1</td><td>MIX</td></tr></table></td></tr>
<tr><td>26
27</td><td>YMIX
YM</td><td>  </td></tr>
<tr><td>28</td><td>V_{CC1}</td><td></td><td>Power source for circuits other than RGB OUT and C.V.OUT.</td></tr>
</table>

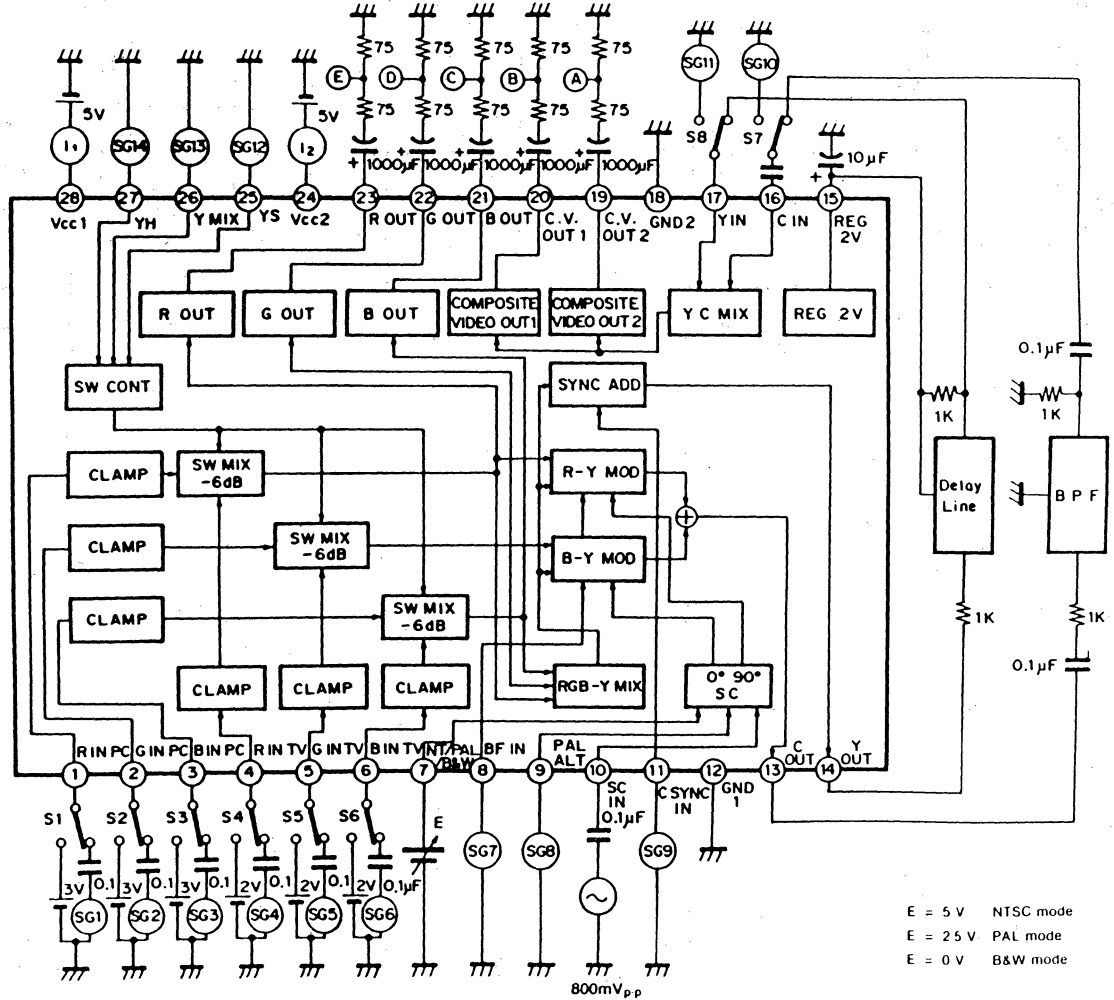
Electrical Characteristics

(Vcc=5V Ta=25° See the Electrical Characteristic Test Circuit)

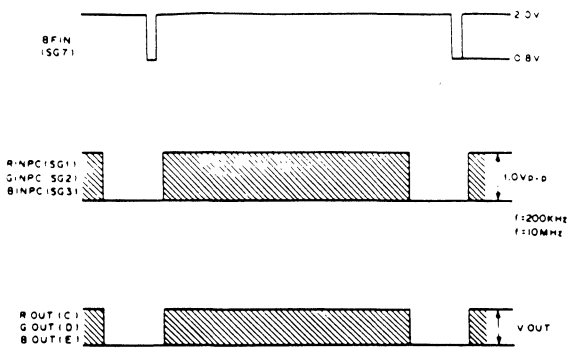
Item	Symbol	Condition		Test point	Min.	Typ.	Max.	Unit
Supply current 1	I_{CC1}	SG1 to SG6 AC 0V SG12 to SG14 DC 0.8V	NTSC mode	I_1	7.0	12.2	17.3	mA
Supply current 2	I_{CC2}			I_2	6.0	14.3	20.0	mA
BW mode supply current 1	I_{BW}	SG7-SG9 DC 2V	BW mode	I_1	4.3	8.1	11.9	mA
R output level	V_R	Fig. 1 RINTV = 1 V_{P-P}, f = 200 kHz		C	0.63	0.71	0.80	V_{P-P}
G output level	V_G	Fig. 1 GINTV = 1 V_{P-P}, f = 200 kHz		D	0.63	0.71	0.80	V_{P-P}
B output level	V_B	Fig. 1 BINTV = 1 V_{P-P}, f = 200 kHz		E	0.63	0.71	0.80	V_{P-P}
RGB frequency characteristic	f_{CRGB}	Fig. 1 RGBINTV = 1 V_{P-P}, f = 10 MHz		CDE	−3			B
RGB crosstalk	CT	Fig. 1 V_{IN} = 1 V_{P-P}, f = 200 kHz		CDE			−40	dB
SW delay time	Td	Fig. 2 SI to S6 On		CDE		40	80	ns
Half-tone level	G_{HT}	Fig. 3 20 log (VM/V)		CDE	−8	−6	−4	dB
MIX level	G_{MIX}	Fig. 3 20 log (VMIX/V)		CDE	−8	−6	−4	dB
Sync level	V_{SYNC}	Fig. 4 Sync level		AB	0.24	0.29	0.34	V
Y level at R 100%	V_{YR}	Fig. 4 Y level at R = 1 V	BW mode	AB	0.18	0.21	0.25	V
Y level at G 100%	V_{YG}	Fig. 4 Y level at G = 1 V		AB	0.37	0.41	0.49	V
Y level at B 100%	V_{YB}	Fig. 4 Y level at B = 1 V		AB	0.05	0.08	0.11	V
Y level at RGB 100%	V_{YW}	Fig. 4 Y level at RGB = 1 V		AB	0.64	0.71	0.82	V
DG	DG	Fig. 5 S7, S8 On		AB			8	%
DP	DP	Fig. 5 S7, S8 On		AB			4	deg
R chroma level	V_{CR}	Fig. 6 R chroma level	NTSC mode	AB	2.53	3.16	3.79	V_{P-P}
R chroma phase	θ_R	Fig. 6 R phase		AB	92	104	116	deg
G chroma level	V_{CG}	Fig. 6 G chroma level		AB	2.36	2.96	3.55	V_{P-P}
G chroma phase	θ_G	Fig. 6 G phase		AB	229	241	253	deg
B chroma level	V_{CB}	Fig. 6 B chroma level		AB	1.79	2.24	2.69	V_{P-P}
B chroma phase	θ_B	Fig. 6 B phase		AB	335	347	359	deg
NTSC burst level	V_{BNT}	Fig. 6 Burst level		AB	0.16	0.29	0.39	V_{P-P}
PAL burst	V_{BPAL}	Fig. 6 Burst level	PAL mode	AB	0.80	1.00	1.20	V_{P-P}
PAL burst phase	θ_{BPAL}	Fig. 6 Burst phase PAL mode	PALALT = 2.0 V	AB	123	135	147	deg
			PALALT = 0.8 V		213	225	237	
Carrier leak	V_{LSC}	Fig. 6 Leak at pedestal		AB			40	mV
Leak at B&W mode	V_{LBW}	Fig. 4 Leak of chroma		AB			30	mV

• All phase reference should be the burst of NTSC = 180°

Electrical Characteristics Test Circuit

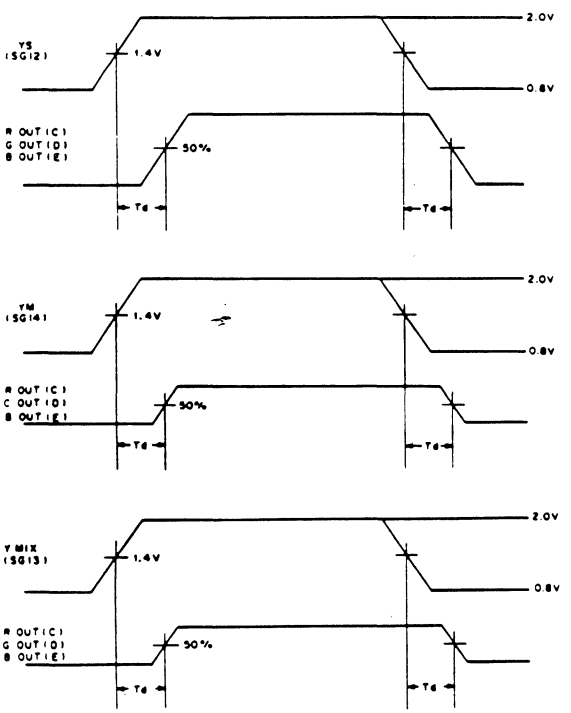


SONY



* YS, YMIX, and YM are 0.8 V (PC mode)

Fig. 1



* RINPC, GINPC, BINPC = 3V
RINTV, GINTV, BINTV = 2V

Fig. 2

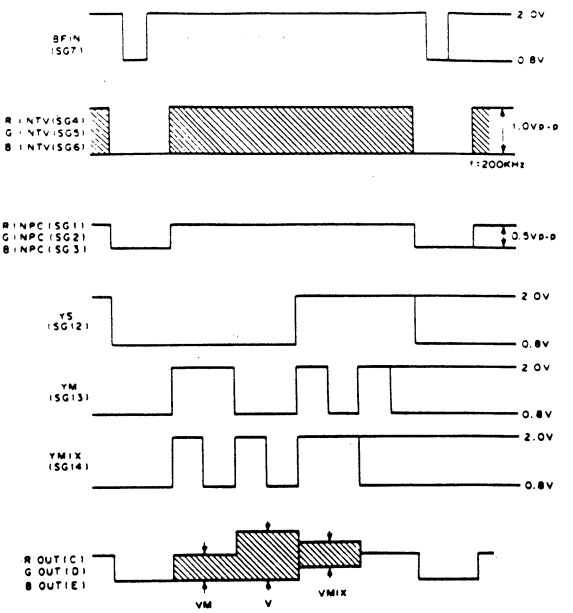
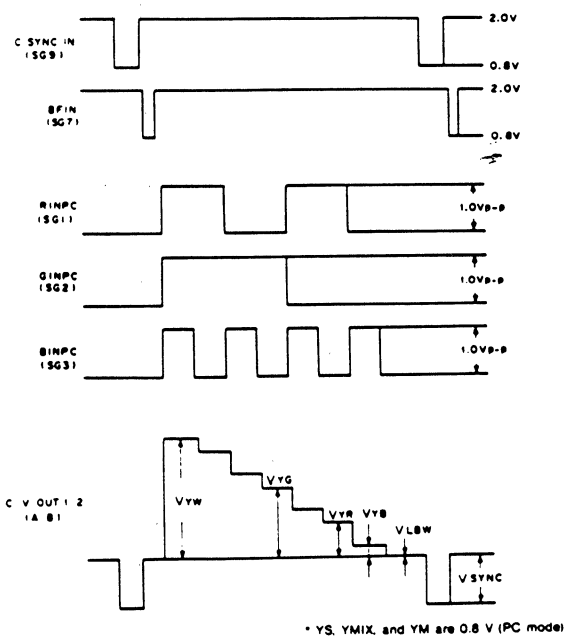


Fig. 3



* YS, YMIX, and YM are 0.8 V (PC mode)

Fig. 4

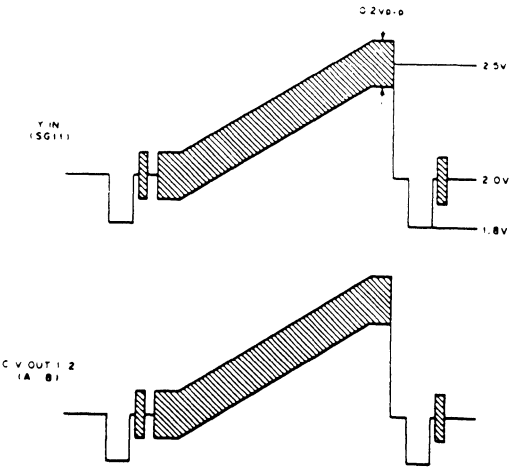
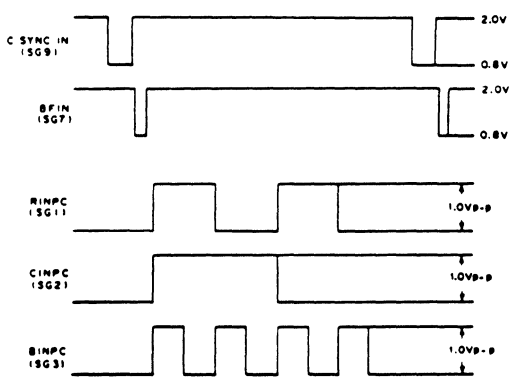
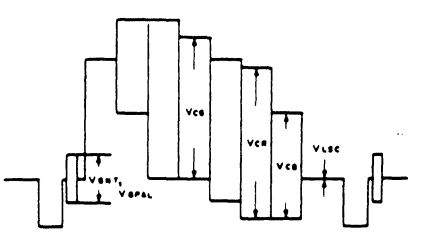


Fig. 5

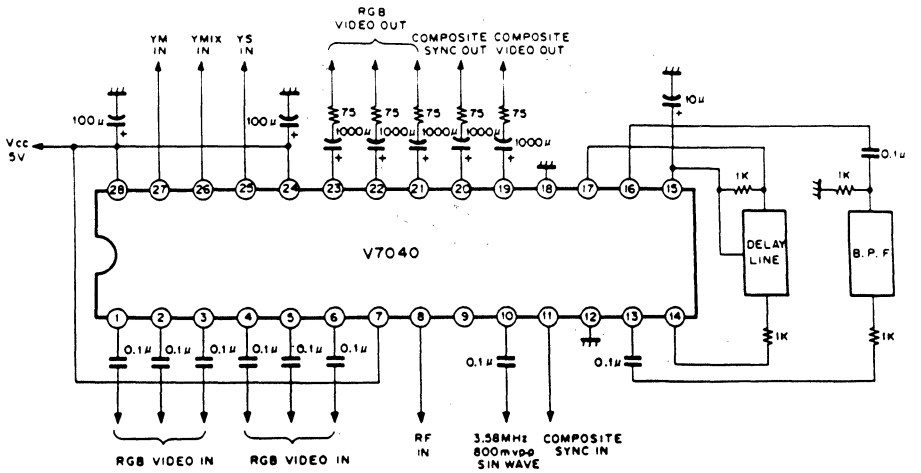




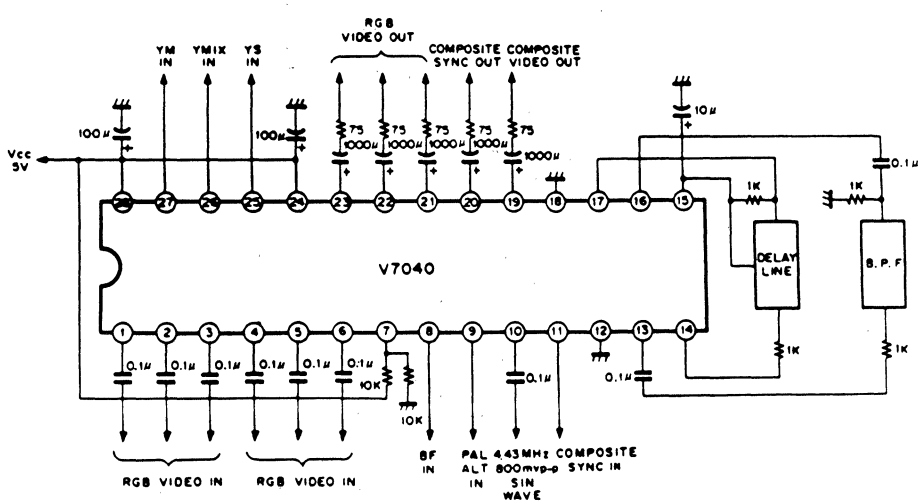
* YS, YMIX, and YM are 0.8 V (PC mode)

Fig. 6

Application Circuit NTSC



Application Circuit PAL



Application Notes

1. RGB signal input
   Input the RGB signal to pins 1 to 3 and 4 to 6 via a clamp capacitor.
   RGB signal is pedestal clamped by means of the burst flag signal input from pin 8. Input with a sufficiently low impedance.

2. SW mode
   RGB signal input from pins 1 to 3 and RGB signal input from pins 4 to 6 are switched into the specified Y mode at the SW circuit. This, by means of the YS, YMIX, YM signals input from pins 25 to 27. The SW mode is in accordance with the following table.
   1 PC mode
   RGB signal input from pins 1 to 3 is output via SW circuit.
   2 TV mode
   RGB signal input from pins 4 to 6 is output via SW circuit.
   3 MIX mode
   RGB signal input from pins 1 to 3 and RGB signal input from pins 4 to 6 are respectively lowered to a level of −6 dB, mixed and output via SW circuit.
   4 Halftone mode
   RGB signal input from pins 4 to 6, lowers −6 dB level and is output. When superimposing, the background can be darkened and the letters made easier to read. For normal superimposing, ground pin 26 YMIX and pin 27 YM. Input superimpose signal to pin 25 YS.

SW Mode

YS	YMIX	YM	SW Mode
Pin 25	Pin 26	Pin 27	
L	L	L	TV
L	L	H	Halftone
L	H	L	TV
L	H	H	Halftone
H	L	L	PC
H	L	H	PC
H	H	L	MIX
H	H	H	MIX

L≦0.8V
H≧2.0V

3. NT/PAL/B & W mode
   By turning pin 7 (NT/PAL/B & W) to 4V and over, NTSC mode is switched on. By turning it to 3 to 2V, PAL mode is switched on. By turning it to 0.8V or under, B & W mode is switched on. In NTSC mode, burst signal, with B-Y shaft at 0°, is output to 180° direction.
   In PAL mode, burst signal, in accordance with PAL ALT signal input from pin 9, is output to 135°, 225° direction. In B & W mode, chroma signal and burst signal are not output. As for V7020, to use in NTSC mode, pin 7 is left open or connected to Vcc.

4. BF signal
In accordance with burst flag signal input from pin 8, the burst signal from the composite video signal, is formed. Also, the clamping of RGB signal is executed in accordance with this burst flag signal.

5. PAL ALT signal
In accordance with PAL ALT signal input from pin 9, the R-Y shaft direction of the modulator from the chroma signal, is inverted. When pin 9 is at "H", (≧2.0V) it is set to normal direction. When it is at "L", it is set to the inverted direction.

6. Subcarrier input
Input the subcarrier through a 0.4 to 0.8 Vp-p sine wave, via pin 10 (SC IN). With the subcarrier input, too many harmonic waves may adversely affect the phase characteristics of the chroma modulator.

7. Vcc, GND
Connect with as low as possible an impedance, pin 12 and GND 1, pin 18 and GND 2. Pin 24 (Vcc 2) and pin 18 (GND 2) are the power supply of 75Ω driver (RGB OUT circuit, C.V.OUT circuit). As large currents flow in, execute decoupling with a sufficiently large capacitor.

8. BPF, DL
Eliminates harmonic waves contained in the chroma demodulator output, at the band-pass filter. Use a delay line matching the band-pass filter delay time.

9. RGBOUT, C.V.OUT
At pins 19 and 20 (V.OUT) a composite video signal of about 2 Vp-p is output. At pins 21 through 23 (RGB OUT), an RGB signal (superimposed or else) of about 1.4 Vp-p is output. For the composite sync signal used together with RGB signal, use the composite video signal of pins 19 and 20.
Both C.V.OUT of pins 19, 20 and RGB OUT of pins 21 through 23, can directly drive a load of 75Ω.

10. Composite sync signal
Through the composite sync signal input from pin 11, sync is added to Y signal. At "H" (≧2.0V) Y signal is activated while at "L" (≦0.8V) sync is activated.

Descriptions of Operation

1. Clamp circuit, SW circuit, SW CONT circuit
   RGB signal from PC is input to pins 1 through 3 via a clamp capacitor. In the same way, RGB signal from TV is input to pins 4 through 6. Input RGB signals are pedestal clamped together, by means of the clamp circuit operating in accordance with the burst flag signal. Clamped RGB signals are switched at the SW circuit, in accordance with the 4 modes, specified by YS, YMIX and YM signals, which are input from pins 25 through 27.
   RGB signals switched at SW circuit are sent to MTX, MOD and RGB OUT circuits.

2. MTX circuit, MOD circuit, SC phase shift circuit
   From RGB signal switched at SW circuit. Y signal is formed by means of MTX circuit.
   As for these Y and R signals, B signal goes to R-Y MOD circuit and B-Y MOD circuit. Also, this Y signal is sent to SYNC ADD circuit; composite sync signal input from pin 11 is added to it, and it is sent through pin 14 to delay line.
   SC shift phase circuit creates 0°, 90° subcarriers by phase shifting the subcarrier input from pin 10.
   0° and 90° subcarriers are respectively sent to B-Y MOD circuit and R-Y MOD circuit. By means of R with Y signals and B with Y signals, they undergo quadrature double phase modulation to become chroma signals. Chroma signals are sent to BPF via pin 13.

3. YC MIX circuit
   Chroma signals from which harmonic waves have been eliminated at BPF, and Y signals that have passed through the delay line are sent to YC MIX circuit via pins 17 and 16. They are mixed, become composite video signals and sent to C.V.OUT circuit.

4. COMPOSITE VIDEO OUT circuit (C.V.OUT circuit)
   Composite video signals from YC MIX circuit, are amplified at C.V.OUT circuit into about 2 Vp-p video signals, and output through pins 19 and 20. C.V.OUT circuit, from each of pins 19 and 20 can directly drive a load of 75Ω.

5. RGB OUT circuit
   Signal RGB switched at SW circuit is amplified to about 1.4 Vp-p by RGB OUT circuit and output via pins 21 through 23. RGB OUT circuit can directly drive a load of 75Ω.

6. REG 2V
   The internal reference voltage is obtained through the band gap reference circuit. The reference voltage becomes the standard for the volume of each of the clamp electric potential, the burst and the sync.

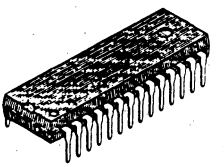
Sync Discrimination for CRT Display

Description

CXA1365S is used for sync signal discrimination and waveform shaping in the CRT display.
There are 3 types of Sync input signals for discrimination.

V. separate sync signals
Composite sync or H. separate sync signals
Sync on video

28pin SDIP (Plastic)



Features

- Polarity and amplitude of input signals

	Polarity	Amplitude (Vp-p)
V. separate sync	: Positive/Negative	2 to 5
Composite sync	: Positive/Negative	0.2 to 1.2
H. separate sync	: Positive/Negative	2 to 5
Sync on video	: Negative (Sync signals part)	0.2 to 0.7
	(Video part)	0 to 1.5

Applications

CRT display monitor

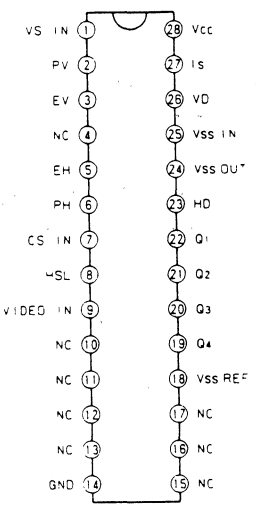
Operating Conditions

Supply voltage Vcc 8.5 to 9.5 V

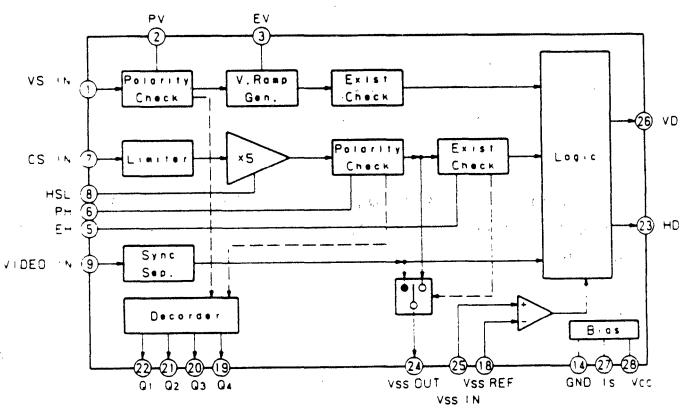
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	1.35	W

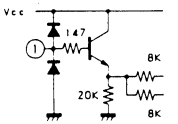
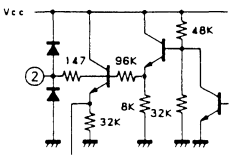
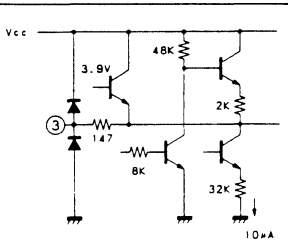
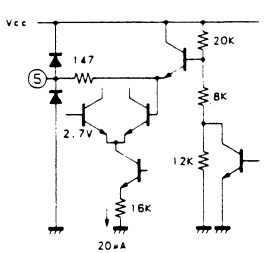
Pin Configuration (Top View)

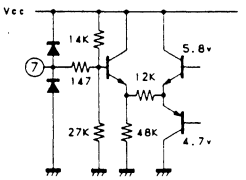
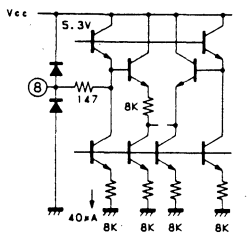
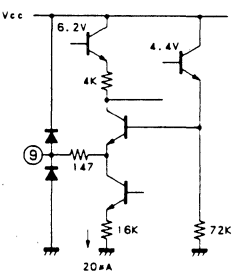
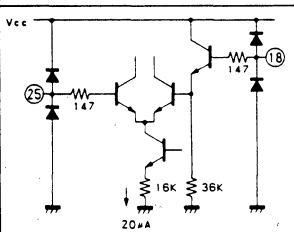


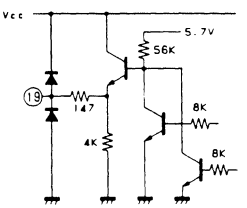
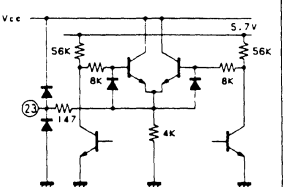
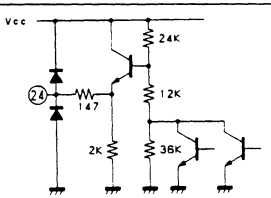
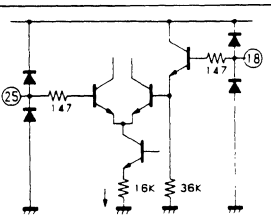
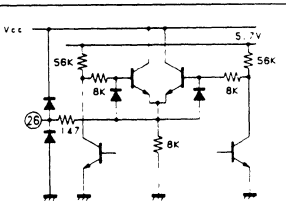
Block Diagram

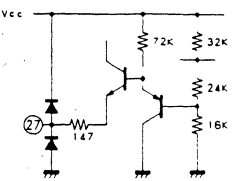


Pin Description and Equivalent Circuit

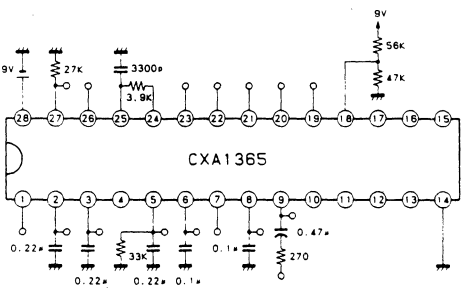
No.	Symbol	Pin voltage	Equivalent Circuit	Description
1	VS IN	——		V. separate sync is input at TTL level in both positive and negative polarity.
2	PV	0, 2.5V		This pin connects a 0.22μF integrating capacitor for the polarity check circuit to GND. When connecting the capacity at positive polarity, it is 2.5V, at negative polarity 0V and at no input 2.5V.
6	PH			
3	EV	3.2V to 6V		V. ramp waveforms generation part. Generates ramp waveforms synchronously with the input separate sync cycle and connects 0.22μF to GND. The ramp waveforms time constant during charge (Rise time) is almost determined through the 2kΩ and external 0.22μF. Same time constant during discharge (Fall time) is determined through the external 0.22 μF and the internal 10μA. When there is a V. separate sync, Pin 3 turns to 3.4V~6.0V, exist check is executed and sync existence established. When there is no V. separate sync, it turns to 3.2V.
4,10,11 12,13,15 16,17	NC	——	——	Pin not in use.
5	EH	2.0, 3.8V		During composite sync input, between this pin and GND is connected a 33 kΩ resistance for sync exist discrimination and a nearly peak hold circuit for 0.22μF capacitor. When there is a composite sync a nearly peak hold is executed at 3.4V to 3.8V, a comparison made with the 2.7V reference voltage and sync exist discriminated. When there is no composite sync, it turns to 2.0V.

No.	Symbol	Pin voltage	Equivalent Circuit	Description
7	CS IN	5.9V		Inputs composite sync (Positive/Negative polarity) and H. separate sync (Positive/ Negative polarity). Amplitude either 0.2Vp-p and above or at TTL level.
8	HSL	4.6V		Connects limiter at composite sync input part and 0.1μF DC offset absorption capacitor for 5 times gain amplifier to GND.
9	VIDEO IN	3.0V		Inputs sync on video (Sync at negative polarity). Connects in series 0.47μF capacitor and 270Ω resistance between signal source and this pin. Slice level is determined by the relation between the total of 147Ω and the external resistance value multiplied by 20μA, the sync frequency, and sync width. When resistance value is small, slice level is low.
14	GND	0V	——	GND pin.
18	Vss REF	——		Reference pin for V. sync-separator. Provides reference voltage by connecting external resistance between Vcc and GND. Sets reference to 4.2V.

<table>
<tr><th>No.</th><th>Symbol</th><th>Pin voltage</th><th>Equivalent Circuit</th><th>Description</th></tr>
<tr><td>19
20
21
22</td><td>Q_4
Q_3
Q_2
Q_1</td><td>0, 4.5V</td><td> 
</td><td>Outputs polarity information of synchronizing signal.
High level at 4.5V.
Low level at 0V.
With V. sync separator polarity at Pv and composite sync polarity at P_H, the following table is obtained:
<table>
<tr><th>Pv</th><th>P_H</th><th>Q_1</th><th>Q_2</th><th>Q_3</th><th>Q_4</th></tr>
<tr><td>Negative</td><td>Negative</td><td>H</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>Negative</td><td>Positive</td><td>L</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>Positive</td><td>Negative</td><td>L</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>Positive</td><td>Positive</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
</table></td></tr>
<tr><td>23</td><td>HD</td><td>0, 4.5V</td><td> 
</td><td>HD (H.Drive Pulse) output pin.
Amplitude output at positive polarity from 0 to 4.5V.</td></tr>
<tr><td>24</td><td>Vss
OUT</td><td>2.3, 5.3V</td><td> 
</td><td>Composite sync or sync separated from sync on video is output for V. sync separator. Amplitude is at 2.3V to 5.3V and output at positive polarity.</td></tr>
<tr><td>25</td><td>Vss IN</td><td>——</td><td> 
</td><td>Input pin for V. sync separator comparator. Connects an integrating circuit composed of 3.9kΩ resistance and 3300pF capacitor between pins 24 and 25. In the V. sync separator section when the integrated sync is anywhere between pin voltage and VBE (0.7V) voltage, the comparator operates.</td></tr>
<tr><td>26</td><td>VD</td><td>0, 4.5V</td><td> 
</td><td>VD (V. Drive Pulse) output pin.
Amplitude at 0 to 4.5V in positive polarity.</td></tr>
</table>

No.	Symbol	Pin voltage	Equivalent Circuit	Description
27	IS	2.0V		Reference voltage pin. Connects 27 kΩ resistance (1%) to GND. Current flowing through this resistance is taken as the reference current.
28	Vcc	9V		Supply pin. (9±0.5V)

Pin Voltage Test External Circuit

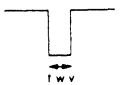
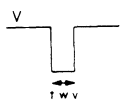
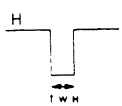
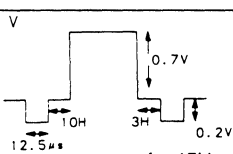
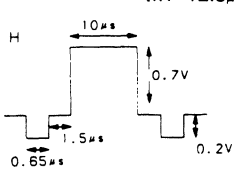


Electrical Characteristics (See the Electrical Characteristics Test Circuit)

No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
1	VD output voltage	E_{VD}	Test VD output peak value during V. separate sync input. Input signal A. (tw=12.5μs)	VD (26pin)	(H level) 3.5 (L level) 0	4.5 0	5.0 0.4	V V
2	VD output pulse width ①	t_{V1}	Test VD output pulse width during V. separate sync input. Input signal A. (tw=12.5μs)	VD (26pin)	11.5	12.5	13.5	μs
3	VD output pulse width ②	t_{V2}	Test VD output pulse width during composite sync input. Input signal B. (tw=12.5μs)	VD (26pin)	8	10	12	μs
4	VD output pulse width ③	t_{V3}	Test VD output pulse width during sync on video input. Input signal C. (tw=12.5μs)	VD (26pin)	8	10	12	μs

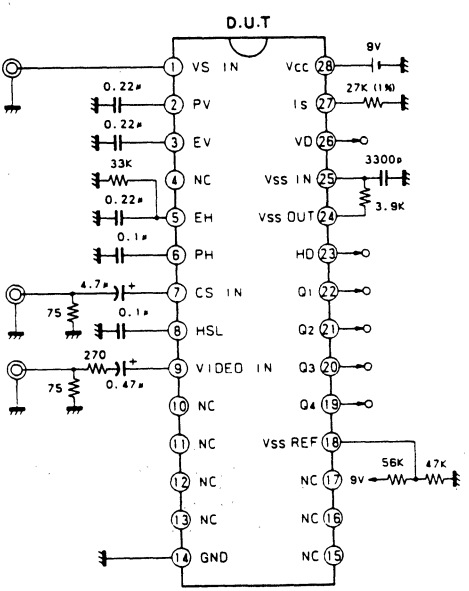
No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
5	HD output voltage	E_{HD}	Test HD output peak value during composite sync input. Input signal D. (tw=0.65µs)	HD (23pin)	(H level) 3.5 (L level) 0	4.5 0	5.0 0.4	V V
6	HD output pulse width ①	th_1	Test HD output pulse width during composite sync input. Input signal D. (tw=0.65µs)	HD (23pin)	0.5	0.6	0.8	µs
7	HD output pulse width ②	th_2	Test HD output pulse width during composite sync input. Input signal E. (tw=2.5µs)	HD (23pin)	2.2	2.5	2.8	µs
8	HD output pulse width ③	th_3	Test HD output pulse width during composite sync input. Input signal B. (tw=0.65µs)	HD (23pin)	0.5	0.7	0.8	µs
9	HD output pulse width ④	th_4	Test HD output pulse width during sync on video input. Input signal C. (tw=0.65µs)	HD (23pin)	0.5	0.7	0.8	µs
10	PV voltage ①	V_{PV1}	Voltage integrated value of V. polarity discrimination circuit during V. separate sync input. Input signal F. (Negative logic)	PV (2pin)	——	0.0	——	V
11	PV voltage ②	V_{PV2}	Voltage integrated value of V. polarity discrimination circuit during V. separate sync input. Input signal G. (Positive logic)	PV (2pin)	——	2.5	——	V
12	PH voltage ①	V_{Ph1}	Voltage integrated value of H. polarity discrimination circuit during composite sync input. Input signal H. (Negative logic)	PH (6pin)	——	0.6	——	V
13	PH voltage ②	V_{Ph2}	Voltage integrated value of H. polarity discrimination circuit during composite sync input. Input signal I. (Positive logic)	PH (6pin)	——	2.1	——	V
14	EV voltage ①	V_{ev1}	Test voltage at V. ramp waveforms generation part during V. separate sync input. Input signal A.	EV (3pin)	——	6.0	——	V

No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
15	EV voltage ②	E_{ev2}	Test voltage at V. ramp waveforms generation part during V. separate sync input. No signal input.	EV (3pin)	——	3.2	—	V
16	EH voltage ①	V_{eh1}	Test sync existence and discrimination voltage during composite sync input. Input signal J.	EH (5pin)	——	3.4	—	V
17	EH voltage ②	V_{eh2}	Test sync existence and discrimination voltage during composite sync input. No signal input.	EH (5pin)	——	2.0	—	V
18	t delay ①	t_{d1}	Test delay difference between CS and HD during composite sync input. Or the time from CS (Positive logic) rise time (50%) to HD output rise time (50%). Input signal K.	HD (23pin)	——	200	250	ns
19	t delay ②	t_{d2}	Test delay difference between input signal sync and HD during sync on video input. Or the time from input sync fall time (50%) to HD output rise time (50%). Input signal C.	HD (23pin)	——	60	100	ns
20	Logic output voltage H	Q_H	Test polarity information output H level voltage of synchronizing signal.	Q_1 to Q_4 (19 pin~22pin)	3.5	4.5	5.0	V
21	Logic output voltage L	Q_L	Test polarity information output L level voltage of synchronizing signal	Q_1 to Q_4 (19 pin~22pin)	0	0	0.4	V
22	Consumption current	I_{CC}	V_{CC}=9V, Test consumption current during no signal input.	V_{CC} (28pin)	11	15	20	mA
23	Reference voltage	I_{REF}	V_{CC}=9V, Test reference current pin voltage during no signal input.	IS (27pin)	1.8	2.0	2.2	V

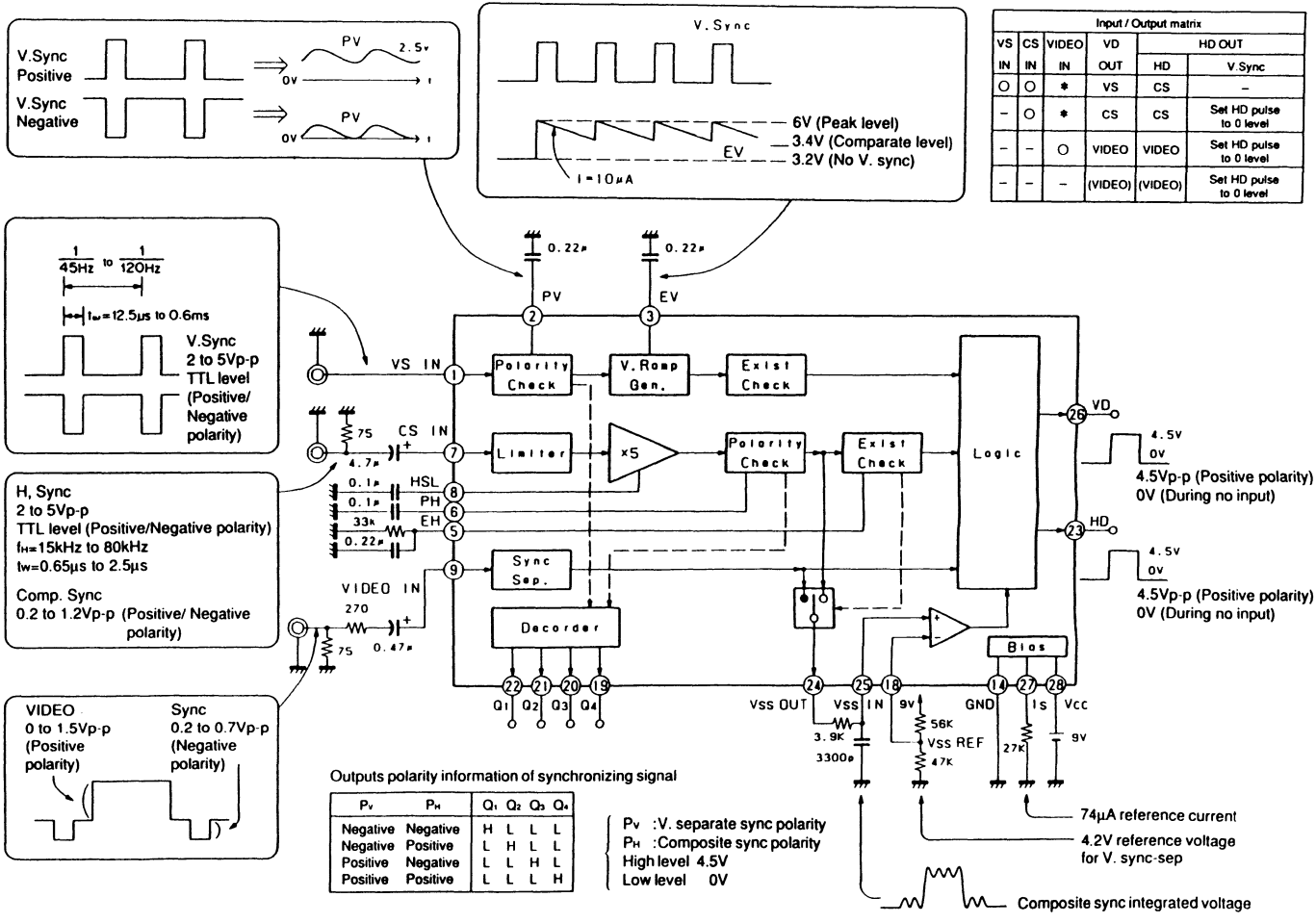
Signal	Item	V.SYNC IN (Pin1)	Composite SUNC IN (Pin 7)	VIDEO IN (Pin 9)
A	1, 2, 14	 fv=45Hz twv=12.5µs Negative logic 2Vpp		
B	3, 8		 fv=45Hz twv=12.5µs Negative logic 2Vpp  fH=80kHz twH=0.65µs Negative logic 2Vpp	
C	4, 9, 19			 fv=45Hz twv=12.5µs  fH=80kHz twH=0.65µs
D	5, 6		fH=80kHz twH=0.65µs Negative logic 0.25Vpp	
E	7		fv=80kHz twH=2.5µs Negative logic 0.25Vpp	

Signal	Item	V.SYNC IN (Pin1)	Composite SYNC IN (Pin 7)	VIDEO IN (Pin 9)
F	10	fv=120Hz twv=600µs Negative logic 2Vpp		
G	11	 fv=120Hz twv=600µs Positive logic 2Vpp		
H	12		fH=80kHz twH=2.5µs Negative logic 2Vpp	
I	13		fH=80kHz twH=2.5µs Positive logic 2Vpp	
J	16		fH=15kHz twH=3.3µs Negative logic 2Vpp	
K	18		fH=80kHz twH=0.65µs Positive logic 0.25Vpp	

Electrical Characteristics Test Circuit (Application Circuit)



Operation and Input/Output Warveforms Description



Input / Output matrix					
VS IN	CS IN	VIDEO IN	VD OUT	HD OUT	
				HD	V.Sync
O	O	*	VS	CS	–
–	O	*	CS	CS	Set HD pulse to 0 level
–	–	O	VIDEO	VIDEO	Set HD pulse to 0 level
–	–	–	(VIDEO)	(VIDEO)	Set HD pulse to 0 level

Outputs polarity information of synchronizing signal

P_V	P_H	Q_1	Q_2	Q_3	Q_4
Negative	Negative	H	L	L	L
Negative	Positive	L	H	L	L
Positive	Negative	L	L	H	L
Positive	Positive	L	L	L	H

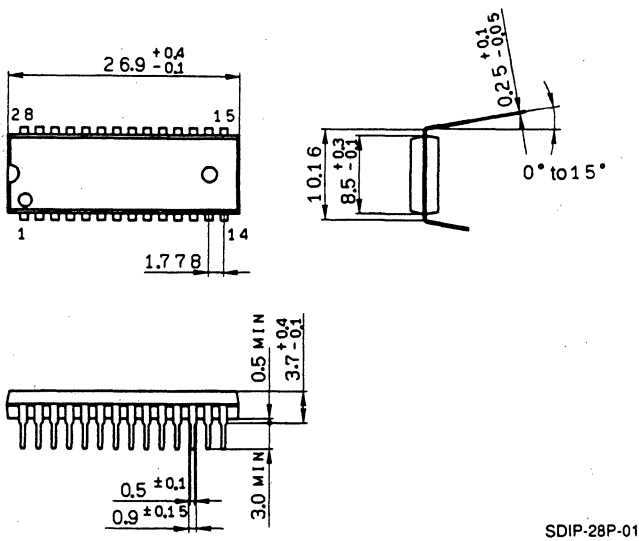
P_V :V. separate sync polarity
P_H :Composite sync polarity
High level 4.5V
Low level 0V

SONY

CXA1365S

Package Outline Unit: mm

CXA1365S 28pin SDIP (Plastic) 400mil 1.7g



SDIP-28P-01

SONY CXD1030M

Sync. Signal Generator for Camera

Description

The CXD1030M is a sync. signal generator for video cameras.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
  (Standard NTSC: 25 mW; PAL: 30 mW)
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync.

Function

Sync. signal generator

Structure

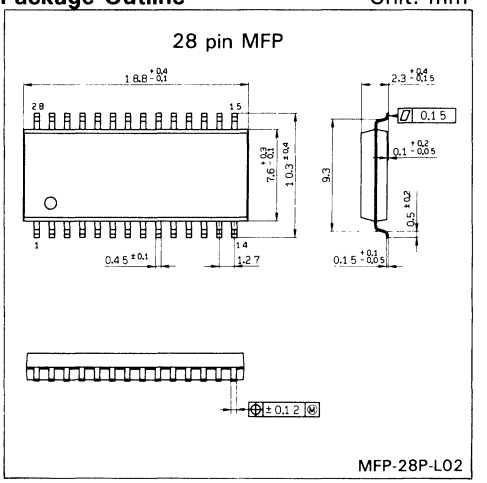
Silicon gate CMOS IC

Application

Video • Camera

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}* − 0.3 to 7.0	V
• Input voltage	V_I	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Operating temperature	T_{opr}	− 20 to + 75	°C
• Storage temperature	T_{stg}	− 55 to + 150	°C

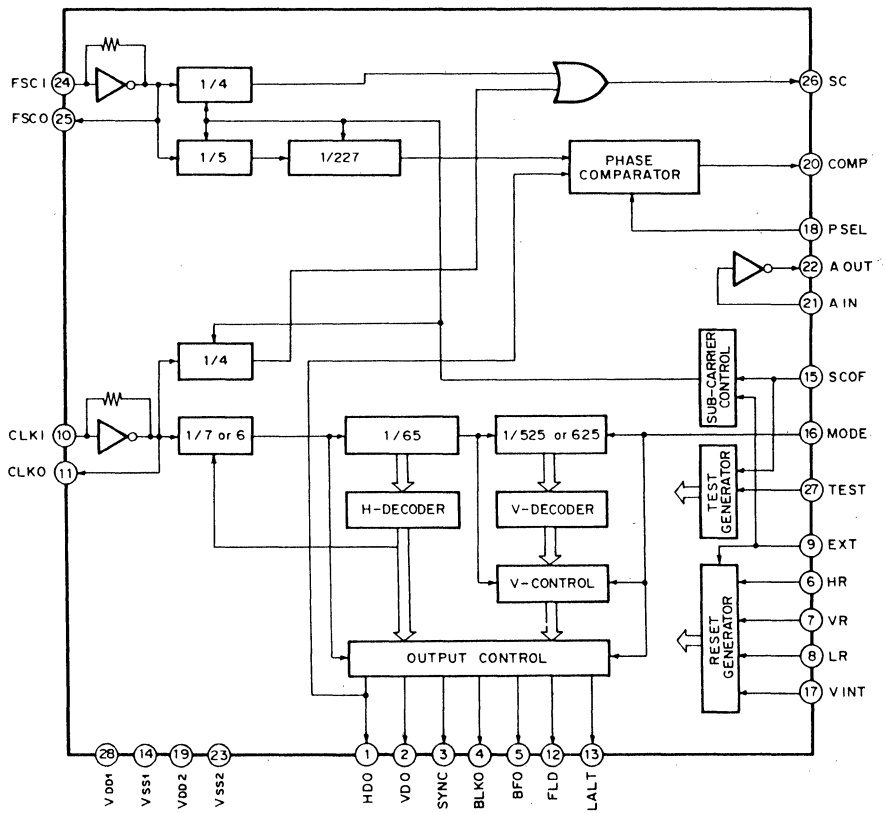
* V_{SS} = 0V

Recommended Operating Conditions

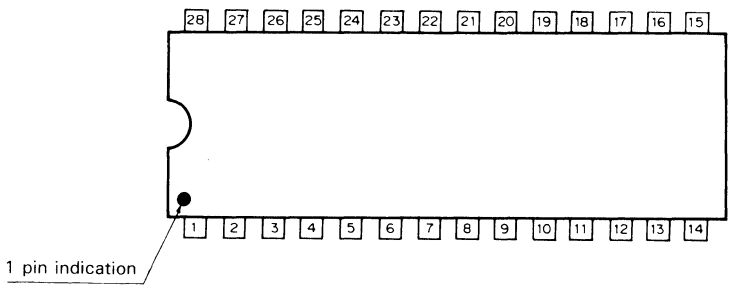
• Supply voltage	V_{DD}	4.50 to 5.50	V
• Operating temperature	T_{opr}	− 20 to + 75	°C

70110-TO

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Complex synchronized pulse
4	BLKO	O	Complex branking pulse
5	BFO	O	Burst flug pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	Internal/external mode switching $\overline{\text{INT}}$/EXT
10	CLKI	I	Clock input (NTSC: 14.31818 MHz, PAL: 14.1875 MHz)
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	V_{SS1}	—	GND
15	SCOF	I	Sub carrier suppress input L: OFF
16	MODE	I	NTSC/PAL mode switching $\overline{\text{NTSC}}$/PAL
17	VINT	I	Initialize input
18	PSEL	I	Phase comparator polarity switching
19	V_{DD2}	—	Inverter +5V for filter
20	COMP	O	Phase comparator output
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	V_{SS2}	—	Inverter GND for filter
24	FSCI	I	$4f_{SC}$ clock input
25	FSCO	O	$4f_{SC}$ clock output
26	SC	O	Sub carrier output
27	TEST	I	Test input (L normal)
28	V_{DD1}	—	+5V

Electrical Characteristics

DC characteristics

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_{opr} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Test circuit (2)		2.0		mA
		I_{DDS}	Static state*1	0		0.1	μA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -1.0$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.0$ mA	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -0.5$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 0.5$ mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		$0.7V_{DD}$			V
	L level	V_{IL}				$0.3V_{DD}$	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	−25		25	μA
Input leak current*4		I_{LZ}		−40		40	μA

Note) *1 $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2 Output pins except "AOUT"
*3 "AOUT" pin
*4 Three state pin

I/O Capacitance

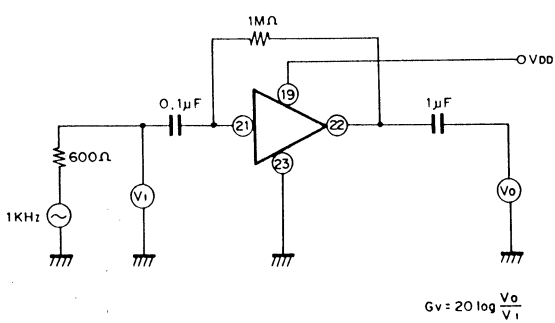
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			12	pF
Output pin	C_{OUT}			12	pF

Test condition: $V_{DD} = V_I = 0V$, $f_M = 1$ MHz

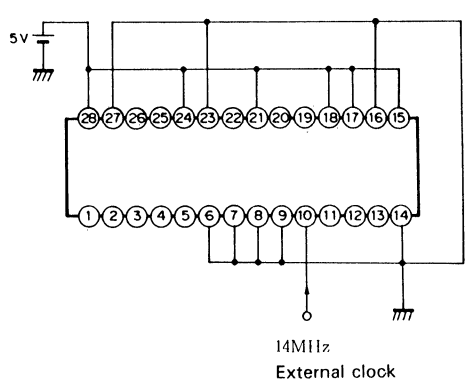
Filter amplifier characteristics

Voltage gain G_V 23dB (Typ.)

Test circuit (1)



Test circuit (2)



Description of Function

1. Generation of various sync. signals (See the Timing Chart.)
   Various sync. signals are generated from clocks.

- Clock frequencies
  NTSC: 910 fH (14.31818 MHz)
  PAL : 908 fH (14.1875 MHz)
  4 fSC (17.734475 MHz)

2. PAL 4 fSC PLL
   Using 908 fH as the master clock, the 4 fSC is put in phase. Corresponding to an external filter (passive or active), the phase comparator polarity can be switched.

Filter	PSEL	Master (908fH)	4fSC	COMP
Passive	L	Fast	Slow	H
		Slow	Fast	L
Active	H	Fast	Slow	L
		Slow	Fast	H

3. SC (SubCarrier) generation

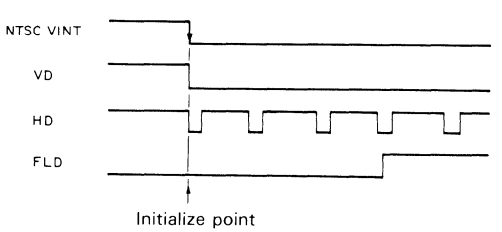
Mode	INT or EXT	SC
NTSC	INT	910fH/4
NTSC	EXT	4fSC/4
PAL	×	4fSC/4

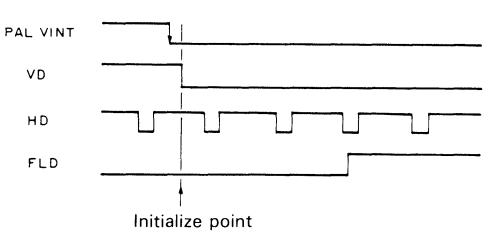
INT : INTERNAL mode (EXT = L)
EXT: EXTERNAL mode (EXT = H)

Unused counters are stopped in any of the mode.
When SC is not required, any counters on SC are stopped and SC is not output by SCOF being set to L.

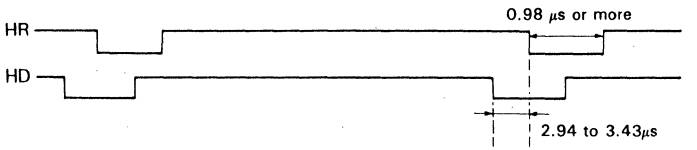
4. Initialization and Reset
   In the INT mode, the circuit is initialized with the fall of VINT. At this time, the H reset, V reset, and LALT reset are not accepted. In the EXT mode, VINT is not accepted but the H reset, V reset, and LALT reset are accepted.

- Initialization (VINT)
  When EXT is L, the fall of VINT is detected and operation is started by the circuit being initialized at the VD fall position immediately prior to field I. (The initialization is completed within 100 ns after the fall is detected.)

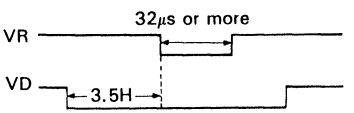




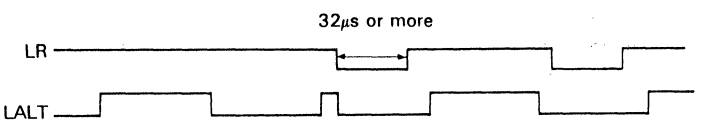
- H reset (HR)
  A reset is executed with the first fall but no reset will be done as long as the subsequent edges do not deviate by more than two clocks (0.98 μs).
  The minimum reset pulse width is 0.98 μs.
  HD is reset 2.94 to 3.43 μs in advance of HR input.



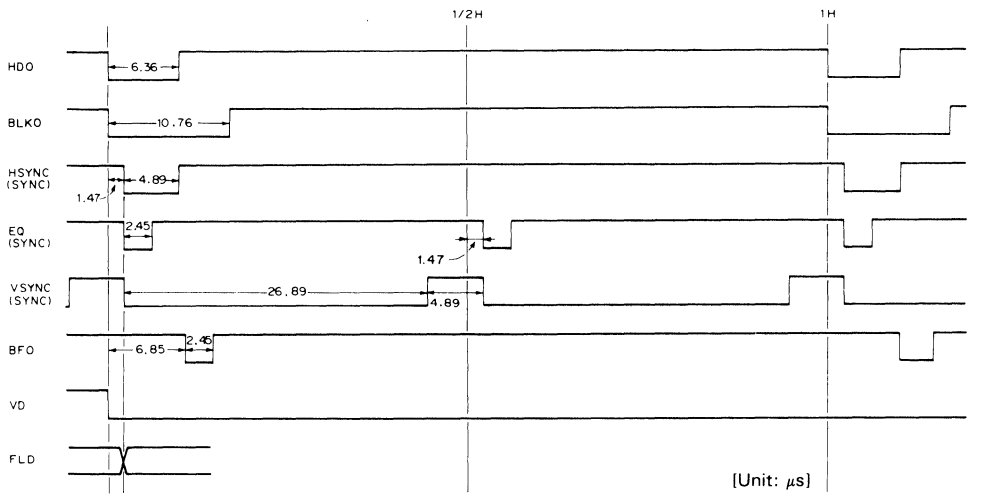
- V reset (VR)
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 μs.



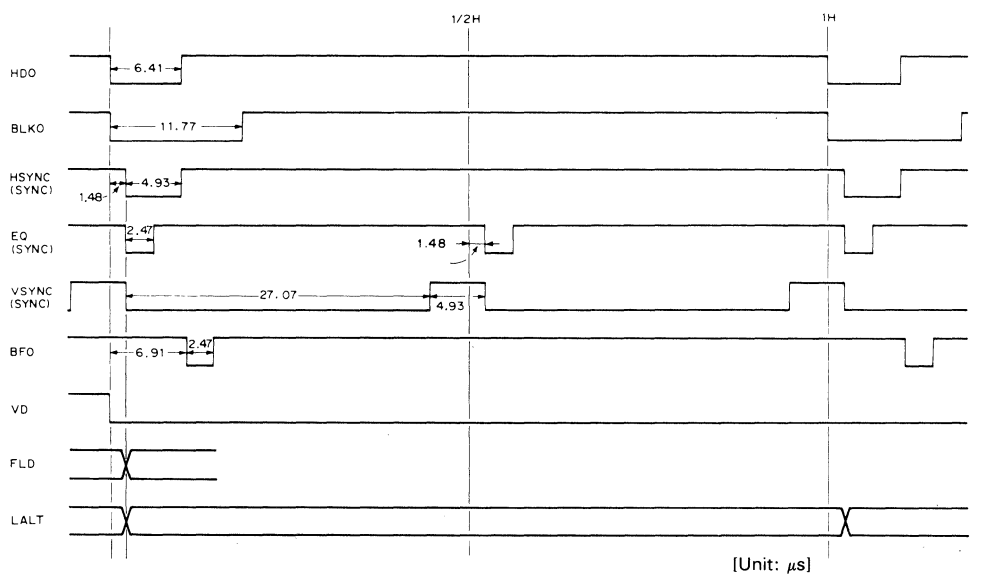
- LALT reset (LR)
  LALT is reset in the same phase as the LR input.
  The minimum reset pulse width is 32 μs.



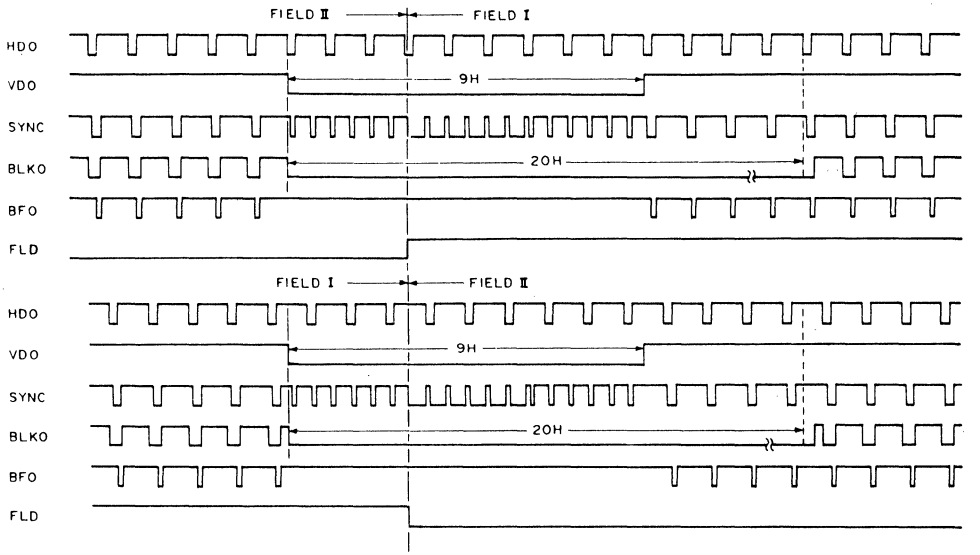
Timing Chart H (NTSC)



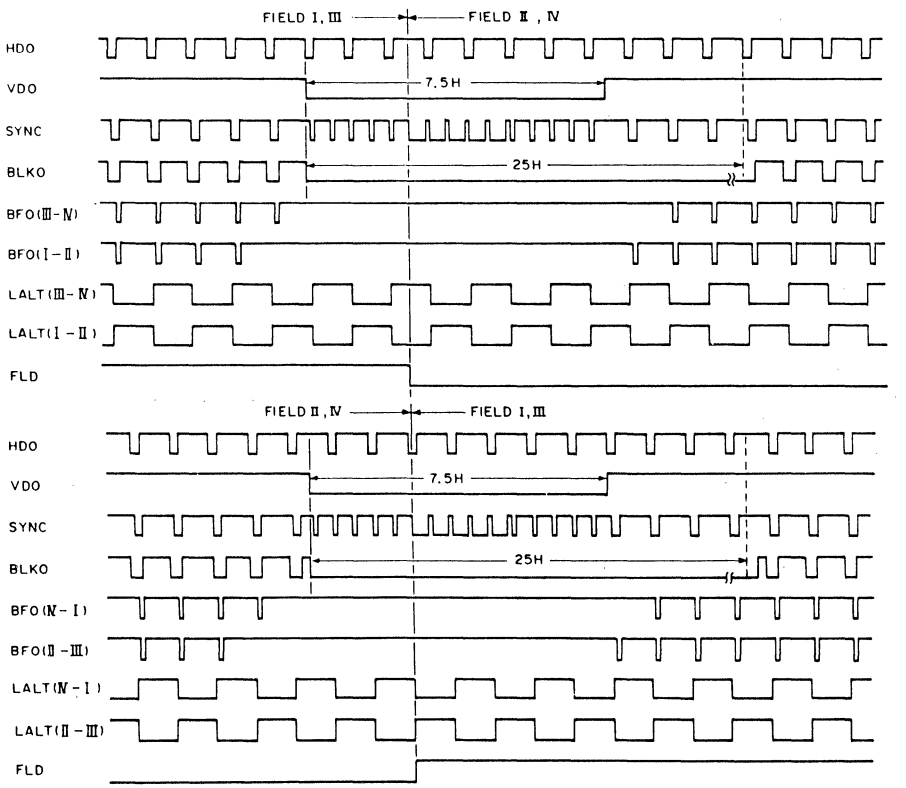
Timing Chart H (PAL)



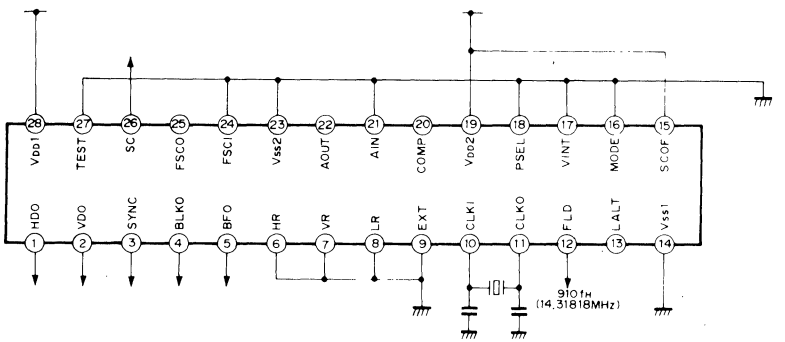
Timing Chart V (NTSC)



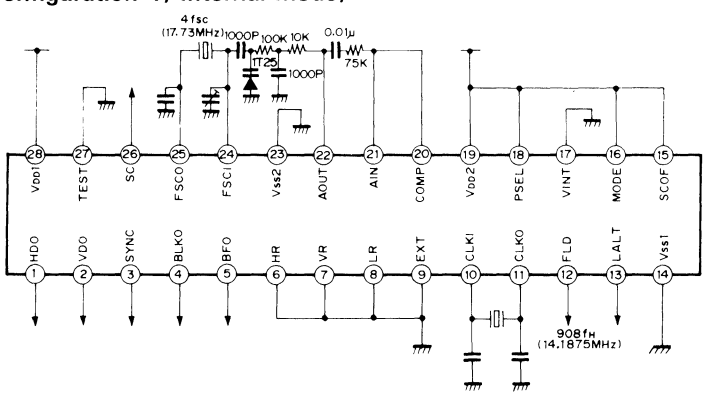
Timing Chart V (PAL)



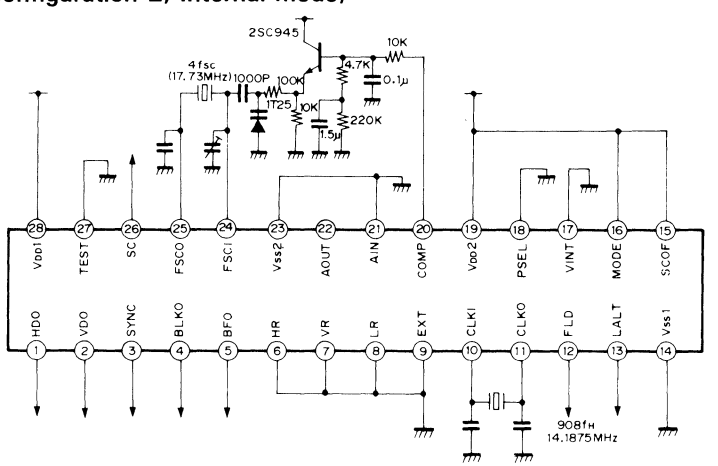
Application Circuits
NTSC (Internal mode)



PAL (Filter configuration 1, Internal mode)



PAL (Filter configuration 2, Internal mode)



Frequency Synthesizer PLL

Description

CXD1225M are used for the digital selection of TV broadcasting as well as AM, FM and various radio waves. These PLL IC's were developed through high speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is guaranteed as follows.
  CXD1225M } 300MHz
  Usage up to 1 GHz is possible when combined with an ECL (general purpose) prescaler.

- Programmable divider permits the division of a program frequency up to 1/262, 151
- Programmable reference divider permits the selection of comparison frequency at will.
  (E.G. Using a 4MHz crystal oscillator selection from 244Hz to 2MHz is possible)
- High-speed phase comparator provides high C/N ratio.
- Operation control through 3pins.
- 3 independent pins (AM1, FM1, TV1) are provided for the signal input at respective frequencies.
- Multipurpose output terminals are provided (A0, B0)
- Low consumption (Standard: 120W)

Structure

N-channel silicon gate MOS

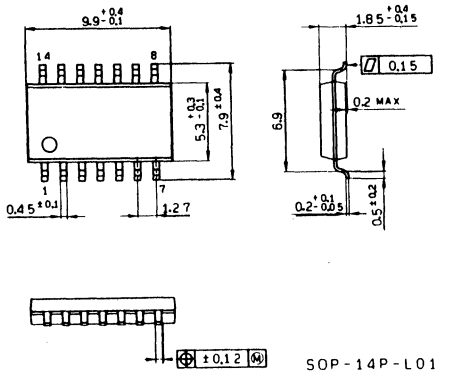
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Input pin voltage	V_{IN}	−1 to +7	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Starage temperature	T_{stg}	−55 to +150	°C

Package Outline

Unit: mm

CXD1225M 14pin SOP (Plastic)

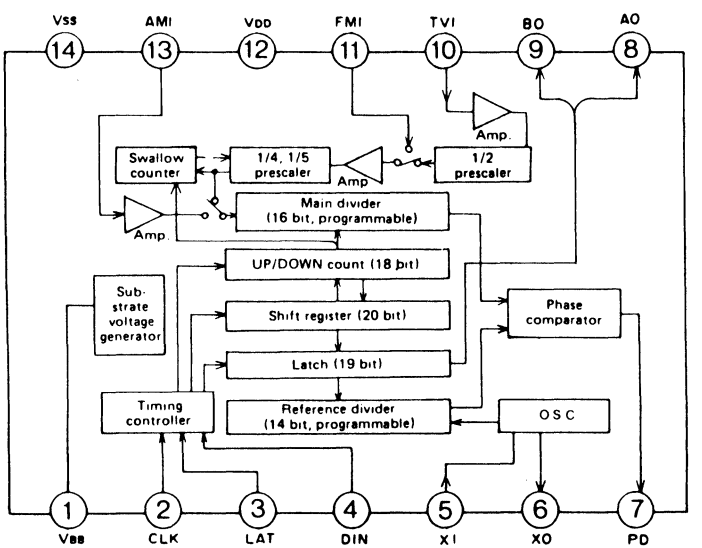


E89224-HP

Recommended Operating Conditions

Item	Pin Remarks	Symbol	Operating range	Unit
Supply voltage		V_{DD}	+4.5 to +5.5	V
High level input voltage	CLK, DIN LAT	V_{IH}	+2.6 to V_{DD} +0.5	V
Low level input voltage		V_{IL}	−1.0 to 0.8	V
High frequency signal input amplitude	TVI	e_{IN}	0.3 to 4.0	Vp-p
High frequency signal input amplitude	FMI	e_{IN}	0.2 to 4.0	Vp-p
High frequency signal input amplitude	AMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	XI	e_{IN}	0.6 to 4.0	Vp-p
Operating temperature		T_{opr}	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

No.	Symbol	Description
1	V_{BB}	Substrate pin. (Connect 0.01μF capacitor between this pin and GND)
2	CLK	Clock input pin for 20bit serial data input.
3	LAT	Latch signal input pin for shift register input data (latched with signal rise) Also, Up/Down clock input pin (state changes with signal rise)
4	DIN	Data input pin. Also, Up/Down mode select pin (Up at 'H' level, Down at 'L' level)
5	XI	Crystal oscillator connection pin for reference signal generation. (Max. 13MHz Standard 4.0MHz)
6	XO	
7	PD	Phase comparator output pin (3States)
8	AO	External control signal output pin/unlock output pin (E/E MOS push-pull)
9	BO	External control signal output pin/data check pin (E/E MOS push-pull)
10	TVI	High frequency signal input pin (Max. 300MHz) 1/2 prescaler built-in.
11	FMI	High frequency signal input pin (Max. 150MHz)
12	V_{DD}	Supply (+5V)
13	AMI	High frequency signal input pin (Max. 40MHz)
14	V_{SS}	Ground pin

Electrical Characteristics

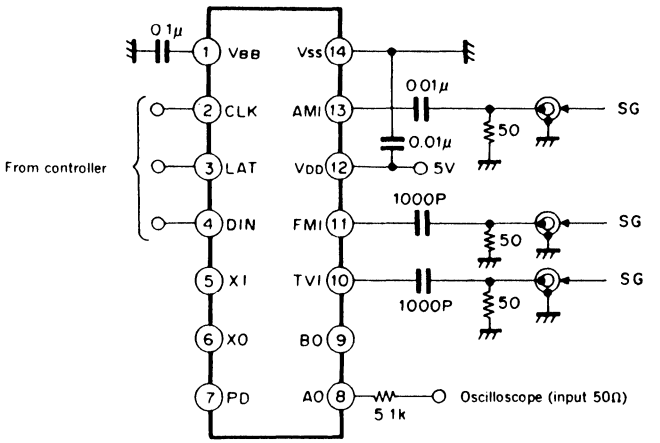
(Within Recommended Operation Conditions range, unless otherwise specified) V_{SS}=0V

Item	Pin, Remarks	Symbol	Conditions	CXD1225M			Unit
				min.	Typ.	Max.	
Operating supply current	V_{DD}	I_{DD}	Note2		24	40	mA
Operating input frequency	TVI	f_{OP}	e_{IN}=0.3 to 4.0Vp-p	20		300	MHz
	FMI	f_{OP}	e_{IN}=0.2 to 4.0Vp-p	20		150	MHz
	AMI	f_{OP}	e_{IN}=0.2 to 2.5Vp-p	0.05		40	MHz
Input leak current	Logic input	I_{IL}	V_{IH}=0 to VDD Note1	-10		+10	μA
High level output current	Phase comparator (3 value output) PD	I_{OH}	V_{OUT}=3V Note2			-0.2	mA
Low level output current		I_{OL}	V_{OUT}=1V Note2				mA
High impedance leak current		I_{HZ}	V_{OUT}=2V Note2	+0.2		+50	nA
High level output voltage	Push-pull by E/E MOS: Composition AO, BO	V_{OH}	I_{OH}=-20μA	-50			V
Low level output voltage		V_{OL}	I_{OL}=-1mA	2.8		0.6	V

Note 1) Ta=25°C

Note 2) V_{DD}=5V Ta=25°C

Operating Input Frequency Test Circuit



Control input data to CX-7925B/CXD1225M: T1-H, T2-H, A-L, B-H
SG: HP's 8640B
(Input level read directly at built-in level meter)

Operation

[1] Signal input from the local oscillator

CXD1225M use 3 independent input pins according to frequency and application.

- AMI pin
  Reception pin for AM and TV broadcast. Signal input up to 40MHz is warranted for CXD1225M. Frequency division ratio when using this pin is 1/2 to 1/65537.
- FMI pin
  Reception pin for FM and TV broadcast. Signal input up to 150MHz is warranted for CXD1225M. Accordingly, the external prescaler is not required for FM reception. For TV reception, the entire TV band width can be overed through combination with an external prescaler up to 1/8. Frequency division ratio ranges from 1/12 to 1/262151. When not in use this pin stays open.
- TVI pin
  This pin is solely used for TV broadcast reception. With the built-in 1/2 prescaler signal input up to 300MHz is warranted for CXD1225M. The entire bandwidth can be covered through combination with an external prescaler up to 1/4. Frequency division ratio ranges from 1/24 to 1/524302. When not in use this pin is grounded internally via a resistor of more than 100kΩ.

[2] Phase comparator output

The phase comparator output (PD pin) has a 3-level value. The pin is at High level when the input signal is more aduanced in phase than the reference signal. At Low level when the phase lags behind and at high impedance when they are in phase.

[3] Control signal and control system

CX-7925B/CXD1225M are designed as controllers compatible with general 4 or 8-bit microcomputers. There are 3 control input pins CLK, LAT, DIN and 2 control output pins AB and BO. Through the proper combination of these pins, the simplification and multi-functionalization of the system can be realized.

CX-7925B/CXD1225M feature 3 data input modes, (normal mode), Up/Down mode and Data check mode with different signal input patterns for each.

[3-1] Control signal input modes

(a) Data input mode (normal mode)

To set all initial values of CXD1225M a total of 40bit of data has to be input 20bits at a time. With LAT pin at Low, as data is input to DIN pin, data is input to the shift register 1 bit at a time with the rising edge of the clock input to CLK pin.

After 20bit of data has been transmitted to the shift register, with CLK at High as LAT pin is set to High, data is latched, (after data is latched, turn LAT pin back to Low, Varying DIN and CLK pins while LAT pin is at High may affect data internally).

As will be described in detail later on, input data is input either in the programmable divider or the reference divider according to the state of the last bitC. In practice input from the controller the 20bit of the data including first the reference divider frequency, input pin selection and AO, BO output pins data using the above methed. Here the data last bit is set to Low.

Next input 20bit including data used to set the programmable divider, in the same way. Here set the last bitC to High. This sets all internal states. After that, to vary only the programmable divider value, varying only the latter 20bit of data will suffice (In this case too, C is to be set to High).

To vary the programmable divider value (channel selection, AFT) the usage of Up/Down mode mentioned hereafter will improve efficiency.

(b) UP/DOWN mode

After setting CLK pin to Low, the contents of UP/DOWN counter can be increased or decreased by one according to DIN pin High, Low level. This by turning LAT pin (normally at Low level) from High to Low. By repeating this process the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

This mode is used to check if data has been correctly input from the controller to the data register. Data left in the shift register immediately after input data has been latched is output bit by bit from BO pin. This at the rising edge of a clock input pin and at to CLK pin while it is held to High and after LAT pin is set to Low. The shift register data can only be output from BO pin when bits T1 and T2 of the data are at High and Low, respectively.

[3-2] Control data assignment

CZD1225M is assigned in 20bits. The last 20bits are the data identification code. Identifying the code will tell the data contents. Though unrelated to users, switching to Test mode is also performed using this code. Each of the programmable divider and reference divider frequency number is given in binary value with LSB at the leading digit.

(a) Control input data of the Reference divider (C=Low)

This can be described as the initialization setting data. It is always input when power is fed or when a channel band is switched. The input data composition is as follows.

	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	PI1	PI2	A	B	T1	C
	LSB													MSB						

- R0 to R13 ; Reference divider frequency division numbers. (binary value with R0 as LSB)
  There is an offset element between the input data and the actual frequency division numbers. The relationship being (actual frequency division numbers)=(Input data+2)
- PI1, PI2 ; Specification of the signal input pin.

Input / PI1, PI2	AMI	FMI	TVI
PI1	—	L	H
PI2	L	H	H

• A, B, T1 ; Each of AO and BO pins features 2 functions selected according to T1 value. When T1 is at Low, A and B values are output as they are to AO and BO pins. These signals can be used to select the prescaler frequency division, the filter constant, the channel band signal and various other purposes. When the prescaler M54465P (mitsubishi) for TV reception is used the following selection codes for frequency division ratio apply.

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at High, AO output pin outputs the phase comparator LOCK/UNLOCK state.
AO pin H; UNLOCK
L; LOCK
BO pin becomes, as described in Paragraph(3-1)C for Data check mode, the shift register data output pin. Through the clock input to CLK pin the shift register content is continuously output. Note that when T1 is at High, AO and BO pins can not be used for external control.

• C ; This code determines the latch direction of the input data. In this case, set to Low.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C=High)
This data determines the Programmable divider frequency division ratio.

N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C

LSB MSB

• N0 to N17; Programmable divider frequen division numbers. (Binary value with N0 as LSB) The actual frequency division number differs according to the pin selected for the signal input as follows.

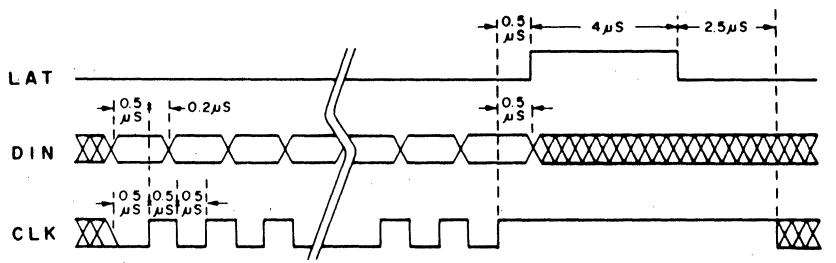
Control data		Input pin	N frequency division input data range	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
—	L	AMI	0 to 65535	N+2	2 to 65537
L	H	FMI	4 to 262143	N+8	12 to 262151
H	H	TVI	4 to 262143	2 • (N+8)	24 to 524302

- T2 ; T2 is used for Test mode selection. Users usually set this data to Low. To test the frequency division output and reference output this T2 bit and afore mentioned T1 bit are set to High while A and B bits are set to Low. Then, a reference output and a frequency division output can be observed at AO and Bo pins respectively.
- C ; As described before, set to High in this case.

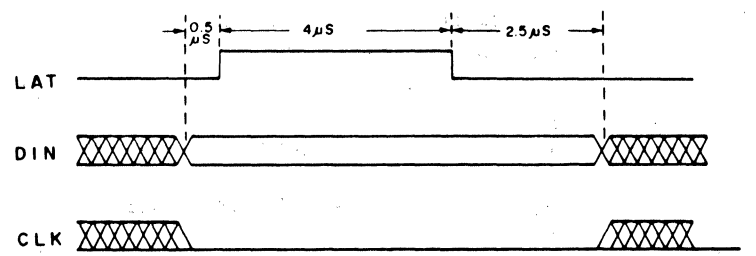
[3-3] Data input and control signal timing

(a) Data input mode (normal mode)

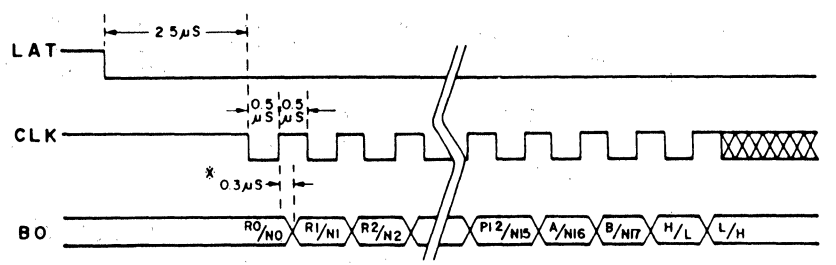
Various timings show the minimum value unless otherwise indicated.



(b) UP/DOWN mode



(c) DATA CHECK mode (Shift register data check)



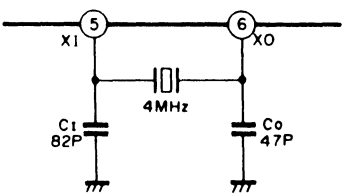
(※ Mark indicates data is output within this timing)

(4) Reference signal (Reference divider input signal)

The connection of a chrystal oscillator to X1 and XO allow these IC's to generate reference signals. The input of an external clock signal to X1 pin permits the usage of an external clock as reference signal.

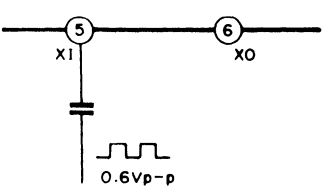
(4-1) Reference signal generation by means of built-in oscillator

Connect a chrystal oscillator with a frequency of 1MHz to 13MHz to X1 and XO pins, as shown below. The diagram below shows an example where a standard 4MHz osillator is used. The capacitance ratio of C_1, C_O should be 1 to 2 : 1 while their serial capacitance values should be the specific load capacitance of the chrystal oscillator.

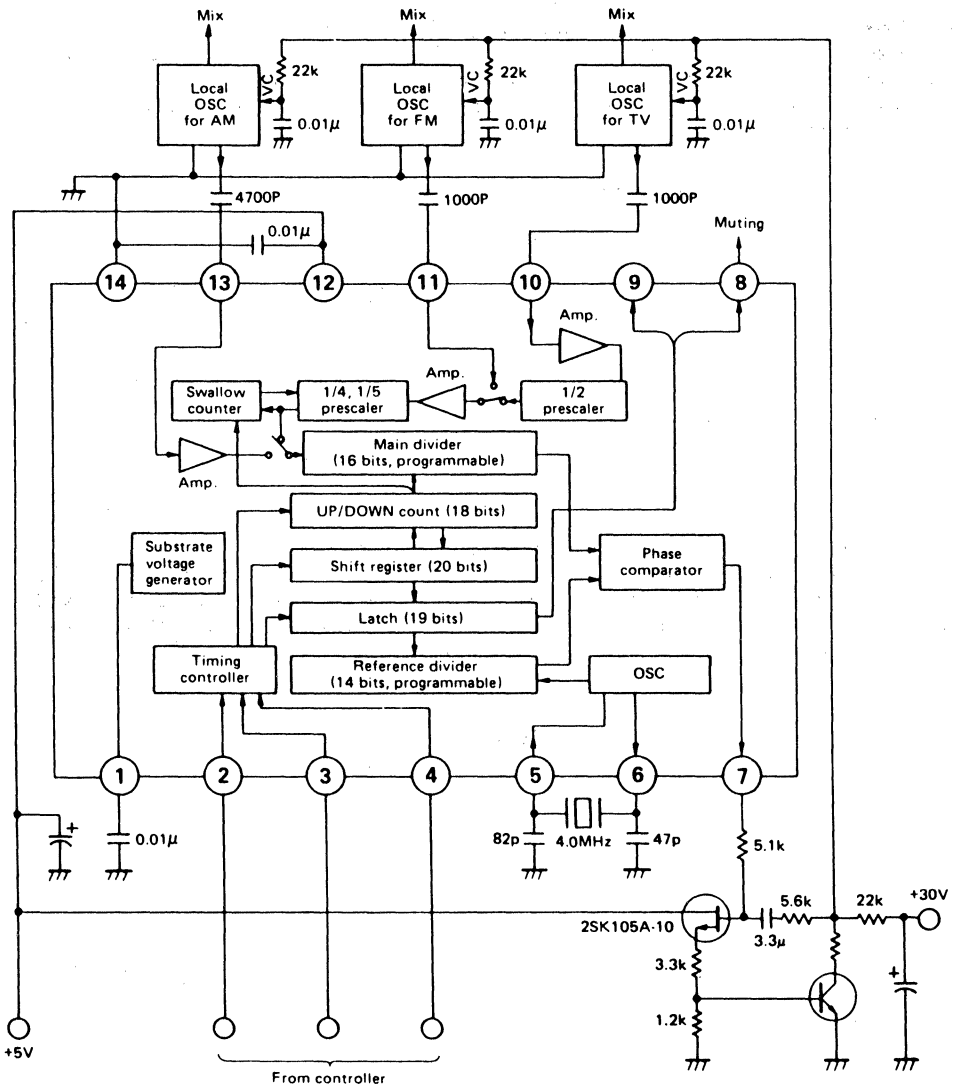


(4-2) Reference signal generation by means of external clock

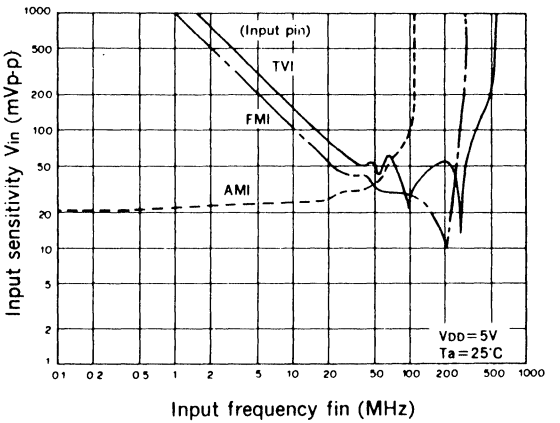
When an external clock signal, such as a clock signal obtained from the controller is to be used as reference clock, input it to X1 pin via a capacitor as shown below. The clock frequency range is guaranteed up to 13MHz. However, the usage of a signal with proper rise and fall (over 5V/μs) is recommended especially when the frequency is low. This is to prevent malfunction.



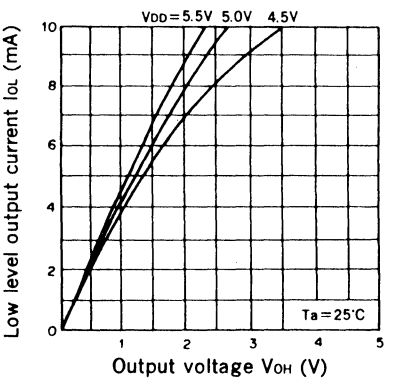
Application Circuit

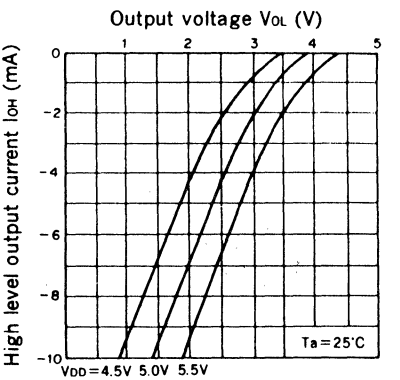


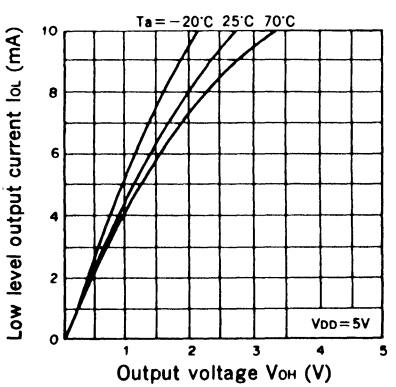
High Frequency Input Sensitivity Characteristics

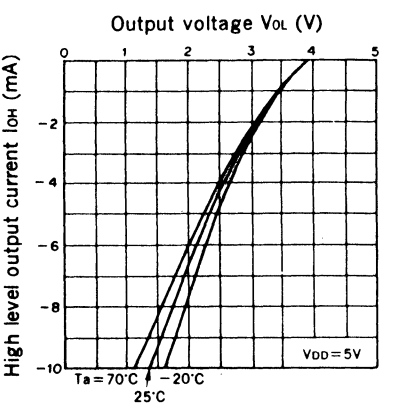


AO, BO pins Output Current Characteristics

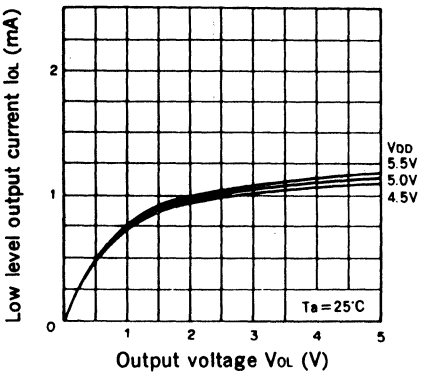


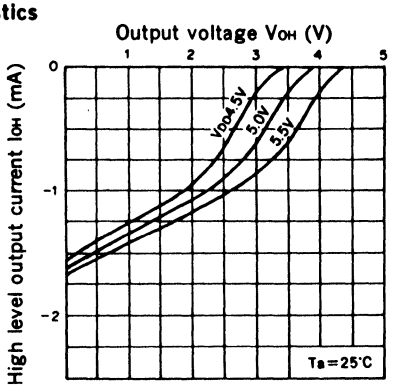


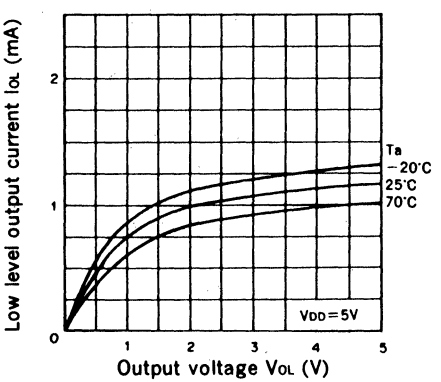


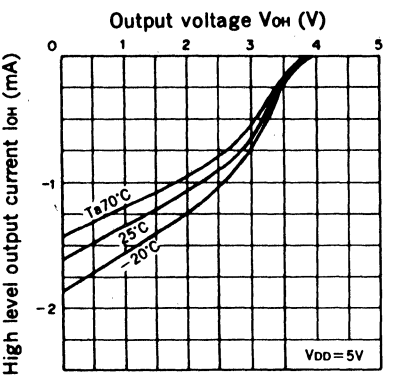


PD (Phase Comparator) pin Output Current Characteristics

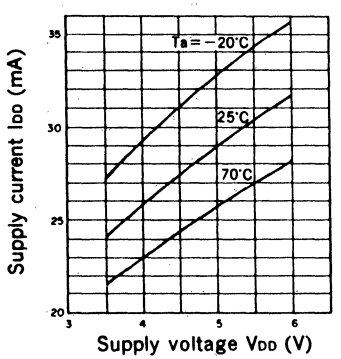








Supply Current I_{DD} and Voltage Characteristics



SONY CXD1229Q

Sync Separation and AFC for Digital Video Processing

Description

The CXD1229Q consists of a sync separation circuit best suited for digital video processors and an AFC that outputs $910f_H$ clocks.

Features

- Double action sync separation circuit copes well with noise and APL fluctuations.
- Fully synchronous AFC circuit. ($910f_H$ generator)
- VD detection circuit does not malfunction when dealing with nonstandard signals.
- First field and second field (ODD/EVEN) discrimination circuit.

Applications

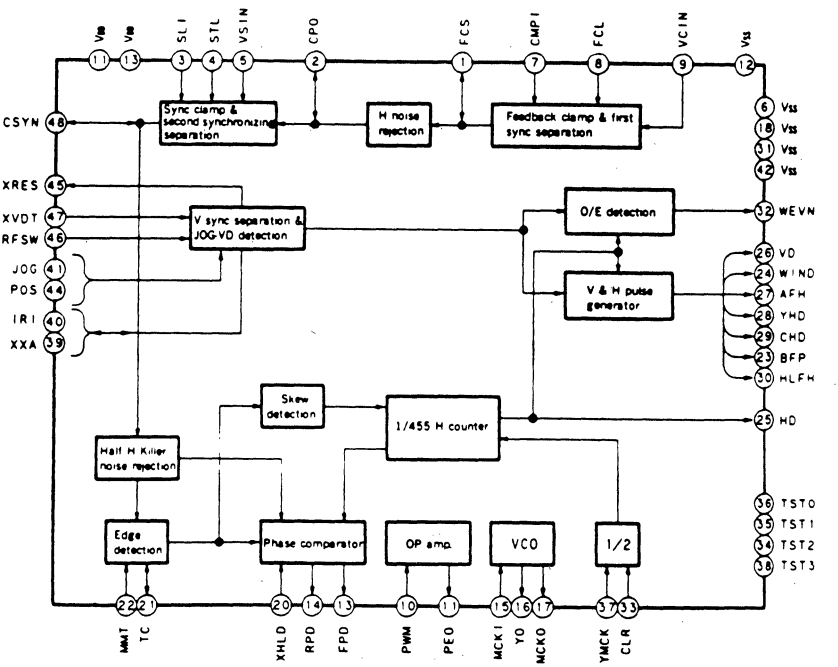
Digital video processor, digital VCR, digital TV

48pin QFP (Plastic)

Structure

Silicon gate CMOS IC

Block Diagram



8/91 version

E89428A0Y-HP

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}		$V_{SS}-0.5$ to $+6.0$	V
• Input voltage	V_I		$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O		$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{stg}		-25 to $+85$	°C
• Storage temperature	T_{stg}		-40 to $+125$	°C
• Output current	I_O	$V_O=V_{DD}$	(Max.) $+70$mA	
		$V_O=0$V	(Max.) -40mA	

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25 (Typ. 5.00)	V
• Operating temperature	T_{opr}	0 to $+70$	°C
• H level output current	V_{OH}	$-$ 0.4 (Max.) -0.4mA	
• L level output current	V_{OL}	(Max.) $+10$mA	

Pin Description

AI: Analog input, AO: Analog output

Pins No.	Symbol	I/O	Description
1	FCS	I/O	Sync separation output of feedback clamp system. (Test monitor)
2	CPO	I/O	Clamp pulse monitor pin for sync clamp.
3	SLI	AI	Slice level of sync clamp system.
4	STL	AI	Sync chip level of sync clamp system.
5	VSIN	AI	Video input of sync clamp system.
6	V_{SS}	—	GND
7	CMPI	AI	Slice level of feedback clamp system.
8	FCL	AI	Sync chip level of feedback clamp system.
9	VCIN	AI	Video input of feedback clamp system.
10	PWM	AI	Operational amplifier input.
11	PEO	AO	Operational amplifier output.
12	V_{SS}	—	GND
13	FPD	O	Phase comparison output of sync rise and built-in H counter. (Phase error output of AFC sub loop)
14	RPD	O	Phase comparison output of sync bottom line and built-in H counter. (Phase error output of AFC main loop)
15	MCKI	I	Inverter input for VCO.
16	YO	O	Inverter output for VCO.
17	MCKO	O	$910f_H$ output. Logically, equivalent to YO.
18	V_{SS}	—	GND
19	V_{DD}	—	+5V
20	XHLD	I	Normally at "H". "H": AFC error, active "L": AFC error, hold
21	TC	I/O	Fine adjustment of AFC lock phase. Pin13 (FPD) pulse width is altered through the connection of a time constant to this pin to enable fine adjustment of Pin27 (AFH) lock phase.
22	MMT	I	Normally at "H". (Built-in monostable multivibrator testing pin.)
23	BFP	O	Burst, flag, pulse output pin.
24	WIND	O	Window pulse for V-PLL. (Connect to CXD1228)

Pins No.	Symbol	I/O	Description
25	HD	I/O	AFC direct output. (Monitor pin for testing)
26	VD	O	Vertical sync output. (Connect to CXD1228)
27	AFH	O	AFC HD output. (Connect to CXD1226/1228)
28	YHD	O	Timing output for pedestal clamp. (Connect to CXD1226)
29	CHD	O	Timing output for burst detection. (Connet to CXD1226)
30	HLFH	O	$1/2f_H$ ($\fallingdotseq$7.5kHz) output (For PAL APC correction)
31	V_{SS}	—	GND
32	WEVN	O	ODD/EVEN detection outputs. "H": First and third fields. (Connect to CXD1226/1228)
33	CLR	I	Normally at "L"
34	TST2	I	Rough adjustment of AFC lock phase. Pin27 (AFH) phase changes by approx. 420nsec, everytime 1 bit changes.
35	TST1	I	
36	TNTO	I	Normally at "L". ("H": Test mode)
37	YMCK	I	Master clock input. (This pin is not internally connected to MCKO.)
38	TST3	I	Normally at "L". ("H": Test mode)
39	XXA	I/O	Monitor pin for testing.
40	IR1	I/O	
41	JOG	I	"H": VD generated from RFSW input "L": VD generated from video input (XVDT In to be precise).
42	V_{SS}	—	GND
43	V_{DD}	—	+5V
44	POS	I	Phase difference between RFSW and VD when VD is generated from RFSW. ("H": 7H, "L": 6H)
45	XRES	O	V-Det LPF output. (Monitor pin for testing)
46	RFSW	I	RFSWP input.
47	XVDT	I	Composite sync input of V-Det system. Connect to "CSYN".
48	CSYN	I/O	Sync separation output of sync clamp system.

Electrical Characteristics

1) DC characteristics

$V_{DD}=5V\pm5\%$, $V_{SS}=0V$, $T_{opr}=0$ to $+70°C$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	V_{DDS}	At stand still			0.1	mA
Digital output voltage H level	V_{OH}	$I_{OH}=-0.4mA$	4.2		V_{DD}	V
Digital output voltage L level	V_{OL1}	$I_{OL}=3.2mA$	V_{SS}		0.4	V
	V_{OL2}	$I_{OL}=10mA$	V_{SS}		0.5	V
Analog output voltage	A_{OUT}	I/O pin of operational amplifier connected to IC external part. CLR=1	$0.48\times V_{DD}$	$0.5\times V_{DD}$	$0.52\times V_{DD}$	V
Input voltage H level	V_{IH1}	TTL level	2.2		V_{DD}	V
		CMOS level	$V_{DD}\times0.7$		V_{DD}	
Input voltage L level	V_{IH2}	TTL level	V_{SS}		0.8	V
		CMOS level	V_{SS}		$V_{DD}\times0.3$	
Input leakage current	I_{LI}	$V_I=0$ to V_{DD} (All input pins)	−10		10	μA

* $1V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$

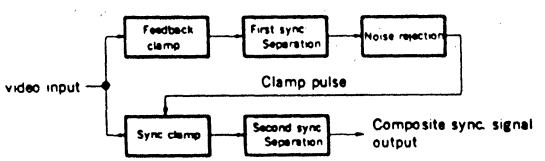
2) I/O capacitance

$V_{DD}=V_I=0V$, $f_M=1MHz$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}	$T_A=25°C$	—	—	9	pF
Output pin	C_{OUT}	$T_A=25°C$	—	—	16	pF
Input/Output pin	$C_{I/O}$	$T_A=25°C$	—	—	21	pF

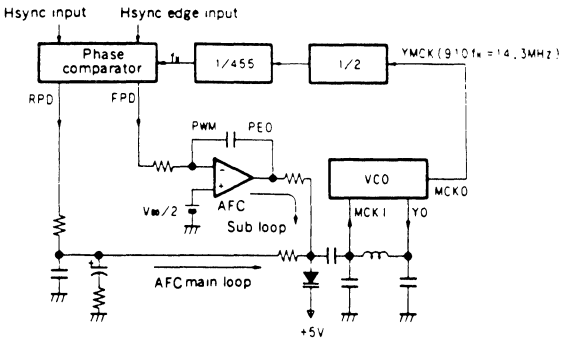
Description of Functions

(1) Sync separation



The video input signal passes through feedback clamp, first sync separation and after noise elimination, clamp pulse is formed. With this clamp pulse, the video input signal is sync clamped and the second sync separation performed.
With this double sync separation circuit structure, a sync separation circuit resistant to noise and APL fluctuations is realized.

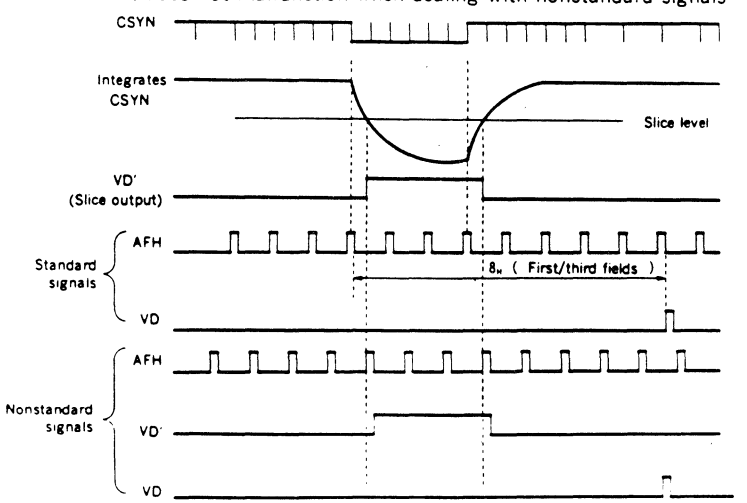
(2) Fully synchronous AFC circuit ($910f_H$ circuit)



Input H sync, that edge and VCO ($\approx 910f_H$) counted down to 1/910 are phase compared. There are 2 such error outputs: RPD: phase comparison output between all sync bottom line and the built-in H counter, and FPD: between sync rising edge and the built-in H counter. RPD output is a lag-lead filter and FPD output is an integrator. Both outputs are converted into DC error respectively.

The added value is applied to a variable capacitor and VCO oscillation frequency maintained at a stable $910f_H$.

(3) VD detection circuit does not malfunction when dealing with nonstandard signals



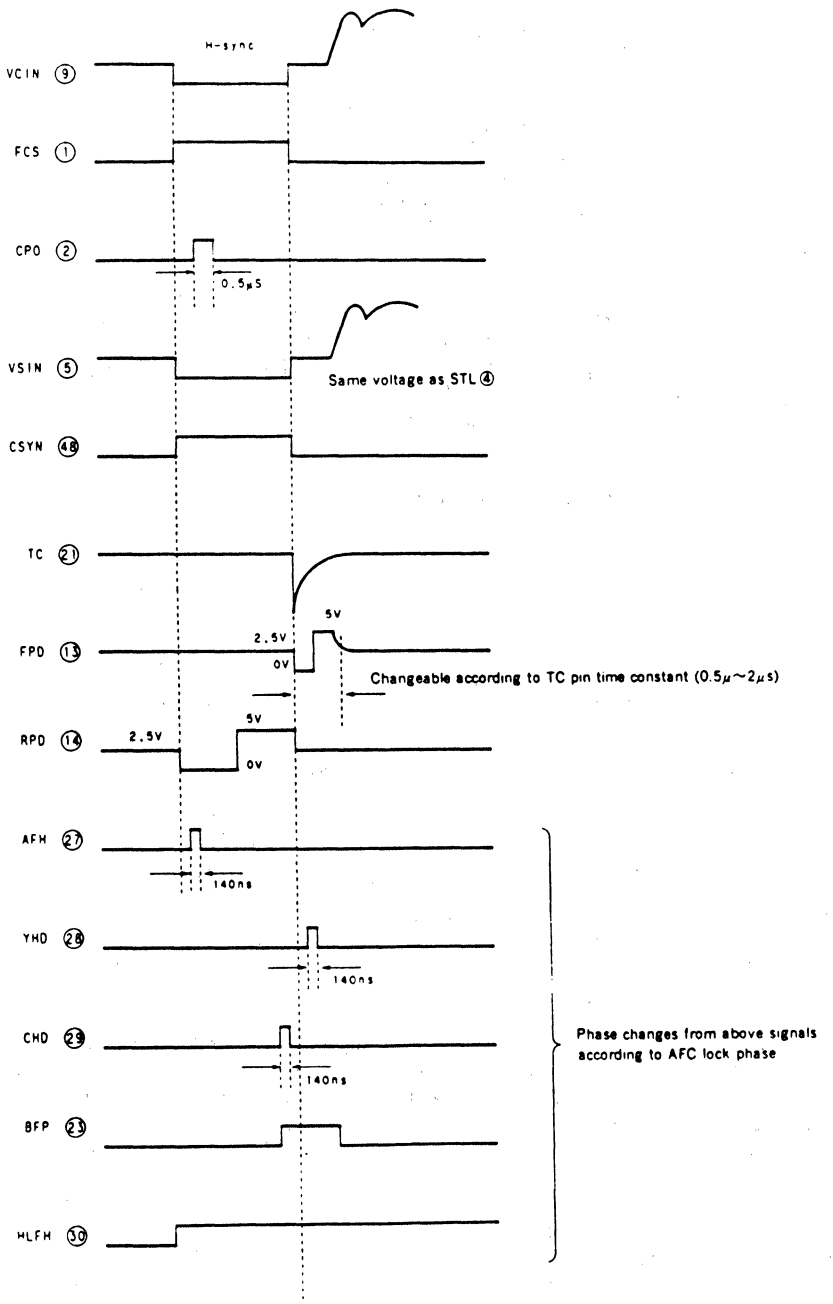
CSYNC is integrated sliced and VD obtained. This VD is resampled at AFH and VD formed. With a standard signal, as shown in the above diagram, a stable VD is obtained. However, in nonstandard signals, the relation between H sync and V sync is not constant. VD rise and AFH overlap and in some cases a stable VD output cannot be obtained. In such cases, CXD1229 varies the slice level and automatically prevents AFH and VD from overlapping to obtain a stable VD output. During variable speed PB in personal computers and VCR's a stable VD output can also be expected.

(4) First field and second field discrimination

When there is no H sync signal in the delay pulse that comes within a constant period from the V sync signal, it is discriminated as the first and third field. If there is a signal then it is discriminated as the second and fourth field and output from Pin WEVN (Pin32). (For "H": first, third field)

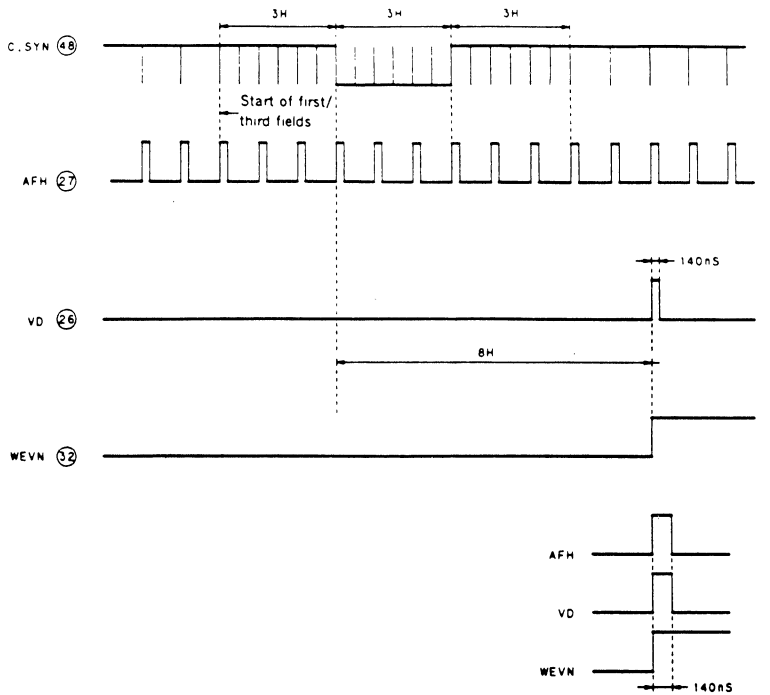
Timing chart

(1) Pin changes by H.

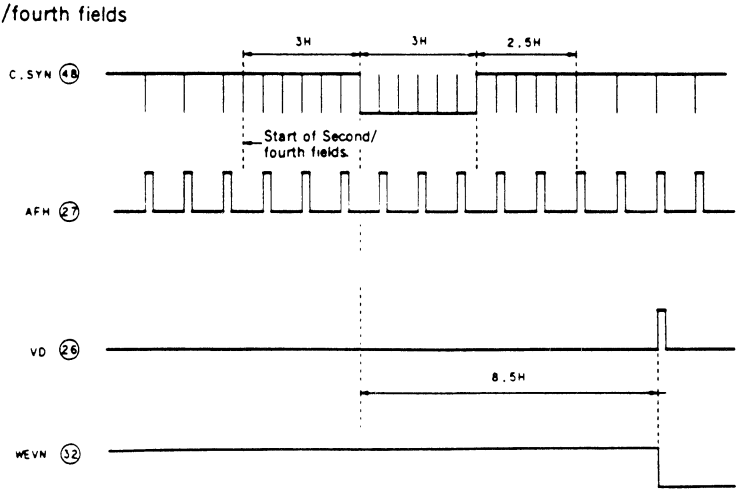


Pin changes by field

- First/third fields

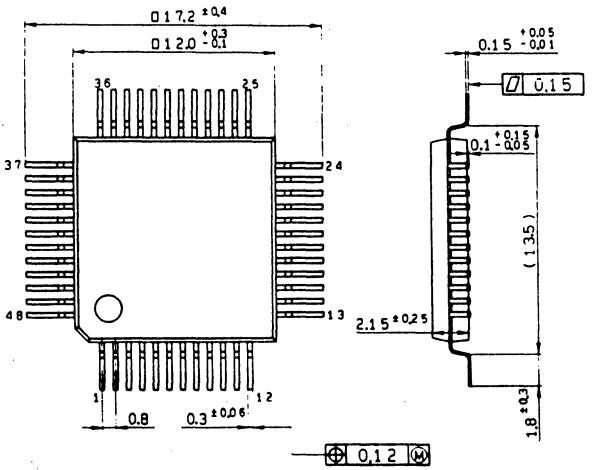


- Second/fourth fields



Package Outline Unit : mm

48pin QFP (Plastic) 0.7g



QFP-48P-L021

SONY®

CXA1496AQ

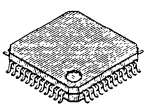
10-bit 20MSPS A/D Converter

Description

The CXA1496AQ is a 10-bit 20MSPS 2-step parallel type A/D converter for video signal processing.

This A/D converter operates on a dual ±5V power supply. The external addition of sample and hold, reference power supply and clock timing circuits permit the conversion of analog signals into digital signals.

48 pin QFP (Plastic)



Features

- Maximum operating frequency 20MHz (Min.)
- Integral linearity error 10-bit ± 1.5LSB
- Differential linearity error 10-bit ± 1LSB
- Low power consumption 310mW (Typ.)
- Wide band analog input 10MHz
- Low input capacity 150pF (Typ.)
- Built-in digital correction
  (Compensation within a range of ± 16LSB)
- TTL input (CLK only: ECL LIKE)
- TTL output (3-state control)
- Output code Binary/2S complement/
  1S complement

Function

10-bit 20MSPS 2-step parallel type A/D converter

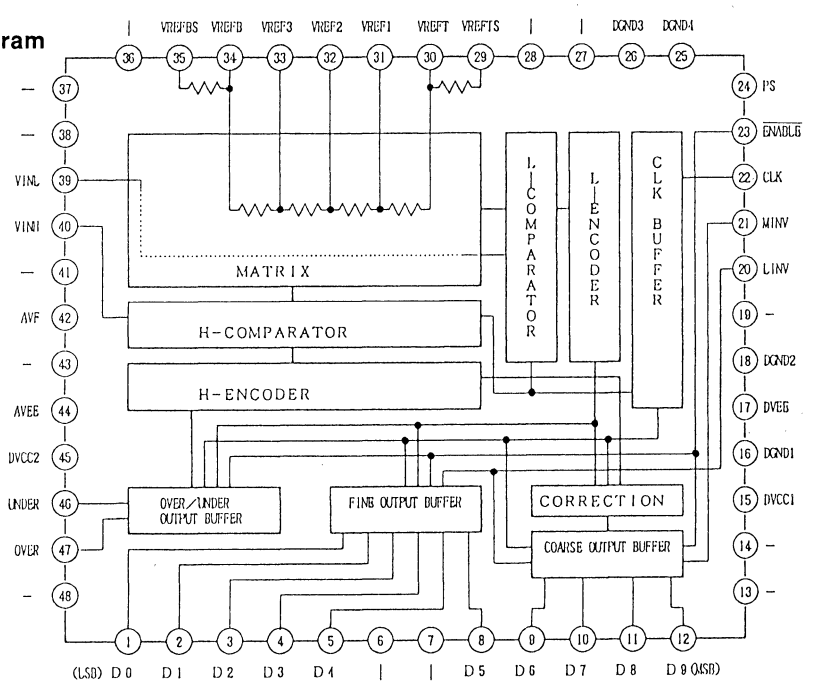
Structure

Bipolar silicon monolithic IC

Applications

High resolution video signal processing

Block Diagram

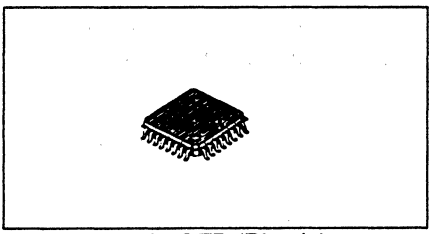


SONY

CXA1693Q

Advanced Information

High Speed Sample and Hold IC



32 pin QFP (Plastic)

Description

The CXA1693Q performs high speed sample and hold of video and various type of signals.

Features

- Maximum sampling frequency
  40MHz (Minimum)
- Built-in -2V constant voltage circuit.
- Built-in clock pulse generating circuit for
  A/D converter
- Low power consumption
  180mW (Typical)

Absolute Maximum Ratings (Ta=25 °C)

• Supply Voltage	V_{CC}	7	V
	Vee	-7	V
• Write current	Iw	50	mA
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power dissipation	P_D	375	mW

Structure

BiPolar silicon monolithic IC.

Operating Conditions

• Supply Voltage	V_{CC}	4.75 to 5.25	V
	Vee	-4.75 to 5.25	V

Application

Usage in combination with the CXA1694Q or CXA1496Q can simplify peripheral circuit design for A/D conversion.

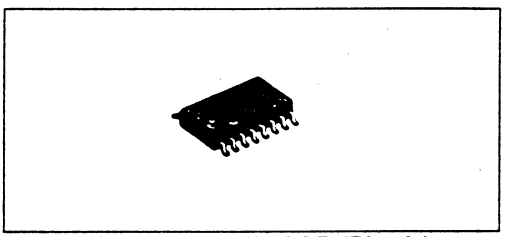
SONY

CXD1172AM/AP

6-bit 20MSPS Video A/D Converter (CMOS)

Description

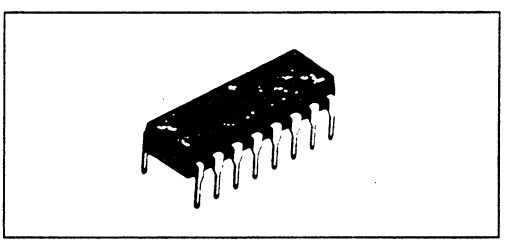
The CXD1172A is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low power consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS is typical.



CXD1172AM 16pin SOP (Plastic)

Features

- Resolution 6-bit ± 1/2 LSB
- Max. sampling frequency 20MSPS
- Low power consumption
  40mW (at 20MSPS Typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- 3-state TTL compatible output.
- Power supply 5V single
- Low input capacity 4pF
- Reference impedance 300Ω (Typ.)
- Pin replaceable with CXD1172.



CXD1172AP 16pin DIP (Plastic)

Structure

Silicon gate CMOS monolithic IC.

Applications

TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RS}	V_{DD} to V_{SS}	V
• Analog Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Digital Input voltage	C_{LK}	V_{DD} to V_{SS}	V
• Digital output voltage	V_{CH}, V_{OL}	V_{DD} to V_{SS}	V
• Storage temperature	Tstg	-55 to +150	°C

SONY

CXD1176Q

8-bit 20MSPS Video A/D converter with Clamp Function

Description

The CXD1176Q is an 8-bit CMOS A/D converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20MSPS.

Features

- Resolution power···8-bit ± 1/2 LSB (DL)
- Max. sampling frequency···20MSPS
- Low power consumption···60mW
  (at 20MSPS Typ.)
  (Reference current excluded)
- Built-in sync type clamp function
- Built-in monostable multivibrator for clamp pulse generation
- Built-in sync pulse polarity selection function
- Clamp pulse direct input possible
- Built-in clamp ON/OFF function
- Built-in reference voltage self bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5V power supply
- Low input capacity···11pF
- Reference impedance···300 Ω (Typ.)

Applications

TV and VCR digital systems and a wide range of applications where high speed A/D conversion is required.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} to Vss	V
• Input voltage (Analog)	V_{IN}	V_{DD} to Vss	V
• Input voltage (Digital)	V_{IH} V_{IL}	V_{DD} to Vss	V
• Output voltage (Digital)	V_{OH} V_{OL}	V_{DD} to Vss	V
• Storage temperature	Tstg	− 55 to + 150	°C

Recommended Operating Conditions

• Supply voltage			
	AV_{DD}, AVss DV_{DD}, DVss	4.75 to 5.25	V
	| DGND − AGND |	0 to 100	mV
• Reference input voltage			
	V_{RB}	0 to	V
	V_{RT}	to 2.7	V
• Analog input	V_{IN}	1.8Vp-p above	
• Clock pulse width	T_{PWI}···25 (min)		ns
	T_{PWO}···25 (min)		ns
• Operating ambient temperature	Topr	− 20 to + 75	°C

SONY

CXD1179Q

Preliminary

8-bit 35MSPS Video A/D Converter with Clamp Function

Description

The CXD1179Q is an 8-bit CMOS A/D Converter for video use that has a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 35MSPS.

32 pin QFP (Plastic)

Features

- Resolution power; 8-bit+ 1/2 LSB (DL)
- Max. sampling frequency; 35MSPS
- Low power consumption; 100mW (at 35MSPS Type.) (Reference current excluded).
- Built-in sync type clamp function.
- Built-in monostable multivibrator for clamp pulse generation.
- Built-in sync pulse polarity selection function.
- Clamp pulse direct input possible.
- Built-in clamp ON/OFF function.
- Built-in reference voltage self bias circuit.
- Input CMOS compatible.
- 3-state TTL compatible output.
- Single 5V power supply.
- Low input capacity; 11pF
- Reference impedance; 300Ω (Typ.)

Applications

Wide range of applications where high speed A/D conversion is required.

Structure

Silicon gate CMOS IC.

Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RS}	V_{DD} to V_{SS}	V
• Input voltage (Analog)	V_{IN}	V_{DD} to V_{SS}	V
• Input voltage (Digital)	V_{IH} (V_{IL})	V_{DD} to V_{SS}	V
• Output voltage (Digital)	V_{CH} (V_{OL})	V_{DD} to V_{SS}	V
• Storage temperature	Tstg	-55 to +150	°C

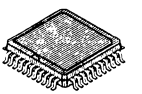
8bit 500MSPS Single VIDEO DAC (ECL input)

Description

The CXA1236Q is an ultra high-speed D/A converter that multiplexes two 8-bit input data.

This IC realizes a maximum conversion speed of 500MSPS and is suitable for signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems and others.

44 pin QFP (Ceramic)



Features

- Ultra high-speed
  : 500MSPS, multiplexed input
- High resolution: 8bit
- Low power consumption
  : 1W (for $V_{EE} = -4.5V$)
- Video control input
  : Sync, Blank, Ref. White, Bright
- ECL 100K and 10K compatible input
- Can drive 25Ω, 37.5Ω, 50Ω, and 75Ω loads
- Differential current output
- RS-343A compatible output
- −5.5 to −4.2V range single power supply operation

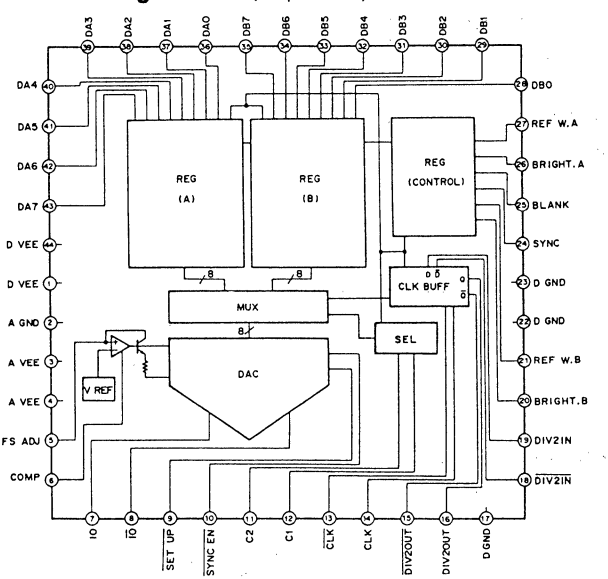
Functions

8bit 500MSPS Single VIDEO D/A Converter

Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration (Top View)



E89932B12 – ST

SONY

CXD1178Q

8-bit 40MSPS RGB 3-Channel D/A Converter

Preliminary

Description

The CXD1178Q is an 8-bit high-speed D/A converter for video band use. It has an input / output equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, and others.

48 pin QFP (Plastic)

Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- RGB 3-channel input/output
- Differential linearity error +0.25LSB
- Low power consumption 240mW (200Ω load at 2Vp-p output)
- Single 5V power supply
- Low glitch noise

Structure

Silicon gate CMOS IC

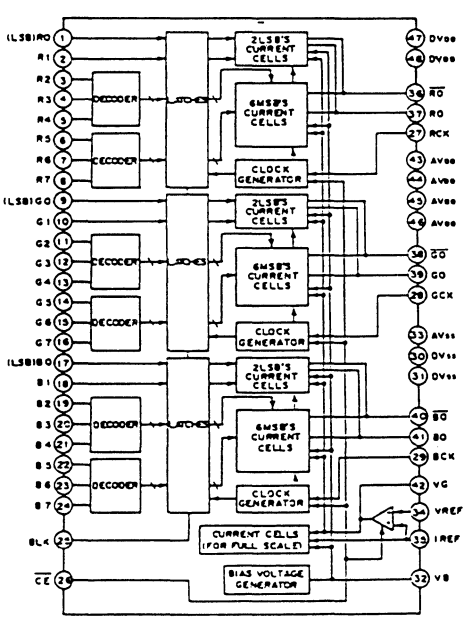
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AVss	4.75 to 5.25	V
	DV_{DD}, DVss	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	T_{PW1}	12.5 (Min.)	ns
	T_{PW0}	12.5 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to Vss	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	−55 to +150	°C

Block Diagram

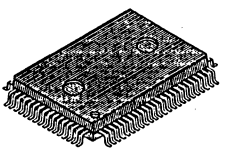


Digital Comb filter

Description

The CXD2011Q is an adaptive comb filter compatible with both NTSC and PAL systems and provides good Y/C separation capability.

80 pin QFP (Plastic)



Features

- Y/C separation by adaptive processing
- Has two built-in 1H delay lines
- Under the PAL system, a comb filter can be easily realized by combined use of the CXD2011Q with a CXK1202S or CXK1203Q.
- Clock 4fsc, 8-bit configuration

Structure

Silicon gate CMOS IC

Application

Y/C separation for color TV and VCR

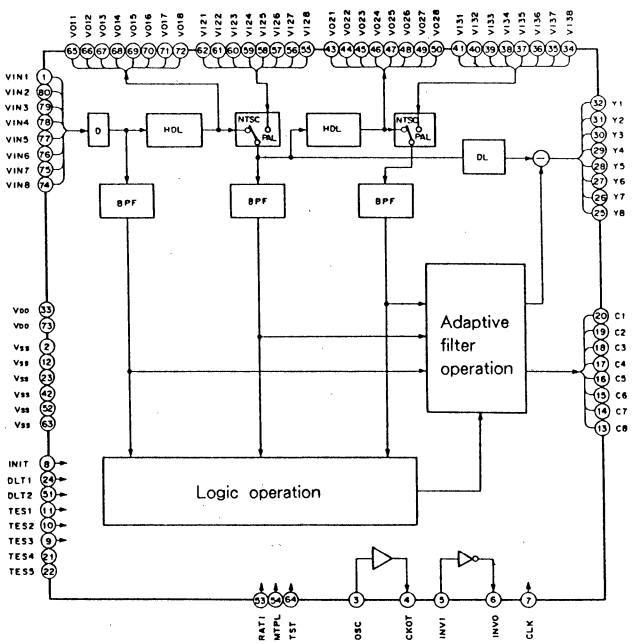
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	Vss–0.5 to +7.0	V
• Input voltage	V_I	Vss–0.5 to V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	VIN7	I	Composite signal input (MSB)
2	Vss	——	GND
3	OSC	I	Clock amplifier input
4	CKOT	O	Clock amplifier output
5	INVI	I	Inverter input
6	INVO	O	Inverter output
7	CLK	I	Clock input
8	INIT	I	Test pins to be set at L level
9	TES3	I	
10	TES2	I	
11	TES1	I	
12	Vss	——	GND
13	C0	O	(LSB)
14	C1	O	Chrominance signal output
15	C2	O	
16	C3	O	
17	C4	O	
18	C5	O	
19	C6	O	
20	C7	O	(MSB)
21	TES4	O	Test pins to be open
22	TES5	O	
23	Vss	——	GND
24	DLT1	I	Test pin to be set at L level
25	Y0	O	(LSB)
26	Y1	O	Luminance signal
27	Y2	O	
28	Y3	O	
29	Y4	O	
30	Y5	O	
31	Y6	O	
32	Y7	O	(MSB)
33	V_{DD}	——	+5V

Pin No.	Symbol	I/O	Description
34	VI30	I	(LSB)
35	VI31	I	
36	VI32	I	
37	VI33	I	Under the PAL system, the signals which are VO20 through 27 delayed 1H by external line memory are to be input.
38	VI34	I	
39	VI35	I	
40	VI36	I	
41	VI37	I	(MSB)
42	Vss	—	GND
43	VO27	O	(MSB)
44	VO26	O	
45	VO25	O	
46	VO24	O	Built-in line memory output 2
47	VO23	O	
48	VO22	O	
49	VO21	O	
50	VO20	O	(LSB)
51	DLT2	I	Test pin to be set at L level
52	Vss	—	GND
53	RATI	I	Internal coefficient switchover: "L" for NTSC, "H" for PAL
54	NTPL	I	NTSC/PAL switchover: "L" for NTSC, "H" for PAL
55	VI20	I	(LSB)
56	VI21	I	
57	VI22	I	
58	VI23	I	Under the PAL system, the signals which are VO10 through 17 delayed 1H by external line memory are to be input.
59	VI24	I	
60	VI25	I	
61	VI26	I	
62	VI27	I	(MSB)
63	Vss	—	GND
64	TST	I	Test pin to be set at L level

Pin No.	Symbol	I/O	Description
65	VO17	O	(MSB)
66	VO16	O	
67	VO15	O	
68	VO14	O	Built-in line memory output 1
69	VO13	O	
70	VO12	O	
71	VO11	O	
72	VO10	O	(LSB)
73	V_{DD}	—	+5V
74	VIN0	I	(LSB)
75	VIN1	I	
76	VIN2	I	
77	VIN3	I	Composite video signal input
78	VIN4	I	
79	VIN5	I	
80	VIN6	I	

Electrical Characteristics

1) DC Characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–20 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	Clock 14.3MHz *1	—	—	60	mA
H level output voltage	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5	—	V_{DD}	V
		I_{OH}=–4mA *2	V_{DD}–0.5	—	V_{DD}	V
L level output voltage	V_{OL}	I_{OL}=4mA	Vss	—	0.4	V
		I_{OL}=8mA *2	Vss	—	0.4	V
H level input voltage	V_{IH}	TTL level	2.5	—	V_{DD}	V
		CMOS level *3	V_{DD} × 0.7	—	V_{DD}	V
L level input voltage	V_{IL}	TTL level	Vss	—	0.5	V
		CMOS level *3	Vss	—	V_{DD} × 0.3	V

*1) V_{IH}=V_{DD}, V_{IL}=Vss
*2) Applicable to Pins 4 and 6
*3) Applicable to Pin 5

2) Input/Output Capacity

(V_{DD}=V_I=0V, f_M=1MHz)

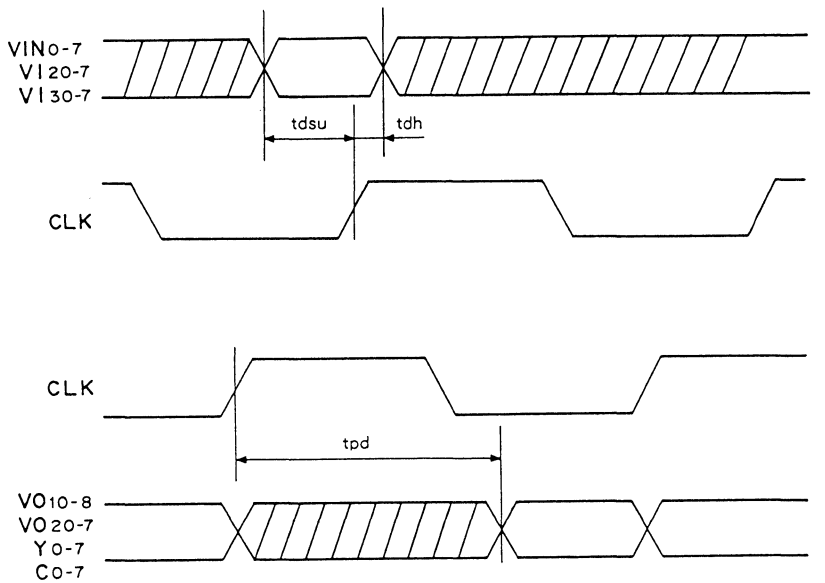
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input pin	C_{IN}	Ta=25°C	—	—	9	pF
Output pin	C_{OUT}	Ta=25°C	—	—	11	pF

3) AC Characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–20 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Setup time for VIN0 to 7 CLK	tdsu		15	—	—	ns
Hold time for VIN0 to 7 CLK	tdh		5	—	—	ns
Setup time for VI20 to 27 CLK	tdsu		20	—	—	ns
Hold time for VI20 to 27 CLK	tdh		5	—	—	ns
Setup time for VI30 to 37 CLK	tdsu		15	—	—	ns
Hold time for VI30 to 37 CLK	tdh		5	—	—	ns
Time from when CLK is input to when VO10 to 17 data is set	tpd	C_L=20pF	—	—	45	ns
Time from when CLK is input to when VO20 to 27 data is set	tpd	C_L=20pF	—	—	45	ns
Time from when CLK is input to when Y0 to 7 data is set	tpd	C_L=20pF	—	—	45	ns
Time from when CLK is input to when C0 to 7 data is set	tpd	C_L=20pF	—	—	45	ns
CLK frequency	f		14	—	18	MHz

AC Characteristics Timing Chart



Description of Functions

The CXD2011Q is an NTSC and PAL compatible digital Y/C separation IC which offers higher performance than the conventional line comb, thanks to adaptive (two-dimensional) processing. Two-dimensional processing, compared with three-dimensional processing, makes it possible to get a lower cost system.

In the case of NTSC, the conventional simple line comb always produces an error in the vertical non-correlated portion, because it calculates non-correlated signals together as shown in Fig. 1. In order to minimize the possibility of calculating non-correlated signals together, two line combs are provided for Y/C separation of signals of a line. One of the line combs (referred to as the upper line comb for the sake of convenience) is for calculation of signals of the line and the one above the line, whereas the other line comb (referred to as the lower line comb for the sake of convenience) is for calculation of signals of the line and the one below the line. These two line combs are separately used to ensure calculation of correlated signals together.

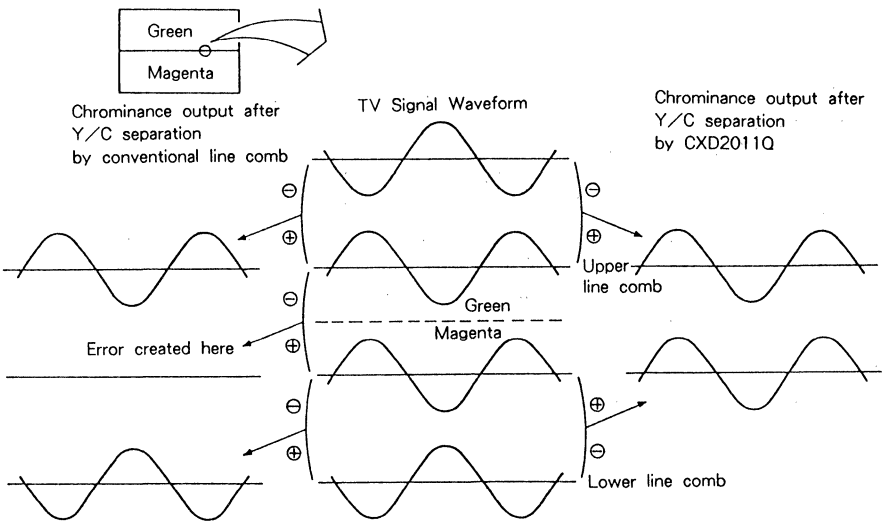


Fig. 1.

When only a line for example is colored as shown in Fig. 2, an error occurs in both the upper and lower line combs. In the case of signals like this where the vertical frequency is high but the horizontal frequency is low, the bandpass and trap are used for Y/C separation.

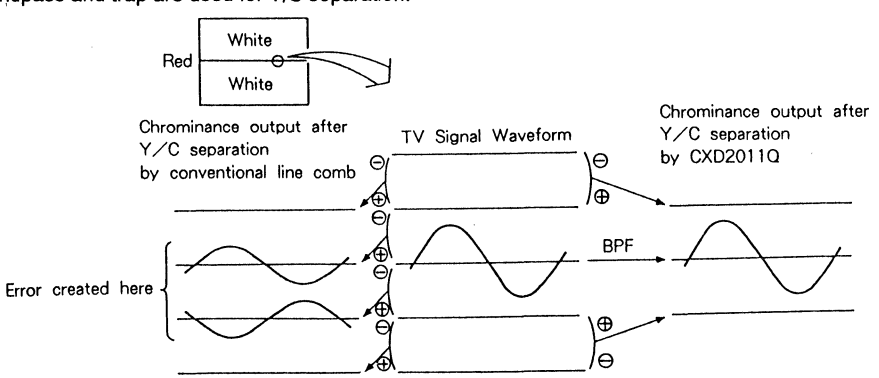


Fig. 2.

When both the vertical and horizontal frequencies are high and vertical correlation strong, the 2H comb output derived by averaging the upper and lower comb outputs is used.

In this manner the upper comb, lower comb, 2H comb or BPF output whichever is an optimum output is selected on the basis of signal correlation, thereby assuring much higher accuracy in Y/C separation than by the conventional line comb.

In addition, digital implementation eliminates ringing, etc. that used to occur in the conventional glass delay line.

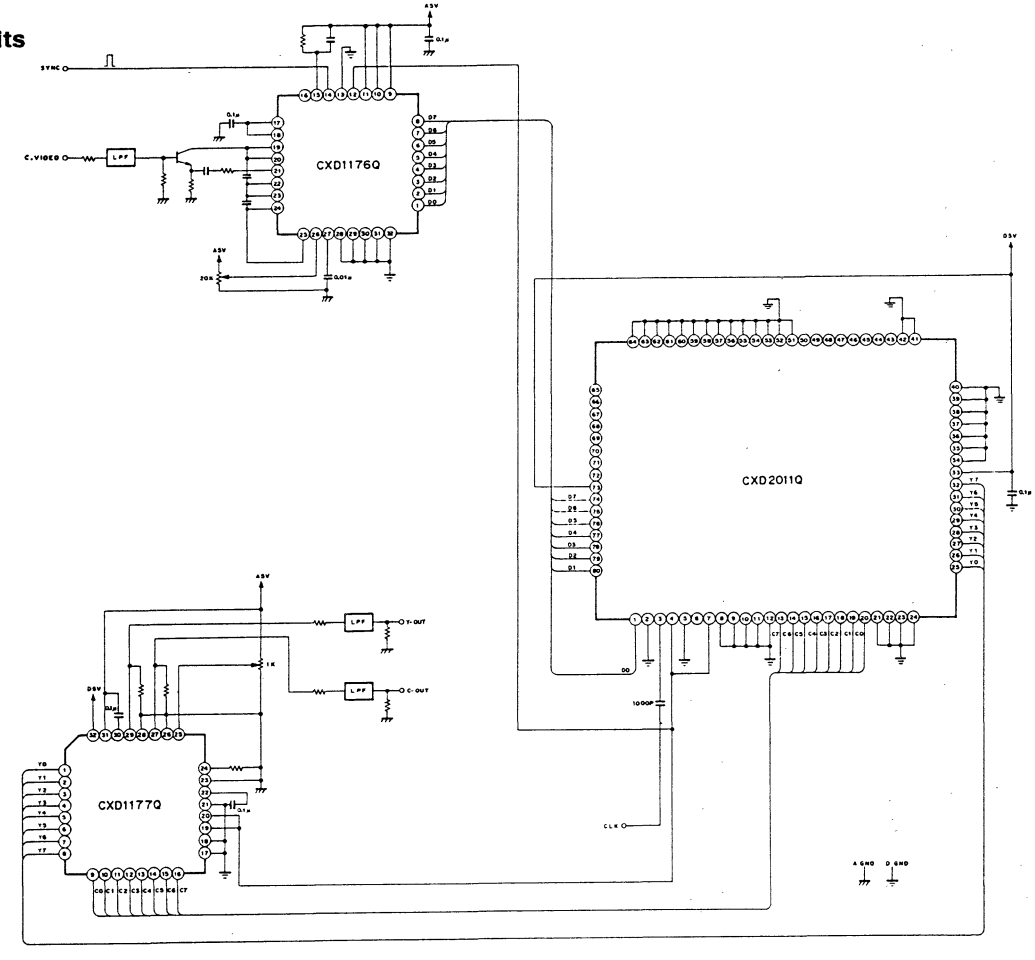
In the case of PAL, Y/C separation by use of the conventional BPF and trap presented problems such as considerable cross color and poor frequency response. These problems can be solved by use of the CXD2011Q without causing any side effects.

Summary of Advantages Offered by CXD2011Q

(1) Accomplishes Y/C separation with much higher accuracy than the conventional line comb.
(2) Helps reduce the number of parts in sets because of compatibility with both NTSC and PAL.
(3) Reduces cross colors and improves the frequency response in the PAL system.
(4) Digital implementation eliminates ringing, etc. encountered in the glass delay line.
(5) Reduces the load on the manufacturing line because there is no need for comb adjustments.

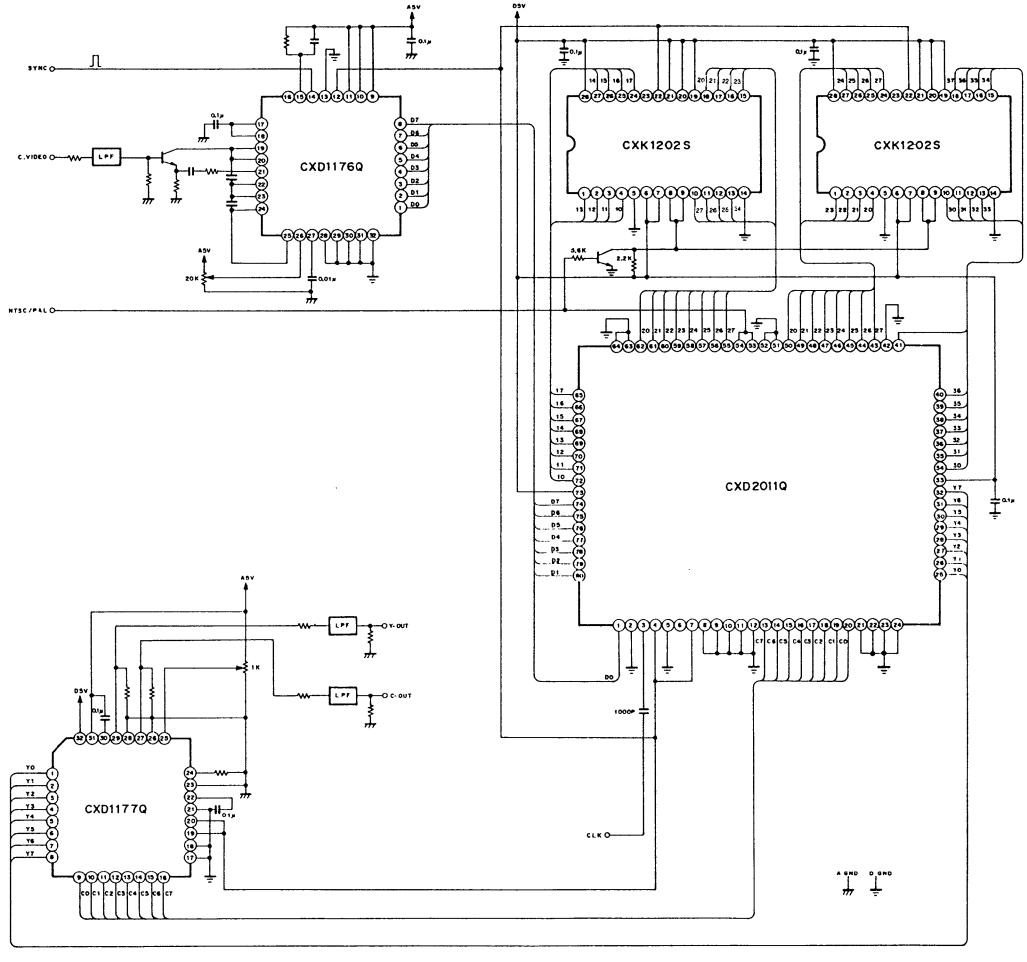
Application Circuits

For NTSC



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

For NTSC/PAL

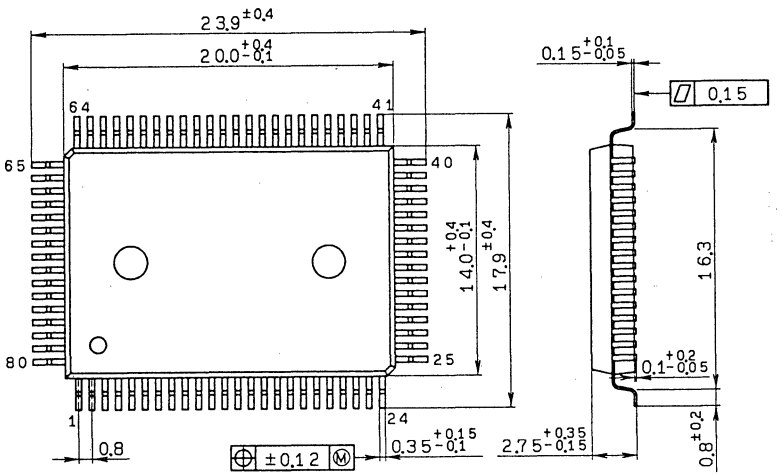


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit : mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

SONY®

CXK1202Q

Digital Delay Line

Description

CXK1202Q is a digital line memory pertaining to 8-bit structure which employs silicon gate CMOS process. It can easily be used to realize compensation for dropout of VTR and used as a digital filter, noise reduction, etc.

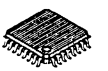
Features

- 1144 words×8 bit structure
- Number of delay steps is 17 to 1144 bits and variable.
- Possible to select the following 16 delay lines (Peripheral circuit is unnecessary) for NTSC, PAL and SECAM
  - 905 to 912 bits
  - 1129 to 1136 bits
- High speed cycle time
  - Minimum write cycle time 25ns
  - Minimum read cycle time 25ns
- I/O level Compatible with TTL level
- Data output three-states
- 5V single power supply operation
- Low power dissipation (200mW typ.)

Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_{IN}	−0.3 to +7.0	V
• Operating temperature	Topr	−10 to +85	°C
• Storage temperature	Tstg	−55 to 150	°C
• Power consumption	P_D	500	mW

32 pin QFP (Plastic)



Recommended Operating Conditions

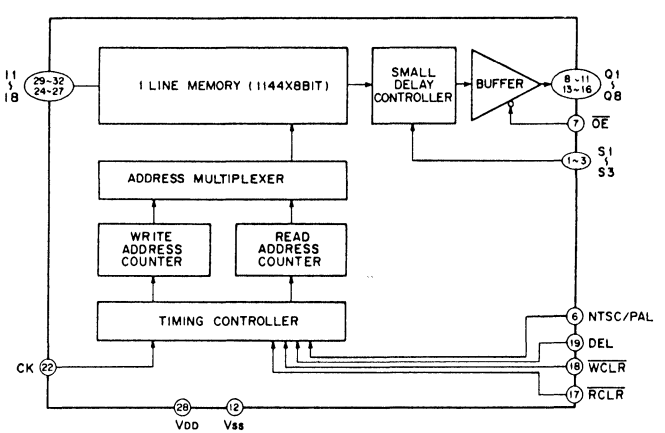
(Ta=0 to 70°C)

• Supply voltage	V_{DD}	4.5 to 5.5 (5.0V typ.)	V
• Supply voltage	Vss	0	V
• Input voltage "H" level	V_{IH}	2.4 to V_{DD}+0.3	V
• Input voltage "L" level	V_{IL}	−0.3 to +0.8	V

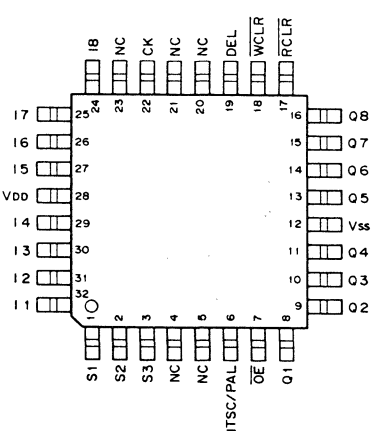
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Pin symbol	Pin description
1 to 3	S_1 to S_3	These are small delay steps setting input pins. The setting number of the delay steps is determined by the cycle of the clear signal and the level of S_1 to S_3. At this point, the clear signal sets rough number of delay steps of every multiple of 8 bits. However, pins S_1 to S_3 set delay step of 1 bit-unit with 8-bit width.
6	NTSC/PAL	An input pin which selects the number of delay steps either 905 to 912 bits or 1129 to 1136 bits when the DEL pin is set at "H" level. The 905 to 912 bits of delay steps are selected when it is at "H" level and 1129 to 1136 bits of delay steps are selected when it is at "L" level.
7	$\overline{OE}$	An output enable input pin. The data output pins (Q_1 to Q_8) become into output mode when they are at "L" level. They become into high impedance state when they are at "H" level.
8 to 11	Q_1 to Q_4	These are data output pins. The outputs against the respective inputs of I_1 to I_4 correspond to Q_1 to Q_4. The access time is determined from the rising edge of the clock.
13 to 16	Q_5 to Q_8	Data output pins. The outputs against the respective inputs of I_5 to I_8 correspond to Q_5 to Q_8. The access time is determined from the rising edge of the clock.
17	$\overline{RCLR}$	A clear signal input pin of the read address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{RCLR}$ pin is ignored when the DEL pin is at "H".
18	$\overline{WCLR}$	A clear signal input pin of the write address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{WCLR}$ pin is ignored when the DEL pin is at "H".
19	DEL	An input pin which selects the external and internal clear signals. When at "L", it becomes into external clear signal input mode and the number of delay steps can be set at any bit from 17 to 1144 bits. When at "H", it becomes into internal clear signal using mode and the number of delay steps can be set at any bit from 905 to 912 bits and from 1129 to 1136 bits.
22	CK	A clock input pin. The I/O timing of the respective signals and the delay step, etc. can be defined against the clock input from this pin.
24 to 27	I_8 to I_5	Data input pins. The data set up time and hold time are determined from the rising edge of the clock.
29 to 32	I_4 to I_1	Data input pins. Data set up time and hold time are determined from the rising edge of the clock.
28	V_{DD}	The power supply pin (+5V).
12	Vss	A grounding pin.
4, 5, 20, 21, 23	NC	Non-connection

Electrical Characteristics

(1) DC characteristics

(V_{DD}=5.0V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply current (Active)	I_{DD}	—	—	70	mA	
Input leakage current	I_{IL}	−2	—	2	μA	V_{IN}=0V to V_{DD}
Output leakage current	I_{OL}	−2	—	2	μA	V_{OUT}=0V to V_{DD}
Output voltage "H" level	V_{OH}	2.7	—		V	I_{OH}=−400μA
Output voltage "L" level	V_{OL}	—	—	0.4	V	I_{OL}=4.0mA

(2) AC characteristics

(V_{DD}=4.5 to 5.5V, Ta=0 to 70°C)
(Regarding the timing chart, see next page.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Data set up time	tdsu	5	—	—	ns	
Data hold up time	tdh	5	—	—	ns	
$\overline{WCLR}$, $\overline{RCLR}$ set up time	tcsu	15	—	—	ns	
$\overline{WCLR}$, $\overline{RCLR}$ hold time	tch	5	—	—	ns	
Clock pulse width	tckw	10	—	—	ns	Low or High
Clock frequency	f	1	—	40	MHz	C_L=30pF
From clock input to output data determination	tpda	—	—	25	ns	
From $\overline{OE}$ input to output data determination	tpdb	—	—	25	ns	
Output disable time (from $\overline{OE}$)	tpdh	—	—	25	ns	
Output enable time (from $\overline{OE}$)	tpdi	—	—	25	ns	

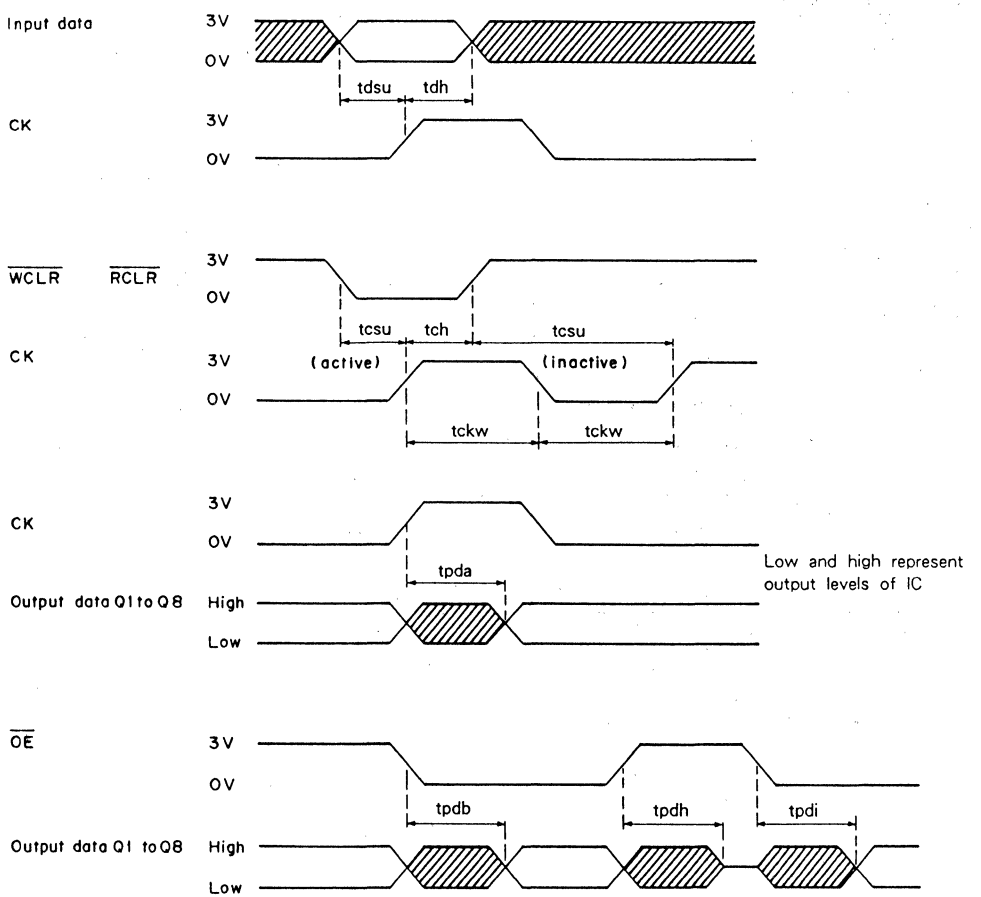
(3) Pin capacity

(Ta=25°C, fM=1 MHz, V_{IN}=V_{OUT}=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacity	C_{IN}	—	—	7	pF
Output pin capacity	C_{OUT}	—	—	10	pF

Timing Chart

(1) The input signal levels are at the low level=0V and at the high level=3V, and 5ns for both rising and falling edges.
(2) The voltage judging level of the low and high levels is 1.5V.



Application

1. 1H delay line (Delay steps 905 to 912 bits, 1129 to 1136 bits)
   Since a clear signal generation circuit is incorporated in the CXK1202Q, an external clear signal is unnecessary when it is used as an 1H delay line. By selecting the DEL pin (pin 19) to "H" level and the $\overline{OE}$ pin (pin 7) to "L" level, they can be used as the delay lines of the delay steps as shown in Tables 1 and 2.
   A circuit and timing chart when they are used as the delay line of the delay step 908 bits are as shown in Figs. 1 and 2.

NTSC/PAL (pin 6) pin is at "H"			
S_1	S_2	S_3	Delay step
L	L	L	905
H	L	L	906
L	H	L	907
H	H	L	908
L	L	H	909
H	L	H	910
L	H	H	911
H	H	H	912

Table 1. Delay steps when NTSC mode

NTSC/PAL (pin 6) pin is at "L"			
S_1	S_2	S_3	Delay step
L	L	L	1129
H	L	L	1130
L	H	L	1131
H	H	L	1132
L	L	H	1133
H	L	H	1134
L	H	H	1135
H	H	H	1136

Table 2. Delay steps when PAL mode

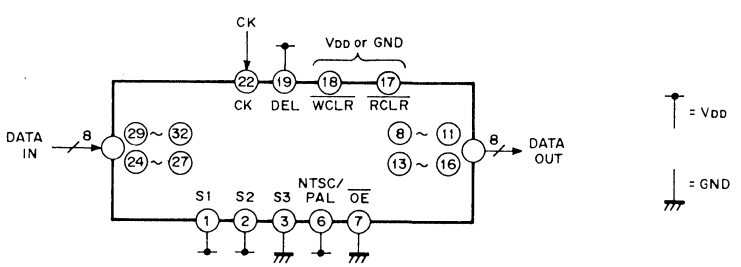


Fig. 1. Circuit of 908 bits delay

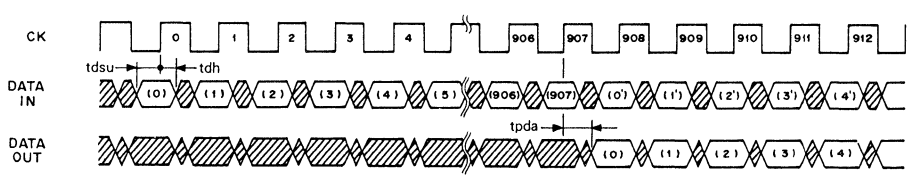


Fig. 2. Timing chart of 908 bits delay

2. Delay line (Delay step 17 to 1144 bits)

By setting the DEL pin (pin 19), NTSC/PAL pin (pin 6), and $\overline{OE}$ pin (pin 7) to "L" level, they can be used as a delay line of delay steps 17 to 1144 bits.

The delay steps can be determined by the clear signal and the input level of S_1 to S_3. The clear signal is input always every 8n (n is an integer. n=1, 2, ... 141) clocks. At that time, the obtained delay step is either one from 8 steps of 8 (n+1) +1 to 8 (n+2) bits. The selection is performed by S_1 to S_3 pins. The number of delay steps to be obtained by the input levels of S_1 to S_3 are tabulated in Table 3.

For example, when used as a delay line of delay step of 123, it is written as 123=8 (14+1) +3 and it becomes n=14. Accordingly, input the clear signal every 8×14=112 clocks and set the S_1, S_2 and S_3 pins respectively to "L", "H" and "L" levels and it can be used as a delay line of delay step of 123 bits. The circuit and timing chart at that time are respectively as shown in Figs. 3 and 4.

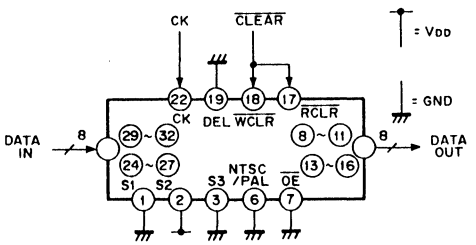


Fig. 3. Circuit of 123 bits delay

n=1, 2, ...141

S_1	S_2	S_3	Delay step
L	L	L	8 (n+1) +1
H	L	L	8 (n+1) +2
L	H	L	8 (n+1) +3
H	H	L	8(n+1) +4
L	L	H	8 (n+1) +5
H	L	H	8 (n+1) +6
L	H	H	8 (n+1) +7
H	H	H	8 (n+2)

Table 3. Delay steps when clear signal is input every 8n clocks

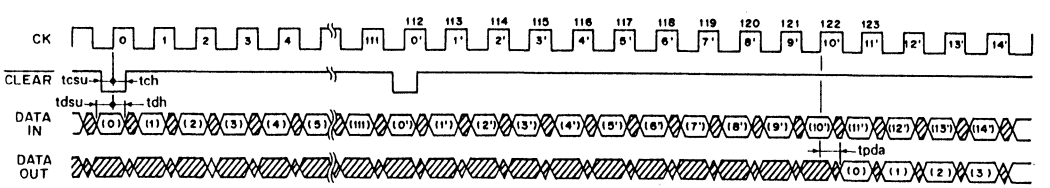


Fig. 4. Timing chart of 123 bits delay

Special Application Example — Data Holding

Since SRAM is incorporated in the CXK1202Q, data holding can be carried out. However, it is unable to perform random access of the held data. The maximum data holding amount is 1120 words×8 bit.

The data holding can be carried out by controlling the input timing and clock of the $\overline{WCLR}$ and $\overline{RCLR}$ signals. Set to $\overline{WCLR}$ and $\overline{RCLR}$ signals input modes by selecting the DEL pin (pin 19) to "L" level. By selecting the NTSC/PAL pin (pin 6) to "L" level, the maximum data holding amount of it becomes 1120 words×8 bit.

- Data writing in

  When the $\overline{WCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the write address counter is cleared and the data input at that moment is written into the top address. After the $\overline{WCLR}$ signal has been transferred to "H" level from "L" level, the write address counter is incremented and the data are recorded in the order they have been input. If there are data, which are desired to be written in, up to i-th (i is an integer. i=0, 1, 2, ... 1119) and when the condition is $8m \leqq i \leqq 8m+7$ (m is an integer. m=0, 1, 2, ... 139), input the clock signals up to 8 (m+1) 2 to 8 (m+1) +7 counted from the $\overline{WCLR}$ signal input and it becomes necessary to stop the input of the clock signal there-after. (Fig. 6)

  Note) • Be sure that if the clock signal after 8 (m+1) +7th clock signal is not stopped, it keeps counting on as if there are input data.
  • When the clock is stopped at other than 8 (m+1) +2 to 8 (m+1) +7, the power supply current is somewhat increased so it is desired not to stop it.

- Data read out

  When the $\overline{RCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the data having been held commence to output data after 8 to 15 clocks from that clock. The data are output in the same order as they have been written in. The data output commencing period is dependent on the levels of S_1 to S_3 as shown in Table 4.

  A circuit example when data is output from after 11 clocks is as shown in Fig. 5 and its timing chart is as shown in Fig. 7.

  Moreover, the data read out once is held unless it is rewritten.

  Note) • If the $\overline{RCLR}$ signal is input during data writing, reading out from after 8 to 15 clocks is possible. At that time, input the $\overline{RCLR}$ signal after 8k clocks (k is an integer. k=1, 2, 3, ... 141) from the $\overline{WCLR}$ signal input. (Fig. 8)
  • Do not stop the clock while reading the data is being performed.

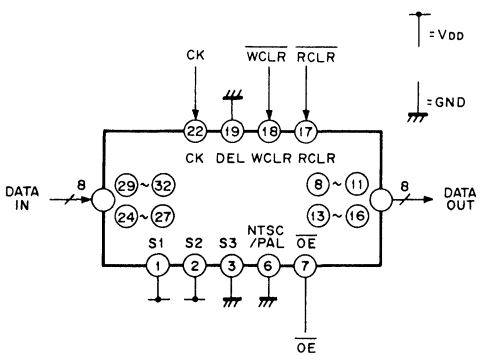


Fig. 5. A circuit from the $\overline{RCLR}$ signal is input to the data output commencement

S_1	S_2	S_3	Output commencing period
L	L	L	After 8 clocks
H	L	L	After 9 clocks
L	H	L	After 10 clocks
H	H	L	After 11 clocks
L	L	H	After 12 clocks
H	L	H	After 13 clocks
L	H	H	After 14 clocks
H	H	H	After 15 clocks

Table 4. Number of clocks when the $\overline{RCLR}$ signal is input to the data output commencement (Make clock in which $\overline{RCLR}$ signal has been input to 0)

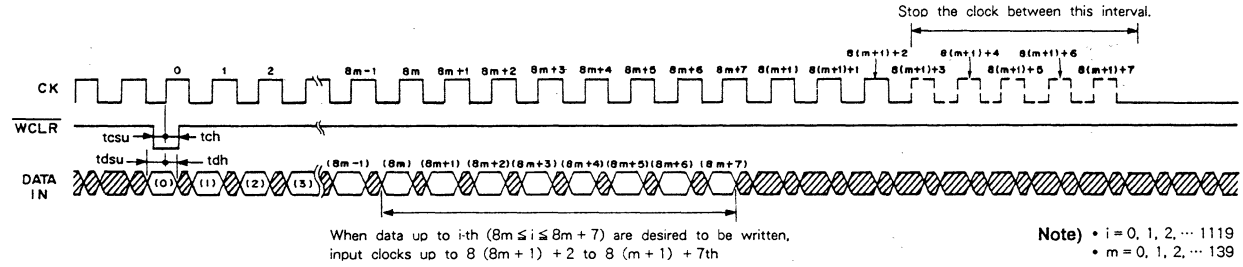


Fig. 6 The data write in timing when they are being held

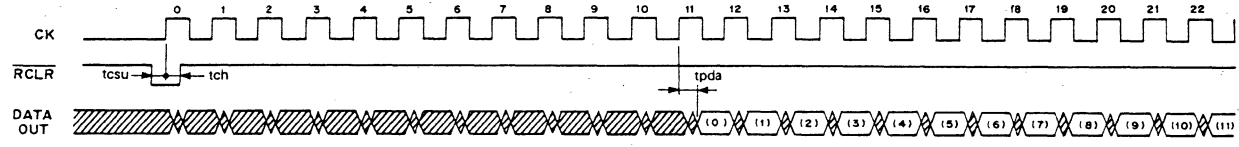


Fig. 7 The data read OUT timing
(When S1="H", S2="H" and S3="L"
After 11 clocks outputs commencing period in Table 4.)

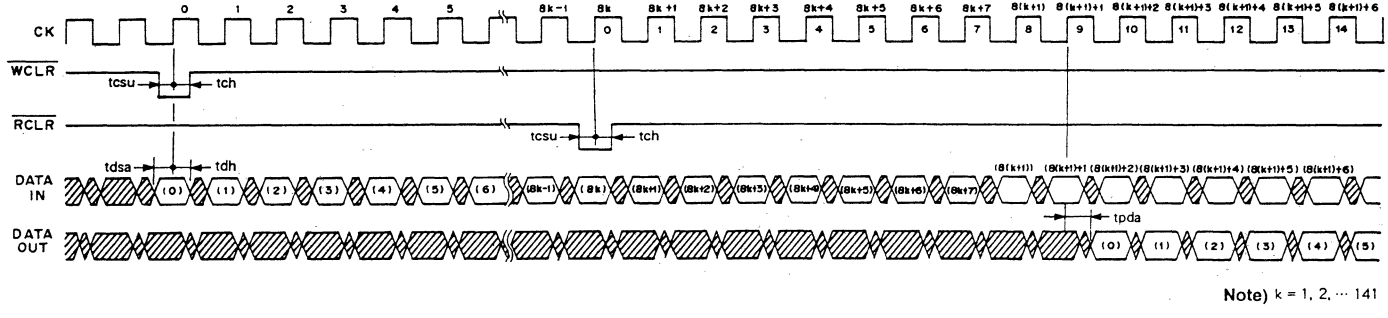
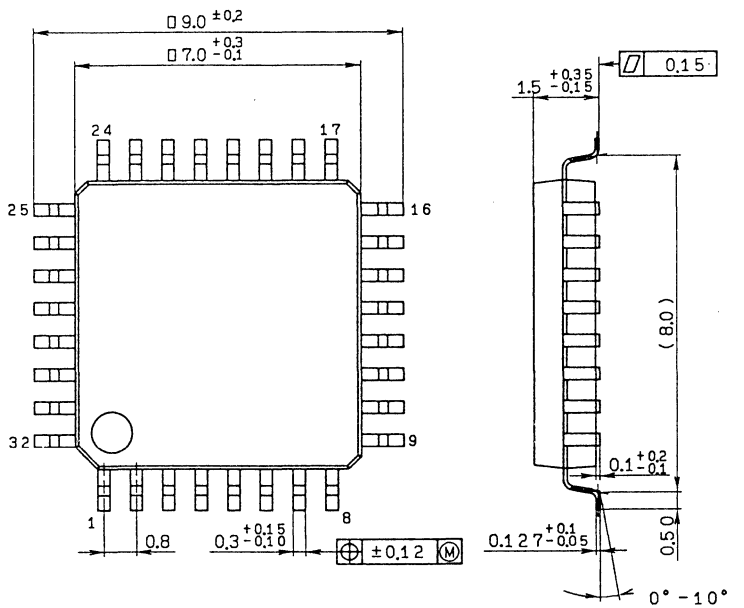


Fig. 8 The timing of data read out while writing in data (When S1="H", S2="L" and S3="L")

Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

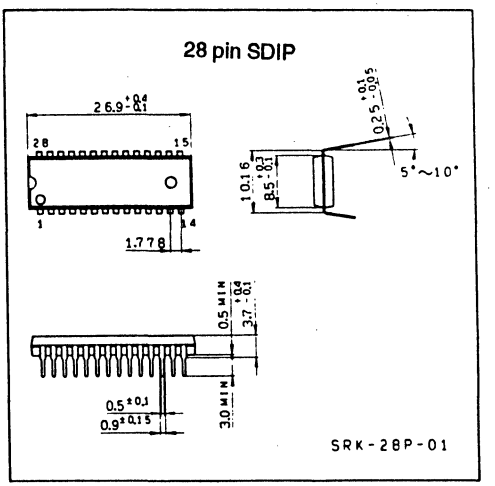
SONY® **CXK1202S**

Digital Delay Line

Description

The CXK1202S is a digital line memory pertaining to 8-bit structure which employs silicon gate CMOS process. It can easily be used to realize compensation for dropout of VTR and used as a digital filter, noise reduction, etc.

Package Outline Unit: mm



Features

- 1144 words × 8 bit structure
- Number of delay steps is 17 to 1144 bits and variable.
- Possible to select the following 16 delay lines (Peripheral circuit is unnecessary) for NTSC, PAL and SECAM
  - 905 to 912 bits
  - 1129 to 1136 bits
- High speed cycle time
  - Minimum write cycle time 25ns
  - Minimum read cycle time 25ns
- I/O level Compatible with TTL level
- Data output three-states
- 5V single power supply operation
- Low power dissipation (200 mW typ.)

Structure

Silicon gate CMOS

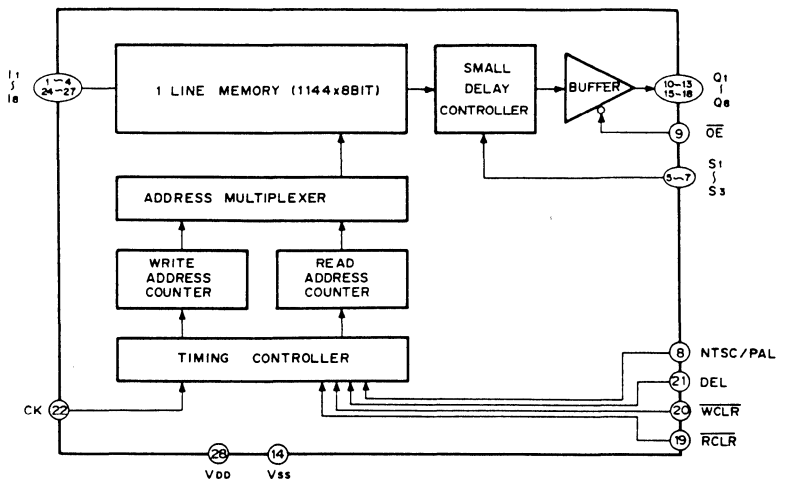
Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_{IN}	−0.3 to +7.0	V
• Operating temperature	Topr	−10 to +85	°C
• Storage temperature	Tstg	−55 to 150	°C
• Power consumption	P_D	500	mW

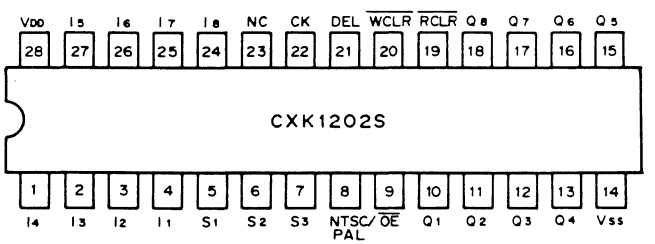
Recommended Operating Conditions (Ta=0°C to 70°C)

• Supply voltage	V_{DD}	4.5 to 5.5	V (5.0V typ.)
• Supply voltage	V_{SS}	0	V
• Input voltage "H" level	V_{IH}	2.4 to V_{DD}+0.3	V
• Input voltage "L" level	V_{IL}	−0.3 to +0.8	V

Block Diagram



Pin Configuration (Top view)



Pin Description

Pin No.	Pin symbol	Pin description
1~4	I_4~I_1	Data input pins. Data set up time and hold time are determined from the rising edge of the clock.
5~7	S1~S3	These are small delay steps setting input pins. The setting number of the delay steps is determined by the cycle of the clear signal and the level of S_1 to S_3. At this point, the clear signal sets rough number of delay steps of every multiple of 8 bits. However, pins S_1 to S_3 set delay step of 1 bit-unit with 8-bit width.
8	NTSC/PAL	An input pin which selects the number of delay steps either 905 to 912 bits or 1129 to 1136 bits when the DEL pin is set at "H" level. The 905 to 912 bits of delay steps are selected when it is at "H" level and 1129 to 1136 bits of delay steps are selected when it is at "L" level.
9	$\overline{OE}$	An output enable input pin. The data output pins (Q_1 to Q_8) become into output mode when they are at "L" level. They become into high impedance state when they are at "H" level.
10~13	Q_1~Q_4	These are data output pins. The outputs against the respective inputs of I_1 to I_4 correspond to Q_1 to Q_4. The access time is determined from the rising edge of the clock.
14	Vss	A grounding pin.
15~18	Q_5~Q_8	Data output pins. The outputs against the respective inputs of I_5 to I_8 correspond to Q_5 to Q_8. The access time is determined from the rising edge of the clock.
19	$\overline{RCLR}$	A clear signal input pin of the read address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{RCLR}$ pin is ignored when the DEL pin is at "H".
20	$\overline{WCLR}$	A clear signal input pin of the write address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{WCLR}$ pin is ignored when the DEL pin is at "H".
21	DEL	An input pin which selects the external and internal clear signals. When at "L", it becomes into external clear signal input mode and the number of delay steps can be set at any bit from 17 to 1144 bits. When at "H", it becomes into internal clear signal using mode and the number of delay steps can be set at any bit from 905 to 912 bits and from 1129 to 1136 bits.
22	CK	A clock input pin. The I/O timing of the respective signals and the delay step, etc. can be defined against the clock input from this pin.
23	NC	Non-connection
24~27	I_8~I_5	Data input pins. The data set up time and hold time are determined from the rising edge of the clock.
28	V_{DD}	The power supply pin (+5V).

Electrical Characteristics

(1) DC characteristics

V_{DD}=5.0V, Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply current (Active)	I_{DD}	—	—	70	mA	
Input leakage current	I_{IL}	−2	—	2	μA	V_{IN}=0V~V_{DD}
Output leakage current	I_{OL}	−2	—	2	μA	V_{OUT}=0V~V_{DD}
Output voltage "H" level	V_{OH}	2.7	—		V	I_{OH}=−400μA
Output voltage "L" level	V_{OL}	—	—	0.4	V	I_{OL}=4.0mA

(2) AC characteristics

V_{DD}=4.5V to 5.5V, Ta=0°C to 70°C
(Regarding the timing chart, see next page.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Data set up time	t_{dsu}	5	—	—	nS	
Data hold up time	t_{dh}	5	—	—	nS	
$\overline{WCLR}$, $\overline{RCLR}$ set up time	t_{csu}	15	—	—	nS	
$\overline{WCLR}$, $\overline{RCLR}$ hold time	t_{ch}	5	—	—	nS	
Clock pulse width	t_{ckw}	10	—	—	nS	Low or high

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	f	—	—	40	MHz	CL=30pF
From clock input to output data determination	t_{pda}	—	—	25	nS	
From $\overline{OE}$ input to output data determination	t_{pdb}	—	—	25	nS	
Output disable time (from $\overline{OE}$)	t_{pdh}	—	—	25	nS	
Output enable time (from $\overline{OE}$)	t_{pdl}	—	—	25	nS	

(3) Pin capacity

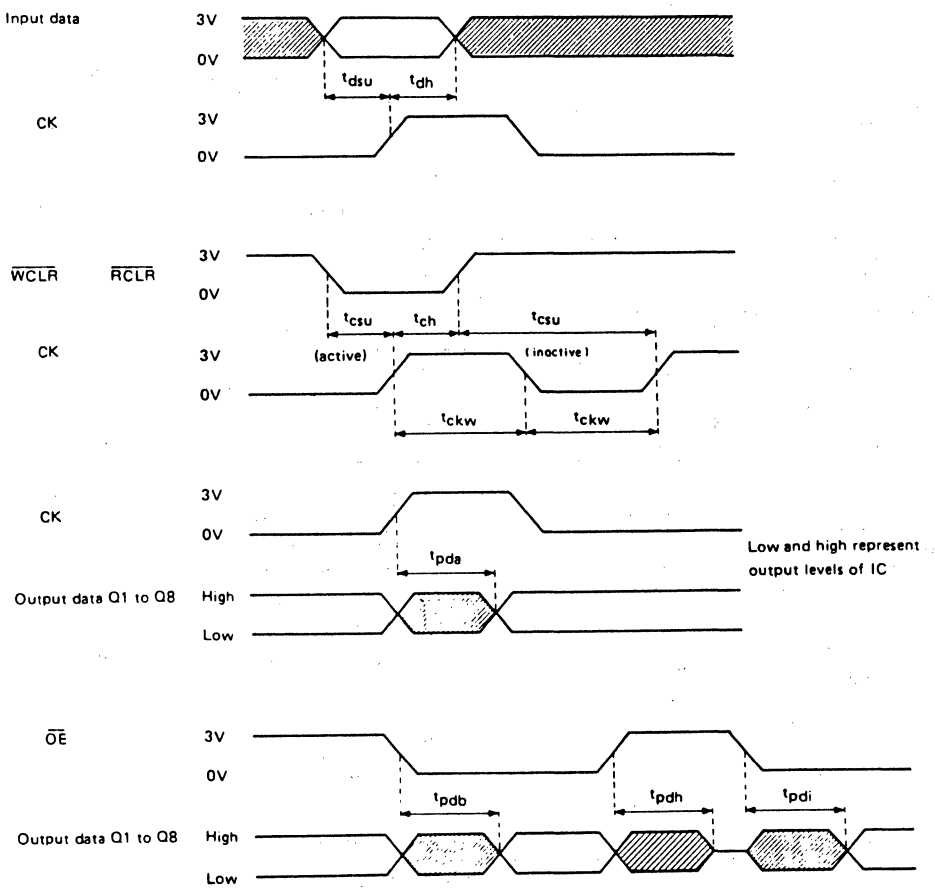
Ta=25°C, fM=1MHz, V_{IN}=V_{OUT}=0V

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacity	C_{IN}	—	—	7	pF
Output pin capacity	C_{OUT}	—	—	10	pF

Timing Chart

(1) The input signal levels are at the low level = 0V and at the high level = 3V, and 5nS for both rising and falling edges.

(2) The voltage judging level of the low and high levels is 1.5V



Application

1. 1H delay line (Delay steps 905 to 912 bits, 1129 to 1136 bits)

Since a clear signal generation circuit is incorporated in the CXK1202S, an external clear signal is unnecessary when it is used as an 1H delay line. By selecting the DEL pin (pin 21) to "H" level and the $\overline{OE}$ pin (pin 9) to "L" level, they can be used as the delay lines of the delay steps as shown in Tables 1 and 2.

A circuit and timing chart when they are used as the delay line of the delay step 908 bits are as shown in Figs. 1 and 2.

NTSC/PAL (pin 8) pin is at "H"			
S_1	S_2	S_3	Delay step
L	L	L	905
H	L	L	906
L	H	L	907
H	H	L	908
L	L	H	909
H	L	H	910
L	H	H	911
H	H	H	912

Table 1. Delay steps when NTSC mode

NTSC/PAL (pin 8) pin is at "L"			
S_1	S_2	S_3	Delay step
L	L	L	1129
H	L	L	1130
L	H	L	1131
H	H	L	1132
L	L	H	1133
H	L	H	1134
L	H	H	1135
H	H	H	1136

Table 2. Delay steps when PAL mode

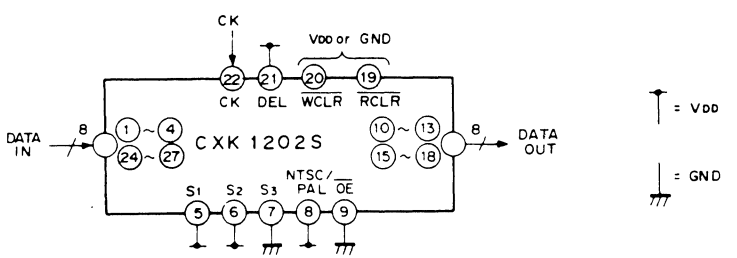


Fig. 1 Circuit of 908 bits delay

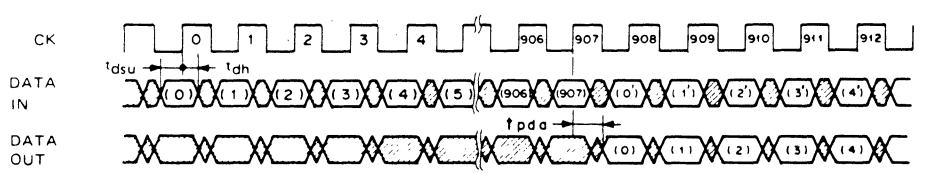


Fig. 2 Timing chart of 908 bits delay

2. Delay line (Delay step 17 to 1144 bits)

By setting the DEL pin (pin 2), NTSC/PAL pin (pin 8), and $\overline{OE}$ pin (pin 9) to "L" level, they can be used as a delay line of delay steps 17 to 1144 bits.

The delay steps can be determined by the clear signal and the input level of S_1 to S_3. The clear signal is input always every 8n (n is an integer: n=1, 2, ... 141) clocks. At that time, the obtained delay step is either one from 8 steps of 8(n+1)+1 to 8(n+2) bits. The selection is performed by S_1 to S_3 pins. The number of delay steps to be obtained by the input levels of S_1 to S_3 are tabulated in Table 3.

For example, when used as a delay line of delay step of 123, it is written as 123=8(14+1)+3 and it becomes n=14. Accordingly, input the clear signal every 8×14=112 clocks and set the S_1, S_2 and S_3 pins respectively to "L", "H" and "L" levels and it can be used as a delay line of delay step of 123 bits. The circuit and timing chart at that time are respectively as shown in Figs. 3 and 4.

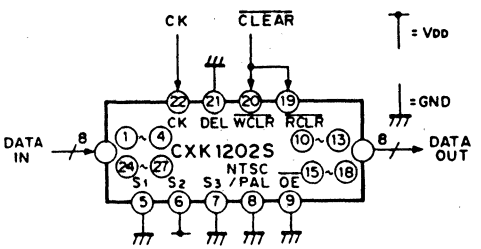


Fig. 3 Circuit of 123 bits delay

n=1, 2, . . . 141

S_1	S_2	S_3	Delay step
L	L	L	8(n+1)+1
H	L	L	8(n+1)+2
L	H	L	8(n+1)+3
H	H	L	8(n+1)+4
L	L	H	8(n+1)+5
H	L	H	8(n+1)+6
L	H	H	8(n+1)+7
H	H	H	8(n+2)

Table 3. Delay steps when clear signal is input every 8n clocks

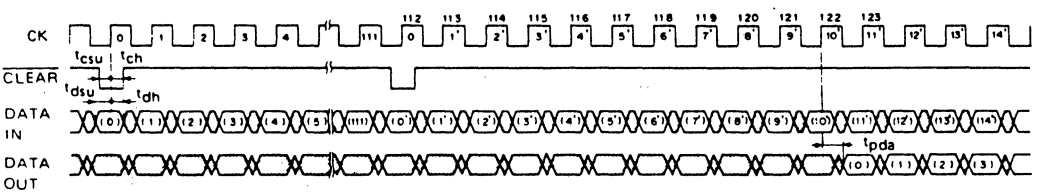


Fig. 4 Timing chart of 123 bits delay

3. Special Application Example — Data Holding

Since SRAM is incorporated in the CXK1202S, data holding can be carried out. However, it is unable to perform random access of the held data. The maximum data holding amount is 1120 words × 8 bit.

The data holding can be carried out by controlling the input timing and clock of the $\overline{WCLR}$ and $\overline{RCLR}$ signals. Set to $\overline{WCLR}$ and $\overline{RCLR}$ signals input modes by selecting the DEL pin (pin 21) to "L" level. By selecting the NTSC/PAL pin (pin 8) to "L" level, the maximum data holding amount of it becomes 1120 words × 8 bit.

- Data writing in

When the $\overline{WCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the write address counter is cleared and the data input at that moment is written into the top address. After the $\overline{WCLR}$ signal has been transferred to "H" level from "L" level, the write address counter is incremented and the data are recorded in the order they have been input. If there are data, which are desired to be written in, up to i-th (i is an integer: i=0, 1, 2 . . . 1119) and when the condition is $8m \leqq i \leqq 8m+7$ (m is an integer: m=0, 1, 2, . . . 139), input the clock signals up to 8(m+1)2 to 8(m+1)+7 counted from the $\overline{WCLR}$ signal input and it becomes necessary to stop the input of the clock signal there-after. (Fig. 6)

Note) • Be sure that if the clock signal after 8(m+1)+7th clock signal is not stopped, it keeps counting on as if there are input data.
• When the clock is stopped at other than 8(m+1)+2 to 8(m+1)+7, the power supply current is somewhat increased so it is desired not to stop it.

- Data read out

When the $\overline{RCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the data having been held commence to output data after 8 to 15 clocks from that clock. The data are output in the same order as they have been written in. The data output commencing period is dependent on the levels of S_1 to S_3 as shown in Table 4.

A circuit example when data is output from after 11 clocks is as shown in Fig. 5 and its timing chart is as shown in Fig. 7.

Moreover, the data read out once is held unless it is rewritten.

Note) • If the $\overline{RCLR}$ signal is input during data writing, reading out from after 8 to 15 clocks is possible. At that time, input the $\overline{RCLR}$ signal after 8k clocks (k is an integer: k=1, 2, 3, . . . 141) from the $\overline{WCLR}$ signal input. (Fig. 8)
• Do not stop the clock while reading the data is being performed.

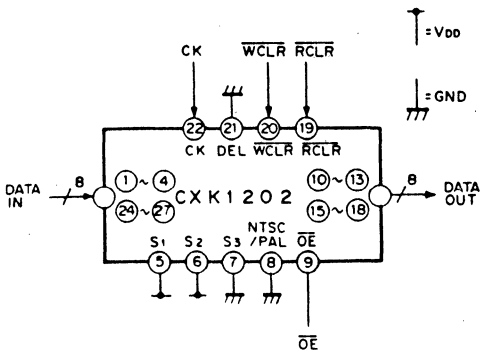
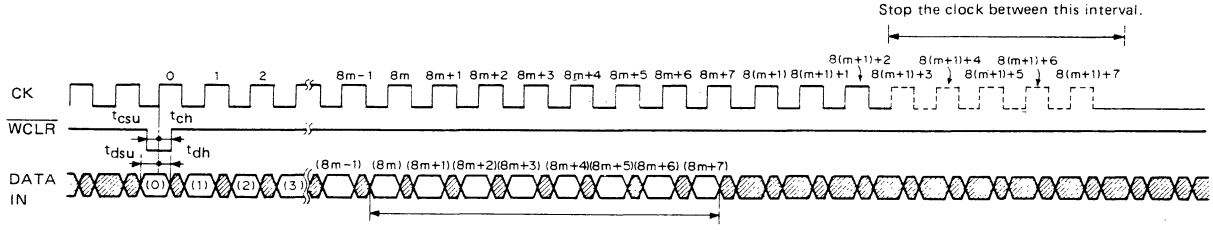


Fig. 5 A circuit from the $\overline{\text{RCLR}}$ signal is input to the data output commencement

S_1	S_2	S_3	Output commencing period
L	L	L	After 8 clocks
H	L	L	After 9 clocks
L	H	L	After 10 clocks
H	H	L	After 11 clocks
L	L	H	After 12 clocks
H	L	H	After 13 clocks
L	H	H	After 14 clocks
H	H	H	After 15 clocks

Table 4. Number of clocks when the $\overline{\text{RCLR}}$ signal is input to the data output commencement (Make clock in which $\overline{\text{RCLR}}$ signal has been input to 0)



Note) • i = 0, 1, 2, . . . 1119
• m = 0, 1, 2, . . . 139

Fig. 6 The data write in timing when they are being held

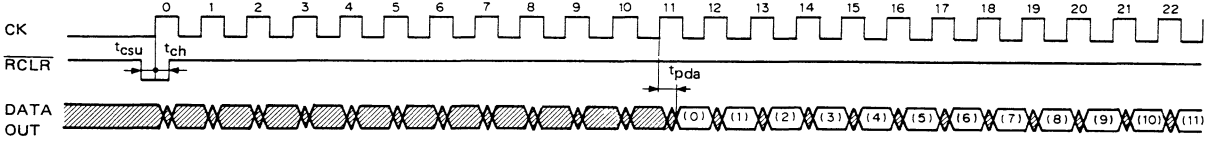


Fig. 7 The data read OUT timing
(When S_1="H", S_2="H" and S_3="L"
After 11 clocks outputs commencing period in Table 4.)

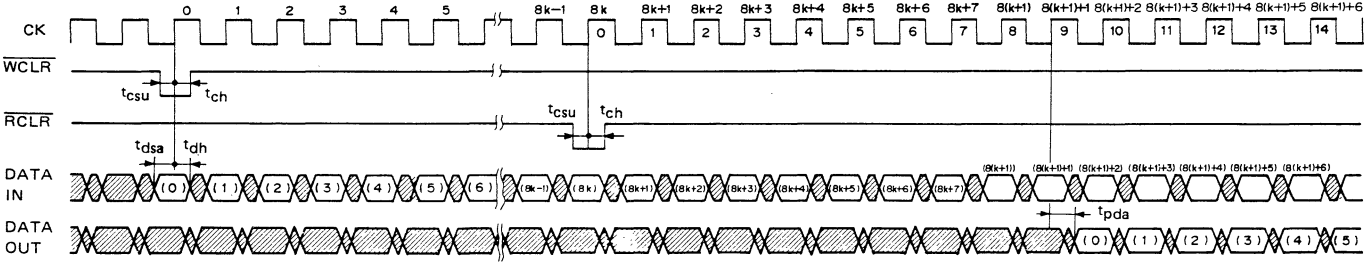


Fig. 8 The timing of data read out while writing in data
(When S_1="H", S_2="L" and S_3="L")

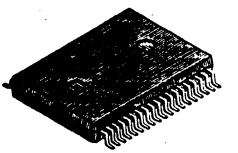
Note) k = 1, 2, . . . 141

SONY

CXK1206M

Video Signal Field Memory

38 pin SOP (Plastic)



Description

The CXK1206M is a 3-port VRAM capable of coping with both NTSC and PAL and of storing pictures for one 8-bit field with two chips, and is suitable as a memory for improving the picture quality including NR + TBC, and NR + double speed.

Features

- Asynchronous 3-ports, one for Write and two for Read.
- 960 column x 306 row x 4 bit structure (suitable for video signal processing).
- NTSC and PAL are respectively compatible with 4 fsc.
- Applicable to various uses in recursive mode/non-recursive mode.
- Random access : column → by block (Write only)
  row → by line.
- Transmission between I/O ports and the internal memory can be automatically controlled from the inside.
- Transfer synchronizing function.
- Power consumption: 100 mW (Typ.)
- Power supply: +5V ±10%.
- I/O level: TTL Low input capacitance.
- Substrate bias generator built in.

Structure

Silicon gate three-layered polysilicon, CMOS

Applications

Video signal processing field memory

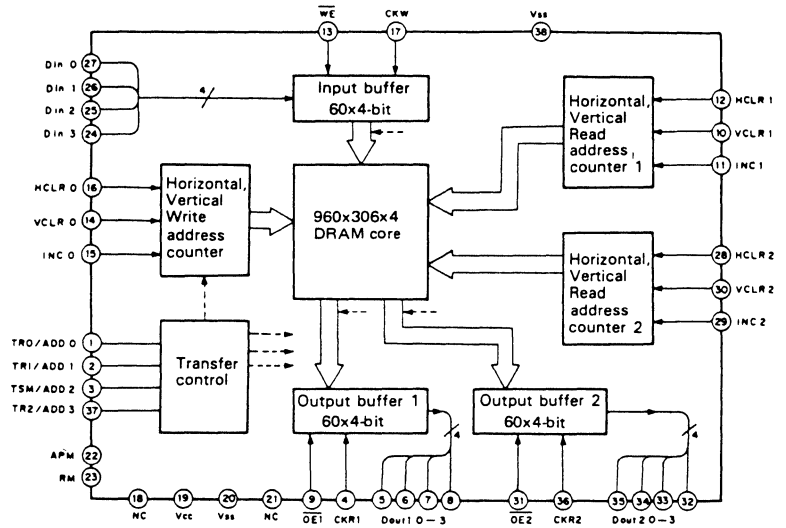
Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

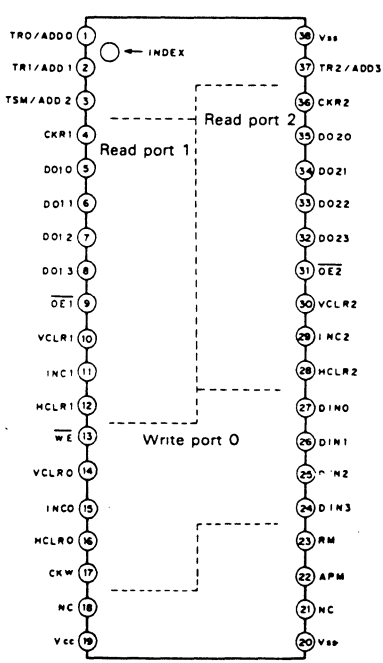
• Supply voltage	V_{CC}	−1.0 to +7.0	V
• Operating temperature	T_{opr}	0 to +70	°C
• Storage temperature	T_{stg}	−55 to +125	°C
• Allowable power dissipation	P_D	1.0	W

Recommended Operating Conditions (Ta = 0 to 70°C, Vss = 0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Supply voltage	V_{SS}	0	V
• Input voltage "H level"	V_{IH}	2.4 to 6.5	V
• Input voltage "L level"	V_{IL}	−2.0 to +0.8	V

Block Diagram





Pin Description

No.	Symbol	I/O	Description
1	TR0/ADD0	I/O	Write port 0 transfer synchronous Signal/Address 0 input
2	TR1/ADD1	I/O	Read port 1 transfer synchronous Signal/Address 1 input
3	TSM/ADD2	I	Transfer synchronous Mode/Address 2 input
4	CKR1	I	Port 1 shift signal
5	DO10	O	Port 1 data output
6	DO11	O	Port 1 data output
7	DO12	O	Port 1 data output
8	DO13	O	Port 1 data output
9	$\overline{OE1}$	I	Port 1 output enable
10	VCLR1	I	Port 1 vertical clear
11	INC1	I	Port 1 line increment
12	HCLR1	I	Port 1 horizontal clear
13	$\overline{WE}$	I	Port 0 write enable
14	VCLR0	I	Port 0 vertical clear
15	INC0	I	Port 0 line increment
16	HCLR0	I	Port 0 horizontal clear
17	CKW	I	Port 0 shift signal
18	NC	–	No connection
19	Vcc	–	Power supply (+5V)
20	Vss	–	Ground
21	NC	–	No connection
22	APM	I	Address preset mode enable
23	RM	I	Recursive mode enable
24	DIN3	I	Port 0 data input
25	DIN2	I	Port 0 data input
26	DIN1	I	Port 0 data input
27	DIN0	I	Port 0 data input
28	HCLR2	I	Port 2 horizontal clear
29	INC2	I	Port 2 line increment
30	VCLR2	I	Port 2 vertical clear
31	$\overline{OE2}$	I	Port 2 output enable
32	DO23	O	Port 2 data output
33	DO22	O	Port 2 data output
34	DO21	O	Port 2 data output
35	DO20	O	Port 2 data output
36	CKR2	I	Port 2 shift signal
37	TR2/ADD3	I/O	Read port 2 transfer synchronous Signal/Address 3 input
38	Vss	–	Ground

RM

According to the status of this pin, the CXK1206 operates in any of the two modes : one is the recursive mode with this pin set at high level, and the other is the non-recursive mode with this pin set at low level.

- Recursive mode : This mode permits sequential access to 960 × 306 memory cells up to 0 to 293759. Initialization is conducted by VCLR0, 1 and 2 pin input. In the case of Write, the serial data input when VCLR0 high level is latched by CKW is treated as the data input of Line 0 /Block 0. In the case of Read, the serial data output is given as the data for Line 0/Block 0 with a lag of 64 clocks from the moment when VCLR1 and 2 high level is latched by CKR1 and 2, respectively.
- Non-recursive mode : The mode treats 960 × 306 memory cells with a unit of 1 line/16 blocks (60 bits per block) and controls lines with VCLR0, 1 and 2 and INC0, 1 and 2 and blocks with HCLR0, 1 and 2. It is different from the recursive mode in that, in the case of Write, the serial data input when HCLR0 is latched by CKW is handled as the data input for Line 0 /Block 0, and in the case of Read, the serial data output is output from Read ports 1 and 2 as the data for line 0/Block 0 with a lag of 64 clocks from the moment when HCLR1 and 2 are latched by CKR1 and 2.

APM

This pin is necessary for the mode for presetting the block address in one line of the Write port, and the address preset mode is valid only when RM is set to low level (non-recursive mode). If this pin is at high level when HCLR0 is latched by CKW, one of 16 blocks is selected by four bits ADD0 to 3. When the address preset mode is not in use, do not fail to select low level, in which case, TSM, TR0, TR1 and TR2 become available from among the multi-functional pins (TR0/ADD0, TR1/ADD1, TSM/ADD2 and TR2/ADD3).

TR0/ADD0, TR1/ADD1, TSM/ADD2, TR2/ADD3

These pins serve as block address presetting pins when APM is at high level (address preset mode), (non-recursive mode) and as pins for transfer synchronization mode when APM is at low level.

- In the address preset mode, one of 16 line blocks of the Write port with the use of ADD0 to 3 four-bit binary data can be selected, and the data input is accepted as in the non-recursive mode.
- When TSM is at low level (master), signals for synchronizing other CXK1206s with master CXK1206 are output from TR0, TR1 and TR2, and when it is at high level (slave), in contrast, synchronizing signals are received. Also, use TSM pin with a fixed DC and does not change it during device operation.
- TR0 is the I/O pin for Write transfer synchronization of the Write port.
- TR1 is the I/O pin for Read transfer synchronization of the Read port 1.
- TR2 is the I/O pin for Read transfer synchronization of the Read port 2.
- When using in Transfer Synchronize mode, be sure to connect between master and slave for all of TR0, TR1 and TR2.

CKW

The rising edge of this pin issues a signal for latching data from input pins DIN0 to 3 into the shift register and input of internal address pointer control pins (VCLR0, HCLR0 and INC0). Since this signal serves also as the basic signal for start control of the internal clock synchronizing logical circuit and the dynamic RAM, it is necessary to cause clock operation irrespective of the presence of Write operation.

VCLR0

The pin plays different roles between high level (recursive mode) and low level (non-recursive mode) of pin RM.

The number of counts of VCLR0 is counted only for latch of high level after recognition of low level of the latched state by CKW. Continuation of high level is counted as one.

- In recursive mode : When CKW latches VCLR0's high level, the then Serial write data input is taken in as the data of * (0, 0). From among the data entered so far data of less than a block as partitioned by block (60 bits) are rejected.
  * (0, 0) means Line 0/Block 0 ; (v, h) means the number of lines and that of blocks upon input of control signal.
- In non-recursive mode : When CKW latches high level of VCLR0, shift advances until the block (60 bits) during Serial write is filled up, and the line is cleared. More specifically, if VCLR0 is entered during Serial write, it is transferred to the (v, h) memory cell after the completion of input of 60 bits, and the data to be serially written are transferred to (0, h + 1) memory cell.

HCLR0

When high level of this pin is latched by CKW, the then input data is first taken in as (v, 0) data. Input data already entered and not sufficient to fill up a block (60 bits) are rejected. When pin RM is at high level (recursive mode), a signal to this pin has no meaning.

The number of counts of HCLR0 is counted only for the latch of high level after recognition of low level of the latched state by CKW for each time. Continuation of high level is counted as one.

INC0

When this pin is latched by CKW, the lines in the corresponding number are incremented. The incremented lines become valid in two cases : when HCLR0's high level is latched, or when VCLR0's high level is latched, and the shift register then advances to the end of that block. When pin RM is at high level (recursive mode), a signal to this pin has no meaning.

The number of counts of INC0 is counted only for the latch of high level after recognition of low level of the state latched by CKW. Continuation of high level is counted as one.

- When combining with VCLR0, the number of counts n of INC0 during the time from the state of VCLR0 latched by CKW until the shift register is filled up with 60 bits during Write causes Write of data input for the next 60 bits to be written into (n, h + 1) memory cell.
  INC0 is invalid, however, when INC0 is used simultaneously with VCLR0.
- When combining with HCLR0, the number of counts n of INC0 during the period from HCLR0's state latched by CKW last time up to the current latch causes 60 bits of data input to be entered next to be written into (v + n, 0) memory.
  INC0 is valid when INC0 is used simultaneously with HCLR0.

CKR1 and 2

The rising edge of these pins moves the shift register of the Read port and issues a signal for output of data to output pins DO10 to 13 and DO20 to 23 and a signal for latching the input of each internal address pointer control pin (VCLR1 and 2, HCLR1 and 2, and INC1 and 2).

VCLR1 and 2

The role of these pins is different between high level (recursive mode) and low level (non-recursive mode) of pin RM.

The number of counts of VCLR1 and 2 is counted only for latch of high level after recognition of low level of the state latched by CKR1 and 2, respectively. Continuation of high level is counted as one.

- In recursive mode : When CKR1 or 2 latches high level of VCLR1 or 2, (0, 0) data is output with a lag of 64 clocks from that moment. In the meantime, the shift register (60 bits) in shift is output to the full to retain the last output.
- In non-recursive mode : When CKR1 or 2 latches high level of VCLR1 or 2, it outputs the block currently in Serial read and 60 bits of the next block, and then output of consecutive blocks of the cleared line is started. More particularly, when VCLR1 or 2 is latched and the line of the internal address counter is hence cleared, the data (v, h + 1) for the next serial output have already been transferred from the memory cell to the data register, and while outputting the data, it transfers (0, h + 2) data and then outputs (0, h + 2) data.

HCLR1 and 2

When high level of this pin is latched by CKR1 or 2, (v, 0) data are output with a lag of 64 clocks from that moment. In the meantime, it outputs the shift register data in shift to the full to retain the final output. When pin RM is at high level (recursive mode), a signal to any of these pins has no meaning.

The number of counts of HCLR1 and 2 is counted only for high level latch after recognition of the state latched by CKR1 or 2. Continuation of high level is counted as one.

INC1 and 2

When high level of these pins is latched by CKR1 or 2, lines corresponding to the number of times of latching are incremented. The incremented lines become valid in two cases : when HCLR1 or 2 high level is latched, or when high level of VCLR1 or 2 is latched, and then the line address is latched at clock 57 of that block. When pin RM is at high level (recursive mode), a signal to any of these pins has no meaning.

The number of counts n of INC1 and 2 is counted only for the latch of high level after recognition of low level of the state latched by CKR1 or 2. Continuation of high level is counted as one.

- When combining with VCLR1 or 2, the number of counts n of INC1 and 2 prior to clock 56 of the block of VCLR1 or 2 latched by CKR1 or 2 causes (n, h + 2) memory cell data to become data to be output from the shift register for the 2'nd next time.

  When INC1 and 2 are used simultaneously with VCLR1 and 2, respectively, however, INC1 and 2 are invalid.
- When combining with HCLR1 and 2, the number of counts n of INC1 and 2 during the time from the last latching of HCLR1 and 2 by CKR1 and 2, respectively, up to the current latching causes (v + n, 0) memory cell data to become shift data to be output with a lag of 64 clocks from HCLR1 and 2.

  When INC1 and 2 are used simultaneously with HCLR1 and 2, respectively, INC1 and 2 are valid.

Data Input (DIN0 to 3)

Information to a data input pin is accepted at rising edge of CKW in the state of "L" of $\overline{WE}$, and entered into the shift register. When $\overline{WE}$ is at "H", input data are not accepted, without operation of the Write shift register (Write clock gate function).

Input into the shift register is accomplished immediately, whereas the information is loaded to the data register after completion of input of one block (60 bits) and transferred to the memory cell before the shift register is filled up with new data. Therefore, Serial write data input in the case of Serial write is transferred to the memory cell with a lag of one block.

Input control ($\overline{WE}$)

Input control to DIN0 to 3 is conducted with $\overline{WE}$. When $\overline{WE}$ is at "L", synchronization with CKW enables input, and when $\overline{WE}$ is at "H", input is not accepted and shift operation of the Write shift register is discontinued. This is used, for example, when thinning out data input (gate function of Write-side input clock (CKW) by $\overline{WE}$).

Data output (DO10 to 13, DO20 to 23)

The three-state TTL level is adopted for the output buffer. When $\overline{OE1}$ and $\overline{2}$ are at "L", output is immediately enabled and data in synchronization with CKR1 and 2 are output. When $\overline{OE1}$ and $\overline{2}$ are at "H", output is in high impedance state, but the shift register operates in synchronization with CKR1 and 2 and conducts transfer between memory cell and data register and load between data register and shift register.

Output from the shift register is made from time to time. Data in output are those transferred from the memory cell to the shift register by one block prior to the block in current output.

Output control ($\overline{OE1}$ and $\overline{2}$)

$\overline{OE1}$ conducts output control of only output pins DO10 to 13, and $\overline{OE2}$ conducts output control of only output pins DO20 to 23, without arresting shift operation of the shift register of Read port. Output control of DO10 to 13 and DO20 to 23 brings about output enable without being synchronized with CKR1 and 2 when $\overline{OE1}$ and $\overline{OE2}$ are at "L", and brings the output to high impedance state without being synchronized with CKR1 and 2 at "H".

Electrical Characteristics

DC characteristics

(Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	I_{CC1}	tscw0 = 70ns tscr1, 2 = 70ns	—	—	45	mA
(Normal operation)	I_{CC2}	tscw0 = 70ns tscr1, 2 = 35ns	—	—	60	mA
(Normal operation)	I_{CC3}	tscw0 = 50ns tscr1, 2 = 50ns	—	—	60	mA
(Normal operation)	I_{CC4}	tscw0 = 50ns tscr1, 2 = 30ns	—	—	75	mA
Supply current (upon refreshing) *1, 2	I_{CC5}	tscw0 = 420ns tscr = 70ns	—	—	20	mA

Item	Symbol	Min.	Max.	Unit
Input leak current (total input) (0V ≦ Vin ≦ 5.5V; 0V, Vcc = 5.5V except for testing pins)	I_I (L)	−10	10	μA
Output leak current (output high impedance state; 0V ≦ Vout ≦ 5.5V)	Io (L)	−10	10	μA
Output voltage "H" level (I_{OH} = −2 mA)	V_{OH}	2.4	—	V
Output voltage "L" level (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V

Note) *1. Output pin is open.
Supply current is dependent upon cycle time and output load.
*2. WE = "H", only one Read port operates.

AC characteristics

(Vcc = 5V ± 10%, Vss = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Refreshing interval	t_{REF}		—	—	21	ms
CKR cycle time	t_{SCR}		30	—	70	ns
CKR, CKW pulse duration	t_{CK}		8	—	—	ns
CKR, CKW precharge time	t_{SP}		8	—	—	ns
Access time from CKR	t_{SAC}		—	—	25	ns
Data output hold time from CKR	t_{SOH}		5	—	—	ns
Access time from $\overline{OE}$	t_{OEA}		—	—	20	ns
Data output hold time from $\overline{OE}$	t_{OEH}		5	—	—	ns

Note) Input dummy cycle after a pause of over 200 μs from the time power supply is turned on. Input dummy cycle to each port at least one. In recursive mode, input VCLR, and in non recursive mode, input VCLR and HCLR.

Item	Symbol	Min.	Typ.	Max.	Unit
Data output turnoff delay time from $\overline{OE}$	t_{OEZ}	–	–	20	ns
VCLR HCLR – CKR active setup time INC CKW	t_{CKS}	5	–	–	ns
VCLR HCLR – CKR active hold time INC CKW	t_{CKH}	7	–	–	ns
VCLR HCLR – CKR inactive setup time INC CKW	t_{CK1}	5	–	–	ns
VCLR HCLR – CKR inactive hold time INC	t_{CK2}	7	–	–	ns
CKW cycle time	t_{SCW}	50	–	2tscr	ns
DIN, CKW setup time	t_{DS}	5	–	–	ns
DIN, CKW hold time	t_{DH}	7	–	–	ns
$\overline{WE}$, CKW active setup time	t_{WES}	5	–	–	ns
$\overline{WE}$, CKW active hold time	t_{WEH}	7	–	–	ns
$\overline{WE}$, CKW inactive setup time	t_{WE1}	5	–	–	ns
$\overline{WE}$, CKW inactive hold time	t_{WE2}	7	–	–	ns
ADD, CKW setup time	t_{AS}	10	–	–	ns
ADD, CKW hold time	t_{AH}	8	–	–	ns
Input pulse rising and falling period	t_T	3	–	40	ns

Clock correlation

CXK1206M uses a DRAM in the memory block. Accordingly and in order to hold data, either of the following clock relations has to be satisfied. In NRM (Non Recursive Mode) and using HCLR with INC, keep access time to all memory zones utilized, within 21msec.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 2 × T_{SCR1}	30 to T_{MAX}	T_{SCR1} to stop	ns
50 to 2 × T_{SCR2}	T_{SCR2} to stop	30 to T_{MAX}	ns

To access 1 picture (960 dots × 306 lines) in less than 21msec, maximum cycle time, TMAX when CKR1 (or CKR2) is applied continuously is obtained as follows.

$$T_{MAX} = \frac{21\,msec}{960\ dots \times 306\ lines} \fallingdotseq 70nsec$$

Standby mode to hold image data

To reduce power consumption while image data is held, keep WE = H fixed and use only 1 port of the read side. In this case write in is not performed. Clock correlation turns out as either of the following cases. In NRM (Non Recursive Mode) and using HCLR with INC, keep access time to all memory zones utilized, within 21msec.

T_{SCW}	T_{SCR1}	T_{SCR2}	
50 to 6 × T_{SCR1}	30 to T_{MAX}	Stop	ns
50 to 6 × T_{SCR2}	Stop	30 to T_{MAX}	ns

To access 1 picture (960 dots × 306 lines) in less than 21msec, maximum cycle time, TMAX when CKR1 (or CKR2) is applied continuously is obtained as follows.

$$T_{MAX} = \frac{21\,msec}{960\ dots \times 306\ lines} \fallingdotseq 70nsec$$

I/O capacity

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input	C_{IN}	TA = 0°C to +70°C	—	—	7	pF
Data output capacity (DO10 to DO23)	C_D	Vcc = +5V ± 10%	—	—	7	pF
I/O capacity (ADD0 to ADD3)	C_T		—	—	10	pF

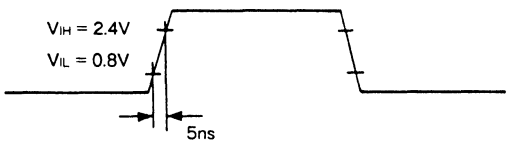
Transfer Synchronize AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Transfer access time from CKW *1	t_{TAC}	—	—	25	ns
Number of transfer output pulse TR0 *1 TR1, TR2 *1	 t_{TWOP} t_{TROP}	 5 4	 5 4		*2
Transfer output • Turn off delay time from CKW *1	t_{TZ}	—	—	25	ns
Transfer output interval • Number of pulse	t_{TOI}	1			*2
TR0 TR1—CKW active set up time TR2	t_{TS}	15	—	—	ns
TR0 TR1—CKW active hold time TR2	t_{TH}	7	—	—	ns
TR0 TR1—CKW inactive set up time TR2	t_{TSS1}	7	—	—	ns
TR0 TR1—CKW inactive hold time TR2	t_{TSS2}	7	—	—	ns
Number of transfer input pulse TR0 TR1, TR2	 t_{TWIP} t_{TRIP}	 5 4	 5 4		*2
Transfer input interval • Number of pulse	t_{TII}	1			*2

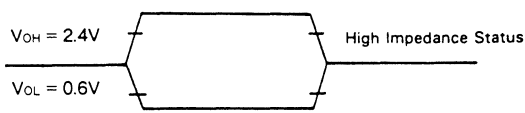
Note) *1. 40pF load
*2. Number of tscw.

AC Characteristic Test Condition

1) Input

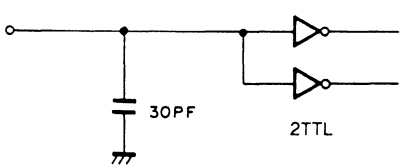


2) Output



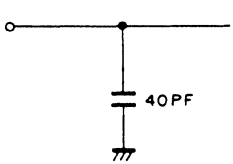
3) Data Output Load

DO10 to 13, 20 to 23



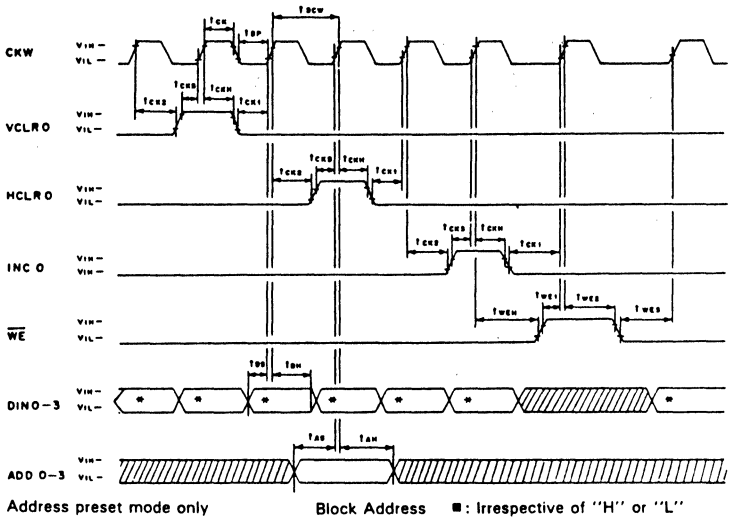
4) Transfer Output Load

TRO, 1, 2



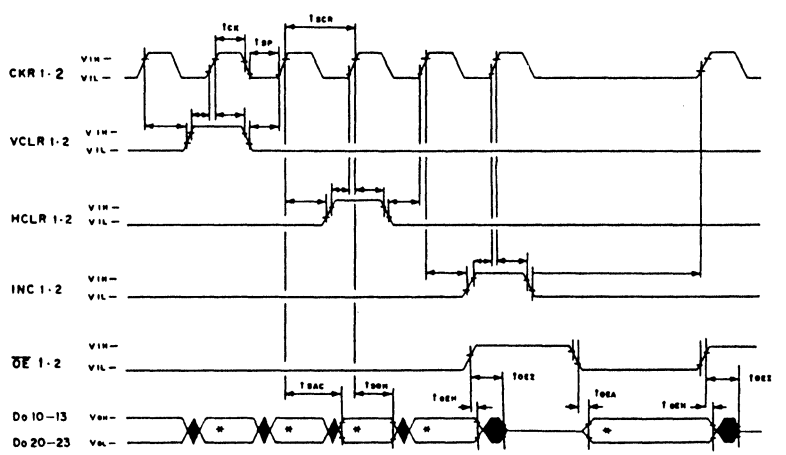
Timing Chart

Write port



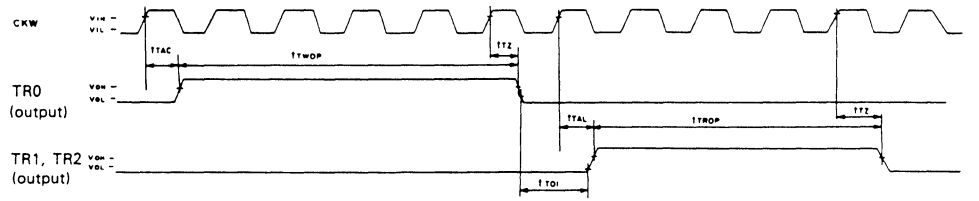
*: Input determination period; irrespective of "H" or "L" by certain control of VCLR0, etc.

Read port

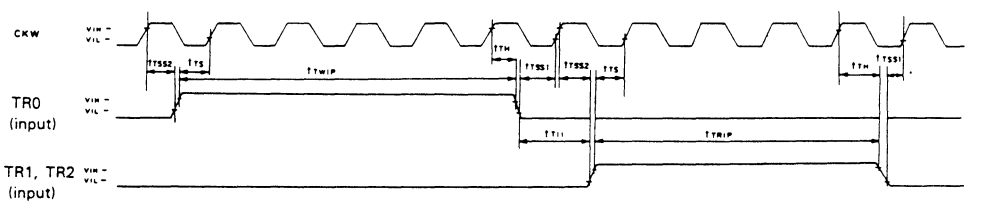


*: Output determination period ■: Invalid data

Transfer synchronizing master chip



Transfer synchronizing slave chip



Description of Operation

CXK1206 has the following five operating modes. As to the details of timing, etc., refer to the separate description:

1. Recursive mode, transfer synchronous mode output:
   These modes handle the memory as a simple delay line. Control is accomplished via VCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$ and $\overline{OE2}$. The synchronizing signal for use of multiple chips is output (forming master chips).

2. Recursive mode, transfer synchronous mode input:
   A synchronizing signal is entered in the mode as described in 1 above (becoming slave chip).

3. Non-recursive mode, transfer synchronous mode output:
   This is the mode for controlling the memory by block or line. Control is accomplished via VCLR0, 1 and 2, INC0, 1 and 2, HCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$ and $\overline{OE2}$. The synchronizing signal for use of multiple chips is output (forming master chips).

4. Non-recursive mode, transfer synchronous mode input:
   A synchronizing signal is entered in the three modes as described above (becoming slave chips).

5. Non-recursive mode, address preset mode:
   This is the mode for controlling the memory by block or line, and permits setting any address by block when writing in the memory. Control is accomplished via VCLR0, 1 and 2, INC0, 1 and 2, HCLR0, 1 and 2, $\overline{WE}$, $\overline{OE1}$, $\overline{OE2}$, and ADD0, 1, 2 and 3. A synchronizing signal cannot be entered or output when using multiple chips in this mode.

Function Table

Function table 1 [List of Operating modes]

Operating mode	Control input			Address input	TS input/output
	RM	TSM	APM	ADD0 to 3	TR0 to 2
Recursive mode, Transfer synchronous mode output	H	L	L	—	Output determination
Recursive mode, Transfer synchronous mode input	H	H	L	—	Input determination
Non-recursive mode, Transfer synchronous mode output	L	L	L	—	Output determination
Non-recursive mode, Transfer synchronous mode input	L	H	L	—	Input determination
Non-recursive mode, Address preset mode	L	—	H	Input determination	—

—: This pin name is non-existent in this mode.

Address-block division correspondence table

Block No.	ADD3	ADD2	ADD1	ADD0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Note) The block number indicates the increasing direction in the order of Write or Read in a line.

Function table 2 [Write]

Mode		Operating cycle	RM	VRO	HRO	ICO	APM	A0 to 3	Internal address pointer
Recursive mode	1	Initial cycle	H	H	—	—	L	—	Goes back to 0.
	2	Normal cycle		L	—	—	L	—	After advancing in order from 0 to 293759, goes back to 0 to repeat the cycle to 293759.
Non-recursive mode	1	Initial cycle	L	H*1	H*1	L	L*5	—	v and h are both cleared. (v, h) → (0, 0)
	2	Normal cycle		L	L	L	L*5	—	Advances up to the end of v line. After that write operation is not performed.
	3	First block cycle		L	H	L	L*5	—	Only h is cleared. (v, h) → (v, 0)
	4	Line address cycle		L	H	nH*2	L*5	—	v advances to n line and h is cleared. (v, h) → (v + n, 0)
	5	VCLR0 special cycle No. 1		H	L	L	L*5	—	After advancing to the end of h block, v is cleared. (v, h) → (0, h + 1)
	5	VCLR0 special cycle No. 2		H	L	nH*3	L*5	—	After advancing to the end of h block, v is set to n line. (v, h) → (n, h + 1)
	5	VCLR0 special cycle No. 3		H*4	H*4	nH*4	L*5	—	v is set to n line and h is cleared. (v, h) → (n, 0)

VRO: VCLR0
HRO: HCLR0
ICO: INC0
A0 to 3: ADD0 to 3
(v, h), v: Number of the line for Write port upon input of control signal
h: Number of the block for Write port upon input of control signal
H: High level latched by CKW
nH: Number of times of high level latched by CKW is n.

Note) • This device is arranged in 306 lines, 16 blocks and 60 bits.
• For Write address counter reset, it is necessary to make at least one input of VCLR0 in recursive mode, or VCLR0 and HCLR0 in non-recursive mode.
• It is necessary to set low or high in DC manner for pins RM and APM input.

*1. It is necessary to enter VCLR0 and HCLR0 at the same time, or to enter HCLR0 prior to the first clock of the block next to the block containing VCLR0.
*2. nH: Number of times of "H" of INC0 prior to HCLR0 after the current HCLR0.
*3. nH: Number of times of "H" of INC0 prior to the first clock of the block next to the h block containing VCLR0.
*4. It is necessary to enter INC0 and HCLR0 prior to the first clock of the block next to that containing VCLR0.
*5. When pin APM is at low level, pin TSM becomes valid, and the Read ports and the Write port are in transfer synchronous mode. When pin TSM is at low level, transfer output is provided (master), and when it is at high level, transfer input is accepted (slave).

Function table 3 [Write]

Mode		Operating cycle	RM	VRO	HRO	ICO	APM	A0 to 3	Internal address pointer
Non-recursive, address preset mode	1	Initial cycle	L	H*1	H*1	L	H*5	Input determination	v is cleared and preset address ADD is set to h. (v, h) → (0, ADD)
	2	Normal cycle		L	L	L	H*5	——	Advances up to the end of v line. After that write operation is not performed.
	3	Address preset cycle		L	H	L	H*5	Input determination	Preset address ADD is set to h. (v, h) → (v, ADD)
	4	Line address, block address preset cycle		L	H	nH*2	H*5	Input determination	v advances to n line, and preset address ADD is set to h. (v, h) → (v + n, ADD)
	5	VCLR0 special cycle No. 1		H	L	L	H*5	——	After advancing to the end of h block, v is cleared. (v, h) → (0, h + 1)
	5	VCLR0 special cycle No. 2		H	L	nH*3	H*5	——	After advancing to the end of h block, v is set to n line. (v, h) → (n, h + 1)
	5	VCLR0 special cycle No. 3		H*4	H*4	nH*4	H*5	Input determination	n line is set to v and preset address ADD is set to h. (v, h) → (n, ADD)

VR0: VCLR0
HR0: HCLR0
IC0: INC0
A0 to 3: ADD0 to 3
(v, h), v: Number of the line for Write port upon input of control signal
h: Number of the block for Write port upon input of control signal
H: High level latched by CKW
nH: Number of times of high level latched by CKW is n.

Note) • This device is arranged in 306 lines, 16 blocks and 60 bits.
• For Write address counter reset, it is necessary to make at least one input of VCLR0 in recursive mode, VCLR0 and HCLR0 in non-recursive mode.
• It is necessary to set low or high in DC manner for pins RM and APM input.

*1. It is necessary to enter VCLR0 and HCLR0 at the same time, or to enter HCLR0 prior to the first clock of the block next to the block containing VCLR0.
*2. nH: Number of times of "H" of INC0 prior to HCLR0 after the current HCLR0.
*3. nH: Number of times of "H" of INC0 prior to the first clock of the block next to the h block containing VCLR0.
*4. It is necessary to enter INC0 and HCLR0 prior to the first clock of the block next to that containing VCLR0.
*5. In the Function table for address preset mode, the block address is latched with high level of HCLR0 latched by CKW.

Function table 4 [Read]

Mode		Operating cycle	RM	VR1	HR1	IC1	Internal address pointer
Recursive mode	1	Initial cycle	H	H	–	–	Advancing to end of (v, h) to (0, 0) with lag of 64 clocks from VCLR1
	2	Normal cycle		L	–	–	Circulating between 0 and 293759
Non-recursive mode	1	Initial cycle	L	H*1	H*1	L	Advancing to end of (v, h), clearing both v and h with lag of 64 clocks from HCLR1, to (0, 0)
	2	Normal cycle		L	L	L	To end of (v, h)
	3	First block cycle		L	H	L	Advancing to end of (v, h) to (v, 0) with lag of 64 clocks from HCLR1
	4	Line address cycle		L	H	nH*2	Advancing to end of (v, h) to (v+n, 0) with lag of 64 clocks from HCLR1
	5	VCLR1 special cycle No. 1		H	L	L	Advancing to end of (v, h+1), clearing v, to (0, h+2)
	5	VCLR1 special cycle No. 2		H	L	nH*3	Advancing to end of (v, h+1), setting v, to (n, h+2)
	5	VCLR1 special cycle No. 3		H*4	H*4	nH*4	Advancing to end of (v, h), setting v and clearing h with lag of 64 clocks from HCLR1, to (n, 0)

VR1: VCLR1
HR1: HCLR1
IC1: INC1
(v, h) v: Number of the line for Read port upon input of control signal
h: Number of the block for Read port upon input of control signal
H: High level latched by CKR1
nH: Number of times of high level latched by CKR1 is n.

Note)
- This device is configured with 306 lines, 16 blocks and 60 bits.
- In Read, address preset cannot be done irrespective of pin APM control, but when pin APM is at low level, the mode becomes transfer synchronous mode.
- For Read address counter reset, it is necessary to make at least one input of VCLR1 and HCLR1 in non-recursive mode.
- It is necessary to set low or high in DC manner for pins RM and APM input.

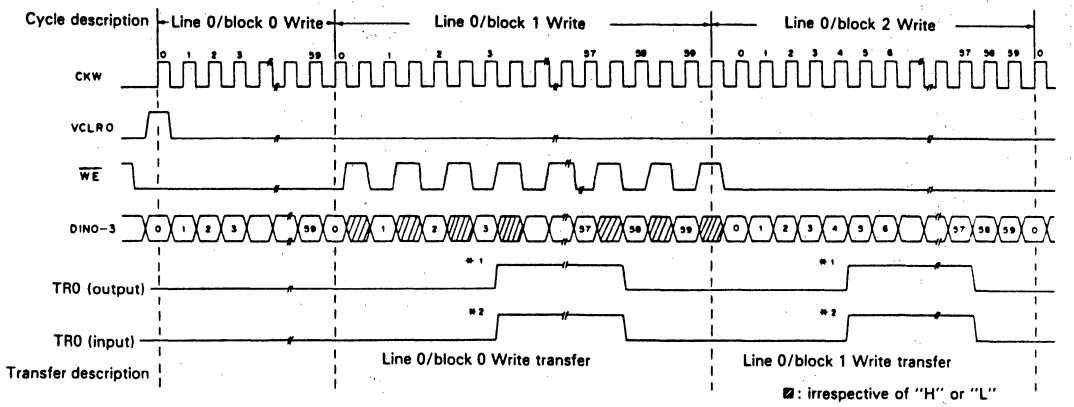
*1. It is necessary to enter VCLR1 and HCLR1 simultaneously, or to enter HCLR1 prior to clock 55 of the block containing VCLR1. To enter VCLR1 before the lapse of 64 clocks from HCLR1 is unabled.
*2. nH: Number of times of "H" of INC1 prior to HCLR1 after the current HCLR0.
*3. nH: Number of times of "H" of INC1 prior to the clock 55 of the h block after the current VCLR 1.
*4. It is necessary to enter INC1 and HCLR1 prior to the clock 55 of the h block containing VCLR0.

Function table 5 [Read 2]

The same particulars as those in Function table 4 apply also for VCLR2, HCLR2 and INC2.

Recursive mode, Write

1. Initial cycle 2. Normal cycle



Note) • After Write of up to Line 0/block 15, the next 60 bits are automatically written in block 0 of the next line.

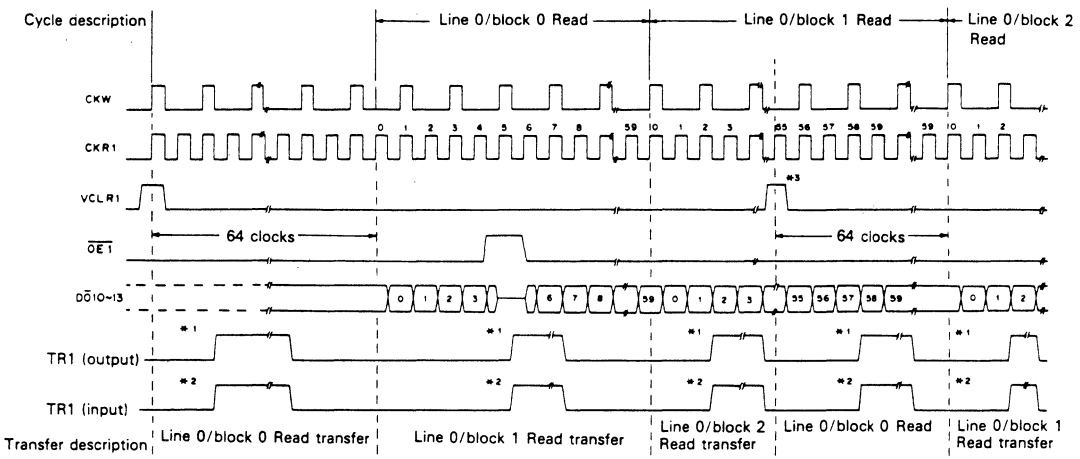
• After Write of up to Line 305/block 15, the next 60 bits are automatically written in line 0/block 0.

*1. When pin TSM = "L", output is made through automatic synchronization with CKW from the interior of device.

*2. Transfer input should be completed within a block Write. In the case of synchronous transfer between two chips, processing is made automatically between devices.

Recursive mode, Read

1. Initial cycle 2. Normal cycle



Note)

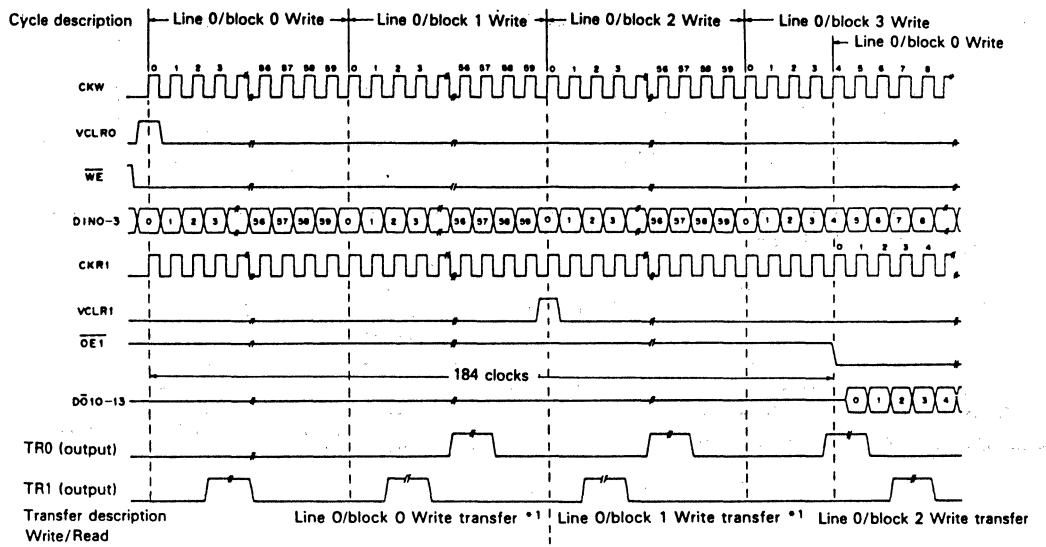
- After Read of up to Line 0/block 15, the next 60 bits are automatically read from block 0 of the next line.
- After Read of up to Line 305/block 15, the next 60 bits are automatically read from line 0/block 0.

*1. When pin TSM = "L", output is made through automatic synchronization with CKW from the interior of device.

*2. Transfer input should be completed within a block Read. In the case of synchronous transfer between two chips, processing is made automatically between devices.

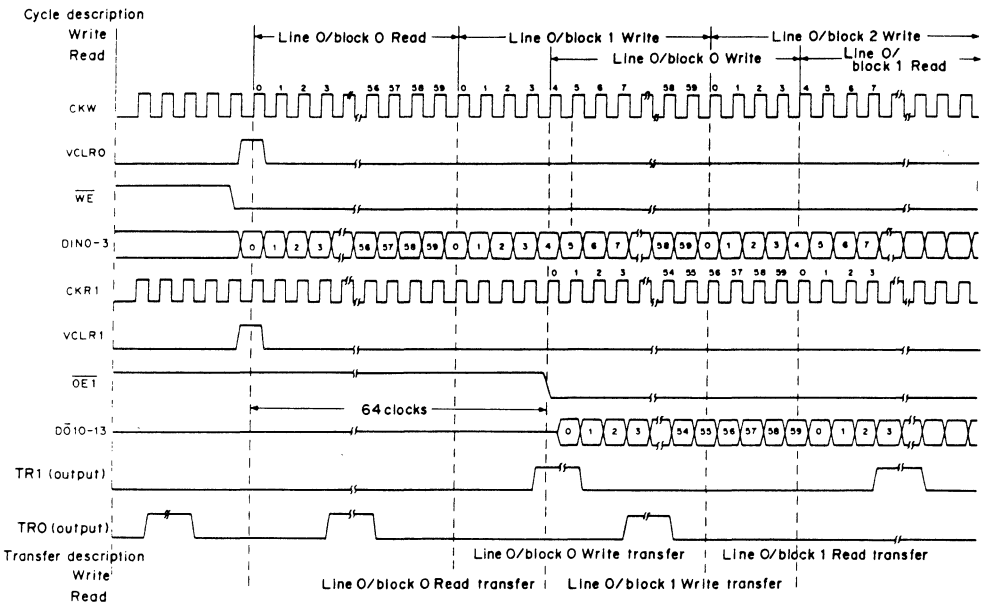
*3. If VCLR comes before 55th clock of the block currently Read, the final data of the block is retained. If VCLR comes after 56th clock of the block currently Read, data of the next block are read, following the current block. and the data of block 0 are output with a lag of 64 clocks from VCLR.

Recursive mode (in non-recursive mode, VCLR in the figure below corresponds to HCLR)
New data access mode



Note) *1. In order to access new data, block Write transfer is conducted after Write of 60 bits, and readout is made after Read transfer of that block. A lag of more than 184 clocks is necessary for Read clock from Write clock.

Recursive mode (in non-recursive mode, VCLR in the figure below corresponds to HCLR)
Old data access mode

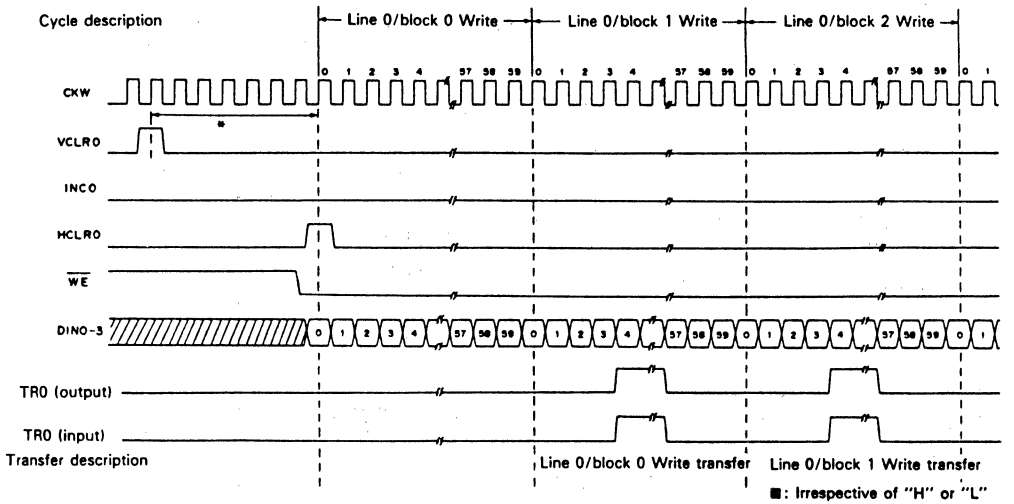


Note) • When the lag of Read clock from Write clock is more than 65 clocks and less than 183 clocks, Write of new data is guaranteed, although it is uncertain whether new data access or old data access.

* In order to access old data, Read transfer of that block should be accomplished before Write transfer of new data. A lag of less than 64 clocks is necessary for Read clock from Write clock.

Non-recursive mode, Write

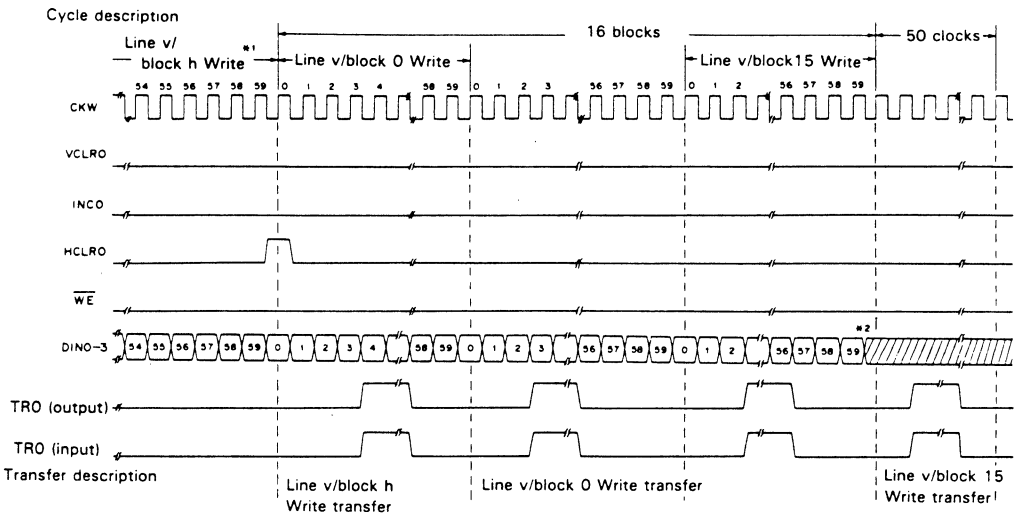
1. Initial cycle (the cycle for Writing from line 0/block 0)
2. Normal cycle



*Note) In the case of initial cycle, it is necessary to enter VCLR0 and HCLR0 simultaneously, or to enter HCLR0 before the first clock of the block next to that containing VCLR0.

Non-recursive mode, Write

3. First block cycle (the cycle for Writing data from the start of block)

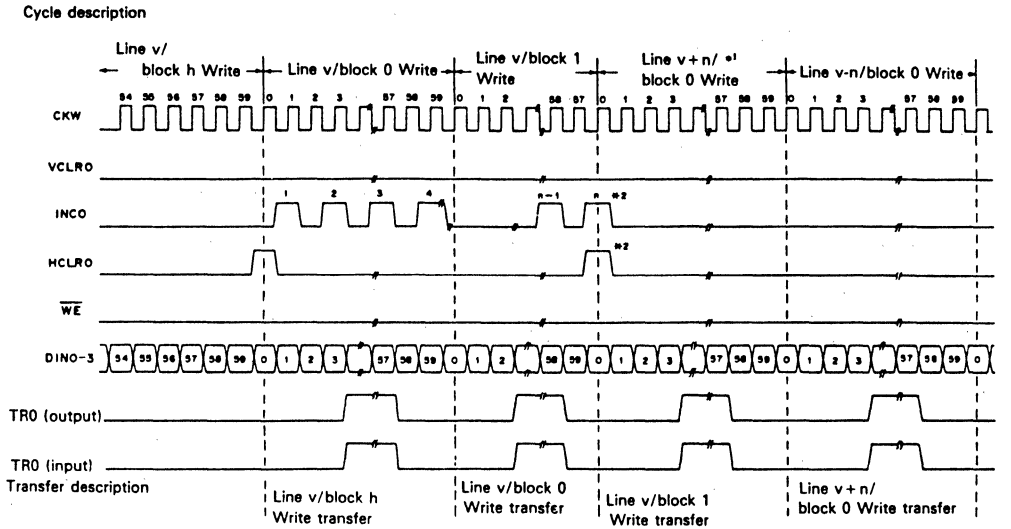


Note) *1. After Write of one block (60 bits), Write transfer is conducted in the next block.

*2. In non-recursive mode, after Write up to the final block of a line, no further Write is performed. Write transfer of the final block is accomplished during 60 clocks after the completion of final block Write.

Non-recursive mode, Write

4. Line address cycle (for address control in line direction)

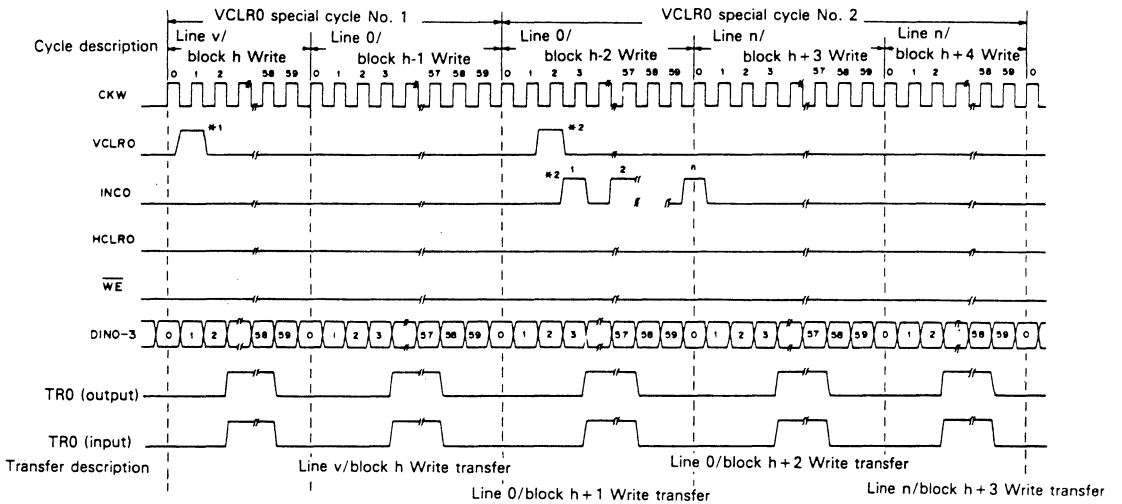


Note) *1. n is the number of times of INC0.

*2. Latch of this HCLR0 covers the range from the last HCLR0 up to INC0 entered at the same time as this HCLR0. Line address recursively circulates from the current address, depending upon the number of times of INC0.

Non-recursive mode, Write

5. VCLR0 special cycle No. 1 and No. 2



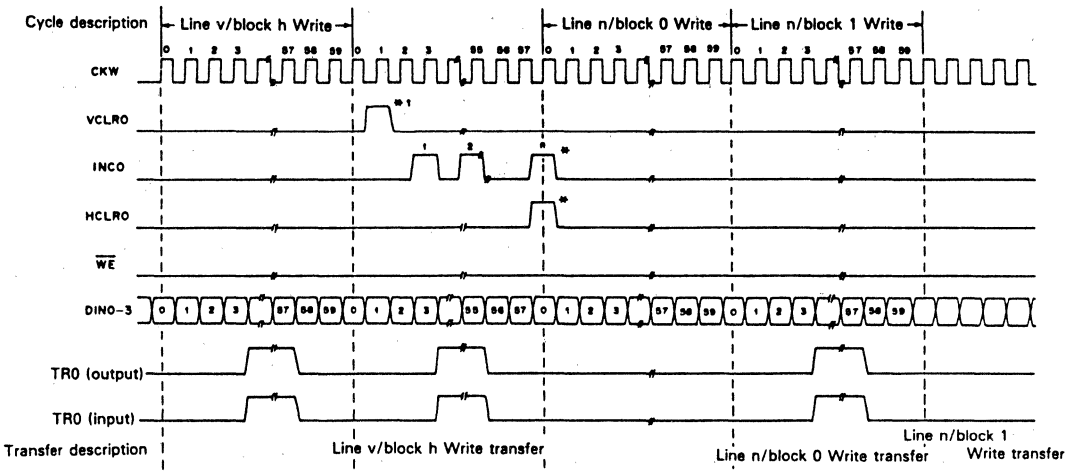
Note) *1. VCLR0 having entered after the 1st clock in the written block resets the line address, and is latched at the end of the block.

*2. When VCLR0 enters after the 1st clock in the written block, followed by INC0, the line address is reset, and line address in the number equal to the number of times of INC0 having entered block 1 Write are incremented, latching the line address at the beginning of the next block.

When VCLR0 and INC0 are simultaneously entered, only address reset becomes valid.

Non-recursive mode, Write

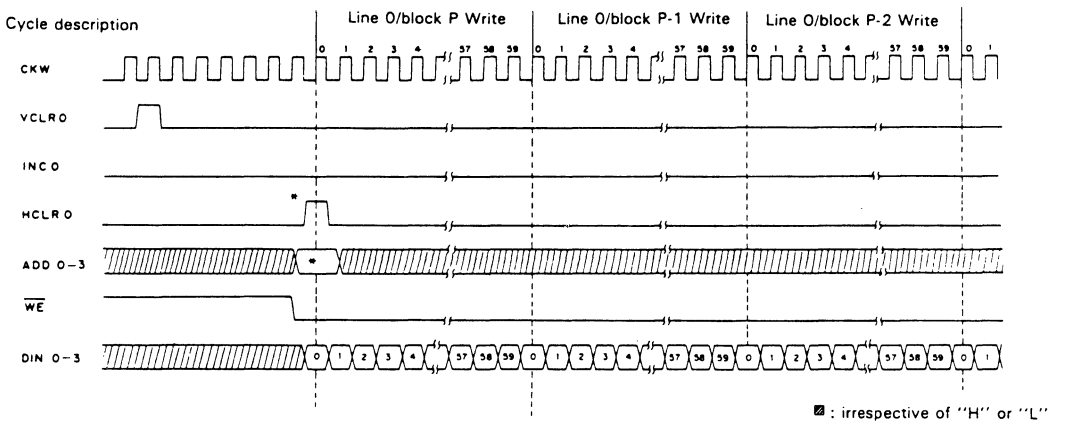
6. VCLR0 special cycle No. 3



***Note)** When VCLR0 enters after the 1st clock in the written block, followed by INC0 n times, and then by HCLR0, the line address is reset, and incremented in the number equal to the number of times of INC0. Latch of the line address and reset of the block address are carried out.

Non-recursive address preset mode, Write

1. Initial cycle 2. Normal cycle



***Note)** The block address is latched by HCLR0 in the case of address preset mode.

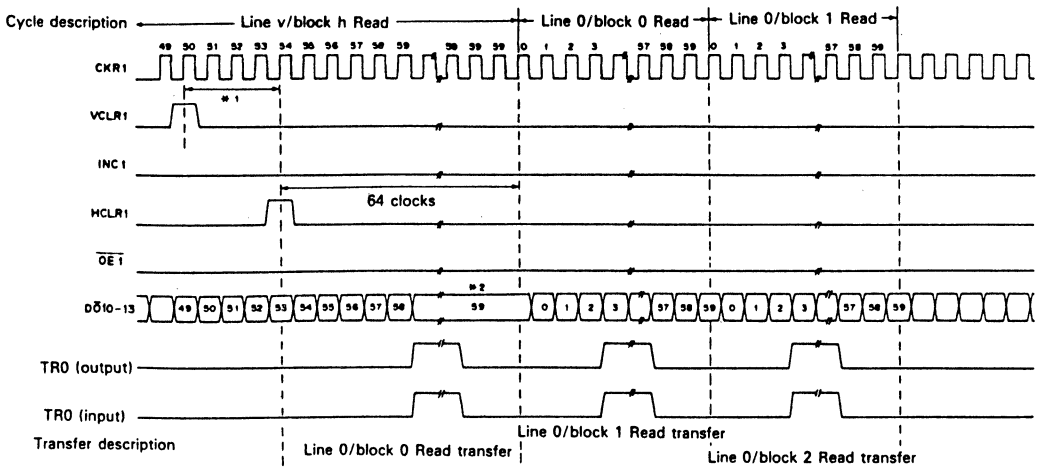
Non-recursive address preset mode, Write

3. Address preset cycle
4. Line address and block address preset cycle
5. VCLR0 special cycles Nos. 1, 2 and 3

For these cycles, refer to non-recursive mode considering the difference from non-recursive mode lying in that the block address is latched by HCLR0.

Non-recursive mode, Read

1. Initial cycle (the cycle Reading data from line 0/block 0)
2. Normal cycle

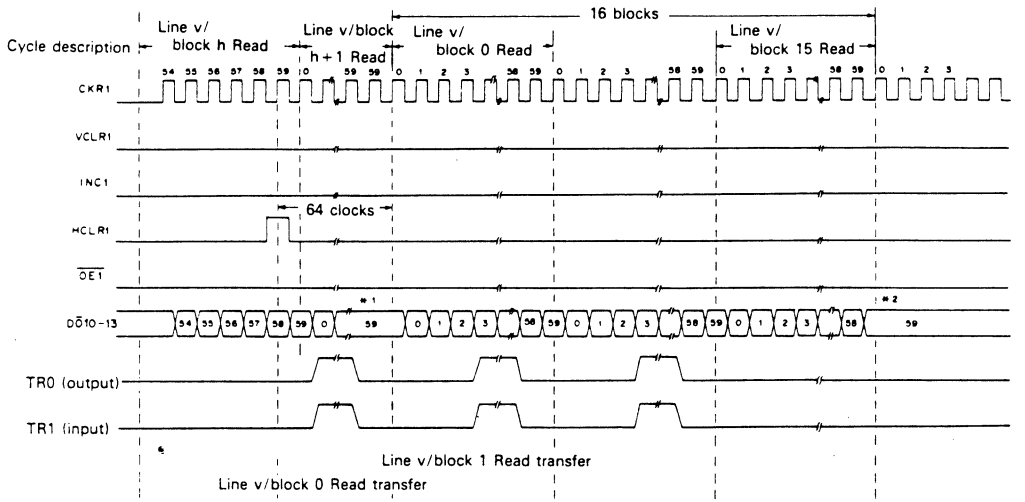


Note) *1. When VCLR1 and HCLR1 are simultaneously entered, or HCLR1 is entered before clock 55 of the block containing VCLR1, the data of line 0/block 0 are output with a lag of 64 clocks from HCLR1.

*2. If HCLR enters before clock 55 of the block currently Read, the final data of the block is retained. If HCLR enters after clock 56 of the block currently Read, the next block data are read, following the current block, and the data of block 0 are output with a lag of 64 clocks from HCLR.

Non-recursive mode, Read

3. First block cycle

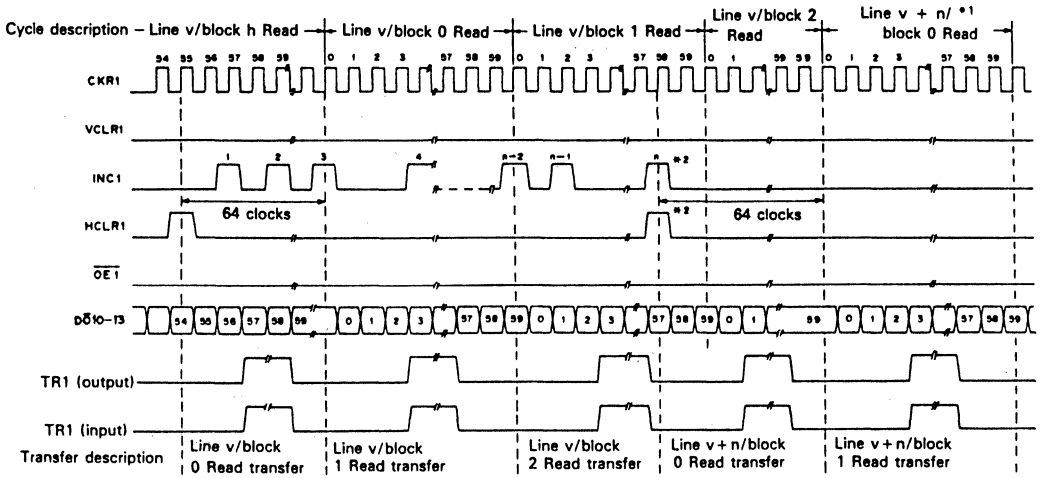


Note) *1. If HCLR enters before clock 55 of the block currently Read, the final data of the block is retained. If HCLR enters after clock 56 of the block currently Read, the next block data are read, following the current block, and the data of block 0 are output with a lag of 64 clocks from HCLR.

*2. In non-recursive mode, after Reading up to the final block of the line, the final data output is retained.

Non-recursive mode, Read

4. Line address cycle

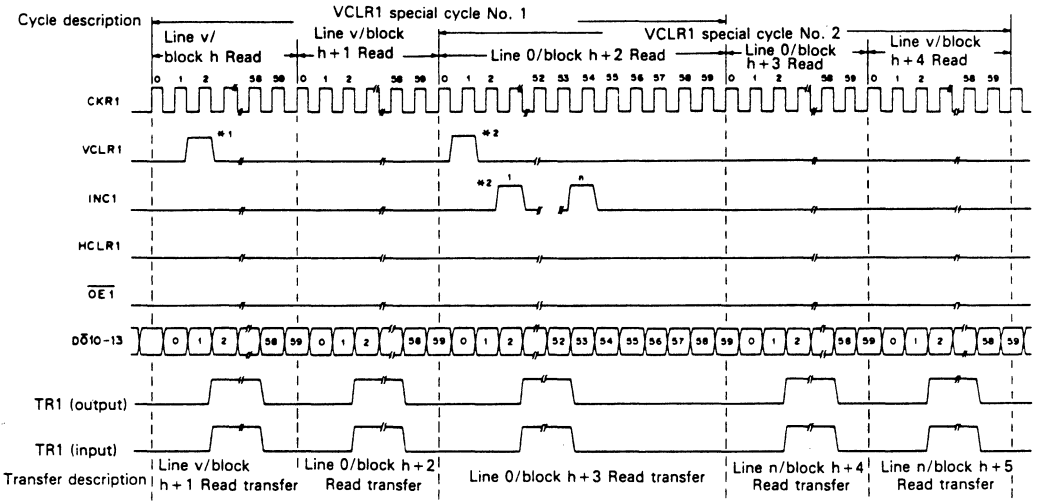


Note) *1. n is the number of times of INC1.

*2. Latch by this HCLR1 covers the range from the clock next to the last HCLR1 up to INC1 having entered simultaneously with this HCLR1. The line address recursively circulates from the current address, depending upon the number of times of INC1.

Non-recursive mode, Read

5. VCLR1 special cycle Nos. 1 and 2

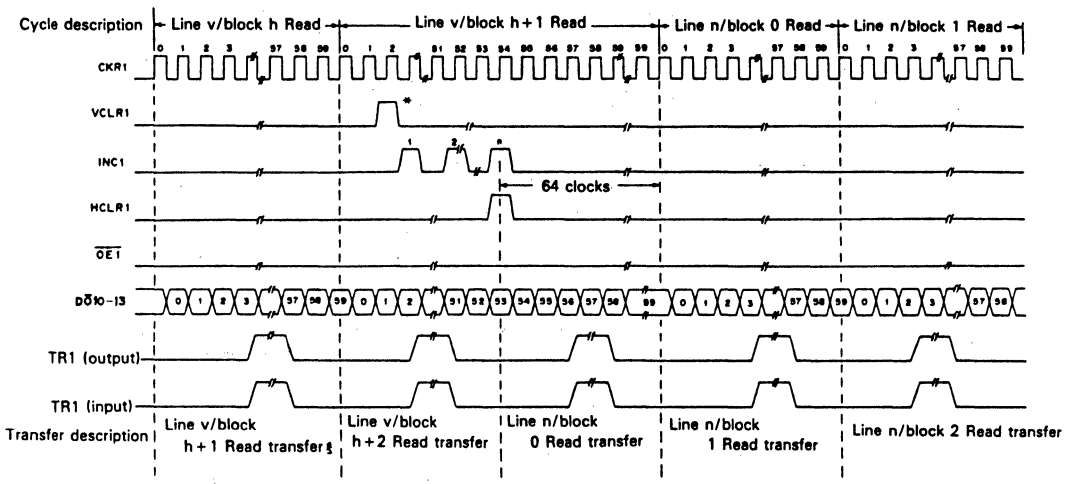


Note) *1. VCLR1 having entered before clock 56 in one block which has been read resets the line address and is latched at clock 57 of the block. In the next block, Read transfer of line 0/block h+2 is carried out.

*2 When VCLR1 enters before clock 56 in one block which has been read, followed by INC1, the line address is reset, and the line address is incremented in the number equal to the number of times of INC1 having entered before clock 56 in the block which has been read. The line address is latched at clock 57 of the block. When VCLR1 and INC1 enter simultaneously, the address reset becomes valid.

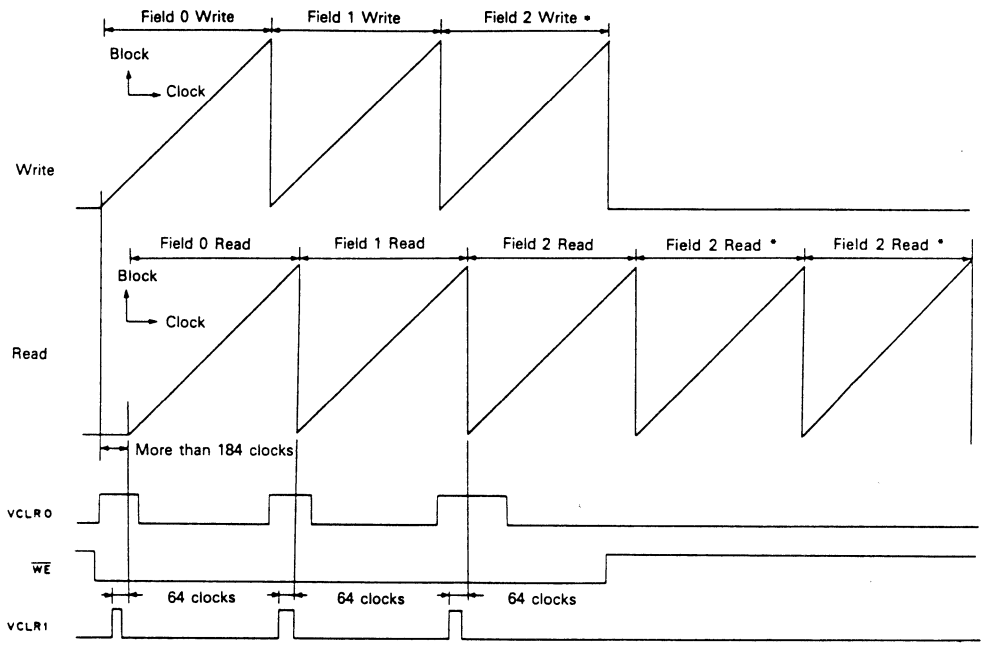
Non-recursive mode, Read

6. VCLR1 special cycle No. 3



*Note) When VCLR1 enters in one block, followed by INC1 n times, and then followed by HCLR1 before clock 56 of the block, the line address is incremented in the number equal to the number of times of INC1 after reset, and line address latch and block address reset are carried out at the next clock.

Example of Application 1 Delay line, field memory in case of recursive mode



Continuous input of CKW0, CKR1, $\overline{OE1}$ = "L"

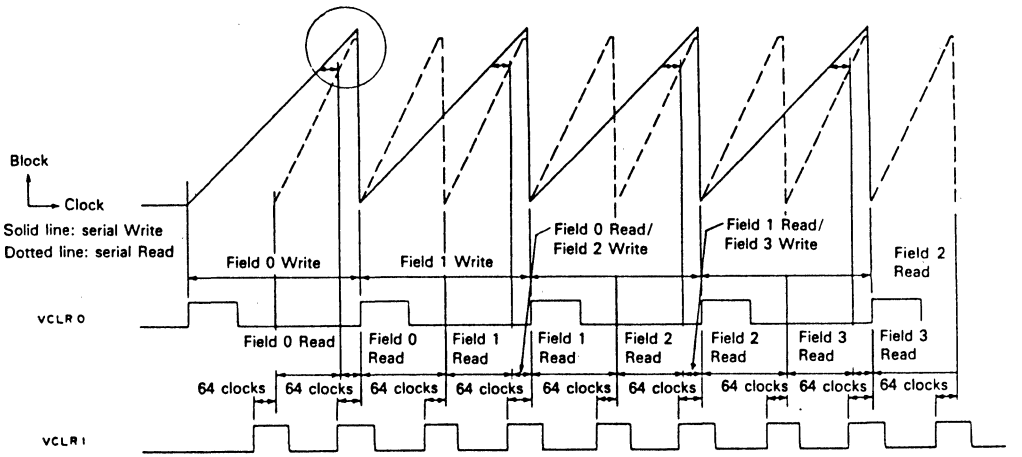
Note) • If the cycle time is equal between CKW and CKR1, this is possible also in the case of asynchronization.

• If the cycle time differs between CKW and CKR1, Read overtaking may occur. Refer to Example of Application 2.

• In non-recursive mode, it is necessary to advance the line for each line through combination of INC and HCLR input.

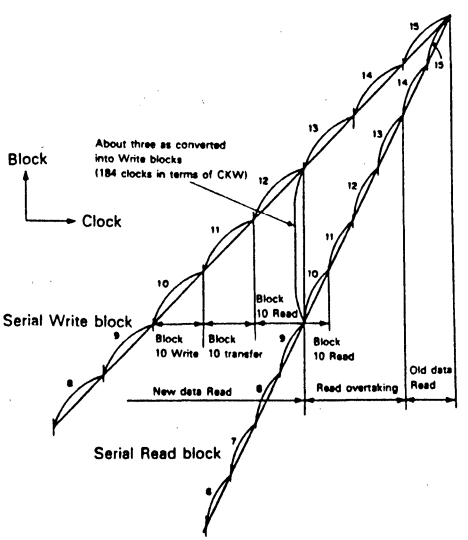
* When using 306 lines/16 blocks/60 bits, continuous Read is possible by only entering CKR1 and CKW without entering VCLR1.

Example of Application 2 Field double scan conversion in case of recursive mode



Note) Continuous input of CKW0 and CKR1. $\overline{WE}$ = "L", $\overline{OE1}$ = "L"

Description of circled drawing



- Read overtaking
  In order to Read data of written block in the case of field double scan conversion, the phase lag of Read as compared with write must be about three as converted into Write blocks (184 clocks in terms of CKW).
- When using two chips in 8-bit digitalized signal configuration, independent operation of the two chips may cause Read overtaking between the two chips. In order to synchronize Read overtaking between the two chips, use the transfer synchronous mode using one as the master chip, and the other as the slave chip.

Example of Application 3

Write of 1/2-compressed data in memory, non-recursive mode, address preset mode:

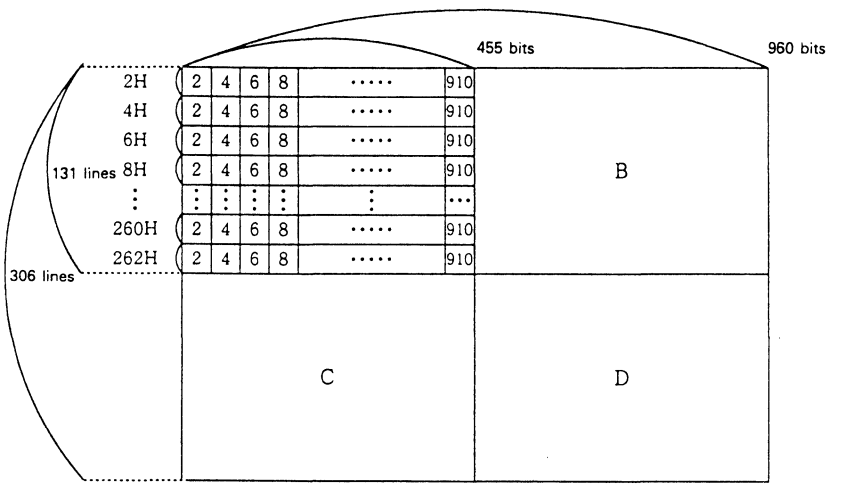
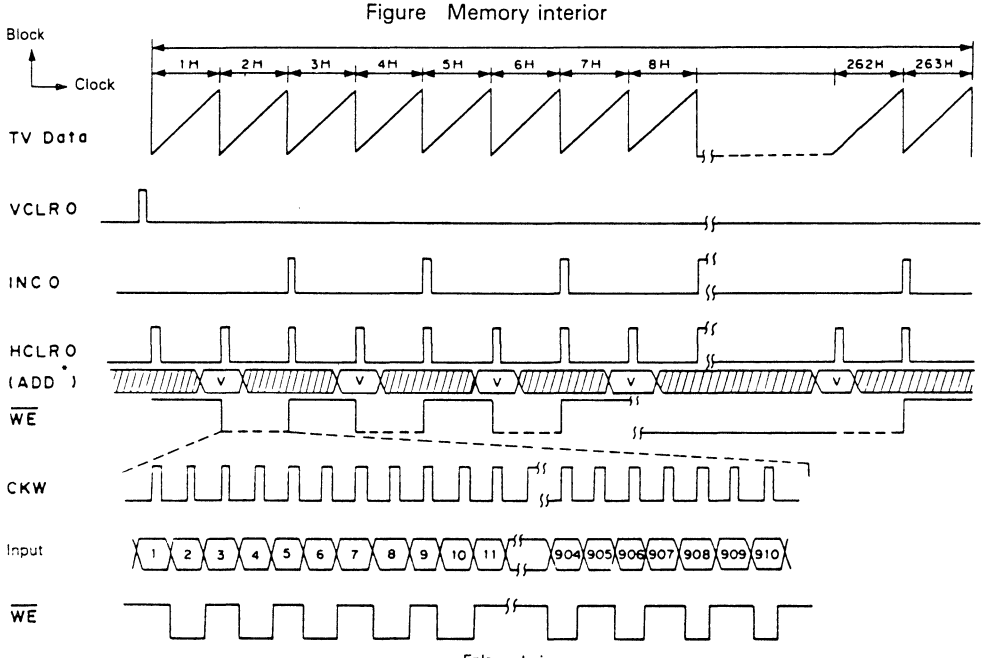


Figure Memory interior



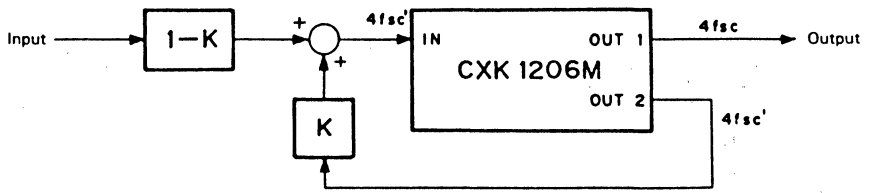
V: Valid address

▨: Irrespective of "H" or "L"

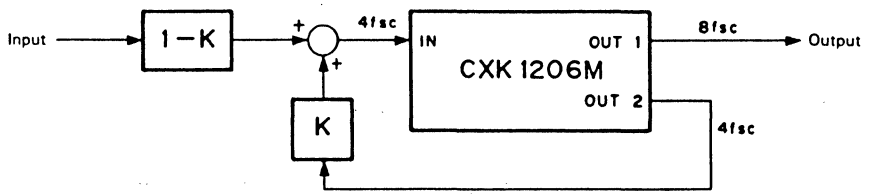
*Note) Use of the address preset mode permits Write to B, C and D areas. Write to area C is also possible by operating INC0 in non-recursive mode.

3-port VRAM Application Example

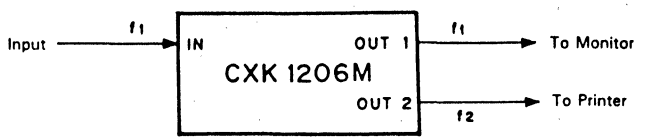
1. NR + TBC



2. NR + double-speed



3. Monitor and Printer Concurrent Drive

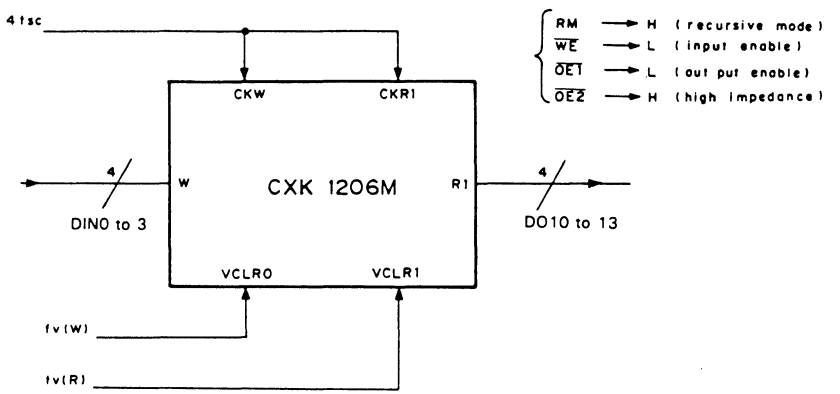


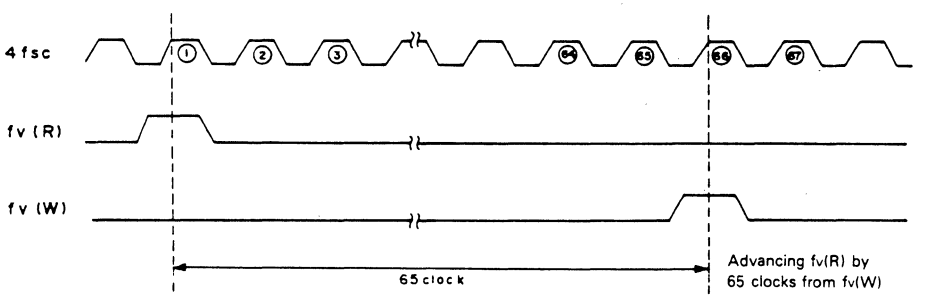
Application Circuit (1)

Using recursive mode: The following diagram shows a circuit with:

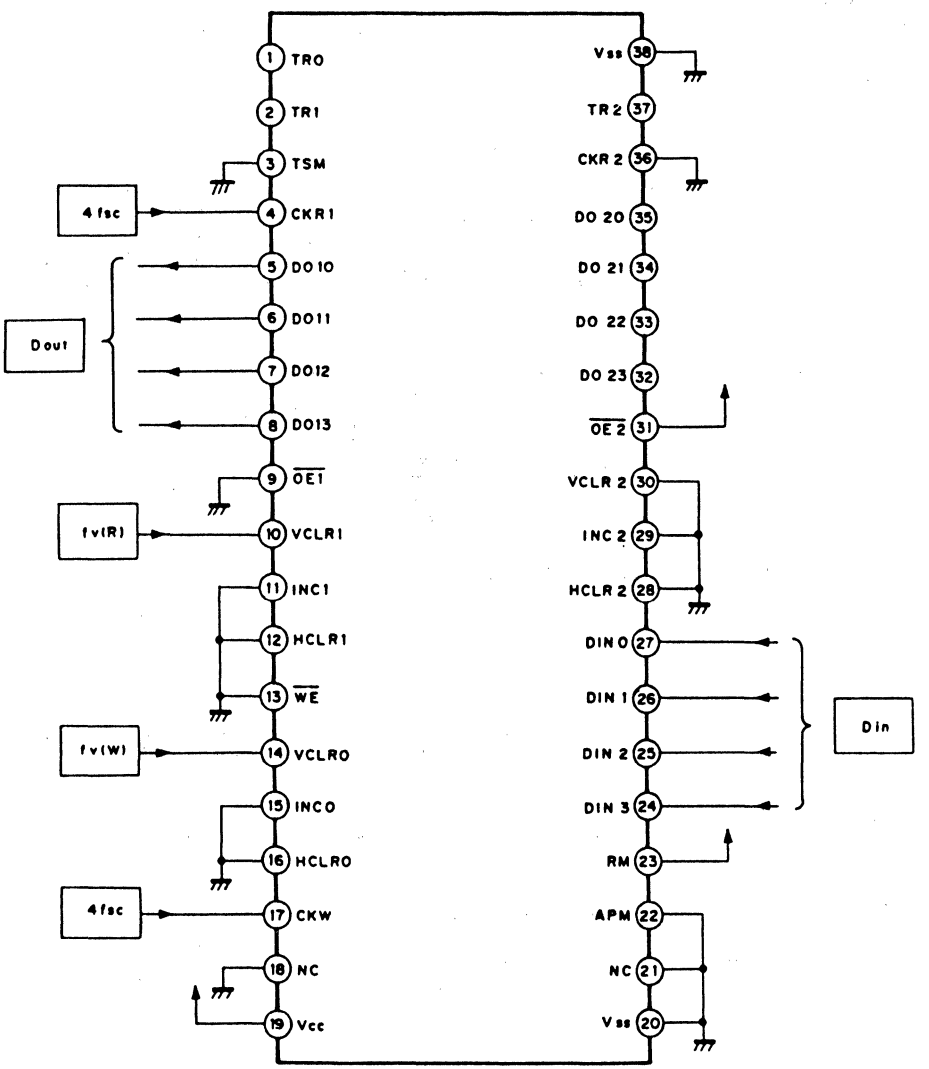
1) 1 field delay
2) 1 frame delay

(1) 1 field delay:

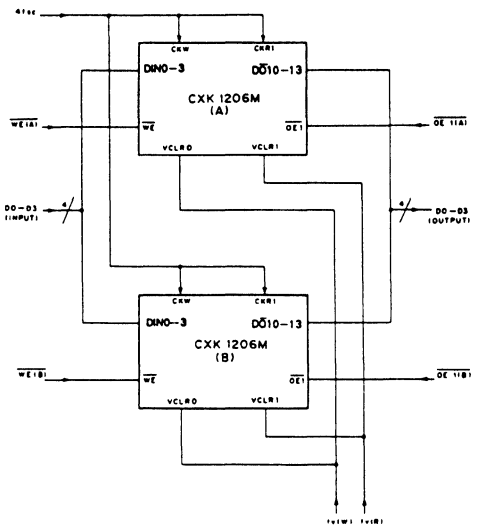


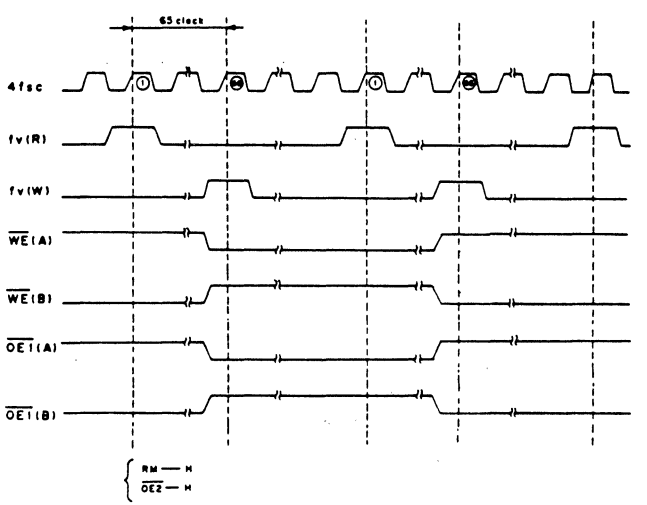


VRAM peripheral connection with 1 field delay



Application Circuit (2) 1 frame delay

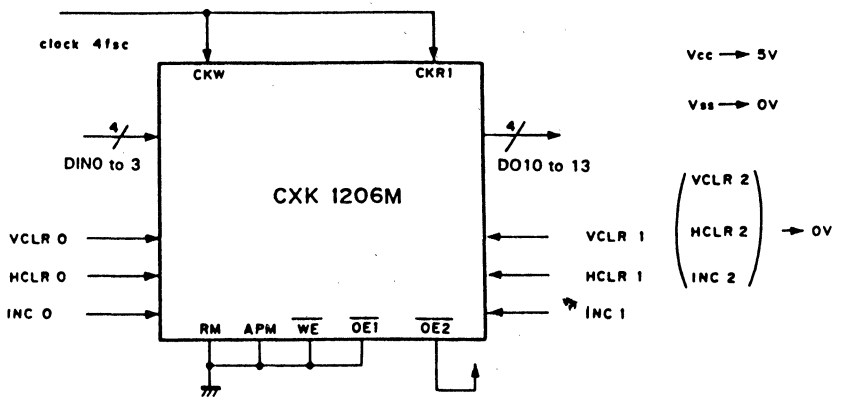


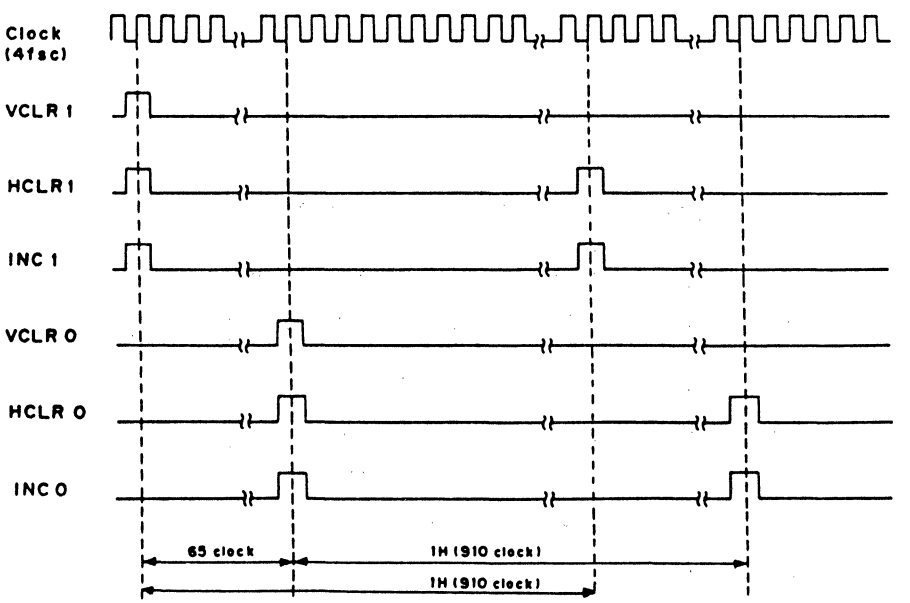


Note) 1. Do not turn off CKW for transfer control between DRAM and I/O port.
2. Do not turn off CKR1 for refreshing.
3. Switchover A chip and B chip with $\overline{WE}$ and $\overline{OE1}$.

Application Circuit (3)

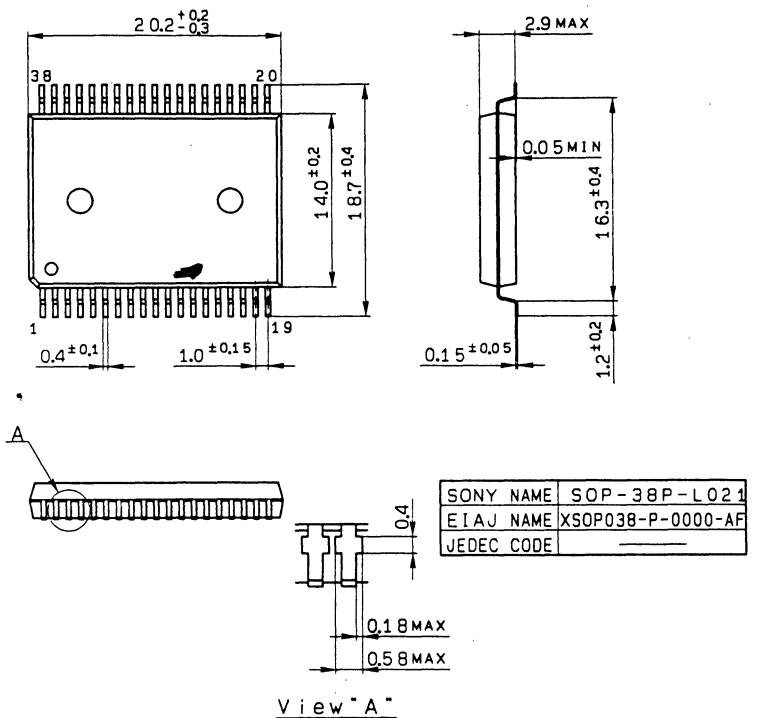
The following is a circuit achieving "1 field delay" using non-recursive mode.





Package Outline Unit : mm

38pin SOP (Plastic)



SONY CXA1387S

Aperture Compensation for TV

Description

The CXA1387S is a bipolar IC for aperture compensation designed to improve TV picture quality.

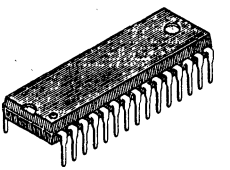
Features

- Aperture compensation using built-in delay line.
- Luminance signal coring function.
- VM (velocity modulation) signal output.
- Tracking delay for luminance signal output, VM output and Chroma signal output.
- Chroma signal image interval gain control (excluding burst signal interval).

Applications

Improvement of picture quality for TV, monitor, etc.

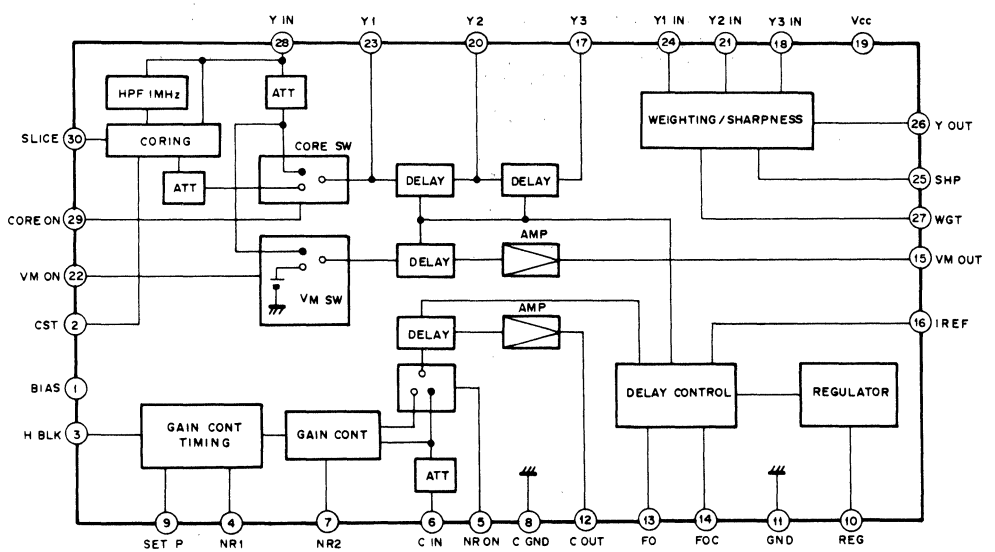
30pin SDIP (Plastic)



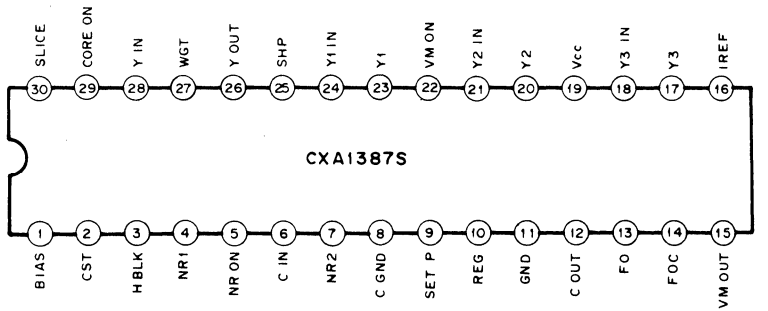
Structure

Bipolar silicon monolithic IC

Block Diagram



Pin Configuration



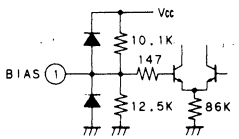
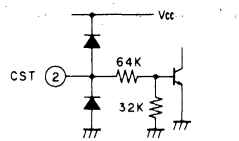
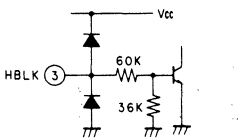
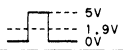
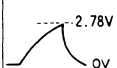
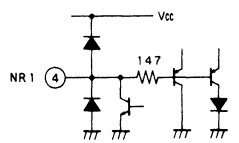
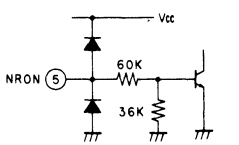
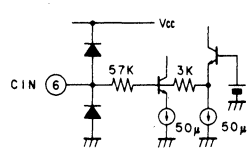
Absolute Maximum Ratings(Ta=25°C)

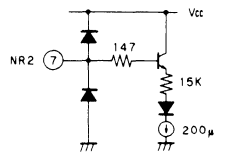
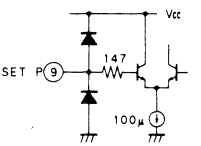
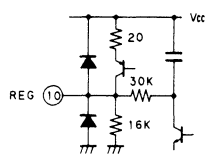
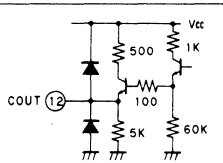
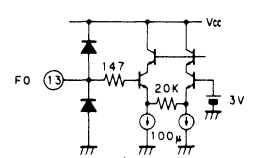
• Supply voltage	V_{CC}	12	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.35	W
• Voltage impressed to pin		−0.3 to V_{CC}+0.3	V

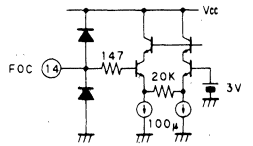
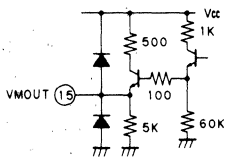
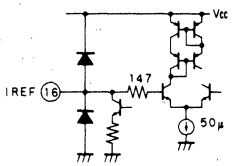
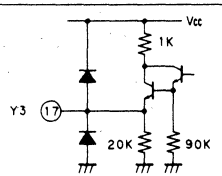
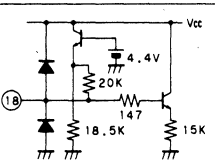
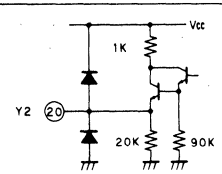
Operating Conditions

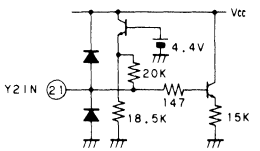
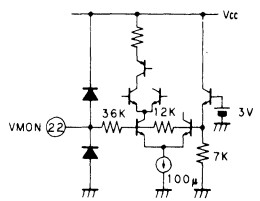
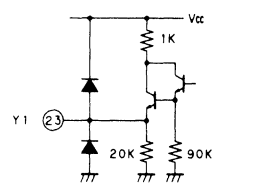
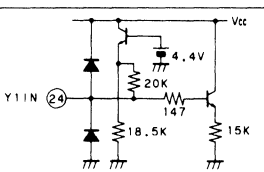
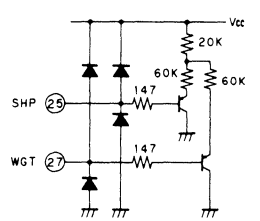
• Supply voltage	V_{CC}	8.5 to 9.5	V

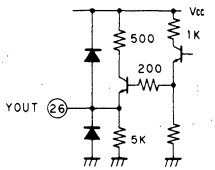
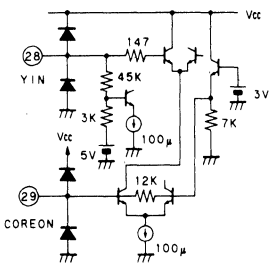
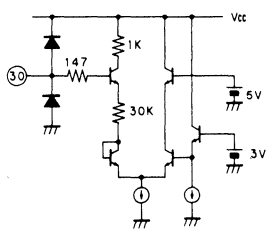
Pin Description

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
1	BIAS	5V		Bias pin used inside the IC. Connect capacitor between this and GND.
2	CST			Connect to GND.
3	HBLK			H Blanking pulse input pin. Provides the timing for gain control when CNR is ON through this HBLK pulse. 
4	NR1			Connect 5.6kΩ±1% resistance to V_{CC} and 4700pF±5% capacitor to GND.
5	NRON			Chroma signal gain control ON/OFF switchover pin. At L : Gain control OFF At H : Gain control ON
6	CIN	3V		Chroma signal input pin. Chroma signal input dynamic range within 500mVp-p. When low-frequency Y signal included, within 2Vp-p. (Max.)

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
7	NR2	2 to 7V*		Gain control voltage when CNR SW is ON. 7V (Typ.) at 0dB. 2V at less than −26dB.
8	CGND			GND pin.
9	SET P			Control pin that determines the timing of periods where gain control is applied and where it is not when chroma signal gain control is ON. When this pin's voltage is set to 2.87V, gain control is not applied for approx. The 10 μsec period from the rising edge of HBLK pulse (Pin 3 input). The input of the burst signal period in the period where gain control is not applied enables color control.
10	REG	8V		Built-in constant voltage supply output pin. Connect capacitor between this and GND.
11	GND			GND pin.
12	COUT	4.4V		Chroma signal output pin.
13	FO	2 to 4V*		Delay control pin of built-in delay line. Controls Y, VM, and C signal at the same time. Raising control voltage reduces delay.

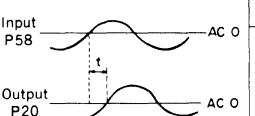
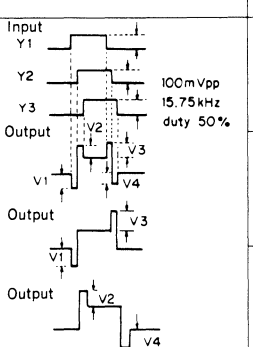
Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
14	FOC	2 to 4V*		Delay control pin of built-in delay line. Controls only C signal independently. Delay of Y and VM signal does not change. Control characteristics is the same as FO.
15	YMOUT	4.6V		Y signal output pin for VM control.
16	IREF	6.7V		External resistance pin for internal reference current. Connect 6.8kΩ±1% resistance between this pin and REG (Pin 10). Also, connect to GND with capacitor. See Application Circuit (P.18).
17	Y3	3.65V		Output pin for Y signal passed through 2 delay lines. Attenuated by −24.5dB compared with input.
18	Y3IN	3.7V		Input pin of signal for aperture control. Pin 17 signal (Y3) is coupled through a capacitor and input.
19	V_{CC}	9.0V*		Supply pin.
20	Y2	3.65V		Output pin of Y signal passed through one delay line. Attenuated by −24.5dB compared with input.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
21	Y2IN	3.7V		Input pin of signal for aperture control. Pin 20 signal (Y2) is coupled through a capacitor and input.
22	YMON	2.3V		VM output switchover control pin. At L : VM signal (Y signal) output. At H : No output (DC).
23	Y1	3.65V		Attenuates input Y signal by −24.5dB before output.
24	Y1IN	3.7V		Input pin of signal for aperture control. Pin 23 signal (Y1) is coupled through capacitor and input.
25	SHP	3 to 5V*		Controls preshoot and overshoot magnitude of Y output signal. At 3V : Sharpness flat ⟆ At 5V : Sharpness maximum.
27	WGT	0 to 6V*		Controls the ratio of preshoot and overshoot of Y output signal. At 0V : Only preshoot At 3V : Preshoot : Overshoot=1 : 1 At 5V : Only overshoot.

Pin No.	Symbol	Pin Voltage	Equivalent circuit	Description
26	YOUT	5.0V		Y signal output pin.
28	YIN	5V		Y signal input pin. Input dynamic range at 2Vp-p (Max.)
29	COREON	2.3V		Y signal coring ON/OFF switchover pin. At L : Coring OFF At H : Coring ON
30	SLICE	1 to 6.5V*		Core level control pin when coring is ON. When voltage is set to 6.5V, controls −3dB (Typ.) at 4.5MHz.

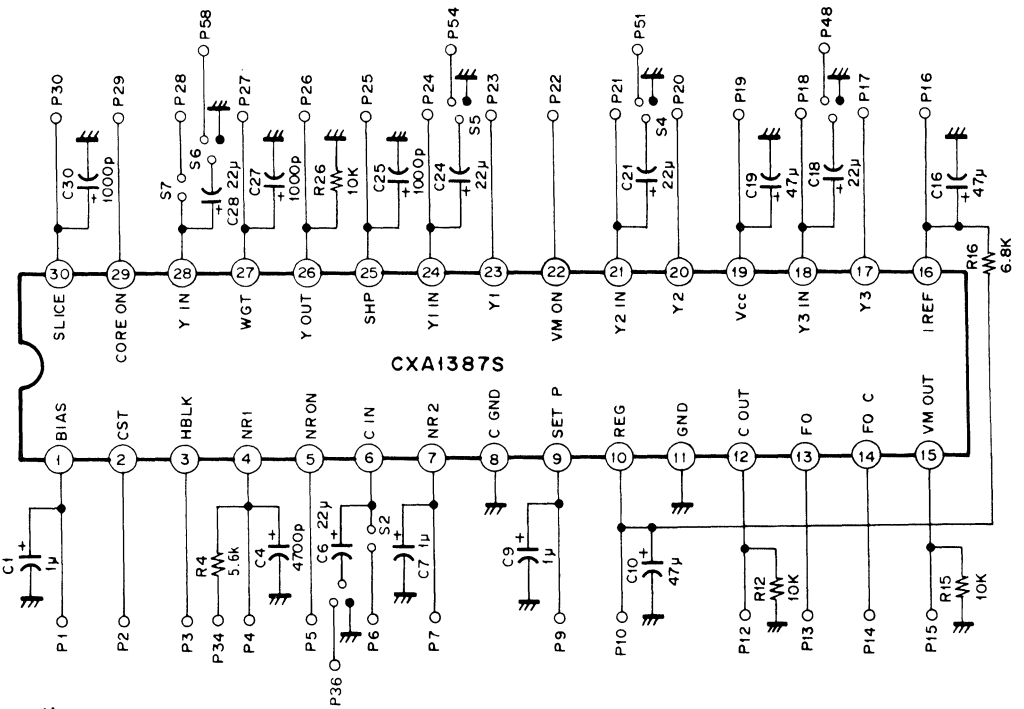
* : External applied voltage

Electrical Characteristics (T_a=25°C, V_{CC}=9.0V, See Electrical Characteristics Test Circuit, P.11)

No.	Item	Symbol	Bias condition	Switch set ON	Input point and input signal	Test point	Test contents Standard value	Min.	Typ.	Max.	Unit
1	Consumption current	I_{CC}	P13, P14, P25, P27 } 3V P19……9V			P19		20	30	40	mA
2	Constant voltage output	V_{REG1}				P10		7.70	8.00	8.30	V
3	Constat voltage output supply voltage characteristics	dV					Output voltage fluctuation at REG (Pin 10) when 9.5V or 8.5V is applied to V_{CC} (Pin 19). Ref. voltage at 9.0V)	−10	0	10	mV
4	Chroma level	CG		S1	3.58MHz, 500mVp-p } Sine wave at Pin 36.	P12	Gain tested.	−3.0	−1.5	0.0	dB
5	Y output level	YG	P13,P14, P25, P27 } 3V P19……9V P22……GND P29……GND	S6	1MHz, 2.0Vp-p } Sine wave at Pin 58.	P26	Signal output from Y2 (Pin 20) is input to Y2 IN and the gain from Y out (Pin 26) output is tested.	−2.0	−0.5	1.0	dB
6	Y signal frequency characteristics.	Yf			8MHz, 2.0Vp-p } Sine wave at Pin 58.		Gain difference between f=1MHz and F=8MHz. (Sharpness center)	−6.0	−3.0	0.0	dB
7	VM output level	VMG			1MHz, 2.0Vp-p } Sine wave at Pin 58.	P15	Gain tested.	−2.0	−1.0	0.0	dB
8	Y coring	COR	P13,P14, P25, P27 } 3V P22……3V P29……3V P19……9V		4.5MHz, 400mVp-p } Sine wave at Pin 58.	P23	Output gain difference when the voltage at Pin 30 is varied from 1V to 6.5V.	−10.0	−6.0	−2.0	dB
9	Maximum delay time	DL_{max}	P13……2V P14,P25, P27 } 3V P22……GND P29……GND P19……9V		1MH, 2Vp-p } Sine wave at Pin 58.	P20	Output delay time in relation to the input. Difference in delay time 	220	270		ns
10	Minimum delay time	DL_{min}	P13……4V P14,P25, P27 } 3V P22……GND P29……GND P19……9V						120	160	ns
11	Aperture level	AP1	P13, P14, P27 } 3V P25……5V P22……GND P29……GND P19……9V	S3, S4, S5	P54 : Y1 P51 : Y2 P48 : Y3	P26		430	530	630	mV
12	Maximum preshoot	PR_{max}	P13, P14…3V P27……0V P25……5V P22……GND P29……GND P19……9V					900	1000	1100	mV
13	Maximum overshoot	OV_{max}	P13, P14…3V P27……6V P25……5V P22……GND P29……GND P19……9V					950	1100	1200	mV

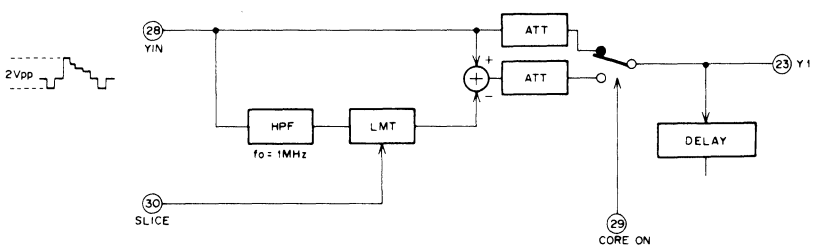
No.	Item	Symbol	Bias condition	Switch set ON	Input point and input signal	Test point	Test contents Standard value	Min.	Typ.	Max.	Unit
14	VM switch threshold level	V_{VM}					Threshold level when VM is ON/OFF. At L : VM ON At H : VM OFF	2.0	2.2	2.4	V
15	Coring switch threshold level	V_{COR}					Threshold level when coring is ON/OFF. AT L : Coring OFF AT H : Coring ON	2.0	2.2	2.4	V
16	CNR switch threshold level	V_{CNR}					Threshold level when CNR is ON/OFF. At L : CNR OFF At H : CNR ON	1.5	2.0	2.5	V
17	CNR ON time	T_{CNR}	P13, P14, P25, P27 } 3V P22,P29···GND P19, P34···9V P9·····2.78V		P3 5μ 3V 0V f=15.75kHz	P4	Input signal 5μsec P3 3V 0V f=15.75kHz Output waveforms P4 t • t time is tested. ※ Time here is when CNR is ON and when gain control of the chroma signal is not applied.	9.7	10.0	10.3	μs
18	CNR offset	CNOS				P12	Input signal 5μsec P3 H.BLK 3V 0V f=15.75kHz Output waveforms P12 C.OUT V • Test electric potential gradient V. ※ Offset voltage when gain control is applied in the chroma signal and when it is not with CNR ON.	0	150	600	mV
19	Chroma gain control	CNR	P13, P14, P25, P27 } 3V P19,P34···9V P5·····3V P7·····2V	S1	P36 3.58MHz 500mVp-p		Gain between input and output is tested.			−26	dB

Electrical Characteristics Test Circuit

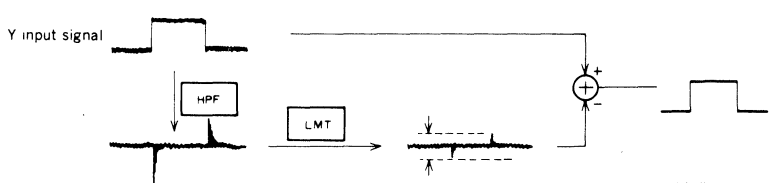


Operation

1. Y coring



As shown in the above diagram, Y signal is passed through HPF, amplitude limitation is performed and the result substracted from the original signal to execute Y signal coring.



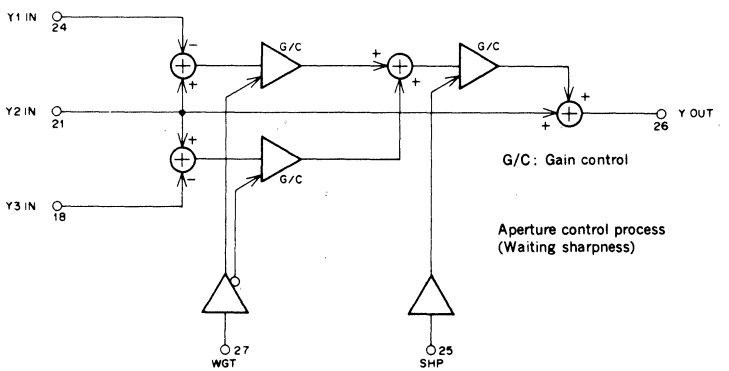
Cut off frequency of the HPF (high pass filter) used for coring stands at approx. 1MHz (Typ.). The amplitude limiting range of the limiter stands within 0 to 400mV (Typ.). Control is performed through Pin 30 (SLICE).

- Raising the voltage of Pin 30 (SLICE) raises the limiter level and coring effect is more amply expressed.
- Coring is controlled through Pin 29. At L level, coring is OFF and at H, it is ON. At this threshold level, this pin is biased.

2. Aperture control

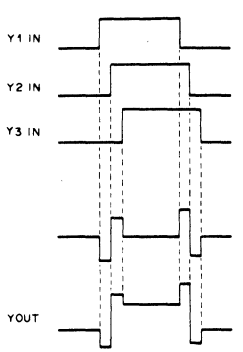
Y signal is attenuated by approx. −24.5dB passing through the coring (process) circuit to be output from Pin 23 as Y1 output. Y1 output passes through one built-in delay line to be output as Y2 output from Pin 20. Then Y2 output passes through still another delay line to be output as Y3 output from Pin 17. (See Block Diagram, P.4)

These three outputs (Y1, Y2, and Y3) are input to Pins 24 (Y1IN), 21 (Y2IN), and Pin 18 (Y3IN) through capacity coupling to start aperture control process.



Aperture control process controls preshoot/overshoot ratio through WGT pin (Pin 27) and sharpness level through SHP pin (Pin 25) respectively. This control process is indicated on the above diagram.

The basic principle of delay line aperture control is shown on the below diagram.



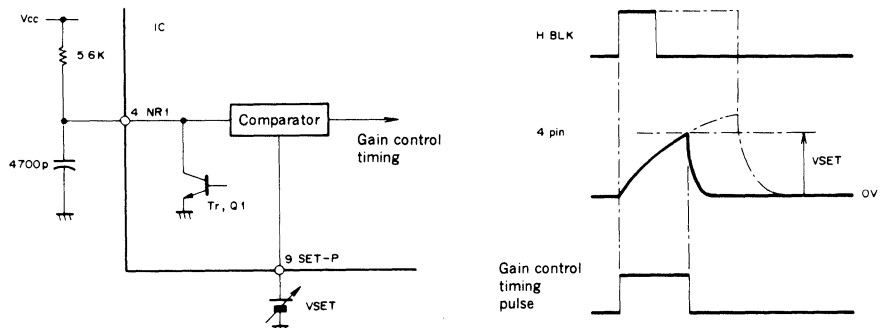
3. Chroma signal gain control

When CNR is ON, chroma signal gain control in executed at a timing other than that of burst signal. As a result, chroma signal is restrained and pales. In signals with numerous noise components, this gain control pales color to reduce conspicuous color noise and evenly distribute CNR (chroma noise reduction) effects.

(1) Timing

When CNR is ON, gain control is executed in the image section only (With the exception of burst section). The timing is, therefore, formed by using H. BLK pulse input from Pin 3.

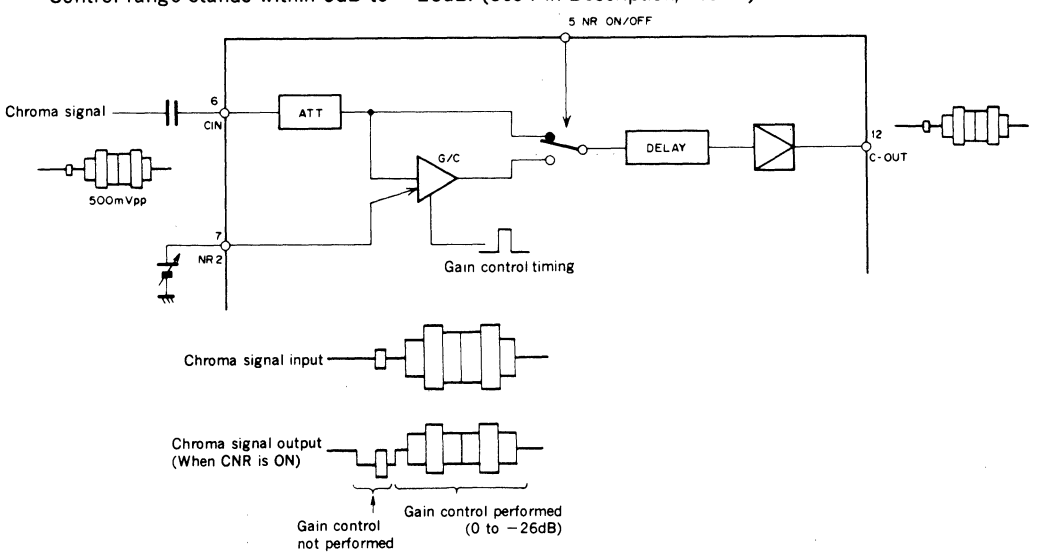
Simultaneously with the input of H. BLK pulse Tr. Q1 turns OFF and Pin 4 (NR1) voltage rises. Tr. Q1 turns ON again when H. BLK pulse turns to L level and Pin 4 voltage reaches the voltage set at Pin 9 (SET-P). Gain control timing pulse is emitted during the period when H. BLK pulse is input (When it turns to H level) until Pin 4 voltage reaches the voltage set at Pin 9. During this period gain control is not performed.



(2) Gain control

When CNR is ON, gain control is performed according to the timing set in (1). The amount of gain control is set at Pin 7 (NR2).

Control range stands within 0dB to −26dB. (See Pin Description, P.5 ~)

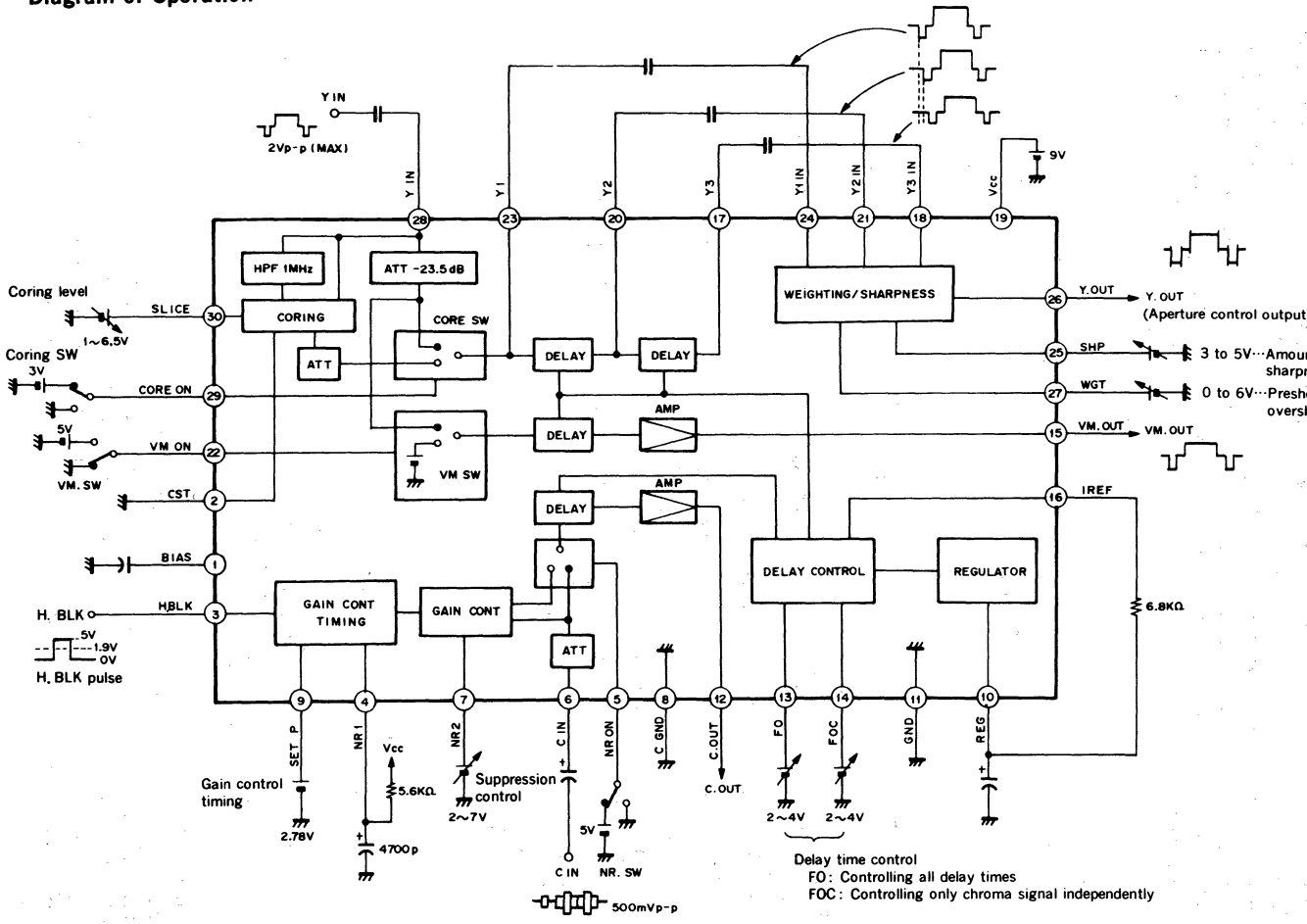


4. VM output

CXA1387S features a VM (velocity modulation) signal output. (Pin 15)

Basically, it is similar to Y input. Since Y output is contour accentuated by means of the built-in delay line. VM output has the same delay time as Y output. Changing the delay time of Y output delay (that is, changing Y output peak frequency). means simultaneously changing VM output delay time. This goes the same with C output, except that C output, can be canged independently.

Diagram of Operation

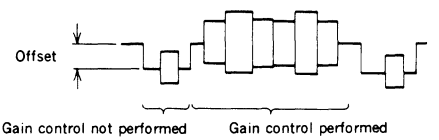


Notes on Operation

Consider the following points during usage.

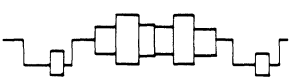
1. Oscillation
   Output stage (YOUT, VMOUT, and COUT) in this IC is an emitter follower. When loads concerned with capacity are involved oscillation may occur. Use a buffer. Connect a by-pass capacitor to each of pins, FO (Pin 13) and FOC (Pin 14), that control the delay time of the built-in delay line.

2. Offset of chroma signal when CNR is ON
   There is an offset between where image signals are gain controlled and burst signal not gain controlled. (See Fig. below.)

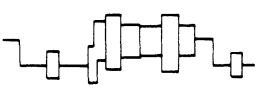


(This offset is specified in Item, No.18, Electrical Characteristics.)

When the changing offset applies to the image chroma signal, the TV screen is adversely affected. Adjust Pin 9 (SET. P) voltage, controlling Pin 9 voltage so that it does not apply to the image.



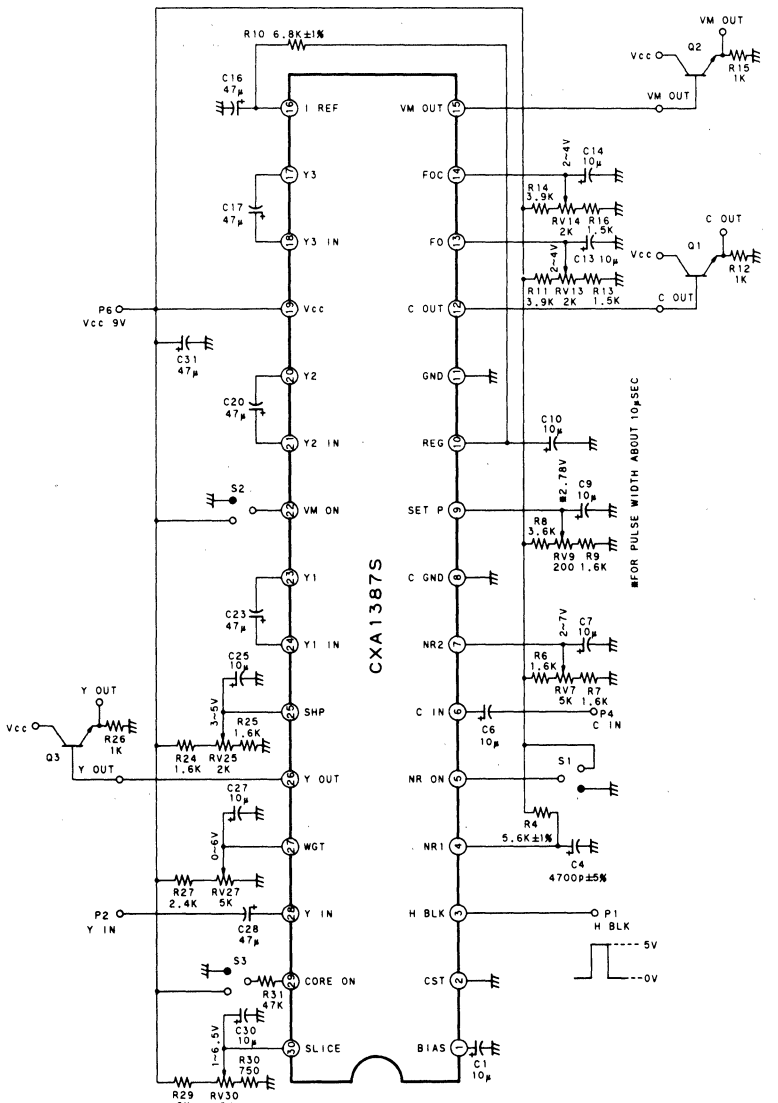
〈Good example〉



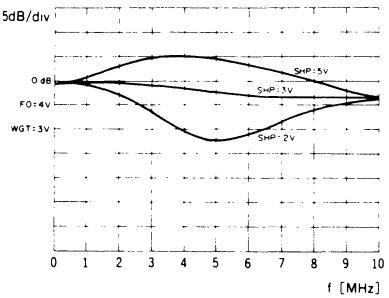
〈Bad example〉

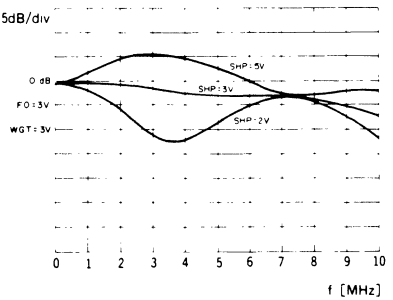
3. Input signal dynamic range
   i) The max. input dynamic range of Y signal stands at 2Vp-p. This is the value from Sync to White peak. When the input signal exceeds 2Vp-p, it may be clipped and distorted.
   ii) The max. input dynamic range in the chroma signal stands at 500mVp-p (Max.). This is when the chroma signal is at burst signal. When a low frequency Y signal is mixed with the chroma input signal (CIN), this input dynamic range may reach a max. of 2Vp-p.

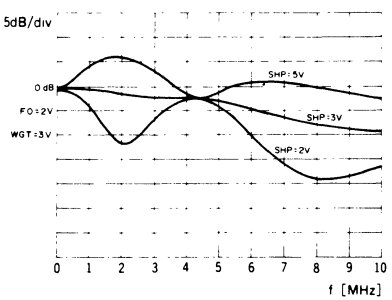
Application Circuit



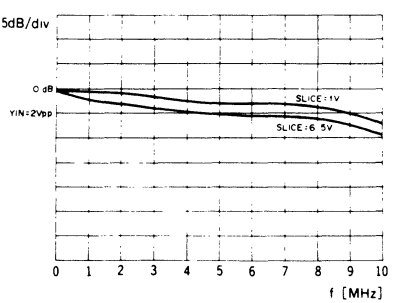
1. Sharpness characteristics

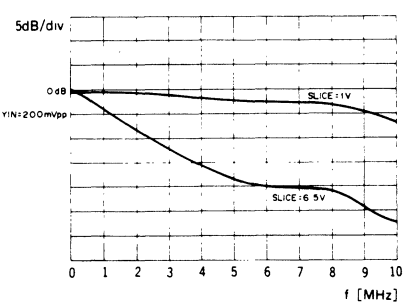






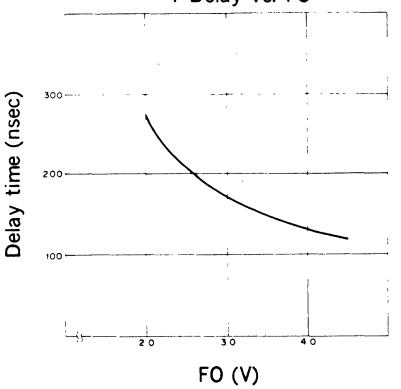
2. Coring characteristics



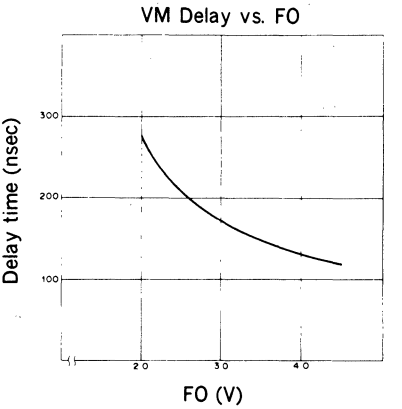


3. Delay characteristics

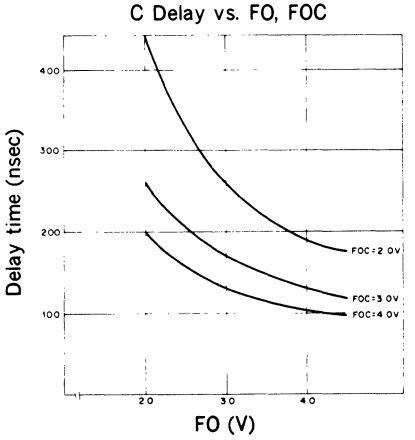
Y Delay vs. FO



VM Delay vs. FO

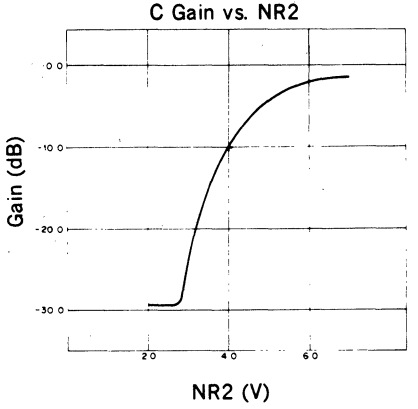


C Delay vs. FO, FOC



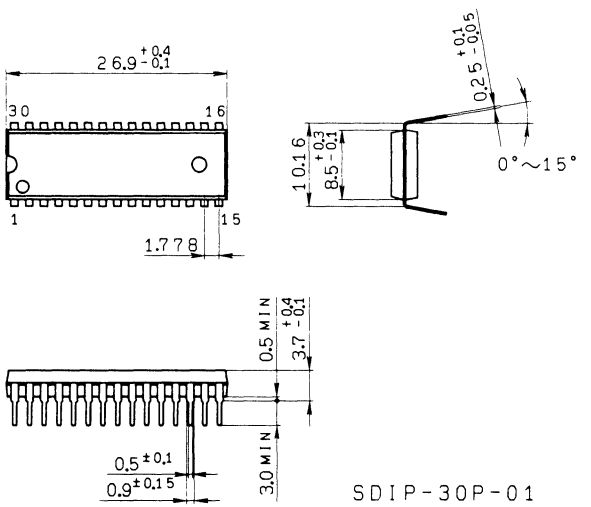
4. Chroma signal gain control characteristics

C Gain vs. NR2



Package Outline Unit: mm

30pin SDIP (Plastic) 400mil 1.8g



SDIP-30P-01

SONY

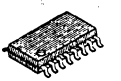
CXA1451M

Switch and Driver for VCR

Description

The CXA1451M is a wide-band switch and driver IC for application to video signals. It has 75Ω drivers for two channels.

16 pin SOP (Plastic)



Features

- Provided with 75Ω drivers for two channels with the same voltage gain.
- Capable of switching video signals at frequencies over a wide-band (up to 25MHz).
- 75Ω drivers with power save function.
- Low current consumption (16mA, Typ.)
- Frequency response: Relative to 500kHz;
  Within ± 0.1dB (Typ.) at 5MHz
  Within ± 0.3dB (Typ.) at 10MHz
  Within ± 1dB (Typ.) at 25MHz

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	$V_{CC}-V_{EE}$	14	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	650	mW

Operating Conditions

Supply voltage	V_{CC}	4.0 to 6.0	V
	V_{EE}	−4.0 to −6.0	V

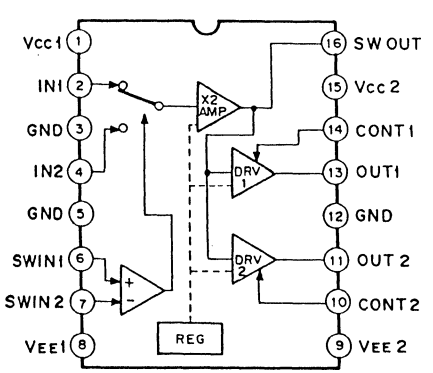
Structure

Bipolar silicon monolithic IC

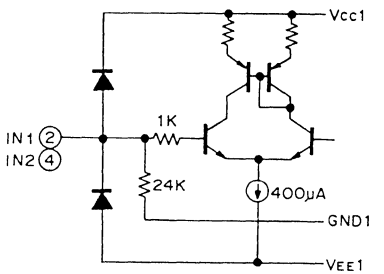
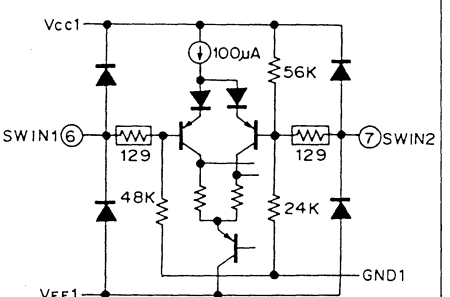
Applications

- Switching video signals
- 75Ω driver

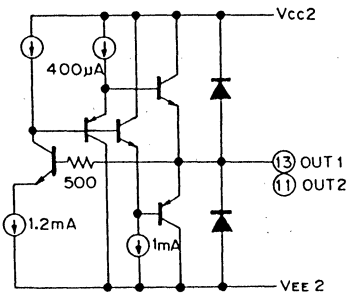
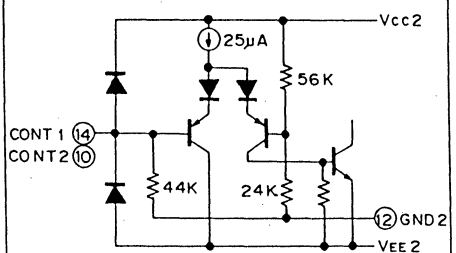
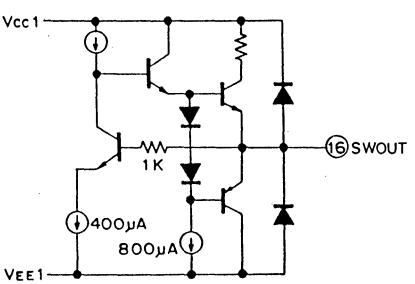
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage (V)	Equivalent circuit	Description
1	Vcc1	+5 *		Positive power supply pin for switch
2 4	IN1 IN2	0 0		Channel 1 input pin Channel 2 input pin Input resistance is 24kΩ for each channel.
3 5	GND1	0 *		GND pin for switch
6 7	SWIN1 SWIN2	0 1.5		IN1/IN2 switching control pin. When this pin is open or low (<1.0V), the IN1 signal is output. When it is high (>2.0V), the IN2 signal is output. The SWIN2 pin is internally biased at 1.5V.
8	VEE1	−5 *		Negative power supply pin for switch
9	VEE2	−5 *		Negative power supply pin for driver

* External input pin voltage

Pin No.	Symbol	Pin voltage (V)	Equivalent circuit	Description
13	OUT1	0		DRV.1 output pin capable of driving 75Ω load directly.
11	OUT2	0		DRV.2 output pin capable of driving 75Ω load directly.
12	GND2	0*		GND pin for driver
14	CONT1	0		Power save control pins for drivers, DRV.1 and DRV.2. When Pin 14 and 10 are open or low (<1.0V), the corresponding driver operates. When it is high (>2.0V), the corresponding driver does not operate, resulting in power saving.
10	CONT2	0		
15	Vcc2	+5*		Positive power supply pin for driver
16	SWOUT	0		Outputs the IN1 or IN2 signal selected by the switch with a 6dB amplification.

* External input pin voltage

Electrical Characteristics

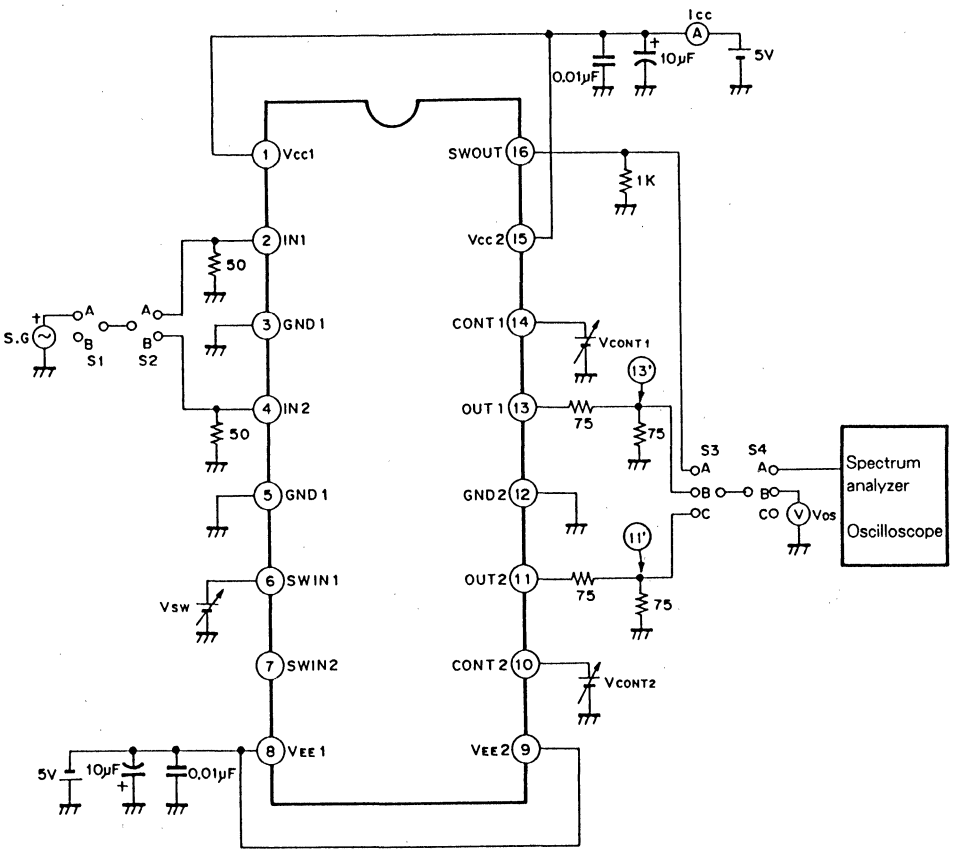
(Ta=25℃, V_{CC}=+5V, V_{EE}=–5V. See Electrical Characteristics Test Circuit.)

Test item		Symbol	Test conditions	Input pin	Test pin	Switches S1	S2	S3 *1	S4	Min.	Typ.	Max.	Unit
Voltage gain		G_{V1}	With an input voltage of 1Vp-p, measure the voltage gain at an input frequency of 500kHz.	2	13	A	A	B (C)	A	5.5	6.0	6.5	dB
		G_{V2}		4 *2	11	A	B	B (C)	A				
Frequency response characteristics		f_{O1}	With an input voltage of 1Vp-p, measure the gain difference between input frequencies of 500kHz and 25MHz.	2	13	A	A	B (C)	A	–1	0	1	dB
		f_{O2}		4	11	A	B	B (C)	A				
Output dynamic range	+side	V_{D1}	Measure the output voltage with an input voltage of 3V DC. 75Ω termination.	2	13'	A	A	B (C)	A	+1.4			V
				4	11'	A	B	B (C)	A				
	–side	V_{D2}	Measure the output voltage with an input voltage of –3V DC. 75Ω termination.	2	13'	A	A	B (C)	A			–1.4	V
				4	11'	A	B	B (C)	A				
Output DC offset		V_{OS1}	75Ω termination with no input signal.		13'	B	—	B (C)	B	–60	0	+60	mV
		V_{OS2}			11'	B	—	B (C)	B				
Control voltage	SW	V_{SW}	Measure the Vsw voltage value at the output signal switches. 75Ω termination.	2 4	6	A	—	A	A	1.0	1.5	2.0	V
	DRV1	V_{CONT1}	Measure the V_{CONT} voltage value at the output signal switches. 75Ω termination.	2	14	A	—	B (C)	A	1.0	1.5	2.0	V
	DRV2	V_{CONT2}		4	10	A	—	B (C)	A				
Current consumption		Icc	75Ω termination with no input signal.		15	B	—		C	8.5	16.2	23.5	mA

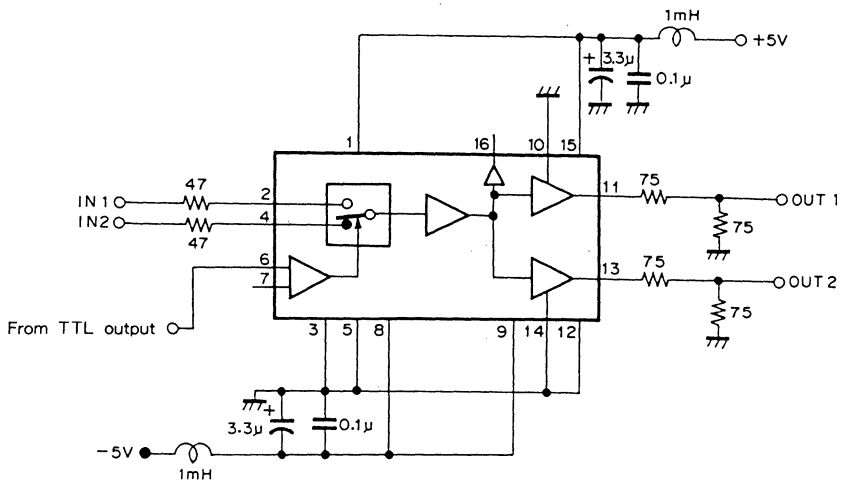
*1. B for DRV.1; C for DRV.2

*2. When input pin 4 is used, Vsw=5V.

Electrical Characteristics Test Circuit



Application Circuit



When the TTL output is low, the IN1 signal is output.
When it is high, the IN2 signal is output.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

The IN1 and IN2 signals input to Pins 2 and 4 are switched by the control signal input to Pin 6.

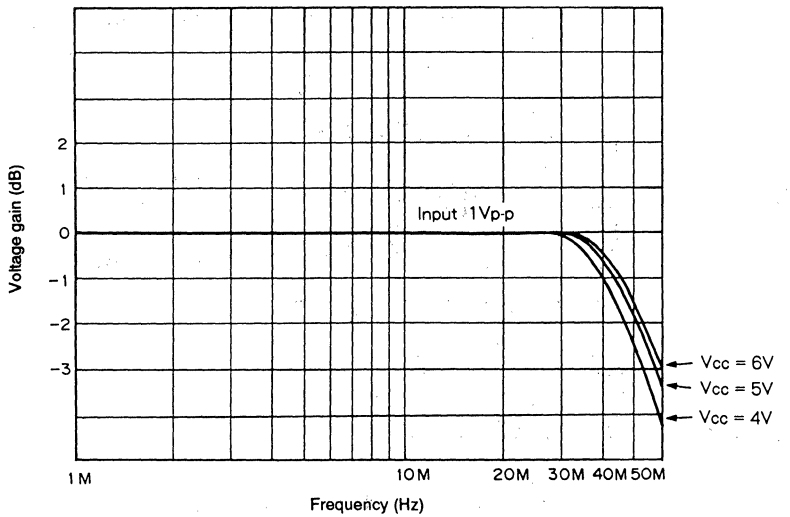
When Pin 6 is open or low (<1.0V), the Pin 2 input signal is selected. When it is high (>2.0V), the Pin 4 input signal is selected. The selected input signal is output from driver output Pins 11 and 13 as well as SW output Pin 16.

Drivers 1 and 2 (DRV.1 and DRV.2) have power save control pins 14 and 10, respectively. Each driver operates only when its power save control pin is open or low (<1.0V), so that power is saved when its power save control pin is high (>2.0V).

This power saving corresponds to a reduction of about 5mA in current consumption per driver.

Example of Representative Characteristics

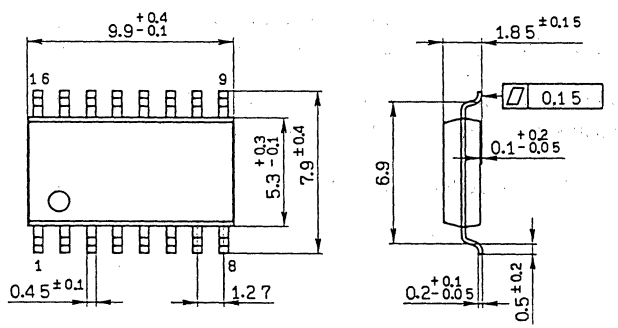
Frequency – Voltage gain characteristics

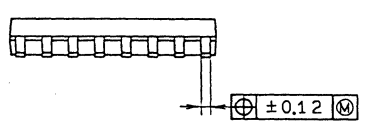


Package Outline

Unit : mm

16pin SOP (Plastic) 300mil 0.2g





SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

Audio Processing

Audio Processing

Part Number	Function	Voltage	Package	Page
CXD1160AP/AQ	Digital Audio Signal Processor	5V	28P DIP/ 80P QFP	299
CXD1244S	100dB Attenuation Digital Filter	5V	40P SDIP	351
CXD2552Q	Pulse D/A Converter	5V	44P QFP	364
CXD2555Q	Audio Delta Sigma Type A/D+D/A+D/F	5V	48P QFP	372

SONY®

CXD1160AP/AQ

Digital Audio signal processing LSI

Description

CXD1160AP/AQ is a digital audio signal processing LSI.

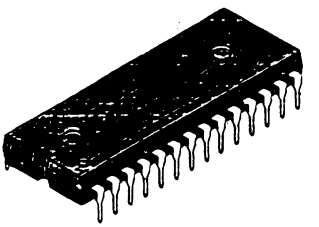
Features

This LSI features built-in instruction RAM, coefficient RAM, multiplier, barrel shifter and others. With regards to peripheral interface usage, serial I/O, delay I/O (stereo delay for a max. of 1024 samples possible) and microcomputer interface provide excellent system cost performance.

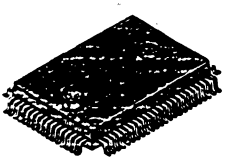
Structure

Silicon gate CMOS

CXD1160AP 28pin DIP (Plastic)



CXD1160AQ 80pin QFP (Plastic)



Functions

(1) Hardware

• Master clock	30.72MHz max. (during MCK1 input) 15.36MHz max. (during MCK2 input)
• Machine cycle	130ns min. (160 cycle max./fs=48KHz)
• Instruction	1 to 3 cycle (single precision/ double precision)
• Built-in RAM	Instruction RAM 24bit×64w coefficient RAM 16bit×64w data RAM 16bit×64w
• Multiplying part	16bit×16bit built-in multiplier data coefficient (1) 16×16 (1 cycle) (2) 16×32 (2 cycle) (3) 32×16 (2 cycle) (4) 32×32 (3 cycle)
• Adder-Subtractor	34bit±34bit Acc 34bit with 2bit shifter
• Register	For adder-subtractor R (H/L) Serial I/O I 1 (H/L) I 2 (H/L) O 1 (H /L) O 2 (H/L) Delay I/O D1 (H/L) D 0 (H/L) Every register 32bit H/L can be used independently
• Barrel shifter	Positive floating point Type conversion Arithmetic left shift Arithmetic right shift 32bit IN 16bit OUT shift max. 15bit
• Address stack	double
• Loop counter	4bit

(2) Interface

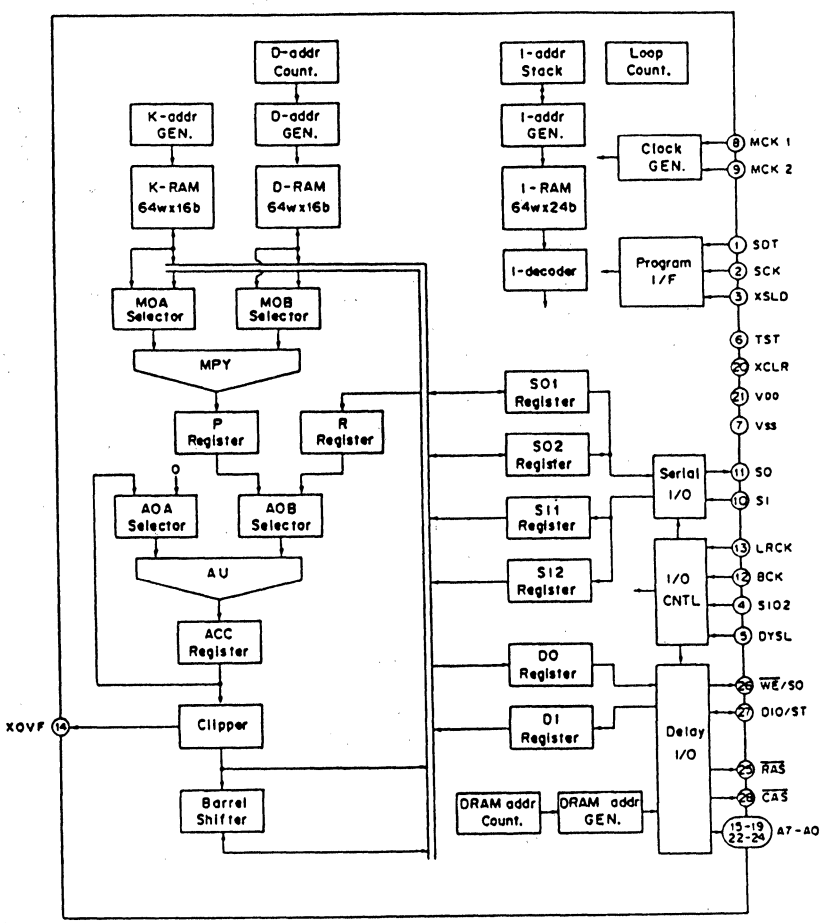
• Serial I/O	Time-shared 2ch input 2ch output Every channel data format 32bit, (16bit+16bit), 24bit, 16bit, Every channel bit clock format 32ck, 24ck MSB first
• Delay I/O	Every channel variable delay (1 to 1024 samples) Usage also possible as serial I/O
• Microcomputer interface	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings		Unit
		Min.	Max.	
Supply voltage	V_{DD}	Note 1 Vss −0.5	7.0	V
Input voltage	V_I	Note 1 Vss −0.5	V_{DD} +0.5	V
Output voltage	V_O	Note 1 Vss −0.5	V_{DD} +0.5	V
Operational temperature	Topr	−20	75	°C
Storage temperature	Tstg	−55	150	°C

Note 1) Vss=0V

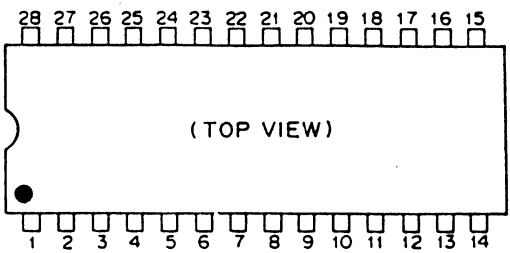
Block Diagram



Note) Pin numbers are those of CXD1160AP

Pin Configuration and Description (CXD1160AP)

Pin Configuration



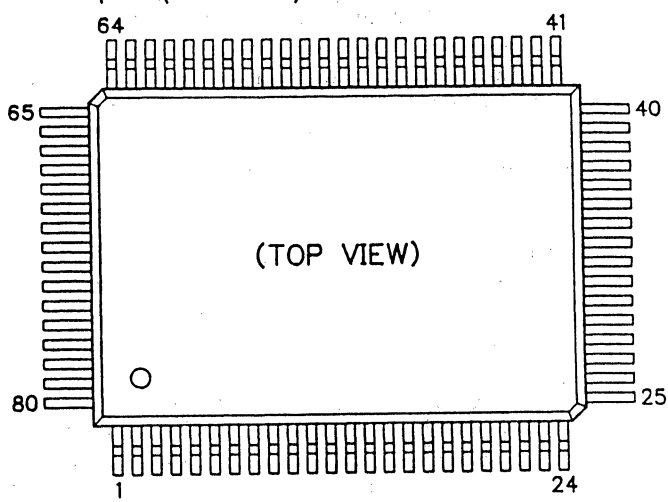
Pin Description

No.	Symbol	I/O	Description
1	SDT	I	Serial data input pin that receives commands, coefficient and I/O control transfer from the microcomputer. In each transfer modes, single 40-bit block is transferred at a time.
2	SCK	I	SDT serial clock input pin. Takes in data with the rising edge.
3	XSLD	I	Latch input pin that serves to latch inside the IC 1 block of serial data 40bit in length active at 'L'.
4	SIO2	I	Input pin. Sets the number of BCK clocks used for data transfer per channel (ch1 and 2) in one sampling section. When fixed to GND it turns to 32bit clock mode. When fixed to +5V it turns to 24bit clock mode.
5	DYSL	I	Delay I/O mode select input pin. When GND is fixed it turns to serial mode. Operates similarly as serial I/O. Fixed at +5V it turns to delay mode. Connected to an external DRAM (64kbit) composes a delay line for 2 channels.
6	TST	I	Test pin. Normally fixied to GND.
7	Vss	-	GND pin.
8	MCK1	I	Master clock input 1. Master clock ACK inside the IC is half this frequency. To input the master clock through MCK1 fix MCK 2 to +5V.
9	MCK2	I	Master clock input 2. Master clock ACK inside the IC has the same frequency. To input the master clock through MCK2 fix MCK1 to +5V or to GND.
10	SI	I	Input pin for 1 sampling 2ch serial data. Data format complement on two. At last LSB, various modes 32/24/16bit available.
11	SO	O	1 sampling 2 channel serial data output pin. Data format complement on two. At last LSB, various modes 32/24/16bit available.
12	BCK	I	Serial bit clock input pin of serial input data SI and serial output data SO. With the rising edge of this BCK serial input data is taken in and with the falling edge serial output data is sent out.
13	LRCK	I	Serial I/O sampling frequency clock input pin. Transfers ch1 data when level at 'H' and ch 2 data when level at 'L'.
14	XOVF	O	Adder-subtracter overflow detection output. Outputs 'L' during overflow detection.
15	A6	O	External DRAM address output A6
16	A3	O	External DRAM address output A3
17	A4	O	External DRAM address output A4
18	A5	O	External DRAM address output A5

No.	Symbol	I/O	Description
19	A7	O	External DRAM address output A7
20	XCLR	I	Test pin. Normally fix to +5V
21	V_{DD}	-	+5V Supply pin
22	A1	O	External DRAM address output A1
23	A2	O	External DRAM address output A2
24	A0	O	External DRAM address output A0
25	XRAS	O	External DRAM low address strobe output pin
26	XWSO	O	When DYSL is at 'L', turns to serial data output pin, and operates according to the various serial I/O modes. When DYSL is at 'H' turns into the write enable output pin of the external DRAM.
27	DIO	I/O	Turns to serial data input pin when DYSL is at 'L' and takes in according to the various serial I/O modes. Turns into external DRAM data I/O pin when DYSL is at 'H' to assume a common bus with DRAM data input D_{IN} and data output D_{OUT}.
28	XCAS	O	External DRAM column address strobe output pin

Pin Configuration and Pin Description (CXD1160AQ)

Pin Configuration



Pin Description

No.	Symbol	I/O	Description
1-3	N.C		
4	TST	I	Test pin. Normally fixed to GND.
5-8	N.C		
9	Vss	-	GND pin
10-15	N.C		
16	MCK1	I	Master clock input 1. Master clock ACK inside the IC is half this frequency. To input the master clock through MCK 1 fix MCK2 to +5V.

No.	Symbol	I/O	Description
17-20	N.C		
21	MCK2	I	Master clock input 2. Master clock ACK inside the IC has the same frequency. To input the master clock through MCK2 fix MCK1 to +5V or to GND.
22-26	N.C		
27	SI	I	Input pin for 1 sampling 2ch serial data. Data format complement on two. At last LSB various modes 32/24/16 bit available.
28	SO	O	1 sampling 2 channel serial data output pin. Data format complement on two. At last LSB, various modes 32/24/16bit available.
29	BCK	I	Serial bit clock input pin of serial input data SI and serial output data SO. With the rising edge of this BCK serial input data is taken in and with the falling edge serial output data is sent out.
30	LRCK	I	Serial I/O sampling frequency clock input pin. Transfers ch1 data when level at 'H' and ch 2 data when level at 'L'.
31	XOVF	O	Adder-subtracter overflow detection output. Outputs 'L' during overflow detection.
32-33	N.C		
34	A6	O	External DRAM address output A6
35	A3	O	External DRAM address output A3
36	A4	O	External DRAM address output A4
37	A5	O	External DRAM address output A5
38	A7	O	External DRAM address output A7
39-43	N.C		
44	XCLR	I	Test pin. Normally fixed to 5V.
45-48	N.C		
49	V_{DD}	-	+5V supply pin
50-55	N.C		
56	A1	O	External DRAM address output A1
57-60	N.C		
61	A2	O	External DRAM address output A2
62-66	N.C		
67	A0	O	External DRAM address output A0
68	XRAS	O	External DRAM low address strobe output pin.
69	XWSO	O	When DYSL is at 'L', turns to serial data output pin, and operates according to the various serial I/O modes. When DYSL is at 'H' turns into the write enable output pin of the external DRAM.
70	DIO	I/O	Turns to serial data input pin when DYSL is at 'L' and takes in according to the various serial I/O modes. Turns into external DRAM data I/O pin when DYSL is at 'H' to assume a common bus with DRAM data input D_{IN} and data output D_{OUT}.
71	XCAS	O	External DRAM column addess strobe output pin.
72-73	N.C		

No	Symbol	I/O	Description
74	SDT	I	Serial data input pin that receives commands, coefficient and I/O control transfer from the microcomputer. In each transfer modes, single 40-bit block is transferred at a time.
75	SCK	I	SDT serial clock input pin. Takes in data with the rising edge.
76	XSLD	I	Latch input pin that serves to latch inside the IC 1 block of serial data 40bit in length active at 'L'.
77	SIO2	I	Input pin. Sets the number of BCK clocks used for data transfer per channel (ch1 and 2) in one sampling section. When fixed to GND it turns to 32bit clock mode. When fixed to +5V it turns to 24bit clock mode.
78	DYSL	I	Delay I/O mode select input pin. When GND is fixed it turns to serial mode. Operates similarly as serial I/O. Fixed at +5V it turns to delay mode. Connected to an external DRAM (64kbit) composes a delay line for 2 channels.
79–80	N.C		

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Operating temperature	Topr	-20		75	°C

Electrical Characteristics

DC Characteristics (V_{DD}=5V±10%, Vss=0V, Topr=-20 to 75°C)

Item		Symbol	Conditions	Min.	Max.	Unit
Output voltage (1)	H level (1)	V_{OH} (1)	I_{OH}=-2mA	V_{DD} -0.5V	V_{DD}	V
	L level (1)	V_{OL} (1)	I_{OL}= 4mA	Vss	0.4	V
Note1 Input voltage (1)	H level (1)	V_{IH} (1)		2. 2		V
	L level (1)	V_{IL} (1)			0.8	V
Note 2 Input voltage (2)	H level (2)	V_{IH} (2)		0.7 V_{DD}		V
	L level (2)	V_{IL} (2)			0.3 V_{DD}	V
Input leak current		I_{LI}	V_I=0V to V_{DD}	-10	10	μA
Input leak current	Note3	I_{LZ}		-40	40	μA

Note 1) TTL input pin (CXD1160AP–27 pin, CXD1160AQ–70 pin)
Note 2) CMOS input pin
Note 3) During tristate pin input

Input/Output Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	CIN			12	pF
Output pin	COUT			12	pF
I/O pin	CI/O			12	pF

Test Conditions V_{DD}=V_I=0V, f=1MHz

Operation

Block Diagram Description

(1) I-RAM

I-RAM Instruction RAM with command word length of 24bit × 64 word. Write in from the exterior possible through microcomputer interface. Commands are divided into 1/2/3/ cycle commands according to type. Jumps to No. 0 every sampling cycle.

1-address stack 6bit address 2-stage stack. Combination with double sub routine or loop jump is possible.

Loop Counter 4bit loop counter. Loop jump possible from 0 to 15 times.

(2) K-RAM

K-RAM 16bit × 64 word coefficient RAM. Write in from the exterior can be performed through the microcomputer interface as well as write through execution command coefficient is in the format of complement on two while single precision (16b) and double precision (32b) are handled concurrently.

(3) D-RAM

D-RAM 16bit × 64 word data. Address space is ring shaped while the method adopted is for users to make access without knowledge of the physical address. Data is in the format of complement on two with single (16b) and double precision (32b) are handled concurrently.

D-address Counter 6bit long address counter counted up every sampling cycle. Users are aware of the address relative to that of the address counter value. The counter indicates the actual physical address and can be handled as a delay tap fixed address.

(4) Data Register (all in complement on two format)

SI1 Register This register (32b) stores CH1 data input from serial I/O used for read only. Upper 16bit (I1H) and lower 16bit (I1L) can be handled independently.

SI2 Register This register (32b) stores CH2 data input from serial I/O used for read only. Upper 16bit (I2H) and lower 16bit (I2L) can be handled independently.

SO1 Register This register (32b) stores CH1 data output from serial I/O. Beside read/write, can also be handled as a temporary register. upper 16bit (O1H), and lower 16bit (O1L) can be handled independently.

SO2 Register This register (32b) stores CH2 data output from serial I/O. Beside read/write, can also be handled as a temporary register. Upper 16bit (O2H) and lower 16bit (O2L) can be handled independently.

DI Register This register (32b) stores CH1 or CH2 data input from delay I/O. Used for read only. Upper 16bit (DIH) and lower 16bit (DIL) can be handled independently.

DO Register This register (32b) stores CH1 or CH2 data output from delay I/O. Used for write only. Upper 16bit (DOH) and lower 16bit (DOL) can be handled separately.

P Register This register 33bit in length, stores the multiplied results of various bit lengths.

R Register Data set in this register (32b) through the transfer command can be utilized as one sided input to AV. Upper 16bit (RH) and lower 16bit (RL) can be set independently.

ACC Register — This 34bit long register stores AU operation results. However during comparison commands ('ACC-R' or 'ACC-4R') values are not renewed.

(5) MPY

MOA Selector — Selects either K-RAM data or data from various registers called out through the bus, by means of the multiplying command.

MOB Selector — Selects either D-RAM data or data from various registers called out through the bus, by means of the multiplying command.

MPY — Data selected by means of the above 2 selectors is multiplied together. There are 4 ways of multiplying K*D, K*X, X*D and X*X. Also 4 multiplying modes 16b*16b, 16b*32b, 32b*16b and 32b*32b.

(6) AU

AOA Selector — Selects either ACC or O by means of AU command

AOB Selector — Selects either P (33b) or R (32b) to convert into 34 bit length

AU — Data selected by means of the above 2 selectors is either added, subtracted, turned into absolute value or compared together.

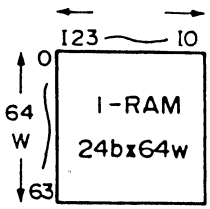
Clipper — When ACC data is transferred or multiplied, or sent to the below mentioned barrel shifter via the bus, clip processing is executed on the 34bit length to obtain a 32bit length. During transfer or multiplying the upper 16bit of this output (ACCH) and the lower 16bit (ACCL) can be handled independently

Barrel Shifter — ACC value passed through the clipper can be handled as follows 1) converted into positive value floating point form 2) arithmetic left shift executed 3) arithmatic - right shift executed.

Internal RAM structure

I-RAM

Instruction RAM (I-RAM) integrated in CXD1160AP/AQ is composed of address 0 to 63 (24b*64w) with a command word length of 24bit. Commands are transferred one (24bit) at a time through the microcomputer interface mode 1, from the exterior. Each transfer can be sent to the desired address.



External interrupt is executed at serial I/O LRCK and BCK. Every sampling cycle a jump is forcibly made to 0 address. That is, at every sampling the command is repeatedly executed from 0 address.

For executive commands there are, forced jump (JMP), condition jump, sub routine call (CAL), sub routine turn (RTN) and loop jump (LPJ). They all fly to the absolute address.

There are 2 stack stages and usage in conjunction with double sub routine or loop jump is possible.

Loop counter is conposed of 4bit and loop jump can be executed up to 15 times.

Command execution cycle is given according to MPY mode in 1/2/3/ cycle time.

The number of cycles that can be executed within 1 sampling section depends on the sampling frequency (fs) and the cycle clock ($f_{XCK}=f_{ICK}$). Let's assume that at sampling section 1 we have L cycle (cycle 0 to cycle L-1). Here, the last cycle (L-1) called KSH cycle cannot be executed because of the command or coefficient transfer section of the microcomputer interface. Cycle (L-2) called KSL cycle can be executed with the exception of K-RAM handling.

Example 1) $f_S=48kHz$ $f_{XCK}=\frac{1}{4}f_{MCK1}=\frac{1}{2}f_{MCK2}=6.144MHz(=48k\times128)$

In this case $f_{XCK}/f_S=128$. There are 128 cycles (cycle 0 to 127).

- Cycle 0 to cycle 125 ..... Execution cycle
- Cycle 126 ..... Execution possible with the exception of K-RAM handling.
- Cycle 127 ..... Execution impossible

Example 2) $f_S=44.1k$ $f_{XCK}=6.144M$

In this case at $f_{XCK}/f_S=139.3...$ both 139 cycle (cycle 0 to cycle 138) and 140 cycle (cycle 0 to cycle 139) exist.

- Cycle 0 to cycle 136 ..... Execution cycle
- Cycle 137 ..... Execution possible with the exception of K-RAM handling
- Cycle 138, 139 ..... Execution impossible.

The sequencial execution address of 63 address is 0 address.
When Power is ON the contents of I-RAM are not determined.

K-RAM

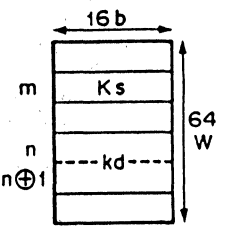
Coefficient RAM (K-RAM) built-in CXD1160AP/AQ is composed of 16bit × 64 word (address 0 to address 63). Single precision coefficient 1w (16b), double precision coefficient are expressed by 2w (32b) in succession, and can coexist on K-RAM. In the operation system both are complement on 2 and MSB can be handled as $1 > K \geq -1$ at Sign bit.

$$Ks = -K_{15} + \sum_{i=1}^{15} 2^{-i} K_{15-i} \qquad Kd = -K_{31} + \sum_{i=1}^{31} 2^{-i} K_{31-i}$$

Coefficient transfers from the exterior in the microcomputer interface K mode the required successive 2 addresses (32b) at one time. As there is also inside the execution command a command that serves to write in K-RAM, one part can be used as a temporary register. At Power ON K-RAM contents are undetermined.

Referring to the fig on the right the storage position can be defined as follows.

- When m address single precision is specified, the single precision coefficient Ks in m address can be used.
- When n address double precision is specified, the double precision coefficient kd in n address n⊕ address 1 can be used. Here low word K_L is stored in n address and high word K_H is stored in n⊕ 1 address.



K-RAM address specify can be mentioned in the command that actually handles K-RAM. There are 2 types of K-RAM address specify absolute address specify and relative address specify.

- Absolute adderss specify Absolute address→addr
- Relative address specify addr⊕relative address→addr

During commands that do not handle K-RAM, the present address addr does not change. (addr→addr)

At the forced 0 address jump every sampling cycle, reset is executed to addr=0. Accordingly and for the first time only, both the absolute address specify and relative address specify indicate the same physical address.

When double precision command is utilized with addr, after the command execution, addr+1→addr is obtained. Note that the present address obtained is 1 increment over that of the address specified from the user side.

Address 63 and address 0 are ring addresses. (0⊕−1=63, 63⊕1=0)

As a total of 2 cycles, the last cycle of the sampling section and the cycle before that, are coefficient transfer sections, K-RAM cannot be utilized.

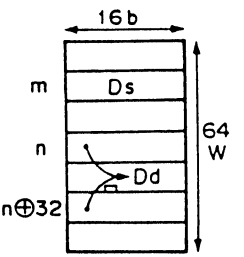
D-RAM

Data RAM(D-RAM) built-in CXD1160AP/AQ is organized in 16 bit x 64 word (address 0 to address 63). Single precision data is indicated in 1W (16b) and double precision data at a 32 address distance in 2W (32b). Both can be disposed on D-RAM. For operations both are used with complement on two. MSB is at Sign Bit to be handled as $1>D\geq-1$. D-RAM contents is unspecified at Power On.

$$Ds=-D_{15}+\sum_{i=1}^{15}2^{-i}D_{15-i} \qquad Dd=-D_{31}+\sum_{i=1}^{31}2^{-i}D_{31-i}$$

Referring to the fig. on the right the storage position can be defined as follows.

- When m address single precision is specified, single precision data Ds can be used.
- When n address double precision is specified, double precision data Dd in n ⊕ address 32 can be used. Here high word D_H is stored in n address and low word D_L in n ⊕ address 32.



D-RAM address specification by users is a logical address and not a physical one.
Inside the IC there is a 6 bit ring address counter that is incremented every I/O sampling. The logical address addr which is modulo added to this counter value DAC because the physical address.

Physical address=DAC ⊕ addr

Example) Logical address is assigned to the respective data in the formula at right.

formula: $y(n)=k_1y(n-1)+k_2X(n)+k_3X(n-1)$

addr: 3 2 1 0

If y(n) is entered in addr=3 and X(n) in addr=1 then y(n-1) is constantly in addr=2 and X(n-1) in addr=0

Physical address⇨	4	3	2	1	0
DAC=0 n		y(n)	y(n-1)	X(n)	X(n-1)
DAC=1 n+1 →n	y(n)	y(n-1)	X(n)	X(n-1)	X(n-2)

D-RAM address specify can be mentioned in the command that actually handles D-RAM.
There are 2 types of address specify, absolute address specify and relative address specify.

- Absolute address specify Absolute address → addr
- Relative address specify addr ⊕ relative address → addr

With commands where there is no D-RAM address specify, the present address addr remains unchanged. (addr → addr).
Reset to addr=0 is effected at address 10 forable jump every sampling cycle. Accordingly and for the first time only, absolute address specify and relative address specify indicate the same logical address.
Address 63 and address 0 are ring addresses (0⊕−1=63, 63⊕1=0)

Note that double precision data low word side is far away to determine all the data location.

The last cycle in the sampling section is a command transfer section and commands cannot be executed.

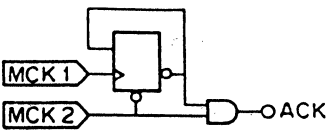
Interface

Clock circuit

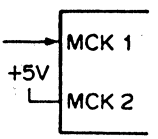
There are 2 methods to generate the master clock ACK in this IC.

(1) The clock input from MCK1 input pin is frequency divided by 2 internally to be ready for use.

(2) The clock input from MCK2 input pin is directly used.

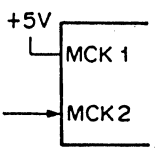


(1) When the input is from input pin MCK1
Fix input pin MCK2 to +5V



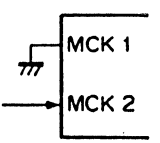
$$f_{MCK1} = 2f_{ACK}$$

(2) When the input is from input pin MCK2
Fix input pin MCK1 to +5V or to GND



$$f_{MCK2} = f_{ACK}$$

In any case the maximum frequency of master clock ACK is



$$f_{ACK} \leq 15.36\text{MHz}(=48\text{K} \times 320)$$

Moreover as this IC makes use of a dynamic F/F internally, it is not possible to stop the the master clock and keep the internal condition as it is.

Cycle clock ICK (or KCK) inside the IC is twice ACK master clock.

$$f_{ICK} = f_{KCK} = \frac{1}{1} f_{ACK}$$

Commands differ according to type. There are 1 cycle/2 cycle and 3 cycle commands.

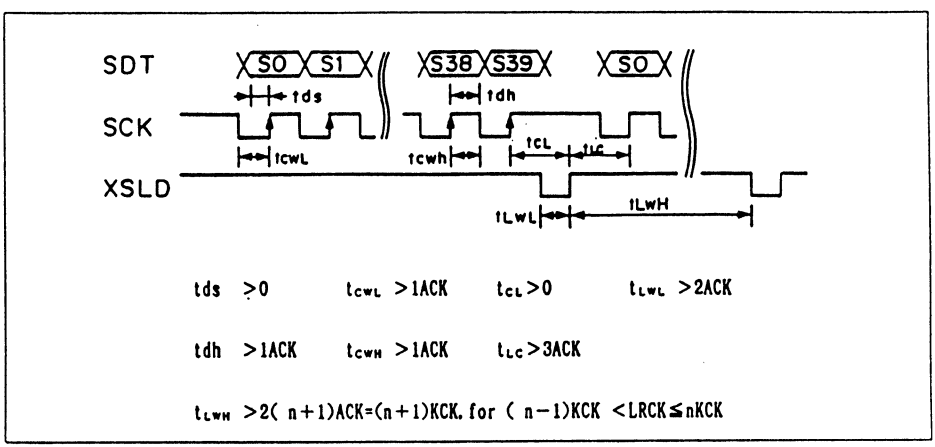
Microcomputer Interface

There are 3 input pins used for microcomputer control. Those are used to rewrite in part or totally K-RAM or I-RAM inside the IC, as well as to execute the various settings of serial I/O and delay I/O.

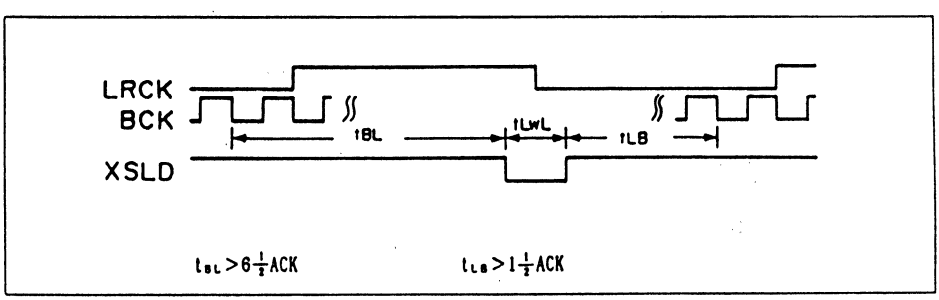
• SDT	40 bit in length of serial data per transfer.
• SCK	This serial clock transfers serial data to the internal shift register at the rising edge.
• XSLD	This gate pulse (active low level) latches in a lump the 40 bit serial data input to the shift register. At the same time and with this rising edge processing inside the IC is requested.

* When this IC is used as a multi-processor, all SDT pins or SCK pins on the respective IC's may be linked.

The transfer format (shown later on) timing system features serial data from S0 (top bit) to S39 as shown in the big below.



By applying the below conditions to XSLD the above t_{LWH} conditions can be prevented and the max. Transfer rate of 40 bit/LRCK realized.



The setting contents transferred through this microcomputer interface are undetermined inside the IC when Power is ON.
SDT, SCK and XSLD timing is regulated inside the IC before usage.

Transfer format

	K mode	I mode	R mode
S0	K0 (LSB)	I0	R0 (LSB)
S1	K1	I1	R1
S2	K2	I2	R2
S3	K3	I3	R3
S4	K4	I4	R4
S5	K5	I5	R5
S6	K6	I6	R6
S7	K7	I7	R7
S8	K8	I8	R8
S9	K9	I9	R9 (MSB)
S10	K10	I10	———
S11	K11	I11	———
S12	K12	I12	———
S13	K13	I13	———
S14	K14	I14	———
S15	K15	I15	———
S16	K16	I16	SIO0
S17	K17	I17	SIO1
S18	K18	I18	———
S19	K19	I19	DIO
S20	K20	I20	———
S21	K21	I21	———
S22	K22	I22	———
S23	K23	I23	MUTE
S24	K24	———	———
S25	K25	———	———
S26	K26	———	———
S27	K27	———	———
S28	K28	———	———
S29	K29	———	———
S30	K30	———	———
S31	K31 (MSB)	<L>	<H>
S32	KA0 (LSB)	IA0 (LSB)	———
S33	KA1	IA1	———
S34	KA2	IA2	———
S35	KA3	IA3	———
S36	KA4	IA4	———
S37	KA5 (MSB)	IA5 (MSB)	———
S38	———	———	———
S39	<L>	<H>	<H>

* In brackets < > respective modes proper value
* Between "———"=don't care

(1) K mode

This mode transfers the coefficient (complement on 2 and MSB at sign bit) to K-RAM (16bit × 64w). S39 is at 'L'.

With the 6 bits of KA5 (MSB) to KA0 K-RAM address (address 0 to 63) is specified. 16 bits, K15 to K0 are input from MSB side to KA address. 16 bits, K31 to K16 are input from MSB side to KA⊕1 address. When KA specifies address 63, KA⊕1 goes to 0 address. When K31 to K0 are at double precision coefficient (32bits), handle through the low word side KA address for instructions.

$$K_{KA}=-K_{31}+\sum_{i=1}^{15} 2^{-i}K_{31-i}$$

Then,

If K15 to K0 or K 31 to K 16 are at single precision coefficient(16bit)

$$K_{KA}=-K_{15}+\sum_{i=1}^{15} 2^{-i}K_{15-i} \quad \text{or} \quad K_{KA+1}=-K_{31}\oplus\sum_{i=1}^{15} 2^{-i}K_{31-i}$$

Then,

Whatever the contents be, there is no change as far as the transfer of a 2 word part to an address where KA and KA⊕1 are in succession, is executed each time.

Moreover,note that there are write in commands to K-RAM in the instructions too.

(2) I mode

This mode transfers instructions to I-RAM (24 bit × 64W) S39 is at 'H' and S 31 at 'L'. IA5 (MSB) to IA0 (LSB) 6 bit specify I-RAM address IA (address 0 to 63). To this IA address I23 to I0 24 bit are input.

(3) R mode

This mode transfers information relative to the setting of serial I/O and Delay I/O. S39 is at 'H' and S31 at 'H' too.

Beside this, setting is executed at pins DYSL and SIO2 of the IC according to requirements.

DYSL	Delay I/O
Fix to GND	Serial mode
Fix to +5V	Delay mode

SIO2	Bit clock (BCK)
Fix to GND	32 bit clock mode
Fix to +5V	24 bit clock mode

□ $\overline{\text{MUTE}}$

Controls serial I/O output (SO) and output (XWSO) during delay I/O serial mode. When delay I/O is in delay mode, only serial I/O is controlled.

The actual MUTE switching is synchronous with the rising edge of LRCK and serial output data. In any case, serial output data doesn't change in the middle of a bit.

$\overline{\text{MUTE}}$	Serial I/O output	Delay I/O (Serial mode) output
"L" Mute ON	0 (all L)	0 (all L)
"H" Mute OFF	Serial out register value	Delay out register value

☐ DIO
Sets the bit length of delay sample data during Delay I/O delay mode.

DIO	Delay data	Conditions to be met for proper operation
"L"	30 bit length	LRCK≧128KCK=256ACK
"H"	32 bit length	LRCK≧136KCK=272ACK

☐ SIO1, SIO0
In combination with IC Pin SIO2, select I/O format of serial I/O and Delay I/O (Serial mode)

SIO2	SIO1	SIO0	Bit clock	IN data		Out data
GND	X	X	32 clock	32 bit	——	32 bit
+5V	L	L	24 clock	16 bit	——	24 bit
"	L	H	"	24 bit	——	24 bit
"	H	L	"	24 bit	——	16 bit
"	H	H	"	16 bit	——	16 bit

☐ R9 to R0
Sets the delay sample quantity common to Delay I/O (delay mode) 2ch number of delay samples.

R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Number of delay samples
L	L	L	L	L	L	L	L	L	L	1
H	H	H	H	H	H	H	H	H	H	2
H	H	H	H	H	H	H	H	H	H	3
H	H	H	H	H	H	H	H	H	H	4
				≀						≀
L	L	L	L	L	L	L	L	H	H	1022
L	L	L	L	L	L	L	L	H	L	1023
L	L	L	L	L	L	L	L	L	H	1024

Control bits not in usage may be set to either H or L.
For Serial I/O and Delay I/O see different paragraph for details.

Serial I/O

Serial data interface I/O corresponding to 16 bit stereo D/A converter (CX20152) format.
One each for input and output, operate in common synchronously with external LRCK and BCK.
Each inputs and outputs data for 2ch at every sample cycle. For bit clock BCK there are 2 kinds, 32 bit clock mode and 24 bit clock mode.
Data format is in complement on 2 positive logic binary fixed decimal point type.
There is 32 bit/24 bit/16 bit data according to the various modes. Transfer order for each and all is at the last LSB.

Pin	I/O	Contents
LRCK	IN	Serial mode clock (Sampling cycle clock). Transfers channel 1 at H level and channel 2 at L level.
BCK	IN	Serial data bit clock. Features for each channel 32 bit clock mode and 24 bit clock mode.
SI	IN	Serial data input. Takes in synchronously with BCK rising edge.
SO	OUT	Serial data output. Outputs synchronously with BCK falling edge.

Inside the IC the following registers are compatible with Serial I/O. Handling is possible in 16 bit or 32 bit units.

Reg.	Contents	bit length	R/W	Bit expression for later mention
I1H	Channel 1 input high word register	16	R	A_{31} A_{30} ---------- A_{17} A_{16}
I1L	Channel 1 input low word register	16	R	A_{15} A_{14} ---------- A_{1} A_{0}
I2H	Channel 2 input high word register	16	R	B_{31} B_{30} ---------- B_{17} B_{16}
I2L	Channel 2 input low word register	16	R	B_{15} B_{14} ---------- B_{1} B_{0}
O1H	Channel 1 output high word register	16	R/W	C_{31} C_{30} ---------- C_{17} C_{16}
O1L	Channel 1 output low word register	16	R/W	C_{15} C_{14} ---------- C_{1} C_{0}
O2H	Channel 2 output high word register	16	R/W	D_{31} D_{30} ---------- D_{17} D_{16}
O2L	Channel 2 output low word register	16	R/W	D_{15} D_{14} ---------- D_{1} D_{0}

For Instructions read only available for input register. For output register either read or write available. For use as single precision (16 bit) register, the above 8 registers can all be handled independently. For instance when I1H is specified the numerical expression becomes, A_{31} at MSB (sign bit) and A_{16} at LSB

$$A_S = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i}$$

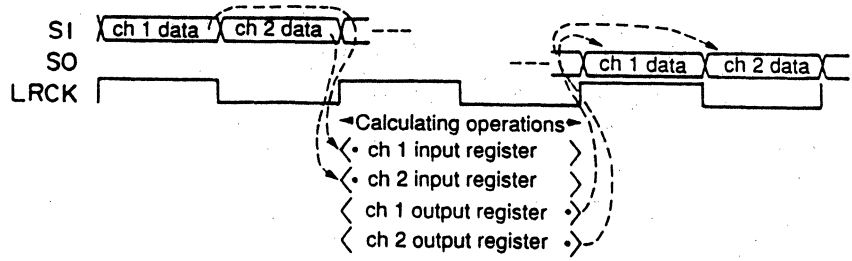
For use as double precision (32 bit) register, I1H/L, I2H/L, O1H/L and O2H/L come in pairs. For instance when I1H is specified the numerical expression becomes, A31 at MSB (sign bit) and A0 at LSB.

$$A_d = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i}$$

This is not usual but when I1L is specified at double precision, numerical expression becomes A15 at MSB (sign bit) and A16 at LSB.

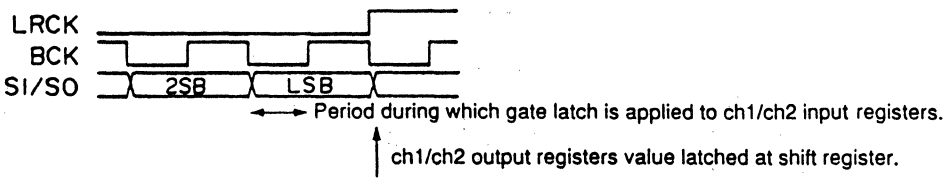
$$A_d = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i} + \sum_{i=1}^{15} 2^{-16-i} A_{31-i}$$

Outline of Serial I/O timing



First, during 1LRCK period, ch1/ch2 serial data that is input from SI is latched at ch1/ch2 input register with the rising edge of the following LRCK. Also,during 1LRCK, if the results of the calculating operations are enclosed into ch1/ch2 output registers, those are latched by the shift register at the following rising edge of LRCK to be respectively output as serial data from SO.

Detailed timing between Serial I/O and I/O register is as follows.



Serial I/O and I/O register are dependent on the timing with LRCK and BCK from the exterior. Also the only interrupt is executed between this LRCK and BCK on the Instructions.

The IC operates on the master clock. Now, should the operation be going on in 1LRCK period at cycle 0 to cycle L (L+1 cycle), the following restrictions would apply to the I/O register handling.

<Input register read command>

Cycle (L-3), (L-2), (L-1), L cannot read.

Cycle 0 to cycle (L-4) can read.

<Output register write command>

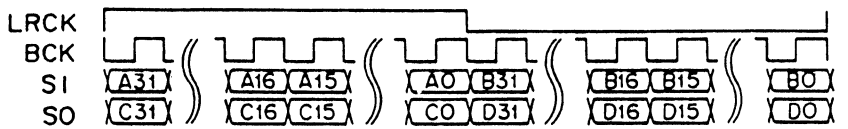
The following are standards of cycles where write cannot be executed in the output register. This is because of the frequency relationship between bit clock BCK and cycle clock KCK (ICK).

Order of cycle	24 clock mode	32 clock mode
L-3	12KCK ≧LRCK≧ 0	16KCK ≧LRCK≧ 0
L-2	60KCK 〃 0	80KCK 〃 0
L-1	108KCK 〃 0	144KCK 〃 0
L	all	all
0	LRCK ≧ 132KCK	LRCK≧176KCK
1	LRCK ≧ 180	LRCK ≧ 240
2	LRCK ≧ 228	LRCK ≧ 304
⋮		
n	LRCK ≧ 132+48n	LRCK ≧ 176+64n

(1) 32 bit clock mode 32 bit IN-32 bit OUT

SIO2	SIO1	SIO0
GND	×	×

Timing



Register

	MSB	(LSB)	(MSB)	LSB
I1H	A_{31} A_{30} ……A_{17} A_{16}	I1L	A_{15} A_{14} ……A_1 A_0	
I2H	B_{31} B_{30} ……B_{17} B_{16}	I2L	B_{15} B_{14} ……B_1 B_0	

	MSB	(LSB)	(MSB)	LSB
O1H	C_{31} C_{30} ……C_{17} C_{16}	O1L	C_{15} C_{14} ……C_1 C_0	
O2H	D_{31} D_{30} ……D_{17} D_{16}	O2L	D_{15} D_{14} ……D_1 D_0	

If all data is handled as 32 bit data then, we have 2ch IN 2ch OUT.
If all data is handled as 16 bit data, then we have 4ch IN 4ch OUT.
Mixed handling in single precision (16 bit) and double precision is possible.

Example of Single precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i} \qquad I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i}$$

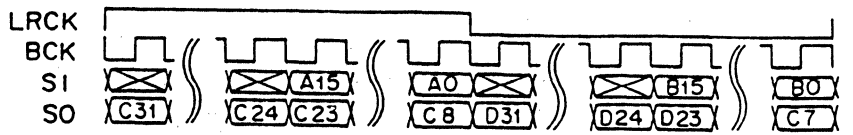
Example of Double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i}$$

(2) 24 bit clock mode 16 bit IN-24 bit OUT

SIO2	SIO1	SIO0
+5V	L	L

Timing



Register

		MSB LSB	
I1H	×·····×	I1L	A_{15} A_{14} ·····A_1 A_0
I2H	×·····×	I2L	B_{15} B_{14} ·····B_1 B_0

	MSB		LSB 8LSB
O1H	C_{31} C_{30} ·····C_{17} C_{16}	O1L	C_{15} C_{14} ·····C_8 × ·····×
O2H	D_{31} D_{30} ·····D_{17} D_{16}	O2L	D_{15} D_{14} ·····D_8 × ·····×

Input register enters on low word register side. Output register is at lower 8 bit don't care.

Example of single precision numerical expression

$$I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i}$$

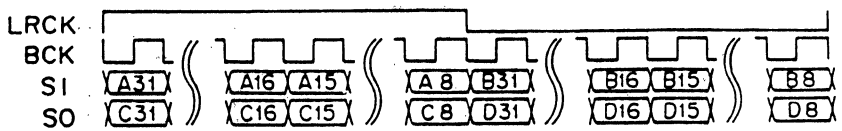
Example of double precision numerical expression

$$O1H = -C_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} \Rightarrow -C_{31} + \sum_{i=1}^{23} 2^{-i} C_{31-i}$$

(3) 24 bit clock mode 24 bit IN-24 bit OUT

SIO2	SIO1	SIO0
+5V	L	H

Timing



Register

	MSB		LSB	8LSB
I1H	A_{31} A_{30} ····· A_{17} A_{16}	I1L	A_{15} A_{14} ····· A_8 0 ····· 0	
I2H	B_{31} B_{30} ····· B_{17} B_{16}	I2L	B_{15} B_{14} ····· B_8 0 ····· 0	

	MSB		LSB
O1H	C_{31} C_{30} ····· C_{17} C_{16}	O1L	C_{15} C_{14} ····· C_8 × ····· ×
O2H	D_{31} D_{30} ····· D_{17} D_{16}	O2L	D_{15} D_{14} ····· D_8 × ····· ×

0 is input in the lower 8 bit of the input register, while the output register lower 8 bit are at don't care.
24 bit 2ch IN-24 bit 2ch OUT.
Can be handled as the data between 16 bit and 8 bit..

Example of single precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i} \qquad I1L = -A_{15} + \sum_{i=1}^{15} 2^{-i} A_{15-i} = -A_{15} + \sum_{i=1}^{7} 2^{-i} A_{15-i}$$

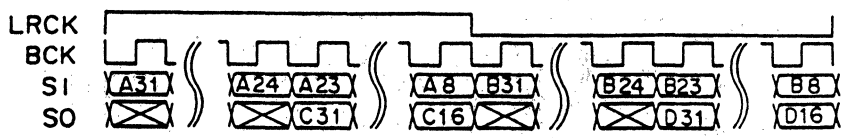
Example of double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} \Rightarrow -A_{31} + \sum_{i=1}^{23} 2^{-i} A_{31-i}$$

(4) 24 bit clock mode 24 bit IN-16 bit OUT

SIO2	SIO1	SIO0
+5V	H	L

Timing



Register

MSB LSB 8 LSB

I1H	A_{31} A_{30} ·····A_{17} A_{16}	I1L	A_{15} A_{14} ·····A_8 0 ·····0
I2H	B_{31} B_{30} ·····B_{17} B_{16}	I2L	B_{15} B_{14} ·····B_8 0 ·····0

MSB LSB

O1H	C_{31} C_{30} ·····C_{17} C_{16}	O1L	×·····×
O2H	D_{31} D_{30} ·····D_{17} D_{16}	O2L	×·····×

In the input register lower 8 bit there are eight 0's. The output register uses the high word side. Accordingly O1L and O2L are used as temporary registers.

Example of single precision numerical expression

$$O1H = -C_{31} + \sum_{i=1}^{15} 2^{-i} C_{31-i}$$

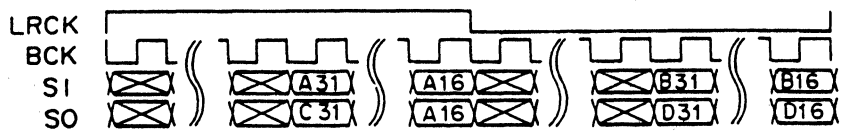
Example of double precision numerical expression

$$I1H = -A_{31} + \sum_{i=1}^{31} 2^{-i} A_{31-i} = -A_{31} + \sum_{i=1}^{23} 2^{-i} A_{31-i}$$

(5) 24 bit clock mode 16 bit IN-16 bit OUT

SIO2	SIO1	SIO0
+5V	H	H

Timing



Register

	MSB		LSB		
I1H	A_{31} A_{30} ·····	A_{17} A_{16}	I1L	× ····· ×	
I2H	B_{31} B_{30} ·····	B_{17} B_{16}	I2L	× ····· ×	

	MSB		LSB		
O1H	C_{31} C_{30} ·····	C_{17} C_{16}	O1L	× ····· ×	
O2H	D_{31} D_{30} ·····	D_{17} D_{16}	O2L	× ····· ×	

As the input register uses high word register only.
Accordingly I1L and I2L are not use. O1L and O2L are used as temporary registers.

Example of single precision numerical expression.

$$I1H = -A_{31} + \sum_{i=1}^{15} 2^{-i} A_{31-i}$$

Delay I/O

There are 2 modes. When input pin DYSL is grounded serial mode is on. When it is set to +5V delay mode is ON.

Here serial mode means delay I/O operates similarly as serial I/O. Also, in delay mode DRAM is connected to the exterior and sample delay executed at will.

The following registers correspond to delay I/O inside the IC. Handling is either in units of 16 bit or 32 bit.

Reg.	Contents	bit length	R/W	Bit expression for later mention
DIH	Input high word register	16	R	E_{31} E_{30} ..... E_{17} E_{16}
DIL	Input low word register	16	R	E_{15} E_{14} ..... E_{1} E_{0}
DOH	Output high word register	16	W	F_{31} F_{30} ..... F_{17} F_{16}
DOL	Output low word register	16	W	F_{15} F_{14} ..... F_{1} F_{0}

In the Instructions, input register is for read only while output register is for write only.

When used as single precision register (16 bit), the 4 registers shown above may be used individually. That is when DIH is specified, numerical expression turns out as MSB at E_{31} and LSB at E_{16}.

for $$E_s=-E_{31}+\sum_{i=1}^{15}2^{-i}E_{31-i}$$

When used as double precision register (32 bit), DIH/L and DOH/L come in pairs. That is when DIH is specified, numerical expression turns out as MSB at E_{31} and LSB at E0.

for $$E_d=-E_{31}+\sum_{i=1}^{31}2^{-i}E_{31-i}$$

as much as similarity with serial I/O register is concerned. However there is a decisive difference where the following points are concerned.

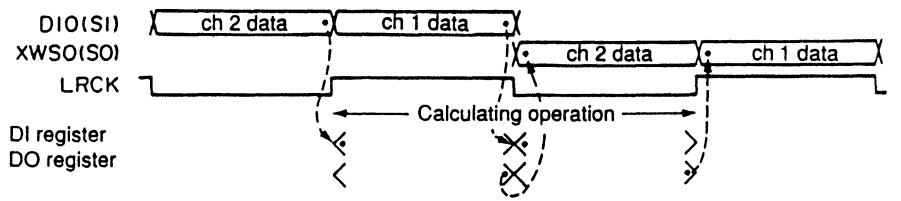
In serial I/O register two 32 bit stereo for 1ch each, are available. The 2 input registers maintain the same value for about 1LRCK. That is from the time both are input near LRCK rising edge until around the next LRCK rising edge. During this period read is possible any time. Move over after both the 2 output registers are output to S/R around LRCK rising edge, until the following LRCK rising edge and for about the period of 1LRCK, the next value to be output should be input. During this period, usage as temporary register is possible.

On the other hand, delay I/O register has only 32 bit 1ch. to stereo operate that, the input register has to be input twice during 1LRCK period.
Similarly the output register is input twice. Accordingly programs have to be written along those lines.

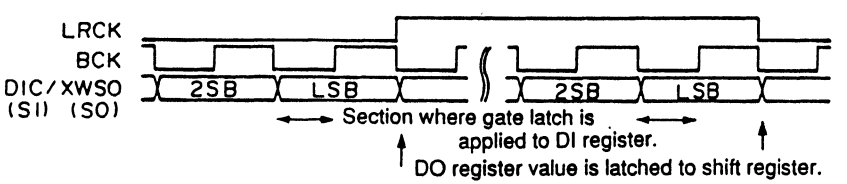
Delay I/O serial mode

By fixing input pin DYSL to GND delay I/O turns to serial mode.
In this case delay I/O operates as serial I/O. That is the timing system is regulated by LRCK and BCK and the format by SIO2, SIO1 and SIO0. Also serial input data is input and output through XWSO pin.

Delay I/O register is monoral. When it is input/output twice to 1LRCK, stereo operation is executed. An outline of delay I/O input/output system timing is as follows.



The detailed timing of delay I/O input/output register is as follows.



DI register value contained in the first half of 1LRCK calculating operations is the serial input data of the second half of the preceding LRCK. DI register value is similarly the serial input data of LRCK first half.
Also, the value entered to DO register in the first half becomes the serial output data of the same LRCK latter half in the 1LRCK calculating operations. The value entered in DO register during the second half becomes the serial output data in the first half of the following LRCK.

DI register read prohibit cycle around LRCK falling edge and DO register write prohibit cycle change in relation to LRCK, BC and the original oscillation. DI or DO registers handling around this area should be performed after due confirmation.

During delay I/O serial mode, turn open the external DRAM pins for delay mode, that is XRAS, XCAS and A7 to A0, 10 in all.

Delay I/O delay mode

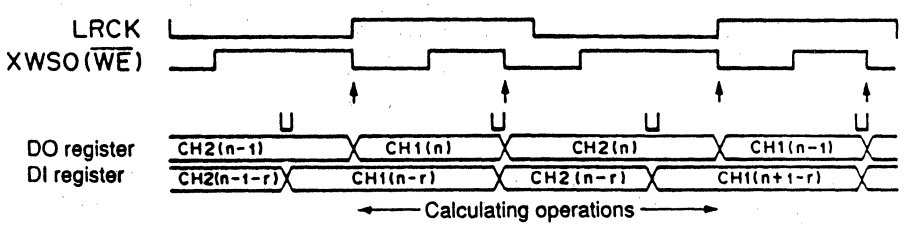
By fixing input pin DYSL to +5V, delay I/O turns to delay mode.
In this case, delay I/O composes the delay space by utilizing the 64K bit × 1 DRAM connected to the exterior.

64K × 1=1024 sample × (32 bit + 32 bit)

That is, 32 bit data 1 to 1024 sample stereo delay is performed. This stereo delay sample volume is set through the microcomputer interface R mode (R9 to R0).

R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	No. of delay sample r
L	L	L	L	L	L	L	L	L	L	1
H	H	H	H	H	H	H	H	H	H	2
H	H	H	H	H	H	H	H	H	L	3
H	H	H	H	H	H	H	H	L	H	4
				⌇						⌇
L	L	L	L	L	L	L	L	H	H	1022
L	L	L	L	L	L	L	L	H	L	1023
L	L	L	L	L	L	L	L	L	H	1024

Outline of the timing system is as follows.



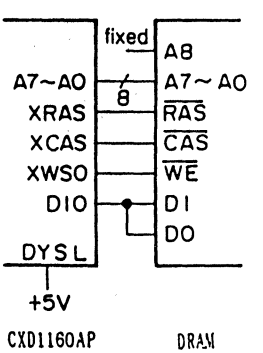
*DO register indicates data entered in the last part of that space.

That is if data CH1 (n) is written in DO register of 1LRCK (calculating operations) first half, then data CH1 (n-r) can be read from DI register. If data CH2 (n) is written in DO register at the second half, then data CH2 (n-r) can be read from DI register.

Connection to the external DRAM is as seen on the fig at right fixed.
Fix addresses over A8 to +5V or GND.

Moreover, for addresses that move frequently the order is: Column A0 to A4, Row A0 to A7, and column A5 to A7.

There are 2 kinds of data bit length for delay 32 bit and 30 bit. Timing system differs according to type.



(1) 32bit delay mode

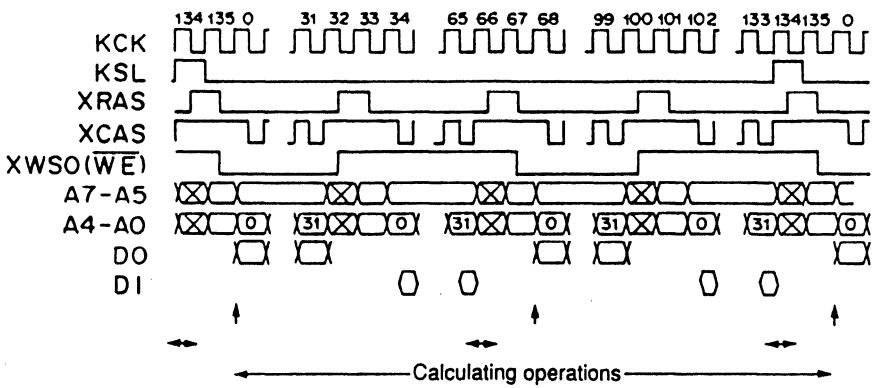
By turning DIO, of the microcomputer interface R mode to 'H', 32bit delay mode is set on. To realize this, the following hardware conditions should be met.

LRCK≧136KCK=272ACK

With 32bit delay mode, delay for all 32bit DI/DO registers is possible.

DIH	E_{31} E_{30}·····E_{17} E_{16}	DIL	E_{15} E_{14}·····E_{1} E_{0}
DOH	F_{31} F_{30}·····F_{17} F_{16}	DOL	F_{15} F_{14}·····F_{1} F_{0}

Timing (LRCK=136KCK Example)



Should the data written last between cycle 0 to 66 in DO register be at CH1(n), data CH1(n-r) from the previous cycle 134 up to the present cycle 65 in DI register can perform read.

Similarly, should data written last between cycle 68 and last cycle 1 in DO register be at CH2(n), data CH2(n-r) between cycle 66 to 133 in DI register can perform read.

(2) 30bit delay mode

By turning DIO, of the microcomputer interface R mode to 'L', 30bit delay mode is set on. To realize this, the following hardware conditions should be met.

$$LRCK \geq 128KCK = 256ACK$$

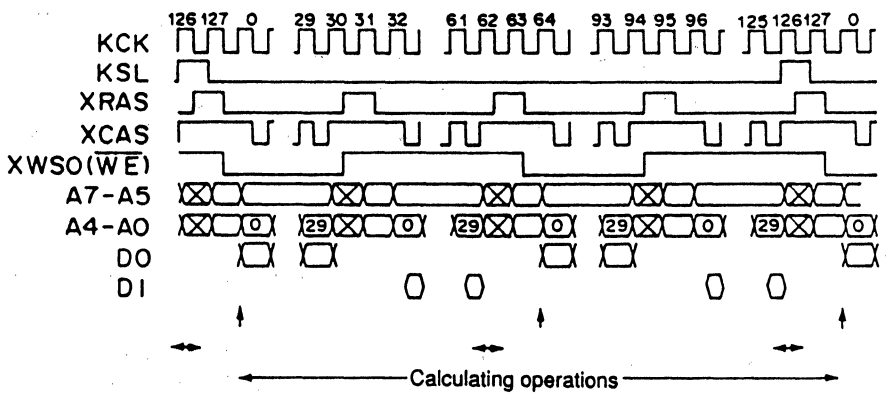
That is, 512 $f_{SMP} \leq f_{MCK1}$ or 256 $f_{SMP} \leq f_{MCK2}$

30bit delay mode can perform the delay of DI/DO register upper 30bit.

DIH	E_{31} E_{30}·····E_{17} E_{16}	DIL	E_{15} E_{14}·····E_3 E_2 0 0
DOH	F_{31} F_{30}·····F_{17} F_{16}	DOL	F_{15} F_{14}·····F_3 F_2 × ×

Here, DOL register lower 2bit are at don't care, DIL register lower 2bit contain 0.

Timing (LRCK=128KCK Example)



Should the data written last between cycle 0 to 62 in DO register be at CH1(n), data CH1(n-r) from the previous cycle 126 up to the present cycle 61 in DI register can perform read.

Similarly, should data written last between cycle 64 and last cycle 1 in DO register be at CH(n), data CH2(n-r) between cycle 62 to 125 in DI register can perform read.

Instructions

Outline

In one 24bit word length command the following can be executed in parallel. ① K-RAM and D-RAM address setting, ② MPY Command, ③ AU Command ④ Transfer Command ⑤ Jump Command. Data handled include, single precision (16b), double precision (32b) or through a combination of the 2, from 1 cycle to 3 cycle commands are available.

①K-RAM and D-RAM address setting

Sets the RAM address to be handled by a given command. For address setting there are, absolute address specify and relative address specify.

- K-RAM Single precision coefficient and double precision coefficient (2W in succession) can be used in this order or otherwise. Write is also enabled through a command allowing for use as a temporary register

- D-RAM Ring address. The modulo added value of the address counter value incremented at each serial I/O sampling cycle and that of the address set by the user becomes the actual value. Single precision data and double precision data (2W mutually separated by 32 addresses.) can be used in this order or otherwise.

②MPY Command

4 Types (K*D, K*X, X*D, X*X) and 4 kinds of modes (16b*16b, 16b*32b, 32b*16b, 32b*32b) can be handled. Through the respective modes the execution cycle of the command is determined.

K....K-RAM value D....D-RAM value

X....From the register related ones hanging to the main bus, those that can output Acc.

③AU Command

Can perform addition, subtraction, absolute value and comparison. A 2bit shifter is also biult-in.

④Transfer Command

Single precision data internally transfers double precision data via the main bus. Barrel shifter operations are executed through this transfer command.

⑤Jump Command

There are unconditional jump, conditional jump, subroutine call and return, loop jump. Stack features a 2-stage structure and combination with double sub routine or loop jump is possible. Loop counter can perform loop jump 0 to 15 times at 4b. At every serial I/O sampling cycle forced 0 address jump is executed.

Points in Execution Commands

Each execution command with a 24 bit word length can, widely speaking, process the following in parallel. RAM address setting, MPY command AU command, transfer command and jump command. Specially through MPY command, data to be handled is defined as single precision or double precision. According to what the execution cycle is determined.

Data register and data format

The following data resgisters relate to command execution

Symbol	bit	R/W	functions
I1H	16	R	Serial I/O channel 1 input high word register and low word register
I1L	16	R	
I2H	16	R	Serial I/O channel 2 input high word register and low word register
I2L	16	R	
O1H	16	R/W	Serial I/O channel 1 output high word register and low word register
O1L	16	R/W	
O2H	16	R/W	Serial I/O channel 2 output high word register and low word register
O2L	16	R/W	
D1H	16	R	Delay I/O input high word register and low word register
D1L	16	R	
DOH	16	W	Delay I/O output high word register and low word register
DOL	16	W	
RH	16	W	High word register and low word register for AU operations
RL	16	W	
P	33	—	Register where multiplication results are entered
Acc	34	—	Register where AU operation results are entered
AH	16	R	High word and low word from the 32 bit that passed
AL	16	R	Clipper in Acc register value
BSI	31	—	Barrel shufter input register and output register
BSO	16	R	

From the above commands that can execute Read become the source of transfer of the transfer command through the main bus or the multiplicator input data of MPY command.
In single precision (16b) commands, respective registers are handled independently. In double precision commands (32b) high word registers and low word registers are handled in pairs.

At power ON the respective registers data value become indefinite.

RAM address setting

(1) K-RAM address setting

Absolute address specify • K_{ϕ} (d) → addr

I12	I11 I10 I9 I8 I7 I6
H	a5 a4 a3 a2 a1 a0

At absolute expression 0 to 63

Relative address specify • addr⊕K_{ϕ} (r) → addr

I12	I11 I10 I9 I8 I7 I6
L	a5 a4 a3 a2 a1 a0

At complement on 2 expression −32 to +31

• addr⊕K_4 → addr

I9 I8 I7 I6
a3 a2 a1 a0

At complement on 2 expression −8 to +7

• addr⊕K_2 → addr

I7 I6
a1 a0

At complement on 2 expresion −2 to +1

• addr⊕K_* → addr K=+1

During single precision command, 1 word of K (addr) is handled.

$$K_s = -d_{15} + \sum_{i=1}^{15} 2^{-i} d_{15-i}$$

During double precision command, 2 word (32b) of K (addr) and K (addr ⊕ 1) are handled. Here,

$$K_4 = -d_{31} + \sum_{i=1}^{31} 2^{-i} d_{31-i}$$

With K (addr) at low word, K (addr ⊕ 1) at high word, 1 increment from the addr specified by the user, (addr ⊕ 1 → addr) execution is completed.
For commands where K-RAM is not handled, the present address remains unchanged.

At the forced 0 address jump every sampling cycle, reset is performed to addr=0.
K-RAM address space is shaped as a ring. (63 ⊕ 1 → 0, 0 ⊕ (−1) → 63).
During Power ON K-RAM contents are not defined.

(2) D-RAM address setting

D-RAM address specify by the user is a logical address and not a physical address. At the forced 0 address jump every sampling cycle, the ring address counter DAC is incremented by 6 bit.
The logical address addr modulo added to the ring address counter DAC is the physical address that actually points.

Physical addr=DAC⊕addr

What follows is all about logical address addr.

Absolute address specify • D_6 (d) →addr

I12	I5 I4 I3 I2 I1 I0
H	a5 a4 a3 a2 a1 a0

At absolute expression 0 to 63

Relative address specify • addr⊕D_6 (r) →addr

I12	I5 I4 I3 I2 I1 I0
L	a5 a4 a3 a2 a1 a0

At complement on 2 expression −32 to +31

• addr⊕D_4→addr

I3 I2 I1 I0
a3 a2 a1 a0

At complement on 2 expression −8 to +7

• addr⊕D_2→addr

I1 I0
a1 a0

At complement on 2 expression −2 to +1

• addr⊕D_0→addr D=+1

During single precision command, 1 word of D (addr) is handled

$$D_S = -d_{15} + \sum_{i=1}^{15} 2^{-i} d_{15-i}$$

During double precision command, 2 word (32b) of D (addr) and D (addr ⊕ 1) are handled.

$$D_d = -d_{31} + \sum_{i=1}^{31} 2^{-i} d_{31-i}$$

D (addr) is high word and D (addr ⊕ 32) is low word.
When there is no D-RAM address specify command the present address remains unchanged. (addr → addr)

At the forced 0 address jump every sampling cycle, reset is executed to addr=0.
Address space between D-RAM is ring shaped. (63 ⊕ 1 → 0, 0 ⊕ (−1) → 63)
At Power ON, D-RAM contents are undefined.

MPY Command

With the 2 bit of instructions I23 and I22, data length that is input to the multiplicator, is determined. Through this 4 types of MPY mode can be handled. Also, the command execution cycle is regulated by each mode.

I23	I22	bit*bit	Execution cycle
L	L	16 * 16	1
H	H	16 * 32	2
H	L	32 * 16	2
H	H	32 * 32	3

With the 2 bit of instructions I21 and I20, the type of data input to the multiplicator is determined. Here K indicates that the address specified with this command is from K-RAM data. Similarly, D indicates the address specified with this command is from D-RAM data.

I21	I20	type*type
L	L	K * D
H	H	K * X
H	L	X * D
H	H	X * X

X indicates this is the register assigned by the command. It is input to the multiplicator through the main bus.
When X is double precision specified, respective H/L registers are handled in pairs. In this case the resister assigned is handled in high word and the corresponding register in low word.

A more detailed table will turn out as follows.

I21 I20	L L	L H	H L	H H
I23 I22	K * D	K * X	X * D	X * X
L L	K16 *D16	K16 *X16	X16 *D16	X16 *X16
L H	K16 *D32	K16 *X32	X16 *D32	———
H L	K32 *D16	K32 *X16	X32 *D16	———
H H	K32 *D32	K32 *X32	X32 *D32	X32 *X32

For X*X with MPY command, either 16b*16b or 32b*32b is used. However for transfers where double precision X is at the source, X16*X32 type can be used.

Multiplication results enter register P and can be used with the next command.
P bit length is at 33 bit and (-1) * (-1)=+1 can also be stored.

$$P = -2d_{32} + \sum_{i=0}^{31} 2^{-i} d_{31-i}, \qquad +1 \geq P \geq -1 + 2^{-31}$$

The multiplicator itself operates all the time. P is renewed with every command.
In save commands where there is no X16*X32, X32*X16 or MPY command, P is undefined.

I9	I8	I7	I6	×
I3	I2	I1	I0	
L	L	L	L	I1H
L	L	L	H	I1L
L	L	H	L	I2H
L	L	H	H	I2L
L	H	L	L	O1H
L	H	L	H	O1L
L	H	H	L	O2H
L	H	H	H	O2L
H	L	L	L	DIH
H	L	L	H	DIL
H	L	H	L	BO1H
H	L	H	H	BO1L
H	H	L	L	BO2H
H	H	L	H	BO1L
H	H	H	L	AH
H	H	H	H	AL

AU Command

I19	I18	I17	I16=L	I16=H	Zero	Nz	Plus	Minus	OVF	XOVF
L	L	L	0+P →Acc	0+4P→Acc	○	○	○	○	○	○
L	L	H	Acc+P →Acc	Acc+4P→Acc	×	×	○	○	○	○
L	H	L	0−P →Acc	0−4P→Acc	○	○	○	○	○	○
L	H	H	Acc−P →Acc	Acc−4P→Acc	○	○	○	○	○	○
H	L	L	0+R →Acc	0+4R→Acc	○	○	○	○	○	○
H	L	H	Acc+R →Acc	Acc+4R→Acc	×	×	○	○	○	○
H	H	L	|R| →Acc	|4R| →Acc	○	○	○	○	○	○
H	H	H	Acc−R	Acc−4R	○	○	○	○	○	○

For the 4bit of Instructions I19 to I16 AU command is provided |R| and |4R| are absolute values. 'Acc-R' and 'Acc-4R' are absolute values. 'Acc-R' and 'Acc-4R' are comparison commands. Multiplication results are not stored in Acc, and Acc holds the previous value.

Acc bit length is at 34bit.

$$Acc=-4d_{33}+\sum_{i=-1}^{31}2^{-i}d_{31-i} \qquad 4-2^{-31}\geq Acc \geq -4 \qquad \text{Min. resolution capability } 2^{-31}$$

P is at 33bit of multiplication results from the previous command. It is code expanded to 34bit for use. R stands at a 32bit value as entered in R register by transfer commands from the commands received up to that. It is similarly code expanded to 34bit for use.

There are 5 Flags for the multiplication results of AU commands to be used when the following command is a conditional jump command. However where X mark is shown on the above chart, it is undefined, so exercise care.

Zero ····· Acc = 0
Non Zero ····· Acc ≠ 0
Plus ····· Acc ≥ 0
Minus ····· Acc < 0
Over Flow ····· Acc ≥1 or Acc<-1

Only for comparison commands Flag is raised for 'Acc-R' and Acc-4R.
XOVF output pin turns to active L during the command in execution after OVF has turned to true.

When Acc value is used for MPY, transfer or barrel shifter, it passes through clipper to be used in 32bit length.
Assuming clipper output=A, we have:

IF Acc ≥ 1 then A=1-2^-31
else 1 >Acc ≥-1 then A=Acc
else -1>Acc then A=-1

Transfer command

(1) Source and Destination

For the origin (source) of Transfer command K-RAM, D-RAM and X are provided.
Similarly, for the destination of transfer command K-RAM, D-RAM and Y are provided.
Accordingly, K-RAM and Serial I/O output registers (O1H~O2L) can be used as temporary registers.
Combinations are provided as follows.
{K-RAM, D-RAM} → Y
X → Y
X → {K-RAM, D-RAM}
In between RAM there is no direct transfer.

I9	I8	I7	I6	I3	I2	I1	I0	X
L	L	L	L					I1H
L	L	L	H					I1L
L	L	H	L					I2H
L	L	H	H					I2L
L	H	L	L					O1H
L	H	L	H					O1L
L	H	H	L					O2H
L	H	H	H					O2L
H	L	L	L					DIH
H	L	L	H					DIL
H	L	H	L					BO1H
H	L	H	H					BO1L
H	H	L	L					BO2H
H	H	L	H					BO2L
H	H	H	L					AH
H	H	H	H					AL

I9	I8	I7	I6	I3	I2	I1	I0	Y
L	L	L	L					——
L	L	L	H					——
L	L	H	L					RH
L	L	H	H					RL
L	H	L	L					O1H
L	H	L	H					O1L
L	H	H	L					O2H
L	H	H	H					O2L
H	L	L	L					DOH
H	L	L	H					DOL
H	L	H	L					BI1H
H	L	H	H					BI1L
H	H	L	L					BI2H
H	H	L	H					(keep)
H	H	H	L					(keep)
H	H	H	H					(keep)

Even if there is a transfer command to Y, incase it is not actually used, Y assignment uses 0 or 1.
BO1H to BO2L for X and BI1H to BI2H for Y, relate to the barrel shifter and will be referred to later on. X and Y assignment can be set independently for the transfer command of single precision data. For the transfer command of double precision data, X and Y came in pair as H/L registers. The one assigned is processed as high word register.
Whether the transfer command is of single precision or double precision depends on the transfer origin (source). That is determined through I23 and I22bit of MPY command.
MPY command uses for X*X, 16b*16b (I23, I22=LL, 1 cycle) or 32b*32b (I23, I22=HH, 3 cycle). Should the multiplication be ignored, double precision transfer can be executed at 16b*32b (I23, I22=LH, 2 cycle).

Be careful with 2 the following types of transfer commands that are prohibited.
① Between serial I/O output register of the same register (EX) O1H → O1H
② Respective registers relating to the barrel shifter B2H → B1L

(2) Barrel Shifter

Barrel shifter operation command is inserted in the transfer commands.
There are 3 types of barrel shifter operation commands depending on the transfer destination Y register.

Barrel shifter operaiton command	Transfer destination Y Register	Transfer data (16b) d_{15} d_{14} d_{13} d_{12} d_{11} d_{10} ~ d_0
①Positive value floating-point type conversion	BI1H	— — — — — — — —
②Arithmetic left shift	BI1L	— S_3 S_2 S_1 S_0 — ~ —
③Arithmetic right shift	BI2H	— S_3 S_2 S_1 S_0 — ~ —

As a rule those are single precision transfer commands. As for transfer data in the case of ① Positive value floating-point type conversion, anything will do. For ② Arithmetic left shift and ③ Arithmetic right shift the amount of shift S is specified in the 4 bit d_{14} to d_{11}. Conversion scale is, for ① also included, 0 to 15 bit .

$$S = \sum_{i=0}^{3} 2^i S_i \qquad 15 \geq S \geq 0$$

Input data to be converted is 31 bit data A^V, excluding LSB, taken from value A (32b) or the result value Acc from the previous command, passed through a clipper.

$$A^V = -a_{31} + \sum_{i=1}^{30} 2^{-i} a_{31-i} \qquad 1-2^{-30} \geq A^V \geq -1$$

The converted results can be observed from the following 4 registers. The value is kept until the following barrel shifter operation command is issued.

B01H is the respective data converted value.

$$BO1H = -d_{15} + \sum_{i=1}^{15} 2^{-i} d_{15-i}$$

BO1L shows input A with the exclusion of sign bit, where the upper 4 bit are inverted and the rest is filled with zero.

BO2H and BO2L apply a only during floating-point type conversion. The amount of shift Q is included.

$$Q = \sum_{i=0}^{3} 2^i q_i \qquad 15 \geq Q \geq 0$$

Output X register	Output data (16b) d_{15} d_{14} d_{13} d_{12} d_{11} d_{10} ~ d_0
BO1H	b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} ~ b_0
BO1L	a_{31} $\overline{a_{30}}$ $\overline{a_{29}}$ $\overline{a_{28}}$ $\overline{a_{27}}$ 0 ~ 0
BO2H	0 q_3 q_2 q_1 q_0 0 ~ 0
BO2L	0 0 q_3 q_2 q_1 0 ~ 0

① Positive value floating-point type conversion

Positive value A^{∇} (≥ 0, $a_{31}=0$) is converted to floating-point type ($A^{\nabla} \approx BO1H \cdot 2^{-Q}$).

Case I $A^{\nabla} \geq 2^{-16}$

$$A^{\nabla} = -0+\sum_{i=1}^{30} 2^{-i}a_{31-i} \quad \text{for} \quad 15 \geq Q \geq 0 \ , a_{31-(Q+1)} = 1$$

$$= \left\{\sum_{i=1}^{30-Q} 2^{-i}a_{31-Q-i}\right\} \cdot 2^{-Q} \approx \left\{-0+\sum_{i=1}^{15} 2^{-i}a_{31-Q-i}\right\} \cdot 2^{-Q} = BO1H \cdot 2^{-Q}$$

This, to turn into the regular form $BO1H \geq \frac{1}{2}$ ($b_{14}=1$)

Case II $2^{-16} > A^{\nabla}$

$$A^{\nabla} = -0+\sum_{i=1}^{30} 2^{-i}a_{31-i} = \sum_{i=17}^{30} 2^{-i}a_{31-i} = \left\{-0+\sum_{i=2}^{15} 2^{-i}a_{16-i}\right\} \cdot 2^{-15} = BO1H \cdot 2^{-Q}$$

This becomes $\frac{1}{2} > BO1H (d_{14}=0)$, $Q=15$

② Arithmetic left shift

With sign bit fixed, S bit of A^{∇} is shifted left

$$O1H = -a_{31}+\sum_{i=1}^{15} 2^{-i}a_{31-s-i}$$

Case I $2^{-s} > A^{\nabla} \geq 0$

$$A^{\nabla} \cdot 2^{s} = \left\{-0+\sum_{i=1}^{30} 2^{-i}a_{31-i}\right\} \cdot 2^{s} = \left\{\sum_{i=s+1}^{30} 2^{-i}a_{31-i}\right\} \cdot 2^{s} = \sum_{i=1}^{30-s} 2^{-i}a_{31-s-i}$$

$$\approx -0+\sum_{i=1}^{15} 2^{-i}a_{31-s-i} = BO1H$$

Case II $0 > A^{\nabla} \geq -2^{-s}$

$$A^{\nabla} \cdot 2^{s} = \left\{-1+\sum_{i=1}^{30} 2^{-i}a_{31-i}\right\} \cdot 2^{s} = -\left\{\sum_{i=1}^{30} 2^{-i}\overline{a_{31-i}}+2^{-30}\right\} \cdot 2^{s}$$

$$= -\left\{\sum_{i=s+1}^{30} 2^{-i}\overline{a_{31-i}}+2^{-30}\right\} 2^{s} = -\left\{\sum_{i=1}^{30-s} 2^{-i}\overline{a_{31-s-i}}+2^{-(30-s)}\right\}$$

$$= -1+\sum_{i=1}^{30-s} 2^{-i}a_{31-s-i} \approx -1+\sum_{i=1}^{15} 2^{-i}a_{31-s-i} = BO1H$$

Case III $A^{\nabla} \geq 2^{-s}$ or $-2^{-s} > A^{\nabla}$

In this case conversion cannot be executed correctly

③Arithmetic right shift
With sign bit fixed, S bit of A^{ν} is shifted right.

$$BO1H = -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{15} 2^{-i} a_{31+S-i}$$

However,

$$S = 0 \quad BO1H = -a_{31} + \sum_{i=1}^{15} 2^{-i} a_{31-i} \approx A^{\nu}$$

$$S = 15 \quad BO1H = -a_{31} + \sum_{i=1}^{15} 2^{-i} a_{31} = -2^{-15} a_{31}$$

$$A^{\nu} \cdot 2^{-S} = \{-a_{31} + \sum_{i=1}^{30} 2^{-i} a_{31-i}\} \cdot 2^{-S} = -2^{-S} a_{31} + \sum_{i=1}^{30} 2^{-S-i} a_{31-i}$$

$$= -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{30+S} 2^{-i} a_{31+S-i}$$

$$\approx -a_{31} + \sum_{i=1}^{S} 2^{-i} a_{31} + \sum_{i=S+1}^{15} 2^{-i} a_{31+S-i} = BO1H$$

Flag BSQ

This flag is renewed with every barrel shifter operation command. This applies only during positive floating-point conversion.
When positive value floating-point conversion is executed, from that bit shift Q

$$Q = \sum_{i=0}^{3} 2^{i} q_i$$

q_0 becomes the Flag BSQ.
That flag value is kept until the following barrel shifter operation command comes.
When condition jump command and barrel shifter operation command are on the same command, Flag BSQ that is utilized for condition jump, is the flag value of the previous barrel shifter operation command.

BSQ=ON The bit shift amount of the positive value floating-point conversion is an odd number
BSQ=OFF The bit shift amount of the positive value floating-point conversion is an even number

Jump system command

Jump commands for the instruction address include: conditional jump, unconditional jump and sub routine call. They all jump to addresses expressed in 6bit and containing an A.

$$A=\sum_{i=0}^{5} 2^i A_i \qquad 63 \geq A \geq 0$$

A5	A4	A3	A2	A1	A0
I5	I4	I3	I2	I1	I0
I5	I4	I3	I2	I11	I10
I5	I4	I9	I8	I11	I10

Sub routine call and loop jump can stack instruction address. They are formed by a 2-address FILO and can execute up to a double conbination. When stack performs a forced 0 address jump, it also keeps the previous condition.

(1) Conditional jump JP(F)

I15	I14	I13
H	H	H

When the condition is met, the following command executes the command of the address ahead of the jump.
When the condition is not met, the command after that executes the command of the address in the order.

I12	I11	I10	Flag	Conditions
L	L	L	Zero	Results of previous commands Acc=0
L	L	H	Non zero	Results of previous commands Acc=0
L	H	L	Plus	Results of previous commands Acc≧0
L	H	H	Minus	Results of previous commands Acc<0
H	L	L	Over flow	Results of previous commands Acc≧1 or Acc<-1
H	L	H	BSQ	Barrel shifter operation command (positive value floating-point type conversion) up to the previous command is odd numbered shift bit
H	H	L	(keep)	Actually same value as unconditional jump
H	H	H	(keep)	

* Below zero and Non zero cannot be used

Acc+P →Acc Acc+4P→Acc
Acc+R →Acc Acc÷4R→Acc

(2) Non conditional jump JMP

I15	I14	I13	I12
H	L	H	L
H	H	L	L

Elements from this command, execute the command of the address ahead of the jump, unconditionally

(3) Sub routine call CAL

I15	I14	I13	I12
H	L	H	H
H	H	L	H

This command executes the command of address ahead of the jump for the sub routine. Also it pushes to the stack the address following this command.

Return RTN

I15	I11	I10
I15	I5	I4
L	H	L

Next this command pops out the address from the stack and executes the command of that address.

(4) Loop jump

Sets the number of loops (0 to 15) in the 4 bit loop counter to repeatedly execute a certain group of commands (1 to 16 times).

Loop counter set
LCS (C)

I15 I14 I13	I12	I11 I10 I5 I4
H L L	L	C_3 C_2 C_1 C_0

Number of loops

$C=\sum_{i=0}^{3} 2^{-i} C_i \quad 15 \geq C \geq 0$

Sets the number of loops in the loop counter

Loop counter and loop address set
LTS (C)

I15 I14 I13	I12	I11 I10 I5 I4
H L L	H	C_3 C_2 C_1 C_0

Number of loops

$C=\sum_{i=0}^{3} 2^{-i} C_i \quad 15 \geq C \geq 0$

Sets the number of loops in the loop counter and also pushes into the stack the next instruction address (loop head address)

Loop address set
LPS

I15	I11 I10 I5 I4
L	H H

Pushes the next instruction address (loop head address) into the next instruction address

Loop jump
LPJ

I15	I11 I10 I5 I4
L	L H

Decrements the loop counter value
① C≧0 jumps to the address in the stack
② C<0 Pops out the stack and proceeds in order to the command of the following address

Example)

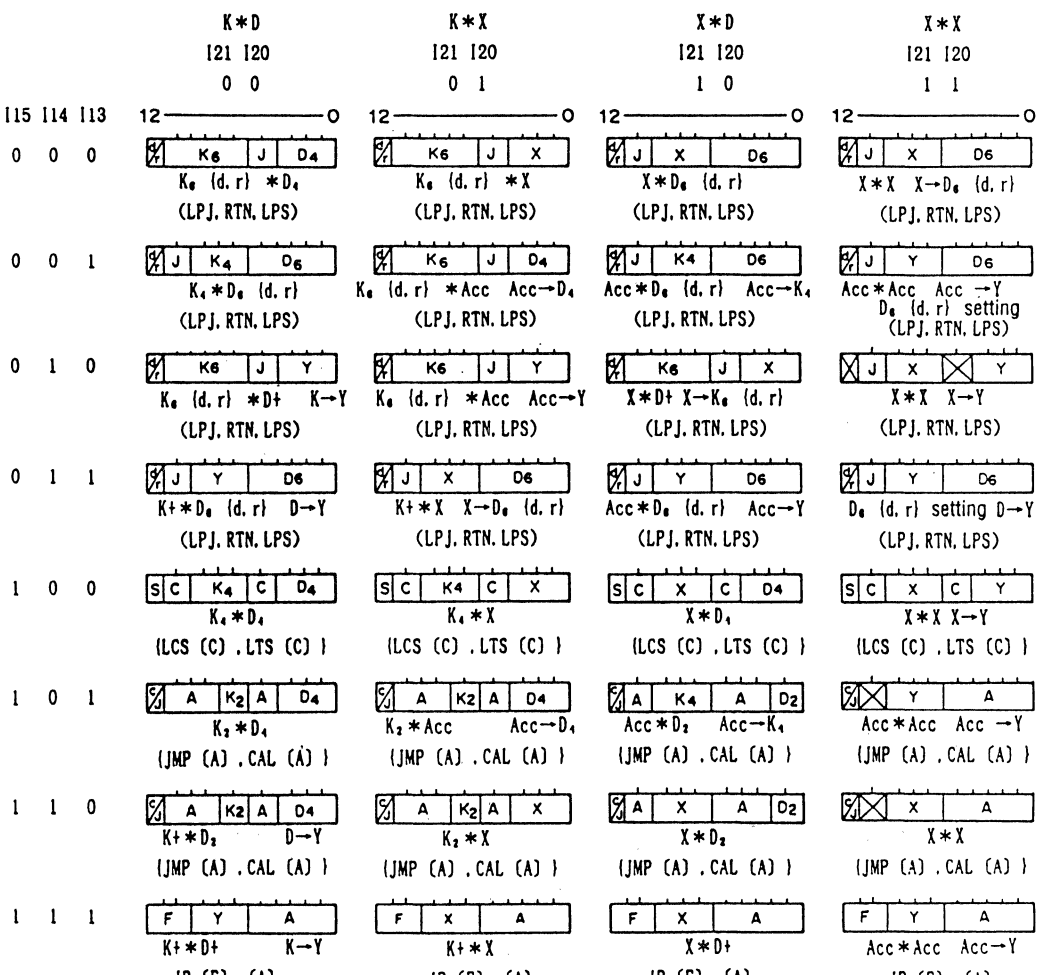
Program	Execution
LTS (1)	LTS 1→C
Command group A	Command group A
LPJ	LPJ C-1= 0→C (≧0)
Command group B	Command group A
	LPJ C-1= -1→C (<0)
	Command group B

The stack has a double structure. Accordingly, the following can be executed.
- The subroutine inside the subroutine
- The loop jump inside the sub routine
- The subroutine inside the loop jump

The loop jump inside the loop jump cannot be executed

Execution command and machine language

I23	I22		I21	I20		I19	I18	I17	I16=0	I16=1
0	0	16*16	0	0	K*D	0	0	0	0+P	0+4P
0	1	16*32	0	1	K*X	0	0	1	Acc+P	Acc+4P
1	0	32*16	1	0	X*D	0	1	0	0−P	0−4P
1	1	32*32	1	1	X*X	0	1	1	Acc−P	Acc−4P
						1	0	0	0+R	0+4R
						1	0	1	Acc+R	Acc+4R
						1	1	0	|R|	|4R|
						1	1	1	Acc−R	Acc−4R ····· Acc Without latching



I9 I8 I7 I6 / I3 I2 I1 I0	X	
0 0 0 0	I1H	Serial I/O CH1
0 0 0 1	I1L	Input register
0 0 1 0	I2H	Serial I/O CH2
0 0 1 1	I2L	Input register
0 1 0 0	O1H	Serial I/O CH1
0 1 0 1	O1L	Output register
0 1 1 0	O2H	Serial I/O CH2
0 1 1 1	O2L	Output register
1 0 0 0	DIH	Delay I/O
1 0 0 1	DIL	Input register
1 0 1 0	BO1H	Barrel shifter output data
1 0 1 1	BO1L	a15 $\overline{a14}$ $\overline{a13}$ $\overline{a12}$ $\overline{a11}$ 0—0
1 1 0 0	BO2H	0 q3 q2 q1 q0 0—0
1 1 0 1	BO2L	0 0 q3 q2 q1 0—0
1 1 1 0	AH	ACC data output
1 1 1 1	AL	

I9 I8 I7 I6 / I3 I2 I1 I0	Y	
0 0 0 0	——	Assignment when transfer command is not to be given
0 0 0 1	——	
0 0 1 0	RH	R register
0 0 1 1	RL	
0 1 0 0	O1H	Serial I/O CH1
0 1 0 1	O1L	Output register
0 1 1 0	O2H	Serial I/O CH2
0 1 1 1	O2L	Output register
1 0 0 0	DOH	Delay I/O
1 0 0 1	DOL	Output register
1 0 1 0	BI1H	Positive value floating point type
1 0 1 1	BI1L	Arithmetic left shift
1 1 0 0	BI2H	Arithmetic right shift
1 1 0 1	(keep)	unused
1 1 1 0	(keep)	
1 1 1 1	(keep)	

I12 I11 I10	Flag
0 0 0	Zero
0 0 1	Non zero
0 1 0	Plus
0 1 1	Minus
1 0 0	Over flow
1 0 1	BSQ
1 1 0	(keep)
1 1 1	(keep)

I11 I10	J
0 0	none
0 1	LPJ
1 0	RTN
1 1	LPS

I12	S
0	LCS
1	LTS

I12	C/J
0	JAP
1	CAL

I11 I10 I5 I4	C (15≧C ≧0)
C_3 C_2 C_1 C_0	loop counter setting quantity

I11 I10 I9 I8 I5 I4 I3 I2 I1 I0	
a_5 a_4 a_3 a_2 a_1 a_0	Jump system address 0~63
a_1 a_0 a_5 a_4 a_3 a_2	
a_1 a_0 a_3 a_2 a_5 a_4	

K	I12 I11 I10 I9 I8 I7 I6	address
K_0(d)	1 R_5 R_4 R_3 R_2 R_1 R_0	0 to 63
K_0(r)	0 R_5 R_4 R_3 R_2 R_1 R_0	−32 to +31
K_4	R_3 R_2 R_1 R_0	−8 to +7
K_2	R_1 R_0	−2 to +1
K_+		+1

D	I12 I11 I10 I9 I8 I7 I6	address
D_0(d)	1 d_5 d_4 d_3 d_2 d_1 d_0	0 to 63
D_0(r)	0 d_5 d_4 d_3 d_2 d_1 d_0	−32 to +31
D_4	d_3 d_2 d_1 d_0	−8 to +7
D_2	d_1 d_0	−2 to +1
D_+		+1

Points on Execution Commands

Execution cycle

A command can be repeatedly executed from the command 0 address by means of the forced 0 address jump every Serial I/O sampling cycle.

Now, Assume that from the time 0 address has started, up until just before 0 address jump the number of cycles is N. [Cycle 0 to cycle (N-1)]

① Cycle 0 to cycle (N-3) ..... Normal cycle: Execution possible
② Cycle (N-2) ..... KSL cycle: with the exception of K-RAM access, execution possible
③ Cycle (N-1) ..... KSH cycle: Execution impossible (Any command will do)

* To provide time for K-RAM, I-RAM and the micro computer to interface ② and ③ are available.

The number of cycles N is given through the following formula, with fs for sampling frequency and fkck as cycle clock frequency.

$$\frac{fkck}{fs} - 1 < N < \frac{fkck}{fs} + 1 \quad \text{for } fkck = \frac{1}{2} f_{ACK} = \begin{cases} \frac{1}{2} f_{MCK1} \\ \frac{1}{2} f_{MCK2} \end{cases}$$

If fkck is a whole number N=fkck/fs=N1. Cycle 0 to cycle (N_1-1)
If fkck is not a whole number there are 2 cycle patterns

$$N = \begin{cases} N_1, \text{ Cycle 0 to Cycle } (N_1\text{-}1) \\ N_1+1, \text{ Cycle 0 to Cycle } N_1 \end{cases}$$

General expression	N	Cycle 0 to cycle (N-3) Normal cycle	Cycle (N-2) KSL cycle	Cycle (N-1) KSH cycle
fkck/fs whole number	$N=N_1$	Cycle 0 to cycle (N_1-3)	Cycle (N_1-2)	Cycle (N_1-1)
fkck/fs is not a whole number	$N=N_1$	Cycle 0 to cycle (N_1-3)	Cycle (N_1-2)	Cycle (N_1-1)
	N_1+1	Cycle 0 to cycle (N_1-2)	Cycle (N_1-1)	Cycle N_1

Therefore when fkck/fs is a whole number

① Cycle 0 to cycle (N_1-3)	Normal cycle:	Execution possible
② Cycle (N_1-2)	KSL cycle:	with the exception of K-RAM access, execution possible
③ Cycle (N_1-1)	KSH cycle:	Execution impossible (Any command will do)

Or when fkck/fs is not a whole number

A Cycle 0 to cycle (N_1-3)	: Execution always possible at normal cycle.
B cycle (N_1-2)	: Turns into normal cycle or KSL cycle. Execution possible with the exception of K-RAM
C cycle (N_1-1)	: Turns into KSL cycle or KSH cycle. A command that does not use transfer command. (In fact, execution impossible)
D cycle N_1	: Turns into KSH cycle or does not exist. Execution impossible (Any command will do)

Example 1) When fkck=6.144 MHz fs=48 KHz

$$\frac{fkck}{fs}=128 \qquad \therefore N=N_1=128 \text{ Cycle 0 to cycle 127}$$

$$\therefore \begin{cases} ① \text{ Cycle 0 to 125} \\ ② \text{ Cycle 126} \\ ③ \text{ Cycle 127} \end{cases}$$

Example 2) When fkck=6.144 MHz fs=44.1 KHz

$$\frac{fkck}{fs}=139.3... \qquad \therefore N=\begin{cases} N_1 = 139 \text{ cycle 0 to cycle 138} \\ N_1+1 = 140 \text{ cycle 0 to cycle 139} \end{cases}$$

$$\therefore \begin{cases} \text{A Cycle 0 to cycle 136} \\ \text{B Cycle 137} \\ \text{C Cycle 138} \\ \text{D Cycle 139} \end{cases}$$

Serial I/O and Register

(1) Serial I/O input register

The conditions for transfers with serial I/O input register as source or for cycle n without MPY are:

$$N-4\frac{1}{4} < n < N-2\frac{3}{4}+M$$ SIN delay from M ··· BCK falling edge

As $M=2\frac{3}{4}$ (KCK)

$$N-4\frac{1}{4} < n < N \quad \therefore N-4 \leq n \leq N-1$$

- $\frac{fKCK}{fS}$ = for whole number $n = \{N-4 \leq n \leq N-1\} = \{N_1-4 \leq n \leq N_1-1\}$

Cycle 0 to cycle (N_1-5)	Serial input data transferred to the previous sampling space is in this space register and can be handled freely.
Cycle (N_1-4) to cycle (N_1-1)	In this space usage of serial I/O input register is prohibited.

* In certain cases cycle (N_1-2) can be used. Check when necessary.

- $\frac{fKCK}{fS}$ = for whole number $n = \{N-4 \leq n \leq N-1\} = \{N_1-4 \leq n \leq N_1\}$

Cycle 0 to cycle (N_1-5)	Serial input data transferred to the previous sampling space is in this space register and can be handled freely.
Cycle (N_1-4) to cycle N_1	In this space usage of serial I/O input register is prohibited.

(2) Serial I/O output register

Cycle n conditions for transfers that can not be executed with serial I/O output register as destination

$$N-4\frac{1}{4}+\frac{fKCK}{fB}-M<n<N-2\frac{3}{4}+\frac{fKCK}{fB}$$ fB ... bit clock frequency

M is a delay margin to be ignored here $N-4\frac{1}{4}+\frac{fKCK}{fB} < n < N-2\frac{3}{4}+\frac{fKCK}{fB}$

24 bit clock system

$$N-4\frac{1}{4}+\frac{1}{48}\frac{fKCK}{fS} < n < N-2\frac{3}{4}+\frac{1}{48}\frac{fKCK}{fS}$$

32 bit clock system

$$N-4\frac{1}{4}+\frac{1}{64}\frac{fKCK}{fS} < n < N-2\frac{3}{4}+\frac{1}{64}\frac{fKCK}{fS}$$

* As no margin is taken for the left side, in certain cases prohibited cycles are not included. Check when necessary.

Example 1) fKCK=6.44 MHz fs=48 KHz N=N1=128 (Cycle 0 to cycle 127)

Serial I/O input register $n = \{N_1-4 \leq n \leq N_1-1\} = \{124 \leq n \leq 127\}$

$\therefore$ { Cycle 0 to cycle 123 ..... usable
Cycle 124 to cycle 127 ..... unusable

Serial I/O output register 24 clock system $N-4\frac{1}{4}+\frac{1}{48}128<n<N-2\frac{3}{4}+\frac{1}{48}128$

$$N-1\frac{7}{12}<n<N-\frac{1}{12}$$

$$N-1 \leq n \leq N-1$$

$n=N-1=N_1-1=127$

$\therefore$ { Cycle 0 to cycle 126 ..... usable
Cycle 127 ..... unusable

Serial I/O output register 32 clock system $N-4\frac{1}{4}+\frac{1}{64}128<n<N-2\frac{3}{4}+\frac{1}{64}128$

$$N-2\frac{1}{4}<n<N-\frac{3}{4}$$

$$N-2 \leq n \leq N-1$$

$n = \{N-2 \leq n \leq N-1\} = \{N_1-2 \leq n \leq N_1-1\} = \{126 \leq n \leq 127\}$

$\therefore$ { Cycle 0 to cycle 125 ..... usable
Cycle 126 to cycle 127 ..... unusable

Example 2) f_{KCK}=6.144 MHz fs=44.1 KHz $N = \begin{cases} N_1 = 139 \text{ (Cycle 0 to cycle 138)} \\ N_1+1 = 140 \text{ (Cycle 0 to cycle 139)} \end{cases}$

Serial I/O input register $n = \{N_1-4 \leq n \leq N_1\} - \{135 \leq n \leq 139\}$

$\therefore$ { Cycle 0 to cycle 134 ..... usable
Cycle 135 to cycle 139 ..... unusable

Serial I/O output register 24 clock system $N-4\frac{1}{4} + \frac{1}{48}(139.3...) < n < N-2\frac{3}{4} + \frac{1}{48}(139.3...)$

$N-1.3... < n < N+0.1...$

$n = \{N-1, 0\} = \{N_1-1, N_1, 0\} = \{138, 139, 0\}$

$\therefore$ { Cycle 1 to cycle 137 ..... usable
Cycle 137, 139, cycle 0 ..... unusable

Serial I/O output register 32 clock system $N-4\frac{1}{4} + \frac{1}{64}(139.3...) < n < N-2\frac{3}{4} + \frac{1}{64}(139.3...)$

$N-2.0... < n < N-0.5...$

$N-2 \leq n \leq N-1$

$n = \{N-2, N-1\} = \{N_1-2, N_1-1, N_1\} = \{137, 138, 139\}$

$\therefore$ { Cycle 0 to cycle 136 ..... usable
Cycle 137 to cycle 139 ..... unusable

Delay I/O (Serial mode) and register

(1) Delay I/O input register

Delay I/O input register is input twice during 1 sampling period. For one of those 2 instances the timing is the same as for serial I/O. For the other instance the conditions for the transfer with this register as source or the cycle n when MPY cannot be executed are:

$$\frac{1}{2}\frac{f_{KCK}}{fS} - 4\frac{1}{4} < n < \frac{1}{2}\frac{f_{KCK}}{fS} - 2\frac{3}{4} + M$$

as $M = \frac{1}{2}\{KCK\}$

$$\frac{1}{2}\frac{f_{KCK}}{fS} - 4\frac{1}{4} < n < \frac{1}{2}\frac{f_{KCK}}{fS} - 2\frac{1}{4}$$

accordingly $n_2 = \{\max n : n < \frac{1}{2}\frac{f_{KCK}}{fS} - 4\frac{1}{4}\}$

Cycle 0 to cycle n_2	data transferred during LRCK L level of the previous sampling level is in the register and can be handled freely.
Cycle (n_2+1), cycle (N_2+2)	Usage prohibit cycle
Cycle (n_2+3) to cycle (N_1-5).....	data transferred during LRCK H level of the present sampling period is in the register and can be handled freely
Cycle (N_1-4) to cycle (N_1-1)	Usage prohibit cycle

*In certain cases cycle (n_2+3) also becomes usage prohibit cycle. Please check when necessary.

(2) Delay I/O output register

Delay I/O output register outputs twice during 1 sampling period. For one of those 2 instances the timing is the same as for serial I/O. For the other instance, the conditions for cycle n where transfer with this register as destination can not be executed are

$$\frac{1}{2}\frac{fKCK}{fS}-4\frac{1}{4}+\frac{fKCK}{fB}-M<n<\frac{1}{2}\frac{fKCK}{fS}-2\frac{3}{4}+\frac{fKCK}{fB}$$

as M=0 [KCK]

$$\frac{1}{2}\frac{fKCK}{fS}-4\frac{1}{4}+\frac{fKCK}{fB}<n\frac{1}{2}\frac{fKCK}{fS}-2\frac{3}{4}+\frac{fKCK}{fB}$$

24 bit clock system

$$\frac{25}{48}\frac{fKCK}{fS}-4\frac{1}{4}<n<\frac{25}{48}\frac{fKCK}{fS}-2\frac{3}{4}$$

32 bit clock system

$$\frac{33}{64}\frac{fKCK}{fS}-4\frac{1}{4}<n<\frac{33}{64}\frac{fKCK}{fS}-2\frac{3}{4}$$

*In certain cases, as the left side margin is not included, cycles that become prohibited are not included. Please check when necessary.

Example 1) f_{KCK}=6.144 MHz f_S=48 kHz $N-N_1=128$ (Cycle 0 to cycle 127)

Delay I/O input register $n_2<\frac{1}{2}\ 128-4\frac{1}{4}=60-\frac{1}{4}$ $\therefore n_2=59$

$\therefore$
- Cycle 0 to cycle 59 ..... usable
- Cycle 60 to cycle 61 ..... unusable
- Cycle 62 to cycle 123 ..... usable
- Cycle 124 to cycle 127 ..... unusable

Delay I/O output register 24 clock system $\frac{25}{48}\ 128-4\frac{1}{4}<n<\frac{25}{48}\ 128-2\frac{3}{4}$

$$62\frac{5}{12}<n<63\frac{11}{12}$$

N=63

$\therefore$
- Cycle 0 to cycle 62 ..... usable
- Cycle 63 ..... unusable
- Cycle 64 to cycle 126 ..... usable
- Cycle 127 ..... unusable

Delay I/O output register 32 clock system $\frac{33}{64}128-4\frac{1}{4} < n < \frac{33}{64}128-2\frac{3}{4}$

$$61\frac{3}{4} < n < 63\frac{1}{4} \qquad n = \{62, 63\}$$

$\therefore$
- Cycle 0 to cycle 61 ..... usable
- Cycle 62 to cycle 63 ..... unusable
- Cycle 64 to cycle 125 ..... usable
- Cycle 126 to cycle 127 ..... unusable

Example 2) f_{KCK}=6.144 MHz fs=44.1 KHz N= N_1 =139 (Cycle 0 to cycle 138)
N_1+1 =140 (Cycle 0 to cycle 139)

Delay I/O input register $n_2 < \frac{1}{2}139.3\ldots - 4\frac{1}{4} = 65.4\ldots \quad \therefore n=65$

$\therefore$
- Cycle 0 to cycle 65 ..... usable
- Cycle 66 to cycle 67 ..... unusable
- Cycle 68 to cycle 134 ..... usable
- Cycle 135 to cycle 139 ..... usable

Delay I/O output register 24 clock system $\frac{25}{48}139.3\ldots - 4\frac{1}{4} < n < \frac{25}{48}139.3\ldots - 2\frac{3}{4}$

$$68.3\ldots < n < 69.8\ldots \qquad n=69$$

- Cycle 1 to cycle 68 ..... usable
- Cycle 69 ..... unusable
- Cycle 70 to cycle 137 ..... usable
- Cycle 138 to cycle 0 ..... unusable

Delay I/O output register 32 clock system $\frac{33}{64}139.3\ldots - 4\frac{1}{4} < n < \frac{33}{64}139.3\ldots - 2\frac{3}{4}$

$$67.5\ldots < n < 69.0\ldots \qquad n = \{68, 69\}$$

- Cycle 0 to cycle 67 ..... usable
- Cycle 68 to cycle 69 ..... unusable
- Cycle 70 to cycle 136 ..... usable
- Cycle 137 to cycle 139 ..... unusable

Delay I/O (delay mode) and register

(1) 32 bit delay mode
32 bit Conditions where delay mode can be realized

$$fS \leq \frac{1}{136} fKCK \quad \text{that is} \quad N_1 \geq 136$$

The relation between data to write in DO register and data to read from DI register is.

- DO register
  - Cycle 0 to cycle 66 : data written last in this period is set as CH1 (n)
  - Cycle 67 : write prohibit
  - Cycle 68 to cycle (N_1-2) : data written last in this period is set as CH2 (n)
  - Cycle (N_1-1), (N_1) : write prohibit

- DI register
  - Previous cycle 134 to cycle (N_1-2), cycle 0 to cycle 65 : In this period CH1 data (n-r) can read
  - Cycle 62 to cycle 125 : In this period CH2 data (n-r) can read.
  - Cycle (N_1-1), (N_1) : read prohibit

(2) 30 bit delay mode
30 bit Conditions where delay mode can be realized

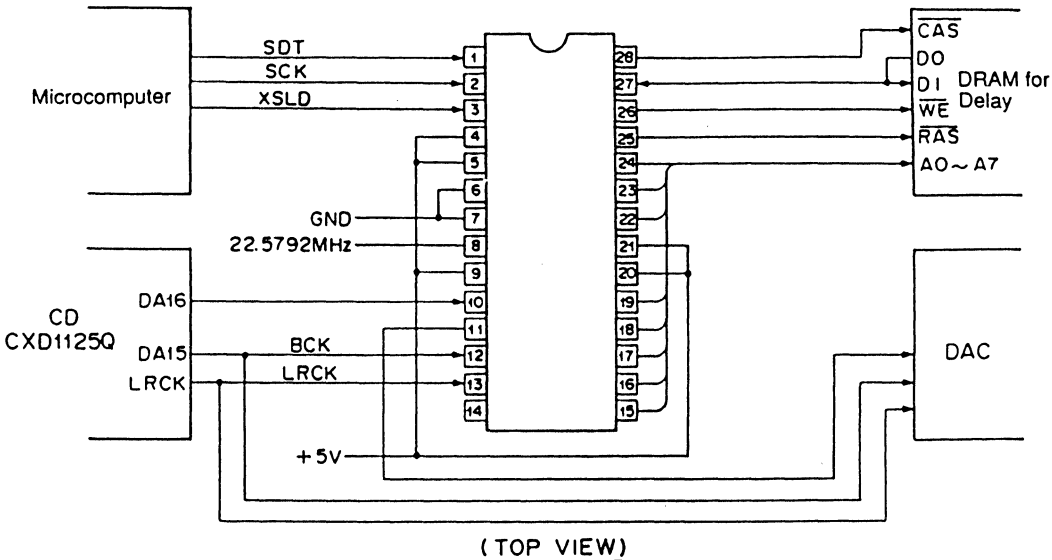
$$fS \leq \frac{1}{128} fKCK \quad \text{that is} \quad N_1 \geq 128$$

The relation between data to write in DO register and data to read from DI register is.

- DO register
  - Cycle 0 to cycle 62 : data written last in this period is set as CH1 (n)
  - Cycle 63 : write prohibit
  - Cycle 64 to cycle (N_1-2) : data written last in this period is set as CH2 (n)
  - Cycle (N_1-1), (N_1) : write prohibit

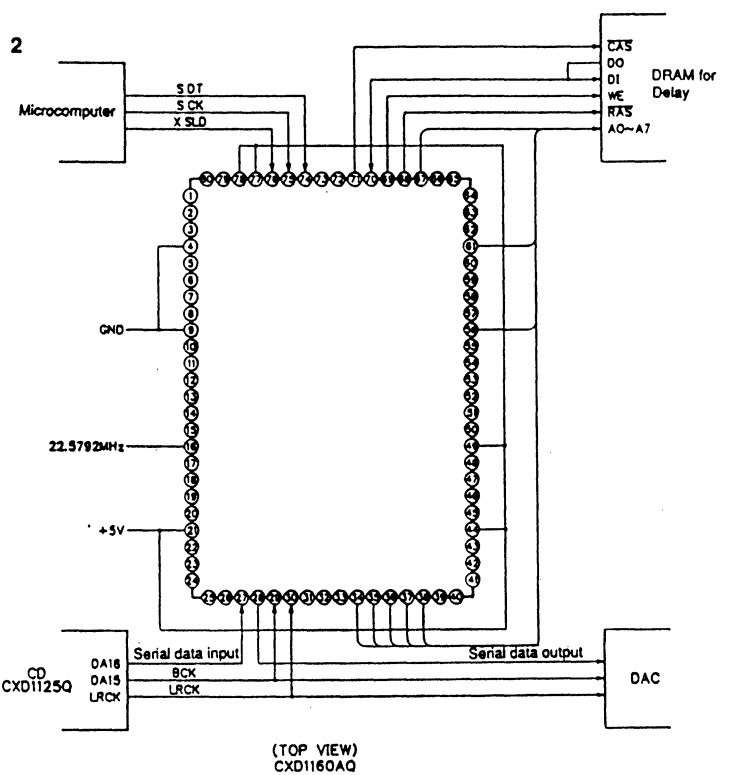
- DI register
  - Previous cycle 126 to cycle (N_1-2), cycle 0 to cycle 61 : In this period CH1 data (n-r) can read
  - Cycle 62 to cycle 125 : In this period CH2 data (n-r) can read.
  - Cycle (N_1-1), (N_1) : read prohibit

Application example 1



(TOP VIEW)

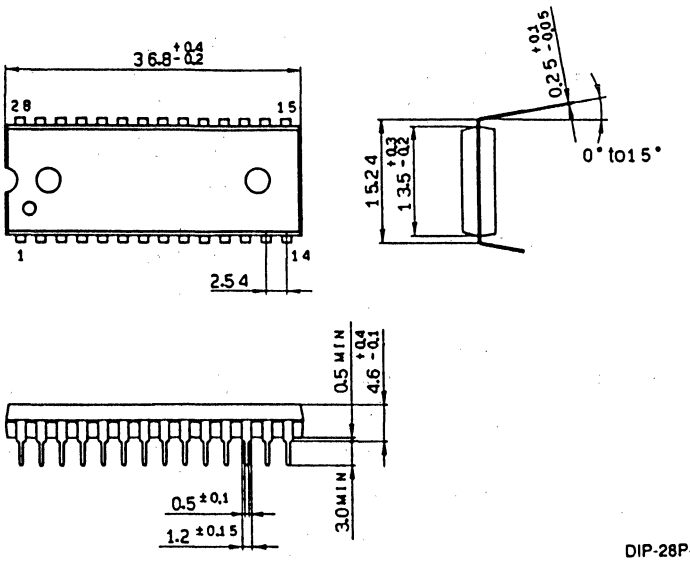
Application example 2



(TOP VIEW)
CXD1160AQ

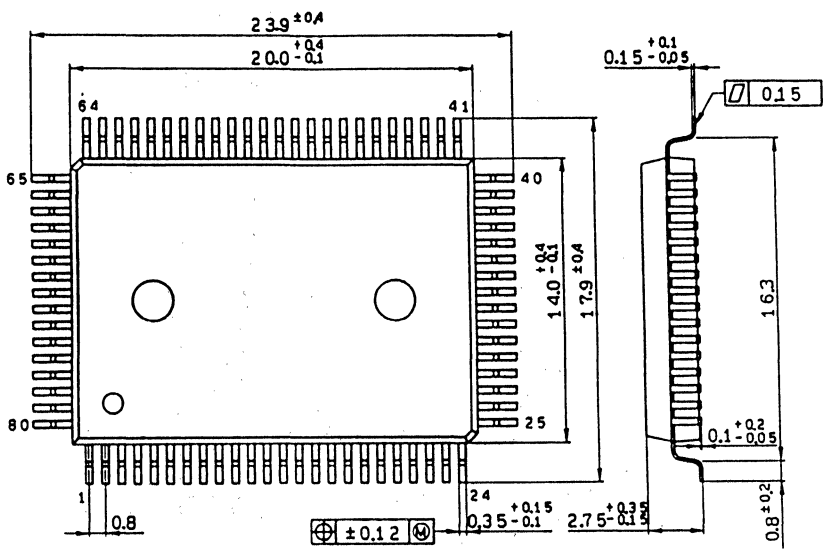
Package Outline Unit: mm

CXD1160AP 28pin DIP (Plastic) 600 mil 4.2 g



DIP-28P-04

CXD1160AQ 80pin QFP (Plastic) 1.6 g



QFP-80P-L01

SONY® CXD1244S

Digital Filter for CD Player

Description

CXD1244S is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Built-in 4-times/8-times sampling digital filter for 2 channels.
- Ripple within 0.00001dB
- Attenuation within -100dB(24.1k).
- Noise shaping, Attenuator
- Soft muting, de-emphasis and a wide variety of built-in functions.

Application

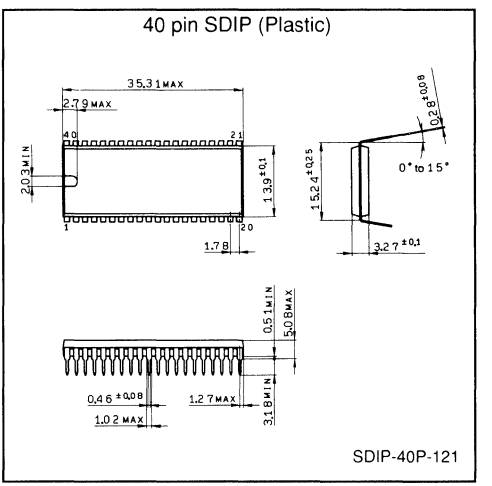
Compact disc player

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

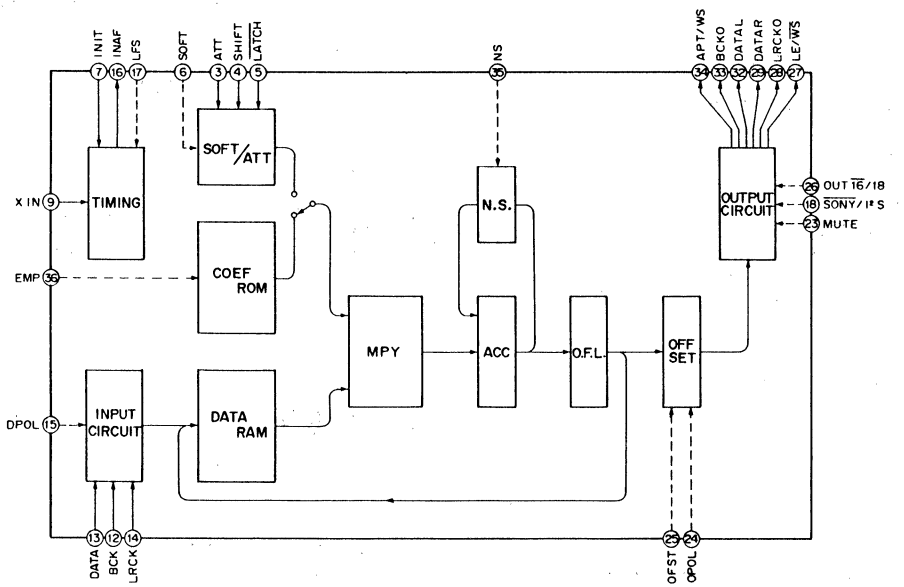
• Supply voltage	V_{DD}	-0.5	to	+6.5	V	
• Input voltage	V_I	-0.5	to	V_{DD} +0.5	V	
• Storage temperature	Tstg	-55	to	+150	°C	
• Allowable power dissipation	P_D			500	mW	(Ta=60°C)

Recommended Operating Conditions

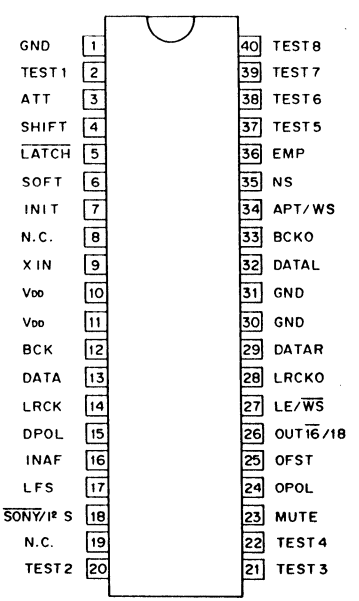
• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	-10	to	+60	°C
• OSC frequency	fx	12.0	to	18.5	MHz

81114-YA

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	
2	TEST1	I	Test pin (Normally fixed to "L" level)
3	ATT	I	Attenuate data input
4	SHIFT	I	Attenuate data shift clock input
5	LATCH	I	Attenuate data latch clock input
6	SOFT	I	Soft muting ON/OFF active at "H".
7	INIT	I	Synchronous again with the rising edge of this signal.
8	NC		
9	XIN	I	Master CLK input (f=384 Fs)
10, 11	V_{DD}	—	Supply (+5V)
12	BCK	I	BCK input
13	DATA	I	Serial data input (2's complement)
14	LRCK	I	LRCK input
15	DPOL	I	Output data polarity "L" : non inversion "H" : inversion.
16	INAF	O	When I/O sync is missed "H" is output.
17	LFS	I	4Fs mode ON/OFF available at "H" only during I^2S.
18	SONY/I^2S	I	Output format specified at "L": Sony, at "H": I^2S
19	NC	I	
20 to 22	TEST 2 to 4	I	Test pin (Normally fixed to 'L' level)
23	MUTE	I	Turns output to 0 or offset value. Active at 'H'.
24	DPOL	I	Offset polarity 'L': (–) 'H': (+)
25	OFST	I	Offset ON/OFF Active at 'H'
26	OUT16/18	I	Output data word length specified at 'L': 16 bit at 'H': 18 bit
27	LE/WS	O	LE output (Sony format)/WS output (I^2S format)
28	LRCKO	O	LRCKO output
29	DATAR	O	Rch serial data output (2's complement)
30, 31	GND	—	
32	DATAL	O	Lch serial data output (2's complement)
33	BCKO	O	BCKO output
34	APT/WS	O	APT output (Sony format)/WS output (I^2S format)
35	NS	I	Noise shaping ON/OFF Active at 'H'
36	EMP	I	Deemphasis ON/OFF Active at 'H'
37 to 40	TEST 5 to 8	I	Test pin (Normally fixed to 'L' level)

Electrical Characteristics
DC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
'H' input voltage (Except Shift, Latch)	V_{IH}	—	0.76 V_{DD}			V
'H' input voltage (Shift, Latch)						
'L' input voltage (Except Shift, Latch)	V_{IL}	—			0.24 V_{DD}	V
'L' input voltage (Shift, Latch)						
Input leak voltage	I_{LI}	—			±5	μA
'H' output voltage	V_{OH}	Io=-2mA	V_{DD}-0.5			V
'L' output voltage	V_{OL}	Io= 2mA			0.4	V

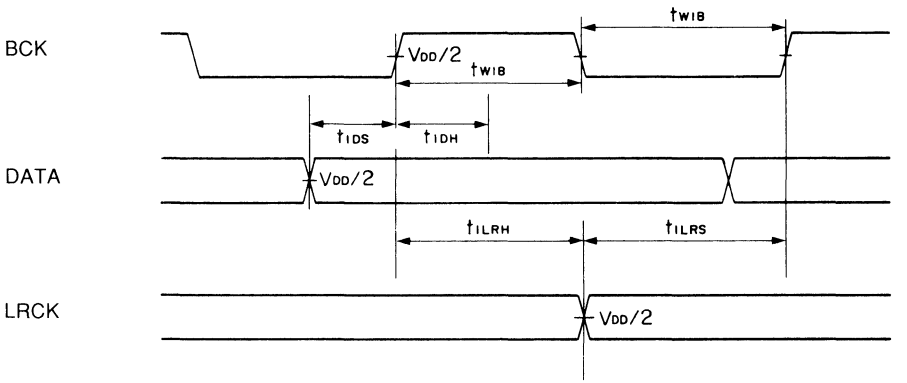
AC characteristics

Item	Symbol	Conditions	Min.	Typ.	Min.	Unit
OSC frequency	Fx		12.0	16.9	18.5	MHz
Input BCK frequency	F_{BCX}				2.31	MHz
Input BCK pulse width	t_{WIB}	Defined at Duty	40*	50	60	%
Input data set up time	t_{IDS}		20			ns
Input data hold time	t_{IDH}		20			ns
Input LRCK set up time	t_{ILRS}		50			ns
Input LRCK hold time	t_{ILRH}		50			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		25			ns
Output data hold time	t_{ODH}		25			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I^2S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		35			ns
Output data hold time	t_{ODH}		35			ns
Output BCK pulse width	t_{WOB}	Fx=18.5MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		20			ns
Output data hold time	t_{ODH}		20			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I^2S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		32			ns
Output data hold time	t_{ODH}		32			ns
Output signal Rise/Fall time	t_R, t_F	CL=50pF			30	ns

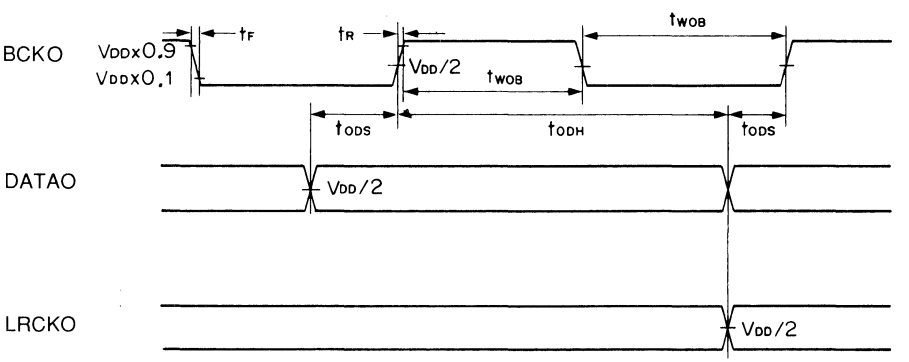
Note) Duty defined at 1/2 VDD, see the Timing Chart.

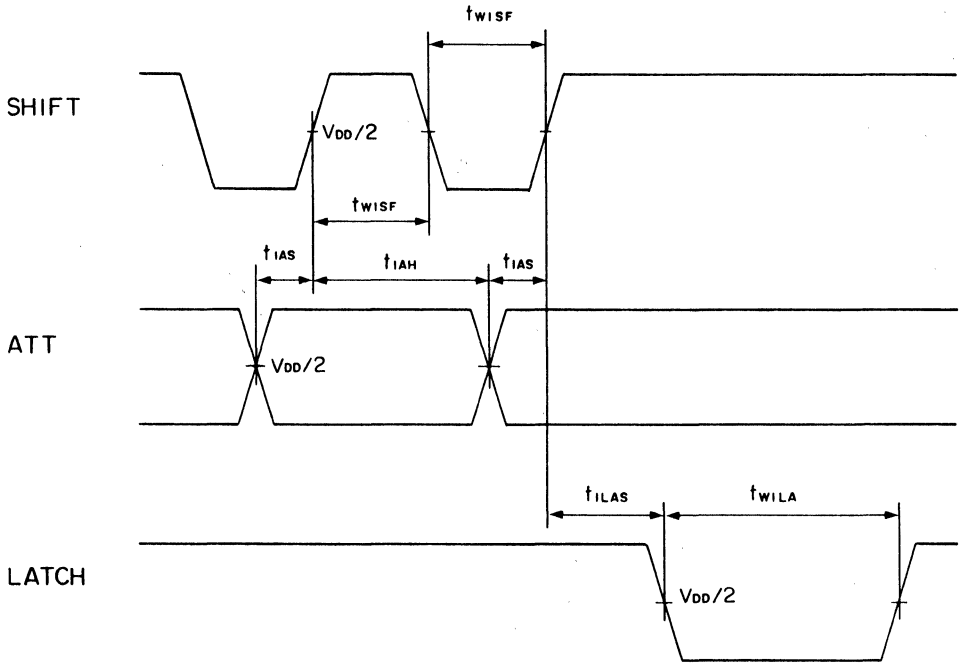
Timing Chart

- Input



- Output





Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift pulse width	T_{WISF}		600			ns
ATT set up time	T_{IAS}		300			ns
ATT hold time	T_{IAH}		600			ns
Latch pulse width	T_{WILA}		400			ns
Latch set up time	T_{ILAS}		500			ns

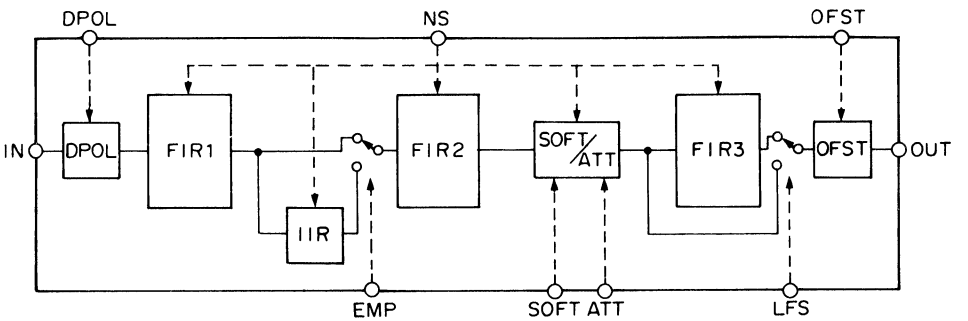
Schmitt input characteristics (SHIFT, LATCH)

	Min.	Typ.	Max.	Unit
V_{T+}	0.54×V_{DD}	3.0	0.76×V_{DD}	V
V_{T-}	0.24×V_{DD}	2.0	0.43×V_{DD}	V
HYST	0.52	1.0	———	V

Functions

Conceptual block diagram

An outline block diagram of this LSI is shown below.

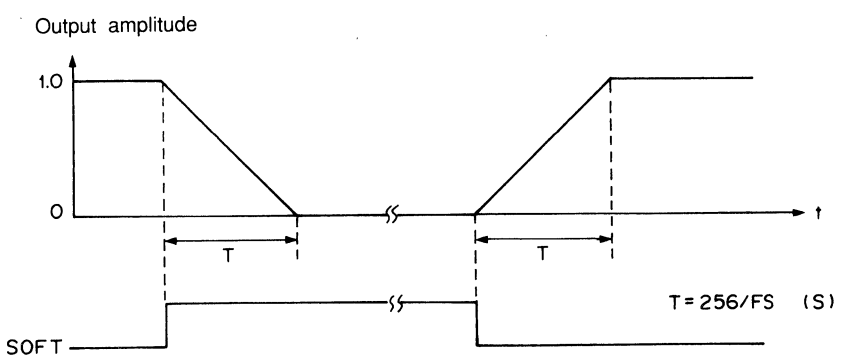


1. Noise shaping

For respective outputs FIR 1 to 3, IIR, SOFT/ATT figures are usually rounded off. However, by turning NS to "H" noise shaping can be applied.
NS register is cleared when INIT is at "L" or NS at "L".

2. Soft muting

By turning SOFT to "H"/"L", data can be smoothly muted or demuted.



3. Digital attenuator

Can attenuate output data by means of transfer data from an external microcomputer.

1) Command and Audio output
Attenuate data is in 12 bit and can be set in 1024 steps.
The relationship between command and output is shown in the chart below.

Attenuate data	Audio output
400 (H)	0 dB
3FF (H) 3FE (H) ⋮ 001 (H)	−0.0085 dB −0.017 dB ⋮ −60.206 dB
000 (H)	−∞

The attenuate value from 001 (H) to 3FF (H) can be obtained through the following formula.

$$ATT=20\log\left[\frac{\text{Input data}}{1024}\right]\text{dB}$$

Example: Attenuate data for 3FA (H)

$$ATT=20\log\left[\frac{1018}{1024}\right]\text{dB}=-0.051\text{ dB}$$

2) Attenuator operation
Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that ATT1>ATT3> ATT2 and that the place of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before. The value of ATT2 is reached (during the state of A in Fig.1),the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of softmuting.

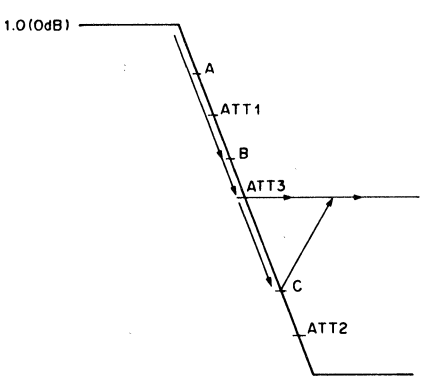
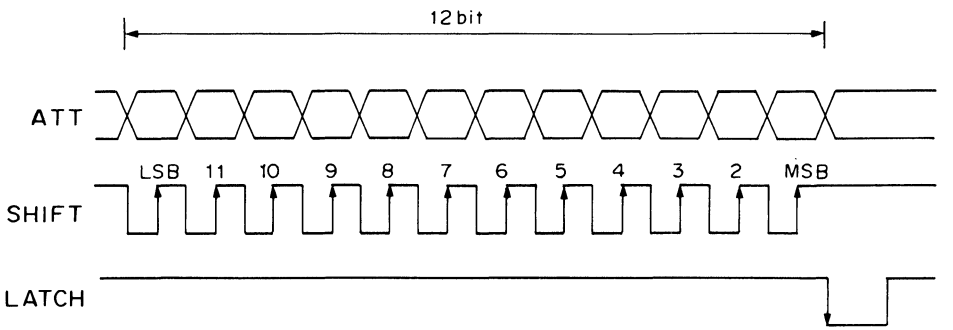
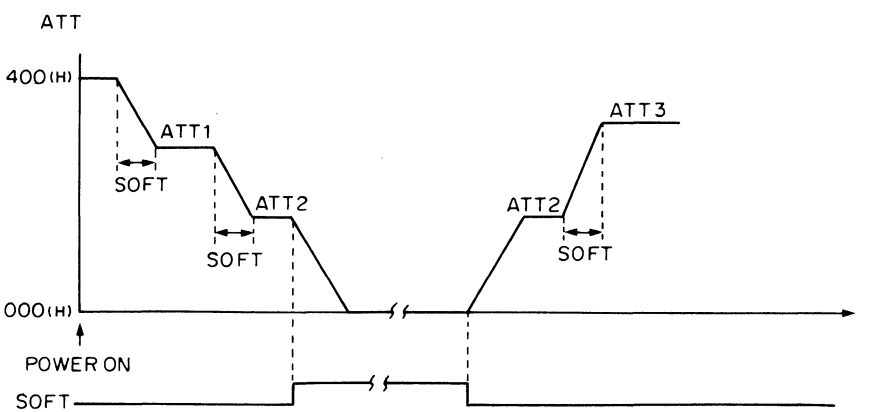


Fig.1 Transition from one attenuator value to another

3) Input data timing
Attenuate function can be activated by means of ATT, Shift and Latch.
Transfer format is indicated as follows.



(1) ATT data is a 12 bit word length and LSB first transfer ATT data is available 000(H) to 400(H).
(2) When Latch is at "L", ATT cannot be transferred.
(3) With INIT at ƒ, 400 (H) is set as ATT data.



- The transition from ATT1 to ATT2 takes place in soft muting operation.
- During attenuate operation SOFT is set to either ON or OFF, it turns back to the original ATT data.
- When ATT data =400 (H) Noise shaping is not applied regardless of NS ON or OFF.
  When ATT data =400 (H) Noise shaping is applied regardless of NS ON or OFF.

4. Digital deemphasis
By turning EMP to "H", deemphasis can be applied by means of IIR filter.
Time constant of de-emphasis are τ_1=50μs and τ_2=15μs at f_s=44.1kHz.

5. Offset

Offset can be applied to the output data by means of OFST and OPOL.
Pos/Neg selection of the offset value is possible as indicated in the following chart.

OFST	OPOL	OUT $\overline{16}$/18	Offset value
L	×	L	0000 (H)
L	×	H	00000 (H)
H	H	L	02AA (H)
H	H	H	02AA8 (H)
H	L	L	FD55 (H)
H	L	H	FD554 (H)

6. Muting

By turning MUTE to "H" or INIT to "L", the output can be muted. Then, the offset value set at the offset is output. When INIT is at "L", 0 data is input to this LSI.

7. Data polarity

Inversion and non inversion of the output data can be selected by means of DPOL.
When DPOL is at "H", non inversion.
when DPOL is at "L", inversion.

8. I/O synchronizing circuit

1) Principle

A window featuring 10 internal system clocks (XIN/2) is set. The sync circuit observes whether the rising edge (LRCK ƒ) of LRCK that is input, has entered the window or not. When the power supply is turned on, should LRCK ƒ be out of the window the sync circuit stops the internal processing in timing with the center of the window. Synchronously with the appearance of the next LRCK ƒ the processing is started. Through this operation synchronization between the exterior system and this LSI is established.

2) Resynchronization by means of INIT

Even when LRCK ƒ is inside the window but located close to one of the 2 edges of the window, the sync may miss with the mingling of external noise or other Re sync operation. To this effect it is necessary to apply resync, without fault, after supply is turned on. ReSync operation is executed with the INIT ƒ timing. Sync. circuit is initialized and LRCK is located in the center of the window.
Moreover, when the sync falls out of the window, INAF output turns to "H" level.

3) Non synchronous MUTE

When INAF is at H, 0 data is output regardless of offset ON/OFF.

9. Output format

The output format of this LSI can be selected as shown in the chart below.

	8Fs		4Fs
	SONY	I²S	I²S
(Control pin)			
$\overline{\text{SONY}}$/I2S	'L'	'H'	←
LEFS	no effect	'L'	'H'
OUT$\overline{16}$/18	At will	no effect	←
(Output pin)			
LRCKO	8LRCK	4LRCK	←
BCKO	24BCK	16BCK	←
DATAL	DATAL	Staggered	MIX data
DATAR	DATAR	DATA	'L'
APT/WS	APT	WS	←
LE/$\overline{\text{WS}}$	LE	$\overline{\text{WS}}$	←

10. I/O signal latch timing

1) Input

DPOL, SOFT, MUTE, OFST, OPOL, INIT, $\overline{\text{SONY}}$/I²S, LFS, OUT$\overline{16}$/18, NS, EMP

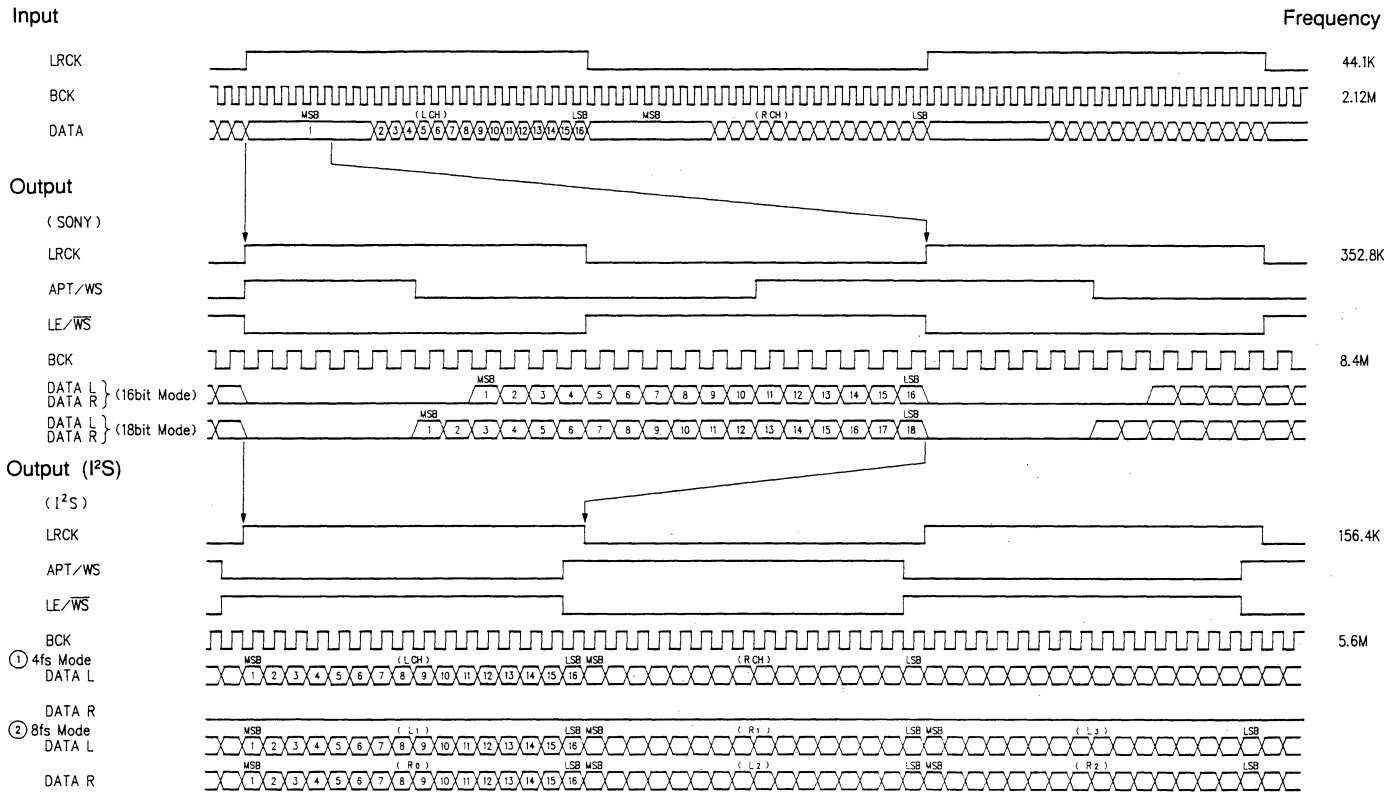
The above indicated input signals are latched by means of internal clocks equivalent to LRCK.

2) Output

LRCKO, DATAL, DATAR, APT.WS, LE/$\overline{\text{WS}}$

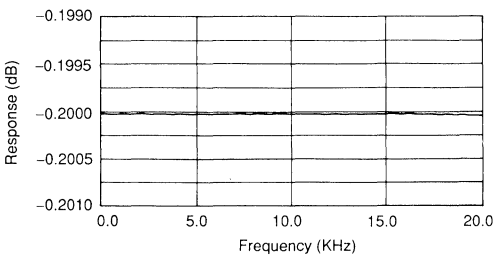
The above indicated output signals are latched by means of internal clocks equivalent to BCKO.

I/O Timing Chart

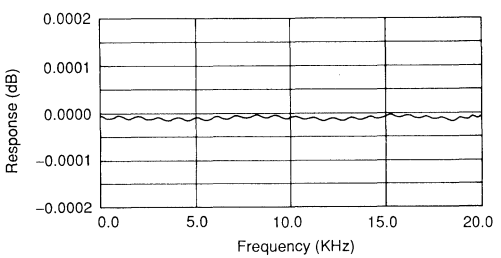


Filter characteristics (for 4Fs)

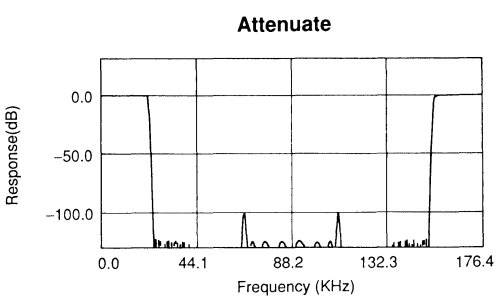
Frequency characteristics



Ripple characteristics

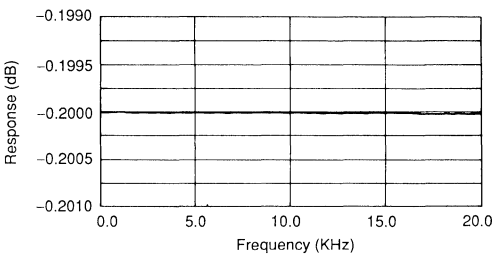


Attenuate

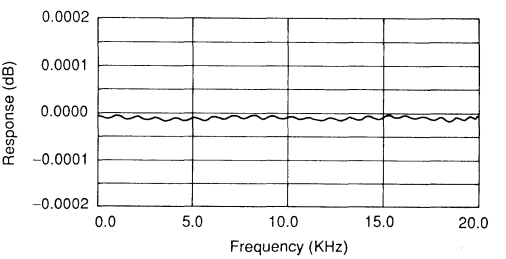


Filter characteristics (for 8Fs)

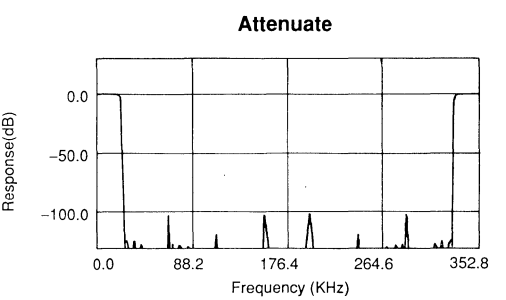
Frequency characteristics



Ripple characteristics



Attenuate



SONY

CXD2552Q

Pulse D/A Converter *

Description

The CXD2552Q is a pulse D/A converter developed for digital audio products; compact disc player and others.

44 pin QFP (Plastic)

Features

- PLM pulse converter
- 3rd order noise shaper
- Direct digital sync
- Master clock 1024Fs
- 2 channel built in

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +6.5 V
- Input voltage V_I −0.3 to V_{DD}+0.3 V
- Allowable power dissipation
  P_D 500 mW (Ta=60°C)
- Storage temperature
  Tstg −55 to +150 °C

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25 V
- Operating temperature Topr −10 to 60 °C
- OSC frequency fx 32.0 to 49.7 MHz
- Supply voltage difference
  V_{DD}–V_{DD2}, V_{DD}–DV_{DD}, V_{DD}–XV_{DD} ± 0.1V
  V_{SS}–V_{SS2}, V_{SS}–DV_{SS}, V_{SS}–XV_{SS} ± 0.1V

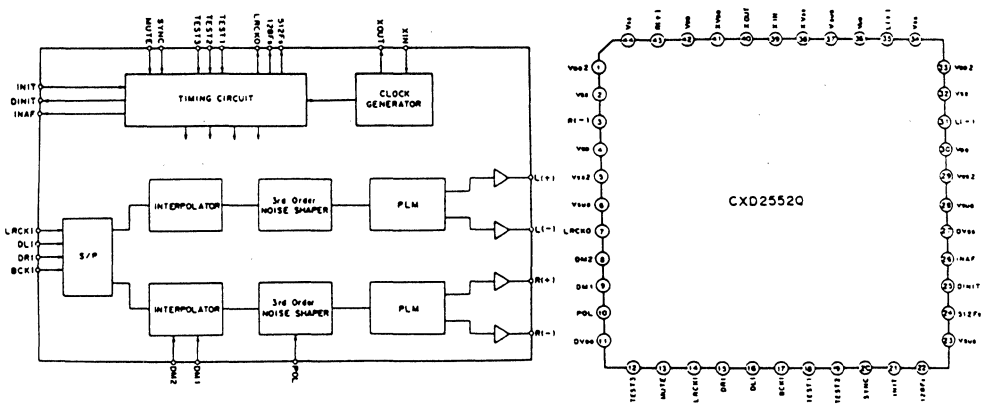
Structure

Silicon gate CMOS IC

Applications

Compact disc player, digital amplifier, BS tuner

Block Diagram and Pin Configuration



* Sony Corporation developed the Pulse D/A converter and designed the LSI circuitry that incorporates the Multi-Stage Noise Shaping technique originated by NTT (Nippon Telegraph and Telephone Corporation).

E89858 – ST

Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD2}	—	Analog power supply
2	Vss	—	Analog GND
3	R (–)	O	Rch PLM output (Opposite phase)
4	V_{DD}	—	Analog power supply
5	V_{SS2}	—	Analog GND
6	V_{SUB}	—	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV_{DD}	—	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin.Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V_{SUB}	—	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DVss	—	Digital GND
28	V_{SUB}	—	Sub straight. Connect to GND.
29	V_{SS2}	—	Analog GND
30	V_{DD}	—	Analog power supply
31	L (–)	O	Lch PLM output (Opposite phase)
32	Vss	—	Analog GND
33	V_{DD2}	—	Analog power supply
34	Vss	—	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V_{DD}	—	Analog power supply
37	V_{SUB}	—	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	——	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XV_{DD}	——	Clock power supply
42	V_{DD}	——	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	Vss	——	Analog GND

Electrical Characteristics

DC Characteristics

(V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V ± 5%, Vss=V_{SS2}=DVss=XVss=0V, Topr=−10 to 60°C)

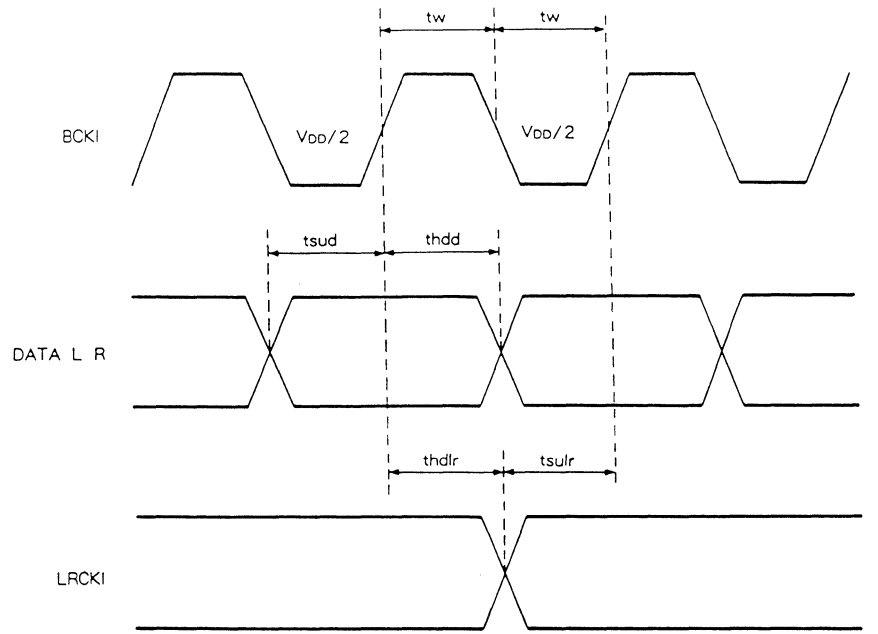
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	——	0.76V_{DD}			V
"L" input voltage	V_{IL}	——			0.24V_{DD}	V
Input leak current	I_{LI}	——			± 5.0	μA
"H" output voltage (DINIT, INAF)	V_{OH}	I_O=−1mA	V_{DD}−0.5			V
"L" output voltage (DINIT, INAF)	V_{OL}	I_O=1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V_{OH}	I_O=−0.4mA	V_{DD}−0.5			V
"L" output voltage(512Fs, LRCKO)	V_{OL}	I_O=0.4mA			0.4	V
"H" output voltage (128Fs)	V_{OH}	I_O=−0.3mA	V_{DD}−0.5			V
"L" output voltage (128Fs)	V_{OL}	I_O=0.3mA			0.4	V
"H" output voltage (R+, R−, L+, L−)	V_{OH}	I_O=−15mA	V_{DD}−0.5			V
"L" output voltage (R+, R−, L+, L−)	V_{OL}	I_O=15mA			0.5	V
"H" output voltage (XOUT)	V_{OH}	I_O=−2.0mA	V_{DD}−0.5			V
"L" output voltage (XOUT)	V_{OL}	I_O=2.0mA			0.4	V
Current consumption	I_{DD}	——		55	80	mA

AC Characteristics

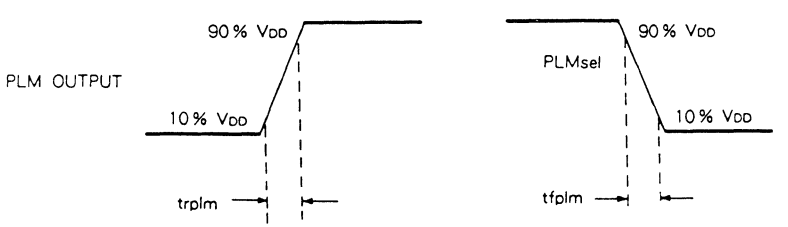
(V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V ± 5%, Vss=V_{SS2}=DVss=XVss=0V, Topr=−10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw		38			nsec
DATAL, R set up time	tsud		18			nsec
DATAL, R hold time	thdd		18			nsec
LRCKI set up time	tsulr		18			nsec
LRCKI hold time	thdlr		18			nsec
PLM output rise/fall time	tr, tf	CL=300pF		10		nsec

• Input



• Output



Analog Characteristics (V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V, V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V, Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	1kHz, 0dB/– ∞ dB data (Fs=44.1kHz) (A filte used)	96			dB

Electrical Characteristics Testing Method

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

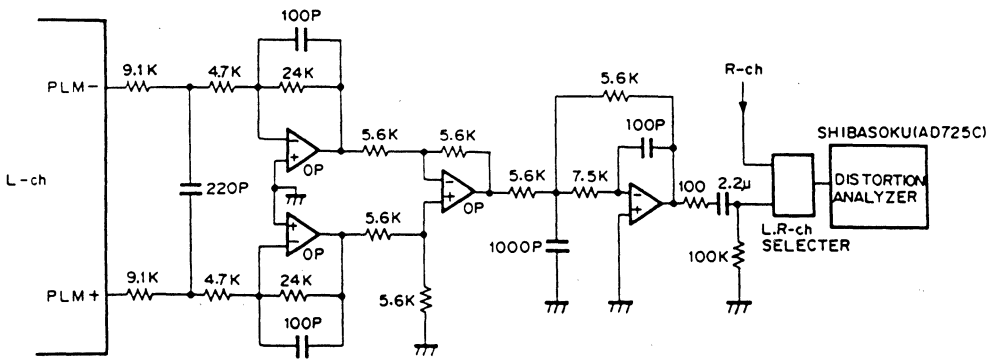


Fig. 1.

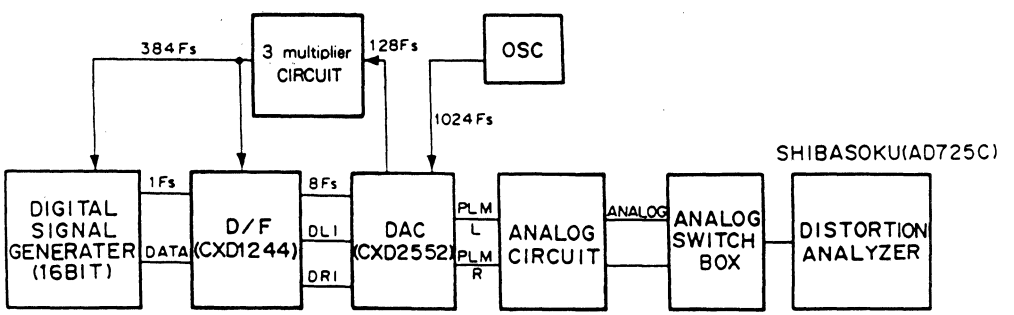


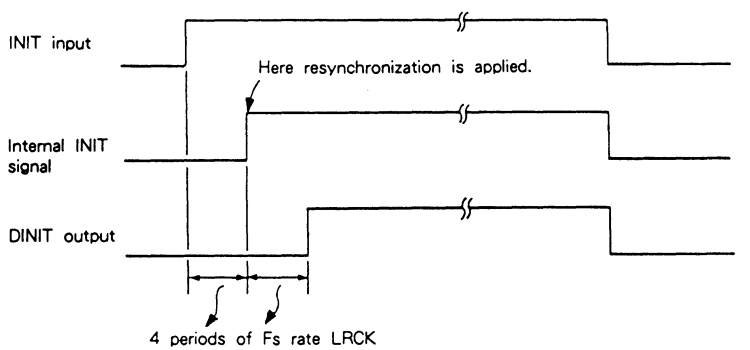
Fig. 2.

Description of Function

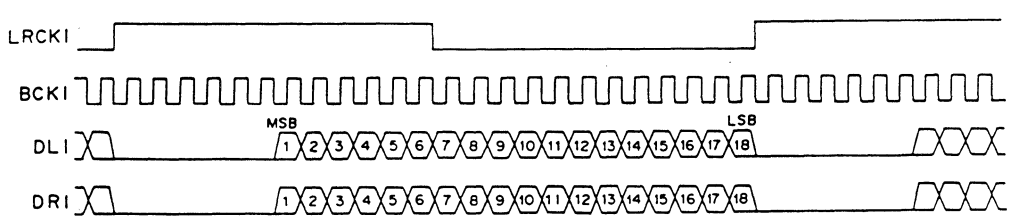
I/O Synchronizing Circuit

1) Theory of operation
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK ⌐) of the LRCK input has entered the window or not.
When power supply is turned on, should LRCK ⌐ be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK ⌐. Synchronization between the exterior system and this LSI is established through this operation.

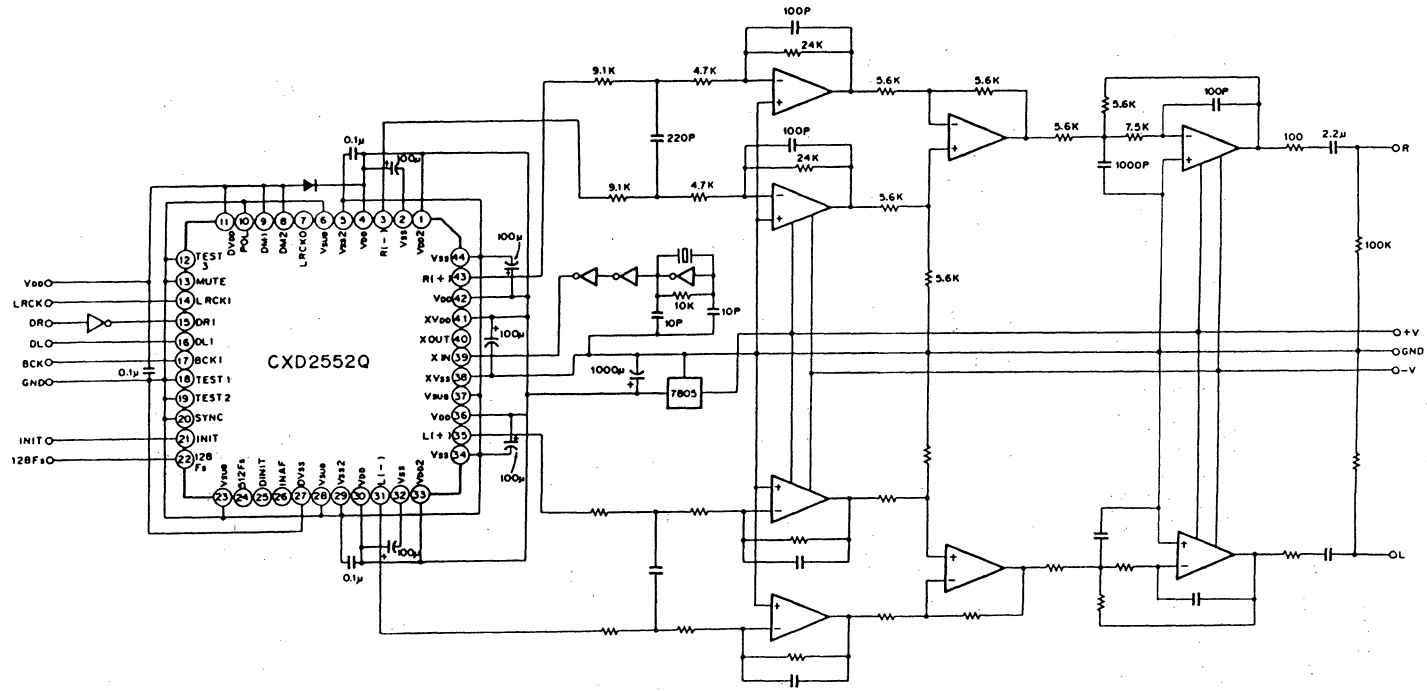
2) Resynchronization by means of INIT
Even when LRCK ⌐ is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK ⌐ is located at the center of the window.
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.



Input Timing (8fs rate)



Application Circuit

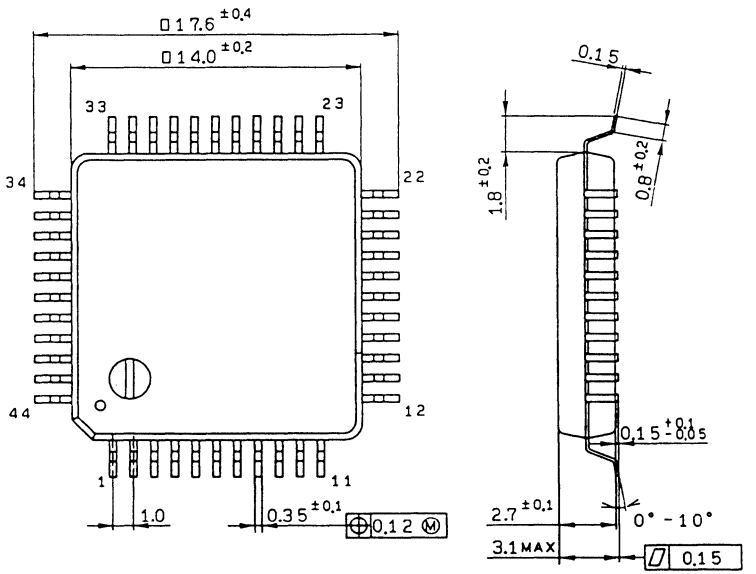


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	———

Audio Delta Sigma Type A/D+D/A+D/F

ADVANCED INFORMATION

CXD2555Q is a delta sigma type (2nd order delta sigma noise shaping) A/D & D/A with a digital filter.

48pin QFP (Plastic)

Features

- Two Channel A/D, D/A with over-sampling, Decimation digital filter.
- Analog circuit for A/D included
- Distortion level: 0.01% (A/D, D/A)
- S/N: 90dB for D/A
  80dB for A/D

Functions

- 1 Fs data rate I/O possible
- Multi chip system possible
- Serial data inter face:32 slot
  Right/Left Adjusted Data
  MSB/LSB first in selections
- Master clock Selection:
  256Fs/512Fs/768Fs/1024Fs
- Fs selection:
  8KHz/16KHz/32KHz/44.1KHz/48KHz
- Provides several clock outputs, devided by a masterclock

Description of Operation

1. Serial Data Interface LRCK, BCK, SOUT, SIN, MASL, MLSL

Serial data format is same for both SIN and SOUT - 2's complementary 2 channel serial data. Each channel has 16bit data at 32bit slot. MASL mode select the 16bit data timing - data comes first or later. MLSL mode select MSB first or LSB first.

MASL	
H	Data First
L	Data Late

MASL	
H	MSB first
L	LSB first

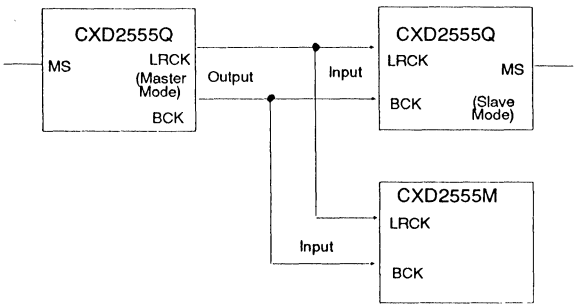
2. Master Mode/Slave Mode MS, LRCK, BCK

When multiple chips are used together, one of the ICs is used as "Master" and output LRCK, BCK. Other ICs are receiveing these clocks as "Slave" chips.

MS	Mode	LRCK, BCK I/O
H	Master Mode	Output
L	Slave Mode	Input

2. (Con't) Slave Mode

(Example)



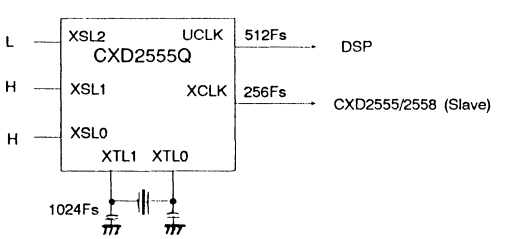
3. Crystal Oscillation Frequency Select XTLI, XTLO, XSLO, XSL1, UCLK, XCLK.

If XSL2 = "L" the crystal frequency is selected by XSL0 and XSL1 as shown in Table 1.
If XTLI receives CMOS level input signal, XTL0 should open.

XSL2	XSL1	XSL0	Crystal Freq	XCLK	UCLK
L	L	L	256Fs	256Fs	128Fs
L	L	H	512Fs	256Fs	256Fs
L	H	L	768Fs	256Fs	384Fs
L	H	H	1024Fs	256Fs	512Fs

Table 1 - Crystal Frequency Select

(Example)



4. Low Frequency Fs Mode XTLI, XTL0, XSL0, XSL1, XSL2

If XSL2 = "H", Low frequency sample rate (Fs=8KHz, 16KHz) can be selected as shown in Table 2.

XSL2	XSL1	XSL0	Crystal Freq.	*Low Freq. Fs Mode
H	L	L	256x32KHz	16KHz
H	L	H	256x32KHz	8KHz
H	H	L	512x32KHz	16KHz
H	H	H	512x32KHz	8KHz

Table 2 - Low Fequency Fs Mode Select.

*32KHz based crystal frequency gives these Fs frequencies.
If 44.1KHz is base frequency then Low Frequency Fs are either 22.05KHz or 11.025KHz.
If 48KHz is base frequency then Low Frequency Fs are either 24KHz or 12KHz.

5. D/A Output Mode Selection

D/A Output Mode	Common	Differential
DASL0	L	H
DASL1	L	L

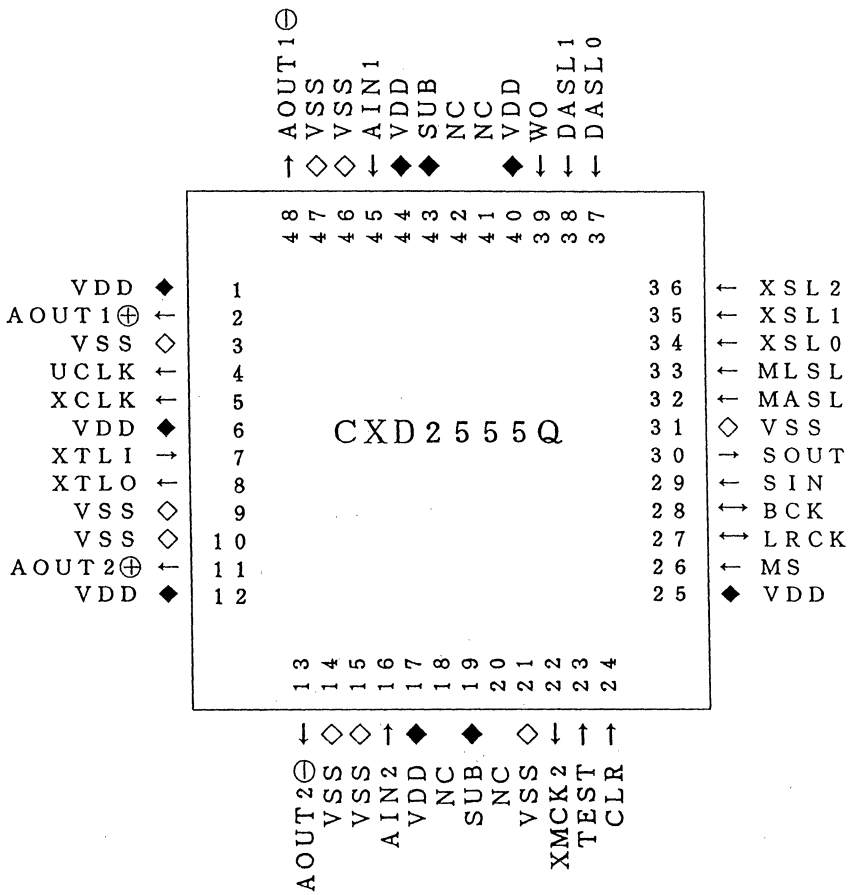
Mode Application
Common: Low output impedance, use "+" pin only.
Differential: Common noise cancel.

Pin Description

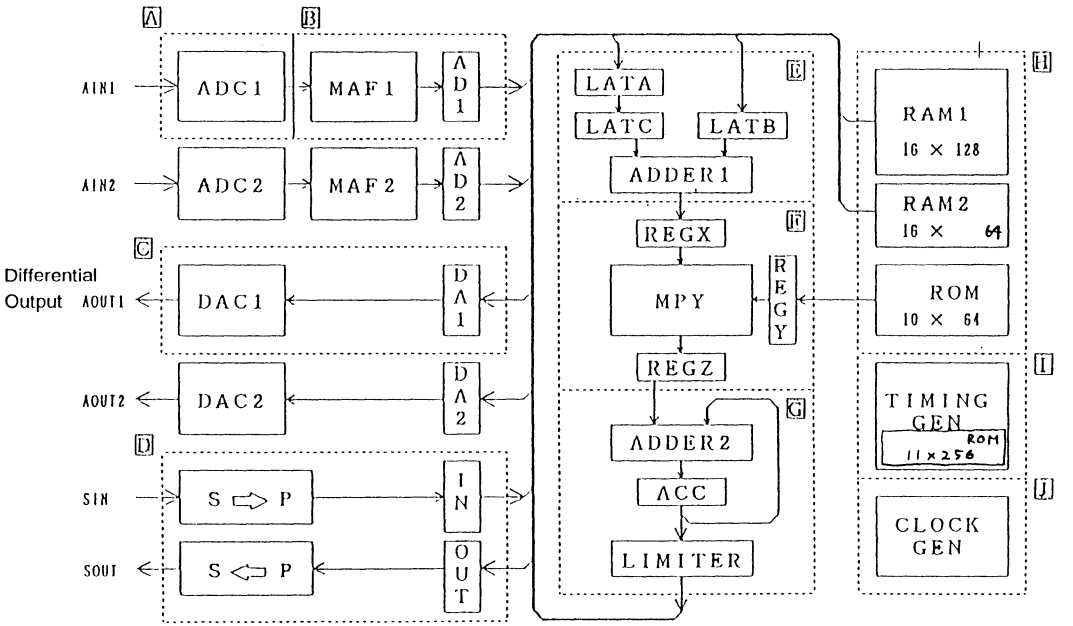
Pin No.	Symbol	I/O	Description
1	VDD	-	CH-1 D/A Analog V_{CC}
2	AOUT1+	O	CH-1 D/A Analog Output (+)
3	VSS	-	CH-1 D/A Analog GND
4	UCLK	O	User clock output 1/2 of master clock frequency
5	XCLK	O	256Fs Clock output
6	VDD	-	Digital V_{CC}
7	XTLI	I	Oscillating input for Master Clock. Crystal freq. is dependent upon the selection of XSLO 0~2
8	XTLO	O	Oscillating output for Master Clock
9	VSS	-	Digital GND
10	VSS	-	CH-2 D/A Analog GND
11	AOUT2+	O	CH-2 D/A Analog Output (+)
12	VDD	-	CH-2 D/A Analog V_{CC}
13	AOUT2-	O	CH-2 D/A Analog Output (-)

Pin Description (Con't)

Pin No.	Symbol	I/O	Description
14	VSS	-	CH-2 D/A Analog GND
15	VSS	-	CH-2 A/D Analog GND
16	AIN2	I	CH-2 A/D Analog Input
17	VDD	-	CH-2 A/D Analog V_{CC}
18	NC	-	
19	SUB	-	IC SUB terminal AC couple to GND
20	NC	-	
21	VSS	-	Digital GND
22	XMCK2	O	Over Sampling Clock Output (128Fs)
23	TEST	I	Test Pin
24	$\overline{CLR}$	I	$\overline{Clear}$ (Active Low)
25	VDD	-	Digital V_{CC}
26	MS	I	Master/Slave Selection "H"-Master Mode, "L"-Slave Mode
27	LRCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
28	BCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
29	SIN	I	Serial Data Input (2's complementary, 32bit slot)
30	SOUT	O	Serial Data Output (2's complementary, 32bit slot)
31	VSS	-	Digital GND
32	MASL	I	16bit serial data slot selection "H"-data first "L"-data late
33	MLSL	I	Selection for MSB first or LSB first "H"-MSB first "L"-LSB first
34	XSLO	I	Crystal Frequency Selection
35	XSL1	I	Crystal Frequency Selection
36	XSL2	I	Crystal Frequency Selection
37	DASL0	I	D/A Output Select
38	DASL1	I	D/A Output Select
39	WO	I	Window Open Mode "H"-Window Mask, "L"-Window Open
40	VDD	-	Digital V_{CC}
41	NC	-	
42	NC	-	
43	SUB	-	IC Subterminal AC Couple to GND
44	VDD	-	CH-1 A/D Analog V_{CC}
45	AIN1	I	CH-1 A/D Analog Input
46	VSS	-	CH-1 A/D Analog GND
47	VSS	-	CH-1 D/A Analog GND
48	AOUT1-	O	CH-1 D/A Analog Output (-)

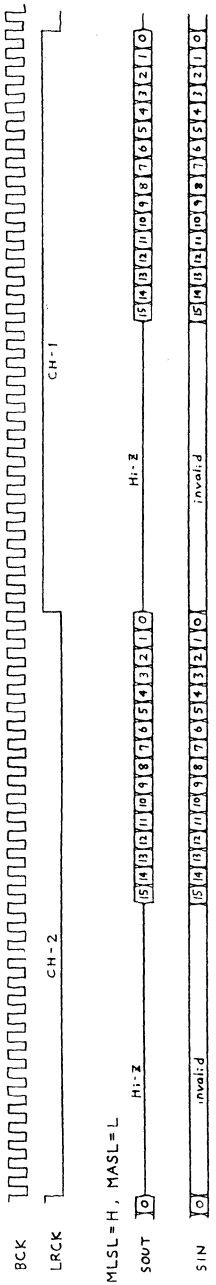

CXD2555Q
1 VDD
2 AOUT1
3 VSS
4 UCLK
5 XCLK
6 VDD
7 XTLI
8 XTLO
9 VSS
10 VSS
11 AOUT2
12 VDD
13 AOUT2
14 VSS
15 VSS
16 AIN2
17 VDD
18 NC
19 SUB
20 NC
21 VSS
22 XMCK2
23 TEST
24 CLR
25 VDD
26 MS
27 LRCK
28 BCK
29 SIN
30 SOUT
31 VSS
32 MASL
33 MLSL
34 XSL0
35 XSL1
36 XSL2
37 DASL0
38 DASL1
39 WO
40 VDD
41 NC
42 NC
43 SUB
44 VDD
45 AIN1
46 VSS
47 VSS
48 AOUT1

ADC/DAC Block Diagram

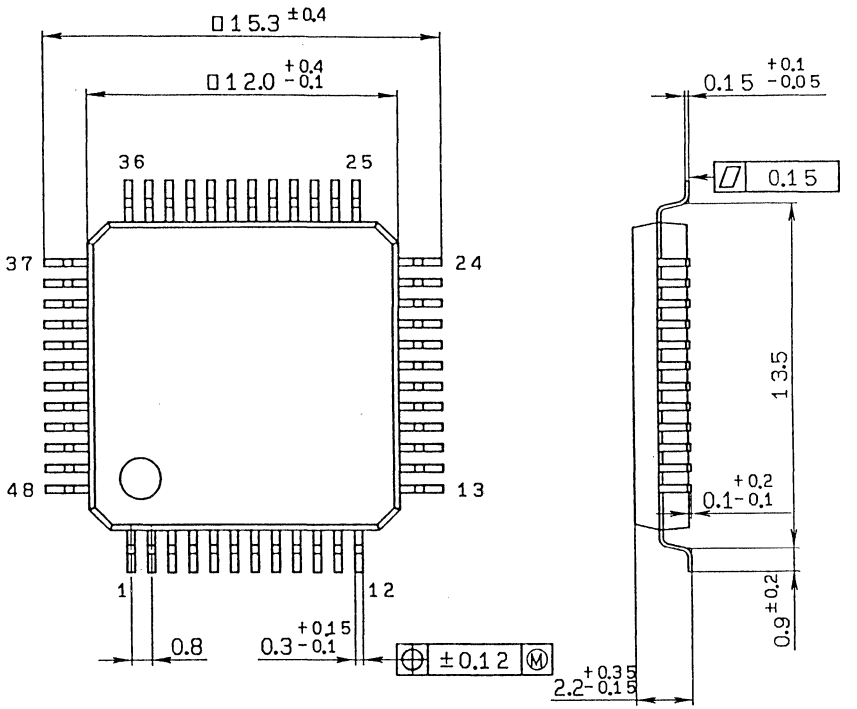


Block Name

A : ADC
B : MAF
C : DAC
D : I/F
E : ADD
F : MPY
G : ACC
H : MEM
I : TIM
J : CLK

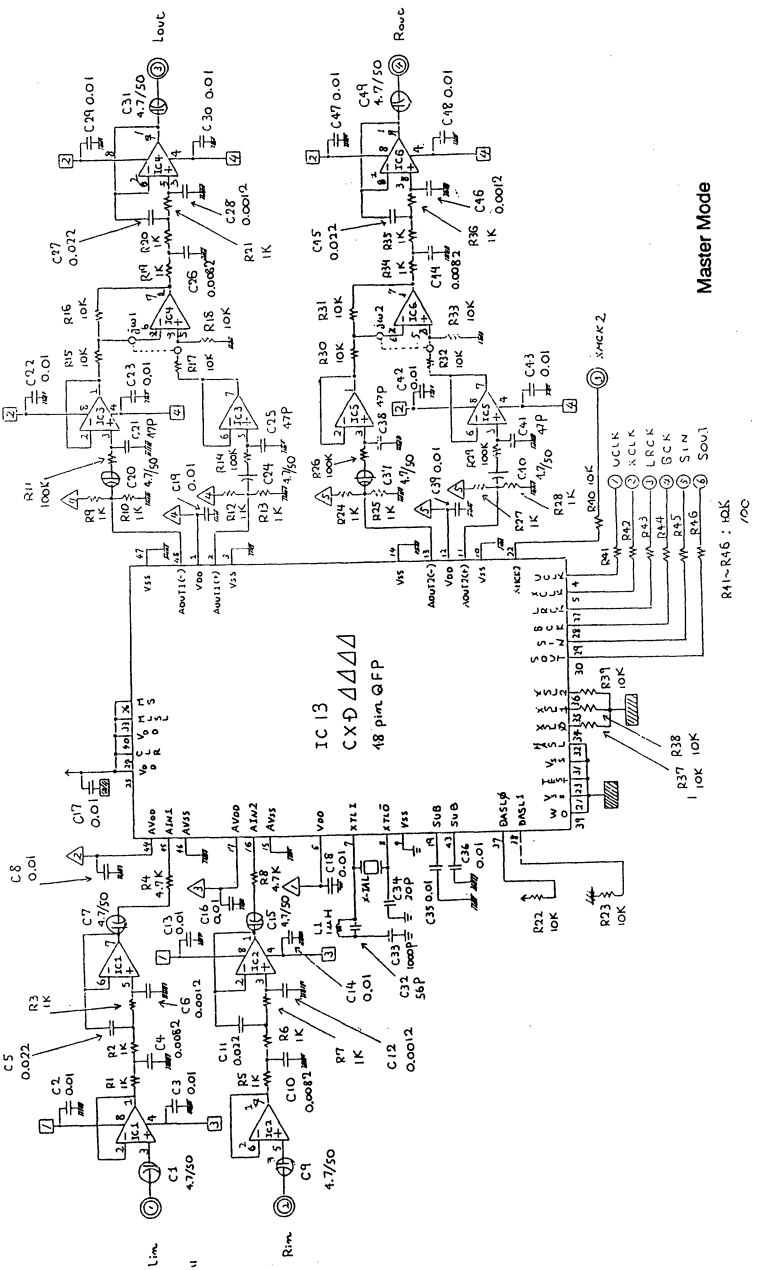

BCK
LRCK
CH-2
CH-1
MLSL=H, MASL=L
SOUT
SIN
Hi-Z
invalid
MLSL=H, MASL=H
MLSL=L, MASL=L
MLSL=L, MASL=H

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

Test System


IC 13
CXD4444
48 pin QFP
Master Mode
Test Circuit
Lout
Rout
Lin
Rin
XMCK2
VCLK
XLCK
LRCK
SCK
SIN
SOUT
R41~R46 : 10K

CD-ROM Processing

CD-ROM Processing

Part Number	Function	Voltage	Package	Page
CXD1185AQ	SCSI Controller Direct interface w/CXD1186Q	5V	64P QFP	383
CXD1186Q	CD-ROM Decoder (ECC, Buffer control)	5V	80P QFP	413
CXD1196R	CD-ROM Decoder with ADPCM, D/F	5V	80P VQFP	457
CXD2500AQ/AQZ	CD Digital Signal Processor	5V	80P QFP	460

SONY CXD1185AQ

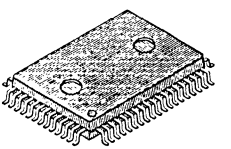
SCSI Controller LSI — Preliminary

Description

The CXD1185AQ is a high performance CMOS SCSI controller LSI that conforms to ANSIX3. 131-1986 standards. The CXD1185AQ is capable of operating in both initiator and target modes. It satisfies all standard SCSI bus features, such as arbitration, selection and parity generation/check functions. A 24-bit data transfer byte counter and 16-byte FIFO are built into the hardware. Two separate buses for data and processor makes high speed data transfer possible. 48 mA (sinking) port is built-in to achieve reduction in the number of external components.

The chip offers a set of high level commands at SCSI phase level. It is also possible to read/write all individual SCSI signals. The combination of the above two makes programs simpler and at the same time improves programability.

64pin QFP (Plastic)



Features

- Satisfies all SCSI bus features, including arbitration, selection, parity generation/check and synchronous data transfer mode.
- Maximum synchronous data transfer rate of 4.0MB/sec and maximum asynchronous data transfer rate of 2.5 MB/sec.
- Provides two separate parts for the data bus and the CPU bus.
- Built-in user-programmable timer for selection/reselection timeout operation.
- Supports 8-bit microcomputer bus.
- Supports programmed I/O and DMA transfer modes.
- Built-in 48mA (sinking) SCSI port. The SCSI port can be used as either single-ended port or differential port.
- Built-in 24-bit data transfer counter.
- Built-in 16-byte FIFO.
- Supports SCSI phase commands.
- All SCSI control signals are software controllable.
- All interrupt conditions are software maskable.
- Built-in 4-bit general-use I/O port.
- Programmable SCSI $\overline{RST}$ drive time.
- Programmable interrupt pin (IRQ) active logic level.
- 64-pin QFP.

Application

SCSI controller

Structure

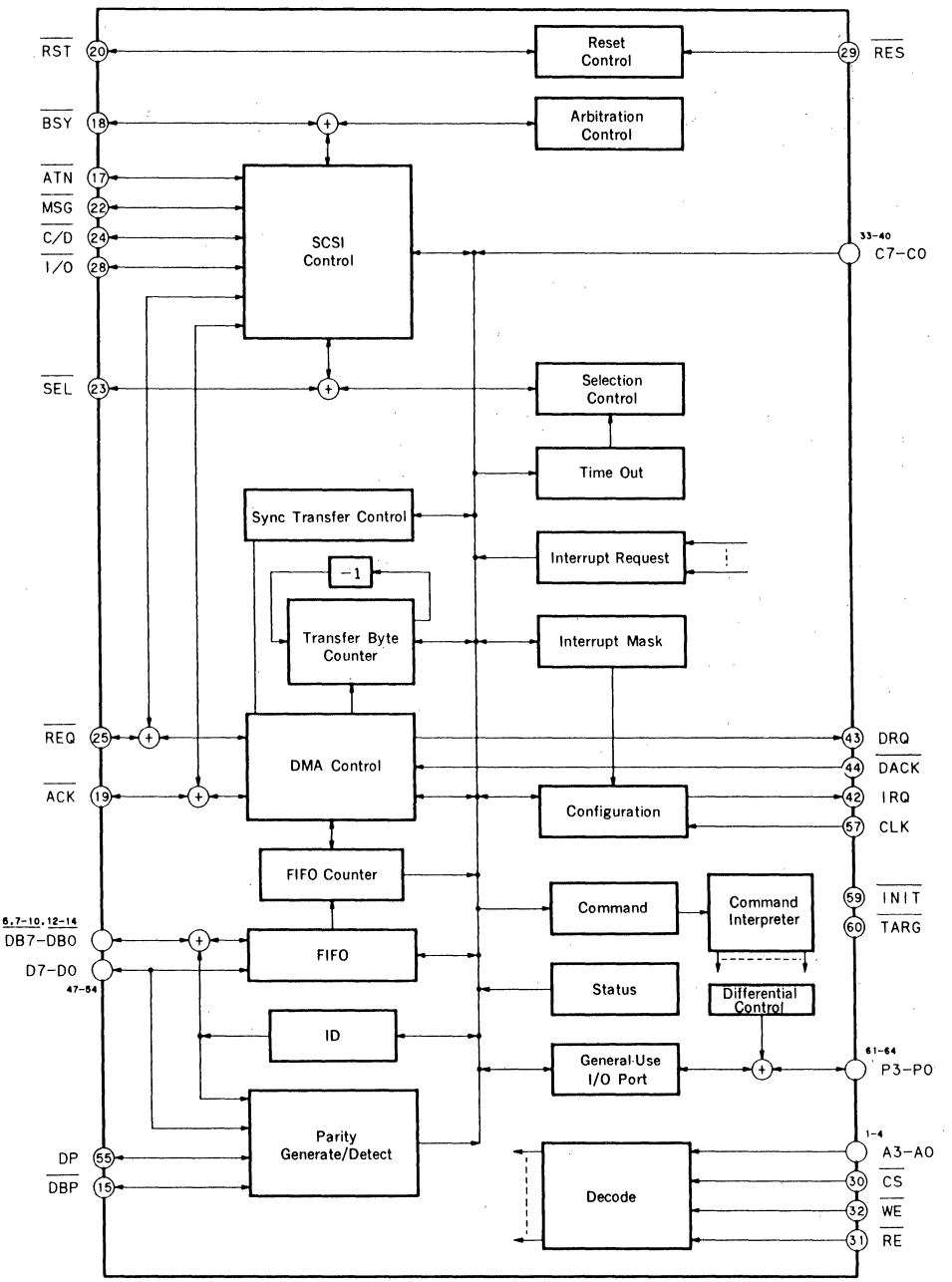
CMOS process

Absolute Maximum Ratings (Ta=25°C, V_{SS}=0V)

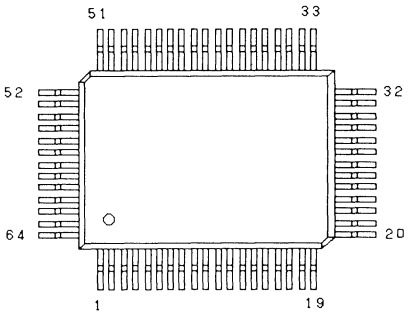
• Supply voltage	V_{DD}	$V_{SS}-0.5$ to $+7.0$	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{opr}	-20 to $+75$	°C
• Storage temperature	T_{stg}	-55 to $+150$	°C

PE90271-HP

Block Diagram



Pin Configuration



Pin Description

Pin no.	Symbol	I/O	Description
1	A3	I	Register select signal bit 3
2	A2	I	Register select signal bit 2
3	A1	I	Register select signal bit 1
4	A0	I	Register select signal bit 0
5	$\overline{DB0}$	I/O	SCSI bus $\overline{DB0}$ signal
6	V_{SS}		GND ⟨note 1⟩
7	$\overline{DB1}$	I/O	SCSI bus $\overline{DB1}$ signal
8	$\overline{DB2}$	I/O	SCSI bus $\overline{DB2}$ signal
9	$\overline{DB3}$	I/O	SCSI bus $\overline{DB3}$ signal
10	$\overline{DB4}$	I/O	SCSI bus $\overline{DB4}$ signal
11	V_{SS}		GND ⟨note 1⟩
12	$\overline{DB5}$	I/O	SCSI bus $\overline{DB5}$ signal
13	$\overline{DB6}$	I/O	SCSI bus $\overline{DB6}$ signal
14	$\overline{DB7}$	I/O	SCSI bus $\overline{DB7}$ signal
15	$\overline{DBP}$	I/O	SCSI bus $\overline{DBP}$ signal, odd parity
16	V_{SS}		GND ⟨note 1⟩
17	$\overline{ATN}$	I/O	SCSI bus $\overline{ATN}$ signal
18	$\overline{BSY}$	I/O	SCSI bus $\overline{BSY}$ signal
19	$\overline{ACK}$	I/O	SCSI bus $\overline{ACK}$ signal
20	$\overline{RST}$	I/O	SCSI bus $\overline{RST}$ signal
21	V_{SS}		GND ⟨note 1⟩
22	$\overline{MSG}$	I/O	SCSI bus $\overline{MSG}$ signal
23	$\overline{SEL}$	I/O	SCSI bus $\overline{SEL}$ signal
24	$\overline{C/D}$	I/O	SCSI bus $\overline{C/D}$ signal
25	$\overline{REQ}$	I/O	SCSI bus $\overline{REQ}$ signal
26	V_{DD}		+5 V ⟨note 1⟩
27	V_{SS}		GND ⟨note 1⟩
28	$\overline{I/O}$	I/O	SCSI bus $\overline{I/O}$ signal

Pin no.	Symbol	I/O	Description
29	$\overline{RES}$	I	Reset all registers, negative logic
30	$\overline{CS}$	I	Chip select signal, negative logic
31	$\overline{RE}$	I	Internal register read signal, negative logic
32	$\overline{WE}$	I	Internal register write signal, negative logic
33	C7	I/O	CPU bus bit 7
34	C6	I/O	CPU bus bit 6
35	C5	I/O	CPU bus bit 5
36	C4	I/O	CPU bus bit 4
37	C3	I/O	CPU bus bit 3
38	C2	I/O	CPU bus bit 2
39	C1	I/O	CPU bus bit 1
40	C0	I/O	CPU bus bit 0
41	V_{SS}		GND 〈note 1〉
42	IRQ	O	Interrupt request signal
43	DRQ	O	DMA request signal
44	$\overline{DACK}$	I	DMA acknowledge signal, negative logic
45	$\overline{WED}$	I	Data bus write signal, negative logic 〈note 3〉
46	$\overline{RED}$	I	Data bus read signal, negative logic 〈note 3〉
47	D0	I/O	Data bus bit 0 〈note 3〉
48	D1	I/O	Data bus bit 1 〈note 3〉
49	D2	I/O	Data bus bit 2 〈note 3〉
50	D3	I/O	Data bus bit 3 〈note 3〉
51	D4	I/O	Data bus bit 4 〈note 3〉
52	D5	I/O	Data bus bit 5 〈note 3〉
53	D6	I/O	Data bus bit 6 〈note 3〉
54	D7	I/O	Data bus bit 7 〈note 3〉
55	DP	I/O	Data bus parity signal 〈note 4〉
56	V_{SS}		GND 〈note 1〉
57	CLK	I	Clock input,5 - 16MHz
58	V_{DD}		+5 V 〈note 1〉
59	$\overline{INIT}$	O	Initiator operation indicator signal
60	$\overline{TARG}$	O	Target operation indicator signal
61	P0 (DOE)	I/O	General-use port bit 0 (SCSI data output authorization) 〈note 2〉
62	P1 (ARB)	I/O	General-use port bit 1 (arbitration in progress) 〈note 2〉
63	P2 (BSYO)	I/O	General-use port bit 2 (SCSI $\overline{BSY}$ output) 〈note 2〉
64	P3 (SELO)	I/O	General-use port bit 3 (SCSI $\overline{SEL}$ output) 〈note 2〉

〈Note 1〉 All V_{DD} and V_{SS} pins should be connected to the power supply and ground, respectively.

〈Note 2〉 Items in parentheses ( ) indicate the meaning of the signal when operating in the SCSI differential mode.

〈Note 3〉 In systems where the CPU and data buses are not separate , connect the $\overline{WED}$ and $\overline{RED}$ pins to $\overline{WE}$ and $\overline{RE}$, respectively, and Pins D7-D0 to Pins C7-C0.

〈Note 4〉 If the data bus parity signal is not used, pull up the DP pin using a resistor.

Electrical Characteristics

DC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage	V_{IHT}		2.2			V
Low level input voltage	V_{ILT}				0.8	V
SCSI bus pin input voltage hysteresis	V_{T+}-V_{T-}		0.2			V
High level output voltage	V_{OH}	$I_{OH}=-2mA$	$V_{DD}-0.5$			V
Low level output voltage	V_{OL}	$I_{OL}=4mA$			0.4	V
SCSI bus pin output voltage	V_{OLS}	$I_{OL}=48mA$			0.5	V
Input leak current	I_{LI1}		−10		10	μA
Input leak current (double-way pin)	I_{LI2}		−40		40	μA

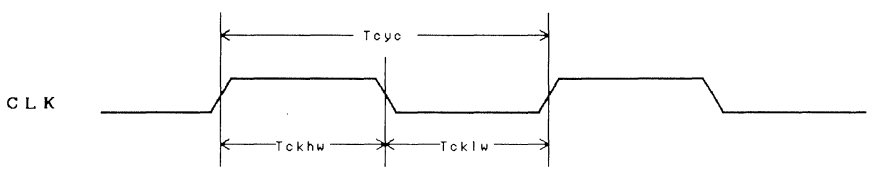
I/O Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
Input/Output pin	$C_{I/O}$			11	pF

AC characteristics (Ta = −20 to +75°C, V_{DD} = 5V ± 10%)

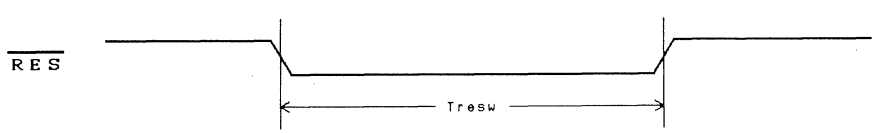
The following capacitances are assumed : input, output pins : 65pF, input /output pins : 125pF.

Clock input



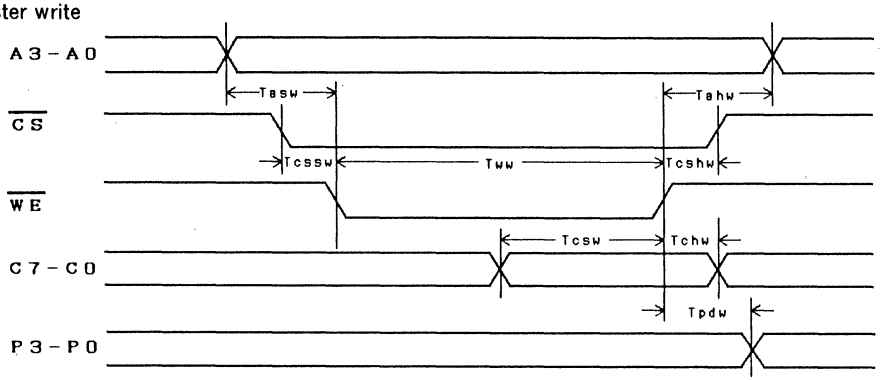
Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	T_{cyc}	5		16	MHz
Clock pulse high level width (period: 16MHz)	T_{ckhw}	31		33	ns
Clock pulse low level width (period: 16MHz)	T_{cklw}	31		33	ns

Reset input



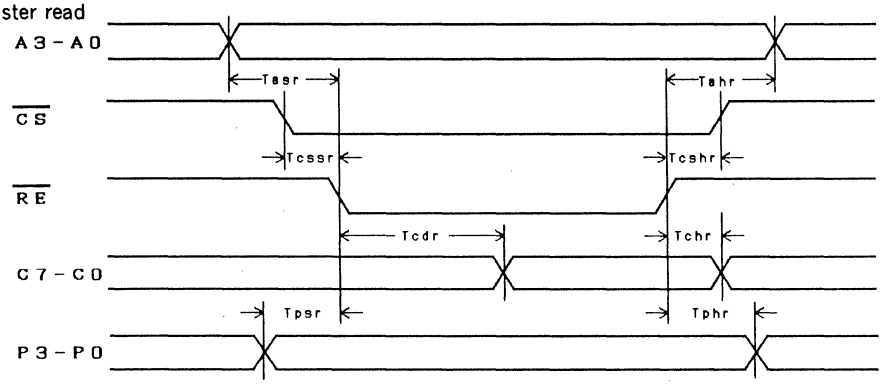
Item	Symbol	Min.	Typ.	Max.	Unit
Reset pulse width	T_{resw}	100			ns

Register write



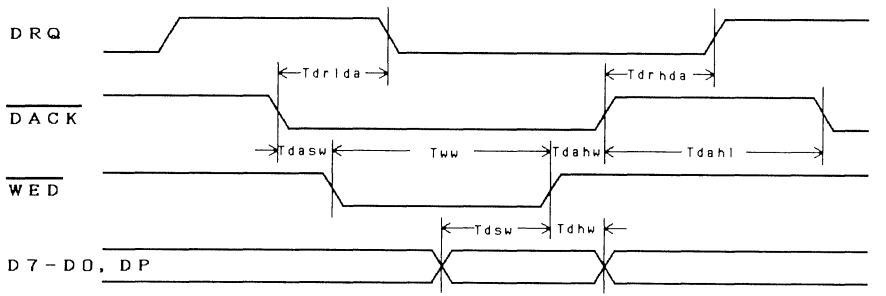
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. $\overline{WE}$ ↓)	Tasw	0			ns
$\overline{CS}$ setup time (vs. $\overline{WE}$ ↓)	Tcssw	0			ns
$\overline{WE}$ pulse width	Tww	70			ns
Date setup time (vs. $\overline{WE}$ ↑)	Tcsw	30			ns
Address hold time (vs. $\overline{WE}$ ↑)	Tahw	0			ns
$\overline{CS}$ hold time (vs. $\overline{WE}$ ↑)	Tcshw	0			ns
Data hold time (vs.$\overline{WE}$ ↑)	Tchw	10			ns
Port delay time (vs. $\overline{WE}$ ↑)	Tpdw			100	ns

Register read



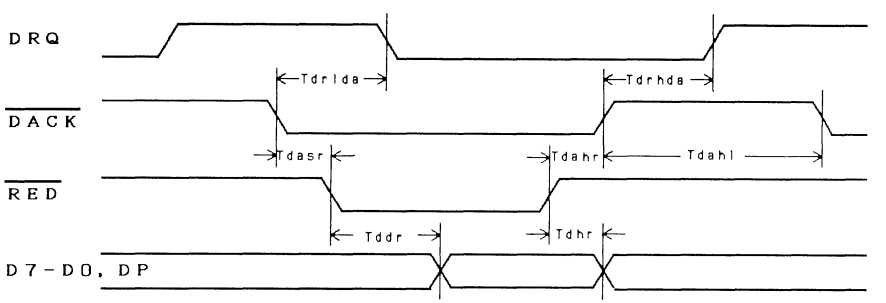
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. $\overline{RE}$ ↓)	Tasr	0			ns
$\overline{CS}$ setup time (vs. $\overline{RE}$ ↓)	Tcssr	0			ns
Data delay time (vs.$\overline{RE}$ ↓)	Tcdr			130	ns
Address hold time (vs. $\overline{RE}$ ↑)	Tahr	0			ns
$\overline{CS}$ hold time (vs. $\overline{RE}$ ↑)	Tcshr	0			ns
Date hold time (vs. $\overline{RE}$ ↑)	Tchr	5		25	ns
Port setup time (vs. $\overline{RE}$ ↓)	Tpsr	0			ns
Port hold time (vs.$\overline{RE}$ ↑)	Tphr			0	ns

DMA write



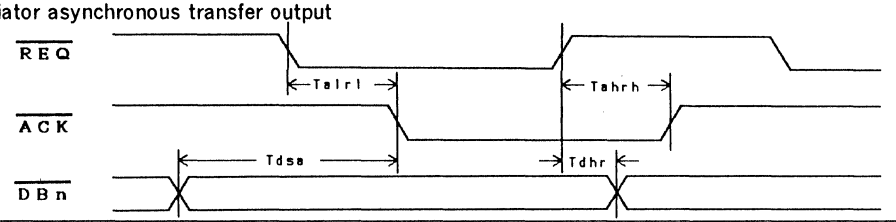
Item	Symbol	Min.	Typ.	Max.	Unit
DRQ fall time (vs. $\overline{\text{DACK}}$ ↓)	Tdrlda			70	ns
$\overline{\text{DACK}}$ setup time (vs. $\overline{\text{WED}}$ ↓)	Tdasw	0			ns
$\overline{\text{WED}}$ pulse width	Tww	50			ns
Data setup time (vs. $\overline{\text{WED}}$ ↑)	Tdsw	20			ns
$\overline{\text{DACK}}$ hold time (vs. $\overline{\text{WED}}$ ↑)	Tdahw	10			ns
Data hold time (vs. $\overline{\text{WED}}$ ↑)	Tdhw	10			ns
DRQ rise time (vs. $\overline{\text{DACK}}$ ↑)	Tdrhda			110	ns
$\overline{\text{DACK}}$ fall time (vs. $\overline{\text{DACK}}$ ↑)	Tdahl	50			ns

DMA read



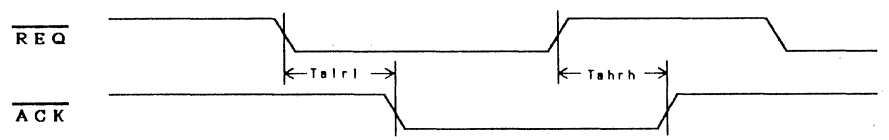
Item	Symbol	Min.	Typ.	Max.	Unit
DRQ fall time (vs. $\overline{\text{DACK}}$ ↓)	Tdrlda			70	ns
$\overline{\text{DACK}}$ setup time (vs. $\overline{\text{RED}}$ ↓)	Tdasr	0			ns
Data delay time (vs. $\overline{\text{RED}}$ ↓)	Tddr			90	ns
$\overline{\text{DACK}}$ hold time (vs. $\overline{\text{RED}}$ ↑)	Tdahr	10			ns
Data hold time (vs. $\overline{\text{RED}}$ ↑)	Tdhr	5		25	ns
DRQ rise time (vs. $\overline{\text{DACK}}$ ↑)	Tdrhda			110	ns
$\overline{\text{DACK}}$ fall time (vs. $\overline{\text{DACK}}$ ↑)	Tdahl	50			ns

Initiator asynchronous transfer output



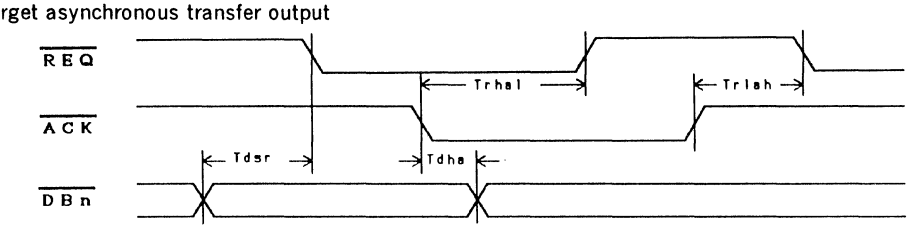
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. $\overline{REQ}$ ↓)	Talrl			120	ns
Data setup time (vs. $\overline{ACK}$ ↓)	Tdsa	55			ns
$\overline{ACK}$ rise time (vs. $\overline{REQ}$ ↑)	Tahrh			90	ns
Data hold time (vs. $\overline{REQ}$ ↑)	Tdhr			195	ns

Initiator asynchronous transfer input



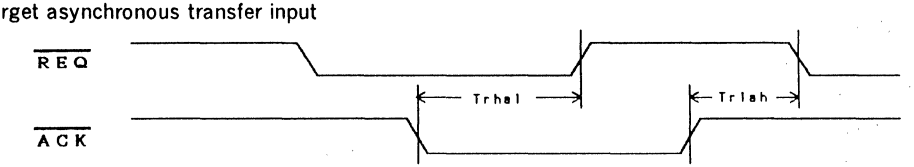
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. $\overline{REQ}$ ↓)	Talrl			120	ns
$\overline{ACK}$ rise time (vs. $\overline{REQ}$ ↑)	Tahrh			90	ns

Target asynchronous transfer output



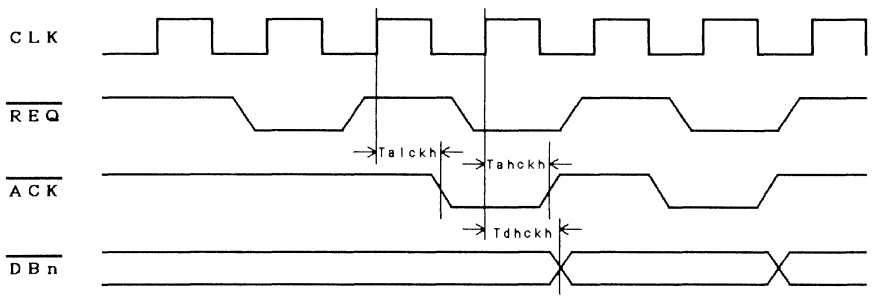
Item	Symbol	Min.	Typ.	Max.	Unit
Data setup time (vs. $\overline{REQ}$ ↓)	Tdsr	55			ns
$\overline{REQ}$ rise time (vs. $\overline{ACK}$ ↓)	Trhal			90	ns
Data hold time (vs. $\overline{ACK}$ ↓)	Tdha			195	ns
$\overline{REQ}$ fall time (vs. $\overline{ACK}$ ↑)	Trlah			120	ns

Target asynchronous transfer input



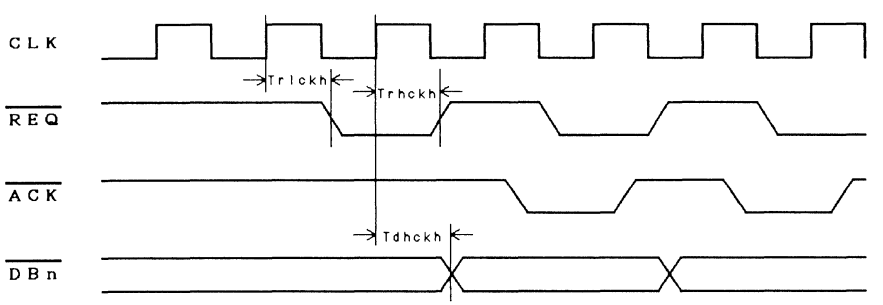
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ rise time (vs. $\overline{ACK}$ ↓)	Trhal			90	ns
$\overline{REQ}$ fall time (vs. $\overline{ACK}$ ↑)	Trlah			120	ns

Initiator synchronous transfer output



Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. CLK ↑)	Talckh			130	ns
$\overline{ACK}$ rise time (vs. CLK ↑)	Tahckh			100	ns
Data hold time (vs. CLK ↑)	Tdhckh			170	ns

Target synchronous transfer output



Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ fall time (vs. CLK ↑)	Trlckh			130	ns
$\overline{REQ}$ rise time (vs. CLK ↑)	Trhckh			100	ns
Data hold time (vs. CLK ↑)	Tdhckh			170	ns

Description of Functions

1. Internal registers

CXD1185AQ possesses 16 internal registers. The CPU can control CXD1185AQ by reading and writing these registers.

A summary of the registers is provided below.

Address	Read	Write
0	Status	Command
1	SCSI data	←
2	Interrupt request 1	〈 * 〉
3	Interrupt request 2	Environment setting
4	SCSI control monitor	Selection/reset timer
5	FIFO status	〈 * 〉
6	SCSI ID	←
7	Transfer byte counter (low)	←
8	Transfer byte counter (middle)	←
9	Transfer byte counter (high)	←
A	Interrupt authorization 1	←
B	Interrupt authorization 2	←
C	Mode	←
D	Sync transfer control	←
E	SCSI bus control	←
F	I/O port	←

〈*〉 No register assigned to this address.

1-1. Status register (R0 : R)

This register is used to monitor the status of CXD1185AQ.

7	6	5	4	3	2	1	0
MRST	MDBP		INIT	TARG	TRBZ	MIRQ	CIP

MRST : Monitors the SCSI bus $\overline{RST}$ signal, positive logic.

MDBP : Monitors the SCSI bus $\overline{DBP}$ signal, positive logic.

INIT : "1" when CXD1185AQ is in initiator status.
When this bit is set to "1", all commands except ones which are valid in target status and in disconnected status are accepted.

TARG : "1" when CXD1185AQ is in target status.
When this bit is set to "1", all commands except ones which are valid in initiator status and in disconnected status are accepted.

TRBZ : When this bit is set to "1", it indicates that the transfer byte counter count is zero.

MIRQ : Monitors the interrupt request signal (IRQ signal).
This bit is set whenever interrupt request occurs and cleared once interrupt request 1 register and interrupt 2 register are read. This bit is not affected by the content of the interrupt authorization register. The logic level of this bit is not affected by the SIRM bit in the environment setting register.

CIP : Indicates that a chip command is being executed.
While this bit is "1", no new commands can be written to the command register, with the exception of the "Reset Chip" command.

1-2. Command register (R0 : W)

This is the register to which CXD1185AQ commands are written.

When a command is written to this register, status register bit 0 (CIP) is set. When the command is executed and terminated, interrupt request register bit 7 (FNC) is set, and the CIP bit and command register are cleared.

7	6	5	4	3	2	1	0
CAT1	CAT0	DMA	TRBE	CMD3	CMD2	CMD1	CMD0

CAT1, CAT0 :

Sets the category code given to CXD1185AQ.

CXD1185AQ commands are divided into the following four categories :

CAT1	CAT0	Mode
0	0	Commands which are valid in any status
0	1	Commands which are valid in disconnected status
1	0	Commands which are valid in target status
1	1	Comannds which are valid in initiator status

If the current status of CXD1185AQ does not match with the category code in the command received, the CIP and command registers are cleared. No interrupt is generated in this case.

DMA : DMA mode

When this bit is set to "1" and a transfer command is executed, DMA transfer takes place via the data bus (D7-D0). During the DMA transfer, any attempts by the CPU to read/write SCSI data register via CPU bus is ignored.

TRBE : Activates the transfer byte counter.

When this bit is set to "1" and a transfer command is executed, the transfer byte counter value is decremented each time a byte of data is transferred.

When the counter reaches "0" the next data request is stopped. At this point, if the data transfer mode is output to SCSI or in DMA mode, CXD1185AQ will continue to transfer any data remaining in FIFO until it is empty. If a transfer command is executed when this bit is set to "0", 1 byte of data will be transferred regardless of the value of the transfer byte counter. In this case the transfer byte counter is not decremented. When DMA bit is set, TRBE bit must also be set. These two bits can be set simultaneously during command write.

CMD3, CMD2, CMD1, CMD0 :

Indicates the command code.

CXD1185AQ responds to the following commands. See the command description section for detailed information.

Category	DMA	TRBE	Command code	Command
0 0	0	0	0 0 0 0	No Operation
	0	0	0 0 0 1	Reset Chip
	0	0	0 0 1 0	Assert $\overline{RST}$
	0	0	0 0 1 1	Flush FIFO
	0	0	0 1 0 0	Assert SCSI Control
	0	0	0 1 0 1	Deassert SCSI Control
	0	0	0 1 1 0	Assert SCSI Data
	0	0	0 1 1 1	Deassert SCSI Data
0 1	0	0	0 0 0 0	Reselect
	0	0	0 0 0 1	Select without $\overline{ATN}$
	0	0	0 0 1 0	Select with $\overline{ATN}$
	0	0	0 0 1 1	Enable Selection/Reselection
	0	0	0 1 0 0	Disable Selection/Reselection
1 0	*	*	0 0 0 0	Send Message
	*	*	0 0 0 1	Send Status
	*	*	0 0 1 0	Send Data
	0	0	0 0 1 1	Disconnect
	*	*	0 1 0 0	Receive Message Out
	*	*	0 1 0 1	Receive Command
	*	*	0 1 1 0	Receive Data
1 1	*	*	0 0 0 0	Transfer Information
	*	*	0 0 0 1	Transfer Pad
	0	0	0 0 1 0	Deassert $\overline{ACK}$
	0	0	0 0 1 1	Assert $\overline{ATN}$
	0	0	0 1 0 0	Deassert $\overline{ATN}$

〈*〉 Don't care, except that if DMA bit is set to "1", TRBE bit must be set to "1".

1-3. SCSI data register (R1 : R/W)

This register is used when transferring data between the SCSI bus and the CPU bus.

When data is output to the SCSI bus via the CPU bus, data can be written to this register if the FIFO status register bit 4 (FIF) is "0".

When data is input from SCSI bus, data can be read from this register if the FIFO status register bit 7 (FIE) is "0".

When "Assert SCSI data" is executed the 16 byte FIFO becomes a 1 byte FIFO. Any value written to the register will be on the SCSI bus instantly and a read operation will return the current SCSI data bus value.

When a DMA transfer is performed via the data bus, reads and writes to the SCSI data register are performed using the $\overline{WED}$, $\overline{RED}$ and $\overline{DACK}$ signals.

1-4. Interrupt request registers 1 and 2

These registers show the cause of the interrupt.

When an interrupt authorized by interrupt authorization registers 1 or 2 is generated, the IRQ pin is set immediately.

Bits in the interrupt request registers 1 and 2 are cleared once the registers are read by the CPU. When all interrupt bits are cleared, MIRQ bit (in the status register) and the IRQ pin are cleared.

Note that interrupt bits in these registers are set regardless of the values in the interrupt authorization registers. If interrupt requests are software polled, interrupt request registers 1 and 2 should only be read

when the MIRQ bit, in the status register, is "1".

1-4-1. Interrupt request register 1 (R2 : R)

This register's interrupt conditions can be masked in the interrupt authorization register 1.

When one of the bits in this register is set, MIRQ bit in the status register is set. If the interrupt bit is authorized in the interrupt authorization register 1, the IRQ pin is activated simultaneously.

7	6	5	4	3	2	1	0
			STO	RSL	SWA	SWOA	ARBF

STO : Selection Time Over
Indicates a time out error during selection. Also, indicates that the SCSI bus $\overline{RST}$ signal has been driven for the time set in the selection/reset timer if the mode register bit 4 (TMSL) is set to "1". The selection time out time and SCSI bus $\overline{RST}$ signal drive time are determined by the value of the selection/reset timer register.

RSL : Reselected
Indicates that reselection has taken place. FNC bit in the interrupt register 2 is set after reselection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the "Enable Selection/ Reselection" command is executed.

SWA : Selection With ATN
Indicates that selection has taken place with the SCSI bus $\overline{ATN}$ signal driven. FNC bit in the interrupt register 2 is set after selection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the " Enable Selection/Reselection" command is executed.

SWOA : Selection Without ATN
Indicates that selection has taken place. FNC bit in the interrupt register 2 is set after selection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the "Enable Selection/Reselection" command is executed.

ARBF : Arbitration Fail
Indicates that CXD1185AQ lost in the arbitration for the right to use the SCSI bus. This bit is set when, after receiving a selection/reselection command, the chip waited for bus free and entered arbitration only to be encountered by another device with higher priority. As soon as this bit is set the selection/reselection command is terminated. To participate in another arbitration a new selection/reselection command must be written to the command register.

1-4-2. Interrupt request register 2 (R3 : R)

This register's interrupt conditions can be masked in the interrupt authorization register 2.

When one of the bits in this register is set, MIRQ bit in the status register is set. If the interrupt bit is authorised in the interrupt authorization register 2, the IRQ pin is activated simultaneously.

7	6	5	4	3	2	1	0
FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG

FNC : Function Complete
Indicates that the received command was executed and terminated.

DCNT : Disconnected
Indicates that a disconnect has taken place in the initiator mode.

SRST : SCSI Reset
Indicates that the SCSI bus $\overline{RST}$ pin was driven. This bit is also set when the "Assert $\overline{RST}$" command is executed.

PHC : Phase Change
Indicates that the SCSI phase has been changed. This bit is set if CXD1185AQ is operating in the initiator mode and the target has changed the SCSI phase ($\overline{MSG}$, $\overline{I/O}$, $\overline{C/D}$ signal), and drove $\overline{REQ}$.

DATN : Drive ATN
Indicates that the SCSI bus $\overline{ATN}$ signal has been driven. This bit is set if the CXD1185AQ is operating in the target mode and the initiator has driven the $\overline{ATN}$ signal.

DPE : Data bus Parity Error
Indicates a parity error on the data bus. This bit is only set if environment setting register bit 5 (DPEN) is set to "1". In initial status odd parity (environment register bit 6 set to "0") is selected.

SPE : SCSI bus Parity Error
Indicates a parity error on the SCSI bus. Parity check takes place during the selection phase and data transfer phases.

RMSG : $\overline{REQ}$ in Message Phase
Indicates that the $\overline{REQ}$ signal has been driven during the message phase when the CXD1185AQ is in initiator mode. This bit is used when two different batches of message data have been received during the message phase or if the target requests that a message be resent.

1-5. Environment setting register (R3: W)
This register is used to set the operating mode of the CXD1185AQ.
Normally, some value must be written to this register immediately after a hardware reset from the CPU.

7	6	5	4	3	2	1	0
DIFE	SDPM	DPEN	SIRM			FS1	FS0

DIFE : Selects the differential mode.
When this bit is set to "1", general-use I/O port Pins P3-P0 are assigned for differential mode bits.

SDPM : Selects the data bus parity condition.
This bit is set to "0" for odd parity and to "1" for even parity. However, its value is irrelevant if the DPEN bit is set to "0".

DPEN : Enables parity generation/check for the data bus.
If this bit is set to "1", data bus parity signal is input/output via the DP pin.

SIRM : Selects the IRQ signal logic level.
After a hardware reset is performed, the IRQ signal output is positive logic. To change the IRQ signal to negative logic. "1" must be set in this bit.

FS1, FS0 :
Used to select the CXD1185AQ clock division ratio.
The appropriate values, as shown in the table below, must be written into these bits to match the external clock frequency applied to the CXD1185AQ:

Input frequency (MHz)	FS1	FS0	Clock division ratio
16-13	0	0	4
12-9	0	1	3
8-5	1	*	2

For the changes made to these bits to be effective, "Chip Reset" command must be executed.
Bits FS1 and FS0 are set for a clock division ratio of "4" after a hardware reset.

1-6. SCSI control monitor register (R4 : R)

Current status of all SCSI control signals can be read directly from this register.

7	6	5	4	3	2	1	0
MBSY	MSEL	MMSG	MCD	MIO	MREQ	MACK	MATN

MBSY : Monitors the SCSI bus $\overline{BSY}$ signal. Positive logic.
MSEL : Monitors the SCSI bus $\overline{SEL}$ signal. Positive logic.
MMSG : Monitors the SCSI bus $\overline{MSG}$ siganl. Positive logic.
MCD : Monitors the SCSI bus $\overline{C/D}$ signal. Positive logic.
MIO : Monitors the SCSI bus $\overline{I/O}$ signal. Positive logic.
MREQ : Monitors the SCSI bus $\overline{REQ}$ signal. Positive logic.
MACK : Monitors the SCSI bus $\overline{ACK}$ signal. Positive logic.
MATN : Monitors the SCSI bus $\overline{ATN}$ signal. Positive logic.

1-7. Selection/reset timer register (R4 : W)

This register is used to set the selection time out time or the SCSI bus $\overline{RST}$ drive time.
The real selection time out time can be calculated by the following equation :

$$\text{TIME } (\mu s)=\frac{Div}{f_{cyc}}\times(VAL+1)\times 8{,}192$$

f_{cyc} : Input frequency (MHz)
Div : Clock division ratio (See section on Environment setting register)
VAL : Value written to the selection/reset timer register

Generally the selection time out time is set to 250ms.
When the selection/reset timer register is used to set the drive time for the $\overline{RST}$ signal a "1" must be written to mode register bit 4 (TMSL).
The real $\overline{RST}$ signal drive time can be calculated by the following equation :

$$\text{TIME}(\mu s) = \frac{Div}{f_{cyc}}\times(32\times VAL+38)$$

f_{cyc} : Input frequency (MHz)
Div : Clock division ratio (See section on Environment setting register)
VAL : Value written to the selection/reset timer register

1-8. FIFO status register (R5 : R)

This register is for monitoring the FIFO status.

7	6	5	4	3	2	1	0
FIE			FIF	FC3	FC2	FC1	FC0

FIE : FIFO Empty
Indicates that the FIFO is empty.
FIF : FIFO Full
Indicates that the FIFO is full.
FC3, FC2, FC1, FC0 :
Indicate the number of bytes of data stored in the FIFO.

1-9. SCSI ID register (R6 : R/W)

This register is used to set the SCSI owner ID and the target ID for selection.

The upper three bits in this register have different meanings during reads and writes.

7	6	5	4	3	2	1	0	
SID2	SID1	SID0			OID2	OID1	OID0	(Read)

7	6	5	4	3	2	1	0	
TID2	TID1	TID0			OID2	OID1	OID0	(Write)

SID2, SID1, SID0 :

Indicates which device last selected/reselected the CXD1185AQ.

TID2, TID1, TID0 :

The target ID is written to these bits prior to selection.

OID2, OID1, OID0 :

The owner ID is written to these bits.

1-10. Transfer byte counter (high, middle, low) (R9, R8, R7 : R/W)

The 24-bit counter calculates the number of remaining bytes of transfer data during data transfer between SCSI bus and the CPU bus or data bus. To activate the transfer byte counter, command register bit 4 (TRBE) must be set when writing to the command register.

When data is output to the SCSI bus, the transfer byte counter is decremented at each rise of the $\overline{WE}$ or $\overline{WED}$ signal. When data is input from the SCSI bus, is decremented at each fall of the $\overline{ACK}$ signal when in the initiator mode and at each fall of the $\overline{REQ}$ signal when in the target mode.

1-11. Interrupt authorization registers 1 and 2 (RA, RB : R/W)

These registers are used to determine on which interrupt the IRQ pin should be activated.

The bit positions in these two registers correspond to the bit positions in the interrupt request registers. The IRQ pin will be activated if an interrupt bit becomes "1" and the corresponding bit in the interrupt authorization register is also set to "1".

1-12. Mode register (RC : R/W)

This register is used for setting the modes of CXD1185AQ.

7	6	5	4	3	2	1	0
HDPE	HSPE	HATN	TMSL	SPHI			BDMA

HDPE : When this bit is set to "1", data transfer will be terminated if a parity error is detected on the data bus during a data transfer. However, this bit is irrelevant if environment setting register bit 5 (DPEN) is set to "0".

HSPE : When this bit is set to "1", data transfer will be terminated if a parity error is detected on the SCSI bus during a data transfer.

HATN : When this bit is "1" in target mode, data transfer will be terminated if an $\overline{ATN}$ signal is driven on the SCSI bus.

TMSL : When this bit is set to "1", the selection/reset timer register is used to set the duration of the SCSI bus $\overline{RST}$ signal.

This bit must not be overwritten with a new value if status register bit 0 (CIP) is set to "1". If it is required to drive $\overline{RST}$ signal when the CIP bit is "1", first execute "Reset Chip" command, then overwrite this bit.

SPHI : When this bit is set to "0", if target changes the phase signal during the execution of a transfer command and the $\overline{REQ}$ pin is active, interrupt request register 2 bit 4 (PHC) is set immediately. If this bit is set to "1", in the mode in which data is input from the SCSI bus, the PHC bit is not set until all the FIFO contents are transferred to the CPU bus or the DMA bus.

BDMA : Burst DMA mode. When this bit is set to "1", the DRQ pin be "1" for the whole of the DMA transfer.

1-13. Synchronous transfer control register (RD : R/W)

This register is used to set the transfer period and the offset for synchronous transfers.

7	6	5	4	3	2	1	0
TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0

TPD3, TPD2, TPD1, TPD0 :

Bits used to set the transfer period for synchronous transfers.
The transfer period is designated according to the following equation :

$$RATE\ (\mu s)=\frac{Div}{f_{cyc}\times 2}\times(VAL+1)$$

fcyc : Input frequency (MHz)

Div : Clock division ratio (see section on Environment setting register)

VAL : Value written to TPD3-0

TOF3, TOF2, TOF1, TOF0 :

Bits used to set the offset for synchronous transfers.
The asynchronous transfer mode is selected by writing "0" to all of these bits.

1-14. SCSI bus control register (RE : R/W)

This register is used to control the control signals used by the SCSI bus.
Reading this register consists simply of reading the value which was written there previously. However, if the "Assert SCSI Control" command is executed, "0"s will be read out. The "Assert SCSI Control" command must be executed in order to output this register's value to the SCSI bus.

7	6	5	4	3	2	1	0
ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN

ABSY : When this bit is set to "1", the SCSI bus $\overline{BSY}$ signal is driven.

ASEL : When this bit is set to "1", the SCSI bus $\overline{SEL}$ signal is driven.

AMSG : When this bit is set to "1", the SCSI bus $\overline{MSG}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

ACD : When this bit is set to "1", the SCSI bus $\overline{C/D}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AIO : When this bit is set to "1", the SCSI bus $\overline{I/O}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AREQ : When this bit is set to "1", the SCSI bus $\overline{REQ}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AACK : When this bit is set to "1", the SCSI bus $\overline{ACK}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the initiator mode.

AATN : When this bit is set to "1", the SCSI bus $\overline{ATN}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the initiator mode.

1-15. I/O port (RF : R/W)

This register is used for input/output switching of the general-use 4-bit port and for reading/writing the contents of the port.

7	6	5	4	3	2	1	0
PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0

PCN3, PCN2, PCN1, PCN0 :

These bits are used for input/output switching of individual bits when Pins P3-P0 are used as a general-use port. When a "1" is written to any of these bits, the corresponding port is set to the output mode.

All these bits are cleared when a hardware reset is performed. Note that first "0" must be written to all these bits before writing a "1" to environment setting register bit 7 (DIFE).

PRT3, PRT2, PRT1, PRT0 :

This is the 4-bit I/O port.

The values written to whichever of these four bits have been set to output mode by PCN3-PCN0 are output via Pins P3-P0. By reading these bits it is possible to monitor the values of Pins P3-P0 directly.

2. Command Description

This section gives description of all the commands supported by the CXD1185AQ.

With the exception of "Reset Chip", the following commands can only be written to the command register when the CIP bit in the status register (bit 0) is "0".

2-1. Commands valid in any status

The following commands can be issued when the CXD1185AQ is in any of its three statuses : disconnected, initiator or target.

The chip is, at any given time, in one of the three status disconnected, initiator or target. This section is divided into following subsections.

- Commands valid in any status
- Commands valid in disconnected state
- Commands valid in initiator mode
- Commands valid in target mode

- No Operation

  This command has no effect on the CXD1185AQ.

  However, the FNC bit is set when the command is completed.

- Reset Chip

  This command initializes the CXD1185AQ.

  Except for the environment setting register, all registers of the CXD1185AQ are cleared. If the clock division ratio is changed in the environment setting register, this command must be executed.

  This command can be executed regardless of the value of the CIP bit.

- Assert $\overline{RST}$

  This command drives the SCSI bus $\overline{RST}$ pin.

  When this command is executed, interrupt request register 2 bit 5 (SRST) is set and an interrupt is generated. The SCSI $\overline{RST}$ signal is active for 25 μs. However, if the $\overline{RST}$ signal drive duration needs to be changed, it is necessary to set mode register bit 4 (TMSL) to "1" and write the drive duration to the selection/reset timer register before executing this command.

- Flush FIFO

  Initializes FIFO.

- Assert SCSI Control
  Outputs the value of the SCSI bus control register to the SCSI bus.
  In initiator mode $\overline{ACK}$ and $\overline{ATN}$ signals can be asserted.
  In target mode $\overline{REQ}$, $\overline{MSG}$, $\overline{C/D}$ and $\overline{I/O}$ signals can be asserted.
  This instruction is only needed in program I/O transfer.
  On program I/O, see 5-1.

- Deassert SCSI Control
  Prohibits the content of the SCSI bus control register from being output to the SCSI bus.
  Once the "Assert SCSI Control" command is executed, some of the SCSI bus control signals are output from the SCSI bus control register until this command is executed.

- Assert SCSI Data
  Outputs the value of the SCSI data register to the SCSI bus.
  However, data is not output in the following circumstances :

  i) A phase change interrupt (PHC) is generated in initiator mode.
  ii) In initiator receive mode (SCSI bus $\overline{I/O}$ signal is high).
  iii) In target receive mode (SCSI bus $\overline{I/O}$ signal is low).
  iv) The mode is neither initiator nor target.

  This instruction is only needed in program I/O transfer.
  On program I/O, see 5-1.

- Deassert SCSI Data
  Prohibits the value of the SCSI data register from being output to the SCSI bus.
  Once the "Assert SCSI Data" command is executed, the SCSI bus data signals are output from the SCSI data register until this command is executed.

2-2. Commands valid in disconnected status

The following commands are valid only in disconnected status. If any of these commands are issued in any other state, the CIP bit and the content of the command register are cleared immediately.

- Reselect
  This command executes arbitration/reselection from disconnected status.
  When this command is executed, the CXD1185AQ switches to the target mode.
  Before issuing this command, the owner ID (OID2-0) and target ID (TID 2-0) values must be written in the SCSI ID register.

- Select without $\overline{ATN}$
  This command executes arbitration/selection from disconnected status.
  When this command is executed, the CXD1185AQ switches to the initiator mode. Before issuing this command, the owner ID (OID2-0) and target ID (TID2 -0) values must be written in the SCSI ID register.

- Select with $\overline{ATN}$
  This command executes arbitration/selection from disconnected status.
  During selection the $\overline{ATN}$ signal is driven on the SCSI bus.
  When this command is executed, the CXD1185AQ switches to the initiator mode. Before issuing this command, the owner ID (OID2-0) and target ID (TID2-0) values must be set in the SCSI ID register. If, after this command is executed, message-out phase is to be terminated, the "Deassert $\overline{ATN}$" command must be executed prior to the transfer of the last message byte.

• Enable Selection/Reselection
Activates selection/reselection interrupts.
When this command is executed, the FNC bit is set immediately and the contents of the CIP bit and command register are cleared. Once this command is executed, RSL/SWA/SWOA interrupts (in interrupt request 1 register) are set during selection/reselection phase. When one of the selection/reselection is executed this will occur before the FNC interrupt.

Selection/reselection is also enabled after the following events.
- ○ Hardware reset
- ○ Execution of "Reset Chip"
- ○ Assertion of SCSI bus $\overline{RST}$ signal
- ○ Disconnect in initiator mode

• Disable Selection/Reselection
Prohibits any response to selection/reselection.
Once this command is executed, the RSL/SWOA/SWA interrupts in interrupt request register 1 will not be generated.

2-3. Commands valid in target status
The following commands are valid only in target status.
If any of these commands are issued in any other state, the CIP bit and the Content of the command register are cleared immediately.
In the case of data send commands, the transfer data must not be written before the command is written in the command register and the necessary SCSI phase change is confirmed by software. In target mode, handshaking on the SCSI bus is terminated under the following conditions :

1. The $\overline{REQ}$ signal is in any state and if :
   - ○ a hardware reset is performed.
   - ○ the "Reset Chip" command is executed.
   - ○ the SCSI bus $\overline{RST}$ pin is driven.

2. The command completes with $\overline{REQ}$ inactive if :
   - ○ a parity error is generated on the SCSI bus or the data bus. (However, this is not the case if the mode register HDPE and HSPE bits are set to "0".)
   - ○ the SCSI bus $\overline{ATN}$ signal is driven. (However, this is not the case if the mode register HATN bit is set to "0".)
   - ○ while the transfer byte counter is in use :
     the DMA bit is set to "1", the status register TRBZ bit is set to "1" and the FIFO status register FIE bit is set to 1, or in receive mode, the DMA bit is set to "0" and the status register TRBZ bit is set to "1".
   - ○ While executing a single byte transfer :
     the mode is send and the FIE bit is set to "1",
     or the mode is receive and FIFO status register bits FC3-FC0 are all set to "1".

3. Handshaking is temporarily interrupted with $\overline{REQ}$ inactive if :
   - ○ while the transfer byte counter is in use :
     the mode is send and the FIFO status register FIE bit is set to "1",
     or the mode is receive and the FIFO status register FIF bit is set to "1".
   - ○ during synchronous transfer, the difference in the number of $\overline{REQ}$s and $\overline{ACK}$s reaches the offset specified in the synchronous transfer register.
   - ○ the mode is receive, during synchronous transfer, the number of FIFO bytes remaining is fewer than the offset specified in the synchronous transfer register.

- Send Message
  The CXD1185AQ changes the phase to Message In by making the SCSI bus $\overline{MSG}$ and $\overline{I/O}$ signals active and the $\overline{C/D}$ signal inactive. The message bytes are then sent.
  If there is more than one message byte or if the message must be sent all at once, the transfer byte counter must be used.

- Send Status
  The CXD1185AQ changes the phase to Status and sends the status byte to the initiator.
  It makes the SCSI bus $\overline{I/O}$ and $\overline{C/D}$ signals active and the $\overline{MSG}$ signal inactive.

- Send Data
  The CXD1185AQ changes the phase to Data In and sends the data bytes to the initiator.
  It makes the SCSI bus $\overline{I/O}$ signal active and $\overline{MSG}$ and $\overline{C/D}$ signals inactive.
  If more than one data byte must be sent all at once, the transfer byte counter must be used.

- Disconnect
  Makes all SCSI signals inactive, except for the $\overline{RST}$ signal.

- Receive Message Out
  The CXD1185AQ changes the phase to Message In and receives the message bytes from the initiator.
  It makes the SCSI bus $\overline{MSG}$ signal active and the $\overline{I/O}$ and $\overline{C/D}$ signals inactive.
  If there is more than one message byte or if the message must be received all at once, the transfer byte counter must be used.

- Receive Command
  The CXD1185AQ changes the phase to Command and receives the command bytes from the initiator.
  It makes the SCSI bus $\overline{C/D}$ signal active and the $\overline{MSG}$ and $\overline{I/O}$ signals inactive.
  If the command bytes must be received all at once, the transfer byte counter must be used.

- Receive Data
  The CXD1185AQ changes the phase to Data Out and receives the data bytes from the initiator.
  It makes the SCSI bus $\overline{MSG}$, $\overline{C/D}$ and $\overline{I/O}$ signals inactive and received the data bytes.
  If more than one data byte must be received all at once, the transfer byte counter must be used.

2-4. Commands valid in initiator status

The following commands are valid only in initiator status.
If any of these commands are issued in any other state, the CIP bit and the content of the command register are cleared immediately.
In the case of data send commands, the transfer data must not be written before the command is written in the command register.
Once the execution of a transfer command is commenced in initiator mode, handshaking on the SCSI bus is terminated under the following conditions:

1. The $\overline{ACK}$ signal is in any status and if :
   - ○ a hardware reset is performed.
   - ○ the "Reset Chip" command is executed.
   - ○ the SCSI bus $\overline{RST}$ pin is driven.

2. The command completes with $\overline{ACK}$ inactive if :
   - ○ phase change occurs and PHC bit in interrupt request register 2 is set to "1".
     If this is the case and the DMA bit is set to "1", the DRQ signal also remains inactive.
   - ○ while the transfer byte counter is in use :
     the DMA bit is set to "1", the status register TRBZ bit is set to "1" and the FIFO status register FIE

bit is set to 1, or in receive mode, the DMA bit is set to"0" and the status register TRBZ bit is set to "1".

- ○ while executing a single byte transfer :
  the mode is send and the FIE bit is set to 1,
  or the mode is receive, FIFO status register FIE bits FC3-FC0 are all set to "1".

3. The command completes with $\overline{ACK}$ active if :
   - ○ the mode is receive and a parity error occurs on the SCSI bus. (However, this is not the case if the mode register HSPE bit is set to "0".)
   - ○ status is message-in phase, the TRBE bit is set to "0", the $\overline{REQ}$ signal is active and a 1-byte message is received.

   Note that in the above two cases the "Deassert $\overline{ACK}$" command must be executed afterwards.

4. Handshaking is temporarily interrupted with $\overline{ACK}$ inactive if :
   - ○ while the transfer byte counter is in use :
     the mode is send and the FIFO status register FIE bit is set to "1".
   - ○ during synchronous transfer , the difference in the number of $\overline{REQ}$s and $\overline{ACK}$s reaches the offset specified in the synchronous transfer register.
   - ○ during synchronous transfer, the number of FIFO bytes remaining is fewer than the offset specified in the synchronous transfer register.

5. Handshaking is temporarily interrupted with $\overline{ACK}$ active if :
   - ○ while the transfer byte counter is in use :
     the mode is receive and the FIFO status register FIF bit is set to "1".

- Transfer Information
  In the initiator mode, causes data transfer to take place.

- Transfer Pad
  In the initiator mode, causes data transfer to take place.
  Note that unlike "Transfer Information", the data output by the CXD1185AQ are all "0"s and parity generation is not performed.
  In addition, no parity check is performed on any data input to the CXD1185AQ.
  Except for these two exceptions, this command is identical to the "Transfer Information" command.

- Deassert $\overline{ACK}$
  Makes the SCSI $\overline{ACK}$ signal inactive.

- Assert $\overline{ATN}$
  Makes the SCSI $\overline{ATN}$ signal active.

- Deassert $\overline{ATN}$
  Makes the SCSI $\overline{ATN}$ signal inactive. After executing the "Select with $\overline{ATN}$" or "Assert $\overline{ATN}$" command, the SCSI bus $\overline{ATN}$ signal remains active until this command is executed.

3. Reset Operation

There are four initializing methods for the CXD1185AQ:

- hardware reset
- execution of the "Reset Chip" command
- assertion of $\overline{RST}$ signal on the SCSI bus
- disconnection

3-1. Hardware reset

This returns the CXD1185AQ to its initial status.
However, environment setting register bit 1 (FS1) is set to "1", making the initial clock division ratio to "4".
All of the internal circuits are also initialized.

3-2. Execution of the "Reset Chip" command

CXD1185AQ can be initialized by "Reset Chip" command (command code "01"). This command is effective regardless of the CIP bit in the status register.
This command resets all registers with the exception of the environment setting register.
All read only registers except for bits 7 and 6 of the status register and the SCSI control monitor register are cleared.
Since the "Reset Chip" command clears all write registers, any SCSI bus signal it used to drive will also be cleared.

3-3. Assertion of $\overline{RST}$ signal on the SCSI bus

When the SCSI bus $\overline{RST}$ signal is active, signals on the SCSI bus being driven by the CXD1185AQ are made inactive with the exception of the $\overline{RST}$ pin.
Bits 4 and 3 (INIT and TARG bits) are also cleared.

3-4. Disconnection

If the CXD1185AQ is operating in initiator mode and a disconnect interrupt is generated, a reset identical to the one in 3-3 takes place.

4. Interrupt Operation

In this section various interrupts, generated by the CXD1185AQ, are discussed in greater detail. If the internal interrupt conditions of the CXD1185AQ are satisfied, "1"s are written to the appropriate bits in interrupt request registers 1 and 2 and the MIRQ bit in the status register. IRQ pin becomes active only if the interrupt is authorised in the interrupt authorization registers.

4-1. Arbitration interrupts

When a selection command is executed, the CXD1185AQ waits for bus free. Once bus free is detected it outputs the $\overline{BSY}$ signal and the owner ID to the SCSI bus and enters arbitration. If, during arbitration, another device with higher priority enters arbitration or if the $\overline{SEL}$ signal is driven on the SCSI bus, arbitration fails and ARBF is set to "1". The FNC bit is also set a while later. If arbitration is successful it enters selection phase.

4-2. Interrupts when selected/reselected

After "Enable Selection /Reselection" is executed, if the owner ID and the $\overline{SEL}$ signal appear on the SCSI bus, SWOA bit is set to "1". If $\overline{ATN}$ signal also appear at the same time, SWA bit is set instead. If $\overline{I/O}$ signal appears instead of $\overline{ATN}$ signal, then, RSL is set.

4-3. Interrupts when selection/reselection command is executing

CXD1185AQ enters arbitration and after obtaining the right to use the SCSI bus it enters selection/reselection phase by sending the target ID, the owner ID and $\overline{SEL}$ signal onto the bus. At this point, the value of the selection/reset timer register is loaded into the hardware timer (not user accessible) and decrementing begins. Note that TMSL bit in the mode register must be "1" for the loading to take place. If there is no response from the target device by the time the hardware timer reaches "0", selection time over occurs and the STO bit is set to "1" and, afterward, the FNC bit is set to "1".

4-4. Data transfer phase interrupts

- The RMSG and PHC bits are valid interrupts only when INIT bit (status register bit 4) is set to "1". Also, the DATN bit is valid only when the TARG bit (status register bit 3) is set to "1". The SPE and DPE bits are valid both in initiator and target modes.
- The RMSG bit is set to "1", if, in initiator mode, the target device activates $\overline{REQ}$ after changing the SCSI bus phase to either Message-In or Message-Out. If the message is of multiple byte, it is set each time $\overline{REQ}$ is activated.
- The PHC bit is set to "1", if, in initiator mode, the target device activates $\overline{REQ}$ after changing the SCSI bus phase. If the new phase is either Message-In or Message-Out, RMSG bit is also set to "1".
- The DATN bit is set to "1", if, in target mode, the initiator asserts $\overline{ATN}$ on the SCSI bus. Once the interrupt request register 2 is read by the CPU the bit is cleared even if $\overline{ATN}$ continues to be active.
- The SPE bit is set when a parity error is detected on the SCSI bus during receive mode data transfer in both initiator and target mode. In initiator mode, it is set on receiving the $\overline{REQ}$. In target mode it is set on receiving the $\overline{ACK}$. The SPE bit is also set if parity error is detected during selection/reselection.
- DPE bit is set when a parity error is detected on the data bus while writing data into FIFO. It is set at the rise of the FIFO write signal, $\overline{WED}$. This bit is valid only if the DPEN bit in the environment setting register is set to "1". If the SDPM bit in the environment register is "1", even parity check is carried out. Otherwise odd parity check is carried out.

4-5. Other interrupts

- The SRST bit is set to "1" when the SCSI bus $\overline{RST}$ signal becomes active. It is also set if the "Assert $\overline{RST}$" command is executed and the CXD1185AQ drives the $\overline{RST}$ pin.
- The DCNT bit is set to "1" if the CXD1185AQ is operating in the initiator mode and the target device makes the $\overline{BSY}$ signal on the SCSI bus inactive. Normally, in initiator mode, this bit is set at the end of a series of SCSI operation when the SCSI bus phase becomes bus free.

5. Data Transfer

In this section procedures for transferring data to and from the CXD1185AQ is described. Data can be transferred between the CPU and the CXD1185AQ in the following three ways:

1. Program I/O transfer
2. CPU I/O transfer
3. DMA transfer

5-1. Program I/O transfer

This method is used to transfer data between the CPU bus and the CXD1185AQ. The CPU manages SCSI handshaking entirely through software. By issuing the "Assert SCSI Control" and "Assert SCSI Data" commands, all of the SCSI bus bits can be software controlled. After the above two commands are issued, values can be written to the SCSI bus control register and the SCSI data register to carry out the SCSI handshake.

When the "Assert SCSI Data" command is issued, the CXD1185AQ internal FIFO counter is fixed at "0". As a result, only one byte of data can be received by the data register. Reading the SCSI data register results in reading the SCSI data bus directly. If the CXD1185AQ is in neither initiator nor target mode (status register bits 4 and 3 both set to "0"), none of the bits in the SCSI bus control register can be output to the SCSI bus except ABSY and ASEL. If the CXD1185AQ is in initiator mode, the AACK and AATN bits are output to the SCSI bus. In the target mode, the AMSG, ACD, AIO and AREQ bits are output.

When phase change (PHC) interrupt occur in initiator mode, output to the SCSI data bus is inhibited. In such case, read the SCSI control monitor register and watch the phase in the SCSI control register with that of the SCSI bus. When "Assert SCSI Control" instruction is executed in target mode, pins on the SCSI bus, except $\overline{BSY}$, are released.

The phase can be controlled by setting appropriate values to the SCSI bus control register. The contents of the SCSI control register and/or SCSI data register are output continually after "Assert SCSI Control" and/or "Assert SCSI data". Therefore, when program I/O transfer is completed the "Deassert SCSI Control "or" Deassert SCSI Data" command must be written to the command register.

5-2. CPU I/O transfer

This method is used to transfer data between the CPU bus and the CXD1185AQ without using DMA. Transfer commands can be issued when the CPU is in either the initiator or the target mode. When issuing these commands, command register bit 5 (DMA) must be set to "0".

- Outputting data to the SCSI bus
  During the transfer, the CPU must monitor the FIFO status and make sure that it does not attempt to write to the FIFO when it is full (FIFO is full when FIF bit in the FIFO status register is "1") (*). In target mode, after issuing the transfer command, the CPU must check that the SCSI bus phase is changed to the appropriate phase, by software, before any transfer data is written.

  (*) Before writing a value to the data register a transfer command must be written to the command register.

- Reading data from the SCSI bus
  After a transfer command is written to the command register, the CPU must monitor the FIE bit in the FIFO status register so as to make sure that it does not attempt to read an empty FIFO. The CPU must monitor the FNC bit in the status register to detect the end of transfer. The CPU, at the end of the transfer, must continue to read any remaining data in the FIFO.

5-3. DMA transfer

This method is used to transfer data between the Data bus and the CXD1185AQ. Transfer commands can be issued when the CPU is in either the initiator or the target mode. When issuing commands command register bits 5 (DMA) and 4 (TRBE) must be set to "1". When a transfer is initiated the DRQ pin (Pin 43) becomes active. Then, when the $\overline{\text{DACK}}$ pin (Pin 44) becomes active, the DRQ pin becomes inactive (when mode register bit 0 (BDMA) is set to "0") and one byte of data is either written to or read from the FIFO. If the environment setting register bit 5 (DPEN) is set to "1", the data bus parity is calculated from the DP pin (Pin 55). During reads the parity bit is generated, and during writes parity bit check takes place. During DMA transfer, the CPU bus and data register are cut off. Hence, data register reads/writes from the CPU are ignored.

6. Programming Overview

The CXD1185AQ supports SCSI phase level commands. As a result, when it is operating it is possible to perform programming without imposing a burden on the software. In this section actual methods for programming CXD1185AQ are introduced along with an explanation of all SCSI phases, assuming that the CXD1185AQ is in the initiator mode.

〈 Initial settings 〉

The CXD1185AQ is completely initialized when the power is turned on or after a hardware reset. Therefore, the following initial settings must be performed.

① Environment setting register initialization
The enviroment setting register is set to an initial value and initial clock division ratio of "4". Therefore, a new appropriate value must be written to match the external clock frequency as described in section 1-5. If required, "1"s must be written to the other bits at the same time.

② "Reset Chip" command execution

The new clock division ratio becomes valid only after executing the "Reset Chip" command. (The other bits are valid as soon as they are written.) Therefore, if the clock division ratio is to be changed, the "Reset Chip" command must be executed after changing the FSI and FSO bits in the environment setting register.

〈 Arbitration/selection execution 〉

③ SCSI ID setting

The owner ID and target ID must be written to the SCSI ID register to prepare for selection.

④ Arbitration/selection

Write "1"s to some of the bits of interrupt authorization registers 1 and 2 (ARBF, STO, FNC, etc.) as required. Write "Select with $\overline{ATN}$" command into the command register. If message-out phase is not necessary after selection, instead, write "Select without $\overline{ATN}$" command. In this example "Select with $\overline{ATN}$" is assumed. Wait for the CIP bit in the status register to become "1" and read the interrupt request registers.

If arbitration failed and ARBF bit is "1", repeat ④. Normally, if selection time over occurs and STO bit set to "1", "Assert $\overline{RST}$" command is executed.

〈 Message-out phase execution 〉

⑤ Switching to the message-out phase

Wait until the target device switches the SCSI bus to the message-out phase (PHC bit set to "1").

⑥ Halting $\overline{ATN}$ signal drive

Execute "De-assert $\overline{ATN}$" command to inactivate the $\overline{ATN}$ signal on the SCSI bus.

⑦ Sending message byte

Confirm that the CIP bit is "0" in the status register. Write "Transfer Information" command to the command register (DMA bit and TRBE bit are set to "0"s for a single byte message). Write the message byte into the SCSI data register. After confirming that the CIP bit is to "0", read interrupt request registers 1 and 2.

〈 Command phase execution 〉

⑧ Switching to the command phase

Wait until the target device switches the SCSI bus to the command phase (PHC bit set to "1").

⑨ Command send

Set the number of command bytes in the transfer byte counter. Write "Transfer Information" command into the command register. (this time set the TRBE bit to "1" and DMA bit to "0"). Write the command bytes into the SCSI data register. After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.

〈 Data-in phase execution 〉

⑩ Switching to the data-in phase
Wait until the target device switches the SCSI bus to the data-in phase (PHC bit set to "1").

⑪ Data receive
Set the number of transfer data bytes in the transfer byte counter. Write "Transfer Information" command into the command register (with both DMA bit and TRBE bit set to "1"). Note that programming of DMA controller is also required before starting DMA transfer. After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.

〈 Status phase execution 〉

⑫ Switching to the status phase
Wait until the target device switches the SCSI bus to the status phase (PHC bit set to "1").

⑬ Status receive
Write "Transfer Information" command in the command register (both DMA bit and TRBE bit are "0"). After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.
The status byte is read from the data register.

〈 Message-in phase execution 〉

⑭ Switching to the message-in phase
Wait until the target device switches the SCSI bus to the message-in phase (PHC bit set to "1").

⑮ Message receive
Write "Transfer Information" command in the command register (both DMA bit and TRBE bit are "0"). After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2. The message byte is read from the data register.

⑯ Halting $\overline{\text{ACK}}$ signal drive
Message-In is exceptional in that after the message byte is read, $\overline{\text{ACK}}$ is not inactivated automatically. "Deassert $\overline{\text{ACK}}$" command must be executed to inactivate $\overline{\text{ACK}}$ signal.
Write " Deassert $\overline{\text{ACK}}$" command in the command register. After confirming that the CIP bit is "0", read the interrupt request registers.

〈 Disconnect 〉

⑰ Wait until the DCNT bit is set to "1".
All SCSI phases are covered in ① - ⑰ above. If a disconnect message is sent from the target device when in the data phase, the status phase is skipped and processing continues with the message in phase. When reselection is performed from the target device (RSL bit set to "1"), it is necessary to wait until the FNC bit is set to "1". Then read the monitor SCSI control register and perform the processing appropriate for the current SCSI phase.

Appendix A

Register Summary

READ

	7	6	5	4	3	2	1	0	Register
R0	MRST	MDBP		INIT	TARG	TRBZ	MIRQ	CIP	Status register
R1									Data register
R2				STO	RSL	SWA	SWOA	ARBF	Interrupt request register 1
R3	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt request register 2
R4	MBSY	MSEL	MMSG	MCD	MIO	MREQ	MACK	MATN	SCSI control monitor register
R5	FIE			FIF	FC3	FC2	FC1	FC0	FIFO status register
R6	TID2	TID1	TID0			OID2	OID1	OID0	SCSI ID register
R7									Transfer byte counter (low)
R8									Transfer byte counter (middle)
R9									Transfer byte counter (high)
RA				STO	RSL	SWA	SWOA	ARBF	Interrupt authorization register 1
RB	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt authorization register 2
RC	HDPE	HSPE	HATN	TMSL	SPHI			BDMA	Mode register
RD	TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0	Synchronous transfer register
RE	ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN	SCSI bus control register
RF	PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0	I/O port register

WRITE

	7	6	5	4	3	2	1	0	Register
R0	CAT1	CAT0	DMA	TRBE	CMD3	CMD2	CMD1	CMD0	Command register
R1									Data register
R2									⟨ * ⟩
R3	DIFE	SDPM	DPEN	SIRM			FS1	FS0	Environment setting register
R4									Selection/reset timer register
R5									⟨ * ⟩
R6	SID2	SID1	SID0			OID2	OID1	OID0	SCSI ID register
R7									Transfer byte counter (low)
R8									Transfer byte counter (middle)
R9									Transfer byte counter (high)
RA				STO	RSL	SWA	SWOA	ARBF	Interrupt authorization register 1
RB	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt authorization register 2
RC	HDPE	HSPE	HATN	TMSL	SPHI			BDMA	Mode register
RD	TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0	Synchronous transfer register
RE	ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN	SCSI bus control register
RF	PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0	I/O port register

⟨ * ⟩ No register assigned to this address.

Appendix B

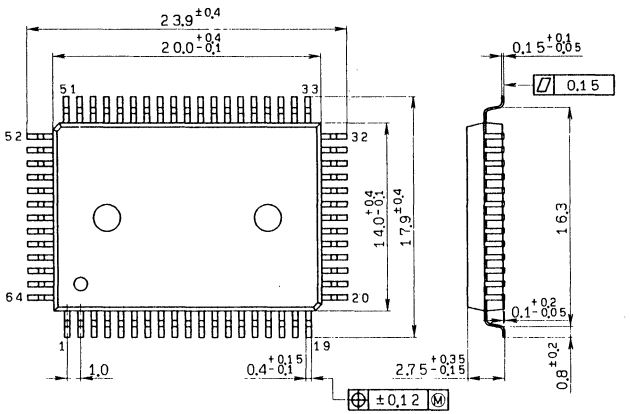
Command Summary

Category	DMA	TRBE	Command code	Command
0 0	0	0	0 0 0 0	No Operation
	0	0	0 0 0 1	Reset Chip
	0	0	0 0 1 0	Assert $\overline{RST}$
	0	0	0 0 1 1	Flush FIFO
	0	0	0 1 0 0	Assert SCSI Control
	0	0	0 1 0 1	Deassert SCSI Control
	0	0	0 1 1 0	Assert SCSI Data
	0	0	0 1 1 1	Deassert SCSI Data
0 1	0	0	0 0 0 0	Reselect
	0	0	0 0 0 1	Select without $\overline{ATN}$
	0	0	0 0 1 0	Select with $\overline{ATN}$
	0	0	0 0 1 1	Enable Selection/Reselection
	0	0	0 1 0 0	Disable Selection/Reselection
1 0	*	*	0 0 0 0	Send Message
	*	*	0 0 0 1	Send Status
	*	*	0 0 1 0	Send Data
	0	0	0 0 1 1	Disconnect
	*	*	0 1 0 0	Receive Message Out
	*	*	0 1 0 1	Receive Command
	*	*	0 1 1 0	Receive Data
1 1	*	*	0 0 0 0	Transfer Information
	*	*	0 0 0 1	Transfer Pad
	0	0	0 0 1 0	Deassert $\overline{ACK}$
	0	0	0 0 1 1	Assert $\overline{ATN}$
	0	0	0 1 0 0	Deassert $\overline{ATN}$

〈 * 〉 Don't care.
However, if the DMA bit is set to "1", the TRBE bit is always also set to "1".

Package Outline Unit: mm

64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	

SONY

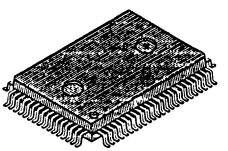
CXD1186Q

CD-ROM Decoder

Description

CXD1186Q is a CD-ROM decoder LSI.

80pin QFP (Plastic)



Features

- Corresponds to CD-ROM, CD-I and CD-ROM XA formats.
- Real time error Correction. (Erasure Correction using C2 pointer from CD player.)
- Double speed playback.
- Connection to standard SRAM up to 64K bytes, as buffer memory, possible.

Applications

CD-ROM driver

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C)

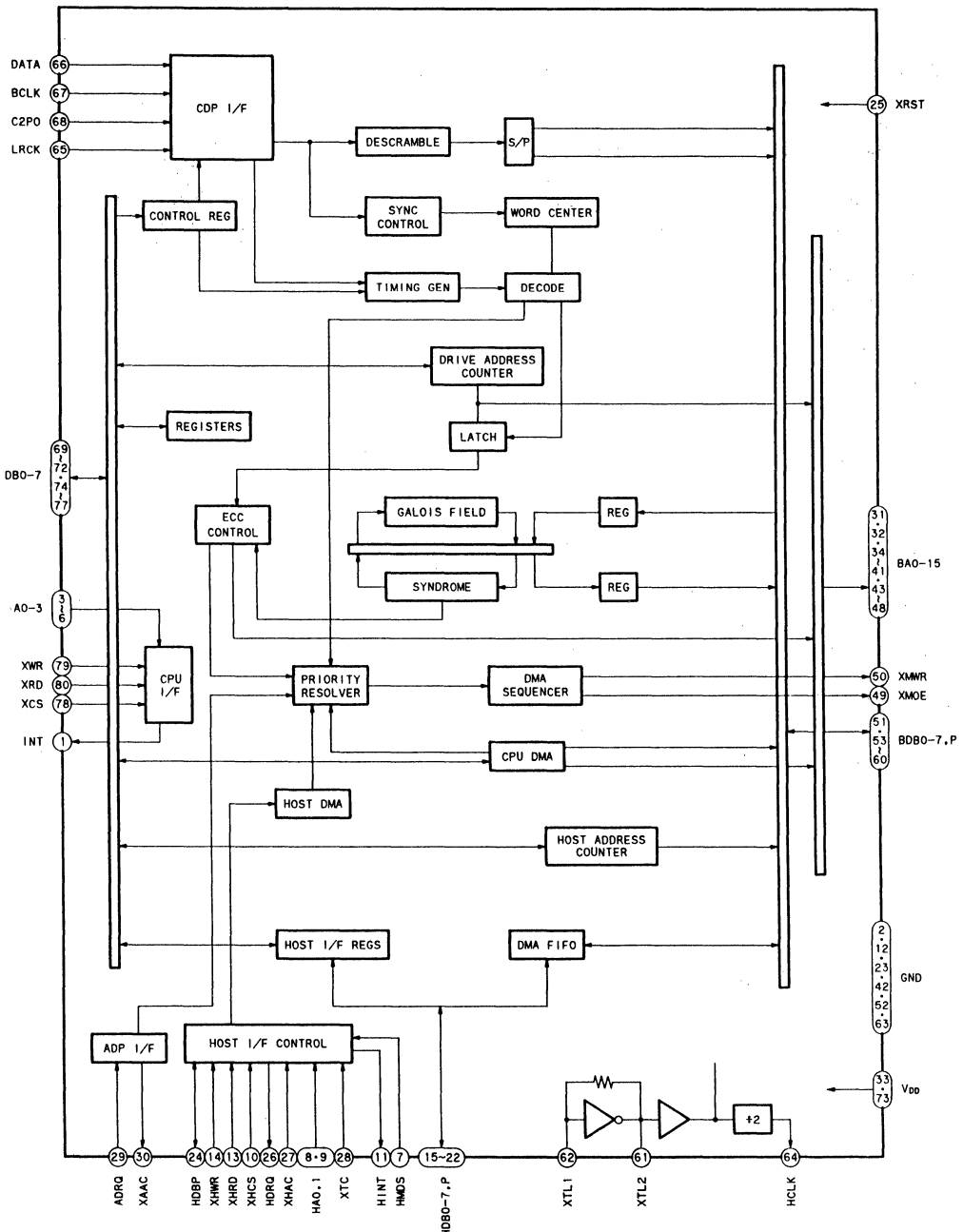
• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_I	−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	−0.5 to V_{DD}+0.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+4.5 to +5.5 (standard+5.0)	V
• Operating temperature	T_{opr}	−20 to +75	°C

E90765-HP

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	INT	O	Interrupt request signal VS, CPU
2	GND	—	GND pin
3	A0	I	CPU address signal
4	A1	I	CPU address signal
5	A2	I	CPU address signal
6	A3	I	CPU address signal
7	HMDS	I	Host mode select signal
8	HA0	I	Host address signal
9	HA1	I	Host address signal
10	XHCS	I	Chip select negative logic signal from host
11	HINT	O	Interrupt request negative logic signal to host
12	GND	—	GND pin
13	XHRD	I/O	Data read strobe signal from host or to SCSI control IC
14	XHWR	I/O	Data write strobe signal from host or to SCSI control IC
15	HDB0	I/O	Host data bus
16	HDB1	I/O	Host data bus
17	HDB2	I/O	Host data bus
18	HDB3	I/O	Host data bus
19	HDB4	I/O	Host data bus
20	HDB5	I/O	Host data bus
21	HDB6	I/O	Host data bus
22	HDB7	I/O	Host data bus
23	GND	—	GND pin
24	HDBP	I/O	Error flag, Host data bus
25	XRST	I	Reset negative logic signal
26	HDRQ	O	Data request positive logic signal to host. Or DMA aknowledge negative logic signal to SCSI control IC
27	XHAC	I	DMA aknowledge negative logic signal from host. Or data request positive logic signal from SCSI control IC
28	XTC	I	Terminal count negative logic signal
29	ADRQ	I	DMA request positive logic signal from ADP
30	XAAC	O	DMA aknowledge negative logic signal
31	BA0	O	Buffer memory address
32	BA1	O	Buffer memory address
33	V_{DD}	—	Power (+5V) supply pin
34	BA2	O	Buffer memory address
35	BA3	O	Buffer memory addres
36	BA4	O	Buffer memory address
37	BA5	O	Buffer memory address
38	BA8	O	Buffer memory address
39	BA7	O	Buffer memory address

Pin No.	Symbol	I/O	Description
40	BA8	O	Buffer memory address
41	BA9	O	Buffer memory address
42	GND	—	GND pin
43	BA10	O	Buffer memory address
44	BA11	O	Buffer memory address
45	BA12	O	Buffer memory address
46	BA13	O	Buffer memory address
47	BA14	O	Buffer memory address
48	BA15	O	Buffer memory address
49	XMOE	O	Buffer memory output enable negative logic signal
50	XMWR	O	Buffer memory write negative logic signal
51	BDB0	I/O	Buffer memory data bus
52	GND	—	GND pin
53	BDB1	I/O	Buffer memory data bus
54	BDB2	I/O	Buffer memory data bus
55	BDB3	I/O	Buffer memory data bus
56	BDB4	I/O	Buffer memory data bus
57	BDB5	I/O	Buffer memory data bus
58	BDB6	I/O	Buffer memory data bus
59	BDB7	I/O	Buffer memory data bus
60	BDBP	I/O	Buffer memory pointer data bus
61	XTL2	O	Crystal oscillation circuit output pin
62	XTL1	I	Crystal oscillation circuit input pin
63	GND	—	GND pin
64	HCLK	O	1/2 frequency divided clock signal of XTL1
65	LRCK	I	LR clock from CD player
66	DATA	I	Serial data from CD player
67	BCLK	I	Bit clock from CD player
68	C2PO	I	C2 pointer from CD player
69	DB0	I/O	CPU data bus
70	DB1	I/O	CPU data bus
71	DB2	I/O	CPU data bus
72	DB3	I/O	CPU data bus
73	V_{DD}	—	Power (+5V) supply pin
74	DB4	I/O	CPU data bus
75	DB5	I/O	CPU data bus
76	DB6	I/O	CPU data bus
77	DB7	I/O	CPU data bus
78	XCS	I	Chip select negative logic signal from CPU
79	XRD	I	CPU Strobe negative logic signal to read out this IC internal register
80	XWR	I	CPU strobe negative logic signal to write in this IC internal register

Electrical characteristics

DC characteristics $V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_{OP}=-20$ to $75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH1}		2.2			V
	L level	V_{IL1}				0.8	V
TTL SCHMITT hysterisis		$V_{t+}-V_{t-}$		0.2	0.4		V
Input current of pull up input		I_{IL}	$V_{IL}=0V$	−40	−100	−240	μA
Input current of pull down input		I_{IH}	$V_{IH}=V_{DD}$	40	100	240	μA
Output voltage	H level	V_{OH1}	$I_{OH}=-2mA$	$V_{DD}-0.8$			V
	L level	V_{OL1}	$I_{OL}=4mA$			0.4	V
Open drain output L level		V_{OL2}	$I_{OL}=4mA$			0.4	V
Oscillation cell Input voltage	H level	V_{IH}		$0.7V_{DD}$			V
	L level	V_{IL}				$0.3V_{DD}$	V
Logic threshold value		LV_{th}			$V_{DD}/2$		V
Feedback resistance		R_{FB}	$V_{IN}=V_{SS}$ or V_{DD}	500K	1M	2M	Ω
Output voltage	H level	V_{OH}	$I_{OH}=-8mA$	$V_{DD}/2$			V
	L level	V_{OL}	$I_{OL}=8mA$			$V_{DD}/2$	V

- Input pin with pull up resistance : XHCS, HA0, HA1, XTC
- Input pin with pull down resistance : C2PO, HMDS, ADRQ
- TTL Schmitt input pin : XRST
- Open drain output pin : HINT
- Two-way data bus always pulled up.
- Oscillation cell
  Input : XTL1
  Output : XTL2

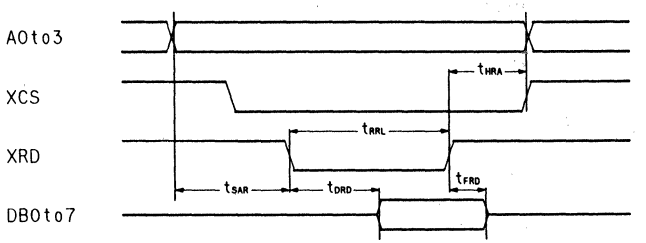
I/O capacitance $V_{DD}=V_I=0V$, $f=1MHz$

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
I/O pin	$C_{I/O}$			11	pF

AC Characteristics (Ta=−20 to 75°C, V_{DD}=5V±10%, Output Load=50pF, f ≤ 24.576MHz)

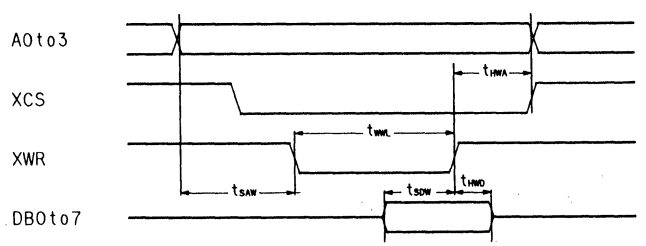
1. CPU Interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XCS & XRD ↓)	t_{SAR}	30			n
Address hold time (vs. XCS & XRD ↑)	t_{HRA}	20			n
Data delay time (vs. XCS & XRD ↓)	t_{DRD}			60	n
Data float time (vs. XCS & XRD ↑)	t_{FRD}	0		10	n
Low level XRD pulse width	t_{RRL}	100			n

(2) Write

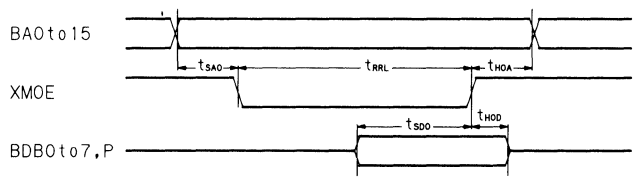


Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XCS & XWR ↓)	t_{SAW}	30			n
Address hold time (vs. XCS & XWR ↑)	t_{HWA}	20			n
Data setup time (vs. XCS & XWR ↑)	t_{SDW}	40			n
Data hold time (vs. XCS & XWR ↑)	t_{HWD}	10			n
Low level XWR pulse width	t_{WWL}	50			n

Where & in the chart indicates logical multiplication.

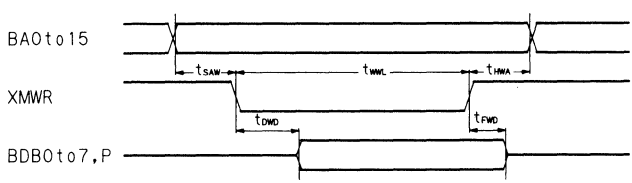
2. Memory interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XMOE ↓)	t_{SAO}	Tw-22			n
Address hold time (vs. XMOE ↑)	t_{HOA}	Tw-9			n
Data setup time (vs. XMOE ↑)	t_{SDO}	45			n
Data hold time (vs. XMOE ↑)	t_{HOD}	0			n
Low level XMOE pulse width	t_{RRL}	2•Tw		2•Tw+16	n

(2) Write



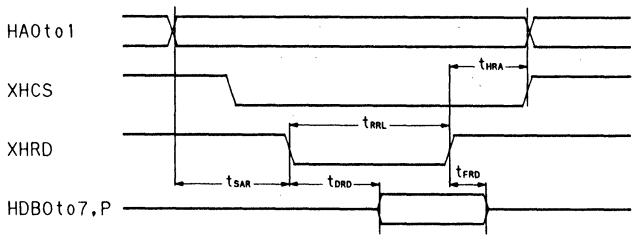
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XMWR ↓)	t_{SAW}	Tw-29			n
Address hold time (vs. XMWR ↑)	t_{HWA}	Tw-9			n
Data delay time (vs. XMWR ↓)	t_{DWD}			0	n
Data float time (vs. XMWR ↑)	t_{FWD}	10			n
Low level XMWR pulse width	t_{WWL}	2•Tw			n

Where Tw=1/f.

Usually, when f=16.934MHz, use a RAM with access time within 120nsec.

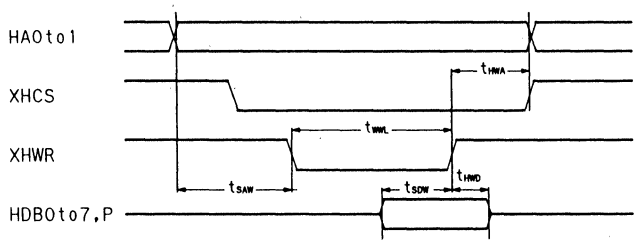
3. Host interface

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHCS & XHRD ↓)	t_{SAR}	30			n
Address hold time (vs. XHCS & XHRD ↑)	t_{HRA}	20			n
Data delay time (vs. XHCS & XHRD ↓)	t_{DRD}			60	n
Data float time (vs. XHCS & XHRD ↑)	t_{FRD}	0		10	n
Low level XHRD pulse width	t_{RRL}	100			n

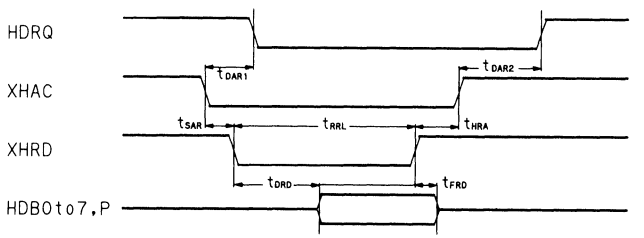
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. XHCS & XHWR ↓)	t_{SAW}	30			n
Address hold time (vs. XHCS & XHWR ↑)	t_{HWA}	20			n
Data setup time (vs. XHCS & XHWR ↑)	t_{SDW}	40			n
Data hold time (vs. XHCS & XHWR ↑)	t_{HWD}	10			n
Low level XHWR pulse width	t_{WWL}	50			n

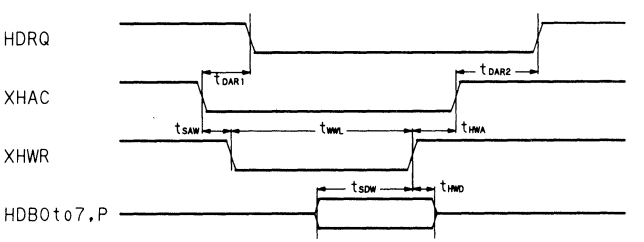
4. HOST DMA cycle (80 type bus)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC ↓)	t_{DAR1}			35	n
HDRQ rise time (vs. XHAC ↑)	t_{DAR2}			48	n
XHAC setup time (vs. XHRD ↓)	t_{SAR}	5			n
XHAC hold time (vs. XHRD ↑)	t_{HRA}	0			n
Low level XHRD pulse width	t_{RRL}	100			n
Data delay time (vs. XHRD ↓)	t_{DRD}			60	n
Data float time (vs. XHRD ↑)	t_{FRD}	0		10	n

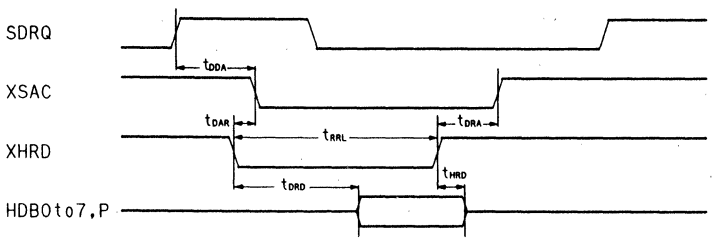
(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
HDRQ fall time (vs. XHAC ↓)	t_{DAR1}			35	n
HDRQ rise time (vs. XHAC ↑)	t_{DAR2}			48	n
XHAC setup time (vs. XHWR ↓)	t_{SAW}	5			n
XHAC hold time (vs. XHWR ↑)	t_{HWA}	0			n
Low level XHWR pulse width	t_{WWL}	50			n
Data setup time (vs. XHWR ↑)	t_{SDW}	40			n
Data hold time (vs. XHWR ↑)	t_{HWD}	10			n

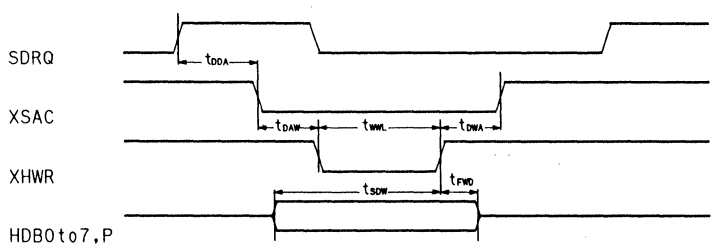
5. HOST DMA cycle (SCSI bus)

(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ ↑)	t_{DDA}			Tw	n
XSAC delay time (vs. XHRD ↓)	t_{DAR}	0			n
XSAC delay time (vs. XHRD ↑)	t_{DRA}			Tw	n
Low level XHRD pulse width	t_{RRL}	T+59			n
Data delay time (vs. XHRD ↓)	t_{DRD}			90	n
Data hold time (vs. XHRD ↑)	t_{HRD}	0			n

(2) Write



Item	Symbol	Min.	Typ.	Max.	Unit
XSAC fall time (vs. SDRQ ↑)	t_{DDA}			Tw	n
XHWR delay time (vs. XSAC ↑)	t_{DAW}			Tw	n
XSAC delay time (vs. XHWR ↑)	t_{DWA}			Tw	n
Low level XHWR pulse width	t_{WWL}	T			n
Data setup time (vs. XHWR ↓)	t_{SDW}	T+24			n
Data float time (vs. XHWR ↓)	t_{FWD}	27			n

Where T in the chart indicates:

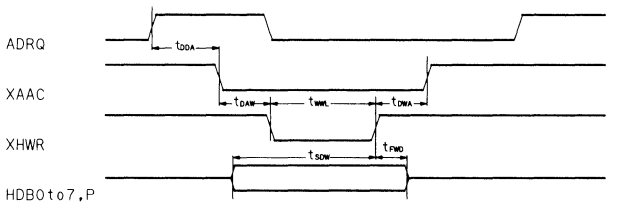
Tw for 3 cycle mode

2•Tw for 4 cycle mode

3•Tw for 5 cycle mode

Here TW=1/f

6. ADPCM DMA cycle



Item	Symbol	Min.	Typ.	Max.	Unit
XAAC fall time (vs. ADRQ ↑)	t_{DDA}			Tw	n
XHWR delay time (vs. XAAC ↓)	t_{DAW}			Tw	n
XAAC delay time (vs. XHWR ↑)	t_{DWA}			Tw	n
Low level XHWR pulse width	t_{WWL}	T			n
Data setup time (vs. XHWR ↓)	t_{SDW}	T+24			n
Data float time (vs. XHWR ↓)	t_{FWD}	27			n

where T in the chart indicates:
Tw for 3 cycle mode
2•Tw for 4 cycle mode
3•Tw for 5 cycle mode
Here Tw=1/f

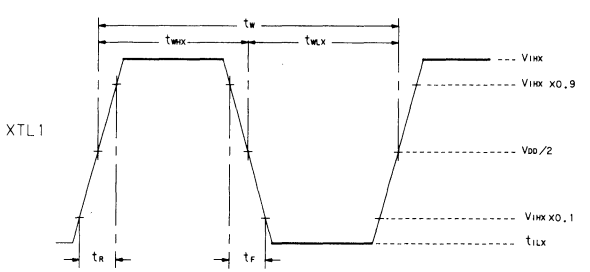
7. XTL1 and XTL2 pins

(1) For Self oscillation (T_{opr}=−20 to 75°C, V_{DD}=5.0V±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	16.9344		24.576	MHz

(2) When a pulse is input to XTL1 (T_{opr}=−20 to 75°C, V_{DD}=5.0V±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
"H" level pulse witdh	t_{WHX}	15			ns
"L" level pulse witdh	t_{WLX}	15			ns
Pulse period	t_W	40.7			ns
Input "H" level	V_{IHX}	V_{DD}−1.0			V
Input "L" level	V_{ILX}			0.8	V
Rise time Fall time	t_R, t_F			15	ns



Description of Function

1. Pin description

Below is a description of pins by function.

1.1 CD player interface (4pins)

(1) DATA (input)
Serial data from CIRC LSI (digital signal processing LSI for CD)

(2) BCLK (input)
Bit clock. Clock for DATA Strobe.

(3) LRCK (input)
LR clock. Indicates L_{CH} and R_{CH} of Data input.

(4) C2PO (positive logic input)
C2 pointer signal from CIRC. Indicates an error is included in the Data input.
Interface mode with the CD player is controlled at DRVIF register.

1.2 Buffer memory interface (27 pins)

(1) XMWR (memory write, negative logic output)
Data write strobe signal of the buffer memory.

(2) XMOE (memory output enable, negative logic output)
Data read strobe signal of the buffer memory.

(3) BA0 to 15 (Buffer memory address, output)
Address signal of the buffer memory.

(4) BDB0 to 7 (Buffer data bus, I/O)
Data bus signal of the buffer memory.

(5) BDBP (Buffer data bus, I/O)
Buffer memory data bus signal for error pointer.

1.3 CPU interface (16 pins)

(1) XWR (CPU write, negative logic input)
Write strobe signal of the CPU register.

(2) XRD (CPU read, negative logic input)
Read out strobe signal of the CPU register.

(3) XCS (CPU chip select, negative logic input)
Chip select negative logic signal from the CPU.

(4) A0 to 3 (CPU address, input)
Address signal for the CPU selection of the IC internal register.

(5) DB0 to 7 (CPU data bus, I/O)
CPU data bus signal.

(6) INT (CPU interrupt, output)
Interrupt request output to the CPU. This pin polarity is controlled at the CONFIG register.

1.4 Host interface (19 pins)

(1) HMDS (Host mode select, input)
Signal for the host mode selection. This pin is pulled down inside the IC by means of a resistor at a standard 50kΩ.
"L" or open: connected to Intel 80 type host Bus.
"H": connected to SCSI controller IC.

(2) HDRQ/XSAC (Host data request/SCSI aknowledge, output)
When HMDS is at "L", DMA data request positive logic signal to host.
When HMDS is at "H", DMA aknowledge negative logic signal to SCSI control IC.

(3) XHAC/SDRQ (Host DMA aknowledge/SCSI data request, input)
When HMDS is at "L", DMA aknowledge negative logic signal from host.
When HMDS is at "H", DMA data request positive logic signal from SCSI control IC.

(4) XHWR (Host write, negative logic I/O)
When HMDS is at "L" and ADMAEN also at "L", data write strobe input from host.
When HMDS is at "H" and ADPCMEN at "L", data write strobe output to SCSI control IC.
When ADMAEN is at "H", data write strobe output to audio processor (ADP).

(5) XHRD (Host read, negative logic I/O)
When HMDS is at "L" and ADMAEN also at "L", data read strobe input from host.
When HMDS is at "H" and ADMAEN at "L", data read strobe output to SCSI control IC.
When ADMAEN is at "H", data read strobe output to ADP.

(6) XHCS (Host chip select, negative logic input)
This pin is pulled up inside the IC by means of a resistor at a standard 50kΩ.
When HMDS is at "L", chip select input from host.
When HMDS is at "H", this signal is not used. Either Fix to "H" or keep open.

(7) HA0 and 1 (Host address, input)
These pins are pulled up inside the IC by means of a resistor at a standard 50kΩ.
When HMDS is at "L", address input from the host.
When HMDS is at "H", these signals are not used. Either fix to "H" or keep open.

(8) HDB0 to 7 (Host data bus, I/O)
Host data bus signal.

(9) HDBP (Host data bus, I/O)
Host data bus signal for error pointer.

(10) HINT (HOST interrupt, output)
This pin is an open drain output.
When HMDS is at "L", interrupt request negative logic output to host.
When HMDS is at "H", this signal is not used.

(11) XTC (Terminal count, negative logic output)
This is pulled up inside the IC by means of a resistor at a standard 50kΩ.
When HMDS is at "L", data transfer complete instruction negative logic input from the host.
When HMDS is at "H", this signal is not used. Either fix to "H" or keep open.

1.5 Audio processor (ADP) interface (2 pins)

(1) ADRQ (audio processor DMA request, positive logic input)
This pin is pulled down inside the IC by means of a resistor at a standard 50kΩ.
DMA data request signal to ADP. When not connected to ADP and CXD1186Q, either fix to "L" or keep open.

(2) XAAC (audio processor DMA aknowledge, negative logic output)
DMA aknowledge signal from ADP.

1.6 Others (4pins)

(1) XTL1 (Chrystal1, input)

(2) XTL2 (Chrystal2, output)
Crystal oscillator connecting pin for master clock oscillation.

(3) HCLK (halfclock, output)
Half frequency divided clock of the master clock.

(4) XRST (Reset, negative logic input)
Chip reset signal.

Pins BDB0 to 7, BDBP, DB0 to 7, HDB0 to 7 and HDBP are pulled up inside the IC by means of a resistor at a standard 25kΩ.

2. Register function

This IC is controlled from the CPU by means of 19 registers for each of write and read, respectively.

2.1 Write register

2.1.1 Drive Interface (DRVIF) register

bit0 : DIGIN (Digital IN)

"H" ; When Digital In (See fig. 2.1.1) is connected, this bit is set to "H".

"L" ; When connected to CIRC LSI, this bit is set to "L".

bits 2 to 5 are effective only when DIGIN is at "L".

bit1 : LSB1ST (LSB First)

"H" ; When data is connected to CIRC LSI output through LSB first, this bit is set to "H".

"L" ; When data is connected to CIRC LSI output through MSB first, this bit is set to "L"

bits 2 and 3: BCKMD0, 1 (BCLK mode 0, 1)

These bits are set according to the number of BCLK clocks output during one word by CIRC LSI.

BCVKMD1	BCKMD0	
"L"	"L"	16BCLKs/Word
"L"	"H"	24BCLKs/Word
"H"	"X"	32BCLKs/Word

More over, when there are 24 or 32 clocks within 1 word, the 16 bits of data before LRCK edge, become effective.

bit4 : BCKRED (BCLK Rising Edge)

"H" ; Data is strobed with BCLK rise.

"L" ; Data is strobed with BCLK fall.

bit5 : LCHLOW (LCH LOW)

"H" ; When LRCK is at "L", it is determined to be L_{CH} data.

"L" ; When LRCK is at "H", it is determined to be L_{CH} data.

※1. When DIGIN="H", We automatically have.

LSBIST=BCKMD1="H", BCKRED=LCHLOW="L".

bit6 : DBLSPD (Double Speed)

"H" ; at double speed PB, this bit is set to "H".

"L" ; at normal speed PB, this bit is set to "L".

bit7 : C2PLIST (C2PO Lower-byte 1st)

"H" ; When 2 bytes of data are input to C2PO, the Lower-byte and the upper-byte are input in the order.

"L" ; When 2 bytes of data are input to C2PO, the Upper-byte and the Lower-byte are input in the order.

Table 2.1.1 indicates the setting value of bits 0 to 7 when Sony made CIRC LSI is connected. Fig. 2.1.1 (1) to (4) indicates the input timing chart.

Here, the upper byte means the upper 8 bits including MSB from CIRC LSI, Lower byte indicates the lower 8 bits including LSB from CIRC LSI.

Changes in value for the respective bits in this register have to be executed in the decoder disable condition.

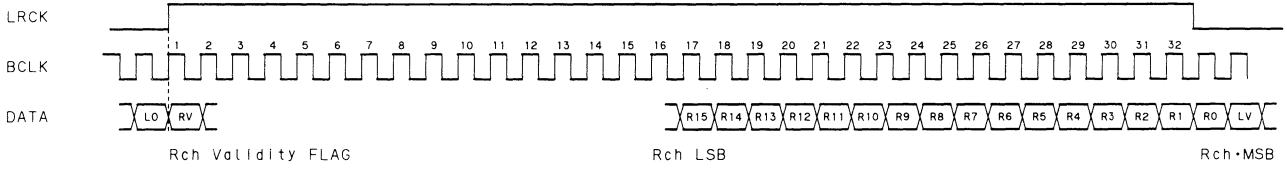


Fig. 2.1.1 (1) Digital In Timing Chart (C2PO don't care, no need for connection)

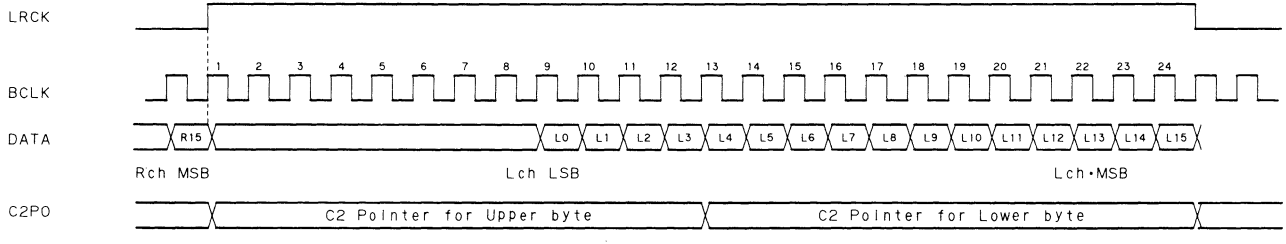


Fig. 2.1.1 (2) CDL30, 35 Series, Timing Chart

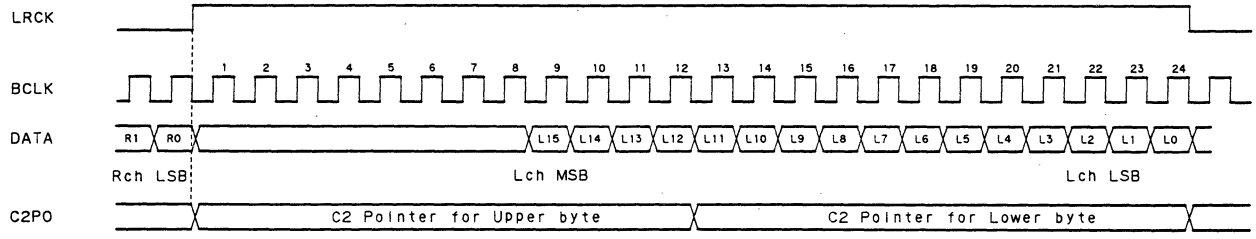


Fig. 2.1.1 (3) CXD2500Q, 48 bit slot mode, timing chart

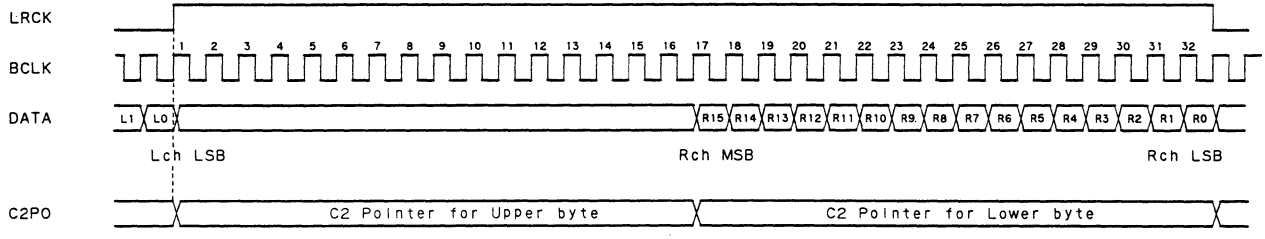


Fig. 2.1.1 (4) CXD2500Q, 64 bit slot mode, timing chart

Table 2.1.1 DRVIF Register setting value

Sony made CIRC LSI	DRV IF Register								Timing chart
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
CDL30 series CDL35 series	L	*	L	L	L	H	L	L	Fig. 2.1.1 (2)
CDL40 series (48bit slot mode)	L	*	L	H	L	H	L	L	Fig. 2.1.1 (3)
CDL40 series (64bit slot mode)	L	*	H	L	H	X	H	L	Fig. 2.1.1 (4)

(Note 1) * at normal speed PB set to "L", at double speed PB set to "H".
(Note 2)

CDL30 series	CXD1125Q/QZ, CXD1130Q/QZ, CXD1135Q/QZ, CXD1241Q/QZ, CXD1245Q, CXD1246Q/QZ, CXD1247Q/QZ/R and others.
CDL35 series	CXD1165Q, CXD1167Q/QZ/R and others.
CDL40 series	CXD2500Q/QZ and others.

2.1.2 Decoder Control (DECCTL) register

bit0 to 2: DECMDSL2, 1, 0
(Decoder Mode Select 2, 1, 0)

DECMDSL2	1	0	
"L"	"L"	"X"	Decoder disable
"L"	"H"	"X"	Monitor only mode
"H"	"L"	"L"	Write only mode
"H"	"L"	"H"	Real time correction mode
"H"	"H"	"L"	Repeat correction mode
"H"	"H"	"H"	CD-DA mode

bit3 : AUTODIST (Auto Distinction)
"H" ; Error Correction perfomed according to the Mode byte and FORM bit read from Drive.
"L" ; Error Correction is performed according to the following MODESEL and FORMSEL bits.
bit4 : FORMSEL (Form Select)
bit5 : MODESEL (Mode Select)
When AUTODIST is at "L" the sector is corrected as the following MODE or FORM.

MODESEL	FORMSEL	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit6 : ECCSTR (ECC Strategy)
"H" ; Error correction is performed with consideration to respective data error flag.
"L" ; Error correction is performed without consideration to respective data error flag. When an 8bit/Word RAM is connected, turn this bit to "L".
bit7 : ENDLADR (Enable DLADR)
"H" ; When this bit is set to "H", DLADR is enabled.
When, either write only mode, real time correction, or CD-DA mode is being executed, the decoder stops the buffer write as DADRC and DLADR turn equal.

"L" ; When this bit is set to "L", DLADR is disabled.
During the execution of write only mode or real time coreection, even if DADRC and DLADR turn equal, the decoder does not stop buffer write.
(See paragraph 4 for details)

2.1.3 DMA Control (DMACTL) register
bit0 : HSRC (Host Source)
"H" ; Data is transferred from the host to the buffer memory.
"L" ; Data is transferred from the buffer memory to the host.
bit1 : HDMAEN (HOST DMA Enable)
"H" ; DMA of the host port is enabled.
"L" ; DMA of the host port is prohibited.
bit2 : ENXTC (Enable XTC)
"H" ; DMA completion of the host port through XTC pin input is enabled.
"L" ; DMA completion of the host port through XTC pin input is disabled.
bit3 : ENHXFRC (Enable XHFRC)
"H" ; DMA Completion of the host port through HXFRC is enabled.
"L" ; DMA completion of the host port through HXFRC is disabled.
bit4 : ADMAEN (ADP DMA Enable)
"H" ; DMA of the audio processor port is enabled.
"L" ; DMA of the audio processor port is prohibited.
Also, prohibits turning HDMAEN and ADMAEN simultaneously to "H".
bit5 : CSRC (CPU Source)
"H" ; Data is transferred from the CPU to the buffer memory.
"L" ; Data is transferred from the buffer memory to the CPU.
bit6 : CDMAEN (CPU DMA Enable)
"H" ; DMA of the CPU port is enable.
"L" ; DMA of the CPU port is prohibited.
bit7 : RESERVED
Unused, Keep set to "L".

2.1.4 Configuration (CONFIG) register
bit0 : RESERVED
Unused, Keep set to "L".
bits 1 and 2: SDMACYC1, 0 (SCSI DMA CYCLE)
DMA transfer between this IC, SCSI control IC and ADPCM processor is executed in the following cycle.

SDMACYC1	0	
"L"	"L"	3 cycle.
"L"	"H"	4 cycle,
"H"	"X"	5 cycle,

bit3 : SBSCTL (SCSI Bus Control)
Setting this bit to "H" forces XHWR, XHRD, HDB0 to 7 and HDBP into high impedance condition.
bit4 : CINTPOSI (CPU Interrupt Positive)
"H" ; INT pin turns to High active.
"L" ; INT pin turns to Low active.
bit5 : 9 BITRAM
"H" ; When a 9 bit/word RAM is connected, this bit is turned to "H".
"L" ; When a 8 bit/word RAM is connected, this bit is turned to "L".
bits 6 and 7: RESERVED
Unused, Keep set to "L".

2.1.5 Interrupt Mask (INTMSK) register

Turning the respective bits of the register to "H" enables interrupt request from this IC to the CPU by means of the corresponding interrupt status (That is, When interrupt status is turned on, INT pin is activated) The value of the respective bits in this register does not affect the corresponding interrupt status.

bit0 : DECINT (Decoder Interrupt)

When the Decoder is executing one of the respective modes, write only, monitor, or real time correction, if Sync mark is detected or introduced, DECINT status is turned on. However, When Sync detection window is open, if sync interval is less than 2352 byts, Decint status is not turned on.

Also, when Decoder repeat correction mode is being executed, everytime one correction is completed DECINT status is turned on.

bit1 : HDMACMP (Host DMA Complete)

When DMA of the host port is completed through HXFRC or XTC pins, HDMACMP status is turned on.

bit2 : DRVOVRN (Drive Over Run)

When ENDLADR bit (bit7) of DECCTL register is set to "H", and the DECODER has executed write only, real time correction mode or CD-DA mode, as DADRC and DLADR become equal, DRVOVRN status is turned on.

However, in CD-DA mode, even when ENDLADR bit is turned to "L", DRVOVRN status is turned on.

bit3 : HSTCMND (Host Command)

As the host writes a command in the Command register, HSTCMND status is turned on.

bit4 : HCRISD (Host Chip Reset Issued)

By having the host write "H" in CHPRST bit (bit7) of the Control register, this IC is reset and HCRISD status is turned on.

bit5 : RSLTEMPT (Result Empty)

The host reads the Result register, As the Result register becomes empty RSLTEMTS status turns on.

bit6 : DECTOUT (Decoder Timeout)

After setting the Decoder to either, monitor only, write only or real time correction modes, if, even after sector 3 time (normal speed PB 40.6ms) passes, sync is not detected, DECTOUT status is turned on.

2.1.6 Clear Interrupt Status (INTCLR) register

When any of the respective bits of this register is set to "H", the corresponding interrupt status is cleared. After the interrupt status clearance, the bit automatically turns to "L". Accordingly there is no need for the CPU to set to "L" again.

bit0 : DECINT (Decoder Interrupt)
bit1 : HDMACMP (Host DMA Complete)
bit2 : DRVOVRN (Drive Over Run)
bit3 : HSTCMND (Host Command)
bit4 : HCRISD (Host Chip Reset Issued)
bit5 : RSLTEMPT (Result Empty)
bit6 : DECTOUT (Decoder Timeout)

2.1.7 Drive•Last•Address register Low (DLADR-L)

2.1.8 Drive•Last•Address register High (DLADR-H)

When the Decoder is executing either of write only, real time correction mode or CD-DA mode, CPU sets the last address that writes into the buffer, data from the drive. When ENDLADR bit of DECCTL register is set to "H" and the Decoder is executing the above modes, if data from the drive is written into the buffer at the address specified from DLADR, all writing into the buffer is prohibited after that.

2.1.9 Drive•Addres•Counter Low (DADRC-L)

2.1.10 Drive•Addres•Counter High (DADRC-H)

This counter keeps the address that writes data from the drive into the buffer. When drive data is written into the buffer, DADRC contents is output form BA0 to 15. For every byte written in the buffer, DADRC is incremented. Before the Decoder executes either write only, real time correction mode or CD-DA mode, CPU sets the buffer write head address to DADRC.

This counter can alse be used as the DMA address of the CPU port. During DMA execution of the CPU port, DADRC contents is output from BA0 to 15, DADRC is incremented at every byte of DMA execution.

CPU can read or set DADRC contents at any time. Do not alter DADRC contents during either write only, real time correction or CD-DA mode and the DMA execution of CPU port.

2.1.11 Host•Address•Counter Low (HADRC-L)

2.1.12 Host•Address•Counter High (HADRC-H)

This counter keeps the address that writes data from the host into the buffer or reads from the buffer. During execution of the host port DMA, HADRC contents are output from BA0 to 15. The counter is incremented at every DMA of the host port.

Before execution of the host port DMA, CPU sets the DMA head address to HADRC.

CPU can read or set HADRC contents at any time, Do no alter HADRC contents during host port DMA execution.

2.1.13 Host•Transfer•Counter Low (HXFRC-1)

2.1.14 Host•Transfer•Counter High (HXFRC-H)

This counter indicates the number of host port DMA transfers. It is decremented at every host port DMA.

When ENHXFRC bit (bit3) of DMACTL register is set to "H" and HXFRC value turns to 0, the host port DMA is disabled. At that time it is possible to send an interrupt request from this IC to the CPU.

CPU can read and set HXFRC contents at any time. Do not alter HXFRC contents during Host port DMA execution.

2.1.15 Chip Control (CHPCTL) register

bit0 : CPUBWOP (CPUBWPO)
Sets the pointer value for CPU port DMA (buffer write).

bit1 : CHPRST (Chip Reset)
Setting this bit to "H" initializes the interior of this IC. After the initialization of the interior of this IC is completed, this bit automatically turns to "L". Accordingly it is not necessary to set the CPU to "L".

bit2 : SWOPN (Sync Window Open)

"H" ; Setting this bit to "H" opens the window to allow for SYNC Mark detection.Sync protection circuit inside this IC is disabled.

"L" ; Setting this bit to "L" controls the window through the sync protection circuit inside the IC.

bit3 : PRSTART (Repeat Correction Start)
Setting the Decoder to repeat correction mode and this bit to "H" starts the sector error correction. As correction starts, this bit automatically turns to "L". Accordingly it is not necessary to set the CPU to "L".

bit4 to 7: Do not fail to set to "L". If set to "H" IC operation is not guaranteed.

2.1.16 CPU Buffer Write Data (CPUBWDT) register

With the CPU port DMA (buffer and write), data is written into this register. When CDMAEN of DMACTL register=CSRC="H", write into this register is subject to the request of CPU port DMA (buffer write). See paragraph 6 for details.

2.1.17 Host Interface Control (HIFCTL) register

When HMDS is at "L", this register controls the hard ware of the host interface.

bit0 : HINT #1 (Host Interrupt #1)
This bit value becomes the value of HINTSTS #1 (bit0) from STATUS register on the host side.

bit1 : HINT #2 (Host Interrupt #2)
This bit value becomes the value of HINTSTS #2 (bit1) from STATUS register on the host side.

bit2 : HINT #3 (Host Interrupt #3)
This bit value becomes the value of HINTSTS #3 (bit2) from STATUS register on the host side.

(Note) Once "H" is written, until bits 0 to 2 are cleared from the host or the chip is reset, keep at "H". It is not possible to access the register from the CPU and turn bits 0 to 2 from "H" to "L". Accordingly, to set any of these bits, it is not necessary to take into consideration the value of other bits.

When HINTSTS bits #1 to 3 from HIFSTS register that corresponds to the above bits are at "H", it is prohibited to write "H" in the above bits. Therefore, before the CPU writes "H" in the above bits HIFSTS register should be read, and confirmation made that corresponding HINTSTS bits #1 to 3 are at "L".

bit3 to 5: RESERVED
Unused. Keep set to "L". If set to "H" the IC operation is not guaranteed.

bit6 : CLRRSLT (Clear Result)
When this bit is set to "H", the result register is cleared. When these register's clearance is completed, this bit automatically turns to "L". Therefore, there is no need for the CPU to set back to "L".

bit7 : CLRBUSY (Clear, Busy)
When this bit is set to "H", BUSYSTS bit of HINTSTS register is cleared. When these register' s clearance is complete, this bit turns automatically turns to "L". Therefore, there is no need for the CPU to reset to L.

2.1.18 Drive Result (DRVRSLT) register

This register is utilized to transfer the command execution result to the host, when HMDS="L". This register is composed of a 10 byte FIFO. For details see 4.2.1.

2.1.19 Register Adress (REGADR) register

bit0 to 6: Do not fail to set to "L". If set to "H" the IC operation is not guaranteed.

bit7 : REGADR0 (Register Address0)
This bit is used for the register address expansion.

2.2 Read out register

2.2.1 Current Minute Address Low (CMADR-L) register

2.2.2 Current Minute Address High (CMADR-H) register

Indicates the buffer memory address where the current sector (after correction is completed) minute bytes are writen.

2.2.3 Header (HDR) register

A 4 byte register that indicates the current sector Header byte.

By reading address 0H successively 4 times the CPU can know the Header byte value of the current sector, starting from the MINUTE byte.

2.2.4 Sub Header (SHDR) register

A 4 byte register that indicates the current sector Sub Header byte.

By reading address 1H successively 4 times, the CPU can know the Sub Header byte value of the current sector, starting from the File byte.

2.2.5 Header Flag (HDRFLG) register
Indicates the Header and Sub Header error pointer value.

2.2.6 Interrupt Status (INTSTS) register
The value of the respective bits in this register indicates the condition of the corresponding interrupt status. The bit value of INTMSK register does not affect the above mentioned bits.

bit0 : DECINT (DECODER Interrupt)
bit1 : HDMACMP (Host DMA Complete)
bit2 : DRVOVRN (Drive Over Run)
bit3 : HSTCMND (Host Command)
bit4 : HCRISD (Host Chip Reset Issued)
bit5 : RSLTEMPT (Result Empty)
bit6 : DECTOUT (Decoder Timeout)

2.2.7 DECODER Status (DECSTS) register

bit0 : NOSYNC
Indicates that Sync Mark could not be detected and that SYNC was inserted.

bit1 : SHRTSCT (Short Sector)
Indicates the Sync Mark interval was within 2352 bytes. This sector does not execute ECC and EDC.

bit2 : ECCOK (ECC OK)
Indicates there are no more errors from the header of the sector where error correction was completed up to P Perity byte.
(In FORM2, this bit turns to don't care.)

bit3 : EDCOK
Indicates EDC check showed there were no errors.

bit4 : CORDONE (Correction Done)
Indicates that sector contains bytes that were error corrected.

bit5 : CORINH (Correction Inhibit)
Indicates there was an error flag at MODE (and FROM) bytes when AUTODIST bit of DECODER register was turned to "H". This sector does not execute ECC and EDC.

bit6 : ERINBLK (Erasure in Block)
Turns to "H" when C2 pointer from CIRC LSI stood in 1 byte or more of all the bytes, with the exception of current sector sync byte.

bit7 : EDCALL0 (EDC ALL ZERO)
This bit turns to "H" when there are no error flags in any of EDC parity bytes of current sector, and the value is at 00H.

2.2.8 MODEFORM (MDFM) register
This register is effective only during the execution of Real time correction mode or Repeated correction mode.

bit0 : CFORM (Correction FORM)
bit1 : CMODE (Correction MODE)
These bits indicate whether this IC identified MODE or FORM in that sector and executed error correction.

CMODE	CFORM	
"L"	"L"	MODE1
"H"	"L"	MODE2, FORM1
"H"	"H"	MODE2, FORM2

bit2 to 4: RMODE0, 1, 2 (Raw MODE)
RMODE1, 0 : Indicates the lower 2 bits value of raw MODE byte.
RMODE2 : Indicate the logical sum of the upper 6 bits and pointer in raw MODE byte.

2.2.9 DMA Status (DMASTS) register

bit0 : CBFWRDY (CPU Buffer Write Ready)
This bit turns to "H" when data written from CPU into CPUBWDT register is written in the buffer memory. As CPU writes the next data into CPUBWDT register, it turns to "L" until that data is written into the buffer memory. Also, when CSRS is set to "H" and CDMAEN to "H" (DMACTL register), this bit turns to "H".
CPU confirms this bit is at "H" and writes in the data into CPUBWDT register.

bit1 : CBFRRDY (HPU Buffer Read Ready)
When data read from buffer memory is kept ready in CPUBRDT register, this bit turns to "H". When CPU reads CPUBRDT register out it turns to "L".
CPU confirms this bit is at "H" and reads out data from CPUBRDT register.

bit2 : CBFRDPO (CPU Buffer Read Pointer)
Indicates the value of the pointer bit read from the buffer memory.

bit7 : REGADR (Register Address)
This bit indicates the value of bit7 from Register Address register.

2.2.10 DADRC-L

2.2.11 DADRC-H

2.2.12 HADRC-L

2.2.13 HADRC-H

2.2.14 HXFRC-L

2.2.15 HXFRC-H

2.2.16 CPU Buffer Read Data (CPUBRDT) register

CPU port DMA (buffer read) data is read out from this register.
When CDMAEN of DMACTL register is at "H" and CSRC at "L", the read out of this register is set for the DMA (buffer read) request of the next CPU port.

2.2.17 Host Parameter (HSTPRM) register

When HMDS is at "L", this register is used to know the command parameter from the host. This register is composed of 10 byte FIFO.

2.2.18 Host Command (HSTCMD) register

When HMDS is at "L", this register is used to know the command from the host.

2.2.19 Host Interface Status (HIFSFS) register

When HMDS is at "L", this register is used to know the host interface condition.

bit0 : HINTSTS #1 (HOST Interrupt Status #1)
This bit turns to "H" as CPU writes "H" into HINT #1 (HIFCTL register bit0). It turns to "L" when the host writes "H" into CLRINT #1 (Control register bit0). This bit is used as interrupt status monitor to the host.

bit1 : HINTSTS #2 (Host Interrupt Status #2)
This bit turns to "H" as CPU writes "H" into HINT #2 (HIFCTL register bit1). it turns to "L" when the host writes "H" into CLRINT #2 (Control register bit1). This bit is used as interrupt status monitor to the host.

bit2 : HINTSTS #3 (Host Interrupt Status #3)
This bit turns to "H" as CPU writes "H" into HINT #3 (HIFCTL register bit2). it turns to "L" when the host writes "H" into CLRINT #3 (Control register bit2). This bit is used as interrupt status monitor to the host.

bit3 : PRMRRDY (Parameter, Read Ready)
This bit at "H" indicates that HSTPRM register is not empty, so that Parameter data can be read out from the CPU. When this bit is at "L", HSTPRM register is empty and Parameter data cannot be read out from the CPU.

bit4 : PRMFULL (Parameter Full)
This bit at "H" indicates HSTPRAM register is full.

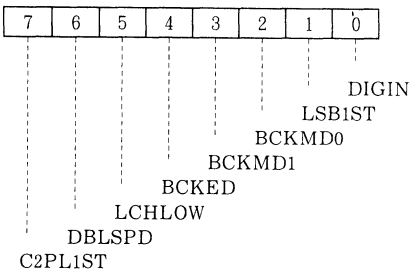
bit5 : RSLWRDY (Result Write Ready)
This bit at "H" indicates that HSTPRM register is not full, so that the CPU can write Result data. When this bit is at "L" DRVRSLT register is full and the CPU can not write Result data.

bit6 : RSLEMPT (Result Empty)
This bit at "H" indicates DRVRSLT register is empty.

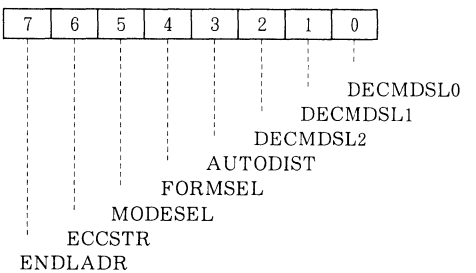
bit7 : BUSYSTS (Busy Status)
This bit has the same value as that of BUSYSTS (bit7) of the status register on the host side.
This bit turns to "H" as the host writes a command in the Command register. It turns to "L", as the CPU sets CLRBUSY bit of HIFCTL register.

* * * * * Write register * * * * *

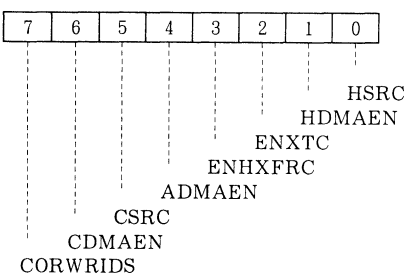
Drive Interface (DRVIF)



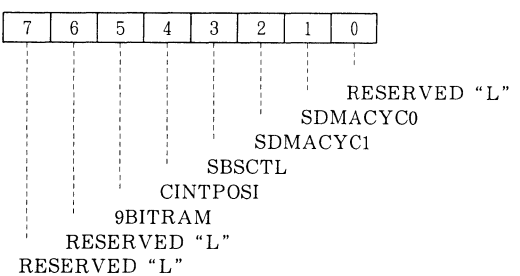
DECODER Control (DECCTL)



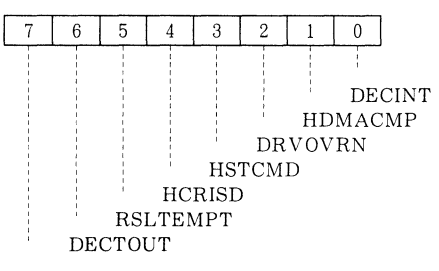
DMA Control (DMACTL)



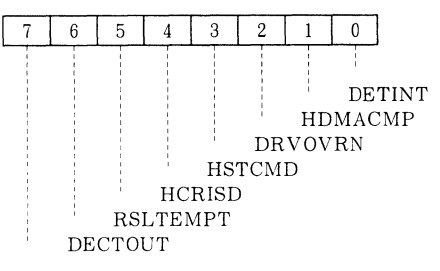
Configuration (CONFIG)



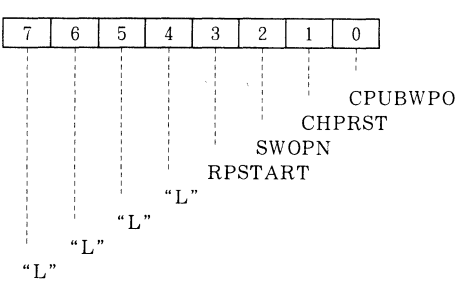
Interrupt Mask (INTMSK)



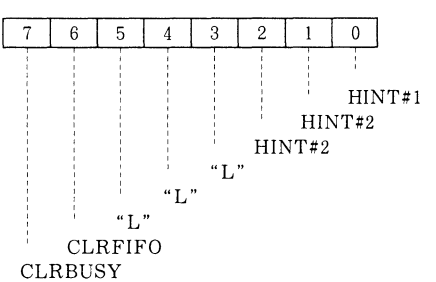
Clear Interrupt Status (INTCLR)



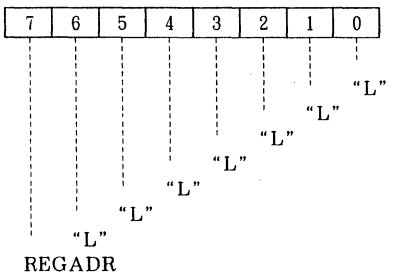
Chip Control (CHPCTL)



Host Interface Control (HIFCTL)



Register Address (REGADR)



Drive•Last•Address•Low
Drive•Last•Address•High

Drive•Address•Counter•Low
Drive•Address•Counter•High

Host•Transfer•Counter•Low
Host•Transfer•Counter•High

Host•Address•Counter•Low
Host•Address•Counter•High

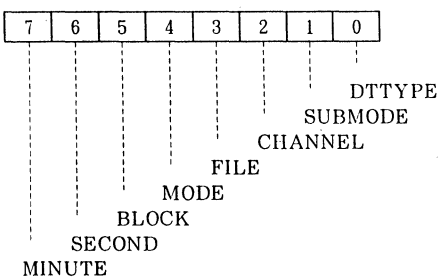
CPU Buffer Write register

Drive Status register

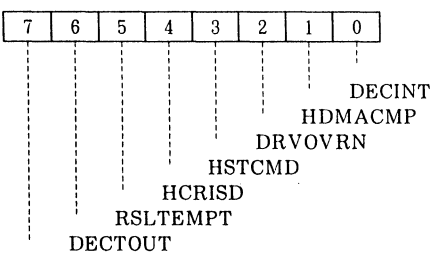
Register Address register

*** * * * * Read register * * * * ***

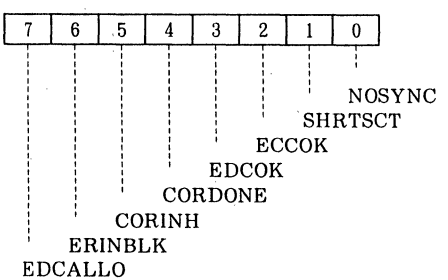
Header Flag



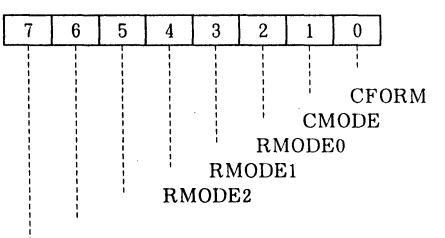
Interrupt Status



DECODER Status

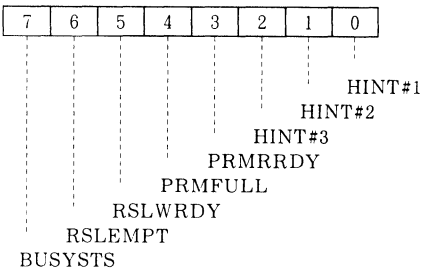


MODEFORM



DMA Status

Host Interface Status



Header register

Sub Header register

Current•Minute•Address•Low
Current•Minute•Address•High

Drive•Last•Address•Low
Drive•Last•Address•High

Drive•Address•Counter•Low
Drive•Address•Counter•High

Host•Transfer•Counter•Low
Host•Transfer•Counter•High

Host•Address•Counter•Low
Host•Address•Counter•High

CPU•Address•Couter•Low
CPU•Address•Couter•High

CPU Buffer Read register

Host Command register
Host Parameter register

CXD1186Q register

ADDRESS	Write REGISTER-ADDRESS L	Write REGISTER-ADDRESS H	Read REGISTER-ADDRESS L	Read REGISTER-ADDRESS H
0	DRVIF	CONFIG	HDR	
1	DECCTL		SHDR	
2	DMACTL		HDRFLG	
3	INTMSK		MODEFORM	
4	INTCLR		DECSTS	
5	DLADR-L		INTSTS	
6	DLADR-H		DMASTS	
7	DADRC-L			
8	DADRC-H			
9	HXFRC-L			
A	HXFRC-H			TEST2
B	HADRC-L			TEST1
C	HADRC-H			TEST0
D	CPUBWDT	HIFCTL	CPUBRDT	HSTCMD
E	CHPCTL	DRVRSLT	CMADR-L	HSTPRM
F	REGADR		CMADR-H	HIFSTS

3. DECODER Operation

Here after, the block containing functions ① and ② is called DECODER.

① Interface with CIRC LSI

The data stream from CIRC LSI is taken in, while sync detection, descramble and data write to the buffer are executed.

② Error correction

Executes error correction of the sector written in the buffer.

3.1 DECODER operation mode

The Decoder features 4 operation modes set by means of DECMDSEL0 to 2 bits of DECCTL register.

DECMDSL2	1	0	
"L"	"L"	"X"	Decoder disable
"L"	"H"	"X"	Monitor only mode
"H"	"L"	"L"	Write only mode
"H"	"L"	"H"	Real time correction mode
"H"	"H"	"L"	Repeat correction mode
"H"	"H"	"H"	CD-DA mode

(1) Decoder disable

DECODER operation is disabled.

(2) Monitor only mode

Data from the drive is not written in the buffer. Raw data from the drive is written in the Header, Sub Header and HDRFLG registers.

(3) Write only mode

Set to this mode, first Sync pattern detection is performed. As sync pattern is detected, write from that sector into the buffer starts from minute byte. The buffer memory address of this minuute byte, is the value set to DADRC though the CPU before setting the DECODER mode. Sectors after that, and the Sync pattern too, are written into the buffer.

This buffer write continues until either ① Decoder is disabled or ② when ENDLADR is at "H", DLADR value becomes equal to that of DADRC.

(4) Real time correction mode

Buffer write works the same as write only mode.

At the same time, error correction of the sectors already written in the buffer is executed in real time. (When this mode is set and while the first sector is being written in the buffer, as long as a whole sector is not yet stored in the buffer, correction is not executed.)

(5) Repeat correction mode

Data from the drive is not written in the buffer. Error Correction of sectors already written in the buffer can be executed repeatedly. This way, errors that could not be corrected during real time correction mode, can now be corrected.

(6) CD-DA mode

To write CD-DA (Digital audio) Disc data into the buffer, this mode is set. As this mode is set, write into the buffer is executed from the lower byte of LCH.

This buffer write continues until either ① Decoder is disabled, or ② When ENDLADR is at "H", DLADR value becomes equal to that of DADRC.

3.2 DADRC (Drive Address Counter)

DADRC is the counter that holds the address when data from the drive is written into the buffer. When data from the drive is written into the buffer, the contents are output from BA0 to 15 as buffer memory address. CPU can set or read DADRC contents. CPU sets the buffer write head address in DADRC before the setting of Decoder write only mode, real time correction mode and CD-DA mode.

3.3 DLADR (Drive Last Address)

DLADR is the register that indicates in bytes the value of DADRC that stops the drive data buffer write during the execution of write only mode, real time correction mode and CD-DA mode. When ENDLADR bit of DECCTL register is at "H" and the above modes are being executed, if DADRC value becomes equal to DLADR, it stops the buffer write data from the drive. Then, DRVOVRN status is on. When sync interrupt applies and DRVOVRN bit is at "H", have CPU disable the DECODER. When ENDLADR bit is at "L", even if DADRC value becomes equal to DLADR, buffer write of the data from the drive is not stopped and DRVOVRN status does not turn on.

Through the usage of DLADR, buffer overran of the drive can be prevented.

When a value is set to DLADR, make sure to set the upper byte first and the lower byte next in the order. (Even in case only the value of one of the bytes is to be changed, set both bytes in the mentioned order. If this is not performed, IC operation can not be guaranteed.) The DLADR upper byte is first set then the lower byte is set and until data from the drive is written in the buffer, the above function is disabled. DLADR setting should be made carefully.

3.4 Error correction

(1) MODE FORM discrimination

Mode and Form discrimination in the sector that performs error correction is executed in bits AUTODIST, FORMSEL and MODESEL of DECCTL register, as indicated in Fig. 3.5.

(2) ECC strategy can be chosen through ECCSTR bit of DECCTL register.

At "H", error correction is performed taking into consideration error flags from respective data.

At "L", error correction is performed without taking into consideration error flags from respective data.

For systems using 8 bit word RAM, turn ECCSTR to "L".

When double speed PB is executed (DBLSPD of DRVIF register is at "H"), transfer speed to the host slows down. Data transfer speed to the host when XTL1 frequency is set to 16.9344MHz is shown below, Moreover, this data transfer speed is the value obtained when data buffer write from the drive, error correction and data transfer to the host are executed at the same time.

	ECCSTR	Data Transfer Speed
Normal PB speed	L	2.1MB/S
	H	
Double PB speed	L	
	H	0.7MB/S

From the above table, it appears that during double speed PB, data transfer speed to the host decreases. During double speed PB, Read data speed from the Drive is at 176.4KB/S. Data transfer speed to the host at 0.7MB/S is quite faster than this Read speed. Actually, transfer speed to the host does not decrease and as Read data speed from the drive doubles, transfer speed to the host also approximately doubles.

3.5 CPU control of the IC during Real time correction

CPU control of the IC during the IC execution of Real time correction mode is shown in Fig. 3.6.

3.6 CPU control of the IC during Repeat correction

CPU control of the IC during the IC execution of Repeat correction mode is shown in Fig. 3.7.

4. Host interface

4.1 Host I/F mode

This IC can be connected to the following, as the host interface.

① SCSI controller IC (CXD1180AQ, CXD1185DQ and others)

② Intel 80 type host bus

This mode is set by means of HMDS pin, as shown below.

When Type 80 is connected, HMDS input is at "L". Otherwise, HMDS pin is set to open.

When SCSI control IC is connected, HMDS input is at "H".

4.2 Connected to Intel 80 type host bus

When this IC is connected to Intel 80 type host bus either "L" is input to pin HMDS or it is left open. This connection is shown an Fig. 4.2.

4.2.1 Command/Status transfer between the Host and the CPU.

(1) Register

The host can access each of the 4 write and read registers. Using pins XHCS, HA0, HA1, XHRD and XHWR, it reads and writes their registers. DMA transfer is also possible with RDDATA and WRDATA registers despite XHCS, HA0 and HA1 values. Their registers are selected by means of XHAC, XHRD, XHWR and DMA transfers perfomed with the host. Parameter register and Result register are 10 bytes FIFO registers. "L" input to XHAC and XHCS is prohibited at the same time.

* Write register
  - Command register (address 0)
    The host writes commands in this register. As the host writes in this register, interrupt request is applied from this IC to the CPU. Bit assignment and function attribution is performed by means of a control program.
  - Parameter register (address 1)
    To execute commands, the host writes into this register command parameters. This is a 10 bytes FIFO register.
  - Write Data (WRDATA) register (address 2)
    This register serves to write data from the host into the buffer memory. Data can be written into either I/O mode or DMA mode. This register is composed of a 2×9 bits FIFO.
  - Control register (address 3)
    This register is for the direct control of the hard ware in this IC by the host.
    bit0 to 2: INTCLR #1 to 3 (Clear Interrupt #1 to 3)
    Setting these bits to "H" will clear the corresponding interrupt status, After the clearance of interrupt status in these bits, they automatically go back to "L".
    bit3 to 5: ENINT #1 to 3 (Enable Interrupt #1 to 3)
    Setting these bits to "H" will enable the corresponding interrupt status.
    The host can read the respective bits value from the status register.
    When the corresponding interrupt status is at "H", it is prohibited to write "H" to these bits, accordingly, before the host sets these bits to "H", the status register should be read out and interrupt status confirmed.
    bit6 : CLRPRM (Clear FIFO)
    Setting this bit to "H" clears the Parameter register, After these registers are cleared, this bit automatically goes back to "L".
    bit7 : CHPRST (Chip Reset)
    Setting this bit to "H" initializes the inside of this IC. As the inside of this IC initialization is completed, this bit automatically return to "L". Setting this bit to "H" enables interrupt request to the CPU.

* Read out register
  - Status register (Address 0)
    The host uses this register to read this IC status.
    bit0 to 2: INTSTS #1 to 3 (Interrupt Status #1 to 3)
    The value of the respective bits is the same as that of the bits corresponding to HIFCTL register of the sub CPU. When interrupt corresponding to the respective bits is enabled, they turn to "H" and interrupt request to the host is output.
    bit3 to 5: ENINTST #1 to 3
    (Enable Interrupt Status #1 to 3)
    The value of the respective bits is the same as that of the bits corresponding to Control register.
    bit6 : DREQSTS (Data Request Status)
    Indicates this IC is in buffer memory data transfer request condition versus the host. This bit has the same value as that of pin HDRQ. In I/O mode, when buffer memory data tranfer is executed, access WRDATA register or RDDATA register after the host confirms this bit is at "H".
    bit7 : BUSYSTS (Busy Status)
    This bit turns to "H" as the Host writes a command into the command register. It turns to "L" as the CPU sets CLRBUSY bit of HIFCTL register.
  - Result register (address 1)
    The Host reads the results after the command execution from this register.
    This is a 10 bytes FIFO.

• Read Data (RDDATA) register (addres 2)

This register is for the Host to read data from the buffer memory. Data can be read in I/O mode or DMA mode. It is composed of a 2×9 bits FIFO.

• FIFO Status register (address 3)

This register is for the HOST to read the status of Parameter or Result register.

bit0 : PRMWRDY (Parameter Write Ready)
When this bit is at "H" it indicates that parameter register is not full, and that the Host can write parameter data.

bit1 : PRMEEMPT (Parameter Empty)
This bit at "H" indicates Parameter register is empty.

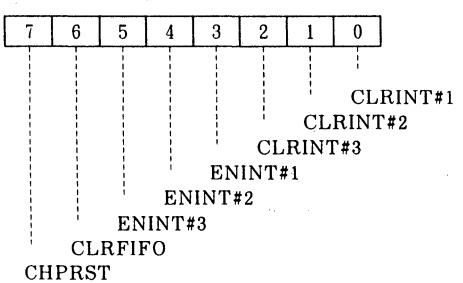
bit2 : RSLRRDY (Result Read Ready)
This bit at "H" indicates that Result register is not empty, and that the Host can read Result data.

bit3 : RSLFULL (Result Full)
This bit at "H" indicates Result register is full.

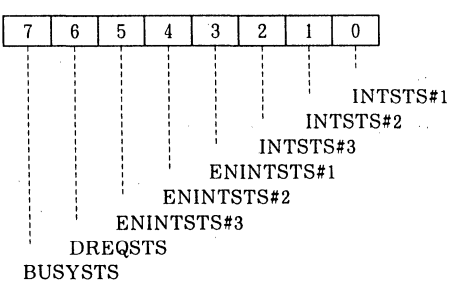
bit4 to 7: RESERVED
Unused.

Address	Write	Read
0	Command	Status
1	Parameter	Result
2	Write Data	Read Data
3	Control	FIFO Status

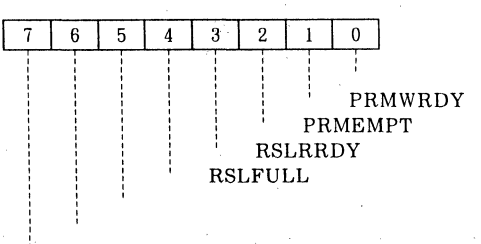
Control



Status



FIFO Status



(2) Host and sub CPU controlling order

An example of the Host and CPU controlling order is shown in Fig. 4.2.1.

In this case the host gets to know interrupt status by polling Status register, Interrupt request can also be enabled.

4.2.2 Data transfer between the Host and the buffer memory.

Data transfer between the Host and the buffer memory is executed through this IC. This IC incorporates a 2×9 bits FIFO (WRDATA, RDDATA register) to speed up data transfer.

(1) Data transfer in DMA mode

Data transfer between the Host and FIFO inside this IC, is performed through handshake utilizing HDRQ/XSAC and XHAC/SDRQ,

HDRQ/XSAC becomes the HDRQ data transfer request signal from this IC to the host while XHAC/SDRQ becomes the corresponding aknowledge signal XHAC.

① Data transfer from the Host to the buffer memory (HSRC at "H")

When HDMAEN is at "H" while FIFO in not FULL and XHAC is at "H", this IC activates HDRQ. As aknowledge signal XHAC comes back from the host, HDRQ is inactivated. With the rising edge of XHAC, data is written into FIFO. Data written into FIFO is written in the buffer memory address in the order prescribed by HADRC.

② Data traunfer from the buffer memory to the host (HSRC at "L")

When HDMAEN is at "H", buffer read data from the address prescribed by HADRC is written into the FIFO. As data is written into FIFO, if XHAC is at "H", this IC activates HDRQ. As the aknowledge XHAC comes back from the bost, HDRQ is inactivated. During the period when XHAC is at "L", This IC outputs the FIFO data to HDB0 to 7.

(2) Data transfer in I/O mode

The host can transfer data to and from the buffer memory, by writing or reading registers WRDATA and RDDATA. In this case the control of CXD1186Q by the CPU is the same as during DMA transfer mode.

Fig. 4.2.2 indicates the Host control flow when data transfer is performed in I/O mode between the Host and the buffer memory.

(3) Data transfer completion

The 3 following methods are for data transfer completion.

- HXFRC is used.
- XTC pin is used.
- HDMAEN bit is set to "L".

① When HXFRC is used

When HXFRC is used for data transfer completion, perform the following before the CPU starts data transfer.

- Set the number of data transfer bytes at HXFRC.
- Set ENHXFRC=HDMAEN="H" and the data transfer direction (HSRC bit). This starts data transfer.

HXFRC is decremented everytime data is written into FIFO.

When HXFRC turns to 0, writing of data into FIFO after that is not performed. Then, when all the FIFO data is transferred to the buffer memory or the Host, HDMACMP status (DMASTS register) sets on. When HDMACMP bit of INTMSK register is set to "H", this IC outputs interrupt request (INT output) to the CPU.

② When XTC pin is used

When XTC pin is used for data transfer completion, perform the following before the CPU starts data transfer.

- Set ENXTC=HDMAEN="H" and the data transfer direction (HSRC bit). This status data transfer.

During the Host final DMA byte transfer, turn XTC pin and XHAC, XHAC, XHWR, XHRD to "L". This way, data transfer to the host is no more perfomed. (HDRQ is not output to the host.) When HSRC is at "L" and XTC turns to "L", after XHAC becomes inactive, this IC turns to HDMACMP status. In this case, 1 byte of unnecessary data from the buffer memory may already be written in the FIFO.

There, care should be exercised as the last address of HADRC transfer +2 is indicated. When HSRC is at "H", the IC turns to HDMACMP status, when the writing into the buffer memory of data written into the FIFO as XTC at "L", is completed.

In either case, as HDMACMP status sets on, and HDMACMP bit of INTMSK register is set to "H", this IC outputs interrupt request (INT output) to the CPU.

Both ENXTC and ENHXFRC bits of DMACTL register, can simultaneously be set to "H".

(Note) In either ① or ② case, after HDMACMP sets on, before starting up data transfer again, turn bit 1 of INTCLR register to "H" and clear HDMACMP register.

③ When HDMAEN bit is set to "L"

When HDMAEN bit is set to "L" during data transfer with the Host, data transfer is stopped. There data transfer between this IC and the Host or the buffer memory may be stopped half-way. The value of HADRC and HXFRC after that is not guarauteed. Also, in this case, HDMACMP status does not set on.

(4) CPU control of the IC

CPU control of the IC when data transfer is perfomed between the Host and the buffer memory is illustrated as follows. (In this exanple execute data transfer completion using HXFRC)

① The number of transfer bytes is set to HXFRC.
② HADRC is set at the DMA head address.
③ HDMEAN and ENHXFRG bits of DMACTL register are set to "H".
④ As the transfer of the specified number of bytes is completed, HDMACMP bit of DMASTS register turns to "H". (There, this IC can output an interrupt request to the CPU)
⑤ Also, HXFRC is at 0000H, while HADRC value stands as the value next to that of the buffer memory address transferred last.

4.3 When connected to SCSI control IC

When this IC is connected to SCSI control IC, HMDS pin is set to "H".

4.3.1 Connection method to SCSI control IC

- An example for the connection of this IC to an SCSI control IC where CPU bus and DMA bus are not separated (IE CXD1180AQ) is shown in Fig. 4.3.1.
  To switch CPU and DMA buses, an external circuit is required.
- An example for the connection of this IC to an SCSI control IC where CPU and DMA buses are separated (IE CXD1185AQ) is shown in Fig. 4.3.1-2.

4.3.2 Data transfer between SCSI control IC and the buffer memory

Data transfer between SCSI control IC and buffer memory is performed through this IC.

(1) Data transfer handshake

XHAC/SDRQ become the data transfer request signal SDRQ from SCSI control IC to this IC. HDRQ/XSAC become the corresponding aknowledge signal XSAC.

① Data transfer from SCSI control IC to this IC (HSRC at "H")

When HDMAEN is at "H", SDRQ input while FIFO is not Full will make this IC activate XSAC. Data is written into FIFO with the rising edge of XHWR.

② Data transfer from this IC to SCSI control IC (HSRC at "L")

When HDMAEN is at "H", SDRQ input while FIFO is not EMPTY will make this IC activate XSAC. It also outputs data from FIFO to HDB0 to 7 during the period XHAC is at "L".

(2) Completion of data transfer

The 2 following methods are for the completion of data transfer.

- HXFRC is used.
- HDMAEN is set to "L".

For either method refer to paragraph 4.2.2.

(3) Data transfer cycle

The data transfer cycle between, this IC and SCSI control IC can be controlled through SDMACYC 0 and 1 bits from CONFIG register. CPU sets these bits in coordination with the speed of SCSI control IC (See A. C characteristics)

SDMACYC1	0	
"L"	"L"	3 cycles.
"L"	"H"	4 cycles.
"H"	"X"	5 cycles.

(4) CPU control of the IC

For CPU control of the IC when data transfer is executed between SCSI control IC and the buffer memory, see paragraph 4.2.2.

5. Data transfer between audio processor and buffer memory

Data transfer between ADP and the buffer memory is performed through this IC.

(1) Data transfer handshake

ADRQ pin is the data transfer request signal from ADP to this IC. XAAC pin becomes the corresponding aknowledge signal. When ADMAEN is at "H" and ADRQ is input while FIFO is not Empty, this IC activates XAAC and outputs FIFO data to HDB0 to 7 during the period where XAAC is at "L".

(Note 1) HADRC and HXFRC are used for the transfer of data between both this IC and the host and this IC and ADP. Accordingly, HDMAEN and ADDMAEN cannot be set to "H" simultaneously. In case both are set to "H" simultaneously, HDMAEN will turn to "H" and admaen to "L", inside the IC.

(Note 2) Even When HMDS is at "L" (connected to Intel 80 type host bus), turning ADMAEN to "H" will make XHWR and XHRD pins change from input to output. Therefore access from the host to this IC register is not possible. Watch out for signals collision.

(2) Completion of data transfer

There are 2 ways to complete data transfer.

- Using HXFRC.
- Turning ADMAEN bit to "L".

For details on the 2 methods refer to Paragraph 4.2.2.

(3) Data transfer cycle

The data transfer cycle between this IC and ADP can be controlled using bits SDMACYC 0 and 1 from CONFIG register. CPU sets these bits to match ADP transfer speed.

(See figure)

SDMACYC1	0	
"L"	"L"	3 cycles.
"L"	"H"	4 cycles.
"H"	"X"	5 cycles.

(4) CPU control of the IC

For CPU control of the IC when data is transferred between ADP and the buffer memory, refer to Paragraph 4.2.2.

6. CPU port DMA

• CPU control of the IC

An example on CPU control of the IC when CPU port performs DMA is indicated in Fig. 5.1.2. When CPU port performs DMA, the address uses DADRC Accordingly, when the Decoder is performing any of the following modes write only, real time correction, CD-DA, CPU cannot access the buffer memory.

When CSRC is at "L", turning CDMAEN to "H" (DMACTL register) will cause data from the buffer memory to be read and written into CPUBRDT register.

When CDMAEN is turned to "H", it is prohibited to change CSRC value. To change CSRC value turn CDMAEN to "L".

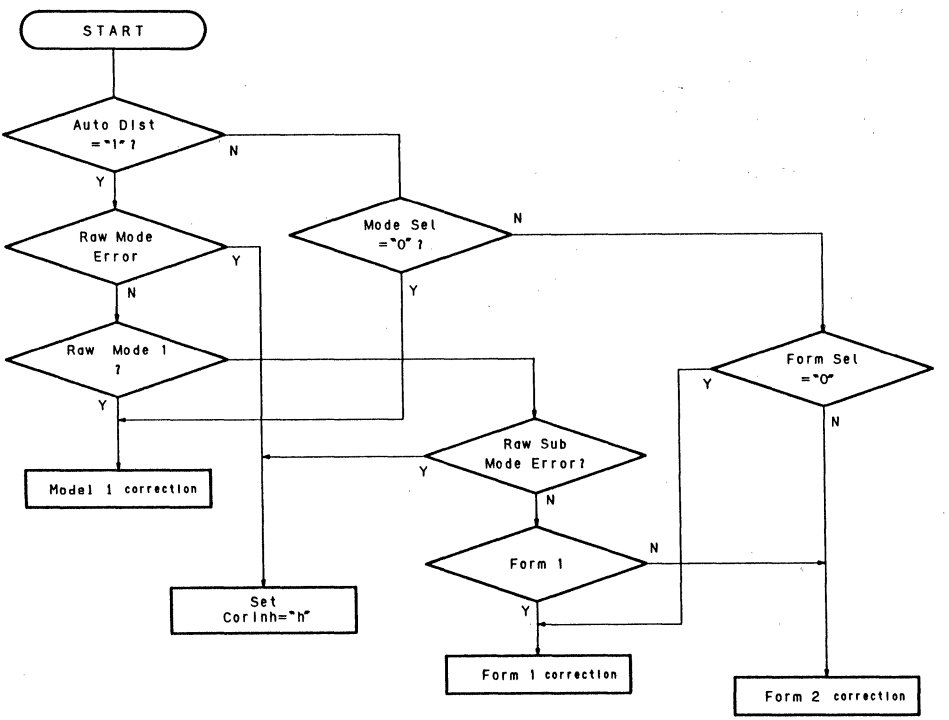


Fig. 3.5 MODE FORM Discrimination method

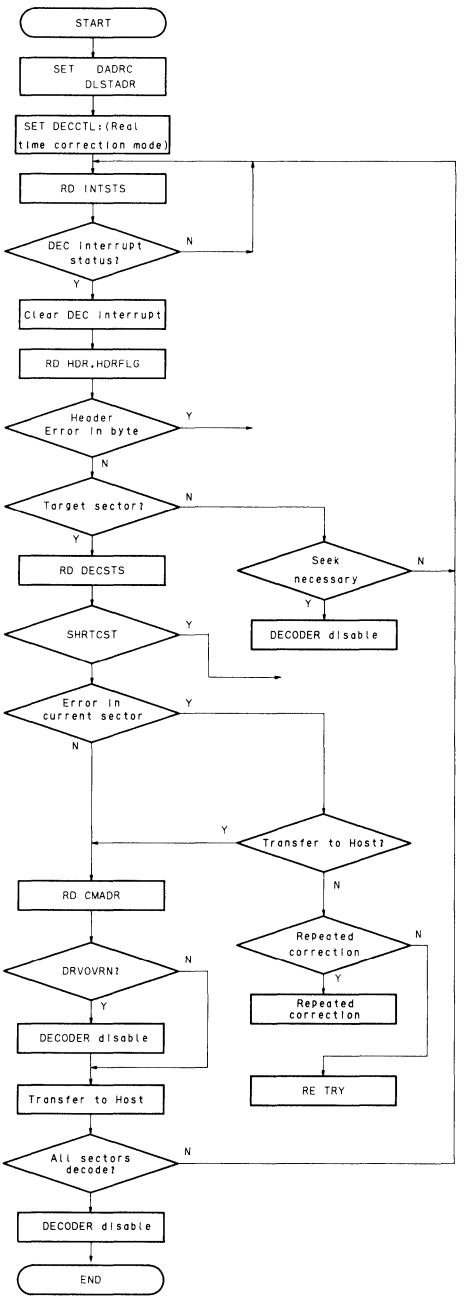


Fig. 3.6 CPU control of the IC during real time correction

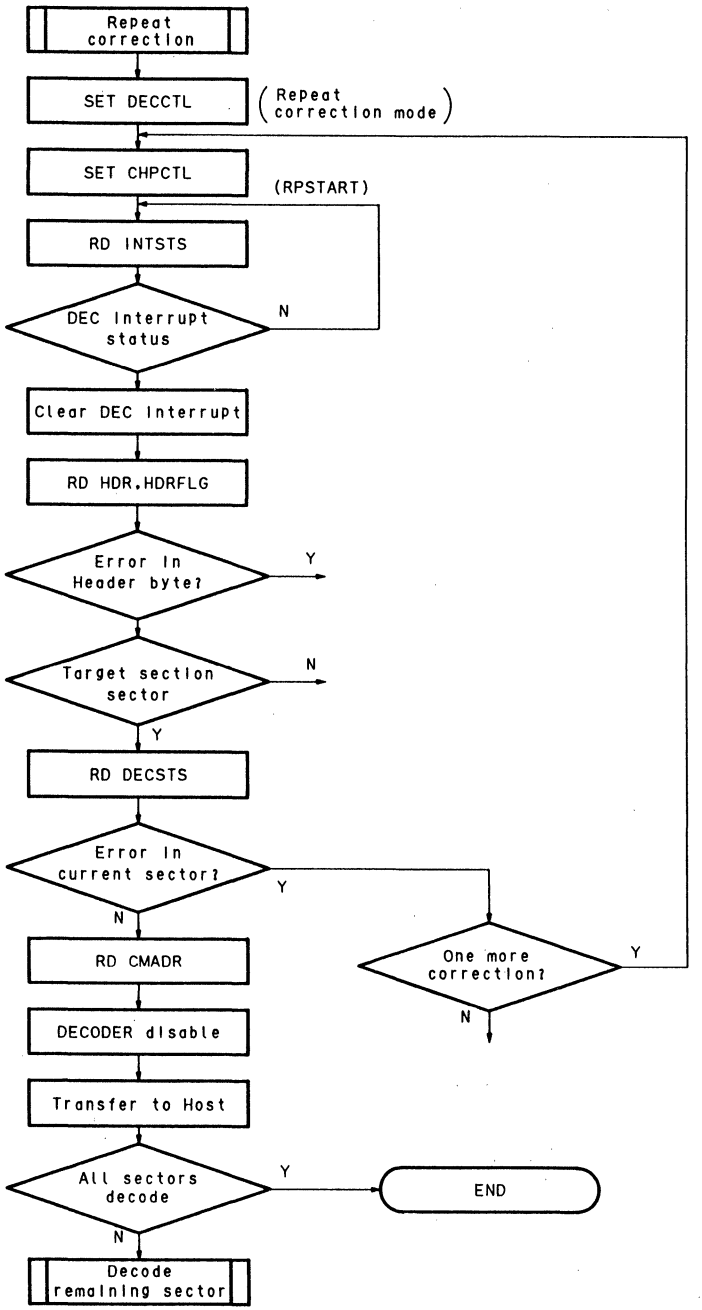


Fig. 3.7 CPU control of the IC during repeated correction

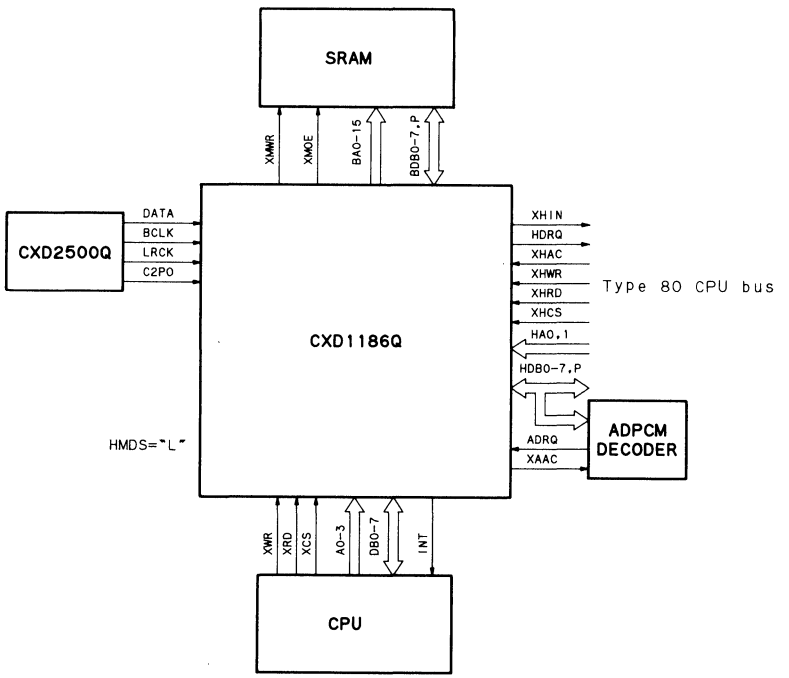


Fig. 4.2 CXD1186Q connection (Type80 CPU bus)

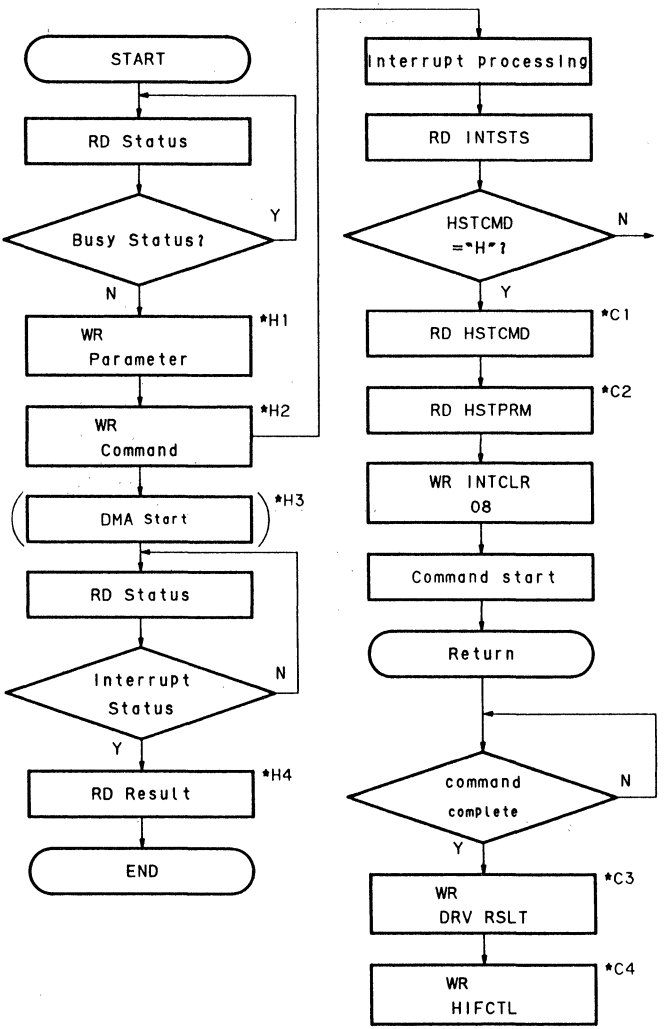


Fig. 4.2.1 Host and Sub CPU control

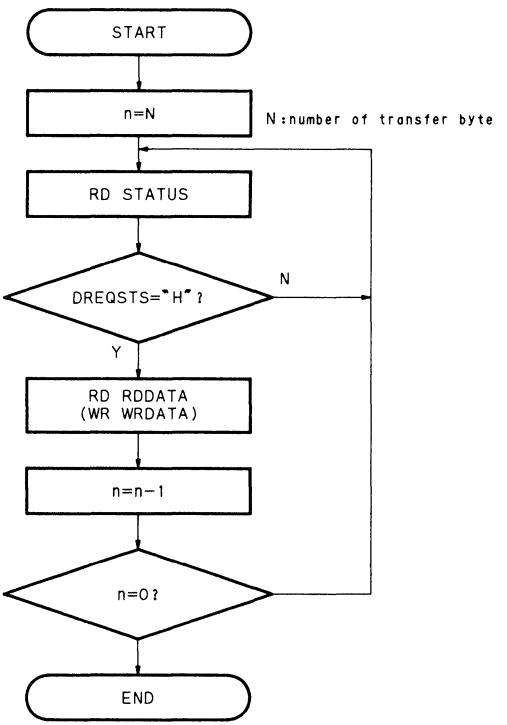


Fig. 4.2.2 I/O mode data transfer

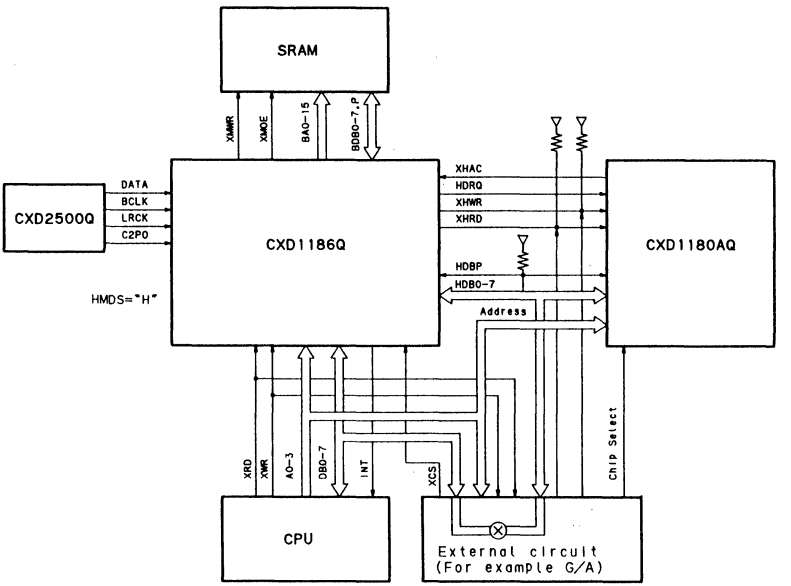


Fig. 4.3.1-1 CXD1186Q connection (connecting method 1 with SCSI control IC)

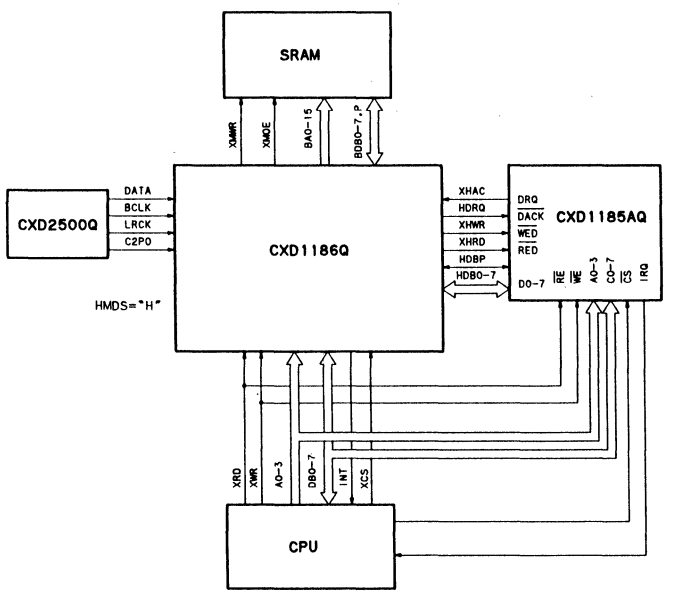


Fig. 4.3.1-2 CXD1186Q connection (connecting method 2 with SCSI control IC)

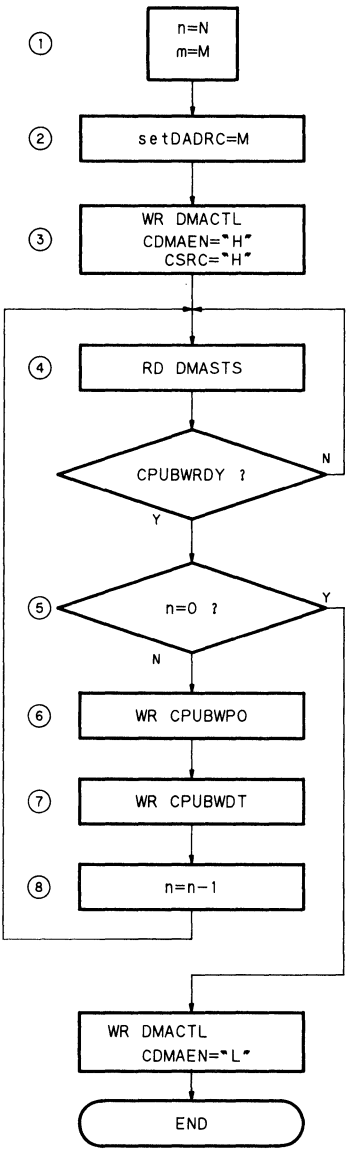


Fig. 5.1 CPU buffer write control

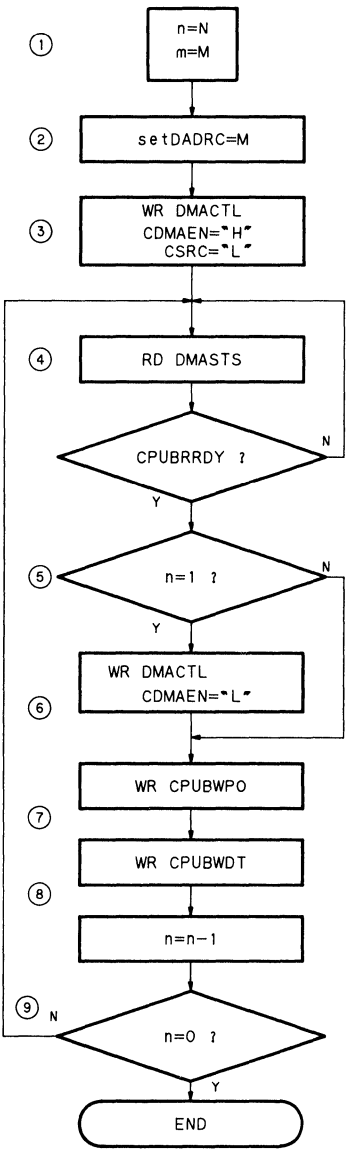
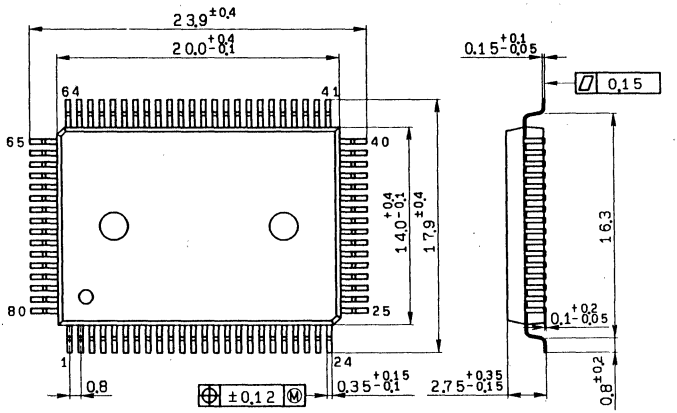


Fig. 5.2 CPU buffer read control

Package Outline unit: mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

CXD1196R

CD-ROM Decoder

80pin VQFP (Plastic)

Description

The CXD1196R is a CD-ROM decoder LSI with a built-in ADPCM decoder.

Features

- CD-ROM, CD-I, CD-ROM XA format compatible
- Real time error correction
- Double speed reproduction compatible (when V_{DD}=5.0±10%)
- Can be connected to a standard SRAM up to 32Kbytes (256 Kbits)
- All audio output sampling frequency of 132.3kHz (Bulit-in oversampling filter)
- Built-in de-emphasis digital filter
- Capable of V_{DD} 3.5V operation

Application

CD-ROM drive

Structure

Silicon gate CMOS IC

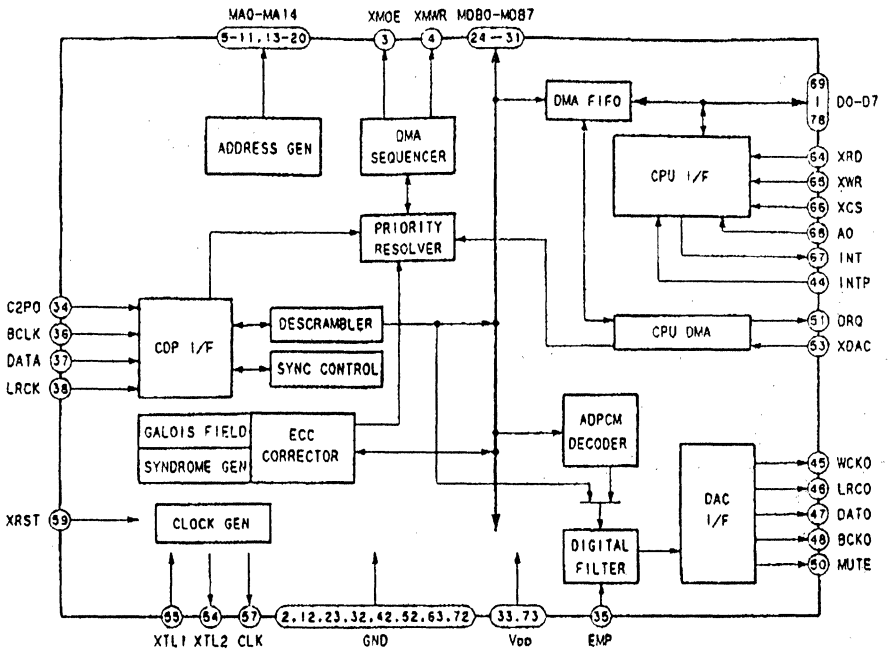
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	V_{SS} -0.5 to +7.0	V
• Input voltage	V_I	V_{SS} -0.5 to V_{DD} +0.5	V
• Output voltage	V_I	V_{SS} -0.5 to V_{DD} +0.5	V
• Operating temperature	T_{opr}	-20 to +75	°C
• Storage temperature	T_{stg}	-55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.5 to +5.5 (+5.0 Typ.)	V
• Operating temperature	T_{opr}	-20 to +75	°C

Block Diagram



Pin Description

No.	Symbol	I/O	Description
1	TD7	I/O	Test pin
2	GND	---	Ground pin
3	XMOE	O	Buffer memory output enable negative logic signal
4	XMWR	O	Buffer memory write enable negative logic signal
5	MA0	O	Buffer memory address (LSB)
6	MA1	O	Buffer memory address
7	MA2	O	Buffer memory address
8	MA3	O	Buffer memory address
9	MA4	O	Buffer memory address
10	MA5	O	Buffer memory address
11	MA6	O	Buffer memory address
12	GND	---	Ground pin
13	MA7	O	Buffer memory address
14	MA8	O	Buffer memory address
15	MA9	O	Buffer memory address
16	MA10	O	Buffer memory address
17	MA11	O	Buffer memory address
18	MA12	O	Buffer memory address
19	MA13	O	Buffer memory address
20	MA14	O	Buffer memory address (MSB)

SONY®

CXD2500AQ/AQZ

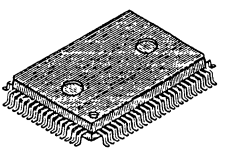
CD Digital Signal Processor

Description

The CXD2500AQ/AQZ is a digital signal processing LSI designed for use in compact disc players. It has the following functions:

- A wide frame jitter margin (±28 frames) realized by a built-in 32K RAM.
- Generation by the use of a digital PLL of bit clock pulses for strobing the EFM signal with a capture range of ±150kHz or more.
- EFM data demodulation
- Enhanced protection of EFM Frame Sync signals
- Powerful error correction based on a refined super strategy
  Error correction C1 : Double correction C2: Quadruple correction
- Double-speed play back and vari-pitch play back
- Reduced noise generation at track jumping
- Auto zero-cross muting
- Subcode demodulation and subcode Q data error detection
- Digital spindle servo system (incorporating an oversampling filter)
- 16-bit traverse counter
- Built-in asymmetry correction circuit
- CPU interface using a serial bus

80pin QFP (Plastic)



- Servo auto sequencer
- Output for digital audio interface
- Digital level meter and peak meter
- Bilinguality

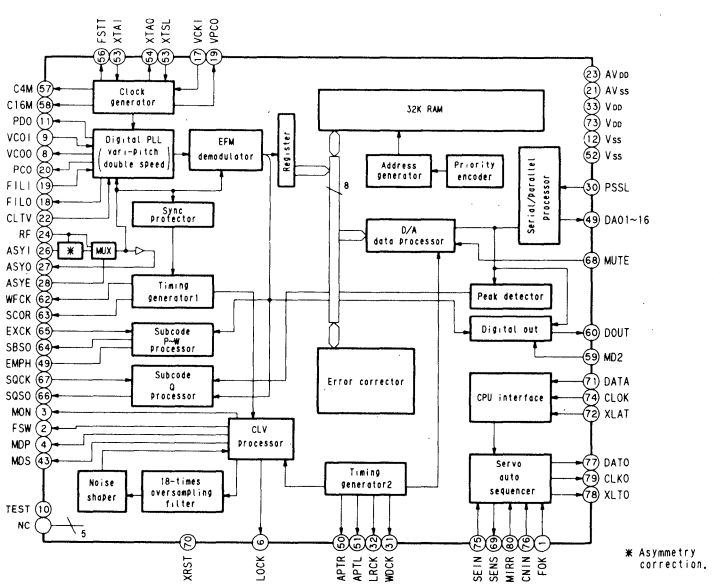
Features

- All digital signals for regeneration are processed using one chip.
- The built-in RAM enables high-integration mounting.

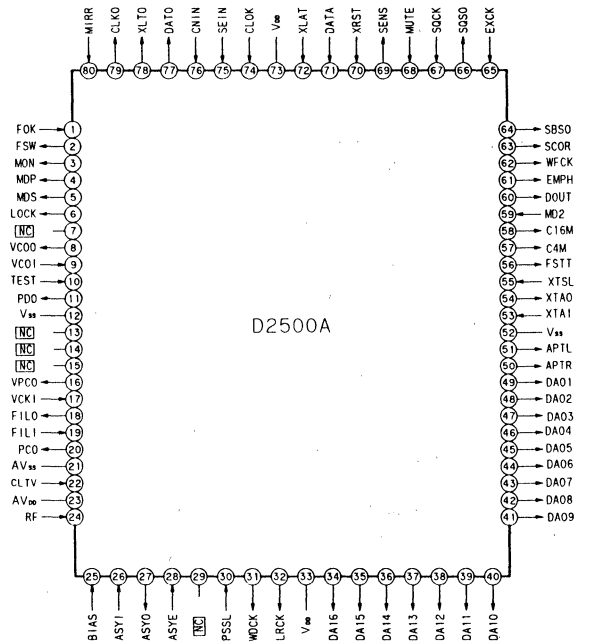
Structure

Silicon-gate CMOS IC

Block Diagram



Pin Configuration



Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_I	−0.3 to +7.0	V
• Output voltage	V_O	−0.3 to +7.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75*1 to 5.25*3 (5.0V typ.)	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Input voltage	V_{IN}	V_{SS}−0.3V to V_{DD}+0.3	V
• Supply voltage differences	$V_{SS}-AV_{SS}$	−0.1 to +0.1	V
	$V_{DD}-AV_{DD}$	−0.1 to +0.1	V

* 1 The minimum V_{DD} value of 4.75V is for the double-speed play back mode with vari-pitch control reset. It is 3.6V in the low power consumption, special regeneration mode. * 2 In normal-speed play back mode the minimum V_{DD} value is 4.5V

* 2 Low power comsumption, special play back mode
This is a normal-speed play back mode entered when the LSI is set for double-speed internal operation whereas the crystal oscillation frequency is halved.

* 3 The maximum V_{DD} value of 5.25V is for the double-speed play back mode with vari-pitch control reset. For normal-speed play back and low power consumption special play back mode, the maximum V_{DD} value is 5.5V.

I/O Capacity

• Input pins	CI	12pF max.
• Output pins	CO	12pF max. at high impedance

Note: Test Conditions
$V_{DD}=V_I=0V$
$f_M=1MHz$

Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input pin. Used for SENS output and servo auto sequencer.
2	FSW	O	Z.0	Output used to switch the spindle motor output filter.
3	MON	O	1.0	Output for spindle motor ON/OFF control
4	MDP	O	1,Z,0	Output for spindle motor servo control
5	MDS	O	1,Z,0	Output for spindle motor servo control
6	LOCK	O	1,0	The output of this pin is "H" when the GFS signal sampled at 460Hz is "H". It turns "L" when the GFS signal turns out "L" 8 or more times in succession.
7	NC	———		
8	VCOO	O	1,0	Output of oscillation circuit for analog EFM PLL
9	VCOI	I		Input to oscillation circuit for analog EFM PLL. f_{LOCK}=8.6436MHz
10	TEST	I		Test pin. Normally at 0V (GND).
11	PDO	O	1,Z,0	Output of charge pump for analog EFM PLL
12	V_{SS}			GND
13	NC	———		
14	NC	———		
15	NC	———		
16	VPCO	O	1,Z,0	Output of charge pump for vari-pitch PLL
17	VCKI	I		Clock input from external VCO for vari-pitch control. fc_{center}=16.9344MHz
18	FILO	O	Analog	Output of filter for master PLL (Slave=Digital PLL)
19	FILI	I		Input to filter for master PLL
20	PCO	O	1,Z,0	Output of charge pump for master PLL
21	AV_{SS}			Analog GND
22	CLTV	I		VCO control voltage input for master PLL
23	AV_{DD}			Analog power supply (+5V)
24	RF	I		EFM signal input
25	BIAS	I		Asymmetry circuit constant current input
26	ASYI	I		Asymmetry comparator circuit voltage input
27	ASYO	O	1,0	EFM full-swing output
28	ASYE	I		At "L" asymmetry circuit OFF. At "H" asymmetry circuit ON
29	NC	———		
30	PSSL	I		Input used to switch the audio data output mode. "L" for serial output, "H" for parallel output.
31	WDCK	O	1,0	D/A interface for 48-bit slot. Word clock f=2Fs
32	LRCK	O	1,0	D/A interface for 48-bit slot. LR clock f=Fs
33	V_{DD}			Power supply (+5V)
34	DA16	O	1,0	Outputs DA16(MSB) when PSSL=1 or serial data from 48-bit slot (2's complements, MSB first) when PSSL=0.
35	DA15	O	1,0	Outputs DA15 when PSSL=1 or bit clock from 48-bit slot when PSSL=0.

Pin No.	Symbol	I/O		Description
36	DA14	O	1,0	Outputs DA14 when PSSL=1 or serial data from 64-bit slot (2's complements, LSB first) when PSSL=0.
37	DA13	O	1,0	Outputs DA13 when PSSL=1 or bit clock from 64-bit slot when PSSL=0.
38	DA12	O	1,0	Outputs DA12 when PSSL=1 or LR clock from 64-bit slot when PSSL=0.
39	DA11	O	1,0	Outputs DA11 when PSSL=1 or GTOP when PSSL=0.
40	DA10	O	1,0	Outputs DA10 when PSSL=1 or XUGF when PSSL=0.
41	DA09	O	1,0	Outputs DA9 when PSSL=1 or XPLCK when PSSL=0.
42	DA08	O	1,0	Outputs DA8 when PSSL=1 or GFS when PSSL=0.
43	DA07	O	1,0	Outputs DA7 when PSSL=1 or RFCK when PSSL=0.
44	DA06	O	1,0	Outputs DA6 when PSSL=1 or C2PO when PSSL=0.
45	DA05	O	1,0	Outputs DA5 when PSSL=1 or XRAOF when PSSL=0.
46	DA04	O	1,0	Outputs DA4 when PSSL=1 or MNT3 when PSSL=0.
47	DA03	O	1,0	Outputs DA3 when PSSL=1 or MNT2 when PSSL=0.
48	DA02	O	1,0	Outputs DA2 when PSSL=1 or MNT1 when PSSL=0.
49	DA01	O	1,0	Outputs DA1 when PSSL=1 or MNT0 when PSSL=0.
50	APTR	O	1,0	Control output for aperture correction. "H" for R-ch.
51	APTL	O	1,0	Control output for aperture correction. "H" for L-ch.
52	V_{SS}			GND
53	XTAI	I		Input to 16.9344MHz Xtal oscillation circuit or 33.8688MHz input
54	XTAO	O	1,0	Output of 16.9344MHz Xtal oscillation circuit
55	XTSL	I		Xtal selection input pin. "L" for 16.9344MHz Xtal, "H" for 33.8688MHz Xtal.
56	FSTT	O	1,0	2/3 divided output of Pins 53 or 54. Unaffected by vari-pitch control.
57	C4M	O	1,0	4.2336MHz output. Subject to vari-pitch control.
58	C16M	O	1,0	16.9344MHz output. Subject to vari-pitch control.
59	MD2	I		Digital-Out ON/OFF control. "H" for ON, "L" for OFF.
60	DOUT	O	1,0	Digital-Out output pin
61	EMPH	O	1,0	Stays "H" for regeneration disc provided with emphasis or "L" for that without emphasis.
62	WFCK	O	1,0	WFCK(Write Frame Clock) output
63	SCOR	O	1,0	Turns "H" when subcode Sync S0 or S1 is detected.
64	SBSO	O	1,0	Serial output of Sub P to W
65	EXCK	I		Clock input for reading SBSO
66	SQSO	O	1,0	Outputs 80-bit Sub Q and 16-bit PCM peak-level data.
67	SQCK	I		Clock input for reading SQSO
68	MUTE	I		"H" for muting, "L" for release.
69	SENS	—	1,Z,0	SENS output to CPU
70	XRST	I		System reset. "L" for resetting.
71	DATA	I		Inputs serial data from CPU.
72	XLAT	I		Latches serial data input from CPU at falling edge.

Pin No.	Symbol	I/O		Description
73	V_{DD}			Power supply (+5V)
74	CLOK	I		Inputs serial data transfer clock from CPU.
75	SEIN	I		Inputs SENSE from SSP.
76	CNIN	I		Inputs track jump count signal.
77	DATO	O	1,0	Outputs serial data to SSP.
78	XLTO	O	1,0	Latches serial data output to SSP at falling edge.
79	CLKO	O	1,0	Outputs serial data transfer clock to SSP.
80	MIRR	I		Inputs mirror signal to be used by auto sequencer when jumping 128 or more tracks.

Notes:
- The data at the 64-bit slot is output in 2's complements on an LSB-first basis. The data at the 48-bit slot is output in 2's complements on an MSB-first basis.
- GTOP monitors the state of Frame Sync protection. ("H": Sync protection window released)
- XUFG is a negative Frame Sync pulse obtained from the EFM signal before Frame Sync protection is effected.
- XPLCK is an inversion of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK coincides with a change point of the EFM signal.
- The GFS signal turns "H" upon coincidence between Frame Sync and the timing of interpolation protection.
- RFCK is a signal generated at 136-μs periods using a crystal oscillator.
- C2PO is a signal to indicate a data error.
- XRAOF is a signal issued when a jitter margin of $\pm$28F is exceeded by the 32K RAM.

Electrical Characteristics

DC characteristics (V_{DD}=AV_{DD}=5.0V±5%, V_{SS}=A V_{SS}=0V, T_{opr}=−20 to +75°C)

Item			Condition	Min.	Typ.	Max.	Unit	Related pins
Input voltage (1)	Input voltage "H" level	V_{IH}(1)		0.7V_{DD}			V	* 1
	Input voltage "L" level	V_{IL}(1)				0.3V_{DD}	V	
Input voltage (2)	Input voltage "H" level	V_{IN}(2)		0.8V_{DD}			V	* 2
	Input voltage "L" level	V_{IN}(2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN}(3)	Analog input	V_{DD}		V_{SS}	V	* 3
Output voltage (1)	Output voltage "H" level	V_{OH}(1)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 4
	Output voltage "L" level	V_{OL}(1)	I_{OL}=1mA	0		0.4	V	
Output voltage (2)	Output voltage "H" level	V_{OH}(2)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 5
	Output voltage "L" level	V_{OL}(2)	I_{OL}=2mA	0		0.4	V	
Output voltage (3)	Output voltage "L" level	V_{OL}(3)	I_{OL}=2mA	0		0.4	V	* 6
Output voltage (4)	Output voltage "H" level	V_{OH}(4)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 7
	Output voltage "L" level	V_{OL}(4)	I_{OL}=2mA	0		0.4	V	
Input leak current		I_{LI}	VI=0 to 5.25V			±5	μA	* 1, * 2, * 3
Tristate pin output leak current		I_{LO}	V_O=0 to 5.25V			±5	μA	* 8

Related pins

* 1 XTSL, DATA, XLAT, MD2, PSSL
* 2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, MIRR, VCKI, ASYE
* 3 CLTV, FILI
* 4 MDP, PDO, PCO, VPCO
* 5 ASYO, DOUT, FSTT, C4M, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO,CLKO, XLTO, SENS, MDS, DA01 to DA16, APTR, APTL, LRCK, WFCK
* 6 FSW
* 7 FILO
* 8 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

2. AC Characteristics

① XTAI and VCOI pins

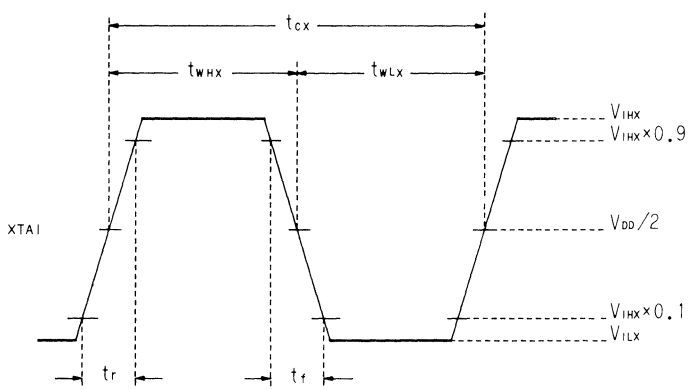
(1)During self-oscillation (T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7MHz		18	MHz

(2)With pulses input to XTAL and VCOI pins

(T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
"H" level pulse width	t_{WHX}	13		500	ns
"L" level pulse width	t_{WLX}	13		500	ns
Pulse period	t_{CX}	26		1,000	ns
Input "H" level	V_{IHX}	V_{DD}−1.0			V
Input "L" level	V_{ILX}			0.8	V
Rising time Falling time	t_R, t_F			10	ns



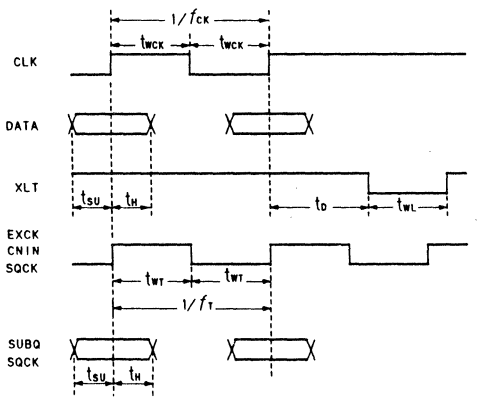
(3)With sine waves input to XTAI and VCOI pins via capacitor

(T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

② CLOK, DATA, XLAT, CNIN, SQCK, and EXCK pins
(V_{DD}=AV_{DD}=5.0V±5%, V_{SS}=AV_{SS}=0V, T_{opr}=−20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK, CNIN, SQCK frequency	f_T			1	MHz
EXCK, CNIN, SQCK pulse width	t_{WT}	300			ns

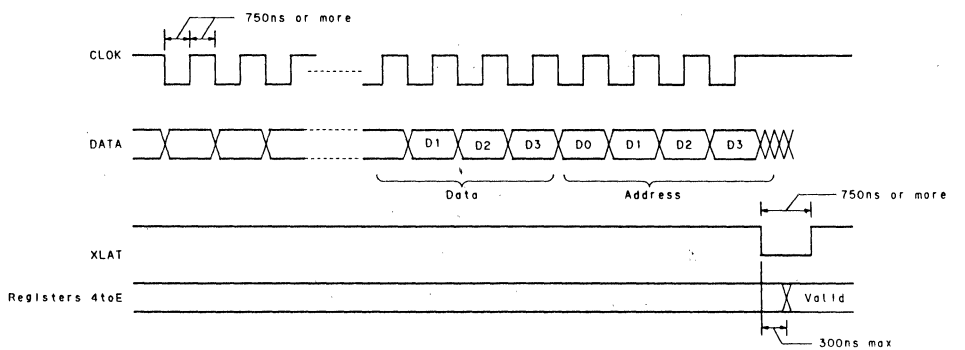


Description of Functions

§ 1 CPU Interface and Commands

○ CPU interface

This interface is used to set various modes using DATA, CLK, and XLAT.
The interface timing chart is shown below.



○ The command addresses of the CXD2500 and the data that can be set there are shown in Table 1-1.

○ When XRST is set to 0, the CXD2500 is reset, causing its internal registers to be initialized to the values listed in Table 1-2.

CXD2500A Commands

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36ms	0.18ms	0.09ms	0.045ms												
6	KICK(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump (N) setting	0	1	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CDROM	0	D OUT Mute-F	WSEL	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	D CLV ON-OFF	DSPB ON-OFF	A SEQ ON-OFF	D PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	Vari UP	Vari Down	Mute	ATT	PCT1	PCT2	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
C	Servo factor setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	DCLV PWMMD	TB	TP	CLVS Gain	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-1

CXD2500A Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK(D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump (N) setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	1	0	0	1	0	0	0	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Servo factor setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-2

§ 1-2 Meanings of Data Set at Command Addresses

$4X Command

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2NTRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF=0 FORWARD
RXF=1 REVERSE

- If a Focus-ON command ($47) being executed is canceled, $02 is issued and the auto sequence operation is discontinued.
- If a Track Jump or Track Move command ($48 to $4F) being executed is canceled, the auto sequence operation is discontinued.

$5X Command

Used to set timers for the auto sequencer.
Timers set: A, E, C, and B

Command	D3	D2	D1	D0
Blind(A,E), Over flow(C)	0.18ms	0.09ms	0.045ms	0.022ms
Brake(B)	0.36ms	0.18ms	0.09ms	0.045ms

Example: D2=D0=1, D3=D1=0 (Initial Reset)
A=E=C=0.112ms
B=0.225ms

$6X Command

Used to set a timer for the auto sequencer.
Timer set: D

Command	D3	D2	D1	D0
KICK(D)	11.6ms	5.8ms	2.9ms	1.45ms

Example: D3=0 D2=D1=D0=1 (Initial Reset)
D=10.15ms

$7X Command

Used to set the number (N) of auto sequencer track jumps/moves.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequencer track jump number setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set the value of "N" for execution of a 2N track jump or N track move.

- The maximum number of tracks that can be counted is 65,535. However, in the case of 2N track jumps, it is subject to the mechanical restrictions due to the optical system.
- When the number of tracks to be jumped is smaller than 16, the signals input from the CNIN pin are counted. When it is 16 or larger, the signals input from the MIRR pin are counted. This count signal selection contributes toward improving the accuracy of high-speed track jumping.

$8X Command

Command	D3	D2	D1	D0
MODE specification	CDROM	0	D. OUT Mute-F	WSEL

Command bit	C2PO timing	Processing
CDROM=1	1-3	CDROM mode is entered. In this mode, average value interpolation and preceding value holding are not performed.
CDROM=0	1-3	Audio mode is entered. In this mode, average value interpolation and preceding value holding are performed.

Command bit	Processing
D.out Mute F=1	When Digital Out is ON (pin MD2=1), DA output is muted.
D.out Mute F=0	DA output muting is unaffected by the setting of Digital Out.

D/A Out D.out Mute with F=1

	MD2=1 (D. out-ON)	MD2=0 (D. out-OFF)
Mute-ON	$-\infty$dB	$-\infty$dB
Mute-OFF	$-\infty$dB	0dB

Command bit	Sync protection window width	Application
WSEL=1	±26 channel clock pulses *	Antirollingness is enhanced.
WSEL=0	±6 channel clock pulses	Sync window protection is enhanced.

* In normal-speed play back, the channel clock frequency is 4.3218MHz.

$9X Command

Command	Data 1				Data 2		
	D3	D2	D1	D0	D3	D2	D1
Func specification	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL Sub	FLFC

Command bit	CLV mode	Contents	
DCLV ON-OFF=0	In CLVS mode	FSW=L, MON=H, MDS=Z, MDP=servo control signal with carrier frequency of 230Hz at T_B =0 or 460Hz at T_B =1	
	In CLVP mode	FSW=Z, MON=H, MDS= speed control signal with carrier frequency of 7.35kHz, MDP=phase control signal with carrier frequency of 1.84kHz	
DCLV ON-OFF=1 (FSW and MON are unnecessary)	In CLVS or CLVP mode	DCLV When PWM, MD=1	MDS=PWM polarity signal, Carrier frequency=132kHz MDS=PWM absolute value output (binary), Carrier frequency=132kHz
		DCLV When PWM, MD=0	MDS=Z MDP=ternay PWM output Carrier frequecy=132kHz

In the Digital CLV servo mode with DCLV ON-OFF set to 1, the sampling frequency of the internal digital filter is switched at the same time as switching between CLVP and CLVS.
Therefore, for CLVS, the cut-off frequency fC is 70Hz with T_B set to 0 or 140Hz with T_B set to 1.

Command bit	Processing
DSPB=0	Normal-speed play back. ECC quadruple correction is made. Vari-pitch control is enabled.
DSPB=1	Double-speed play back. ECC double correction is made. Vari-pitch control is disabled.

However, during PLL lock in FLFC can be set to 0.

SENS Output

Microcomputer serial register values (Latching unnecessary)	ASEQ=0	ASEQ=1
$0X	Z	SEIN(FZC)
$1X	Z	SEIN(A.S)
$2X	Z	SEIN(T.Z.C)
$3X	Z	SEIN(SSTOP)
$4X	Z	XBUSY
$5X	Z	FOK
$6X	Z	SEIN(Z)
$AX	GFS	GFS
$BX	COMP	COMP
$CX	COUT	COUT
$EX	$\overline{OV64}$	$\overline{OV64}$
$7X, 8X, 9X, DX, FX	Z	0

Description of SENS signals

SENS output	Meaning
Z	SENS pin is at high-Z state.
SEIN	Output of the SEIN signal input from the SSP to the CXD2500
XBUSY	Turns "H" when auto sequencer operation is terminated.
FOK	Output of the signal (normally FOK input from RF) input to the FOK pin. Turns "H" when Focus OK is received.
GFS	Turns "H" when regenerated Frame Sync is obtained at the correct time.
COMP	Used in counting the number of tracks set in register B. This output turns "H" when the count is latched in register B then the count is latched in register B once more. It is reset to "L" level when the count of CNIN inputs reaches the value set in the first register B.
COUT	Used in counting the number of tracks set in register B. This output turns "H" when the count is latched in register B then the count is latched in register C. It is toggled every time the count of CNIN inputs reaches the value set in register B.
$\overline{OV64}$	Turns "L" when the channel clock pulse count has exceeded 64 after passage of the EFM signal through the sync detection filter.

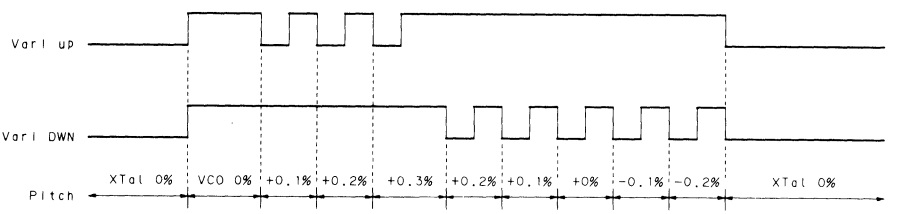
Command bit	Meaning
DPLL=0	RFPLL enters analog mode. PDO, VCOI, and VCOO are used.
DPLL=1	RFPLL enters digital mode. PDO becomes Z.

Command bit	BiliGL MAIN=0	BiliGL MAIN=1
BiliGL SUB=0	STEREO	MAIN
BiliGL SUB=1	SUB	Mute

Definition of Bilingual MAIN, SUB, and STEREO
MAIN: The input L-ch signal is output to both L-ch and R-ch.
SUB: The input R-ch signal is output to both L-ch and R-ch.
STEREO: The input L-ch signal is output to both L-ch and R-ch.

$AX Command

Command	Data 1				Data 2	
	D3	D2	D1	D0	D3	D2
Audio CTRL	Vari UP	Vari DWN	Mute	ATT	PCT1	PCT2



Command bit	Meaning
Mute=0	Muting is off unless condition to make muting occurs.
Mute=1	Muting is on. Peak register reset.

Command bit	Meaning
ATT=0	Attenuation is off.
ATT=1	−12dB

Condition for Muting CXD2500A

① Mute=1 in register A
② Pin Mute=1
③ D.OUT Mute F=1 in register 8 with D.Out ON (pin MD2=1)
④ Elapse of over 35ms after the turning low of GFS
⑤ BiliGL MAIN=Sub=1 in register 9
⑥ PCT1=1 and CPT2=2 in register A
In the case of ①~④, zero-cross muting not exceeding 1 ms is performed.

Command bit		Meaning	PCM Gain	ECC correction capacity
PCT1	PCT2			
0	0	Normal mode	×0dB	C1 : Double, C2 : Quadruple
0	1	Level meter mode	×0dB	C1 : Double, C2 : Quadruple
1	0	Peak meter mode	Mute	C1 : Double, C2 : Double
1	1	Normal mode	×0dB	C1 : Double, C2 : Double

Level Meter Mode (See timing chart 1-4.)

- This mode makes the digital level meter function available.
- Inputting 96 clock pulses to SQCK causes 96bits of data to be output to SQSO. Of the output data, the first 80bits comprise Sub-Q data communicating the data format to the Sub Code interface. The next 15 bits constitute PCM data (absolute value) ordered LSB-first. The last bit identifies the channel involved. That is, if the last bit is "H", the PCM data has been generated in L-ch. If it is "L", the data has been generated in R-ch.
- The PCM data is reset once it is read. At the same time, the L/R flag is reversed. While this state is kept until the next read operation is started, maximum value detection is continued; the detected maximum value is subsequently output.

Peak Meter Mode (See timing chart 1-5.)

- In this mode, the maximum value of PCM data is detected whether the channel involved is L-ch or R-ch. To read the detected maximum value, it is necessary to input 96 clock pulses to SQCK.
- When 96 clock pulses have been input to SQCK, 96bits of data is output to SQSO. At the same time, the data is re-set in an internal register of the LSI.
  That is, the PCM peak detection register is not reset when it is read.
- To reset the PCM peak register, set both PCT1 and PCT2 to 0. Or, Set $AX mute.
- In this mode, the absolute time of Subcode Q is controlled automatically.
  Namely, every time a peak value is detected, the absolute time when the CRC was passed is stored. The program time operation is performed in the normal way.
- The last bit (L/R flag) of the 96-bit data stays 0.
- In this mode, the preceding value holding and average value interpolation data are fixed to level ($-\infty$).

$CX Command

Command	D3	D2	D1	D0	Explanation
Servo factor setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Only DCLV=1 is effective.
CLV CTRL ($DX)				Gain CLVS	DCLV=1 and DCLV=0 are both effective.

This command is used to externally set the spindle servo gain when DCLV=1.

- Gain setting for CLVS mode: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	−12dB
0	0	1	−6dB
0	1	0	−6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note: When DCLV=0, the CLVS gain is determined as follows:
If Gain CLVS=0, then GCLVS=−12dB.
If Gain CLVS=1, then GCLVS=0dB

- Gain setting for CLVP mode: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	−6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	−6dB
0	1	0dB
1	0	+6dB

$DX Command

Command	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	CLVS Gain

└── See "$CX Command."

Command bit	Explanation (See timing chart 1-6.)
DCLV PWM MD=1	Specification of PWM mode for digital CLV. Both MDS and MDP are used.
DCLV PWM MD=0	Specification of PWM mode for digital CLV. Ternary MDP values are output.

Command bit	Explanation
TB=0	In CLVS or CLVH mode, bottom value is held at periods of RFCK/32.
TB=1	In CLVS or CLVH mode, bottom value is held at periods of RFCK/16.
TP=0	In CLVS mode, peak value is held at periods of RFCK/4.
TP=1	In CLVS mode, peak value is held at periods of RFCK/2.

In CLVH mode, peak holding is made at 34kHz.

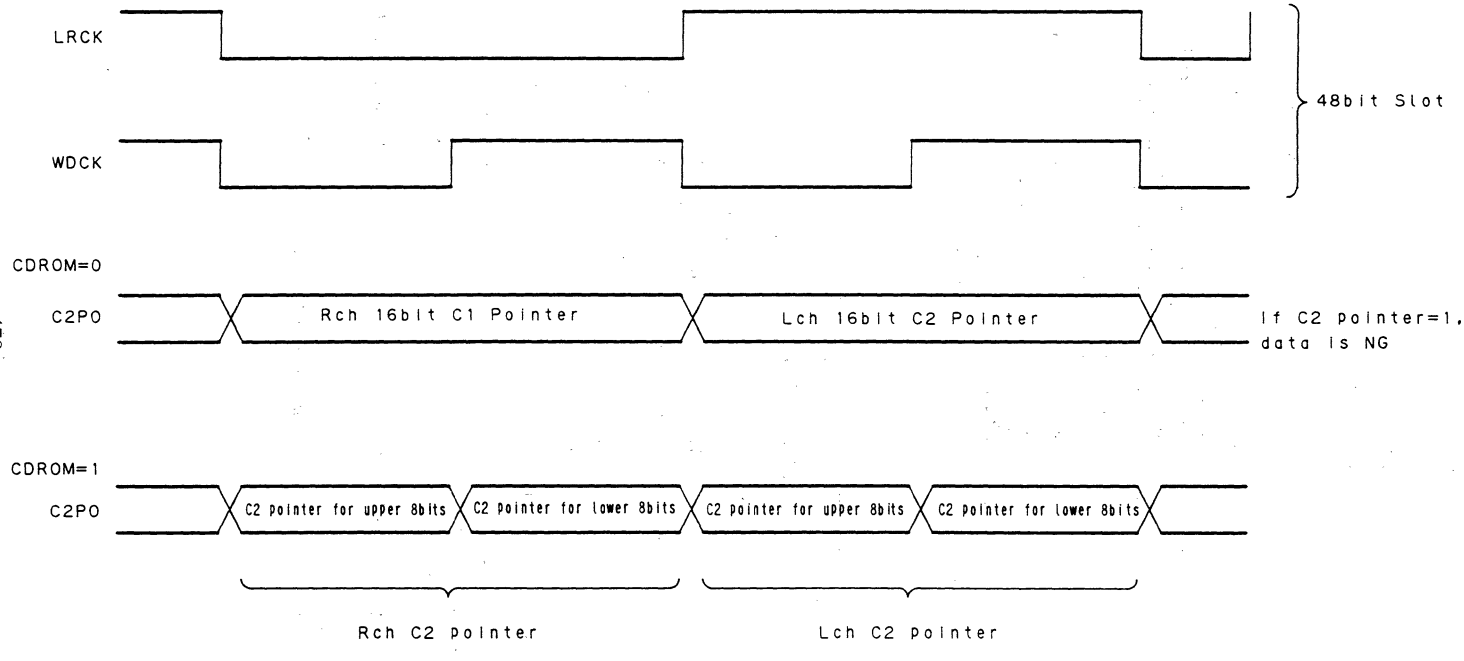
$EX Command

Command	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0

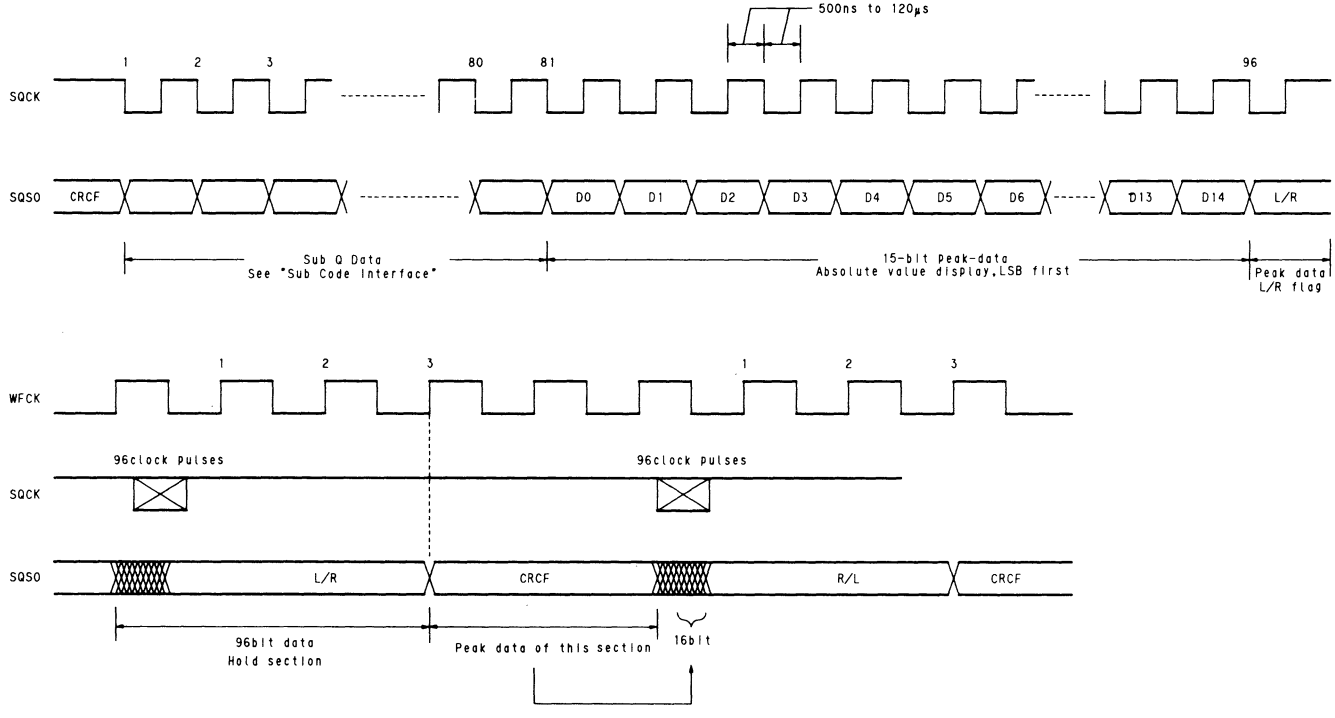
CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See Timing Chart 1-7.
1	0	0	0	KICK	See Timing Chart 1-8.
1	0	1	0	BRAKE	See Timing Chart 1-9.
1	1	1	0	CLVS	
1	1	0	0	CLVH	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP : Spindle motor stop mode
KICK : Spindle motor forward run mode
BRAKE : Spindle motor reverse run mode
CLVS : Rough servo mode for use for drawing disc run into RF-PLL capture range when the RF-PLL circuit lock has been disengaged
CLVP : PLL servo mode
CLVA : CLVS and CLVP are automatically switched modes during normal player status.

Timing Chart 1-3

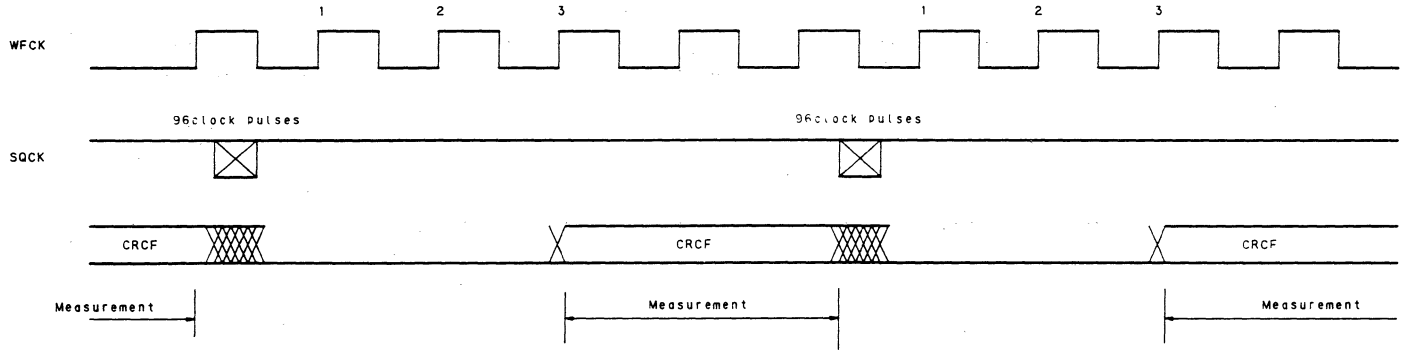


Timing Chart 1-4



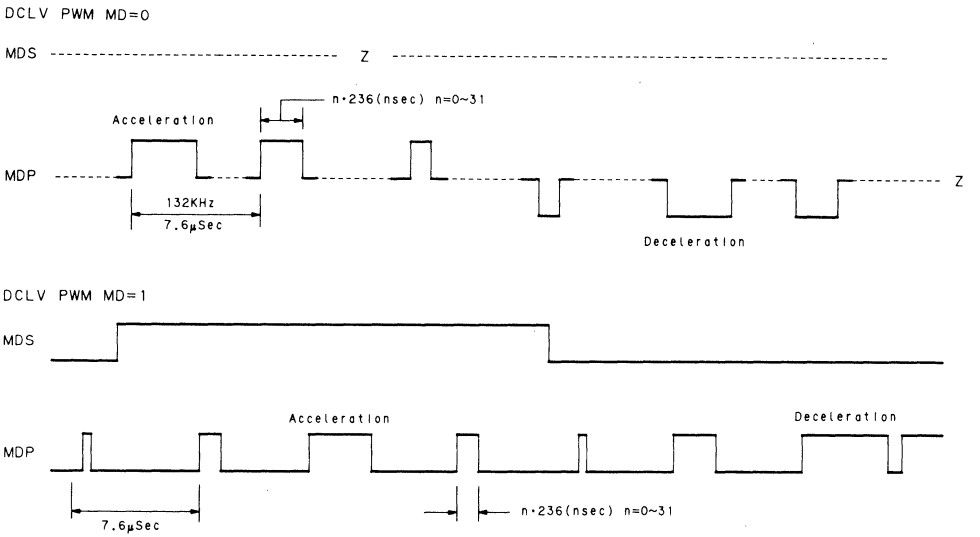
Level Meter Timing

Timing Chart 1-5



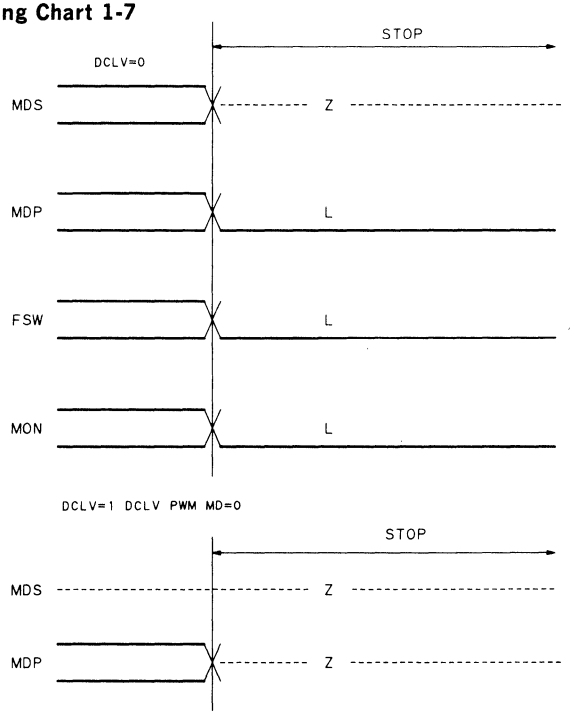
Peak Meter Timing

Timing Chart 1-6

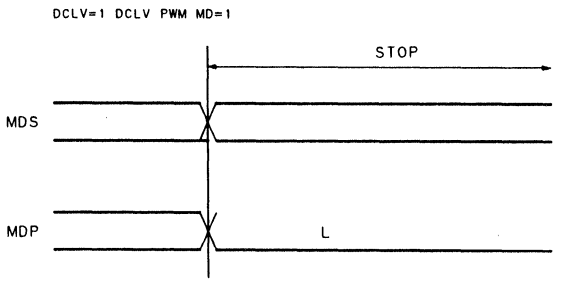


Output Waveforms with DCLV=1

Timing Chart 1-7

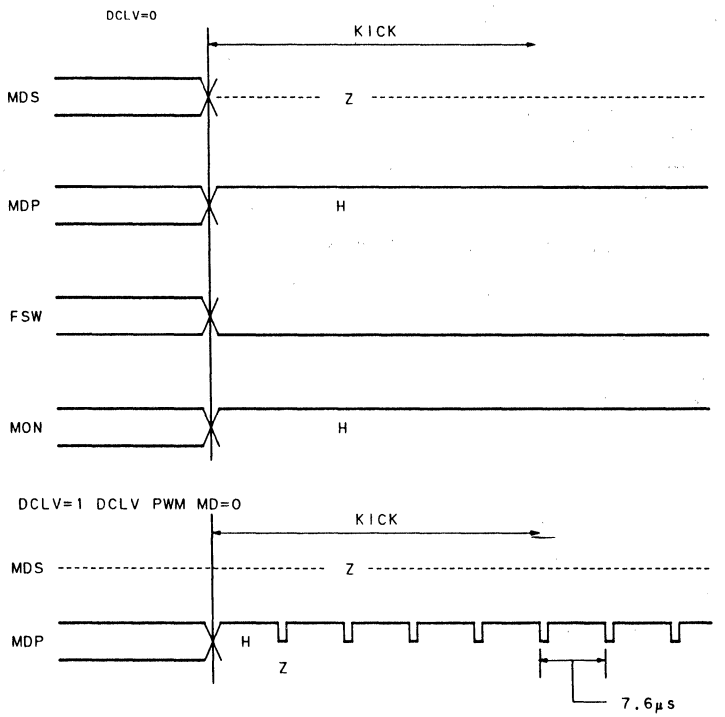


FSW and MON are the same as for DCLV=0

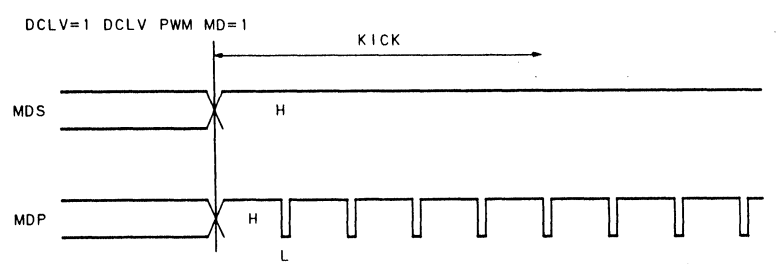


FSW and MON are the same as for DCLV=0

Timing Chart 1-8

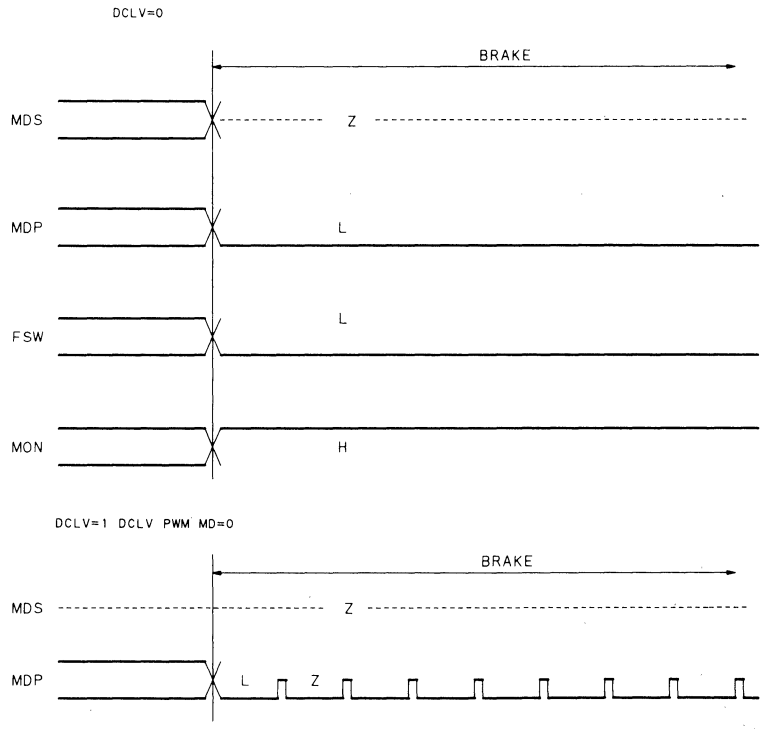


FSW and MON are the same as for DCLV=0

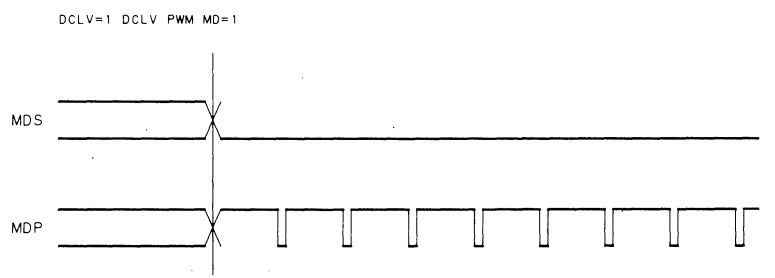


FSW and MON are the same as for DCLV=0

Timing Chart 1-9



FSW and MON are the same as for DCLV=0



FSW and MON are the same as for DCLV=0

§ 2 Subcode Interface

In this section, the subcode interface will be explained.
The contents of the subcode interface can be externally read in two ways. The subcodes P through W totaling 8bits can be read from SBSO by inputting EXCK to the CXD2500.
Sub Q can be read after conducting a CRC check on the 80bits of information in the subcode frame.
First, check SCOR and CRCF, then input 80 clock pulses to SQCK and read the data.

§ 2-1 P-W Subcode Read

These subcodes can be read by entering EXCK immediately after the fall of WFCK. (See Figure 2-1).

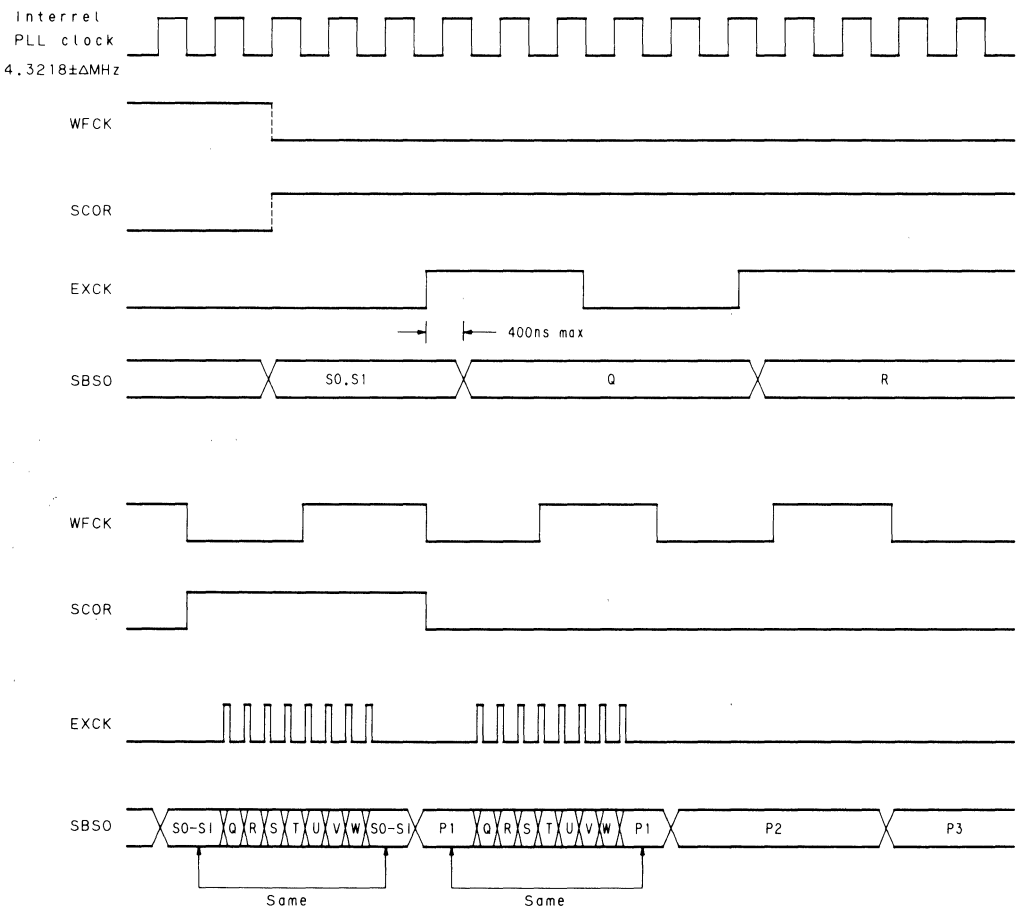
§ 2-2 80bit Sub Q Read

Figure 2-2 shows a block diagram of the peripheral part of the 80-bit Sub Q register.

- The Sub Q regenerated on a bit-per-frame basis is input to the 80-bit serial/parallel register and the CRC circuit.
- When the results of a CRC on the 96bits of Sub Q are OK, CRCF is set to 1 and the 96-bit data is output to SQSO.
  Furthermore, the 80-bit data is loaded into the 80-bit, parallel/serial register.
  If SQSO is found "H" after the output of SCOR, the CPU realizes that a new set of data has been loaded after passing a CRC.
- When 80-bit data is loaded CXD2500A, the bit arrangement is reversed within each byte of the data. Therefore, the bits are ordered LSB-first within each byte, even though the byte arrangement is kept unchanged.
- When 80bits of data are confirmed to have been loaded, SQCK is input to read the data. Subsequently in the CXD2500A, the input of SQCK is detected and the retriggerable Mono/Multi is reset during Low.
- The time constant of the retriggerable Mono/Multi ranges from 270 to 400 us. During SQCK High if it is less than this time constant, the Mono/Multi is kept being reset, preventing the contents of the P/S register from being loaded into the P/S register.
- While the Mono/Multi is kept reset, data loading into the peak detection parallel/serial register and 80-bit parallel/serial register is forbidden.
  Therefore, while data read operation is carried out at clock periods not exceeding the time constant for the Mono/Multi, the contents of these registers are retained without being rewritten, for example, when a CRC is passed.
- The CXD2500A permits the peak detection register to be connected to the shift-in of the 80-bit P/S register. The input and output terminals of Ring Control 1 are interconnected in the peak meter mode as well as level meter mode, while those of Ring Control 2 are interconnected only in the peak meter mode.
  The purpose of these Ring Control arrangements is to reset the registers every time their contents are read in the level meter mode, while preventing their contents from being destroyed by read operation during the peak meter mode.
  To enable this control, it is essential to input 96 clock pulses for read operation in the peak meter mode.
- As mentioned earlier, the detection of a peak value in the peak meter mode is followed by the storing of the next absolute time.
  A timing chart for these operations is shown in Figure 2-3.

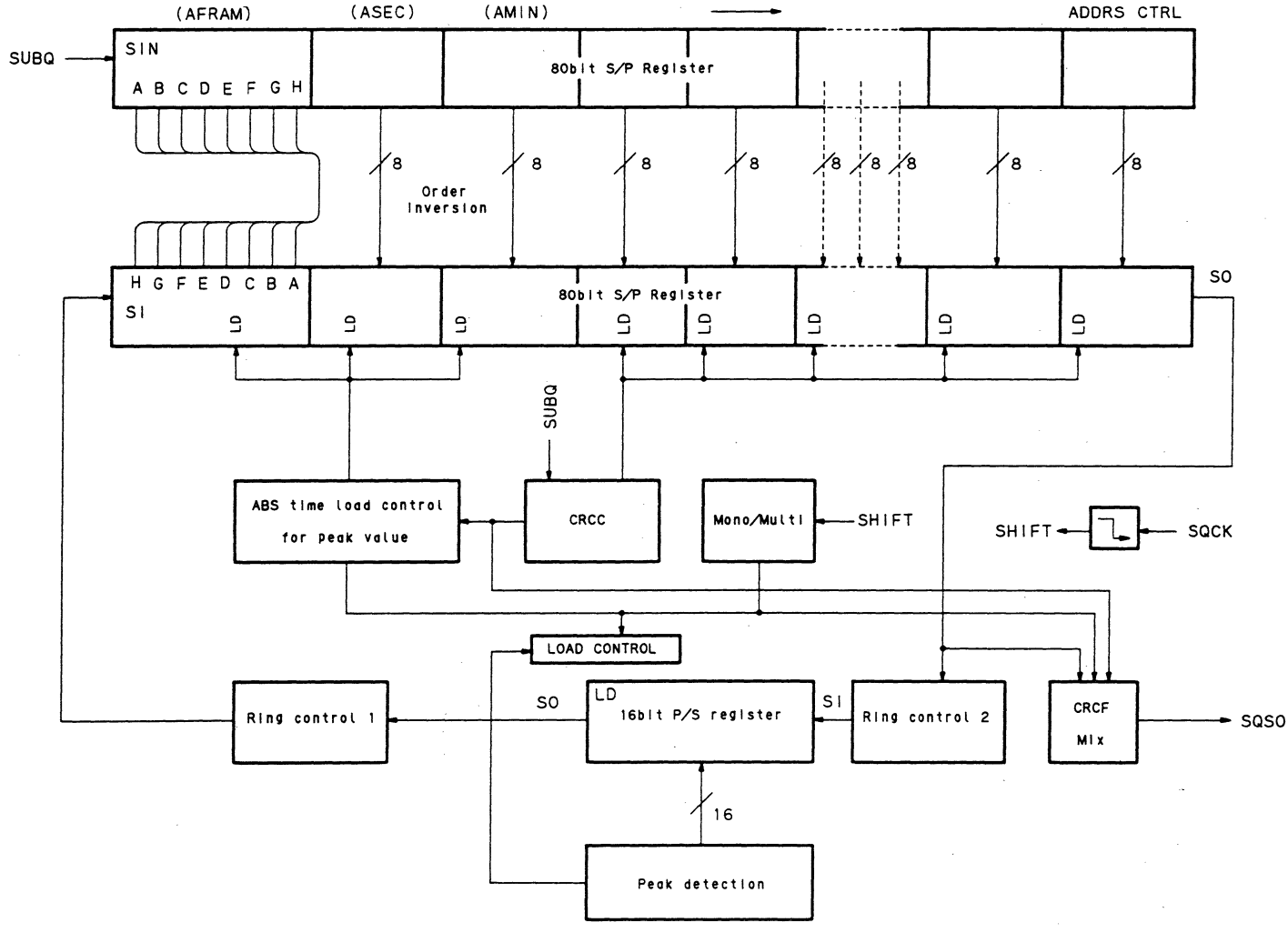
Note: The "H" as well as "L" duration of the clock pulses to be input to the SQCK pin to perform the above-described operations must be between 750ns and 120μs.

Timing Chart 2-1

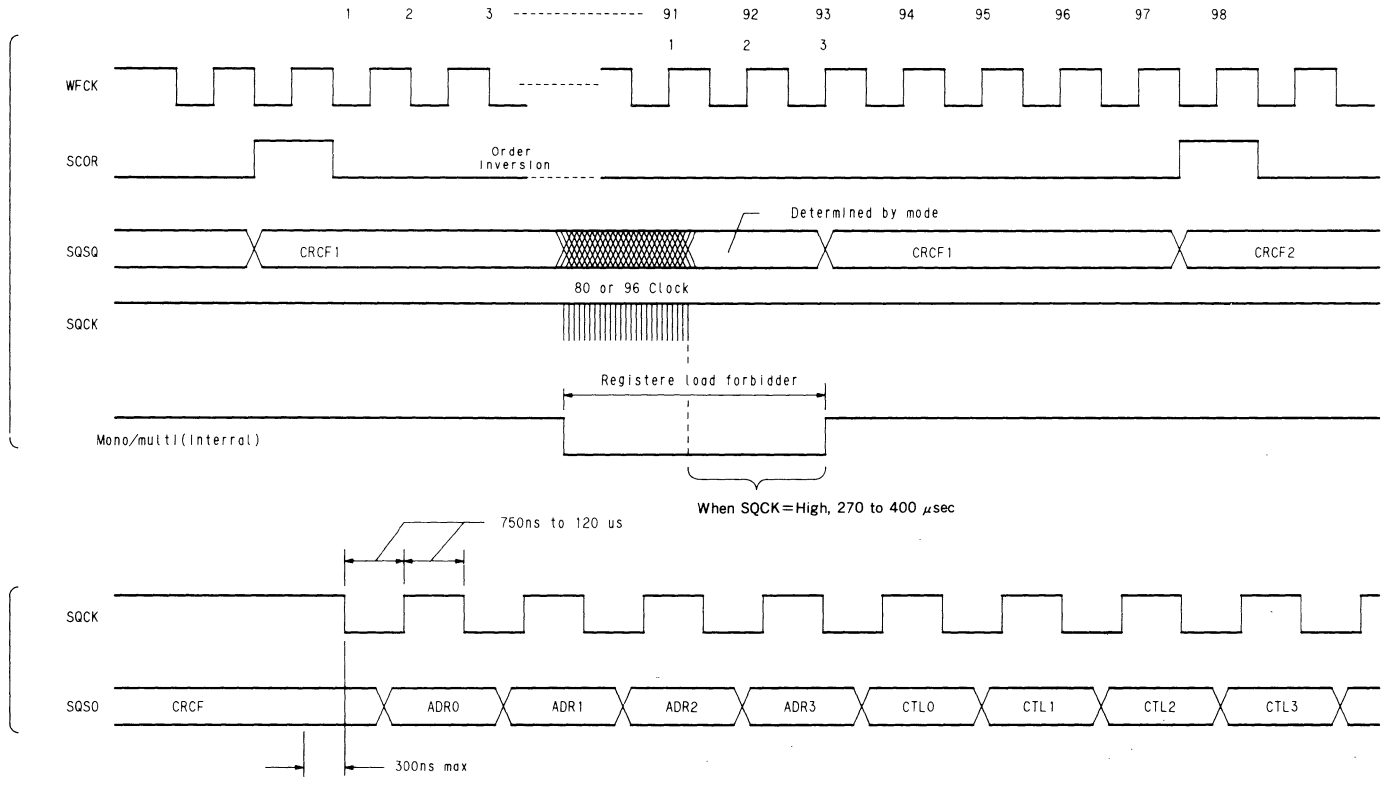


Subcode P. Q. R. S. T. U. V. W Read Timing

Block Diagram 2-2



Timing Chart 2-3



§ 3 Other Functions

§ 3-1 Channel Clock Regeneration Using Digital PLL Circuit

○ Demodulation of the EFM signal regenerated using an optical system requires the use of channel clock pulses.
The EFM signal to be demodulated has been modulated into an integer multiple of the channel clock period T, ranging from 3T to 11T.
To read the information conveyed by the EFM signal, it is essential to correctly recognize the value of the integer and, hence, to use channel clock pulses.
In a real CD player, the pulse width of the EFM signal fluctuates being affected by fluctuations of the disc rotation. For this reason, it is necessary to use a PLL in regenerating channel clock pulses.

Figure 3-1 shows a block diagram of the 3-stage PLL contained in the CXD2500A.

○ The 1st-stage PLL is used for vari-pitch regeneration. To use this PLL, it is necessary to prepare an LPF and a VCO as external parts.
The minimum pitch variation achievable is 0.1%. The output of this 1st-stage PLL is used as the base signal for all the clock pulses to be used in the LSI.
When vari-pitch control is not performed, connect the output pin of XTAO to the VCKI pin.

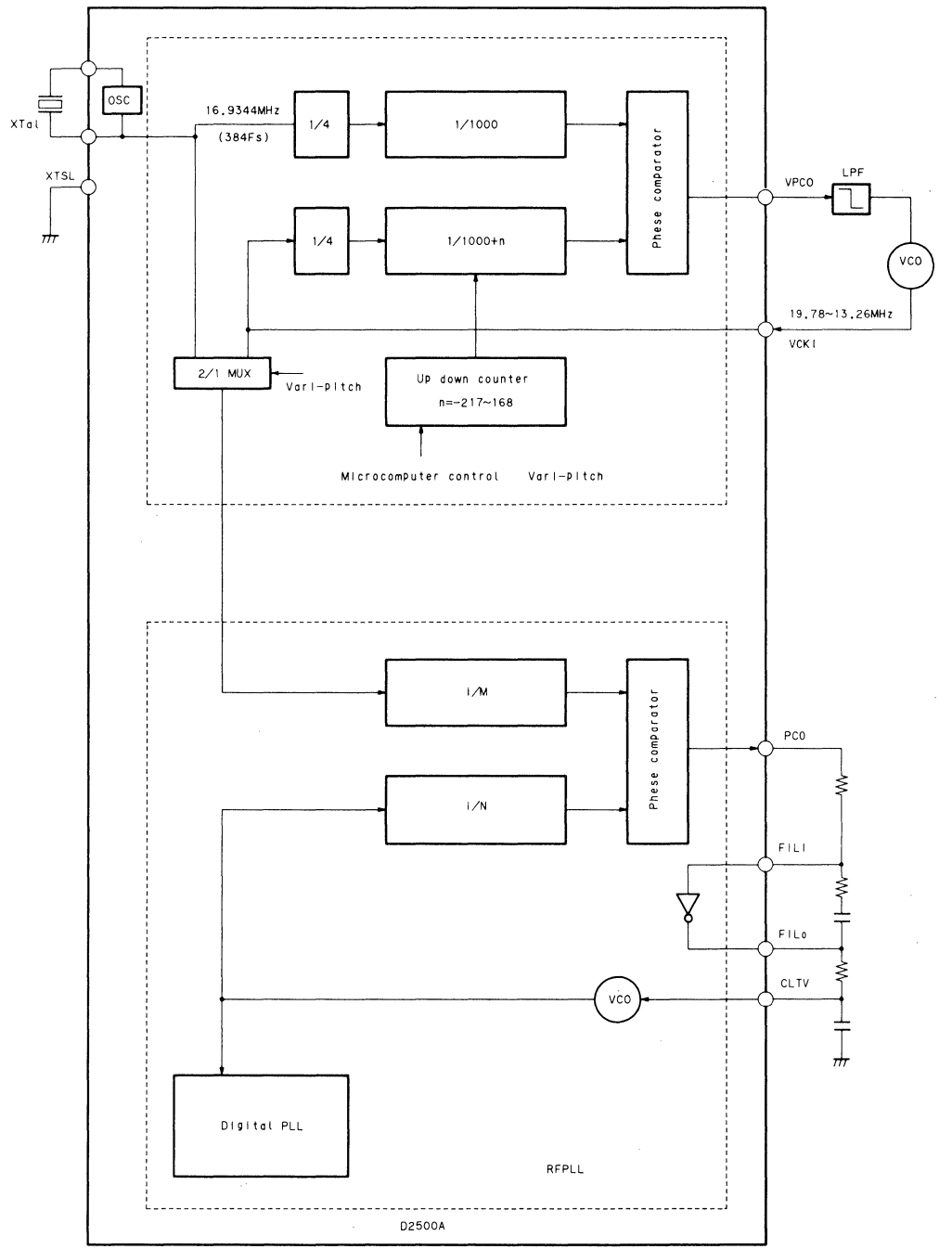
○ The 2nd-stage PLL generates R.F. clock pulses for use by the 3rd-stage digital PLL.

○ The 3rd-stage comprises a digital PLL used to regenerate channel clock pulses. It realizes a capture range of ±150kHz (normal condition) or more.

○ The digital PLL features a secondary loop. It is controlled through the primary loop (phase) and secondary loop (frequency).
When FLFC=1, the secondary loop can be turned off.

○ When high frequency components such as 3T, 4T or else, are offset, turning off the secondary loop will provide better play ability.
In this case, however, capture range reaches 50kHz.

Block Diagram 3-1



§ 3-2 Frame Sync Protection

○ During CD player operation at normal speed, Frame Sync is recorded about every 136μs (at 7.35kHz). This signal can be used to identify the data within each frame. When Frame Sync cannot be recognized for any data, the data cannot be identified and, as a result, it is treated as an error. Therefore, correct Frame Sync recognition is very important to ensure high playability for the CD player.

○ For Frame Sync protection, the CXD2500A employs window protection, front protection and rear protection. These measures combined realize powerful Frame Sync protection. The CXD2500 offers two window widths, one for use when the player is subjected to rotational disturbance and the other for use without such disturbance involved (WSEL=0/1).

The front portection counter is fixed at count 13 and the rear protection counter at 3. Therefore, if, while Frame Sync signals are regenerated normally, regenerated signals cannot be detected, for example, due to flaws on the disc, up to 13 frames can be interpolated. If the number of frames with undetected Frame Sync exceeds 13, the window is released and the Frame Sync signals are re-synchronized. If no Frame Sync is correctly detected in 3 successive frames immediately after Frame Sync re-synchronization performed following a window release, the window is released at once.

§ 3-3 Error Correction

○ On CDs, each data unit (8bits) is formated so that it is contained in two correction codes, C1 and C2. C1 consists of 28 bytes of information and a 4-byte parity, whereas C2 are made up of 24 bytes of information and a 4-byte parity. Both C1 and C2 comprise a reed Solomon code with a minimum distance of 5.

○ C1 realizes double corrections and C2 quadruple corrections, both, by the refined superstrategy method.

○ When correction by C1 is made, a C1 pointer determined according to the contents of the error, the status of EFM signal regeneration and the condition of CD player operation is attached to the corrected data so as to prevent erroneous correction by C2.

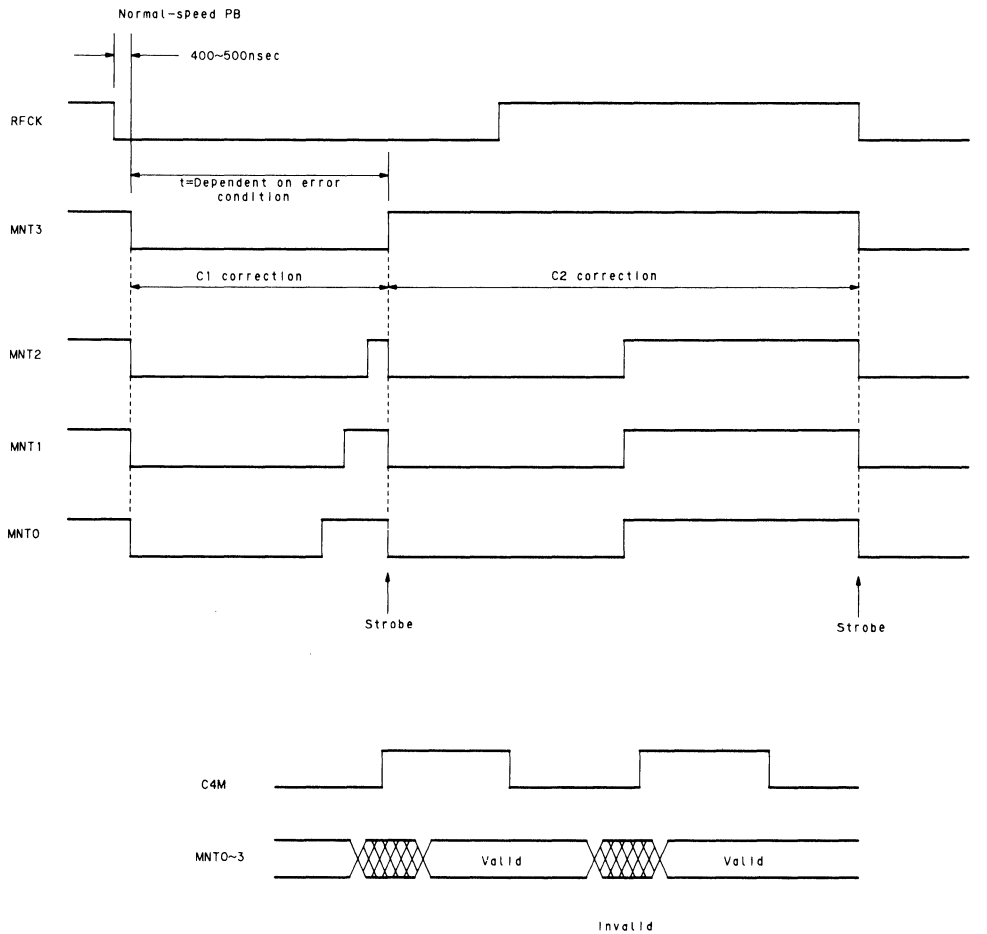
○ The status of error correction can be monitored from outside the LSI. It is indicated as shown in Table 3-2.

○ If an uncorrectable data error is detected, the previous data that has been held is substituted for the erroneous data or substitute data is created by average-value interpolation. In either case, a C2 pointer attached to the substitute data is set high.

MNT3	MNT2	MNT1	MNT0	Description	
0	0	0	0	C1 : No error detected.	C1 pointer reset.
0	0	0	1	C1 : 1 error corrected.	C1 pointer reset.
0	0	1	0	———	
0	0	1	1	———	
0	1	0	0	C1 : No error detected.	C1 pointer set.
0	1	0	1	C1 : 1 error corrected.	C1 pointer set.
0	1	1	0	C1 : 2 errors corrected.	C1 pointer set.
0	1	1	1	C1 : Uncorrectable error.	C1 pointer set.
1	0	0	0	C2 : No error detected.	C2 pointer reset.
1	0	0	1	C2 : 1 error corrected.	C2 pointer reset.
1	0	1	0	C2 : 2 errors corrected.	C2 pointer reset.
1	0	1	1	C2 : 3 errors corrected.	C2 pointer reset.
1	1	0	0	C2 : 4 errors corrected.	C2 pointer reset.
1	1	0	1	———	
1	1	1	0	C2 : Uncorrectable error.	C1 pointer copied.
1	1	1	1	C2 : Uncorrectable error.	C2 pointer set.

Table 3-2 Indication of error correction status

Timing Chart 3-3



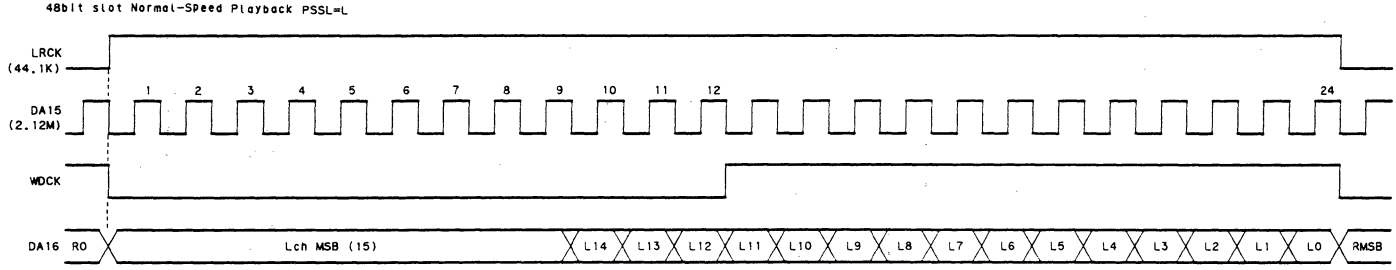
§ 3-4 DA Interface

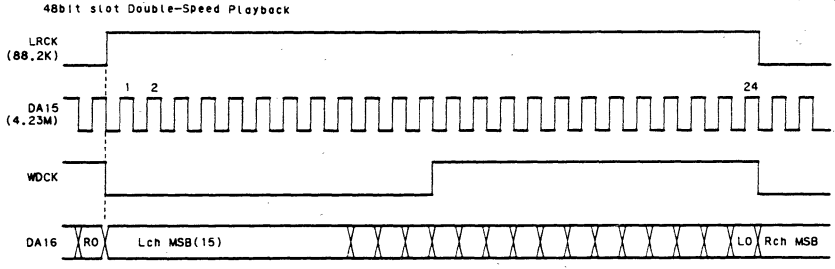
○ The CXD2500A has two modes of DA interface.

a). 48-bit slot interface
This is an MSB-first interface made up of LRCK signals with 48bit clock cycles per LRCK cycle. While the LRCK signal is high, the data going through this interface is of the left channel.

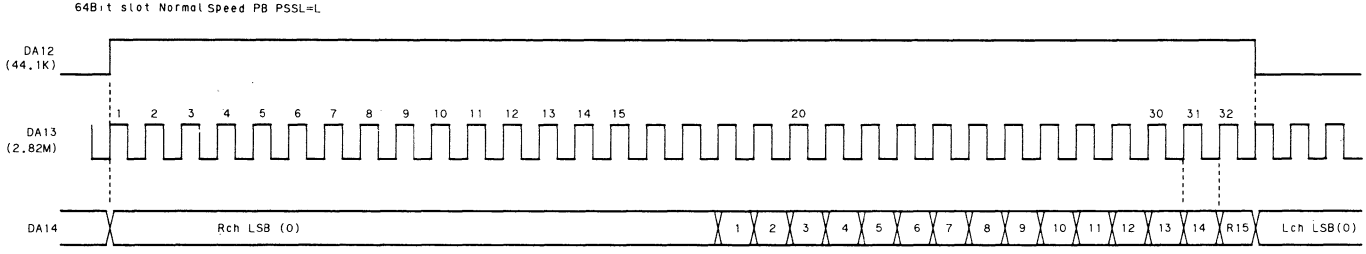
b). 64-bit slot interface
This is an LSB-first interface made up of LRCK signals with 64bit clock cycles per LRCK cycle. While the LRCK signal is low, the data going through this interface is of the left channel.

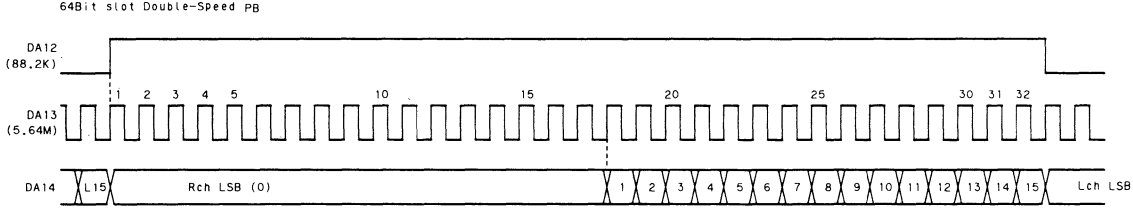
Timing Chart 3-4





Timig Chart 3-5





§ 3-5 Digital Out

There are three digital-out formats: type 1 for use at broadcasting stations, type 2, form 1 for use in general civil applications, and type 2, form 2 for use in software production. The CXD2500A supports type 2, form 1.

The clock accuracy for the channel status is automatically set at level II when the Xtal clock is used or level III when vari-pitch control is made.

CRC checks are conducted on the Sub Q data on the first 4 bits (bits 0-3). The data is input only after two checks are passed in succession.

The Xtal clock is set to 32MHz, and variable pitch is reset. When DSPB is set to 1, as D out is output, set MD2 to 0 and D out to off.

Digital Out C bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

Bits 0-3: Sub Q control bits required to pass the CRC twice in succession.
bit 29 : Varipitch: 1 Xtal: 0

Table 3-6 Digital Out C bits

§ 3-6 Servo Auto Sequencer

The servo auto sequencer controls a series of operation including auto-focusing and track jumping. When an auto sequence command is received from the CPU, the servo auto sequencer automatically executes auto-focusing, 1-track jumping, 2N track jumping and N track moving.

During auto sequence execution (X Busy=Low), as SSP (servo signal processing LSI) is used exclusively, commands from the CPU are not transferred to SSP. Still, commands can be sent to CXD2500A.

To make this servo auto sequencer usable, connect a CPU, RF and SSP to the CXD2500Q as shown in Figure 3-7 and set A.SEQ ON-OFF of register 9 to ON.

When X Busy is at Low, as the clock turns from Low to High, from there and for a maximum of 100μsec, X Busy does not turn to High.

As this clock is at Low (when X Busy is at Low), and through the monostable multivibrator that is reset, when X Busy changes from Low to High, transfer of error data to SSP is prevented.

(a) Auto Focus ($47)

In auto focus operation, 'focus search up' is perfomed, FOK and FZC are checked, and the focus servo is turned on. When a $47 is received from the CPU, the focus servo is turned on through the steps shown in Figure 3-8. Since this auto focus sequence bigins with 'focus search up,' it requires the pickup to be put down (focus search down) beforehand.

Blind E of register 5 is used to prevent FZC from flapping. The focus servo is turned on when FZC goes low after staying high for a period longer than E.

CXD2500Q System Configuration for Auto Sequencer Operation (Example)

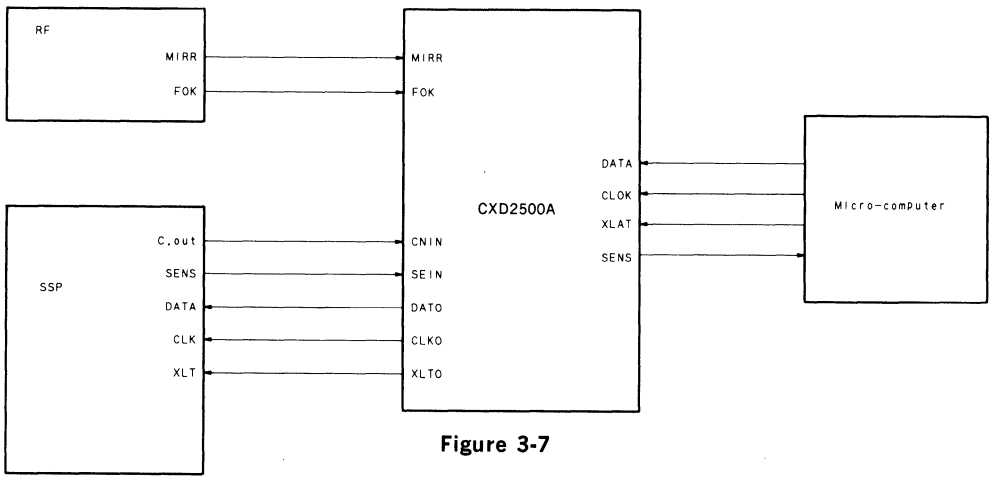


Figure 3-7

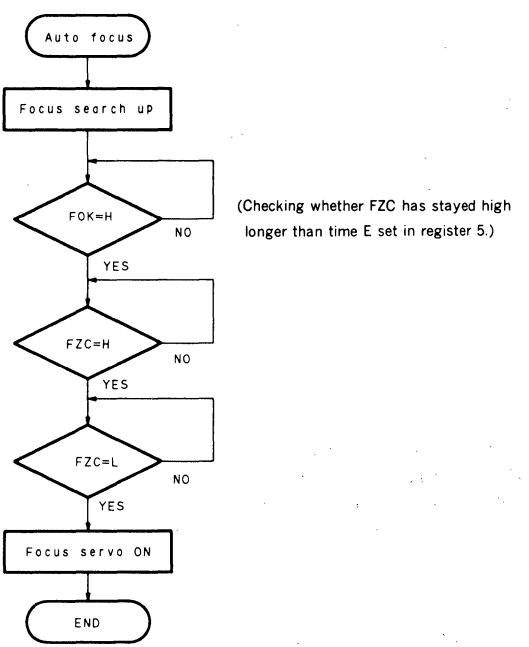


Figure 3-8 (a) Flowchart of auto focus operation

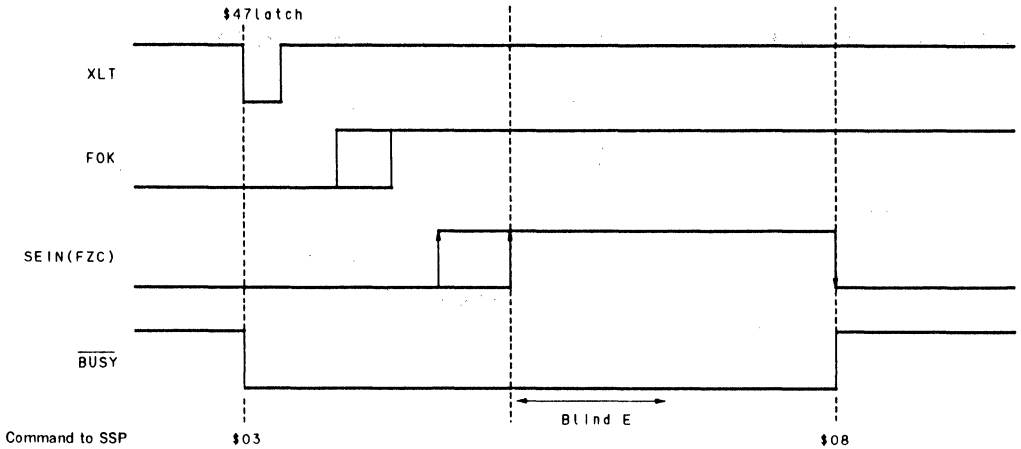


Figure 3-8 (b) Timing chart for auto focus operation

(b) Track Jump

Track jump operation includes 1, 10 and 2N track jumps. Do not perform this track jump unless the focus, tracking and sled servos are on. Such steps as tracking gain up and braking are not included in this track jump. Therefore, the commands for tracking gain up and brake on ($17) must be issued in advance.

○ 1-track jump

When a $48 (or a $49 for a REV jump) is received from the CPU, the servo auto sequencer executes a FWD (REV) 1-track jump as shown in Figure 3-9. The values of blind A and brake B must be set in register 5.

○ 10-track jump

When a $4H (or a $4B for a REV jump) is received from the CPU, the servo auto sequencer executes a FWD (REV) 10-track jump as shown in Figure 3-10. The principal difference between the 1-track and 10-track jumps is whether the sled is kicked or not. In the 10-track jump, the actuator after being kicked is braked when CNINs have been counted for 5 tracks. When the actuator has adequately slowed down as a result of braking, the tracking and sled servos are turned on (this actuator slow-down is detected by checking whether the CNIN period has exceeded the time specified as overflow C in register 5).

○ 2N track jump

When a $4C (or a $4D for a REV jump) is received, the servo auto sequencer executes a FWD (REV) 2N track jump. The number of tracks to be jumped is determined by N whose value is to be set in register 7 beforehand. The maximum permissible number is 2^{16}. In reality, however, it is subject to limitation imposed by the actuator.

When N is smaller than 16, the jumps are counted by means of counting CNIN signals. If N is not smaller than 16, MIRR signals are counted instead of the CNIN signals.

The 2N track jump sequence is basically the same as the 10-track jump sequence. The only difference between them is that, in the 2N track jump sequence, the sled is kept moving for time D specified in register 6 after the tracking servo is turned on.

○ N track move

When a $4E (or a $4F for a REV move) is received from the CPU, the servo auto sequencer executes a FWD (REV) N-track move as shown in Figure 3-12. The maximum value that can be set for N is 2^{16}. The track moves are counted in the same way as for 2N track jumps. That is, when N is smaller than 16, the moves are counted by means of counting CNIN signals. If N is not smaller than 16, MIRR signals are counted instead of the CNIN signals. In this N track move, only the sled is moved. This method is suitable for a large track move ranging from several thousand to several tens of thousand of tracks.

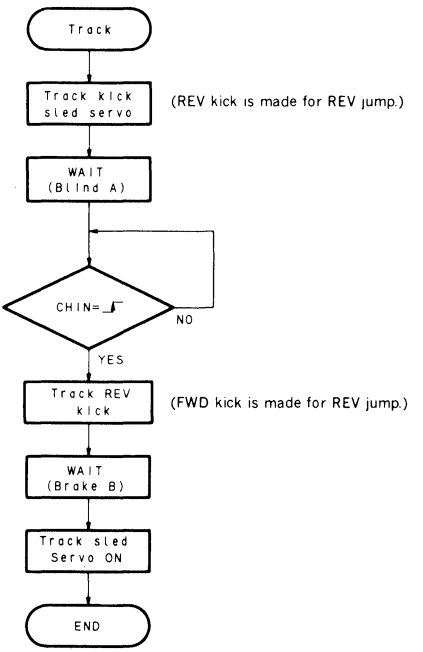


Figure 3-9 (a) Flowchart of 1-track jump

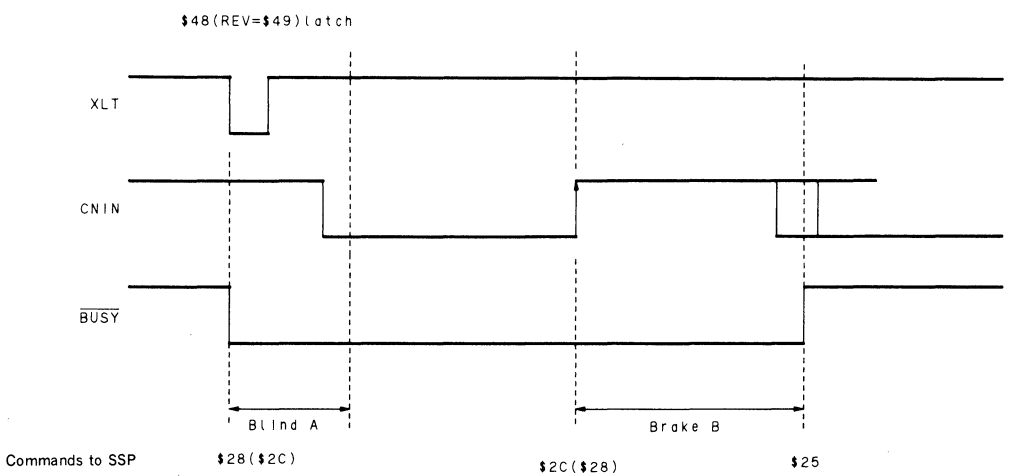


Figure 3-9 (b) Timing chart for 1-track jump

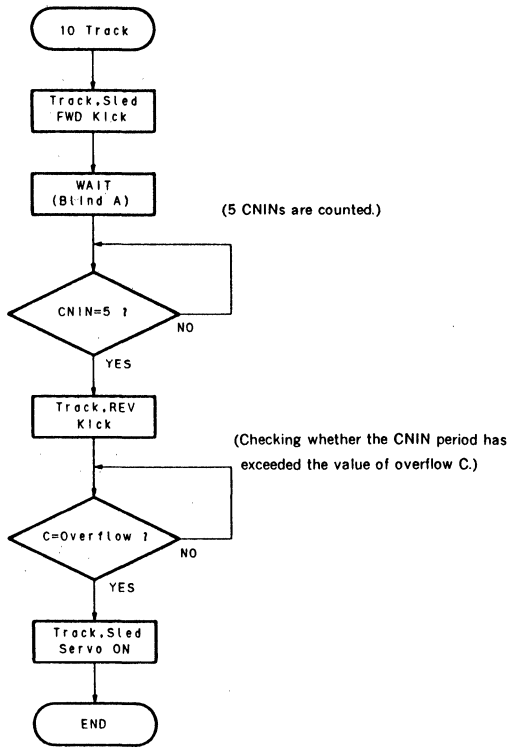


Figure 3-10 (a) Flowchart of 10-track jump

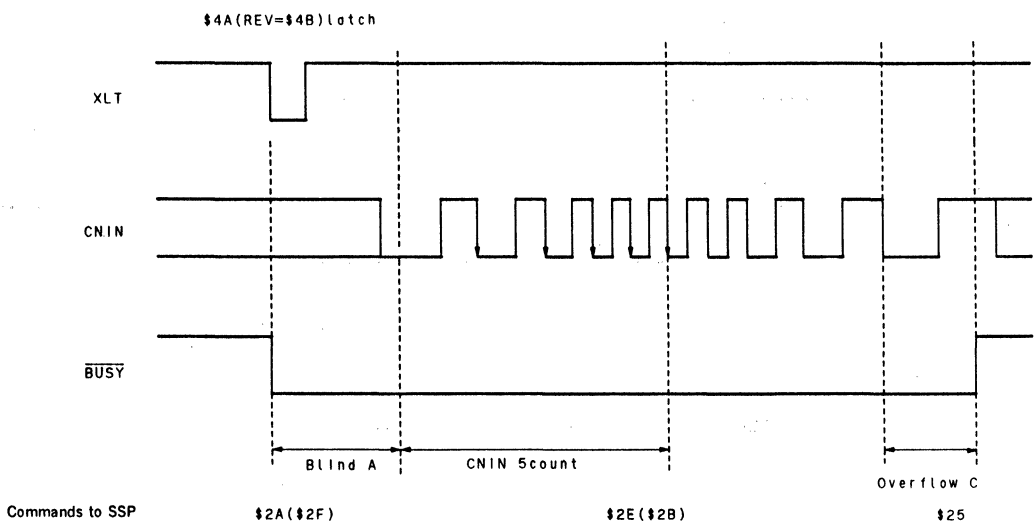


Figure 3-10 (b) Timing chart for 10-track jump

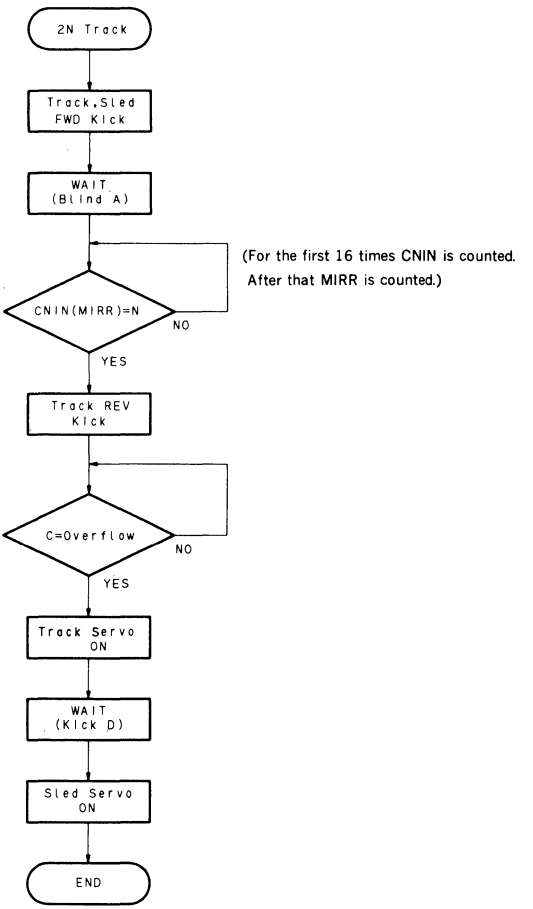


Figure 3-11 (a) Flowchart of 2N track jump

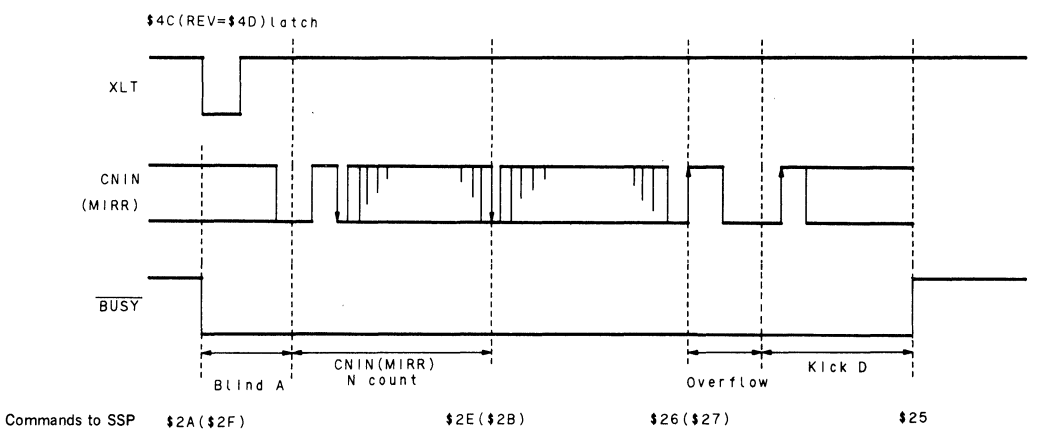


Figure 3-11 (b) Timing chart for 2N track jump

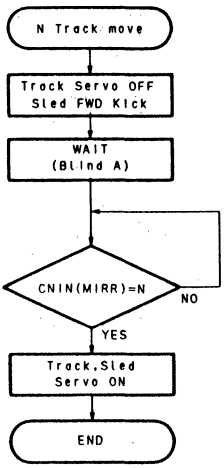


Figure 3-12 (a) Flowchart of N track move

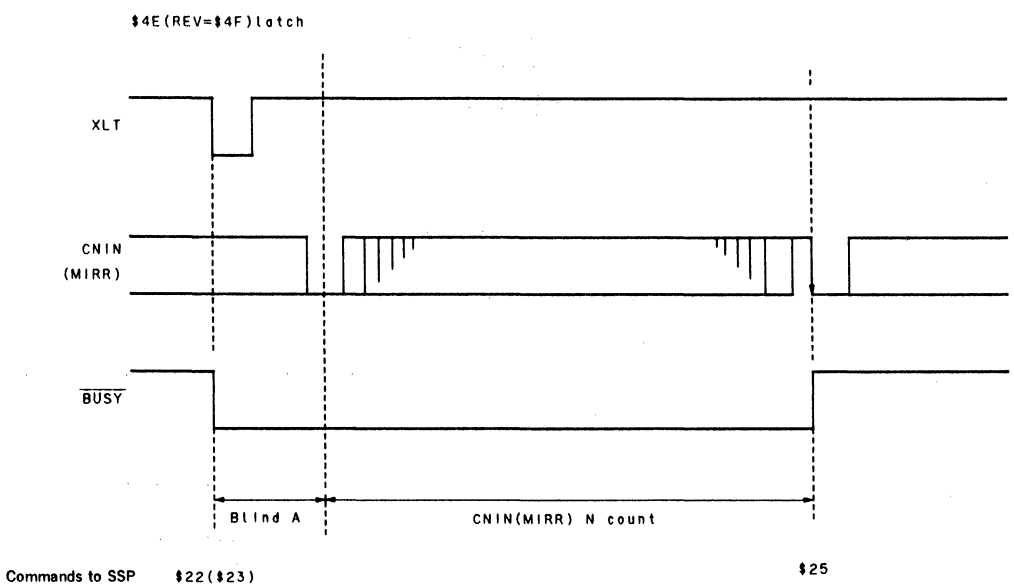


Figure 3-12 (b) Timing chart for N track move

§ 3-7 Digital CLV

The digital CLV is a digital spindle servo, a block diagram of which is shown in Figure 3-14. It is capable of outputting MDS or MDP error signals by the PWM method after raising the sampling frequency up to 130kHz based on the normal speed in the CLVS, CLVP or another appropriate mode. It permits gain setting, also.

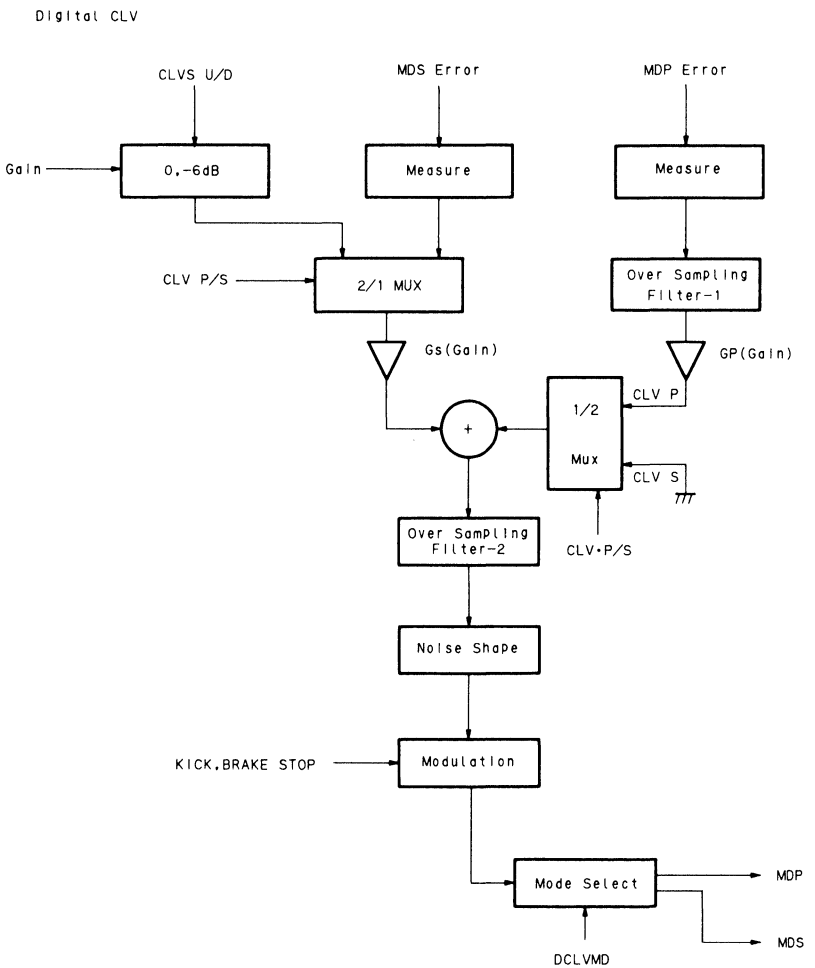


Figure 3-14 Block diagram

§ 3-8 Asymmetry correction

Block diagram and circuit example are shown on Fig. 3-15.

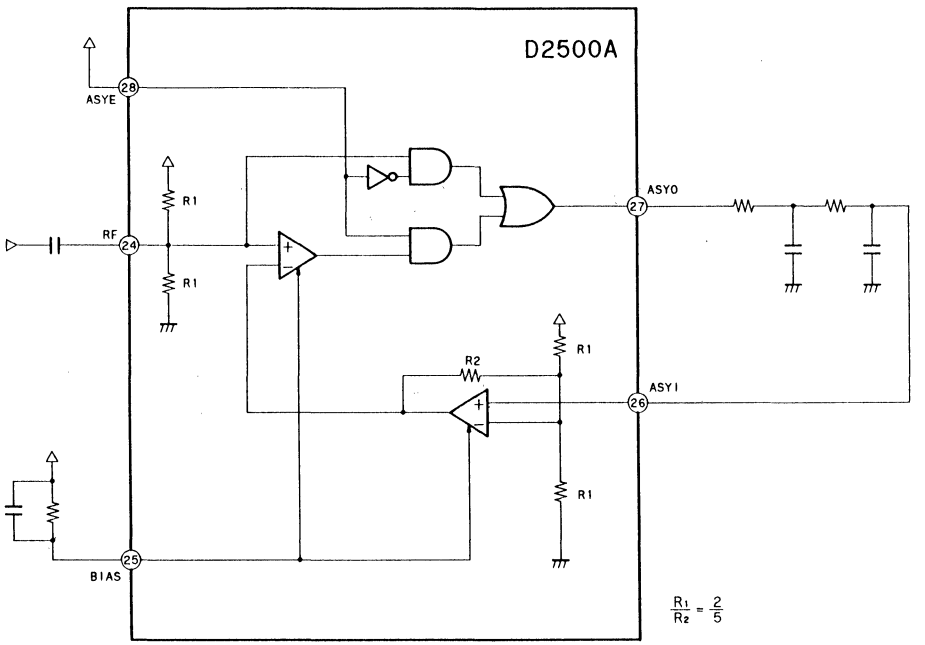
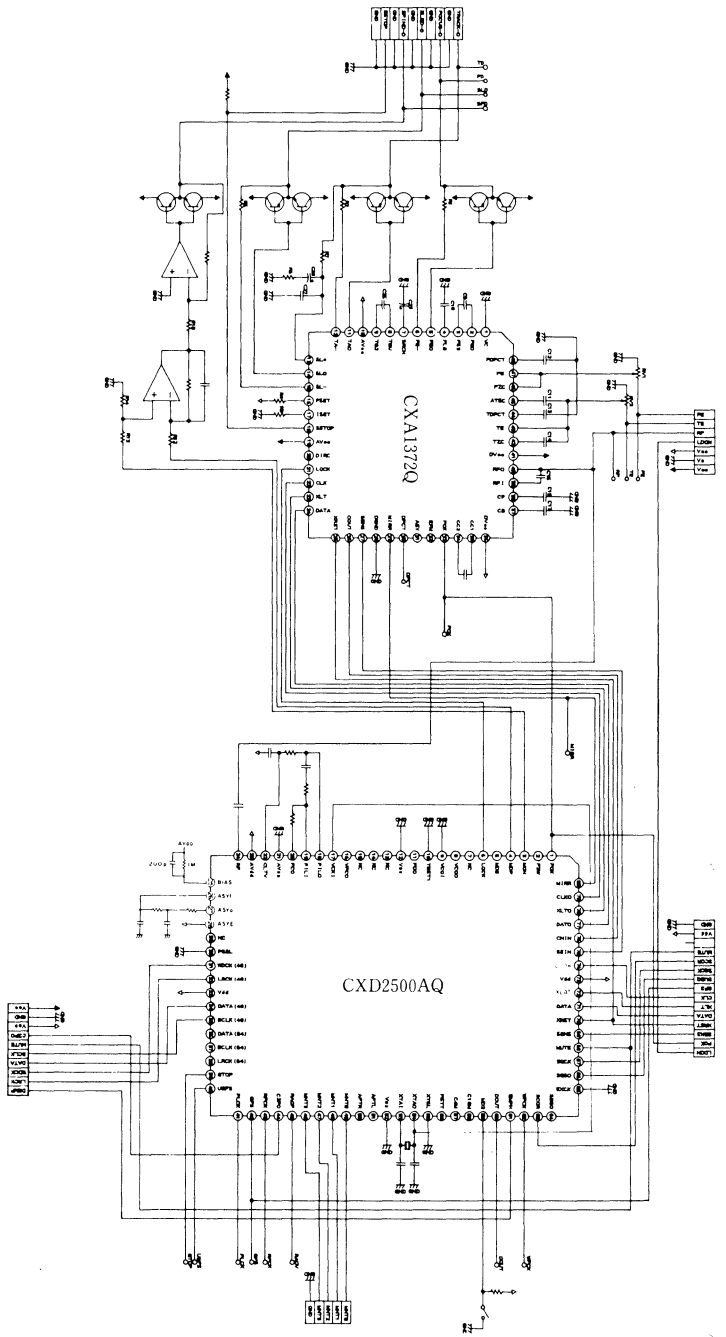


Figure 3-15 Asymmetry correction application circuit example

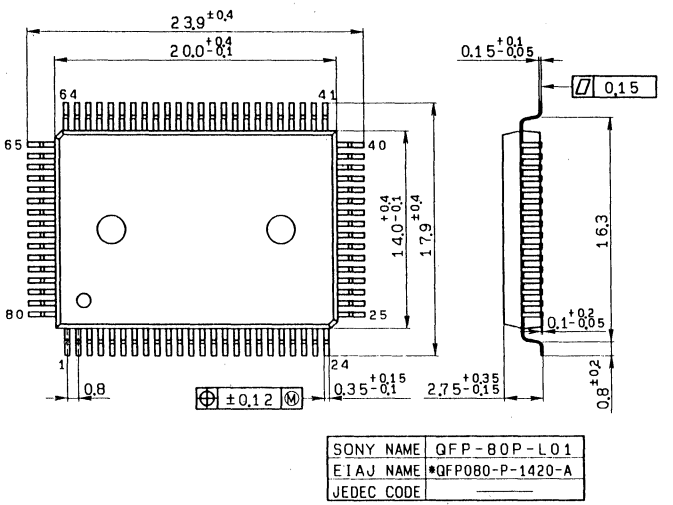
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

CXD2500AQ 80pin QFP (Plastic) 1.6g



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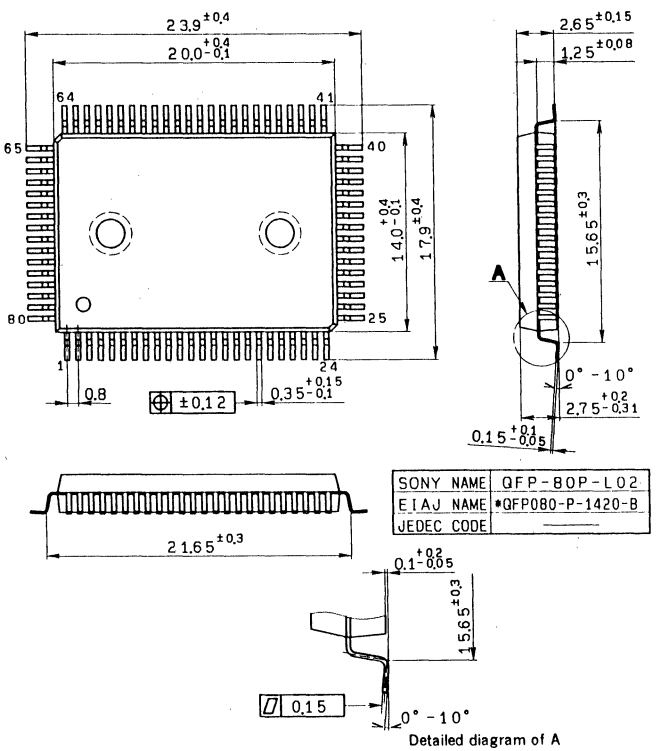
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

CXD2500AQZ 80pin QFP (Plastic) 1.6g

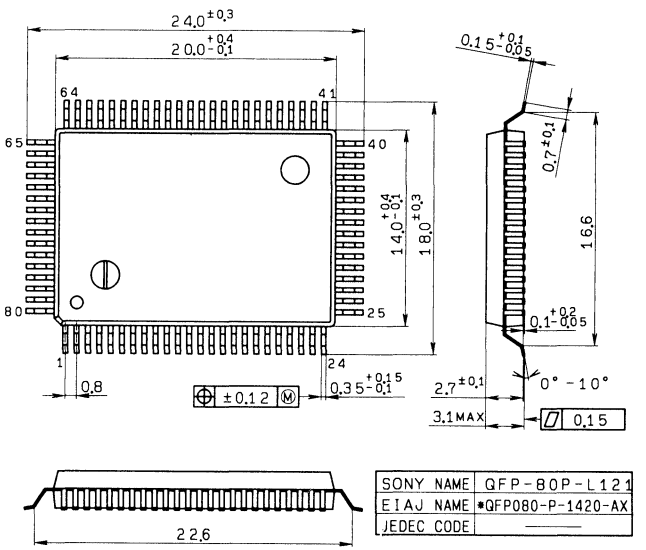


SONY NAME	QFP-80P-L02
EIAJ NAME	*QFP080-P-1420-B
JEDEC CODE	———

Detailed diagram of A

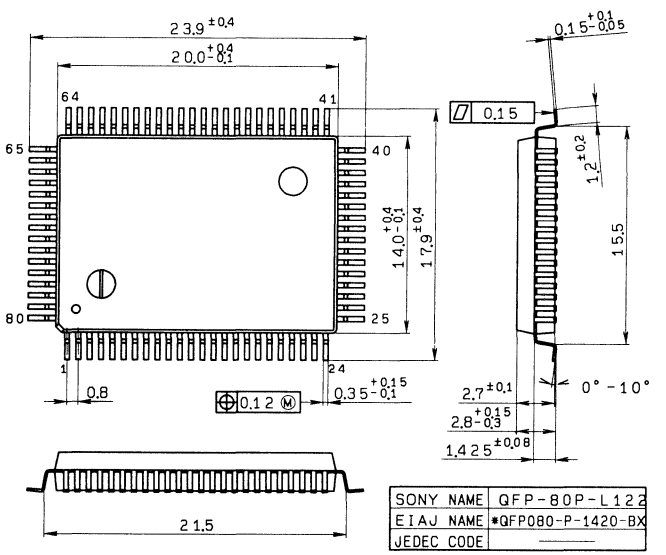
CXD2500AQ

80pin QFP (Plastic)



CXD2500AQZ

80pin QFP (Plastic)



Application Notes

Application Notes

Reference Number	Description	Recommended IC's	Page
CAV01	Audio A/D + D/A interface	CXD2555Q	509
CAV02	NTSC/PAL encoder Y, C interface	CXA1145P/M	511
CAV03	NTSC/PAL decoder & Comb filter	CXA1228S, CXL5504M	512
CAV04	Digital comb filter interface	CXD2011Q, CXK1202S/Q, CXD1176Q, CXA1365S, CXD1030M	515
CAV05	NTSC/PAL Encoder, RAMDAC interface	CXA1145M, CXD1030M, CXK1202S/Q	517
CAV06	Gen Lock circuit	CXA1365S, CXD1030M	518
CAV07	NTSC/PAL Decoder digital interface	CXA1228S, CXD1179Q, V7021, CXD1172AM, CXD1030M, CXK1206M, CXA1365S	520
CAV08	New CD-ROM Decoder	CXD1196R, CXD2552Q	522

Application Note CAV01
Audio A/D+D/A - CXD2555Q interface

1. Minimum requirement for ADC input.

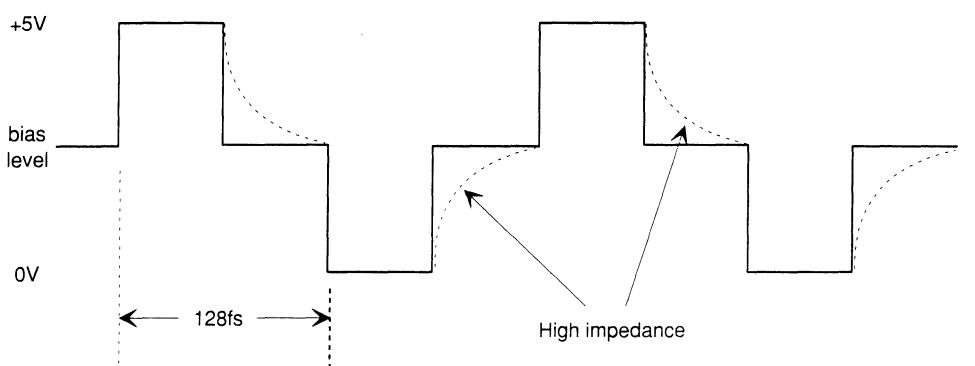
The external Low Pass Filters are used for eliminating aliasing noise, because there is a decimation filter (128fs sampling). This IC only needs to cut off more than 64fs frequency component. The sampling frequency (Fs) is more than 8KHz. Therefore, the roll off can be more than 500KHz. Only 1st order filter is required.

2. MAF (Moving Average Filter)

This block is down sampling, PDM (Pulse Density Modulation) data which is filtered at 128 times over sampled. The data rate will be 4 times fs. 32 input data are manipulated, averaged and transferred to the next stage.

3. PDM Output

Output data rate is 128fs. If fs=48KHz, the rate is 6.144MHz. The Wave form is as follows: A middle level represents high impedance output. The number of "1" and "0" pulses give the analog output level. If its analog output level is at center level, the number of "1" and "0" are equal.



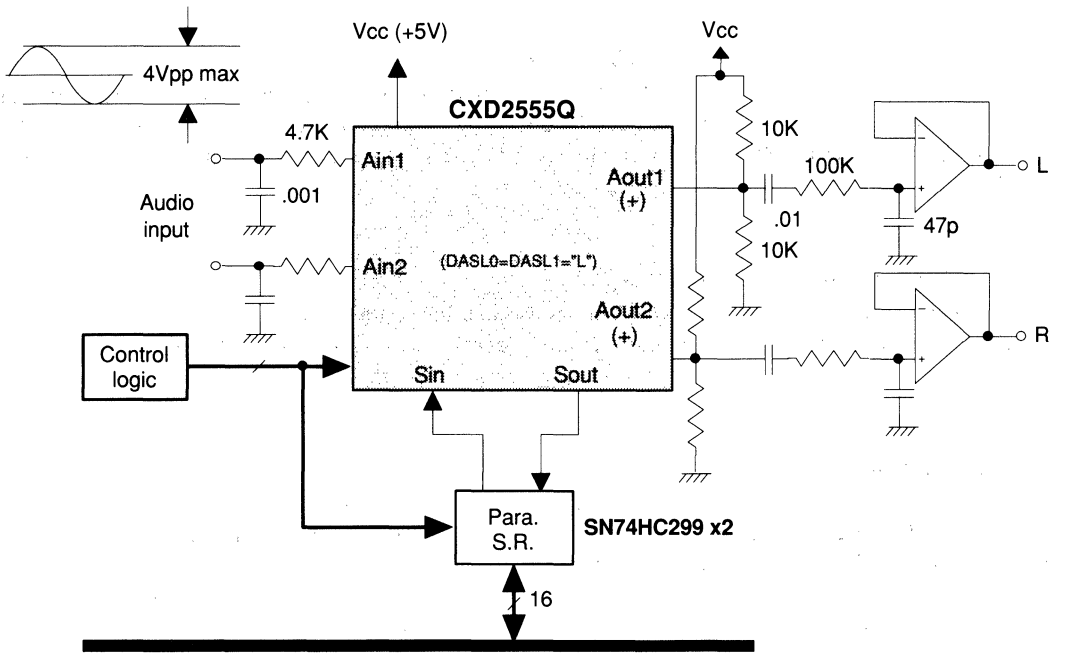
Filtering is necessary to eliminate 128fs component. Attenuation level for stop band frequency component is -45dB level. If it is necessary to increase this level, additional LPF is recommended to be used.

4. Simple External Circuit (See attached circuit diagram)

It is recommended that the two peripheral chips to be used for computer applications, and the Common mode DAC output may simplify your system.

SN74HC299 TI 8 bit Seri-Para Converter

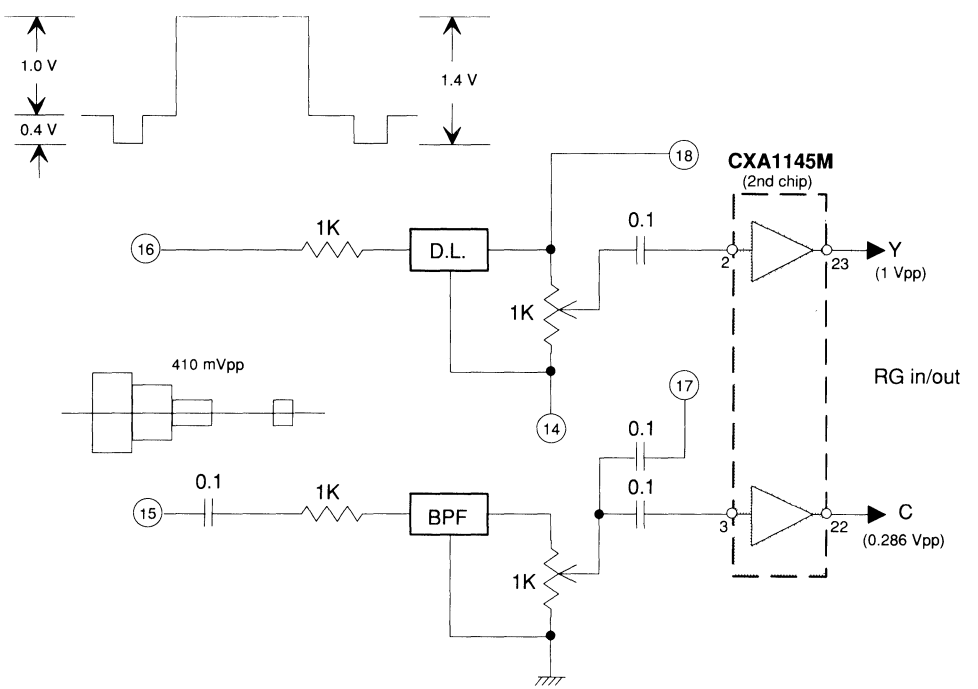
CXD2555Q External Circuit Example



Application Note CAV02
NTSC/PAL Encoder Y, C Interface

RGB encoder - CXA1145P/M can provide Y, C output. The following is the circuit diagram to apply this output. S-VHS requires 75ohm drive capability for Y, C output. Output level should be adjusted with 1K ohm potentiometers. Recommended parts are the following, and are available from TOKO America (Telephone: 708/297-0070).

3.58MHz Band Pass Filter	H286BAIS-6276DCD
4.43MHz Band Pass Filter	H286BAIS-4963DCD
Delay Line	H288LSMS-3245PKD



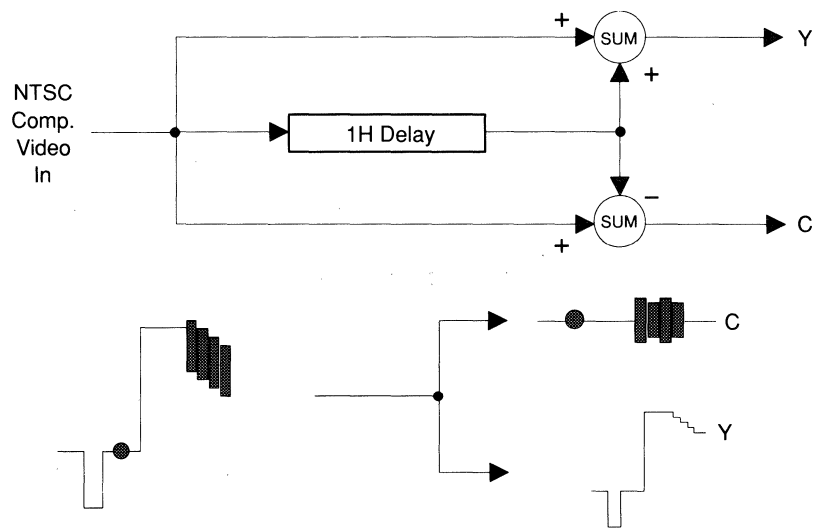
Application Note CAV03
NTSC/PAL Decoder & Comb Filter

1. NTSC Composite Video Y/C Separation

Because NTSC composite video signal is a modulated signal of Y and C, the following crosstalk may occur in signal process:

Cross Color	Y to C Crosstalk
Dot Crawling	C to Y Crosstalk

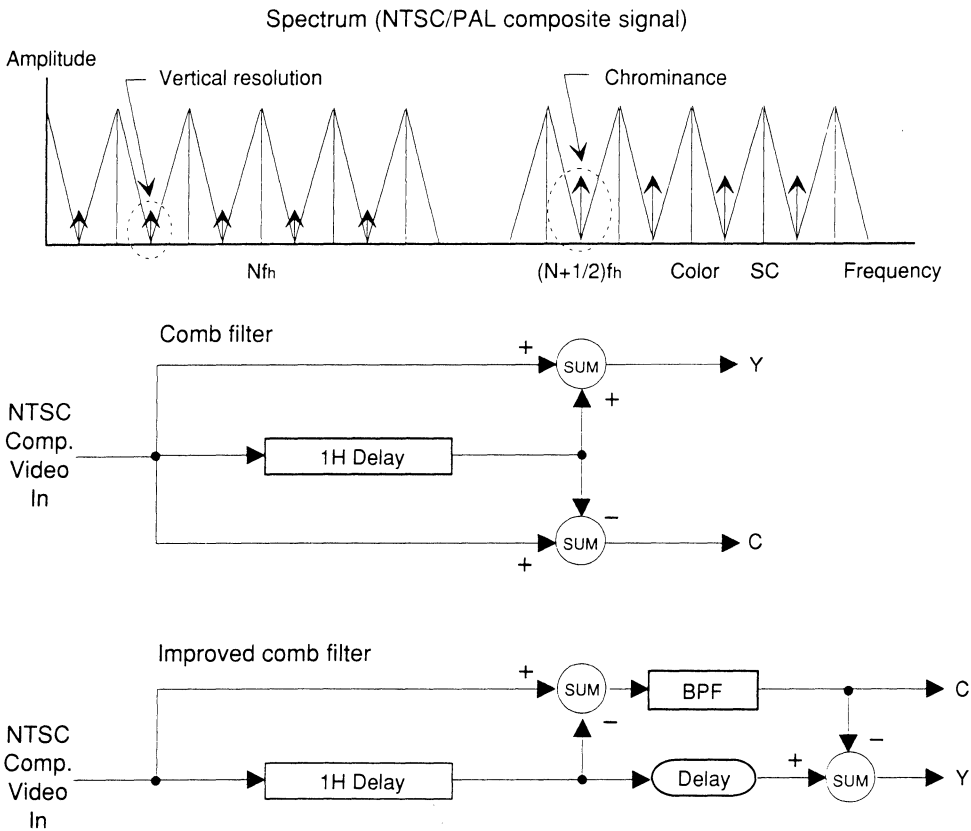
To avoid above errors, normally 1H delay line is used for Y/C separation. The chroma signal phase has a 180 degree shift in evey H interval (Interlaced), the Y and C signal can be separated in the following way:



However, the low frequency components concentrated on harmonics of the sub carrier frequency will be combed away, and it will reduce the vertical resolution and decrease the sharpness of image in the vertical direction.

The following scheme can improve the vertical resolution:

Amplitude Vertical Resolution Chrominance



This can improve both cross color error and vertical resolution, but requires more components. Sony Digital comb filters can be recommended if the digital signal processor converting the digital Y, C data to RGB is available (See Application Note CAV04).

The simple solution may be the combination of BPF (Band Pass Filter) and Notch filter as mentioned in Sony NTSC/PAL decoder data sheet. It is better in video applications because there are more low frequency components existing in the sub carrier harmonics (n + 1/2) x fh.

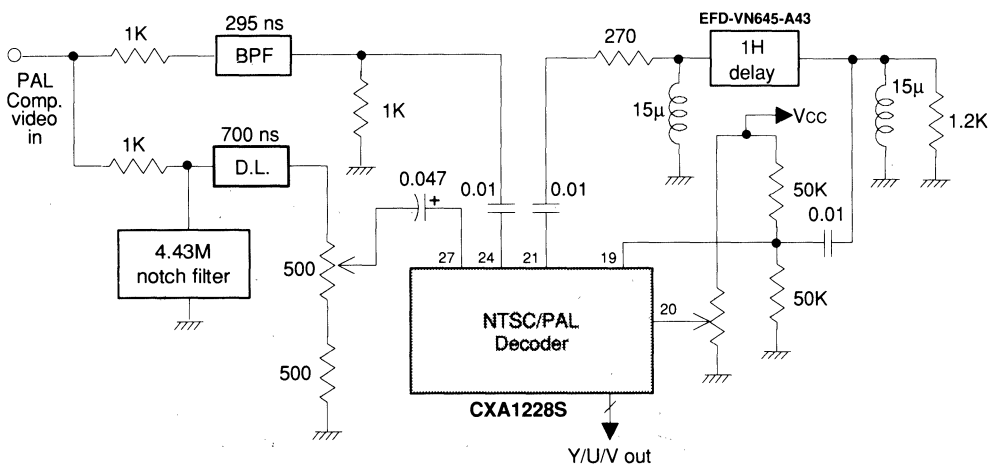
The comb filter is suitable for the still picture application, it can increase SNR. CXL5504M is NTSC CCD delay line recommended for Y/C separation.

3. PAL Decoder

4.43MHz trap and BPF (Band Pass Filter) combination are used for the PAL system. Besides, DAT and 1H delay line (Glass delay type) for chroma demodulation, Ultrasonic Delay line is also recommended. A supplier for the 1H delay line and a notch filter is Panasonic (Telephone: 201/348-5200). 1H CCD delay line can not be used for this application because there is no sync signal added on the chroma output signal at pin 21. Asahi Glass Corporation (Telephone: 011-81-3-3218-5781)

4.43MHz notch filter	A285TCHS-7566	TOKO
4.43MHz notch filter	EFC-A4434BF	Panasonic
4.43MHz Band Pass Filter	H286BAIS-4963DCD	TOKO
400ns Delay Line } 700ns	H345HEC-6277VFD	TOKO
300ns LPF	H288LSMS-3245PKD	TOKO
1H Ultrasonic Delay Line (PAL)	FED-VN645-A43	Panasonic
1H Glass delay line (PAL)	ADL-CP144S	Asahi
Delay Adjust Transformer	BTKANS-18267DTY	TOKO

An application circuit is shown below:



Application Note CAV04
CXD2011Q Application Note 1

1. What is the digital comb filter?

The NTSC/PAL digital video system requires many ICs to compensate for several errors - cross color, dot crawling, interline flickers, and so on. Y/C separation process is the key to eliminate these errors. The 1H comb filter is used for eliminating cross color, and dot crawling because these errors are caused by Y to C or C to Y crosstalk (See Application Note CAV03).

The current digital TV system uses interframe Y/C separation, which is superior for the still video application. However the number of field memories are necessary and the noise from the moving picture can not be eliminated. (Therefore, 1H comb filter is used together with the interframe Y/C separators and the detector circuit for movement detection decide to switch between two Y/C separators.) But, the simple 1H comb filter can not compensate the cross color when there is no correlation in the adjacent lines. It is better to use BPF in such a case.

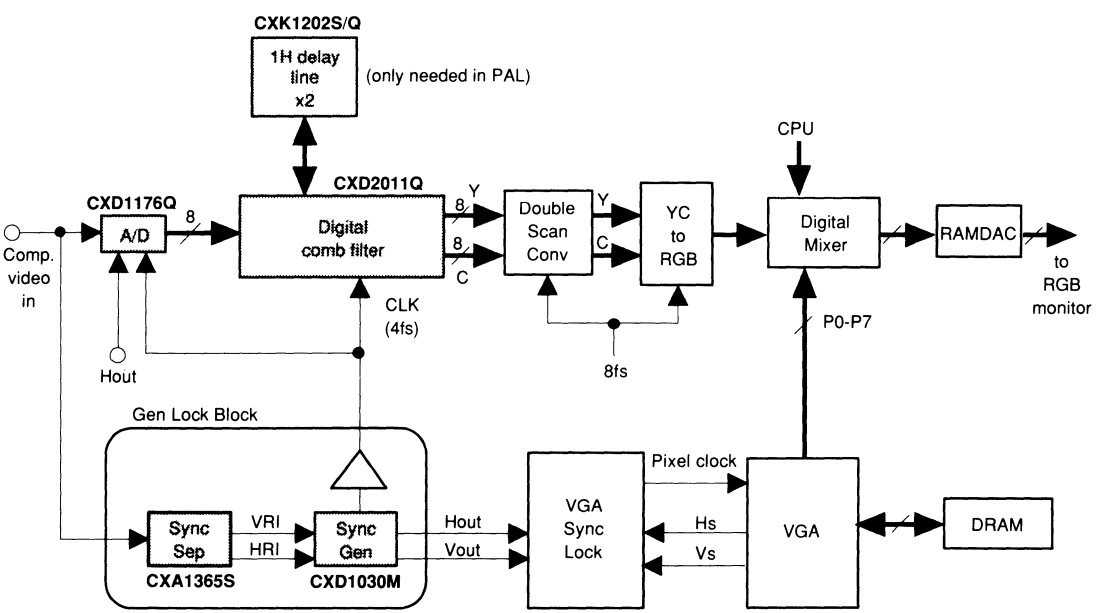
The digital comb filter - CXD2011Q is developed for improving the quality of the moving picture Y/C separation, combining together with the interframe Y/C separation. Both still video and moving picture quality can be improved.

In typical video applications (VCR, TV), the CXD2011Q alone can fulfill the function of noise compensation. IC switches 1H comb and BPF by detecting the difference in the adjacent line data.

2. How to use CXD2011Q in the computer system.

Combination of 8 bit 20MSPS A/D - CXD1176Q, the digital Y/C data (8 bit) can be generated. This example shows the overlay application with VGA controller IC. 1H Digital delay line - CXK1202S/Q are utilized to change the H sync frequency from 15.743KHz to 31.486KHz for NTSC system.

VGA Interface Block Diagram

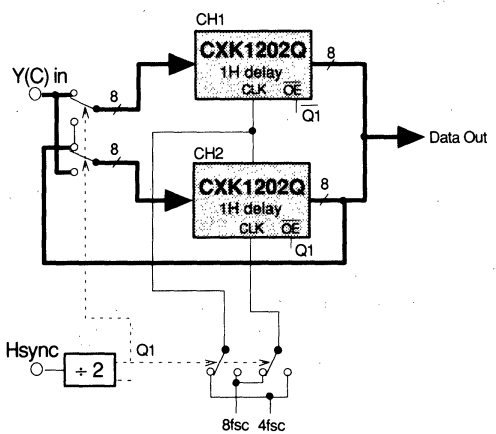


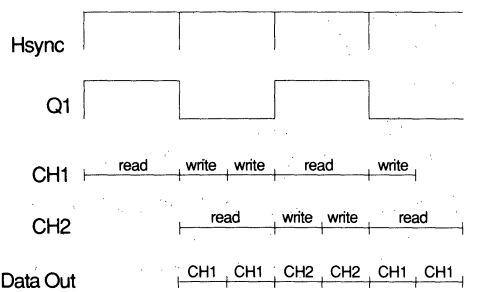
Double Scan Speed Converter

The VGA chip does not have H, V sync input to synchronize with the external video sync. The future VGA chip may have the internal PLL to lock the pixel clock with the external sync signal. The Gen Lock circuit example will be described in Application note - CAV06. The Digital mixer circuit, and Y/C to RGB conversion circuit may be necessary. The double scan method can be used for converting external H sync frequency to that of VGA.

Y, C signals from Digital Comb filter are interlaced signals with 15.743KHz sync cycle.

Double scan means interlace to non-interlaced conversion - Read one line and write 2 lines with double speed. 2 ICs can be switched Read and Write Cylce each other. However, this method cause flicker between the fields. Recommendation is using just one field (even or odd).

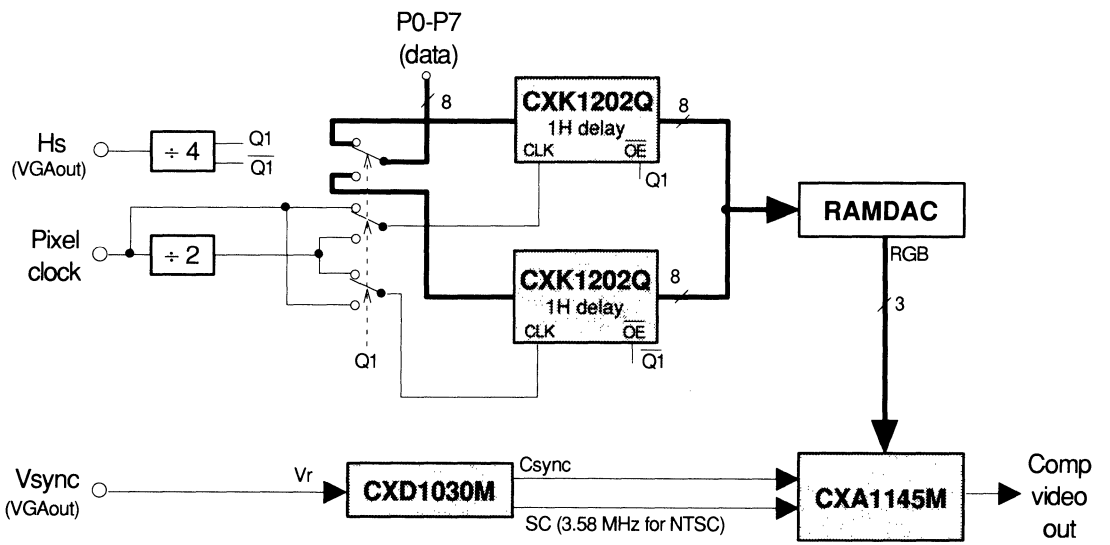




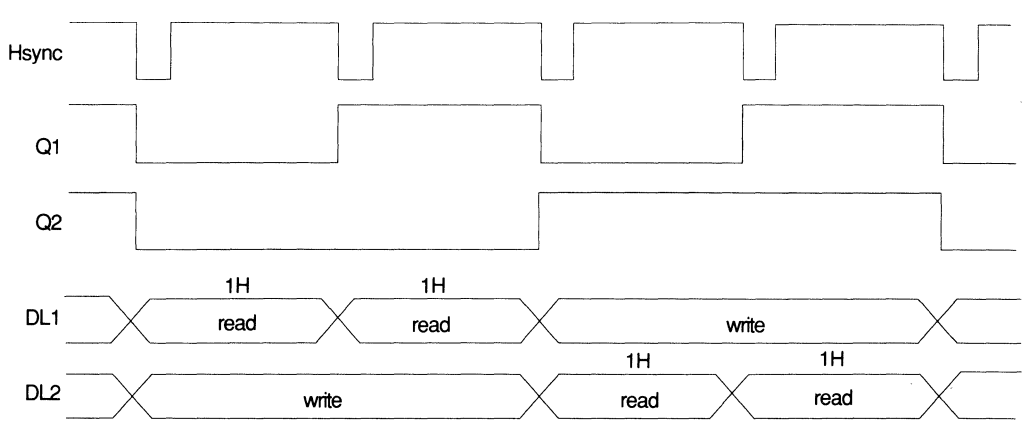
Application Note CAV05
NTSC/PAL Encoder, RAMDAC Interface

1. VGA Interface

Utilizing the NTSC/PAL encoder, RAMDAC output can be stored into the VCR and/or can be displayed on a TV monitor. However, the non-interlaced signal should be converted to the interlaced video. One way of doing this, is by using the 1H digital delay lines in the following circuit:



Timing Diagram



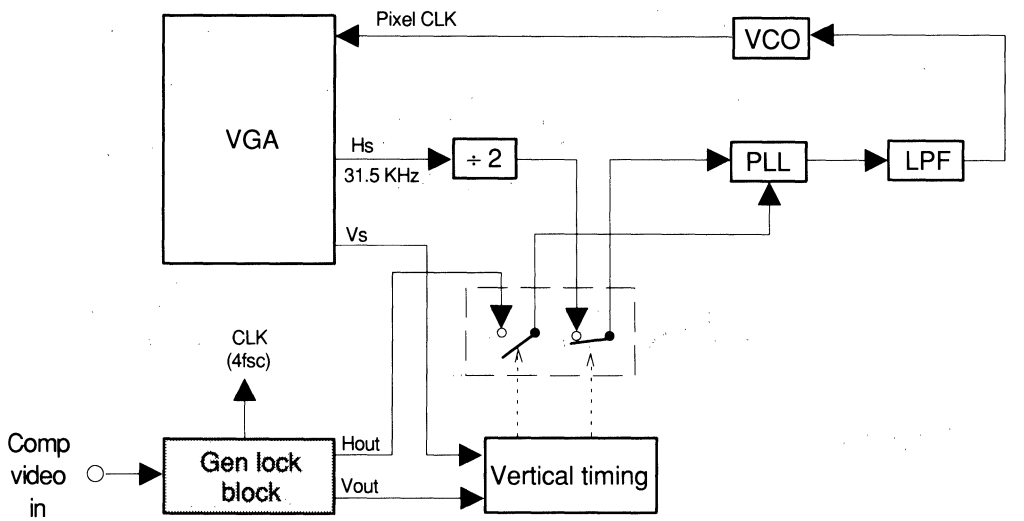
Application Note CAV06
Gen Lock Circuit

1. Gen Lock System

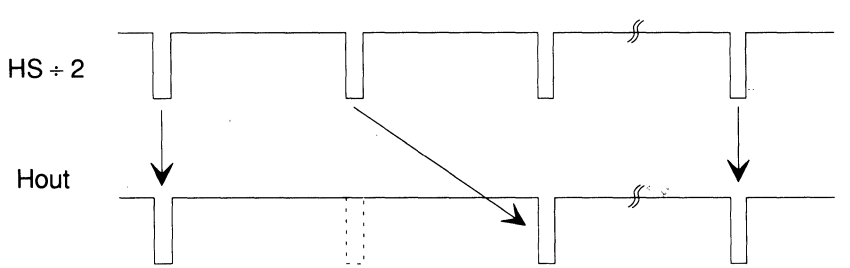
The Sync separator - CXA1365S and the Sync generator - CXD1030M are recommended to be used together. When the H sync drop happens in the VCR signal source, CXD1030 can generate H sync during the lack of sync period. Also 4fsc (4 times sub carrier frequency) generated in Gen Lock circuit. (Detail circuit diagram is shown on page 6-11).

2. VGA Sync Lock Circuit

The software solution may work in V sync lock with the external video. The future VGA chip needs to have V reset input at least to simplify the interface circuit. Because of lack of V, H sync input the VGA chip should be locked with the pixel clock. The hardware solution; H sync from both VGA and video are compared together with PLL and lock the pixel frequency. To adjust the timing difference in V sync, H sync from either VGA or video is taken away in each V interval, if there is more than 1 H time difference. The following is the diagram for this PLL circuit:

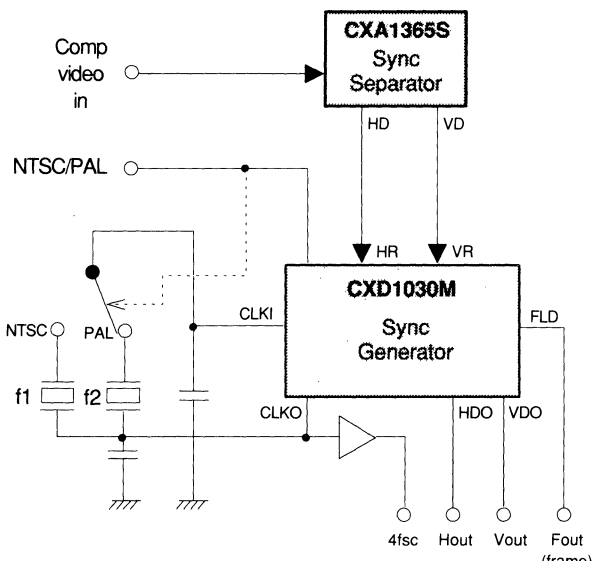


H extraction timing
(1H shift/V interval)



Normally the Gen Lock circuit does synchronize the sub carrier of the video to that of the internal clock generator. 1H delay line (CXL5504M or CXK1202S/Q type) requires an accurate, 4 times sub carrier frequency; the NTSC/PAL signal process needs this frequency clock. However, it is not necessary to be locked with Y sync in the computer applications. Instead, H sync must to be locked with the pixel clock for Graphic displays. The pixel clock frequency is quite different from Video sub carrier (See Application note CAV07).

The actual video signal sometimes has the unstable H sync signal - jitter and tracking error. Loosing H sync in several H sync intervals may occur, so extracting H from video can not fulfill the Gen Lock function. Gen Lock circuit "generates" the H sync; CXD1030M is used for this purpose. Simplified Gen Lock block is as shown here:



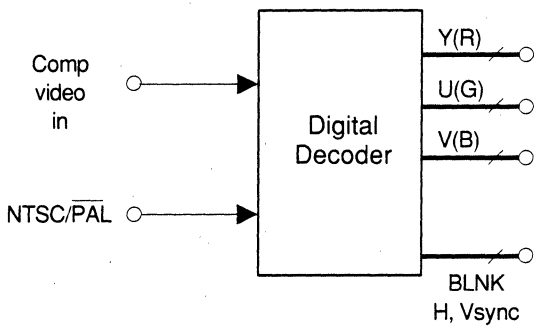
f1 = 14.31818 MHz (NTSC)
f2 = 14.1875 MHz (PAL)

Application Note CAV07
NTSC/PAL Decoder Digital Interface

1. Computer Video In Applications

Digital interface to the computer requires A to D converters (A/D's). The speed range is 12-18 MHz, the resolution is 5-10 bit. RAMDAC requires RGB input with 5 bit resolution for video. XGA requires additional bit for B. Possibly the 6 bit 20 MHz A/D is the best choice for VGA overlay application.
Teleconference type applications require Y/U/V (Y/R-Y/B-Y) digital interface. The sampling frequency is chosen by the display resolution. (Typically 640x480) D1 (4:2:2) format set the sampling frequency 13.5 MHz both for NTSC and PAL system.

2. NTSC/PAL Digital decoder with D1/Square pixel mode selection.



SC11410 M,N selection

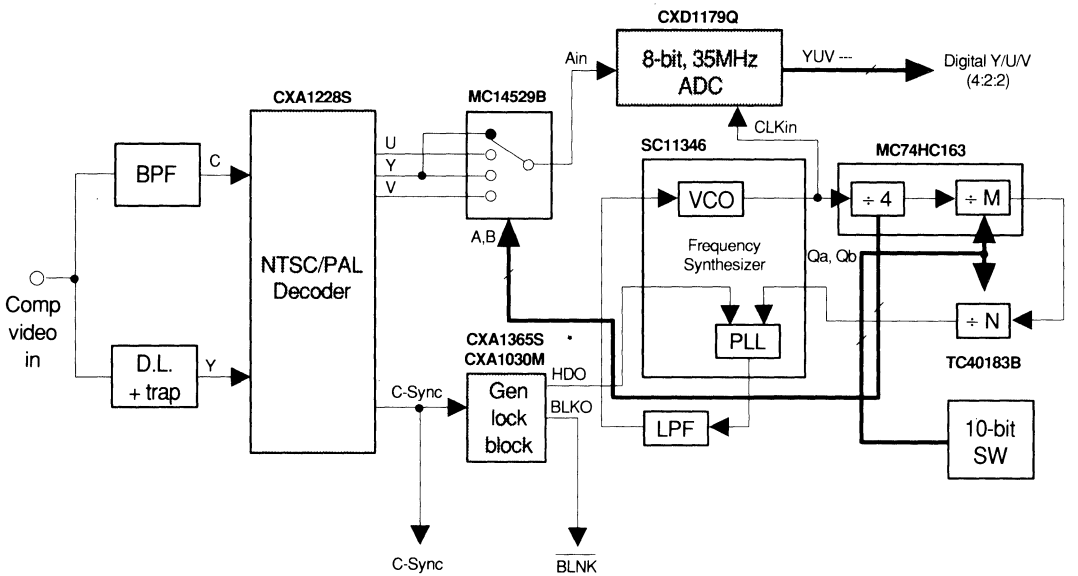
Mode / Clock freq.	NTSC		PAL	
	M	N	M	N
D1: 27 MHz	3	143	2	216
S. Pixel NTSC: 24.54MHz PAL: 29.5MHz	2	195	2	236

The circuit example is on page 6-13 (A).

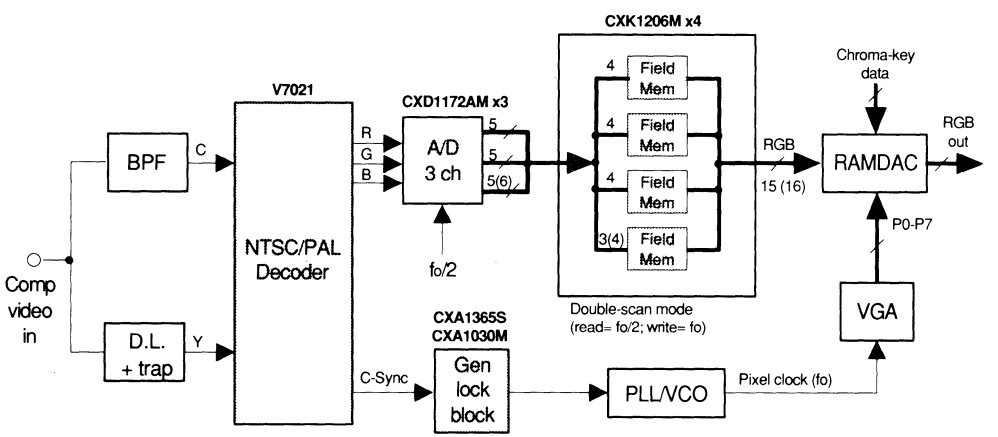
3. RGB Digital Interface for VGA.

Compared with YUV interface, each R, G, B have up to 4.5 MHz signal band width (U, V have less than 1.5 MHz band width). The 6 bit 20 MHz A/D - CXD1172AM/AP is recommended to be used. The replacement of CXD1179Q circuit can be found in the drawing on page 6-13(B).

(A). NTSC/PAL Digital Decoder with D1/Square pixel mode selection.



(B). The replacement block for RGB interface (VGA Application)



Application Note CAV08
New CD-ROM Decoder

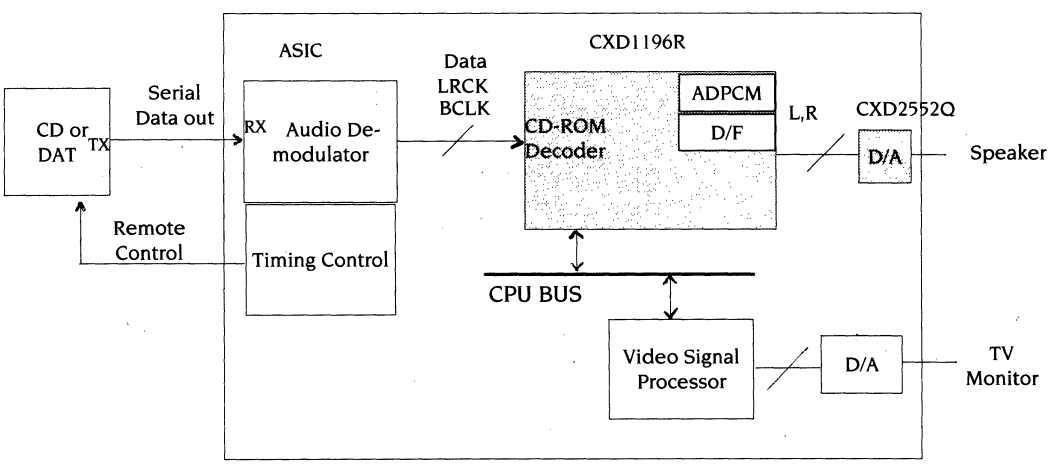
The Sony CD-ROM chip set is developed for PC, Workstation applications. On the other hand there are simple applications like computer games. They normally use the inexpensive storage device inside; however this does not use SCSI interface.

So, Sony developed the simplified version of CXD1186Q CD-ROM decoder. This new IC -CXD1196R is a CD-ROM decoder with ADPCM decoder and Digital filter for Audio out. The package is 20mil center 80pin Quad flat package. It is very small outline package.

The block diagram shown here is a proposed Computer game system; where CD or DAT are used as a storage devices outside: CD or DAT media should be developed by the customers.

CD-ROM Chip set:	CXD2500AQ	CD-DSP
	CXD1186Q	CD-ROM Decoder
	CXD1185AQ	SCSI 1 Controller

Computer Game



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Danbury	Phase I, 203/791-9042
Milford	Milgray, 203/878-5538 or 800/922-6911
Wallingford	Marshall, 203/265-3822

Florida:

Deerfield	Vantage, 305/429-1001 (Semi)
Ft. Lauderdale	Marshall, 305/977-4880
Orlando	Marshall, 407/767-8585
Tampa	Marshall, 813/573-1399
Winter Park	Milgray, 407/647-5747 or 800/432-0645

Georgia:

Atlanta	Marshall, 404/923-5750
Norcross	Milgray, 404/446-9777 or 800/241-5523

Illinois:

Chicago	Milgray, 708/202-1900
Chicago	Marshall, 708/490-0155

Indiana:

Indianapolis	Marshall, 317/297-0483

Kansas:

Kansas City	Marshall, 913/492-3121
Overland Park	Milgray, 913/236-8800

Maryland:

Columbia	Milgray, 301/621-8169 or 800/638-6656
Columbia	Vantage, 301/720-5100 (Semi)
Silver Springs	Marshall, 301/622-1118

Massachusetts:

Andover	Vantage, 508/687-3900 (Semi)
Boston	Marshall, 508/658-0810
Burlington	Western Micro, 617/273-2800 or 800/345-2921
Wilmington	Milgray, 508/657-5900

Michigan:

Livonia	Marshall, 313/525-5850

Minnesota:

Minneapolis	Marshall, 612/559-2211 or 1014

Missouri:

St. Louis	Marshall, 314/291-4650

New Jersey:

Clifton	Vantage, 201/777-4100 (Semi)
Fairfield	Marshall, 201/882-0320
Elmwood Park	Phase 1, 201/791-2990
Mt. Laurel	Marshall, 609/234-9100
Marlton	Milgray, 609/983-5010 or 800/257-7111
Marlton	Western Micro, 609/596-7775
Parsippany	Milgray, 201/335-1766

New York:

Binghamton	Marshall, 607/798-1611
Farmingdale	Milgray, 516/420-9800 or 800/MILGRAY
Long Island	Marshall, 516/273-2424
New York	Chori America, 212/563-3264 (Cameras)
N. Lindenhurst	Phase I, 516/957-4900
Rochester	Marshall, 716/235-7620
Pittsford	Milgray, 716/834-9405
Smithtown	Vantage, 516/543-2000 (Semi)

North Carolina:

Raleigh	Marshall, 919/878-9882
Raleigh	Milgray, 919/790-8094

Ohio:

Cleveland	Marshall, 216/248-1788
Cleveland	Milgray, 216/447-1520 or 800/321-0006
Columbus	Marshall, 614/891-7580
Dayton	Marshall, 513/898-4480

Oregon:

Beaverton	Western Micro, 503/629-2082
Portland	Marshall, 503/644-5050
Tigard	Daitron, 503/620-2879 (Cameras)

Pennsylvania:

Pittsburgh	Marshall, 412/788-0441

Texas:

Austin	Marshall, 512/837-1991
Dallas	Marshall, 214/233-5200
Dallas	Milgray, 214/248-1603 or 800/637-7227
Dallas	Industrial Vision, 800/627-6734 (Cameras)
Houston	Marshall, 713/895-9200
Houston	Milgray, 713/240-5360

Utah:

Salt Lake City	Marshall, 801/973-2288
Salt Lake City	Milgray, 801/261-2999

Washington:

Redmond	Western Micro, 206/881-6737
Seattle	Marshall, 206/486-5747

Wisconsin:

Milwaukee	Marshall, 414/797-8400

Canada:

Montreal	Marshall, 514/694-8142
Montreal	Milgray, 514/426-5900
Ottawa	Marshall, 800/465-6640
Ottawa	Milgray, 800/268-3315
Toronto	Marshall, 416/458-8046
Toronto	Milgray, 416/756-4481
Vancouver	Marshall, 800/465-6640

SONY

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