STANDARD
MICROSYSTEMS
CORPORATION

1988
COMPONENTS
CATALOG

1988 STANDARD MICROSYSTEMS CORPORATION
COMPONENTS CATALOG

TABLE OF CONTENTS

SECTION I
SECTION II
SECTION III
SECTION IV
SECTION V
SECTION VI
SECTION VII
SECTION VIII
SECTION IX
SECTION X
SECTION XI

PART NUMBER INDEX

FUNCTIONAL INDEX

Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A Controller	MIL-STD-1553A Manchester Interface Controller	1 MB	+5	40 DIP/ 44SMT	39-40
COM 1553B	MIL-STD-1553B Controller	MIL-STD-1553B Manchester Interface Bus Controller/Remote Terminal	1 MB	+5, −5, +12	40 DIP/ 44SMT	41-56
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	57-58
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	59-60
COM 2651	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock	1 MB	+5	28 DIP/ 28 SMT	61-62
COM 2661-1 -2 -3	USART/EPCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock	1 MB	+5	28 DIP/ 28 SMT	63-64
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	65-76
COM 52C50	TWINAX	Interface Controller for IBM System/ 34, 36, 38 designated TWINAX or 5250 environment	1 MB	+5	28 DIP/ 28 SMT	77-94
COM 7210	GPIB Interface	Intelligent Interface Controller for GPIB (IEEE-488-1978)	8 MHz	+5	40 DIP	95-106
COM 78808	OCTAL UART	8 UART's, 8 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	68 CERDIP/ PLCC	135-136
COM 78C808	OCTAL UART	CMOS Version of the COM 78808	19.2 KB	+5	68 PLCC	137-150
COM 78C804	QUAD UART (QUART)	4 UARTS, 4 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	48 DIP 44 PLCC	121-134
COM 78C802	DUAL UART (DUART)	2 UARTS, 2 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	40 DIP 44 PLCC	107-120
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 Dual 32 bit CRC Generator/Checker	2.0 MB	+5	20 DIP	151-152
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (compatible with COM 2017)	40 KB	+5	40 DIP	153-160
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion, margin	62.5 KB	+5	40 DIP	59-60
COM 81C17	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex with built-in Baud Rate Generator	100 KB	+5	20 DIP/ 20 SMT	161-168
COM 82C11	PAI	CMOS Programmable Centronics Parallel Printer Adapter Interface (PAI) with high current driving capability	1 MHz	+5	40 DIP	169-176
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	177-192
COM 82586	LANC	Ethernet Local Area Network Coprocessor for CSMA/CD Medium Access Control	10 MHz	+5	48 DIP/ 68 PLCC	193-196
COM 82C501	ESI	Ethernet Serial Interface compatible with COM 82586. Generates clocks and performs Manchester Encoding/Decoding	10 MHz	+5	20 DIP	197-200

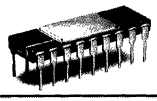
Data Communication Products CONT.

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 82C502	LANT	Ethernet Transceiver chip. Compatible with COM 82586 and COM 82C501.	10 MHz	+5, +10V	16 DIP	201-204
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (compatible with COM 2502)	40 KB	+5	40 DIP	153-160
COM 9026	LANC	Local Area Network Controller for token pass systems	2.5 MB	+5	40 DIP/ 44 SMT	205-206
COM 90C26	LANC	CMOS Version of COM 9026	2.5 MB	+5	40 DIP	207-222
COM 90C32	LANT	Local Area Network Transceiver	2.5 MB	+5	16 DIP	223-228
COM 9046	SSBSS	Single Side Band Speech Scrambler, Low Power, Full Duplex, uses 3.58 MHz TV burst crystal	NA	±2.6	14 DIP	229-232
COM 90C56[2]	ELANC	CMOS Enhanced Local Area Network Controller, with high throughput, network management and network diagnostic	5 MBps	+5	48 PLCC	233-234
COM 90C62[2]	COMBO CHIP	Complete Local Area Network Controller on a chip. Includes the combined functions of the COM 90C26 and the COM 91C32	2.5 MB	+5	40 DIP	235-238
COM 9064	IBM 3270	IBM 3270 COAX type "A" controller +5V only version of COM 9004	2.36 MB	+5	40 DIP/ 44 SMT	239-246
COM 91C32	LANT	Improved COM 90C32 LAN Transceiver, which integrates an internal crystal oscillator and reset circuitry for the COM 9026/COM 90C26.	2.5 MB	+5	16 DIP	247-252
COM 92C32[2]	LANT	This transceiver performs Manchester Encoding/Decoding to allow twisted pair operation of ARCNET. Compatible with COM90C26 and HYC9078	2.5 MB	+5	16 DIP	253-256
HYC 9058	HIT 1	High Impedance Transceiver for Local Area Networks allows BUS topology with multi drop nodes	2.5 MBps	+5	20 SIP	257-262
HYC 9068	LAND	Local Area Network Driver with (93 Ω) line matching impedance for ARCNET networks	2.5 MBps	+5	20 SIP	263-266
HYC 9078[2]	HIT 2	High Impedance Transceiver for Local Area Networks for operation at 5MHz	5 MBps	+5	20 SIP	267-268

[2]For future release

Baud Rate Generator

Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input (use 8116 for new designs)	+5, +12	18 DIP	271-272
COM 5016T[1]	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	271-272
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input (use 8126 for new designs)	+5, +12	14 DIP	273-274
COM 5026T[1]	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	273-274
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4 (use 8136 or 81C36 for new designs)	+5, +12	18 DIP	271-272
COM 5036T[1]	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	271-272
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4 (use 8146 for new designs)	+5, +12	14 DIP	273-274
COM 5046T[1]	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	273-274
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	275-276
COM 8046T[1]	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	275-276



Baud Rate Generator CONT.

Part Number	Description	Features	Power Supplies	Package	Page
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	277-278
COM 8116T[1]	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	277-278
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	279-286
COM 8126T[1]	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	279-286
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	277-278
COM 8136T[1]	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	277-278
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	279-286
COM 8146T[1]	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	279-286
COM 8156	Dual Baud Rate Generator	High-frequency clock input version of COM 8116 with additional outputs of input frequency ÷ 2 and ÷ 8	+5	18 DIP	287-290
COM 8156T[1]	Dual Baud Rate Generator	External clock input version of COM 8156	+5	18 DIP	287-290
COM 81C66[2]	Timer/Clock Generator	CMOS User Programmable Clock and Timer	+5	16 DIP	291-292
COM 81C66T[2]	Timer/Clock Generator	External Frequency Input version of COM 8166T	+5	16 DIP	291-292
COM 81C67[2]	Timer/Clock Generator	CMOS User Programmable Clock and Timer. Built-in XTAL oscillator, 2 timers	+5	8 DIP	291-292
COM 81C68[2]	Timer/Clock Generator	TTL Clock Driver Version of the COM81C67 with 3 timers	+5	8 DIP	291-292

[1]May be custom mask programmed [2]For future release

Display Products

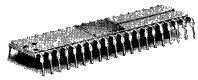
TIMING CONTROLLERS

Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	Provides all of the timing and control for interlaced and non-interlaced CRT display		Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 5037		Balanced beam interlace	Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 5047		Fixed format	80 column 24 row	4MHZ	+5, +12	40 DIP	297-298
CRT 5057		Line-lock	Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 7220A, −1, −2	Graphics Display Controller	Intelligent graphics display controller	1024 x 1024 Pixel	6, 7, 8 MHz	+5	40 DIP	299-322
CRT 9007A2, A1, A, B, C	CRT video processor and controller	Sequential or row-table driven memory programmable DMA	Programmable	A2-6.5 MHz A1-5.0 MHz A-3.7 MHz B-3.33 MHz C-2.5 MHz	+5	40 DIP	335-356
CRT 97C11	3rd generation CRT controller which allows manipulation of independent window areas on screen	Control of window size and position, window attributes, prog cursor, max of 127 windows, DRAM refresh	Up to 16K pixels vertical and 1KxN (N = display memory width) in horizontal pixels	TBD	+5	68 PLCC	433-452

TERMINAL LOGIC CONTROLLERS

Part Number	Description	Features	Display Format	Attributes	Max Clock	Power Supply	Package	Page
CRT 9028/ 9128[1]	Complete CRT video processor and controller. Display and attribute control for alphanumeric and graphics display. Two types of processor interface signals differentiate the two parts.	Separate display memory eliminates contention, smooth scroll, status row, on-board clock, and video shift register	Mask programmable, 5x8 character font, 8x12 character cell.	Tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics.	14MHz	+5	40 DIP	369-384
CRT 9053/ 9153[1]			Mask programmable, 7x11 character font, 9x13 character cell.	Embedded or tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics.	18.7MHz			401-416

[1]May be custom mask programmed



Display Products CONT.

TERMINAL LOGIC CONTROLLERS CONT.

Part Number	Description	Features	Display Format	Attributes	Max Clock	Power Supply	Package	Page
CRT92C07	Complete timing and attributes controller. Uses external character generator.	Double speed architecture and separate display memory bus eliminates memory contention. Multiple smooth scroll regions on screen.	Register programmable, maximum 12x16 character cell.	Tagged, embedded or parallel attributes: reverse video, blank, blink, underline, DH/DW, protected field, intensity.	42 MHz	+5	84 PLCC	417-420

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supplies	Package	Page
CRT 8002H	Provides complete display and attributes control for alphanumeric and graphic display. Consists of 7 x 11 x 128 character generator, video shift register latches, graphics and attributes circuits.	7x11 dot matrix, wide graphics, thin graphics, on-chip cursor	Reverse video blank blink underline strike-thru	25 MHz	+5	28 DIP	325-326
CRT 8002A[1,3]				20 MHz			323-324
CRT 8002B[1,3]				15 MHz			323-324
CRT 8002C[1,3]				10 MHz			323-324

[1]May be custom mask programmed [3]Also available as CRT8002A, B, C-001 Katakana
CRT8002A, B, C-003, -018 5 x 7 dot matrix

VIDEO ATTRIBUTES CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8021	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor	Reverse video, blank, blink underline, strike-thru	20 MHz	+5	28 DIP	327-328
CRT 9021B	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width	Reverse video, blank, blink underline, intensity	28.5 MHz	+5	28 DIP	357-368
CRT 9041A, B, C	Provides attributes and graphics control for CRT video displays. Full VT100® and VT220® compatible	Alphanumeric, wide and thin graphics, 4 cursor modes, double height/width, 12 bit shift register	Reverse video, blink, blank, underline, 4 intensity levels	A-33 MHz B-30 MHz C-28.5 MHz	+5	40 DIP	385-400

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83	8 bit wide serial cascadable single row buffer memory for CRT or printer	83 characters	+5	24 DIP	329-334
CRT 9006-135		135 characters			
CRT 9212	8 bit wide serial cascadable double row buffer memory for CRT or printer	135 characters	+5	28 DIP	421-426
CRT 94C12	8 bit wide serial, quad row buffer memory for CRT or printer	135 characters	+5	40 DIP	427-432

VT100® and VT220® are registered trademarks of Digital Equipment Corp.

Floppy Disk

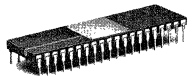
Part Number	Software Compatability	Max. Recommended Disk Data Transfer Rate	Data Separator	Power Supply	Package	Page
FDC 9268	IBM® PC/AT®, PC/XT, PS/2®	500 Kb/sec	16 MHz Digital	+5V	40 DIP, 44 PLCC	541-556
FDC 9266	IBM® PC/AT®, PC/XT, PS/2®	250 Kb/sec	8 MHz Digital	+5V	40 DIP, 44 PLCC	525-540
FDC 765A, 765A-2, 7265	IBM® PC/AT®, PC/XT, PS/2®	500 Kb/sec	external	+5V	40 DIP, 44 PLCC	455-470
FDC 72C65, 72C66	IBM® PC/AT®, PC/XT, PS/2®	Up to 1 Mb/sec	external	+5V	40 DIP, 44 PLCC	473-496
FDC 92C81	IBM® PC/AT®, PC/XT, PS/2®	Up to 1 Mb/sec	Dual Gain Analog	+5V	24 DIP, 28 PLCC	557-564
FDC 91C36/B, 92C36/B	IBM® PC/AT®, PC/XT, PS/2®	250/500 Kb/sec	16 MHz Digital	+5V	8 DIP	497-500
FDC 92C38/B	IBM® PC/AT®, PC/XT, PS/2®	250 /500/500/250 Kb/sec	16 MHz Digital	+5V	14 DIP	513-516
FDC 92C39/B/BT/T	IBM® PC/AT®, PC/XT, PS/2®	250/500/500/250 Kb/sec	16 MHz Digital	+5V	20 DIP, 28 PLCC	517-524
FDC 9229T/BT	IBM® PC/AT®, PC/XT, PS/2®	125/250 Kb/sec	8 MHz Digital	+5V	20 DIP, 28 PLCC	505-512
FDC 9216/B	IBM® PC/AT®, PC/XT, PS/2®	125/250 Kb/sec	8 MHz Digital	+5V	8 DIP	501-504
FDC 9791, 9793, 9795, 9797	179X	250 Kb/sec	external	+5V	40 DIP, 44 PLCC	565-566
FDC 1791, 1793, 1795, 1797	179X	250 Kb/sec	external	+5V, +12V	40 DIP, 44 PLC	471-472

Hard Disk

Part Number	Disk Format	Data Encoding	Max. Disk Data Transfer Rate	Hard Disk Data Separator	Power Supply	Package	Page
MSD 95C00	SCSI	RLL 2,7/MFM/NRZ/GCR	20 Mb/sec	external	+5V	68 PLCC	681-692
MSD 95C02	User Defined	RLL 2,7/MFM/NRZ/GCR	24 Mb/sec	external	+5V	68 PLCC	693-736
MSD 7262	ESDI	NRZ	18 Mb/sec	external	+5V	40 DIP	677-680
HDC 9234	IBM® PC/AT®, ST-506	MFM, FM	5 Mb/sec	external	+5V	40 DIP, 44 PLCC	637-676
HDC 92C26	ST-506	MFM, FM	5 Mb/sec	Analog, external VCO	+5V	24 DIP, 28 PLCC	627-634
HDC 9223	ST-506	MFM, FM	5 Mb/sec	VCO only	+5V	14 DIP	585-588
HDC 9224	DEC VAX®, MICROVAX®, ST-506	MFM, FM	5 Mb/sec	external	+5V	40 DIP, 44 PLCC	589-624
HDC 9227	ST-506	MFM, FM	5 Mb/sec	Analog, external VCO	+5V	28 DIP, 28 PLCC	635-636
HDC 9225	ST-506	MFM, FM	5 Mb/sec	external	+5V	48 DIP	625-626
HDC 7261	NEC ST-506	MFM, FM	12 Mb/sec	external	+5V	40 DIP	583-584
HDC 7260	NEC ST-506	MFM, FM	6 Mb/sec	external	+5V	40 DIP	579-582
HDC 1100-01, -12, -03, -05	SA1000, ST-506	NRZ, MFM, FM	5 Mb/sec	external	+5V	20 DIP	569-578

Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-9600 XX(1)	90	4	2 or N Key Rollover	-PRO -STD	Binary Sequential ASCII	+5	40 DIP/ 44 SMT	739-752
KR-9601 XX(1)	90	4	2 or N Key Rollover, caps-lock, auto-repeat	-STD -012(2)	Binary Sequential ASCII	+5	40 DIP/ 44 SMT	739-752
KR-9602 XX(1)	90	4	2 or N Key Rollover, caps-lock, auto-repeat, serial output	-STD -012(2)	Binary Sequential ASCII	+5	28 DIP/ 28 SMT	739-752



Microprocessor Products

Part Number	Description	Size	Process	Speed	Power Supplies	Package	Page
MPU800	Microprocessor	8 Bit	CMOS	2.5 MHz	5V	40 DIP	755-756
MPU800-1	Microprocessor	8 Bit	CMOS	1.0 MHz	5V	40 DIP	755-756
MPU800-4	Microprocessor	8 Bit	CMOS	4.0 MHz	5V	40 DIP	755-756
MPU810A	RAM-I/O-Timer	8 Bit	CMOS	2.5 MHz	5V	40 DIP	757-758
MPU810A-1	RAM-I/O-Timer	8 Bit	CMOS	1.0 MHz	5V	40 DIP	757-758
MPU810A-4	RAM-I/O-Timer	8 Bit	CMOS	4.0 MHz	5V	40 DIP	757-758
MPU830	ROM-I/O	8 Bit	CMOS	2.5 MHz	5V	40 DIP	759-760
MPU830-1	ROM-I/O	8 Bit	CMOS	1.0 MHz	5V	40 DIP	759-760
MPU830-4	ROM-I/O	8 Bit	CMOS	4.0 MHz	5V	40 DIP	759-760
MPU831	I/O	8 Bit	CMOS	2.5 MHz	5V	40 DIP	759-760
MPU831	I/O	8 Bit	CMOS	1.0 MHz	5V	40 DIP	759-760
MPU831-4	I/O	8 Bit	CMOS	4.0 MHz	5V	40 DIP	759-760

Shift Register

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-80, 81, 133	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls	1 MHz	+5	16 DIP	763-764
SR 5017	Quad 133 Bit	Shift Left/Shift Right, Recirculate Controls	1 MHz	+5	16 DIP	765-766
SR 5018	Quad 81 Bit					

SMC CROSS REFERENCE GUIDE–STORAGE IC'S

Description	SMC Part #	NEC	Western Digital	Siemens	Fujitsu
IBM® Compatible Floppy Disk Controller	FDC765A/B	μPD765A/B	—	—	—
Hi-Speed Floppy Disk Controller	FDC765A-2	μPD765A-2	—	—	—
Sony Microfloppy Disk Controller	FDC7265	μPD7265	—	—	—
CMOS Floppy Disk Controller	FDC72C65/B	μPD72065/B	—	—	—
CMOS Sony Microfloppy Disk Controller	FDC72C66	μPD72065	—	—	—
ESDI Disk Controller	MSD7262	μPD7262	—	—	—
ST-506 Winchester Disk Controller	HDC7261	μPD7261A	—	—	—
ST-506 Winchester Disk Controller	HDC7261B	μPD7261B	—	—	—
ST-506 Winchester/Floppy Disk Controller	HDC7260	μPD7260	—	—	—
CMOS Floppy Disk Data Separator	FDC92C36/B	—	FD9216/B	—	—
Floppy Disk Data Separator	FDC9216/B	—	FD9216/B	—	—
Floppy Disk Controller	FDC9791	—	FD1791-02	SAB-1791	MB8876
Floppy Disk Controller	FDC9793	—	FD1793-02	SAB-1793	MB8877
Floppy Disk Controller	FDC9795	—	FD1795-02	SAB-1795	—
Floppy Disk Controller	FDC9797	—	FD1797-02	SAB-1797	—
Floppy Disk Controller	FDC1791	—	FD1791-02	SAB-1791	MB8876
Floppy Disk Controller	FDC1793	—	FD1793-02	SAB-1793	MB8877
Floppy Disk Controller	FDC1795	—	FD1795-02	SAB-1795	—
Floppy Disk Controller	FDC1797	—	FD1797-02	SAB-1797	—
ST-506 Winchester Disk Controller	HDC1100-01	—	WD1100-01	—	—
ST-506 Winchester Disk Controller	HDC1100-12	—	WD1100-12	—	—
ST-506 Winchester Disk Controller	HDC1100-03	—	WD1100-03	—	—
ST-506 Winchester Disk Controller	HDC1100-05	—	WD1100-05	—	—

SMC CROSS REFERENCE

Description	SMC Part #	AMI	AMD	Fairchild	General Instrument	Harris	Intel
UART (n-Channel)**	COM8017	S6850*	—	F6850*	AY 3-1013/15	HM6402*	—
UART (n-Channel)**	COM8502	—	—	—	AY 3-1013/15	HM6403*	—
UART (n-Channel)*	COM1863	S1602*	—	—	—	—	—
Octal UART	COM78808	—	—	—	—	—	—
ASTRO	COM1671	—	—	—	—	—	—
PCI	COM2651	—	—	—	—	—	—
EPCI	COM2661	—	—	—	AY2661	—	—
USART	COM8251A	—	8251	—	—	—	8251A
Multi-Protocc USYNRT	COM5025	S6852*	—	F3846* F3856*	—	—	—
IEEE-488	COM7210	—	—	F68488* 96LS488*	—	—	8291/92*
IBM 3270 COAX I/F Circuit	COM9064	—	—	—	—	—	—
LAN Controller	COM9026	—	—	—	—	—	—
IBM Twinax Interface Controller	COM52C50	—	—	—	—	—	—
Dual Baud Rate Gen.	COM5016/36/ COM8116/36	—	—	—	AY5-8116/36	—	—
Single Baud Rate Gen.	COM5026/46/ COM8126/46	—	—	F4702*	AY5-8126	HD4702* HD6405*	—
90 Key KB Encoder	KR9600/01/02	—	—	—	AY 5-3600*	—	—
CMOS Microprocessor	MPU800	—	—	—	—	—	—
CMOS RAM-I/O-Timer	MPU810A	—	—	—	—	—	—
CMOS ROM-I/O	MPU830	—	—	—	—	—	—
CMOS Input/Output	MPU831	—	—	—	—	—	—
Ethernet Controller	COM82586	—	—	—	—	—	82586
Ethernet Serial Interface	COM82C501	—	—	—	—	—	82501
Ethernet Transceiver	COM82C502	—	—	—	—	—	82502

SMC CROSS REFERENCE

Description	SMC Part #	AMI	AMD	Fairchild	General Instrument	Harris	Intel
CRT Controller	CRT5037	—	—	—	—	—	8275
Character Generator Display Controller	CRT8002	—	—	—	—	—	—
Graphics Controller	CRT7220/ CRT7220A	—	—	—	—	—	82720
Video Processor and Controller	CRT9007	—	—	—	—	—	—
Video Attributes Controller	CRT9041	—	—	—	—	—	—
Video Terminal Logic Controller	CRT9028/9128/ CRT9053/9153	—	—	—	—	—	—

*Functional equivalent.
**Most UART'S are interchangeable; consult the factory for detailed information on interchangeability.

GUIDE–DATA COMMUNICATIONS

Motorola	National	NEC	Signetics	Solid State Scientific	DEC	Texas Instruments	Western Digital
MC6850*	NSC858*	—	—	SCR1854*	—	TMS6011*	TR1602
—	—	—	—	—	—	—	TR1983*
—	—	—	2536*	—	—	—	TR1863
—	—	—	—	—	78808	—	—
—	INS1671	—	—	—	—	—	UC1671
—	INS2651	—	2651	—	—	—	—
MC2661*	—	—	2661	—	—	—	—
—	INS8251	μPD8251A	—	—	—	—	TR1983*
2652*	6852*	—	2652	SND5025	—	—	SD1933*
MC68B488*	—	μPD7210	—	—	—	TMS9914*	WD9914*
—	DP8340/41* DP8344*	—	—	—	—	—	—
—	—	—	—	—	—	—	WD2840*
—	DP8344*	—	—	—	—	—	—
—	—	—	—	—	—	—	WD1941 WD1943/5
MC14411*	MM307*	—	—	—	—	—	—
—	MM5740*	—	—	—	—	TMS5001	—
—	NSC800	—	—	—	—	—	—
—	NSC810A	—	—	—	—	—	—
—	NSC830	—	—	—	—	—	—
—	NSC831	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—

GUIDE–DISPLAY PRODUCTS

Motorola	National	NEC	Signetics	Solid State Scientific	DEC	Texas Instruments	Western Digital
MC6845*	DP8350*	—	—	—	—	TMS9927/37	—
—	—	—	—	—	—	—	—
—	—	UPD7220 UPD7220A	—	—	—	—	—
—	—	—	SCN2674*	—	—	—	—
—	—	—	SCN2675*	—	—	—	—
—	NS455*	—	—	—	—	—	—

Innovation in Microelectronic Technology is the Key to Growth at Standard Microsystems.

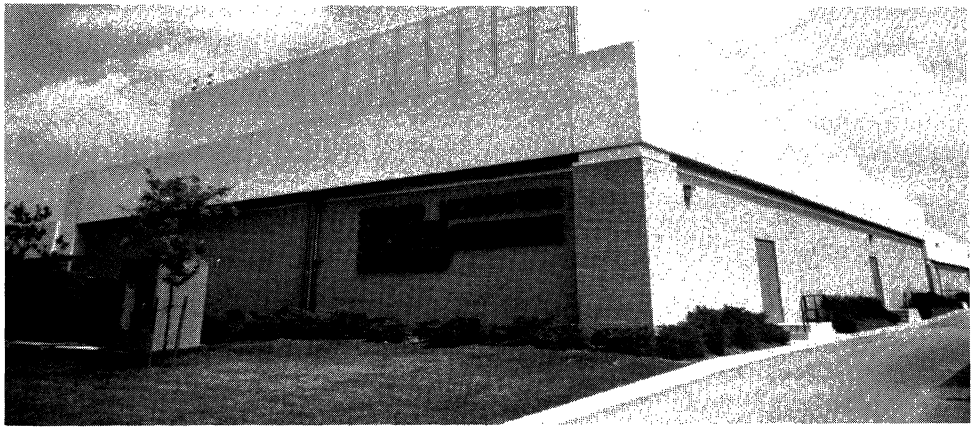
Since its inception, Standard Microsystems has been a leader in creating new technology for metal oxide semiconductor large scale integrated (MOS/LSI) and very large scale integrated (MOS/VLSI) circuits.

Standard Microsystems' COPLAMOS® silicon gate n-channel process, licensed to over 15 prominent semiconductor companies, is the de facto standard for high speed, high density integrated circuits.

COPLAMOS® utilizes a self-aligned, field-doped, locally oxidized structure to eliminate parasitic currents and shunt capacitance. This allows the tight packing of circuitry essential for VLSI, yet with performance rivaling that of bipolar technologies.

In addition, on-chip generation of substrate bias, also pioneered by Standard Microsystems, when added to the COPLAMOS® technology, results in the ability to design dense, high-speed, low-power n-channel MOS integrated circuits through the use of one external power supply voltage.

Engineering, marketing and sales personnel occupy SMC®'s 50,000 square foot facility at 300 Kennedy Drive.



This 43,000 square foot building is the center of SMC®'s research and development and wafer fabrication operations.

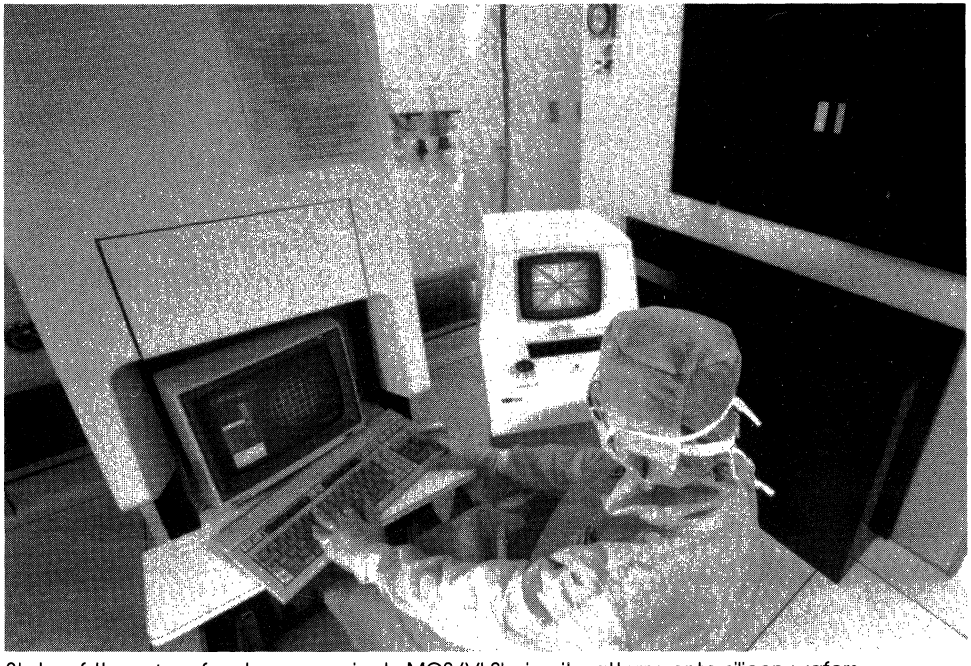
These innovations in both process and circuit technology have received widespread industry recognition. In fact, many of the world's most prominent semiconductor companies have been granted patent and patent/technology licenses covering various aspects of these technologies. The companies include Texas Instruments, IBM, General Motors, ITT, Western Electric, Hitachi, Fujitsu, National Semiconductor, Mitsubishi Electric, NEC, AT&T, Data General, Oki Electric, Gould/AMI, Sprague Electric, Toshiba, NCR and Intel.

Over the past few years, scientists and engineers at Standard Microsystems have been developing a technology to significantly reduce the sheet resistivity of the gate material used in MOS, dramatically decreasing internal time constants in MOS devices.

This technology replaces the polycrystalline silicon normally used in n-channel MOS devices with an alternate material, titanium disilicide. This has enabled Standard Microsystems to become the first semiconductor manufacturer to market and sell MOS/VLSI circuits which employ a metal silicide to replace the conventional doped polycrystalline silicon layer.

Standard Microsystems has continued its technological leadership with the introduction of new products utilizing an advanced low-power, high-speed two micron n-well CMOS process. With its 1.6 micron effective channel lengths and its double layer metal option, this process is ideally suited for standard products, standard cells and full custom designs. Another processing option which incorporates analog capacitors on the device allows for efficient, high-speed analog applications.

In CMOS circuitry, an obvious reliability concern is latch up. To avoid the problem with the two micron n-well CMOS process, Standard Microsystems' design, processing and quality engineers have worked together to create layout and processing specifications which assure latch-up-free design in accordance with the proposed JEDEC 7A specification.



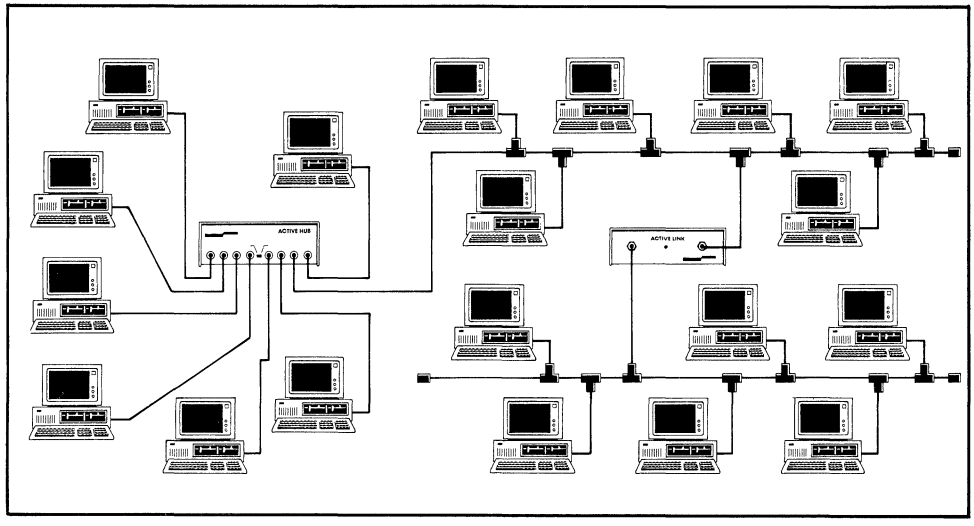
State-of-the-art wafer stepper projects MOS/VLSI circuit patterns onto silicon wafers.

We've Established a Position as the Industry Leader in Microperipherals with a Steady String of Industry "Firsts."

Standard Microsystems Corporation has made significant contributions in addressing the challenges inherently associated with connectivity: "That is the creation of a path from one computer system to another, so that information can be meaningfully exchanged between those systems."

In local area networking (LANs), SMC® was the first to introduce a single-chip local area network controller. This device (the COM9026) implements the ARCNET® LAN protocol, and is now a de facto standard. This early introduction has placed Standard Microsystems' ARCNET® products very high on the price/performance curve. Over 500,000 ARCNET® nodes are currently installed, giving this mature, reliable LAN close to a 50% market share. Standard Microsystems continues to maintain its position as premier supplier of ARCNET® LAN products. The revolutionary High Impedance Transceiver (HIT™) introduced in 1986, which enabled the implementation of a new bus topology for ARCNET® , has achieved strong market acceptance. But SMC® is far from resting on its laurels and is readying several new products to further increase ARCNET® performance while reducing its cost. These include: the COM90C62 (which integrates the COM90C26 LAN Controller and the COM90C32 LAN Transceiver) and the ELANC COM90C56 (Enhanced LAN controller that doubles the data bit rate and offers, among other features, LAN Management and LAN Diagnostics).

As a result of the second source agreement recently signed with Intel Corp., SMC® will also be able to offer the chip set required to implement Ethernet™ Local Area Networks. The chip set will include the industry standard COM82586 LANC as well as the COM82C501 transceiver and the COM82C502 serial interface chip. Standard Microsystems Corporation thus becomes the only supplier of components for the two LAN implementations with the largest installed market base.



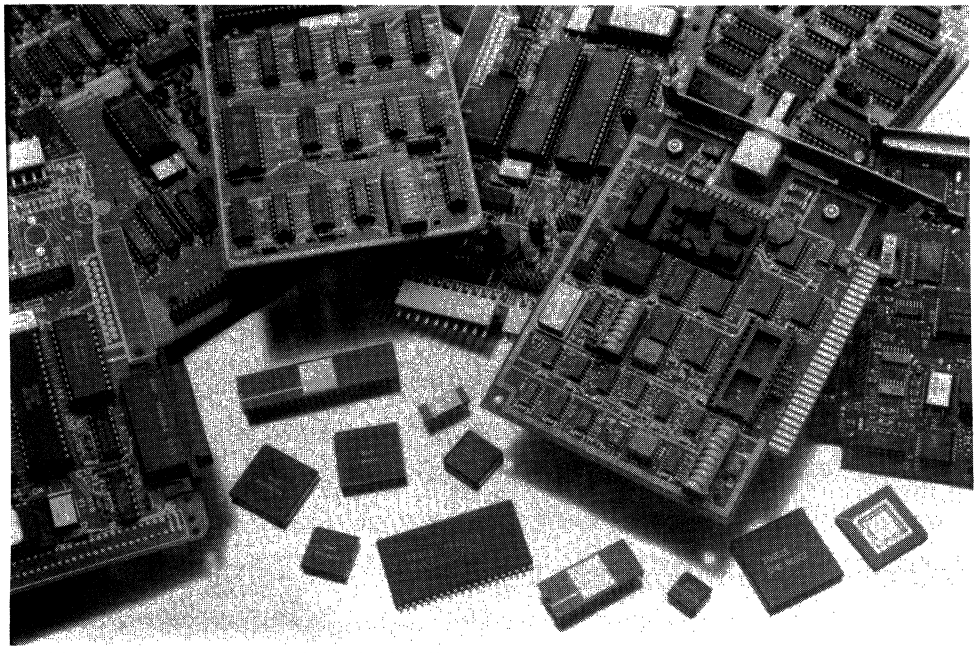
SMC® 's ARCNET® LAN supports a star topology, bus topology or combination of both.

Standard Microsystems Corporation is also at the forefront of the micro-to-mainframe connectivity in an IBM® environment. No matter which IBM® mainframe connection is considered, the IBM® 3270 or IBM® System/3X, SMC® interface devices are the most cost-effective design approach available in the market. SMC® was first to introduce 3270 COAX and 5250 TWINAX interface devices. The COM9064 and COM52C50 are unique single-chip solutions that enable PC, terminal and printer manufacturers to provide communication links within the IBM® mainframe environment at reasonable cost.

Standard Microsystems Corporation, known worldwide for many industry firsts in the field of UARTs, is continuing its tradition with the introduction of two new products that will definitely change the design implementation of asynchronous data communications. The COM81C17, the only 20-pin CMOS UART in the market, has a size which is overshadowed only by its speed. The COM81C17 features a 100K bits-per-second transfer rate–a far cry from the usual 19.2 Kbits per second offered by most UARTs currently available.

However, it is our new family of multiple UARTs, designated COM78C80X, that will bring the asynchronous data communication market to new heights. These VLSI devices, which integrate 2, 4 or 8 complete channel interfaces in one chip, revolutionize the distribution of data communication.

In another area, CRT display systems have traditionally required a great deal of support circuitry for the complex timing, refresh and control functions. This need led the engineers at SMC® to develop the CRT5027 VTAC, the first CRT controller to provide all of these functions on a single chip. A second generation CRT controller, the CRT9007 VPAC was then introduced, and became an industry standard when it was designed into the DEC VT220 terminal. The CRT9007 is the heart of a complete high performance CRT controller family, which includes single, double and quad row buffers, and a variety of video attribute controllers. Various elements of the VPAC family



SMC®'s chip and board-level products offer definite space, cost and performance advantages in a wide range of applications.

can be selected to provide the optimal video control solution from low-end to high-end systems.

For lower cost designs, a family of single-chip solutions exists which integrates the entire timing, video and attribute control functions on a single VLSI circuit. Two of the devices in this family are the CRT9028/9128 VTLC and the CRT9053/9153 EVTLC which are mask programmable and, by also including the character generator on the chip, provide the lowest cost solution. The latest edition to this single-chip family is the CRT92C07 ATLC (Advanced Terminal Logic Controller) which is fully register programmable and supports all the features of higher performance terminals, including the ability to emulate the DEC VT100 and VT220 environments. A complete terminal can be built using these devices with just the inclusion of a RAM and microprocessor.

One of the most popular features appearing in PC and terminal display interfaces is the capability of windowing. This feature is now supported by a third generation CRT controller, the CRT97C11 VIEW (Video Engine for Windows). This device is capable of generating up to 127 hardware windows on screen and provides the ability to pan images behind windows in real time. The overhead associated with the management of windows on-screen is highly simplified when compared to software techniques.

Standard Microsystems Corporation has also spearheaded many developments in the areas of disk controllers and data separators for both Winchester and floppy disks. SMC® offers more industry standard floppy disk ICs than any other source. These include the FDC765A controller, the CMOS FDC72C65 and the FDC9216, FDC9229 and FDC9239 series of data separators.

Only SMC® offers the licensed industry standard FDC765A and a patented high resolution digital data separator in a single IC. Called FDC9268, this single chip offers designers of personal home computers the lowest cost floppy disk controller possible.

Extracting the actual stored data and clock signals from the distorted and jittery signal provided by a disk drive, has historically required a trade off between data integrity and the need to use additional off-chip analog components which sometimes required production line adjustments. However, SMC® 's advanced Digital Floppy Disk Data Separators with built-in write precompensation (like the one in the FDC9268) assure reliable data transfers to and from disk, even when reading and writing high density floppy disk on different disk drives.

SMC® also offers the most advanced self-tuning Analog Floppy Disk Data Separator for the ultimate in data integrity. The FDC92C81 CMOS Dual Gain Analog Floppy Disk Data Separator adjusts its gain automatically when attempting to lock to data, guaranteeing both optimal bit shift tolerance and quick locking to data. This results in the greatest tolerance to bit shift in the industry for IBM® PC/AT® compatible environments. These advances in data separator technology should come as no surprise from the company that invented the present-day digital data separator.

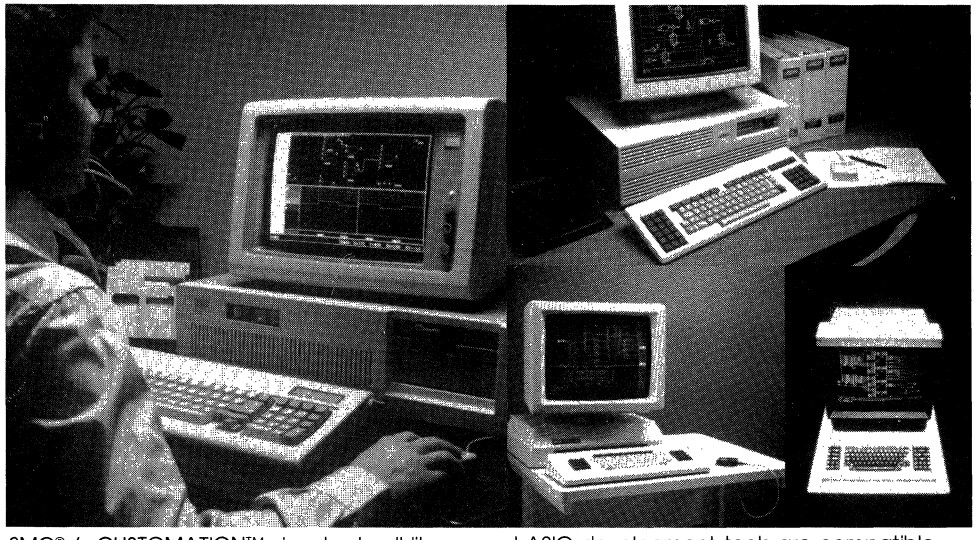
IBM® compatible hard disk controllers can be designed at a very low cost using SMC® 's HDC9234 Winchester Controller IC. Used with the HDC92C26 Hard Disk Data Separator and the HDC9223 VCO, the HDC9234 may be used on the motherboard of an AT® or XT™ type personal computer or on a separate controller card. Combined with the HDC9234, the FDC9268 Floppy Disk Controller adds floppy disk and tape backup capability to the controller card.

For space-conscious designs requiring a single controller for both Winchester and floppy disks, the HDC9224 is ideal. When used with the HDC9227, which performs data separation on data from both Winchester and floppy disks, and with the HDC9223 VCO, the HDC9224 provides a truly optimal multi-media controller for Winchester, floppy and tape drives.

An embedded SCSI (Small Computer System Interface) disk drive, that sustains a continuous 20 M bits per second disk transfer rate simultaneously across both the SCSI bus and the media, is possible when the disk controller is SMC®'s MSD95CO2 and the SCSI bus controller is SMC®'s MSD95COO. Individual data busses for processor, disk, and SCSI information allow 5 Mbyte per second SCSI bus transfers to continue uninterrupted by processor bus accesses. Zero latency reads, multiple sector read look-ahead, fully programmable disk format and error correction on-the-fly all contribute to saving disk revolutions and decreasing the disk access time. The MSD95CO2 handles GCR formatted tape as well, and can also be used in non-SCSI applications.

SMC®'s MSD95CO2 VLSI Storage Controller is built from a set of highly advanced dedicated SuperCells™. Each SuperCell™ performs a specialized function (e.g., DMA, Microsequencer, disk encoder/decoder, microprocessor interface, or error correction). By modifying a particular SuperCell™, or by substituting a user defined cell, it is possible to build a peripheral controller for specialized applications with minimum modification. This technique results in an optimal solution for each application and offers the advantage of allowing design engineers to build in special features necessary for product differentiation.

Standard Microsystems' long list of successes in the microperipheral area has, in many cases, allowed us to satisfy specific customer requirements by modifying our standard products offerings accordingly. As illustrated in our modular design approach to the MSD95CO2, SMC® has gone a step beyond the Standard Cell by defining and building Standard Products made up of SuperCells™. These SuperCells™, which are highly complex pieces of logic in their own right, can provide the customer with a set of high level building blocks which have been defined specifically for end-user applications.



SMC® 's CUSTOMATION™ standard cell library and ASIC development tools are compatible with virtually all industry-standard workstations.

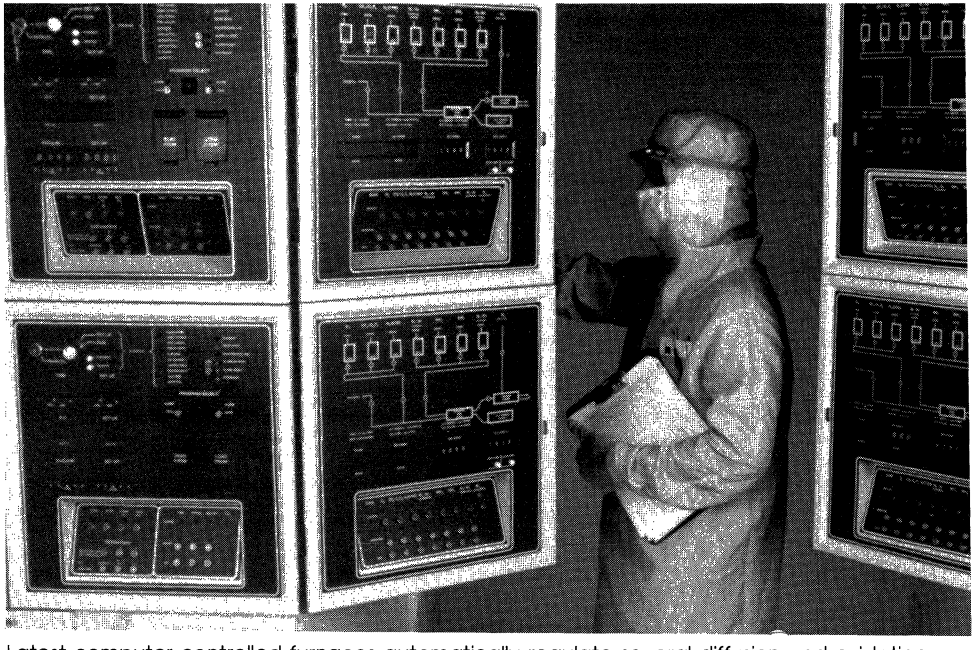
These cells may be combined with other SuperCells™, or user defined logic, resulting in fast turnaround, highly area efficient ASIC circuits. This approach offers the customer system level tools to which he can relate. It is now possible for Standard Microsystems Corporation to tailor our systems expertise, acquired over years of designing and fabricating standard microperipherals, to the customer's specific needs to add that additional measure of assurance that the best possible solution is attained.

Improvements in Processing and Manufacturing Keep Pace with Advances in Semiconductors.

With the phenomenal growth of the electronics industry, processing innovations are critical. But, if the products are to perform as designed, they also have to be reliable.

At Standard Microsystems Corporation, we make every effort to ensure the highest degree of quality and reliability in our products. Consequently, "state-of-the-art" applies not only to our products, but to the manufacturing processes as well.

Self-aligned, fully ion-implanted, short channel NMOS, p-well CMOS and n-well CMOS technologies require the most modern wafer fabrication equipment and facilities. Consequently, Standard Microsystems has continued to upgrade its wafer fabrication facility with the latest state-of-the-art technologies. Requirements for better incoming raw material quality control have necessitated the purchase of the latest KLA and Leitz inspection systems. The correct tolerances are achieved with the use of Perkin Elmer's scanning projection printers, ASET's 5X reduction steppers, and Tegal's



Latest computer-controlled furnaces automatically regulate several diffusion and oxidation processes simultaneously.

plasma etching systems. Improvements in the clean room atmosphere of Standard Microsystems Corporation's wafer fabrication facility and in the gas distribution system have been achieved.

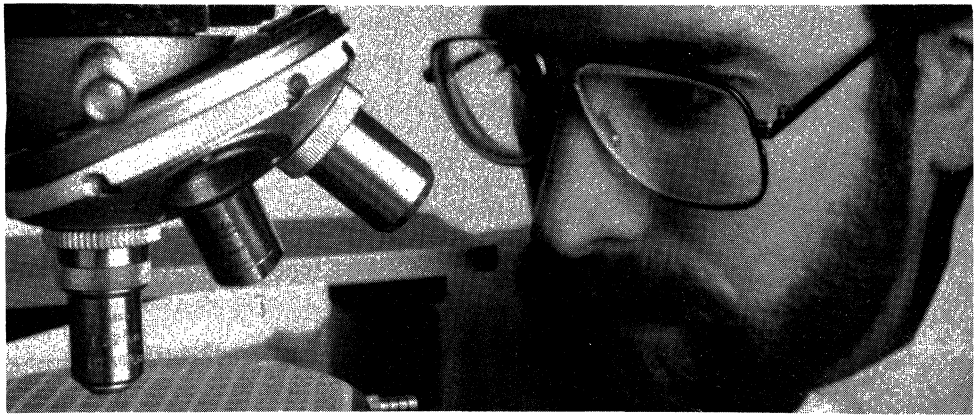
SMC® 's commitment to excellence is further demonstrated in the use of the latest Sentry, Gen Rad and Megatest test equipment. Our components tests are derived from extensive logic simulations which ensure maximum fault coverage on each circuit. These simulations are run on our variety of in-house workstations as well as our VAX 11/785 computer cluster system. This service capability allows us to make full use of the technologies we develop. We can produce any quantity of semiconductors customers require. What's more, we can provide our customers with the fast delivery times that they demand in today's increasingly competitive environment.

Throughout its history, Standard Microsystems Corporation has been at the forefront in the design, development and manufacturing of highly complex integrated circuits for the computer, microperipheral and data communications fields. Breakthrough technologies such as those previously outlined have certainly contributed to our success, but even more important is our ability to satisfy our customers.

Quality is our bottom line and the responsibility of each and every employee at SMC® . We are constantly striving to make sure that our products' performance meets your highest expectations. Our unprecedented growth over the last decade is proof that we're doing the job.

With five modern buildings on Long Island alone, including state-of-the-art design, test and wafer fabrication facilities, we have the people, resources and dedication to fill your design needs quickly, at competitive prices and with the highest degree of reliability.

Design the name Standard Microsystems Corporation into your next project. Our leading edge could provide just the competitive edge you need when you take your product to market.



The laser cutter in SMC®'s Special Analysis Laboratory helps isolate small sections of complex circuitry for investigation.

Your Semicustom Design Partner.

When your need is ASIC (application specific integrated circuit), the right semicustom partner is extremely important. The success of your company's program is dependent upon selecting the ASIC vendor who can give you the service, technology, flexibility and stability that you need.

Standard Microsystems is that company.

Standard Microsystems has been designing and building custom and semicustom integrated circuits for major corporations worldwide since 1971. Circuits designed by Standard Microsystems are used all over the world: in computers and computer peripheral equipment, data communications, telecommunications, over-the-air and cable TV systems, business machines, avionics and a wide range of consumer products.

Our experience has taught us that success in the ASIC marketplace demands a strong orientation towards advanced technology and, just as important, quick cost-effective response to our customers' special needs.

As a company committed to serving the ASIC marketplace, Standard Microsystems has all of the essential resources: a top-flight staff, state-of-the-art CAD, CAE and manufacturing equipment as well as tried and proven procedures and software. We can help you define and specify all of your ASIC needs, then design, fabricate, package, and test the circuits which your company requires.

Our semicustom design system combines the technological advantages of full custom with rapid turnaround, low cost and virtually guaranteed first-time success.

Our system, CUSTOMATION™, combines a large, proven and versatile family of standard cells with a powerful set of procedures and software that we call STANSURE™.

Unlike gate array approaches, CUSTOMATION™ provides an optimized design with little waste, and guaranteed performance. Yet CUSTOMATION™ offers turnaround and ease of design that rivals the best gate arrays. In addition, CUSTOMATION™ combines digital and analog building blocks with macrocells and SuperCells™ for microprocessor, micro-peripheral equipment, memory and other applications.

Standard Microsystems has been at the forefront of semiconductor technology since our inception. We pioneered the micro-peripheral market with innovative standard products and leading-edge custom products. We've also developed and licensed many of the world's most advanced semiconductor process technologies. CUSTOMATION™ epitomizes our forward thinking and strong service orientation.

The CUSTOMATION™ Design System.

SMC®'s Leading-edge ASIC Technology and Microperipheral SuperCells™ Combine to Make Your Competitive-edge Circuits.

With CUSTOMATION™ you can invent the semicustom circuits you need without reinventing the wheel. Everything Standard Microsystems has learned in over a decade of developing innovative standard products and high-performance ASICs is at your disposal.

Your Place or Ours.

The real beauty of our system is that it puts you in total control of your design. You work at your own pace—at your own facility, if you wish—verifying logic through simulation every step of the way.

This hands-on involvement can help reduce production costs, speed up turnaround and virtually guarantee that first silicon is working silicon.

Standard Microsystems will provide everything you need to perform the entire design function, including a turnkey workstation complete with our cell library and "industry-standard" software, formal classroom training on how to use the CUSTOMATION™ design system and ongoing technical support.

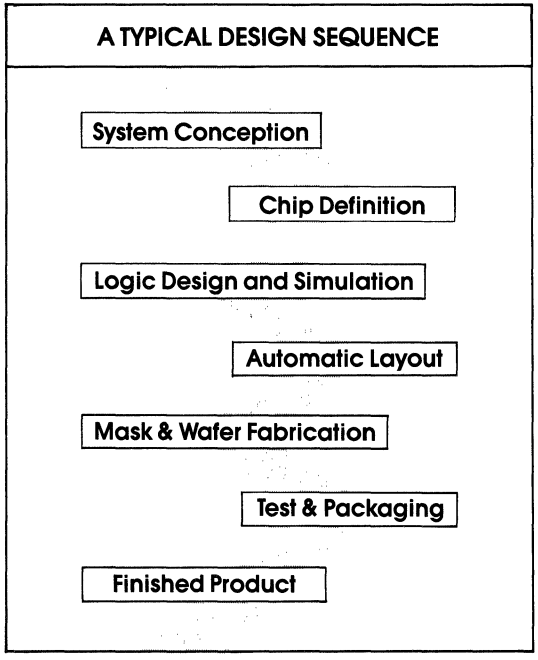
Once you are totally satisfied with your design, we will then use your netlist database for automatic placement and routing, carrying the process through masks, wafers and prototypes.

Or, if you prefer, we can do the full job, handling everything for you from start to finish. At your request, we can do the job at Standard Microsystems' Hauppauge design and manufacturing facility or at any of our worldwide network of design centers.

A Typical Design Sequence.

A CUSTOMATION™ design sequence typically involves the use of a progression of software design tools, with the output of one serving as the input for the next. (See flow chart.)

Although the designer is constantly monitoring this process, he is not actually "in line." Therefore, problems due to human error are almost completely eliminated, virtually assuring first-time success.



Process Technology You Can Count On.

The cornerstones of the CUSTOMATION™ technologies are our production-proven 1.6, 2 and 3 micron, silicon-gate CMOS processes that are compatible with the design rules of several other major semiconductor manufacturers.

A Library of Best-sellers.

There are hundreds of cells in the CUSTOMATION™ cell library, including a complete array of 74LS SSI and MSI logic functions, and a large and growing number of analog cells, macrocells and SuperCells™. The design system stores the cell layouts, logical models and performance characteristics of each cell in its database.

Because most of our standard cells emulate 74LS logic functions, many of your design engineers should already be familiar with them.

We are always prepared to develop new cells to meet your specific requirements. For digital applications this might include special counter cells or special I/O buffers. Analog applications often require customized cells for your particular requirements.

SuperCells™:

UART Tool-Kit
UART Building Cell-Set

Manchester SuperCell™
Encoder/Decoder

RTC SuperCell™
Real Time Clock

PC-KBRD SuperCell™
PC Keyboard Interface Controller

SCSI SuperCell™
SCSI Interface Controller

IBM® 5250 TWINAX
5250 Interface Controller

8250 SuperCell™
UART

8259 SuperCell™
Programmable Interrupt Controller

8254 SuperCell™
Programmable Interval Timer

6845 SuperCell™
CRT Controller

8237 SuperCell™
DMA Controller

TIMER SuperCell™
Master Timer

FDDS SuperCell™
Data Separator

65CX02 SuperCell™
65C02 Core Microprocessor

RAM SuperCell™
Modular RAM (512 bits/block)

ROM SuperCell™
Modular ROM (512 bits/block)

VCO SuperCell™
Voltage Controller Oscillator

555 SuperCell™
555 Timer

DTMF SuperCell™
DTMF Tone Generator

ATOD SuperCell™
8-Bit Analog to Digital Converter

You can feel totally confident about the performance of the CUSTOMATION™ cells, too. They are thoroughly characterized and have been used successfully in numerous applications. Before a cell can be added to our library, it is completely modeled, characterized, tested and "certified."

Standard Microsystems is also dedicated to incorporating more micro-peripheral SuperCells™ into the library. These currently encompass such functions as ROMs, RAMs, UART "Tool-Set," 8250, 8259 BRG, Manchester Encoder/Decoder, 555 RC Oscillator, Real time clock, DTMF encoder, RLL decoder, SCSI interface, floppy disk digital data separator, counter/timer, and A to D converter.

CUSTOMATION™ CELL LIBRARY PERFORMANCE

Voltage: 3V to 10V

Temperature: -55°C to + 125°C

Speed: DC to 50 MHZ

Process: 2μ DLM & 3μ SLM CMOS SIGATE

I/O: TTL & CMOS Compatible

Fanout: Capacitive Loading Restricted Only

Delay: <1.1 NSEC Typical

In addition to the customized layout of cells, we've also helped pioneer the use of "soft-macrocells," which are the implementation of large logic blocks through the stored interconnection of more basic "core cells."

By using standardized core cells and "soft-macrocells," digital designs presently fabricated in one technology are easily portable to next-generation processes. This means your design will never become dated or obsolete.

Industry-standard Software.

CUSTOMATION™ utilizes software that provides a well-proven package of design aids which your engineers will be comfortable using. If you wish, the entire package can be licensed through Standard Microsystems.

We think you'll find our software to be comprehensive, easy to use and incredibly powerful. Netlists developed on any workstations supported by Standard Microsystems can be transported quickly and easily to any other. Logic can also be simulated on any workstation.

Our software is designed to virtually guarantee that your chip will work the first time, every time. We not only provide schematic capture, but logic simulation, timing analysis and automatic test program generation as well.

Ongoing Technical Support.

As a CUSTOMATION™ user, you'll receive continuing technical support from Standard Microsystems. Our applications engineers are seasoned professionals who can provide prompt, expert assistance from our home office or regional sales offices. One such applications engineer will be personally assigned to your program to assist you with any problems that may arise during the actual course of development.

Standard Microsystems has a particularly strong applications expertise in data communications, video displays, disk controllers and small computer peripherals. Over the course of our history, we've introduced a number of breakthroughs in the CRT, floppy disk, hard disk and data communications areas.

Fast Turnaround.

Nowhere is the adage, "time is money", more applicable than in semicustom design. The faster you develop your ASICs, the faster you can get your products to market. In today's fast paced, highly competitive electronics industry, that can mean the difference between success and failure.

With CUSTOMATION,™ we can usually supply working prototypes within eight weeks of receipt of your signed-off netlist. Of course, design time and logic simulation is dependent on how fast you work.

With an experienced designer using CUSTOMATION,™ front-end design should take approximately 12 weeks. (Both design and prototype development cycles are based on a 3000-gate equivalent chip design.)

Firm Pricing.

Standard Microsystems will calculate and commit to both a development cost and a production price for your CUSTOMATION™ chip based on your design specifications. So you will know your exact production costs *before* you undertake the design. Furthermore, you will never pay for computer time or any other "uncapped" charge.

Unit cost, of course, depends on a variety of factors: gate count, complexity of interconnect, package cost and performance requirements. A CUSTOMATION™ design, however, almost always results in a smaller die size than a comparable gate array design.

Our cell library also includes RAM, ROM, Microprocessor, UART and many other SuperCells,™ as well as analog functions that are not available on gate arrays. This can lower prices when you get into volume production. Your system will have fewer ICs compared to MSI, gate array or microprocessor-based designs, resulting in lower assembly costs, lower power consumption and enhanced reliability.

WHY STANDARD CELL?

Standard Cell vs. Full Custom vs. Gate Array

Design Method	NRE	Design Cycle	Unit Cost Ratio	Min Qty/Yr
Gate Array	$9K-$20K	6-15 Wks	1.20	0.5K-45K
Standard Cell	$12-$25K	8-15 Wks	1.00	5K-10K
Full Custom	$80K-$125K	6-18 Mths	0.80	100K

Guaranteed Success.

With CUSTOMATION,™ you're virtually guaranteed first-time success. We've designed our system for outstanding accuracy with a number of strategic checkpoints to find and eliminate problems before your circuit is fabricated.

We also offer the following guarantee: *Standard Microsystems will bear the cost of any design iteration that is required as a result of any error in cells, utilities and design tools comprising the CUSTOMATION™ system.*

TRAINING OUTLINE

DAY 1 OVERVIEW
- Introduction and Goals
- Workstation Operating System
- Workstation Familiarity
- Workstation Laboratory

DAY 2 SCHEMATIC ENTRY
- Cell Library
- Schematic Entry
- Design for Ease of Test
- Schematic Entry Laboratory

DAY 3 SIMULATION
- Stimulus File Generation
- STANSURE™
- Tester Considerations
- Simulations Laboratory I

DAY 4 SIMULATION
- Test Vector Extraction
- Advanced Simulation Language
- Fault Analysis
- Simulation Laboratory II

DAY 5 REVIEW
- Review of Procedures
- Review of Results

Comprehensive Training.

If you elect to design your own ICs, Standard Microsystems can quickly teach you to create cell-based circuits using CUSTOMATION™ whether you've had previous semicustom design experience or not.

At our plant in suburban New York, conveniently located just 8 miles from Long Island's MacArthur Airport, we conduct classes for all skill levels, tailoring our instruction to your particular needs and experience level. We cover all phases of design, and you'll work on an actual CUSTOMATION™ workstation to get hands-on experience and sharpen your design technique.

Your instructors are Standard Microsystems' engineers who are not only experts in IC design, but have a wealth of experience working with customers to meet their custom and peripheral controller needs.

We'll also assign a staff engineer who will personally oversee your progress and provide valuable insights that will ensure your design success. You'll complete our training session poised, confident and ready to produce useable designs utilizing CUSTOMATION.™

A Total Commitment.

In addition to the many capabilities already touched on, Standard Microsystems offers many others that clearly indicate our technical prowess and commitment to the custom/semi-custom marketplace.

For example, we provide MIL-STD-883B screening. We have the ability to test circuits up to 40 MHz using our GenRad™ and Sentry® testers.

We not only offer the industry-standard Dual-In-Line Package (DIP), but can provide J-Leaded chip carriers (28 to 84 pins) in both plastic and ceramic. We can also supply pin-grid arrays for higher pin count requirements.

Standard Microsystems also has been actively involved in the development of a true "Silicon Compiler." Most so-called compilers are actually silicon "assemblers" which simply optimize the layouts of existing designs. At Standard Microsystems, however, we are using systems to compile the actual circuit design, not just the layout.

We input circuit requirements to our compiler in the form of equations or algorithms which reflect the actual logical and arithmetic functions. The compiler then outputs a completely minimized circuit netlist using our standard cell functions.

Outstanding Checks and Balances.

The heart of the CUSTOMATION™ design system, STANSURE™, is a system of interrelated procedures, programs and data files that convert your input data into a working integrated circuit. The STANSURE™ system is designed to maximize the probability that all circuits designed using the CUSTOMATION™ cell library will be "first time" successes.

STANSURE™ provides not only schematic capture, but logic simulation, timing analysis, fault coverage, automatic test program generation and automated breadboarding.

The **STANSURE™ system of procedures consists of the following elements:**

STANNET™: the STANNET™ family of programs works with the workstation based schematic capture tools to convert the resulting netlists into a common database format and verifies the results. Also included in the STANNET™ family are the STANROM™ and STANRAM™ ROM and RAM memory generators.

STANSIM™: provides logic simulation, interfaces between the workstations and back annotation.

STANTIME™: timing verification programs calculate and display the propagation delays (rise and fall times) of each circuit element. The STANTIME™ programs may be run before and after layout. They will also calculate the cumulative propagation delays of each path on the design.

STANCOMP™: provides the chip layout and design rule checking functions. Further, it provides the capability of checking the netlist extracted from the layout with the logical netlist to assure the correctness of the layout data.

STANWIRE™: produces a wirewrap breadboard from the logical netlist of any circuit designed using the 74LS family of CUSTOMATION™ cells.

STANTEST™: produces Sentry® or GenRad™ compatible test files from the simulation vectors.

The **STANFAULT™** system of fault grading ensures that your simulation will completely check the logic. The test program is then automatically generated from the proven simulation files. This ensures that your custom design will be adequate for tomorrow's demanding quality standards.

A Complete Turnkey Workstation.

Standard Microsystems offers a complete set of design tools, everything you need to develop your circuit from start to finish without ever leaving your facility. Our tools combine high performance and user-friendly operation. What's more, our standard cell library and circuit development tools are currently compatible with virtually all industry-standard workstations, including the IBM® PC (no hardware modification required with the VIEWlogic® Workview™ software), Daisy™, Mentor Graphics™ Valid™ Logic, and VAX.® (Note: VAX® hardware is supported through the use of IBM® PC/compatible-based VIEWlogic™ graphic front-end systems.)

If one of these workstations is not your preferred model, check with Standard Microsystems. We are constantly enhancing our software to support other workstations and mainframes.

Each CUSTOMATION™ design system includes:

- **Symbols and Schematics**
  For Standard Microsystems' advanced standard cell library.
- **Circuit Simulation**
  Detailed and proven simulation models for each supported workstation.
- **Timing Analysis Package**
  A supplement to workstation capabilities which performs detailed analysis of propagation delays for each circuit path and node throughout the design.
- **Automated Test Program Extraction**
  Standard Microsystems' software rapidly compiles IC test program files based on simulation data.
- **Complete "How To" Documentation**
  Design and Simulation Instruction Manual dedicated to your specific workstation.

If you like, we'll even install the CUSTOMATION™ cell library and software on your workstation, at your facility.

The Right Company For the Job.

Standard Microsystems is the right sized company for all of your ASIC needs. With five modern buildings housing 250,000 sq. ft. on our 30-acre Long Island, N.Y. site, we have the resources, including state-of-the-art wafer fabrication, assembly, design and test, to bring your program in on time, within budget and with remarkable results.

Yet we aren't too large. We can work with you in the way that *you* desire, to provide the results that you need.

Our 16 years of ASIC experience has taught us that service, support and communications are the keys to successful ASIC development. So, we open a direct pipeline to you and keep it open throughout the entire development and production program.

We've established an environment that stimulates creativity while encouraging adherence to pragmatic objectives. Our intensive research and development efforts have resulted in over 30 patents, and a list of licensees that is virtually a "who's who" of the semiconductor industry.

We monitor each project very carefully. Strict scheduling via program management and frequent customer contact has become the hallmark of our CUSTOMATION™ program.

Just as important, we have a track record of success. Numerous testimonials from satisfied customers are proof of our ability to perform. Quite simply, we make no promises we can't keep.

For more information or to get started with CUSTOMATION™, call your nearest Standard Microsystems regional office. Or contact Standard Microsystems Corporation, Custom Marketing Department, 35 Marcus Boulevard, Hauppauge, NY 11788. (516) 273-3100.

SMC® CUSTOMATION™ STANDARD CELL LIBRARY

LOGIC GATE CELLS

CELL NAME	DESCRIPTION
LS00	2-Input NAND Gate
LS02	2-Input NOR Gate
LS04	Inverter
LS08	2-Input AND Gate
LS10	3-Input NAND Gate
LS11	3-Input AND Gate
LS20	4-Input NAND Gate
LS21	4-Input AND Gate
LS25	4-Input NOR Gate with Strobe
LS27	3-Input NOR Gate
LS28	2-Input NOR Gate with Buffer
LS30	8-Input NAND Gate
LS32	2-Input OR Gate
LS37	2-Input NAND Gate with Buffer
LS40	4-Input NAND Gate with Buffer
LS51A	2-Wide, 2-Input AND-OR-Invert Gate
LS51B	2-Wide, 3-Input AND-OR-Invert Gate
LS54	4-Wide, 2-Input & 3-Input AND-OR-Invert Gate
LS55	2-Wide, 4-Input AND-OR-Invert Gate
LS64	4-2-3-2 Input AND-OR-Invert Gate
LS86	2-Input Exclusive OR (XOR) Gate
LS133	13-Input NAND Gate
LS134	12-Input NAND Gate with 3-State Output
LS260	5-Input NOR Gate
LS266	2-Input Exclusive NOR (XNOR) Gate

BUFFER CELLS

LS125	Non-Inverting 3-State Buffer
LS126	Non-Inverting 3-State Buffer
LS240	Inverting 3-State Buffer
LS242	Inverting Transceiver
LS243	Non-Inverting Transceiver
LS244	Non-Inverting 3-State Buffer
LS245	Octal Non-Inverting Transceiver
LS265A	1-Input, Dual Complimentary Output Gate
LS265B	2-Input AND Gate w/Complimentary Dual Output
LS365	Hex Non-Inverting 3-State Buffer
LS366	Hex Inverting 3-State Buffer
LS367	Quad Non-Inverting 3-State Buffer
LS368	Quad Inverting 3-State Buffer

SHIFT REGISTER CELLS

LS95	4-Bit Parallel I/O, Serial Input Left/Right SR
LS164	8-Bit Parallel Output, Serial Input SR w/Clear
LS166	8-Bit Parallel/Serial Input, Serial Output SR Clear
LS178	4-Bit Universal Shift Register
LS179	4-Bit Universal SR with Async. Clear
LS194	4-Bit Bidirectional Universal SR w/Clear
LS195	4-Bit Parallel Input/Output SR w/Clear
LS198	8-Bit Bidirectional Universal SR w/Clear
LS295	4-Bit Universal Shift Register
LS395	4-Bit Universal SR w/Async. Clear, 3-State Outputs

FLIP-FLOP CELLS

LS73	J-K Flip Flop with Clear
LS74A	D Flip Flop with Set & Reset
LS76A	J-K Flip Flop
LS174	Hex D Flip-Flop with Direct Clear
LS175	Quad D Flip-Flop with Direct Clear
LS374	Octal D Flip-Flop with 3-State Output
LS377	Octal D Flip-Flop

LATCH CELLS

LS75	Dual Transparent Latch
LS77	Dual Transparent Latch
LS100	Quad Transparent Latch
LS116	Quad Transparent Latch with Clear
LS375	Dual Transparent Latch

MULTIPLEXER/SELECTOR CELLS

LS151	8:1 Multiplexer with Strobe
LS152	8:1 Multiplexer, Inverting
LS153	4:1 Multiplexer
LS157	Quad 2:1 Multiplexer
LS158	Quad 2:1 Multiplexer, Inverting
LS253	4:1 Multiplexer, 3-State Output
LS352	4:1 Multiplexer, Inverting
LS353	4:1 Multiplexer, 3-State, Inverting
MUX2TO1	2:1 Multiplexer Cell

COUNTER CELLS

LS163	4-Bit Synchronous Binary Counter
LS169	4-Bit Synchronous Binary Up/Down Counter

DECODER/ENCODER CELLS

LS138	3:8 Decoder with Enable
LS139	2:4 Decoder with Enable
LS148	8:3 Priority Encoder

COMPARATOR CELL

LS85	4-Bit Magnitude Comparator

ARITHMETIC OPERATOR CELL

LS83	4-Bit Full Adder
LS283	4-Bit Full Adder
LS183	Full Adder

PARITY GENERATOR CELL

LS180	9-Bit Odd/Even Parity Checker

GATE CELLS

AND8	8 Input AND Gate
AOI211	2-1-1 AND-OR-Invert
AOI22	2-2 AND-OR-Invert
AOI31	3-1 AND-OR-Invert
EXNOR	Exclusive NOR Gate
EXOR	Exclusive OR Gate
HBUF	High Drive Buffer.
HBUFL	Large High Drive Buffer
MBUF	Medium Drive Buffer
INBUF	Input Buffer
INV	Inverter
INV3/OUTINV	High Drive INV/Output Buffer
OUTINVL	Large Inverting High Drive Output Buffer
IOBUF	Input/Output Buffer
IOBUFL	Large I/O Buffer
DLYCEL	Delay Cell
NAN2	2 Input NAND Gate
NAN3	3 Input NAND Gate
NAN4	4 Input NAND Gate
NAN5	5 Input NAND Gate
NOR2	2 Input NOR Gate
NOR3	3 Input NOR Gate
NOR4	4 Input NOR Gate
OR8	8 Input OR Gate
OA122	2-2 OR-AND-Invert
OAI31	3-1 OR-AND-Invert
INVT	Inverting 3-State Driver
TBUF	Non-Inverting 3-State Driver

LATCH & FLIP-FLOP CELLS

CCND	Cross Coupled NAND Latch
CCNR	Cross Coupled NOR Latch
DFF	D Flip Flop
DFFR	D Flip Flop with Reset
DFFRS	D Flip Flop w/Set & Reset
JKFF	J-K Flip Flop
LAT	Transparent Latch
LATBUF	3-Stateable Transparent Latch
LATR	Transparent Latch with Reset
SRBN	Shift Register
UDC	Up/Down Counter
PCL2	Two Phase Clock

ANALOG CELLS

ANSW	Analog Switch
CBGX	Current Bias Generators
DS1216	Schmitt Trigger (1.2-1.6V)
DS1218	Schmitt Trigger (1.2-1.8V)
DS1238	Schmitt Trigger (1.2-3.8V)
DS1323	Schmitt Trigger (1.3-2.3V)
DS1527	Schmitt Trigger (1.5-2.7V)
DS1728	Schmitt Trigger (1.7-2.8V)
DS2028	Schmitt Trigger (2.0-2.8V)
DS2232	Schmitt Trigger (2.2-3.2V)
OSCP	General Purpose Oscillator
POR	Power On Reset
PORLC	Low Current Power On Reset
VCM1	Voltage Reference (50uA)
VCM2	Voltage Reference (100uA)
VCM3	Voltage Reference (200uA)
OPAMP	General Purpose Operational Amplifier
COMP05	High Speed Low Power Comparator
COMPG	General Purpose Comparator

PAD CELLS

INPD	Input PAD
IODPD48	48mA Input/Open-Drain Output Pad
IOPD2S	2mA Split P-Channel I/O PAD
IOPD4	4mA Input/Output PAD
IOPD4S	4mA Split P-Channel I/O PAD
IOPD8	8mA Input/Output PAD
IOPD16	16mA I/O Pad
IOPD24	24mA I/O Pad
IPPD4	Input PAD with 400uA Pullup
IPPD8	Input PAD with 800uA Pullup
ODPD4	4mA 5V Open-Drain Output PAD
ODPD8	8mA 5V Open-Drain Output PAD
ODPD16	16mA 5V Open-Drain Output Pad
ODPD48	48mA 5V Open-Drain Output Pad
ONPD4	4mA 7V Open-Drain Output PAD
ONPD8	8mA 7V Open-Drain Output PAD
OPD4	4mA Output PAD
OPD8	8mA Output PAD
OPD16	16mA Output Pad
OPD24	24mA Output Pad
OPPD4	4mA 3-State Output PAD
OPPD8	8mA 3-State Output PAD
PU30	P-Channel Pullup
PD30	N-Channel Pulldown

SUPERCELLS™:

UART Tool-Kit	UART Building Cell-Set
Manchester SuperCell™	Encoder/Decoder
RTC SuperCell™	Real Time Clock
PC-KBRD SuperCell™	PC Keyboard Interface Controller
SCSI SuperCell™	SCSI Interface Controller
TWINAX SuperCell™	5250 Interface Controller
8250 SuperCell™	UART
8259 SuperCell™	Prog. Interrupt Controller
8254 SuperCell™	Programmable Interval Timer
6845 SuperCell™	CRT Controller
8237 SuperCell™	DMA Controller
TIMER SuperCell™	Master Timer
FDDS SuperCell™	Data Separator
65CX02 SuperCell™	65C02 Core Microprocessor
RAM SuperCell™	Modular RAM (512 bits/block)
ROM SuperCell™	Modular ROM (512 bits/block)
VCO SuperCell™	Voltage Controlled Oscillator
555 SuperCell™	555 Timer
DTMF SuperCell™	DTMF Tone Generator
ATOD SuperCell™	8-Bit Analog to Digital Converter

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Boulevard, Hauppauge, NY 11788 (516)273-3100

STANDARD MICROSYSTEMS CORPORATION

Quality Assurance and Quality Control

Volume manufacturing of quality products requires a rigorous commitment by Standard Microsystems and all of its employees. Each phase of the operation from design to shipping must conform to documented procedures which have created a product of proven reliability.

The design of a reliable product is assured by adherence to tested and proven design rules. Any change in design rules must be evaluated using a design-rule test vehicle. Each new product is evaluated first by prototype wafer runs and thorough preliminary production and device characterization.

Manufacturing is monitored by Quality Control. They insure that parameters meet specifications on incoming material, within the line and at outgoing inspection. They are responsible for monitoring clean room standards and work methods.

The Quality Assurance Department is the customer representative. They have the primary responsibility of insuring that products meet current industry standards. They also evaluate developmental processes and products, and perform equipment calibration.

The following is a more detailed description of how SMC® is organized to produce quality products.

1.0 Scope

The measures taken by SMC® to produce reliable integrated circuits and the assembly/screening options available to the customer are given in this section.

2.0 Approach

Factors relating to quality and reliability are discussed in the following order: documentation, package options, screening, test and characterization, quality monitoring, reliability assessments, and record keeping.

3.0 Applicable Documentation

SMC® internal specifications define every phase of manufacturing from product development through production and must be approved by the designated representatives of Engineering, Manufacturing, Processing, Quality Control and Quality Assurance departments.

3.1 Design Rules

3.1.1 Geometric design rules define layout considerations, alignment structures, critical-dimension targets, and input/output protection networks.

3.1.2 Electrical design rules define performance criteria, measurement methods, device parameters, and process parameters.

3.2 Procurement Specifications

All critical material is purchased to SMC® specifications from qualified vendors.

3.3 Process Specifications

3.3.1 The procedures used for wafer processing and assembly of microcircuits are fully documented.

3.4 Quality Control Procedures

QC procedures define the sampling techniques, accept/reject criteria and test methods used in quality audits.

3.5 Quality Assurance Procedures

QA procedures define methods for product/process qualification, reliability testing and failure analysis.

3.6 Military Standards and Specifications

Where applicable, SMC® specifications are based on the following Military Standards:

MIL-C-45662	Calibration System Requirements
MIL-I-45208	Inspection System Requirements
MIL-M-38510	General Specification for Microcircuits
MIL-M-55565	Packaging of Microcircuits
MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-1331	Microelectronics Terms and Definitions
MIL-Q-9858	Quality System Requirements

4.0 Package Options, Features

4.1 Ceramic

Gold plating on external leads and die cavity, gold eutectic die attach.

4.2 Cerdip

Meets MIL-STD-883 internal moisture content requirements of Method 5005. Substrate connections are made through jumper chips, gold eutectic die attach.

4.3 Plastic

The plastics used are SMC® approved low stress, low mobile ion compounds. SMC® offers Plastic Dual Inline (PDIP), Small Outline Integrated Circuit (SOIC), and Plastic Leaded Chip Carrier (PLCC) Packages.

5.0 Screening Options

5.1 High-Reliability Screening

The routing is as defined in MIL-STD-883 Method 5004 for Class B product. Periodic Quality Conformance data (para. 9.2) is taken on generically similar parts. A sample flow chart for high-reliability ceramic product is given at the end of this section.

5.1.1 Internal Visual
Both die visual and preseal visual inspections are to the criteria of Method 2010, Condition B of MIL-STD-883. An AQL audit is performed on each lot by Quality Control.

5.1.2 Stabilization Bake
All parts are given the stabilization bake according to Method 1008, Condition C of MIL-STD-883.

5.1.3 Temperature Cycling
All parts are subjected to 10 cycles of -65°C to + 150°C per Method 1010, Condition C of MIL-STD-883.

5.1.4 Constant Acceleration
All parts are subjected to a 30,000 g force in the Y1 orientation per Method 2001, Condition E.

5.1.5 Seal
Hermeticity testing is performed to conditions A and C of MIL-STD-883 Method 1014.

5.1.6 Pre Burn-in Electrical Test.
Ordinarily this is the same as final electrical test.

5.1.7 Burn-in
Condition A and Condition D of MIL-STD-883 Method 1015 are available. The stress is applied for 160 hours at 125°C or at other temperatures according to the time-temperature regression.

5.1.8 Final Electrical Test
Verifies functional and parametric performance to the device specifications.

5.1.9 Final Visual Inspection
All parts are inspected to Method 2009 of MIL-STD-883.

5.2 Standard Screening

Standard Screening is designed for the industrial-commercial customer and is available in all package types. For hermetic packages, temperature cycling, centrifuge and hermeticity are specified as well as die, preseal, and final visual inspection.

5.2.1 Standard Die and Preseal Visual Inspections (AC-04, AC-08, AD-98, AD-90, AP-98, AP-92, QC-32, QC-33).

These inspections were developed from Method 2010 of MIL-STD-883. The inspection criteria are specific to SMC's® PMOS, NMOS COPLAMOS® and CMOS technologies.

5.2.2 Temperature Cycling (AC-15, AD-86)
Temperature cycling is performed to the MIL-STD-883, equivalent of Method 1010 Condition C, -65°C/ +150°C, ten cycles.

5.2.3 Constant Acceleration (centrifuge) (AC-16, AD-85)
Constant Acceleration is performed to the MIL-STD-883, equivalent of Method 2001, Condition E, 30,000 g in the Y1 orientation.

5.2.4 Hermeticity (AC-11, AD-84)
This screen includes fine and gross leak testing to SMC® equivalent of MIL-STD-883 Method 1014 Conditions A and C.

5.2.5 Final Electrical Test
This test verifies functional and parametric performance to the device specifications.

5.3 Custom Screening

Certain applications require special screening which can be arranged upon request.

6.0 Electrical Test

Test areas for wafer probe and final test are equipped with temperature, humidity and air-ionization control for ESD protection and test repeatability.

6.1 Probe and Final Test

SMC® test programs are developed by Test Engineering and verified by device characterization. An approval procedure is required for the transfer of a new test program or a revised test program from engineering to production.

6.2 Characterization/correlation

Characterization of parts and correlation of test results with customer incoming testing performed on SMC® test equipment, including Megatest™ and Sentry®, and GenRad™ test systems.

6.3 Product Engineering

SMC® product engineers characterize parts to improve processing target parameters and test correlation with customers.

7.0 Purchased Material

Manufacturing materials are purchased from qualified vendors to SMC® procurement specifications.

8.0 Quality Control

The Quality Control Department reports to the Vice President of Quality Assurance. QC is responsible for incoming inspection, in-process audits, out-going inspection, document control, processing returned material and certification of compliance to specification.

8.1 Incoming Inspection

Inspectors verify critical parameters on all material used in manufacturing. The department maintains an approved vendor list and interfaces directly with vendor QC departments.

8.2 In-process Audits

QC performs an on-going monitoring of wafer processing, test and assembly functions.

8.3 Outgoing Audit

QC inspectors verify proper documentation and perform an external mechanical/visual inspection prior to shipment.

8.4 Document Control

All procedures for design, wafer processing, assembly, quality control and quality assurance are maintained by document control.

8.5 Returned Material Processing

Returned material, whether for device performance or clerical reasons, is processed through visual and electrical testing.

8.6 Certificates of Compliance

Certificates of Compliance are available for specified screening and/or for products ordered under a customer part number/specification.

9.0 Quality Assurance

The Quality Assurance Department is the customer's representative and is independent of the product line and manufacturing organizations. Quality Assurance is responsible for reliability assessment of new and existing processes, material analysis, failure analysis, calibration and development of evaluation methods.

9.1 Process Qualification

All new processes and process revisions must equal or exceed the reliability of existing processes on applicable sections of the SMC® Quality Conformance Test.

9.2 Quality Conformance Test

Samples of finished product are tested periodically to the criteria of QA-01 (see Table 1). This test sequence provides historical data which is also used for qualification of new products and processes. The various subgroups contain tests referenced in Method 5005 of MIL-STD-883 as well as tests designed around industry requirements not yet incorporated in military standards.

9.3 Analysis

9.3.1 Analytical Capabilities include:
Complete functional and parametric test
Radiography
Decapsulation of ceramic cerdip and plastic packages
Chemical and plasma layer removal
High power optical inspection
Infrared and thermal imaging
Liquid crystal analysis
Laser circuit isolation
Multipoint probing
Precision cross-sectioning
Scanning electron microscope (SEM)
Energy dispersive X-ray (EDX)
Voltage contrast and specimen current imaging
Fast-fourier transform infrared (FTIR)

9.3.2 Scanning electronic microscopy is used in the periodic evaluation of workmanship in wafer processing and assembly, to support engineering efforts at process development and improvement, and in failure analysis.

9.3.3 Failure Analysis is performed upon request by sales, marketing or manufacturing organizations and is also performed on reliability test failures. The analysis activity supports the development of new product, process improvements, and the evaluation of screening methods.

9.3.4 Material analysis is performed on layers of the integrated circuit and on packaging to support the engineering development. This characterization is performed on in-house facilities. Independent outside analytical laboratories are used if and when required.

9.4 Calibration

The Quality Assurance Calibration Laboratory specifies calibration intervals, performs calibration and maintains calibration records. The laboratory is traceable to the National Bureau of Standards.

10.0 Manufacturing Lot Traceability

SMC® maintains traceability on all product types in all packaging options (including plastic). The information available includes:

10.1 Wafer Processing Records

Sign-off and date on all operations, critical measurements and inspection records.

10.2 Wafer Lot Acceptance (Mapping)

Device parameters are recorded using a high-speed Accutest® 3600 system. Further evaluation is performed using an HP 4145A semiconductor parametric analyzer.

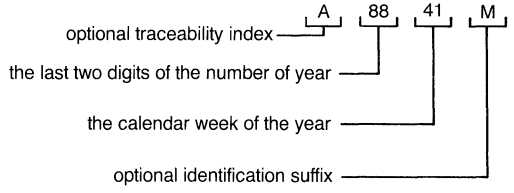
10.3 Wafer Probe and Final Test Data

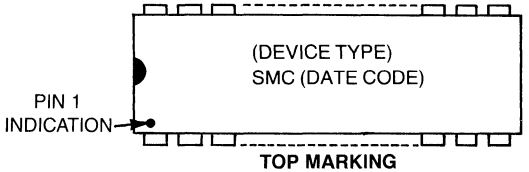
These are correlated with mapping results to develop optimized process targets and yield improvement.

10.4 Assembly Records

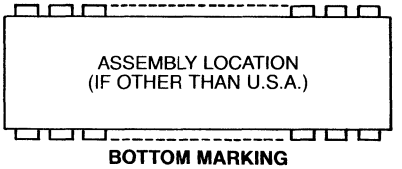
Inspection results and screening throughput are recorded with date and sign-off for each lot.

DATE CODE INTERPRETATION





TOP MARKING



BOTTOM MARKING

BI = BURN-IN (ADDED WHEN APPROPRIATE)

TABLE 1—QA-01 QUALITY CONFORMANCE

ROUTINE MONITOR (REFERENCE MIL-STD-883, METHOD 5005, GROUP B)

Test	SMC® Test Method	MIL-STD-883 Method	MIL-STD-883 Condition	accept no. or LTPD	Frequency Package Type
Subgroup 1					
Physical dimensions		2016		2 devices (no failures)	every package lot
Subgroup 2					
Resistance to solvents	QC-21	2015	Marking Permanence	4 devices	every shipment
Subgroup 3					
Solderability	QC-15	2003	Soldering temperature of 245°C ± 5° C	10	every shipment
Subgroup 4					
Internal visual and mechanical	QC-33	2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (no failures)	every shipment
Subgroup 5					
Bond strength		2011		15	
(1) Thermosonic	QC-31		(1) Test condition C or D		every
(2) Ultrasonic or wedge			(2) Test condition C or D		shipment
Die shear strength	QC-35	2019			
Subgroup 6					
Internal water-vapor content		1018	5,000 ppm maximum water content at 100°C	3 devices (no failures) or 5 devices (1 failure)	periodic conformance all hermetic [1]
Subgroup 7					
Seal	AC-11	1014	As applicable	5	every shipment all hermetic [1]
(a) Fine					
(b) Gross					
Subgroup 8					
Electrical parameters			Group A, subgroup 1	15 (no failures)	new device types
Electrostatic discharge sensitivity	QA-11	3015			
Electrical parameters			Group A, subgroup 1		

DIE RELATED TESTS (REFERENCE MIL-STD-883, METHOD 5005, GROUP C)

Test	SMC® Test Method	MIL-STD-883 Method	MIL-STD-883 Condition	accept no. or LTPD	Package Type
Subgroup 1					
Steady state life test	QA-02	1005	Test condition to be specified (typically 1,000 hours at 125°C)	5	all
End-point electrical parameters	Final test		As specified in the applicable device specification		
Subgroup 2					
Temperature cycling	AC-15	1010	Test condition C, 10 cycles	15	
Constant acceleration	AC-16	2001	Test condition E min. Y_1, orientation only		all hermetic [1]
Seal		1014	As applicable		
(a) Fine	AC-11				
(b) Gross					
Visual examination	QC-22				
End-point electrical parameters	Final test		As specified in the applicable device specification		

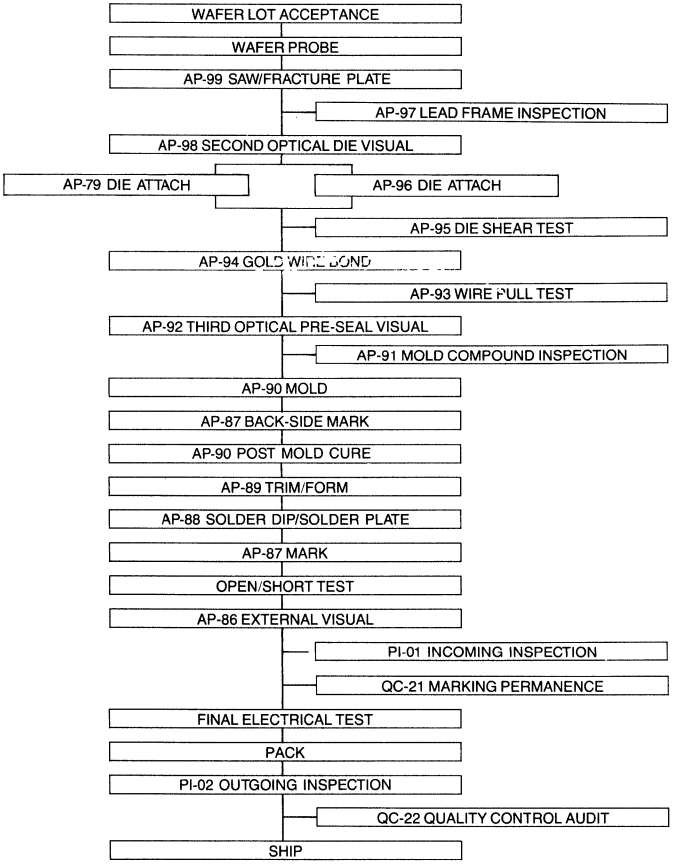
PACKAGE RELATED (REFERENCE MIL-STD-883, METHOD 5005, GROUP D)

Test	SMC® Method	MIL-STD-883 Method	MIL-STD-883 Condition	accept no. or LTPD	Package Type
Subgroup 1					
Physical dimensions		2016		15	all
Subgroup 2					
Lead integrity	QC-19	2004	Test condition B2 (lead fatigue)	15	all
Seal	AC-11	1014	As applicable		
(a) Fine					all hermetic[1]
(b) Gross					
Lid torque		2024	As applicable		cerdip only
Subgroup 3					
Thermal shock		1011	Test condition B, 15 cycles	15	
Temperature cycling	AC-15	1010	Test condition C, 100 cycles		all hermetic[1,2]
Moisture resistance		1004			
Seal	AC-11	1014	As applicable		
(a) Fine					
(b) Gross					
Visual examination			Per visual criteria of Method 1004 and 1010		
End-point electrical parameters			As specified in the applicable device specification		
Subgroup 4					
Mechanical shock		2002	Test condition B minimum	15	
Vibration, variable frequency		2007	Test condition A minimum		all hermetic
Constant acceleration	AC-16	2001	Test condition E minimum, Y_1 orientation only		
Seal	AC-11	1014	As applicable		
(a) Fine					
(b) Gross					
Visual examination					
End-point electrical parameters			As specified in the applicable device specification		
Subgroup 5					
Salt atmosphere		1009	Test condition A minimum	15	
Seal	AC-11	1014	As applicable		all hermetic[1,2]
(a) Fine					
(b) Gross					
Visual examination			Per visual criteria of Method 1009		
Subgroup 6					
Internal water-vapor content		1018	5,000 ppm maximum water content at 100°C	3 devices (no failures) or 5 devices (1 failure)	all hermetic[1]
Subgroup 7					
Adhesion of lead finish		2025		15	all
Subgroup 8					
Lid Torque		2024		5 devices (no failures)	cerdip
Subgroup 9					
Humid Environment	QA-04		1000 hours 85°C/85% Relative Humidity	15	plastic
End-point electrical parameters	Final test				
Subgroup 10					
Autoclave (Pressure Cooker)	QA-05		96 hours at 2 atm, 121°C	5	plastic
End-point electrical parameters	Final test				
Subgroup 11					
Temperature Cycling	AC-15	1010	Test Condition C, 100 cycles	15	plastic
End-point electrical parameters	Final test				

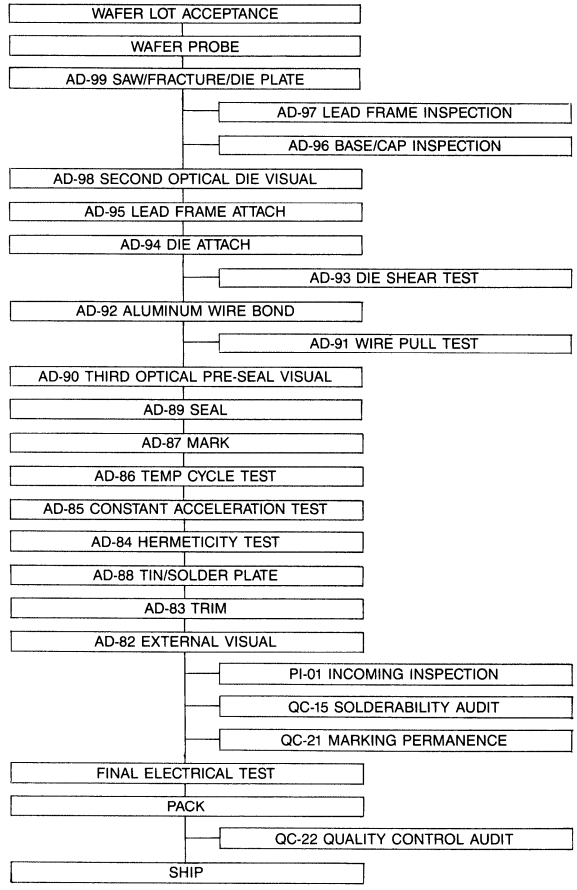
[1] Hermetic packages include ceramic and cerdip.
[2] Packages having gold plating thicknesses of 200 microinches or less are not required to pass subgroups 3 and 5.

PACKAGE ASSEMBLY FLOW DIAGRAMS

PLASTIC (NOTE 1)



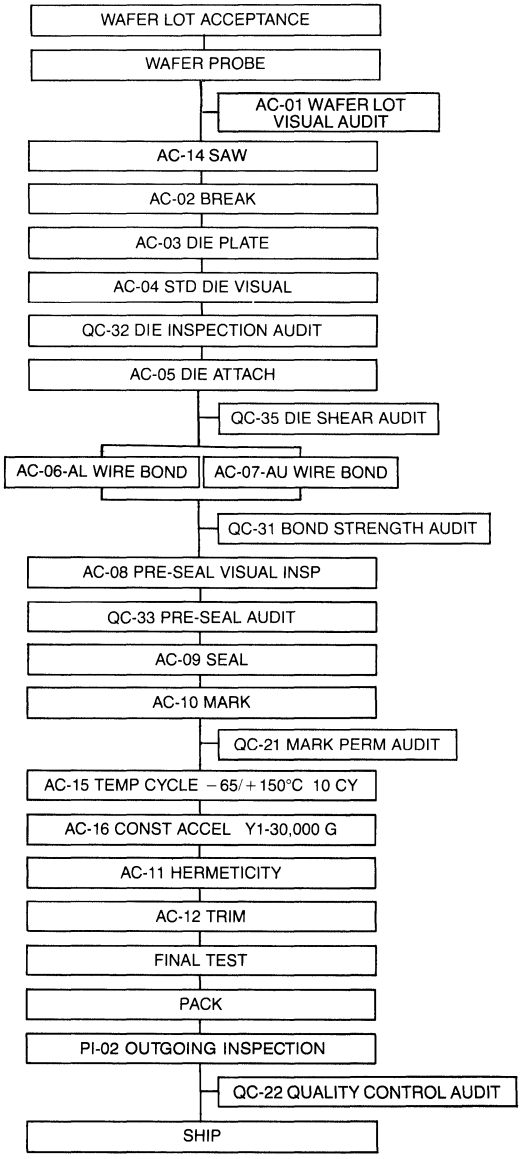
CERDIP (NOTE 1)



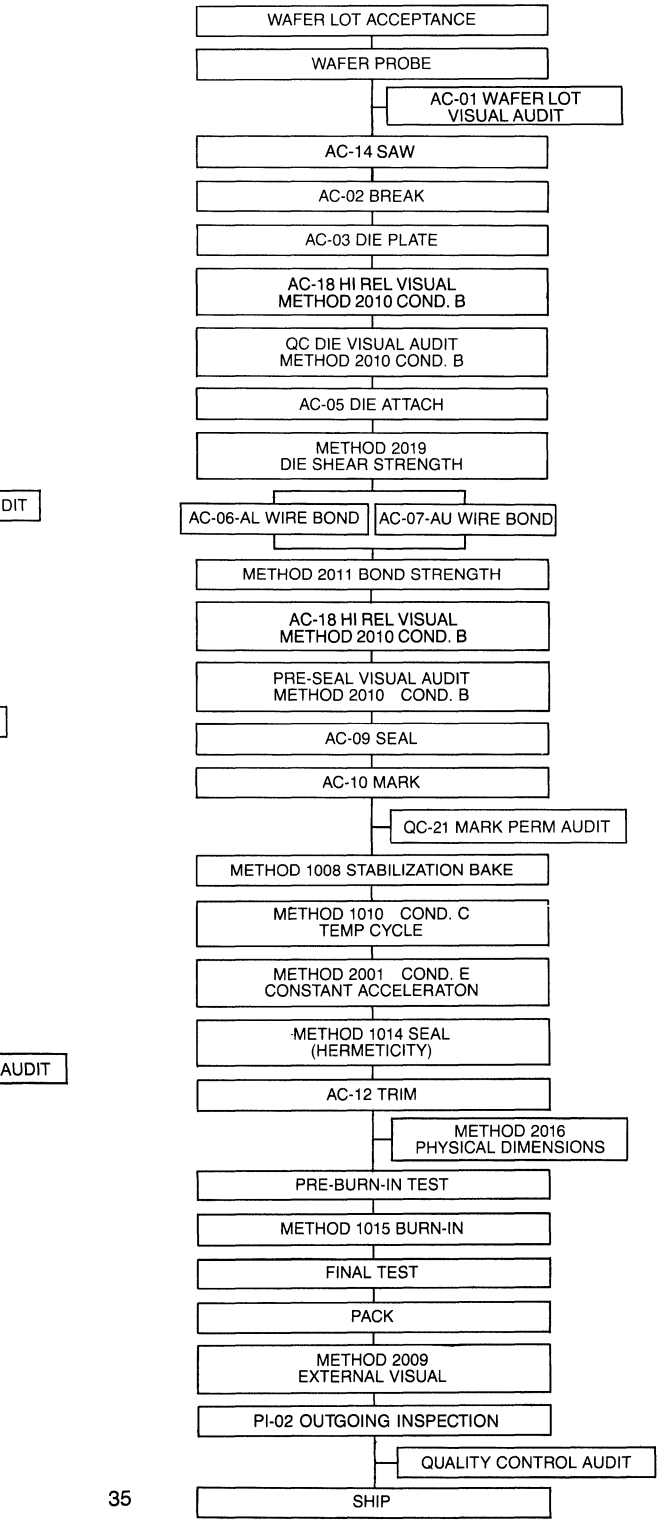
Note 1—Plastic and cerdip assembly is sub-contracted Assembly operations are controlled by SMC® approved sub-contractor specifications.

PACKAGE ASSEMBLY FLOW DIAGRAMS

CERAMIC



HI REL AVAILABLE ON ALL HERMETIC PACKAGES



Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A Controller	MIL-STD-1553A Manchester Interface Controller	1 MB	+5	40 DIP/ 44SMT	39-40
COM 1553B	MIL-STD-1553B Controller	MIL-STD-1553B Manchester Interface Bus Controller/Remote Terminal	1 MB	+5, −5, +12	40 DIP/ 44SMT	41-56
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	57-58
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	59-60
COM 2651	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock	1 MB	+5	28 DIP/ 28 SMT	61-62
COM 2661-1 -2 -3	USART/EPCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock	1 MB	+5	28 DIP/ 28 SMT	63-64
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	65-76
COM 52C50	TWINAX	Interface Controller for IBM System/ 34, 36, 38 designated TWINAX or 5250 environment	1 MB	+5	28 DIP/ 28 SMT	77-94
COM 7210	GPIB Interface	Intelligent Interface Controller for GPIB (IEEE-488-1978)	8 MHz	+5	40 DIP	95-106
COM 78808	OCTAL UART	8 UART's, 8 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	68 CERDIP/ PLCC	135-136
COM 78C808	OCTAL UART	CMOS Version of the COM 78808	19.2 KB	+5	68 PLCC	137-150
COM 78C804	QUAD UART (QUART)	4 UARTS, 4 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	48 DIP 44 PLCC	121-134
COM 78C802	DUAL UART (DUART)	2 UARTS, 2 Baud Rate Generators plus control logic and modem signals all on a single chip	19.2 KB	+5	40 DIP 44 PLCC	107-120
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 Dual 32 bit CRC Generator/Checker	2.0 MB	+5	20 DIP	151-152
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (compatible with COM 2017)	40 KB	+5	40 DIP	153-160
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion, margin	62.5 KB	+5	40 DIP	59-60
COM 81C17	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex with built-in Baud Rate Generator	100 KB	+5	20 DIP/ 20 SMT	161-168
COM 82C11	PAI	CMOS Programmable Centronics Parallel Printer Adapter Interface (PAI) with high current driving capability	1 MHz	+5	40 DIP	169-176

Data Communication Products CONT.

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	177-192
COM 82586	LANC	Ethernet Local Area Network Coprocessor for CSMA/CD Medium Access Control	10 MHz	+5	48 DIP/ 68 PLCC	193-196
COM 82C501	ESI	Ethernet Serial Interface compatible with COM 82586. Generates clocks and performs Manchester Encoding/Decoding	10 MHz	+5	20 DIP	197-200
COM 82C502	LANT	Ethernet Transceiver chip. Compatible with COM 82586 and COM 82C501.	10 MHz	+5, +10V	16 DIP	201-204
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (compatible with COM 2502)	40 KB	+5	40 DIP	153-160
COM 9026	LANC	Local Area Network Controller for token pass systems	2.5 MB	+5	40 DIP/ 44 SMT	205-206
COM 90C26	LANC	CMOS Version of COM 9026	2.5 MB	+5	40 DIP	207-222
COM 90C32	LANT	Local Area Network Transceiver	2.5 MB	+5	16 DIP	223-228
COM 9046	SSBSS	Single Side Band Speech Scrambler, Low Power, Full Duplex, uses 3.58 MHz TV burst crystal	NA	±2.6	14 DIP	229-232
COM 90C56[2]	ELANC	CMOS Enhanced Local Area Network Controller, with high throughput, network management and network diagnostic	5 MBps	+5	48 PLCC	233-234
COM 90C62[2]	COMBO CHIP	Complete Local Area Network Controller on a chip. Includes the combined functions of the COM 90C26 and the COM 91C32	2.5 MB	+5	40 DIP	235-238
COM 9064	IBM 3270	IBM 3270 COAX type "A" controller +5V only version of COM 9004	2.36 MB	+5	40 DIP/ 44 SMT	239-246
COM 91C32	LANT	Improved COM 90C32 LAN Transceiver, which integrates an internal crystal oscillator and reset circuitry for the COM 9026/COM 90C26.	2.5 MB	+5	16 DIP	247-252
COM 92C32[2]	LANT	This transceiver performs Manchester Encoding/Decoding to allow twisted pair operation of ARCNET. Compatible with COM90C26 and HYC9078	2.5 MB	+5	16 DIP	253-256
HYC 9058	HIT 1	High Impedance Transceiver for Local Area Networks allows BUS topology with multi drop nodes	2.5 MBps	+5	20 SIP	257-262
HYC 9068	LAND	Local Area Network Driver with (93 Ω) line matching impedance for ARCNET networks	2.5 MBps	+5	20 SIP	263-266
HYC 9078[2]	HIT 2	High Impedance Transceiver for Local Area Networks for operation at 5MHz	5 MBps	+5	20 SIP	267-268

[2]For future release

STANDARD MICROSYSTEMS CORPORATION

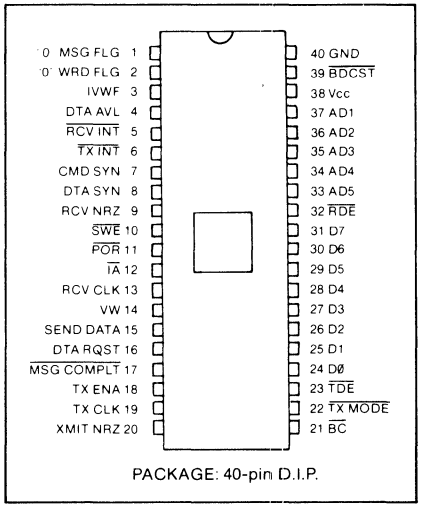
COM 1553A
μPC FAMILY

MIL-STD-1553A "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553A
- ☐ Operates as a: Remote Terminal Responding
  Bus Controller Initiating
- ☐ Performs Parallel to Serial Conversion when Transmitting
- ☐ Performs Serial to Parallel Conversion when Receiving
- ☐ Compatible with HD-15531 Manchester Encoder/Decoder
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N Channel MOS Technology
- ☐ Available in PC Board Form from Grumman Aerospace Corporation

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

GENERAL DESCRIPTION

The COM 1553A SMART® (Synchronous Mode Avionics Receiver/Transmitter) is a special purpose COPLAMOS N-Channel MOS/LSI device designed to provide the interface between a parallel 8-bit bus and a MIL-STD-1553A serial bit stream.

The COM 1553A is a double buffered serial/parallel and parallel/serial converter providing all of the "hand shaking" required between a Manchester decoder/encoder and a microprocessor as well as the protocol handling for both a MIL-STD-1553 bus controller and remote terminal.

The COM 1553A performs the following functions in response to a 16 bit Command Word. It provides address detection for the first five bits of the serial data input. If all 1's appear in the address field, a broadcast signal is generated. The sixth bit is decoded as mode: transmit or receive. The next five bits are decoded for zero message flag and special flags in the subaddress/mode field. The last five bits (word-count field) are decoded determining the number of words to be received or transmitted.

When receiving data sync the COM 1553A performs a serial to parallel conversion, buffers the 16 bit message word, and formats it into two parallel (8 bit) bytes for presentation to the I/O bus under processor or hard wired logic control.

In the transmit mode the COM 1553A takes two parallel 8 bit data words from the I/O bus and serially transmits the resultant 16 bit word to the Manchester encoder. This is done under the control of Send Data. To facilitate data transfer the COM 1553A provides all necessary buffering and storage for transmitted and received data. It also provides all necessary hand shaking, control flags and interrupts to a processor or hard wired logic terminal. See block diagram 1.

The COM 1553A can be set up as either a remote terminal or a bus controller interface.

The COM 1553A is compatible with Harris' HD-15531 CMOS Manchester Encoder-Decoder chip and interfaces directly with it. A 3 device kit consisting of: SMC's COM 1553A, Harris' HD-15531 and Circuit Technology's CT1231 forms a complete system interface for the message structure of MIL-STD-1553A. See block diagram 2.

Note: All terminology utilized in this data sheet is consistent with MIL-STD-1553.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

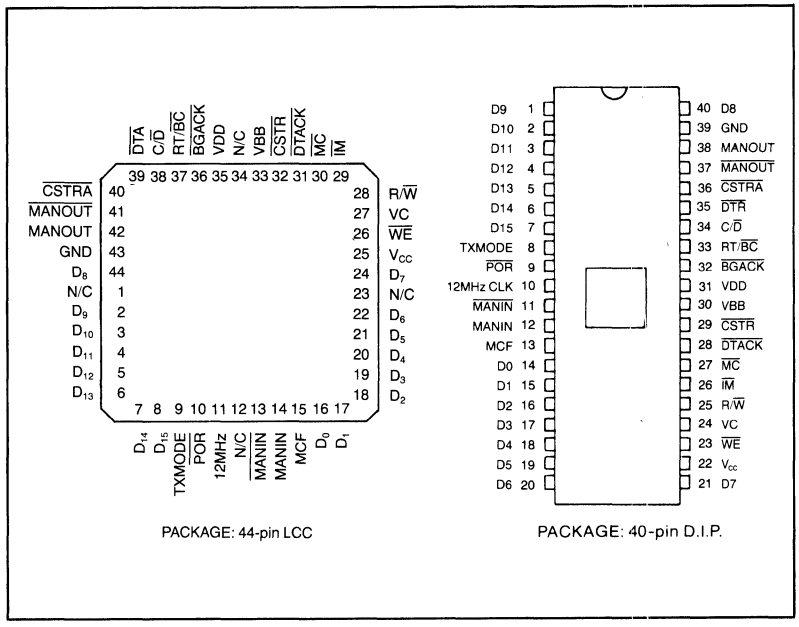
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

MIL-STD-1553B "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553B
- ☐ Operates as both Remote Terminal and Bus Controller
- ☐ Manchester II Serial Biphase Input/Output
- ☐ 16 bit Microprocessor compatible
- ☐ Command/Data Sync Detection/Identification
- ☐ Automatic Command Response Generation
- ☐ On-Chip Address Recognition
- ☐ Error Detection For:
  - Sync Errors
  - Parity Errors
  - Word Count Errors
  - Bit Count Errors
  - Invalid Manchester Code
  - Incorrect Address
  - Incorrect Bus Response Time
- ☐ TTL Compatible
- ☐ Recognizes Mode Codes and Broadcast Commands
- ☐ Provides DMA handshaking signals
- ☐ COPLAMOS® n-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 44-pin LCC

PACKAGE: 40-pin D.I.P.

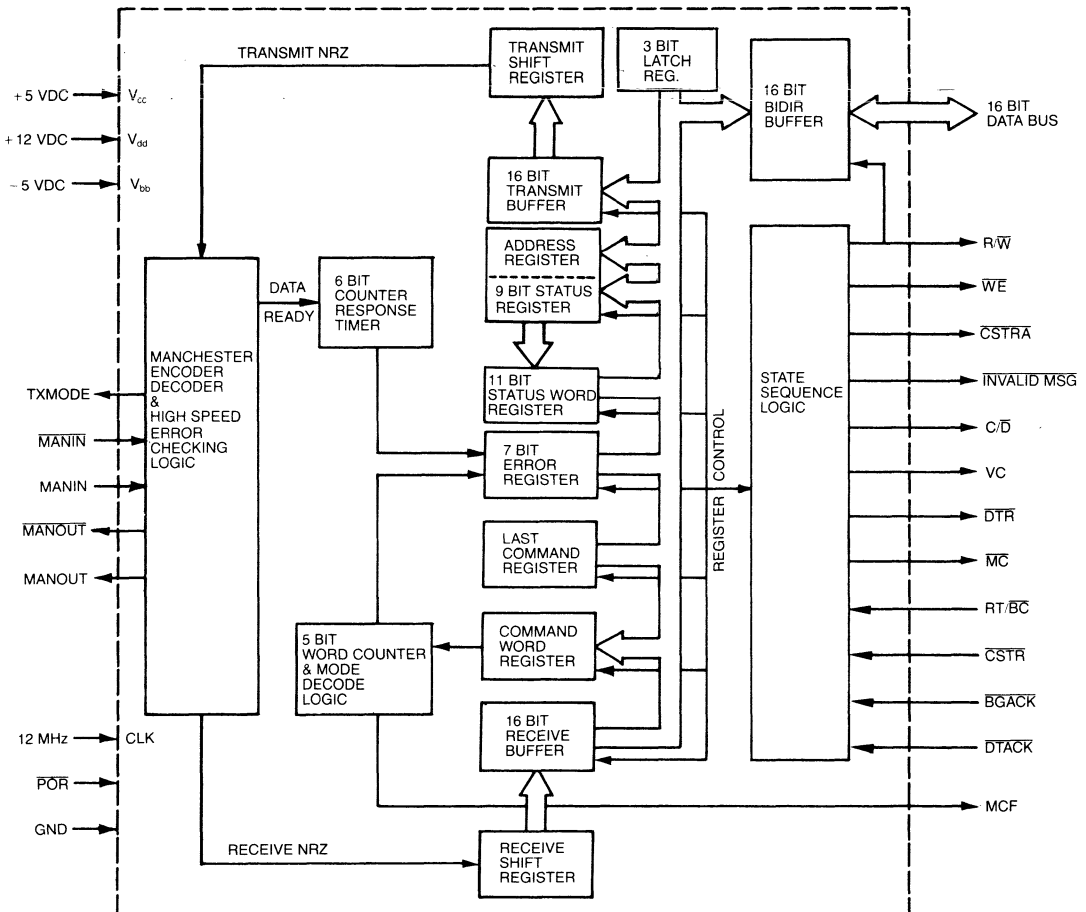
GENERAL DESCRIPTION

The COM1553B SMART® (Synchronous Mode Avionic Receiver-Transmitter) is a 40-pin COPLAMOS® n-Channel MOS/VLSI circuit designed to simplify the interface of a microprocessor or buffer to the serial MIL-STD-1553B data bus.

The COM1553B is a double buffered serial to parallel, parallel to serial converter. It receives serial Manchester II biphase encoded data from a 1553B bus receiver and converts it to 16 bit parallel data. When receiving Manchester II data, the COM1553B detects and identifies sync polarity, reconstructs the clock, detects zero crossing, checks for the proper number of bits and performs a parity check on the incoming data. In addition to parity check, the COM1553B also checks for sync errors, invalid Manchester code, improper word count, incorrect address and incorrect bus response time. The transmitter in turn, accepts 16 bits parallel data and serially transmits it as Manchester II data, appending the appropriate sync and parity.

The COM1553B recognizes protocol commands, and automatically generates the proper response, thereby offloading what otherwise would be microprocessor tasks. This feature eliminates critical software timing requirements.

The COM1553B is designed to work both as a Bus Controller and Remote Terminal, making it universal within the MIL-STD-1553B environment. The COM1553B automatically loads and recognizes its own address. It determines the type of transfer required in both the Bus Controller and Remote-Terminal modes and generates the proper control signals to complete the transfer. It automatically transmits the status word and detects message errors and mode commands. Furthermore, it generates the control signals for DMA operation, therefore eliminating processor intervention.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-7, 14-21, 40	16-bit Data Bus	D0-D15	Three-state bidirectional data lines used to transfer Command, Data, Error and Status Words between the COM1553B and external memory.
8	Transmit Mode	TXMODE	This output signal when high indicates that the COM1553B is transmitting information on the 1553B bus.
9	Power On Reset	$\overline{POR}$	Input signal used to initialize or reset the Error registers. The RT address must be reloaded after POR is issued.
10	12 MHz Clock	12 MHz CLK	12 MHz clock input.
11	Complementary Manchester In	$\overline{MANIN}$	This input is low when there is no data on the bus. A high level indicates that the data is in its negative state (Refer to receive waveform, figure 3).
12	Manchester In	MANIN	This input is low when there is no data on the bus. A high level indicates that the data is in its positive state (Refer to receive waveform, figure 3).
13	Mode Code Flag	MCF	Output signal that is active high when a mode command (all 1's or all 0's in subaddress) has been detected.
22	Power Supply	VCC	+ 5 volts DC supply.
23	Write Enable	$\overline{WE}$	Output signal. When low, $\overline{WE}$ indicates that the data on the 16 bit data bus is stable and can be written into the external memory.
24	Valid Command	VC	Output signal that is pulsed high to signify the reception of a valid command.
25	Read/Write	R/$\overline{W}$	Output signal that indicates whether a DMA transaction is a COM1553B read (when high) or a write (when low) operation.
26	Invalid Message	$\overline{IM}$	Output signal which is pulsed low at the same time as MC to indicate that a message error has occurred. $\overline{IM}$ is also pulsed low while MC remains high if there are errors in the Command word with matching address.
27	Message Complete	$\overline{MC}$	Output signal used as either an interrupt or flag to the processor whenever a COM1553B transaction has been completed.
28	Data Transfer Acknowledge	$\overline{DTACK}$	This input signal when low indicates that the Data Transfer Request ($\overline{DTR}$) and $\overline{BGACK}$ has been acknowledged and data is on the data bus.
29	Command Strobe	$\overline{CSTR}$	This input signal when low is used to inform the COM1553B that a Command Control Code is available in external memory. When the COM1553B is ready, it issues a Command Strobe Acknowledge and initiates a memory read cycle to load the Command Control Code bits CB2-CB0.
30	Power Supply	VBB	− 5 volts DC supply voltage.
31	Power Supply	VDD	+ 12 volts DC supply.
32	Bus Grant Acknowledge	$\overline{BGACK}$	This input signal, when low, indicates that the processor has acknowledged $\overline{DTR}$ and relinquished the data bus.
33	Remote Terminal/Bus Controller	RT/$\overline{BC}$	When this input is high the COM1553B operates as a Remote Terminal. When RT/$\overline{BC}$ is low, the COM1553B operates as a Bus Controller.
34	Command/Data	C/$\overline{D}$	This output signal during memory write operations indicates either a Command or Data Word transfer. A low level indicates that the COM1553B is writing a Data Word, Status Word, the contents of the Error Register, or the contents of the Last Command Register into external memory. A high level indicates that the transferred word is a Command Word. During memory read operations this output is low. It goes high to indicate that data has been latched internally and the read operation is completed.
35	Data Transfer Request	$\overline{DTR}$	Output signal that initiates a DMA transfer with the processor.
36	Command Strobe Acknowledge	$\overline{CSTRA}$	This output pulse acknowledges the receipt of the command strobe and initiates the Command Control Code (CB2-CB0) transfer.
37	Complementary Manchester Output	$\overline{MANOUT}$	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a positive state (refer to driver waveform, figure 4).
38	Manchester	MANOUT	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a negative state (refer to driver waveform, figure 4).
39	Ground	GND	Ground

FUNCTIONAL DESCRIPTION

The COM1553B is organized into the following five sections:

Manchester Encoder/Decoder

This section performs the manchester encoder and decoder functions and code error check. The receiver continuously monitors the MANIN and the $\overline{\text{MANIN}}$ input lines for a valid sync. After the reception of the 3 bit sync, the receiver is in full synchronization. It then checks for transition errors and correct (odd) parity. If an error is detected in the Command Word the receiver resets itself, pulses IM and waits for another valid sync. If any errors are detected in Data and Status Words, the appropriate error bits in the Status and Error register are set.

The transmitter section encodes the NRZ data from the data bus into Manchester II and appends, depending on word type, the proper sync and parity.

State Sequencer Logic

The State Sequencer section generates the appropriate signals to various internal sections to control the overall device operation.

Inputs to the State Sequencer which establish its operational modes are as follows:

Remote Terminal/Bus Controller (RT/$\overline{\text{BC}}$)

Determines whether the data terminal is operating as a Remote Terminal or as a Bus Controller. As a result of Dynamic Bus Allocation, any terminal shall be capable of performing either function at different times.

Command Control Code bits D2-D0 (CB2-CB0)

These Command Control Code bits determine the type of memory operation the COM1553B will execute. Transfer of these commands to the COM1553B are initiated by asserting Strobe Command ($\overline{\text{CSTR}}$) low. This informs the COM1553B that a command is available in external memory. When the COM1553B acknowledges the $\overline{\text{CSTR}}$ signal, it sets the $\overline{\text{CSTRA}}$ output low. The $\overline{\text{CSTR}}$ must be reset within 1.5 μs after $\overline{\text{CSTRA}}$. The COM1553B then initiates a memory read cycle by setting R/$\overline{\text{W}}$ high, C/$\overline{\text{D}}$ low, and DATA TRANSFER REQUEST ($\overline{\text{DTR}}$) low. When the Command Control Code bits are valid on the bidirectional data bus (D2-D0), $\overline{\text{DTACK}}$ and $\overline{\text{BGACK}}$ are generated by the processor and these bits are loaded into the COM1553B 3-bit latch decode register. The command is then decoded in accordance with Table A. Timing associated with loading these control bits into the COM1553B is shown in Figure 1.

Transmit Last Command

Allows the State Sequencer to bypass a memory read cycle to external memory and transmit the Last Command from the TRLC register following the Status Word transmission.

Broadcast

When the address field of the Command Word is all ones (11111), the State Sequencer is informed that a Bus Controller or a Remote Terminal is transmitting a Broadcast Command.

Word Count Zero

Input from the 5-bit counter and count decode logic informing the State Sequencer that all Data Word memory cycles are complete.

Sync Input

Indicates the type of sync word just strobed into the receive register.

Address Compare

When programmed as a Remote Terminal, the COM1553B compares the contents of the address register with the address field of the received Command Word. If the addresses compare, the State Sequencer will respond to the received command.

Any Error

This input to the State Sequencer indicates that one of the seven possible errors have been set in the error register at the end of a message (Refer to Error register).

Contiguous Word

Set if there is a transition 2 μs. after the parity transition of the last word, this signifies that a contiguous word follows the word presently in the receive register (Refer to figure 5).

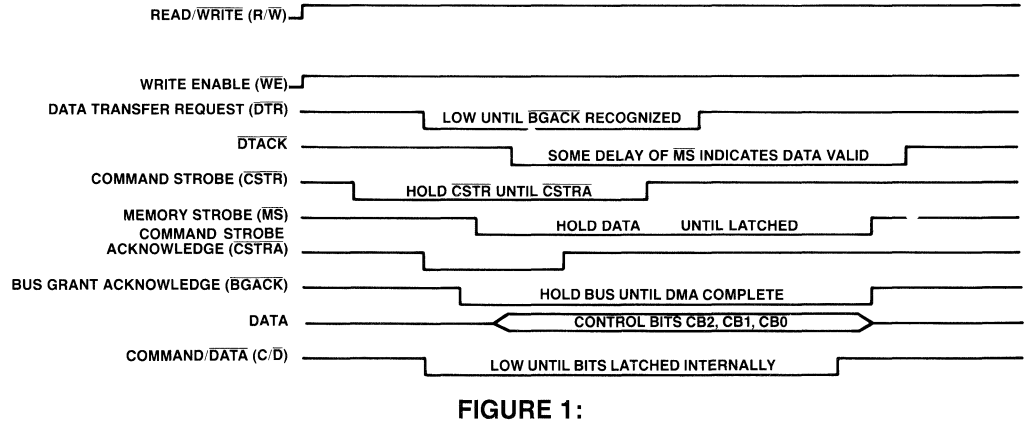


FIGURE 1:
BUS CONTROLLER TIMING SEQUENCE

Loading the Command Control Code Bits into the COM1553B prior to transmitting a Command or initiating a Diagnostic Sequence.

Error Detection Logic

The error detection logic of the COM1553B detects the following errors:

Improper Sync

One or more words have been received with incorrect sync polarity (For example a Status Word with Data Sync).

Invalid Manchester II Code

One or more words have been received with a missing transition during the 17 μs. data and parity bit time.

Information Field Greater Than 16 Bits

The decoder has detected a transition within one bit time (1 μs.) following the parity bit in one or more words.

Odd Parity Error

One or more words have been received with a parity error.

Improper Word Count

An improper word count error occurs when the number of Data Words received is not equal to the number of words indicated in the word count field of the Command Word. In the case of a Mode Code without data, no Data Words should follow the Mode command. Mode Codes with data should consist of only one Data Word. If the contents of the word counter are not zero, and there is no contiguous Data Word, then the receive message is considered incomplete (e.g., fewer words were received than indicated by the word count in the Command word). If the contents of the word counter are zero and there is a transition detected 2 μs. after the parity transition of the last Data Word, then this also will cause an improper word count. In either case, the Message Error bit of the Status Word is set and not transmitted and the invalid message ($\overline{IM}$) output pin pulsed at the same time as the message complete ($\overline{MC}$) signal output.

Response Time

The amount of time between the end of transmission of a Command or Data Word and the Status Word reply by a Remote Terminal should be less than 14 μs. If the response is greater than 14 μs. the response error bit is set in the error register.

Address Mismatch

An address mismatch occurs when a Bus Controller detects a mismatch between the address of the Status Word reply from a Remote Terminal and the Remote Terminal address of the Command.

Internal Register Description

Remote Terminal Address And Status Code Register

This register is loaded when the processor issues a load Remote Terminal Address (RTA) command. The word that is loaded in this register consists of 9 bits of status information (D0-D8) and the 5-bit address (D11-D15). The Remote Terminal Address may be checked any time by reading out the Error register. The RTA and Status Code register must be loaded before the COM1553B may respond as a Remote Terminal.

Table 1 defines the data bus bits which correspond to the Remote Terminal Address and Status Code register and Status Word that transmitted. Bits D0, D2, D3 and D8 are double buffered to allow the RT to retain this information after the Status Code register is updated. For all legal commands, other than Transmit Last Status and Transmit Last Command Mode command, the Status Word register is updated with these four bits, Any Error and the Broadcast flag. The Dynamic Bus Control and Terminal Flag bits are modified by the appropriate Mode Code commands whereas, the Broadcast Flag and Any Error bits are set by the COM1553B internal logic. The Reserved Bits and the RT address bits are transferred directly into the Status Word register during the RTA and Status Code command.

Bits D0, D2, D3, and D5-D9 are cleared after transmission for all commands except Transmit Last Status and Transmit Last Command Mode Code.

TABLE A:
COMMAND CONTROL CODE BIT DEFINITION

	DATA BITS													CONTROL BITS CB2-CB0			
RT/$\overline{BC}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	FUNCTION
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	READ DATA REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	LOAD RT ADDRESS REGISTER AND STATUS CODE REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	READ LAST CMD
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	READ ERROR AND REMOTE TERMINAL ADDRESS REGISTERS
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	BUS CONTROLLER TRANSMISSION
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	BUS CONTROLLER RT TO RT TRANSFER

X—DON'T CARE

TABLE 1

Data Bus Bit	RTA and Status Code Reg. Bits	Internal Logic Signals	Status Word Transmitted
D15 (MSB)	RTA Bit 4 (MSB)	—	RTA Bit 4 (MSB)
D14	RTA Bit 3	—	RTA Bit 3
D13	RTA Bit 2	—	RTA Bit 2
D12	RTA Bit 1	—	RTA Bit 1
D11	RTA Bit 0 (LSB)	—	RTA Bit 0 (LSB)
D10	Not used	Any Error	Message Error
D9	Instrumentation Bit	—	Instrumentation
D8	Service Request Bit	—	Service Request
D7	Reserved	—	Reserved
D6	Reserved	—	Reserved
D5	Reserved	—	Reserved
D4	Not Used	Broadcast Flag	Broadcast Flag
D3	Busy	—	Busy
D2	Subsystem Flag Bit	—	Subsystem Flag
D1	Dynamic Bus Control Acceptance Enable Bit (See Note)	Dynamic Bus Mode Code command	Dynamic Bus Control Bit
D0 (LSB)	Terminal Flag Enable Bit (See Note)	Inhibit Terminal Flag (set) or Override Terminal Flag (reset) Mode Code command	Terminal Flag

Note: When the Dynamic Bus Control Acceptance Enable bit is set, the RT will accept a Dynamic Bus Mode code request. If this bit is reset the RT will reject a Dynamic Bus Mode Code command request. The Terminal Flag Bit (if enabled) is only set high if no Inhibit Terminal Mode Code command has been received, or if an Override Inhibit Terminal bit command is received.

Last Command Word Register

The last valid Command Word received by a Remote Terminal is stored in an internal 16 bit Last Command Register. This makes it readily available for transmission onto the data bus whenever the Remote Terminal receives a Mode Command to transmit the last Command Word. The Last Command Register contents are automatically written into external memory following a receive or a transmit message.

As a bus controller (BC), the Last Command Register is used to hold the command transmitted before the present command. In RT-RT transfers this register of the BC holds the receive command while the transmit command is being transmitted.

The processor has the option of reading the Last Command Register of either a bus controller or remote terminal, by issuing a Read Last Command Register command code.

Error Register And RTA Register (Error Register)

A 7-bit error register is provided in the COM1553B to hold any errors associated with the previous message. If one or more of the 7 error types exists, the COM1553B asserts the Invalid Message output pin ($\overline{IM}$) at the same time that Message Complete ($\overline{MC}$) is asserted, cueing either a Remote Terminal or a Bus Controller that an error occurred in the previous message. If desired, the processor may read out the 16-bit error word by issuing a read error register command code. When operating as a Remote Terminal, the COM1553B will write the Receive register, Error register and Last Command register automatically into external memory at the end of each command message because these registers may change before the processor has determined the necessity of reading them. The Error register may be read anytime during a message except during message transfers.

TABLE 2

The 16-bit error word is defined as follows:

DATA BUS LINE	ERROR BIT DEFINITION
D15	RT Address Bit 4
D14	RT Address Bit 3
D13	RT Address Bit 2
D12	RT Address Bit 1
D11	RT Address Bit 0
D10	Unused
D9	Improper Sync
D8	Address Mismatch Error
D7	Improper Word Count
D6	Response Time Error
D5	Information Field > 16 Bits
D4	Unused
D3	Invalid Manchester II
D2	Parity Error
D1	Unused
D0	Unused

*Unused bits are set high.

Mode Detection Logic

Both receive and transmit Command Words for a Remote Terminal and Bus Controller are decoded by the Mode Detection Logic. The Mode Detection Logic examines the following Command Word field to establish the correct operating mode for the COM1553B (Refer to TABLE B).

Subaddress/Mode Code Field (D5-D9) and Data Word Count/Mode Code (D0-D4)

This field Determines if the command is a normal command or a Mode command. A subaddress field of 00000 or 11111 implies a Mode command. All other codes are interpreted as a subaddress. Once a Mode Command is detected the most significant bit of the Data Word Count/Mode Code field is decoded. A most significant bit of "zero" implies no associated data with the Code Command. A "one" in this position implies that a Data Word will follow.

The COM1553B recognizes five Mode Code commands (Refer to TABLE B). Transmit Last Command or Transmit Last Status word Mode Code commands, when received by the COM1553B, will automatically transfer the contents of the Transmit Last Command or Transmit Last Status register onto the 1553B serial bus.

The Override/Inhibit Terminal Flag and Dynamic Bus Control Mode Code commands, when received by the COM1553B, may change the state of the Terminal Flag and Dynamic Bus Control bits of the Status Word register. The Inhibit Terminal Flag Bit Mode Code command resets the Terminal Flag bit.

The Override Inhibit Terminal Flag Mode Code command enables the Terminal Flag bit if it was previously disabled. Finally, Dynamic Bus Control Mode Code command sets the Dynamic Bus Control bit in the Status Word if the Dynamic Bus Control Enable bit is high. If the enable bit is low, the Dynamic Bus Control bit in the Status Word remains low when a Dynamic Bus Control Mode Code command is received.

Broadcast Mode Code

Broadcast Mode Code Commands are acknowledged if the T/$\overline{R}$ bit is low. If the T/$\overline{R}$ bit is high all Broadcast Mode Code commands without associated Data words are acknowledged except Dynamic Bus Control and Transmit Last Status Word.

Illegal Broadcast Commands are not acknowledged; the IM output pin is, however, pulsed low.

TABLE B
MODE CODE DEFINITION

FUNCTION	DETECT CONDITION	DETECTED BY	SPECIAL CONDITIONS	COMMENTS
Broadcast	All ones in RT address field of CMD WD	Broadcast Decode Logic	Status word is written into Memory but not transmitted	Address compare must recognize all ones as Broadcast
Mode Codes	All zeros or ones in sub-address field of CMD WD	Mode Code Decode Logic	MSB of Word Count 0 = No data Word 1 = With Data Word	Word Count is Decoded as mode code
(1) Dynamic Bus Control			Word Count Field = 00000	Dynamic Bus Accept Bit of Status word enabled for transmission
(2) Transmit Last Status Word			Word Count Field = 00010	Status Word remains unchanged
(3) Inhibit Terminal Flag Bit			Word Count Field = 00110	Terminal Flag Bit of Status word inhibited until overriden
(4) Override Inhibit Terminal Flag Bit			Word Count Field = 00111	Removes Inhibit from Terminal Flag Bit of Status Word
(5) Transmit Last Command			Word Count Field = 10010	Status Word Transmitted followed by Last Command Register. Status Word remains unchanged.

OPERATION

When operating as either a Bus Controller or Remote Terminal, the COM1553B decodes the Command Word and determines the type of message transfer. Having determined the type of message transfer, the COM1553B generates the proper control and timing signals to complete the transfer (refer to Figure 2). The types of messages are listed below:

1) Bus Controller to Remote Terminal
2) Remote Terminal to Bus Controller
3) Remote Terminal to Remote Terminal
4) Mode Code without Data Word
5) Mode Code with Data Word (transmit)
6) Mode Code with Data Word (receive)
7) Broadcast Bus Controller to Remote Terminal
8) Broadcast Remote Terminal to Remote Terminal
9) Broadcast Mode Code without data
10) Broadcast Mode Code with data

Bus Controller Transaction (RT/$\overline{BC}$ of the COM1553B set low)

The following section describes each 1553B information transfer format from the Bus Controller viewpoint. A table showing external memory operation is also provided for each message format.

Note that all MIL-STD-1553B serial bus activity is initiated by the Bus Controller.

Bus Controller-to-Remote Terminal Transfer (BC to RT)

This message format covers transactions where the Bus Controller transmits a receive Command and Data Words to a Remote Terminal. Initializing the COM1553B is accomplished by the processor loading an external memory address counter with the starting address of the COM1553B memory control block (address where the Command Control Code CB2-CB0 resides). The Bus Controller processor next issues a Command Strobe ($\overline{CSTR}$) and holds it low until the COM1553B issues a Command Strobe Acknowledge ($\overline{CSTRA}$). The COM1553B then responds with a Data Transfer Request ($\overline{DTR}$) which initiates a normal memory cycle.

Refer to figure 1 for timing associated with loading the Command Control Codes (CB2-CB0) into the COM1553B prior to transmitting the Command Word.

The first memory cycle loads the Command Control Code bits CB2-CB0 from external memory into the COM1553B functioning as Bus Controller (BC). The BC decodes this command to determine the type of memory transaction to perform (refer to TABLE A). The next read cycle loads the Command Word into the BC command register and then transmits it onto the 1553B bus. This Command Word, while in the command register, determines the BC mode of operation. The BC then completes this BC to RT transaction by issuing a predetermined number of read cycles (determined by the value in the word count field of the Command Word) and transmitting the data onto the 1553B bus. After transmission of the last Data word, the BC initializes its response timer, expecting a Status Word from the remote terminal within 14 μs.

After the reception of the Status Word, the BC initiates a memory write cycle which writes the Status Word into the external memory. If the BC doesn't receive the Status Word within the allowed response time the message error bit is set.

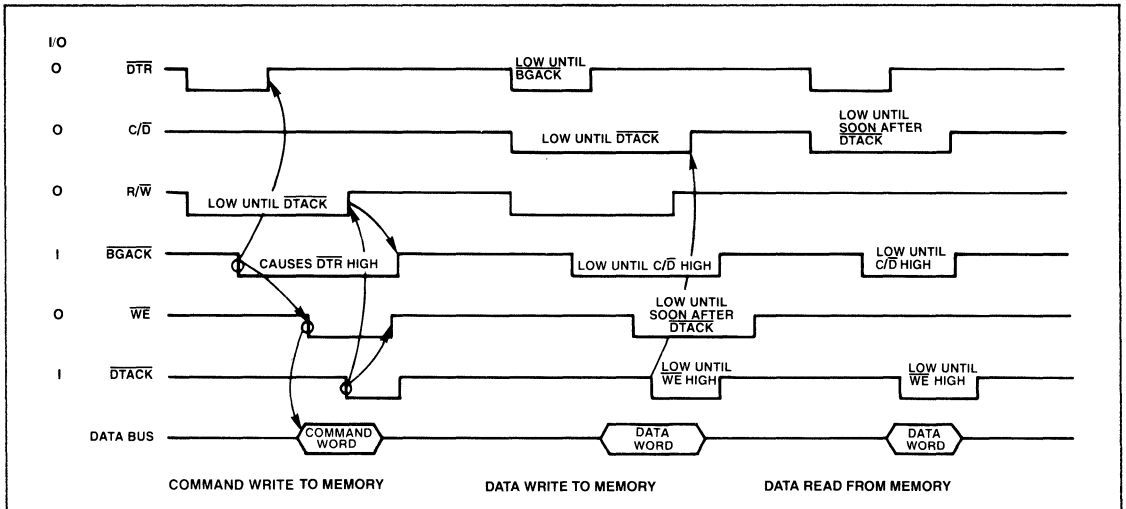


FIGURE 2

TABLE 3
BC to RT (The BC transmits a receive command to the RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ
	**	
35	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Remote Terminal Transfer to Bus Controller

This message format covers transactions where the Bus Controller sends a transmit command to a Remote Terminal and requests data from it. Initialization of the BC for normal memory cycles is the same as the previous transfer. The difference between this transfer and the previous transfer is that after the Command Word is transmitted, the BC waits 14 μs for the Status Word and the requested number of Data Words. The Status and Data Words are written into external memory via write cycles as they are received by the BC.

TABLE 4
BC to RT (The BC transmits a Transmit Command to an RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	TRANSMIT COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
35	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

RT-to-RT Transfer

In this message format, the Bus Controller first issues a receive Command Word to the receiving Remote Terminal, followed by a transmit Command Word to the transmitting terminal. Next, the transmitting RT responds with a Status Word and the requested number of Data Words to both the receiving RT and BC. The receiving RT at the end of the message sends a Status Word to the BC. As Status and Data Words are received by the BC they are written into external memory.

TABLE 5
RT to RT

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
4	STATUS (transmitting RT)	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE
	**	
37	STATUS (receiving RT)	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Code Command without Data

The Bus Controller transmits a specific Mode Command and expects a Status Word back from the addressed Remote Terminal.

TABLE 6

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Command with Data (BC receives a single word)

In this mode the Bus Controller issues a transmit Mode Command to an RT. The addressed Terminal responds to the Bus Controller with a Status Word and a single Data Word.

TABLE 7

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Command with Data
(BC transmits a single word)

The Bus Controller issues a receive Mode Command and one Data Word to a Remote Terminal. A Status Word is returned by the Remote Terminal to the Bus Controller.

TABLE 8

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
3	DATA	READ
	**	
4	STATUS	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

Bus Controller (Broadcast) to Remote Terminal Transfer

In this mode the Bus Controller issues a Broadcast Command followed by a number of Data Words. In all Broadcast Command transfers a BC will not expect to receive a Status Word back.

TABLE 9

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ

*reads command control code bits CB2-CB0
**response time
X = don't care

RT to RT Transfer (Broadcast)

This transfer is similar to the normal RT to RT transfer with the exception that the Status Word is not returned by the receiving RT.

TABLE 10

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
	**	
4	STATUS	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

THE FOLLOWING NOTE APPLIES TO THE CURRENT VERSION OF THE COM 1553B:

When operating as a Bus Controller in a RT (Remote Terminal) to RT transfer, the COM1553B may incorrectly set the Invalid Sync Bit in the Error Register if the status word response from the receiving RT occurs between 4 and 7 microseconds.

The Bus Controller (BC) may confirm that an error free message transmission occurred by requesting that the receiving RT transmit the last status word. If this status word matches the previous status word, then an error-free transmission occurred.

Remote Terminal Transaction (RT/$\overline{BC}$ input of the COM1553B set high)

The following section addresses each COM1553B information transfer format from the Remote Terminal viewpoint.

Bus Controller to Remote Terminal Transfer
(BC to RT, where RT receives data)

In this transfer the COM1553B designated as the RT receives a command to receive data. As the Command Word is completely shifted into the receive shift register, the RT compares the Command Word address field with the preloaded Remote Terminal address. This determines if the message is addressed to the receiving RT. If the Command Word is valid, the RT issues a Data Transfer Request ($\overline{DTR}$) to initiate a memory cycle. Once the processor relinquishes control of the data bus, during the Bus Acknowledge ($\overline{BGACK}$) time, the Command Word is placed on the data bus.

The Subaddress field is thereafter decoded by external logic and the Command word is written into external memory. The RT then receives a predetermined number of Data Words (specified by the word count field). As each Data Word is received it is written into external memory. After the reception of the last Data Word the RT transmits the Status Word, the Message Error, Broadcast Flag, Terminal Flag, Subsystem Flag, Busy, and Service Request bits are updated for all commands except for the Transmit Status Word and Transmit Last Command Code commands. While transmitting the Status, the RT writes it into memory. The RT also writes the Last Command Register, Error Register and Receive Register into memory and then asserts Message complete.

Note that the receive register of the RT will contain the transmitted Status Word.

TABLE 11
BC TO RT (RT receives data from BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	DATA	WRITE
•	•	WRITE
•	•	WRITE
34	DATA **	WRITE
35	STATUS	WRITE
36	LAST COMMAND	WRITE
37	ERROR REGISTER	WRITE
38	RECEIVE REGISTER	WRITE

Remote Terminal-to-Bus Controller Transfer (RT transmits data to BC)

The Remote Terminal receives a Transmit Command Word from the Bus Controller. The RT will then proceed to decode the Command Word, as in the previous case and within the response time transmits the Status Word.

While the Status Word is being transmitted the RT issues a write memory cycle to write the Status Word into external memory. Thereafter, the Data words are read from memory and transmitted. After the last word is transmitted the RT writes the contents of the Last Command Register, Error Register and the Receive Register into memory.

TABLE 12
Remote Terminal to Bus Controller (RT Transmits Data to BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND **	WRITE
2	STATUS	WRITE
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ
35	LAST COMMAND	WRITE
36	ERROR REGISTER	WRITE
37	RECEIVE REGISTER	WRITE

** response time

Remote Terminal-to-Remote Terminal Transfers

From the Remote Terminal viewpoint, RT-to-RT transfers are similar to the RT to BC receive or transmit data transfers. The only exception is that the receiving terminal waits for the first Data Word from the transmitting terminal. This satisfies the protocol requirement that the transmitting terminal first send its status to the controller before it transmits the data to the receiving terminal.

Mode Command with Data (RT receives a Mode Code Command to transmit)

In this transfer, after the Transmit Mode Command is received, the RT transmits the Status and one Data Word.

TABLE 13

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND **	WRITE
2	STATUS	WRITE
3	DATA	READ*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

*For a Transmit Last command Mode Code, Data is not read from memory but transmitted from the internal Last Command register.

** response time

Mode Code Command with Data (RT receives a Mode Command to receive)

This transfer is similar to a Receive Command having only one Data Word.

TABLE 14

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA **	WRITE
3	STATUS	WRITE
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

** response time

Bus Controller Broadcast Transfer to RT

The RT receives a Broadcast Command to receive data. If data received during a broadcast message is invalid, the COM1553B will set the message error bit.

TABLE 15
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
32	DATA	WRITE
33	STATUS	WRITE*
34	LAST COMMAND	WRITE
35	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command with Data

This Broadcast Mode Code command is detected if the MSB of the word count field is a logical high.

Transmission of the Status Word is suppressed as in the previous case but is loaded into external memory.

TABLE 16
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	STATUS	WRITE*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command Without Data

This Mode Code command is detected if the MSB of the word count field is zero. This transaction is the same as the previous transfer except that there is no Data Word transfer.

TABLE 17

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	STATUS	WRITE*
3	LAST COMMAND	WRITE
4	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast RT to RT Transfer

For this message transfer a Broadcast Command to receive is issued by the Bus Controller. This is followed by a normal Transmit Command to the transmitting Remote Terminal. The Remote Terminal responds with a normal transmit message format of Status Word and Data Word(s). The receiving terminals do not transmit a Status Word after receiving the data. However, they do go through a memory cycle to load the Status Word into their respective memories.

For the Remote Terminal receive transfer refer to Table 15. The only difference in this transfer is that there is a gap time between the Command and Data word.

For the Remote Terminal transmit transfer refer to Table 12. The only difference in this transfer is that the Receive Register is not written into memory.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −55 to +125°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... +15V
Negative Voltage on any pin except VBB, with respect to ground ..... −.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = -55$ to 125°C, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	3		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = -3.2$ mA
V_{OH}	Output High Voltage	2.4	4	5	V	$I_{OH} = .8$ mA
I_L	Input Leakage Current			10	μA	
C_{IN}	Input Capacitance		10	25	pf	
C_o	Output Capacitance		10	15	pf	
C_L	Load Capacitance		100	150	pf	
P_W	Power Dissipation		0.8		W	$T_A = 25$°C
I_{DD}				40	mA	
I_{CC}				100	mA	
I_{BB}				5	mA	

AC ELECTRICAL CHARACTERISTICS

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
clk	clock frequency		12		MHz	50% duty cycle
t_r	Clk, rise time		6		ns	
t_f	Clk, fall time		6		ns	
t_1	$\overline{DTR}$ and $\overline{WE}$	0.5	0.6	1	μs	
t_2	$\overline{BGACK}$ to $\overline{DTR}$	0.8	1.3	2	μs	
t_3	$\overline{WE}$ to DATA	50	100		ns	
t_4	$\overline{DTACK}$ to $\overline{WE}$		1.5	2	μs	
t_5	$\overline{DTACK}$ to R/$\overline{W}$		1	1.5	μs	
t_6	$\overline{DTACK}$ to C/$\overline{D}$		1.5	2.5	μs	
t_7	$\overline{CSTR}$ to $\overline{CSTRA}$			673	μs	
t_8	$\overline{CSTRA}$ to $\overline{CSTR}$			1.5	μs	
t_9	$\overline{CSTRA}$ width		500		ns	
t_{10}	C/$\overline{D}$ to DATA	0				
t_{11}	CMD to IM			3.25	μs	
t_{12}	IM width			500	ns	
t_{13}	VC width			1	μs	
t_{14}	VC to IM			1.75	μs	
t_{15}	C/$\overline{D}$ to MC			700	ns	
t_{16}	C/$\overline{D}$ to IM			2.25	μs	
t_{17}	C/$\overline{D}$ to MC			750	ns	
t_{18}	C/$\overline{D}$ to MC			1.25	μs	
t_{19}	CMD to MCF reset			3.75	μs	
t_{20}	CMD to MCF set			4.75	μs	
t_{21}	CMD to VC			2.75	μs	
t_{22}	C/$\overline{D}$ to MCF reset			1.5	μs	
t_{23}	C/$\overline{D}$ to MCF set			1	μs	
t_{24}	POR width	2.5			μs	
t_{25}	Receive CMD to $\overline{DTR}$			4.25	μs	
t_{26}	Transmit CMD to $\overline{DTR}$			5.75	μs	

FIGURE 3:
RECEIVER LOGIC WAVEFORMS

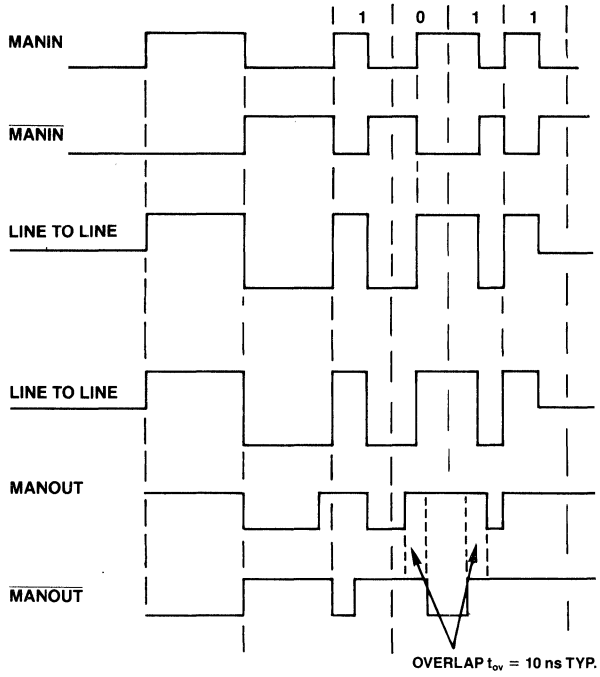
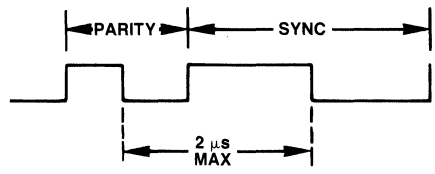
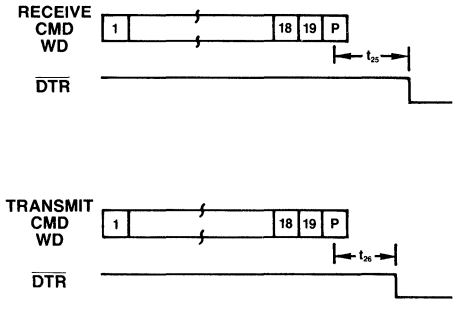


FIGURE 4:
DRIVER LOGIC WAVEFORMS

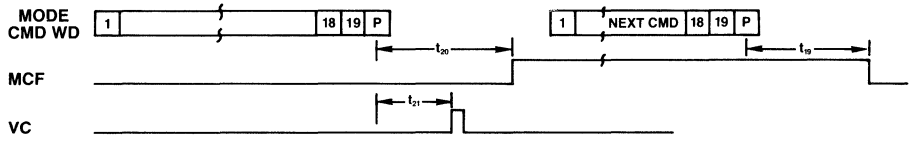
FIGURE 5:
CONTIGUOUS WORD



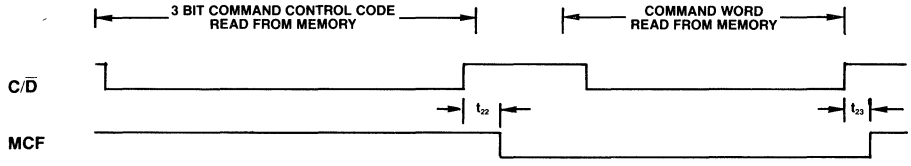
$\overline{\text{DTR}}$ VS COMMAND WORD



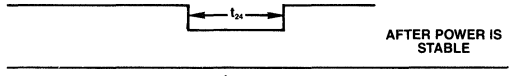
MODE CODE FLAG (MCF)
AS A RT



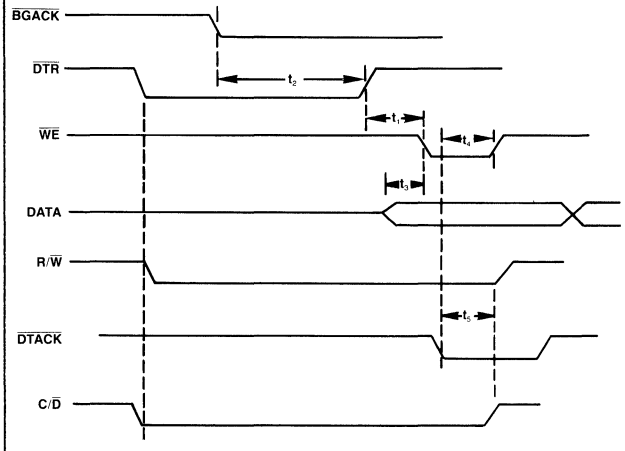
AS A BC



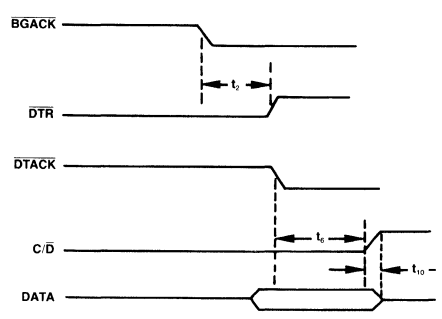
POR

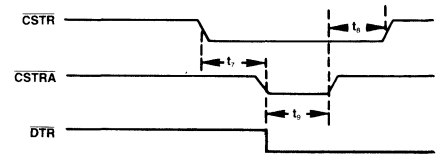


AC CHARACTERISTICS

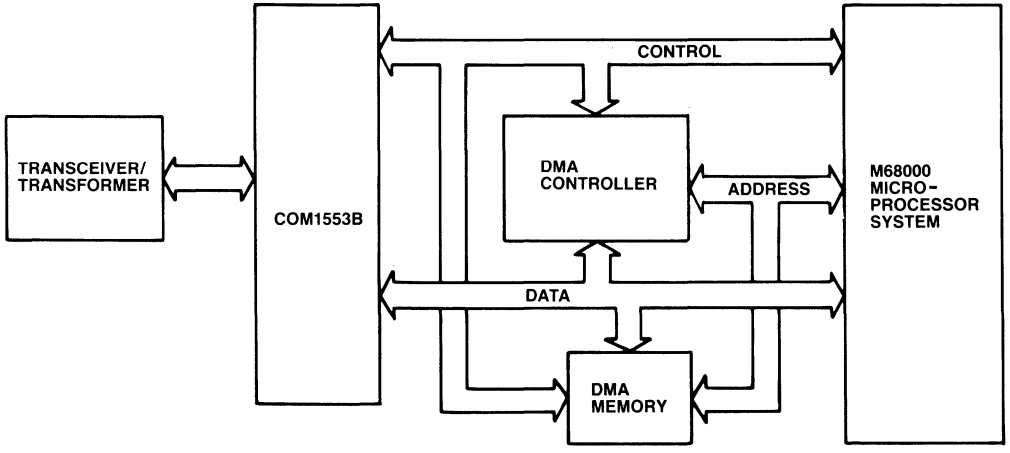


WRITE CYCLE





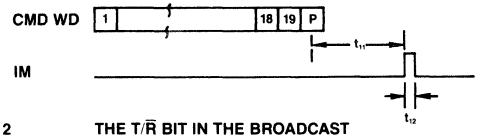
READ CYCLE



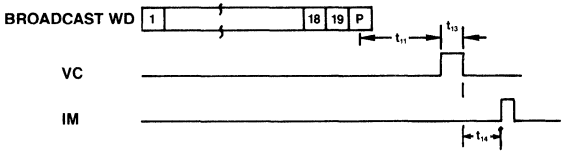
TYPICAL SYSTEM IMPLEMENTATION

INVALID MESSAGE (IM) AS A RT

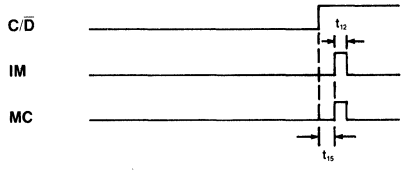
CASE 1



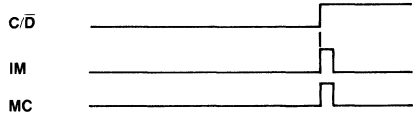
CASE 2 THE T/$\overline{R}$ BIT IN THE BROADCAST CMD IS SET HIGH.



CASE 3 AN ERROR OCCURRED DURING A BROADCAST CMD

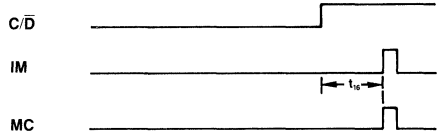


CASE 4 NON BROADCAST CMD



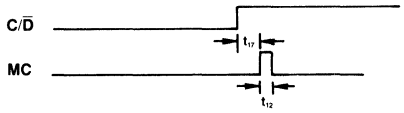
AS A BC

CASE 5 A TRANSMIT OR RECEIVE BC TRANSFER

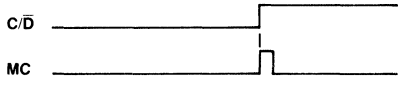


MESSAGE COMPLETE (MC) AS A RT

CASE 1 AT THE COMPLETION OF AN ERROR FREE BROADCAST COMMAND TRANSACTION AFTER THE ERROR REGISTER IS WRITTEN INTO MEMORY.

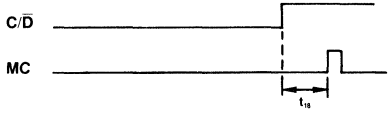


CASE 2 AT THE COMPLETION OF A TRANSMIT OR RECEIVE COMMAND TRANSACTION AFTER THE DATA REGISTER IS WRITTEN INTO MEMORY.



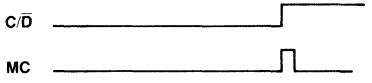
AS A BC

CASE 3 WHEN THE BC ISSUES A RECEIVE COMMAND, THE MC SIGNAL OCCURS AFTER THE STATUS WORD IS WRITTEN INTO MEMORY.
OR
WHEN THE BC ISSUES A TRANSMIT COMMAND, THE MC SIGNAL OCCURS AFTER THE LAST DATA WORD IS WRITTEN INTO MEMORY.

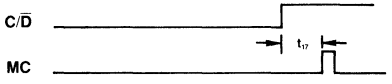


AS A BC OR RT

CASE 4 AT THE COMPLETION OF LOADING THE RT ADDRESS REGISTER OR READING THE DATA REGISTER.



CASE 5 AFTER READING THE ERROR REGISTER.



NOTE: Message complete and invalid message outputs of the COM 1553B are negative pulses i.e. $\overline{MC}$ and $\overline{IM}$.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM1671
μPC FAMILY

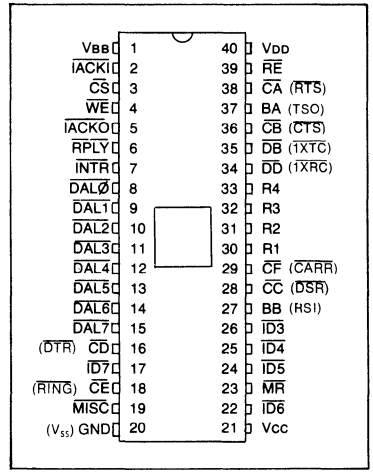
Asynchronous/Synchronous Transmitter-Receiver

ASTRO

FEATURES

- ☐ SYNCHRONOUS AND ASYNCHRONOUS
  - Full Duplex Operations
- ☐ SYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Two Successive SYN Characters Sets Synchronization
  - Programmable SYN and DLE Character Stripping
  - Programmable SYN and DLE-SYN Fill
- ☐ ASYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Selection
  - Start Bit Verification
  - Automatic Serial Echo Mode
- ☐ BAUD RATE—DC TO 1M BAUD
- ☐ 8 SELECTABLE CLOCK RATES
  - Accepts 1X Clock and Up To 4 Different 32X Baud Rate Clock Inputs
  - Up to 47% Distortion Allowance With 32X Clock
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data
  - 8-Bit Bi-Directional Bus For Data, Status, and Control Words
  - All Inputs and Outputs TTL Compatible
  - Up To 32 ASTROS Can Be Addressed On Bus
  - On-Line Diagnostic Capability
- ☐ ERROR DETECTION
  - Parity, Overrun and Framing

PIN CONFIGURATION



- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Pin for Pin replacement for Western Digital UC1671 and National INS 1671
- ☐ Baud Rate Clocks Generated by COM5036 @ 1X and COM5016-6 @ 32X

APPLICATIONS

Synchronous Communications
Asynchronous Communications
Serial/Parallel Communications

General Description

The COM1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO contains several "handshaking" signals to insure easy interfacing with modems or other peripheral devices such as display terminals. In addition, a programmable diagnostic mode allows the selection of an internal looping feature which allows the device to be internally connected for processor testing.

The COM1671 provides the system communication designer with a software responsive device capable of handling complex communication formats in a variety of system applications.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM 1863
COM 8018
μPC FAMILY

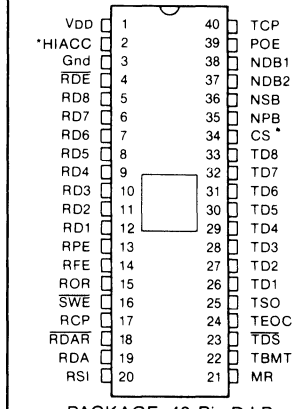
SECTION III

Universal Asynchronous Receiver/Transmitter UART

FEATURES

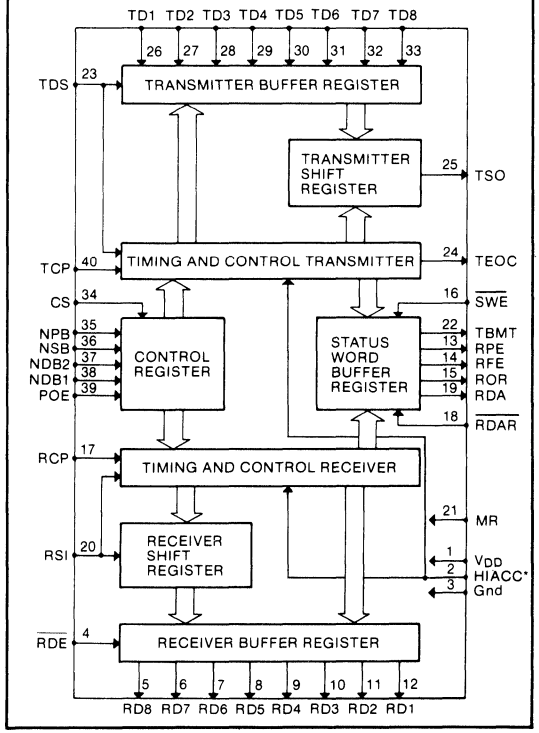
- ☐ Compatible with TR1863 timing
- ☐ High accuracy 32X clock mode: 48.4375% Receiver Distortion Immunity and improved RDA/ROR operation (COM 8018 only)
- ☐ High Speed Operation—62.5K baud, 200ns strobes
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Input pull-up options: COM 8018 has low current pull-up resistors; COM 1863 has no pull up resistors
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Improved Start Bit Verification—decreases error rate
- ☐ 46.875% Receiver Distortion Immunity
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ Master Reset—Resets all status outputs and Receiver Buffer Register
- ☐ Three State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic DIP Package—easy board insertion
- ☐ Baud Rates available from SMC's COM 8046, COM 8116, COM 8126, COM 8136, COM 8146 baud rate generators

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1 or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

*If pin 2 is taken to a logic 1 the COM 8018 will operate in a high accuracy mode. If pin 2 is connected to −12V, GND, a valid logic zero, or left unconnected, the high accuracy feature is disabled, and the UART will operate in a 16X clock mode. Pin 2 is not connected on the COM 1863.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

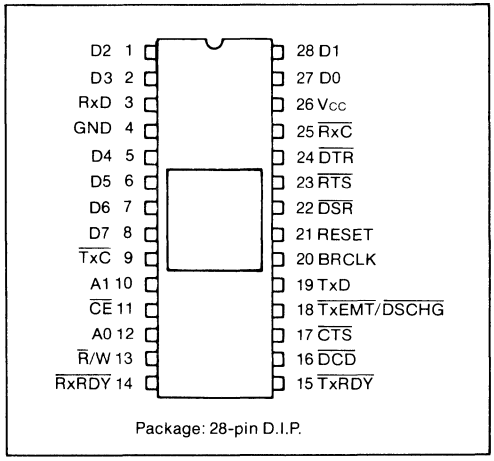
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

Programmable Communication Interface PCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC or DLE Stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)
- ☐ Double Buffering of Data

PIN CONFIGURATION



Package: 28-pin D.I.P.

- ☐ Internal or External Baud Rate Clock
  - —16 Internal Rates:50 to 19,200 Baud
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with 2651, INS2651

GENERAL DESCRIPTION

The COM 2651 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. The on-chip baud rate generator can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2651 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

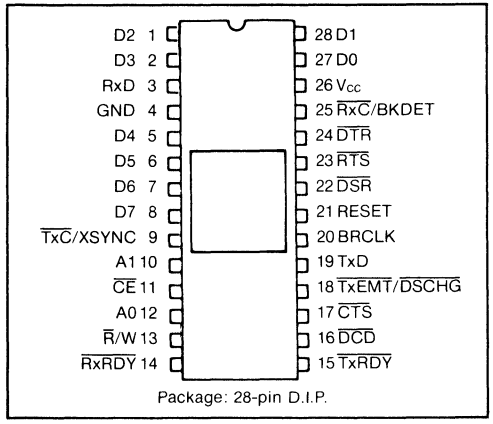
COM 2661-1
COM 2661-2
COM 2661-3
μPC FAMILY

Enhanced Programmable Communication Interface EPCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal or External Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Transparent mode DLE stuffing (Tx) and detection (Rx)
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC, DLE and DLE-SYNC stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters plus parity
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)

PIN CONFIGURATION



Package: 28-pin D.I.P.

- ☐ Double Buffering of Data
- ☐ RxC and TxC pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2661-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with EPCI 2661

GENERAL DESCRIPTION

The COM 2661 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is an enhanced pin and register compatible version of the COM 2651 that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2661 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2661 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

COM 5025
μPC FAMILY

Multi-Protocol Universal Synchronous Receiver/Transmitter

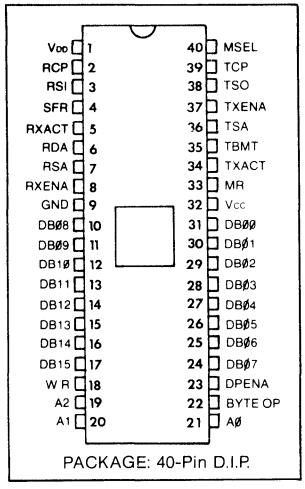
USYNR/T

SECTION III

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Three-state Input/Output BUS
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—1.5 M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP
- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP
- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Intelligent Terminals
- ☐ Line Controllers
- ☐ Network Processors
- ☐ Front End Communications
- ☐ Remote Data Concentractors
- ☐ Communication Test Equipment
- ☐ Computer to Computer Links
- ☐ Hard Disk Data Handler

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

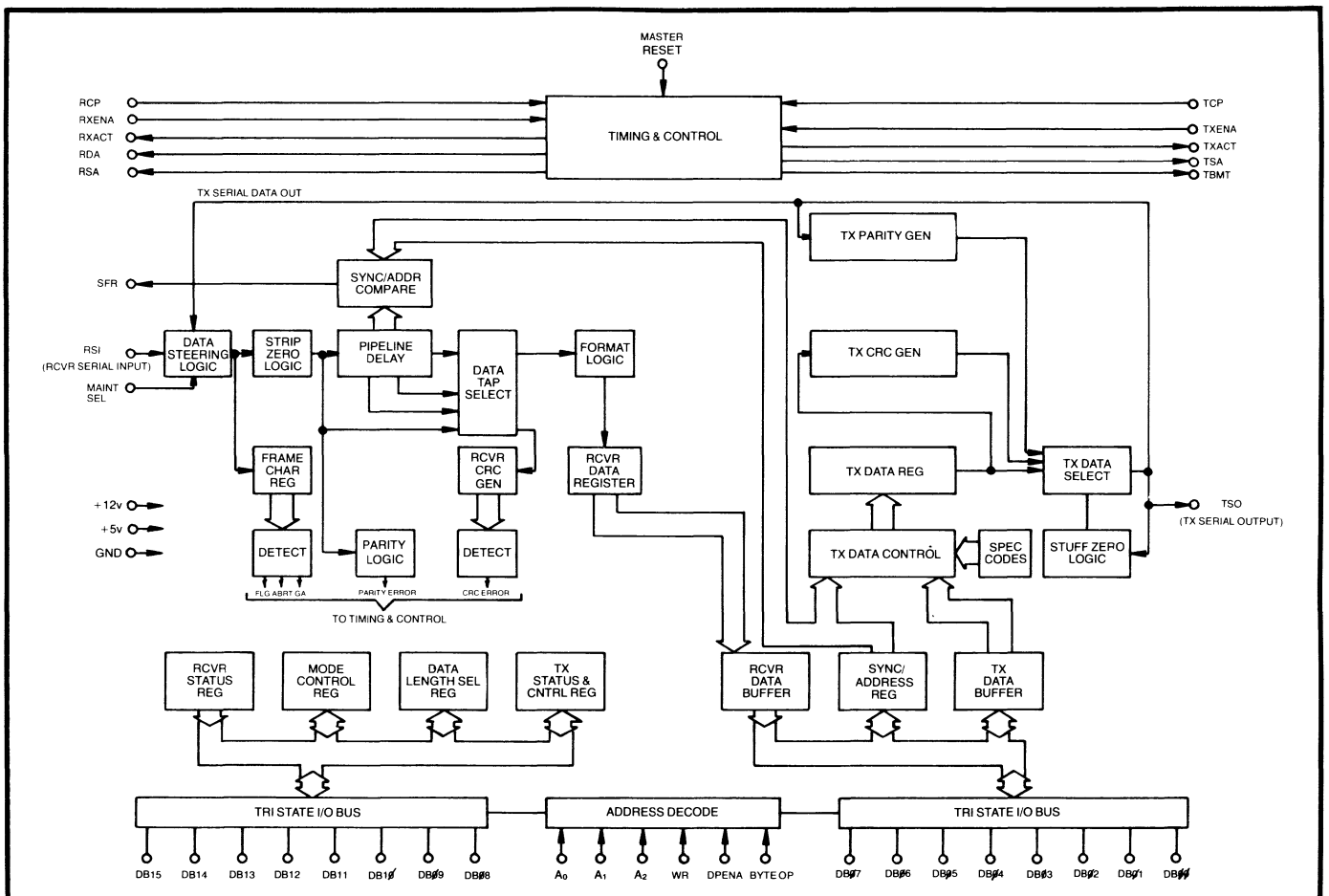
References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

Terminology

Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

BLOCK DIAGRAM



Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus.
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus.
				Wire "OR" with DBØØ-DBØ7 For 8 bit data bus
18	W/R	Write/Read	I	Controls direction of data port. W/R=1, Write. W/R=0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Buffer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO=1.

Definition of Terms
Register Bit Assignment Chart 1 and 2

Data Bu	Term	Definition	
DBØ8	RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.	Receiver Status Register
DBØ9	REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.	
DB1Ø	RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.	
DB11	ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.	
DB12-14	A, B, C	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).	
DB15	ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.	
DB8	TSOM	Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.	Transmitter Status and Control Register
DB9	TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line.	
DB1Ø	TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.	
DB11	TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.	
DB15	TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM.	
DB8-1Ø	X, Y, Z	Z Y X —W/R bits. These are the error control bits. 0 0 0 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "1" 0 0 1 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "0" 0 1 0 Not used 0 1 1 $X^{16}+X^{15}+X^2+1$—CRC16 1 0 0 Odd Parity—CCP Only 1 0 1 Even Parity—CCP Only 1 1 0 Not Used 1 1 1 Inhibit all error detection and transmission Note: Do not modify XYZ until both data paths are idle	Mode Control Register
DB11	IDLE	IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register.	
DB12	SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.	
DB13	STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.	
DB14	PROTOCOL	PROTOCOL—W/R bit. BOP=0, CCP=1	
DB15	*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.	
DB13-15	TXDL	Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode).	Data Length Select Register
DB8-1Ø	RXDL	Receiver Data Length—W/R bits. RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character	
DB11	EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1.	
DB12	EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1.	

*Note: Product manufactured before 1Q79 may not have this feature.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs=X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

* Note: Product manufactured before 1Q79 may not have this feature.

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

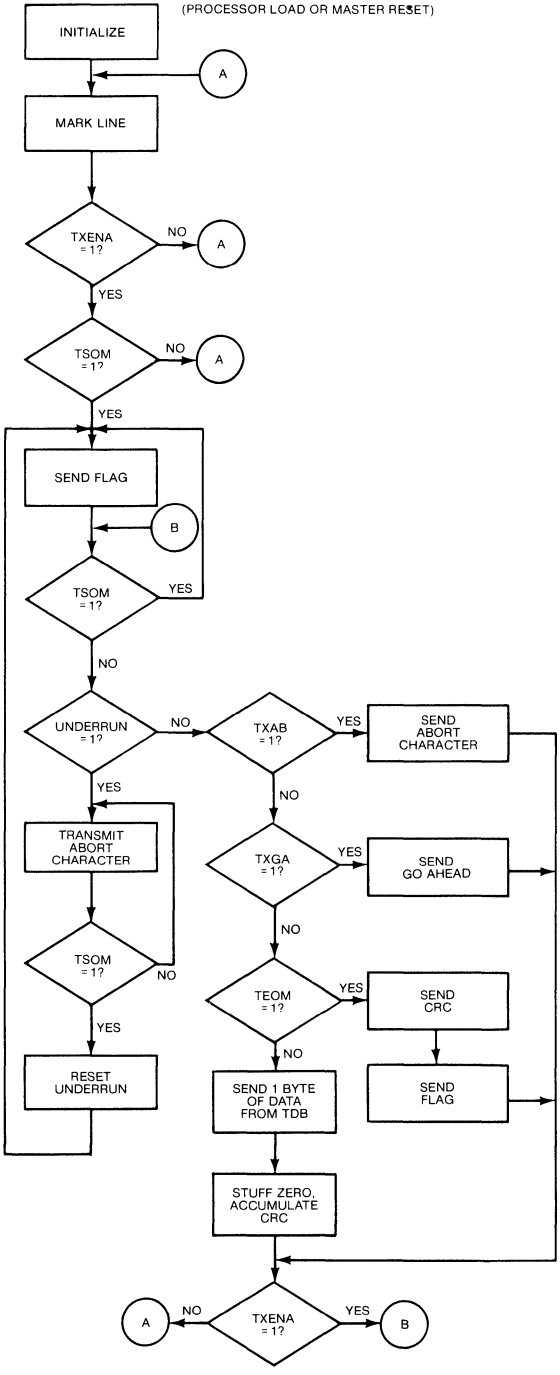
A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

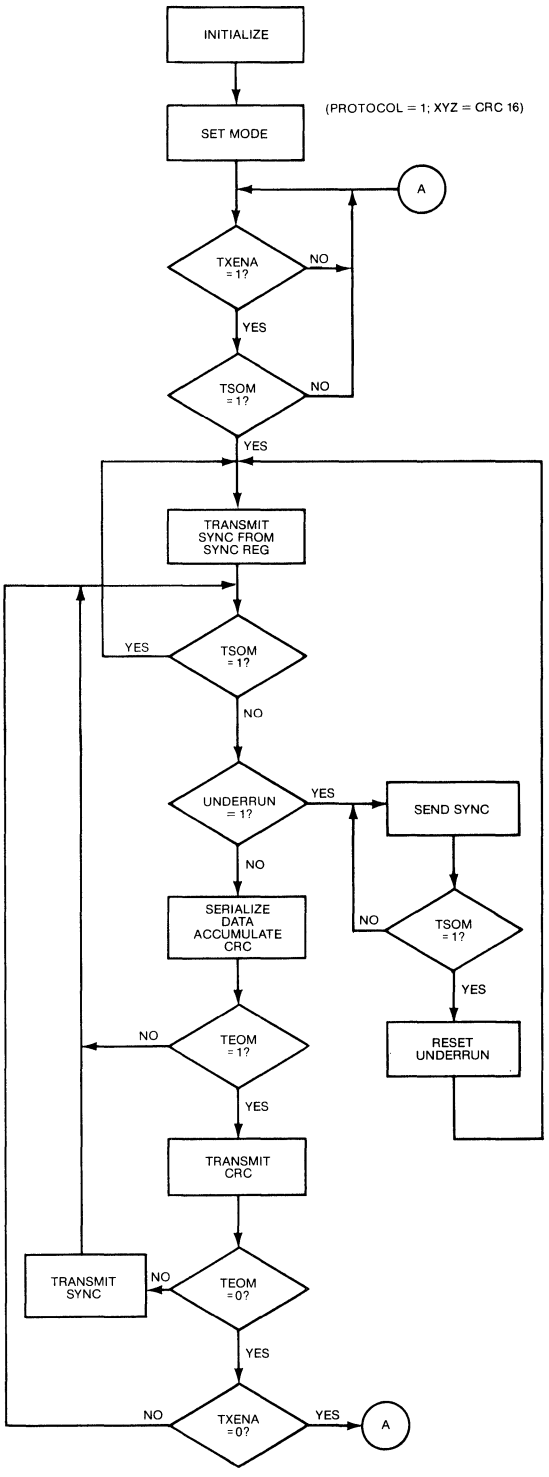
2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———————
1	1	1	Data Length Select Register

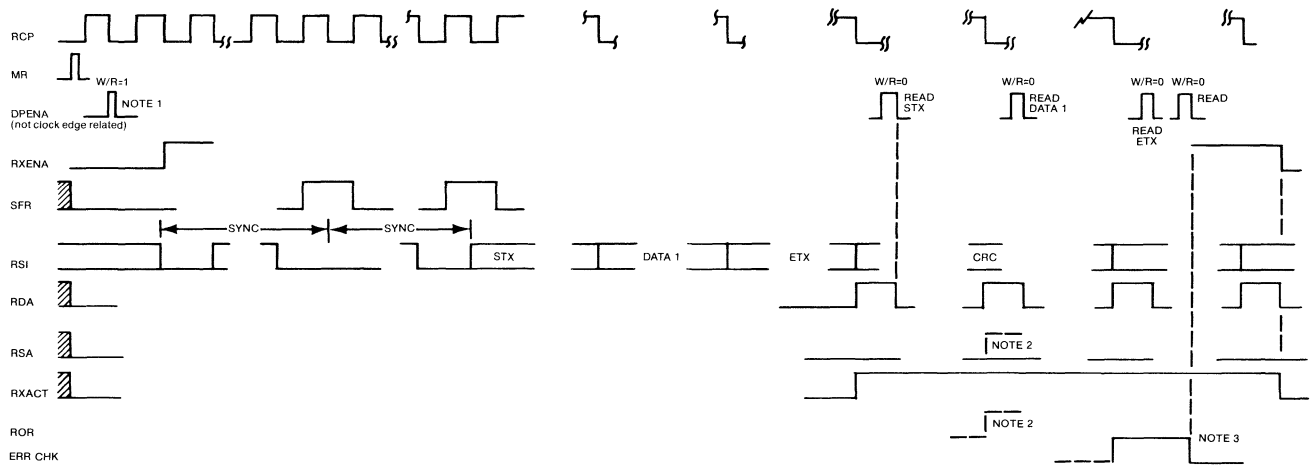
BOP TRANSMITTER OPERATION



CCP TRANSMITTER OPERATION

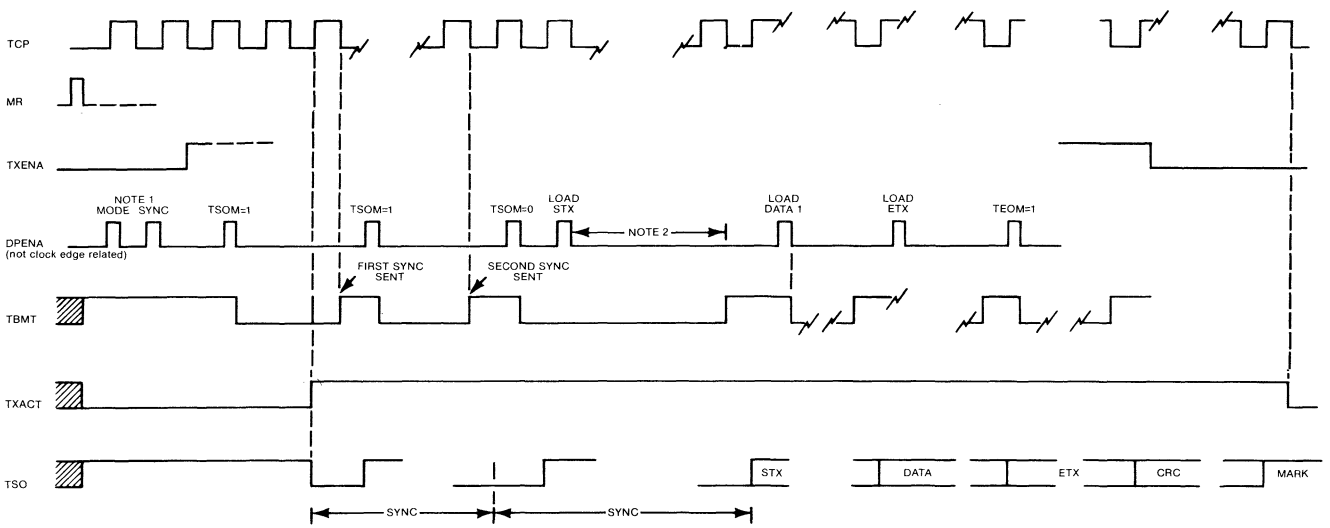


CCP RECEIVER TIMING



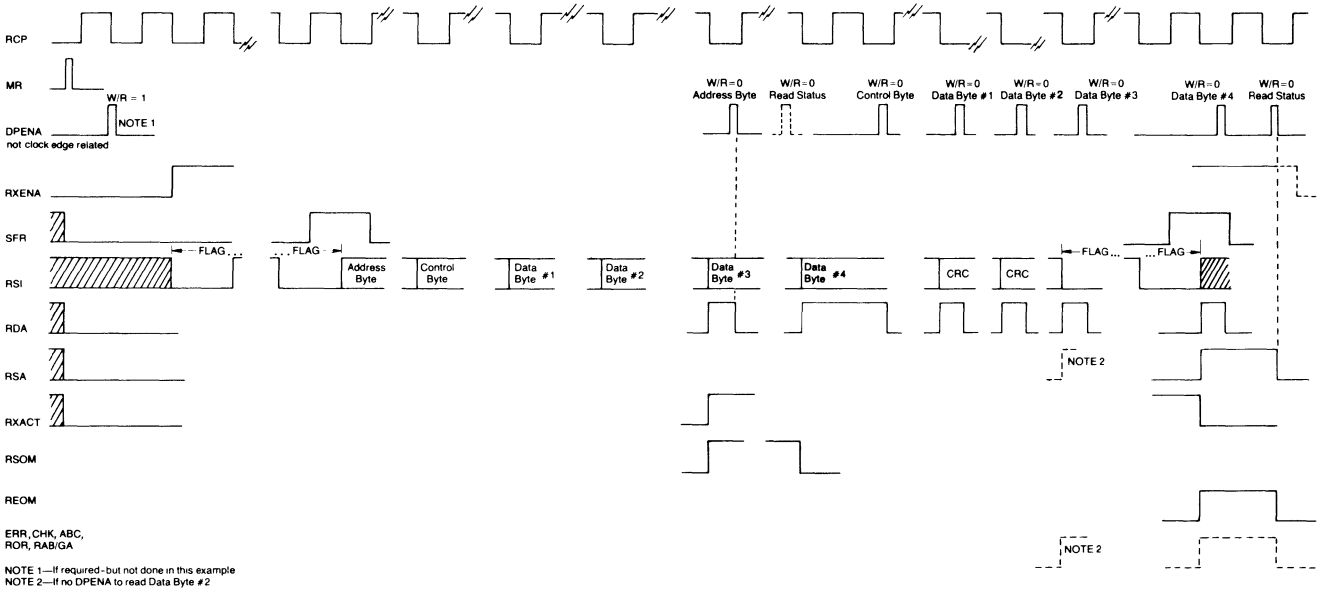
NOTE 1—Mode set for CCP with CRC selected
NOTE 2—If overrun had occured—no READ STX
NOTE 3—ERR CHK must be sampled before next byte or before RXENA brought low

CCP TRANSMITTER OPERATION



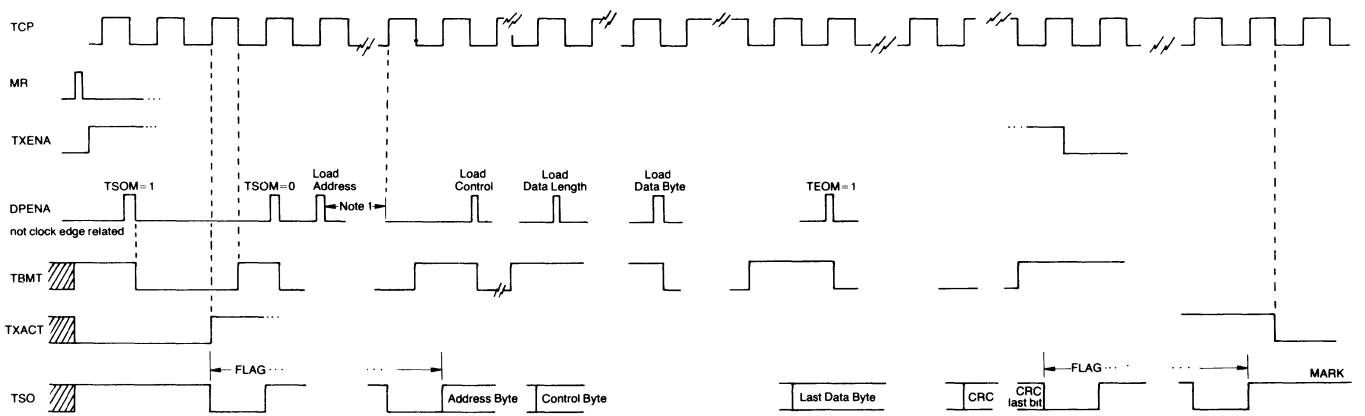
NOTE 1—Mode is CCP with CRC selected
NOTE 2—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1 to avoid underrun

BOP RECEIVER TIMING



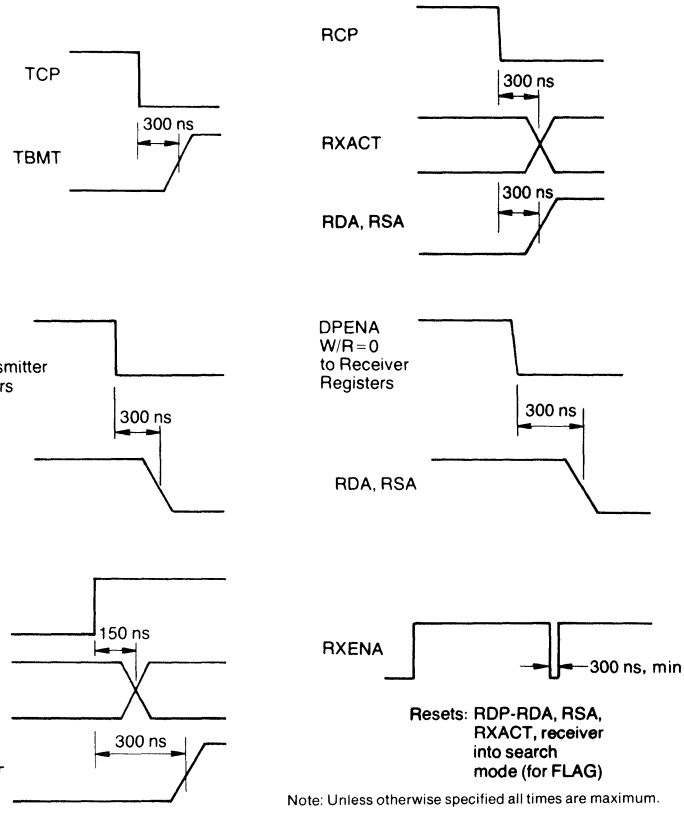
NOTE 1—If required - but not done in this example
NOTE 2—If no DPENA to read Data Byte #2

BOP TRANSMITTER OPERATION



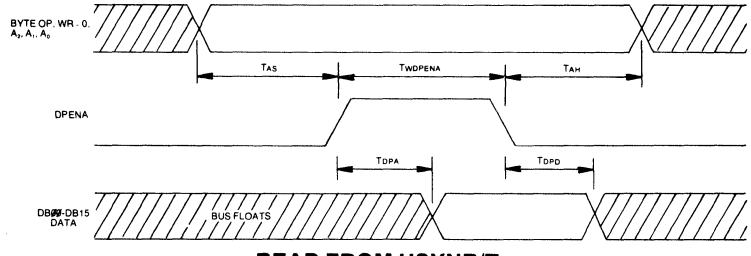
Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT = 1. To avoid underrun.

AC TIMING DIAGRAMS

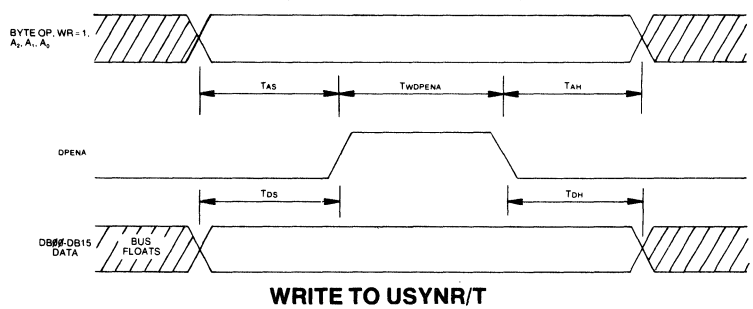


Note: Unless otherwise specified all times are maximum.

Data Port Timing



READ FROM USYNR/T



WRITE TO USYNR/T

MAXIMUM GUARANTEED RATINGS*

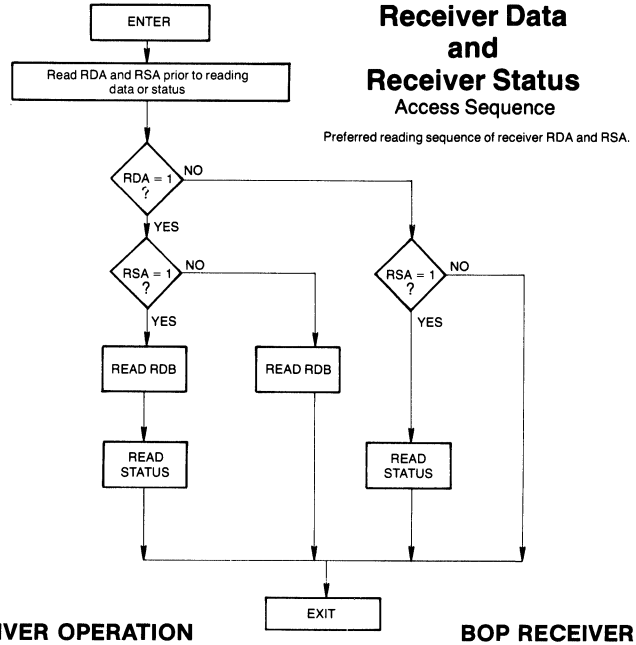
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	2.4				I_{OH}=40μa
INPUT LEAKAGE					
Data Bus		5.0	50.0	μa	0≤V_{IN}≤5v, DPENA=0 or W/R=I
All others				μa	V_{IN}=+5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}			70	ma	
I_{DD}			90	ma	
A.C. Characteristics					T_A=25°C
CLOCK-RCP, TCP					
frequency	DC		1.5	MHz	
PW_H	325			ns	
PW_L	325			ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}	250		50 μs	ns	
Set-up Time, T_{AS}	0			ns	
Byte Op, W/R					
A_2, A_1, A_0					
Hold Time, T_{AH}	0			ns	
Byte Op, WIR,					
A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}			150	ns	
DATA BUS DISABLE DELAY, T_{DPD}			100	ns	
DATA BUS SET-UP TIME, T_{DBS}	0			ns	
DATA BUS HOLD TIME, T_{DBH}	100			ns	
MASTER RESET, MR	350			ns	

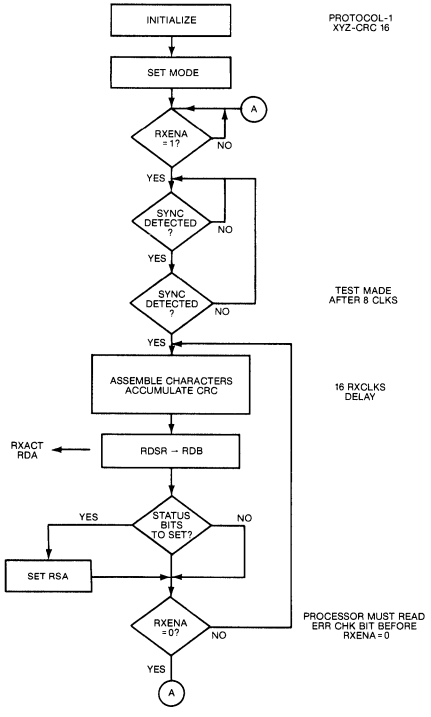


Receiver Data and Receiver Status

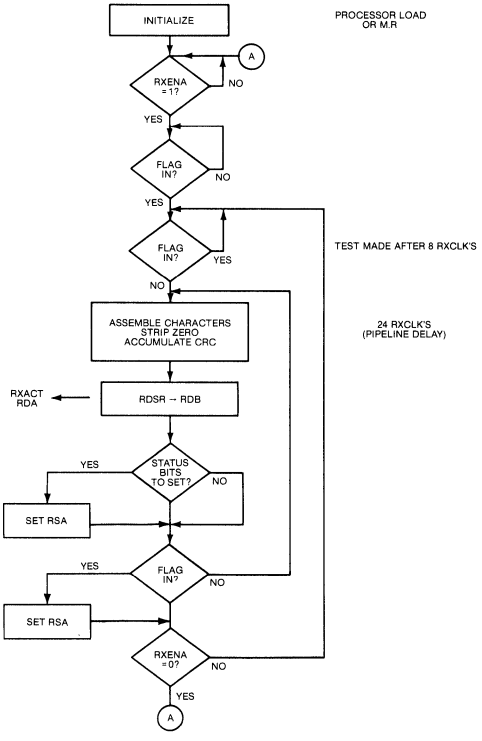
Access Sequence

Preferred reading sequence of receiver RDA and RSA.

CCP RECEIVER OPERATION



BOP RECEIVER OPERATION



STANDARD MICROSYSTEMS CORPORATION

COM52C50
PRELIMINARY

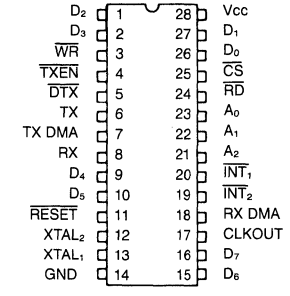
TWINAX Interface Circuit (TIC)

SECTION III

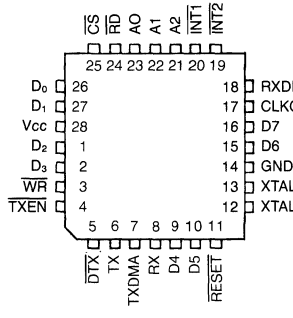
FEATURES

- ☐ Conforms to IBM® 5250 Standard used in IBM System /36 and /38.
- ☐ Operates at 1Mbps Data Rate
- ☐ Transmits and Receives Manchester II Encoded Data
- ☐ On Chip Odd or Even Parity Generation and Checking
- ☐ Programmable Interframe Zero Bit Insertion
- ☐ Handles Multi Byte and Single Byte Transfers
- ☐ Multiple Address Select Register Allows for Up to 7 Node Address Emulation
- ☐ Programmable Extended TX Enable
- ☐ Internal/External Loopback Capability for Self Test Diagnostics
- ☐ On Board Predistortion Circuitry
- ☐ Low Power CMOS
- ☐ On Board Crystal Oscillator Simplifies Clock Generation
- ☐ 8 MHz Clock Output for General Use
- ☐ Incorporates a Three Level Receive FIFO to Simplify Processor Interface
- ☐ Compatible with high speed microprocessor with no wait state up to 10 MHz (80186, 68000 etc...)
- ☐ Programmable DMA and Jump Vectoring Interface
- ☐ Independent RX DMA and TX DMA Request Signals
- ☐ Programmable Interrupt Selection
- ☐ 28 Pin Plastic Dual In Line and Chip Carrier Packages
- ☐ Open Drain Output on Interrupt Pins
- ☐ TTL Compatible Inputs and Outputs
- ☐ Single +5v Supply

PIN CONFIGURATION



PACKAGE: 28-pin DIP



PACKAGE: 28-pin PLCC

GENERAL DESCRIPTION

The COM52C50 TWINAX controller is a CMOS device that performs the communications interface to the IBM 5250 TWINAXIAL bus. It interfaces to a general purpose microprocessor on one side and to the IBM 5250 TWINAXIAL bus on the other side. The COM52C50 handles the parallel to serial and serial to parallel conversion of data to and from the TWINAXIAL bus and the encoding and decoding of data in Manchester II format. The COM52C50 consists of a RECEIVE BLOCK, a TRANSMIT BLOCK, and CONTROL circuitry. The Receive and Transmit sections of the COM52C50 are separate and may be used independent of one another. The COM52C50 generates and detects the bit sync, frame sync, parity, and the fill zero bit patterns according to the IBM 5250 standard.

IBM® is a registered trademark of the International Business Machines Corporation.

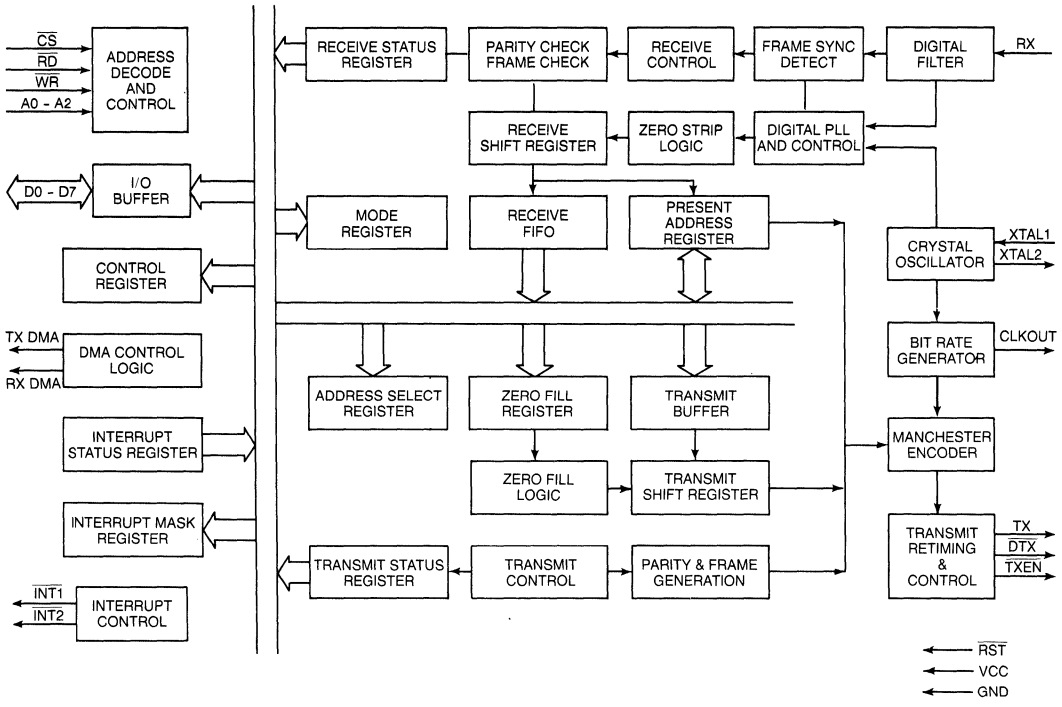


Fig. 1—COM52C50 INTERNAL BLOCK DIAGRAM

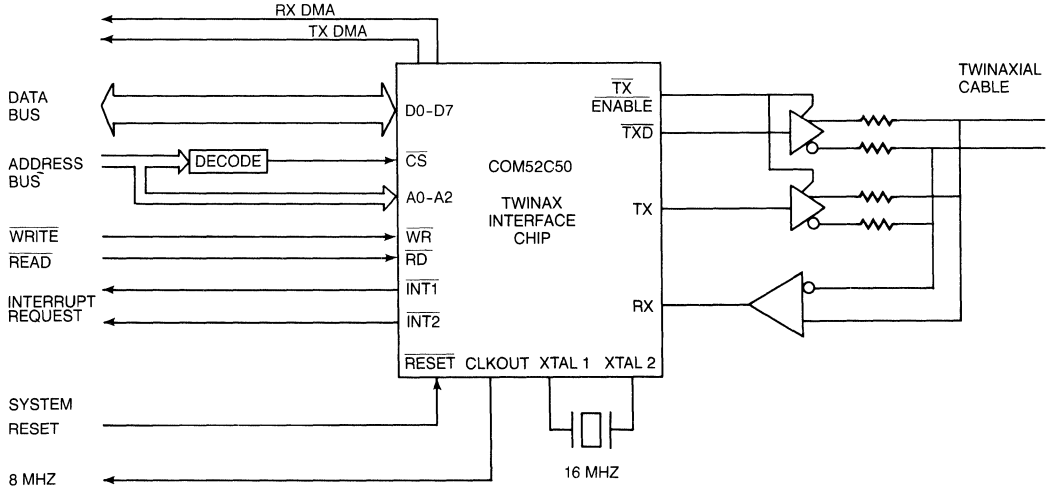


Fig. 2—TYPICAL COM52C50 INTERFACE

TABLE 1 - COM52C50 TWINAX DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1, 2, 9, 10, 15, 16, 26, 27	Bidirectional Data Bus	D_0-D_7	An 8 bit DATA BUS is used to interface the COM52C50 to the processor Data Bus.
3	Write Data Strobe	$\overline{WR}$	A low pulse on this input (when $\overline{CS}$ is low) enables the COM52C50 to accept the data or control information from the DATA BUS into the COM52C50.
4	TX Enable	$\overline{TX\ EN}$	This output is active low when the transmit data is valid. It is used to enable the external TX driver circuitry.
5	Delayed TX	$\overline{DTX}$	Delayed $\overline{TX}$ Manchester encoded.
6	TX Data	TX	Transmit data Manchester encoded.
7	TX Buffer	TX DMA	The TX Buffer Empty signal is used as a transmit DMA request.
8	RX Data	RX	This input accepts the receive Manchester II encoded bit stream.
11	Reset	$\overline{RST}$	This pin resets the COM52C50 to a known state. In addition, it disables the TX and puts an inactive state on the interrupt lines.
12 13	Crystal 2 Crystal 1	$XTAL_2$ $XTAL_1$	An external 16 MHz crystal is connected to these two pins. If an external 16 MHz TTL clock is used, it should be connected to $XTAL_1$ with a 390 ohm pullup resistor; $XTAL_2$ must be left floating.
14	Ground	GND	Ground
17	Clock Out	CLKOUT	This is a divide by two of the $XTAL_1$, 16 MHz input clock. It has a 50/50 duty cycle and can be used as a clock input to the host microprocessor.
18	RX Buffer	RX DMA	The RX Buffer Full signal is used as a receive DMA request.
19	Error Related Interrupt	$\overline{INT_2}$	This active low, open drain output provides the interrupt signal for error related operations.
20	Data Related Interrupt	$\overline{INT_1}$	This active low, open drain output provides the interrupt signal for data related operations.
21 22 23	Register Address Select	A_2 A_1 A_0	During processor to COM52C50 communications, these inputs are used to indicate which internal register will be selected for access by the processor.
24	Read Data Strobe	$\overline{RD}$	A low pulse on this input (when $\overline{CS}$ is low) enables the COM52C50 to place the data or status information on the DATA BUS.
25	Chip Select	$\overline{CS}$	A low level on this input enables the COM52C50 for reading and writing by the processor. When $\overline{CS}$ is high, the DATA BUS is in high impedance and the $\overline{WR}$ and $\overline{RD}$ will have no effect on the chip.
28	Power Supply	Vcc	+5V Power Supply.

FUNCTIONAL DESCRIPTION

RECEIVE BLOCK

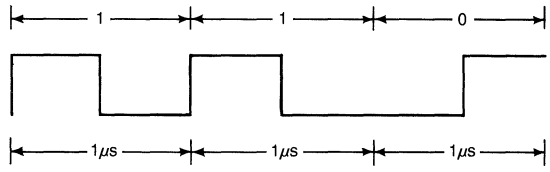
The COM52C50 recovers frames that conform to the IBM 5250 protocol. It also checks the received frame for proper sync, parity and trailing zeros. The RX input is sampled at 8 times the bit rate. The receive logic is brought into synchronization during bit and frame synchronization patterns. The internal receive clock is adjusted after each RX transition to compensate for bit jitter and distortion in the received data signal. In addition to the Receive Shift Register, the Receive block incorporates a two level First-in-First-out (FIFO) buffer. At the start of a message, the host microprocessor is alerted by handshake signals like Line Idle, Frame Sync Detect, Poll Command Detect, and Address Match. Thereafter, the RX Buffer Full signal informs the host microprocessor of the availability of received data. The end of a receive message is marked by either the detection of 1) End Of Message sequence 2) Line Idle or 3) Receive Error.

TRANSMIT BLOCK

The COM52C50 transmits data frames that conform to the IBM 5250 protocol. The transmit block consists of an 8 bit data buffer register, a present address register, 16 bit parallel to serial shift register, and parity generation logic. A transmit operation is initiated by loading the transmit buffer register. The transmitted frame will consist of the sync bit, the 8 bits loaded by the host microprocessor into the buffer register, the present address from the PRESENT ADDRESS REGISTER, or the (111) end of message code if the last frame is being transmitted, followed by a parity and three zero fill bits. After the host microprocessor loads the transmit buffer register, the TRANSMIT BUFFER EMPTY bit in the status register will become inactive. After a transfer of a data frame from the buffer register to the shift, register is accomplished, the TRANSMIT BUFFER EMPTY bit in the INTERRUPT AND TRANSMIT STATUS REGISTER becomes active.

BIT STREAM

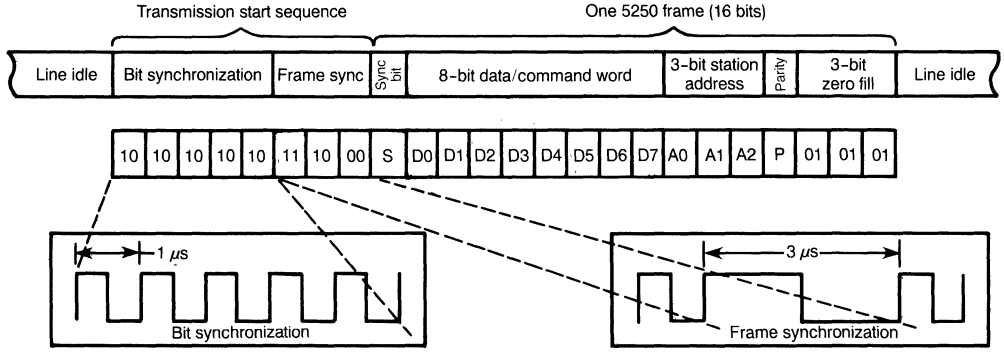
The bit stream is serially transmitted to (or received from) the System Unit at a transmission bit rate of 1 Mbps (±2%). Therefore, 1 microsecond is required for each bit, and 16 microseconds are required for each frame. All information between a station and the System Unit is transmitted on the twinaxial cable. The COM52C50 provides the transmitted serial data in Manchester encoded format where a "1" (one) bit is represented by a half bit cell of logical high followed by a half bit cell of logical low, and a 0 (zero) bit is represented by a half bit cell of logical low followed by a half bit cell of logical high. In addition, the COM52C50 provides a Delayed Transmit Data signal which is delayed by 1/4 of a bit time to simplify the interface to the external driver circuitry.



A message contains a bit sync pattern, a frame sync pattern, and a frame. The bit sync and the frame sync patterns establish synchronization between the station and the System Unit, and are transmitted prior to transmission of the first frame.

TABLE 2 - IBM 5250 FRAME FORMAT

The frame format for command and data to and from the IBM 5250 attachment is a fixed 16 bit frame. Only 13 bits contain information. The general format is as follows:



BIT	DESCRIPTION
0-2	These bits are always 0.
3	This is designated as the parity bit and will be set to ensure even parity in each frame.
4-6	These are the physical station address. Valid addresses are 000 to 110, and 111 is the end of message delimiter for the cable. A frame containing a 111 station address causes the station to ignore all following cable activity until a bit and frame synchronization is detected following a line turnaround. In addition, if only one frame is sent from the system unit, these bits represent the station address. If only one frame is sent from the work station, these bits are set to 111.
7-14	These bits contain command or data information. They represent a data byte or a status byte from the station, or they represent a data byte or a command from the system unit.
15	This is the sync bit. It is the first bit on the line and it is always set to 1.

RESETTING THE COM52C50

The COM52C50 must be reset on power up. This is accomplished by either of two methods: Hardware Reset or Software Reset.

Hardware Reset:

On the COM52C50 a $\overline{\text{RESET}}$ pin is dedicated to allow resetting of the device by applying a low level on the $\overline{\text{RST}}$ pin. The $\overline{\text{RESET}}$ signal should have a minimum duration of 1μs.

Software Reset:

The chip will also be reset when the Software Reset bit in the Control Register is asserted. The host microprocessor asserts Software Reset by writing a "zero" in bit 0 of the Control Register. To take the COM52C50 out of reset, the host microprocessor should write a "one" in bit 0 of the Control Register. Writes to the Control Register bit 0 should be spaced such that the Internal Reset signal has a minimum duration of 1μs.

Upon reset, all of the internal registers of the COM52C50 will be cleared. In addition, the COM52C50 enters an idle state in which it can neither transmit nor receive data. To disable undesired interrupts, the Interrupt Mask Register is set to 00 and the Status Registers bits are all inactive.

INITIALIZING THE COM52C50

Following RESET, the COM52C50 should be initialized by writing a valid bit pattern to the Interrupt Mask Register, the Mode Register, the Station Address Select Register. At this point, the Control Register can be used to enable Receive and Transmit.

TABLE 3 - REGISTER DECODE & TRUTH TABLE FOR INTERNAL REGISTER SELECT

ADDRESS	A2	A1	A0	$\overline{RD}$	$\overline{WR}$		
00	0	0	0	1	0	Mode Register	W
	0	0	0	0	1	Not Used	R
01	0	0	1	1	0	Interrupt Mask Register	W
	0	0	1	0	1	Interrupt Status Register	R
02	0	1	0	1	0	Address Select Register	W
	0	1	0	0	1	RX Status Register	R
03	0	1	1	1	0	Control Register	W
	0	1	1	0	1	RX Buffer	R
04	1	0	0	1	0	Zero Fill	W
	1	0	0	0	1	Not Used	R
05	1	0	1	1	0	Present Address Register	W
	1	0	1	0	1	Present Address Register	R
06	1	1	0	1	0	TX Buffer	W
	1	1	0	0	1	TX Status Register	R
07	1	1	1	1	0	TX Buffer EOM	W
	1	1	1	0	1	TX Status Register	R

REGISTER DESCRIPTIONS

RX BUFFER

This is the second level of a two byte deep Receive FIFO where the COM52C50 Receive Block provides new data and the microprocessor reads it. This register contains the 8 bit information field of an IBM5250 frame (bits 14-7). It is read by the host microprocessor after each frame reception which is indicated by the RX Buffer Full bit. This is an 8 bit read only register.

TX BUFFER

This register contains the 8 bit information field of an IBM5250 frame (bits 14-7). It is written to by the host microprocessor and contains the information to be sent out in the next frame. This is an 8 bit write only register.

ZERO FILL REGISTER

This eight bit register is loaded by the host microprocessor and contains the number of zero bits that should be filled between two frames. The host microprocessor would read a Set Mode Command and find out how many zero bytes must be padded on the next reply and then convert it to bits and write it to this register. The COM52C50 takes care of inserting the programmed number of zero bits between two frames. Up to 255 zero bits may be inserted in between frames. If no zero bit fill is required, this register should be cleared by writing a zero. The host microprocessor may not write to this register during data transmission. This register is cleared following RESET.

INTERRUPT MASK REGISTER

This is an 8 bit write only register which is loaded by the host microprocessor. This register controls interrupt generation on both the $\overline{INT1}$ and $\overline{INT2}$ interrupt pins. The most significant 5 bits enable the generation of $\overline{INT1}$, the least significant 3 bits enable the generation of $\overline{INT2}$.

$\overline{INT1}$

A logical one in a particular bit position will enable the corresponding bit in the Interrupt Status Register (bits 7-3) to cause an interrupt when it is set.

$\overline{INT2}$

A logical one in a bits (2-1-0) will enable bits (7-6-5) in the RX Status Register to cause an $\overline{INT2}$ interrupt when it is set.

Upon Reset, this register is cleared to all zeros thereby disabling interrupts. This is an 8 bit write only register.

ADDRESS SELECT REGISTER

This is an eight bit Write Only Register that controls address bit recognition of any of the seven possible node addresses. A node may emulate more than one address at a time by programming a "one" in the corresponding bit of the Address Register.

A "one" in any one or more of the Address Select bits allows the COM52C50 to respond to that group of addresses.

D7	D6	D5	D4	D3	D2	D1	D0
ONE	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Examples:

Emulate one address: (3)	1	0	0	0	1	0	0	0
Emulate four addresses: (6-4-3-0)	1	1	0	1	1	0	0	1
Emulate All Addresses: (6-5-4-3-2-1-0)	1	1	1	1	1	1	1	1

TABLE 4 - REGISTER DIAGRAMS

READ REGISTERS

ADDRESS	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	**Not Used**								
01	**Interrupt Status Register**	frame sync detect	address match	poll command detect	RX buffer full	TX buffer empty	RX overrun error	RX biphase error	RX parity error
		← generate interrupt 1 →						← generate RX error →	
02	**RX Status Register**	RX Errors	line idle detect	end of message detect	RX buffer full	A2	A1	A0	zero
		← generate interrupt 2 →							
03	**RX Buffer**	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
04	**Not Used**								
05	**Present Address Register**	zero	zero	zero	zero	zero	A2	A1	A0
06	**TX Status Register**	zero	zero	zero	zero	zero	TX underrun	TX buffer empty	zero
07	**TX Status Register**	zero	zero	zero	zero	zero	TX underrun	TX buffer empty	zero

WRITE REGISTERS

ADDRESS	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	**Mode Register**	Test mode	auto EOM 111	.25μs 16μs TX en.	Test mode	TX parity	RX parity	internal external loop	loop / norm
01	**Interrupt Mask Register**	frame sync detect	address match	poll command detect	RX buffer full	TX buffer empty	RX errors	line idle detect	end of message detect
		← Interrupt 1 Mask →					← Interrupt 2 Mask →		
02	**Address Select Register**	one	A6	A5	A4	A3	A2	A1	A0
03	**Control Register**	reset errors	zero	disable biphase	enable TX DMA	enable RX DMA	enable TX	enable RX	software reset
04	**Zero Fill Register**	D7	D6	D5	D4	D3	D2	D1	D0
05	**Present Address Register**	zero	zero	zero	zero	zero	A2	A1	A0
06	**TX Buffer**	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
07	**TX Buffer EOM**	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

PRESENT ADDRESS REGISTER

This register holds the present address information of the first frame following frame sync. It is used to convey the address information to the host microprocessor and has the address field information on all outgoing frames. This register is loaded by the Receive Block with the address information from the first frame following frame sync detect. This register can also be written to by the host microprocessor prior to initiating a Transmit sequence. The contents of this register are fed to the address compare logic which compares the Present Address to the Address Select Register. If a valid compare is detected, the Address Match bit in the Interrupt Status Register is set.

During a receive session, the contents of this register are valid only after the RX Buffer Full bit is set "one".

This is an eight bit read/write register.

TABLE 5—COM52C50 INTERRUPT STATUS REGISTER (BITS 0-7)

This is an eight bit register that can be read by the host microprocessor. The Interrupt Status Register is cleared following software or hardware reset. The bits in this register are used to indicate the following information:

BIT	DESCRIPTION
0	**RX PARITY ERROR** Signals the microprocessor that the frame received contained an incorrect number of binary "1" bits. This bit is set when the received frame has an incorrect parity bit and parity is enabled. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting internal RESET. d. asserting external hardware Reset.
1	**RX BIPHASE ERROR** Signals the microprocessor that a bit within a received frame has violated Biphase Manchester code (i.e. the two half bit cells of a bit were not complements). This bit is set when a Biphase error occurs during bits 0-15 of a frame. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting internal RESET. d. asserting external hardware Reset.
2	**RX OVERRUN ERROR** Signals the microprocessor that an Overrun condition has occured. This bit is set when a byte stored in the Receive Holding Register is overwritten with a new byte from the Receive Shift Register before the microprocessor has read the Receive Holding Register. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting Internal RESET. d. asserting External Hardware Reset. e. Frame Sync Detect going active.
3	**TX BUFFER EMPTY** Signals the processor that the Transmit Character Buffer is empty and that the COM52C50 can accept a new character for transmission. This bit is set when a character has been loaded from the Transmit Holding Register to the Transmit Shift Register. This bit is cleared by: a. writing to the Transmit Buffer Register b. clearing TX Enable in the Control Register c. asserting internal RESET. d. asserting external hardware Reset. This bit is initially set when the transmitter logic is enabled by setting the TXenable bit in the Control Register (also TX BUFFER is empty because of reset). Data can be overwritten if a consecutive write is performed while TX buffer empty is zero.
4	**RX BUFFER FULL** Signals the processor that a completed character is present in the Receive Buffer Register for transfer to the processor. This bit is set when a character has been loaded from the receive deserialization logic to the Receive Holding Register. This bit is cleared by: a. reading the Receive Holding Register b. clearing RX Enable in the Control register c. Frame Sync Detect going active d. asserting internal RESET. e. asserting external hardware Reset.

TABLE 5—COM52C50 INTERRUPT STATUS REGISTER (BITS 0-7) CONTINUED

BIT	DESCRIPTION
5	**POLL COMMAND DETECTED** Signals the microprocessor that the command in the Receive Holding Register is a POLL command. (xxx10000) This bit is set when the first frame following Frame Sync has the binary 10000 pattern in the least significant 5 bits of the data section. This bit is cleared by: a. reading the RX Buffer Register when RX Buffer Full is set. b. Frame Sync Detect going active. c. asserting internal RESET. d. asserting external hardware Reset.
6	**ADDRESS MATCH** Signals the microprocessor that a match has occured between the address field of the first frame following Frame Sync and any bit within the Address Select Register. This bit is set after a valid compare has occured between the address field of the first frame following frame sync and any bit of the Address Select Register. This bit is cleared by: a. reading the RX Buffer Register when RX Buffer Full is set. b. Frame Sync Detect going active. c. asserting internal RESET. d. asserting external hardware Reset.
7	**FRAME SYNC DETECTED** Signals the microprocessor that a Frame Sync has been detected on the RX pin of the COM52C50. The Frame Sync detect circuitry checks for one "1" bit (10 half bit) followed by a three half bit times of ones followed by a three half bit times of zeros (111000). This bit is set when a Valid Frame Sync pattern is detected. This bit is cleared by: a. reading the Interrupt Status Register. b. Line Idle going active. c. asserting internal RESET. d. asserting external hardware Reset.

RESETTING OF INTERRUPTS

The $\overline{INT1}$ and $\overline{INT2}$ signals feature an automatic interrupt acknowledge that will take interrupt away when the proper action is taken by the processor. The following describes how each of the eight interrupting conditions get cleared.

When the interrupt is caused by:	The interrupt is cleared by:
Frame Sync Detect	Reading the Interrupt Status Register twice Line Idle going active Internal Reset External Reset
Address Match	Frame Sync Detect Reading the RX Buffer Register when the RX Buffer is full Internal Reset External Reset
Poll Command Detect	Frame Sync Detect Reading the RX Buffer Register when RX Buffer is full Internal Reset External Reset
RX Buffer Full	Clearing the RX Enable bit Reading the RX Buffer Register when the RX Buffer is full Internal Reset External Reset
TX Buffer Empty	Writing to the TX Buffer Register Clearing the TX ENable bit Internal Reset External Reset
RX Errors	Asserting Reset Errots Clearing RX Enable Internal Reset External Reset
Line Idle Detect	Reading the RX Status Register twice Internal Reset External Reset
End of Message (EOM) Detect	Reading the RX Status Register twice Internal Reset External Reset

TABLE 6—COM52C50 RX STATUS REGISTER (BITS 0-7)

This is an eight bit register that can be read by the host microprocessor. The bits in this register are used to indicate the following information:

BIT	DESCRIPTION
0	**FIXED ZERO**
1-3	**PRESENT ADDRESS BIT 0-1-2** These three bits hold the value of the Present Address. They are the same as the bits 1, 2, 3, of the Present Address Register.
4	**RX BUFFER FULL** Signals the processor that a completed character is present in the Receive Buffer Register for transfer to the processor. This bit is set when a character has been loaded from the receive deserialization logic to the Receive Buffer Register. This bit is cleared by: a. reading the Receive Buffer Register b. clearing RX Enable in the Control register c. Frame Sync Detect going active d. asserting internal RESET e. asserting external hardware RESET
5	**LAST FRAME/End Of Message (EOM)** Signals the microprocessor that a "1 1 1" pattern has been detected in the address field of an incoming frame. This bit is propagated through the RX FIFO logic and it corresponds to the data byte immediately available to the processor. This bit is set when the 3 bit address field of a frame gets a match with a constant "1 1 1" pattern. This bit is cleared by: a. Frame Sync Detect going active. b. clearing RX Enable in the Control Register. c. asserting internal RESET. d. asserting external hardware RESET
6	**LINE IDLE** Signals the microprocessor that the RX line has not seen a transition for the past 3μs time interval. This can be used by the microprocessor to learn that the RX line is idle. This bit is set when the RX line remains idle for a 3 microseconds duration. This bit is cleared by: a. activity on the RX line. b. clearing RX Enable in the Control Register c. asserting Internal RESET. d. asserting External Hardware Reset.
7	**RX ERRORS** Signals the microprocessor that a Receive Error condition has occured. This bit is set when any one or both of the Interrupt Status Register bits 0 and 1 are set. This bit is cleared by: a. asserting Reset Errors in the Control Register b. clearing RX Enable in the Control Register. c. asserting Internal Software RESET. d. asserting External Hardware RESET.

TABLE 7—COM52C50 TX STATUS REGISTER (BITS 0-7)

BIT	DESCRIPTION
0	**Fixed at Zero**
1	**TX BUFFER EMPTY** Signals the processor that the Transmit Buffer Register is empty and that the COM52C50 can accept a new character for transmission. This bit is set when a character has been loaded from the Transmit Buffer Register to the Transmit Shift Register. This bit is cleared by: a. writing to the Transmit Buffer Register b. clearing TX Enable in the Control Register c. asserting internal software RESET. d. asserting external hardware RESET. This bit is initially set when the transmitter logic is enabled by setting the TXenable bit in the Control Register. Data can be overwritten if a consecutive write is performed while TX buffer empty is "zero".
2	**TX UNDERRUN ERROR** Signals the microprocessor that an Underrun condition has occured. This bit is set when, during a transmission process, the microprocessor writes to the TX Holding Register after the TX Shift Register has already shifted its last bit out. This bit is cleared by: a. clearing TX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting Internal RESET. d. asserting External Hardware RESET.
3-7	These bits are fixed zeros.
The TX Status Register is cleared following software or hardware reset.	

TABLE 8—COM52C50 CONTROL REGISTER (BITS 0-7)

The Control Register is an eight bit write only register that is used by the microprocessor to control the COM52C50. Following External Reset all bits of the Control Register are cleared to "zero" except for the Software Reset bit. Internal Reset does not affect any of the Control Register bits. The bits of the Control Register are defined as follows:

BIT	DESCRIPTION
0	**SOFTWARE RESET** This bit is used by the microprocessor to reset the COM52C50 via a software command. When this bit is cleared, Internal Reset is asserted and the COM52C50 is reset. This bit should be set to "one" during normal operations.
1	**ENABLE RECEIVE** This bit is used by the microprocessor to enable the Receive Logic in the COM52C50 to function. When this bit is cleared, the RX BUFFER FULL bit in the Status Register will be disabled. This bit should be set to "one" during normal operations.
2	**ENABLE TRANSMIT** Data transmission cannot take place via the COM52C50 unless this bit is set to logic "one". When this bit is reset (disabled), transmission will be disabled only after the previously written data has been transmitted. (This simply disables loading of the TX Buffer Register).
3	**ENABLE RX DMA** This bit, when set, will enable the RX DMA handshake signal on the COM52C50. When this bit is cleared, the RX DMA signal on the COM52C50 is kept low.
4	**ENABLE TX DMA** This bit, when set, will enable the TX DMA handshake signal on the COM52C50. When this bit is cleared, the TX DMA signal is kept low.
5	**DISABLE BIPHASE ERRORS** This bit, when set, will disable the detection of biphase errors in the receive block. This bit is cleared upon power up and biphase error detection is enabled.
6	**NOT USED—MUST BE ZERO**
7	**RESET ERRORS** This bit, when set, will clear the Receive Error Status bits in the Interrupt Status Register (Parity, Biphase, Overrun). As a result of this, the RX Error bit in the RX Status Register will be cleared. Reset Errors also resets the TX Underrun status bit in the TX Status Register. No latch is provided in the Control Register for saving the state of this bit; therefore there is no need for clearing it.

THE COM52C50 ON CHIP CRYSTAL OSCILLATOR

The COM52C50 incorporates an on chip crystal oscillator. A 16 MHZ parallel resonant crystal is connected to the XTAL1 and the XTAL2 pins of the COM52C50 along with a 1.0 MOhm resistor across the crystal and two 22pf capacitors from each node of the crystal to ground. (see figure 18, CONNECTION DIAGRAM FOR PARALLEL RESONANT CRYSTAL)

A TTL clock can also be used to supply the clock signal to the COM52C50. This is done by supplying a TTL level clock to the XTAL1 pin of the COM52C50 along with a 390 ohm resistor from the XTAL1 pin to Vcc. The XTAL2 pin should not be connected when an external clock is supplied. (see figure 19, RECOMMENDED EXTERNAL TTL CLOCK CONNECTION)

DMA OPERATION

The COM52C50 features two independent DMA Request signals. These signals are provided to allow the COM52C50 to interface to one or two channels of a DMA controller such as that of the 80188 and the 80186. Each of the RX DMA and TX DMA request signals can be individually enabled via software commands in the Control Register. DMA interface is most useful when moving blocks of data following an activate read or an activate write command.

RX DMA

Following an active read command, the host microprocessor would initialize the RX DMA channel and enable RX DMA by writing a one in the Control Register bit 3. The COM52C50 will automatically generate the RX DMA Request signal as soon as a received frame is moved from the Receiver Shift Register to the Receiver FIFO. At this time, the DMA channel will initiate a Read Receive Buffer cycle which in turn will be used as an automatic DMA Acknowledgment. When a new frame arrives and is ready to be read by the DMA channel, the COM52C50 will assert the RX DMA Request signal and inform the DMA channel of the availability of the next word. The Receiver FIFO will be in use during DMA operations. This gives the DMA channel a maximum of three frame times for DMA latency. On the average, however, the DMA channel must be able to keep up with the COM52C50 byte rate.

TX DMA

When transmitting blocks of data, the host microprocessor would initialize the TX DMA channel and enable TX DMA by writing a one in the Control Register bit 4. The COM52C50 will automatically generate the TX DMA Request signal when the TX Buffer is empty. When the DMA channel performs a write cycle to the COM52C50 TX Buffer, the TX DMA Request signal will be inactive until the TX Buffer becomes empty again. After writing the last data frame to the TX Buffer, the host microprocessor can disable the TX DMA Request signal by writing to the Control Register.

TABLE 9—COM52C50 MODE REGISTER DESCRIPTION (BITS 0-7)

BIT	DESCRIPTION
0	**NORMAL/LOOPBACK MODE** This bit when set will put the COM52C50 in loopback mode. When in loopback mode, bit 1 of the Mode Register specifies Internal or External loopback modes. 0 NORMAL OPERATION 1 LOOPBACK MODE
1	**EXTERNAL/INTERNAL LOOPBACK** This bit specifies External or Internal loopback Modes. When bit 0 of the Mode Register specifies normal mode of operation, this bit is a don't care. 0 EXTERNAL LOOPBACK 1 INTERNAL LOOPBACK
2	**EVEN/ODD RX PARITY** This bit specifies Even or Odd parity for the receive section of the COM52C50. 0 EVEN RX PARITY 1 ODD RX PARITY
3	**EVEN/ODD TX PARITY** This bit specifies Even or Odd parity for the transmit section of the COM52C50. 0 EVEN TX PARITY 1 ODD TX PARITY
4	**NORMAL/TEST MODE** This bit when set puts the COM52C50 in a VLSI test mode. This bit is cleared upon Reset and should be cleared for normal operation. 0 NORMAL OPERATION 1 TEST MODE
5	**TX ENABLE 250ns/16μs** This bit controls the amount of time the Transmit Enable Signal will remain active after the last TX bit is shifted out. When set to "zero", the TX Enable signal goes inactive after 250ns following the last TX data bit. When set to "one", the TX Enable signal goes inactive after 16μs following the last TX data bit. This can be used to drive the Twinax Cable after a transmission in order to reduce line reflection effect. 0 TX enable 250ns 1 TX enable 16μs
6	**EOM/Auto 111** This bit determines if Automatic 111 address should be inserted on a transmitted message upon transmitter underrun. When this bit is a "zero", the microprocessor has to write to TX Buffer EOM to force a 111 address on the last frame of transmitted data. 0 EOM 111 1 Auto 111
7	**NORMAL/TEST MODE** This bit when set puts the COM52C50 in a VLSI test mode. This bit is cleared upon Reset and should be cleared for normal operation. 0 NORMAL OPERATION 1 TEST MODE

Following RESET, the mode register will be cleared to all "zero's" and the default Mode Setting will be:

BIT 0 - 0 NORMAL OPERATION
BIT 1 - 0 EXTERNAL LOOPBACK
BIT 2 - 0 EVEN RX PARITY
BIT 3 - 0 EVEN TX PARITY
BIT 4 - 0 NORMAL OPERATION
BIT 5 - 0 TX ENABLE .250
BIT 6 - 0 EOM 111
BIT 7 - 0 NORMAL OPERATION

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... -55 to 150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... V_{cc} + 0.3V
Negative Voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{cc} ..... +7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied.

NOTE: When powering this device from the laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TABLE 11-ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, Vcc = +5V ±5%.)

FIG. NO.	PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS	COMMENTS
	DC CHARACTERISTICS						
	LOW INPUT VOLTAGE	$V_{IL\ 1}$			0.8	V	Except TLL Input Clock
	HIGH INPUT VOLTAGE	$V_{IH\ 1}$	2.0			V	Except TTL Input Clock
	LOW INPUT VOLTAGE	$V_{IL\ 2}$			1.0	V	TTL Clock Input
	HIGH INPUT VOLTAGE	$V_{IH\ 2}$	Vcc-0.5V			V	TTL Clock Input
	LOW OUTPUT VOLTAGE	$V_{OL\ 1}$			0.4	V	I_{OL} = 3.5ma
	HIGH OUTPUT VOLTAGE	$V_{OH\ 1}$	2.4			V	I_{OH} = 200μa
	LOW OUTPUT VOLTAGE	$V_{OL\ 2}$			3.0	V	For Clock Output
	HIGH OUTPUT VOLTAGE	$V_{OH\ 2}$	3.0			V	For Clock Output
	INPUT LEAKAGE CURRENT	I_L		±10		μA	
	INPUT CAPACITANCE	C_{IN}		25		pF	
	POWER SUPPLY CURRENT	I_{CC}		20	30	mA	

FIG. NO.	PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS	COMMENTS
	AC CHARACTERISTICS						
	WRITE CYCLE						
Fig. 3	Address Setup Time	t_1	50			ns	
Fig. 3	Address Hold Time	t_2	0			ns	
Fig. 3	$\overline{WR}$ Pulse Width	t_3	150			ns	
Fig. 3	Data Setup Time	t_4	75			ns	
Fig. 3	Data Hold Time	t_5	10			ns	
	READ CYCLE						
Fig. 4	Address Setup Time	t_6	50			ns	
Fig. 4	Address Hold Time	t_7	0			ns	
Fig. 4	$\overline{RD}$ Pulse Width	t_8	150			ns	
Fig. 4	T_{zx}	t_9	0		80	ns	
Fig. 4	T_{xz}	t_{10}	0		80	ns	
Fig. 5	READ WRITE INTERVAL	t_{13}	100			ns	
	INTERRUPT ACKNOWLEDGE TIMING						
Fig. 6	Read Int. Status Reg. to INT inactive	t_{14}		300		ns	
	DMA ACKNOWLEDGE TIMING						
Fig. 7	Read RX Buffer to PXDMA inactive	t_{15}		200		ns	
Fig. 8	Write TX Buffer to TXDMA inactive	t_{16}		200		ns	

FIG. NO.	SYMBOL PARAMETER	SYMBOL	MIN.	TYP*	MAX	UNITS	COMMENTS
	TTL CLOCK INPUT TIMING						
Fig. 9	Input Clock fall time	t_{20}			10	ns	
Fig. 9	Input Clock rise time	t_{21}			10	ns	
Fig. 9	Input Clock high time	t_{22}	20			ns	Vcc-1.0V
Fig. 9	Input Clock low time	t_{23}	20			ns	@0.6 V
Fig. 9	Input Clock period	t_{24}		62.5		ns	@1.5 V
	CLOCK OUT TIMING						
Fig. 10	Clock Out fall time	t_{25}			10	ns	@50pF max
Fig. 10	Clock Out rise time	t_{26}			10	ns	@50pF max
Fig. 10	Clock Out high time	t_{27}	55			ns	@50pF max
Fig. 10	Clock Out low time	t_{28}	55			ns	@50pF max
Fig. 10	Clock Out period	t_{29}		125		ns	@50pf max
	TX DATA TIMING						
Fig. 11	$\overline{WR}$ to tx Buffer $\overline{TX\ ENABLE}$	t_{30}		1500		ns	
Fig. 11	$\overline{TX\ ENABLE}$ active to TX DELAY	t_{31}		250		ns	
Fig. 11	$\overline{DTX}$ to $\overline{TX\ ENABLE}$ inactive	t_{32}		250		ns	
Fig. 11	TX to $\overline{DTX}$ delay	t_{33}		250		ns	
Fig. 11	TX, $\overline{DTX}$ half bit cell	t_{34}		500		ns	
Fig. 11	TX, $\overline{DTX}$ full bit cell	t_{35}		1000		ns	
Fig. 11	TX, $\overline{DTX}$ rise time				10	ns	
	TX, $\overline{DTX}$ fall time				10	ns	
	RX DATA TIMING						
	RX half bit cell pulse width			500		ns	(Jitter Tolerance ±20%)
	RX bit cell pulse width			1000		ns	
	RESET TIMING						
Fig. 12	Internal Reset pulse width	t_{40}	1.0			μs	
Fig. 13	External Reset pulse width	t_{41}	1.0			μs	
	Input Clock Frequency			16		MHZ	

*ALL TYPICAL VALUES ARE AT 25°C AND Vcc = 5.0 V

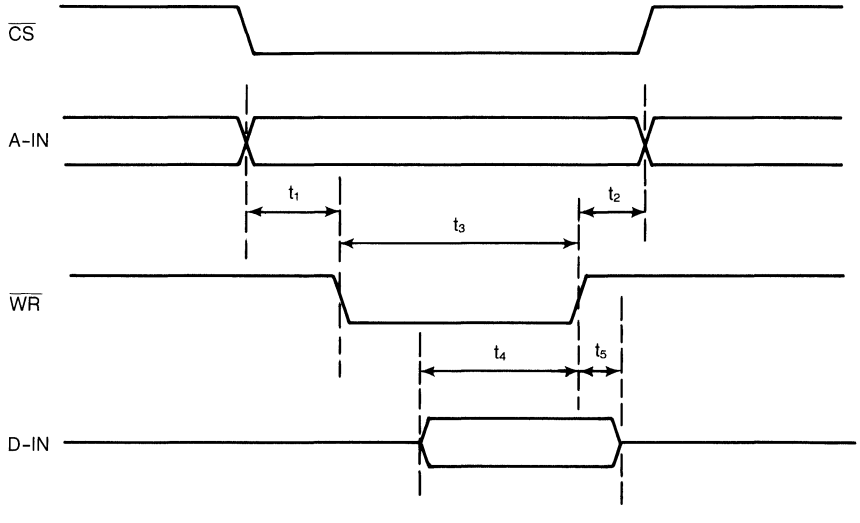


Fig. 3—PROCESSOR WRITE COM52C50 CYCLE

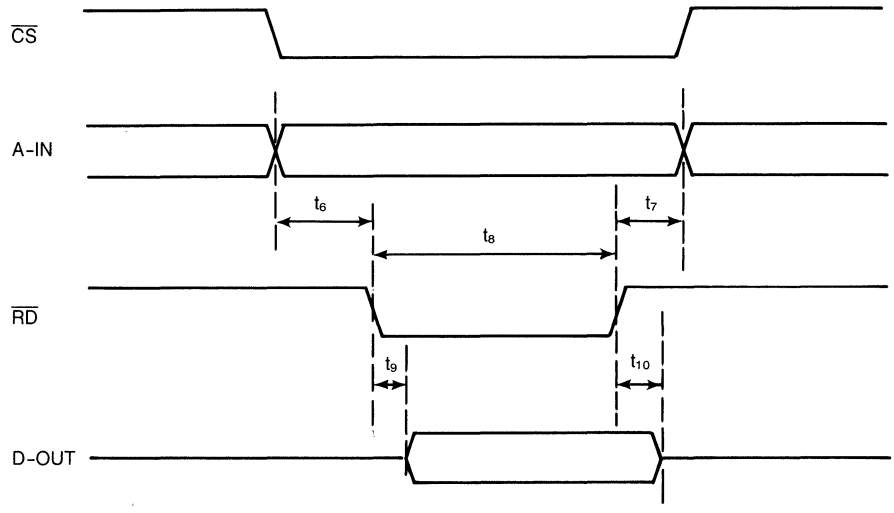


Fig.4—PROCESSOR READ COM52C50 CYCLE

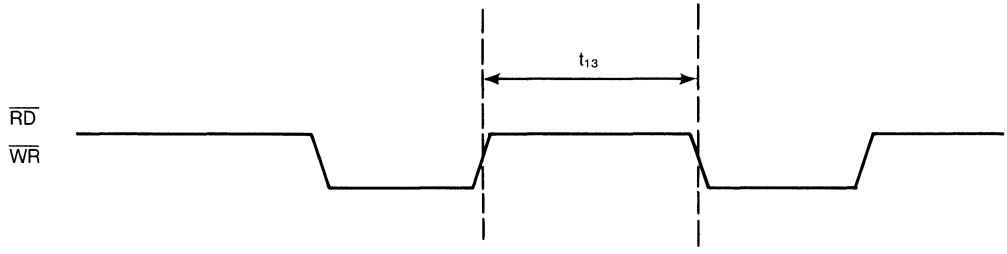


Fig. 5—PROCESSOR ACCESS COM52C50 REPETITION

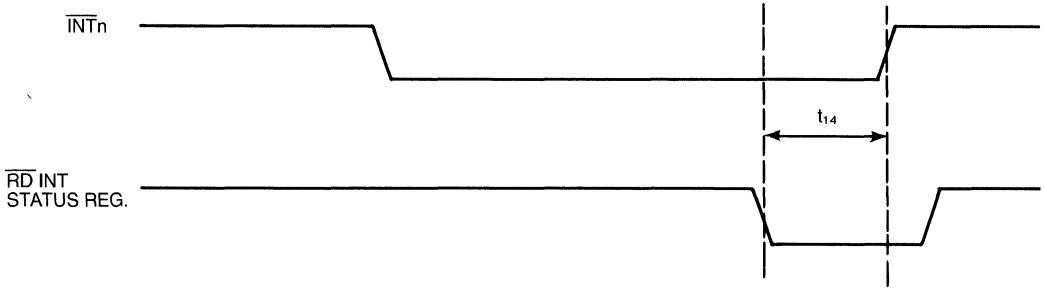


Fig. 6—INTERRUPT ACKNOWLEDGE TIMING

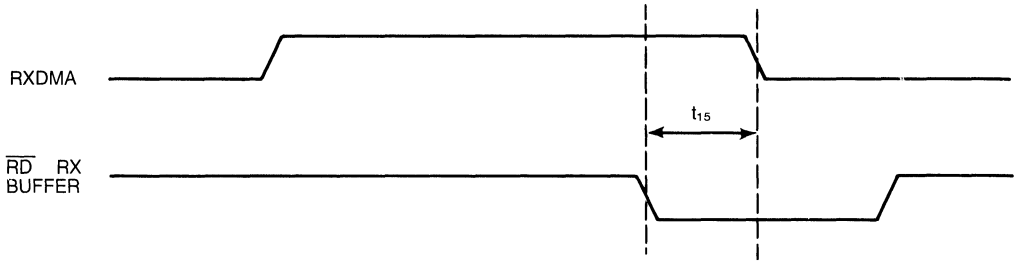


Fig. 7—RX DMA ACKNOWLEDGE TIMING

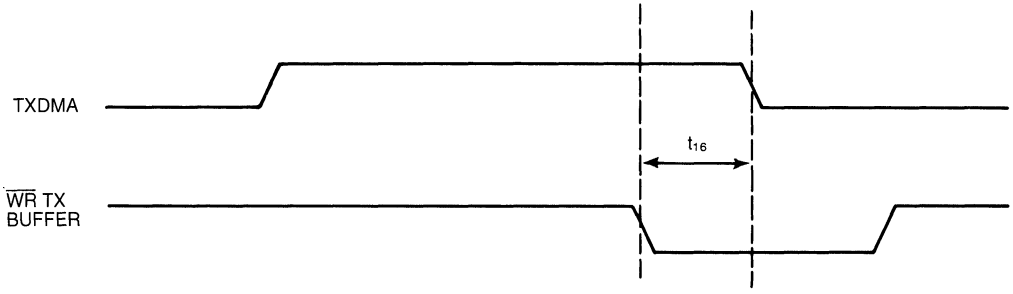


Fig. 8—TX DMA ACKNOWLEDGE TIMING

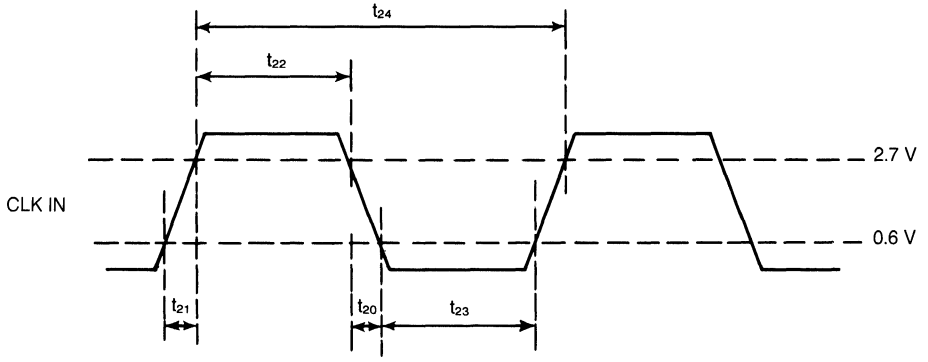


Fig. 9—TTL INPUT CLOCK TIMING

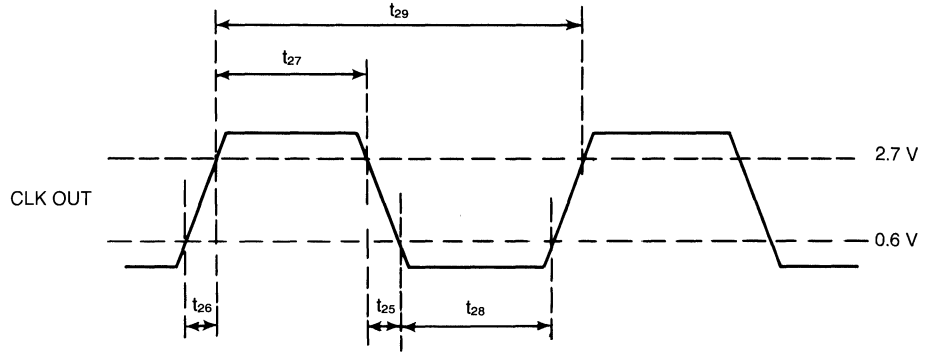


Fig. 10—8 MHZ CLOCK OUT TIMING

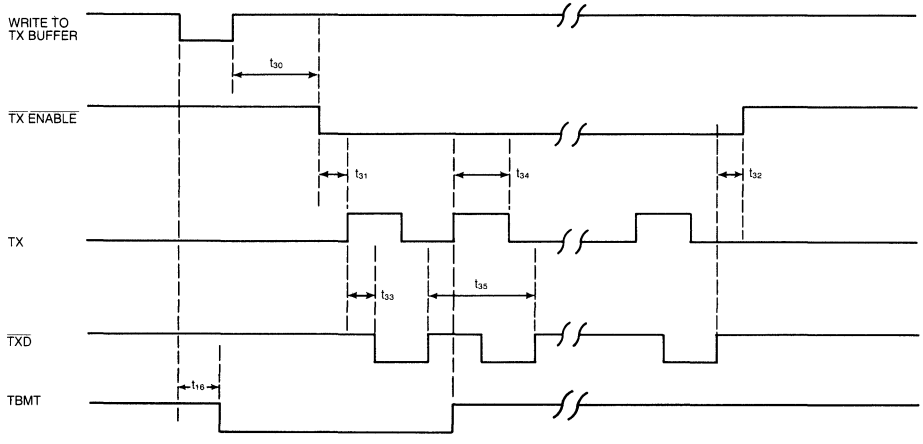


Fig. 11—TX, DTX, TX ENABLE TIMING

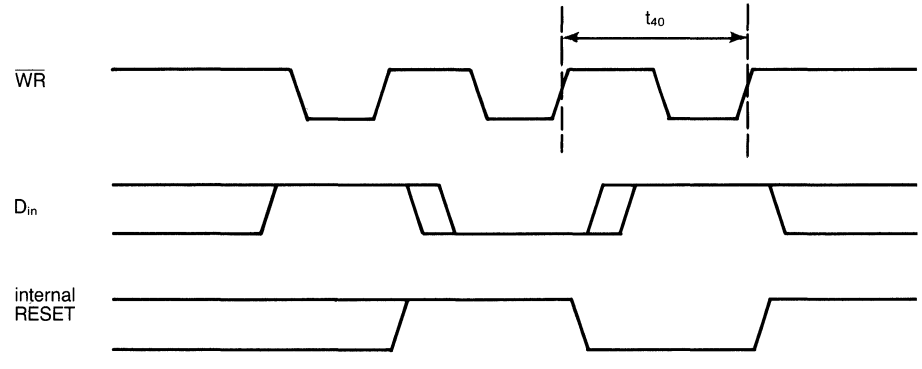


Fig. 12—INTERNAL RESET TIMING

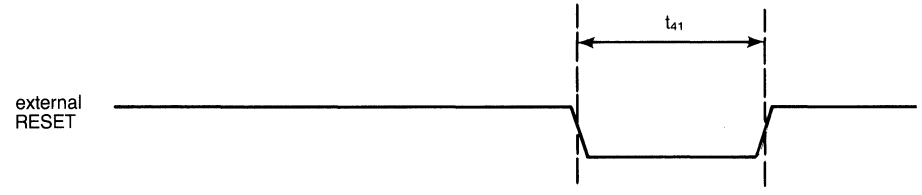


Fig. 13—EXTERNAL RESET TIMING

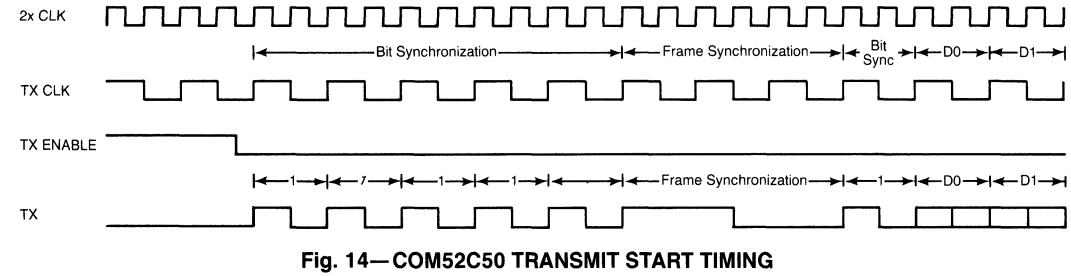


Fig. 14—COM52C50 TRANSMIT START TIMING

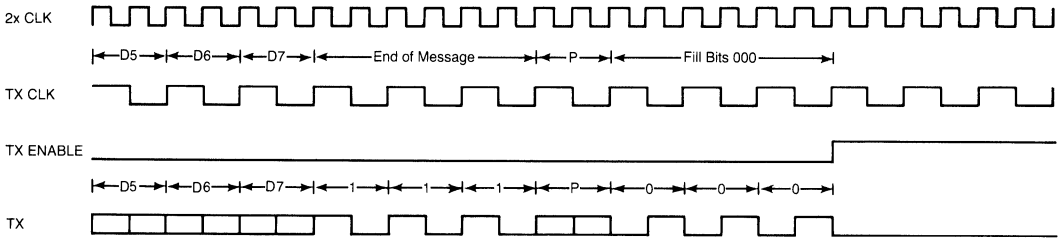


Fig. 15—COM52C50 TRANSMIT END TIMING

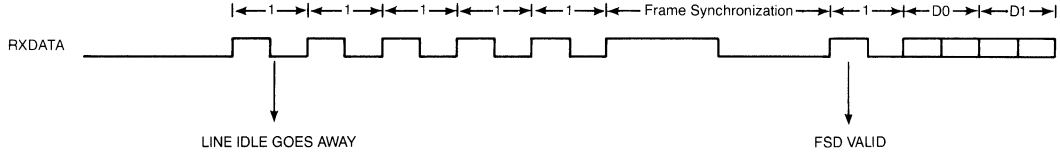


Fig. 16—COM52C50 RECEIVE START TIMING

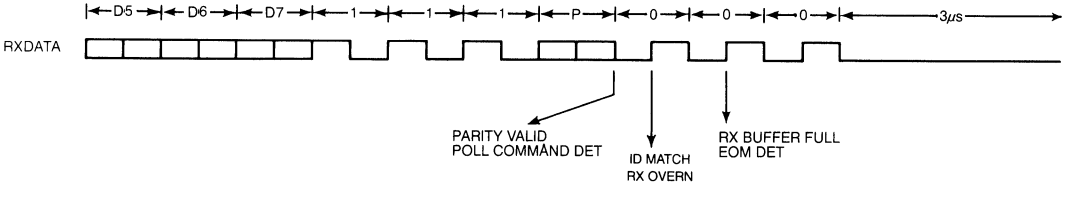


Fig. 17—COM52C50 RECEIVE END TIMING

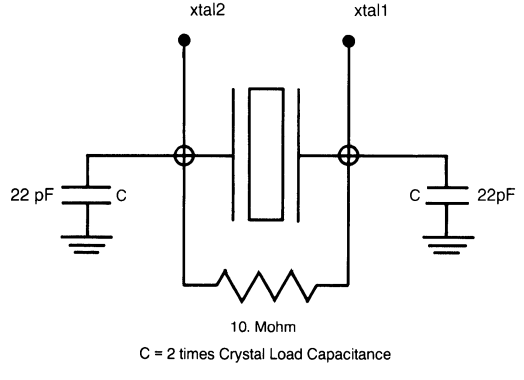


Fig. 18—CONNECTION DIAGRAM FOR PARALLEL RESONANT CRYSTAL

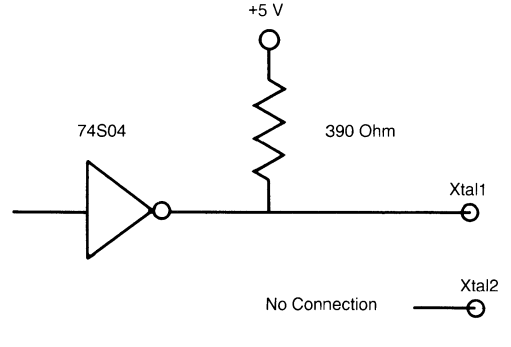
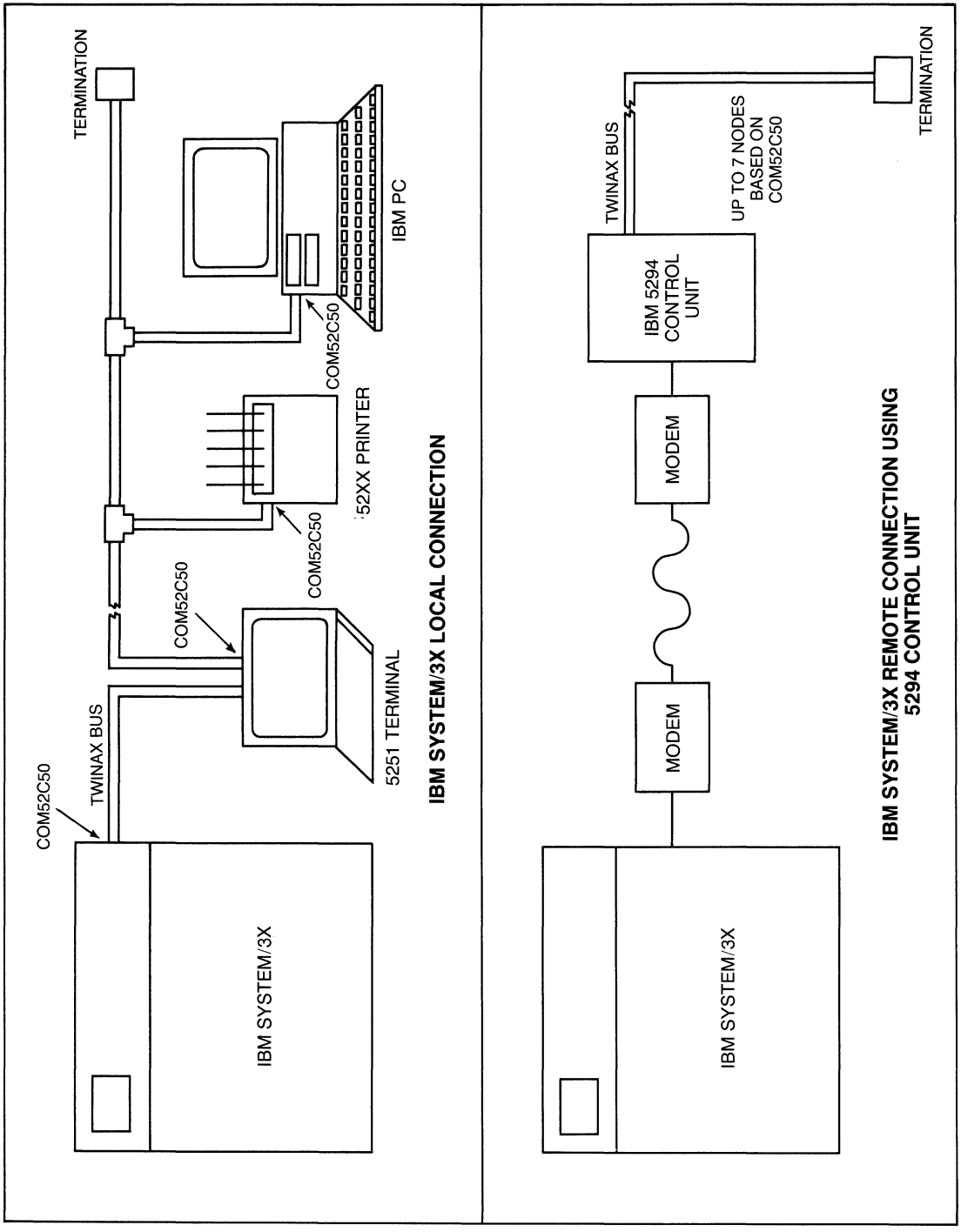


Fig. 19—RECOMMENDED EXTERNAL TTL CLOCK CONNECTION



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM 7210

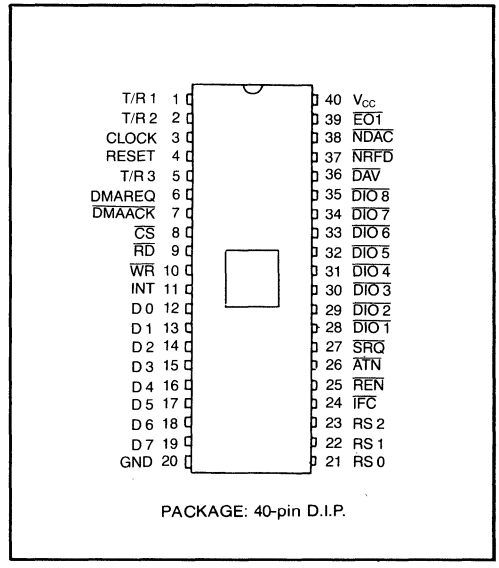
SECTION III

Intelligent GPIB Interface Controller

FEATURES

- ☐ All Functional Interface Capability Meeting IEEE Standard 488-1978
  - —SH1 (Source Handshake)
  - —AH1 (Acceptor Handshake)
  - —T5 or TE5 (Talker or Extended Talker)
  - —L3 or LE3 (Listener or Extended Listener)
  - —SR1 (Service Request)
  - —RL1 (Remote Local)
  - —PP1 or PP2 (Parallel Poll) (Remote or Local Configuration)
  - —DC1 (Device Clear)
  - —DT1 (Device Trigger)
  - —C1-5 ((Controller) (All Functions))
- ☐ Programmable Data Transfer Rate
- ☐ 16 MPU Accessible Registers—8 Read/8 Write
- ☐ 2 Address Registers
  - —Detection of MTA, MLA, MSA (My Talk/Listen/ Secondary Address)
  - —2 Device Addresses
- ☐ EOS Message Automatic Detection
- ☐ Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- ☐ DMA Capability
- ☐ Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- ☐ 1 to 8 MHz Clock Range
- ☐ TTL Compatible

PIN CONFIGURATION

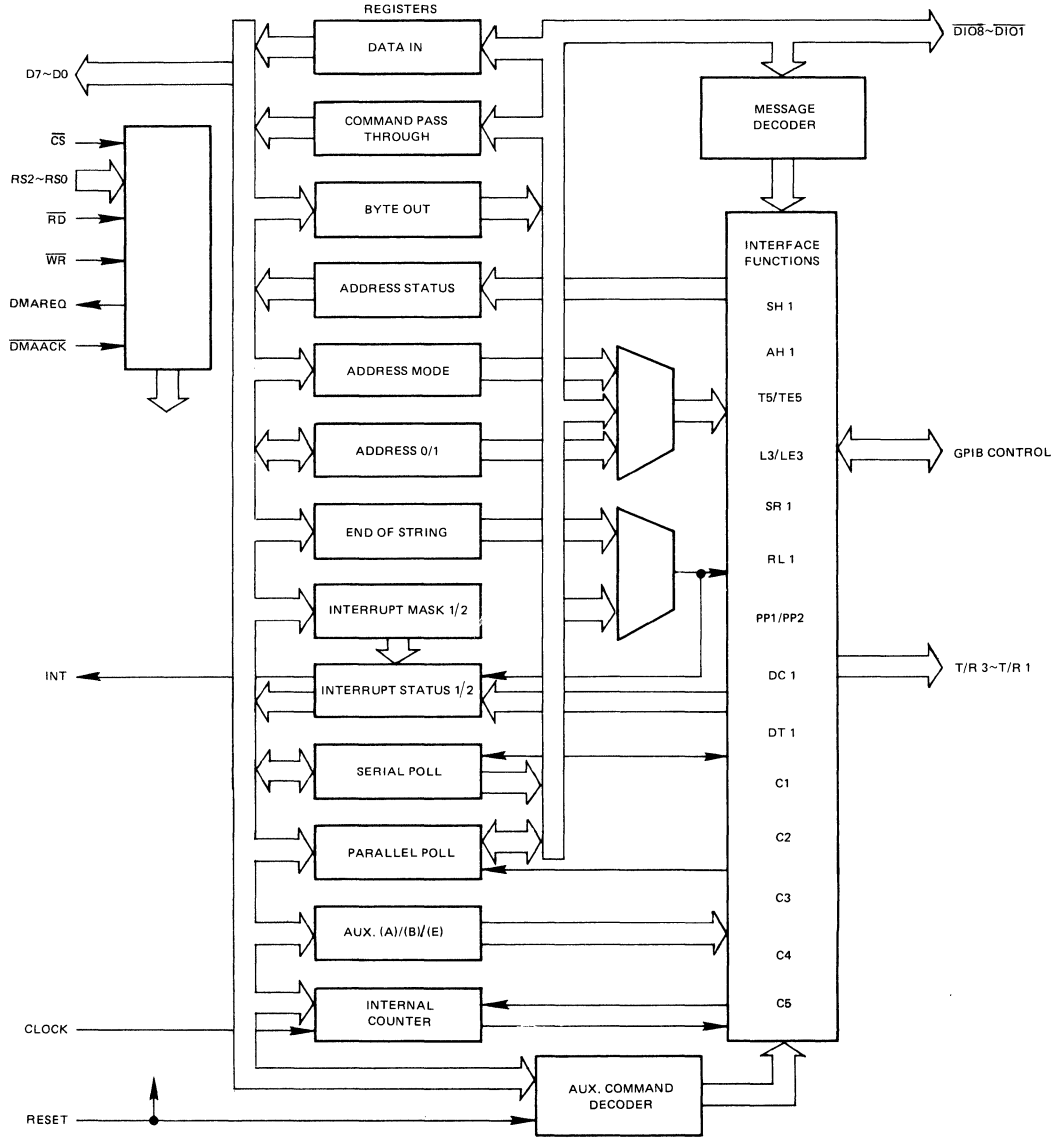


PACKAGE: 40-pin D.I.P.

- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ +5V Single Power Supply
- ☐ 40-Pin DIP
- ☐ 8080/85/86 Compatible

GENERAL DESCRIPTION

The COM7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.



BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN	SYMBOL	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control—Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control—The functions of T/R2, T/R3 are determined by the values of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock—(1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset—Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control—Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DMAREQ	O	DMA Request—7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal DACK.
7	$\overline{\text{DMAACK}}$	I	DMA Acknowledge—(Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{\text{CS}}$	I	Chip Select—(Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{\text{RD}}$	I	Read—(Active Low) Places contents of read register specified by RS0-2—on D0-7 (Computer Bus).
10	$\overline{\text{WR}}$	I	Write—(Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{\text{INT}}$	O	Interrupt Request—(Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus—8-bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select—These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{\text{IFC}}$	I/O	Interface Clear—Control line used for clearing the interface functions.
25	$\overline{\text{REN}}$	I/O	Remote Enable—Control line used to select remote or local control of the devices.
26	$\overline{\text{ATN}}$	I/O	Attention—Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{\text{SRQ}}$	I/O	Service Request—Control line used to request the controller for service.
28-35	$\overline{\text{DIO1-8}}$	I/O	Data Input/Output—8-bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{\text{DAV}}$	I/O	Data Valid—Handshake line indicating that data on DIO lines is valid.
37	$\overline{\text{NRFD}}$	I/O	Ready for Data—Handshake line indicating that device is ready for data.
38	$\overline{\text{NDAC}}$	I/O	Data Accepted—Handshake line indicating completion of message reception.
39	$\overline{\text{EOI}}$	I/O	End or Identify—Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC

FUNCTIONAL DESCRIPTION

Introduction

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The COM7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101-D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The COM7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

The COM7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor

overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

Internal Registers

The TLC has 16 registers, 8 of which are read and 8 write.

REGISTER NAME	ADDRESSING						SPECIFICATION							
	RS2	RS1	RS0	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$								
Data In (0R)	0	0	0	1	0	0	D17	D16	D15	D14	D13	D12	D11	D10
Interrupt Status 1 (1R)	0	0	1	1	0	0	CPT	APT	DET	END	DEC	ERR	D0	D1
Interrupt Status 2 (2R)	0	1	0	1	0	0	INT	SRQ1	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status (3R)	0	1	1	1	0	0	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status (4R)	1	0	0	1	0	0	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through (5R)	1	0	1	1	0	0	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 (6R)	1	1	0	1	0	0	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 (7R)	1	1	1	1	0	0	EO1	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out (0W)	0	0	0	0	1	0	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 (1W)	0	0	1	0	1	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 (2W)	0	1	0	0	1	0	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode (3W)	0	1	1	0	1	0	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode (4W)	1	0	0	0	1	0	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode (5W)	1	0	1	0	1	0	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 (6W)	1	1	0	0	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String (7W)	1	1	1	0	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Data Registers

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

Interrupt Registers

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related bits.

READ

INTERRUPT STATUS 1 (1R).	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT STATUS 2 (2R)	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 (1W)	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT MASK 2 (2W)	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

There are thirteen factors which can generate an interrupt from the COM7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

Serial Poll Registers

READ

SERIAL POLL STATUS (3R)	S8	PEND	S6	S5	S4	S3	S1	S0

WRITE

SERIAL POLL MODE (3W)	S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

Address Mode/Status Registers

ADDRESS STATUS (4R)	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS MODE (4W)	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The functions of T/R2, T/R3 terminals (2 and 5) are determined as below by the TRM1, TRM0 values of the address mode register.

T/R2	T/R3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC • $\overline{CSBS}$

This denotes the input/output of $\overline{EOI}$ terminal.

When "1": Output
When "0": Input

CIC = $\overline{CIDS + CADS}$

This denotes if the controller interface function is active or not.

When "1": $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When "0": $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + $\overline{PPAS}$

This indicates the type of bus driver connected to DI08 to DI01 and DAV lines.

When "1": 3 state type
When "0": Open collector type

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon RESET, TRM0 and TRM1 become "0" (TRM0 = TRM1 = 0) and local message port is provided, so that T/R2 and T/R3 both become "LOW."

Address Modes

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary (No controller on the GPIB)	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1 (A1)	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2 (A2)	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3 (A3)	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: (A1) —Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

(A2) —Address register 0 = primary, Address register 1 = secondary, interface function TE or LE.

(A3) —CPU must read secondary address via Command Pass Through Register interface function (TE or LE).

Address Status Bits

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

Address Registers

ADDRESS 0 (6R)	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 (7R)	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 (6W)	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

Address 0/1 Register Bit Selections

ARS —Selects which address register, 0 or 1

DT —Permits or Prohibits address to be detected as Talk

DL —Permits or Prohibits address to be detected as Listen

AD5-AD1 —Device address value

EOI —Holds the value of EOI line when data is received

Command Pass Through Register

COMMAND PASS THROUGH (5R)	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CP1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

End of String Register

END OF STRING (7W)	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block.

Aux Mode Register A controls the specific use of this register.

Auxiliary Mode Register

AUXILIARY MODE (5W)	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2 1 0	COM 4 3 2 1 0	OPERATION
0 0 0	C_4 C_3 C_2 C_1 C_0	Issues an auxiliary command specified by C_4 to C_0.
0 0 1	0 F_3 F_2 F_1 F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0 1 1	U S P_3 P_2 P_1	Makes write operation to the parallel poll register.
1 0 0	A_4 A_3 A_2 A_1 A_0	Makes write operation to the aux. (A) register.
1 0 1	B_4 B_3 B_2 B_1 B_0	Makes write operation to the aux. (B) register.
1 1 0	0 0 0 E_1 E_0	Makes write operation to the aux. (E) register.

Auxiliary Commands 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210

00000	iepon	— Immediate Execute pon—Generate local pon Message
00010	crst	— Chip Reset—Same as External Reset
00011	rrfd	— Release RFD
00100	trig	— Trigger
00101	rtl	— Return to Local Message Generation
00110	seoi	— Send EOI Message
00111	nvid	— Non Valid (OSA reception)—Release DAC Holdoff
01111	vid	— Valid (MSA reception, CPT, DEC, DET)—Release DAC Holdoff
0X001	sppf	— Set/Reset Parallel Poll Flag
10000	gts	— Go To Standby
10001	tca	— Take Control Asynchronously
10010	tcs	— Take Control Synchronously
11010	tcse	— Take Control Synchronously on End
10011	ltn	— Listen
11011	ltnc	— Listen with Continuous Mode
11100	lun	— Local Unlisten
11101	epp	— Execute Parallel Poll
1X110	sifc	— Set/Reset IFC
1X111	sren	— Set/Reset REN
10100	dsc	— Disable System Control

Internal Counter 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

Auxiliary A Register 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, 2 bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Modes
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME			FUNCTION
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

Auxiliary B Register 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME			FUNCTION
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	$\overline{INT}$	Specifies the active level of $\overline{INT}$ pin.
	0	INT	
B_4	1	ist = SRQS	SRQS indicates the value of ist level local message (the value of the parallel poll flag is ignored). SRQS = 1...ist = 1. SRQS = 0...ist = 0.
	0	ist = Parallel Poll Flag	The value of the parallel poll flag is taken as the ist local message.

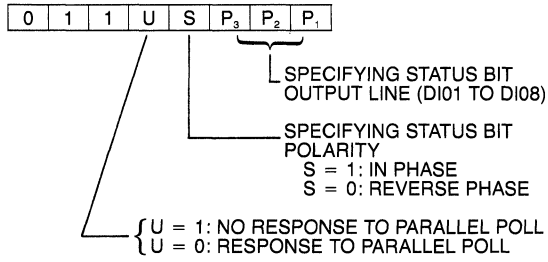
Auxiliary E Register 1 1 0 0 0 0 E_1 E_0

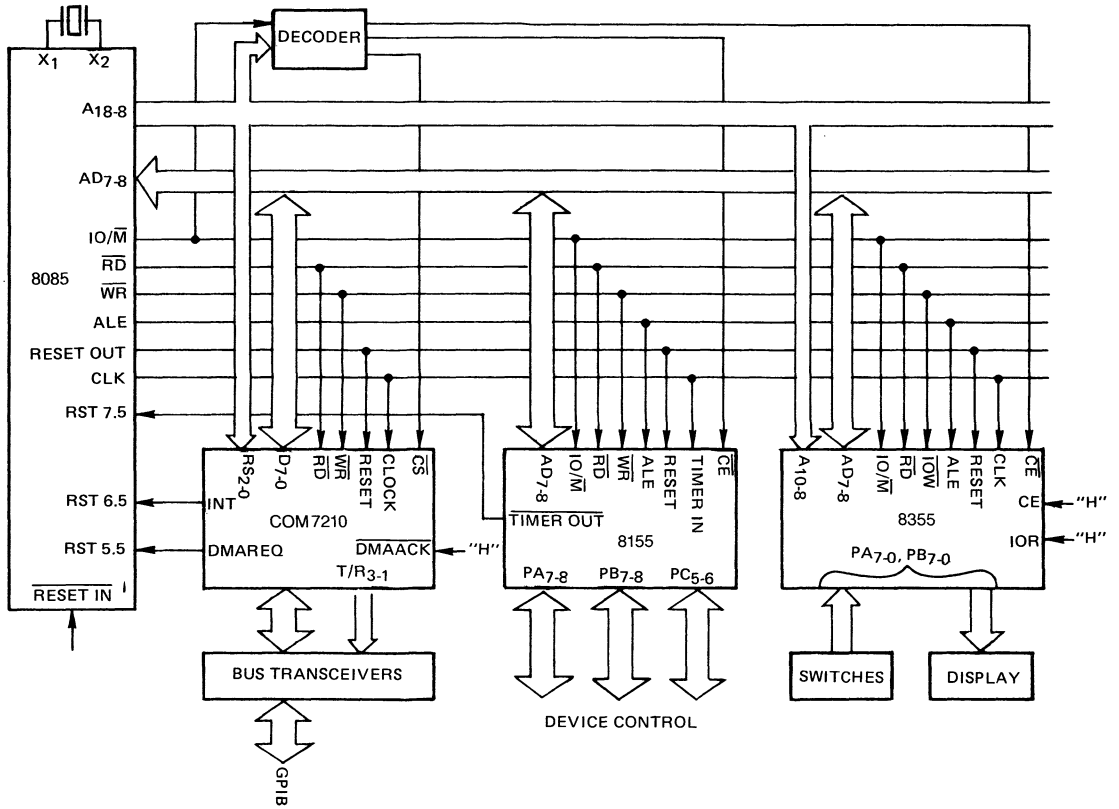
This register controls the Data Acceptance Modes of the TLC.

BIT			FUNCTION
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

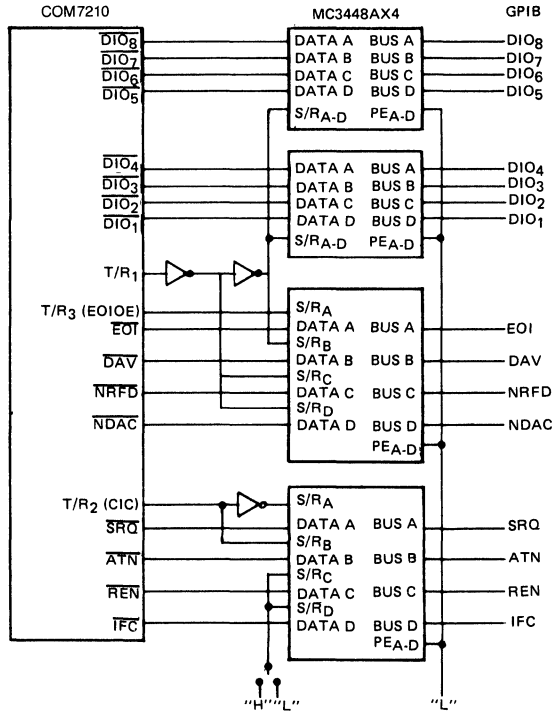
Parallel Poll Register

The Parallel Poll Register defines the parallel poll response of the COM7210.

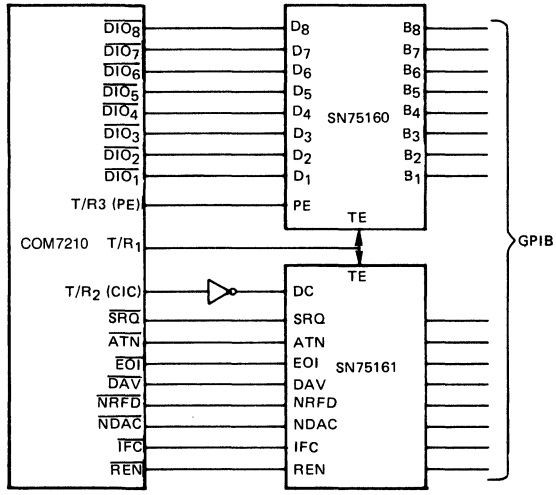




MINIMUM 8085 SYSTEM WITH COM7210



Note: In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0."

MINIMUM 8085 SYSTEM WITH COM7210 (CONT.)

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS (T_a = 25°C)

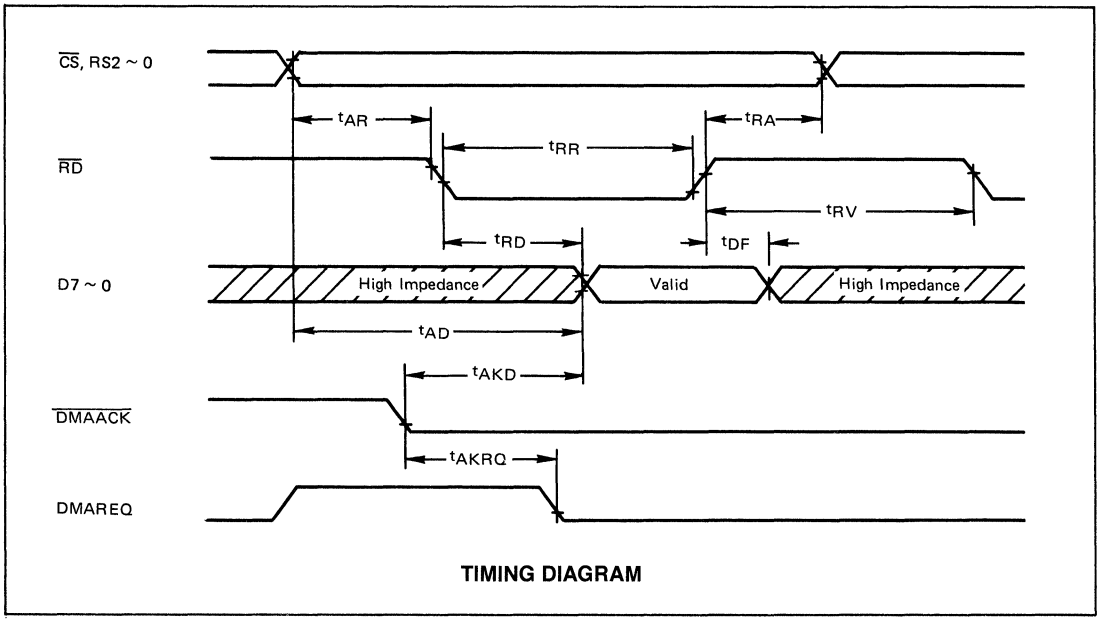
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	−0.5 ~ +7.0	V
Input Voltage	V_I	−0.5 ~ +7.0	V
Output Voltage	V_O	−0.5 ~ +7.0	V
Operating Temperature	T_{opt}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +125	°C

DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Input High Voltage	V_{IH}	+2.0		V_{CC} + 0.5	V	
Low Level Output Voltage	V_{OL}			+0.45	V	I_{OL} = 2 mA (4 mA: T/R1 Pin)
High Level Output Voltage	V_{OH1}	+2.4			V	I_{OH} = −400 μA (Except INT)
High Level Output Voltage (INT Pin)	V_{OH2}	+2.4 +3.5			V	I_{OH} = −400 μA I_{OH} = −50 μA
Input Leakage Current	I_{IL}	−10		+10	μA	V_{IN} = 0V ~ V_{CC}
Output Leakage Current	I_{OL}	−10		+10	μA	V_{OUT} = 0.45V ~ V_{CC}
Supply Current	I_{CC}			+180	mA	

CAPACITANCE (T_a = 25°C, V_{CC} = GND = 0V)

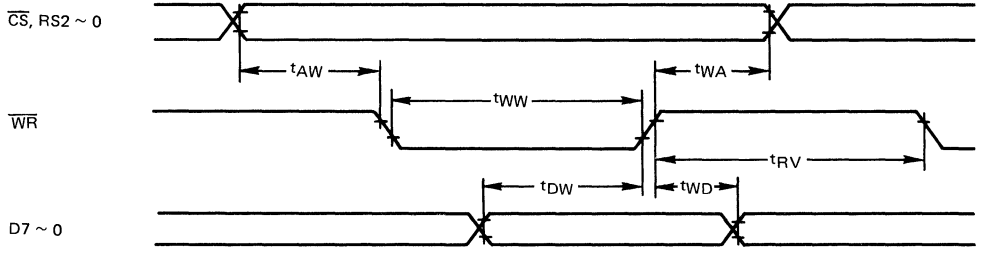
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground
I/O Capacitance	$C_{I/O}$			20	pF	



TIMING DIAGRAM

AC CHARACTERISTICS, (T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	CONDITIONS
$\overline{EOI}$ ↓ → $\overline{DIO}$	t_{EODI}		250	ns	PPSS → PPAS, ATN = True
$\overline{EOI}$ ↓ → T/R1 ↑	t_{EOT11}		155	ns	PPSS → PPAS, ATN = True
$\overline{EOI}$ ↑ → T/RI↓	t_{EOT12}		200	ns	PPAS → PPSS, ATN = False
$\overline{ATN}$ ↓ → $\overline{NDAC}$ ↓	t_{ATND}		155	ns	AIDS → ANRS, LIDS
$\overline{ATN}$↓ → T/R1 ↓	t_{ATT1}		155	ns	TACS + SPAS → TADS, CIDS
$\overline{ATN}$ ↓ → T/R2 ↓	t_{ATT2}		200	ns	TACS + SPAS → TADS, CIDS
$\overline{DAV}$ ↓ → DMAREQ	t_{DVRQ}		600	ns	ACRS → ACDS, LACS
$\overline{DAV}$ ↓ → $\overline{NFRD}$ ↓	t_{DVNR1}		350	ns	ACRS → ACDS
$\overline{DAV}$ ↓ → $\overline{NDAC}$ ↑	t_{DVND1}		650	ns	ACRS → ACDS → AWNS
$\overline{DAV}$ ↑ → $\overline{NDAC}$ ↓	t_{DVND2}		350	ns	AWNS → ANRS
$\overline{DAV}$ ↑ → $\overline{DRFD}$ ↑	t_{DVNR2}		350	ns	AWNS → ANRS → ACRS
$\overline{RD}$ ↓ → $\overline{NRFD}$ ↑	t_{RNR}		500	ns	ANRS → ACRS LACS, DI reg. selected
$\overline{NDAC}$ ↑ → DMAREQ ↑	t_{NDRQ}		400	ns	STRS → SWNS → SGNS, TACS
$\overline{NDAC}$ ↑ → $\overline{DAV}$ ↑	t_{NDDV}		350	ns	STRS → SWNS → SGNS
$\overline{WR}$ ↑ → $\overline{DIO}$	t_{WDI}		250	ns	SGNS → SDYS, BO reg. selected
$\overline{NRFD}$ ↑ → $\overline{DAV}$ ↓	t_{NRDV}		350	ns	SDYS → STRS, T_1 = True
$\overline{WR}$ ↑ → $\overline{DAV}$ ↓	t_{WDV}		830 + t_{SYNC}	ns	SGNS → SDYS → STRS BO reg. selected, RFD = True N_F = fc = 8 MHz, T_1 (High Speed)
TRIG Pulse Width	t_{TRIG}	50		ns	
Address Setup to $\overline{RD}$	t_{AR}	85		ns	RS0 ~ RS2
		0		ns	$\overline{CS}$
Address Hold from $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	170		ns	
Data Delay from Address	t_{AD}		250	ns	
Data Delay from $\overline{RD}$ ↓	t_{RD}		150	ns	
Output Float Delay from $\overline{RD}$ ↑	t_{DF}	0	80	ns	
$\overline{RD}$ Recovery Time	t_{RV}	250		ns	
Address Setup to $\overline{WR}$	t_{AW}	0		ns	
Address Hold from $\overline{WR}$	t_{WA}	0		ns	
$\overline{WR}$ Pulse Width	t_{WW}	170		ns	
Data Setup to $\overline{WR}$	t_{DW}	150		ns	
Data Hold from $\overline{WR}$	t_{WD}	0		ns	
$\overline{WR}$ Recovery Time	t_{RV}	250		ns	
DMAREQ ↓ Delay from $\overline{DMAACK}$	t_{AKRQ}		130	ns	
Data Delay from $\overline{DMAACK}$	t_{AKD}		200	ns	



TIMING DIAGRAM

STANDARD MICROSYSTEMS CORPORATION

35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM78C802
PRELIMINARY

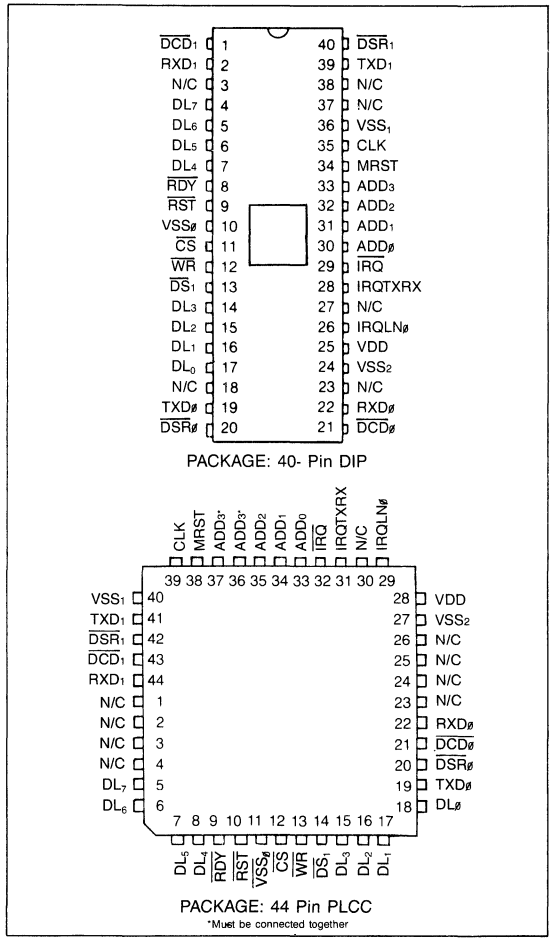
SECTION III

Two-channel Universal Asynchronous Receiver/Transmitter Dual UART

FEATURES

- ☐ Two independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers
- ☐ Single 5V Power Supply
- ☐ TTL Compatible
- ☐ Compatible with SMC COM78C808 OCTAL UART and COM78C804 QUART

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM78C802 Two-channel Asynchronous Receiver/Transmitter (Dual UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on two independent lines. Figure 1 is a functional block diagram of the COM78C802 Dual UART.

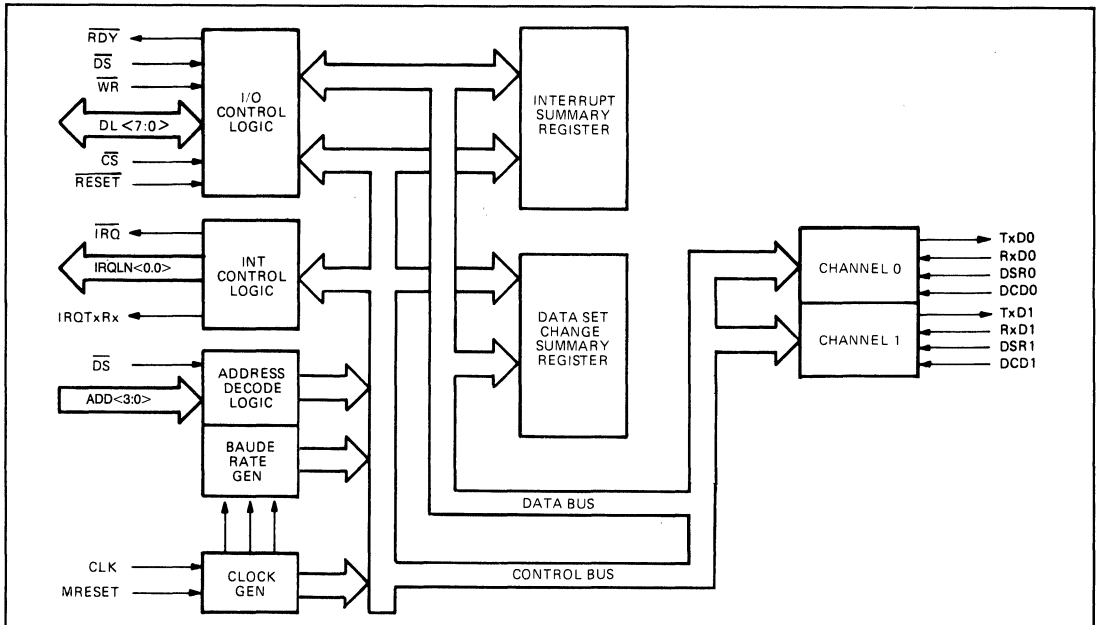


FIGURE 1: COM78C802 DUAL UART FUNCTIONAL BLOCK DIAGRAM

TABLE 1–COM78C802 PIN AND SIGNAL SUMMARY

Pin-PLCC	Pin-Dip	Signal	Input/Output	Definition/Function
5-8,15-18	4-7,14-17	DL<7:0>	input/output	Data lines <7:0>–Receives and transmits the parallel data.
33-37	30-33	ADD<3:0>	input	Address<3:0>–Selects the internal registers in the Dual UART. (Pins 36 and 37 must be connected in PLCC package.)
12	11	$\overline{CS}$	input	Chip select–Activates the Dual UART to receive and transmit data over the DL<7:0> lines.
14	13	$\overline{DS}$	input	Data strobe–Receives timing information for data transfers.
13	12	$\overline{WR}$	input	Write–Specifies direction of data transfer on the DL<7:0> lines.
9	8	$\overline{RDY}$	output	Ready–Indicates when the Dual UART is ready to participate in data transfer cycles.
10	9	RESET	input	Reset–Initializes the internal logic.
38	34	MRST	input	Manufacturing reset–For manufacturing use.
39	35	CLK	input	Clock–Clock input for timing.
20,42	20,40	$\overline{DSR}$<1:0>	inputs	Data set ready–Monitor data set ready (DSR) signals from modems.
21,43	1,21	$\overline{DCD}$<1:0>	inputs	Data set carrier detect–Monitor data set carrier detect (DCD) signals from modems.
32	29	IRQ	output	Interrupt request–Requests a processor interrupt.
29	26	IRQLN<C >	output	Interrupt request line number–Indicates the line number of originating interrupt request.
31	28	IRQTxRx	output	Interrupt request transmit/receive–Indicates whether an interrupt request is for transmitting or receiving data.
19,41	19,39	TxD<1:0>	outputs	Transmit data–Provides asynchronous bit-serial data output streams.
22,44	2,22	RxD<1:0>	input	Receive data–Accepts asynchronous bit-serial data input streams.
28	25	V_{DD}	input	Voltage–Power supply voltage +5 Vdc.
11,27,40	10,24,36	V_{SS}	input	Ground–Ground reference

DATA AND ADDRESS

Data lines (DL<7:0>)–These lines are used for the parallel transmission and reception of data between the CPU and the Dual UART. The receivers are active when the data strobe ($\overline{DS}$) signal is asserted. The output drivers are active only when the chip select ($\overline{CS}$) signal is asserted, the data strobe ($\overline{DS}$) signal is asserted, and the write ($\overline{WR}$) signal is deasserted. The drivers will become inactive (high-impedance) within 50 nanoseconds when one or more of the following occurs: the chip select ($\overline{CS}$) signal is deasserted, the data strobe ($\overline{DS}$) signal is deasserted, or the write ($\overline{WR}$) signal is asserted.

Address (ADD<3:0>)–These lines select which Dual UART internal register is accessible through the data I/O lines (DL<7:0>) when the data strobe ($\overline{DS}$) and chip select ($\overline{CS}$) signals are asserted. Table 2 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is deasserted, the address accesses the receiver buffer register and when asserted, it accesses the transmitter holding register.

SECTION III

TABLE 2–COM78C802 REGISTERS ADDRESS SELECTION

ADD Line* <3>	<2>	<1>	<0>	Read/Write	Register
0	0	0	0	Read	Line 0 Receiver Buffer
0	0	0	0	Write	Line 0 Transmitter Holding
0	0	0	1	Read	Line 0 Status
0	0	1	0	Read/Write	Line 0 Mode Registers 1,2
0	0	1	1	Read/Write	Line 0 Command
1	0	0	0	Read	Line 1 Receiver Buffer
1	0	0	0	Write	Line 1 Transmitter Holding
1	0	0	1	Read	Line 1 Status
1	0	1	0	Read/Write	Line 1 Mode Register 1,2
1	0	1	1	Read/Write	Line 1 Command
X	1	0	0	Read	Interrupt Summary
X	1	0	1	Read	Data Set Change Summary

*X = Either 0 or 1.

BUS TRANSACTION CONTROL

Chip select ($\overline{CS}$)–This signal is asserted to permit data transfers through the DL<7:0> lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS}$) signal and write ($\overline{WR}$) signal.

Data strobe ($\overline{DS}$)– This input receives timing information for data transfers. During a write cycle, the CPU asserts the data strobe signal when valid output data is available and deasserts the data strobe signal before the data is removed. During a read cycle, the CPU asserts the data strobe signal and the Dual UART transfers the valid data. When the data strobe signal is deasserted, the DL<7:0> lines become a high impedance.

Write ($\overline{WR}$)–The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL<7:0> pins. If the $\overline{WR}$ signal is asserted during a data transfer (the $\overline{CS}$ and $\overline{DS}$ signals asserted), the Dual UART is receiving data from DL<7:0>. If the $\overline{WR}$ signal is deasserted during a write data transfer, the Dual UART is driving data onto the DL<7:0> lines.

INTERRUPT REQUEST

Interrupt request $\overline{IRQ}$–The $\overline{IRQ}$ pin is an open drain output. The integral interrupt scanner asserts the IRQ signal when it has detected an interrupt condition on one of the two serial data lines.

Interrupt Request transmit/receive (IRQTxRx)—This signal indicates when the interrupt scanner in the Dual UART stops and asserts $\overline{IRQ}$ because of a transmitter interrupt condition (the IRQTxRx signal is asserted) or because of a receiver interrupt condition (the IRQTxRx signal is deasserted). The signal is valid only while $\overline{IRQ}$ is asserted. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

Interrupt request line number (IRQLN<0:0>)–This line indicates the line number at which the Dual UART interrupt scanner stopped and asserted the interrupt request ($\overline{IRQ}$) signal. The number on this line is valid only while the $\overline{IRQ}$ signal is asserted. The state of this signal also appears a bit in the interrupt summary register: IRQLN<0> as bit 1. Table 3 shows the line numbers corresponding to settings of IRQLN.

TABLE 3–COM78C802 INTERRUPT REQUEST LINE ASSIGNMENTS

IRQ Line	Line
0	0
1	1

SERIAL DATA

Transmit data (TxD<1:0>)–These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and a low level when the TxBRK bit in the associated line's command register is set.

Receive data (RxD<1:0>)–These lines accept asynchronous bit-serial data streams. The input signals must remain in the high state for at least one-half bit time before a high-to-low transition is recognized. (A high-to-low transition is required to signal the beginning of a "start" bit and initiate data reception).

MODEM SIGNALS

Data set ready ($\overline{DSR}$<1:0>)–These two input pins, one for each serial data line on the COM78C802, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the DSR bit (bit 7) in the corresponding line's status register to be asserted. A TTL high at a $\overline{DSR}$ pin causes the DSR bit in the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

Carrier detect (DCD<1:0>)–These two input pins, one for each serial data line of the Dual UART, are typically connected through intervening level converters to the received line signal detect (also called carrier detect) outputs of modems. A TTL low at a $\overline{DCD}$ pin causes the DCD bit of the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit corresponding to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

GENERAL CONTROL SIGNALS

Ready ($\overline{RDY}$)–The $\overline{RDY}$ pin is an open drain output. Upon detecting a negative transition of chip select ($\overline{CS}$), the Dual UART asserts the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deasserts after the trailing edge of $\overline{CS}$.I

Reset ($\overline{RESET}$)–When the $\overline{RESET}$ input in asserted, the TxD<1:0> lines are asserted and all internal status bits listed in the "Architecture Summary" discussion are cleared.

Manufacturing reset (MRESET)–This signal is for manufacturing use only and the input should be connected to ground for normal operation.

MISCELLANEOUS SIGNALS

Clock in (CLK)–All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1 percent and duty cycle is 50 percent ±5 percent.

POWER AND GROUND

Voltage (V_{DD})–Power supply 5 Vdc

Ground (V_{SS})–Ground reference

ARCHITECTURE SUMMARY

The Dual UART functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its two serial data lines (stop bits, parity, character length, split baud rates, etc.)

Each serial line functions the same as a one-line UART-type device thereby reducing the number of chips and conserving space on communication devices that require multiple communications lines.

An integral interrupt scanner checks for device interrupt conditions on the two lines. Its scanning algorithm gives priority to receivers over transmitters. The scanner can also check for interrupts resulting from changes in modem control signals $\overline{DSR}$ and $\overline{DCD}$.

Line-specific Registers

Each of the two serial data lines in the Dual UART has a set of registers for buffering data into and out of the line and for external control of the line's characteristics. These registers are selected for access by setting the appropriate address on lines ADD<3:0>. Lines ADD<4:3> select one of the two data lines. Lines ADD<2:0> selects the specific register for that line. Refer to Table 2 for the register address assignments.

Receiver buffer register–Each line's receiver consists of a character assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line's command register is set, received characters are moved automatically into the line's receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The assertion of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is asserted). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is deasserted) and the interrupt scanner resumes operation.

If there is another entry in a line's FIFO, the RxRDY bit remains asserted. When the interrupt scanner reaches this line again, the assertion of RxRDY causes the scanner to halt and assert the $\overline{IRQ}$ again.

Asserting the $\overline{RESET}$ signal or clearing the RxEN bit initializes the receiver logic of Dual UART. The RxRDY flag is cleared and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

Transmitter holding register–Each line has a writable transmitter holding register. When the TxEN bit in the line's command register is set, characters are moved automatically from the output of this register into the transmitter serialization logic whenever the serialization logic becomes idle.

When this register is empty, the TxRDY bit in the line's status register is set. If the transmitter interrupt enable (TxIE) bit in the line's command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared and the scanner resumes operation.

Assertion of the $\overline{\text{RESET}}$ signal initializes the transmitter logic of the Dual UART. The TxRDY flag is cleared and the transmitter holding register's contents are lost. The transmitter enable (TxEN) bit in the line's command register is also cleared by $\overline{\text{RESET}}$. If at the end of the reset process, the TxEN is reasserted and TxRDY bit is reasserted. Software clearing of TxEN alone produces results different from the full $\overline{\text{RESET}}$ in that the transmitter holding register's contents are not lost; they are transmitted when TxEN is set again.

Status register–Each line has a read-only status register that provides information about the current state of the given line. This register indicates a line's readiness for transmission or reception of data and flags error conditions in its bit fields. Figure 3 shows the format of the status register. Table 3 lists the flag bits in each status register.

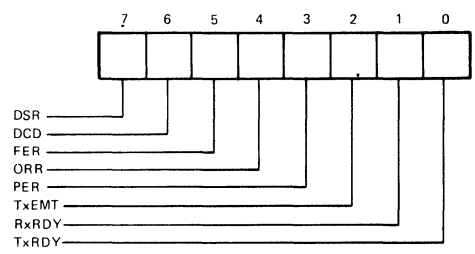


FIGURE 3: COM78C802 STATUS REGISTERS (LINE 0:1) FORMAT

SECTION III

TABLE 4–COM78C802 STATUS REGISTERS (LINES 0-1) DESCRIPTION

Bit	Description
7	DSR (Data set ready)–This bit is the inverted state of the $\overline{\text{DSR}}$ line.
6	DCD (Data set carrier detect)–This bit is the inverted state of the $\overline{\text{DCD}}$ line.
5	FER (Frame error)–Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error)–Set when the character in the receiver buffer register was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity error)–If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{\text{RESET}}$ input, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter empty)–Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmitter holding register. Cleared by loading the transmitter holding register, by clearing TxEN (0) of the command register, or by asserting the $\overline{\text{RESET}}$ input.
1	RxRDY (Receiver buffer ready)–When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by asserting the $\overline{\text{RESET}}$ input.
0	TxRDY (Transmitter holding register ready)—When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or by asserting the $\overline{\text{RESET}}$ input. This bit is initially set when the transmitter logic is enabled by the setting of TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

Mode registers 1 and 2—These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the two communications lines has two of these registers, both accessed by the same address on ADD<3:0>. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1, the next address mode register 2, and another after that would recycle the pointer to mode register 1. The pointer is reset to point to mode register 1 by $\overline{\text{RESET}}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles.

Figure 4 shows the format of mode registers 1 and Table 5 describes the function of the register information.

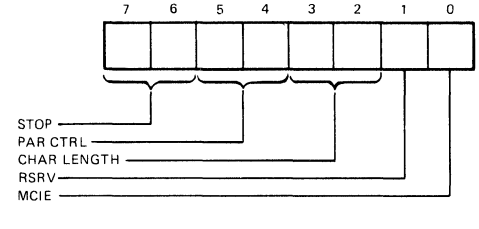


FIGURE 4–COM78C802 MODE REGISTERS 1 (LINE 0:1) FORMAT

TABLE 5–COM78C802 MODE REGISTERS 1 (LINES 0-1) DESCRIPTION

Bit	Description
7,6	STOP–These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by asserting the RESET input. **Bits** **Stop Bits** **7 6** 0 0 Invalid 0 1 1.0 1 0 1.5 1 1 2.0
5,4	PAR CTRL (Parity control)–These bits determine parity as follows and are cleared by asserting the RESET input. X = either 1 or 0. **Bits** **Parity Type** **5 4** 1 1 Even 0 1 Odd X 0 Disabled
3,2	CHAR LENGTH (Character length)–These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by asserting the RESET input. The character length bits are defined as follows: **Bit** **Bit Length** **3 2** 0 0 5 0 1 6 1 0 7 1 1 8
1	RSRV (Reserved and cleared by asserting the RESET input.)
0	MCIE (Modem control interrupt enable)–When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the Interrupt Scanner and Interrupt Handling information. Cleared by asserting the RESET input.

Figure 5 shows the format of mode registers 2 and Table 6 indicates the baud rate selections of the register. Bits 7 through 4 of the mode register 2 control the transmitter baud rate and bits 3 through 0 control the receiver baud rate. These registers are cleared by asserting RESET input.

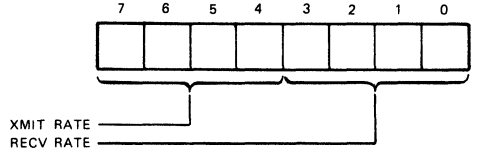


FIGURE 5–COM78C802 MODE REGISTERS 2 (LINE 0-1) FORMAT

Command register–These read/write registers control various functions on the selected line. Figure 6 shows the format of the command registers and Table 7 describes the function of the register information.

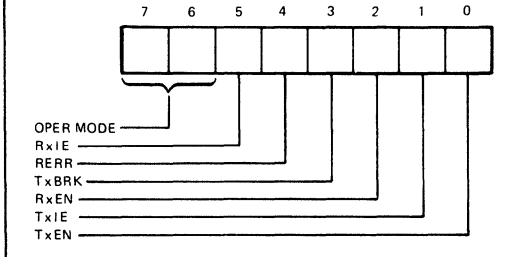


FIGURE 6–COM78C802 COMMAND REGISTERS (LINE 0-1) FORMAT

TABLE 6–COM78C802 MODE REGISTERS 2 (LINES 0-1) DESCRIPTION

Bit	Description
7:0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate)–Selects the baud rate of the transmitter (bits 7:4) and receiver (bits 3:0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error*
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
0	0	0	0	0	0	0	0	50	same	—
0	0	0	1	0	0	0	1	75	same	—
0	0	1	0	0	0	1	0	110	109.09	0.826
0	0	1	1	0	0	1	1	134.5	133.33	0.867
0	1	0	0	0	1	0	0	150	same	—
0	1	0	1	0	1	0	1	300	same	—
0	1	1	0	0	1	1	0	600	same	—
0	1	1	1	0	1	1	1	1200	same	—
1	0	0	0	1	0	0	0	1800	1745.45	3.03
1	0	0	1	1	0	0	1	2000	2021.05	1.05
1	0	1	0	1	0	1	0	2400	same	—
1	0	1	1	1	0	1	1	3600	3490.91	3.03
1	1	0	0	1	1	0	0	4800	same	—
1	1	0	1	1	1	0	1	7200	6981.81	3.03
1	1	1	0	1	1	1	0	9600	same	—
1	1	1	1	1	1	1	1	19200	same	—

*The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1 percent. This variance results in an error that must be added to the error listed.

TABLE 7–COM78C802 COMMAND REGISTERS (LINES 0-1) DESCRIPTION

Bit	Description
7,6	OPER MODE (Operating mode)–These bits control the operating mode of the channel as follows. These bits are cleared by asserting the RESET input. **Bit 7 / Bit 6 — Operating Mode** 0 0 — Normal operation 0 1 — Automatic echo 1 0 — Local loopback 1 1 — Remote loopback
5	RxIE (Receiver interrupt enable)–When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset error)–When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by asserting the RESET input (not self-clearing).
3	TxBRK (Transmit break)–When set, this bit forces the appropriate TxD<1:0> line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by asserting the RESET input.
2	RxEN (Receiver enable)–When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by asserting the RESET input.
1	TxIE (Transmit interrupt enable)–When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is asserted and generates an interrupt by asserting the IRQ signal.
0	TxEN (Transmitter enable)–When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with this line, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by asserting the RESET input.

Bits 5 through 0 enable the line's receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to "Interrupt Scanner" and "Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are:

- ☐ Normal operation–The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. (The RxEN bit must be set.) Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. (The TxEN bit must be set.)

- ☐ Automatic echo–The serial data received is assembled into parallel in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxD<n> pin for serial output. TxEN is ignored and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.
- ☐ Local loopback–The serial data from the RxD<n> input is ignored and the receiver serial input receives data from the transmitter serial output. The data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. (The TxEN bit must be set.) The transmission goes only to the receiver serial input; the TxD<n> output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.
- ☐ Remote loopback–The serial data received on the RxD<n> line is returned to the TxD<n> line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

SUMMARY REGISTERS

The Dual UART contains two registers that summarize the current status of all two serial data lines, making it possible to determine that a line's status has changed with a single read operation. These registers are selected for access by setting the appropriate address on pins ADD <2:0>. Because the registers are shared by two serial lines, the line-selection bits (ADD <4:3>) are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

Interrupt summary register–This read-only register indicates that a transmitter or receiver interrupt condition has occurred, and indicates the line number that generated the interrupt. Figure 7 shows the format of the interrupt summary register and Table 8 describes register information.

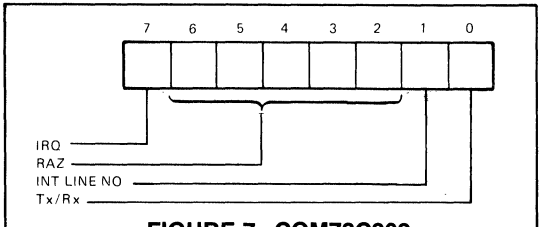


FIGURE 7–COM78C802 INTERRUPT SUMMARY REGISTER FORMAT

TABLE 8–COM78C802 INTERRUPT SUMMARY REGISTER DESCRIPTION

Bit	Description
7	IRQ (Interrupt request)–When set, this bit indicates that the interrupt scanner has found an interrupting condition among the two serial lines of the Dual UART. These conditions also result in the Dual UART asserting the $\overline{IRQ}$ signal.
6:2	RAZ (Read as zero)–Not used
1*	INT LINE NO (Interrupting line number)–This bit indicates the line number upon which an interrupting condition was found. Refer to Table 3.
0*	Tx/$\overline{Rx}$ (Transmit/receive)–This bit indicates whether the interrupting condition was caused by a transmitter (Tx/$\overline{Rx}$ equals 1) or a receiver (Tx/$\overline{Rx}$ equals 0). This bit corresponds to the IRQTxRx signal of the Dual UART and is set when IRQTxRx is asserted.

*Bits 1-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

Data set change summary register–When the $\overline{DSR}$ or $\overline{DCD}$ inputs that are associated with a line change state, the bit corresponding to that line in this read-only register is set. The current state of the $\overline{DSR}$ and $\overline{DCD}$ inputs can then be obtained from that line's status register. If the state of a line changes twice within one microsecond, the change in state may not be detected. Figure 8 shows the format of the data set change summary register.

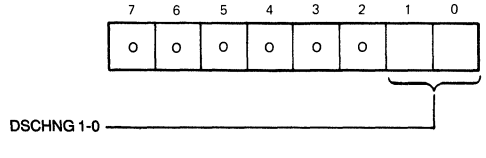


FIGURE 8–COM78C802 DATA SET CHANGE SUMMARY REGISTER FORMAT

When the MCIE bit in a line's mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and assert the $\overline{IRQ}$ signal. The data set change summary register bits are cleared by writing a 1 into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled and writeback should directly follow the read operation.

Assertion of the $\overline{RESET}$ signal disables and initializes the data set change logic. When the $\overline{RESET}$ signal is deasserted, future changes in $\overline{DSR}$ and $\overline{DCD}$ are reported as they occur.

INTERRUPT SCANNER AND INTERRUPT HANDLING

The interrupt scanner sequentially checks each line for a receive interrupt and then checks each one in the same order for a transmitter interrupt. If the scanner detects an interrupt condition, it stops and the $\overline{IRQ}$ signal is asserted. An interrupt must be serviced by software or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line's receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = 1) or either of the line's modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG and RxIE and MCIE = 1).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE = 1).

When the scanner detects an interrupt, it reports the line number on the IRQ<0> line. The IRQTxRx signal is asserted for a transmitter interrupt and deasserted for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line is deasserted and the scanner is restarted for each of the following three types of interrupt conditions.

- ☐ Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- ☐ Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- ☐ Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line 0's receiver), thus giving receivers priority over transmitters.

EDGE-TRIGGERED AND LEVEL-TRIGGERED INTERRUPT SYTSTEMS

If the interrupt system of the Dual UART is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

MODEM HANDLING

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deasserting the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The assertion of the TxEMT bit to indicate the transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to assert before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character (a starter bit–5,6,7, or 8 data bits; plus parity bit if enabled; and 1,1.5, or 2 stop bits), and multiplying by either two characters or one, depending on when TxEMT monitoring begins.

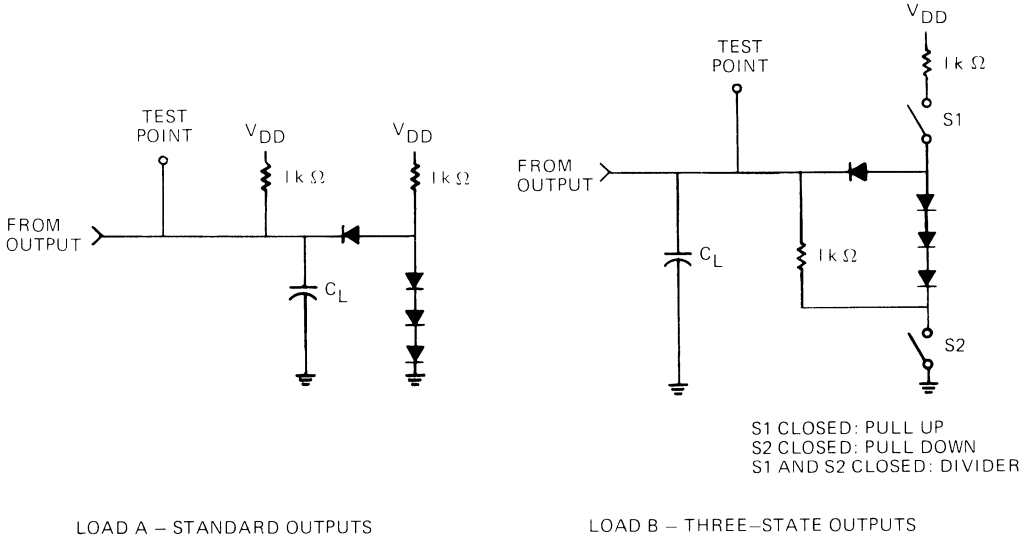


FIGURE 9–COM78C802 OUTPUT LOAD CIRCUITS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +125°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... V_{CC} +0.3V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

TABLE 9–COM78C802

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Requirements Min.	Typ.	Max.	Units
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{DD} = Min. I_{OH} = 3.5 mA for DL<7:0> I_{DH} = 2.0 mA for all remaining output except $\overline{IRQ}$ and RDY	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = Min. I_{OL} = 5.5 mA for DL<7:0> I_{OL} = 3.5 mA for all remaining outputs			0.4	V
I_{IH}	Input current at maximum input voltage	V_{DD} = Max. $V_I = V_{DD}$(Max.)			10	µA
I_{IL}	Input current at miminum input voltage	V_{DD} = Max. V_I = 0.0V			−10	µA
I_{OS}[1]	Short-circuit output current for DL<7:0> all remaining outputs except IRQ and RDY	V_{DD} = Max.	−50 −30		−180 −110	mA mA
I_{OZL}[2]	Three-state output current	V_{DD} = Max. V_O = 0.4V			10	µA
I_{OZH}[2]	Three-state output current	V_{DD} = Max. V_O = 2.4V			10	µA
I_{DD}	Supply current	V_{DD} = Max. T_A = 0°		15		mA
C_{in}	Input capacitance				4	pF
C_{IO}[3]	Input/output capacitance				5	pF

[1]No more than one ouput should be short circuited at a time, and the duration of the short should not exceed 1 second.
[2]All three-state output drivers are wired in an I/O configuration. The parameters include the driver and input receiver leakage currents.
[3]The parameters include the capacitive loads of the output driver and the input receiver.

TIMING PARAMETERS

Figure 10 shows the signal timing for a read cycle to transfer information from the Dual UART to the processor. Figure 11 shows the signal timing for a write cycle to transfer information from the processor to the Dual UART. Table 11 lists the timing parameters for the read and write cycles.

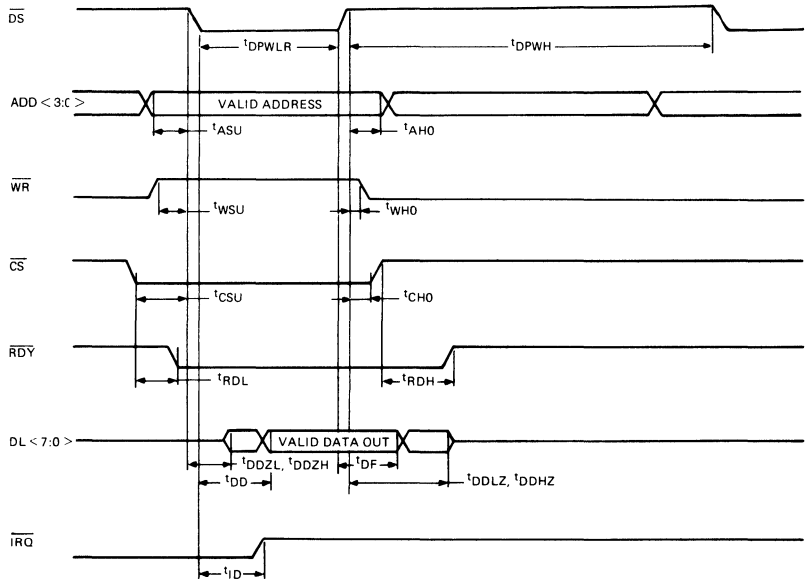


FIGURE 10–COM78C802 BUS READ CYCLE TIMING

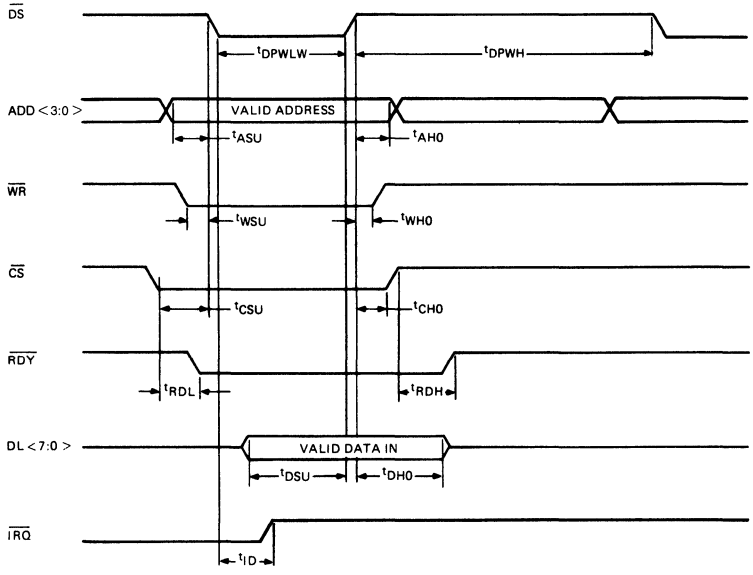


FIGURE 11–COM78C802 BUS WRITE CYCLE TIMING

TABLE 10–COM78C802 BUS READ AND WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Max.	Load Circuit[1]
t_{AHO}	Hold time of a valid ADD <3:0> to a valid high level of $\overline{DS}$.	10		
t_{ASU}	Setup time of a valid ADD <3:0> to the falling edge of $\overline{DS}$.	30		
t_{CHO}	Hold time of a valid low level of $\overline{CS}$ to a valid high level of $\overline{DS}$.	10		
t_{CSU}	Setup time of a valid low level of $\overline{CS}$ to the falling edge of $\overline{DS}$.	30		
t_{DD}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to valid high or low data on DL <0>.	165		$C_L = 150$ pF
t_{DDLZ}[2]	Propagation delay of a valid high level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <0> output drivers disabled.			
	t_{DDLZ}		50	$C_L = 50$pF
	t_{DDHZ}		50	$C_L = 50$pF
	t_{DDLZ}		60	$C_L = 100$pF
	t_{DDHZ}		60	$C_L = 100$pF
	t_{DDLZ}		65	$C_L = 150$pF
	t_{DDHZ}		65	$C_L = 150$pF
t_{DDZL}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output driver enabled.			
	t_{DDZL}		165	$C_L = 150$pF
	t_{DDZH}	0	165	$C_L = 150$pF
t_{DF}	Hold time provided during a read cycle by Dual UART of valid high or low data on DL <7:0> after the rising edge of $\overline{DS}$.	0		
t_{DHO}	Hold time of a valid DL <7:0> to a valid high level of $\overline{DS}$.	30		
t_{DPWH}	Pulse width high of $\overline{DS}$.	450		
t_{DPWLR}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is high (read operation). Refer to timing parameter t_{DPWLW} also.	180	10,000	
t_{DPWLW}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is low (write operation). Refer to timing parameter t_{DPWLR} also.	130	10,000	
t_{DSU}	Setup time of a valid DL <7:0> to the rising edge of $\overline{DS}$.	50		
t_{ID}[3]	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low) to a high level on $\overline{IRQ}$.		635	$C_L = 50$pF
t_{RDH}[4]	Propagation delay of a valid high level of $\overline{CS}$ to a valid high level on $\overline{RDY}$.		210	$C_L = 50$pF
t_{RDL}	Propagation delay of a valid low level on $\overline{CS}$ to a valid low level on $\overline{RDY}$.		90	$C_L = 50$pF
t_{WHO}	Hold time of a valid high or low level of $\overline{WR}$ to a valid high level of $\overline{DS}$.	10		
t_{WSU}	Setup time of a valid high or low level of $\overline{WR}$ to the falling edge of $\overline{DS}$.	30		

[1]Refer to Figure 9 for the load circuits used with these measurements.
[2]The t_{DDLZ} and t_{DDHZ} parameters are measured with $C_L = 150$ pF. The values of t_{DDLZ} and t_{DDHZ} for $C_L = 50$pF and $C_L = 100$ pF have been derived for user convenience.
[3]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{ID} parameter can be calculated by the following: $t_{ID} = 500 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.
[4]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{RDH} parameter can be calculated by the following: $t_{RDH} = 75 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.

Figure 12 shows the signal timing for the clock input, interrupt timing, effect of the $\overline{RESET}$ input on data strobe, data set carrier detect (DCD) and data set ready (DSR) input timing, and the transmit data output timing. Table 11 lists the timing parameters for Figure 12.

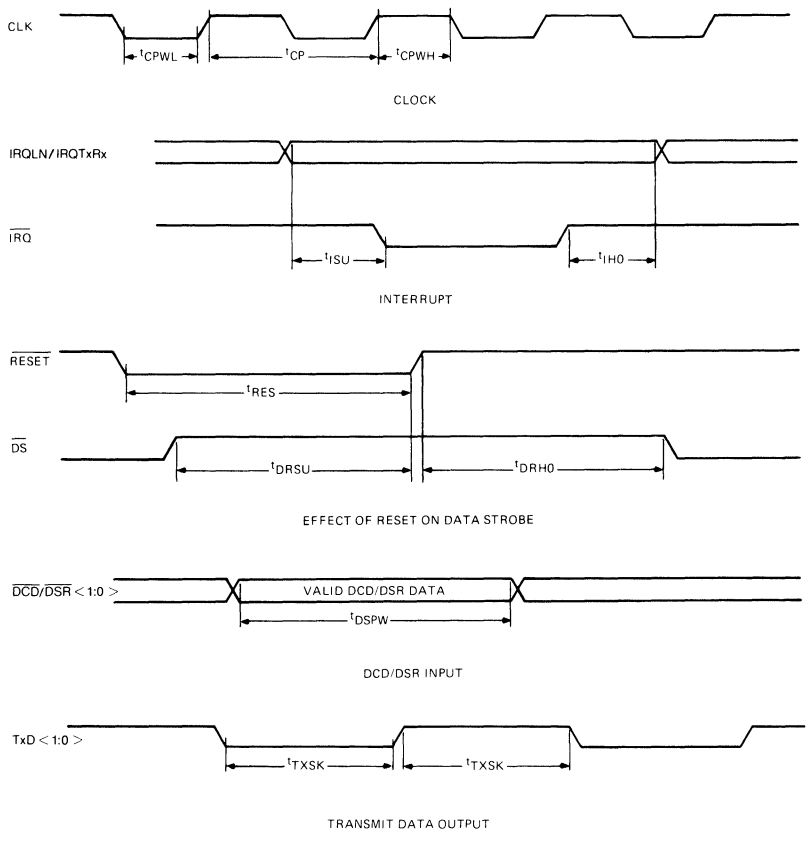


FIGURE 12–COM78C802 MISCELLANEOUS SIGNAL TIMING

TABLE 11–MISCELLANEOUS WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Load Circuit*
t_{CP}	Period of CLK.	203.45 (4.9152 MHz)	
t_{CPWH}	Pulse width high of CLK.	95	
t_{CPWL}	Pulse width low of CLK.	95	
t_{DRHO}	Hold time of a valid high level of $\overline{DS}$ to a valid high level of $\overline{RESET}$.	1,000	
t_{DRSU}	Setup time of a valid high level of $\overline{DS}$ to the rising edge of $\overline{RESET}$.	900	
t_{DSPW}	Pulse width high or low of DCD <1:0> and DSR <1:0>.	1,000	
t_{IHO}	Hold time provided by Dual UART from a valid IRQLN and IRQTxRx to a valid high level of IRQ.	100	$C_L = 50pF$
t_{ISU}	Setup time provided by Dual UART from a valid IRQLN and IRQTxRx to a valid low level of $\overline{IRQ}$.	100	$C_L = 50pF$
t_{RES}	Pulse width low of $\overline{RESET}$.	1,000	
t_{TXSK}	Pulse width high or low provided by Dual UART on the TxD <1:0> lines. At each baud rate, the actual pulse widths provided vary by t_{TXSK}. This timing parameter should be used to determine cumulative reception/transmission errors.	250	$C_L = 50pF$

*Refer to Figure 9 for the load circuits used with these measurements.

Figure 13 shows the input and output voltage waveforms for the propagation delay and setup and hold measurements. Figure 14 shows the waveforms for the three-state outputs measurement.

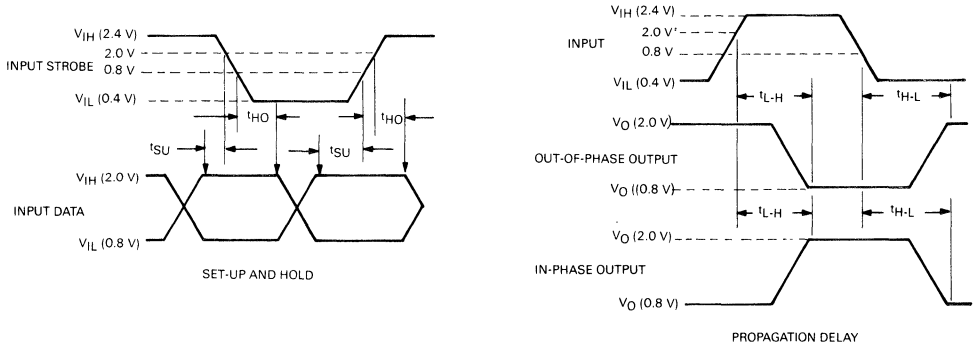
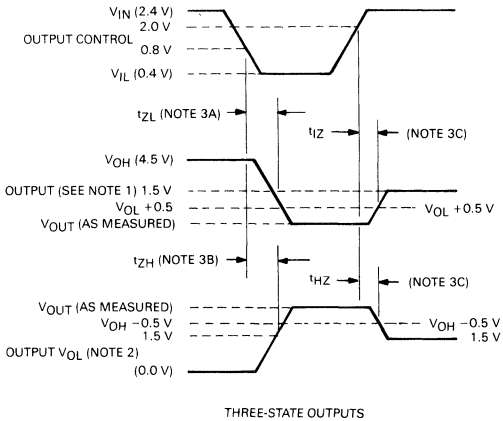


FIGURE 13–COM78C802 PROPAGATION DELAY AND SETUP AND HOLD VOLTAGE WAVEFORMS



THREE-STATE OUTPUTS

NOTES:
1. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
2. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
3. REFER TO FIGURE 9. A = S1 CLOSED, B = S2 CLOSED, C = S1 AND S2 CLOSED.

FIGURE 14–COM78C802 THREE-STATE OUTPUT VOLTAGE WAVEFORMS

STANDARD MICROSYSTEMS CORPORATION

COM78C804
PRELIMINARY

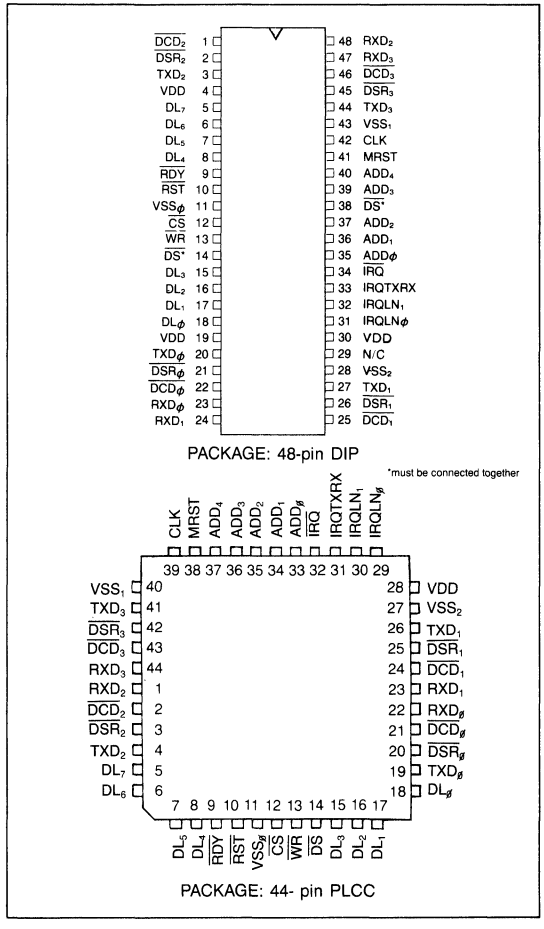
SECTION III

Four-channel Universal Asynchronous Receiver/Transmitter Quad UART

FEATURES

- ☐ Four independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers
- ☐ Single 5V Power Supply
- ☐ TTL Compatible
- ☐ Low Power CMOS Technology
- ☐ Compatible with SMC's COM78C808 and COM78C802

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM78C804 Four-channel Asynchronous Receiver/Transmitter (Quad UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on four independent lines. Figure 1 is a functional block diagram of the COM78C804 Quad UART.

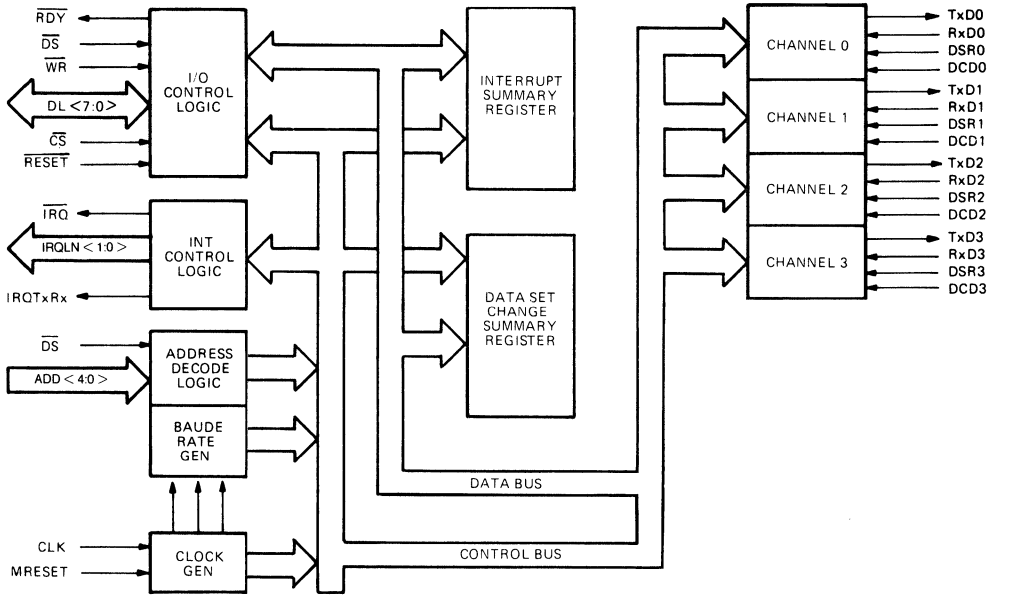


FIGURE 1: COM78C804 QUAD UART FUNCTIONAL BLOCK DIAGRAM

TABLE 1–COM78C804 PIN AND SIGNAL SUMMARY

Pin-PLCC	Pin-DIP	Signal	Input/Output	Definition/Function
5-8,15-18	5-8,15-18	DL<7:0>	input/output	Data lines <7:0>–Receives and transmits the parallel data.
33-37	35-37,39,40	ADD<0:4>	input	Address<0:4>–Selects the internal registers in the Quad UART.
12	12	$\overline{CS}$	input	Chip select–Activates the Quad UART to receive and transmit data over the DL<7:0> lines.
14	14,38	$\overline{DS}$	input	Data strobe–Receives timing information for data transfers.
13	13	$\overline{WR}$	input	Write–Specifies direction of data transfer on the DL<7:0> lines.
9	9	$\overline{RDY}$	output	Ready–Indicates when the Quad UART is ready to participate in data transfer cycles.
10	10	$\overline{RESET}$	input	Reset–Initializes the internal logic.
38	41	MRESET	input	Manufacturing reset–For manufacturing use.
39	42	CLK	input	Clock–Clock input for timing.
3,20,25,42	2,21,26,45	$\overline{DSR}$<3:0>	inputs	Data set ready–Monitor data set ready (DSR) signals from modems.
2,21,24,43	1,22,25,46	$\overline{DCD}$<3:0>	inputs	Data set carrier detect–Monitor data set carrier detect (DCD) signals from modems.
32	34	$\overline{IRQ}$	output	Interrupt request–Requests a processor interrupt.
29,30	31,32	IRQLN<0:1>	output	Interrupt request line number–Indicates the line number of originating interrupt request.
31	33	IRQTxRx	output	Interrupt request transmit/receive–Indicates whether an interrupt request is for transmitting or receiving data.
4,19,26,41	3,20,27,44	TxD<3:0>	outputs	Transmit data–Provides asynchronous bit-serial data output streams.
1,22,23,44	23,24,47,48	RxD<3:0>	input	Receive data–Accepts asynchronous bit-serial data input streams.
28	4,19,30	V_{DD}	input	Voltage–Power supply voltage +5 Vdc.
11,27,40	11,28,43	V_{SS}	input	Ground–Ground reference

DATA AND ADDRESS

Data lines (DL<7:0>)–These lines are used for the parallel transmission and reception of data between the CPU and the Quad UART. The receivers are active when the data strobe ($\overline{DS}$) signal is asserted. The output drivers are active only when the chip select ($\overline{CS}$) signal is asserted, the data strobe ($\overline{DS}$) signal is asserted, and the write ($\overline{WR}$) signal is deasserted. The drivers will become inactive (high-impedance) within 50 nanoseconds when one or more of the following occurs: the chip select ($\overline{CS}$) signal is deasserted, the data strobe ($\overline{DS}$) signal is deasserted, or the write ($\overline{WR}$) signal is asserted.

Address (ADD<4:0>)–These lines select which Quad UART internal register is accessible through the data I/O lines (DL<7:0>) when the data strobe ($\overline{DS}$) and chip select ($\overline{CS}$) signals are asserted. Table 2 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is deasserted, the address accesses the receiver buffer register and when asserted, it accesses the transmitter holding register.

TABLE 2–COM78C804 REGISTERS ADDRESS SELECTION

ADD Line* <4>	<3>	<2>	<1>	<0>	Read/Write	Register
0	0	0	0	0	Read	Line 0 Receiver Buffer
0	0	0	0	0	Write	Line 0 Transmitter Holding
0	0	0	0	1	Read	Line 0 Status
0	0	0	1	0	Read/Write	Line 0 Mode Registers 1,2
0	0	0	1	1	Read/Write	Line 0 Command
0	1	0	0	0	Read	Line 1 Receiver Buffer
0	1	0	0	0	Write	Line 1 Transmitter Holding
0	1	0	0	1	Read	Line 1 Status
0	1	0	1	0	Read/Write	Line 1 Mode Register 1,2
0	1	0	1	1	Read/Write	LIne 1 Command
1	0	0	0	0	Read	Line 2 Receiver Buffer
1	0	0	0	0	Write	Line 2 Transmitter Holding
1	0	0	0	1	Read	Line 2 Status
1	0	0	1	0	Read/Write	Line 2 Mode Register 1,2
1	0	0	1	1	Read/Write	Line 2 Command
1	1	0	0	0	Read	Line 3 Receiver Buffer
1	1	0	0	0	Write	Line 3 Transmitter Holding
1	1	0	0	1	Read	Line 3 Status
1	1	0	1	0	Read/Write	Line 3 Mode Register 1,2
1	1	0	1	1	Read/Write	Line 3 Command
X	X	1	0	0	Read	Interrupt Summary
X	X	1	0	1	Read	Data Set Change Summary

*X = Either 0 or 1.

BUS TRANSACTION CONTROL

Chip select ($\overline{CS}$)–This signal is asserted to permit data transfers through the DL<7:0> lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS}$) signal and write ($\overline{WR}$) signal.

Data strobe ($\overline{DS}$)– This input receives timing information for data transfers. During a write cycle, the CPU asserts the data strobe signal when valid output data is available and deasserts the data strobe signal before the data is removed. During a read cycle, the CPU asserts the data strobe signal and the Quad UART transfers the valid data. When the data strobe signal is deasserted, the DL<7:0> lines become a high impedance.

Write ($\overline{WR}$)–The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL<7:0> pins. If the $\overline{WR}$ signal is asserted during a data transfer (the $\overline{CS}$ and $\overline{DS}$ signals asserted), the Quad UART is receiving data from DL<7:0>. If the $\overline{WR}$ signal is deasserted during a write data transfer, the Quad UART is driving data onto the DL<7:0> lines.

INTERRUPT REQUEST

Interrupt request $\overline{IRQ}$–The $\overline{IRQ}$ pin is an open drain output. The integral interrupt scanner asserts the IRQ signal when it has detected an interrupt condition on one of the four serial data lines.

Interrupt Request transmit/receive (IRQTxRx)—This signal indicates when the interrupt scanner in the Quad UART stops and asserts $\overline{IRQ}$ because of a transmitter interrupt condition (the IRQTxRx signal is asserted) or because of a receiver interrupt condition (the IRQTxRx signal is deasserted). The signal is valid only while $\overline{IRQ}$ is asserted. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

Interrupt request line number (IRQLN<1:0>)–These lines indicate the line number at which the Quad UART interrupt scanner stopped and asserted the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is asserted. Line IRQLN<1> is the high-order bit and the IRQLN<0> line is the low-order bit. The

state of these signals also appears as bits in the interrupt summary register: IRQLN<1> as bit 2, and IRQLN<0> as bit 1. Table 3 shows the line numbers corresponding to settings of IRQLN<1:0>.

TABLE 3–COM78C804 INTERRUPT REQUEST LINE ASSIGNMENTS

IRQ Line <1>	IRQ Line <0>	Line
0	0	0
0	1	1
1	0	2
1	1	3

SERIAL DATA

Transmit data (TxD<3:0>)–These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and a low level when the TxBRK bit in the associated line's command register is set.

Receive data (RxD<3:0>)–These lines accept asynchronous bit-serial data streams. The input signals must remain in the high state for at least one-half bit time before a high-to-low transition is recognized. (A high-to-low transition is required to signal the beginning of a "start" bit and initiate data reception).

MODEM SIGNALS

Data set ready ($\overline{DSR}$<3:0>)–These four input pins, one for each serial data line on the COM78C804, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the DSR bit (bit 7) in the corresponding line's status register to be asserted. A TTL high at a $\overline{DSR}$ pin causes the DSR bit in the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

Carrier detect (DCD<3:0>)–These four input pins, one for each serial data line of the Quad UART, are typically connected through intervening level converters to the received line signal detect (also called carrier detect) outputs of modems. A TTL low at a $\overline{DCD}$ pin causes the DCD bit of the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit corresponding to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

GENERAL CONTROL SIGNALS

Ready ($\overline{RDY}$)–The $\overline{RDY}$ pin is an open drain output. Upon detecting a negative transition of chip select ($\overline{CS}$), the Quad UART asserts the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deasserts after the trailing edge of $\overline{CS}$.

Reset ($\overline{RESET}$)–When the $\overline{RESET}$ input in asserted, the TxD<3:0> lines are asserted and all internal status bits listed in the "Architecture Summary" discussion are cleared.

Manufacturing reset (MRESET)–This signal is for manufacturing use only and the input should be connected to ground for normal operation.

MISCELLANEOUS SIGNALS

Clock in (CLK)–All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1 percent and duty cycle is 50 percent ±5 percent.

POWER AND GROUND

Voltage (V_{DD})–Power supply 5 Vdc

Ground (V_{SS})–Ground reference

ARCHITECTURE SUMMARY

The Quad UART functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its four serial data lines (stop bits, parity, character length, split baud rates, etc.)

Each serial line functions the same as a one-line UART-type device thereby reducing the number of chips and conserving space on communication devices that require multiple communications lines.

An integral interrupt scanner checks for device interrupt conditions on the four lines. Its scanning algorithm gives priority to receivers over transmitters. The scanner can also check for interrupts resulting from changes in modem control signals $\overline{DSR}$ and $\overline{DCD}$.

Line-specific Registers

Each of the four serial data lines in the Quad UART has a set of registers for buffering data into and out of the line and for external control of the line's characteristics. These registers are selected for access by setting the appropriate address on lines ADD<4:0>. Lines ADD<4:3> select one of the four data lines. Lines ADD<2:0> select the specific register for that line. Refer to Table 2 for the register address assignments.

Receiver buffer register–Each line's receiver consists of a character assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line's command register is set, received characters are moved automatically into the line's receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The assertion of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is asserted). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is deasserted) and the interrupt scanner resumes operation.

If there is another entry in a line's FIFO, the RxRDY bit remains asserted. When the interrupt scanner reaches this line again, the assertion of RxRDY causes the scanner to halt and assert the $\overline{IRQ}$ again.

Asserting the $\overline{RESET}$ signal or clearing the RxEN bit initializes the receiver logic of Quad UART. The RxRDY flag is cleared and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

Transmitter holding register–Each line has a writable transmitter holding register. When the TxEN bit in the line's command register is set, characters are moved automatically from the output of this register into the transmitter serialization logic whenever the serialization logic becomes idle.

When this register is empty, the TxRDY bit in the line's status register is set. If the transmitter interrupt enable (TxIE) bit in the line's command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If

a character is then loaded into the register, the interrupt is cleared and the scanner resumes operation.

Assertion of the RESET signal initializes the transmitter logic of the Quad UART. The TxRDY flag is cleared and the transmitter holding register's contents are lost. The transmitter enable (TxEN) bit in the line's command register is also cleared by RESET. If at the end of the reset process, the TxEN is reasserted and TxRDY bit is reasserted. Software clearing of TxEN alone produces results different from the full RESET in that the transmitter holding register's contents are not lost; they are transmitted when TxEN is set again.

Status register–Each line has a read-only status register that provides information about the current state of the given line. This register indicates a line's readiness for transmission or reception of data and flags error conditions in its bit fields. Figure 3 shows the format of the status register. Table 3 lists the flag bits in each status register.

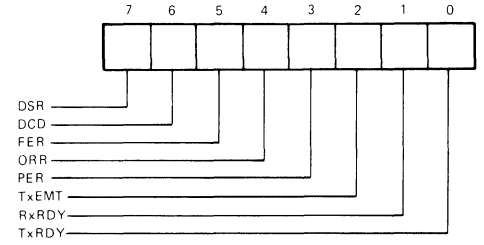


FIGURE 3: COM78C804 STATUS REGISTERS (LINE 0-3) FORMAT

TABLE 4–COM78C804 STATUS REGISTERS (LINES 0-3) DESCRIPTION

Bit	Description
7	DSR (Data set ready)–This bit is the inverted state of the DSR line.
6	DCD (Data set carrier detect)–This bit is the inverted state of the DCD line.
5	FER (Frame error)–Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the RESET input, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error)–Set when the character in the receiver buffer register was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by asserting the RESET input, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity error)–If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the RESET input, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter empty)–Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmitter holding register. Cleared by loading the transmitter holding register, by clearing TxEN (0) of the command register, or by asserting the RESET input.
1	RxRDY (Receiver buffer ready)–When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by asserting the RESET input.
0	TxRDY (Transmitter holding register ready)—When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or by asserting the RESET input. This bit is initially set when the transmitter logic is enabled by the setting of TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

Mode registers 1 and 2—These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the four communications lines has two of these registers, both accessed by the same address on ADD<4:0>. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1, the next address mode register 2, and another after that would recycle the pointer to mode register 1. The pointer is reset to point to mode register 1 by RESET or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 4 shows the format of mode registers 1 and Table 5 describes the function of the register information.

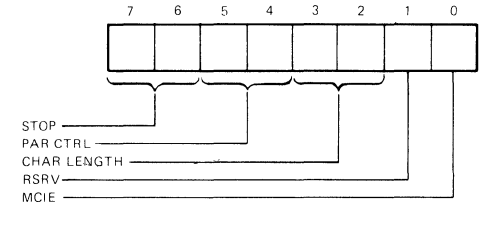


FIGURE 4–COM78C804 MODE REGISTERS 1 (LINE 0-3) FORMAT

TABLE 5–COM78C804 MODE REGISTERS 1 (LINES 0-3) DESCRIPTION

Bit	Description
7,6	STOP–These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by asserting the RESET input. **Bits** **Stop Bits** **7 6** 0 0 Invalid 0 1 1.0 1 0 1.5 1 1 2.0
5,4	PAR CTRL (Parity control)–These bits determine parity as follows and are cleared by asserting the RESET input. X = either 1 or 0. **Bits** **Parity Type** **5 4** 1 1 Even 0 1 Odd X 0 Disabled
3,2	CHAR LENGTH (Character length)–These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by asserting the RESET input. The character length bits are defined as follows: **Bit** **Bit Length** **3 2** 0 0 5 0 1 6 1 0 7 1 1 8
1	RSRV (Reserved and cleared by asserting the RESET input.)
0	MCIE (Modem control interrupt enable)–When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the Interrupt Scanner and Interrupt Handling information. Cleared by asserting the RESET input.

Figure 5 shows the format of mode registers 2 and Table 5 indicates the baud rate selections of the register. Bits 7 through 4 of the mode register 2 control the transmitter baud rate and bits 3 through 0 control the receiver baud rate. These registers are cleared by asserting RESET input.

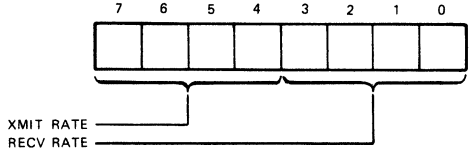


FIGURE 5–COM78C804 MODE REGISTERS 2 (LINE 0-3) FORMAT

Command register–These read/write registers control various functions on the selected line. Figure 6 shows the format of the command registers and Table 6 describes the function of the register information.

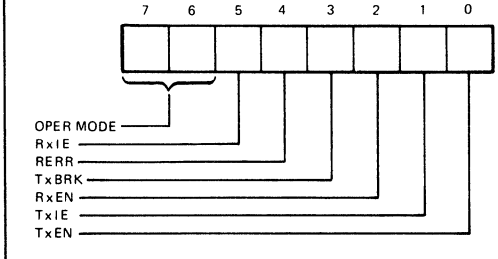


FIGURE 6–COM78C804 COMMAND REGISTERS (LINE 0-3) FORMAT

TABLE 6–COM78C804 MODE REGISTERS 2 (LINES 0-3) DESCRIPTION

Bit	Description
7:0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate)–Selects the baud rate of the transmitter (bits 7:4) and receiver (bits 3:0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error*
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
0	0	0	0	0	0	0	0	50	same	—
0	0	0	1	0	0	0	1	75	same	—
0	0	1	0	0	0	1	0	110	109.09	0.826
0	0	1	1	0	0	1	1	134.5	133.33	0.867
0	1	0	0	0	1	0	0	150	same	—
0	1	0	1	0	1	0	1	300	same	—
0	1	1	0	0	1	1	0	600	same	—
0	1	1	1	0	1	1	1	1200	same	—
1	0	0	0	1	0	0	0	1800	1745.45	3.03
1	0	0	1	1	0	0	1	2000	2021.05	1.05
1	0	1	0	1	0	1	0	2400	same	—
1	0	1	1	1	0	1	1	3600	3490.91	3.03
1	1	0	0	1	1	0	0	4800	same	—
1	1	0	1	1	1	0	1	7200	6981.81	3.03
1	1	1	0	1	1	1	0	9600	same	—
1	1	1	1	1	1	1	1	19200	same	—

*The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1 percent. This variance results in an error that must be added to the error listed.

TABLE 7–COM78C804 COMMAND REGISTERS (LINES 0-3) DESCRIPTION

Bit	Description
7,6	OPER MODE (Operating mode)–These bits control the operating mode of the channel as follows. These bits are cleared by asserting the RESET input. **Bit 7 6 — Operating Mode** 0 0 — Normal operation 0 1 — Automatic echo 1 0 — Local loopback 1 1 — Remote loopback
5	RxIE (Receiver interrupt enable)–When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset error)–When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by asserting the RESET input (not self-clearing).
3	TxBRK (Transmit break)–When set, this bit forces the appropriate TxD<3:0> line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by asserting the RESET input.
2	RxEN (Receiver enable)–When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by asserting the RESET input.
1	TxIE (Transmit interrupt enable)–When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is asserted and generates an interrupt by asserting the IRQ signal.
0	TxEN (Transmitter enable)–When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with this line, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by asserting the RESET input.

Bits 5 through 0 enable the line's receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to "Interrupt Scanner" and "Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are:

- ☐ Normal operation–The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. (The RxEN bit must be set.) Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. (The TxEN bit must be set.)

- ☐ Automatic echo–The serial data received is assembled into parallel in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxD<n> pin for serial output. TxEN is ignored and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.
- ☐ Local loopback–The serial data from the RxD<n> input is ignored and the receiver serial input receives data from the transmitter serial output. The data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. (The TxEN bit must be set.) The transmission goes only to the receiver serial input; the TxD<n> output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.
- ☐ Remote loopback–The serial data received on the RxD<n> line is returned to the TxD<n> line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

SUMMARY REGISTERS

The Quad UART contains two registers that summarize the current status of all four serial data lines, making it possible to determine that a line's status has changed with a single read operation. These registers are selected for access by setting the appropriate address on pins ADD <2:0>. Because the registers are shared by four serial lines, the line-selection bits (ADD <4:3>) are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

Interrupt summary register–This read-only register indicates that a transmitter or receiver interrupt condition has occurred, and indicates the line number that generated the interrupt. Figure 7 shows the format of the interrupt summary register and Table 8 describes register information.

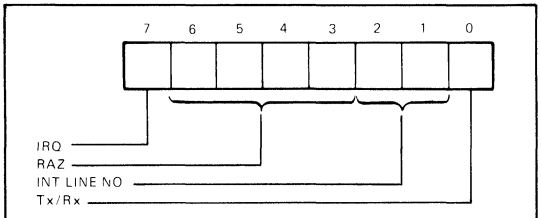


FIGURE 7– COM78C804 INTERRUPT SUMMARY REGISTER FORMAT

TABLE 8–COM78C804 INTERRUPT SUMMARY REGISTER DESCRIPTION

Bit	Description
7	IRQ (Interrupt request)–When set, this bit indicates that the interrupt scanner has found an interrupting condition among the four serial lines of the Quad UART. These conditions also result in the Quad UART asserting the $\overline{IRQ}$ signal.
6:4	RAZ (Read as zero)–Not used
3:1*	INT LINE NO (Interrupting line number)–These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN <1:0> signals–bit 2 = IRQLN<1>, and bit 1 = IRQLN<0>. Refer to Table 3.
0*	Tx/$\overline{Rx}$ (Transmit/receive)–This bit indicates whether the interrupting condition was caused by a transmitter (Tx/$\overline{Rx}$ equals 1) or a receiver (Tx/$\overline{Rx}$ equals 0). This bit corresponds to the IRQTxRx signal of the Quad UART and is set when IRQTxRx is asserted.

*Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

Data set change summary register–When the $\overline{DSR}$ or $\overline{DCD}$ inputs that are associated with a line change state, the bit corresponding to that line in this read-only register is set. The current state of the $\overline{DSR}$ and $\overline{DCD}$ inputs can then be obtained from that line's status register. If the state of a line changes twice within one microsecond, the change in state may not be detected. Figure 8 shows the format of the data set change summary register.

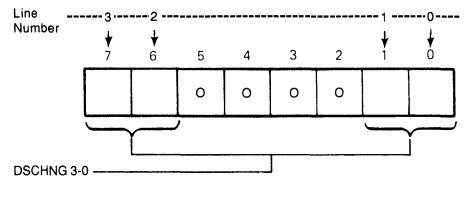


FIGURE 8–COM78C804 DATA SET CHANGE SUMMARY REGISTER FORMAT

When the MCIE bit in a line's mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and assert the $\overline{IRQ}$ signal. The data set change summary register bits are cleared by writing a 1 into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled and writeback should directly follow the read operation.

Assertion of the $\overline{RESET}$ signal disables and initializes the data set change logic. When the $\overline{RESET}$ signal is deasserted, future changes in $\overline{DSR}$ and $\overline{DCD}$ are reported as they occur.

INTERRUPT SCANNER AND INTERRUPT HANDLING

The interrupt scanner sequentially checks each line for a receive interrupt and then checks each one in the same order for a transmitter interrupt. If the scanner detects an interrupt condition, it stops and the $\overline{IRQ}$ signal is asserted. An interrupt must be serviced by software or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line's receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = 1) or either of the line's modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG and RxIE and MCIE = 1).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE = 1).

When the scanner detects an interrupt, it reports the line number on the IRQ<1:0> lines. The IRQTxRx signal is asserted for a transmitter interrupt and deasserted for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line is deasserted and the scanner is restarted for each of the following three types of interrupt conditions.

- ☐ Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- ☐ Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- ☐ Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line 0's receiver), thus giving receivers priority over transmitters.

EDGE-TRIGGERED AND LEVEL-TRIGGERED INTERRUPT SYTSTEMS

If the interrupt system of the Quad UART is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

MODEM HANDLING

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deasserting the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The assertion of the TxEMT bit to indicate the transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to assert before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character (a starter bit–5,6,7, or 8 data bits; plus parity bit if enabled; and 1,1.5, or 2 stop bits), and multiplying by either two characters or one, depending on when TxEMT monitoring begins.

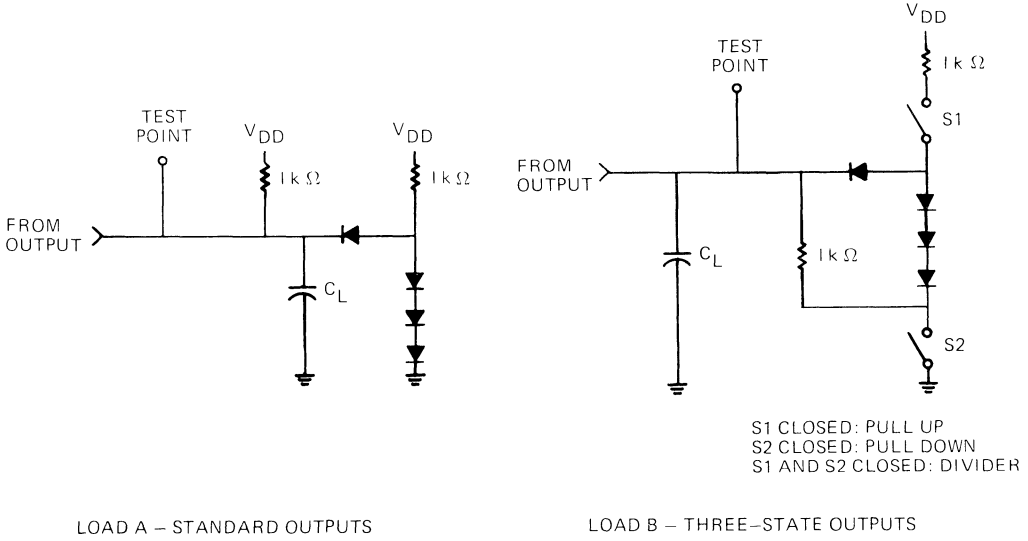


FIGURE 9–COM78C804 OUTPUT LOAD CIRCUITS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +125°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... V_{CC} +0.3V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

TABLE 9–COM78C804

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Requirements Min.	Typ.	Max.	Units
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{DD} = Min. I_{OH} = 3.5 mA for DL<7:0> I_{OH} = 2.0 mA for all remaining output except $\overline{IRQ}$ and $\overline{RDY}$	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = Min. I_{OL} = 5.5 mA for DL<7:0> I_{OL} = 3.5 mA for all remaining outputs			0.4	V
I_{IH}	Input current at maximum input voltage	V_{DD} = Max. V_I = V_{DD}(Max.)			10	µA
I_{IL}	Input current at miminum input voltage	V_{DD} = Max. V_I = 0.0V			−10	µA
I_{OS}[1]	Short-circuit output current for DL<7:0> all remaining outputs except $\overline{IRQ}$ and $\overline{RDY}$	V_{DD} = Max.	−50 −30		−180 −110	mA mA
I_{OZL}[2]	Three-state output current	V_{DD} = Max. V_O = 0.4V			10	µA
I_{OZH}[2]	Three-state output current	V_{DD} = Max. V_O = 2.4V			10	µA
I_{DD}	Supply current	V_{DD} = Max. T_A = 0°			20	mA
C_{in}	Input capacitance				4	pF
C_{IO}[3]	Input/output capacitance				5	pF

[1]No more than one ouput should be short circuited at a time, and the duration of the short should not exceed 1 second.
[2]All three-state output drivers are wired in an I/O configuration. The parameters include the driver and input receiver leakage currents.
[3]The parameters include the capacitive loads of the output driver and the input receiver.

TIMING PARAMETERS

Figure 10 shows the signal timing for a read cycle to transfer information from the Quad UART to the processor. Figure 11 shows the signal timing for a write cycle to transfer information from the processor to the Quad UART. Table 11 lists the timing parameters for the read and write cycles.

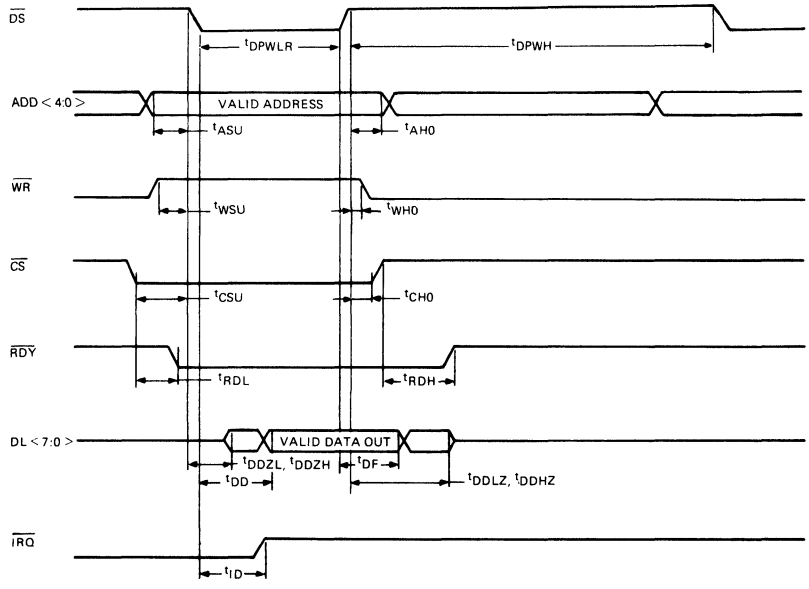


FIGURE 10–COM78C804 BUS READ CYCLE TIMING

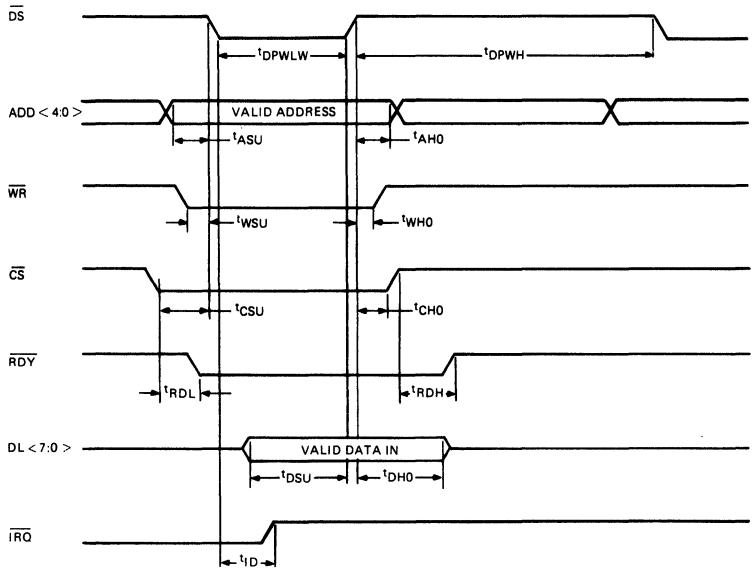


FIGURE 11–COM78C804 BUS WRITE CYCLE TIMING

TABLE 10–COM78C804 BUS READ AND WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Max.	Load Circuit[1]
t_{AHO}	Hold time of a valid ADD <4:0> to a valid high level of $\overline{DS}$.	10		
t_{ASU}	Setup time of a valid ADD <4:0> to the falling edge of $\overline{DS}$.	30		
t_{CHO}	Hold time of a valid low level of $\overline{CS}$ to a valid high level of $\overline{DS}$.	10		
t_{CSU}	Setup time of a valid low level of $\overline{CS}$ to the falling edge of $\overline{DS}$.	30		
t_{DD}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to valid high or low data on DL <7:0>.	165		$C_L = 150$ pF
t_{DDLZ}[2]	Propagation delay of a valid high level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output drivers disabled.			
	t_{DDLZ}		50	$C_L = 50$pF
	t_{DDHZ}		50	$C_L = 50$pF
	t_{DDLZ}		60	$C_L = 100$pF
	t_{DDHZ}		60	$C_L = 100$pF
	t_{DDLZ}		65	$C_L = 150$pF
	t_{DDHZ}		65	$C_L = 150$pF
t_{DDZL}	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output driver enabled.			
	t_{DDZL}		165	$C_L = 150$pF
	t_{DDZH}	0	165	$C_L = 150$pF
t_{DF}	Hold time provided during a read cycle by Quad UART of valid high or low data on DL <7:0> after the rising edge of $\overline{DS}$.	0		
t_{DHO}	Hold time of a valid DL <7:0> to a valid high level of $\overline{DS}$.	30		
t_{DPWH}	Pulse width high of $\overline{DS}$.	450		
t_{DPWLR}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is high (read operation). Refer to timing parameter t_{DPWLW} also.	180	10,000	
t_{DPWLW}	Pulse width low of $\overline{DS}$ when $\overline{WR}$ is low (write operation). Refer to timing parameter t_{DPWLR} also.	130	10,000	
t_{DSU}	Setup time of a valid DL <7:0> to the rising edge of $\overline{DS}$.	50		
t_{ID}[3]	Propagation delay of a valid low level on $\overline{DS}$ (if $\overline{CS}$ is low) to a high level on $\overline{IRQ}$.		635	$C_L = 50$pF
t_{RDH}[4]	Propagation delay of a valid high level of $\overline{CS}$ to a valid high level on $\overline{RDY}$.		210	$C_L = 50$pF
t_{RDL}	Propagation delay of a valid low level on $\overline{CS}$ to a valid low level on $\overline{RDY}$.		90	$C_L = 50$pF
t_{WHO}	Hold time of a valid high or low level of $\overline{WR}$ to a valid high level of $\overline{DS}$.	10		
t_{WSU}	Setup time of a valid high or low level of $\overline{WR}$ to the falling edge of $\overline{DS}$.	30		

[1]Refer to Figure 9 for the load circuits used with these measurements.
[2]The t_{DDLZ} and t_{DDHZ} parameters are measured with $C_L = 150$ pF. The values of t_{DDLZ} and t_{DDHZ} for $C_L = 50$pF and $C_L = 100$ pF have been derived for user convenience.
[3]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{ID} parameter can be calculated by the following: $t_{ID} = 500 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.
[4]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{RDH} parameter can be calculated by the following: $t_{RDH} = 75 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.

Figure 12 shows the signal timing for the clock input, interrupt timing, effect of the $\overline{RESET}$ input on data strobe, data set carrier detect (DCD) and data set ready (DSR) input timing, and the transmit data output timing. Table 11 lists the timing parameters for Figure 12.

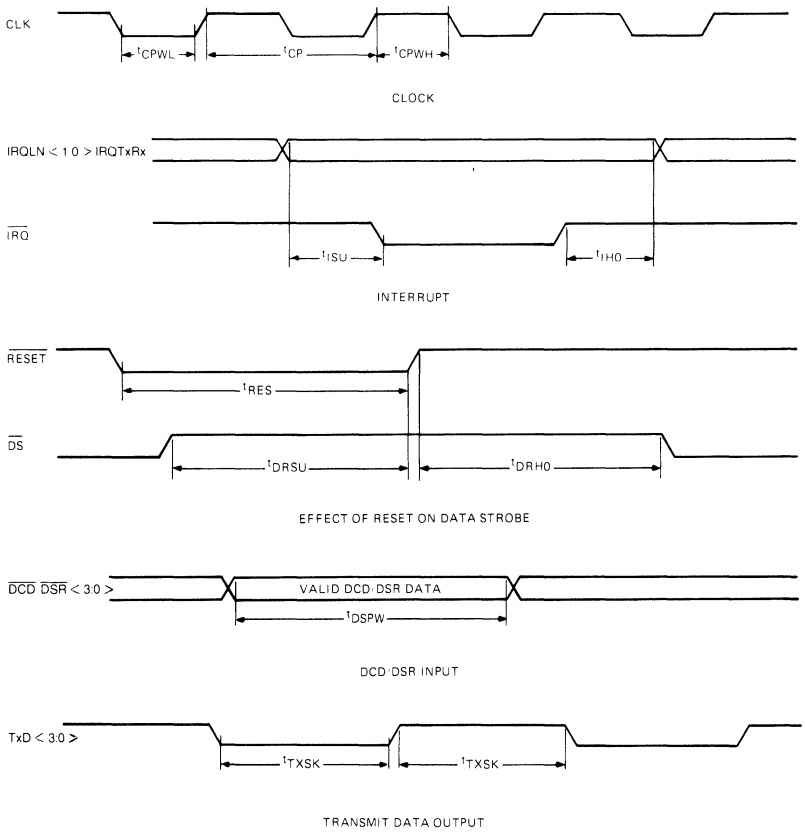


FIGURE 12–COM78C804 MISCELLANEOUS SIGNAL TIMING

TABLE 11–MISCELLANEOUS WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Load Circuit*
t_{CP}	Period of CLK.	203.45 (4.9152 MHz)	
t_{CPWH}	Pulse width high of CLK.	95	
t_{CPWL}	Pulse width low of CLK.	95	
t_{DRHO}	Hold time of a valid high level of $\overline{DS}$ to a valid high level of $\overline{RESET}$.	1,000	
t_{DRSU}	Setup time of a valid high level of $\overline{DS}$ to the rising edge of $\overline{RESET}$.	900	
t_{DSPW}	Pulse width high or low of DCD <3:0> and DSR <3:0>.	1,000	
t_{IHO}	Hold time provided by Quad UART from a valid IRQLN <1:0> and IRQTxRx to a valid high level of IRQ.	100	$C_L = 50pF$
t_{ISU}	Setup time provided by Quad UART from a valid IRQLN <1:0> and IRQTxRx to a valid low level of $\overline{IRQ}$.	100	$C_L = 50pF$
t_{RES}	Pulse width low of $\overline{RESET}$.	1,000	
t_{TXSK}	Pulse width high or low provided by Quad UART on the TxD <3:0> lines. At each baud rate, the actual pulse widths provided vary by t_{TXSK}. This timing parameter should be used to determine cumulative reception/transmission errors.	250	$C_L = 50pF$

*Refer to Figure 9 for the load circuits used with these measurements.

Figure 13 shows the input and output voltage waveforms for the propagation delay and setup and hold measurements. Figure 14 shows the waveforms for the three-state outputs measurement.

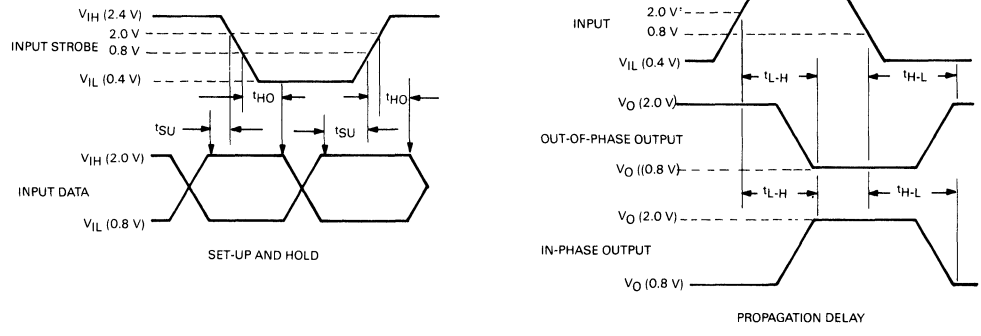
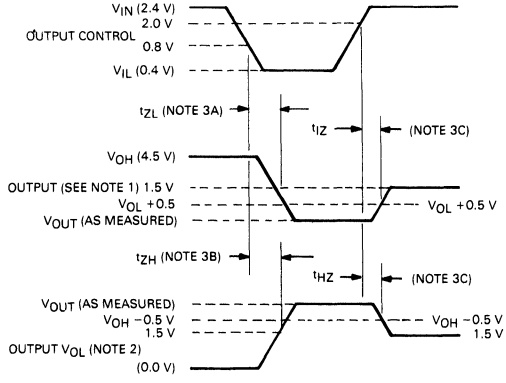


FIGURE 13–COM78C804 PROPAGATION DELAY AND SETUP AND HOLD VOLTAGE WAVEFORMS



THREE-STATE OUTPUTS

NOTES:
1. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
2. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
3. REFER TO FIGURE 9. A = S1 CLOSED, B = S2 CLOSED, C = S1 AND S2 CLOSED.

FIGURE 14–COM78C804 THREE-STATE OUTPUT VOLTAGE WAVEFORMS

STANDARD MICROSYSTEMS CORPORATION

COM78808
PRELIMINARY

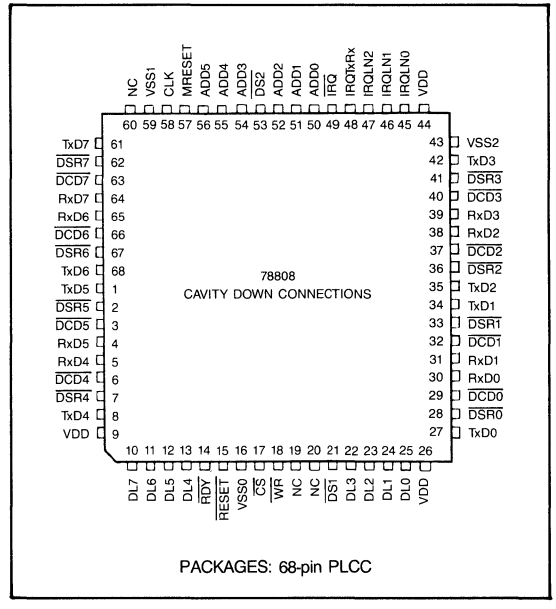
SECTION III

Eight-channel Universal Asynchronous Receiver/Transmitter Octal UART

FEATURES

- ☐ Eight independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers

PIN CONFIGURATION



PACKAGES: 68-pin PLCC

GENERAL DESCRIPTION

The COM78808 Eight-channel Asynchronous Receiver/Transmitter (Octal UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This 68-pin device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines. Figure 1 is a functional block diagram of the COM78808 Octal UART.

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM78C808
PRELIMINARY

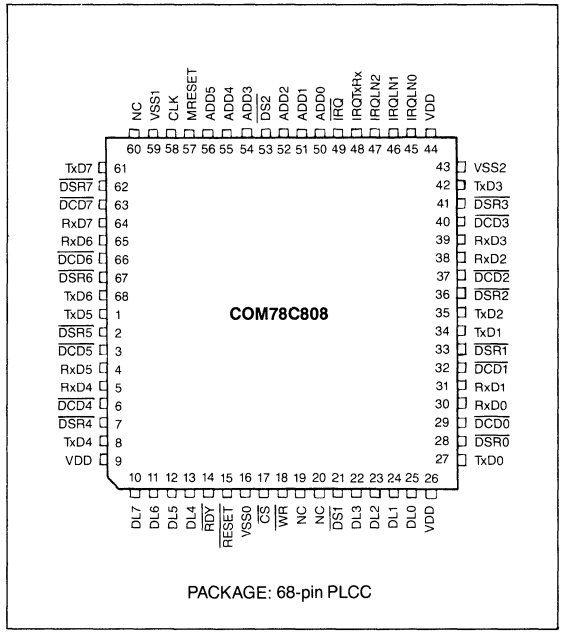
SECTION III

Eight-channel Universal Asynchronous Receiver/Transmitter Octal UART

FEATURES

- ☐ Eight independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers
- ☐ Low power CMOS technology
- ☐ +5V only power supply
- ☐ Compatible with COM78C804 and COM78C802

PIN CONFIGURATION



PACKAGE: 68-pin PLCC

GENERAL DESCRIPTION

The COM78C808 Eight-channel Asynchronous Receiver/Transmitter (Octal UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This 68-pin device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines. Figure 1 is a functional block diagram of the COM78C808 Octal UART.

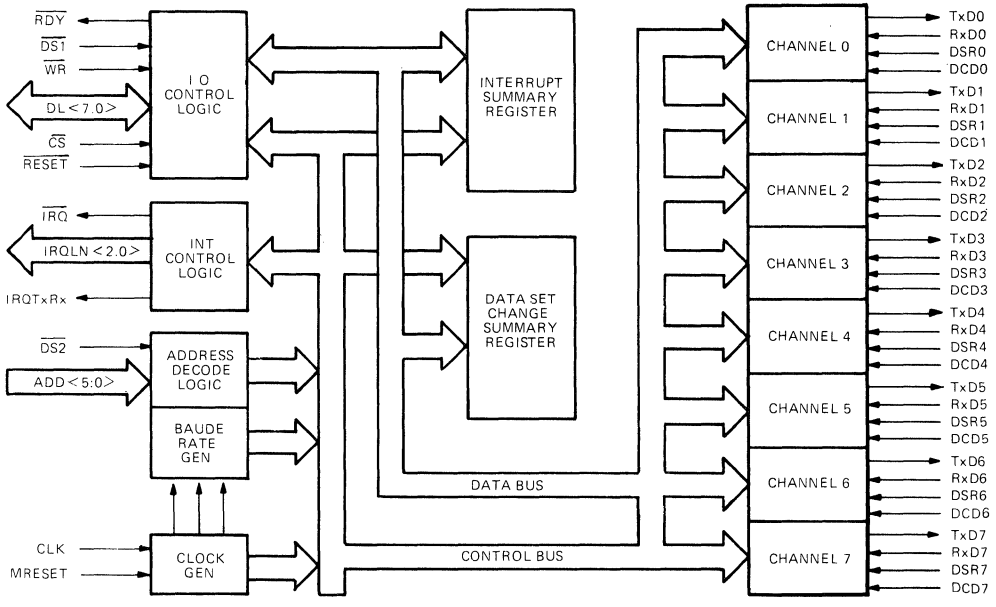


FIGURE 1 – COM78C808 OCTAL UART FUNCTIONAL BLOCK DIAGRAM

TABLE 1 – COM78C808 PIN AND SIGNAL SUMMARY

Pin	Signal	Input/Output	Definition/Function
10-13,22-25	DL<7:0>	input/output	Data lines <7:0>–Receives and transmits the parallel data.
50-52,54-56	ADD <0:5>	input	Address<0:5>–Selects the internal registers in the Octal UART.
17	$\overline{CS}$	input	Chip select–Activates the Octal UART to receive and transmit data over the DL<7:0> lines.
21,53	$\overline{DS1}$,$\overline{DS2}$	input	Data strobe 1 and 2–Receives timing information for data transfers. The $\overline{DS1}$ and $\overline{DS2}$ inputs must be connected together.
18	$\overline{WR}$	input	Write–Specifies direction of data transfer on the DL<7:0> lines.
14	$\overline{RDY}$	output	Ready–Indicates when the Octal UART is ready to participate in data transfer cycles.
15	$\overline{RESET}$	input	Reset–Initializes the internal logic.
57	MRESET	input	Manufacturing reset–For manufacturing use.
58	CLK	input	Clock–Clock input for timing.
62,67,2,7, 41,36,33,28	$\overline{DSR}$<7:0>	inputs	Data set ready–Monitor data set ready (DSR) signals from modems.
63,66,3,6, 40,37,32,29	$\overline{DCD}$<7:0>	inputs	Data set carrier detect–Monitor data set carrier detect (DCD) signals from modems.
49	$\overline{IRQ}$	output	Interrupt request–Requests a processor interrupt.
45-47	IRQLN <0:2>	output	Interrupt request line number–Indicates the line number of originating interrupt request.
48	IRQTxRx	output	Interrupt request transmit/receive–Indicates whether an interrupt request is for transmitting or receiving data.
61,68,1,8, 42,35,34,27	TxD<7:0>	outputs	Transmit data–Provides asynchronous bit-serial data output streams.
64,65,4,5, 39,38,31,30	RxD<7:0>	inputs	Receive data–Accepts asynchronous bit-serial data input streams.
44,26,9	V_{DD}	input	Voltage–Power supply voltage +5 Vdc.
16,59,43	V_{SS}	input	Ground–Ground reference

DATA AND ADDRESS

Data lines (DL<7:0>)–These lines are used for the parallel transmission and reception of data between the CPU and the Octal UART. The receivers are active when the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is asserted. The output drivers are active only when the chip select ($\overline{CS}$) signal is asserted, the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is asserted, and the write ($\overline{WR}$) signal is deasserted. The drivers will become inactive (high-impedance) within 50 nanoseconds when one or more of the following occurs: the chip select ($\overline{CS}$) signal is deasserted, the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is deasserted, or the write ($\overline{WR}$) signal is asserted.

Address (ADD<5:0>)–These lines select which Octal UART internal register is accessible through the data I/O lines (DL<7:0>) when the data strobe ($\overline{DS1}$, $\overline{DS2}$) and chip select ($\overline{CS}$) signals are asserted. Table 2 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is deasserted, the address accesses the receiver buffer register and when asserted, it accesses the transmitter holding register.

TABLE 2 – COM78C808 REGISTERS ADDRESS SELECTION

ADD Line* <5>	<4>	<3>	<2>	<1>	<0>	Read/Write	Register
0	0	0	0	0	0	Read	Line 0 Receiver Buffer
0	0	0	0	0	0	Write	Line 0 Transmitter Holding
0	0	0	0	0	1	Read	Line 0 Status
0	0	0	0	1	0	Read/Write	Line 0 Mode Registers 1,2
0	0	0	0	1	1	Read/Write	Line 0 Command
0	0	1	0	0	0	Read	Line 1 Receiver Buffer
0	0	1	0	0	0	Write	Line 1 Transmitter Holding
0	0	1	0	0	1	Read	Line 1 Status
0	0	1	0	1	0	Read/Write	Line 1 Mode Register 1,2
0	0	1	0	1	1	Read/Write	LIne 1 Command
0	1	0	0	0	0	Read	Line 2 Receiver Buffer
0	1	0	0	0	0	Write	Line 2 Transmitter Holding
0	1	0	0	0	1	Read	Line 2 Status
0	1	0	0	1	0	Read/Write	Line 2 Mode Register 1,2
0	1	0	0	1	1	Read/Write	Line 2 Command
0	1	1	0	0	0	Read	Line 3 Receiver Buffer
0	1	1	0	0	0	Write	Line 3 Transmitter Holding
0	1	1	0	0	1	Read	Line 3 Status
0	1	1	0	1	0	Read/Write	Line 3 Mode Register 1,2
0	1	1	0	1	1	Read/Write	Line 3 Command
1	0	0	0	0	0	Read	Line 4 Receiver Buffer
1	0	0	0	0	0	Write	Line 4 Transmitter Holding
1	0	0	0	0	1	Read	Line 4 Status
1	0	0	0	1	0	Read/Write	Line 4 Mode Register 1,2
1	0	0	0	1	1	Read/Write	Line 4 Command
1	0	1	0	0	0	Read	Line 5 Receiver Buffer
1	0	1	0	0	0	Write	Line 5 Transmitter Holding
1	0	1	0	0	1	Read	Line 5 Status
1	0	1	0	1	0	Read/Write	Line 5 Mode Register 1,2
1	0	1	0	1	1	Read/Write	Line 5 Command
1	1	0	0	0	0	Read	Line 6 Receiver Buffer
1	1	0	0	0	0	Write	Line 6 Transmitter Holding
1	1	0	0	0	1	Read	Line 6 Status
1	1	0	0	1	0	Read	Line 6 Mode Register 1,2
1	1	0	0	1	1	Read/Write	Line 6 Command
1	1	1	0	0	0	Read	Line 7 Receiver Buffer
1	1	1	0	0	0	Write	Line 7 Transmitter Holding
1	1	1	0	0	1	Read	Line 7 Status
1	1	1	0	1	0	Read/Write	Line 7 Mode Register 1,2
1	1	1	0	1	1	Read/Write	Line 7 Command
X	X	X	1	0	0	Read	Interrupt Summary
X	X	X	1	0	1	Read	Data Set Change Summary

*X = Either 0 or 1.

BUS TRANSACTION CONTROL

Chip select ($\overline{CS}$)–This signal is asserted to permit data transfers through the DL<7:0> lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal and write ($\overline{WR}$) signal.

Data strobe ($\overline{DS1}$, $\overline{DS2}$)– The data strobe inputs ($\overline{DS1}$ and $\overline{DS2}$) must be connected together. This input receives timing information for data transfers. During a write cycle, the CPU asserts the data strobe signal when valid output data is available and deasserts the data strobe signal before the data is removed. During a read cycle, the CPU asserts the data strobe signal and the Octal UART transfers the valid data. When the data strobe signal is deasserted, the DL<7:0> lines become a high impedance.

Write ($\overline{WR}$)–The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL<7:0> pins by controlling the direction of their transceivers. If the $\overline{WR}$ signal is asserted during a data transfer (the $\overline{CS}$, $\overline{DS1}$, and $\overline{DS2}$ signals asserted), the Octal UART is receiving data from DL<7:0>. If the $\overline{WR}$ signal is deasserted during a write data transfer, the Octal UART is driving data onto the DL<7:0> lines.

INTERRUPT REQUEST

Interrupt request $\overline{IRQ}$–The $\overline{IRQ}$ pin is an open drain output. The integral interrupt scanner asserts the IRQ signal when it has detected an interrupt condition on one of the eight serial data lines.

Interrupt Request transmit/receive (IRQTxRx)—This signal indicates when the interrupt scanner in the Octal UART stops and asserts $\overline{IRQ}$ because of a transmitter interrupt condition (the IRQTxRx signal is asserted) or because of a receiver interrupt condition (the IRQTxRx signal is deasserted). The signal is valid only while $\overline{IRQ}$ is asserted. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

Interrupt request line number (IRQLN<2:0>)–These lines indicate the line number at which the Octal UART interrupt scanner stopped and asserted the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is asserted. Line IRQLN<2> is the high-order bit and the IRQLN<0> line is the low-order bit. The state of these signals also appears as bits in the interrupt summary register: IRQLN<2> as bit 3, IRQLN<1> as bit 2, and IRQLN<0> as bit 1. Table 3 shows the line numbers corresponding to settings of IRQLN<2:0>.

TABLE 3 – COM78C808 INTERRUPT REQUEST LINE ASSIGNMENTS

IRQ Line <2>	<1>	<0>	Line
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

SERIAL DATA

Transmit data (TxD<7:0>)–These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and a low level when the TxBRK bit in the associated line's command register is set.

Receive data (RxD<7:0>)–These lines accept asynchronous bit-serial data streams. The input signals must remain in the high state for at least one-half bit time before a high-to-low transition is recognized. (A high-to-low transition is required to signal the beginning of a "start" bit and initiate data reception).

MODEM SIGNALS

Data set ready ($\overline{DSR}$<7:0>)–These eight input pins, one for each serial data line on the COM78C808, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the DSR bit (bit 7) in the corresponding line's status register to be asserted. A TTL high at a $\overline{DSR}$ pin causes the DSR bit in the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

Carrier detect (DCD<7:0>)–These eight input pins, one for each serial data line of the Octal UART, are typically connected through intervening level converters to the received line signal detect (also called carrier detect) outputs of modems. A TTL low at a $\overline{DCD}$ pin causes the DCD bit of the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit corresponding to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

GENERAL CONTROL SIGNALS

Ready ($\overline{RDY}$)–The $\overline{RDY}$ pin is an open drain output. Upon detecting a negative transition of chip select ($\overline{CS}$), the Octal UART asserts the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deasserts after the trailing edge of $\overline{CS}$.

Reset ($\overline{RESET}$)–When the $\overline{RESET}$ input is asserted, the TxD<7:0> lines are asserted and all internal status bits listed in the "Architecture Summary" discussion are cleared.

Manufacturing reset (MRESET)–This signal is for manufacturing use only and the input should be connected to ground for normal operation.

MISCELLANEOUS SIGNALS

Clock in (CLK)–All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1 percent and duty cycle is 50 percent ±5 percent.

POWER AND GROUND

Voltage (V_{DD})–Power supply 5 Vdc

Ground (V_{SS})–Ground reference

ARCHITECTURE SUMMARY

The Octal UART functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, split baud rates, etc.)

Each serial line functions the same as a one-line UART-type device thereby reducing the number of chips and conserving space on communication devices that require multiple communications lines.

An integral interrupt scanner checks for device interrupt conditions on the eight lines. Its scanning algorithm gives priority to receivers over transmitters. The scanner can also check for interrupts resulting from changes in modem control signals $\overline{DSR}$ and $\overline{DCD}$.

Line-specific Registers

Each of the eight serial data lines in the Octal UART has a set of registers for buffering data into and out of the line and for external control of the line's characteristics. These registers are selected for access by setting the appropriate address on lines ADD<5:0>. Lines ADD<5:3> select one of the eight data lines. Lines ADD<2:0> select the specific register for that line. Refer to Table 2 for the register address assignments.

Receiver buffer register–Each line's receiver consists of a character assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line's command register is set, received characters are moved automatically into the line's receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The assertion of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is asserted). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is deasserted) and the interrupt scanner resumes operation.

If there is another entry in a line's FIFO, the RxRDY bit remains asserted. When the interrupt scanner reaches this line again, the assertion of RxRDY causes the scanner to halt and assert the $\overline{IRQ}$ again.

Asserting the $\overline{RESET}$ signal or clearing the RxEN bit initializes the receiver logic of Octal UART. The RxRDY flag is cleared and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

Transmitter holding register–Each line has a writable transmitter holding register. When the TxEN bit in the line's command register is set, characters are moved automatically from the output of this register into the transmitter serialization logic whenever the serialization logic becomes idle.

When this register is empty, the TxRDY bit in the line's status register is set. If the transmitter interrupt enable (TxIE) bit in the line's command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared and the scanner resumes operation.

Assertion of the $\overline{RESET}$ signal initializes the transmitter logic of the Octal UART. The TxRDY flag is cleared and the transmitter holding register's contents are lost. The transmitter enable ($\overline{TxEN}$) bit in the line's command register is also cleared by $\overline{RESET}$. If at the end of the reset process, the TxEN is reasserted and TxRDY bit is reasserted. Software clearing of TxEN alone produces results different from the full $\overline{RESET}$ in that the transmitter holding register's contents are not lost; they are transmitted when TxEN is set again.

Status register–Each line has a read-only status register that provides information about the current state of the given line. This register indicates a line's readiness for transmission or reception of data and flags error conditions in its bit fields. Figure 3 shows the format of the status register. Table 3 lists the flag bits in each status register.

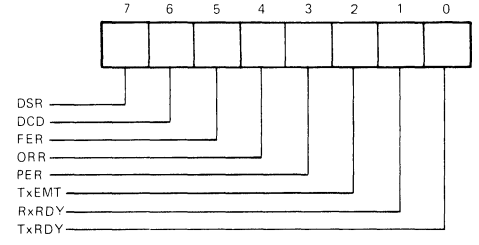


FIGURE 3 – COM78C808 STATUS REGISTERS (LINE 0-7) FORMAT

TABLE 4 – COM78C808 STATUS REGISTERS (LINES 0-7) DESCRIPTION

Bit	Description
7	DSR (Data set ready)–This bit is the inverted state of the $\overline{DSR}$ line.
6	DCD (Data set carrier detect)–This bit is the inverted state of the $\overline{DCD}$ line.
5	FER (Frame error)–Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, or by setting the reset error RERR (bit 4) of the command register.
4	ORR (Overrun error)–Set when the character in the receiver buffer register was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, or by setting reset error RERR (bit 4) of the command register.
3	PER (Parity error)–If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register.
2	TxEMT (Transmitter empty)–Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmitter holding register. Cleared by loading the transmitter holding register, by clearing TxEN (0) of the command register, or by asserting the $\overline{RESET}$ input.
1	RxRDY (Receiver buffer ready)–When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by asserting the $\overline{RESET}$ input.
0	TxRDY (Transmitter holding register ready)—When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or by asserting the $\overline{RESET}$ input. This bit is initially set when the transmitter logic is enabled by the setting of TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared.

Mode registers 1 and 2—These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the eight communications lines has two of these registers, both accessed by the same address on ADD<5:0>. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1, the next address mode register 2, and another after that would recycle the pointer to mode register 1. The pointer is reset to point to mode register 1 by $\overline{\text{RESET}}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 4 shows the format of mode registers 1 and Table 5 describes the function of the register information.

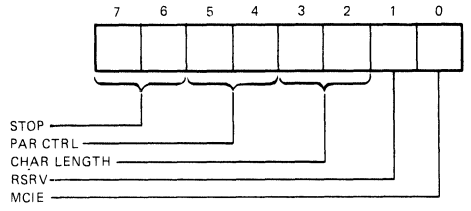


FIGURE 4 – COM78C808 MODE REGISTERS 1 (LINE 0-7) FORMAT

TABLE 5 – COM78C808 MODE REGISTERS 1 (LINES 0-7) DESCRIPTION

Bit	Description
7,6	STOP–These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by asserting the $\overline{\text{RESET}}$ input. **Bits** **Stop Bits** **7** **6** 0 0 Invalid 0 1 1.0 1 0 1.5 1 1 2.0
5,4	PAR CTRL (Parity control)–These bits determine parity as follows and are cleared by asserting the $\overline{\text{RESET}}$ input. X = either 1 or 0. **Bits** **Parity Type** **5** **4** 1 1 Even 0 1 Odd X 0 Disabled
3,2	CHAR LENGTH (Character length)–These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by asserting the $\overline{\text{RESET}}$ input. The character length bits are defined as follows: **Bit** **Bit Length** **3** **2** 0 0 5 0 1 6 1 0 7 1 1 8
1	RSRV (Reserved and cleared by asserting the $\overline{\text{RESET}}$ input.)
0	MCIE (Modem control interrupt enable)–When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the Interrupt Scanner and Interrupt Handling information. Cleared by asserting the $\overline{\text{RESET}}$ input.

Figure 5 shows the format of mode registers 2 and Table 6 indicates the baud rate selections of the register. Bits 7 through 4 of the mode register 2 control the transmitter baud rate and bits 3 through 0 control the receiver baud rate. These registers are cleared by asserting $\overline{\text{RESET}}$ input.

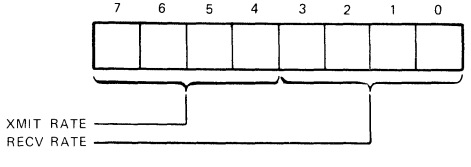


FIGURE 5 – COM78C808 MODE REGISTERS 2 (LINE 0-7) FORMAT

Command register–These read/write registers control various functions on the selected line. Figure 6 shows the format of the command registers and Table 6 describes the function of the register information.

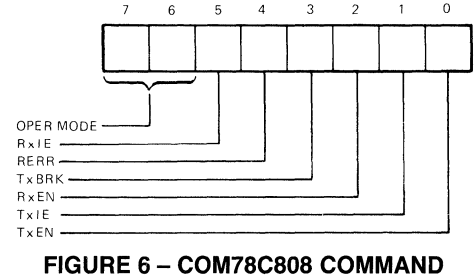


FIGURE 6 – COM78C808 COMMAND REGISTERS (LINE 0-7) FORMAT

TABLE 6 – COM78C808 MODE REGISTERS 2 (LINES 0-7) DESCRIPTION

Bit	Description
7:0	XMIT RATE/RECV RATE (Transmitter/Receiver Rate)–Selects the baud rate of the transmitter (bits 7:4) and receiver (bits 3:0) as follows:

Transmitter Bits				Receiver Bits				Nominal	Actual	Error*
7	6	5	4	3	2	1	0	Rate	Rate	(percent)
0	0	0	0	0	0	0	0	50	same	—
0	0	0	1	0	0	0	1	75	same	—
0	0	1	0	0	0	1	0	110	109.09	0.826
0	0	1	1	0	0	1	1	134.5	133.33	0.867
0	1	0	0	0	1	0	0	150	same	—
0	1	0	1	0	1	0	1	300	same	—
0	1	1	0	0	1	1	0	600	same	—
0	1	1	1	0	1	1	1	1200	same	—
1	0	0	0	1	0	0	0	1800	1745.45	3.03
1	0	0	1	1	0	0	1	2000	2021.05	1.05
1	0	1	0	1	0	1	0	2400	same	—
1	0	1	1	1	0	1	1	3600	3490.91	3.03
1	1	0	0	1	1	0	0	4800	same	—
1	1	0	1	1	1	0	1	7200	6981.81	3.03
1	1	1	0	1	1	1	0	9600	same	—
1	1	1	1	1	1	1	1	19200	same	—

*The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1 percent. This variance results in an error that must be added to the error listed.

TABLE 7 – COM78C808 COMMAND REGISTERS (LINES 0-7) DESCRIPTION

Bit	Description
7,6	OPER MODE (Operating mode)–These bits control the operating mode of the channel as follows. These bits are cleared by asserting the RESET input. **Bit 7 / Bit 6 / Operating Mode** 0 0 Normal operation 0 1 Automatic echo 1 0 Local loopback 1 1 Remote loopback
5	RxIE (Receiver interrupt enable)–When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt.
4	RERR (Reset error)–When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by asserting the RESET input (not self-clearing).
3	TxBRK (Transmit break)–When set, this bit forces the appropriate TxD<7:0> line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by asserting the RESET input.
2	RxEN (Receiver enable)–When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by asserting the RESET input.
1	TxIE (Transmit interrupt enable)–When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is asserted and generates an interrupt by asserting the IRQ signal.
0	TxEN (Transmitter enable)–When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with this line, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by asserting the RESET input.

Bits 5 through 0 enable the line's receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to "Interrupt Scanner" and "Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are:

- ☐ Normal operation–The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. (The RxEN bit must be set.) Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. (The TxEN bit must be set.)

- ☐ Automatic echo–The serial data received is assembled into parallel in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxD<n> pin for serial output. TxEN is ignored and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.
- ☐ Local loopback–The serial data from the RxD<n> input is ignored and the receiver serial input receives data from the transmitter serial output. The data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. (The TxEN bit must be set.) The transmission goes only to the receiver serial input; the TxD<n> output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.
- ☐ Remote loopback–The serial data received on the RxD<n> line is returned to the TxD<n> line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

SUMMARY REGISTERS

The Octal UART contains two registers that summarize the current status of all eight serial data lines, making it possible to determine that a line's status has changed with a single read operation. These registers are selected for access by setting the appropriate address on pins ADD <2:0>. Because the registers are shared by eight serial lines, the line-selection bits (ADD <5:3>) are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

Interrupt summary register–This read-only register indicates that a transmitter or receiver interrupt condition has occured, and indicates the line number that generated the interrupt. Figure 7 shows the format of the interrupt summary register and Table 8 describes register information.

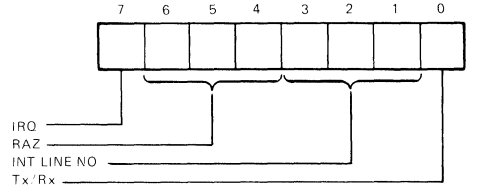


FIGURE 7 – COM78C808 INTERRUPT SUMMARY REGISTER FORMAT

TABLE 8 – COM78C808 INTERRUPT SUMMARY REGISTER DESCRIPTION

Bit	Description
7	IRQ (Interrupt request)–When set, this bit indicates that the interrupt scanner has found an interrupting condition among the eight serial lines of the Octal UART. These conditions also result in the Octal UART asserting the $\overline{IRQ}$ signal.
6:4	RAZ (Read as zero)–Not used
3:1*	INT LINE NO (Interrupting line number)–These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN <2:0> signals–(bit 3 = IRQLN<2>, bit 2 = IRQLN<1>, and bit 1 = IRQLN<0>. Refer to Table 3.
0*	Tx/$\overline{Rx}$ (Transmit/receive)–This bit indicates whether the interrupting condition was caused by a transmitter (Tx/$\overline{Rx}$ equals 1) or a receiver (Tx/$\overline{Rx}$ equals 0). This bit corresponds to the IRQTxRx signal of the Octal UART and is set when IRQTxRx is asserted.

*Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

Data set change summary register–When the $\overline{DSR}$ or $\overline{DCD}$ inputs that are associated with a line change state, the bit corresponding to that line in this read-only register is set. The current state of the $\overline{DSR}$ and $\overline{DCD}$ inputs can then be obtained from that line's status register. If the state of a line changes twice within one microsecond, the change in state may not be detected. Figure 8 shows the format of the data set change summary register.

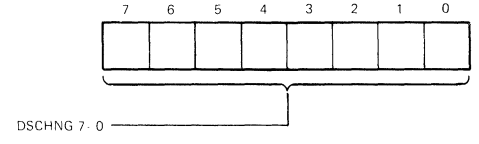


FIGURE 8 – COM78C808 DATA SET CHANGE SUMMARY REGISTER FORMAT

When the MCIE bit in a line's mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and assert the $\overline{IRQ}$ signal. The data set change summary register bits are cleared by writing a 1 into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled and writeback should directly follow the read operation.

Assertion of the $\overline{RESET}$ signal disables and initializes the data set change logic. When the $\overline{RESET}$ signal is deasserted, future changes in $\overline{DSR}$ and $\overline{DCD}$ are reported as they occur.

INTERRUPT SCANNER AND INTERRUPT HANDLING

The interrupt scanner is a four-bit counter that sequentially checks lines 0 through 7 for a receiver interrupt (counter positions (0-7) and then checks the lines in the same order for a transmitter interrupt (counter positions 8-15). If the scanner detects an interrupt condition, it stops and the $\overline{IRQ}$ signal is asserted. An interrupt must be serviced by software or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line's receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = 1) or either of the line's modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG and RxIE and MCIE = 1).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE = 1).

When the scanner detects an interrupt, it reports the line number on the IRQ<2:0> lines. The IRQTxRx signal is asserted for a transmitter interrupt and deasserted for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line is deasserted and the scanner is restarted for each of the following three types of interrupt conditions.

- ☐ Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- ☐ Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- ☐ Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line 0's receiver), thus giving receivers priority over transmitters.

EDGE-TRIGGERED AND LEVEL-TRIGGERED INTERRUPT SYTSTEMS

If the interrupt system of the Octal UART is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

MODEM HANDLING

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deasserting the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The assertion of the TxEMT bit to indicate that transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to assert before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character (a starter bit–5,6,7, or 8 data bits; plus parity bit if enabled; and 1,1.5, or 2 stop bits), and multiplying by either two characters or one, depending on when TxEMT monitoring begins.

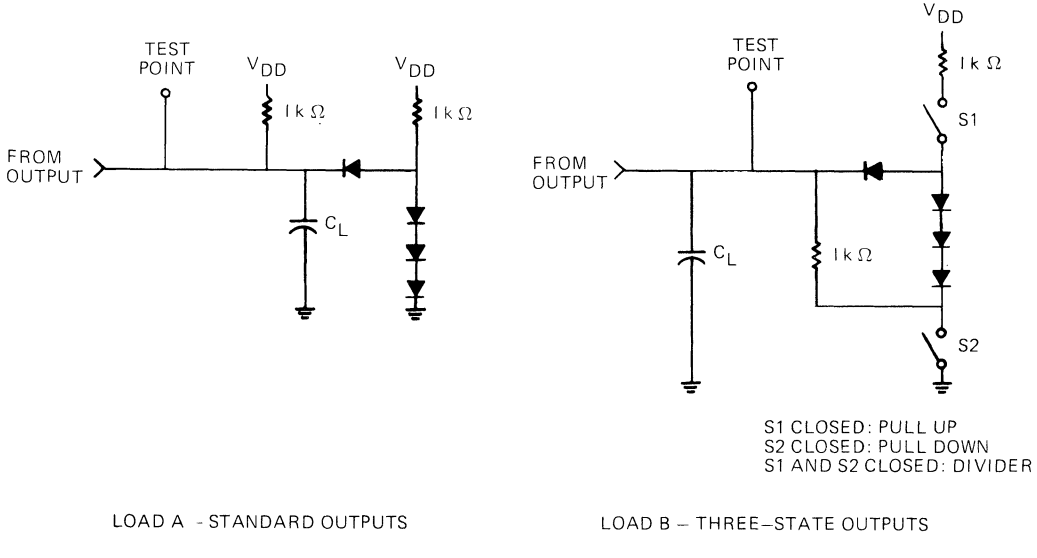


FIGURE 9 – COM78C808 OUTPUT LOAD CIRCUITS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +125°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... Vcc + 0.3
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Maximum Vcc ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

TABLE 9 – COM78C808

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{DD} = +5V ±5%

Symbol	Parameter	Test Condition	Requirements Min.	Requirements Max.	Units
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage	V_{DD} = Min. I_{OH} = 3.5 mA for DL<7:0> I_{OH} = 2.0 mA for all remaining output except $\overline{IRQ}$ and $\overline{RDY}$	2.4		V
V_{OL}	Low-level output voltage	V_{DD} = Min. I_{OL} = 5.5 mA for DL<7:0> I_{OL} = 3.5 mA for all remaining outputs		0.4	V
I_{IH}	Input current at maximum input voltage	V_{DD} = Max. V_I = V_{DD}(Max.)		10	µA
I_{IL}	Input current at miminum input voltage	V_{DD} = Max. V_I = 0.0V		−10	µA
I_{OS}[1]	Short-circuit output current for DL<7:0> all remaining outputs except $\overline{IRQ}$ and $\overline{RDY}$	V_{DD} = Max.	−50 −30	−180 −110	mA mA
I_{OZL}[2]	Three-state output current	V_{DD} = Max. V_O = 0.4V		10	µA
I_{OZH}[2]	Three-state output current	V_{DD} = Max. V_O = 2.4V		10	µA
I_{DD}	Supply current	V_{DD} = Max. T_A = 0°		25	mA
C_{in}	Input capacitance			4	pF
C_{IO}[3]	Input/output capacitance			5	pF

[1]No more than one ouput should be short circuited at a time, and the duration of the short should not exceed 1 second.
[2]All three-state output drivers are wired in an I/O configuration. The parameters include the driver and input receiver leakage currents.
[3]The parameters include the capacitive loads of the output driver and the input receiver.

TIMING PARAMETERS

Figure 10 shows the signal timing for a read cycle to transfer information from the Octal UART to the processor. Figure 11 shows the signal timing for a write cycle to transfer information from the processor to the Octal UART. Table 11 lists the timing parameters for the read and write cycles.

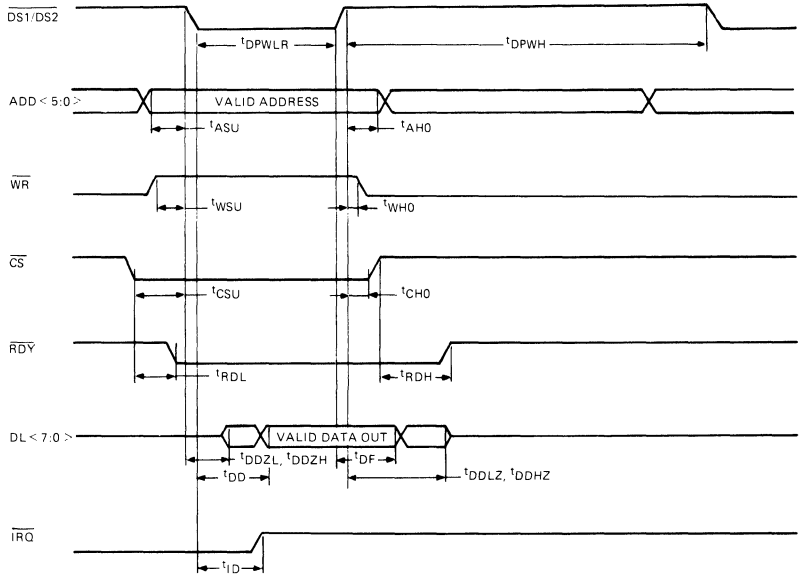


FIGURE 10 – COM78C808 BUS READ CYCLE TIMING

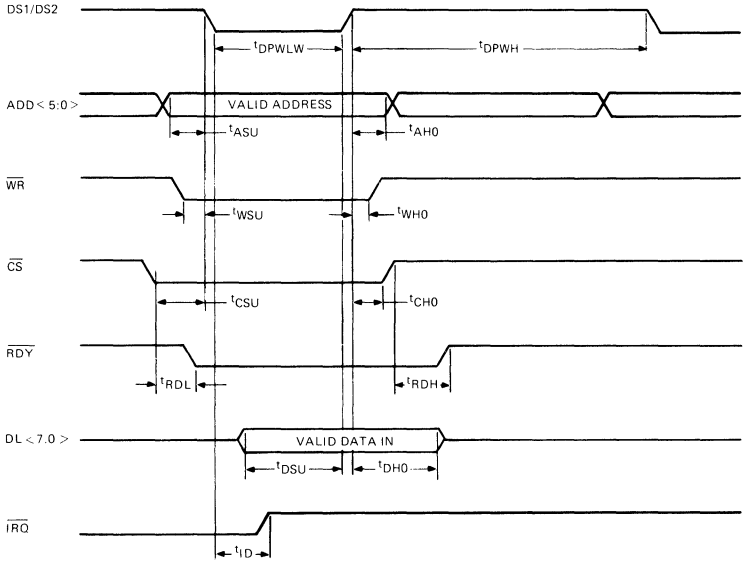


FIGURE 11 – COM78C808 BUS WRITE CYCLE TIMING

TABLE 10 – COM78C808 BUS READ AND WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Max.	Load Circuit[1]
t_{AHO}	Hold time of a valid ADD <5:0> to a valid high level of $\overline{DS1}$ and $\overline{DS2}$.	10		
t_{ASU}	Setup time of a valid ADD <5:0> to the falling edge of $\overline{DS1}$ and $\overline{DS2}$.	30		
t_{CHO}	Hold time of a valid low level of $\overline{CS}$ to a valid high level of $\overline{DS1}$ and $\overline{DS2}$.	10		
t_{CSU}	Setup time of a valid low level of $\overline{CS}$ to the falling edge of $\overline{DS1}$ and $\overline{DS2}$.	30		
t_{DD}	Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to valid high or low data on DL <7:0>.	165		$C_L = 150$ pF
t_{DDLZ}[2] t_{DDHZ}	Propagation delay of a valid high level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output drivers disabled.			
	t_{DDLZ}		50	$C_L = 50$pF
	t_{DDHZ}		50	$C_L = 50$pF
	t_{DDLZ}		60	$C_L = 100$pF
	t_{DDHZ}		60	$C_L = 100$pF
	t_{DDLZ}		65	$C_L = 150$pF
	t_{DDHZ}		65	$C_L = 150$pF
t_{DDZL}	Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output driver enabled.			
	t_{DDZL}	0	165	$C_L = 150$pF
	t_{DDZH}	0	165	$C_L = 150$pF
t_{DF}	Hold time provided during a read cycle by Octal UART of valid high or low data on DL <7:0> after the rising edge of $\overline{DS1}$ and $\overline{DS2}$.	0		
t_{DHO}	Hold time of a valid DL <7:0> to a valid high level of $\overline{DS1}$ or $\overline{DS2}$.	30		
t_{DPWH}	Pulse width high of $\overline{DS1}$ and $\overline{DS2}$.	450		
t_{DPWLR}	Pulse width low of $\overline{DS1}$ and $\overline{DS2}$ when $\overline{WR}$ is high (read operation). Refer to timing parameter t_{DPWLW} also.	180	10,000	
t_{DPWLW}	Pulse width low of $\overline{DS1}$ and $\overline{DS2}$ when $\overline{WR}$ is low (write operation). Refer to timing parameter t_{DPWLR} also.	130	10,000	
t_{DSU}	Setup time of a valid DL <7:0> to the rising edge of $\overline{DS1}$ and $\overline{DS2}$.	50		
t_{ID}[3]	Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low) to a high level on $\overline{IRQ}$.		635	$C_L = 50$pF
t_{RDH}[4]	Propagation delay of a valid high level of $\overline{CS}$ to a valid high level on $\overline{RDY}$.		210	$C_L = 50$pF
t_{RDL}	Propagation delay of a valid low level on $\overline{CS}$ to a valid low level on $\overline{RDY}$.		90	$C_L = 50$pF
t_{WHO}	Hold time of a valid high or low level of $\overline{WR}$ to a valid high level of $\overline{DS1}$ and $\overline{DS2}$.	10		
t_{WSU}	Setup time of a valid high or low level of $\overline{WR}$ to the falling edge of $\overline{DS1}$ or $\overline{DS2}$.	30		

[1]Refer to Figure 9 for the load circuits used with these measurements.
[2]The t_{DDLZ} and t_{DDHZ} parameters are measured with $C_L = 150$ pF. The values of t_{DDLZ} and t_{DDHZ} for $C_L = 50$pF and $C_L = 100$ pF have been derived for user convenience.
[3]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{ID} parameter can be calculated by the following: $t_{ID} = 500 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.
[4]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The t_{RDH} parameter can be calculated by the following: $t_{RDH} = 75 + RC_L$ where R = value of the resistor that connects to capacitor C_L in load A, Figure 9.

Figure 12 shows the signal timing for the clock input, interrupt timing, effect of the $\overline{RESET}$ input on data strobe, data set carrier detect (DCD) and data set ready (DSR) input timing, and the transmit data output timing. Table 11 lists the timing parameters for Figure 12.

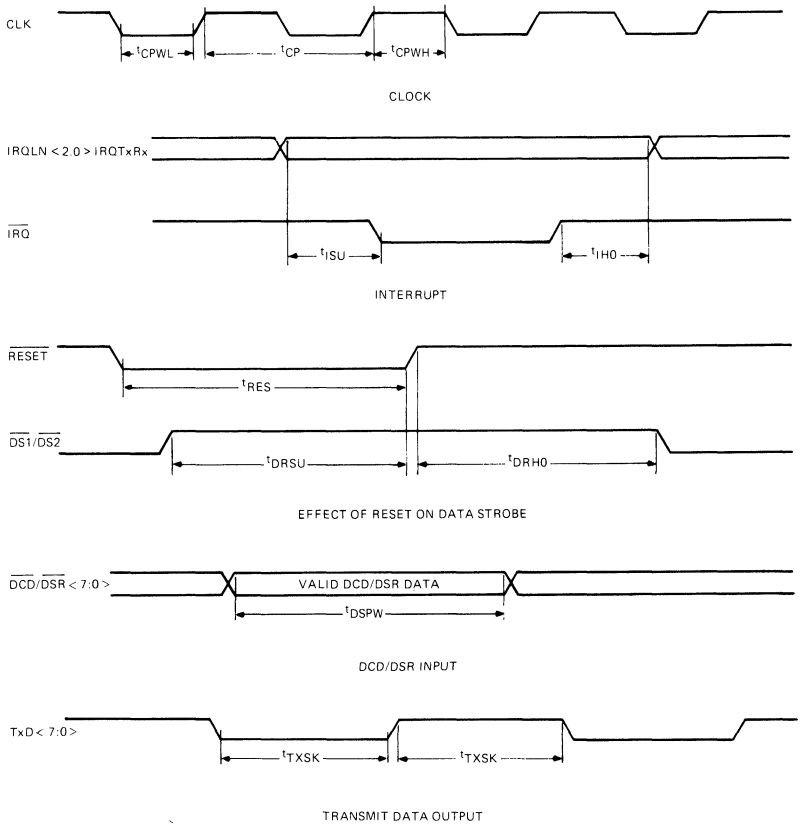


FIGURE 12–COM78C808 MISCELLANEOUS SIGNAL TIMING

TABLE 11–MISCELLANEOUS WRITE TIMING PARAMETERS

Symbol	Definition	Requirements (ns) Min.	Load Circuit*
t_{CP}	Period of CLK.	203.45 (4.9152 MHz)	
t_{CPWH}	Pulse width high of CLK.	95	
t_{CPWL}	Pulse width low of CLK.	95	
t_{DRHO}	Hold time of a valid high level of $\overline{DS1}$ and $\overline{DS2}$ to a valid high level of $\overline{RESET}$.	1,000	
t_{DRSU}	Setup time of a valid high level of $\overline{DS1}$ and $\overline{DS2}$ to the rising edge of $\overline{RESET}$.	900	
t_{DSPW}	Pulse width high or low of DCD <7:0> and DSR <7:0>.	1,000	
t_{IHO}	Hold time provided by Octal UART from a valid IRQLN <2:0> and IRQTxRx to a valid high level of IRQ.	100	$C_L = 50pF$
t_{ISU}	Setup time provided by Octal UART from a valid IRQLN <2:0> and IRQTxRx to a valid low level of $\overline{IRQ}$.	100	$C_L = 50pF$
t_{RES}	Pulse width low of $\overline{RESET}$.	1,000	
t_{TXSK}	Pulse width high or low provided by Octal UART on the TxD <7:0> lines. At each baud rate, the actual pulse widths provided vary by t_{TXSK}. This timing parameter should be used to determine cumulative reception/transmission errors.	250	$C_L = 50pF$

*Refer to Figure 9 for the load circuits used with these measurements.

Figure 13 shows the input and output voltage waveforms for the propagation delay and setup and hold measurements. Figure 14 shows the waveforms for the three-state outputs measurement.

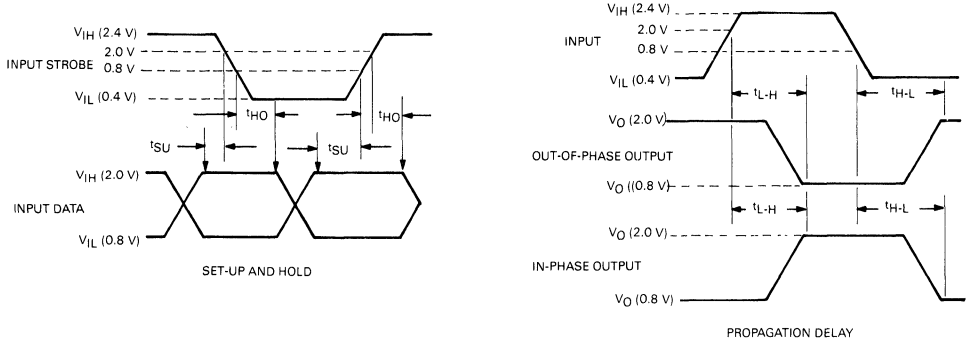
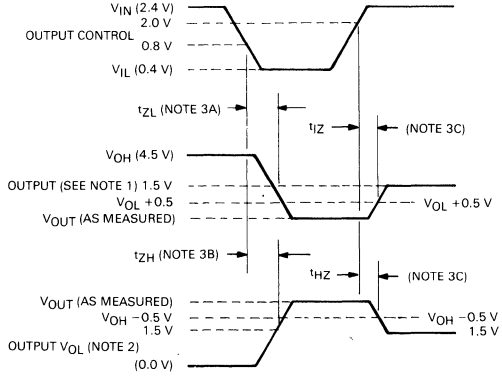


FIGURE 13 – COM78C808 PROPAGATION DELAY AND SETUP AND HOLD VOLTAGE WAVEFORMS



NOTES:
1. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
2. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
3. REFER TO FIGURE 9. A = S1 CLOSED, B = S2 CLOSED, C = S1 AND S2 CLOSED.

FIGURE 14 – COM78C808 THREE-STATE OUTPUT VOLTAGE WAVEFORMS

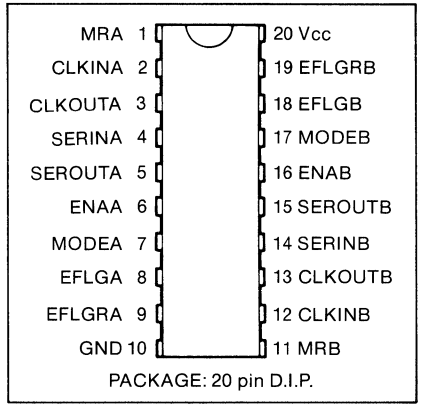
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX 510 227 8898

Dual 32 Bit CRC SDLC Generator/Checker CRC-32

FEATURES

- ☐ SDLC 32 bit CRC
- ☐ COM 5025 USYNRT Companion
- ☐ Data Rate—2MHz typical
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 20 pin D.I.P.

GENERAL DESCRIPTION

SMC's COM 8004 is a dual 32-bit CRC Generator/Checker for use with SDLC protocols. It is a companion device to SMC's COM 5025 USYNRT. It operates at bit rates from DC to 2.0 MHz from a single +5v supply and is housed in a 20 lead x 0.3 inch DIP. All inputs and outputs are TTL compatible with full noise immunity.

The COM 8004 is comprised of two independent halves, and each half may be operated in the check or generate mode. The polynominal used in computations is:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.

The CRC register is initialized to all ones and the result is inverted before being appended to the message. The expected remainder is:
$X^{31} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^4 + X^3 + X + 1$.

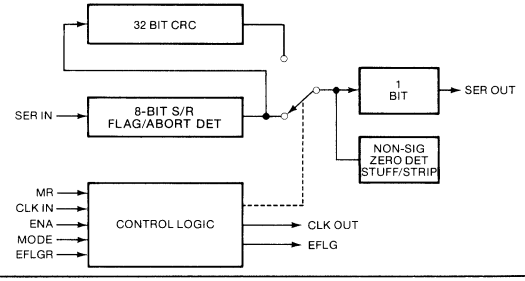
Each half has a nine-bit serial data shift register. Data moves on the positive edge of the clock, and all clocked inputs are designed for zero-hold-time (e.g. 7474). A "clock out" pin provides gated clocks to the accompanying USYNRT (COM 5025).

In the generate mode, computation is initiated upon detection of a flag character in the serial bit stream. CRC computation proceeds upon the serial data until a second flag is detected. CLK OUT to the SDLC transmitter is then halted, and the 32-bit CRC is passed out; CLK OUT is then resumed, and the flag character is passed out. Nonsignificant zeros are automatically stripped and stuffed, and shared flags are supported. If the data between flags is less than two full bytes, the CRC is discarded and the serial data stream remains unaltered.

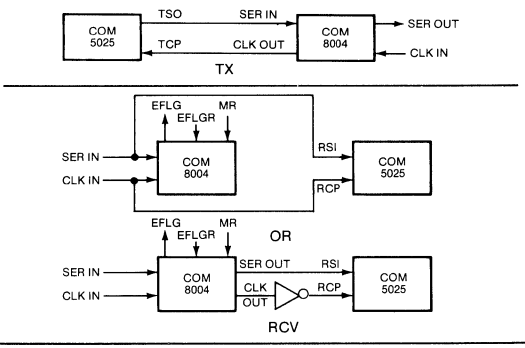
In the check mode, computation is similarly initiated upon detection of a flag. Detection of a second flag causes the conditional setting of the error flag. A separate reset pin is provided for the error flag. No error is flagged on messages of less than two full bytes between flags. Detection of an abort character (7 consecutive ones) in either mode causes computation to be reset and a search for an opening flag resumed.

BLOCK DIAGRAM

FOR ONE-HALF OF THE COM 8004



TYPICAL SYSTEM



For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 • TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

COM 8017
COM 8502

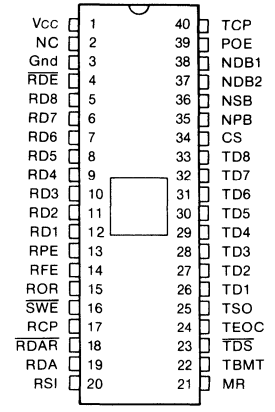
SECTION III

Universal Asynchronous Receiver/Transmitter
UART

FEATURES

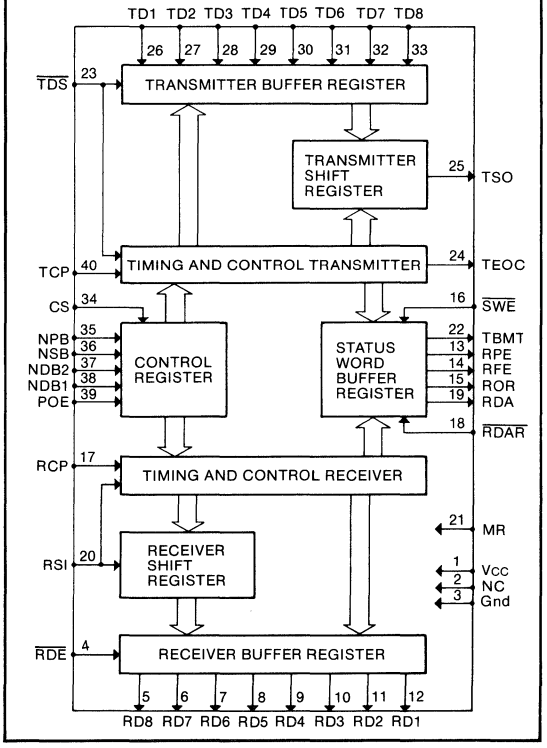
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility — no interfacing circuits required
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ High Speed Operation — 40K baud, 200ns strobes
- ☐ Master Reset — Resets all status outputs
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Low Power — minimum power requirements
- ☐ Input Protected — eliminates handling problems
- ☐ Ceramic or Plastic Dip Package — easy board insertion
- ☐ Compatible with COM 2017, COM 2502
- ☐ Compatible with COM 8116, COM 8126, COM 8136, COM 8146, COM 8046 Baud Rate Generators

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits. In addition the COM 8017 will provide 1.5 stop bits when programmed for 5 data bits and 2 stop bits. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

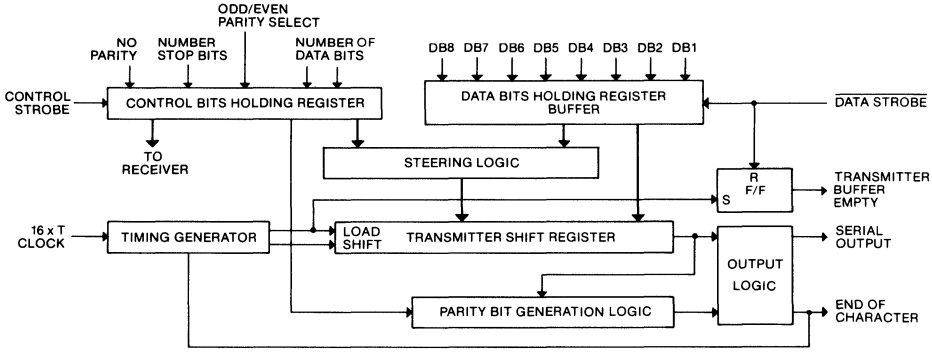
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the $\overline{TBMT}$ signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

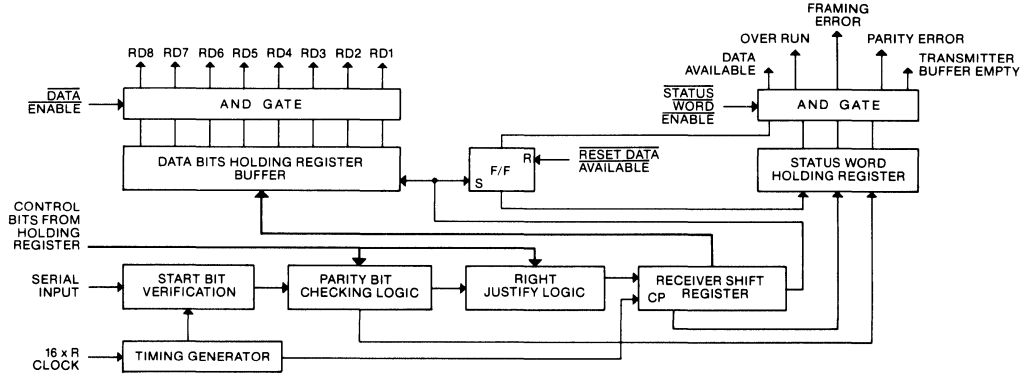
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	NC	No Connection	No Connection
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

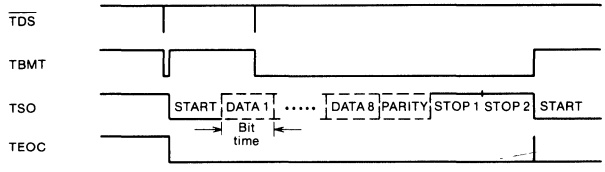
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

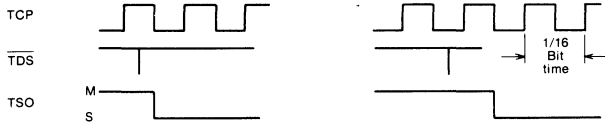
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 8017 or COM 8017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

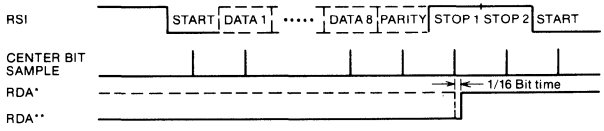


TRANSMITTER START-UP



Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of TDS.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY

If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin. with respect to ground ..... −0.3V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	0		0.8	V	
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	$V_{IN} = GND$
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, Ios**			30	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{CC}
A.C. CHARACTERISTICS					$T_A = +25°C$
CLOCK FREQUENCY					
COM8502, COM 8017	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	0.7			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	$\overline{CS}$
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

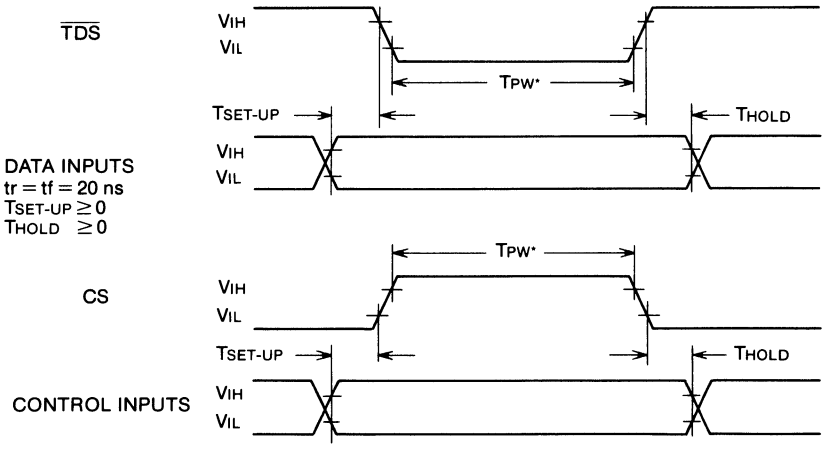
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

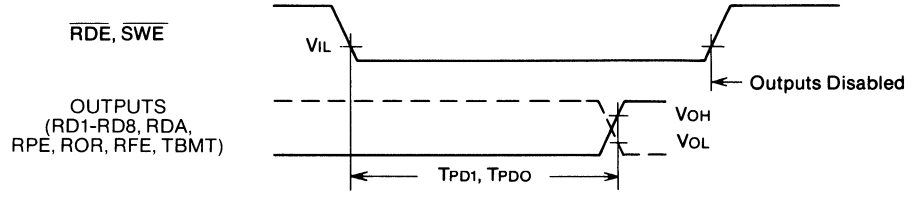
3. The tri-state output has 3 states: 1) low impedance to Vcc 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM

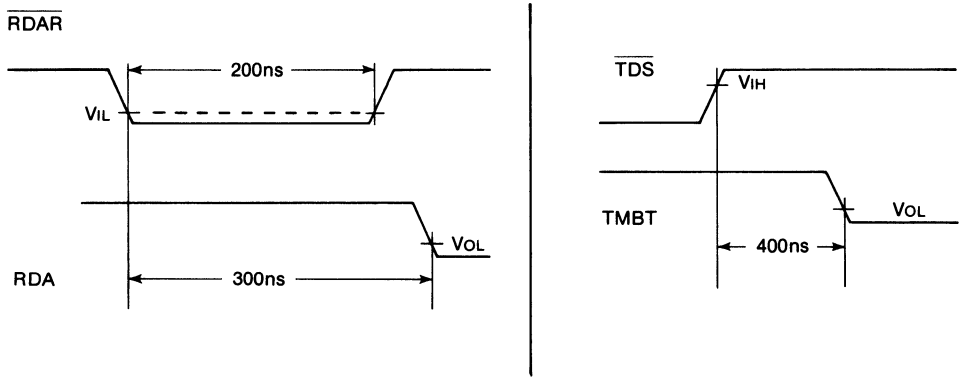


*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

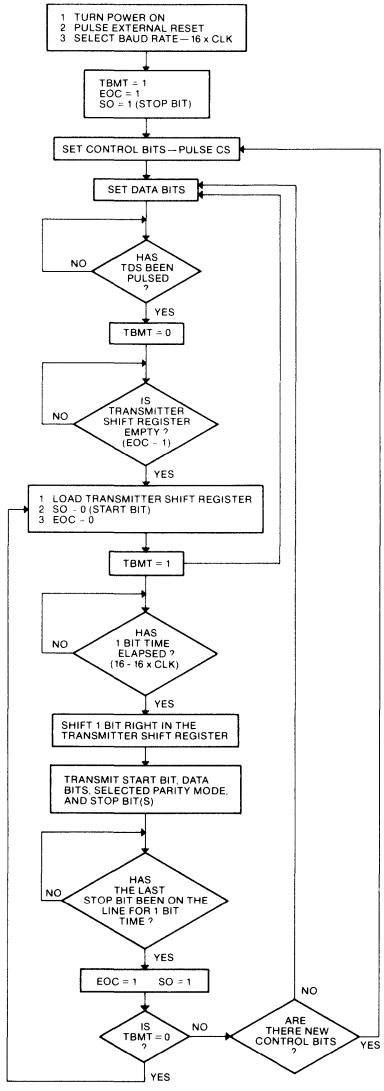
OUTPUT TIMING DIAGRAM



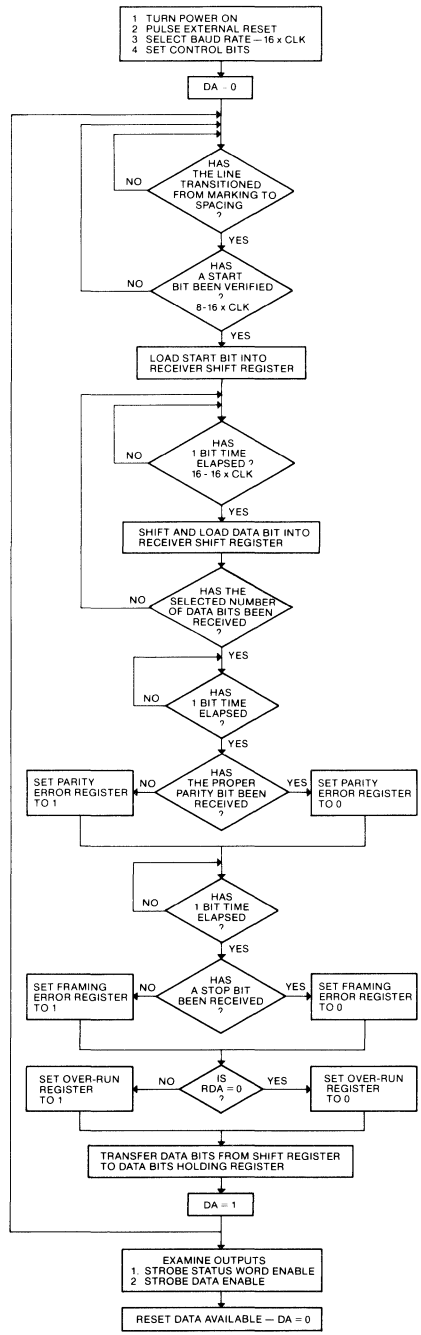
NOTE: Waveform drawings not to scale for clarity.



FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM81C17
PRELIMINARY

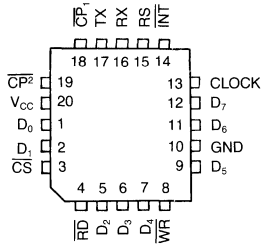
Twenty Pin UART (TPUART)

SECTION III

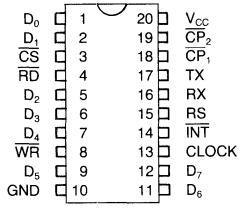
FEATURES

- ☐ Single Chip UART With Baud Rate Generator
- ☐ Asynchronous Operation
  - –16 Selectable Baud Rate Clock Frequencies (Internal)
  - –External 16x Clock (100 KBaud)
  - –Character Length: 7 or 8 Bits
  - –1 or 2 Stop Bit Selection
- ☐ Small 20 Pin DIP (300 mil) or PLCC
- ☐ Full or Half Duplex Operation
- ☐ Double Buffering of Data
- ☐ Programmable Interrupt Generation
- ☐ Programmable Modem/Terminal Signals
- ☐ Odd or Even Parity Generate and Detect
- ☐ Parity, Overrun and Framing Error Detection
- ☐ TTL Compatible Inputs and Outputs
- ☐ High Speed Host Bus Operation (with no wait state)
- ☐ Low Power CMOS
- ☐ Single +5V Power Supply

PIN CONFIGURATION



Package: 20-pin PLCC



Package 20-pin DIP

GENERAL DESCRIPTION

The COM81C17 TPUART is an asynchronous only receiver / transmitter with a built in programmable baud rate generator housed in a twenty pin package. The TPUART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the TPUART will also accept data characters from the processor in parallel format and convert them into serial format along with start, stop and optional parity bits. The TPUART will signal the processor via interrupt when it has completely transmitted or received a character and requires service. Complete status information is available to the processor through the status register. The TPUART features two general purpose control pins that can be individually programmed to perform as terminal or modem control handshake signals.

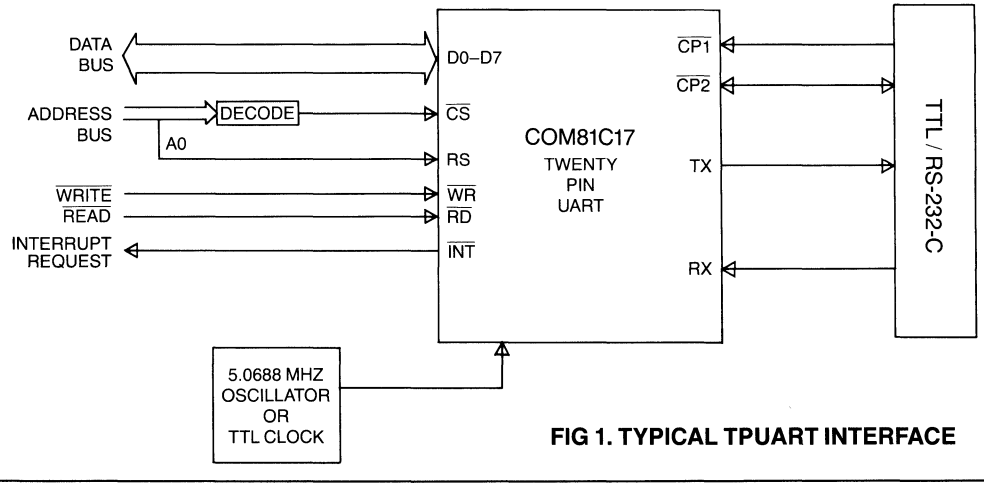


FIG 1. TYPICAL TPUART INTERFACE

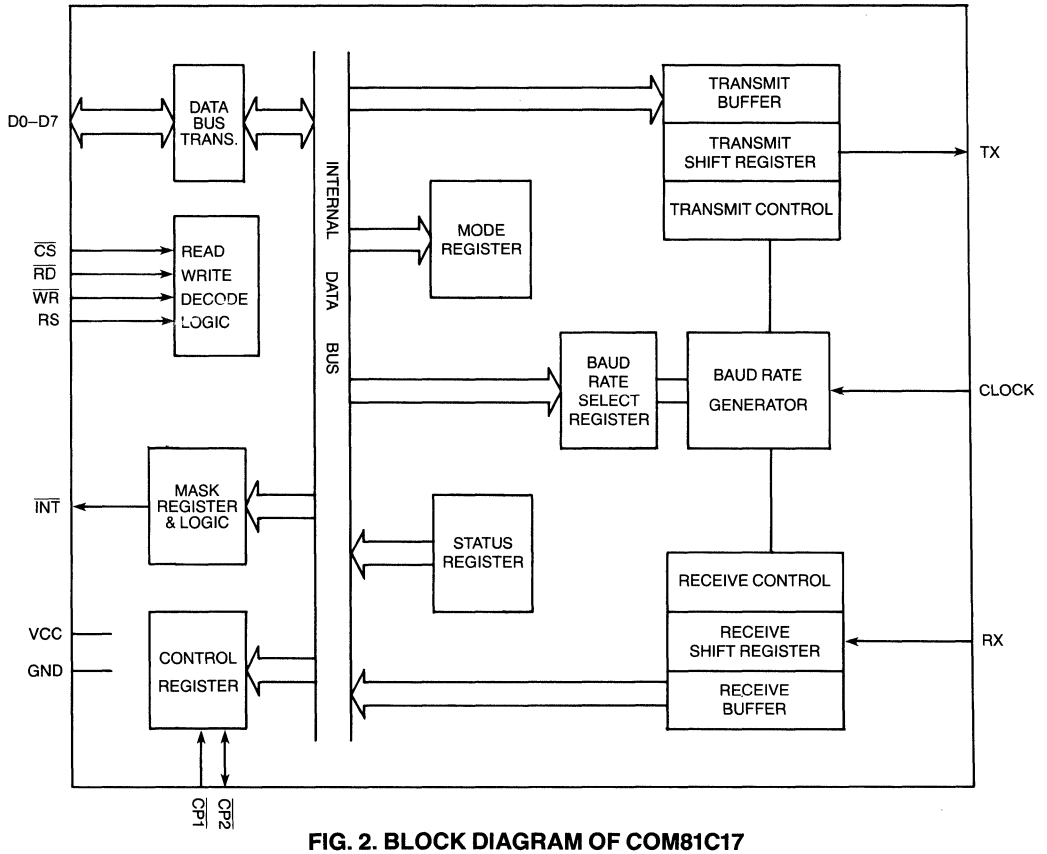


FIG. 2. BLOCK DIAGRAM OF COM81C17

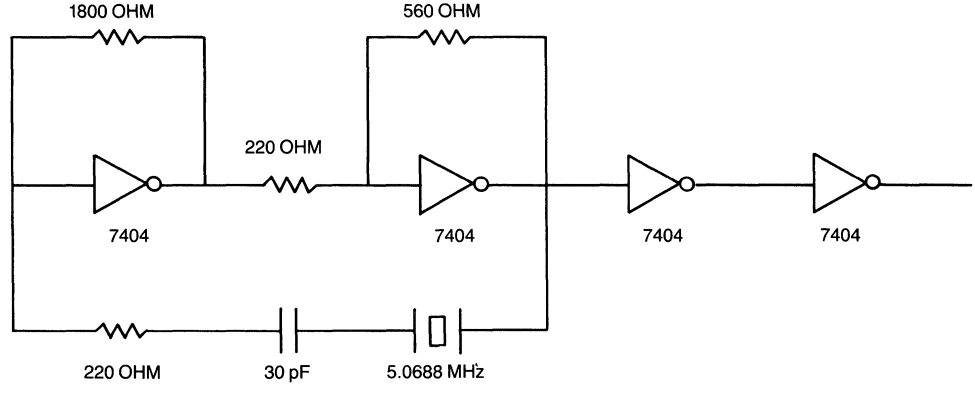


FIG. 2A. 5.0688 MHz CRYSTAL OSCILLATOR CIRCUIT

TABLE 1 – DESCRIPTION OF PIN FUNCTIONS

DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
1, 2, 5–7 9, 11–12	DATA BUS	D_0–D_7	An 8 bit bi-directional DATA BUS is used to interface the TPUART to the processor Data Bus.
3	CHIP SELECT	$\overline{CS}$	A low level on this input enables the TPUART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in high impedance and the $\overline{WR}$ and $\overline{RD}$ will have no effect on the chip.
4	READ DATA STROBE	$\overline{RD}$	A low pulse on this input (when $\overline{CS}$ is low) enables the TPUART to place the data or the status information on the DATA BUS.
8	WRITE DATA STROBE	$\overline{WR}$	A low pulse on this input (when $\overline{CS}$ is low) enables the TPUART to accept the data or control word from the DATA BUS into the TPUART.
10	GROUND	GND	Power Supply Return
13	CLOCK	CLK	External TTL Clock Input (See Table 2)
14	INTERRUPT REQUEST	$\overline{INT}$	An interrupt request is asserted by the TPUART when an enabled condition has occurred in the Status Register. This is an active low, open drain output. This pin has an internal pullup register.
15	REGISTER SELECT	RS	During processor to TPUART communications, this input is used to indicate which internal register will be selected for access by the processor. When this input is low, data can be written to the TX Holding Buffer or data can be read from the RX Holding Register. When this input is high control words can be written to the Control Register or status information can be read from the Status Register.
16	RECEIVER DATA	RX	This input is the receiver serial data. A high to low transition is required to initiate data reception.
17	TRANSMITTER DATA	TX	This output is the transmitted serial data from the TPUART. When a transmission is concluded, the TX line will always return to the mark (High) state.
18	CONTROL PIN 1	$\overline{CP1}$	This control pin is an input only pin. It can be programmed to perform the functions of CTS or DSR/DCD.
19	CONTROL PIN 2	$\overline{CP2}$	This control pin can be programmed to be either an input or an output. When in input mode, this pin can perform the functions of DSR/DCD. When in output mode this pin can perform the functions of DTR or RTS.
20	POWER SUPPLY	V_{CC}	+5V Supply Voltage

FUNCTIONAL DESCRIPTION

RESETTING THE TPUART

The TPUART must be reset on power up. Since there is no external pin allocated for hardware reset, this is accomplished by writing a One (HIGH) followed by writing a Zero (LOW) to the Control Register bit 7. Following reset, the TPUART enters an idle state in which it can neither transmit nor receive data.

INITIALIZING THE TPUART

The TPUART is initialized by writing three control words from the processor. Only a single address is set aside for Mode, Baud Rate Select, Interrupt Mask and TX Buffer Registers. For this to be possible, logic internal to the chip directs information to its proper destination based on the sequence in which it is written.

Following internal reset, the first write to address zero (i.e. RS = 0) is interpreted as a Mode Control word. The second write is interpreted as Interrupt Mask word. The third write is interpreted as Baud Rate Select. The fourth and all subsequent writes are interpreted as writes to the TX Buffer Register.

There is one way in which control logic may return to anticipating a Mode, Interrupt Mask, and Baud Rate Select words. This is following an internal reset. Following initialization, the TPUART is ready to communicate.

PROGRAMMABLE CONTROL PINS

The TPUART provides two programmable control pins that can be configured to perform as modem or terminal control handshake signals. If no handshake signal is required, these pins can be used as general purpose one bit Input or Output ports.

$\overline{CP1}$ – is an input only pin that can be programmed to act as the CTS (Clear To Send) handshake signal, where it will disable data transmission by the TPUART after the contents of the Transmit Shift Register is completely flushed out. When programmed as 1, $\overline{CP1}$ will serve as a general purpose 1 bit input port. The inverted state will be reflected in Status Register bit 0 (when programmed as CTS or general purpose input bit).

$\overline{CP2}$ – is an Input/Output pin. When configured as Output, its state is directly controlled by the host processor via writes to the Control Register. This will serve the purpose of modem and terminal handshake signals as RTS (Request To Send), and DTR (Data Terminal Ready). When configured as Input, its inverted state is reflected in the Status Register bit 1 and read by the processor. This will serve the purpose of handshake signals as DCD (Data Carrier Detect) and DSR (Data Set Ready).

MODE REGISTER		
BIT 1	BIT 2	
0	0	$\overline{CP2}$ is RTS output
0	1	$\overline{CP2}$ is GP output
1	X	$\overline{CP2}$ is GP input
1	X	$\overline{CP2}$ is GP input

THE ON CHIP BAUD RATE GENERATOR

The TPUART incorporates an on chip Baud Rate Generator that can be programmed to generate sixteen of the most popular baud rates. The TPUART also allows the bypassing of the Baud Rate Generator by programming Mode Register bit 3 to accept a 16X external clock. The Baud Rate Generator will not assume any given baud rate upon power up, therefore it must be programmed as desired. The following chart is based on a 5.0688 MHz CLOCK frequency.

TABLE 2 – 16X CLOCK
Clock Frequency = 5.0688 MHz

Baud Rate Select Register				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D_3	D_2	D_1	D_0						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	110	1.76	1.76	—	50/50	2880
0	0	1	0	134.5	2.152	2.1523	0.016	50/50	2356
0	0	1	1	150	2.4	2.4	—	50/50	2112
0	1	0	0	300	4.8	4.8	—	50/50	1056
0	1	0	1	600	9.6	9.6	—	50/50	528
0	1	1	0	1200	19.2	19.2	—	50/50	264
0	1	1	1	1800	28.8	28.8	—	50/50	176
1	0	0	0	2000	32.0	32.081	0.253	50/50	158
1	0	0	1	2400	38.4	38.4	—	50/50	132
1	0	1	0	3600	57.6	57.6	—	50/50	88
1	0	1	1	4800	76.8	76.8	—	50/50	66
1	1	0	0	7200	115.2	115.2	—	50/50	44
1	1	0	1	9600	153.6	153.6	—	48/52	33
1	1	1	0	19.200	307.2	316.8	3.125	50/50	16
1	1	1	1	38.400	614.4	633.6	3.125	50/50	8

REGISTER DESCRIPTIONS
TABLE 3 – COM81C17 MODE REGISTER DESCRIPTION (BITS 0–7)

BIT	DESCRIPTION
0	**CP1**–The Mode Register bit 0 determines whether the CP1 pin will be configured to provide the function of CTS or will serve as a general purpose 1 bit input port. In either case, its state will be reflected in Status Register bit 0. 0→$\overline{CP1}$ = CTS 1→$\overline{CP1}$ = GP INPUT
1	**CP2I/O**–The Mode Register bit 1 determines whether the CP2 pin will be configured as a general purpose 1 bit output port or will serve as a general purpose 1 bit input port. When used as an input, its state is reflected in the Status Register bit 1. When used as an output, its state is controlled by the processor via the Control Register bit 1. 0→$\overline{CP2}$ = OUTPUT 1→$\overline{CP2}$ = INPUT
2	**$\overline{CP2}$**–The mode register bit 2 determines whether the $\overline{CP2}$ pin will be configured to provide the function of RTS or will serve as a general purpose 1 bit output port. 0→$\overline{CP2}$ = RTS 1→$\overline{CP2}$ = GP OUTPUT
3	**CLOCK SELECT**–The Mode Register bit 3 determines whether the internal Baud Rate Generator will supply the TX and RX clocks or the clock on the clock pin will be used as a 16X clock. The Baud Rate Select Register contents will be bypassed when an external 16X clock is used. 0 = INTERNAL CLOCK 1 = EXTERNAL CLOCK (16X)
4	**PARITY ENABLE**–The Mode Register bit 4 determines whether parity generation and checking will be enabled. 0 = PARITY DISABLE 1 = PARITY ENABLE
5	**PARITY**–The Mode Register bit 5 determines whether odd or even parity will be generated and checked. 0 = EVEN PARITY 1 = ODD PARITY
6	**# OF DATA BITS**–The Mode Register bit 6 determines the number of data bit that will be presented in each data character (i.e. 7 or 8). 0 = 7 BITS PER CHARACTER 1 = 8 BITS PER CHARACTER
7	**STOP BITS**–The Mode Register bit 7 determines how many stop bits will trail each data unit (i.e. 1 or 2). 0 = 1 STOP BIT 1 = 2 STOP BITS A data frame will consist of a start bit, 7 or 8 data bits, an optional parity bit, and 1 or 2 stop bits.

TABLE 4 – COM81C17 STATUS REGISTERS DESCRIPTION (BITS 0–7)

BIT	DESCRIPTION
0	**CP1**–This reflects the inverted state of the control pin CP1.
1	**CP2**–This is active only when the $\overline{CP2}$ pin is programmed to be an input. It is set by its corresponding input pin and reflects the inverted state of the control pin $\overline{CP2}$. When the CP2 pin is programmed as an output, this bit is forced to a zero.

2	**TX SHIFT REGISTER EMPTY**–This signals the processor that the Transmit Shift Register is empty. A typical program will usually load the last character of a transmission and then monitor the TX SHIFT REGISTER EMPTY bit to determine when it is a safe time for disabling transmission. This bit is set when the Transmitter Shift Register has completed transmission of a character, and no new character has been loaded in the Transmit Buffer Register. This bit is also set by asserting internal reset. This bit is cleared by: a. loading the TX Buffer Register
3	**PARITY ERROR**–This signals the processor that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. This bit is set when the received character in the Receiver Buffer Register has an incorrect parity bit and parity has been enabled. This bit is cleared by: a. setting Reset Errors in the Control Register b. asserting internal reset
4	**OVERRUN ERROR**–This is set whenever a byte stored in the Receive Character Buffer is overwritten with a new byte from the Receive Shift Register before being transferred to the processor. This bit is cleared by: a. setting Reset Errors in the Control Register b. asserting internal reset
5	**FRAMING ERROR**–This is set whenever a byte in the Receive Character Buffer was received with an incorrect bit format ("0" stop bits). This bit is cleared by: a. setting Reset Errors in the Control Register b. asserting internal reset
6	**TX BUFFER EMPTY**–This signals the processor that the Transmit Buffer Register is empty and that the TPUART can accept a new character for transmission. This bit is set when: a. a character has been loaded from the Transmit Buffer Register to the Transmit Shift Register b. asserting the TRANSMITTER RESET bit in the Control Register c. asserting internal reset This bit is cleared by: a. writing to the Transmit Buffer Register This bit is initially set when the transmitter logic is enabled by setting the TX Enable bit in the Control Register (also TX Buffer is empty because of reset). Data can be overwritten if a consecutive write is performed while TX Buffer Empty is zero.
7	**RX BUFFER FULL**–This signals the processor that a completed character is present in the Receive Buffer Register for transfer to the processor. This bit is set when a character has been loaded from the receive deserialization logic to the Receive Buffer Register. This bit is cleared by: a. reading the Receive Buffer Register b. asserting the RECEIVER RESET bit in the Control Register c. asserting internal reset

TABLE 5 – COM81C17 CONTROL REGISTER DESCRIPTION (BITS 0–7)

BIT	DESCRIPTION
0	Not Used (test mode bit, must be Zero)
1	**CP2**–This bit controls the $\overline{CP2}$ output pin. Data at the output is the logical complement of the register data. When the CP2 bit is set, the $\overline{CP2}$ pin is forced low. When CP2 is RTS, a 1 to 0 transition of the CP2 bit will cause the $\overline{CP2}$ pin to go high one TXc time after the last serial bit has been transmitted.
2	**RX ENABLE**–This bit when reset will disable the setting of the RX BUFFER FULL bit in the Status Register which informs the processor of the availability of a received character in the Receive Buffer Register. The error bits in the Status Register will be cleared and will remain cleared when RX is disabled.
3	**RX RESET**–This will reset the receiver block only.
4	**TX RESET**–This will reset the transmitter block only.
5	**TX ENABLE**–Data transmission cannot take place by the TPUART unless this bit is set. When this bit is reset (disable), transmission will be disabled only after the previously written data has been transmitted.
6	**RESET ERRORS**–This bit when set will reset the parity, overrun, and framing error bits in the Status Register. No latch is provided in the Control Register for saving this bit; therefore there is no need to clear it (error reset = d6.RS. $\overline{WR}$).
7	**INTERNAL RESET**–This bit enables the resetting of the internal circuitry and initializes access to address 0 to be sequential.

INTERRUPT MASK REGISTER DESCRIPTION

This is an eight bit write only register which is loaded by the processor. These bits are used to enable interrupts from the corresponding bits in the Status Register. This register is reset with internal reset.

REGISTER DECODE & TRUTH TABLE

The TPUART provides unique decode capability to three of the seven internal processor accessible register. These are the RX Buffer Register (read only), the Status Register (read only) and the Control Register (write only). The other four registers (write only) are decoded in a sequential manner following reset.

DECODE TRUTH TABLE

RS	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	READ RX BUFFER REGISTER
0	1	0	0	WRITE TO TX BUFFER REGISTER
1	0	1	0	READ STATUS REGISTER
1	1	0	0	WRITE TO CONTROL REGISTER
X	X	X	1	DATA BUS IN TRI STATE

The first write to address zero (RS = 0) will access the Mode Register, the second will access the Interrupt Mask Register, the third will access the Baud Rate Select Register, the fourth and all subsequent writes will access the TX Buffer Register.

INTERNAL REGISTER SELECT

Following reset, the decode sequence of writes to address 0 is as follows:

RS0 – selects the Mode Control Register
RS1 – selects the Interrupt Mask Register
RS2 – selects the Baud Rate Select Register
RS3 – selects the TX Buffer Register

RS0	RS1	RS2	RS3	
0	1	1	1	AFTER RESET
1	0	1	1	AFTER FIRST WRITE
1	1	0	1	AFTER SECOND WRITE
1	1	1	0	AFTER THIRD WRITE
1	1	1	0	ALL SUBSEQUENT WRITES

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... V_{CC} +0.3V
Negative Voltage on any pin, with respect to ground ..... −0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from the laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

TABLE 6 – ELECTRICAL CHARACTERISTICS

T = 0°C to +70°C V_{CC} = 5.0 V ± 5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS						
LOW INPUT VOLTAGE	V_{IL}			0.8	V	
HIGH INPUT VOLTAGE	V_{IH}	2.0			V	
LOW OUTPUT VOLTAGE	V_{OL}			0.4	V	I_{OL} = 5.0ma D_0–D_7 I_{OL} = 3.5ma
HIGH OUTPUT VOLTAGE	V_{OH}	2.4			V	I_{OH} = 100 µa
INPUT LEAKAGE CURRENT	I_L			±10	µA	
INPUT CAPACITANCE	C_{IN}		10		pF	
POWER SUPPLY CURRENT	I_{CC}		15		ma	

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	
AC CHARACTERISTICS						
WRITE CYCLE						
t_1	$\overline{CS}$, RS to $\overline{WR}$ ↓ setup time	50			ns	
t_2	$\overline{CS}$, RS hold time to $\overline{WR}$ ↑	0			ns	
t_3	$\overline{WR}$ pulse width	100			ns	
t_4	Data BUS in setup time to $\overline{WR}$ ↑	75			ns	
t_5	Data BUS in hold time to $\overline{WR}$ ↑	10			ns	
READ CYCLE						
t_6	$\overline{CS}$, RS to $\overline{RD}$ ↓ setup time	50			ns	
t_7	$\overline{CS}$, RS hold time to $\overline{RD}$ ↑	0			ns	
t_8	$\overline{RD}$ pulse width	100			ns	
t_9	Data access time from $\overline{RD}$ ↓	0		60	ns	@50pf max
t_{10}	Data hold time from $\overline{RD}$ ↑	0		60	ns	@50pf max
GENERAL TIMING						
t_{11}	Reset Pulse Width	1.0			µs	
t_{12}	$\overline{CP1}$ active to $\overline{INT}$			300	ns	@25pf
t_{13}	$\overline{WR}$ rising edge to $\overline{CP2}$ change			200	ns	
t_{14}	CP1, CP2 pulse width	1.0			µs	
t_{15}	Read Write Interval	100			ns	
$\overline{CP1}$, $\overline{CP2}$ data						
	Rise Time			30	ns	@25pf
	Fall Time			30	ns	@25pf
Clock Frequency						
	Rise Time			30	ns	
	Fall Time			30	ns	
	Internal Baud Rate Mode			11.0	MHz	
	External Baud Rate Mode			1.6	MHz	
	Duty Cycle			40/60	%	

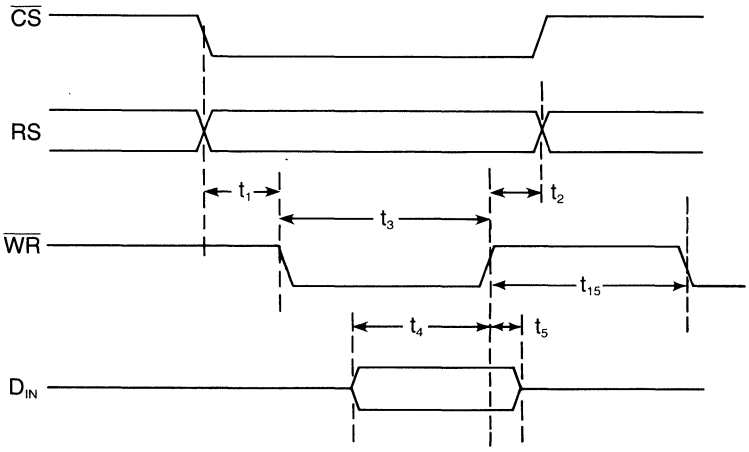


FIG. 3. PROCESSOR TO TPUART WRITE CYCLE

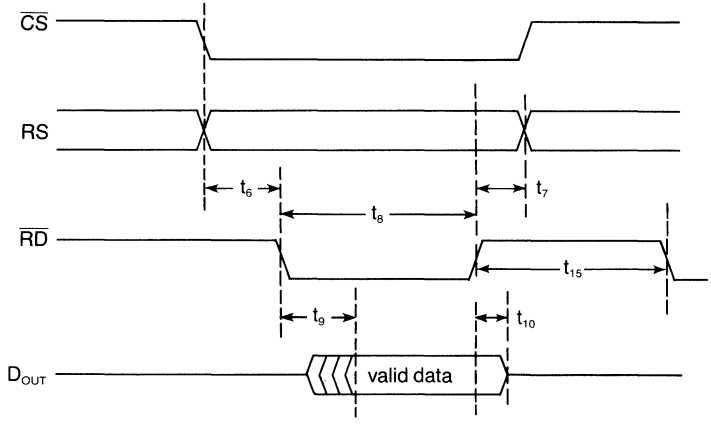


FIG. 4. PROCESSOR FROM TPUART READ CYCLE

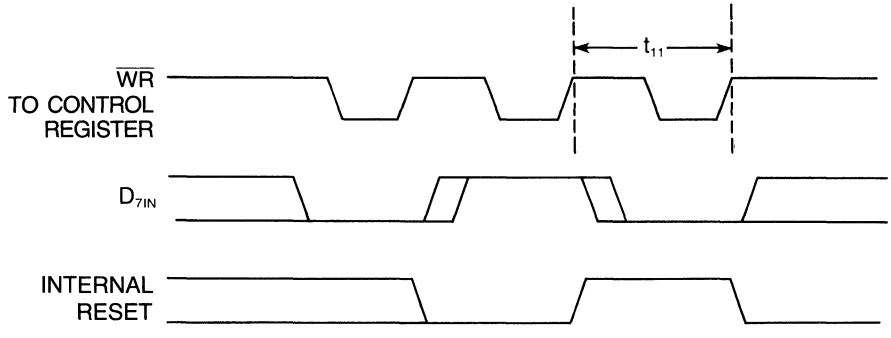


FIG. 5. INTERNAL RESET TIMING

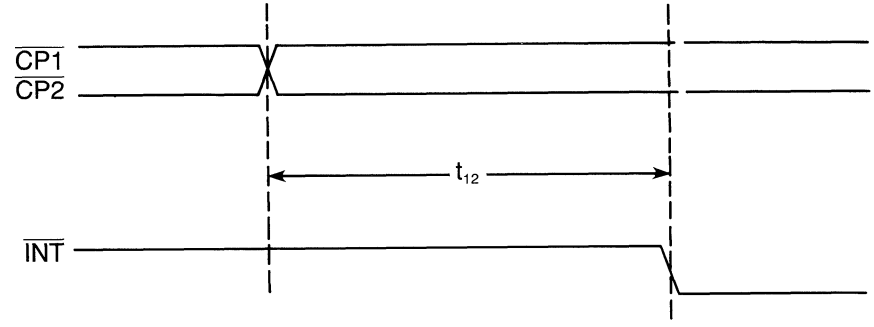


FIG. 6. $\overline{CP1}$ TRANSITION TO $\overline{INT}$

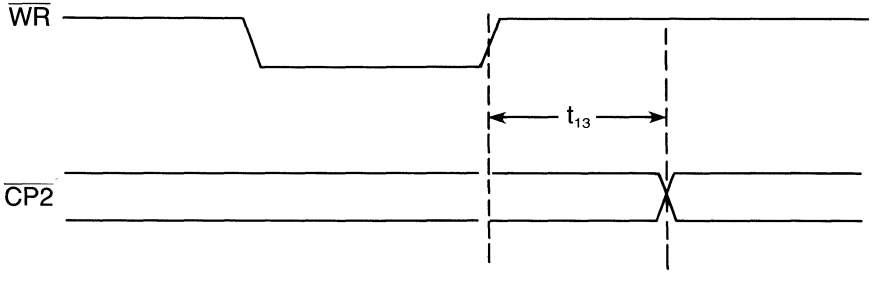


FIG. 7. $\overline{CP2}$ OUTPUT TIMING

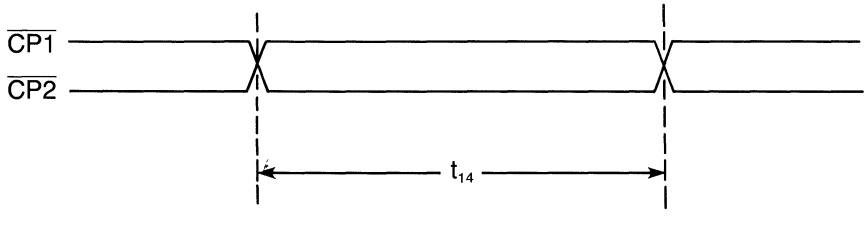


FIG. 8. $\overline{CP1}$, $\overline{CP2}$ INPUT TIMING

STANDARD MICROSYSTEMS CORPORATION

COM82C11
PRELIMINARY

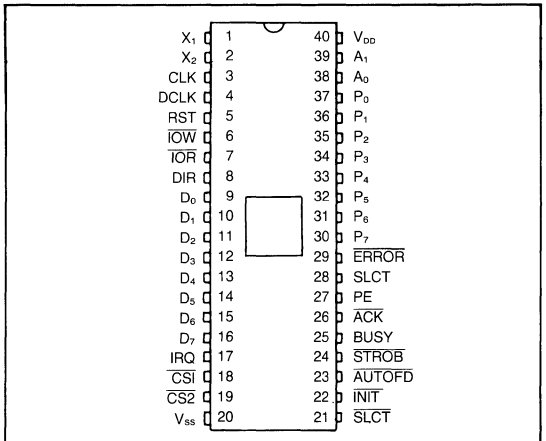
Printer Adapter Interface (PAI)

SECTION III

FEATURES

- ☐ Fits Popular Centronics Printer Interface
- ☐ Programmable parallel printer interface
- ☐ Completely TTL-compatible I/O
- ☐ Reduces system package count
- ☐ User-controlled interrupt request
- ☐ Fully compatible with Z-80 and 8086 microprocessor family
- ☐ High current, direct drive printer interface pins
- ☐ On-chip oscillator can be used to generate 1.5 MHz to 20 MHz oscillation
- ☐ Baud rate generation for serial communication
- ☐ Single 5V supply
- ☐ Low power CMOS

PIN CONFIGURATION



PACKAGE: 40-PIN D.I.P.

GENERAL DESCRIPTION

The COM82C11, Printer Adapter Interface (PAI), fabricated with a silicon gate CMOS process, offers parallel port interface between the CPU and the printer, and is especially suitable to printer adapter for industry-standard personal computers.

The COM82C11 can directly connect to a parallel printer connector. Printer data bus pins can each source 2.6 mA and sink 24 mA. Each of the four printer control pins can source 500μA and sink 7mA. The COM82C11 fits the well-known Centronics printer interface.

The PAI is also suitable for a personal computer interface board which contains RS-232C interface or display interface. The on-chip oscillator and ÷10 divider can be used to offer the BAUD-rate clock with RS-232C interface or the dot clock with monochrome display interface.

The user can use the Data Bus, $\overline{IOR}$, $\overline{IOW}$, IRQ, $\overline{CS1}$ and $\overline{CS2}$ pins to interface the PAI with 8086 or Z-80 microprocessors.

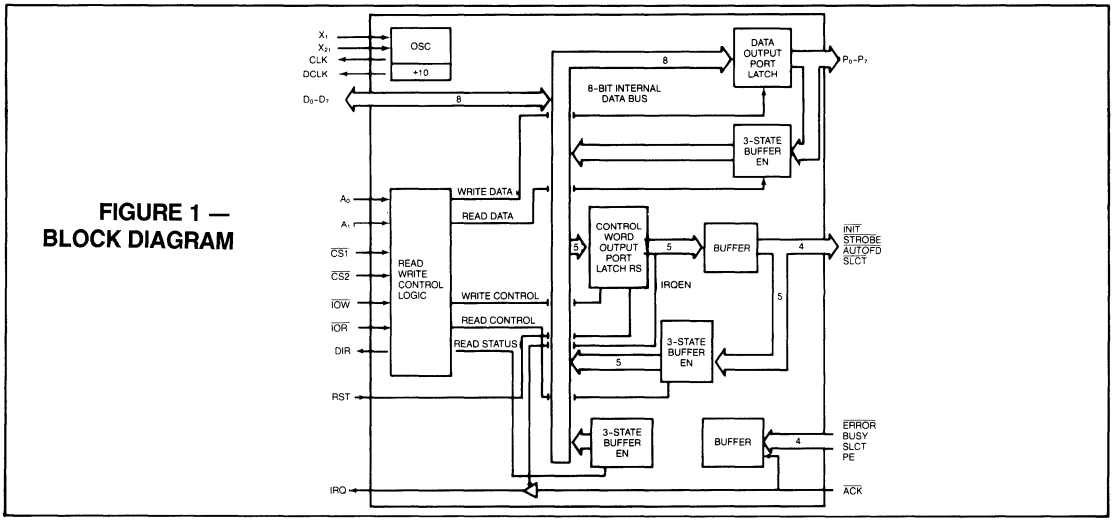


FIGURE 1 — BLOCK DIAGRAM

TABLE 1 — COM82C11 PIN DESCRIPTION

PIN NO.	SYMBOL	NAME	I/O	DESCRIPTION
1 2	X1 X2	Crystal In	I	X1, X2 are the pins to which a crystal (whose frequency is between 1.5 MHz and 20 MHz) is attached. A TTL clock can be used on Pin 2 (X_2) through a pull up resistor. Pin 1 is left open.
3	CLK	Clock Out	O	A buffer oscillating clock output whose frequency is the same as the crystal.
4	DCLK	Divided Clock	O	A buffer clock output whose frequency is one-tenth that of Pin 3.
5	RST	Reset	I	An active high RESET pin. When activated, printer control outputs $\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$ are inactive, $\overline{INIT}$ is active, and IRQ is disabled remaining high impedence.
6	$\overline{IOW}$	I/O Write	I	A "Low" on this pin permits the CPU to write data or control words to the "PAI".
7	$\overline{IOR}$	I/O Read	I	A "Low" on this pin permits the "PAI" to send data, control words or printer status to the CPU. It allows the CPU to read from the PAI.
8	DIR	Direction	O	This output pin is active high only when $\overline{CS1}$, $\overline{CS2}$ and $\overline{IOR}$ are activated. It is low for all other cases. It indicates the direction of data transfer between CPU data bus and the PAI. When activated the PAI sends data, control words or printer status to CPU.
9 ~ 16	D0 ~ D7	System Data Bus	I/O	These bidirectional 8-bit data bus pins are connected to the system data bus. Data or control words are transmitted or received upon execution of input or output instructions by the CPU. Status information of the printer is also received through the data bus.
17	IRQ	Interrupt Request	Z/O	This is an interrupt request output pin, which is generated when $\overline{ACK}$ is activated low. This pin is enabled by writing D4 = 1 in the control word, and is high impedance when D4 = 0. When RST is activated, this pin is put into a high impedance state.
18 19	$\overline{CS1}$ $\overline{CS2}$	Chip Select	I	When $\overline{CS1}$ = 0 and $\overline{CS2}$ = 0, it enables the communication between the CPU and the PAI.
20	V_{ss}	Ground		Power ground pin.
21	$\overline{SLCT}$	Printer Select	O	When activated low, the printer is selected. This pin is programmable in bit $\overline{D3}$ by writing a control command. Writing a one to D_3 outputs a low on the $\overline{SLCT}$ pin.
22	$\overline{INIT}$	Initiate	O	When activated low, the printer buffer is cleared. This pin is programmable in bit D2 by writing a control command and the PAI outputs D2 signal to this pin. The pulse width of the $\overline{INIT}$ must be more than 50 μs for initiation of the printer.
23	$\overline{AUTOFD}$	Auto Feed	O	When this pin is low, the printer is fed automatically, one line after printing. This pin is programmable in $\overline{D1}$ by writing a control command. Writing a one to D1 outputs allow on the $\overline{SLCT}$ pin.
24	$\overline{STROB}$	Data Strob	O	When activated low, the printer reads in the data on printer data bus P0 ~ P7. It syncronizes data strobe between PAI and printer. This pin is programmable in bit D0 by writing a control command, and writing a one to D0 outputs a low on the $\overline{SLCT}$ pin. Read-in of data is performed at the low level of this signal.
25	BUSY	Busy State	I	This is an output from the printer. A "High" indicates that the printer can't receive data "During Data Entry", "During Part of Paper Feed", "During Printer Error Status", "During Printing" or "In Off-Line State". The CPU can read this status in D7 by "Reading Status".
26	$\overline{ACK}$	Acknowledge	I	This is an output from the printer. A "Low" indicates that data bus has been received and that the printer is ready to accept other data. The CPU can read this status in $\overline{D6}$ by a "Read Status" command.

TABLE 1 — COM82C11 PIN DESCRIPTION

PIN NO.	SYMBOL	NAME	I/O	DESCRIPTION
27	PE	Paper End	I	This is an output from the printer. A "High" indicates that the printer is out of paper. The CPU can read this status in $\overline{D5}$ by a "Read Status" command.
28	SLCT	Printer Selected Status	I	This is always "High" unless the printer power is down. The CPU can read this status in $\overline{D4}$ by a "Read Status" command.
29	$\overline{ERROR}$	Error Status		This is an output from the printer. It is "Low" only when the printer is in error status as shown below: (1) Paper end status. (2) Abnormal motor operation. (3) Off-line state. The CPU can read this status in D3 by a "Read Status" command.
30 ~ 37	P0 ~ P7	Printer Data Bus	O	These output pins send out the data to the printer as specified by the CPU in a "Write Data" command. They are compatible with TTL logic level. The CPU can also "Read Back" the data which the CPU last wrote by a "Read Data" command.
38 39	A0 A1	Address	I	These input addresses in conjunction with $\overline{IOR}$, $\overline{IOW}$, $\overline{CS1}$ and CS2 control the selection of one of the five commands.
40	V_{DD}	Power Supply		+5V.

Note: The CPU can "Read Back" the control command it last wrote by reading the control word. There are $\overline{STROB}$, $\overline{AUTOFD}$ $\overline{INIT}$, $\overline{SLCT}$ and IRQEN on the data bus D0 ~ D7.

FUNCTIONAL DESCRIPTION

When reset is activated (RST=1), STROBE=1, AUTOFD=1, INIT=0, SLCT=1, and Interrupt Request "IRQ" is disabled. PAI offers five kinds of commands selected by A0, A1, IOW, IOR and CS1, CS2 as shown below:

Input						Output	Operation
$\overline{CS1}$	$\overline{CS2}$	A1	A0	$\overline{IOR}$	$\overline{IOW}$	DIR	
1	x	x	x	x	x	0*	PAI not activated.
x	1	x	x	x	x	0*	
0	0	0	0	1	0	0	Write data to the printer.
0	0	0	0	0	1	1	Read data on printer data bus.
0	0	0	1	0	1	1	Read status from the printer.
0	0	1	0	1	0	0	Write control word to the printer.
0	0	1	0	0	1	1	Read control word on printer control bus.
0	0	Others					(No operation.**)

Notes: * When $\overline{CS1}$ = 1 or $\overline{CS2}$ = 1, DIR = 0, indicates that D0 ~ D7 remain "I/O Write" state even though intennal data bus is not used.
** It is illegal to read anything when chip select is active and A0 = A1 = 1.

WRITE DATA to the PRINTER

Data on D0 ~ D7 are present on the P0 ~ P7 bus and sent to the printer. At the rising edge of $\overline{IOW}$, data is latched on the P0 ~ P7 bus until the next falling edge of $\overline{IOW}$.

READ DATA on PRINTER DATA BUS

At the falling edge of $\overline{IOR}$, data latched on P0 ~ P7 is set back to the CPU through D0 ~ D7. The CPU reads back the printer data.

READ STATUS from the PRINTER CPU reads the real-time status of the printer. The states are:

Data	$\overline{D7}$	D6	D5	D4	D3	D2	D1	D0
STATE	BUSY	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	—	—	—

Note: The BUSY state is inverted on D7.

WRITE CONTROL WORD to the PRINTER

CPU writes the control word to the printer. The control signals are:

Data Bus	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL Signal	—	—	—	IRQEN	$\overline{SLCT}$	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROB}$

The control signals are latched on printer control bus at the rising edge of $\overline{IOW}$.

Note: "Interrupt Request Enable (IRQEN)" is not present on any output pin, but enables the output pin IRQ when D4 = 1, and disables IRQ (high impedance) when D4 = 0. $\overline{SLCT}$, $\overline{AUTOFD}$ and $\overline{STROB}$ are inverted on D3, D1 and D0 individually.

READ CONTROL WORD on PRINTER CONTROL BUS

At the falling edge of $\overline{IOR}$, IRQEN control bit $\overline{SLCT}$ pin, $\overline{INIT}$ pin, $\overline{AUTOFD}$ pin and $\overline{STROB}$ pin are sent back to the CPU on D4, D3, D2, D1 and D0 individually.
(1) When writing control words D4 = 0 ————→ IRQ pin floating.
(2) When writing control words D4 = 1 ————→ IRQ = $\overline{ACK}$.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -65°C -150°C
Lead Temperature (soldering 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... V_{cc} + 0.3V
Negative Voltage on any I/O Pin, with respect to ground ..... -0.3V
Maximum V_{cc} ..... +7V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

TABLE 2 — ELECTRICAL CHARACTERISTICS (T_a = C° -70°C, V_{cc} = +5V ± 5%, C_l = 50pF)

D.C. Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	COMMENTS
V_{IL}	Input Low Voltage	—	0.4	0.8	V	
V_{IH}	Input High Voltage	2.0	2.4	—	V	
V_{OL}	Output Low Voltage		0.4	0.5	V	I_{OL} = Max
V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} = Max
I_{IN}	Max. Input Current	—	—	±10	μV	V_{IN} = V_{CC} or GND
I_{OLD}	Output Sink Current Printer Data Bus = 0	20	24	—	ma	V_{OL} = 0.45V
I_{OHD}	Output Source Current Printer Data Bus = 1	2.0	2.6	—	ma	V_{OH} = 3.0V
I_{OLC}	Output Sink Current Printer Control Bus = 0	7.0	—	—	ma	V_{OL} = 0.45V
I_{OHC}	Output Source Current Printer Control Bus = 1	—	0.5	1.5	ma	V_{OH} = 3.0V
I_{FL}	Floating Pin Leakage	—	—	±10	μa	V_{FL} = V_{CC} or GND
I_{OP}	Operation Current	—	10	30	ma	

A.C. Characteristics

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE				
T_{WW}	Write Pulse Width	200	—	ns
T_{AW}	Address to $\overline{IOW}$ Set-up Time	0	—	ns
T_{WA}	Address Hold Time after $\overline{IOW}$	20	—	ns
T_{DW}	Data to $\overline{IOW}$ Set-up Time	70	—	ns
T_{WD}	Data Hold Time after $\overline{IOW}$	30	—	ns
T_{WOL}	$\overline{IOW}$ = 1 to Data Latched	—	90	ns
READ				
T_{RR}	Read Pulse Width	300	—	ns
T_{DD}	DIR Delay after $\overline{IOR}$	—	35	ns
T_{AR}	Address to $\overline{IOR}$ Set-up Time	0	—	ns
T_{RA}	Address Hold Time after $\overline{IOR}$	20	—	ns
T_{PR}	Printer Bus to $\overline{IOR}$ Set-up Time	0	—	ns
T_{RP}	Printer Bus Hold Time after $\overline{IOR}$	0	—	ns
T_{RDS}	$\overline{IOR}$ to D0 — D7 Output	—	70	ns
T_{RDR}	D0 — D7 Released after $\overline{IOR}$	—	30	ns

***Note:** When CPU reads the printer's status, it is real-time state.

OTHERS				
T_{RSW}	Reset Pulse Width	40	—	ns
T_{RSCH}	Reset to Control Bus = 1 ($\overline{STROB}$, $\overline{AUTOFD}$, $\overline{SLCT}$) Propagation Delay	—	150	ns
$T_{RSIN\ 1}$	Reset to Control Bus $\overline{INIT}$ = 0 Propagation Delay	—	60	ns
$T_{RSIR\ Z}$	$\overline{IRQ}$ MIGH-z after RST	—	50	ns
T_{ID}	$\overline{ACK}$ to IRQ Propagation Delay	—	45	ns
T_{IZ}	IRQ Disable Time	—	50	ns
T_{IE}	IRQ Enable Time	—	50	ns
T_{RSIZ}	IRQ High-z after RST	—	50	ns
T_{DCKD}	CLK to OCLK Propagation Delay	—	10	ns

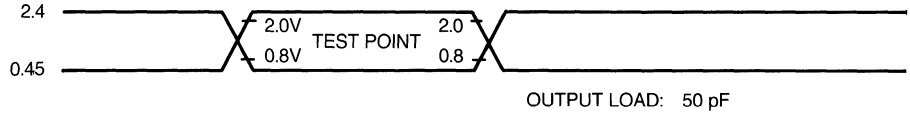


FIGURE 2—A.C. TESTING INPUT WAVEFORM

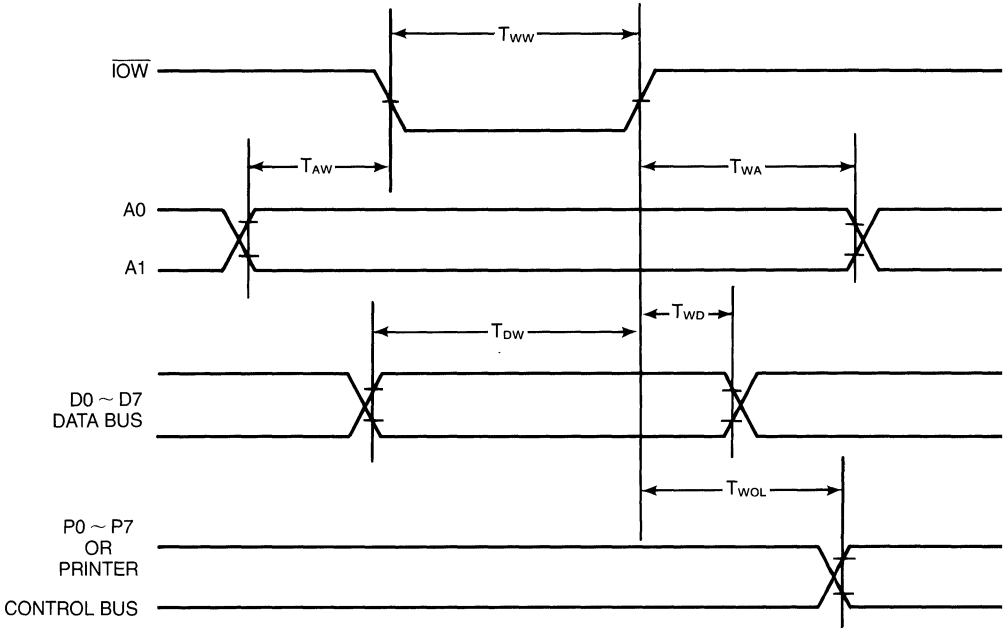


FIGURE 3—WRITE CYCLE WAVEFORM

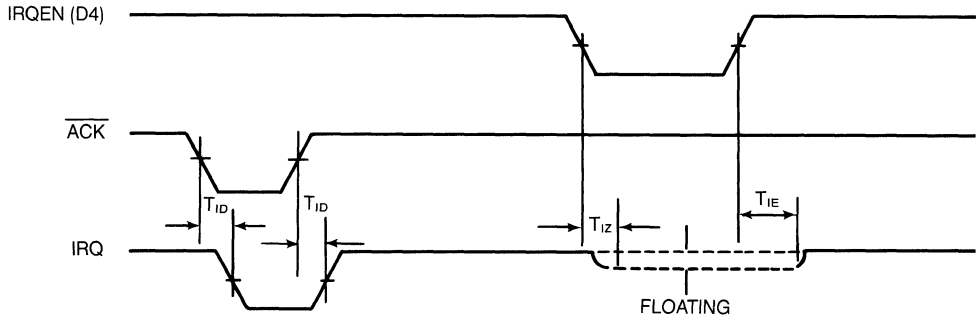


FIGURE 4—INTERRUPT REQUEST WAVEFORM

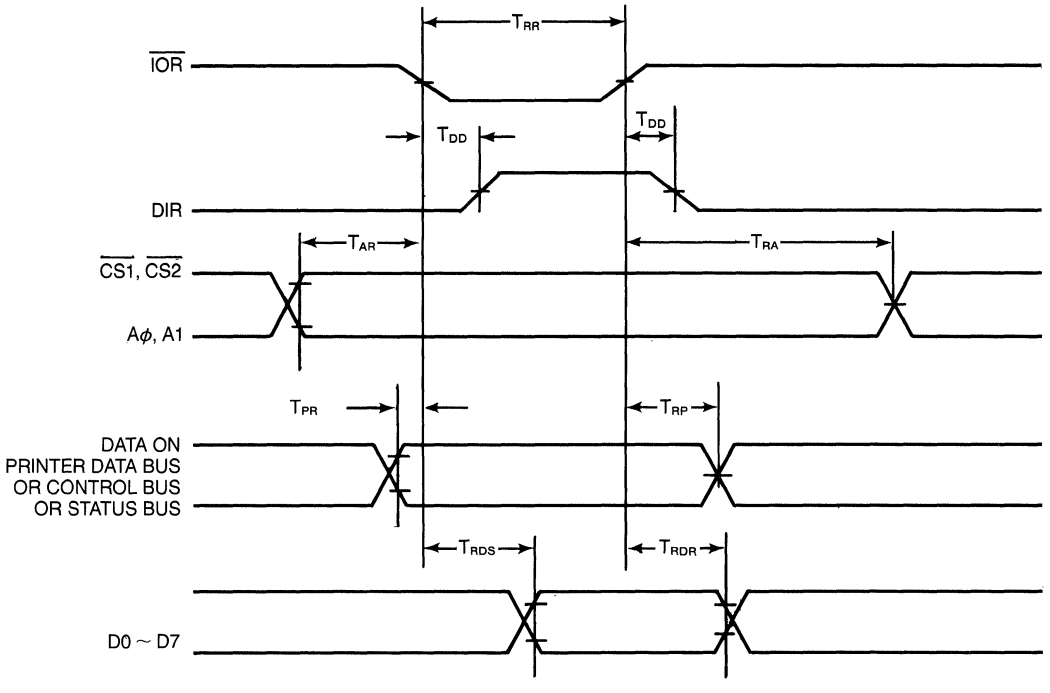


FIGURE 5—READ CYCLE WAVEFORM

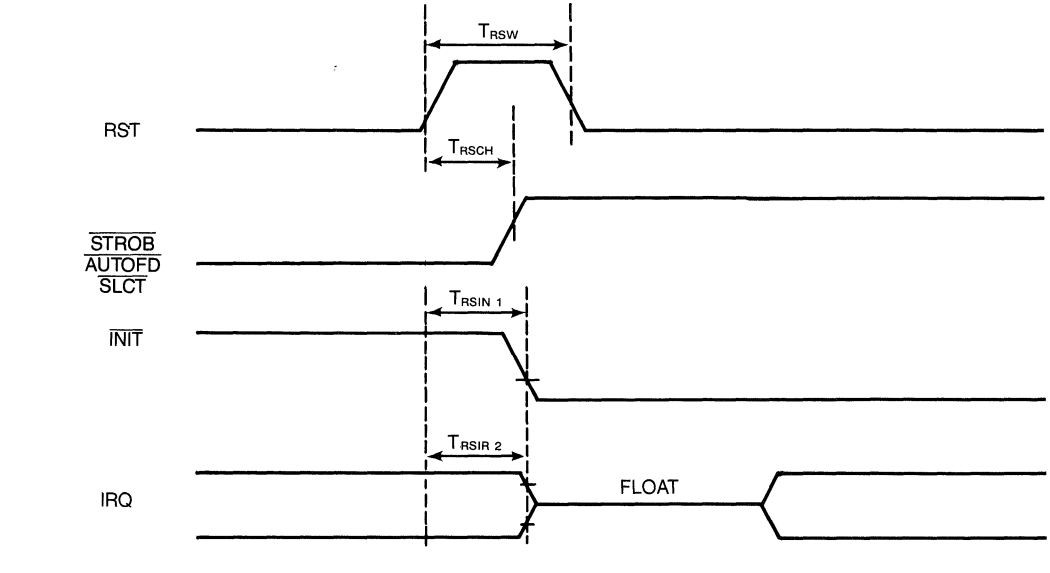


FIGURE 6—RESET WAVEFORM

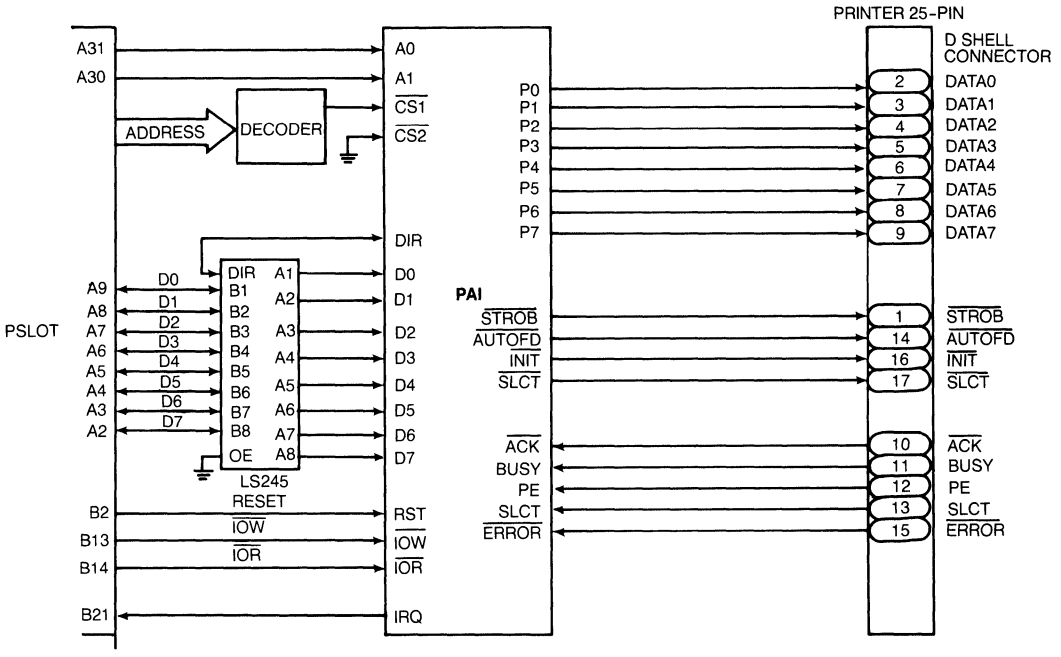


FIGURE 7—PAI ON PRINTER CARD

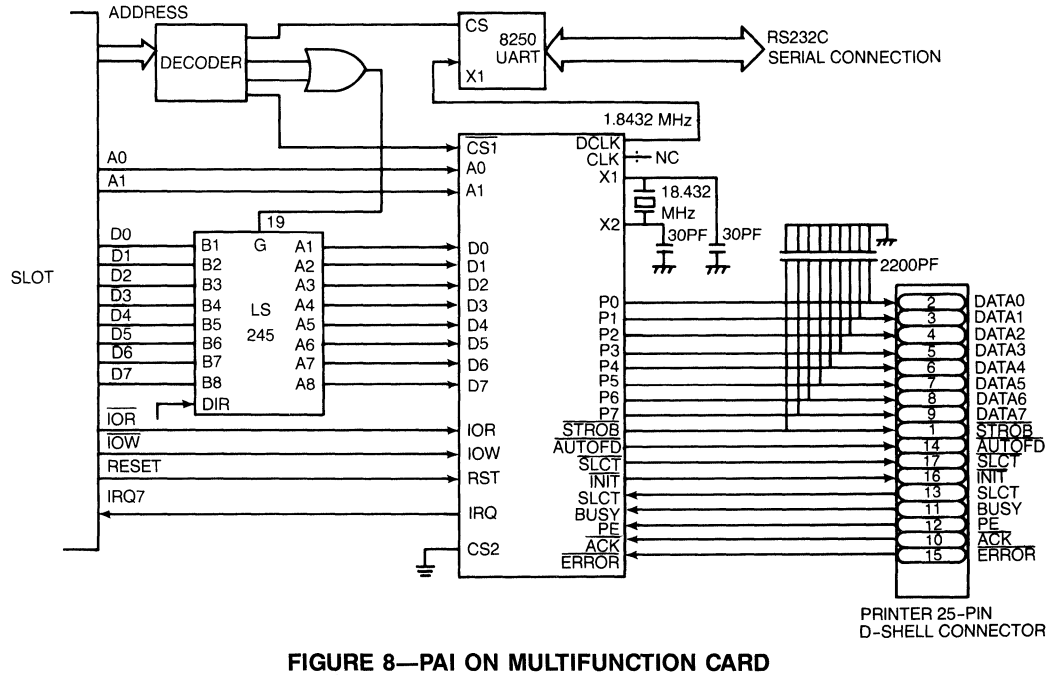
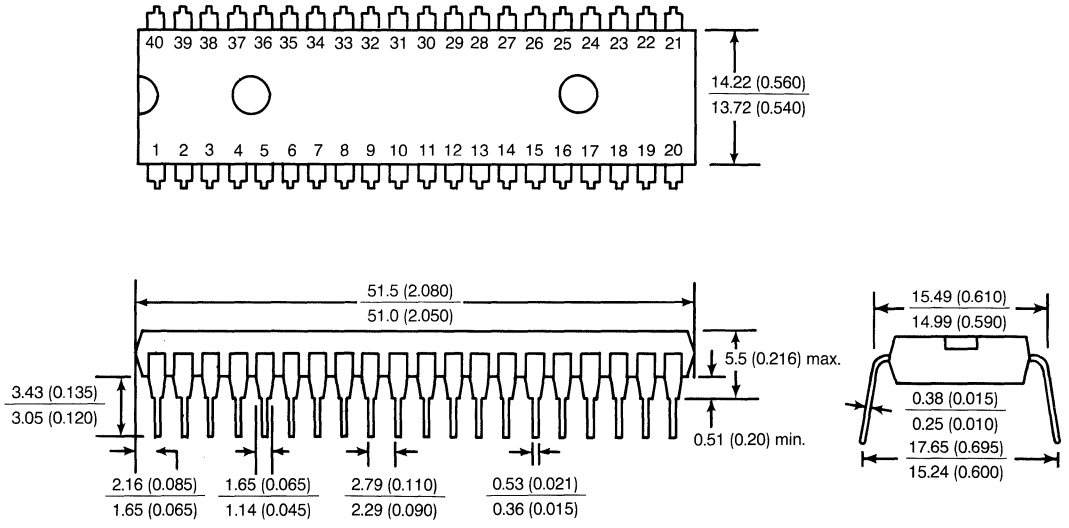


FIGURE 8—PAI ON MULTIFUNCTION CARD

PACKAGE INFORMATION - MILLIMETER (INCH)
40 LEAD PLASTIC DIP



STANDARD MICROSYSTEMS CORPORATION

COM 8251A
μPC FAMILY

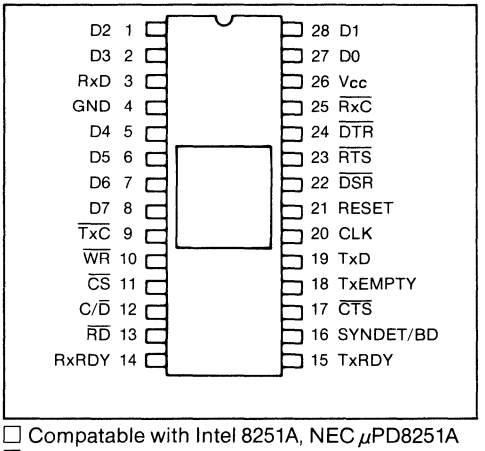
SECTION III

Universal Synchronous/Asynchronous Receiver/Transmitter USART

FEATURES

- ☐ Asynchronous or Synchronous Operation
  - —Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate—1, 16 or 64 X Baud Rate
    - Break Character Generation
    - 1, 1½ or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
  - —Synchronous
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
    - Programmable Sync Character(s)
- ☐ Baud Rate—Synchronous—DC to 64K Baud
  —Asynchronous—DC to 19.2K Baud
- ☐ Baud Rates available from SMC's COM 8116, COM 8126, COM 8136, COM 8146, and COM 8046
- ☐ Full Duplex, Double Buffered Transmitter and Receiver
- ☐ Odd parity, even parity or no parity bit
- ☐ Parity, Overrun and Framing Error Flags
- ☐ Modem Interface Controlled by Processor
- ☐ All Inputs and Outputs are TTL Compatible

PIN CONFIGURATION



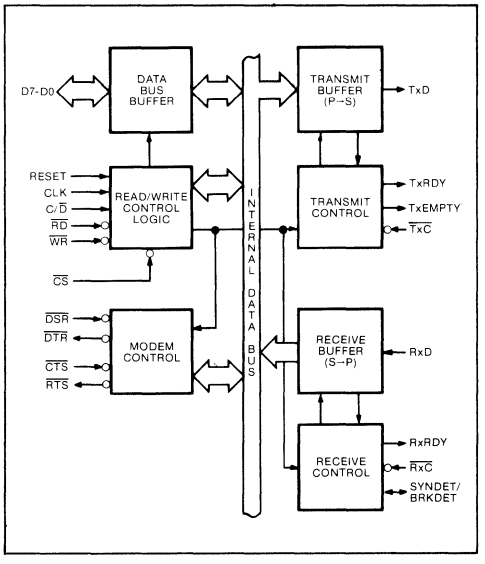
- ☐ Compatable with Intel 8251A, NEC μPD8251A
- ☐ Single +5 Volt Supply
- ☐ Separate Receive and Transmit TTL Clocks
- ☐ Enhanced version of 8251
- ☐ 28 Pin Plastic or Ceramic DIP Package
- ☐ COPLAMOS® N-Channel MOS Technology

GENERAL DESCRIPTION

The COM 8251A is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 8251A is an enhanced version of the 8251.

The COM 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asychronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status, including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 27, 28, 5-8	D2, D3, D0 D1, D4-D7	DATA BUS	I/O	An 8-bit, 3-state bi-directional DATA BUS used to interface the COM 8251A to the processor data bus. Data is transmitted or received by the bus in response to input/output or Read/Write instructions from the processor. The DATA BUS also transfers Control words, Command words, and Status.
3	RxD	RECEIVER DATA	I	This input receives serial data into the USART.
4	GND	GROUND	GND	Ground
9	$\overline{TxC}$	$\overline{TRANSMITTER\ CLOCK}$	I	The $\overline{TRANSMITTER\ CLOCK}$ controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1X, 16X, or 64X the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
10	$\overline{WR}$	$\overline{WRITE\ DATA}$	I	A "zero" on this input instructs the COM 8251A to accept the data or control word which the processor is writing out to the USART via the DATA BUS.
11	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A "zero" on this input enables the USART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.
12	C/$\overline{D}$	CONTROL/$\overline{DATA}$	I	The Control/$\overline{Data}$ input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the DATA BUS. 0 = Data; 1 = Control/Status
13	$\overline{RD}$	$\overline{READ\ DATA}$	I	A "zero" on this input instructs the COM 8251A to place the data or status information onto the DATA BUS for the processor to read.
14	RxRDY	RECEIVER READY	O	The RECEIVER READY output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
15	TxRDY	TRANSMITTER READY	O	TRANSMITTER READY signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information polled operaton. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the processor.
16	SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT	I/O	The SYNDET feature is only used in the Synchronous mode. The USART may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal SYNC mode, the SYNDET output will go to a "one" when the COM 8251A has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second contiguously detected SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input is sampled during the negative half cycle of $\overline{RxC}$ and will cause the COM 8251A to start assembling data character on the next rising edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the COM 8251A is in SYNC. When external SYNC DETECT is programmed, the internal SYNC DETECT is disabled.

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
16 (cont.)				The SYNDET/BRKDET pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the BREAK DETECT output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx Data returns to a logic one state or upon chip RESET. The state of BREAK DETECT can also be read as a status bit.
17	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	I	A "zero" on the $\overline{CLEAR\ TO\ SEND}$ input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one). If either a TxEN off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART written prior to the Tx Disable command before shutting down.
18	TxE	TRANSMITTER EMPTY	O	The TRANSMITTER EMPTY output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around". The TxEN bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a SYNC character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded; an underflow condition. If the USART is operating in the two SYNC character mode, both SYNC characters will be transmitted before the message can resume. TxE does not go low when the SYNC characters are being shifted out. TxE goes low upon the processor writing a character to the USART.
19	TxD	TRANSMITTER DATA	O	This output is the transmitted serial data from the USART. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
20	CLK	CLOCK PULSE	I	The CLK input provides for internal device timing. External inputs and outputs are not referenced to CLK, but the CLK frequency must be greater than 30 times the RECEIVER or TRANSMITTER CLOCKS in the 1X mode and greater than 4.5 times for the 16X and 64X modes.
21	RESET	RESET	I	A "one" on this input forces the USART into the "idle" mode where it will remain until reinitialized with a new set of control words. RESET causes: RxRDY = TxRDY = TxEmpty = SYNDET/BRKDET = 0; TxD = $\overline{DTR}$ = $\overline{RST}$ = 1. Minimum RESET pulse width is 6 t_{CY}, CLK must be running during RESET.
22	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	I	The $\overline{DATA\ SET\ READY}$ input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
23	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	O	The $\overline{REQUEST\ TO\ SEND}$ output is controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
24	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	O	The $\overline{DATA\ TERMINAL\ READY}$ output is controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
25	$\overline{RxC}$	$\overline{RECEIVER\ CLOCK}$	I	The $\overline{RECEIVER\ CLOCK}$ is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1X, 16X or 64X or Synchronous operation at 1X the Baud Rate. Data is sampled into the USART on the rising edge of $\overline{RxC}$.
26	V_{CC}	V_{CC} SUPPLY VOLTAGE	PS	+5 volt supply

DESCRIPTION OF OPERATION—ASYNCHRONOUS

Transmission—

When a data character is written into the USART, it automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at a transmission rate of $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

Receive—

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge (high to low transition) at RxD signals the possible beginning of a START bit and a new character. The receiver is thus prevented from starting in a "BREAK" state. The START bit is verified by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After the STOP bit time, the input character is loaded into the paralled Data Bus Buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

DESCRIPTION OF OPERATION—SYNCHRONOUS

Transmission—

As in Asynchronous transmission, the TxD output remains "high" (marking) until the USART receives the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ at the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Data Protocols require that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the USART Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until the new data characters are available for transmission. If the USART becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Receive—

In Synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, the ENTER HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the contents of the Receive Buffer are compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the (two contiguous) SYNC character(s) programmed have been detected, the USART leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost. Under this condition the Rx register will be cleared to all "ones".

OPERATION AND PROGRAMMING

The microprocessor program controlling the COM 8251A performs these tasks:

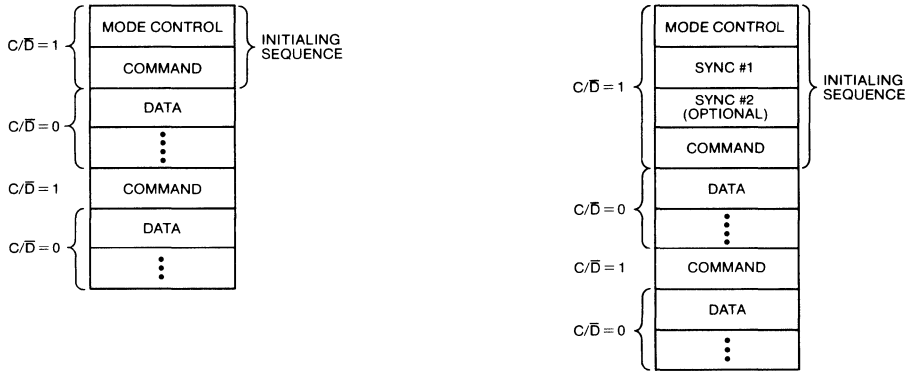
- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which has been received

Control codes determine the mode in which the COM 8251A will operate and are used to set or reset control signals output by the COM 8251A.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE COM 8251A

Figure 1. Control Word Sequences for Initialization



The COM 8251A may be initialized following a system RESET or prior to starting a new seral I/O sequence. The USART must be RESET (external or internal) following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the COM 8251A enters an idle state in which it can neither transmit nor receive data.

The COM 8251A is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the COM 8251A, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a RESET (external or internal), the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following a RESET input or following an internal reset command. A reset operation (internal via IR or external via RESET) will cause the USART to interpret the next "control write", which should immediately follow the reset, as a Mode Instruction.

After receiving the control words the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. Concurrently, the USART is ready to receive serial data.

C/D̄	RD̄	WR̄	CS̄	
0	0	1	0	USART → Data Bus
0	1	0	0	Data Bus → USART
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

MODE CONTROL CODES

The COM 8251A interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse, as programmed. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. In the case of a programmed character length of less than 8 bits, the least significant DATA BUS unused bits are "don't care" when writing data to the USART and will be "zeros" when reading data. Rx data will be right justified onto D0 and the LSB for Tx data is D0.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½ or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16X or 64X baud rate factor. In these two cases, the half stop bit will be equivanlent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the COM 8251A such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the processor to the COM 8251A at any time during the execution of a program in which specific functions are to be initialized within the communication circuit.

Figure 4 shows the format for the Command Word.

Figure 4. COM 8251A Control Command

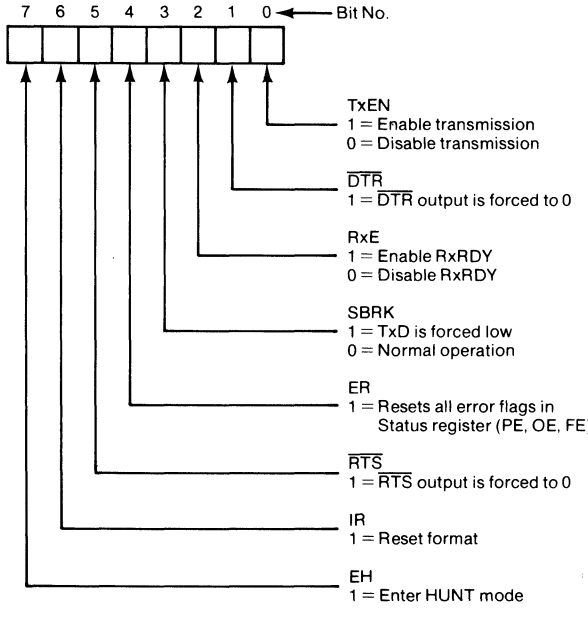


Figure 2. Synchronous Mode Control Code.

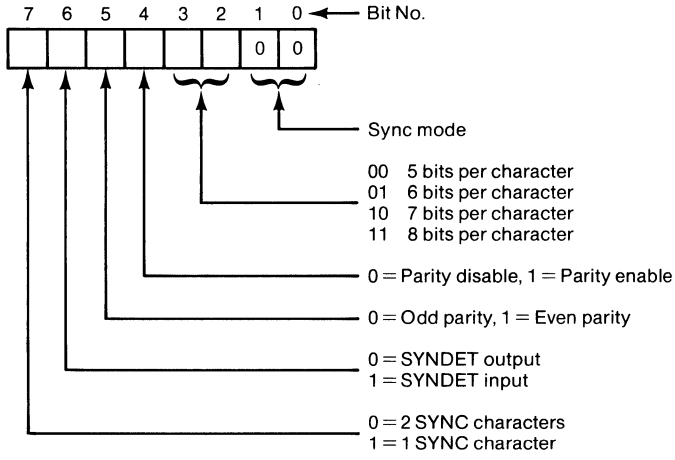
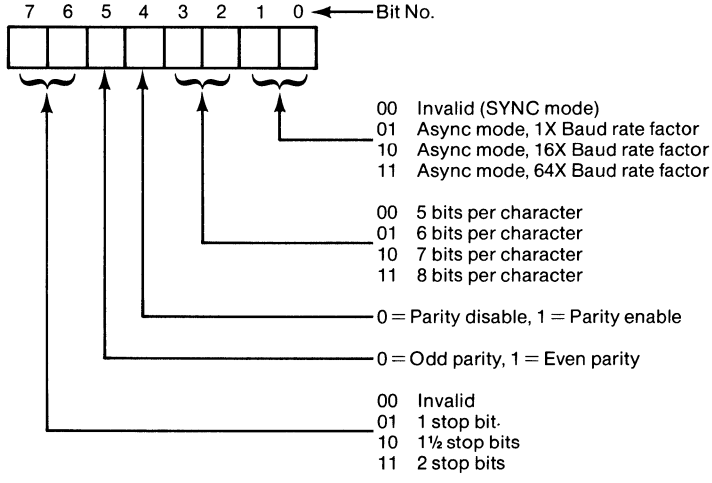


Figure 3. Asynchronous Mode Control Code.



Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission for the COM 8251A cannot take place unless TxEN is set (assuming $\overline{CTS} = 0$) in the command register. The TX Disable command is prevented from halting transmission by the Tx Enable logic until all data previously written has been transmitted. Figure 5 defines the way in which TxEN, TxE and TxRDY combines to control transmitter operations.

Bit 1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the $\overline{DTR}$ command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE, when zero, prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Figure 5.
Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if COM 8251A is in the asynchronous mode. TxD will send SYNC pattern if COM 8251A is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the COM 8251A to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transferred with the ER bit set, all three error flags (PE, OE, FE) in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the COM 8251A. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit ($\overline{RTS}$), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is created independently of other signals in the COM 8251A. As a result, data transfers may be made by the processor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit 6, the Internal Reset (IR), causes the COM 8251A to return to the Idle mode. All functions within the COM 8251A cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a processor program, the COM 8251A must first be reset. Either the RESET input can be activated, or the Internal Reset Command can be sent to the COM 8251A. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the COM 8251A when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input, clear the Rx register to all "ones", and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the COM 8251A, or when SYNC characters are recognized. Parity is not checked in the EH mode.

STATUS REGISTER

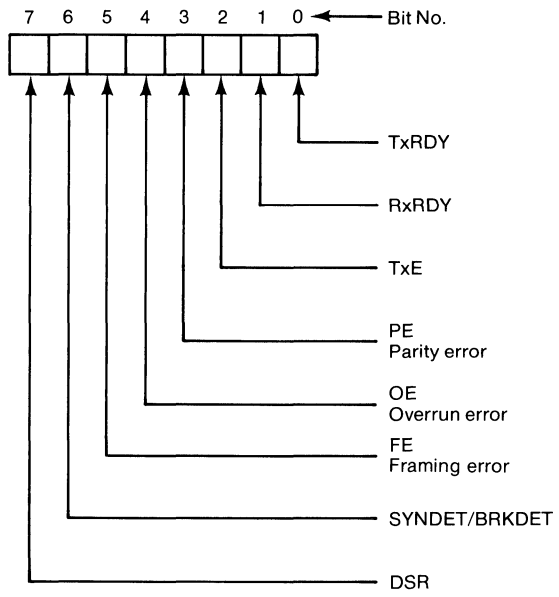
The Status Register maintains information about the current operational status of the COM 8251A. Status can be read at any time, however, the status update will be inhibited during status read. Figure 6 shows the format of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the COM 8251A can accept a new character for transmission. The TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY (status bit) = Tx Character Buffer Empty
TxRDY (pin 15) = Tx Character Buffer Empty • $\overline{CTS}$ • TxEN

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

Figure 6. The COM 8251A Status Register



TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. PE does not inhibit USART operation. PE is reset by the ER bit.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor. OE does not inhibit USART operation. OE is reset by the ER bit.

FE (Async only) is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect bit format ("0" stop bit), as specified by the current mode. FE does not inhibit USART operaton. FE is reset by the ER bit.

SYNDET is the synchronous mode status bit associated with internal or external sync detection.

DSR is the status bit set by the external $\overline{\text{Data Set Ready}}$ signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset by the error reset command or the internal reset command or the RESET input. OE, FE, or PE being set does not inhibit USART operation.

Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both Polled and Interrupt driven environments. Status update can have a maximum delay of 16 t_{CY} periods.

Note:

1. While operating the receiver it is important to realize that the RxE bit of the Command Instruction only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. As the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. This read should be done immediately following the setting of the RxE bit in the asynchronous mode, and following the setting of EH in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.
2. ER should be performed whenever RxE of EH are programmed. ER resets all error flags, even if RxE = 0.
3. The USART may provide faulty RxRDY for the first read after power-on or for the first read after the receiver is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. This is not the case for the first read after hardware or software reset after the device opration has been established.
4. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through an internal flip-flop which clears itself, assuming the External Sync Detect assertion has removed, upon a status read. As long as External Sync Detect is asserted, External Sync Detect Status will remain high.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that as clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
D.C. Characteristics					
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ TO 0.45V
I_{IL}	Input Leakage		±10	μA	$V_{IN} = V_{CC}$ TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High
Capacitance					$T_A = 25°C$, $V_{CC} = GND$
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND
A.C. Characteristics					
Bus Parameters (Note 1)					
Read Cycle:					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	Note 3, $C_L = 150$ pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	
Write Cycle:					
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4
Other Timings:					
t_{CY}	Clock Period	.320	1.35	μs	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	$t_{CY}-90$	ns	
$t_{\bar{\phi}}$	Clock Low Pulse Width	90		ns	

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

NOTES: 1. AC timings measured $V_{OH} = 2.0$, $V_{OL} = 0.8$, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/$\overline{Data}$ ($C/\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $R_D\downarrow$.
4. This recovery time is for RESET and Mode Initialization. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1X Baud Rate, f_{TX} or $f_{RX} \leq 1/(30\ t_{CY})$
   For 16X and 64X Baud Rate, f_{TX} or $f_{RX} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during RESET.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

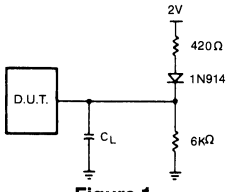
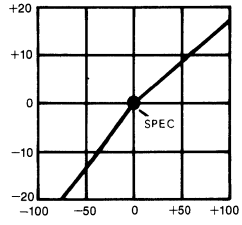


Figure 1.

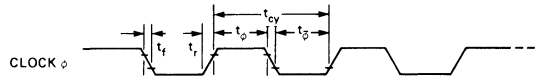
TEST LOAD CIRCUIT

Typical Δ Output Delay Versus Δ Capacitance (pF)

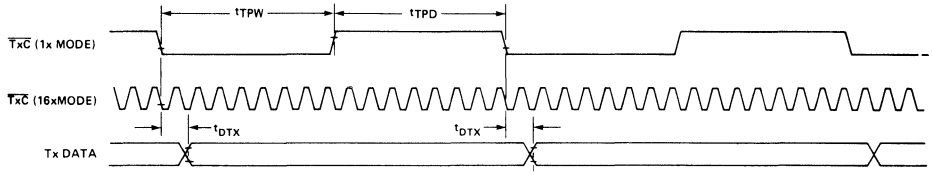


WAVEFORMS

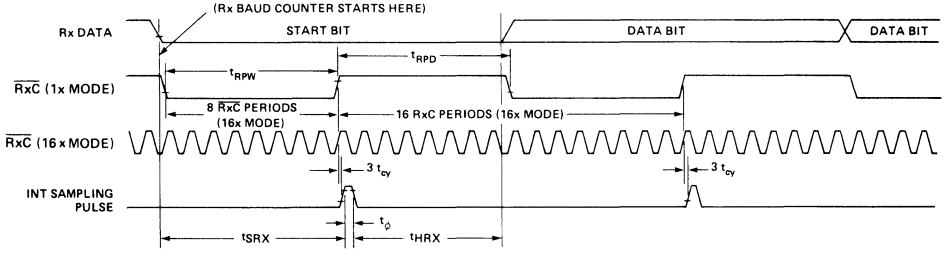
System Clock Input



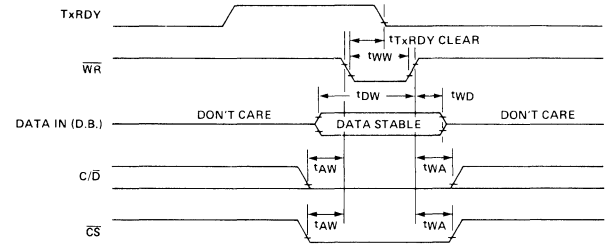
Transmitter Clock & Data



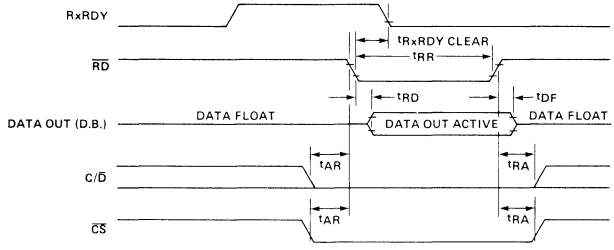
Receiver Clock & Data



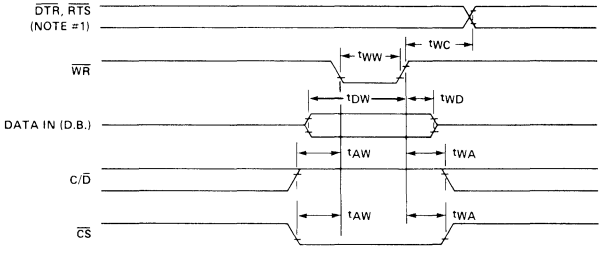
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

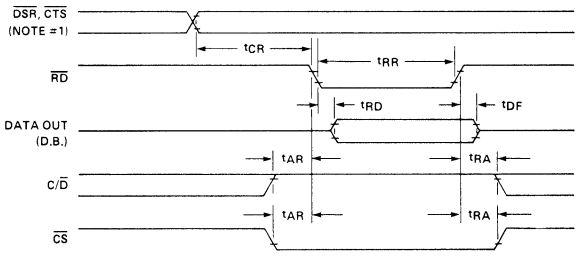


Write Control or Output Port Cycle (CPU → USART)



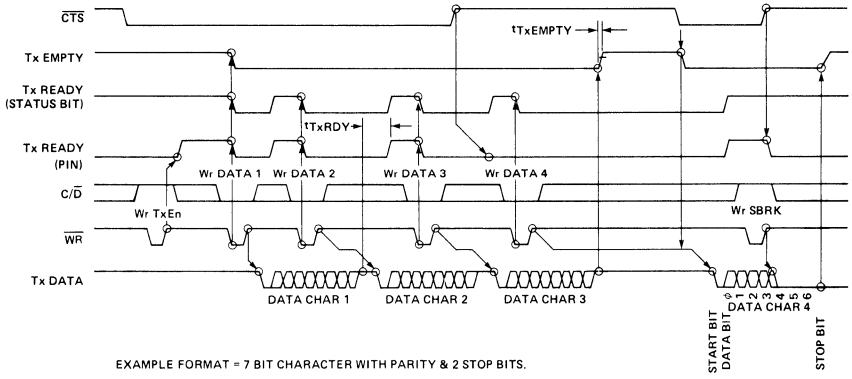
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.

Read Control or Input Port (CPU ← USART)



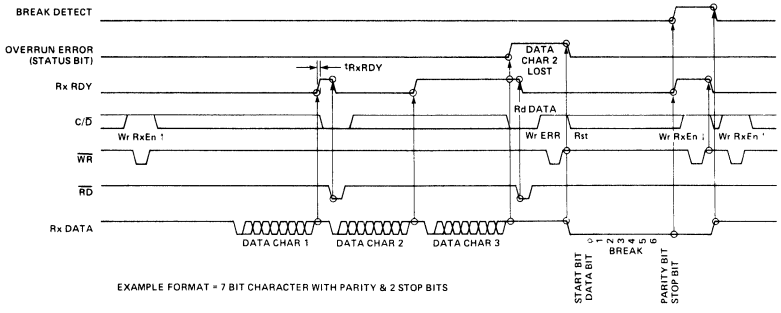
NOTE #1: T_{CR} INCLUDES THE EFFECT OF $\overline{CTS}$ ON THE TxENBL CIRCUITRY.

Transmitter Control & Flag Timing (ASYNC Mode)



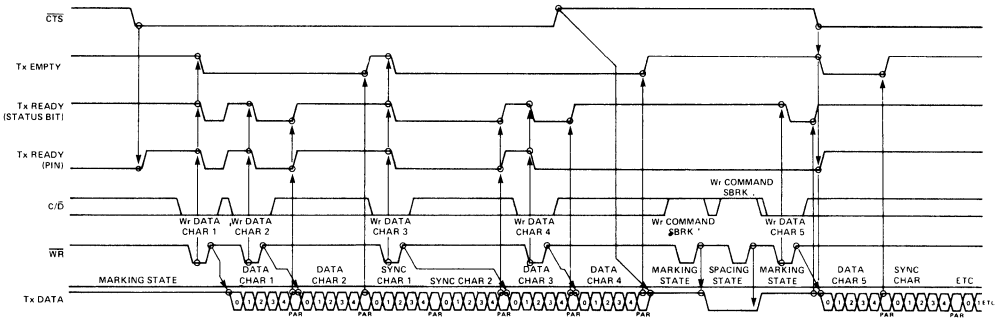
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Receiver Control & Flag Timing (ASYNC Mode)



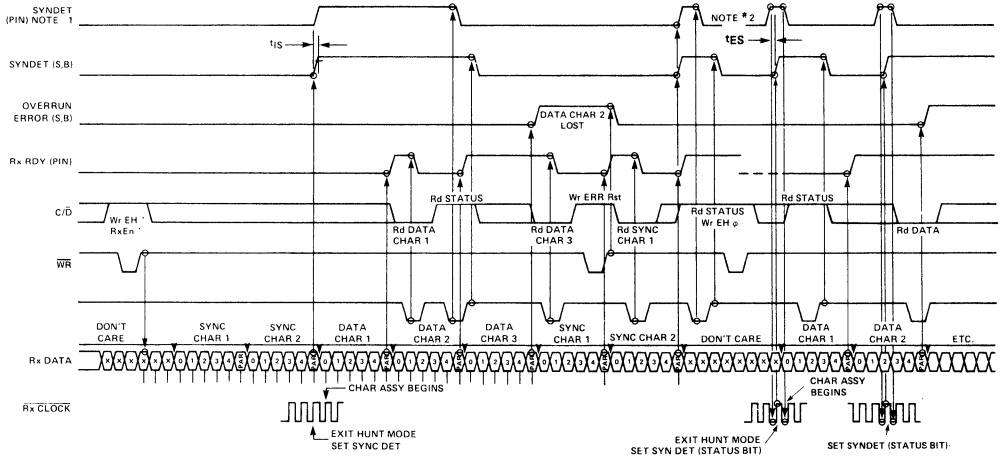
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS

Transmitter Control & Flag Timing (SYNC Mode)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

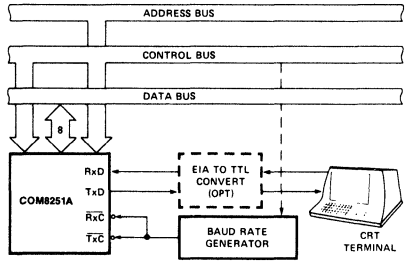
Receiver Control & Flag Timing (SYNC Mode)



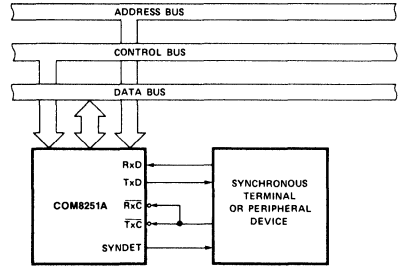
NOTE #1 INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2 EXTERNAL SYNC, 5 BITS, WITH PARITY

APPLICATION OF THE COM8251A

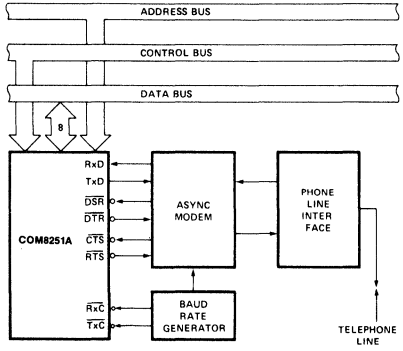
Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



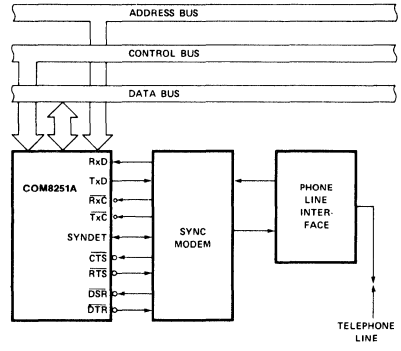
Synchronous Interface to Terminal or Peripheral Device



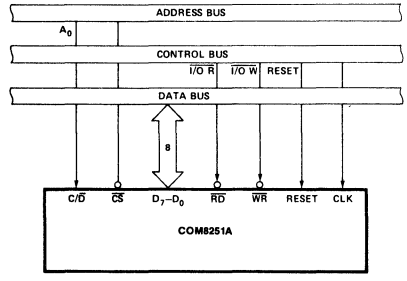
Asynchronous Interface to Telephone Lines



Synchronous Interface to Telephone Lines



COM8251A Interface to μP Standard System Bus



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM82586
PRELIMINARY

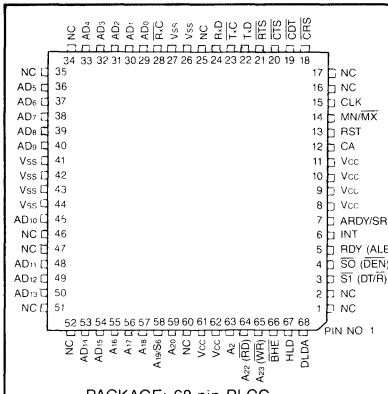
Ethernet™ Local Area Network Coprocessor

SECTION III

FEATURES

- ☐ Performs Complete CSMA/CD Medium Access Control Functions Independently of CPU
  - —High Level Command Interface
- ☐ Supports Established LAN Standards
  - —IEEE 802.3/Ethernet™ (10BASE5)
  - —IEEE 802.3/Cheapernet (10BASE2)
  - —IBM PC Network
  - —IEEE 802.3/StarLAN (1BASE5)
  - —Proprietary CSMA/CD Networks up to 10 Mbps
- ☐ On-Chip Memory Management
  - —Automatic Buffer Chaining
  - —Buffer Reclaim After Receipt of Bad Frames
  - —Save Bad Frames, Optionally
- ☐ Interfaces to 8-bit and 16-bit Microprocessors
- ☐ Supports Minimum Component Systems
  - —Shared Bus Configuration
  - —Interface to IAPX 186 and 188 Microprocessors without Glue
- ☐ Supports High Performance Systems
  - —Bus Master, with On-Chip DMA
  - —5 MBytes/Sec Bus Bandwidth
  - —Compatible with Dual Port Memory
  - —Back to Back Frame Reception at 10 Mbps
- ☐ 48 Pin DIP and 68 Pin PLCC

PIN CONFIGURATION



- ☐ Network Management
  - —CRC Error Tally
  - —Alignment Error Tally
  - —Location of Cable Faults
- ☐ Self-Test Diagnostics
  - —Internal Loopback
  - —External Loopback
  - —Internal Register Dump
  - —Backoff Timer Check
- ☐ Single +5 volt supply
- ☐ Direct replacement for Intel's 82586

GENERAL DESCRIPTION

The COM82586 is an intelligent, high performance Local Area Network coprocessor, implementing the CSMA/CD access method (Carrier Sense Multiple Access with Collision Detection). It performs all time-crystal functions independently of the host processor, which maximizes performance and network efficiency.

The COM82586 performs the full set of IEEE 802.3 CSMA/CD media access control and channel interface functions including: framing, preamble generation and stripping, source address generation, destination address checking, CRC generation and checking, short frame detection. Any data rate up to 10 Mb/s can be used.

The COM82586 features a powerful host system interface. It automatically manages memory structures with command chaining and bidirectional data chaining. An on-chip DMA controller manages 4 channels transparently to the user. Buffers containing errored or collided frames can be automatically recovered. The 82586 can be configured for 8-bit or 16-bit data path, with maximum burst transfer rate of 2 or 4 Mbyte/sec. respectively. Memory address space is 16 Mbyte maximum.

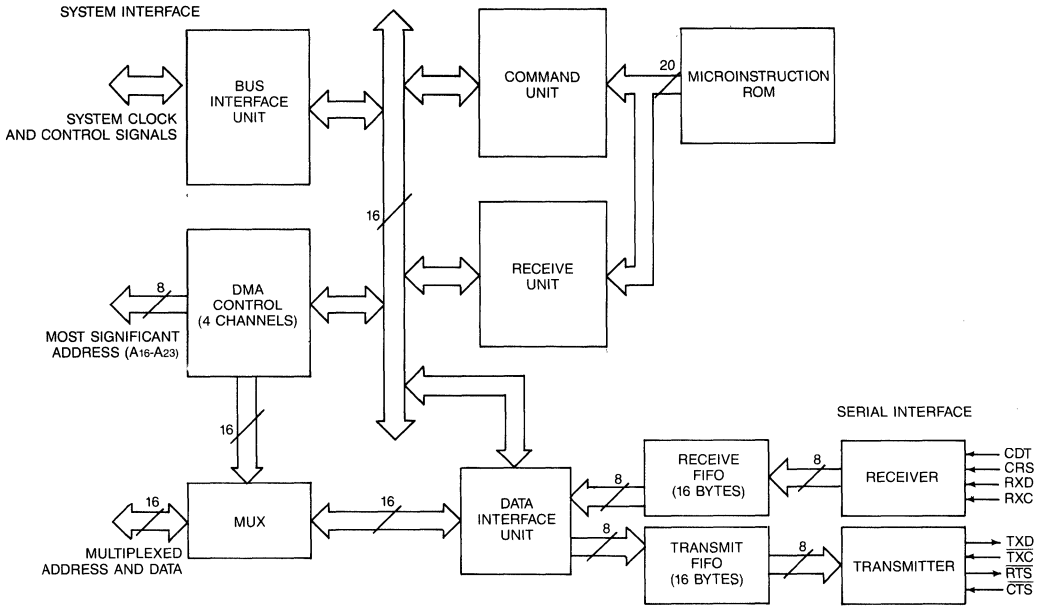
The COM82586 provides two independent 16 byte FIFOs, one for receiving and one for transmitting. The threshold for block transfer to/from memory is programmable, enabling the user to optimize bus overhead for a given worst case bus latency.

The COM82586 provides a rich set of diagnostic and network management functions including: internal and external loopbacks, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address, optional capture of errored or collided frames, and time domain reflectometry for locating faults in the cable.

The COM82586 can be used in either baseband or broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) for any length network operating at any data rate up to 10 Mb/s. The controller supports address field lengths of 1, 2, 3, 4, 5, or 6 bytes. It can be configured for either the IEEE 802.3/Ethernet™ or HDLC method of frame delineation. Both 16-bit and 32-bit CRC are supported.

The COM82586 is available in a 48 pin DIP or 68 pin PLCC package.

Ethernet™ is a trademark of the Xerox Corporation.



FUNCTIONAL BLOCK DIAGRAM

231246-1

DESCRIPTION OF PIN FUNCTIONS

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
48, 36	8, 9, 10, 11, 61, 62	Power Supply	V_{CC}, V_{CC}	+5V Power Supply.
12, 24	26, 27, 41, 42, 43, 44	Ground	V_{SS}, V_{SS}	System Ground.
34	13	Reset	RST	RST is an active HIGH internally synchronized signal, causing the 82586 to terminate present activity immediately. The signal must be HIGH for at least four clock cycles. The 82586 will execute RST within ten system clock cycles starting from RST HIGH. When RST returns LOW, the 82586 waits for the first CA to begin the initialization sequence.
27	22	Transmitted Serial Data	TxD	Output signal. This signal is HIGH when not transmitting.
26	23	Transmit Data Clock	$\overline{TxC}$	This signal provides timing information to the internal serial logic, depending upon the mode of data transfer. For NRZ mode of operation, data is transferred to the TxD pin on the HIGH to LOW clock transition.
25	24	Received Data	RxD	Received Data Input Signal.
23	28	Received Data Clock	$\overline{RxC}$	This signal provides timing information to the internal shifting logic depending upon the mode of data transfer. For NRZ data, the state of the RxD pin is sampled on the HIGH to LOW clock transition.
28	21	Request To Send	$\overline{RTS}$	When LOW, this signal notifies an external interface that the 82586 has data to transmit. It is forced HIGH after a Reset and while the Transmit Serial Unit is not sending data.
29	20	Clear To Send	$\overline{CTS}$	Active LOW Clear To Send input enables the 82586 transmitter to actually send data. It is normally used as an interface handshake to $\overline{RTS}$. This signal going inactive stops transmission. It is internally synchronized. If $\overline{CTS}$ goes inactive, meeting the setup time to $\overline{TxC}$ negative edge, transmission is stopped and $\overline{RTS}$ goes inactive within, at most, two TxC cycles.

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
31	18	Carrier Sense	$\overline{CRS}$	Active LOW Carrier Sense input used to notify the 82586 that there is traffic on the serial link. It is used only if the 82586 is configured for external Carrier Sense. When so configured, external circuitry is required for detecting serial link traffic. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles.
30	19	Collision Detect	$\overline{CDT}$	Active LOW Collision Detect input is used to notify the 82586 that a collision has occurred. It is used only if the 82586 is configured for external Collision Detect. External circuitry is required for detecting the collision. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles. During transmission, the 82586 is able to recognize a collision one bit time after preamble transmission has begun.
38	6	Interrupt	INT	Active HIGH interrupt request signal.
32	15	Clock	CLK	The system clock input from the 80186 or another symmetric clock generator.
33	14	Minimum Mode/ Maximum Mode	MN/$\overline{MX}$	When HIGH, MN/$\overline{MX}$ selects $\overline{RD}$, $\overline{WR}$, ALE $\overline{DEN}$, DT/$\overline{R}$ (Minimum Mode). When LOW, MN/$\overline{MX}$ selects A22, A23, READY, $\overline{S0}$, $\overline{S1}$ (Maximum Mode). Note: This pin should be static during 82586 operation.
6-11, 13-22	29-33, 36-40, 45, 48, 49, 50, 53, 54	Address and Data Bus	AD0-AD15	These lines from the time multiplexed memory address (t1) and data (t2, t3, tW, 14) bus. When operating with an 8-bit bus, the high byte will output the address during the entire cycle. AD0-AD15 are floated after a RESET or when the bus is not acquired.
1, 3-5 45-47	55-57, 59, 63-65	Address Bus	A16-A18 A20-A23	These lines constitute 7 out of 8 most significant address bits for memory operation. They switch during t1 and stay valid during the entire memory cycle. The lines are floated after RST or when the bus is not acquired. Address lines A22 and A23 are not available for use in minimum mode.
2	58	Address 19 or Status 6	A19/S6	During t1 this signal it forms line 19 of the memory address. During t2 through t4 it is used as a status indicating that this is a Master peripheral cycle, and is HIGH. Its timing is identical to that of AD0-AD15 during write operation.
43	67	Hold	HLD	HLD is an active HIGH signal used by the 82586 to request local bus mastership at the end of the current CPU bus transfer cycle, or at the end of the current DMA burst transfer cycle. In normal operation, HLD goes inactive before HLDA. The 82586 can be forced off the bus by HLDA going inactive. In this case, HLD goes inactive within four clock cycles in word mode and eight clock cycles in byte mode.
42	68	Hold Acknowledge	HLDA	HLDA is an active HIGH Hold Acknowledge signal indicating that the CPU has received the HLD request and that bus control has been relinquished to the 82586. It is internally synchronized. After HLD is detected as LOW, the processor drives HLDA LOW. Note, CONNECTING V_{CC} TO HLDA IS NOT ALLOWED because it will cause a deadlock. Users wanting to give permanent bus access to the 82586 should connect HLDA with HLD.
35	12	Channel Attention	CA	The CA pin is a Channel Attention input used by the CPU to initiate the 82586 execution of memory resident Command Blocks. The CA signal is synchronized internally. The signal must be HIGH for at least one system clock period. It is latched internally on HIGH to LOW edge and then detected by the 82586.
44	66	Bus High Enable	$\overline{BHE}$	The Bus High Enable signal ($\overline{BHE}$) is used to enable data onto the most significant half of the data bus. Its timing is identical to that of A16-A23. With a 16-bit bus it is LOW and with an 8-bit bus it is HIGH. Note: after RST, the 82586 is configured to 8-bit bus.

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
39	5	Ready	RDY	This active HIGH signal is the acknowledgement from the addressed memory that the transfer cycle can be completed. While LOW, it causes wait states to be inserted. This signal must be externally synchronized with the system clock. The Ready signal internal to the 82586 is a logical OR between RDY and SRDY/ARDY.
37	7	Synch/Asynch Ready	ARDY/ SRDY	This active HIGH signal performs the same function as RDY. If it is programmed at configure time to SRDY, it is identical to RDY. If it is programmed to ARDY, the positive edge of the Ready signal is internally synchronized. Note, the negative edge must still meet setup and hold time specifications, when in ARDY mode. The ARDY signal must be active for at least one system clock HIGH period for proper strobing. The Ready signal internal to the 82586 is a logical OR between RDY (in Maximum Mode only) and SRDY/ARDY. Note that following RST, this pin assumes ARDY mode.
40, 41	4, 3	Status 0, 1	$\overline{S0}$, $\overline{S1}$	Maximum mode only. These status pins define the type of DMA transfer during the current memory cycle. They are encoded as follows: $\overline{S1}$ $\overline{S0}$ 0 0 Not Used 0 1 Read Memory 1 0 Write Memory 1 1 Passive Status is active from the middle of t4 to the end of t2. They return to the passive state during t3 or during tW when RDY or ARDY is HIGH. These signals can be used by the 8288 Bus Controller to generate all memory control and timing signals. Any change from the passive state signals the 8288 to start the next t1 to t4 bus cycle. These pins are pulled HIGH and floated after a system RST and when the bus is not acquired.
46	64	Read	$\overline{RD}$	Used in minimum mode only. The read strobe indicates that the 82586 is performing a memory read cycle. $\overline{RD}$ is active LOW during t2, t3 and tW of any read cycle. This signal is pulled HIGH and floated after a RST and when the bus is not acquired.
45	65	Write	$\overline{WR}$	Used in minimum mode only. The write strobe indicates that the 82586 is performing a write memory cycle. $\overline{WR}$ is active LOW during t2, t3 and tW of any write cycle. It is pulled HIGH and floats after RST and when the bus is not acquired.
39	5	Address Latch Enable	ALE	Used in minimum mode only. Address Latch Enable is provided by the 82586 to latch the address into the 8282/8283 address latch. It is a HIGH pulse, during t1 ('clock low') of any bus cycle. Not that ALE is never floated.
40	4	Data Enable	$\overline{DEN}$	Used in minimum mode only. Data ENable is provided as output enable for the 8286/8287 transceivers in a stand-alone (no 8288) system. $\overline{DEN}$ is active LOW during each memory access. For a read cycle, it is active from the middle of t2 until the beginning of t4. For a write cycle, it is active from the beginning of t2 until the middle of t4. It is pulled HIGH and floats after a system RST or when the bus is not acquired.
41	3	Data I/O Control	DT/$\overline{R}$	Used in minimum mode only. DT/$\overline{R}$ is used in non-8288 systems using an 8286/8287 data bus transceiver. It controls the direction of data flow through the Transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$. It becomes valid in the t4 preceding a bus cycle and remains valid until the final t4 of the cycle. This signal is pulled HIGH and floated after a RST or when the bus is not acquired.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION

COM82C501
PRELIMINARY

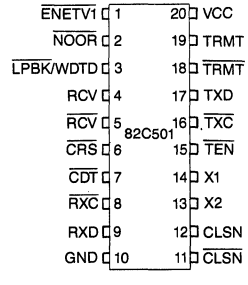
SECTION III

Ethernet™ Serial Interface

FEATURES

- ☐ Direct Replacement for Intel 82501 and 82C501, or SEEQ 8023A
- ☐ Compatible with IEEE 802.3 10BASE5 (Ethernet™) and 10BASE2 (Cheapernet) Specifications
- ☐ 10 Mbps Operation
- ☐ Replaces 8 to 12 MSI Components
- ☐ Manchester Encoding/Decoding and Receive Clock Recovery
- ☐ 10 MHz Transmit Clock Generator
- ☐ Drives/Receives IEEE 802.3 Transceiver Cable (AUI)
- ☐ Defeatable Watchdog Timer Circuit to Prevent Continuous Transmissions
- ☐ Diagnostic Loopback for Network Node Fault Detection and Isolation
- ☐ Direct Interface to the COM82586 LAN Coprocessor and COM82C502 Transceiver
- ☐ Low Power CMOS
- ☐ +5 Volt Only Operation

PIN CONFIGURATION

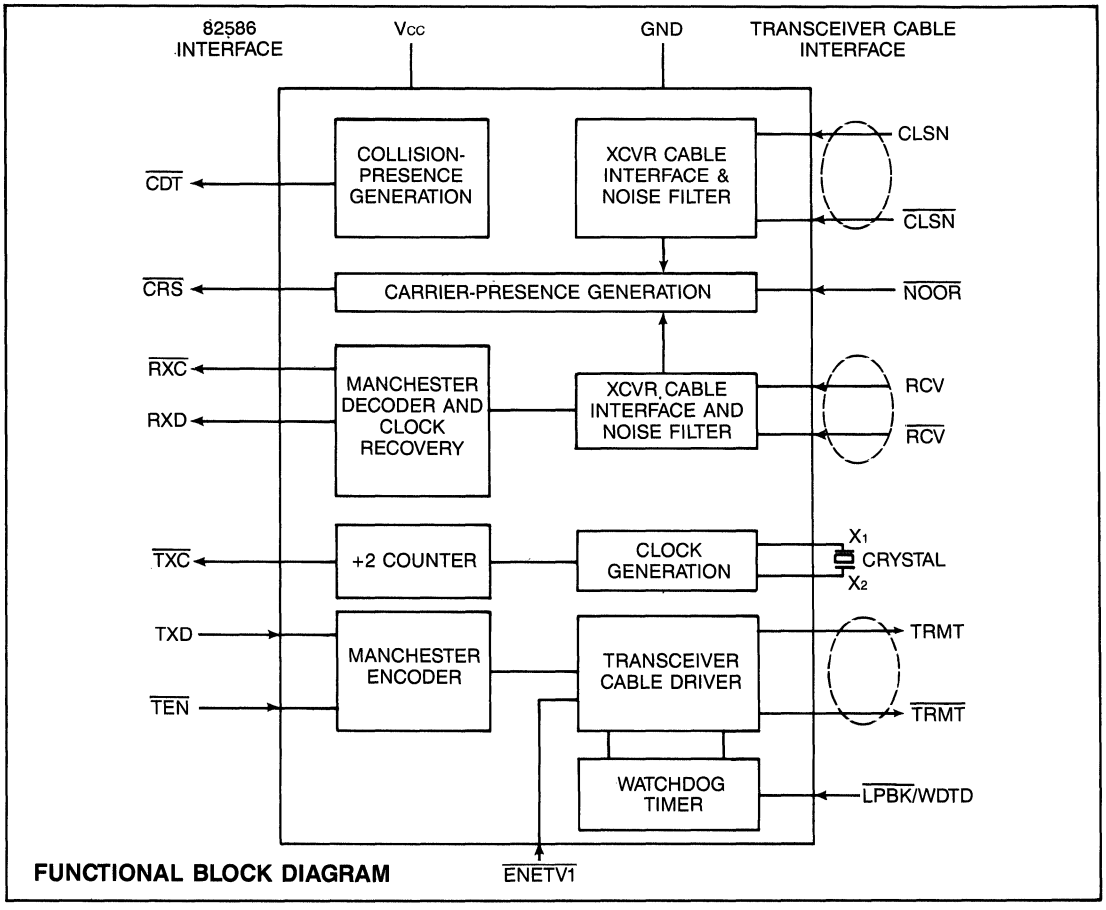


Package: 20-pin DIP

GENERAL DESCRIPTION

The COM82C501 Ethernet™ Serial Interface (ESI) chip is designed to work directly with the COM82586 LAN Coprocessor in IEEE 802.3 (10BASE5 and 10BASE2), 10 Mbps, Local Area Network applications. The major functions of the COM82C501 are to generate the 10 MHz transmit clock for the COM82586, perform Manchester encoding/decoding of the transmitted/received frames, and provide the electrical interface to the Ethernet™ transceiver cable (AUI). Diagnostic loopback control enables the COM82C501 to route the signal to be transmitted from the COM82586 through its Manchester encoding and decoding circuitry and back to the COM82586. The combined loopback capabilities of the COM82586 and COM82C501 result in efficient fault detection and isolation by providing sequential testing of the communications interface. An on-chip watchdog timer circuit (defeatable) prevents the station from locking up in a continuous transmit mode. The COM82C501 is socket compatible with the bipolar Intel 82501, the Seeq 8023A, and the CMOS Intel 82C501.

Ethernet™ is a trademark of the Xerox Corporation.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Ethernet Version 1.0	$\overline{\text{ENETV1}}$	An active low, MOS-level input. When $\overline{\text{ENETV1}}$ is asserted, the TRMT/$\overline{\text{TRMT}}$ pair remains at high differential voltage at the end of transmission. This operation is compatible with the Ethernet Version 1.0 specification. If the $\overline{\text{ENETV1}}$ pin is left floating, an internal pull-up resistor biases the input inactive high.
2	Carrier Sense Option	$\overline{\text{NOOR}}$	An active low, MOS-level input. When $\overline{\text{NOOR}}$ is asserted a valid signal on the collision-presence pair (CLSN/$\overline{\text{CLSN}}$) will not force $\overline{\text{CRS}}$ active low. With $\overline{\text{NOOR}}$ active $\overline{\text{CRS}}$ can only be asserted by the presence of valid data bits on the RCV/$\overline{\text{RCV}}$ pair. If the $\overline{\text{NOOR}}$ pin is floating, an internal pull-up resistor biases the input inactive high.
3	Loopback/Watchdog Timer Disable	$\overline{\text{LPBK}}$/ WDTD	An active low, TTL-level control signal enables the loopback mode. In loopback mode serial data on the TXD input is routed through the 82C501 internal circuits and back to the RXD output without driving the TRMT/$\overline{\text{TRMT}}$ output pair to the transceiver cable. During loopback $\overline{\text{CDT}}$ is asserted at the end of each transmission to simulate the SQE test. An input voltage of 12V ± 10% through a 4 KΩ resistor will disable the on-chip watchdog timer.
4 5	Receiver Pair	RCV $\overline{\text{RCV}}$	A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV will be negative-going to indicate the beginning of a frame. The last transition should be positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.

PIN NO.	NAME	SYMBOL	FUNCTION
6	Carrier Sense	$\overline{CRS}$	An active low, MOS-level output to notify the COM82586 that there is activity on the coaxial cable. The signal is asserted when valid data or a collision-presence signal from the transceiver is present. It is deasserted at the end of a frame; or when the end of the collision-presence signal is detected, synchronous with $\overline{RXC}$. After transmission, once deasserted, CRS will not be reasserted again for a period of 5 μs minimum or 7 μs maximum, regardless of any activity on the collision-presence signal (CLSN/$\overline{CLSN}$) and RCV/$\overline{RCV}$ inputs.
7	Collision Detect	$\overline{CDT}$	An active-low, MOS-level signal which drives the $\overline{CDT}$ input of the COM82586 controller. It is asserted as long as there is activity on the collision pair (CLSN/$\overline{CLSN}$), and during SQE (heartbeat) test in loopback.
8	Receive Clock	$\overline{RXC}$	A 10 MHz MOS level clock output with 5 ns rise and fall times. This output is connected to the COM82586 receive clock input $\overline{RXC}$. There is a maximum 1.2 μs delay at the beginning of a frame reception before the clock recovery circuit gains lock. During idle (no incoming frames) $\overline{RXC}$ is forced low.
9	Receive Data	RXD	A MOS-level output tied directly to the RXD input of the COM82586 controller and sampled by the COM82586 at the negative edge of $\overline{RXC}$. The bit stream received from the transceiver cable is Manchester decoded prior to being transferred to the controller. This output remains high during idle.
10	Ground	GND	Reference.
12 11	Collision Pair	$\overline{CLSN}$ $\overline{CLSN}$	A differentially driven input pair tied to the collision-presence pair of the Ethernet transceiver cable. The collision-presence signal is a 10 MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going to indicate the end of the signal.
14 13	Clock Crystal	X_1 X_2	20 MHz crystal inputs. When X_2 is floated, X_1 can be used as an external MOS level input clock.
15	Transmit Enable	$\overline{TEN}$	An active low, TTL level signal synchronous to TXC that enables data transmission to the transceiver cable and starts the watchdog timer. $\overline{TEN}$ can be driven by the $\overline{RTS}$ from the COM82586.
16	Transmit Clock	$\overline{TXC}$	A 10 MHz MOS level clock output with 5 ns rise and fall times. This clock is connected directly to the $\overline{TXC}$ input of the COM82586.
17	Transmit Data	TXD	A TTL-level input signal that is directly connected to the serial data output, TXD, of the COM82586.
19 18	Transmit Pair	TRMT $\overline{TRMT}$	A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transmission, which is always positive at TRMT, the differential voltage is slowly reduced to zero volts in a series of steps. If $\overline{ENETV1}$ is asserted this voltage stepping is disabled.
20	Power Supply	V_{CC}	+5V $\pm$ 10%.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM82C502
PRELIMINARY

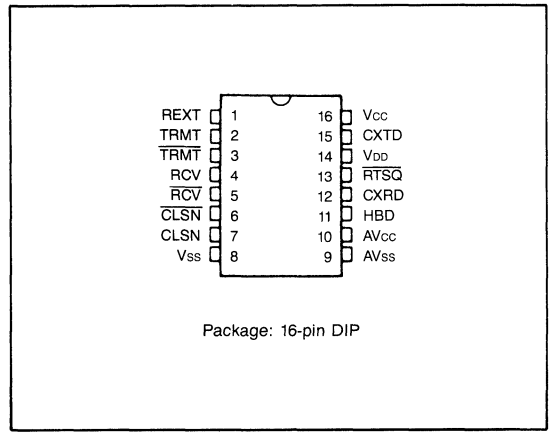
SECTION III

Ethernet™ Transceiver Chip

FEATURES

- ☐ Conforms to the Following Standards:
  - —IEEE 802.3, 10BASE5 (Ethernet™)
  - —IEEE 802.3, 10BASE2 (Cheapernet)
  - —Ethernet™ Version 2.0
- ☐ Jabber Function
- ☐ Receive Based Collision Detection
- ☐ Defeatable Signal Quality Error (Heartbeat) Test
- ☐ Requires Minimum Board Space
  - —On-Chip Voltage Reference
  - —16 Pin DIP
- ☐ No External Adjustments Required
- ☐ Low Power CMOS
- ☐ Direct Replacement for Intel's 82502

PIN CONFIGURATION



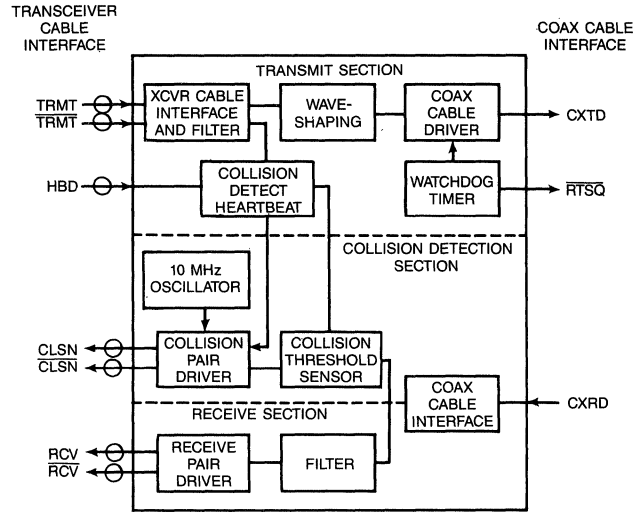
Package: 16-pin DIP

GENERAL DESCRIPTION

The COM82C502 Ethernet™ Transceiver Chip is a CMOS LSI device that provides the complete set of transmit, receive and collision detection functions specified by the IEEE 802.3, 10 BASE5 (Ethernet™) and 10BASE2 (Cheapernet) 10 Mbps baseband standards for the Media Attachment Unit (MAU). The COM82C502 teams up the COM82586 CSMA/CD LAN Coprocessor and the COM82C501 Ethernet™ Serial Interface enabling the designer to implement highly integrated IEEE 802.3 systems.

Three basic functional blocks make up the COM82C502: transmit, receive and collision detection. The transmit and receive sections transfer data from the transceiver drop (Access Unit Interface or AUI) cable to the coaxial cable of the network and vice-versa. The collision detection section senses simultaneous transmissions by two or more network stations (collisions) on the coaxial cable and reacts by sending a 10 MHz signal across the transceiver drop cable to the station that it front ends.

When used in an Ethernet™ application, the COM82C502 can drive a transceiver cable up to 50 meters in length (for Cheapernet, there is no transceiver cable). The COM82C502 provides all active communications circuitry for the transceiver function in the Ethernet™ Cheapernet environment. It is an ideal companion to the COM82C501.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
2 3	Transmit Data Pair	TRMT, $\overline{\text{TRMT}}$	A differentially driven input tied to the transmit pair of the transceiver cable. The transmit pair of the transceiver cable is driven with 10 Mbps Manchester encoded data from the serial interface of the data link (82501). TRMT/$\overline{\text{TRMT}}$ must be isolated from the transceiver cable by a pulse transformer. The last transition is expected to be positive indicating end of packet.
4 5	Receive Data Pair	RCV, $\overline{\text{RCV}}$	An output driver pair that generates an ECL AC signal level to drive the transceiver cable receive pair with the 10 Mbps Manchester encoded data received from the coaxial cable of the network. RCV/$\overline{\text{RCV}}$ must be isolated from the transceiver cable by a pulse transformer. The last transition is always positive indicating the end of the packet. The current from the RCV pin is incrementally decreased after the last transition.
7 6	Collision Presence Pair	CLSN, $\overline{\text{CLSN}}$	An output driver pair that generates a 10 MHz ECL AC signal level square wave on the collision presence pair of the transceiver cable when: a collision is detected on the coaxial cable of the network, during self-test as the collision circuit heartbeat indication, or after the watchdog timer has expired to indicate that the coaxial cable transmitter is disabled.
15	Coaxial Cable Transmit Data	CXTD	An output pin that transmits data onto the coaxial cable of the network by sinking current from the center conductor of the coaxial cable. The last data transition at the end of a packet is always low to high.
12	Coaxial Cable Receive Data	CXRD	An input pin that receives data from the coaxial cable of the network. Typical signal levels (referenced to V_{DD}) received on CXRD are -200 mV for high, -1.8V for a low and 0V during idle. The last data transition received is expected to be positive indicating the end of packet.

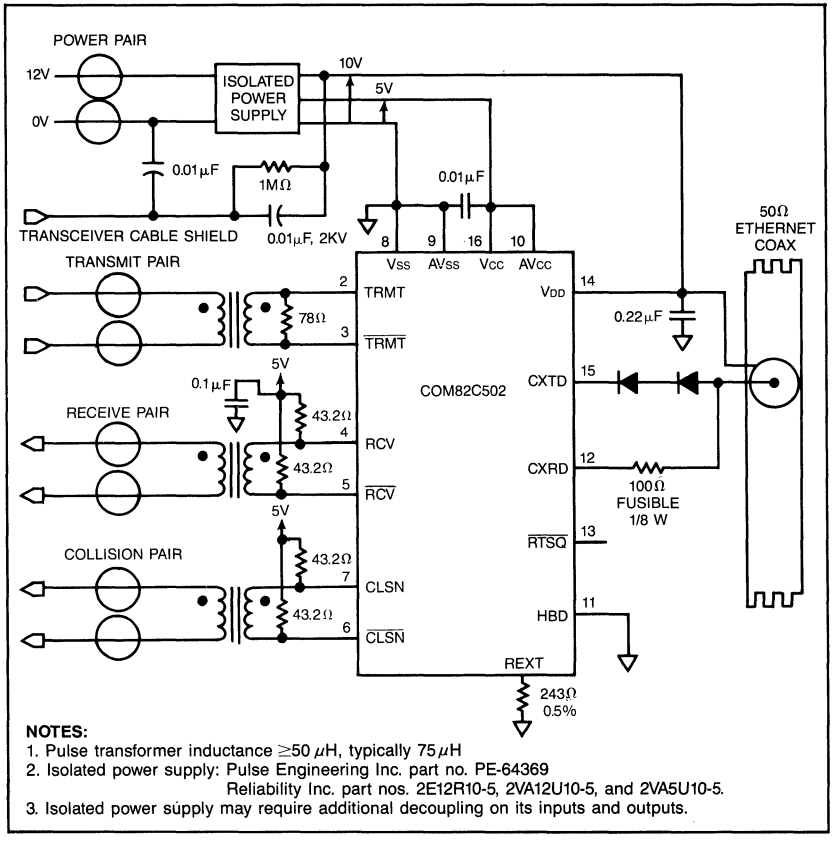
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
11	Heartbeat Disable	HBD	A strapping option that when tied low (V_{SS}), allows the transceiver to generate a collision detect heartbeat signal after each packet. A high (V_{CC}) on this pin disables the heartbeat circuitry as well as the 6.4 μs transmit inhibit timer but keeps the collision circuit enabled for use in repeater applications.
1	External Resistor	REXT	A 243Ω 0.5% resistor is attached between REXT and ground (V_{SS}) to provide precision internal current levels.
13	Redundant Transmit Squelch	$\overline{RTSQ}$	An open drain output that indicates the operational state of the 82502 transmitter. The output can be used to provide a redundant method of disabling the transceiver (MAU) transmitter for greater network reliability.
16	Power Supply	V_{CC}*	+5 ± 10% volts.
8	Ground	V_{SS}*	GROUND
14	Power Coax Shield	V_{DD}*	+10 ± 10% volts.
10	Analog Power	AV_{CC}*	+5 ± 10% volts. Included to reduce the effects of the current fluctuations in the V_{CC} pin.
9	Analog Ground	AV_{SS}*	Included to reduce the effects of current fluctuations in the V_{SS} pin.

***NOTE:**
These voltages are referenced to V_{SS}. The shield of the coaxial cable of the Ethernet™ channel (V_{DD}) is connected to earth ground.

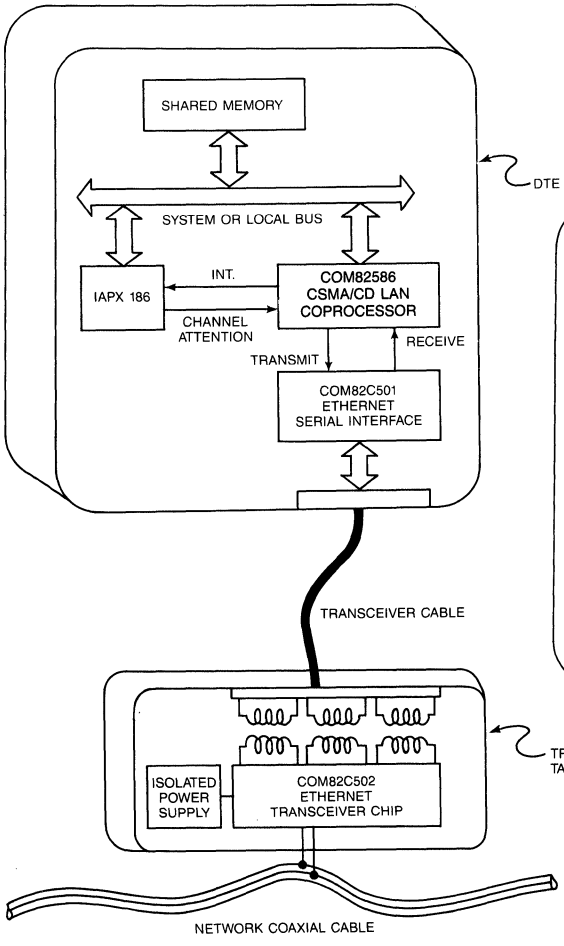
SECTION III

Design Example

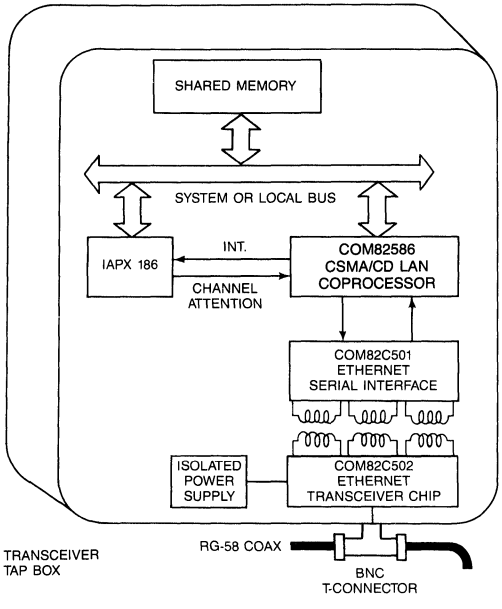


NOTES:
1. Pulse transformer inductance ≥50 μH, typically 75 μH
2. Isolated power supply: Pulse Engineering Inc. part no. PE-64369
   Reliability Inc. part nos. 2E12R10-5, 2VA12U10-5, and 2VA5U10-5.
3. Isolated power supply may require additional decoupling on its inputs and outputs.

Typical 10BASE5 (Ethernet™) Transceiver Implementation Using the COM82C502.



IEEE 802.3 10 Base 5 (Ethernet):
This configuration supports 100 users per segment, each segment being 500 meters long.



IEEE 802.3 10 Base 2 (Cheapernet):
This configuration supports 30 users per segment, each segment being 185 meters long.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

Ethernet™ is a trademark of Xerox Corporation.

STANDARD MICROSYSTEMS CORPORATION

COM 9026

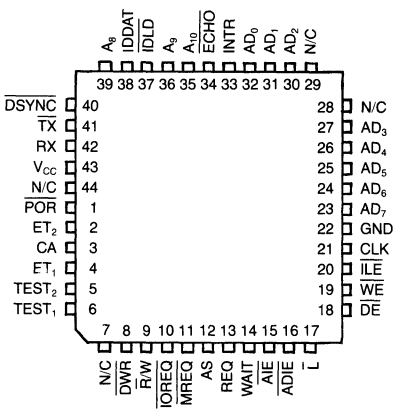
Local Area Network Controller LANC™

SECTION III

FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET® local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 9026
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)
- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single +5 volt supply

PIN CONFIGURATION



PACKAGE: 44-pin PLCC

PACKAGE: 40-pin DIP

GENERAL DESCRIPTION

The COM 90C26 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The Com 90C26 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 90C26 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 90C26 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 90C26 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 90C26. The processor can write commands to the COM 90C26 and also read COM 90C26 status. The COM 90C26 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

ARCNET® is a registered trademark of the Datapoint Corporation.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273 3100 • TWX 510-227 8898

STANDARD MICROSYSTEMS CORPORATION

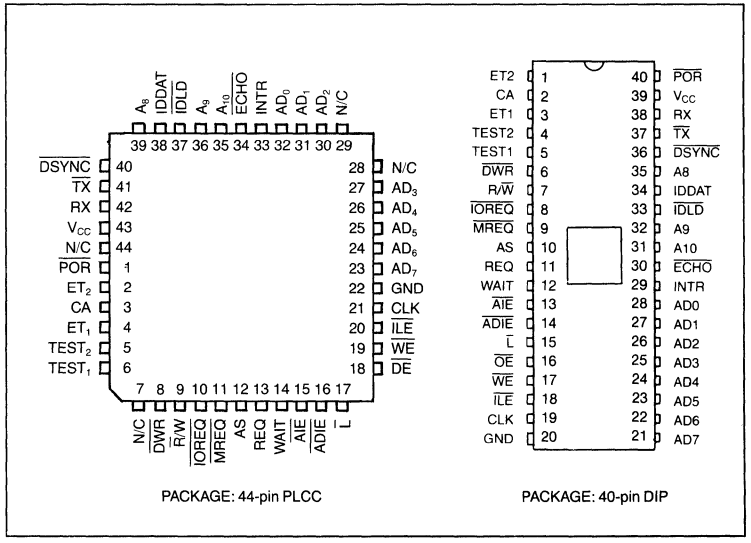
COM 90C26
PRELIMINARY

Local Area Network Controller
LANC™

FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET® local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 90C26
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)
- ☐ Low power CMOS technology
- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single +5 volt supply
- ☐ Compatible with HYC9058 (HITI) and HYC9068 (LAND)

PIN CONFIGURATION



PACKAGE: 44-pin PLCC

PACKAGE: 40-pin DIP

GENERAL DESCRIPTION

The COM 90C26 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The Com 90C26 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 90C26 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 90C26 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 90C26 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 90C26. The processor can write commands to the COM 90C26 and also read COM 90C26 status. The COM 90C26 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

ARCNET® is a registered trademark of the Datapoint Corporation.

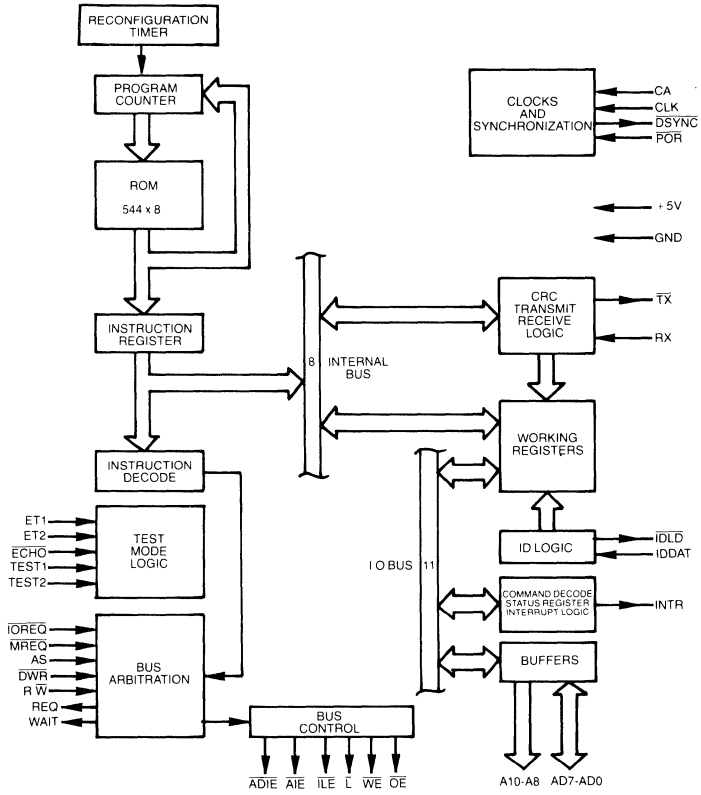


FIGURE 1—COM90C26 BLOCK DIAGRAM

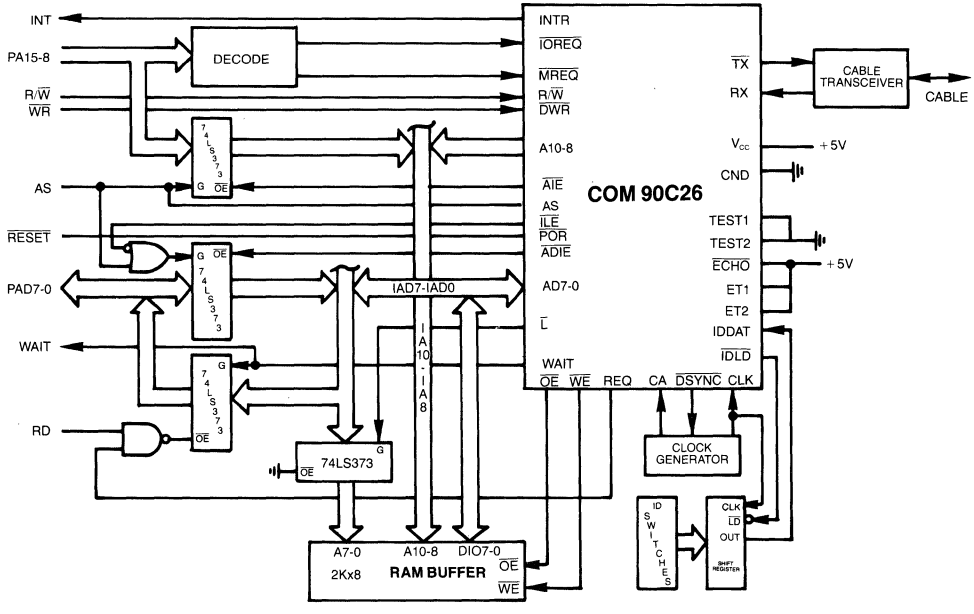


FIGURE 2—TYPICAL COM 90C26 INTERFACE

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

DIP PIN NO.	NAME	SYMBOL	FUNCTION
31, 32, 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 90C26 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21, 22, 23, 24, 25, 26, 27, 28	ADDRESS/ DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 90C26. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 90C26.
8	I/O REQUEST	$\overline{\text{IOREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 90C26. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{\text{MREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	A high level on this input signal indicates that the processor's access cycle to the COM 90C26 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 90C26. The write cycle will not completed, however, until the $\overline{\text{DWR}}$ input is asserted. This signal is sampled internally on falling edge of AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 90C26 to sample the state of the $\overline{\text{IOREQ}}$, $\overline{\text{MREQ}}$ and R/$\overline{\text{W}}$ inputs. The COM 90C26 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{\text{MREQ}}$ or $\overline{\text{IOREQ}}$ passed through an internal transparent latch gated with AS.
12	WAIT	WAIT	This output signal is asserted by the COM 90C26 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 90C26 is ready for the processor to complete its cycle.
6	DELAYED WRITE	$\overline{\text{DWR}}$	This input signal informs the COM 90C26 that valid data is present on the processor's data bus for write cycles. The COM 90C26 will remain in the WAIT state until this signal is asserted. $\overline{\text{DWR}}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	INTR	This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{\text{ILE}}$	This output signal, in conjunction with $\overline{\text{ADIE}}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 90C26 operations.
14	ADDRESS/ DATA INPUT ENABLE	$\overline{\text{ADIE}}$	This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{\text{ILE}}$ onto the interface address/data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{\text{AIE}}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	$\overline{\text{L}}$	This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{\text{WE}}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{\text{WE}}$.
16	OUTPUT ENABLE	$\overline{\text{OE}}$	This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{\text{IDLD}}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 90C26. The shift register is clocked with the same signal that feeds the COM 90C26 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2, 1	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 90C26 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.
37	TRANSMIT DATA	$\overline{\text{TX}}$	This output signal contains the serial transmit data to the CABLE TRANSCEIVER.
38	RECEIVE DATA	RX	This input signal contains the serial receive data from the CABLE TRANSCEIVER.

DESCRIPTION OF PIN FUNCTIONS (Continued)

PIN NO.	NAME	SYMBOL	FUNCTION
4, 5	TEST PIN 2 TEST PIN 1	TEST2 TEST1	These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing.
30	ECHO DIAGNOSTIC ENABLE	$\overline{ECHO}$	When this input signal is low, the COM 90C26 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 90C26 bus cycles, bus arbitration, serial ID input, and the internal timers.
2	CA	CA	This input signal is a 5 MHz clock used to control the operation of the COM 90C26 microcoded sequencer. This input is periodically halted in the high state by the $\overline{DSYNC}$ output.
36	DELAYED SYNC	$\overline{DSYNC}$	This output signal is asserted by the COM 90C26 to cause the external clock generator logic to halt the CA clock. Refer to figure 9.
40	POWER ON RESET	$\overline{POR}$	This input signal clears the COM 90C26 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	V_{CC}	Power Supply
20	GROUND	GND	Ground

PROTOCOL DESCRIPTION

LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 85 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 86 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 90C26's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 90C26 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will

verify the packet. If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsucessful delivery of the packet. An interrupt mask permits the COM 90C26 to generate an interrupt to the processor when selected status bits become true. Figure 4 is a flow chart illustrating the internal operation of the COM 90C26.

NETWORK RECONFIGURATION

A significant advantage of the COM 90C26 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 90C26 is turned on (creating a new active node on the network), or if the COM 90C26 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 90C26 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 90C26 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 90C26 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 90C26 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 90C26 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 90C26 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 90C26 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 90C26 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 90C26 on the network will finally have saved a NID value equal to the ID of the COM 90C26 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

BROADCAST MESSAGES

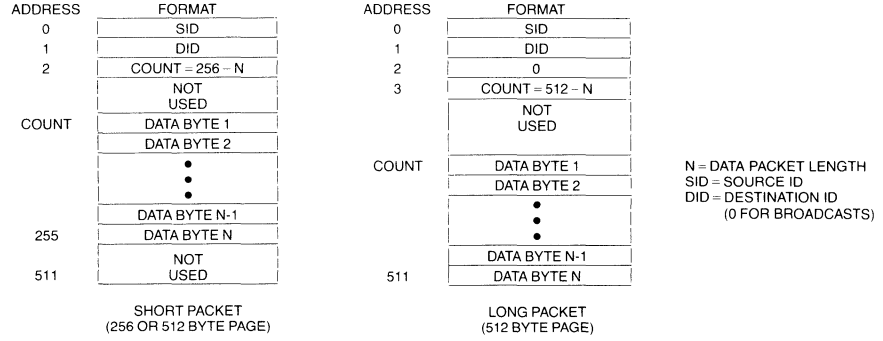
Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 3 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 90C26 COMMANDS") to a logic zero.

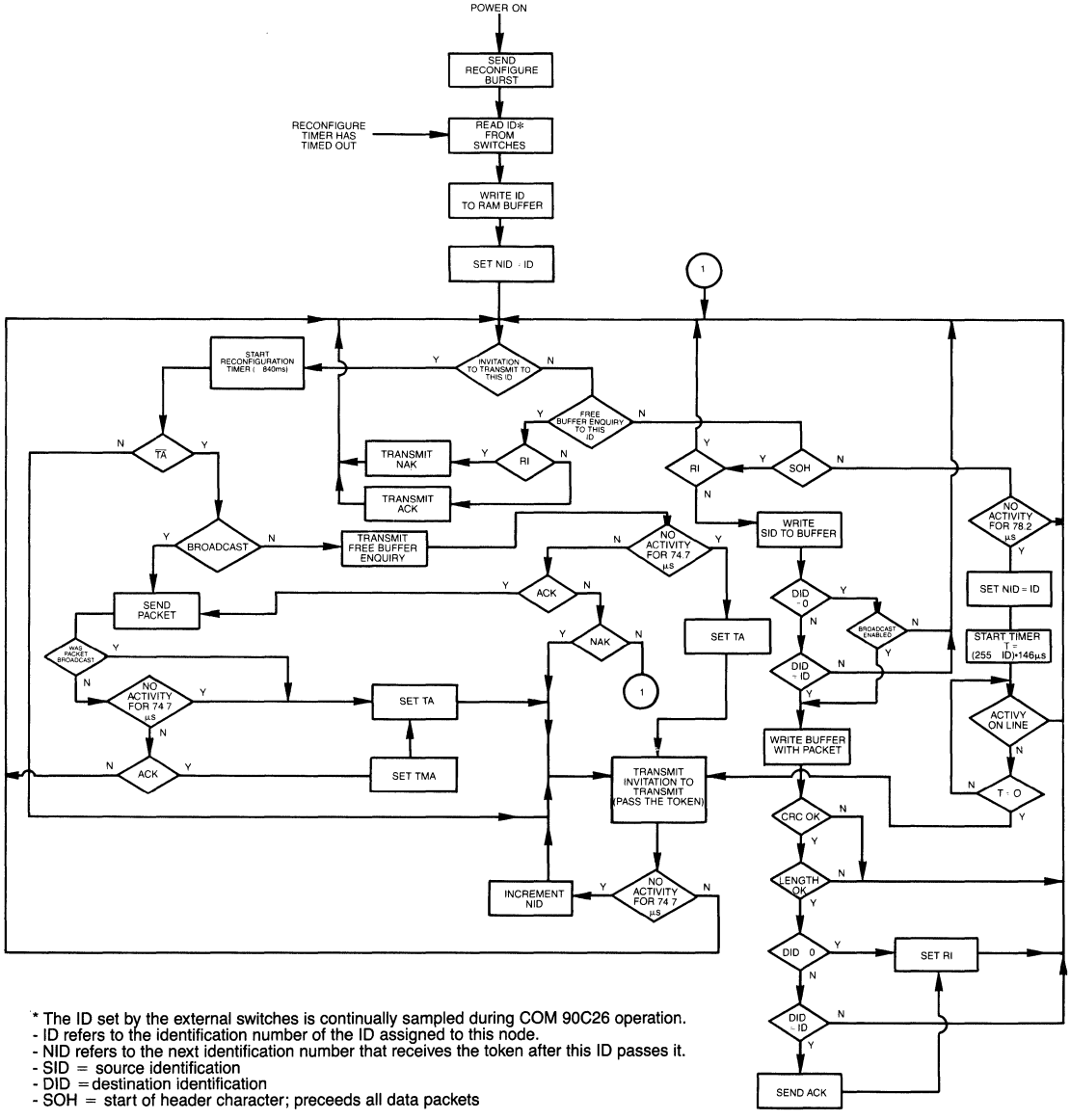
COM 90C26 OPERATION

BUFFER CONFIGURATION

During a transmit sequence, the COM 90C26 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 90C26 will interpret the packet as a long or short packet depending on whether the contents of buffer location 002 is zero or non zero. During a receive sequence, the COM 90C26 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 90C26 receiver or the COM 90C26 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512) byte are shown below.

FIGURE 3— RAM BUFFER PACKET CONFIGURATION





* The ID set by the external switches is continually sampled during COM 90C26 operation.
- ID refers to the identification number of the ID assigned to this node.
- NID refers to the next identification number that receives the token after this ID passes it.
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

FIGURE 4—90C26 OPERATION

PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 90C26 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 90C26, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 90C26.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 90C26 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multimessage transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 90C26, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 90C26 or command writes to the COM 90C26).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 90C26 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 90C26.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{\text{IOREQ}}$ or $\overline{\text{MREQ}}$ is asserted. These access cycles run completely asynchronous with respect to the COM 90C26. Because of this, upon processor access cycle requests, the COM 90C26 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 90C26 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 90C26, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{\text{AIE}}$ and $\overline{\text{ADIE}}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{\text{L}}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{\text{OE}}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

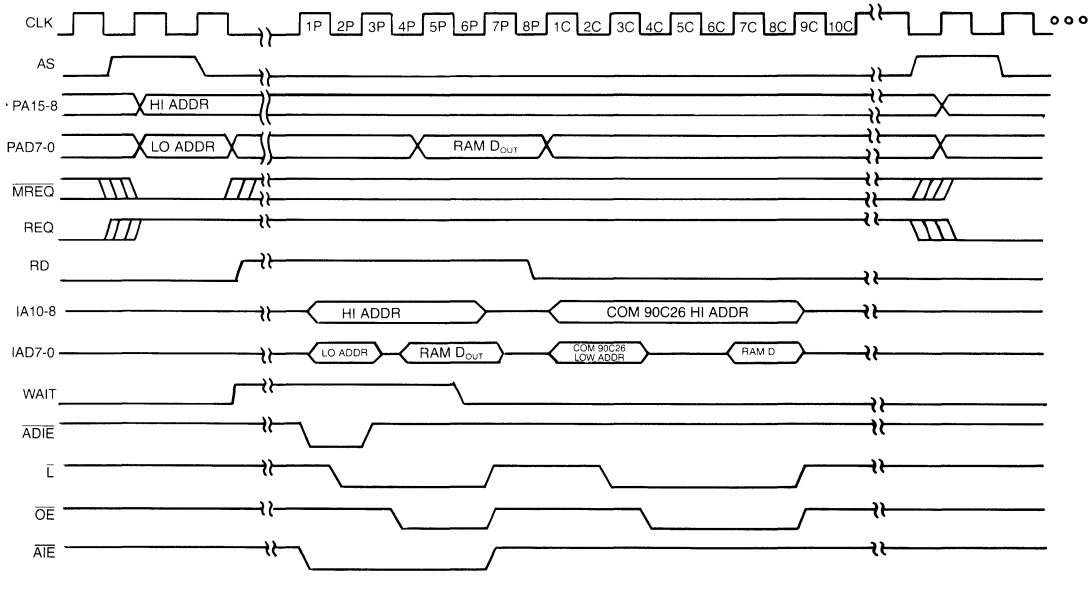


FIGURE 5—PROCESSOR READ RAM FOLLOWED BY COM 90C26 READ RAM

and driven out via the logic function RD ended with REQ. For processor I/O read cycles from the COM 90C26, ADIE and AIE are used to enable the processor address into the COM 90C26. Data out of the COM 90C26 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 90C26 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 90C26 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 90C26 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 90C26 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 90C26, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 90C26. Delaying the activation of DWR will hold up the COM 90C26 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 90C26 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 90C26 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 90C26 cycle will follow immediately after the processor cycle. Figure 5 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 90C26 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 5 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 90C26 access cycle will take 5 CLK periods to end. Figure 5 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 90C26 request has already been granted, the COM 90C26 cycle will occur first, as shown in figure 5. Figure 6 illustrates the timing relationship of a COM 90C26 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 90C26 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 6, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 90C26 produces a leading edge on both ADIE and AIE. If the processor request

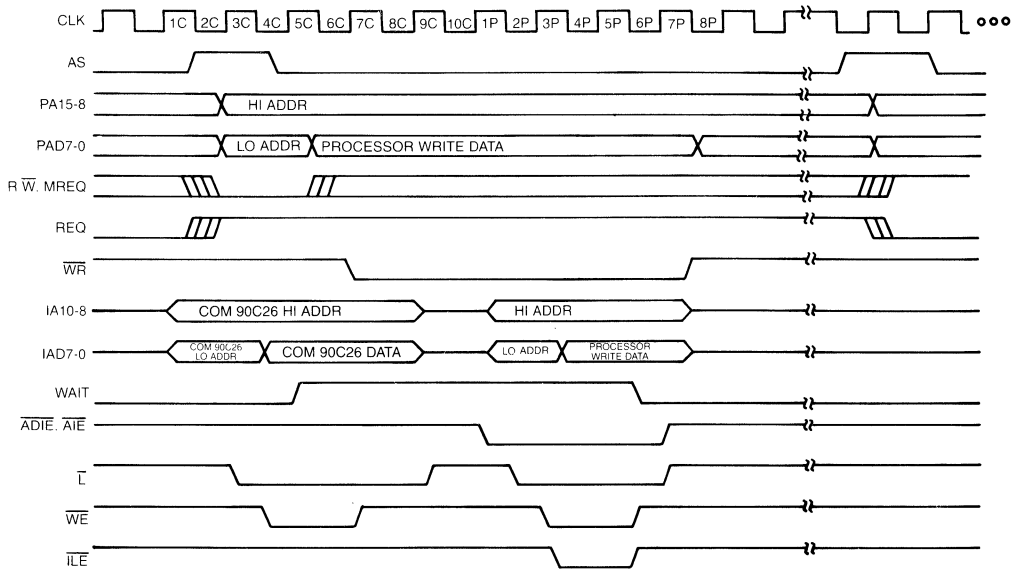


FIGURE 6—COM 90C26 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM

occurs before the end of half CLK interval 5C (figure 6 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 90C26 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 7 and 8 illustrate timing for Processor Read COM 90C26 and Processor Write COM 90C26 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 5 and 6 if these processor cycles occur.

POWER UP AND INITIALIZATION

The COM 90C26 has the following power up requirements:

1—The $\overline{\text{POR}}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the $\overline{\text{POR}}$ input is removed.
3—While $\overline{\text{POR}}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{\text{POR}}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{\text{POR}}$ may be released before CA begins running.

During $\overline{\text{POR}}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{\text{DSYNC}}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{\text{POR}}$ signal is removed, the COM 90C26 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 90C26 will start operation four CA clock cycles after the $\overline{\text{POR}}$ signal is removed. At this time, the COM 90C26, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 90C26 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

CLOCK GENERATOR

The COM 90C26 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 90C26 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{\text{DSYNC}}$ output and the RX input. The $\overline{\text{DSYNC}}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{\text{DSYNC}}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{\text{DSYNC}}$. (See figure 10 for an implementation of this circuit.)

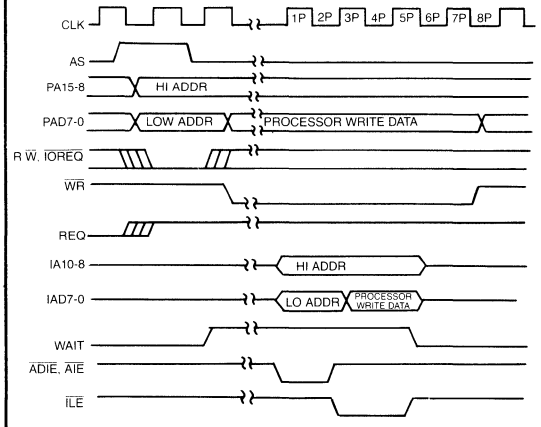


FIGURE 7—PROCESSOR READ COM 90C26

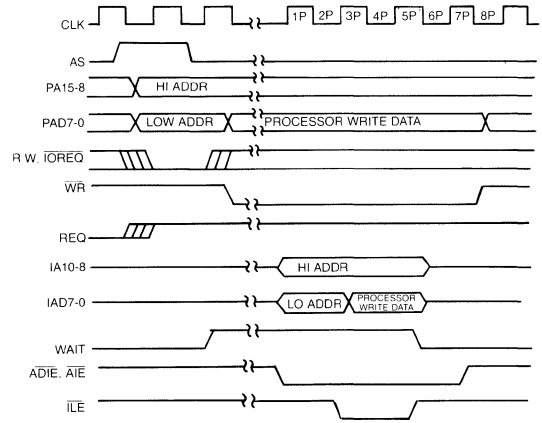


FIGURE 8—PROCESSOR WRITE COM 90C26

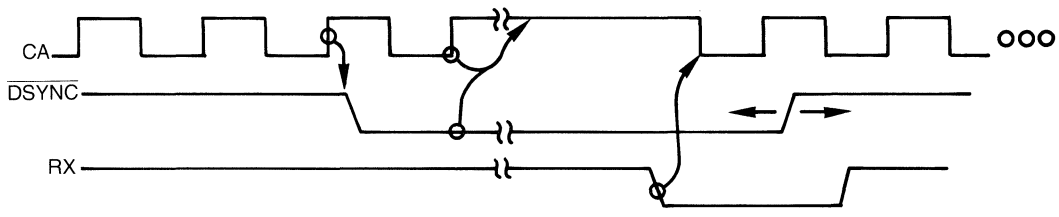


FIGURE 9—CA CLOCK GENERATOR TIMING

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 90C26 operation.

Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 90C26 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 4 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 4, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 90C26 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 90C26 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. It should be noted that for proper network operation, all COM 90C26's connected to the same network must have the same response time, idle time and reconfiguration time.

ET2	ET1	RESPONSE TIME (μs)	IDLE TIME (μS)	RECONFIGURATION TIME (ms)
1	1	78	86	840
1	0	285	316	1680
0	1	563	624	1680
0	0	1130	1237	1680

TABLE 1
COM 90C26 INTERNAL PROGRAMMABLE TIMER VALUES

I/O COMMANDS

I/O commands are executed by activating the $\overline{\text{IOREQ}}$ input. The COM 90C26 will interrogate the AD0 and the R/$\overline{\text{W}}$ inputs at the AS time to execute commands according to the following table:

$\overline{\text{IOREQ}}$	AD0	R/$\overline{\text{W}}$	FUNCTION
low	low	low	write interrupt mask
low	low	high	read status register
low	high	low	write COM 90C26 command
low	high	high	reserved for future use

READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 90C26 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 90C26 has received an active signal on the POR input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

WRITE INTERRUPT MASK

The COM 90C26 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	XXX	XXX	XXX	XXX	RECON TIMER	XXX	TRANSMITTER AVAILABLE

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

WRITE COM 90C26 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

WRITTEN DATA	COMMAND
00000000	reserved for future use
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 90C26 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 90C26 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 90C26 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "1". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 90C26 has received an acknowledgement from the destination COM 90C26. This acknowledgement is strictly hardware level which is sent by the receiving COM 90C26 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM 90C26 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 90C26 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If c is a logic "1", the COM 90C26 will handle short as well as long packets. If c is a logic "0", the COM 90C26 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "l", the RECON status flag is cleared.

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

MAXIMUM GUARANTEED RATINGS*

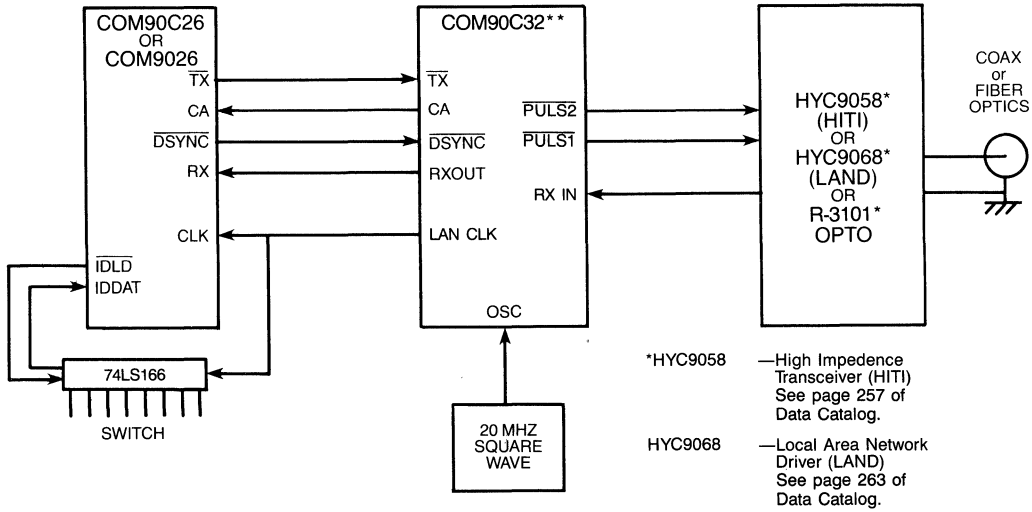
Operating Temperature Range	0 to 70°C
Storage Temperature Range	−55 to 150°C
Lead Temperature (soldering, 10 seconds)	+325°C
Positive Voltage on any pin	V_{CC} +0.3V
Maximum V_{CC}	+7V
Negative Voltage on any pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	input low voltage	−0.3		0.8	V	
V_{IH1}	input high voltage 1	2.2		V_{CC}	V	except CA and CLK
V_{IH2}	input high voltage 2	V_{CC}−1.0		6.5	V	for CA or CLK
V_{OL1}	output low voltage 1			0.4	V	I_{OL} = 1.6ma
V_{OL2}	output low voltage 2			0.5	V	I_{OL} = 2.0ma
V_{OH1}	output high voltage	2.4			V	except $\overline{Tx}$ and $\overline{DSYNC}$ I_{OH} = −100μA
V_{OH2}	output high voltage	3.2			V	$\overline{Tx}$ and $\overline{DSYNC}$ only I_{OH} = −100μA
I_L	input leakage current			±10	μA	
C_{IN}	input capacitance			20	pf	
C_{DB}	data bus capacitance			50	pf	
C_L	all other capacitance			30	pf	
I_{CC}	power supply current		16		ma	



*HYC9058 —High Impedence Transceiver (HITI) See page 257 of Data Catalog.

HYC9068 —Local Area Network Driver (LAND) See page 263 of Data Catalog.

R-3101 —Pin Compatible Fiber Optic Driver Raycom Systems 6395 Gunpark Drive Boulder, Colorado 80301

**COM91C32 —Local Area Network Transceiver is also compatible with the COM9026/COM90C26. See page 247 of Data Catalog

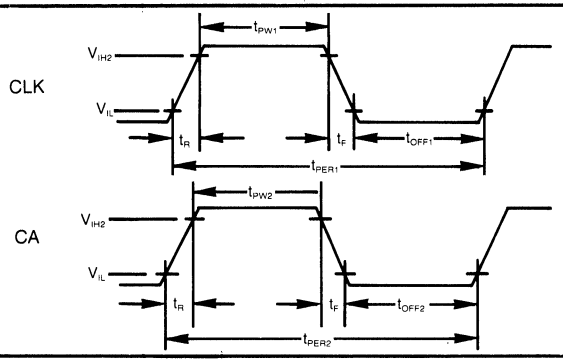
Figure 10–COM90C26 SYSTEM INTERFACE

AC ELECTRICAL CHARACTERISTICS ($T_A = 0°$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{PW1}	CLK pulse width	65			ns	
t_{PER1}	CLK period	190	200	600	ns	
t_{OFF1}	CLK off time	65			ns	
t_{PW2}	CA pulse width	60			ns	
t_{PER2}	CA period	190			ns	
t_{OFF2}	CA off time	60	100	300	ns	
t_R	CLK, CA rise time			20	ns	
t_F	CLK, CA fall time			20	ns	
t_1	width of addr. strobe	50		400	ns	
t_2	REQ output delay	0		100	ns	
t_3	WAIT assertion delay	0		200	ns	
t_4	delay to rising edge of processor cycle	t_P		$2t_P + 100$	ns	$t_P = t_{PER1}$
t_5	data hold into COM 9026	80			ns	
t_6	setup COM 9026 data out	60			ns	
t_7	$\overline{WE}$ delay from CLK	0		100	ns	
t_8	$\overline{TX}$ on delay from CA falling edge	10		150	ns	
t_9	$\overline{TX}$ off delay from CA falling edge	10		150	ns	
t_{10}	AS period	$7/2\ t_P$			ns	$t_P = t_{PER2}$
t_{11}	$\overline{DSYNC}$ delay from CA rising edge	10		150	ns	
t_{12}	delay to wait off	20		100	ns	
t_{13}	$\overline{DWR}$ setup time	50			ns	
t_{14}	$\overline{ILE}$ delay from CLK	10		100	ns	
t_{15}	processor addr. setup from $\overline{ADIE}$,			50	ns	
t_{16}	processor command setup time	125			ns	
t_{17}	addr. enable setup time to $\overline{L}$	50			ns	
t_{18}	addr. hold time from $\overline{L}$	50			ns	
t_{19}	strobe and data hold for read	20			ns	
t_{20}	AD bus HI impedance to $\overline{OE}$s	0			ns	
t_{21}	delay of $\overline{IDLD}$ from CLK rising edge	0		120	ns	
t_{22}	delay of IDDAT from CLK rising edge	0		50	ns	
t_{23}	off delay from CLK rising edge	0		100	ns	
t_{24}	addr. to RAM data valid			300	ns	
t_{25}	$\overline{OE}$ setup to WAIT falling edge	140			ns	
t_{26}	strobe & data hold for write	50			ns	
t_{27}	addr. enable setup to WAIT	300			ns	
t_{28}	$\overline{ADIE}$ to $\overline{OE}$ delay	40			ns	
t_{29}	COM 9026 write data hold time	80			ns	
t_{30}	$\overline{OE}$ to RAM data valid	0		140	ns	
t_{31}	status setup to AS falling edge	50			ns	
t_{32}	status hold from AS falling edge	50			ns	
t_{33}	RX setup to CA rising edge	80			ns	
t_{34}	RX hold time from CA rising edge	30			ns	
t_{35}	$\overline{POR}$ active time	100			us	after V_{CC} has been stable for time t_{35}, the minimum $\overline{POR}$ active time is 10 cycles of CLK.

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

FIGURE 11— CLK, CA AC CHARACTERISTICS



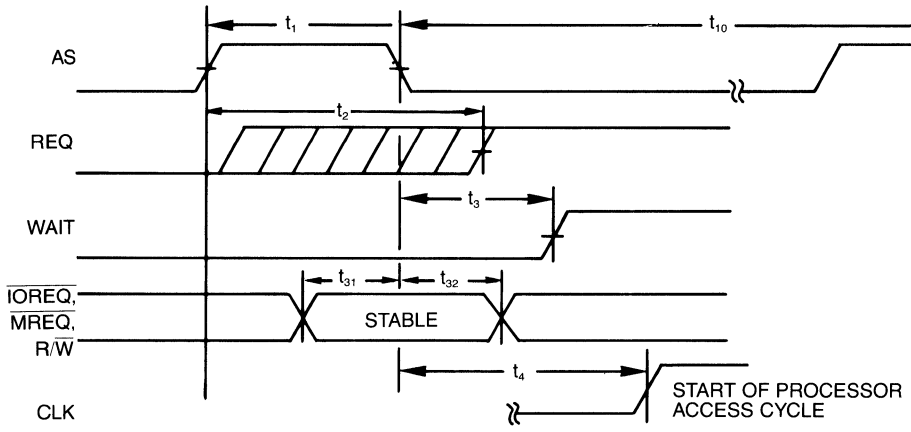


FIGURE 12—PROCESSOR ACCESS SYNCHRONIZATION

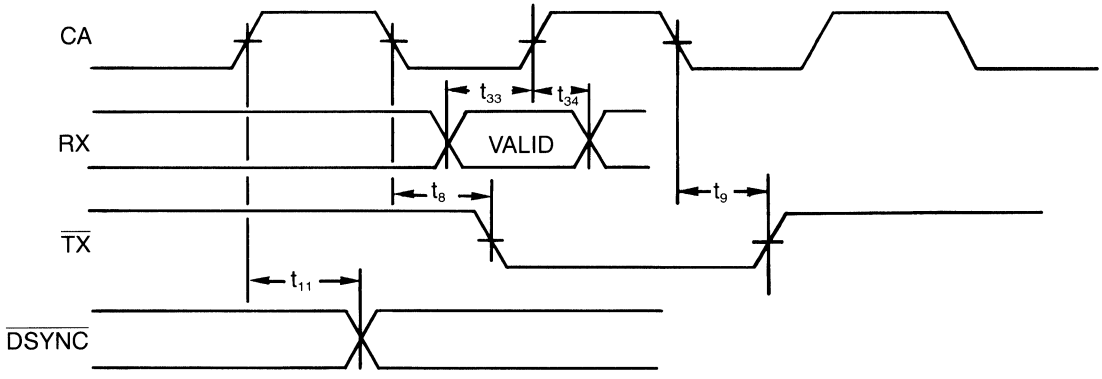


FIGURE 13—TRANSMIT AND RECEIVE TIMING

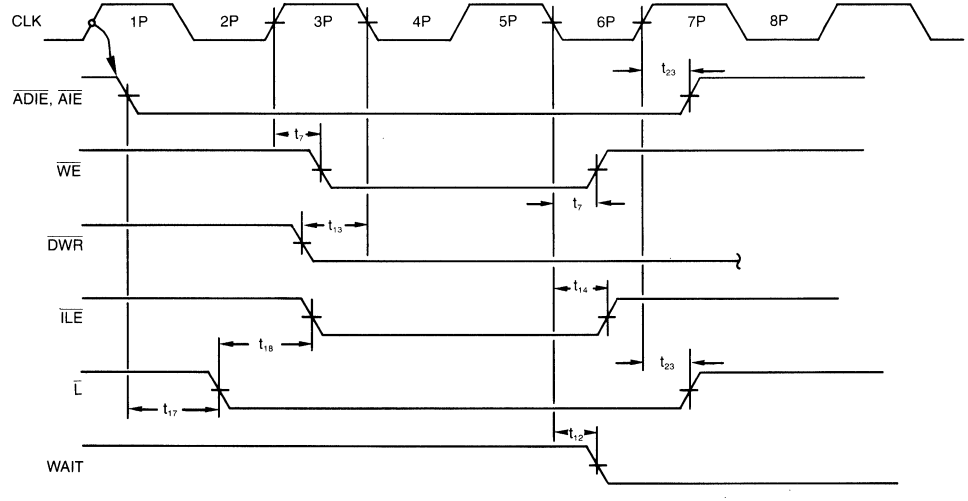


FIGURE 14—PROCESSOR WRITE RAM AC TIMING

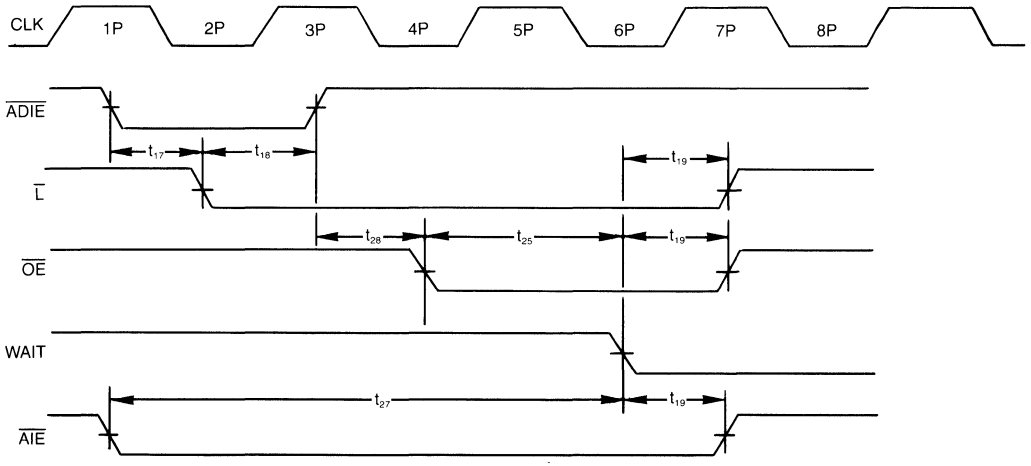


FIGURE 15—PROCESSOR READ RAM AC TIMING

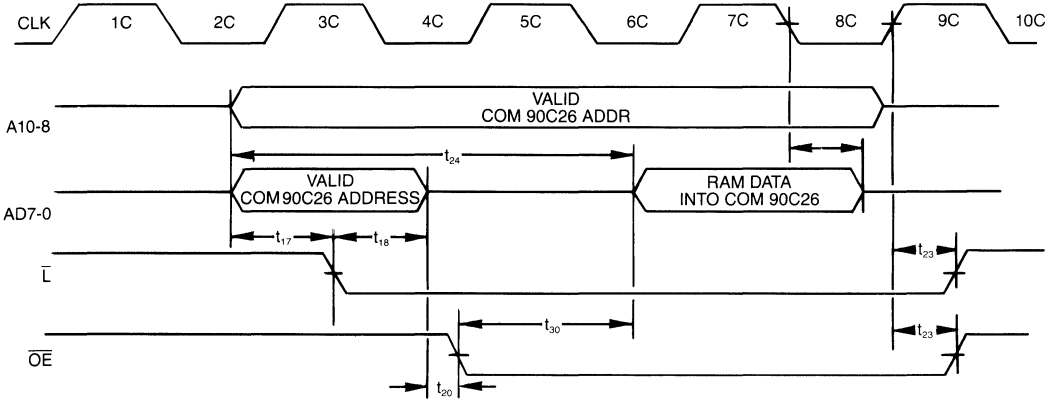


FIGURE 16—COM 90C26 READ RAM AC TIMING

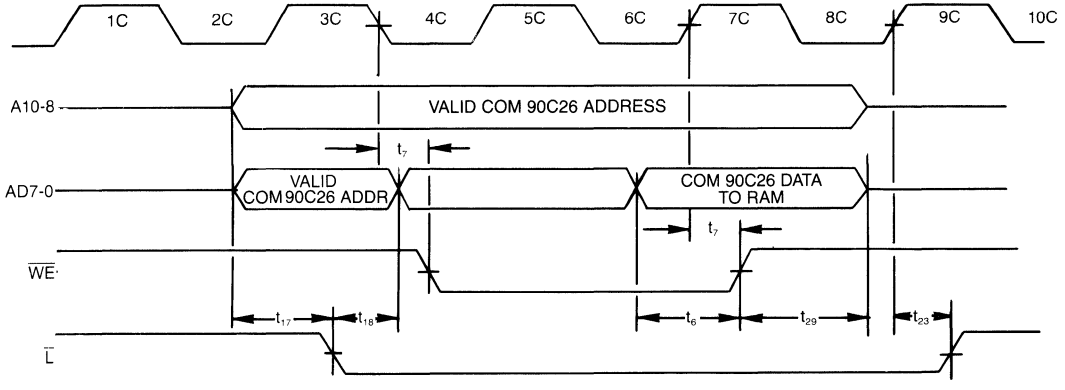


FIGURE 17—COM90C26 WRITE RAM AC TIMING

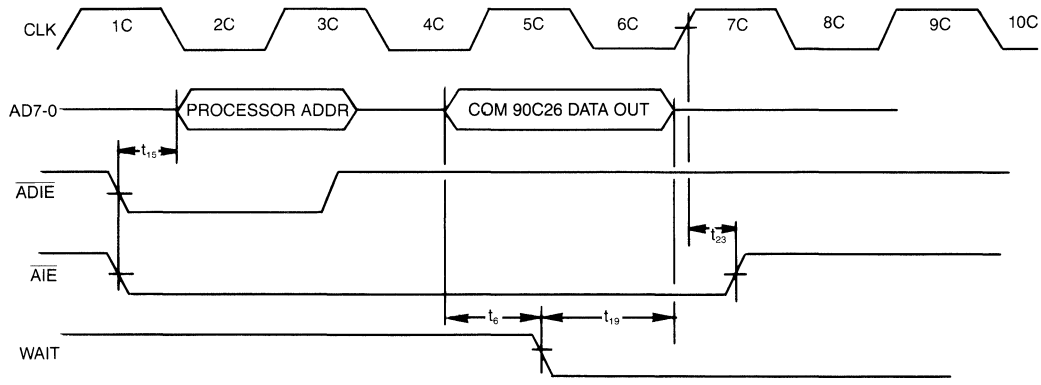


FIGURE 18—PROCESSOR READ COM 90C26 AC TIMING

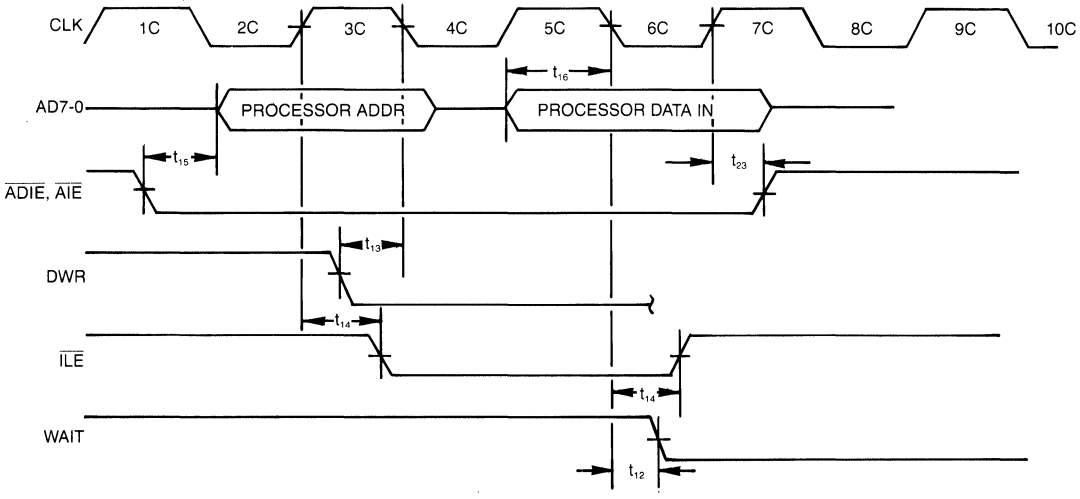


FIGURE 19—PROCESSOR WRITE COM 90C26 AC TIMING

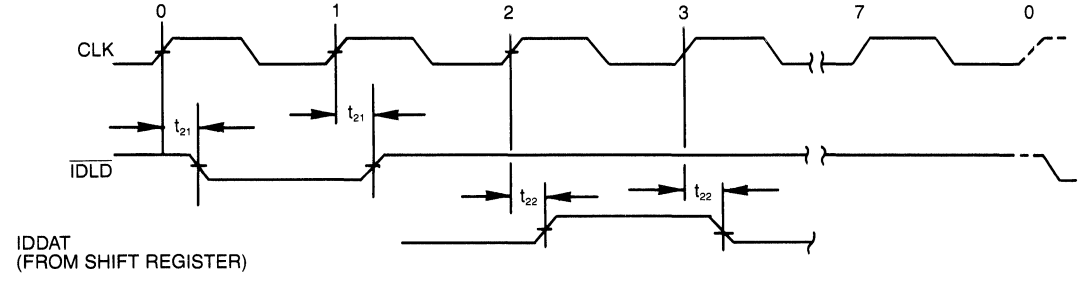


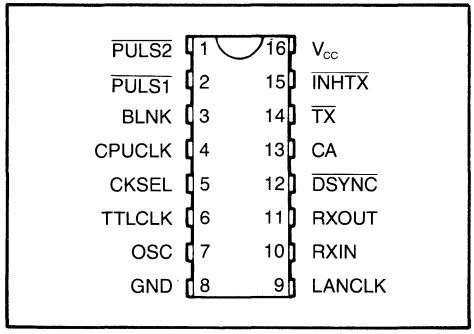
FIGURE 20—ID INPUT AC TIMING

COM 90C32
Local Area Network Transceiver
LANT

FEATURES

- ☐ Reduces chip count for COM 9026 and COM 90C26 ARCNET® implementations by 6-8 TTL chips
- ☐ Performs all clock generation functions for the COM 9026 and COM 90C26
- ☐ Compatible with the COM 9026 and COM 90C26
- ☐ Provides line drive signals for transmission
- ☐ Converts incoming serial receive data to NRZ data format
- ☐ Generates two 4 MHz general purpose clocks
- ☐ See COM 91C32 (Improved version with built-in Crystal Oscillator)

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM 90C32 local area network transceiver is a companion chip to the COM 9026/COM 90C26 Local Area Network Controller (LANC) and will perform the additional functions necessary to allow simple interface to a transmission media for all ARCNET® (or equivalent) local area networks. Using a 20 MHz input clock, the COM 90C32 will produce two, 5 MHz clocks for the COM 9026/ COM 90C26. The first 5 MHz clock is free running and will directly feed the CLK input of the COM 9026/COM 90C26 (pin 19). The second 5 MHz clock has start/stop capability which is controlled by the DSYNC output of the COM 9026/ COM 90C26 (pin 36) and the received data input as required by the COM 9026/COM 90C26 (pin 2). Two additional 4 MHz free running clocks are also generated on the COM 90C32 to allow operation of other logic, a microprocessor, or an LSI controller.

During data reception, the COM 90C32 will convert incoming serial receive data from the transmission media to NRZ form which will directly feed the RX input of the COM 9026/COM 90C26 (pin 38). During transmission, the COM 90C32 converts the transmit data from the COM 9026/ COM 90C26 (TX, pin 37) into the waveforms necessary to drive opposite ends of the rf transformer used in the ARCNET® cable electronics shown in figure 2.

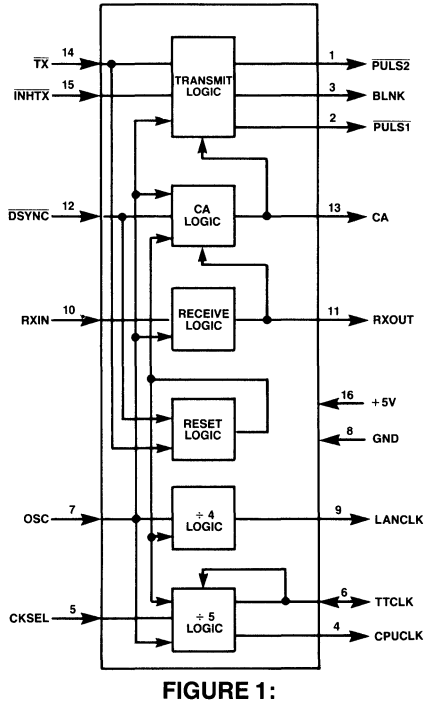
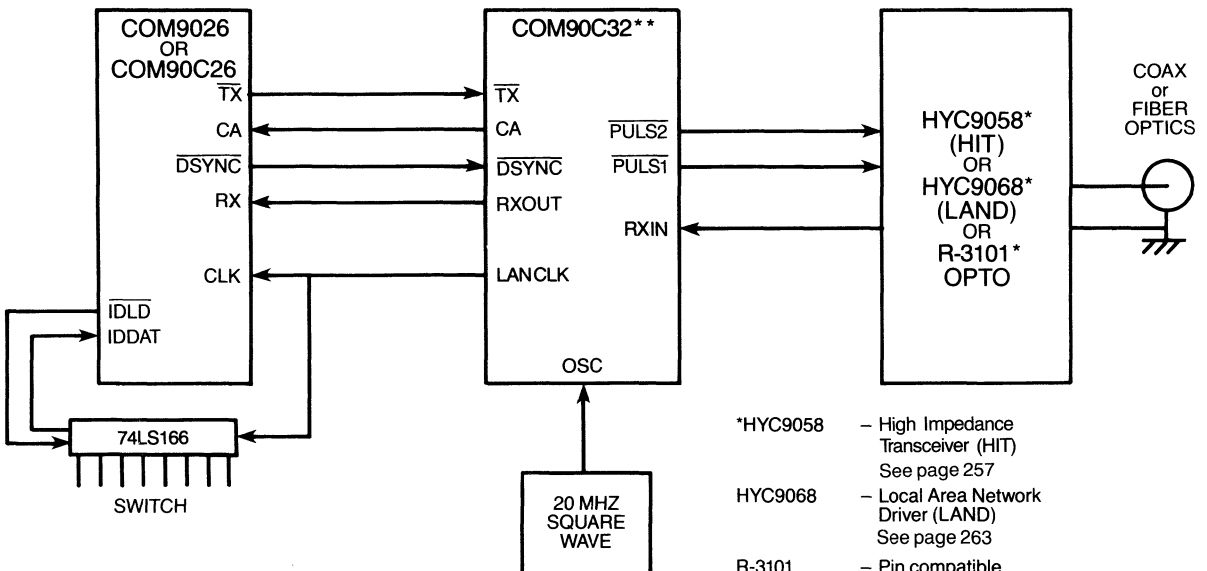


FIGURE 1:
COM 90C32 BLOCK DIAGRAM

®ARCNET is a registered trademark of the Datapoint Corporation.



*HYC9058 – High Impedance Transceiver (HIT)
See page 257

HYC9068 – Local Area Network Driver (LAND)
See page 263

R-3101 – Pin compatible Fiber Optic Driver
Raycom Systems
6395 Gunpark Drive
Boulder, Colorado 80301

**COM91C32 – Improved Local Area Network Transceiver is also compatible with the COM 9026/90C26.
See page 247

FIGURE 2—COM90C32 SYSTEM INTERFACE

DESCRIPTION OF PIN FUNCTIONS

(Refer to figure 2)

COM 9026/COM 90C26 INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
1, 2	PULSE 2 PULSE 1	$\overline{PULS2}$ $\overline{PULS1}$	$\overline{PULS2}$ and $\overline{PULS1}$ are two nonoverlapping negative pulses which occur every time the $\overline{TX}$ input is pulsed. $\overline{PULS2}$ and $\overline{PULS1}$ are used to feed an external driver as shown in figure 2.
3	BLANK	BLNK	When used with the circuitry shown in figure 2, this output should be left unconnected. The timing of this signal is shown in figure 4.
10	RECEIVE IN	RXIN	This input is the recovered receive data from the network. For each dipulse appearing on the network, the comparator shown in figure 2 will produce a positive pulse which directly feeds this input.
11	RECEIVE OUT	RXOUT	This output is the NRZ data generated as a function of the RXIN pulse waveform which directly feeds the RX input of the COM9026/COM90C26, (pin 38).
12	DELAYED SYNC	$\overline{DSYNC}$	This active low input, which is asserted by the COM9026/COM90C26, will halt the CA clock output.
13	CA	CA	This output is a 5 MHz start/stop clock that is halted when $\overline{DSYNC}$ goes active low and restarted by a low signal on the RXOUT output. This clock is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
14	TRANSMIT DATA	$\overline{TX}$	This input, which is asserted by the COM9026/COM90C26, is the serial data transmitted by the node.
15	TRANSMIT INHIBIT	$\overline{INHTX}$	This active low input inhibits the $\overline{TX}$ signal from initiating transmit signals by forcing $\overline{PULS1}$ and $\overline{PULS2}$ to a high and BLNK to a low. This signal should be asserted during a power on reset condition.

SYSTEM CLOCK INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
4	CPU CLOCK	CPUCLK	This output is a 4 MHz free running clock capable of driving 130 pf with 30 nanosecond rise and fall times. It is identical to the TTLCLK input when CKSEL is high. When CKSEL is low, this output becomes the inversion of the signal that is fed into the TTLCLK input.
5	CLOCK SELECT	CKSEL	This input selects the clock interface option for the TTLCLK and CPUCLK. When this signal is high, both the TTLCLK and CPUCLK are identical 4 MHz free running clock outputs which are generated from the 20 MHz input clock (OSC) via a divide by 5 frequency divider. When this input is low, the TTLCLK pin becomes an input and the CPUCLK output will produce the inversion of the signal appearing on TTLCLK input.
6	TTL CLOCK	TTLCLK	This pin can be either an input or an output depending on the state of the CKSEL input. When CKSEL is high, a free running 4 MHz clock is ouput. When CKSEL is low, the pin becomes an input which drives an inverter that feeds the CPUCLK output.
7	OSCILLATOR	OSC	This input requires a 20 MHz clock. (See COM91C32 for built-in oscillator).
9	LOCAL AREA NETWORK CLOCK	LANCLK	This output will supply the free running 5 MHz clock to the COM9026/ COM90C26, pin 19. It is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
8	GROUND	GND	Ground
16	+5 VOLT SUPPLY	V_{CC}	Power Supply

FUNCTIONAL DESCRIPTION

Transmit logic (refer to figures 2 and 4)

The COM 9026/COM 90C26, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Refering to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to two,100 nanosecond non overlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ are used to create a 200 nanosecond wide dipulse by driving opposite ends of the RF transformer shown in figure 2.

Receive logic (refer to figures 2 and 5)

As each dipulse appears on the cable, it is coupled through the RF transformer, passes through the matched filter, and feeds the 75108B comparator. The 75108B produces a positive pulse for each dipulse received from the cable. These pulses are captured by the COM 90C32 and are converted to NRZ data with the NRZ data bit boundaries being delayed by 5 OSC clock periods as shown in figure 5. As each byte is received by the COM 9026/COM 90C26, the CA clock is stopped by the COM 9026/COM 90C26 (via $\overline{DSYNC}$) until the first bit of the next byte is received which will automatically restart the CA clock. The COM 9026/COM 90C26 uses the CA clock to sample the NRZ data and these sample points are shown in figure 5.

Typically, RXIN pulses occur at multiples of the transmission rate of 2.5 MHz (400 nanoseconds). The COM 90C32 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −55° to 150°C
Lead Temperature (soldering, 10 sec.) ..... 325°C
Positive Voltage on any Pin ..... V_{CC} + 0.3V
Negative Voltage on any Pin ..... −0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGES					
V_{IH}	2.7			V	
V_{IL}			0.8	V	
OUTPUT VOLTAGES					
V_{OH1}	2.4			V	I_{OH} = −0.4 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs.
V_{OL1}			0.4	V	I_{OL} = 4.0 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs.
V_{OH2}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CPUCLK output.
V_{OL2}			0.4	V	I_{OL} = 0.1 mA, CPUCLK output.
V_{OH3}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CA and LANCLK outputs.
V_{OL3}			0.4	V	I_{OL} = 0.4 mA, CA and LANCLK outputs.
LEAKAGE CURRENT					
I_{11}			50	µA	TTLCLK input with CKSEL low.
I_{12}			10	µA	all other inputs.
INPUT CAPACITANCE					
C_{IN}			20	pf	
SUPPLY CURRENT					
I_{CC}			20	mA	at 20 MHz OSC frequency.

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
OSC Input					
t_{CY1}		50		ns	
t_{CH1}	20			ns	
t_{CL1}	20			ns	
CA, LANCLK					
t_{CY2}		200		ns	
t_{CH2}	75			ns	
t_{CL2}	75			ns	
t_{F2}			20	ns	
t_{R2}			20	ns	
TTLCLK					
t_{CY3}		250		ns	
t_{CH3}	110			ns	
t_{CL3}	110			ns	
CPUCLK (CKSEL is high)					
t_{CY4}		250		ns	
t_{CH4}	110			ns	
t_{CL4}	110			ns	
t_{F4}			30	ns	
t_{R4}			30	ns	
t_{DCK}			45	ns	for CKSEL low.
TRANSMIT TIMING					
t_{STC}	50	30		ns	
t_{HTC}	10			ns	
t_{DP}			60	ns	
t_{P1W}		$2t_{CY1}$		ns	
t_{WB}		t_{CY1}		ns	
t_{P2W}		$2t_{CY1}$		ns	
t_{RST}			40	ns	
RECEIVE TIMING					
t_{RS}	30			ns	
t_{RW}	10			ns	
t_{DO}			70	ns	
t_{RO}		$5t_{CY1} + t_{DO}$		ns	
t_{SSO}	10			ns	
t_{SSC}		20		ns	
t_{ROW}		400		ns	

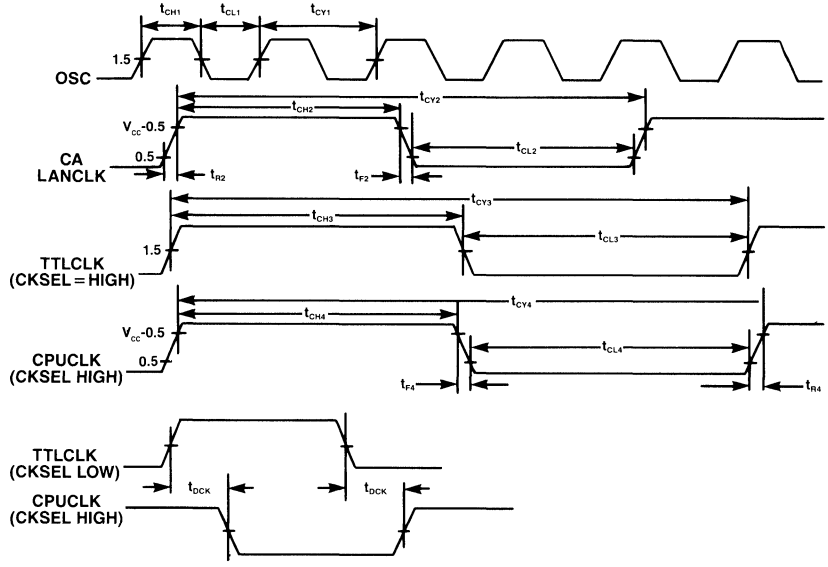


FIGURE 3: CLOCK TIMING

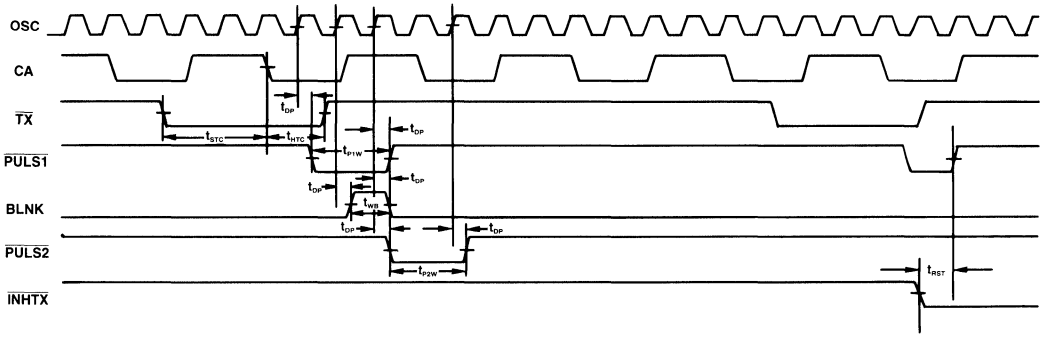


FIGURE 4: TRANSMIT TIMING PARAMETERS

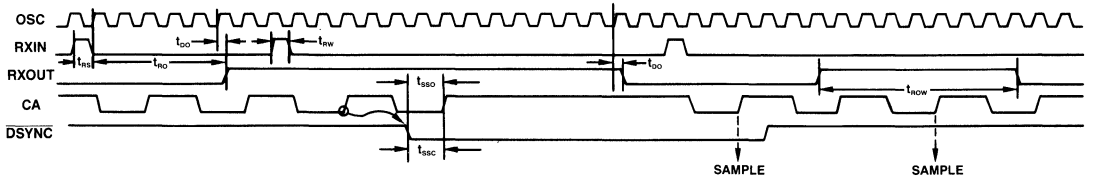


FIGURE 5: RECEIVE TIMING PARAMETERS

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 · TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM9046

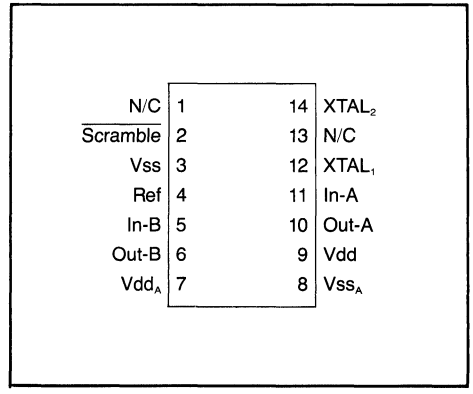
PRELIMINARY

Single Side Band Speech Scrambler

FEATURES

- ☐ Speech Scrambling/Descrambling
- ☐ High Dynamic Range
- ☐ Low Voltage Operation
- ☐ Low Power Consumption
- ☐ On Board Crystal Oscillator
- ☐ Uses Common Color Burst Crystal
- ☐ Full Duplex Operation
- ☐ Selectable Scramble Enable/Disable
- ☐ Switched Capacitor Filter
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM9046 is a monolithic integrated circuit containing a voice scrambler, a descrambler and a crystal oscillator. It is designed to provide speech communication equipment with a privacy feature. The COM9046 is also designed to operate with power supply voltages as low as ±2Volts. The low voltage operation and low power consumption of the COM9046 make it ideal for use in portable equipment.

Two identical speech channels are contained in the COM9046 for full duplex operation. Either channel is capable of performing the scrambling or descrambling function. These functions can be enabled or disabled via an external pin. The on-board oscillator employs an inexpensive 3.58 MHz TV color-burst crystal. Switched capacitor techniques are used to perform analog signal processing in the COM9046.

Typical applications for the COM9046 are Voice Communications, Cellular Phones, Wireless Phones, PBX's, Dictation Machines, Two-way Radios and Audio Recording Equipment.

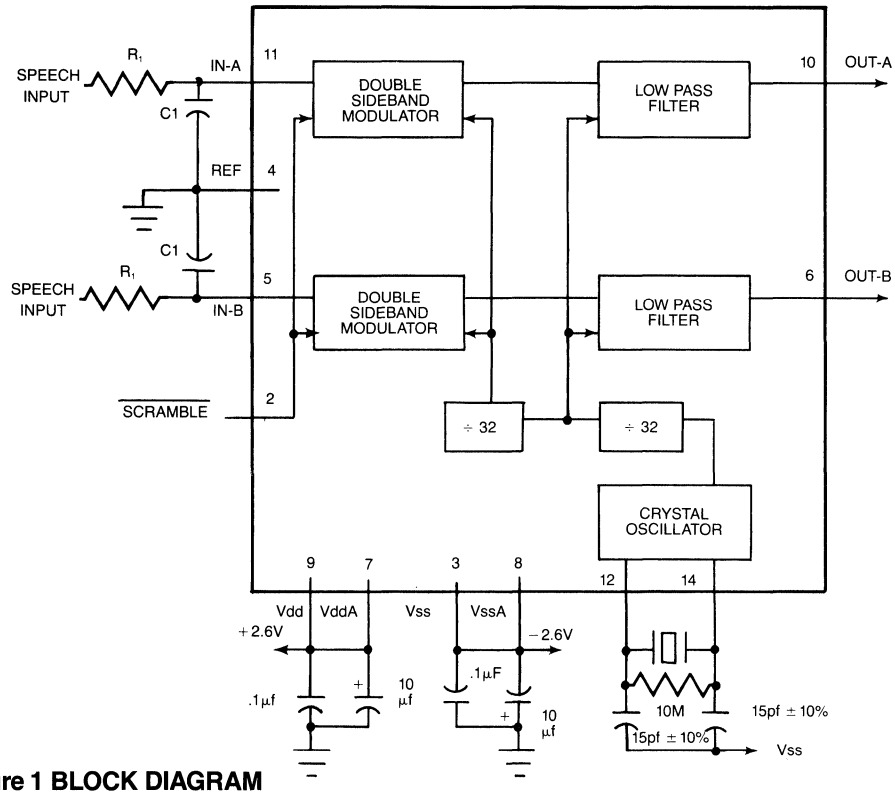


Figure 1 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN #	NAME	SYMBOL	DESCRIPTION
1	N/C		No Connection
2	Scramble	—	Vss applied to this pin asserts the scramble; Vdd asserts non-scramble.
3	Digital Supply	Vss	Negative digital supply. Vss is typically −2.6 volts with respect to pin 4.
4	Ref Input	Ref	Analog ground or mid-supply voltage. This is the chip 0 volt reference.
5	Audio Input B	In-B	Channel B audio input. D.C. voltage must be 0V with respect to pin 4.
6	Audio Output B	Out-B	Channel B audio output. DC voltage is 0V typical with respect to pin 4.
7	Analog Supply	Vdd_A	Positive analog supply. Vdd is typically +2.6 volts with respect to pin 4.
8	Analog Supply	Vss_A	Negative analog supply. Vss_A is typically −2.6 volts with respect to pin 4.
9	Digital Supply	Vdd	Positive digital supply. Vss is typically +2.6 volts with respect to pin 4.
10	Audio Output A	Out-A	Channel A audio output. DC voltage is 0V typical with respect to pin 4.
11	Audio Input A	In-A	Channel B audio input. D.C. voltage must be 0V with respect to pin 4.
12	Crystal input/ Ext Clock	$XTAL_1$	Crystal Oscillator input or external clock. External clock frequency should be 3.58MHz with an amplitude of 4Vp-p and 0VDC.
13	N/C	—	No connection
14	Crystal input	$XTAL_2$	Crystal Oscillator output. This pin is left floating when external clock is applied to pin 12.

OPERATION

Figure 1 shows a block diagram of the chip. Also shown in Figure 1 are the required external components.

Since switched-capacitor filters are used on the chip, the input speech signal must first be filtered by an anti-aliasing one-pole low pass filter before it is applied to the Audio input pin. The filter 3dB break point, which is determined by the product of C1 and R1 plus the output impedance of the audio source, should be less than 20KHz. This filter is required only if high frequency noise is present at the input. To maintain an output signal to noise ratio of 40dB, any unwanted signal higher than 3.5KHz contained in the speech input must be filtered to 40dB below the nominal speech input level, due to the fact that the on-chip modulator is switched at 3.5KHz.

The on-chip double sideband modulator can be turned on or off by asserting the SCRAMBLE input pin. The 3.5KHz switching frequency of the modulator is generated by dividing the output of the oscillator by 1024. The modulator output contains two sidebands centered at the suppressed switching frequency of 3.5KHz. The upper sideband is attenuated by a 4th order Butterworth lowpass filter. The filter, consisting of two biquad switched capacitor filters in cascade, is clocked at 111.9KHz. The inverted input speech spectrum appears at the filter output, and is available at the Audio Output pin. The filter output circuit is designed to drive a maximum capacitive load of 5pf in parallel with a minimum resistance of 15K ohms.

A parallel resonant crystal oscillator is employed in the device. The parallel resonant crystal should have a maximum series resistance of 150 ohms with a shunt capacitance of 5pf. To insure reliable oscillator performance, the components shown connected to XTAL pins 14 and 12 in Figure 1 should be used.

ELECTRICAL CHARACTERISTICS — COM9046

MAXIMUM GUARANTEED RATINGS*:

Operating Temperature Range	−15°C to +55°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any pin with respect to Vss	+6.5 V
Negative Voltage on any pin with respect to Vss	−0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (Ta = −10°C to +50°C, Vdd = Vdd_A = +2.6V ±5%, Vss = Vss_A = −2.6V ±5%.)

Parameter	Min	Typ	Max	Units	Comments
Supply Current		5	8	ma	
Insertion Loss		0	1	db	
Audio Voltage Swing		0.8	1	Vp-p	
S/N Ratio	40			db	
Modulation Frequency		3.5		KHz	
Bandedge of Sideband Filter		3.2		KHz	
Scramble Input High	Vdd-1.0		Vdd	V	
Scramble Logic Low	Vss		Vss+.3	V	
Input Resistance		5		M Ohm	
Dynamic Output Resistance		900		Ohm	
3.5KHz Feedthrough		−60	−50	db	

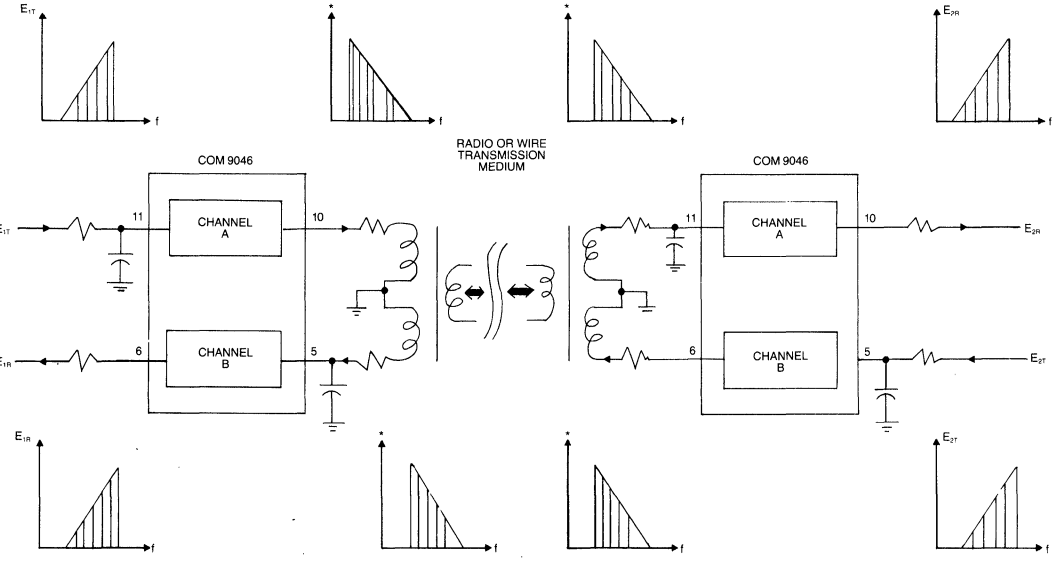
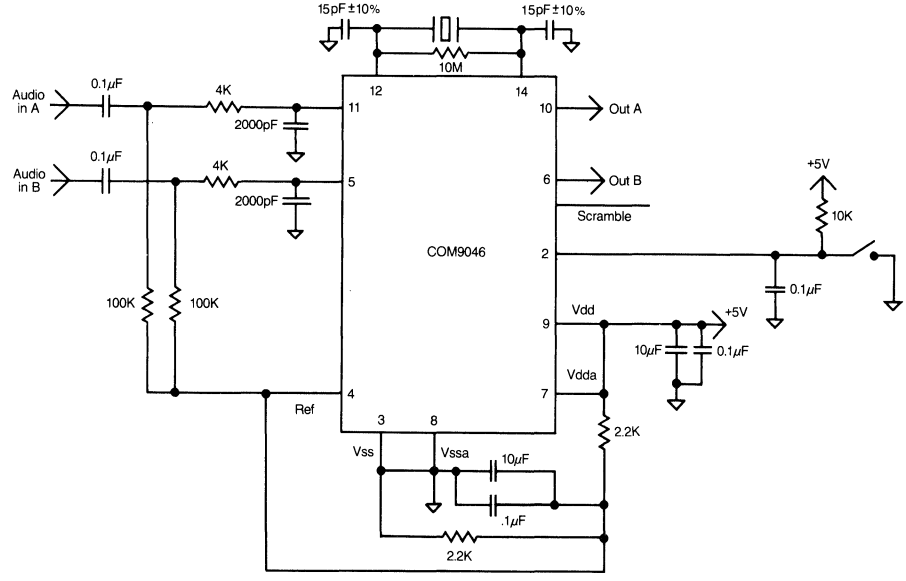


Figure 2 TYPICAL APPLICATION

*Inverted Frequency Spectrum of the Inspect Signals are Transmitted on the Transmission Medium.



RECOMMENDED CONNECTION FOR SINGLE +5V SUPPLY OPERATION

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

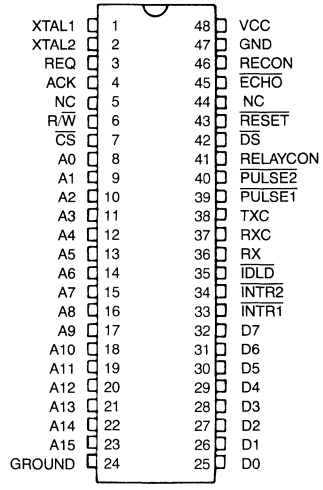
COM90C56
PRELIMINARY

Enhanced Local Area Network Controller ELANC

FEATURES

- ☐ 5.0/2.5 M bit data rates
- ☐ 100% compatible with COM9026 (in slow mode) ARCNET local area network controller
- ☐ 64 K byte shared buffer memory
- ☐ Handles variable length data packets (up to 2 K long)
- ☐ Supports up to 255 nodes per network segment
- ☐ Allows 8/16 bit word per sync to enhance line efficiency
- ☐ Supports event scheduling via buffer descriptors
- ☐ On chip network diagnostics
- ☐ Duplicate ID detection/prevention
- ☐ Supports group broadcast messages
- ☐ Provides the hooks for broadband systems (modem)
- ☐ Internal loopback capability for self test
- ☐ On board oscillator
- ☐ Low power CMOS technology
- ☐ 48 pin D.I.P. plastic package or PLCC
- ☐ Single +5v Supply
- ☐ Compatible with HYC9058, HYC9068, HYC9078
- ☐ RAM buffer test capability

PIN CONFIGURATION*



PACKAGE: 48-pin D.I.P.

*Available in PLCC

Pin configuration subject to change, contact factory for details.

GENERAL DESCRIPTION

The ELANC is a general purpose communications adapter designed to provide high speed intercommunication between a number of intelligent electrical machines. Data is carried over a variable media (twisted pair, coax, or fiber optics) in variable size packets up to 2048 bytes long at speeds of up to 5.0 Mbps. The interconnection of several nodes through their associated ELANCs forms an enhanced local area network. Each node has a unique ID number from 1 to 255 to distinguish it from other nodes on the same network.

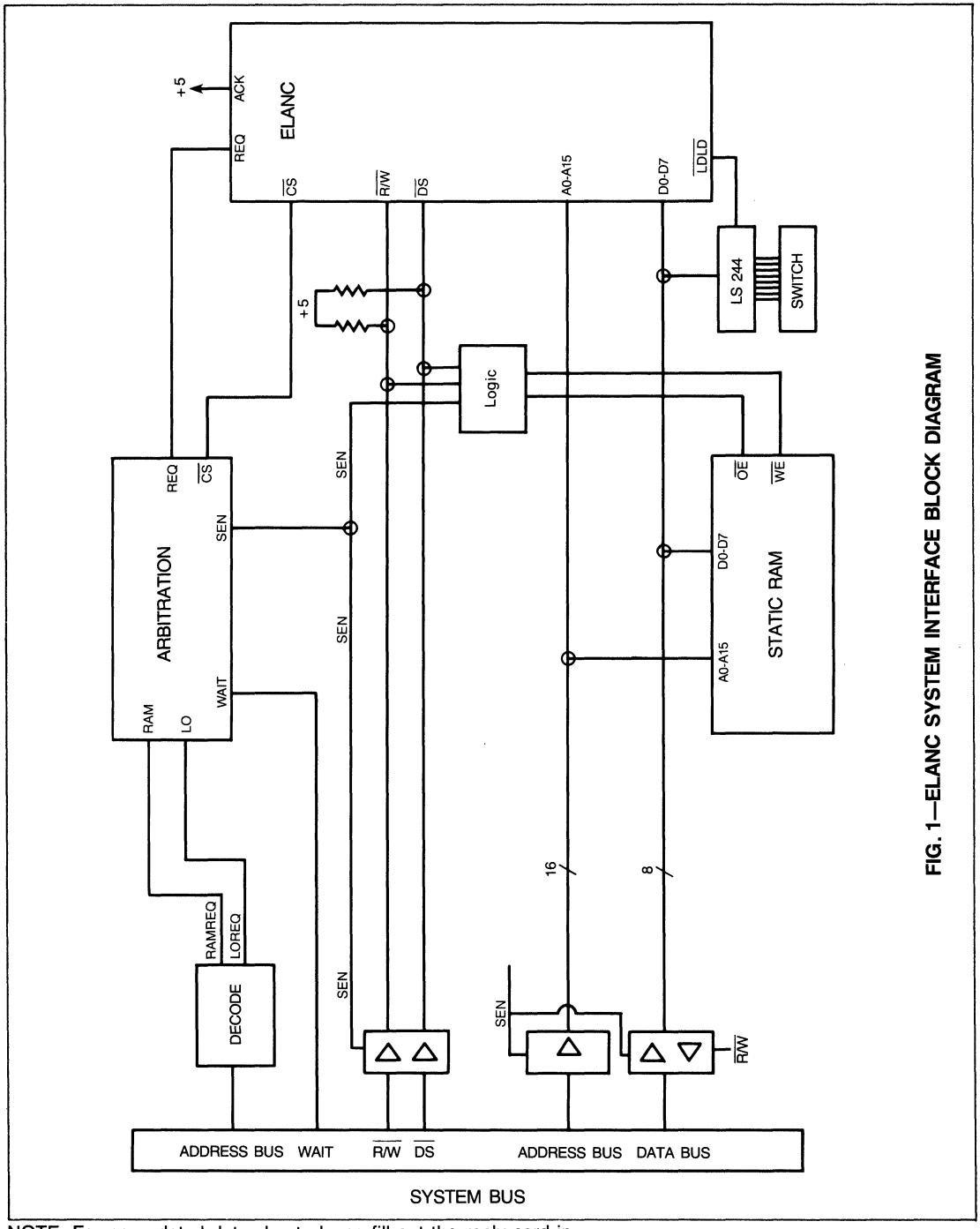


FIG. 1—ELANC SYSTEM INTERFACE BLOCK DIAGRAM

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

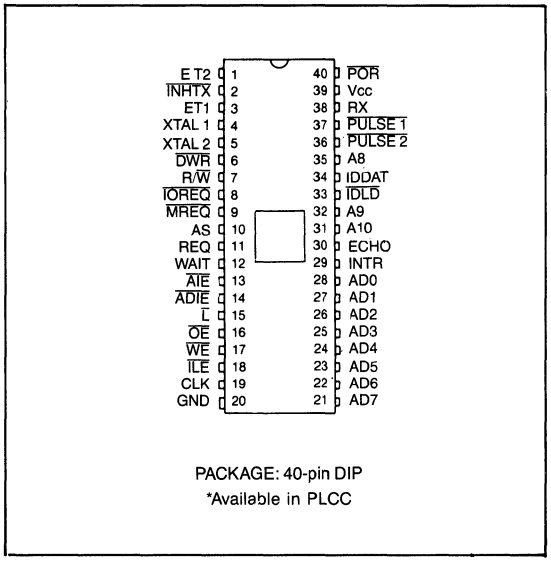
COM 90C62
PRELIMINARY

ARCNET®
Local Area Network Controller/Transceiver
LANC/LANT Combo

FEATURES:

- ☐ ARCNET® LAN Controller/ Transceiver
- ☐ Combines SMC COM90C26/ COM91C32
- ☐ On Board Crystal Oscillator
- ☐ On Board Reset Circuit
- ☐ Compatible with HYC9058 (HIT)
- ☐ Compatible with HYC9068 (LAND)
- ☐ 2.5 MBit Data Rate
- ☐ Modified Token Ring Protocol
- ☐ Self Reconfiguration
- ☐ Variable Data Length Packets
- ☐ 16 Bits CRC Check/Generation
- ☐ Standard Microprocessor Interface
- ☐ Supports Up to 255 Nodes
- ☐ Generate Interrupts Signals
- ☐ Addresses 2k Buffer
- ☐ Arbitrates Buffer Access
- ☐ Replaces Over 100 MSI/SSI Parts
- ☐ Allows Broadcast Messages
- ☐ Compatible with Broadband/Baseband Systems
- ☐ Compatible with various media (Twisted pair, coax...)
- ☐ Compatible with Various Topologies (Star, Tree, Bus...)
- ☐ Low Power CMOS
- ☐ Single +5v Supply

PIN CONFIGURATION



PACKAGE: 40-pin DIP
*Available in PLCC

GENERAL DESCRIPTION

The COM 90C62 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The COM 90C62 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 90C62 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 90C62 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 90C62 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 90C62. The processor can write commands to the COM 90C62 and also read COM 90C62 status. The COM 90C62 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

In addition the COM 90C62 incorporates all the clock generation functions, line drive signals and receive data conversion circuits of the COM 91C32. This high scale integration further reduces ARCNET LAN node chip count, therefore reducing its cost.

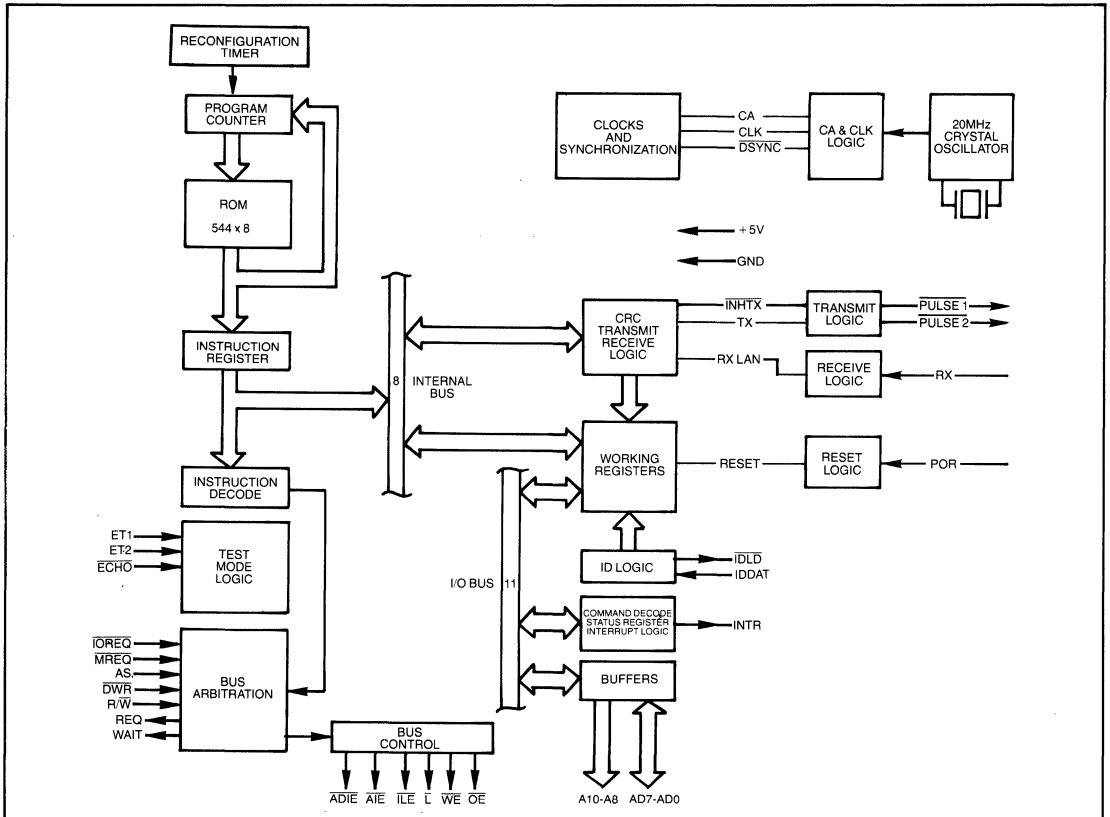


FIGURE 1–COM 90C62 BLOCK DIAGRAM

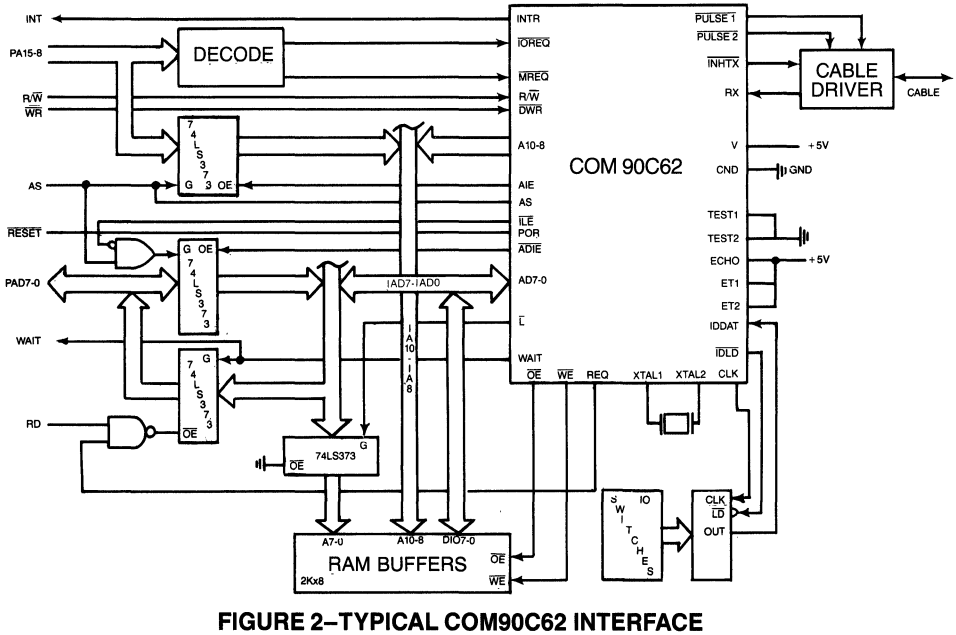


FIGURE 2–TYPICAL COM90C62 INTERFACE

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

DIP PIN NO.	NAME	SYMBOL	FUNCTION
31 32 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 90C62 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes, a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21-28	ADDRESS/DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 90C62. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 90C62.
8	I/O REQUEST	$\overline{\text{IOREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 90C62. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{\text{MREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	A high level on this input signal indicates that the processor's access cycle to the COM 90C62 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 90C62. The write cycle will not be completed, however, until the DWR input is asserted. This signal is an internal transparent latch gated with AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 90C62 to sample the state of the $\overline{\text{IOREQ}}$, MREQ and R/W inputs. The COM 90C62 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{\text{MREQ}}$ or $\overline{\text{IOREQ}}$ passed through an internal transparent latch gated with AS.
12	WAIT	$\overline{\text{WAIT}}$	This output signal is asserted by the COM 90C62 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 90C62 is ready for the processor to complete this cycle.
6	DELAYED WRITE	$\overline{\text{DWR}}$	This input signal informs the COM 90C62 that valid data is present on the processor's data bus for write cycles. The COM 90C62 will remain in the WAIT state until this signal is asserted. $\overline{\text{DWR}}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	INTR	This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{\text{ILE}}$	This output signal, in conjunction with $\overline{\text{ADIE}}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 90C62 operation.
14	ADDRESS DATA INPUT ENABLE	$\overline{\text{ADIE}}$	This output signal enables the processor's address data bus (PAD7-PAD0) captured by AS or ILE onto the interface address data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{\text{AIE}}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	L	This output signal latches the interface address data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{\text{WE}}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{\text{WE}}$.
16	OUTPUT ENABLE	$\overline{\text{OE}}$	This output signal enables the RAM buffer output data onto the interface address data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{\text{IDLD}}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 90C62. The shift register is clocked with the same signal that feeds the COM 90C62 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 2.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2,	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 90C62 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

DIP PIN NO.	NAME	SYMBOL	FUNCTION
2	TRANSMIT INHIBIT	$\overline{\text{INHTX}}$	This active low input inhibits the COM 91C32 from transmitting by forcing $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ high.
37 36	PULSE 1 PULSE 2	$\overline{\text{PULSE1}}$ $\overline{\text{PULSE2}}$	$\overline{\text{PULS1}}$ and $\overline{\text{PULS2}}$ carry the transmit data information encoded in pulse format.
38	RECEIVE IN	RXIN	This input carries the receive data information from the cable interface circuitry.
30	ECHO DIAGNOSTIC ENABLE	ECHO	When this input signal is low, the COM 90C62 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal clip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 90C62 bus cycles, bus arbitration, serial ID input, and the internal timers.
4, 5	CRYSTAL	XTAL1 XTAL2	An external 20 MHz crystal is connected to these pins. If an external 20 MHz TTL clock is used, it should be connected to XTAL1 with a 390 ohm pullup resistor.
40	POWER ON RESET	POR	This input signals clears the COM 90C62 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	Vcc	Power Supply
20	GROUND	GND	Ground

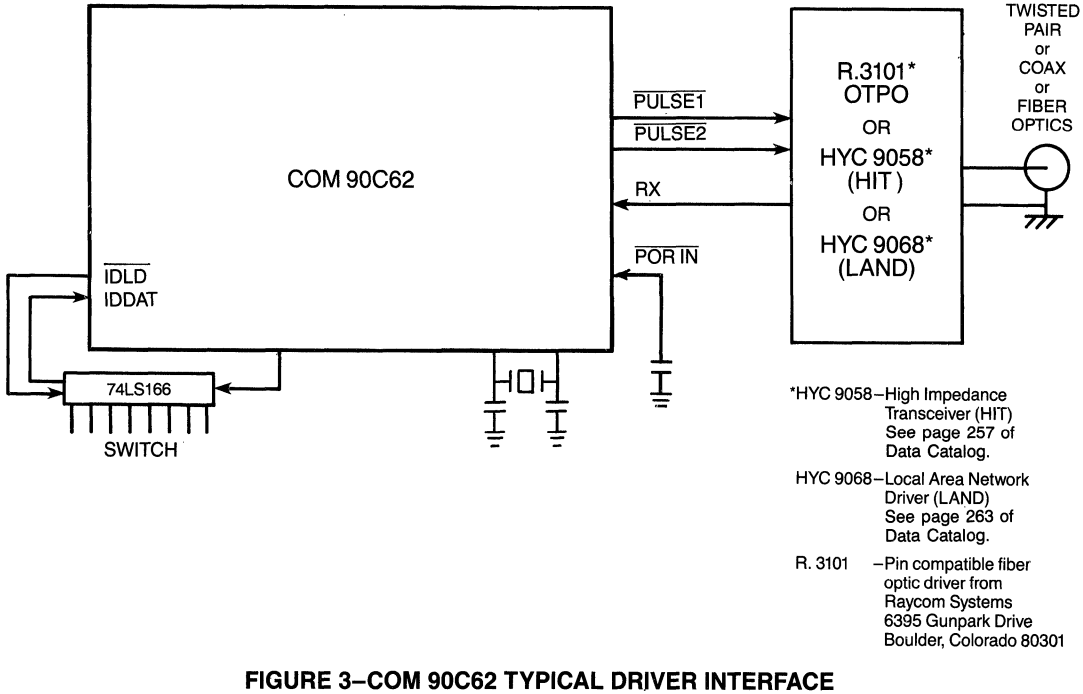


FIGURE 3–COM 90C62 TYPICAL DRIVER INTERFACE

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION

COM 9064
PRELIMINARY

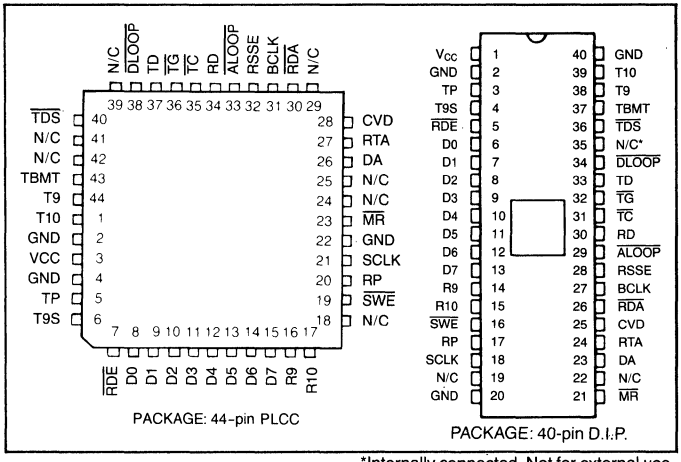
IBM® 3274/3276 Compatible COAX Receiver/Transmitter

SECTION III

FEATURES

- ☐ Conforms to the IBM® 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Single +5 Volt power supply

PIN CONFIGURATION



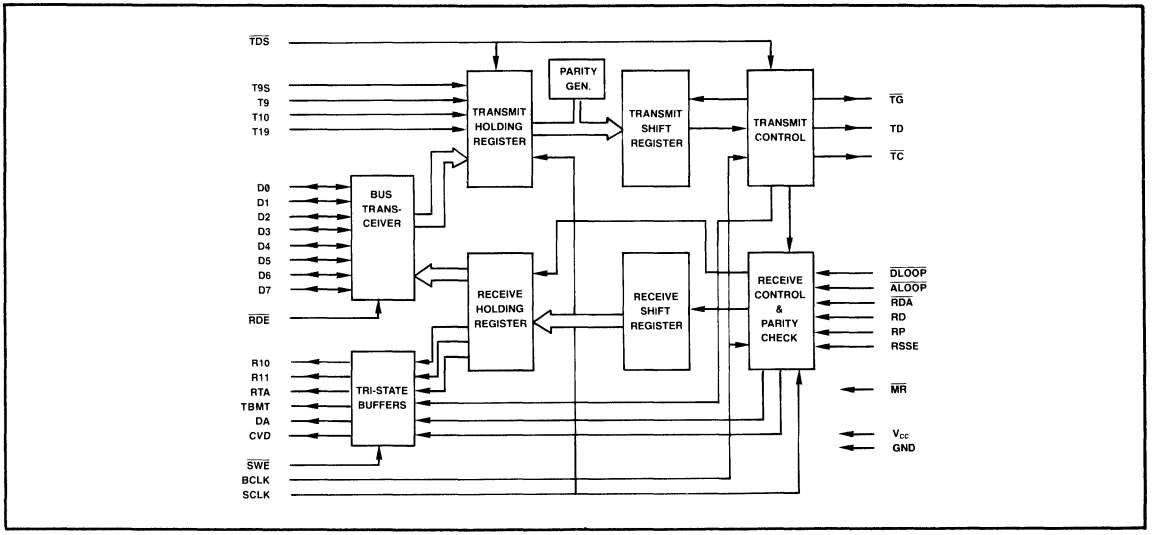
*Internally connected. Not for external use.

GENERAL DESCRIPTION

The COM 9064 is an MOS/LSI circuit which may be used to facilitate high speed data transmission. The COM 9064 is fabricated using SMC's patented COPLAMOS® technology and may be used to implement an interface between IBM® 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. The receiver and transmitter sections of the COM 9064 are separate and may be used independently of each other.

The COM 9064 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit).



ORGANIZATION

The COM 9064 is organized into 9 major sections. Communication between each section is achieved via internal data and control busses.

Transmitter Holding Register

The transmit holding register is a 12 bit latch. This latch is loaded with the transmit data and parity generation information from the system bus.

Tri-State Buffers

These buffers allow gating of the COM 9064's status word onto the system data bus.

Bus Transceiver

The bus transceiver allows bi-directional data transfer between the system data bus and the transmit and receive holding registers.

Parity Generator

This logic determines and generates the correct parity for the data in the transmitter holding register.

Transmitter Control

This logic generates signals required to enable external transmit circuitry. It also generates the Line Quiesce, Code Violation, sync bits and Mini Code Violation patterns.

Transmitter Shift Register

The transmitter shift register is an 11 bit parallel to serial shift register. It accepts data from the transmitter holding register and the parity generation logic and converts it into serial form for transmission.

Receive Control/Parity Check

This logic checks the received character for the specified parity and ensures that no Transmit Check conditions occurred. It also handles the self test mode and generates a strobe when the complete data word is received.

Receiver Shift Register

This logic is a serial to parallel shift register that converts the received information into a 10 bit data word and RTA status bit.

Receiver Holding Register

This register holds the assembled data word until it is read by the processor.

DESCRIPTION OF PIN FUNCTIONS
Processor Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
6-13	Transmit/ Receive Data Bits	D0-D7	Bidirectional: 8 bit, three state data port used to transfer data between the COM 9064 and the processor. D0 is the first bit transmitted.
4	Transmit Bit 9 Select	T9S	Input: A low level on this pin enables T9 to be transmitted as bit 9. A high level on this pin causes T9 to determine the type of parity bit generated for bits D0-D7.
38	Transmit Bit 9	T9	Input: If T9S is low, this supplies transmit bit 9. If T9S is high, then T9 low forces odd parity and T9 high forces even parity to be generated for D0-D7. In this case the parity bit generated is transmit bit 9.
39	Transmit Bit 10	T10	Input: This pin supplies transmit bit 10.
3	Transmit Parity	TP*	Input: This input controls the parity bit for transmit bits 1-10. A low level on this pin causes odd parity and a high level on this pin causes even parity to be generated for bits 1-10. The parity bit generated is transmit bit 11.
18	System Clock	SCLK	Input: This signal is used to synchronize the COM 9064. The transmitter is loaded and started on the low to high transition of SCLK if TDS is low. DA is reset on the low to high transition of SCLK if RDA is low.
36	Transmitter Data Strobe	$\overline{TDS}$	Input: This input and SCLK are used to load the transmitter holding register and start the transmit sequence. Code Violation Detect (CVD) is reset at this time.
26	Reset Data Available	$\overline{RDA}$	Input: This input and SCLK are used to reset DA.
16	Status Word Enable	$\overline{SWE}$	Input: A low level at this pin enables the status word buffer outputs (DA, CVD, TBMT, R9, R10, and RTA). A high level on $\overline{SWE}$ places the status word buffer outputs in a high impedance state.
23	Receive Data Available	DA	This three-state output signal is at a high level when an entire word has been received and transferred into the receiver buffer register. It is only set if a Transmit Check Condition did not occur.
25	Code Violation Detected	CVD	This three-state output signal is at a high level if a valid Code Violation was detected at the receiver since the last time the transmitter was loaded. It is reset when the transmitter is loaded.
37	Transmit Buffer Empty	TBMT	This three-state output signal is at a high level when the transmit holding register may be loaded with new data.
14	Receive Bit 9	R9	This three-state output signal is receiver data bit 9.
15	Receive Bit 10	R10	This three-state output signal is receiver data bit 10.
24	Recever Turn-around	RTA	This three-state output signal is set to a high level when a valid Mini Code Violation is detected. It is only set if a Transmit Check did not occur. It is reset when the transmitter is loaded.
5	Receive Data Enable	$\overline{RDE}$	Input: A low level enables the outputs of the receive data register D0-D7.
17	Receiver Parity	RP*	Input: This input determines whether the entire received word will be checked for even or odd parity. A low at this pin will cause a check for odd parity and a high at this pin will cause a check for even parity. This input has an internal pull-up resistor.

*The SYNC bit is included in parity checking.

DESCRIPTION OF PIN FUNCTIONS (cont.)

PIN NO.	NAME	SYMBOL	FUNCTION
29	Analog Loopback	$\overline{ALOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. A high level on this pin and $\overline{DLOOP}$ will cause the receiver to be disabled while the transmitter is active. $\overline{ALOOP}$ is used to allow loop-back through the line drivers and receivers. This input has an internal pull-up resistor.
34	Digital Loopback	$\overline{DLOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. $\overline{TG}$ is forced to a high level to disable the external coax driver. Data input to the receiver is internally wrapped from the transmitter data output. This input has an internal pull-up resistor.
21	Master Reset	$\overline{MR}$	Input: This input should be pulsed low after power-on. This signal resets DA to a low level and sets $\overline{TG}$ and TBMT to a high level. This input has an internal pull-up.
1	Supply Voltage	V_{cc}	+5 volt supply
19, 22, 35		N/C	No Connection
2, 20, 40	Ground	GND	GROUND

SECTION III

Device Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
27	Baud Rate Clock	BCLK	This input is a clock whose frequency is 8 times the desired transmitter and receiver baud rate (typically 18.8696 MHz for 3274/3276 operation). This input is not TTL compatible.
33	Transmit Data	TD	Output: Serial data from the transmitter. This signal is a biphase Manchester II encoded bit stream. This output is low when no data is being transmitted.
31	Transmit Clock	$\overline{TC}$	The Transmit Clock output is ½ the frequency of BCLK. It is synchronized with TD and used to provide external pre-distortion timing.
30	Receive Data	RD	Input: Accepts the serial biphase Manchester II encoded bit stream.
32	Transmit Gate	$\overline{TG}$	Output: This signal is low during the time that the transmit data is valid. TG is used to turn on the external transmit circuitry.
28	Receive Single Shot Enable	RSSE	Input: A high level on this pin enables an internal digital single shot on RD. This limits a high level on RD to 3 clock times. Also when high it will cause the receiver not to detect a valid Code Violation. A low level disables the single shot causing no reshaping of the RD input signal.

COM 9064 OPERATION

The COM 9064 consists of a receiver section that converts Manchester II phase encoded serial data to parallel data and a transmitter section that converts parallel data to Manchester II phase encoded serial data.

Receiver

Message transfers must conform to the IBM 3270 protocol in order for the COM 9064 to acknowledge them.

The received message is checked for the Code Violation sequence (start sequence) bit pattern, preceding the first data word, and Mini Code Violation (end sequence) following the last data word.

The data word consists of 10 data bits, a sync bit and a parity bit. Receiving data in multiple byte format is functional only when even parity is selected.

The data word along with the first bit of the next word or ending zero (bit 13) is shifted into a shift register. Once it is assembled it is transferred and held in the holding register until another data word is assembled. The 13th bit is inverted and presented to the bus or RTA (receiver turn-around). Therefore RTA is set high on the last word of a message and is reset when the transmitter is loaded with the response.

Once the data word is in the holding register and parity is correct the data available (DA) status signal is set high.

The Code Violation Detect signal (CVD) goes active high after a line Quiesce, Code Violation and sync bit have been detected by the receiver. It is reset when the transmitter of the COM 9064 is asserted. By examining this signal, the processor can determine whether a timeout or Transmit Check condition caused a receiver error.

The receive input is sampled at 8 times the data rate. The receiver logic is brought into bit synchronization during the Line Quiesce pattern. Once the Code Violation following the Line Quiesce is detected, the receiver is brought into bit and word synchronization. The internal receiver clock is adjusted after each transition to compensate for jitter and distortion in the received data signal.

Transmitter

The transmitter section basically consists of a 12-bit holding register, parallel to serial shift register and a parity generator. The firmware initiates a transmit sequence by strobing $\overline{TDS}$ low. The data is loaded into the holding register on the rising edge of SCLK while TDS is low. Nine bits of data (D0-D7 and T10) are transferred without change to the transmit shift register. The logic level of T9S determines whether T9 will be transmitted as parity on the preceding eight bits, or as data.

After the processor loads the transmit holding register with data, status signal TBMT is driven inactive low until the COM 9064 transfers the data from the transmit holding register

to the transmit shift register. After the transfer, TBMT is driven high. The processor should not try to load data into the COM 9064 while TBMT is low. When initiating a data transmission, the COM 9064 automatically transmits a Line Quiesce pattern and a Code Violation. The data is then shifted out of the shift register with a sync bit (1) inserted before the data word, and a parity bit appended after the data word.

If a new word is loaded into the COM 9064 before the parity bit of the previous word has been transmitted, a sync bit (1) followed by the new data bits is transmitted. If not, after the COM 9064 transmits the last data word (no more transmit sequences are started), a sync bit (0) and a Mini Code Violation is appended to the end of the message.

Output $\overline{TG}$ goes active low one-half bit cell time before the first Line Quiesce character is output. It is made inactive (high) during the transmission of the Mini Code Violation.

Diagnostic Modes

NORMAL OPERATION ($\overline{ALOOP}$ AND $\overline{DLOOP}$ HIGH)
Internal read data signal follows the RD input as long as the COM 9064's transmitter is off. The receiver will be disabled while the transmitter is active.

ANALOG LOOPBACK ($\overline{ALOOP}$ LOW AND $\overline{DLOOP}$ HIGH)
The internal read data signal follows the RD input as long as the COM 9064's transmitter is active.

DIGITAL LOOPBACK $\overline{ALOOP}$ HIGH AND $\overline{DLOOP}$ LOW)
The internal read data signal follows an internally generated and latched valid transmit signal (only when the transmitter is active.) The output $\overline{TG}$ is disabled in digital loopback mode.

DISABLE RECEIVER ($\overline{ALOOP}$ AND $\overline{DLOOP}$ LOW)
The internal read data signal is held low and output $\overline{TG}$ is disabled.

MESSAGE FORMATS

Single Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

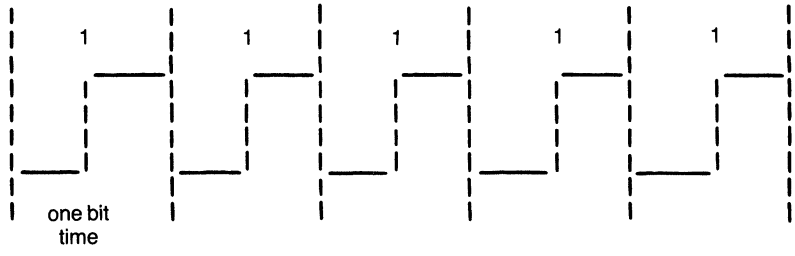
Multiple Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA 1 (10 BITS)	PARITY BIT	SYNC BIT	DATA 2 (10 BITS)

PARITY BIT	.....	SYNC BIT	DATA N (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

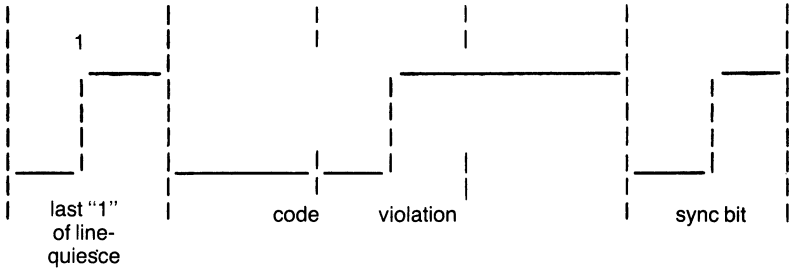
Bits on the coax appear as positive and negative going pulses. A positive pulse to negative pulse transition in the middle of the bit cell is interpreted as a logical '0'. A negative pulse to positive pulse transition in the middle of a bit cell is interpreted as a logical '1'. A predistortion pulse is generated for every pulse transition from an up to down level or a down to up level.

Line Quiesce Pattern



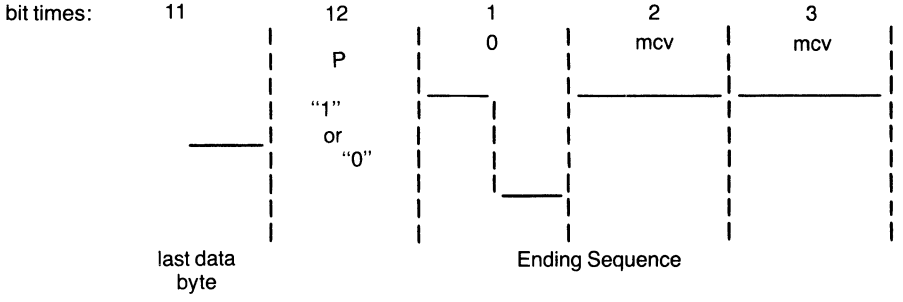
The Line Quiesce pattern consists of five contiguous logical ones. It establishes an equilibrium condition on the coax following line turnaround.

Code Violation Pattern



The Code Violation pattern is a bit sequence containing no mid-bit time level transition in two of its three bit cells. It is a unique pattern that violates the encoding rules and indicates the start of valid data.

Mini Code Violation Pattern



The Mini Code Violation (MCV) pattern is a bit sequence containing no mid-bit time level transition in either of its bit cells. It is a unique code that violates the encoding rules and indicates the end of valid transmit data.

Transmit Check

A Transmit Check is defined as follows:

1) A logical zero sync bit in the ending sequence not followed by a Mini Code Violation.
2) Loss of a level transition at the mid-bit time during other than a normal ending sequence.
3) A transmission parity error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +8.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

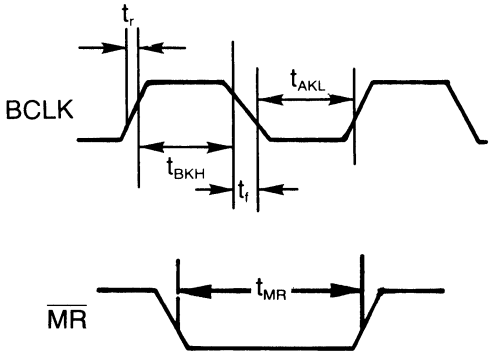
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE					
V_{IL} Low	−0.3		.8	V	
V_{IH} High	2.0		V_{CC}	V	(Except BCLK and $\overline{MR}$)
V_{IH} High	V_{CC}−0.7		V_{CC}+.3	V	(BCLK only)
V_{IH} High	3.5		V_{CC}+.3	V	($\overline{MR}$ only)
OUTPUT VOLTAGE					
V_{OL} Low			.4		I_{OL} = 2.0 mA
V_{OH} High	2.4				I_{OH} = −.25 mA
POWER SUPPLY CURRENT					
I_{CC}		125		mA	All outputs = V_{OH}
INPUT LEAKAGE CURRENT					
All input pins			.01	mA	V_{IN} = 0 to V_{CC}
CAPACITANCE					
C_{IN}			10	pf	(Except BCLK)
C_{IN}			35	pf	(BCLK only)

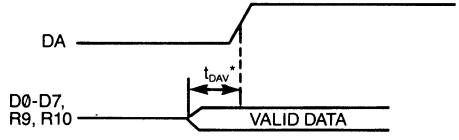
AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER		MIN	TYP	MAX	UNIT	CONDITIONS
Clock Frequency						
B_{CLK}		7	18.8696	18.9	MHz	
S_{CLK}		DC	4.7474	5	MHz	
Clock Width						
t_{SKH}	SCLK High	80			ns	
t_{SKL}	SCLK Low	80			ns	
t_{BKH}	BCLK High	20			ns	
t_{BKL}	BCLK Low	20			ns	
t_r	BCLK rise time			6	ns	
t_F	BCLK fall time			6	ns	
t_{RDD}	$\overline{RDE}$ to Data Valid Delay			50	ns	
t_{SDD}	$\overline{SWE}$ to Data Valid Delay			50	ns	
t_{DF}	Data Read to Bus Float			50	ns	
t_{DS}	Data Setup Time	100			ns	
t_{DH}	Data Hold Time	10			ns	
t_{DAV}	DA to receive data valid delay	−100		100	ns	
t_{TC}	TC clock period		106		ns	
$t_{\overline{TG}LD}$	TC to $\overline{TG}$ low delay	−53		30	ns	
$t_{\overline{TG}HD}$	TC to $\overline{TG}$ high delay			30	ns	
t_{TDS}	Transmit data to TC setup time	10			ns	
t_{TDH}	Transmit data to TC hold time	20			ns	
t_D	TBMT active to de-active		200		ns	
t_{TDDC}	TBMT cycle			3.2	µs	
t_{DD}	$\overline{TBMT}$ de-activated	1		2	µs	
t_{DSS}	$\overline{TDS}$ set up	100		200	ns	
t_{DSH}	$\overline{TDS}$ hold	20		100	ns	
t_{MR}	$\overline{MR}$ pulse width	300			ns	

MISC. TIMING

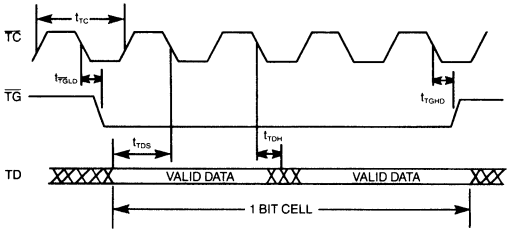


RECEIVE DATA TIMING

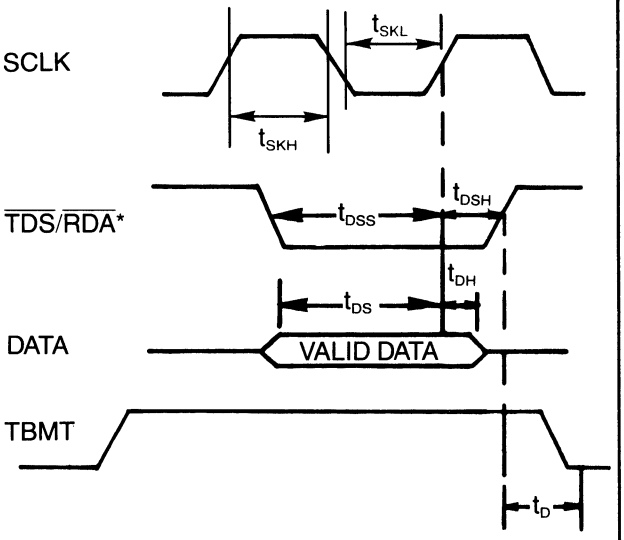


*DA may occur from 100 ns before to 100 ns after data is valid.

TRANSMITTER TIMING

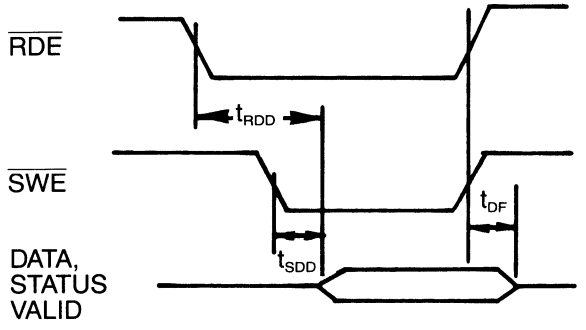


BUS INPUT TIMING

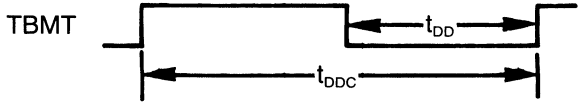


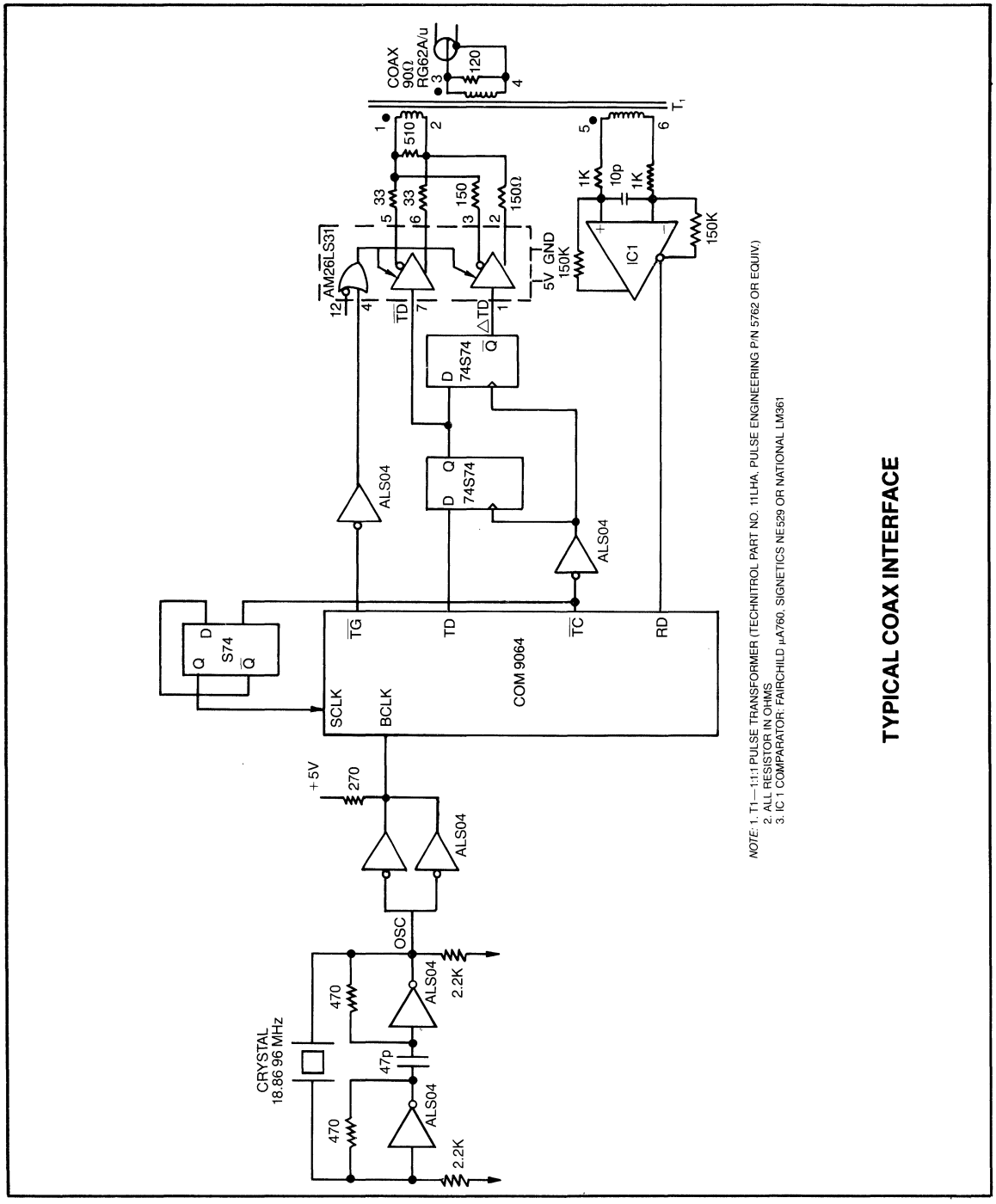
*Only one rising edge of SCLK within this pulse width.

BUS OUTPUT TIMING



TBMT CYCLE





NOTE: 1. T1 — 1:1:1 PULSE TRANSFORMER (TECHNITROL PART NO. 11LHA, PULSE ENGINEERING P/N 5762 OR EQUIV.)
2. ALL RESISTOR IN OHMS
3. IC 1 COMPARATOR: FAIRCHILD μA760, SIGNETICS NE529 OR NATIONAL LM361

TYPICAL COAX INTERFACE

STANDARD MICROSYSTEMS CORPORATION

COM91C32
PRELIMINARY

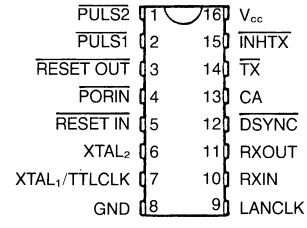
SECTION III

COM91C32
Local Area Network Transceiver
LANT

FEATURES

- ☐ Compatible with the COM9026 and COM90C26 LANCs
- ☐ Compatible with the HYC9058 HIT
- ☐ Compatible with the HYC9068 LAND
- ☐ Functionally compatible with the COM90C32
- ☐ Reduces node chip count
- ☐ Built-in 20MHz crystal oscillator
- ☐ Internal Power On Reset for COM9026/COM90C26
- ☐ Provides all clocks for COM9026/COM90C26
- ☐ Low power CMOS technology
- ☐ TTL compatible
- ☐ 5V only power supply

PIN CONFIGURATION*



*Check with factory for SMT package availability

GENERAL DESCRIPTION

The COM91C32 local area network transceiver (LANT) is an improved version of the COM90C32. It reduces both node cost and board real estate. The COM91C32 is a companion chip to either the COM9026 or COM90C26 local area network controller (LANC), the HYC9068 local area network driver (LAND), and the HYC9058 high impedance transceiver (HIT).

The COM91C32 contains two circuits not available on the COM90C32. A 20MHz crystal oscillator has been built in to eliminate the need for an external oscillator. In addition, the external power on reset circuit required by the COM9026/COM90C26 has been integrated inside the COM91C32 to reduce the number of components, their related costs, and board real estate.

The COM91C32 performs the functions necessary to allow simple interface to the transmission media for ARCNET® local area networks. The COM91C32 produces two 5MHz clocks for the COM9026/COM90C26. The first one (LANCLK) is free running and feeds the clock input (pin 19) of the COM9026/COM90C26. The second one (CA) has start/stop capability controlled by the $\overline{\text{DSYNC}}$ output of the COM9026/COM90C26 as well as the data received from the network.

During data reception, the COM91C32 will convert incoming serial receive data from the HIT or LAND circuit to NRZ form which will directly feed the RX input of the COM9026/COM90C26 (pin 38). During transmission, the COM91C32 converts the transmit data from the COM9026/COM90C26 $\overline{\text{TX}}$, (pin 37) into the waveforms necessary to drive the HYC9058 or HYC9068 as shown in figure 2.

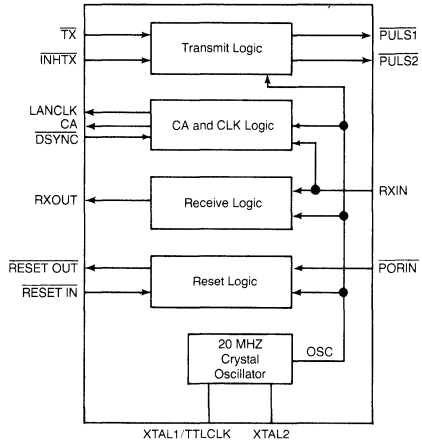


Figure 1: COM91C32 INTERNAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

PIN NO.	NAME	SYMBOL	FUNCTION
COM 9026 Interface			
2 1	PULSE 1 PULSE 2	$\overline{PULS1}$ $\overline{PULS2}$	$\overline{PULS1}$ AND $\overline{PULS2}$ carry the transmit data information encoded in pulse format.
3	RESET OUT	$\overline{RESET\ OUT}$	This output signal provides a reset signal capable of ensuring proper reset of the COM9026/COM90C26. It is TTL compatible. The $\overline{RESETOUT}$ pulse width equals 102.4μsec + ($\overline{RESETIN}$ or $\overline{PORIN}$ pulse width).
10	RECEIVE IN	RXIN	This input carries the receive data information from the cable interface circuitry.
11	RECEIVE OUT	RXOUT	This output provides the NRZ encoded receive data to the COM9026/COM90C26.
12	DELAYED SYNC	$\overline{DSYNC}$	This active low input is asserted by the COM9026 and is used to synchronize the CA clock.
13	CA	CA	This output is a 5 MHz start/stop clock that halts when $\overline{DSYNC}$ goes active. It is used to synchronize the CA clock output to the RX OUT received data.
14	TRANSMIT DATA	$\overline{TX}$	This input represents the serial data transmitted by the COM9026/COM90C26.
15	TRANSMIT INHIBIT	$\overline{INHTX}$	This active low input inhibits the COM91C32 from transmitting by forcing $\overline{PULS1}$ and $\overline{PULS2}$ high.
System Clock Interface			
4	POWER ON RESET IN	$\overline{PORIN}$	This input signal, which is controlled by C_1 (fig. 2) on Power up, disables the transmitter portion of the COM91C32 and generates the $\overline{RESET\ OUT}$ signal. This pin has a schmitt trigger input.
5	RESET IN	$\overline{RESET\ IN}$	This input signal disables the transmitter portion of the COM91C32 and generates the $\overline{RESET\ OUT}$ signal. This pin has a TTL compatible input.
7 6	CRYSTAL	XTAL1 XTAL2	An external 20 MHz crystal is connected to these pins. If an external 20 MHz TTL clock is used, it should be connected to XTAL1 (pin 7) with a 390 ohm pullup resistor; XTAL2 must be left floating.
9	LAN CLOCK	LANCLK	This output supplies a 5 MHz free running clock for the COM9026/COM90C26.
8	GROUND	GND	Ground
16	+5V SUPPLY	VCC	+5 Volt Power Supply

FUNCTIONAL DESCRIPTION

The COM9026/COM90C26, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds to indicate a logic "1" and no pulse to indicate a logic "0." Referring to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to 2, 100 nanosecond nonoverlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ drive the HYC9058 or the HYC9068 which in turn creates a 200 nanosecond dipulse signal on the cable as shown in figure 2.

At the receiving nodes, each dipulse appearing on the cable is coupled through the RF transformer of the HYC9058 or HYC9068 to produce a positive pulse. These pulses are captured by the COM91C32 and are converted to NRZ data. As each byte is received by the COM91C32, the CA clock is stopped by the COM9026/COM90C26 (via $\overline{DSYNC}$) until the zero bit of the next byte is received. This will automatically restart the CA clock. The COM9026/COM90C26 uses the CA clock to sample the NRZ data and these samples points are shown in figure 5.

Typically, RXIN pulses occur at multiples of 400 nanoseconds. The COM91C32 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

RESETTING THE COM91C32

The $\overline{PORIN}$ active low input signal is generated by turning the power on to generate the $\overline{RESET\ OUT}$ signal to the COM9026/COM90C26. The recommended capacitor value (C1 in figure 2) required to properly reset the COM9026/COM90C26 on power up is 0.1 μF.

The $\overline{RESET\ IN}$ active low input signal is provided to generate the $\overline{RESET\ OUT}$ signal used to reset the COM9026/COM90C26. The pulse width of the $\overline{RESET\ OUT}$ signal is 102.4 microseconds, which is wide enough to properly reset the COM9026/COM90C26 local area network controller device.

$\overline{RESET\ OUT}$ = $\overline{RESET\ IN}$ (pulse width) + 102.4 microseconds

$\overline{RESET\ OUT}$ = $\overline{PORIN}$ (pulse width) + 102.4 microseconds

In addition to initializing the COM91C32 to an idle state, the $\overline{RESET\ IN}$ signal disables the transmitter portion of the COM91C32 during reset.

During reset, the COM91C32 output pins are as follows:

$\overline{PULS1}$ - is inactive (high)
$\overline{PULS2}$ - is inactive (high)
LANCLK - is free running during and after reset
CA - is free running during and after reset

The minimum $\overline{RESET\ IN}$ pulse width is 120 nanoseconds (or 2T + 20 nanoseconds for input clocks different than 20 MHz). For the 20 MHz clocks, T equals 50 nanoseconds.

RESET IN/OUT TIMING

The COM91C32 incorporates a digital filter that will suppress glitches on the $\overline{RESET\ IN}$ and $\overline{POR\ IN}$ pins. The digital filter will filter all $\overline{RESET\ IN}$ and $\overline{PORIN}$ glitches that are narrower than 40ns (1T-10ns). It will allow $\overline{RESET\ IN}$ and $\overline{POR\ IN}$ pulses that are wider than 120 ns (2T+20ns). The $\overline{RESET\ OUT}$ pulse width is equal to the $\overline{RESET\ IN}$ pulse width plus 102.4 microseconds.

THE INTERNAL OSCILLATOR

The COM91C32 incorporates on-board circuitry which, in conjunction with an external parallel resonant crystal, forms an oscillator. The oscillator frequency may vary between 8 MHz and 20 MHz to allow for a variable data rate from 1.0 Mbps to 2.5 Mbps.

The oscillator input is divided by 4 to produce the CA and the LANCLK output clocks to the COM9026/COM90C26.

The COM91C32 XTAL oscillator has been designed to work with a parallel resonant crystal and does not require an external resistor. Only two capacitors are needed (one from each leg of the XTAL to ground.) The values of the capacitors are two times the load capacitance of the crystal. Typical capacitor values are 22 pF.

The external crystal must have an accuracy of 0.020% or better.

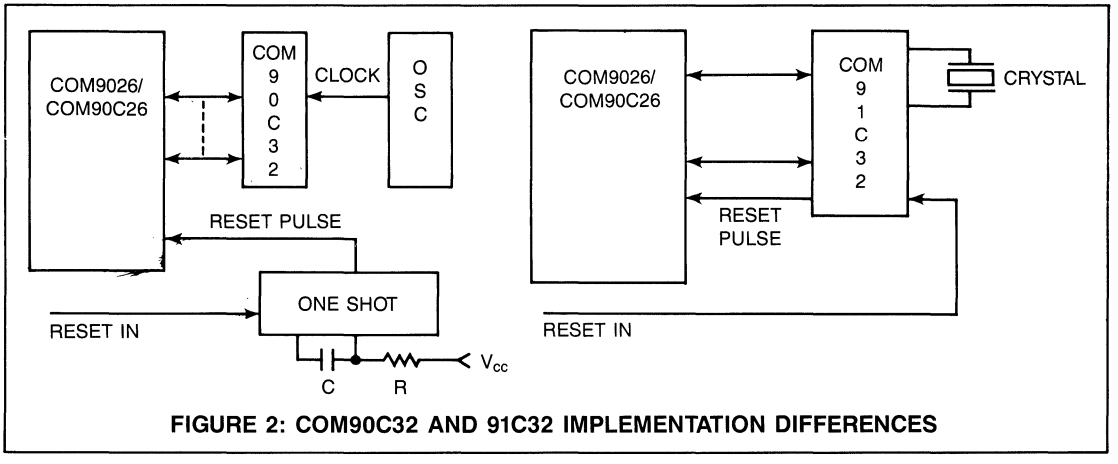


FIGURE 2: COM90C32 AND 91C32 IMPLEMENTATION DIFFERENCES

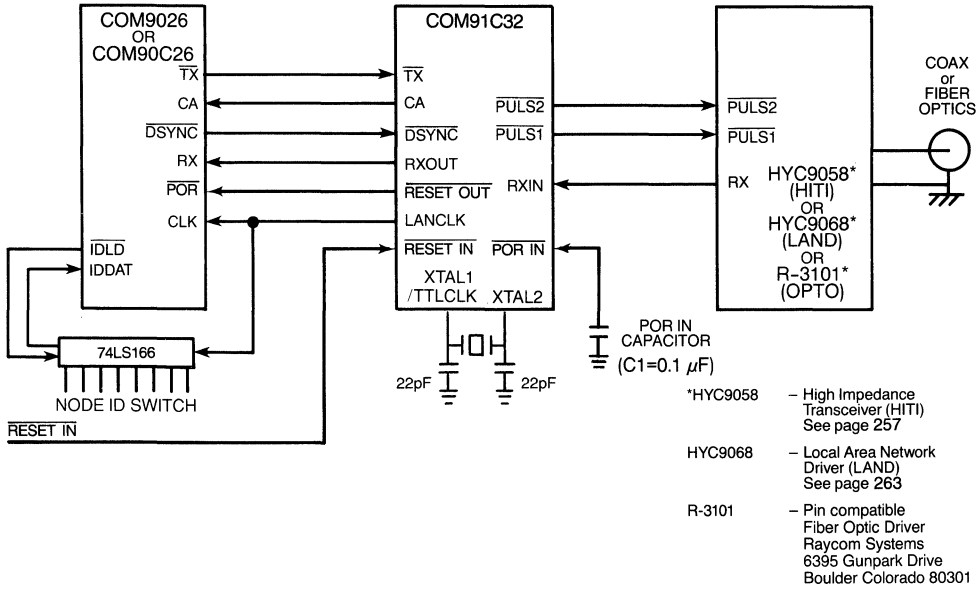


FIGURE 3: COM91C32 SYSTEM INTERFACE

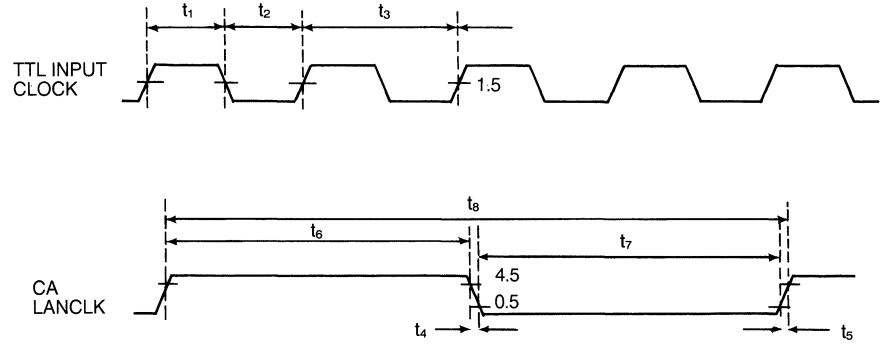


FIGURE 4: COM91C32 CLOCK TIMING

TABLE 1 - COM91C32 ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (soldering, 10 sec.)	325°C
Positive Voltage on any Pin	V_{cc} + 0.3
Negative Voltage on any Pin	-0.3V
Maximum V_{cc}	+ 7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{cc} =5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGES					
V_{IH1} High Input Voltage	2.7			V	except for TTL CLK and $\overline{PORIN}$
V_{IL1} Low Input Voltage			0.8	V	
V_{IH2} High Input Voltage	V_{cc}-0.5V			V	for TTL CLK IN
V_{IL2} Low Input Voltage			1	V	
V_{IH3} High Input Voltage	3.6			V	for $\overline{PORIN}$
V_{IL3} Low Input Voltage			1.0	V	
OUTPUT VOLTAGES					
V_{OH1} High Output Voltage	V_{cc}-1.0			V	IOH = 400 μA except for CA, LANCLK
V_{OL1} Low Output Voltage			0.4	V	IOL = 4.0 mA except for CA, LANCLK
V_{OH2} High Output Voltage	V_{cc}-0.5			V	IOH = 100 μA for CA, LANCLK
V_{OL2} Low Output Voltage			0.4	V	IOL = 100 μA for CA, LANCLK
INPUT LEAKAGE CURRENT					
IL		±10		μA	
INPUT CAPACITANCE					
C_{IN}			15	pF	
POWER SUPPLY CURRENT					
I_{cc}			20	mA	

AC CHARACTERISTICS (T_a = 0°C to +70°C, V_{cc} =5V ± 5%)

FIG NO.	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
	TTL CLOCK INPUT TIMING					
Fig. 3	t_1 Input Clock High Time	20			ns	@ V_{cc}-0.5V
	t_2 Input Clock Low Time	20			ns	@ 1V
	t_3 Input Clock Period		50		ns	
	CA, LANCLK OUTPUT TIMING					
Fig. 3	t_4 Clock Out Fall Time			20	ns	@ 50 pF max
	t_5 Clock Out Rise Time			20	ns	@ 50 pF max
	t_6 Clock Out High Time	75			ns	@ 50 pF max
	t_7 Clock Out Low Time	75			ns	@ 50 pF max
	t_8 Clock Out Period		200		ns	@ 50 pF max
	TRANSMIT TIMING					
Fig. 4	t_9 TX Setup to CA falling edge	50			ns	
	t_{10} TX Hold after CA falling edge	10			ns	
	t_{11} Xtal rising edge to $\overline{PULS1/2}$		60		ns	
	t_{12} $\overline{PULS1/2}$ Pulse Width		2 (t_3)		ns	
	t_{13} $\overline{INHTX}$ to Pulse inactive			100	ns	
	RECEIVE TIMING					
Fig. 5	t_{15} RXIN Pulse Width	10			ns	
	t_{16} RXIN to RXOUT delay		5 (t_3) + 70		ns	
	t_{17} RXOUT Pulse Width		400		ns	
	t_{18} XTAL RISING EDGE TO RXOUT			70	ns	
	$\overline{DSYNC}$, CA TIMING					
Fig. 5	t_{19} $\overline{DSYNC}$ Setup to CA rising edge		20		ns	
	RESET TIMING					
Fig. 6	t_{30} $\overline{RESET\ IN}$ Pulse Width	120			ns	(NOTE 1)
	t_{31} $\overline{RESET\ IN}$ falling edge to $\overline{RESET\ OUT}$ falling edge			170	ns	(NOTE 2)
	t_{32} $\overline{RESET\ IN}$ rising edge to $\overline{RESET\ OUT}$ rising edge	102	102.4	103	us	
	t_{33} $\overline{RESET\ OUT}$ Pulse Width		$t_{30}+t_{32}-2t_3$			
	INPUT CLOCK FREQUENCY	8.0		20	MHz	

NOTE 1: For Input clock frequencies of less than 20 MHz, $t_{30} = 2t_3 + 20$ ns
NOTE 2: For Input clock frequencies of less than 20 MHz, $t_{31} = 2t_3 = 70$ ns

*ALL TYPICAL VALUES ARE AT V_{cc} = 5.0 V and TEMPERATURE = 25°C

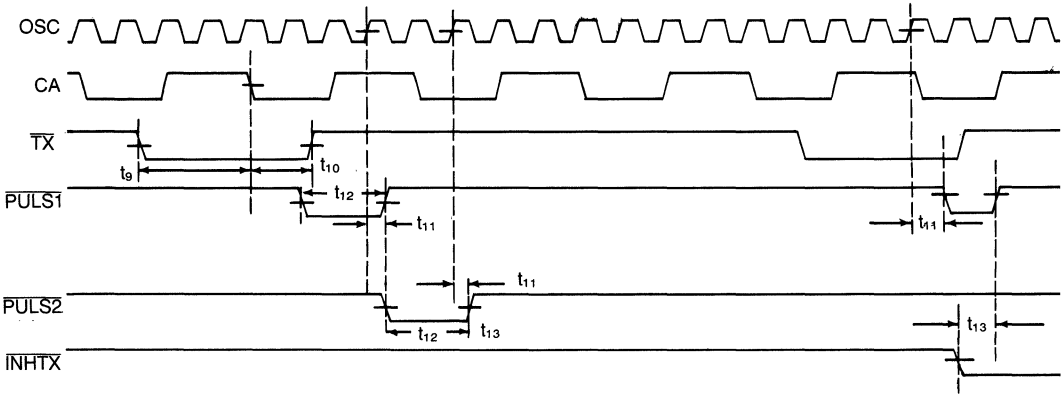


FIGURE 5: TRANSMIT TIMING PARAMETERS

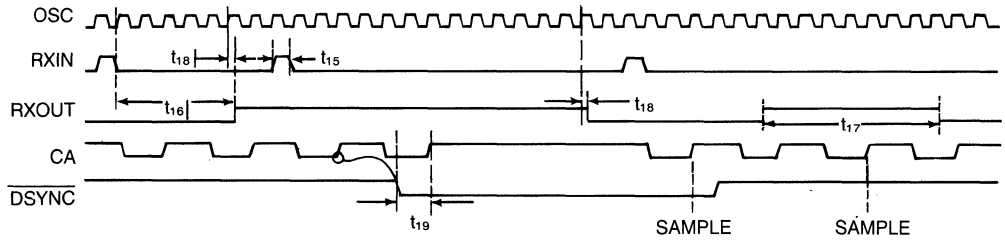


FIGURE 6: RECEIVE TIMING PARAMETERS

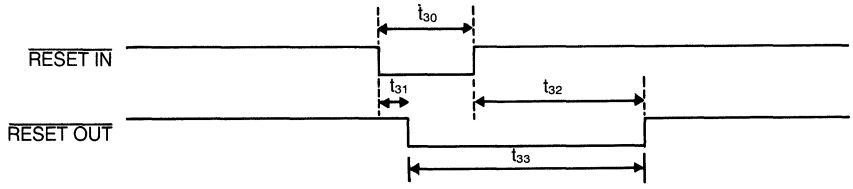


FIGURE 7: RESET IN - TO - RESET OUT TIMING

STANDARD MICROSYSTEMS CORPORATION

COM92C32
ADVANCED INFORMATION
PRELIMINARY

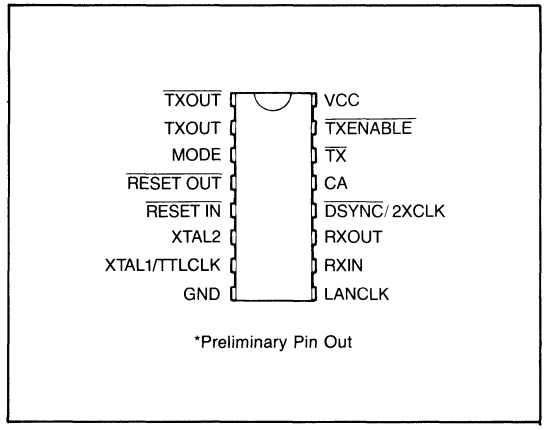
SECTION III

Enhanced Local Area Network Transceiver

FEATURES

- ☐ Compatible with the COM9026 and COM90C26 ARCNET®/LAN controllers
- ☐ Compatible with COM90C56 Enhanced LAN Controller
- ☐ Converts transmit data to NRZ or Manchester format
- ☐ Converts receive Manchester II data to NRZ format
- ☐ High performance DPLL for high bit jitter tolerance
- ☐ Receiver blanking circuit for ignoring line reflections, ringing and inductive effects
- ☐ Compatible with HYC 9078
- ☐ On board predistortion circuitry
- ☐ On board crystal oscillator simplifies clock generation
- ☐ CLK/CA clock generation for the COM9026 and COM90C26
- ☐ 5V only power supply
- ☐ Compatible with RS-422/RS485 Transceivers
- ☐ Low power CMOS
- ☐ Modem control signals
- ☐ 16 pin DIP and PLCC packages

PIN CONFIGURATION



*Preliminary Pin Out

GENERAL DESCRIPTION

The COM92C32 is a companion chip to the COM9026 and COM90C26 Local Area Network Controllers (LANC). It contains all the necessary logic to interface the COM9026 and COM90C26 to baseband or broadband Local Area Networks. It is also compatible with the COM90C56 Enhanced LANC.

During data transmission, the COM92C32 converts the pulsed TX data signal from the COM9026 and COM90C26 to NRZ (Non Returned to Zero) format for Broadband networks, and to Differential Manchester format for baseband networks. It also generates a TX ENABLE signal to enable the media driver circuitry during data transmission.

The use of Manchester encoded data allows bus topologies in the order of 20 nodes and 2000 feet on coaxial cables without active repeaters. In addition, the COM92C32 can be used with discrete RS422/485 drivers to implement the physical layer of the ARCNET® local area network over telephone grade twisted pair media.

When receiving data, the COM92C32 samples and recovers the incoming receive data and presents it synchronously to either the COM9026, COM90C26 or COM90C56. It also performs the necessary handshake and generation of the Bit Clock (CA) for the COM9026 and COM90C26.

The chip incorporates a 25 MHz internal oscillator which simplifies clock generation.

ARCNET® is a registered trademark of the Datapoint Corporation

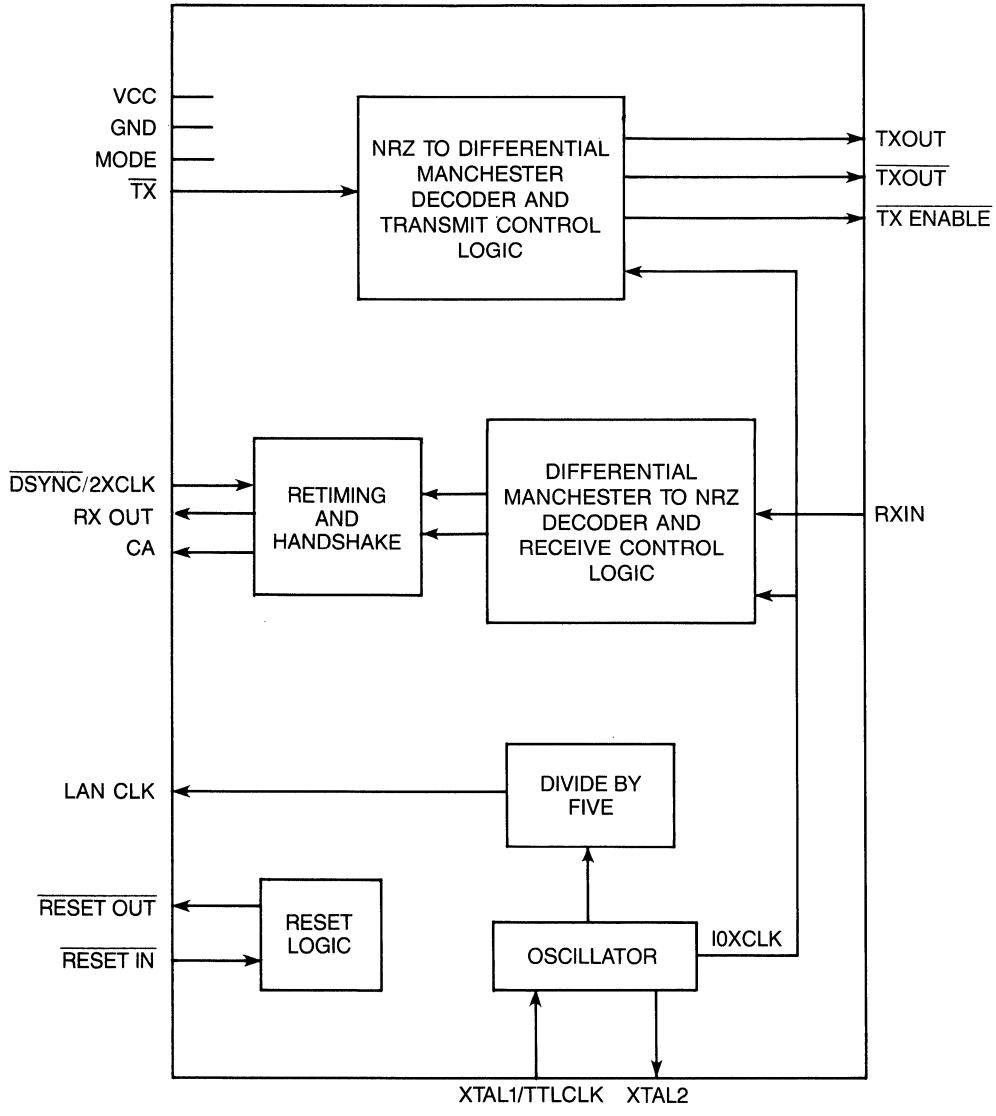


FIG. 1 - COM92C32 INTERNAL BLOCK DIAGRAM

TABLE 1 - COM92C32 DESCRIPTION OF PIN FUNCTIONS

PIN NO	SYMBOL	I/O	NAME AND FUNCTION
	TXOUT	O	TRANSMIT OUT—This output signal carries the transmitted serial data encoded in either differential Manchester format or NRZ format. In the Manchester mode of operation, this pin will idle high when the COM92C32 is not transmitting. In the NRZ mode, this pin will idle low when the COM902C32 is not transmitting.
	$\overline{\text{TXOUT}}$	O	TRANSMIT OUT—This output signal carries the transmitted serial data encoded in either differential Manchester format or NRZ format. In the Manchester mode of operation, this pin will idle high when the COM92C32 is not transmitting. In the NRZ mode, this pin will idle low when the COM92C32 is not transmitting.
	$\overline{\text{TXENABLE}}$	O	TRANSMIT ENABLE—This output signal is active low when the transmitted data on TXOUT and $\overline{\text{TXOUT}}$ is valid. It is used to enable the external media driver circuitry.
	$\overline{\text{TX}}$	I	TRANSMIT DATA—This input represents the serial data transmitted by either the COM9026 or COM90C26.
	$\overline{\text{DSYNC}}$/ 2XCLK	I	$\overline{\text{DSYNC}}$—This active low input is asserted by the COM9026 or COM90C26 and is used to synchronize the CA clock output of the COM92C32 to the received data. When the COM92C32 is used with the COM90C56 ELANC chip, this pin becomes the 2XCLK signal from the ELANC.
	CA	O	BIT CLOCK—This output is a 5 MHz start/stop clock that halts when $\overline{\text{DSYNC}}$ goes active. $\overline{\text{DSYNC}}$ is used to synchronize the CA clock output to the RX OUT received data.
	LANCLK	O	LAN CLOCK—This output supplies a 5 MHz free running clock for the COM9026 or COM90C26, pin 19. It is capable of driving 50pF plus one LS/TTL load with 20ns rise and fall times.
	RXOUT	O	RECEIVE DATA OUT—This output provides the NRZ encoded receive data to the COM9026 and COM90C26. This output is synchronous to the CA clock.
	RXIN	I	RECEIVE DATA IN—This input receives data from the cable interface circuitry.
	XTAL1/TTLCLK XTAL2	I	CRYSTAL—An external 25 MHz crystal is connected to these pins. If an external 25 MHz TTL clock is used, it should be connected to the XTAL1 with a 390 ohm pullup resistor; XTAL2 must be left floating.
	$\overline{\text{RESET IN}}$	I	RESET—This signal resets the COM92C32 to a known state. In addition, it disables the transmitter and generates the $\overline{\text{RESET OUT}}$ signal to the COM9026 and COM90C26.
	$\overline{\text{RESET OUT}}$	O	RESET OUT—This output signal provides a 102.4μs Reset signal to the COM9026 and COM90C26.
	MODE	I	MODE SELECT—This pin is used to select the mode of operation of the COM92C32. The three possible modes are: 1) Vcc - Differential Manchester with COM9026 or COM90C26. 2) GND - NRZ Mode with COM9026 and COM90C26. 3) $\overline{\text{RESET OUT}}$ - Differential Manchester with COM90C56 (ELANC).
	Vcc	—	+5 Volt Power Supply
	GND	—	Ground

*Pin numbers to be determined

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

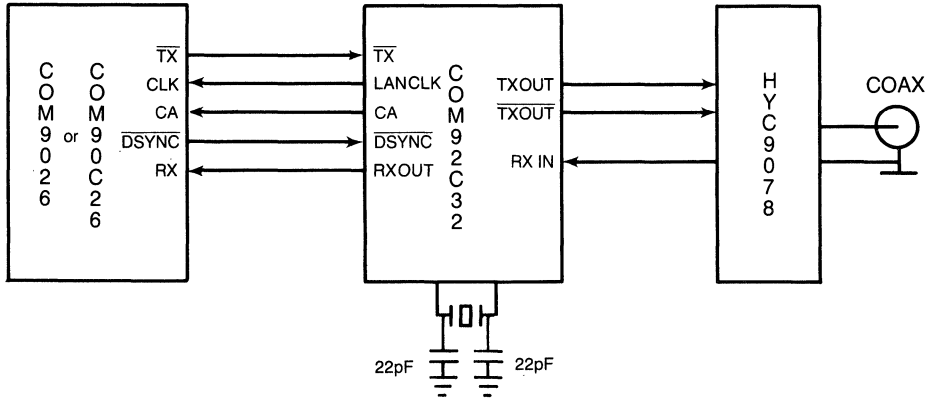


FIG. 2 - COM92C32 TO COAX SYSTEM INTERFACE

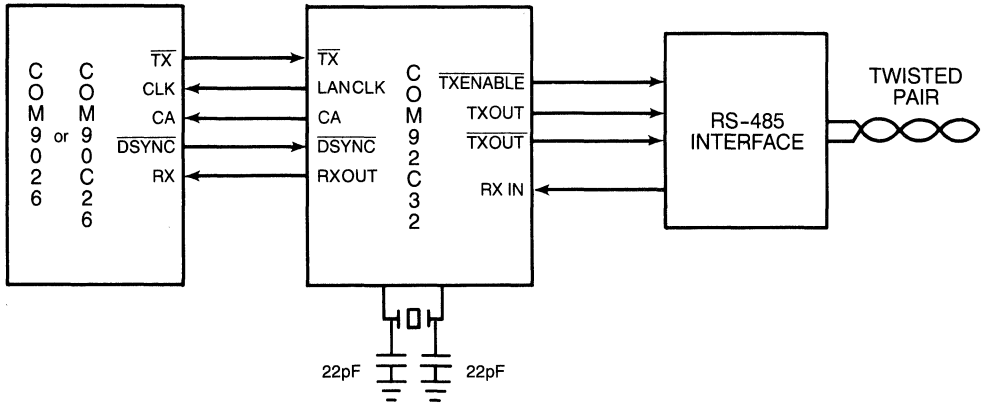


FIG. 3 - COM92C32 TO TWISTED PAIR SYSTEM INTERFACE

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

HYC9058
PRELIMINARY

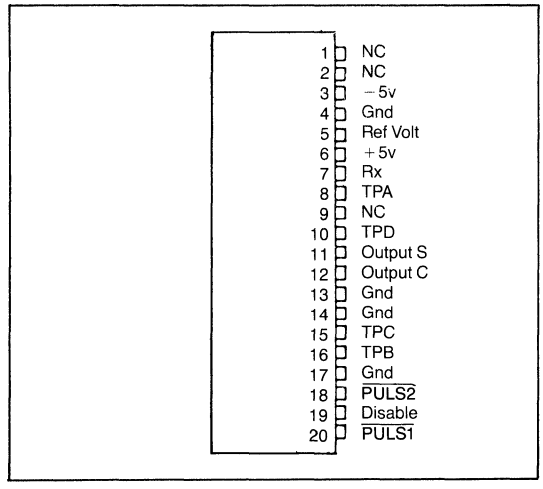
SECTION III

ARCNET® High Impedance Transceiver HIT™

FEATURES

- ☐ Compatible with existing ARCNET® installations
- ☐ Compatible with ARCNET® coax drivers
- ☐ Pin Compatible with ARCNET® fiber-optic drivers
- ☐ Enables Bus topology on ARCNET® LAN's
- ☐ Provides network expansion without any additional repeaters or major rewiring
- ☐ Multi-media drive capability
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity

PIN CONFIGURATION



GENERAL DESCRIPTION

The High Impedance Transceiver (HIT) provides ARCNET® LAN's designers with a new bus configuration option, while reducing hardware and installation costs. The HIT offers ARCNET® LAN's with the ability to provide the highest node performance/cost ratio available heretofore. The bus topology and the reduced need for HUB's (active repeaters) eliminate the excessive costs usually associated with installing a new LAN or modifying an existing one.

The HIT is compatible with SMC monolithic LAN controller chip set the COM9026/COM90C26 and the COM90C32. However it can work with other controllers and its inherent high output impedance enables it to drive several types of media cables.

The HIT is easily incorporated into existing ARCNET® LAN's. The HIT is pin-compatible with other media drivers, like the COAX driver currently used in most ARCNET® baseband applications and the fiber optic driver manufactured by Raycom Systems.

The HIT contains all the necessary filtering to guarantee noise-immunity for interference-free data transfers at 2.5 Mbps.

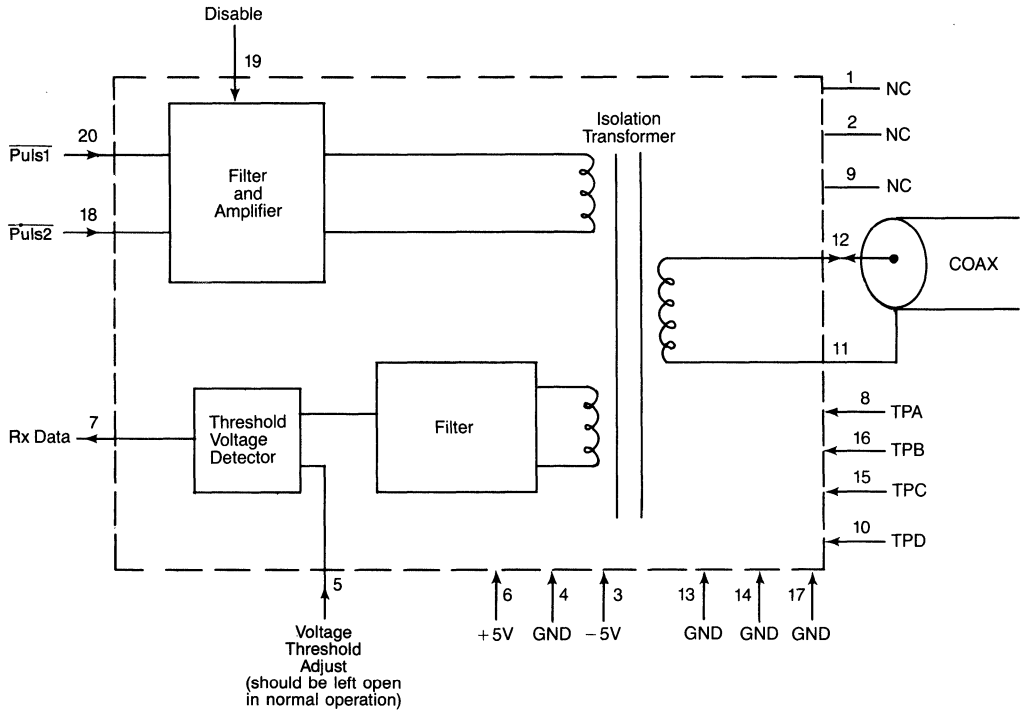


Figure 1—HIT Block Diagram

DESCRIPTION OF PIN FUNCTIONS

PIN #	NAME	SYMBOL	FUNCTION
1, 2, 9	—	NC	Not used. No connection.
3	Power Supply	VDD	−5 Volts Power Supply.
4, 13, 14, 17	Ground	GND	Ground
5	Threshold Voltage	REF V	Internal Set Reference Voltage can be used to adjust Internal Voltage Detector Threshold in Special Situations. Normally, this pin should not be connected.
6	Power Supply	VCC	+5 Volt Power Supply.
7	Received Data Output	RX	Received Data, goes to RXIN of COM90C32 (TTL).
8, 10, 15, 16	Test Points	TPA, TPB TPD, TPC	Test Points. Make no connection to these pins.
11	COAX I/O	OUTPUT S	Connect to Coax Cable Shield (Outer Conductor). Bypass to GND is recommended.
12	COAX I/O	OUTPUT C	Connect to Coax Cable Inner Conductor (Center)
18	Pulse 2	$\overline{\text{PULS2}}$	TTL Level Input to the Transmitter Section (Active Low).
19	Disable	Disable	Normally connected to ground a high disables the transmitting.
20	Pulse 1	$\overline{\text{PULS1}}$	TTL Level Input to the Transmitter Section (Active Low).

FUNCTIONAL DESCRIPTION

The HIT integrates a host of discrete components onto a hybrid microcircuit to provide the Local Area Network design with space and cost reductions as well as the enhanced reliability of a single component.

Transmit section:

Referring to the block diagram of figure 1, Pulse 1 and Pulse 2 signals can be TTL pulses of 100 nsec each with Pulse 2 delayed by 100 nsec. The optimum timing for these signals can be obtained from SMC's COM90C32. Amplification and filtering is used to eliminate undesirable frequencies from the signals, while providing them with the necessary drive, before transmitting onto the line through an isolation transformer. The driving circuitry has been designed to present a very high impedance to the line for minimum loading. The transformer typical voltage output is 20 volts peak to peak. In most applications, it is recommended that the shield of the coaxial cable be bypassed to ground by a parallel R-C combination.

Receive section:

The received dipulse signal from the line is DC isolated by the transformer. It is filtered to reduce noise, voltage transients and intersymbol interference. It is then recovered by a threshold voltage detector. The minimum signal amplitude necessary for reliable operation is 6 volts peak to peak. The TTL Rx Data output is then sent to the receive input of the COM90C32. A voltage threshold pin can be used to vary the threshold voltage for special situations.

In normal operation, the "disable" at pin 19 should be tied to ground. However, in certain cases, this pin can be used to prevent transmission.

APPLICATION INFORMATION

The hit is designed to eliminate the need for Hubs in small (8 nodes) installations extending up to 1000 feet as shown in figure 2. However the number of nodes is inversely proportional to the bus length.

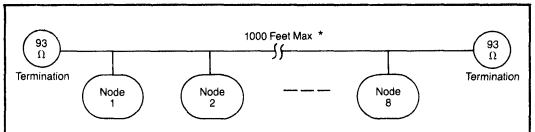


Figure 2—Typical Small Hubless Network

*HYC 9058

Figures 3 and 4 show alternative ARCNET® local area network implementation using the "LAND" and the HIT. As can be easily observed the straight forward approach of the HIT version results in very low per node cost as well as ease of installation.

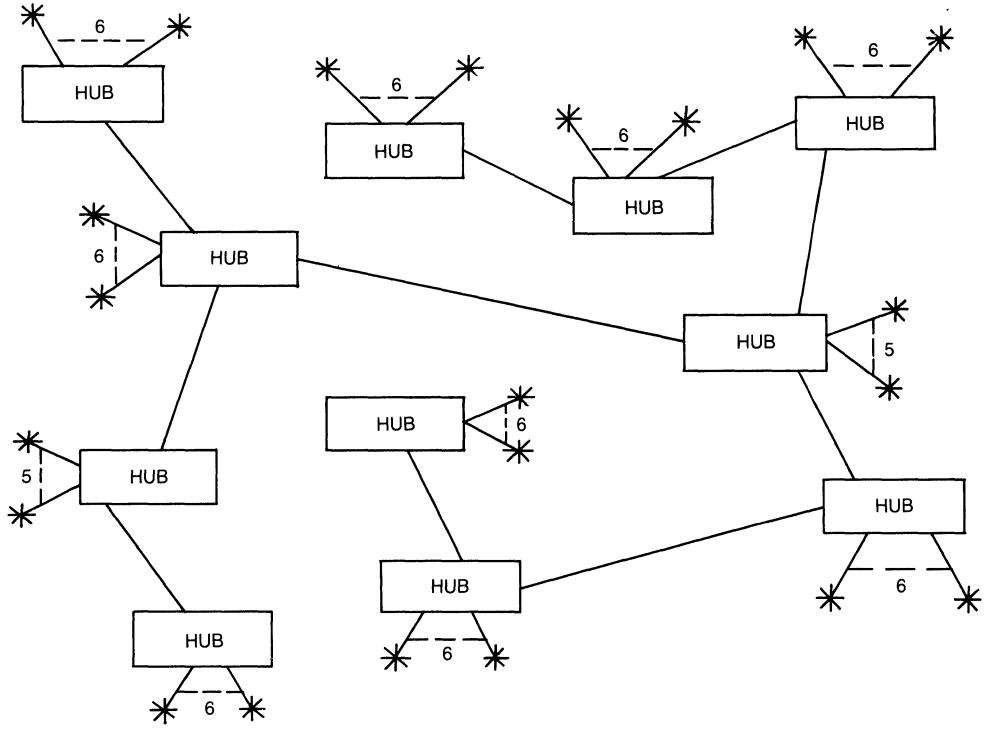


Figure 3—Typical 64 Node Network Using HUBs and LANDs

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*:

Operating Temperature Range ..... 0 C to +70 C
Storage Temperature Range ..... −40 C to +125 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any pin with respect to Gnd ..... 8 V
Negative Voltage on any pin except Vdd with respect to Gnd ..... −0.3 V

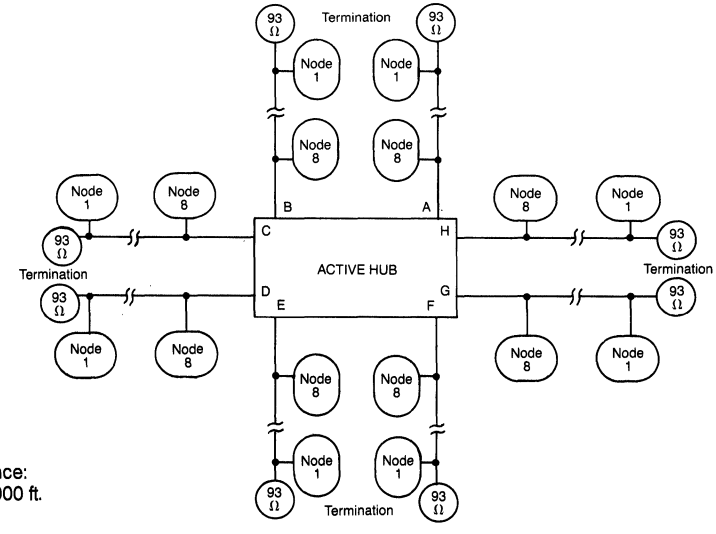
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

Electrical Characteristics Ta = 0 to 70 C, Vcc = +5V ±5%, Vdd = −5V ±5%.

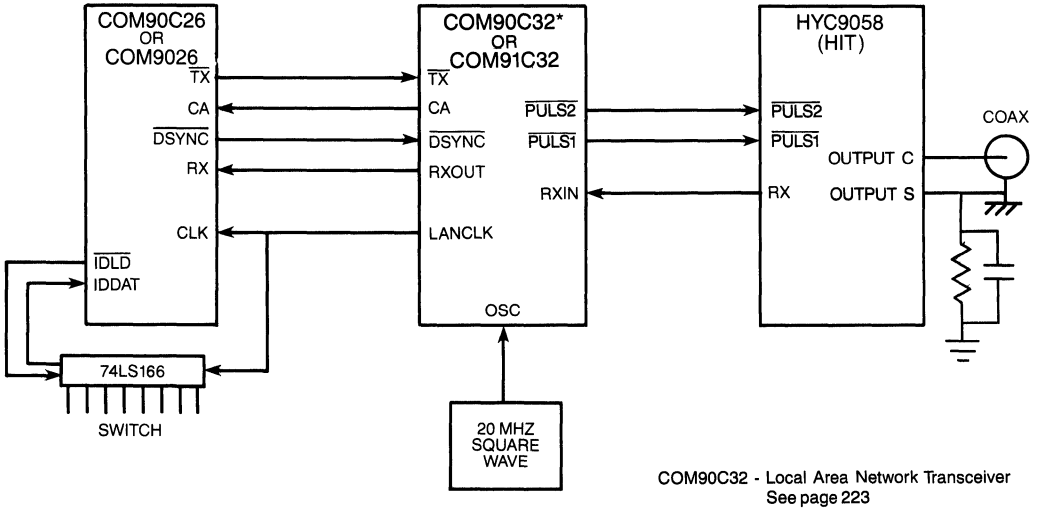
Parameter	Min.	Typ.	Max	Unit	Comments
INPUT VOLTAGE LEVELS					
Pulse 1, 2, DSBL inputs					
Low-level, VIL			0.8	V	Iil = −.8ma
High-level, VIH	2.0			V	Iih = .2ma
Received signal amplitude	6			Vp-p	
OUTPUT VOLTAGE LEVELS					
Rx Data output					
Low-level, VOL			0.4	V	One TTL load
High-level, VOH	2.4			V	One TTL load
Transformer output	16			Vp-p	HYC 9058
POWER SUPPLY CURRENT					
Icc		190	285	mA	
Idd		180	270	mA	
PULSE WIDTH					
Pulse 1, 2 inputs		100		nsec	

Shorting the transformer output can cause permanent damage to the device.



Maximum Distance:
HYC 9058: 1000 ft.

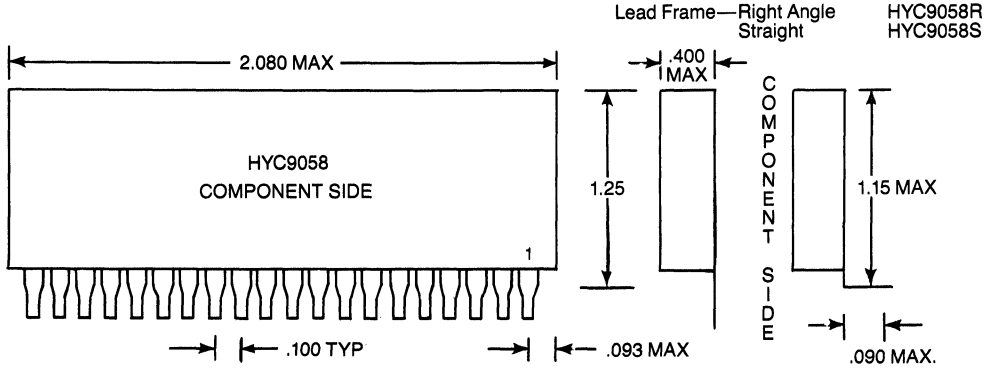
Figure 4—Typical 64 Node Network Using HIT



COM90C32 - Local Area Network Transceiver
See page 223

COM91C32 - Improved Local Area Network Transceiver
See page 247

Figure 5—HYC9058 System Interface



Mechanical Specification

ARCNET® is a registered trademark of the Datapoint Corporation

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8698

STANDARD MICROSYSTEMS CORPORATION

HYC9068
PRELIMINARY

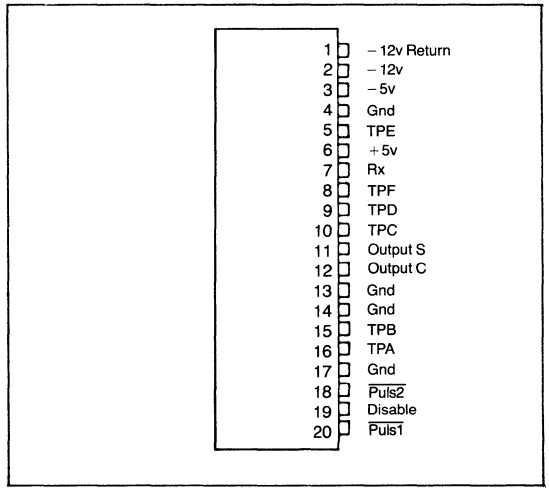
SECTION III

ARCNET® Local Area Network Driver LAND™

FEATURES

- ☐ Compatible with existing ARCNET® installations
- ☐ Compatible with ARCNET® coax drivers
- ☐ Pin Compatible with ARCNET® fiber-optic drivers
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity
- ☐ Drives up to 2,000 ft. of Coax
- ☐ Replaces more than 25 discrete components and IC's

PIN CONFIGURATION



GENERAL DESCRIPTION

The HYC9068 is a Coax Driver for ARCNET Local Area Networks. The HYC9068 is compatible with SMC's COM9026/COM90C26 Local Area Network Controller (LANC) and the COM90C32 Local Area Network Transceiver (LANT). The HYC9068 simplifies network implementation while providing considerable space and cost savings plus the high reliability of a single component.

The HYC9068 contains both receive and transmit filters to guarantee interference-free data transfer over 2,000 ft. of RG-62 coaxial cable at 2.5 Mbps data rate.

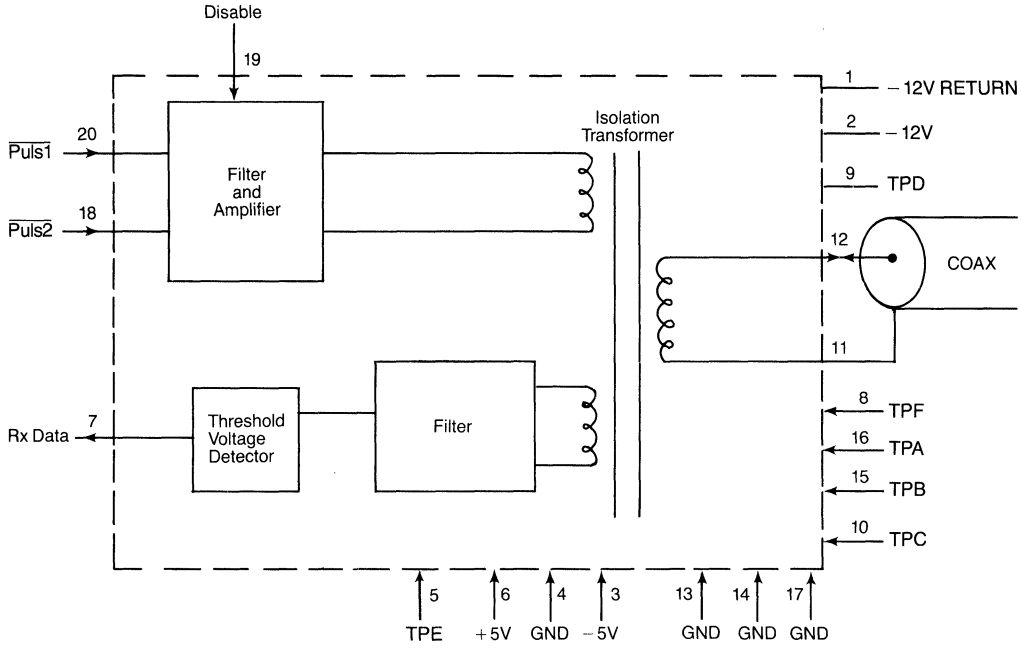


FIGURE 1—HYC9068-LAND BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN #	NAME	SYMBOL	FUNCTION
1	-12V Return	GND	-12V Return
2	Power Supply	Vss	-12V Power Supply
3	Power Supply	VDD	-5 Volts Power Supply.
4, 13, 14, 17	Ground	GND	Ground
6	Power Supply	VCC	+5 Volt Power Supply.
7	Received Data Output	RX	Received Data, goes to RXIN of COM90C32 (TTL).
8, 10, 15, 16, 5, 9	Test Points	TPA, TPB, TPE TPD, TPC, TPF	Test Points. Make no connection to these pins.
11	COAX I/O	OUTPUT S	Connect to Coax Cable Shield (Outer Conductor). Bypass to GND is recommended.
12	COAX I/O	OUTPUT C	Connect to Coax Cable Inner Conductor (Center).
18	Pulse 2	$\overline{\text{PULS2}}$	TTL Level Input to the Transmitter Section (Active Low).
19	Disable	Disable	Normally connected to ground a high disables the transmitting.
20	Pulse 1	$\overline{\text{PULS1}}$	TTL Level Input to the Transmitter Section (Active Low).

FUNCTIONAL DESCRIPTION

When using the optional −12V supply, Pin 3 must not be connected. Pin 1 must be grounded and −12V must be applied to Pin 2.

The easiest way to create the optimum input is to use the SMC COM90C32 to provide $\overline{\text{PULS1}}$ and $\overline{\text{PULS2}}$. The DISABLE (Pin 19) should be grounded during normal operation.

In order to inhibit surge damage as well as limit spurious radiation, it is suggested that the shield of the COAXIAL CABLE be bypassed to ground by a parallel R-C Network (0.005 μFd/1Kv in parallel with two 5.6K ohm/½W resistors in series) as shown in typical interconnect diagram.

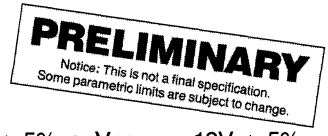
ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*:

Operating Temperature Range ..... 0 C to + 70 C
Storage Temperature Range..... − 40 C to + 125 C
Lead Temperature (soldering, 10 sec.) ..... + 325 C
Positive Voltage on any pin with respect to Gnd ..... 8 V
Negative Voltage on any pin except Vdd and Vss with respect to Gnd ..... − 0.3 V

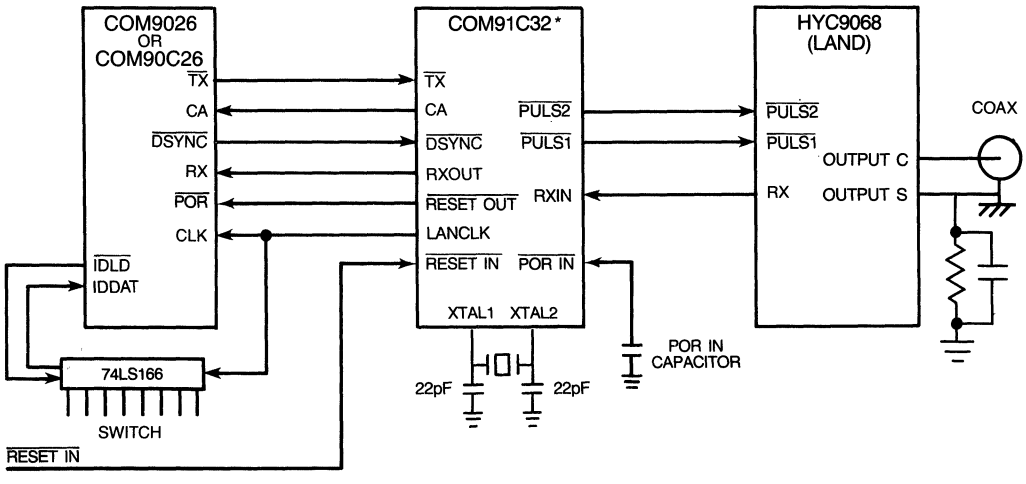
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.



Electrical Characteristics Ta = 0 to 70 C, Vcc = + 5V ± 5%, Vdd = −5V ± 5%, or Vss = −12V ± 5%

Parameter	Min.	Typ.	Max	Unit	Comments
INPUT VOLTAGE LEVELS					
Pulse 1, 2, DSBL inputs					
Low-level, VIL			0.8	V	Iil = −.8ma
High-level, VIH	2.0			V	Iih = .2ma
Received signal amplitude	6			Vp-p	
OUTPUT VOLTAGE LEVELS					
Rx Data output					
Low-level, VOL			0.4	V	One TTL load
High-Level, VOH	2.4			V	One TTL load
Transformer output	15.4	20		Vp-p	
Cable noise amplitude			4	Vp-p	
POWER SUPPLY CURRENT					
Icc			250	mA	
Idd			20	mA	
Iss			50	mA	
PULSE WIDTH					
Pulse 1, 2 inputs		100		nsec	
COAXIAL CABLE					
Type RG-62 (93Ω)			2,000	ft	



* COM90C32 —Local Area Network Transceiver is also compatible with the COM9026 or COM90C26 and HYC9068.

FIGURE 2—TYPICAL HYC9068 INTERCONNECT

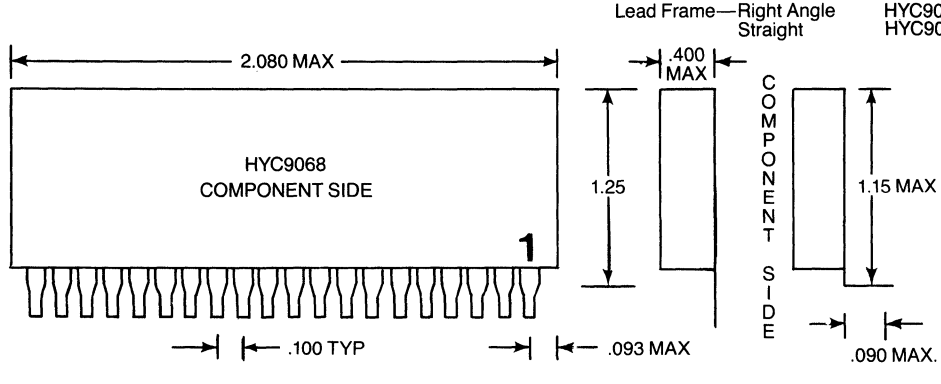


FIGURE 3—MECHANICAL SPECIFICATION

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

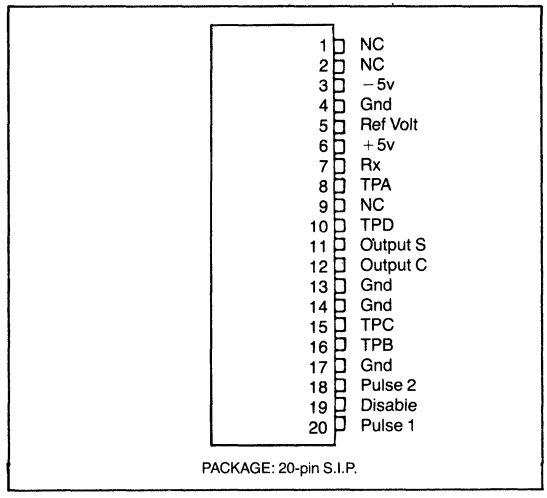
HYC9078
PRELIMINARY

High Impedance Transceiver HIT™ 2

FEATURES

- ☐ Compatible with SMC's COM9056 Enhanced Local Area Network Controller (ELANC)
- ☐ 5 MHz operation
- ☐ High impedance
- ☐ Enables Bus topology on LAN's
- ☐ Provides network expansion without any additional repeaters or major rewiring
- ☐ Multi-media drive capability
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity
- ☐ Common mode isolation
- ☐ Wide dynamic range
- ☐ Very low level receiver sensitivity

PIN CONFIGURATION



PACKAGE: 20-pin S.I.P.

GENERAL DESCRIPTION

The HIT2 is a new media interface hybrid which works with the ELANC in the new high speed 5Mbps mode of signalling. The HIT2 will be available in a 20pin SIP hybrid package.

The HIT2 has been tuned to operate with the ELANC's high speed mode and includes a specially designed receive circuit to receive data in the manchester signalling scheme without introducing a significant amount of bit jitter. The HIT2 also includes a transmit signal amplifier and high frequency filter so that it generates clean signals that are free from high order harmonics that might cause EMI problems. Both the transmit section and receive circuit are transformer coupled to the output and have both been designed with very high input impedances which allow the HIT2 to be used in bus topologies. Additionally, the large dynamic range of the HIT2 provides very relaxed cabling restrictions.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

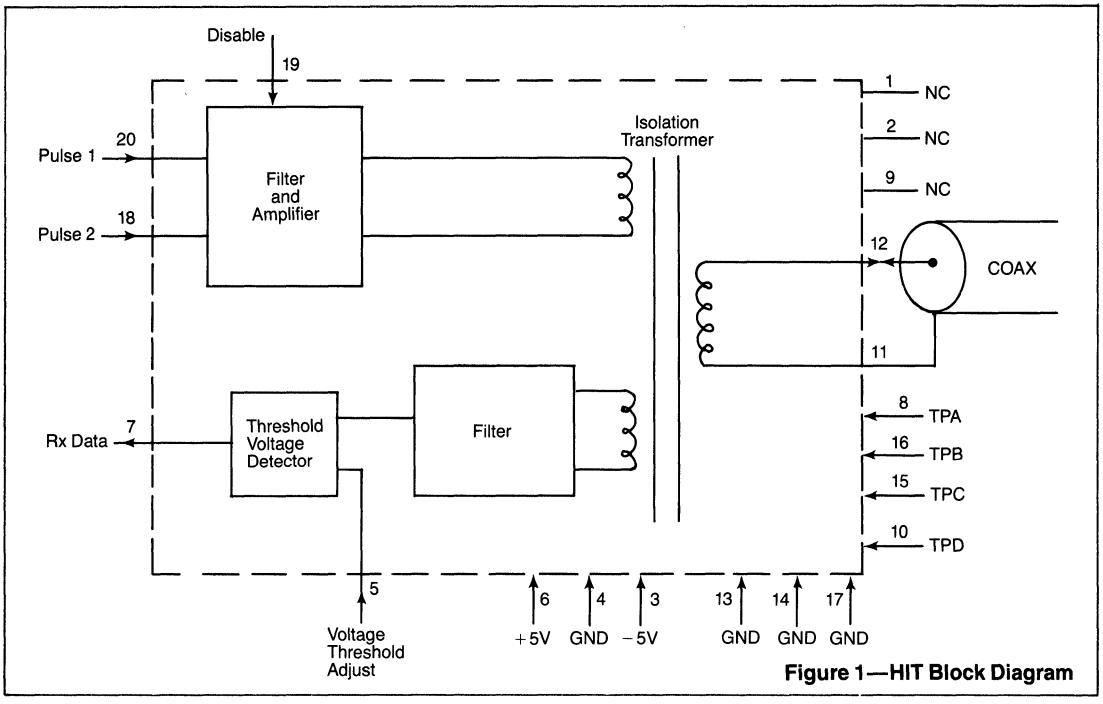
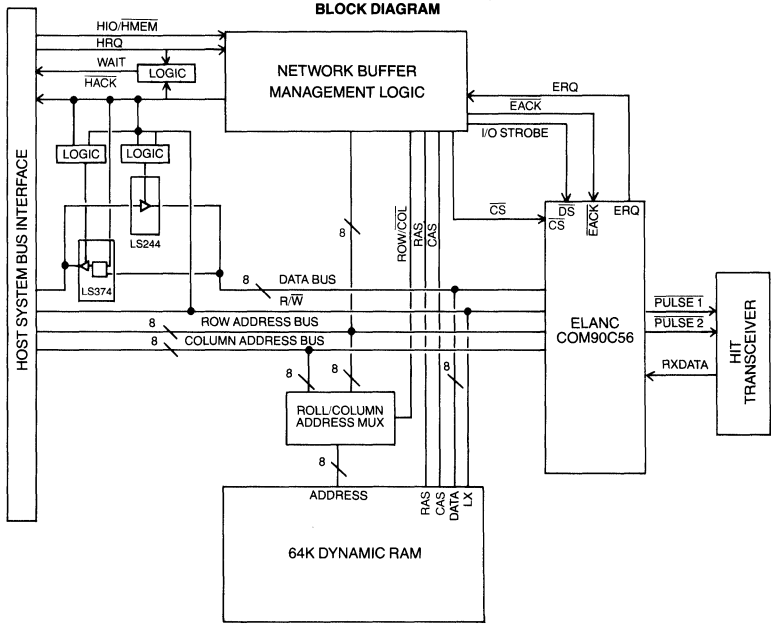


Figure 1—HIT Block Diagram

FIGURE 2:
ELANC INTERFACE WITH DYNAMIC BUFFER
BLOCK DIAGRAM



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd · Hauppauge, N.Y. 11788
(516) 273-3100 · TWX: 510-227-8898

Baud Rate Generator

Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input (use 8116 for new designs)	+5, +12	18 DIP	271-272
COM 5016T[1]	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	271-272
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input (use 8126 for new designs)	+5, +12	14 DIP	273-274
COM 5026T[1]	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	273-274
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4 (use 8136 or 81C36 for new designs)	+5, +12	18 DIP	271-272
COM 5036T[1]	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	271-272
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4 (use 8146 for new designs)	+5, +12	14 DIP	273-274
COM 5046T[1]	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	273-274
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	275-276
COM 8046T[1]	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	275-276
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	277-278
COM 8116T[1]	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	277-278
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	279-286
COM 8126T[1]	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	279-286
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	277-278
COM 8136T[1]	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	277-278
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	279-286
COM 8146T[1]	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	279-286
COM 8156	Dual Baud Rate Generator	High-frequency clock input version of COM 8116 with additional outputs of input frequency ÷ 2 and ÷ 8	+5	18 DIP	287-290
COM 8156T[1]	Dual Baud Rate Generator	External clock input version of COM 8156	+5	18 DIP	287-290
COM 81C66[2]	Timer/Clock Generator	CMOS User Programmable Clock and Timer	+5	16 DIP	291-292
COM 81C66T[2]	Timer/Clock Generator	External Frequency Input version of COM 8166T	+5	16 DIP	291-292
COM 81C67[2]	Timer/Clock Generator	CMOS User Programmable Clock and Timer. Built-in XTAL oscillator, 2 timers	+5	8 DIP	291-292
COM 81C68[2]	Timer/Clock Generator	TTL Clock Driver Version of the COM81C67 with 3 timers	+5	8 DIP	291-292

[1]May be custom mask programmed [2]For future release

STANDARD MICROSYSTEMS CORPORATION

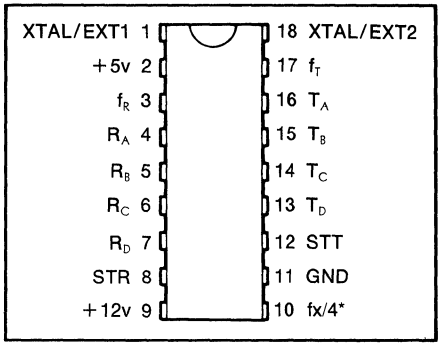
COM 5016
COM 5016T
COM 5036
COM 5036T

Dual Baud Rate Generator
Programmable Divider

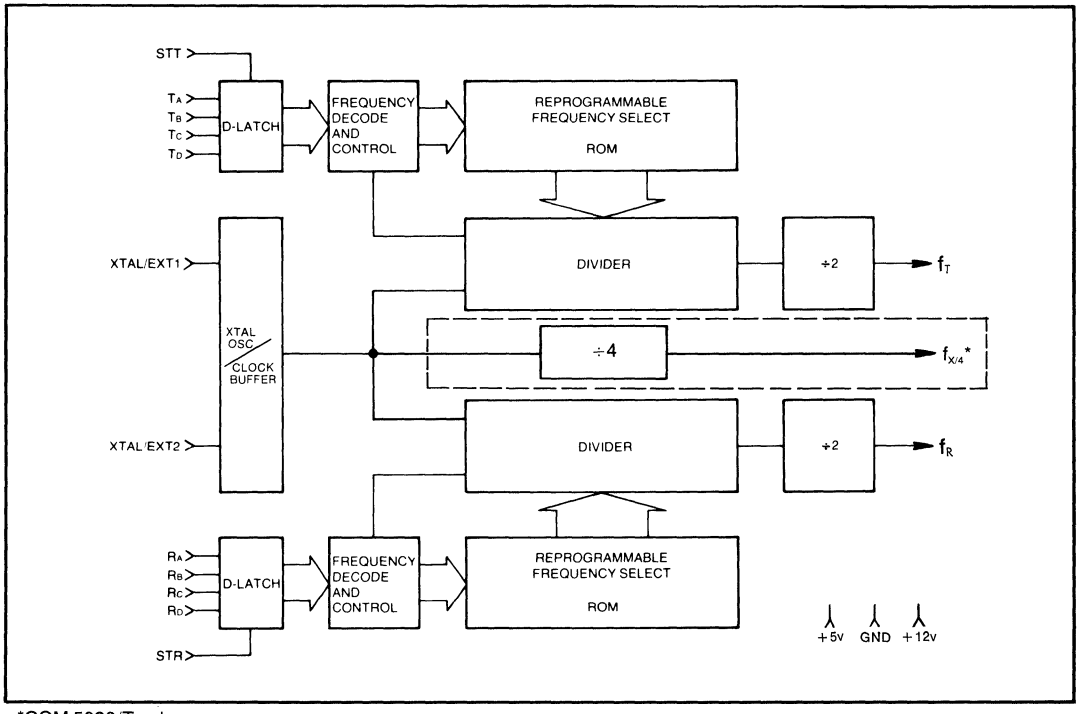
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ DIRECT UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output*
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



*COM 5036/T only

General Description

The Standard Microsystems COM 5016/COM 5036 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016/COM 5036 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016/COM 5036 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016/COM 5036 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016/COM 5036's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016/COM 5036 can be driven by either an external crystal or TTL logic level inputs; COM 5016T/COM 5036T is driven by TTL logic level inputs only.

The COM 5036 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 volt supply
10	$f_X/4$*	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

*COM 5036/T only

STANDARD MICROSYSTEMS CORPORATION

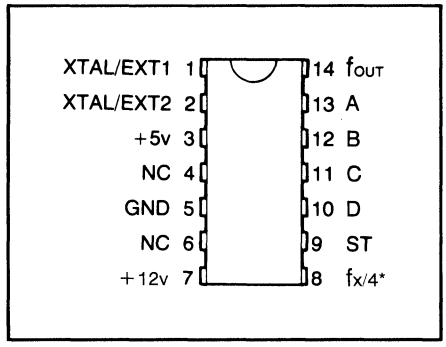
COM 5026
COM 5026T
COM 5046
COM 5046T

Baud Rate Generator
Programmable Divider

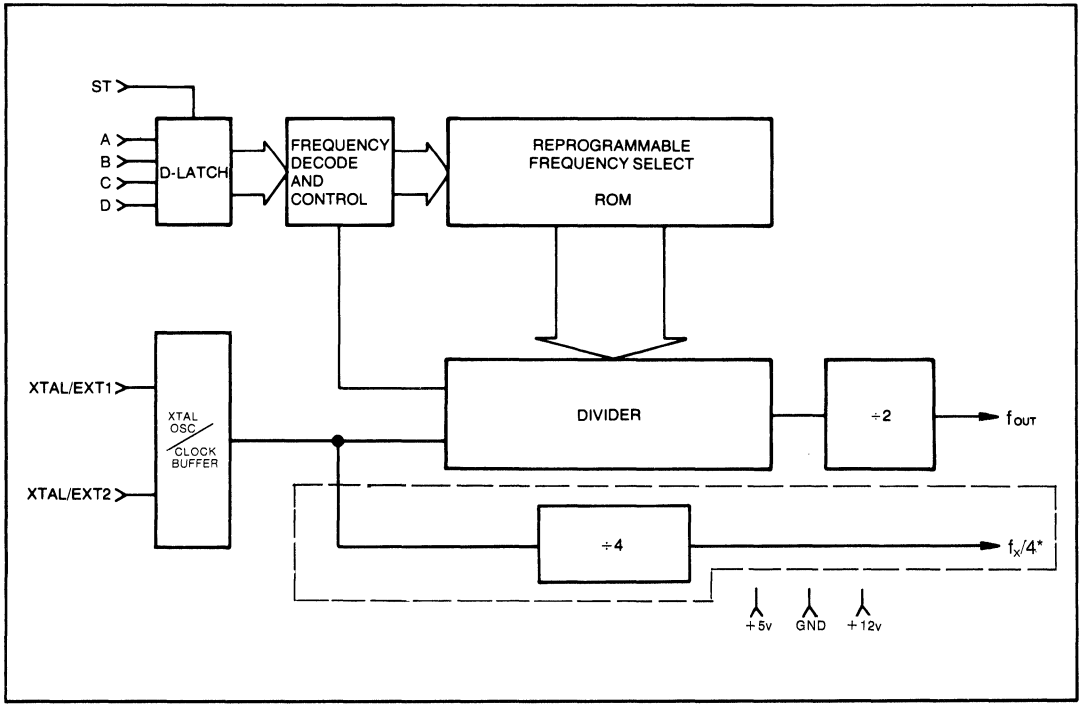
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output*
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



*COM 5046/T only

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

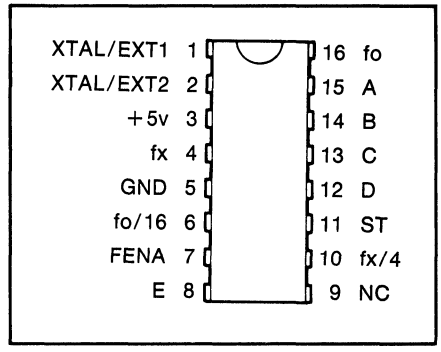
COM 8046
COM 8046T

Baud Rate Generator
Programmable Divider

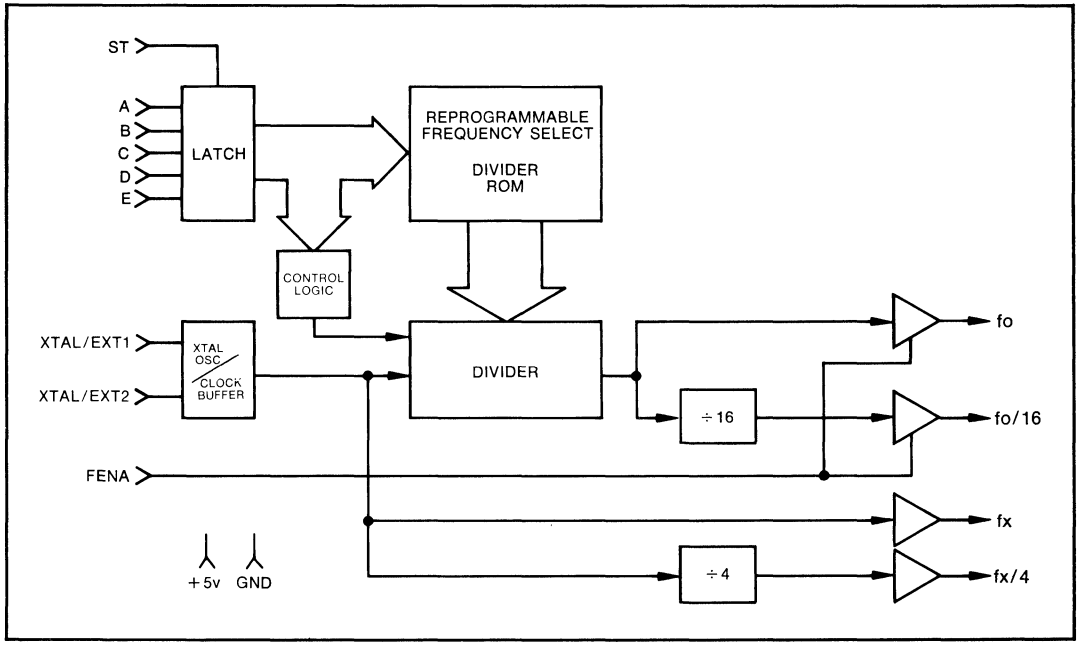
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 32 output frequencies
- ☐ 32 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatible
- ☐ 1X Clock via fo/16 output
- ☐ Crystal frequency output via fx and fx/4 outputs
- ☐ Output disable via FENA

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 8046 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 1X, 16X and 32X UART/USRT/ASTRO/USYNRT devices.

The COM 8046 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8046T. TTL outputs used to drive the COM 8046 or COM 8046T should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The reference frequency (fx) is used to provide two high frequency outputs: one at fx and the other at fx/4. The fx/4 output will drive one standard 7400 load, while the fx output will drive two 74LS loads.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency f_O. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period. The output of the divider is also divided internally by 16 and made available at the $f_O/16$ output pin. The $f_O/16$ output will drive one and the f_O output will drive two standard 7400 TTL loads. Both the f_O and $f_O/16$ outputs can be disabled by supplying a low logic level to the FENA input pin. Note that the FENA input has an internal pull-up which will cause the pin to rise to approximately V_{CC} if left unconnected.

The divisor ROM contains 32 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around-time for ROM patterns.

The five divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the five divisor select bits; strobe activity is not required. This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_O half-cycle All five data inputs have pull-ups identical to that of the FENA input, while the strobe input has no pull-up.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4	f_X	f_X	Crystal/clock frequency reference output
5	GND	Ground	Ground
6	$f_O/16$	$f_O/16$	1X clock output
7	FENA	Enable	A low level at this input causes the f_O and $f_O/16$ outputs to be held high. An open or a high level at the FENA input enables the f_O and $f_O/16$ outputs.
8	E	E	Most significant divisor select data bit. An open at this input is equivalent to a logic high.
9	NC	NC	No connection
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	ST	Strobe	Divisor select data strobe. Data is sampled when this input is high, preserved when this input is low.
12-15	D,C,B,A	D,C,B,A	Divisor select data bits. A=LSB. An open circuit at these inputs is equivalent to a logic high.
16	f_O	f_O	16X clock output

For electrical characteristics, see page 281.

STANDARD MICROSYSTEMS CORPORATION

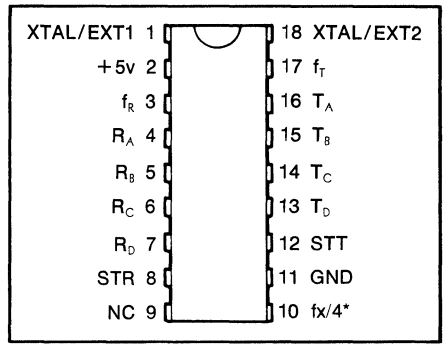
COM 8116
COM 8116T
COM 8136
COM 8136T

Dual Baud Rate Generator
Programmable Divider

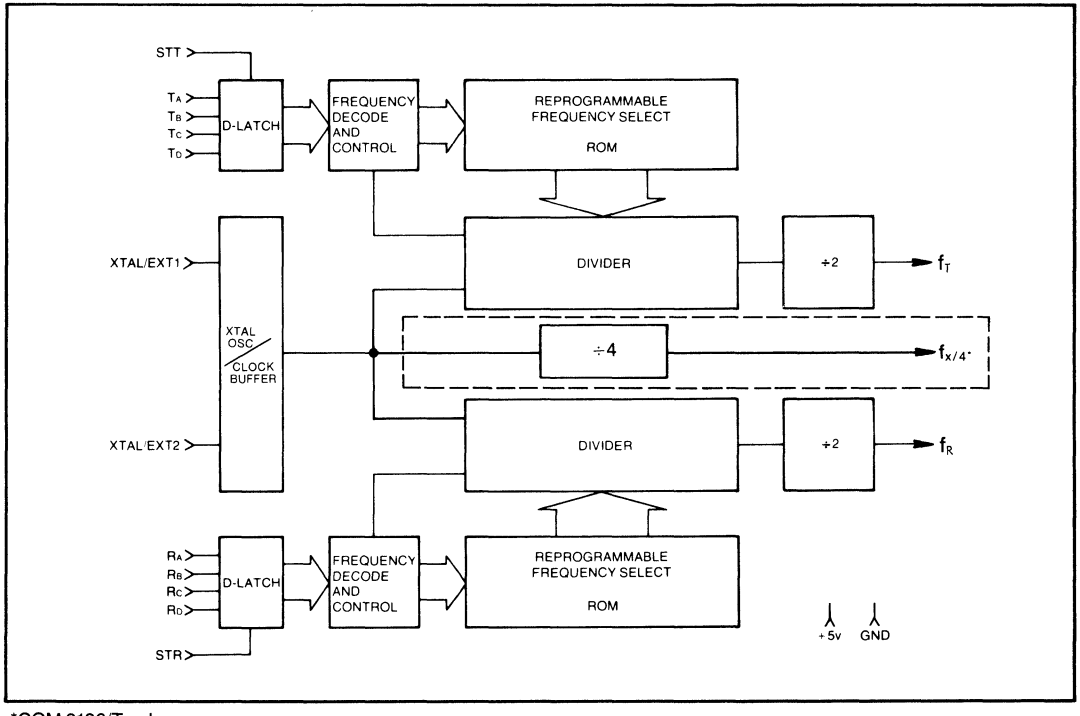
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output*
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016/COM 5036

PIN CONFIGURATION



BLOCK DIAGRAM



*COM 8136/T only

General Description

The Standard Microsystem's COM 8116/COM 8136 is an enhanced version of the COM 5016/COM 5036 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116/COM 8136 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116/COM 8136 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T/COM 8136T. TTL outputs used to drive the COM 8116/COM 8136 or COM 8116T/COM 8136T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4 on the COM 8136/T.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	$f_X/4$*	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

*COM 8136/T only

For electrical characteristics, see page 281.

STANDARD MICROSYSTEMS CORPORATION

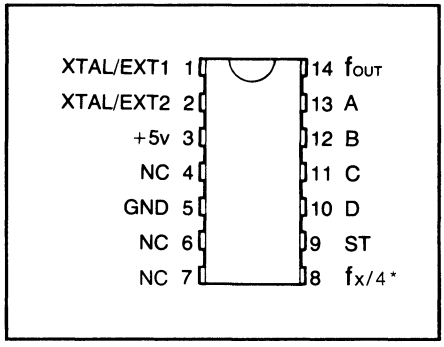
COM 8126
COM 8126T
COM 8146
COM 8146T

Baud Rate Generator
Programmable Divider

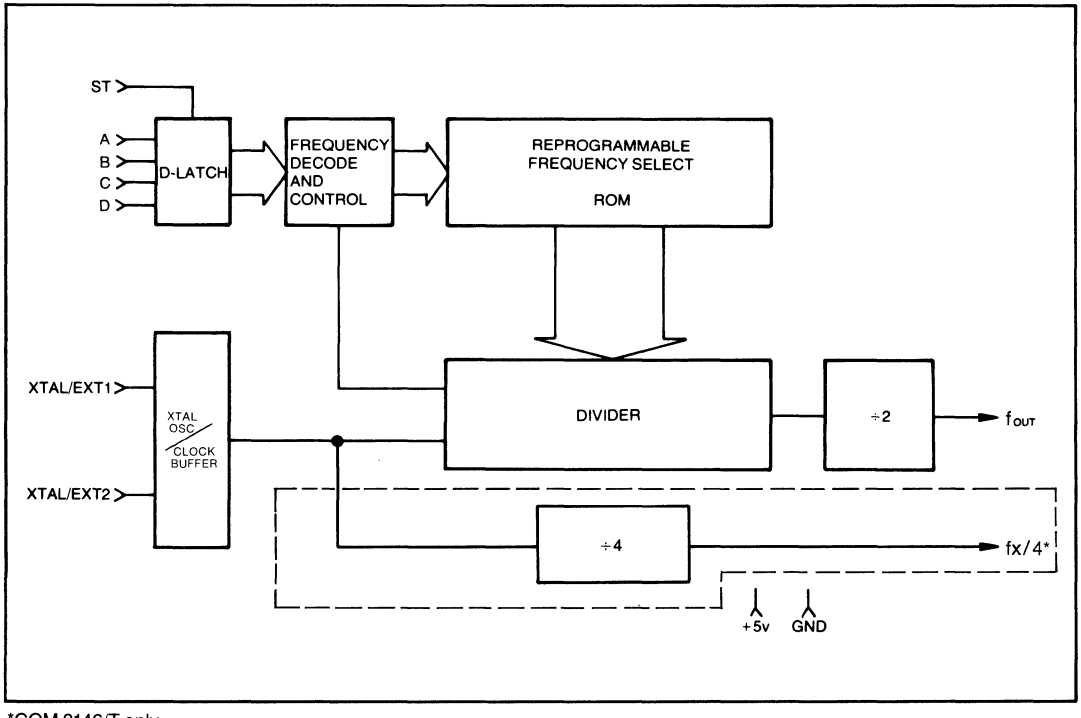
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output*
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5026/COM 5046

PIN CONFIGURATION



BLOCK DIAGRAM



*COM 8146/T only

General Description

The Standard Microsystem's COM 8126/COM 8146 is an enhanced version of the COM 5026/COM 5046 Baud Rate Generator. It is fabricated using SMC's patended COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8126/COM 8146 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8126/COM 8146 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8126T/COM 8146T. TTL outputs used to drive the COM 8126/COM 8146 or COM 8126T/COM 8146T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4 on the COM 8146/T.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turnaround time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is affected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7	NC	No Connection	
5	GND	Ground	Ground
8	$f_X/4$ *	$f_X/4$	¼ crystal/clock frequency reference output.
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C,B,A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

*COM 8146/T only

ELECTRICAL CHARACTERISTICS COM8046, COM8046T, COM8116, COM8116T, COM8126, COM8126T, COM8136, COM8136T, COM8146, COM8146T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

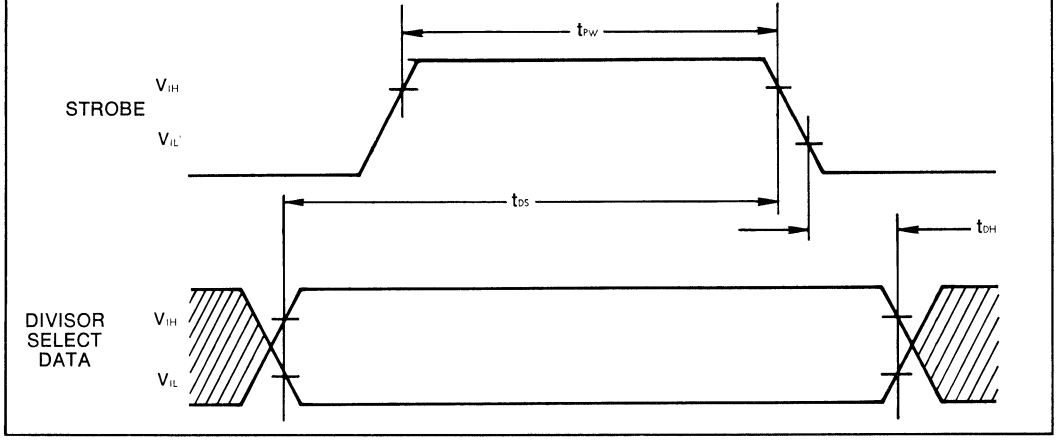
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

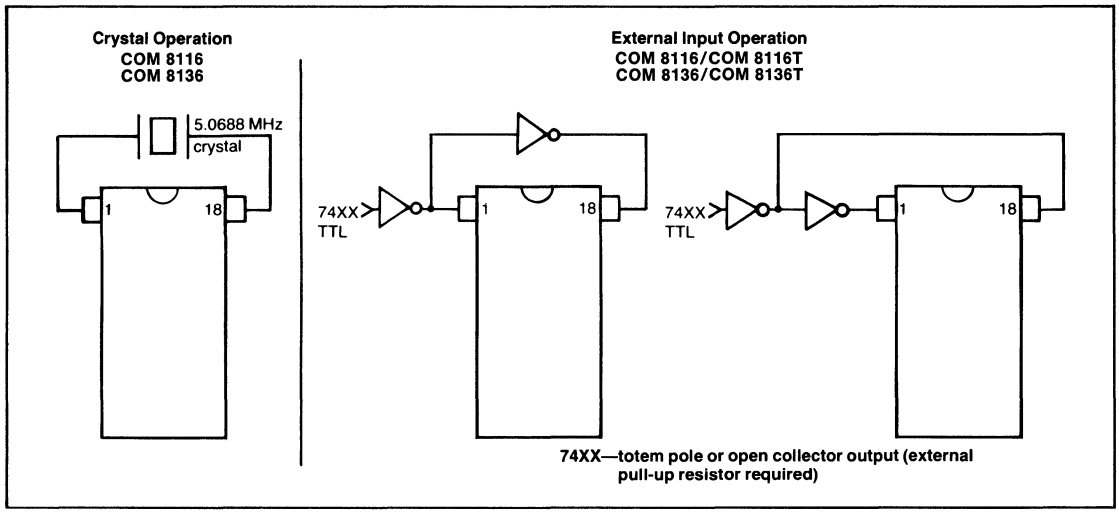
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

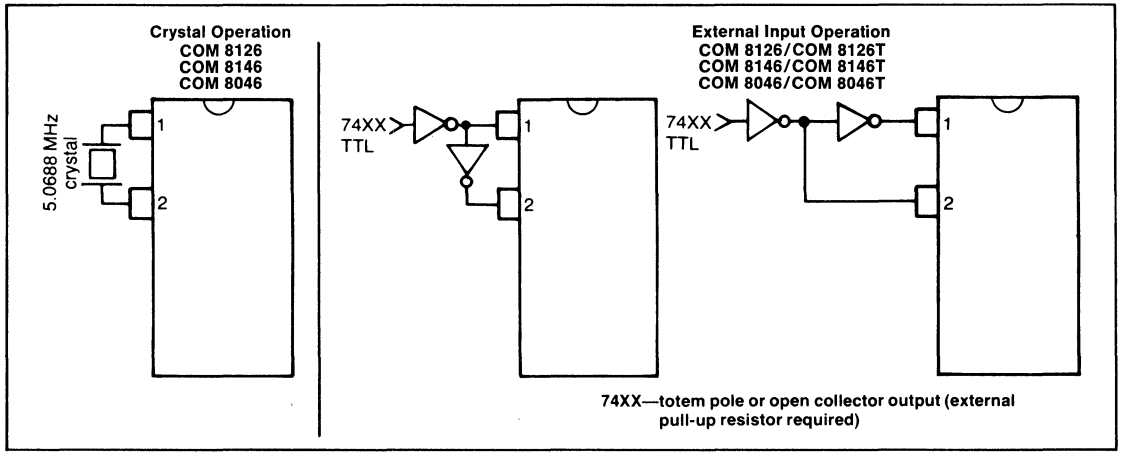
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	excluding XTAL inputs
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=1.6mA, for $f_X/4$, $f_O/16$
			0.4	V	I_{OL}=3.2mA, for f_O, f_R, f_T
			0.4	V	I_{OL}=0.8mA, for f_X
High-level, V_{OH}	3.5			V	I_{OH}=−100μA; for f_X, I_{OH}=−50μA
INPUT CURRENT					
Low-level, I_{IL}			-0.1	mA	V_{IN}=GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN}=GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 equivalent loads
POWER SUPPLY CURRENT					
I_{CC}			50	mA	
A.C. CHARACTERISTICS					T_A= +25°C
CLOCK FREQUENCY, f_{IN}	0.01		7.0	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8046, COM 8126, COM 8146
	0.01		5.1	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8116, COM 8136
STROBE PULSE WIDTH, t_{PW}	150		DC	ns	
INPUT SET-UP TIME					
t_{DS}	200			ns	
INPUT HOLD TIME					
t_{DH}	50			ns	
STROBE TO NEW FREQUENCY DELAY			3.5	μs	@ f_X=5.0 MHz

TIMING DIAGRAM



SECTION IV





For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)

Prefer: HC-18/U or HC-25/U

Frequency — 5.0688 MHz, AT cut

Temperature range 0°C to 70°C

Series resistance $<50\ \Omega$

Series Resonant

Overall tolerance ± .01%
or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

COM 8046
COM 8046T

Table 2

REFERENCE FREQUENCY = 5.068800MHz

Divisor Select EDCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
00000	50.00	32X	1.60000	3168	50.00	1.600000	0.0000%
00001	75.00	32X	2.40000	2112	75.00	2.400000	0.0000%
00010	110.00	32X	3.52000	1440	110.00	3.520000	0.0000%
00011	134.50	32X	4.30400	1177	134.58	4.306542	0.0591%
00100	150.00	32X	4.80000	1056	150.00	4.800000	0.0000%
00101	200.00	32X	6.40000	792	200.00	6.400000	0.0000%
00110	300.00	32X	9.60000	528	300.00	9.600000	0.0000%
00111	600.00	32X	19.20000	264	600.00	19.200000	0.0000%
01000	1200.00	32X	38.40000	132	1200.00	38.400000	0.0000%
01001	1800.00	32X	57.60000	88	1800.00	57.600000	0.0000%
01010	2400.00	32X	76.80000	66	2400.00	76.800000	0.0000%
01011	3600.00	32X	115.20000	44	3600.00	115.200000	0.0000%
01100	4800.00	32X	153.60000	33	4800.00	153.600000	0.0000%
01101	7200.00	32X	230.40000	22	7200.00	230.400000	0.0000%
01110	9600.00	32X	307.20000	16	9900.00	316.800000	3.1250%
01111	19200.00	32X	614.40000	8	19800.00	633.600000	3.1250%
10000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
10001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
10010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
10011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
10100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
10101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
10110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
10111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
11000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
11001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
11010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
11011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
11100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
11101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
11110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
11111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

Baud Rate Generator Output Frequency Options

COM 8116T-013

CRYSTAL FREQUENCY = 2.76480 MHz

Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	0	50/50	3456
0	0	0	1	75	1.2	1.2	0	50/50	2304
0	0	1	0	110	1.76	1.76	−.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−.019	50/50	1285
0	1	0	0	150	2.4	2.4	0	50/50	1152
0	1	0	1	200	3.2	3.2	0	50/50	864
0	1	1	0	300	4.8	4.8	0	50/50	576
0	1	1	1	600	9.6	9.6	0	50/50	288
1	0	0	0	1200	19.2	19.2	0	50/50	144
1	0	0	1	1800	28.8	28.8	0	50/50	96
1	0	1	0	2000	32.0	32.149	+.465	50/50	86
1	0	1	1	2400	38.4	38.4	0	50/50	72
1	1	0	0	3600	57.6	57.6	0	50/50	48
1	1	0	1	4800	76.8	76.8	0	50/50	36
1	1	1	0	9600	153.6	153.6	0	50/50	18
1	1	1	1	19,200	307.2	307.2	0	44/56	9

COM 8116T-003

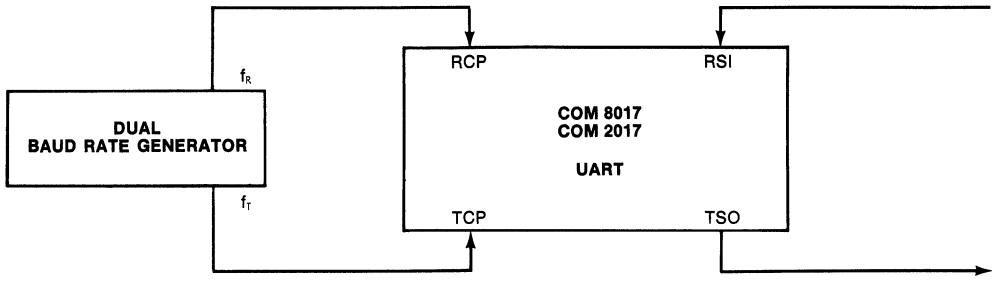
CRYSTAL FREQUENCIES = 6.01835 MHz

Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	799.9 Hz	0	50/50	7523
0	0	0	1	75	1.2	1200.0	0	50/50	5015
0	0	1	0	110	1.76	1759.7	0	50/50	3420
0	0	1	1	134.5	2.152	2151.7	0	50/50	2797
0	1	0	0	150	2.4	2399.6	0	50/50	2508
0	1	0	1	200	3.2	3199.5	0	50/50	1881
0	1	1	0	300	4.8	4799.3	0	50/50	1254
0	1	1	1	600	9.6	9598.6	0	50/50	627
1	0	0	0	1200	19.2	19227.9	+0.14	50/50	313
1	0	0	1	1800	28.8	28795.9	0	50/50	209
1	0	1	0	2000	32.0	32012.5	0	50/50	188
1	0	1	1	2400	38.4	38333.4	−0.17	50/50	157
1	1	0	0	3600	57.6	57868.7	+0.46	50/50	104
1	1	0	1	4800	76.8	77158.3	+0.46	50/50	78
1	1	1	0	9600	153.6	154316.6	+0.46	50/50	39
1	1	1	1	19,200	307.2	300917.5	2.04	50/50	20

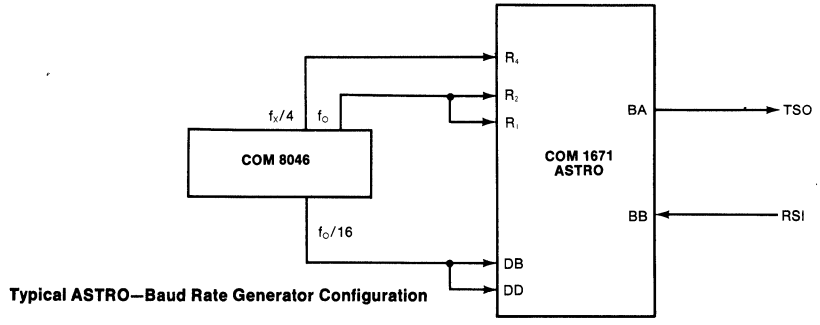
COM 8116T-013A

CRYSTAL FREQUENCY—5.52960 MHz

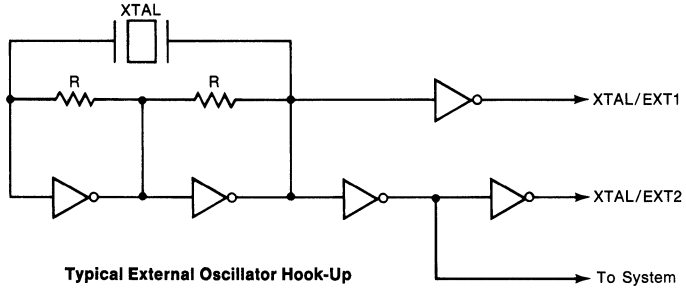
Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	100	1.6 KHz	1.6 KHz	0	50/50	3456
0	0	0	1	150	2.4	2.4	0	50/50	2304
0	0	1	0	220	3.52	3.5197	−.006	50/50	1571
0	0	1	1	269	4.304	4.3032	−.019	50/50	1285
0	1	0	0	300	4.8	4.8	0	50/50	1152
0	1	0	1	400	6.4	6.4	0	50/50	864
0	1	1	0	600	9.6	9.6	0	50/50	576
0	1	1	1	1200	19.2	19.2	0	50/50	288
1	0	0	0	2400	38.4	38.4	0	50/50	144
1	0	0	1	3600	57.6	57.6	0	50/50	96
1	0	1	0	4000	64.0	64.298	+.466	50/50	86
1	0	1	1	4800	76.8	76.8	0	50/50	72
1	1	0	0	7200	115.2	115.2	0	50/50	48
1	1	0	1	9600	153.6	153.6	0	50/50	36
1	1	1	0	19,200	307.2	307.2	0	50/50	18
1	1	1	1	38,400	614.8	614.8	0	44/56	9



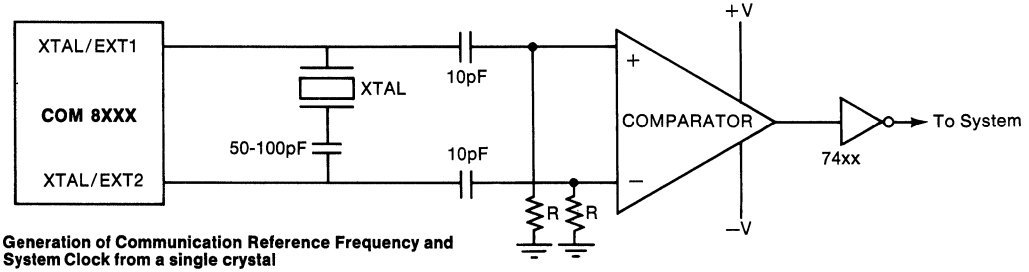
Typical UART—Dual Baud Rate Generator Configuration
Full Duplex—Split Speed



Typical ASTRO—Baud Rate Generator Configuration



Typical External Oscillator Hook-Up



Generation of Communication Reference Frequency and System Clock from a single crystal

STANDARD MICROSYSTEMS CORPORATION

COM 8156
COM 8156T
PRELIMINARY

Dual Baud Rate Generator
Programmable Divider

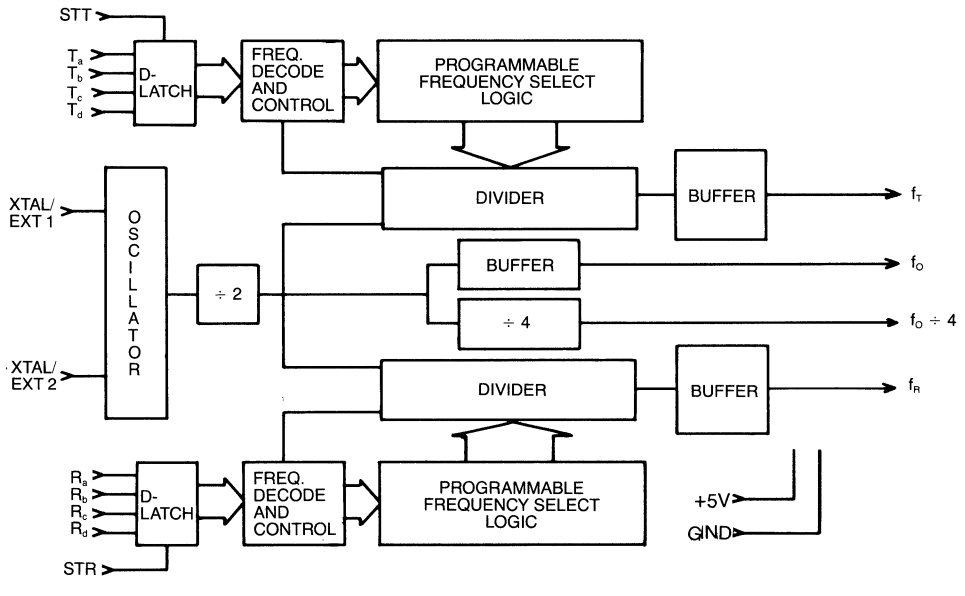
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ High crystal/clock frequency operation
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ High frequency reference outputs
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ N-channel silicon gate technology
- ☐ Single $+5_V$ power supply
- ☐ TTL, MOS compatibility
- ☐ Re-programmable ROM technology allows generation of other frequencies

PIN CONFIGURATION

Rb	1	18	Ra
Rc	2	17	f_R
Rd	3	16	Vcc
STR	4	15	$XTAL_1$
$XTAL_2$	5	14	fo
fo/4	6	13	f_T
GND	7	12	Ta
STT	8	11	Tb
Td	9	10	Tc

BLOCK DIAGRAM



GENERAL DESCRIPTION

The Standard Microsystem's COM8156 is a dual baud rate generator that operates at twice the crystal/clock frequency of the COM8116/36. It is fabricated using SMC's patented COPLAMOS™ technology and employs depletion mode loads allowing operation from a single +5V supply.

The standard COM8156 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM8156 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 9. Parts suitable for use only with an external TTL reference are marked COM 8156T. TTL outputs used to drive the COM8156 or COM8156T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by an integer from 6 to $2^{19}+1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer that it is low by one f_O clock period.

The crystal frequency is divided by two to give (f_O) and again by four to give ($f_{O/4}$). The transmit (f_T) and receive (f_R) frequencies are obtained by dividing (f_O) by N. Up to 32 different divisors can be mask-programmed on custom parts to accommodate different crystal frequencies and divider schemes. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5us of a change in any of the four divisor select bits (strobe activity is not required). The divisor select bits (strobe activity is not required). The divisor select inputs and the strobe inputs have pull-up resistors.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	XTAL/EXT 1	Crystal	This input receives one pin of the crystal package.
16	V_{CC}	Power Supply	+5 Volt Supply.
17	f_R	Receiver Output	This output runs at a frequency selected by the Receiver Address Inputs.
18 1-3	R_a R_b R_c, R_d	Receiver Divisor Select Address	The logic level on these inputs as shown in Table 1, selects the receiver output frequency, f_R.
4	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_a, R_b, R_c, R_d) into the receiver address register. This input may be strobed or hard wired to +5V.
5	XTAL/EXT 2	Crystal	This input receives one pin of the crystal package.
6	$f_{o/4}$	Oscillator Output	This output runs at a frequency selected by the crystal ÷ 8.
7	GND	Ground	Ground
8	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_a, T_b, T_c, T_d) into the transmitter address register. This input may be strobed or hard wired to +5V.
9-12	T_d T_c, T_b T_a	Transmitter Divisor Select Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
13	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
14	f_o	Oscillator Output Frequency	This output runs at a frequency selected by the crystal ÷ 2.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

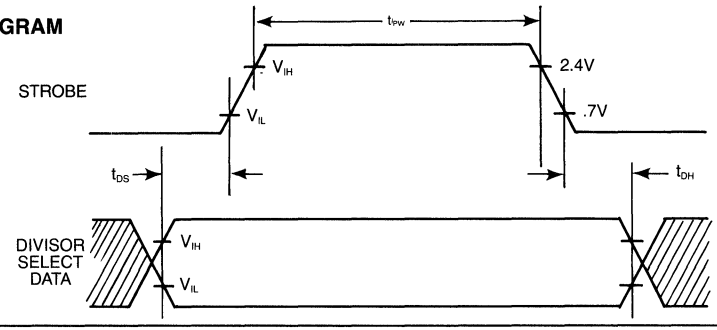
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	excluding XTAL inputs
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA, for $f_{o/4}$
			0.4	V	I_{OL} = 3.2 mA, for f_R, f_T
High Level V_{OH}			0.5	V	I_{OL} = 3.2 mA, for f_O
	2.4			V	I_{OH} = −100 µA
INPUT CURRENT					
Low-level, I_{IL}			−0.1	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 equivalent loads
POWER SUPPLY CURRENT					
I_{CC}			60	mA	
AC CHARACTERISTICS					
CLOCK FREQUENCY, f_{IN}	5.0		11.0	MHz	XTAL/EXT, 50% Duty Cycle ±5%
STROBE PULSE WIDTH, t_{PW}	150		DC	ns	
INPUT SET-UP TIME					
t_{DS}	50			ns	
INPUT HOLD TIME					
T_{DH}	50			ns	
STROBE TO NEW FREQ. DELAY			3.5	µs	
OUTPUT CLOCKS DUTY CYCLE					
f_O	40		60	%	@ 1.5V LEVEL
$f_{O/4}$	45		55	%	@ 1.5V LEVEL
f_R, f_T	48		52	%	@ 1.5V LEVEL
CRYSTAL CHARACTERISTICS					
Series Crystal Resistance		30	70		@ Resonance
Crystal Shunt Capacitance	2	5	10	pf	

TIMING DIAGRAM



Baud Rate Generator Output Frequency Options

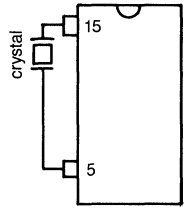
COM8156/COM8156T (16X clock)
CRYSTAL FREQUENCY = 10.1376 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19.200	307.2	316.8	3.125	50/50	16

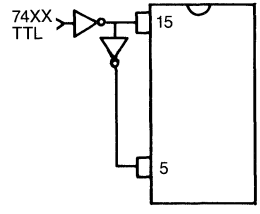
COM8156-005/COM8156T-005 (16X clock)
CRYSTAL FREQUENCY = 9.8304 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7589	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19.200	307.2	307.2	—	50/50	16

Crystal Operation



External Input Operation



74XX—totem pole or open collector output (external pull-up resistor required)

For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency: 10.1376 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance <50 Ω
Series Resonant
Overall tolerance ±.01%
or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM81C66
COM81C67
COM81C68
PRELIMINARY

Universal Rate Generator and Timer

FEATURES

- ☐ Three independent 20 bit programmable counters
- ☐ All counters are cascadeable
- ☐ Clock input up to 16 MHz
- ☐ Square wave, pulse, one shot modes of operation
- ☐ Input clock prescalers divide by 2, 32, or 64
- ☐ Low power CMOS
- ☐ 8 and 16 D.I.P. packages
- ☐ Crystal or TTL frequency source
- ☐ Single +5 Volt power supply

GENERAL DESCRIPTION

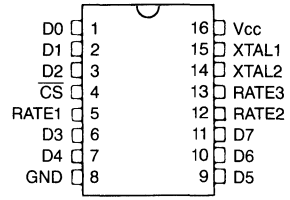
The TIMER chip is a device designed to provide a convenient and inexpensive solution to applications requiring programmable multiple clock divider sources. The source frequency can be either an internal crystal controlled oscillator, or an external TTL signal. The TIMER consists of a data input portion, a register addressing block and three counter blocks.

The Counter blocks are accessed and programmed independently and they can be configured to operate in various modes simultaneously.

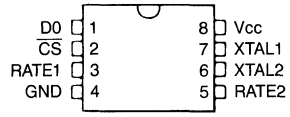
The TIMER chip serves a broad range of applications some of which are: programmable rate generation, pulse generation, motor control, real time clock, interrupt applications and others.

PIN CONFIGURATIONS

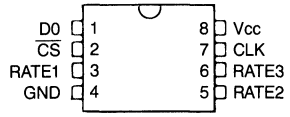
COM81C66 - 16 PIN VERSION



COM81C67 - CRYSTAL OSCILLATOR VERSION



COM81C68 - TTL CLOCK VERSION



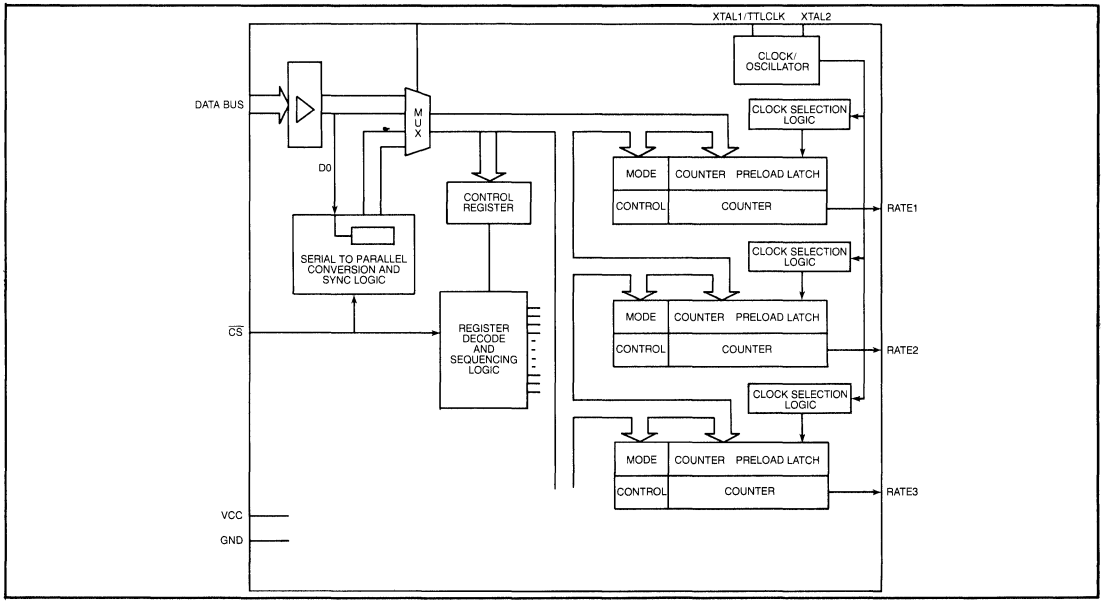


TABLE 1 - COM81C67 AND COM81C68, DESCRIPTION OF PIN FUNCTIONS

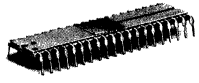
The COM81C67 and COM81C68 are two eight pin versions of the TIMER chip. The COM81C68 is a TTL clock input only and the COM81C67 is a crystal oscillator pin connection.

PIN NO.		SYMBOL	TYPE	NAME AND FUNCTION
81C68	81C67			
1	1	D0	I	DATA BUS—This input only pin is used to program and initialize the Timer.
3 5 6	3 5	RATE1 RATE2 RATE3	0	RATE OUTPUT—These outputs will supply the programmable rate outputs according to the mode and preload on the specified Timer Block.
2	2	$\overline{CS}$	I	CHIP SELECT—A low level on this input enables the processor to write to the TIMER. When $\overline{CS}$ is high, the Data input pin is high impedance.
—	7,6	XTAL1 XTAL2	I	CRYSTAL—An external crystal is connected to these pins on the COM81C67. An external TTL clock can be used on pin 7. Pin 8 must be left floating open.
7	—	CLK	I	CLOCK—This is a TTL clock input used as the main clock for the COM81C68.
8	8	VCC	I	POWER—This is a +5V power supply.
4	4	GND	—	GROUND

TABLE 2 - COM81C66, DESCRIPTION OF PIN FUNCTIONS

The COM81C66 is a sixteen pin version with an internal crystal oscillator.

PIN NO. 81C66	SIGNAL	TYPE	NAME AND FUNCTION
1-3 6,7 9-11	D0-D7	I	DATA BUS—The Timer is programmed by write operations via the Data Bus.
5 12 13	RATE1 RATE2 RATE3	0	RATE OUTPUT—This output will supply the programmable rate output according to the mode and preload on the specified Timer Block.
4	$\overline{CS}$	I	CHIP SELECT—A low level on this input enables the processor to write to the TIMER. When $\overline{CS}$ the Data input(s) are don't cares.
15 14	XTAL1 XTAL2	I	CRYSTAL—An external crystal is connected to these pins on the COM81C66. An external TTL clock can be used on XTAL1.
16	VCC	—	POWER—There is a +5V power supply.
8	GND	—	GROUND



Display Products

TIMING CONTROLLERS

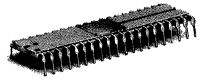
Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	Provides all of the timing and control for interlaced and non-interlaced CRT display		Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 5037		Balanced beam interlace	Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 5047		Fixed format	80 column 24 row	4MHZ	+5, +12	40 DIP	297-298
CRT 5057		Line-lock	Programmable	4MHz	+5, +12	40 DIP	295-296
CRT 7220A, −1, −2	Graphics Display Controller	Intelligent graphics display controller	1024 x 1024 Pixel	6, 7, 8 MHz	+5	40 DIP	299-322
CRT 9007A2, A1, A, B, C	CRT video processor and controller	Sequential or row-table driven memory programmable DMA	Programmable	A2-6.5 MHz A1-5.0 MHz A-3.7 MHz B-3.33 MHz C-2.5 MHz	+5	40 DIP	335-356
CRT 97C11	3rd generation CRT controller which allows manipulation of independent window areas on screen	Control of window size and position, window attributes, prog cursor, max of 127 windows, DRAM refresh	Up to 16K pixels vertical and 1KxN (N = display memory width) in horizontal pixels	TBD	+5	68 PLCC	433-452

TERMINAL LOGIC CONTROLLERS

Part Number	Description	Features	Display Format	Attributes	Max Clock	Power Supply	Package	Page
CRT 9028/ 9128[1]	Complete CRT video processor and controller. Display and attribute control for alphanumeric and graphics display. Two types of processor interface signals differentiate the two parts.	Separate display memory eliminates contention, smooth scroll, status row, on-board clock, and video shift register	Mask programmable, 5x8 character font, 8x12 character cell.	Tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics.	14MHz	+5	40 DIP	369-384
CRT 9053/ 9153[1]			Mask programmable, 7x11 character font, 9x13 character cell.	Embedded or tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics.	18.7MHz			401-416
CRT92C07	Complete timing and attributes controller. Uses external character generator.	Double speed architecture and separate display memory bus eliminates memory contention. Multiple smooth scroll regions on screen.	Register programmable, maximum 12x16 character cell.	Tagged, embedded or parallel attributes: reverse video, blank, blink, underline, DH/DW, protected field, intensity.	42 MHz	+5	84 PLCC	417-420

[1]May be custom mask programmed

SECTION V



Display Products CONT.

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supplies	Package	Page
CRT 8002H	Provides complete display and attributes control for alphanumeric and graphic display. Consists of 7 x 11 x 128 character generator, video shift register latches, graphics and attributes circuits.	7x11 dot matrix, wide graphics, thin graphics, on-chip cursor	Reverse video blank blink underline strike-thru	25 MHz	+5	28 DIP	325-326
CRT 8002A[1,3]				20 MHz			323-324
CRT 8002B[1,3]				15 MHz			323-324
CRT 8002C[1,3]				10 MHz			323-324

[1]May be custom mask programmed [3]Also available as CRT8002A, B, C-001 Katakana
CRT8002A, B, C-003, -018 5 x 7 dot matrix

VIDEO ATTRIBUTES CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8021	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor	Reverse video, blank, blink underline, strike-thru	20 MHz	+5	28 DIP	327-328
CRT 9021B	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width	Reverse video, blank, blink underline, intensity	28.5 MHz	+5	28 DIP	357-368
CRT 9041A, B, C	Provides attributes and graphics control for CRT video displays. Full VT100® and VT220® compatible	Alphanumeric, wide and thin graphics, 4 cursor modes, double height/width, 12 bit shift register	Reverse video, blink, blank, underline, 4 intensity levels	A-33 MHz B-30 MHz C-28.5 MHz	+5	40 DIP	385-400

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83	8 bit wide serial cascadable single row buffer memory for CRT or printer	83 characters	+5	24 DIP	329-334
CRT 9006-135		135 characters			
CRT 9212	8 bit wide serial cascadable double row buffer memory for CRT or printer	135 characters	+5	28 DIP	421-426
CRT 94C12	8 bit wide serial, quad row buffer memory for CRT or printer	135 characters	+5	40 DIP	427-432

VT100 and VT220 are registered trademarks of Digital Equipment Corp.

STANDARD MICROSYSTEMS CORPORATION

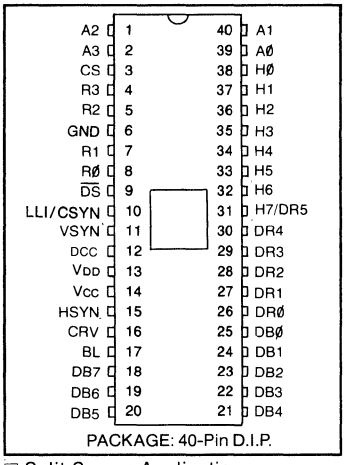
CRT 5027
CRT 5037
CRT 5057

CRT Video Timer and Controller
VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

SECTION V

GENERAL DESCRIPTION

The CRT Video Timer and Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

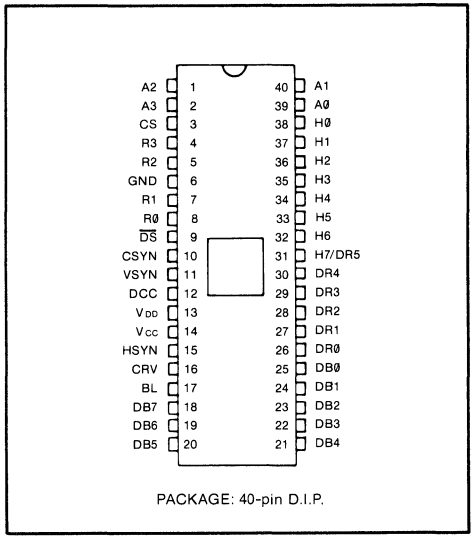
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

Preprogrammed CRT Video Timer and Controller VTAC®

FEATURES

- ☐ Preprogrammed (Mask-Programmed) Display Format
  - 80 Characters Per Data Row
  - 24 Data Rows Per Frame
  - 9 Scan Lines Per Data Row
- ☐ Preprogrammed Monitor Sync Format
  - 262 Scan Lines Per Frame
  - 6 Character Times for Horizontal Front Porch
  - 8 Character Times for Horizontal Sync Width
  - 6 Character Times for Horizontal Back Porch
  - 16 Scan Lines for Vertical Front Porch
  - 3 Scan Lines for Vertical Sync Width
  - 27 Scan Lines for Vertical Back Porch
  - Non-Interlace
  - 15.720KHz Horizontal Scan Rate
  - 60Hz Frame Refresh Rate
- ☐ Fixed Character Rate
  - 1.572MHz Character Rate (636.13ns/Character)
  - 11.004MHz Dot Rate (90.88ns/Dot) for 7 Dot Wide Character Block
- ☐ Character Format
  - 5 X 7 Character in a 7 X 9 Block
- ☐ Compatible with CRT 8002B-003 VDAC™
- ☐ Compatible with CRT 7004B-003
- ☐ May be mask-programmed with other display formats

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

GENERAL DESCRIPTION

The two chip combination of SMC's CRT 5047 and CRT 8002B-003 effectively provide all of the video electronics for a CRT terminal. This chip set along with a μC form the basis for a minimum chip count CRT terminal.

The CRT 5047 Video Timer and Controller is a special version of the CRT 5037 VTAC® which has been ROM-programmed with a fixed format. It is especially effective for low-cost CRT terminals using an 80 X 24 display format with a 5 X 7 character matrix. The use of a fixed ROM program in the CRT 5047 eliminates the software overhead normally required to specify the display parameters and simplifies terminal software design.

The Cursor Character Address Register and the Cursor Row Address Register are the only two registers accessible by the processor. The CRT 5047 is easily initialized by the following sequence of commands:

Reset Load Control Register 6 Start Timing Chain

The parameters of the CRT 5047 have been selected to be compatible with most CRT monitors. The horizontal timing is programmed so that when the two character skew delay of the CRT 8002 VDAC™ is taken into account, the effective timing is: Horizontal Front Porch—four characters, and Horizontal Back Porch—eight characters.

Figure 1 shows the contents of the internal CRT 5047 registers. Other mask-programmed versions of the CRT 5037 are available. Consult SMC for more information.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

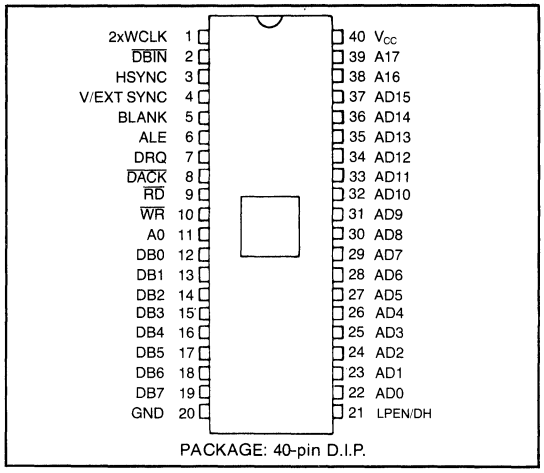
CRT 7220A
CRT 7220A-1
CRT 7220A-2

High-Performance Graphics Display Controller

FEATURES

- ☐ Microprocesser Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles as fast as 500ns
  - Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode
  - Four megabit, bit-mapped display memory
- ☐ Character Mode
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Character Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities
  - Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

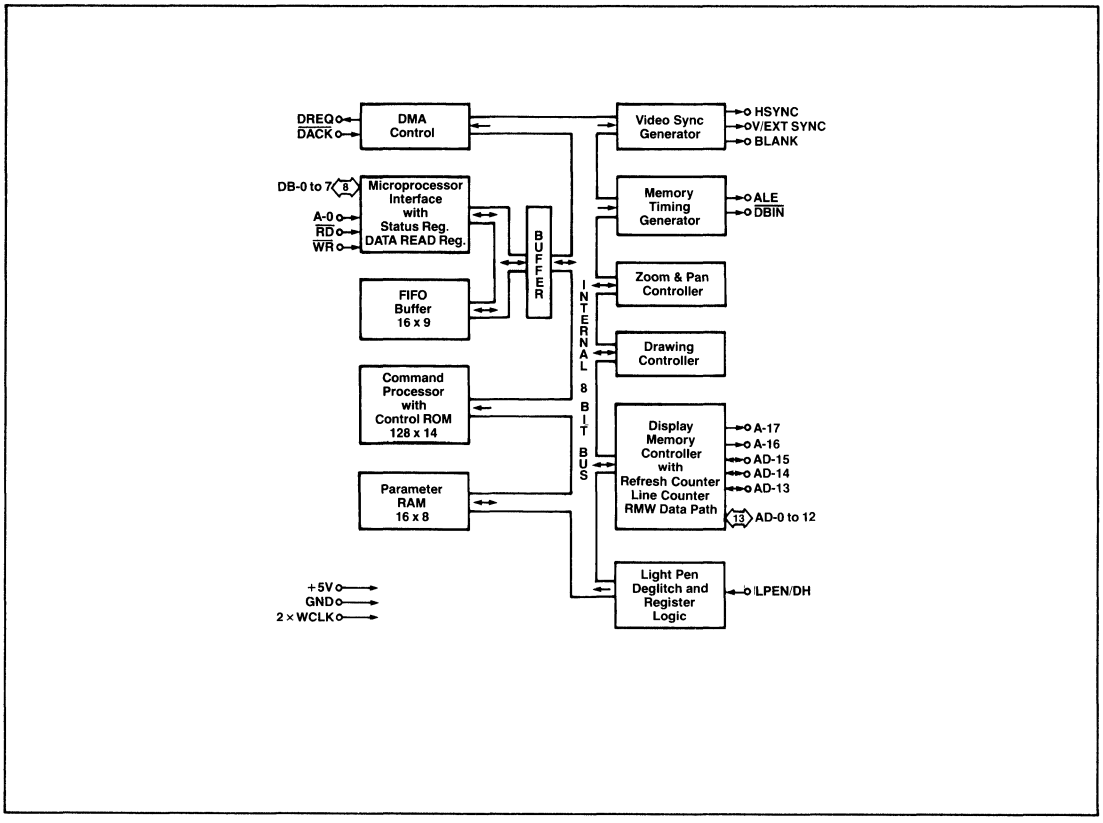
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
- ☐ Single +5 volt Power Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ DMA Capability
  - Bytes or word transfers
  - 4 clock periods per byte transferred

SECTION V

GENERAL DESCRIPTION

The CRT 7220A High-performance Graphics Display Controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	IN/OUT	FUNCTION
1	2XWCLK	IN	Clock Input
2	$\overline{DBIN}$	OUT	Display Memory Read Input Flag
3	HSYNC	OUT	Horizontal Video Sync Output
4	V/EXTSYNC	IN/OUT	Vertical Video Sync Output or External VSYNC Input
5	BLANK	OUT	CRT Blanking Output
6	ALE ($\overline{RAS}$)	OUT	Address Latch Enable Output
7	DRQ	OUT	DMA Request Output
8	$\overline{DACK}$	IN	DMA Acknowledge Input
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface
10	$\overline{WR}$	IN	Write Strobe Input for Microprocessor Interface
11	A0	IN	Address Select Input for Microprocessor Interface
12-19	DB0-DB7	IN/OUT	Bidirectional data bus to Host Microprocessor
20	GND	—	Ground
21	LPEN/DH	IN	Light Pen Detect Input/Drawing Hold Input
22-34	AD0-AD12	IN/OUT	Address and Data Lines to Display Memory
35-37	AD13-AD15	IN/OUT	Character Mode: Line Counter Outputs, Bits 0-2 Mixed Mode: Address and Data Bits 13-15 Graphics Mode: Address and Data Bits 13-15
38	A16	OUT	Character Mode: Line Counter Output, Bit 3 Mixed Mode: Attribute Blink and Clear Line Counter Output Graphics Mode: Address Bit 16 Output
39	A17	OUT	Character Mode: Cursor Output and Line Counter Bit 4 Mixed Mode: Cursor and Bit Map Area Flag Output Graphics Mode: Address Bit 17 Output
40	VCC	—	+5 Volt Power Supply

FUNCTIONAL DESCRIPTION

Microprocessor Bus Interface

Control of the HGDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal HGDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the HGDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the HGDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple HGDC's.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the HGDC's ALE and DBIN outputs.

Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

Drawing Controller

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address. If this input is held high for a period greater than four 2xWCLK cycles, drawing execution is halted.

PROGRAMMER'S VIEW OF HGDC

The HGDC occupies two addresses on the system microprocessor bus through which the HGDC's status register and FIFO are accessed. Commands and parameters are written into the HGDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	Status Register	Parameter Into FIFO
1	FIFO Read	Command Into FIFO

HGDC Microprocessor Bus Interface Registers

Commands to the HGDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate reigsters within the HGDC, and initiates the required operations.

The commands available in the HGDC can be organized into five categories as described in the following section.

HGDC COMMAND SUMMARY

Video Control Commands

1. RESET 1 — Resets the HGDC to its idle state.
2. RESET 2 — Resets the HGDC to its idle state. Does not resynchronize video timing. Blanks the display.
3. RESET 3 — Resets the HGDC to its idle state. Does not resynchronize video timing. Does not blank the display.
4. SYNC — Specifies the video display format.
5. VSYNC — Selects master or slave video synchronization mode.
6. CCHAR — Specifies the cursor and character row heights.

Display Control Commands

1. START — Ends Idle mode and unblanks the display.
2. BLANK 1 — Controls the blanking and unblanking of the display, along with video resynchronization.
3. BLANK 2 — Controls the blanking and unblanking of the display. Does not blank the display.
4. ZOOM — Specifies zoom factors for the display and graphics characters writing.
5. CURS — Sets the position of the cursor in display memory.
6. PRAM — Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
7. PITCH — Specifies the width of the X dimension of display memory.

Drawing Control Commands

1. WDAT — Writes data words or bytes into display memory.
2. MASK — Sets the mask register contents.
3. FIGS — Specifies the parameters for the drawing controller.
4. FIGD — Draws the figure as specified above.
5. GCHRD — Draws the graphics character into display memory.

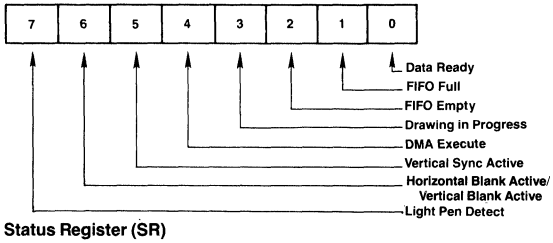
Data Read Commands

1. RDAT: — Reads data words or bytes from display memory.
2. CURD: — Reads the cursor position.
3. LPRD: — Reads the light pen address.

DMA Control Commands

1. DMAR — Requests a DMA read transfer.
2. DMAW — Requests a DMA write transfer.

STATUS REGISTER FLAGS



Status Register (SR)

SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active/Vertical Blank Active

A 1 value for this flag signifies that horizontal retrace blanking or vertical retrace blanking is currently underway dependent on the status of the VH bit in SYNC or the RESETx parameter 6.

SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute

This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress

While the HGDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty

This bit and the FIFO Full flag coordinate system microprocessor accesses with the HGDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the HGDC have been interpreted.

SF-1: FIFO Full

A 1 at this flag indicates a full FIFO in the HGDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked out before each write into the HGDC.

SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO OPERATION & COMMAND PROTOCOL

The first-in, first-out buffer (FIFO) in the HGDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the HGDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the HGDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the HGDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the HGDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the HGDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the HGDC always put the FIFO into write mode if it wasn't in it already.

If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a HGDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the HGDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

READ-MODIFY-WRITE CYCLE

Data transfers between the HGDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of

memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the HGDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

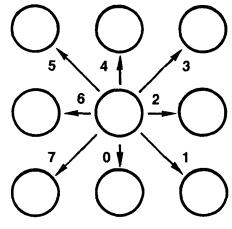
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern Register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

FIGURE DRAWINGS

The HGDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 8MHz, this is equal to 500ns. During the RMW cycle the HGDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the HGDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the HGDC's internal RMW logic.

During the drawing process, the HGDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The HGDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

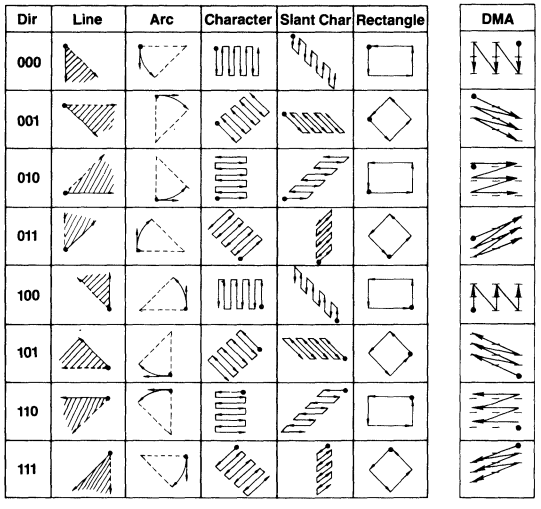
The table below summarizes these operations for each direction.

Dir	Operations to Address the Next Pixel
000	EAD − P → EAD
001	EAD − P → EAD dAD (MSB) = 1:EAD − 1 → EAD dAD → LR
010	dAD (MSB)1:EAD − 1 → EAD dAD → LR
011	EAD − P → EAD dAD (MSB) = 1:EAD − 1 → EAD dAD → LR
100	EAD − P → EAD
101	EAD − P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
110	dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
111	EAD − P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR

Where P = Pitch, LR = Left Rotate, RR = Right Rotate,
EAD = Execute Word Address, and
dAD = Dot Address stored in the Mask Register.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the HGDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

DRAWING PARAMETERS

In preparation for graphics figure drawing, the HGDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the HGDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The HGDC Drawing Controller coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specified details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the HGDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

Drawing Type	DC	D	D2	D1	DM
Initial Value*	0	B	B	−1	−1
Line	$\lvert\Delta I\rvert$	$2\lvert\Delta D\rvert - \lvert\Delta I\rvert$	$2(\lvert\Delta D\rvert - \lvert\Delta I\rvert)$	$2\lvert\Delta D\rvert$	–
Arc**	rsin ϕ	r−1	2(r−1)	−1	rsin $\theta\downarrow$
Rectangle	3	A−1	B−1	−1	A−1
Area Fill	B−1	A	A	–	–
Graphic Character***	B−1	A	A	–	–
Read + Write Data	W−1	–	–	–	–
DMAW	D−1	C−1	–	–	–
DMAR	D−1	C−2	(C−2)/2†	–	–

Notes: All numbers are shown in base 10 for convenience. The HGDC accepts base 2 numbers (2s complement notation) where appropriate.

*Initial values for the various parameters remain as each drawing process ends.

**Circles are drawn with 8 arcs, each of which span 45°, so that $\sin\phi = 1/\sqrt{2}$ and $\sin\theta = 0$.

***Graphic characters are a special case of bit-map area filling in which B and A ≤ 8. If A = 8 there is no need to load D and D2.

Where:

−1= all ONES value.

– = No parameter bytes sent to GDC for this parameter.

ΔI= The larger at Δx or Δy.

ΔD= The smaller at Δx or Δy.

r= Radius of curvature, in pixels.

ϕ= Angle from major axis to end of the arc. $\phi \leq 45°$

θ= Angle from major axis to start of the arc. $\theta \leq 45°$

↑ = Round up to the next higher integer.

↓ = Round down to the next lower integer.

A= Number of pixels in the initially specified direction.

B= Number of pixels in the direction at right angles to the initially specified direction.

W= Number of words to be accessed.

C= Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)

D= Number of words to be accessed in the direction at right angles to the initially specified direction.

DC= Drawing count parameter which is one less than the number of RMW cycles to be executed.

DM= Dots masked from drawing during arc drawing.

†= Needed only for word reads.

GRAPHICS CHARACTER DRAWING

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character display is loaded into the HGDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The HGDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the

drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is narrower than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the HGDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8).

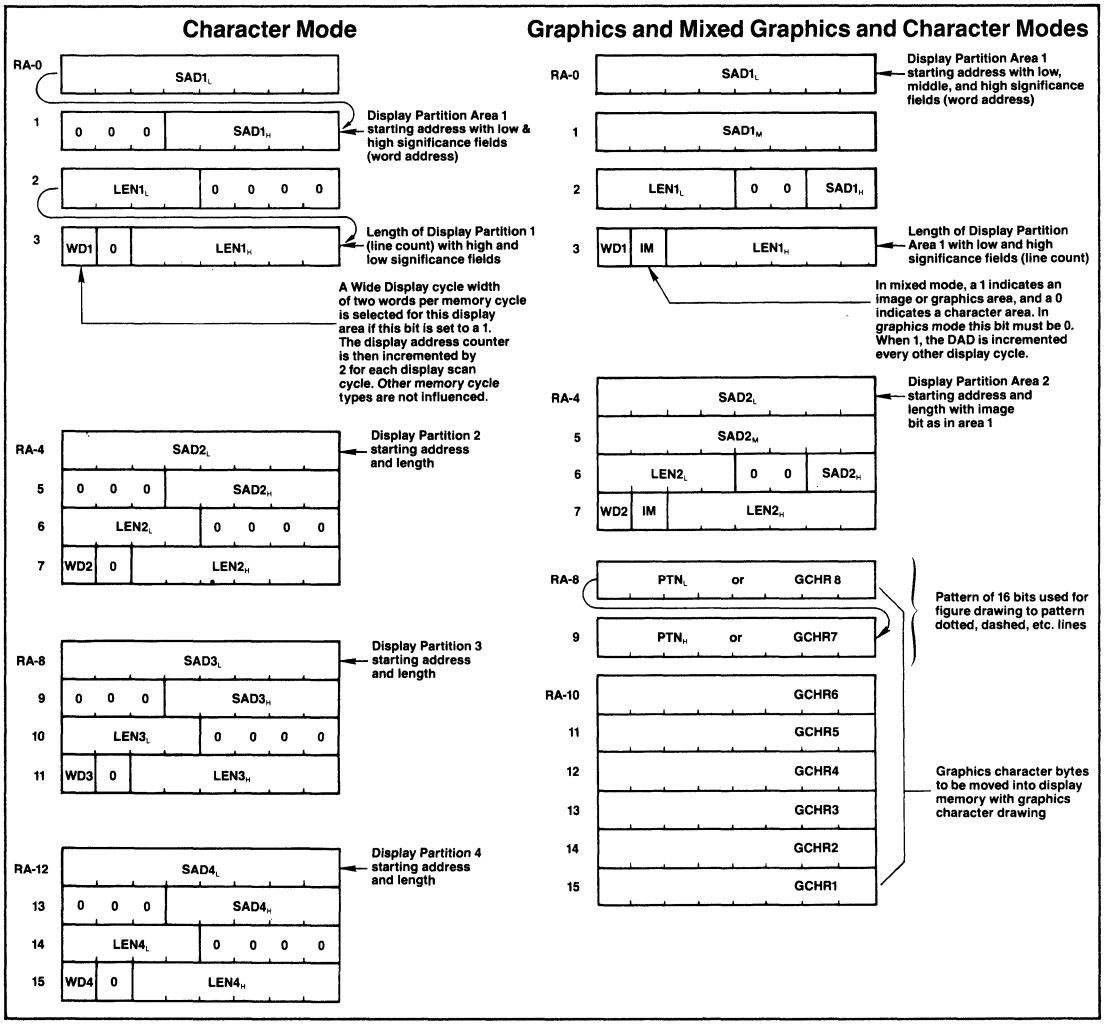
PARAMETER RAM CONTENTS: RAM ADDRESS RA 0 TO 15

The parameters stored in the parameter RAM, PRAM, are available for the HGDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the HGDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

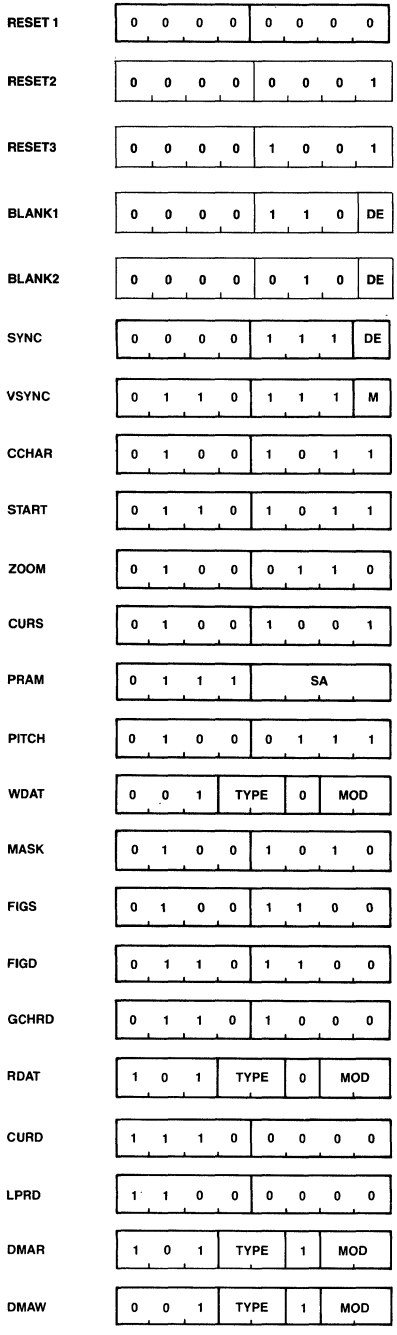
The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the HGDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

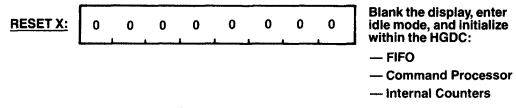


Command Bytes Summary



VIDEO CONTROL COMMANDS

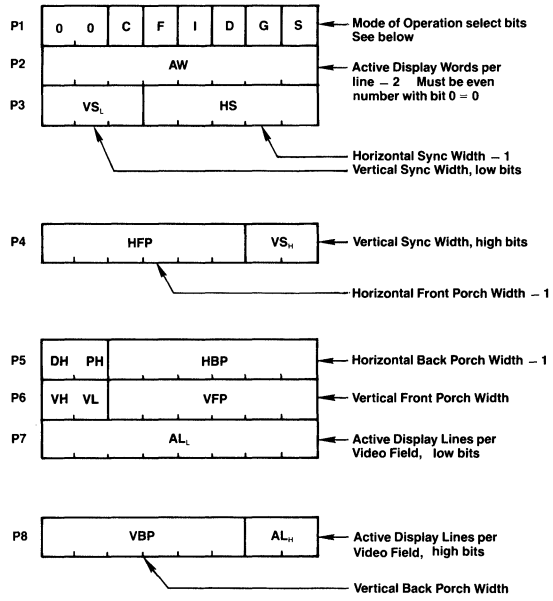
Reset



This command can be executed at any time and does not modify any of the parameters already loaded into the HGDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.

RESET 1: Resync video timing in slave mode.
RESET 2: Blank the display and do not resync.
RESET 3: Unblank the display and do not resync.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical intervals are counted in lines.

If the Drawing Hold (DH) is set to one, pin 21 (LPEN/DH) is used as the drawing hold control pin. When the input to LPEN/DH is held high for over four 2 x WCLK clocks, the drawing address output is temporarily held and the display address is output.

The HGDC allows an even or odd number of lines per frame. Selection is via the VL flag, the seventh bit of the sixth parameter byte following a RESET or SYNC command. When VL is 0, an odd number of display lines is generated.

VL	Number of lines in interlaced mode
0	Odd, as in 7220
1	Even

When VH = 0, status operation is as in CRT 7220.

VH	Blank Status Bit Definition
0	Status register bit 6 indicates Horizontal Blank
1	Status register bit 6 indicates Vertical Blank

PH is the most significant bit (9) of the display pitch parameter. Use the PITCH command to set the lower eight bits.

SYNC GENERATOR PERIOD CONSTRAINTS

Horizontal Back Porch Constraints

1. In general:
   HBP≥3 Display Word Cycles (6 clock cycles).
2. If the Image bit or WD modes change within one video field:
   HBP≥5 Display Word Cycles (10 clock cycles).
3. If interlace, mixed mode, or split screen is used:
   HBP≥5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. In general:
   HFP≥2 Display Word Cycles (4 clock cycles).
2. If the HGDC is used in the video sync Slave mode:
   HFP≥4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP≥6 Display Word Cycles (12 clock cycles).
4. If interlace mode, DMA, or ZOOM is used:
   HFP≥3 Display Word Cycles (6 clock cycles).

Horizontal SYNC Constraints

1. If interlaced display mode is used:
   HS≥5 Display Word Cycles (10 clock cycles).
2. If DRAM Refresh is enabled:
   HS≥2 Display Word Cycles (4 clock cycles).

Modes of Operation Bits

C G	Display Mode
0 0	Mixed Graphics & Character
0 1	Graphics Mode
1 0	Character Mode
1 1	Invalid

I S	Video Framing
0 0	Noninterlaced
0 1	Invalid
1 0	Interlaced Repeat Field for Character Displays
1 1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.

Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.

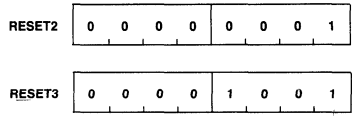
Noninterlaced Framing: 1 field brings all of the information to the screen.

D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

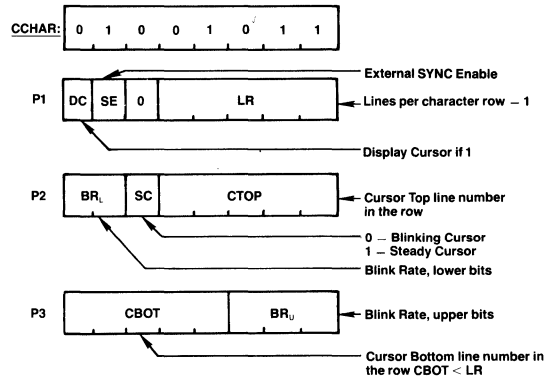
F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.



Both commands allow a reset while presenting reinitialization of the internal sync generator by an external sync source (slave mode).

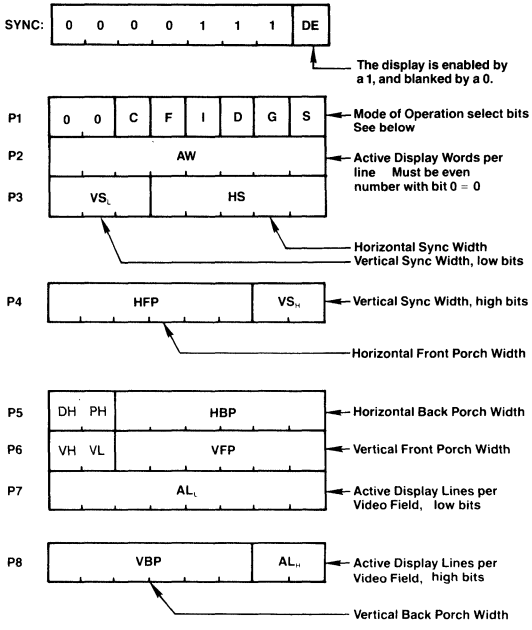
Cursor & Character Characteristics



In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on -¼ off duty cycle. All three parameter bytes must be output for interlace displays, regardless of mode. For interlace displays in graphics mode, the parameter BR_L = 3.

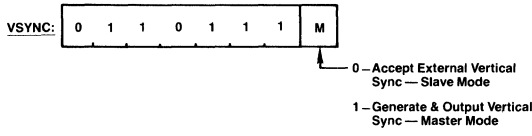
When SE = 0, the HGDC, in slave mode, detects the falling edge of EX. SYNC on the first frame. When SE = 1, the HGDC, in slave mode, detects the falling edge of EX. SYNC on every frame.

SYNC Format Specify



This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The HGDC is not reset nor does it enter idle mode.

Vertical Sync Mode



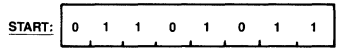
When using two or more HGDCs to contribute to one image, one HGDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all HGDCs are connected together.

A few considerations should be observed when synchronizing two or more HGDCs to generate overlayed video via the V/EXT SYNC pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave HGDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave HGDC to complete the operation before the start of the HSYNC interval.

Once the HGDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master HGDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

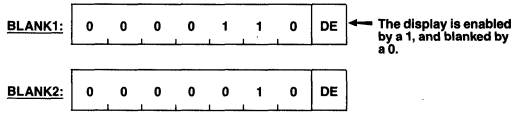
DISPLAY CONTROL COMMANDS

Start Display & End Idle Mode



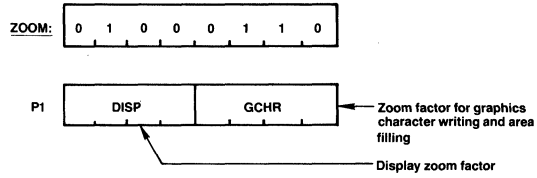
The START command generates the video signals as specified by the RESETX or SYNC command.

Display Blanking Control



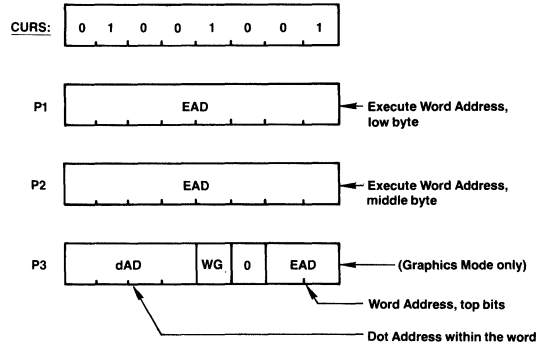
BLANK 2 does not cause the resyncing of an HGDC in slave mode. BLANK 1 does cause the resyncing of an HGDC in slave mode.

Zoom Factors Specify



Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

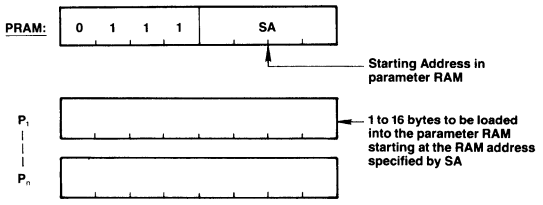
Cursor Position Specify



In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

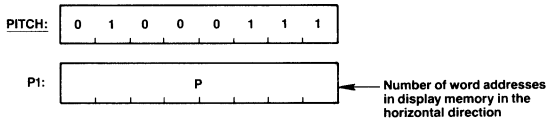
When the WG bit is set to one, any data following the WDAT command is written as is. When the WG bit is set to zero, the 7220A performs as the 7220 does: The pattern written is determined by the least significant bit of each parameter byte following the WDAT command. This bit is expanded into 16 identical bits which form the pattern.

Parameter RAM Load



From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

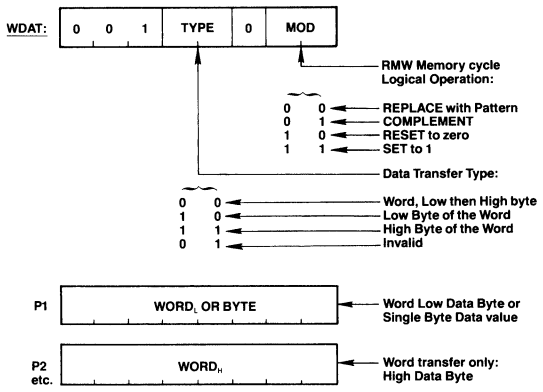


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.

DRAWING CONTROL COMMANDS

Write Data into Display Memory



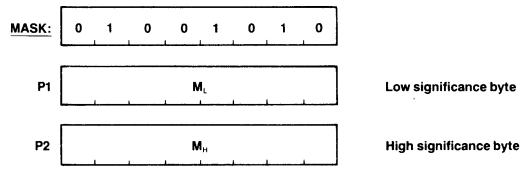
Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. If the WG bit of the third parameter of the CURS command is set to one, any byte following the WDAT command is written as is. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need to be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter + 1 will be the number of RMW cycles done by the HGDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.

Mask Register Load



This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

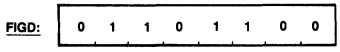
The Mask register is loaded by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 to 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all "ONES" for any "word-at-a-time" operation.

Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted Grapnics Character Drawing and Slanted Area Filling

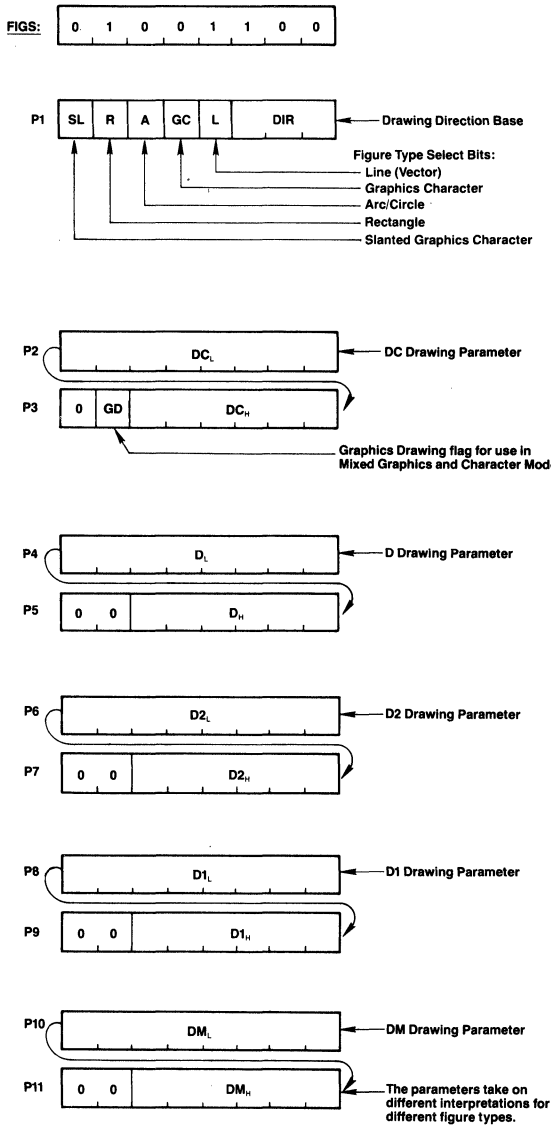
Only these bit combinations assure correct drawing operation.

Figure Draw Start

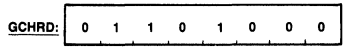


On execution of this instruction, the HGDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

Figure Drawing Parameters Specify



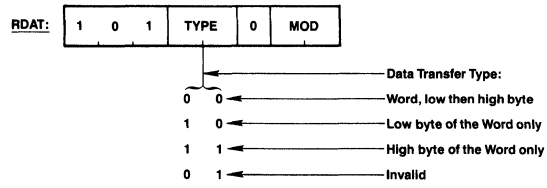
Graphics Character Draw and Area Filling Start



Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

DATA READ COMMANDS

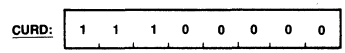
Read Data from Display Memory



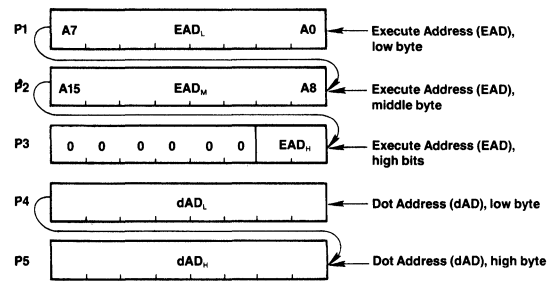
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the HGDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

Cursor Address Read



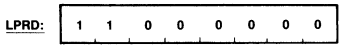
The following bytes are returned by the HGDC through the FIFO:



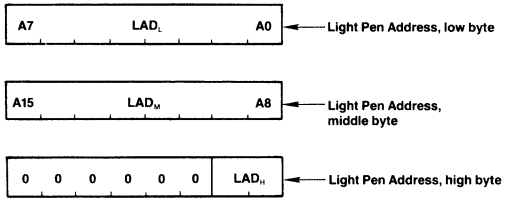
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read



The following bytes are returned by the HGDC through the FIFO:

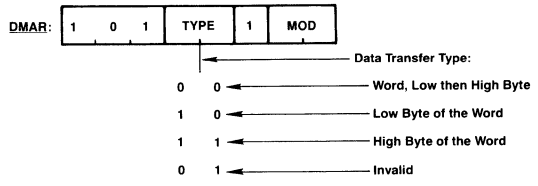


The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

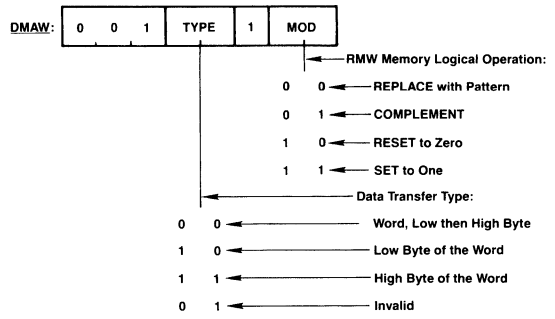
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA CONTROL COMMANDS

DMA Read Request



DMA Write Request



SECTION V

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	①
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	②③
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Low Leak Current (except VSYNC, $\overline{DACK}$)	I_{IL}			−10	μA	V_I = 0V
Input Low Leak Current (VSYNC, $\overline{DACK}$)	I_{IL}			−500	μA	
Input High Leak Current (except LPEN/DH)	I_{IH}			+10	μA	V_I = V_{CC}
Input High Leak Current (LPEN/DH)	I_{IH}			+500	μA	
Output Low Leak Current	I_{OL}			−10	μA	V_O = 0V
Output High Leak Current	I_{OH}			−10	μA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5		0.6	V	
Clock Input High Voltage	V_{CH}	3.5		V_{CC} − 1.0	V	
V_{CC} Supply Current	I_{CC}			270	mA	

CAPACITANCE T_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	V_I (unmeasured) = 0V
Output Capacitance	C_{OUT}			20	pF	
Clock Input Capacitance	Cf			20	pF	

Notes:
① For 2XWCLK, V_{IL} = −0.5V to +0.6V. ② For 2XWCLK, V_{IH} = +3.9V to V_{CC} + 1.0V. ③ For $\overline{WR}$, V_{IH} = 2.5V to V_{CC} + 0.5V.

AC Characteristics, T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Read Cycle (HGDC↔CPU)

Parameter	Symbol	7220AD Min	7220AD Max	7220AD-1 Min	7220AD-1 Max	7220AD-2 Min	7220AD-2 Max	Unit	Test Conditions
Address Setup to $\overline{RD}$ ↓	t_{AR}	0		0		0		ns	
Address Hold from $\overline{RD}$ ↑	t_{RA}	0		0		0		ns	
$\overline{RD}$ Pulse Width	t_{RR1}	t_{RD1} + 20	t_{RCY}-½ t_{CLK}	t_{RD1} + 20	t_{RCY}-½t_{CLK}	t_{RD1} + 20	t_{RCY}-½t_{CLK}	ns	
Data Delay from $\overline{RD}$ ↓	t_{RD1}		75		65		55	ns	C_L = 50 pF
Data Floating from $\overline{RD}$ ↑	t_{DF}	0	75	0	65	0	55	ns	
$\overline{RD}$ Pulse Cycle	t_{RCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

Write Cycle (HGDC↔CPU)

Parameter	Symbol	7220AD Min	7220AD Max	7220AD-1 Min	7220AD-1 Max	7220AD-2 Min	7220AD-2 Max	Unit	Test Conditions
Address Setup to $\overline{WR}$ ↓	t_{AW}	0		0		0		ns	
Address Hold from $\overline{WR}$ ↑	t_{WA}	10		10		10		ns	
$\overline{WR}$ Pulse Width	t_{WW}	80	t_{WCY} − t_{CLK}	70	t_{WCY} − t_{CLK}	60	t_{WCY} − t_{CLK}	ns	
Data Setup to $\overline{WR}$↑	t_{DW}	65		55		45		ns	
Data Hold from $\overline{WR}$	t_{WD}	10		10		10		ns	
$\overline{WR}$ Pulse Cycle	t_{WCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

DMA Read Cycle (HGDC↔CPU)

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
DACK Setup to $\overline{RD}$ ↓	t_{KR}	0		0		0		ns	
DACK Hold from $\overline{RD}$ ↑	t_{RK}	0		0		0		ns	
$\overline{RD}$ Pulse Width	t_{RR2}	t_{RD2} + 20		t_{RD2} + 20		t_{RD2} + 20		ns	
Data Delay from $\overline{RD}$ ↓	t_{RD2}		1.5 t_{CLK} + 80		1.5 t_{CLK} + 70		1.5 t_{CLK} + 60	ns	C_L = 50 pF
DREQ Delay from 2XWCLK ↑	t_{REQ}		100		85		75	ns	C_L = 50 pF
DREQ Setup to $\overline{DACK}$ ↓	t_{QK}	0		0		0		ns	
$\overline{DACK}$ High Level Width	t_{DK}	t_{CLK}		t_{CLK}		t_{CLK}		ns	
$\overline{DACK}$ Pulse Cycle	t_E	4 t_{CLK}*		4 t_{CLK}*		4 t_{CLK}*		ns	
DREQ ↓ Delay from $\overline{DACK}$ ↓	$t_{KQ(R)}$		t_{CLK} + 100		t_{CLK} + 90		t_{CLK} + 80	ns	C_L = 50 pF
$\overline{DACK}$ Low-level Width	t_{LK}	2t_{CLK}		2t_{CLK}		2t_{CLK}		ns	

*for high byte and low byte transfers: t_E = 5 t_{CLK}

DMA Write Cycle (GDC↔CPU)

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
DACK Setup to WR ↓	t_{KW}	0		0		0		ns	
DACK Hold from WR ↑	t_{WK}	0		0		0		ns	

R/M/W Cycle (GDC↔Display Memory)

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address/Data Delay from 2XWCLK ↑	t_{AD}	20	105	20	90	15	80	ns	C_L = 50 pF
Address/Data Floating from 2XWCLK ↑	t_{OFF}	20	105	20	90	15	80	ns	C_L = 50 pF
Input Data Setup to 2XWCLK ↓	t_{DIS}	0		0		0		ns	
Input Data Hold from 2XWCLK ↓	t_{DIH}	t_{DE}		t_{DE}		t_{DE}		ns	
DBIN Delay from 2XWCLK ↓	t_{DE}	20	80	20	70	15	60	ns	C_L = 50 pF
ALE ↑ Delay from 2XWCLK ↑	t_{RR}	20	80	20	70	15	60	ns	C_L = 50 pF
ALE ↓ Delay from 2XWCLK ↓	t_{RF}	20	65	20	55	15	50	ns	C_L = 50 pF
ALE Width	t_{RW}	⅓ t_{CLK}		⅓ t_{CLK}		⅓ t_{CLK}		ns	C_L = 50 pF
ALE Low Width	t_{RL}	1.5t_{CLK} − 30		1.5t_{CLK} − 30		1.5t_{CLK} − 30		ns	
Address Setup to ALE ↓	t_{AA}	30		30		30		ns	

Display Cycle (GDC↔Display Memory)

Parameter	Symbol	7220D Limits		7220D-1 Limits		7220D-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Video Signal Delay from 2XWCLK ↑	t_{VD}		90		80		70	ns	C_L = 50 pF

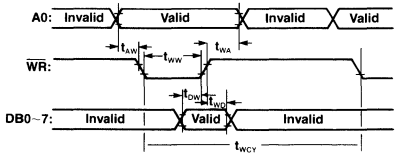
Input Cycle (GDC↔Display Memory)

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Input Signal Setup to 2XWCLK ↑	t_{PS}	10		10		10		ns	
Input Signal Width	t_{PW}	t_{CLK}		t_{CLK}		t_{CLK}		ns	

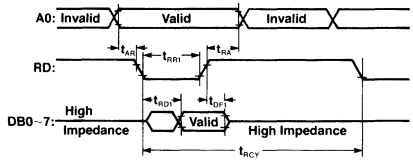
Clock (2XWCLK)

Parameter	Symbol	7220AD Limits		7220AD-1 Limits		7220AD-2 Limits		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Clock Rise Time	t_{CR}		15		15		15	ns	
Clock Fall Time	t_{CF}		15		15		15	ns	
Clock High Pulse Width	t_{CH}	70		61		52		ns	
Clock Low Pulse Width	t_{CL}	70		61		52		ns	
Clock Cycle	t_{CLK}	165	10,000	145	10,000	125	10,000	ns	

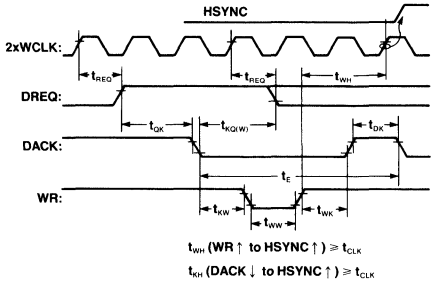
Microprocessor Interface Write Timing



Microprocessor Interface Read Timing



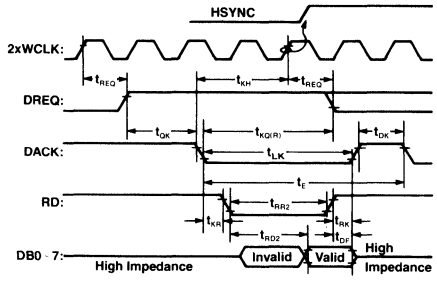
Microprocessor Interface DMA Write Timing



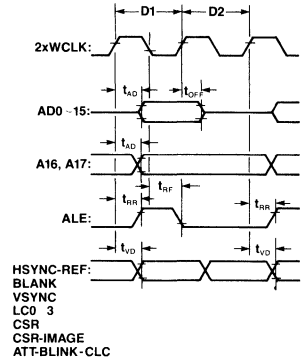
t_{WH} (WR ↑ to HSYNC ↑) ≥ t_{CLK}

t_{KH} (DACK ↓ to HSYNC ↑) ≥ t_{CLK}

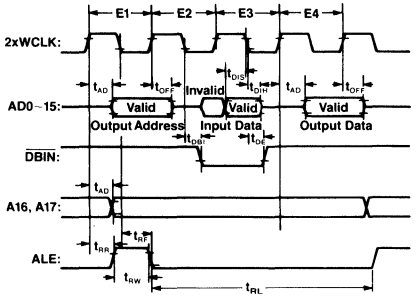
Microprocessor Interface DMA Read Timing



Display Memory Display Cycle Timing

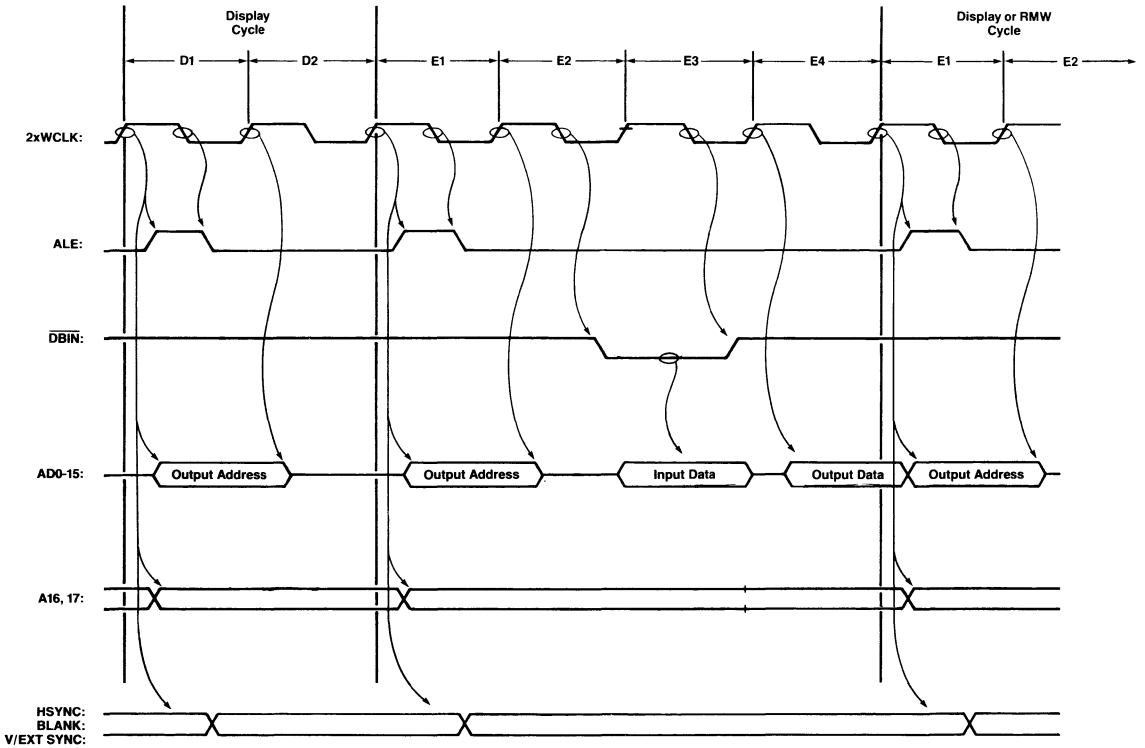


Display Memory RMW Timing



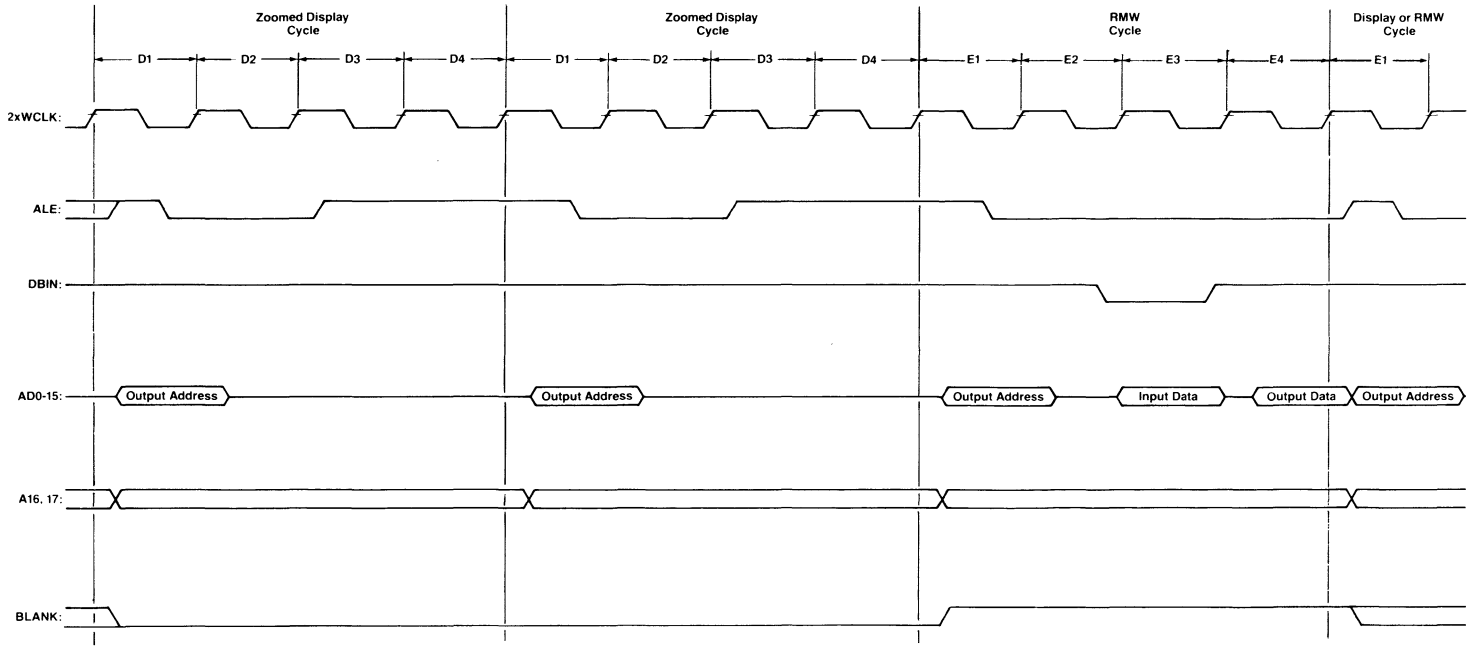
TIMING WAVEFORMS

Display and RMW Cycles (1x Zoom)

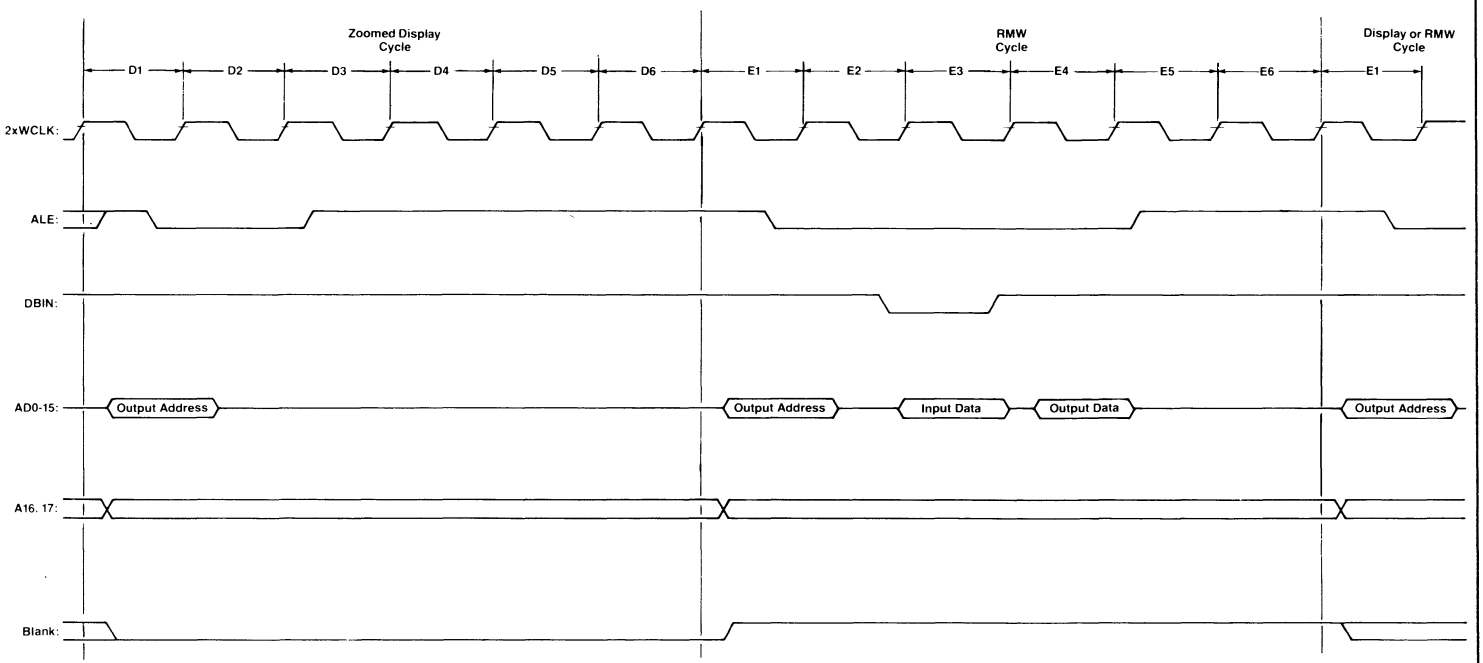


TIMING WAVEFORMS

Display and RMW Cycles (2x Zoom)

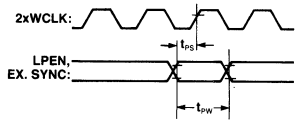


Zoomed Display Operation with RMW Cycle (3x Zoom)

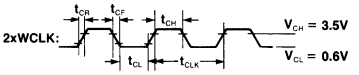


TIMING WAVEFORMS

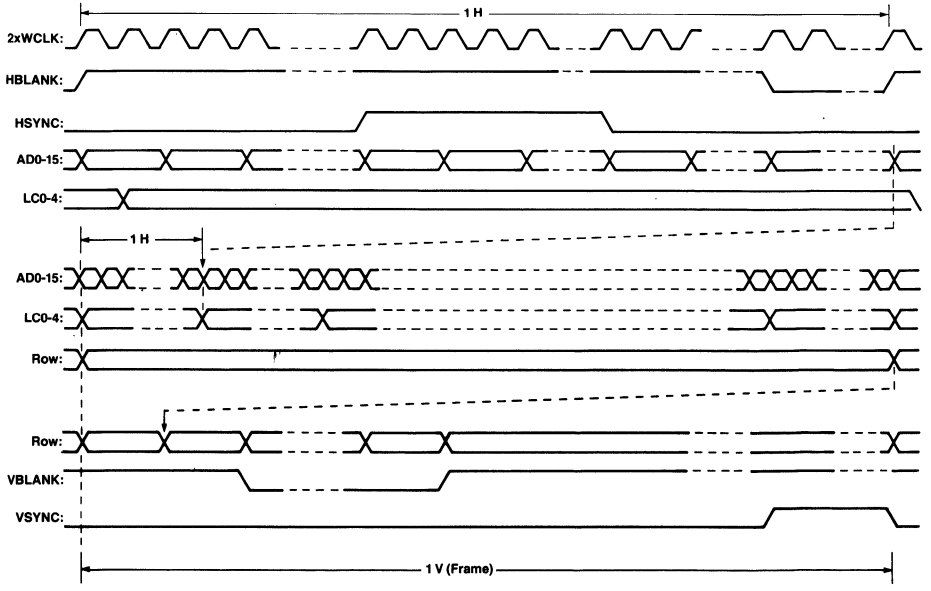
Light Pen and External Sync Input Timing



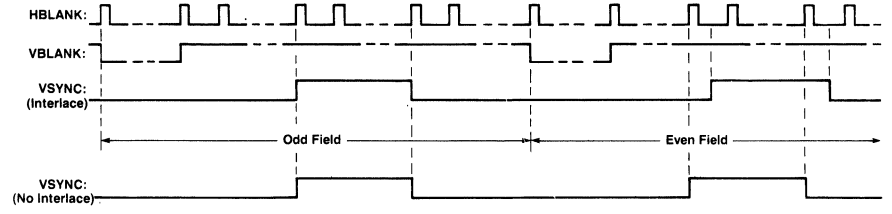
Clock Timing (2XWCLK)



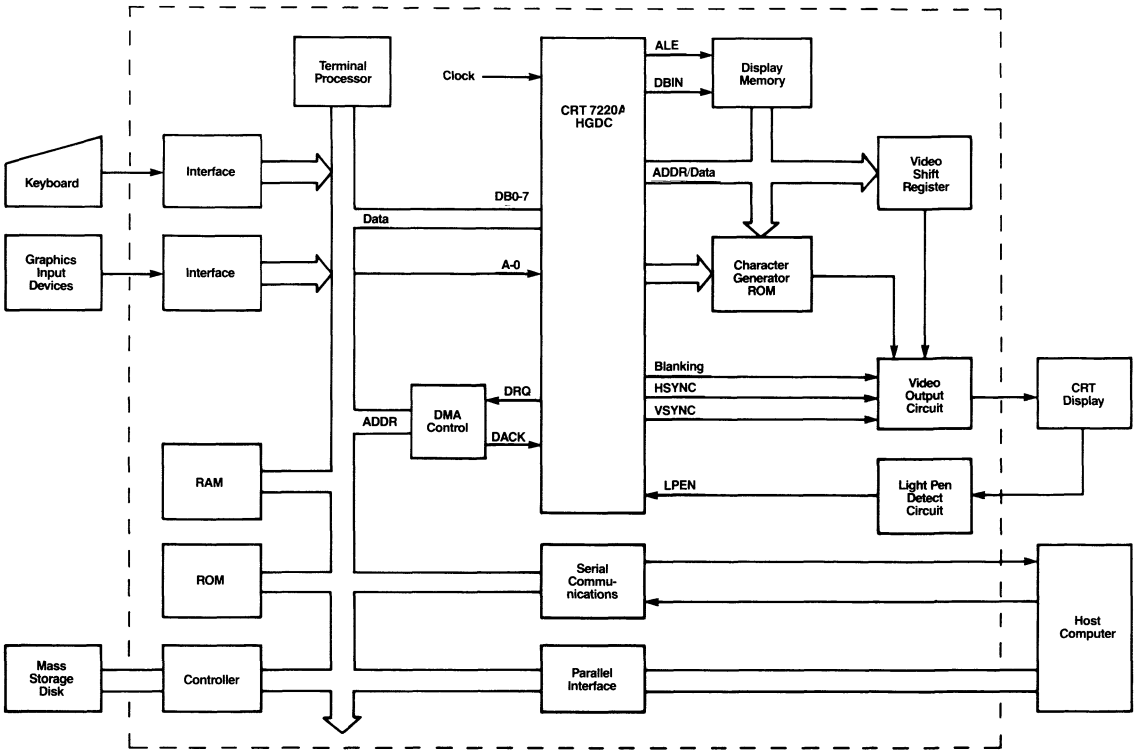
Video Sync Signals Timing



Interlaced Video Timing

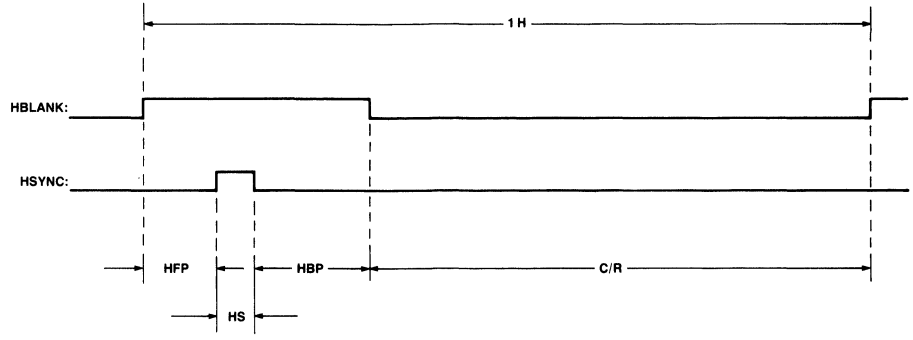


TIMING WAVEFORMS

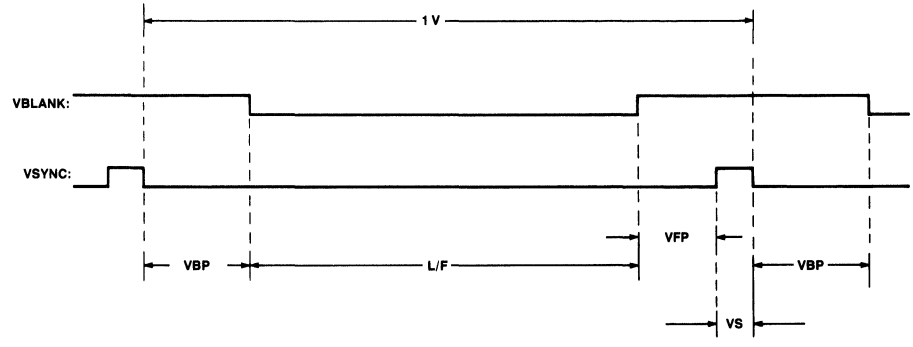


BLOCK DIAGRAM OF A GRAPHICS TERMINAL

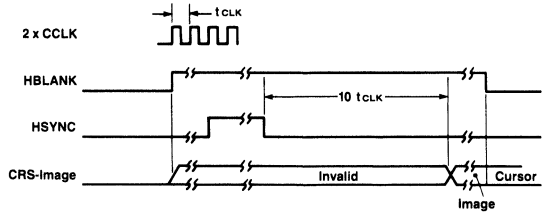
Video Horizontal Sync Generator Parameters



Video Vertical Sync Generator Parameters

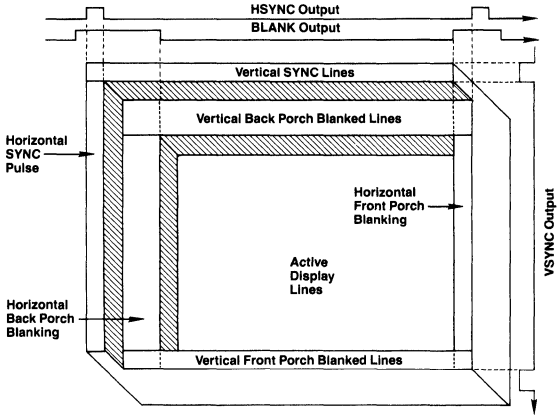


Cursor—Image Bit Flag

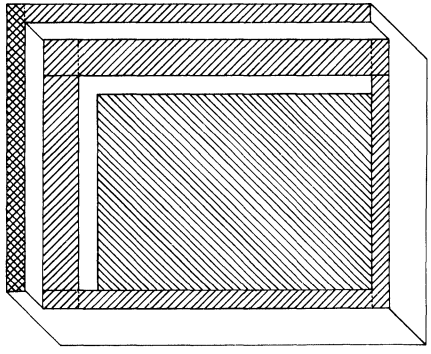


TIMING WAVEFORMS

VIDEO FIELD TIMING



DRAWING INTERVALS

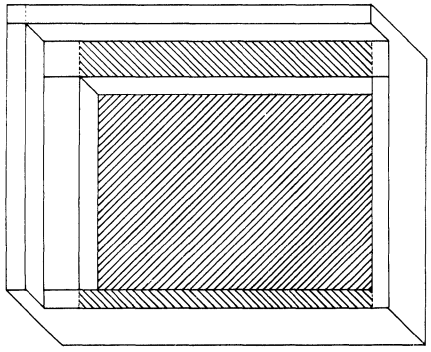


Drawing Interval

Additional Drawing Interval When in Flash Mode

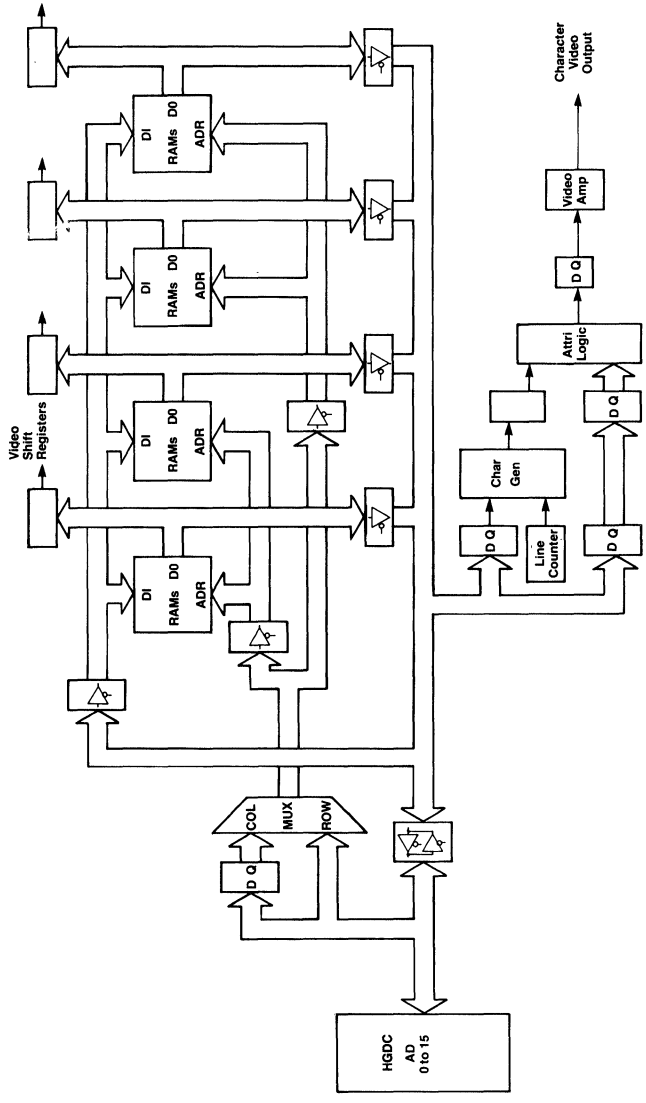
Dynamic RAM Refresh if Enabled, Otherwise Additional Drawing Interval

DMA REQUEST INTERVALS



DMA Request Interval

Additional DMA Request Intervals When in Flash Mode



MULTIPLANE DISPLAY MEMORY DIAGRAM

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

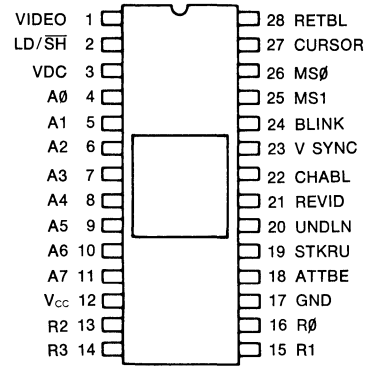
CRT 8002
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
    - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

PIN CONFIGURATION



SECTION V

General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC™ is a companion chip to SMC's CRT 5027 VTAC. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 15Hz to 1Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5Hz to 0.5Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

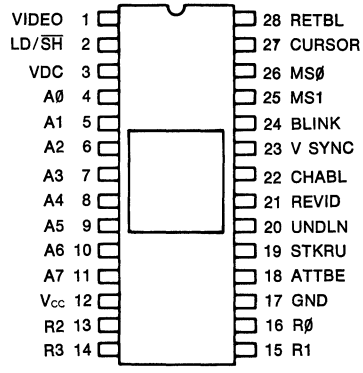
CRT 8002H

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency 25 MHz
- ☐ ROM Access time 310 ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ On chip cursor
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM

PIN CONFIGURATION



- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ N-channel COPLAMOS® Titanium Disilicide Process
- ☐ Compatible with CRT 5027/37 VTAC®

SECTION V

General Description

The SMC CRT 8002H Video Display Attributes Controller (VDAC) is an n-channel COPLAMOS® MOS/LSI device. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002H VDAC is a companion chip to SMC's CRT 5027/37 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002H video output may be connected directly to a CRT monitor video input. The CRT 5027/37 blanking output can be connected directly to the CRT 8002H retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

The CRT 8002H attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002H produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002H can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

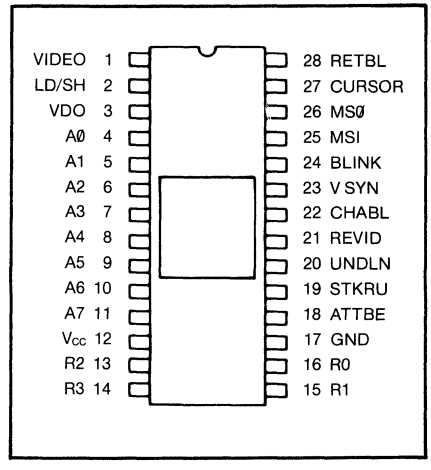
CRT 8021
CRT 8021-003

CRT Video Attributes Controller
Video Generator
VAC

FEATURES

- ☐ ON CHIP VIDEO SHIFT REGISTER
  Maximum shift register frequency—20MHz
  Maximum character clock rate—2.5MHz
- ☐ ON CHIP HORIZONTAL AND VERTICAL RETRACE VIDEO BLANKING
- ☐ ON CHIP GRAPHICS GENERATION
- ☐ ON CHIP ATTRIBUTE LOGIC-CHARACTER, FIELD
  Reverse video
  Character blank
  Character blink
  Underline
  Strike-thru
- ☐ ON CHIP BLINKING CURSOR
- ☐ ON CHIP DATA BUFFER
- ☐ ON CHIP ATTRIBUTE BUFFER
- ☐ +5 VOLT OPERATION
- ☐ TTL COMPATIBLE
- ☐ MOS N-CHANNEL SILICON-GATE COPLAMOS® PROCESS

PIN CONFIGURATION



- ☐ COMPATIBLE WITH CRT 5027/37 VTAC® AND CRT 9007 VPAC

GENERAL DESCRIPTION

The SMC CRT 8021 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device. It contains wide and thin graphics logic, attributes logic, a data latch, field and character attribute latch, a blinking cursor, and a high speed video shift register. The CRT 8021 VAC is a companion to SMC's CRT 5027/37 VTAC® or CRT 9007 VPAC. The CRT 8021 and a character ROM combined with either a CRT 5027/37 or a CRT 9007 comprises the major circuitry required for the display portion of a CRT video terminal.

The CRT 8021 video output may be connected directly to a CRT monitor video input. The CRT 5027/37 or CRT 9007 blanking output can be connected directly to the CRT 8021 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

A blinking cursor is available on the CRT 8021. There is a separate cursor blink rate which is twice the character blink rate and has a duty cycle of 50/50.

The CRT 8021 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions. These attributes are available in all modes.

The thin graphic mode enables the user to create single line drawings and forms.

In the wide graphic mode the CRT 8021 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing 256 unique graphic symbols. Thus, the CRT 8021 can produce either alphanumeric symbols or various graphic entities depending on the mode selected. The mode can be changed on a per character basis.

The CRT 8021 is available in two versions. The CRT 8021 provides an eight-part graphic entity which fills the character block. The CRT 8021 is designed for seven dot wide, nine or eleven dot high characters in nine by twelve or ten by twelve character blocks.

The CRT 8021-003 provides a six part graphic entity for five by seven or five by nine characters in character blocks of up to seven by ten dots.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

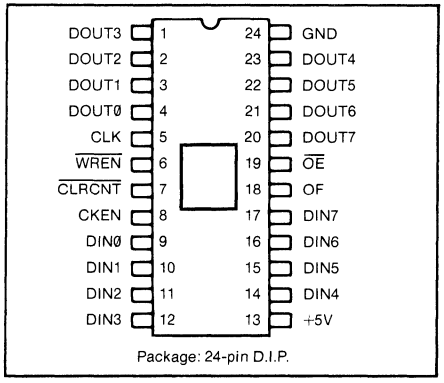
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

Single Row Buffer
SRB

EATURES:

-] Low Cost Solution to CRT Memory Contention Problem
-] Provides Enhanced Processor Throughput for CRT Display Systems
-] Provides 8 Bit Wide Variable Length Serial Memory
-] Permits Active Video on All Scan Lines of Data Row
-] Dynamically Variable Number of Characters per Data Row— ...64, 80, 132,...up to a Maximum of 135
-] Cascadable for Data Rows Greater than 135 Characters
-] Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
-] Three-State Outputs
-] 3.3MHz Typical Read/Write Data Rate
-] Static Operation
-] Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
-] 24 Pin Dual In Line Package
-] +5 Volt Only Power Supply
-] TTL Compatible Inputs and Outputs
-] Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



Package: 24-pin D.I.P.

APPLICATIONS:

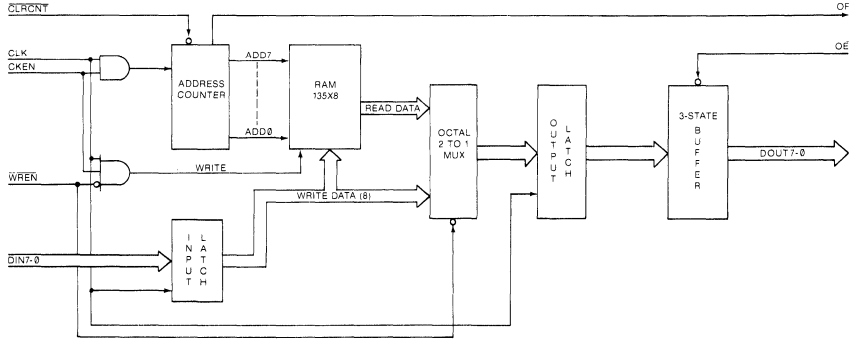
- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION V

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.

The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-4	DATA OUTPUTS	DOUT3-DOUTØ	Data Outputs from the internal output latch.
5	CLOCK	CLK	Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter.
6	WRITE ENABLE	$\overline{\text{WREN}}$	When $\overline{\text{WREN}}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM.
7	CLEAR COUNTER	$\overline{\text{CLRCNT}}$	A negative transition on $\overline{\text{CLRCNT}}$ clears the RAM address counter. $\overline{\text{CLRCNT}}$ is normally asserted low near the beginning of each scan line.
8	CLOCK ENABLE	CKEN	When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM.
9-12	DATA INPUTS	DINØ-DIN3	Data Inputs from system memory.
13	POWER SUPPLY	V_{CC}	+5 Volt supply.
14-17	DATA INPUTS	DIN4-DIN7	Data Inputs from system memory.
18	OVERFLOW FLAG	OF	This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip.
19	OUTPUT ENABLE	$\overline{\text{OE}}$	When $\overline{\text{OE}}$ is low, the data outputs DOUTØ-DOUT7 are enabled. When $\overline{\text{OE}}$ is high, DOUTØ-DOUT7 present a high impedance state.
20-23	DATA OUTPUTS	DOUT7-DOUT4	Data Outputs from the internal output latch.
24	GROUND	GND	Ground.

OPERATION

For CRT operation, the Write Enable ($\overline{\text{WREN}}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{\text{CLRCNT}}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{\text{CLRCNT}}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{\text{WREN}}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... -55° C to + 150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS ($T_A = 0°$ C to 70° C, $V_{CC} = +5 \pm 5\%$, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	$I_{OL} = 2mA$
High Level V_{OH}	2.4			V	$I_{OH} = -100\mu A$
Input Current Leakage, I_{IL}			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output '1' Leakage			10	μA	
Output '0' Leakage (Off State)			10	μA	
Input Capacitance					
CLK		30	45	pF	
All other inputs		10	15	pF	
Power Supply Current					
I_{CC} (SRB-135)			115	mA	
I_{CC} (SRB-83)			100	mA	
AC CHARACTERISTICS					
t_{cy}					
(SRB135)	300	250		ns	
(SRB83)	400	330		ns	
t_{CKL}					
(SRB135)	240	190	DC	ns	
(SRB83)	320	250	DC	ns	
t_{CKH}					
(SRB135)	28		5000	ns	
(SRB83)	34		5000	ns	
t_{CKR}					
(SRB135)			10	ns	$t_{CKH} = 28ns$
(SRB83)			10	ns	$t_{CKH} = 34ns$
t_{CKF}					
(SRB135)			10	ns	$t_{CKL} = 240ns$
(SRB83)			10	ns	$t_{CLK} = 320ns$
t_{DSET}	65			ns	
t_{DHOLD}	5			ns	
t_{ENCKP}	0			ns	
t_{ENCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{ENHOLD}	0			ns	
t_{WRCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{WENHLD}	0			ns	
t_{DOUT}			175	ns	$C_L = 50pF$
t_{TSON}			175	ns	
t_{TSOFF}			175	ns	
t_{OFON}			175	ns	$C_L = 30pF$
t_{CLRS}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{CLRH}	0			ns	

FIGURE 1: AC CHARACTERISTICS

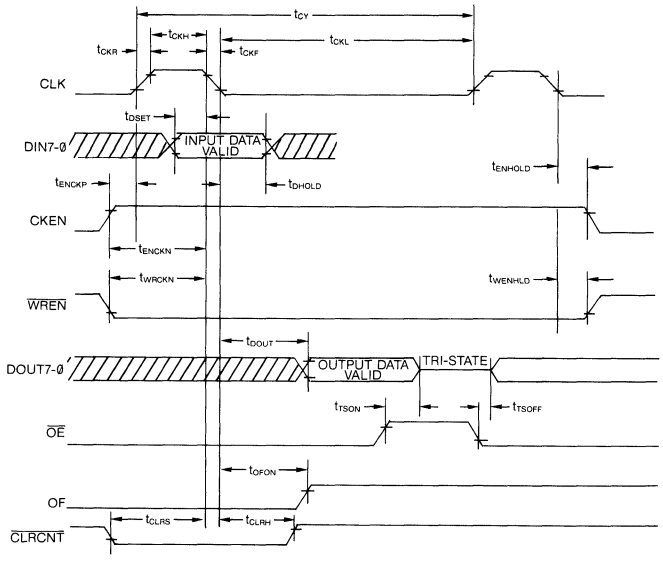
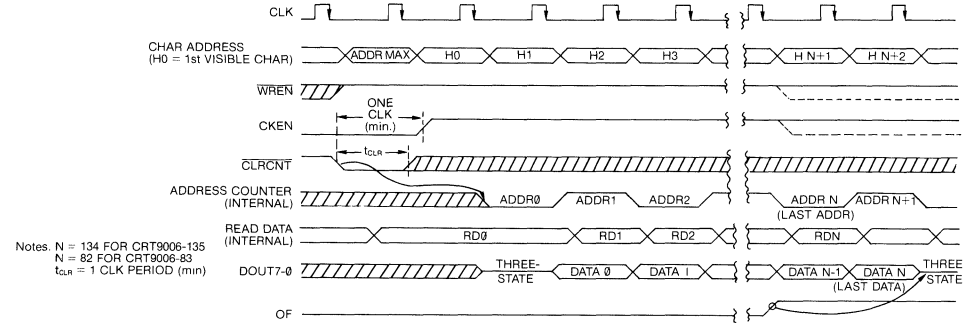
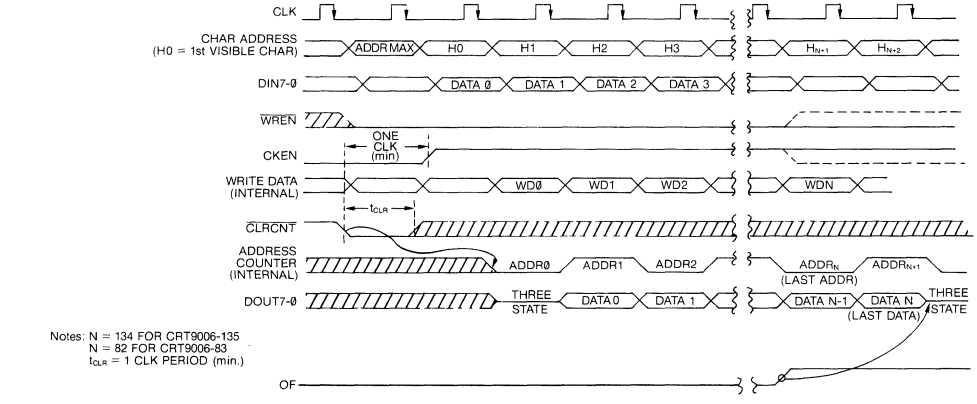


FIGURE 2: SINGLE ROW BUFFER READ TIMING



Notes. N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
t_{CLR} = 1 CLK PERIOD (min)

FIGURE 3: SINGLE ROW BUFFER WRITE TIMING



Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
t_{CLR} = 1 CLK PERIOD (min.)

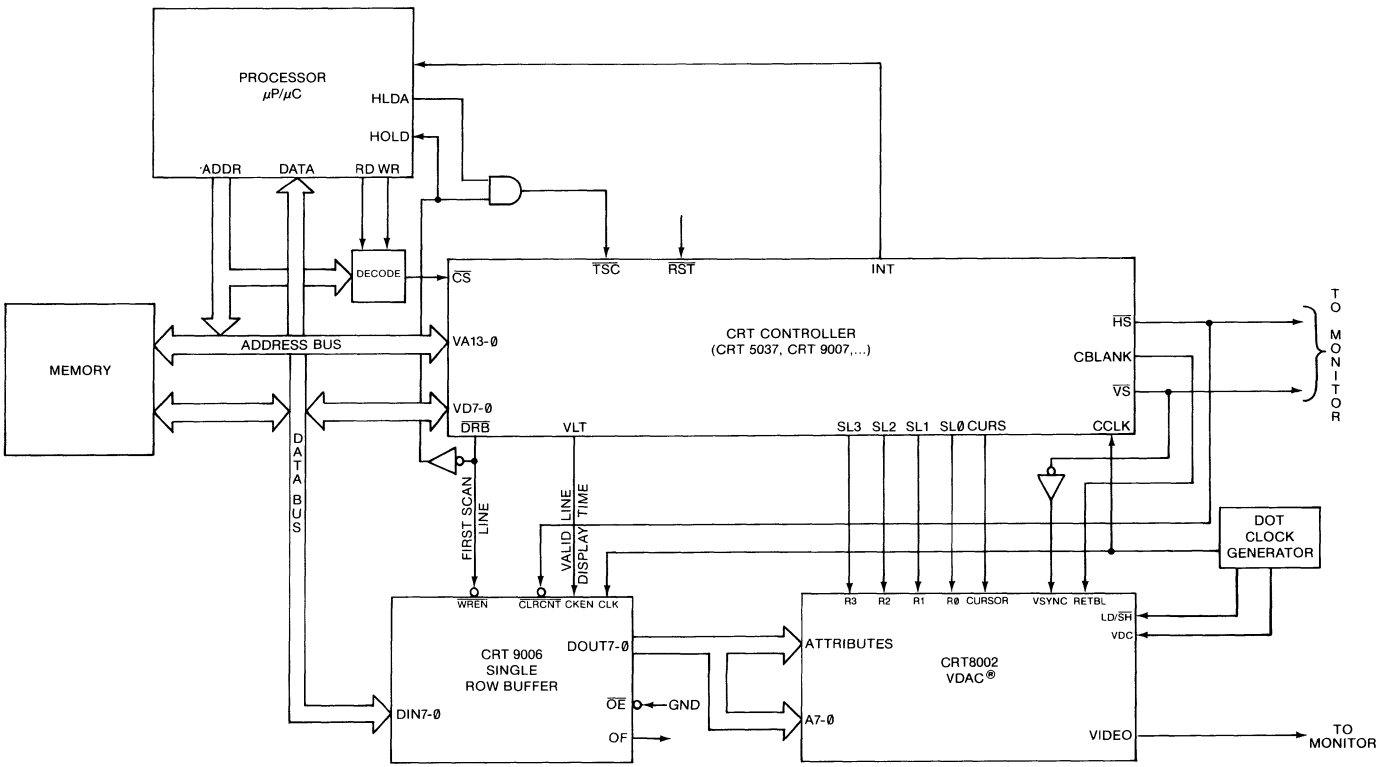
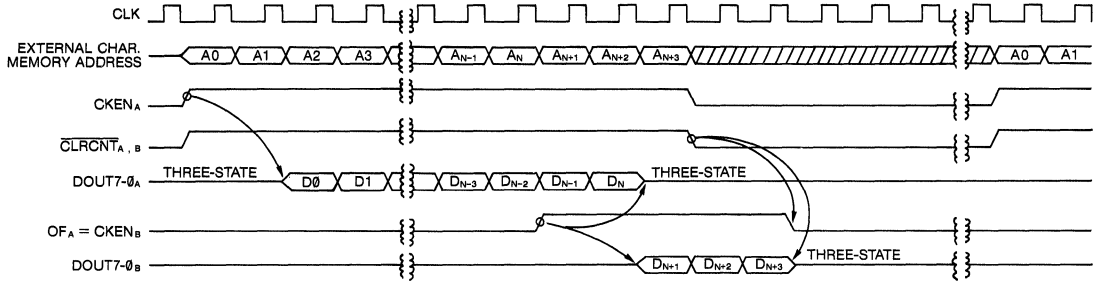


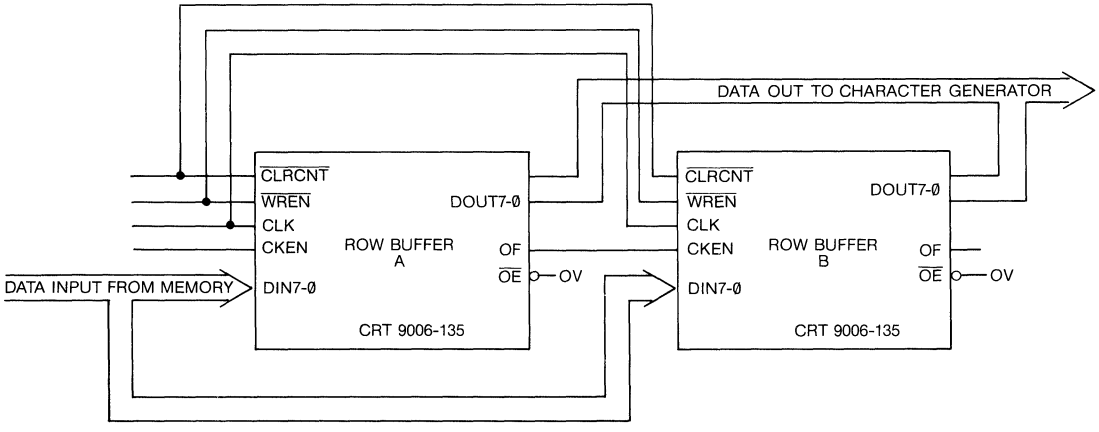
FIGURE 2: TYPICAL CRT CONTROLLER CONFIGURATION WITH SINGLE ROW BUFFER

FIGURE 4:
TYPICAL READ TIMING FOR SRB CASCADED CONFIGURATION



Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
EXAMPLE IS FOR N+3 CHARACTERS TOTAL
A, B REFER TO DEVICES A&B IN FIGURE 5

FIGURE 5:
TYPICAL CASCADE OF SINGLE ROW BUFFERS—270 BYTES TOTAL



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

CRT9007A2*
CRT9007A1*
CRT9007A
CRT9007B
CRT9007C

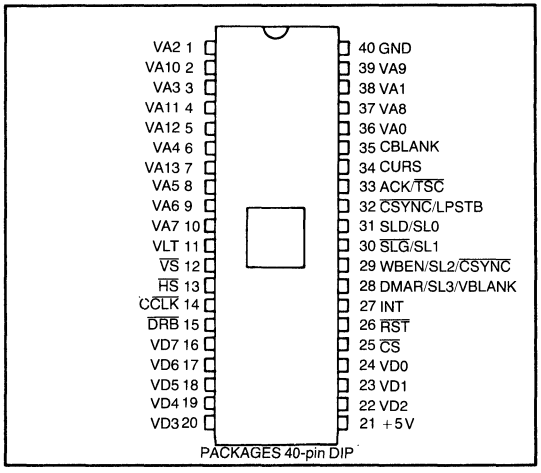
*PRELIMINARY

CRT Video Processor and Controller VPAC™

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch — Horizontal (Negative or Positive)
  - — Vertical
  - Sync Width — Horizontal (1-128 Character Times)
  - — Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
  - — Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

SECTION V

GENERAL DESCRIPTION

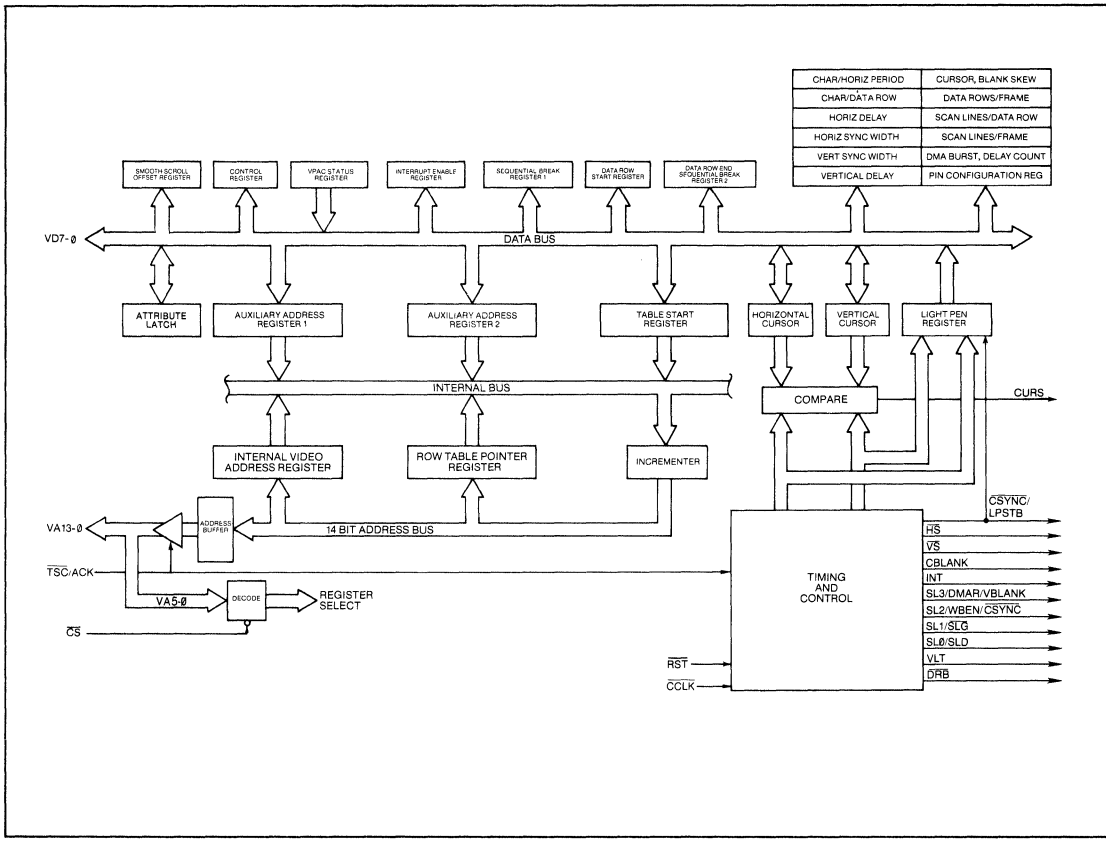
The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".



DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output: this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra $\overline{DRB}$ signal which will become active during the first scan line of the vertical retrace interval.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SLØ are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with SLD (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VAØ in their high impedance state.

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately $[(N-1)/N] \times 100$ where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

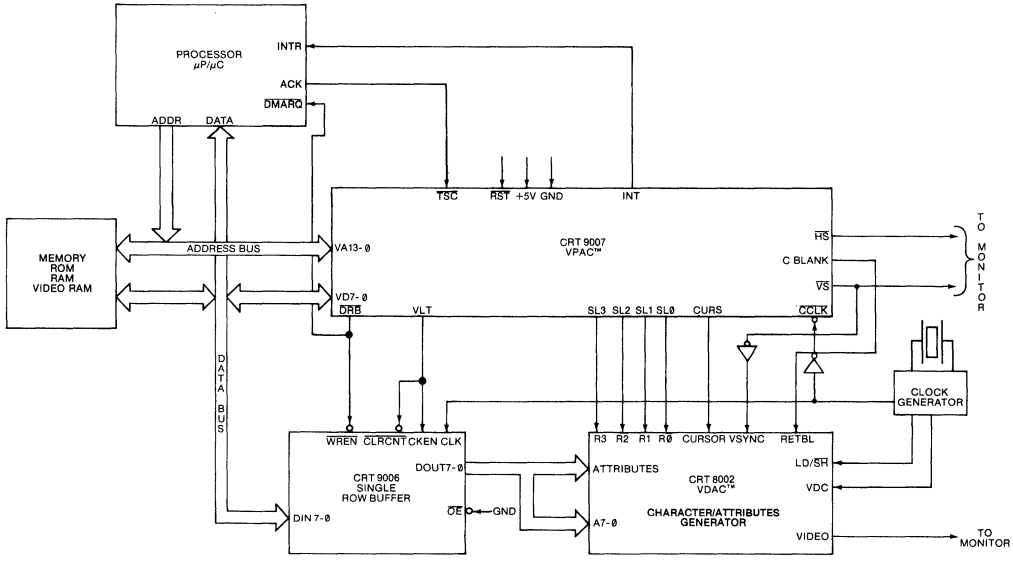


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

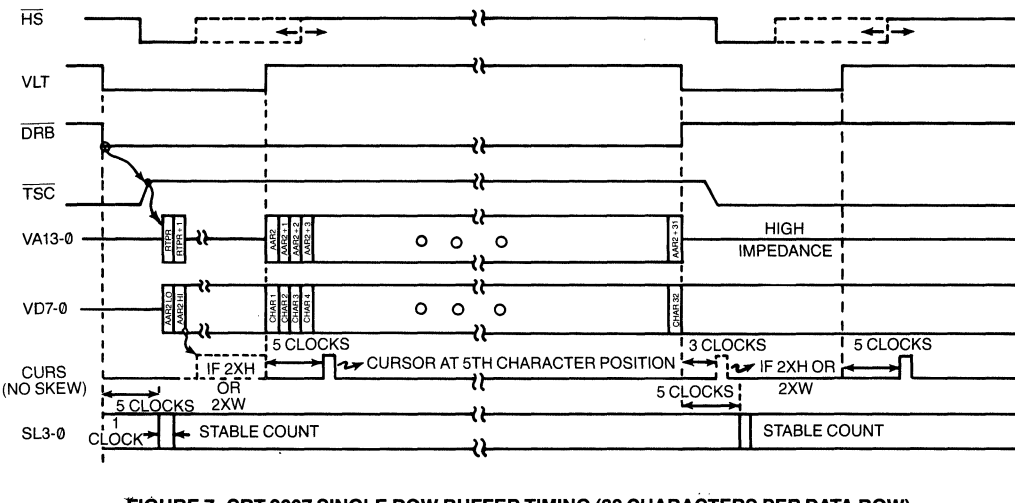


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

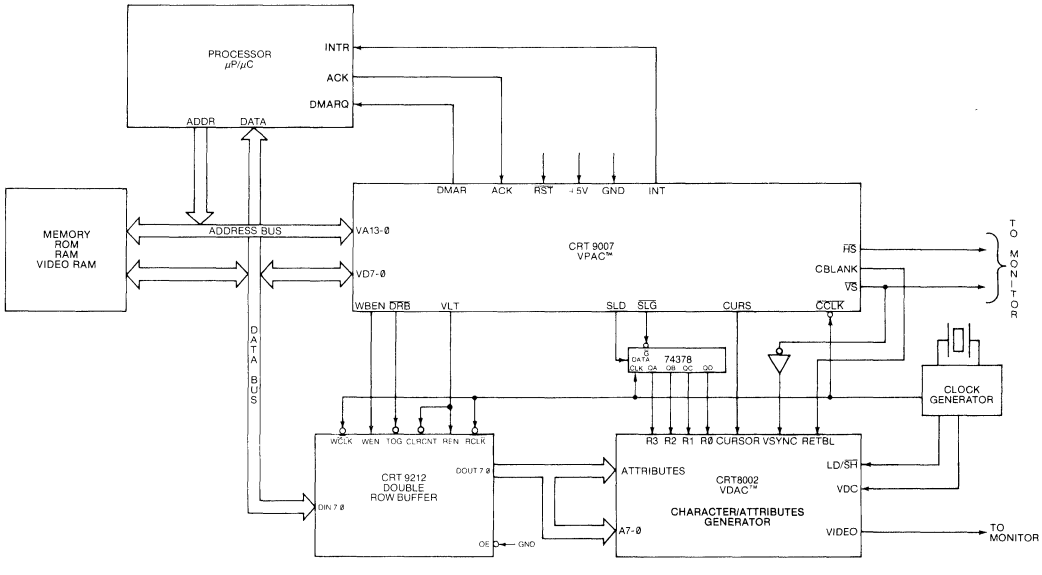


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

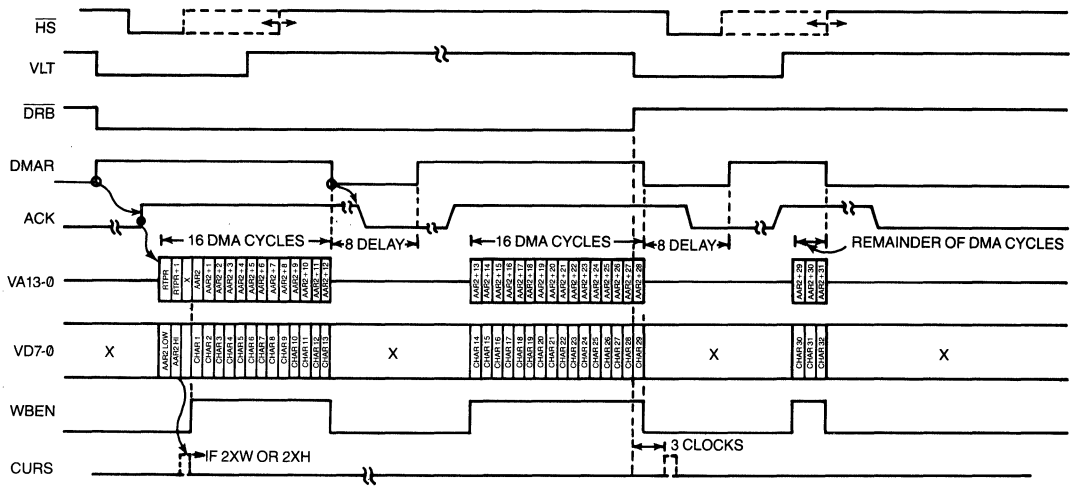


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

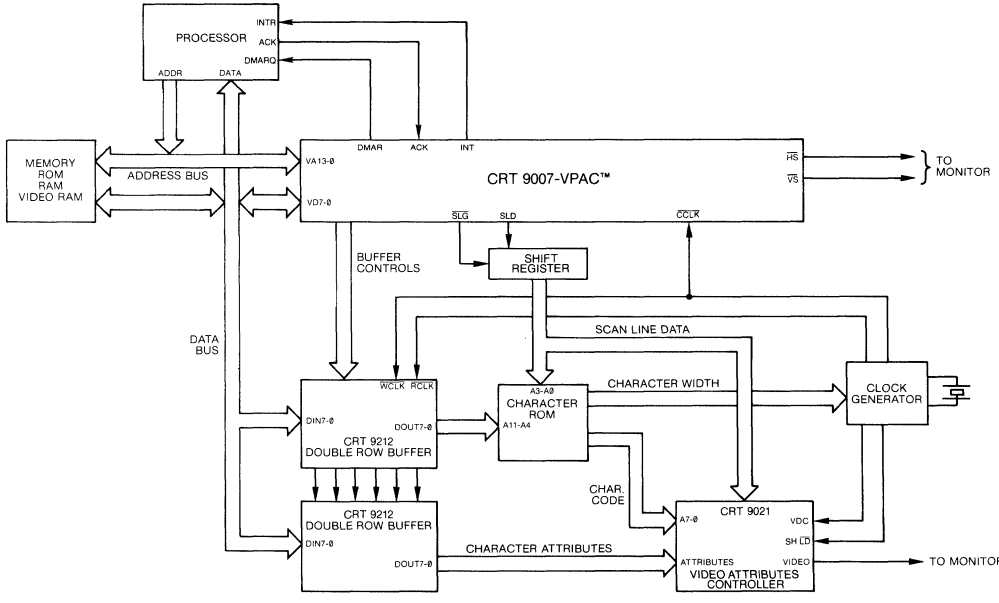


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

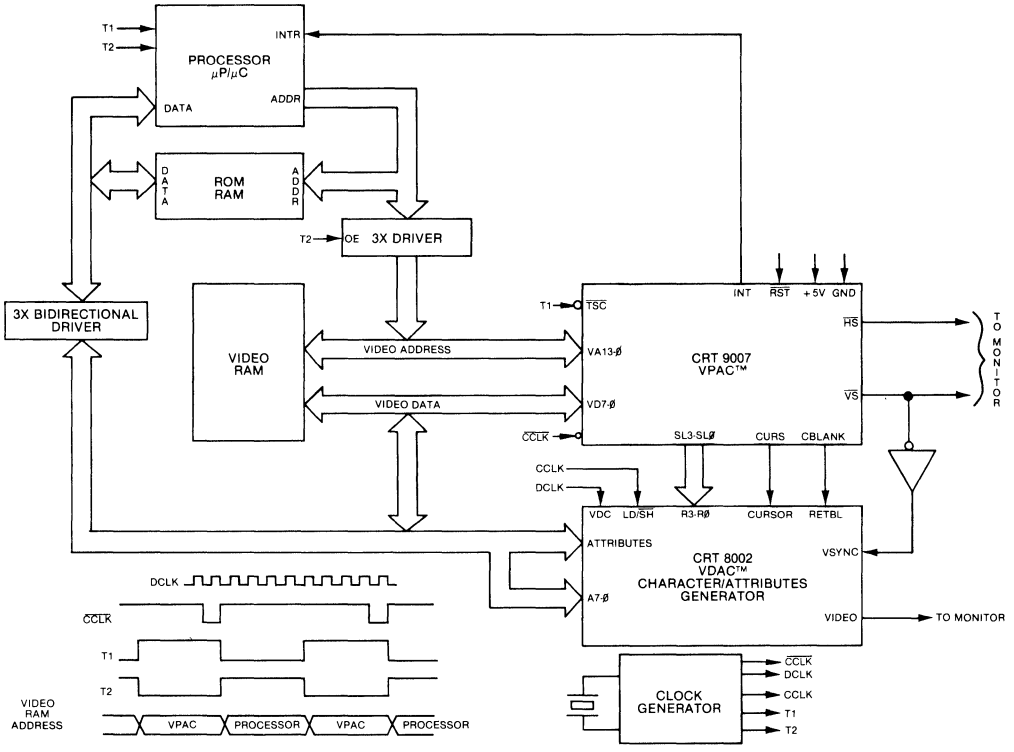


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

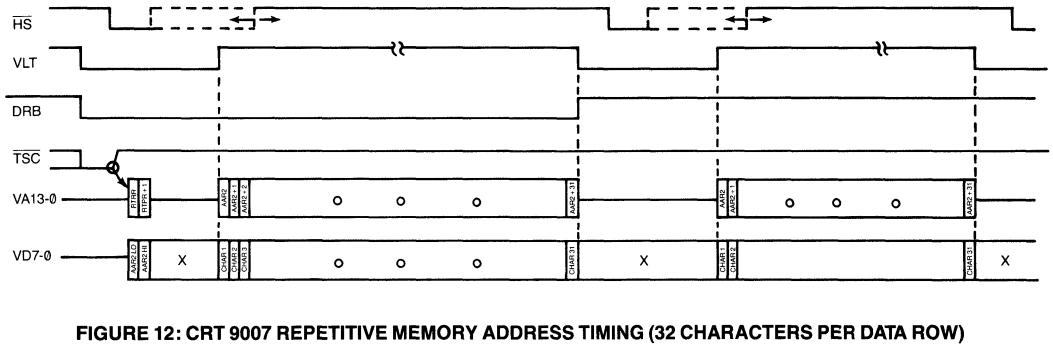


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

SECTION V

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N + 1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

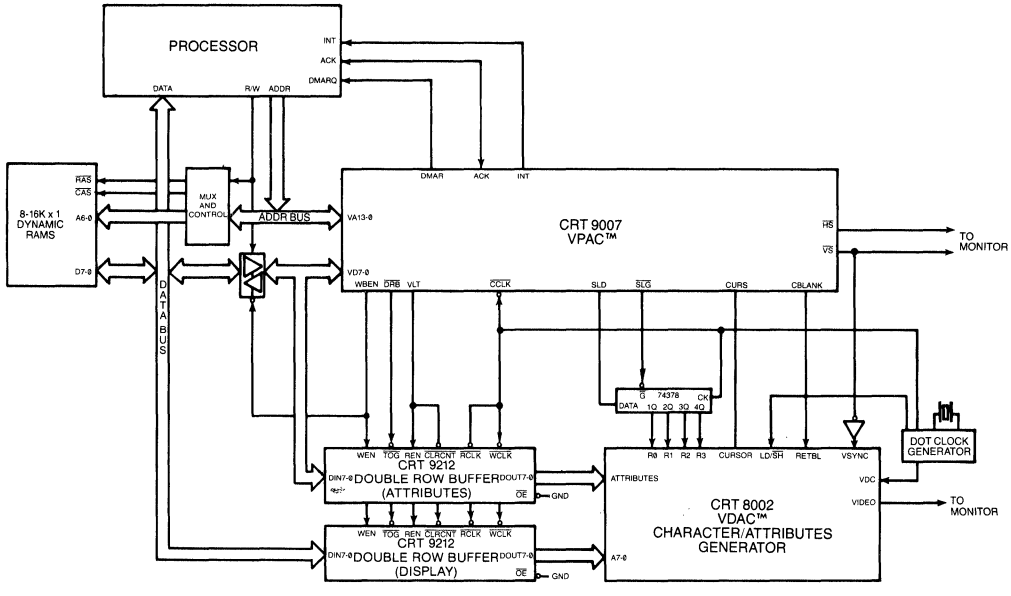
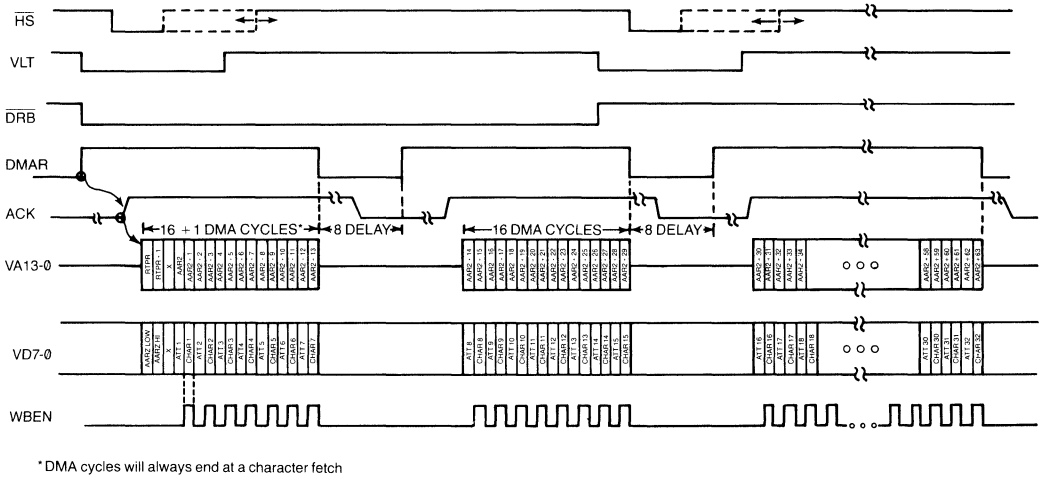


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

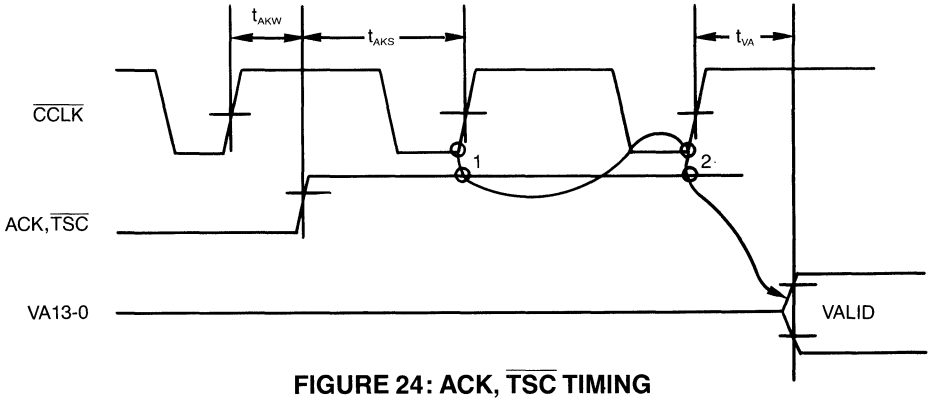


FIGURE 24: ACK, $\overline{TSC}$ TIMING

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

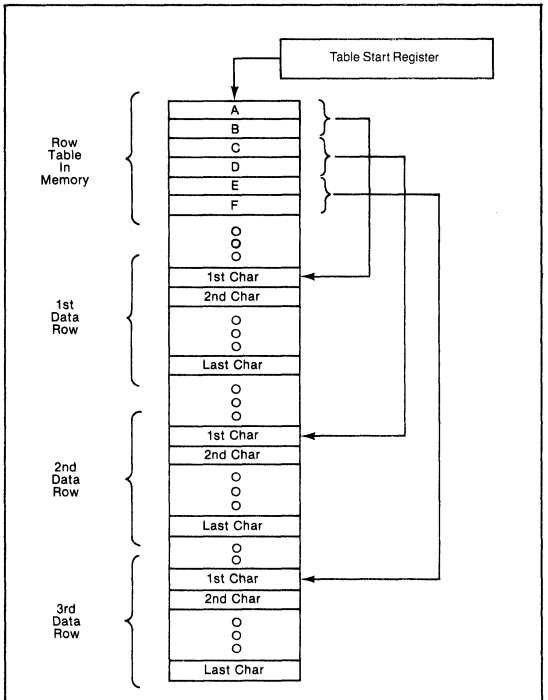


FIGURE 16: CONTIGUOUS ROW TABLE ADDRESS FORMAT

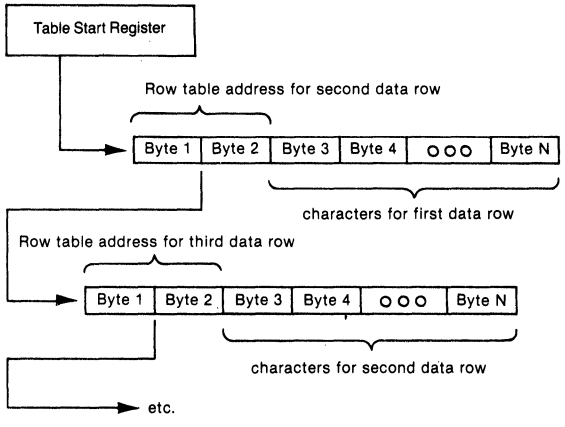


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing[1]

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

[1]SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
0	1000 to 104 F	
1	1050 to 109F	
2	10A0 to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20A0 to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08A0 to 08EF	
	O	
	O	
	O	

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or SLG, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 CCLK's after VLT trailing edge and stays active for exactly 1 CCLK assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 CCLK's to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER 0 rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

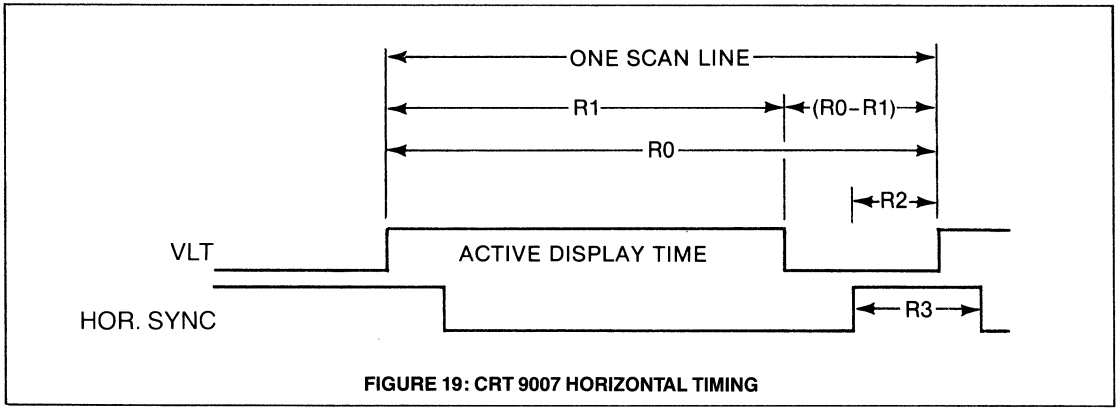


FIGURE 19: CRT 9007 HORIZONTAL TIMING

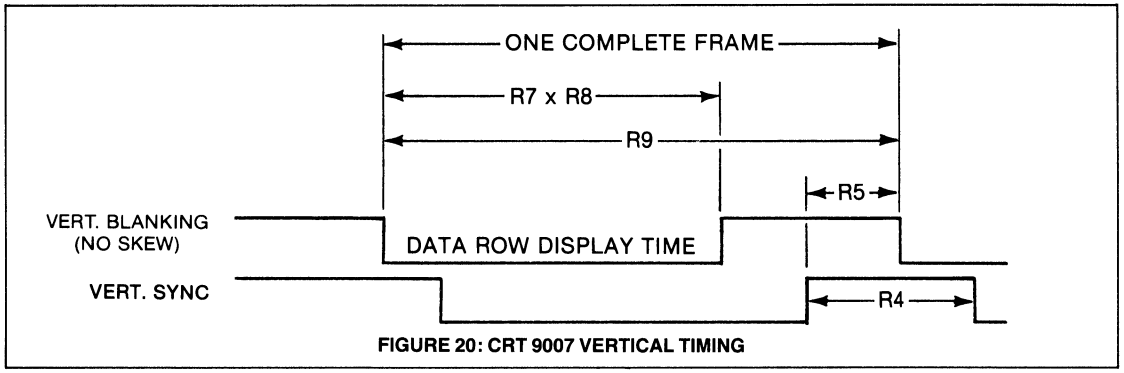


FIGURE 20: CRT 9007 VERTICAL TIMING

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	$\overline{TSC}$
1	0	SL3	$\overline{SL2}$	SL1	SL0	LPSTB	$\overline{TSC}$
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	$\overline{TSC}$
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

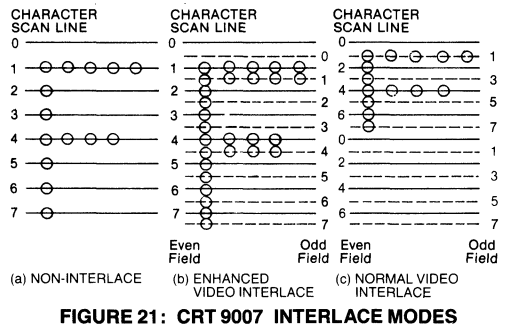


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SECTION V

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the $\overline{RST}$ input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
$\overline{VD}$7-0	High impedance
$\overline{HS}$	High
$\overline{VS}$	High
CBLANK	High
CURS	Low
$\overline{VLT}$	Low
$\overline{DRB}$	High
$\overline{INT}$	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

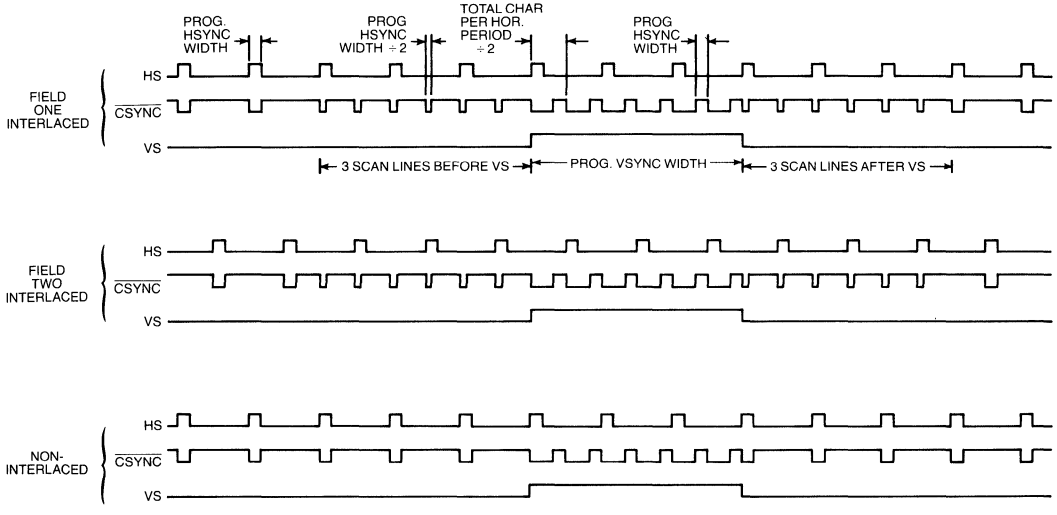


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

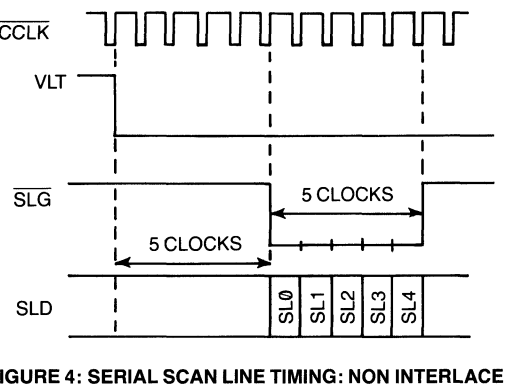


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

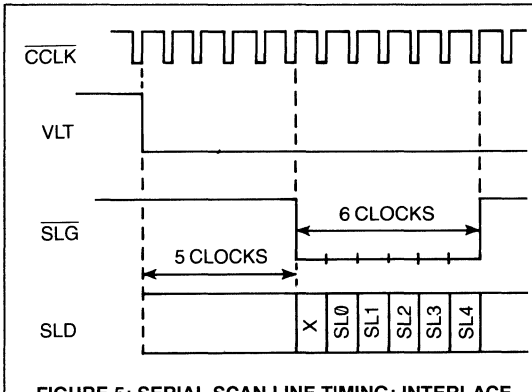


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -55° to + 150°C
Lead Temperature (soldering, 10 sec.) ..... + 325°C
Positive Voltage on any Pin, with respect to ground ..... + 8V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input; see note 4
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL} = 1.6 mA
V_{OH}	High	2.4			V	I_{OH} = 100 μA
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq 3.5V$; excluding $\overline{CCLK}$
I_{L2}				50	μA	V_{IN} = 5V; for $\overline{CCLK}$
				-300	μA	V_{IN} = 0V; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10		pF	all inputs except $\overline{CCLK}$
C_{IN2}			25		pF	$\overline{CCLK}$ input
	Power supply current					
I_{CC}			100		mA	170

AC ELECTRICAL CHARACTERISTICS[3]; T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock:					
t_{CY}	Clock period	290		1200	ns	CRT9007A double row buffer
		330		1200	ns	CRT9007B or attribute assemble
		400		1200	ns	CRT9007C
		270		1200	ns	CRT9007A all other operation
		300		1200	ns	CRT9007B modes
		400		1200	ns	CRT9007C
t_{CKL}	Clock low	90			ns	
t_{CKH}	Clock high	150			ns	
t_{CKR}	Clock rise time			15	ns	measured from 0.8V to 3.5V level
t_{CKF}	Clock fall time			10	ns	measured from 90% to 10% points
	Output Delay[1]:					
t_{D1}				150	ns	CRT9007A/B
				240	ns	CRT9007C
t_{D2}				150	ns	CRT9007A/B
				240	ns	CRT9007C
t_{D3}				150	ns	CRT9007A/B
				200	ns	CRT9007C
t_{D4}				150	ns	CRT9007A/B
				200	ns	CRT9007C
t_{VA}		25		100	ns	CRT9007A measured to the 2.3V
		25		115	ns	CRT9007B or 0.5V level on
		25		125	ns	CRT9007C VA13-VA0
t_{DSL}				500	ns	
t_{D5}				185	ns	CRT9007A/B
				200	ns	CRT9007C
t_{D6}				185	ns	CRT9007A/B
				200	ns	CRT9007C
t_{DSY}				185	ns	CRT9007A/B
				240	ns	CRT9007C
t_{VDS}		50			ns	CRT9007A valid for loading auxiliary
		55			ns	CRT9007B address register 2 or
		60			ns	CRT9007C attribute latch
t_{VDH}		10			ns	
t_{VDO}				185	ns	C_L = 50 pF
t_{SLG}				185	ns	CRT9007A/B
				240	ns	CRT9007C
t_{SLD}				185	ns	CRT9007A/B
				240	ns	CRT9007C

AC ELECTRICAL CHARACTERISTICS[3]; T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{D7}			240	ns	cursor skew of zero
			185	ns	CRT9007A/B cursor skew of one
			240	ns	CRT9007C through five
t_{D8}			300	ns	CRT9007A/B
			310	ns	CRT9007C
Processor Read/Write[2]:					
t_{AS}	100			ns	CRT9007A
	110			ns	CRT9007B/C
t_{AH}	0			ns	
t_{PW}	165			ns	
t_{CSH}	650			ns	
t_{PDS}	100			ns	
t_{PDH}	0			ns	
t_{PDA}			140	ns	CRT9007A/B
			189	ns	CRT9007C
t_{PDO}	10		85	ns	
t_{IRR}			400	ns	CRT9007A/B
			410	ns	CRT9007C
Miscellaneous Timing:					
t_{ATS}	25		115	ns	measured from the 0.4V level of ACK or TSC falling edge
t_{RW}	4tcy			ns	measured from the 0.4V level falling edge to 0.4V level rising edge
t_{AKW}	50			ns	see figure 24
t_{AKS}	50			ns	see figure 24

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of $\overline{CCLK}$.

SECTION V

CRT9007A1/CRT9007A2

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to + 150°C
Lead Temperature (Soldering, 10 sec) ..... + 325°C
Positive voltage on any pin (WRT ground) ..... + 8V
Negative voltage on any pin (WRT ground) ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	
	Input voltage:					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2			V	All inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input; see Note 4
	Output voltage:					
V_{OL}	Low			0.5	V	I_{OL} = 1.6 mA
V_{OH}	High	2.4			V	I_{OH} = 100 μA
	Input leakage current:					
I_{L1}				10	μA	0 = < V_{IN} = < 3.5V; excluding $\overline{CCLK}$
I_{L2}				50	μA	V_{IN} = 5V; for $\overline{CCLK}$
I_{L3}				-200	μA	V_{IN} = 0V; for $\overline{CCLK}$
	Input capacitance:					
C_{IN1}			10	15	pF	All inputs except $\overline{CCLK}$ at 1 MHz
C_{IN2}			25	50	pF	$\overline{CCLK}$ input at 1 MHz
	Power supply current:					
I_{CC}			100	TBD	mA	

AC ELECTRICAL CHARACTERISTICS[3] T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	
	Clock:					
t_{CY}	Clock period	155		TBD	ns	CRT9007A2 All operation modes
		200		TBD	ns	CRT9007A1
t_{CKL}	Clock low	50			ns	CRT9007A2
		75			ns	CRT9007A1
t_{CKH}	Clock high	80			ns	CRT9007A2
		100			ns	CRT9007A1
t_{CKR}	Clock rise time			15	ns	Measured from 0.8V to 3.5V level
t_{CKF}	Clock fall time			10	ns	Measured from 90% to 10% points
	Output delay[1]:					
t_{D1}				100	ns	
t_{D2}				100	ns	
t_{D3}				100	ns	
t_{D4}				100	ns	
t_{VA}		25		TBD	ns	CRT9007A2 Measured to the 2.3V or 0.5V lev
		25		80	ns	CRT9007A1 on VA13-VA0
t_{DBL}				500	ns	
t_{D5}				135	ns	
t_{D6}				135	ns	
t_{DBY}				135	ns	
t_{VDS}		TBD			ns	CRT9007A2 Valid for loading auxiliary addr
		30			ns	CRT9007A1 register 2 or the attribute latch
t_{VDH}		TBD			ns	CRT9007A2
		10			ns	CRT9007A1
t_{VDO}				TBD	ns	C_L = 50 pF
t_{SLB}				135	ns	
t_{SLD}				135	ns	
t_{D7}				135	ns	Cursor skew of one thru five
t_{D8}				200	ns	
	Processor read/write[2]:					
t_{AB}		100			ns	
t_{AH}		0			ns	
t_{PW}		165			ns	
t_{CSH}		650			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDO}		10		85	ns	
t_{IRR}				400	ns	
	Miscellaneous timing:					
t_{ATB}		25		115	ns	Measured from the 0.4V level of ACK or $\overline{TSC}$ falling edge
t_{RW}		$4t_{CY}$			ns	Measured from the 0.4V level falling edge to 0.4V level rising edge
t_{AKW}		50			ns	
t_{AKB}		50			ns	

NOTE:
1. Timing measured from the 1.5V level of the rising edge of CCLK (-) to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of CCLK (-).

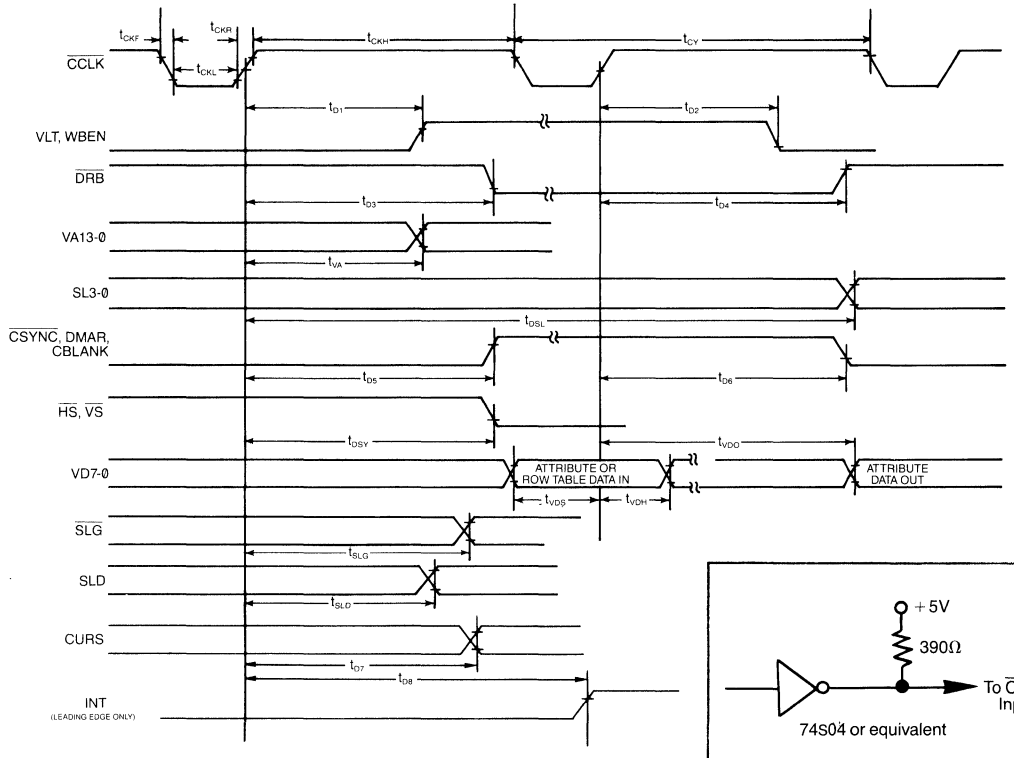


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

FIGURE 25: RECOMMENDED $\overline{CCLK}$ DRIVER CIRCUIT

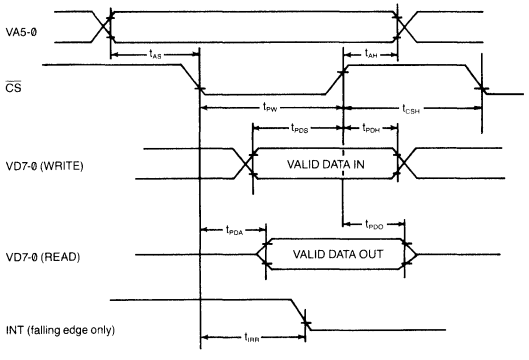
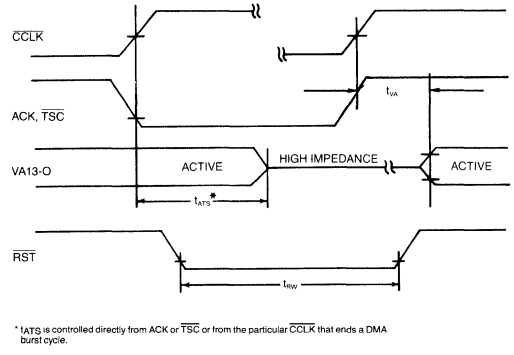


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{ATS} is controlled directly from ACK or $\overline{TSC}$ or from the particular $\overline{CCLK}$ that ends a DMA burst cycle.

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB			LSB	BLANK SKEW MSB		LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES/FRAME (B10))	(B8)	SCAN LINES PER DATA ROW MSB					LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSBA		LSB	DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/$\overline{SS}$	INTERLACE MODES		OPERATION MODES			$\overline{2XC}$/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	VERTICAL CURSOR REGISTER (ROW COORD.)								
READ	1	1	1	0	0	0	MSB							LSB	R18 or R38
WRITE	0	1	1	0	0	1	HORIZONTAL CURSOR REGISTER (COL. COORD.)								
READ	1	1	1	0	0	1	MSB							LSB	R19 or R39
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	INTERRUPT ENABLE REGISTER LIGHT PEN	X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	STATUS REGISTER LIGHT PEN			ODD/ EVEN	X	FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD.)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL. COORD.)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

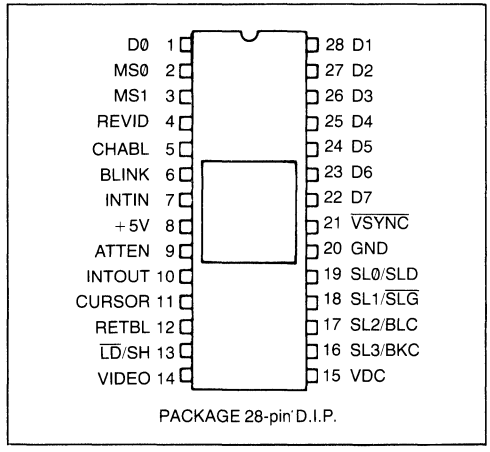
CRT 9021A
CRT 9021B

CRT Video Attributes Controller
VAC

FEATURES

- ☐ On chip video shift register
  Maximum shift register frequency
  CRT 9021A 30 MHz
  CRT 9021B 28.5 MHz
- ☐ On chip attributes logic
  Reverse video
  Character blank
  Character blink
  Underline
  Full/half intensity
- ☐ Four modes of operation
  Wide graphics
  Thin graphics
  Character mode without underline
  Character mode with underline
- ☐ On Chip logic for double height/double width characters
- ☐ Accepts scan line information in parallel or serial format
- ☐ Four cursor modes dynamically selectable via 2 input pins
  Underline
  Blinking underline
  Reverse video
  Blinking reverse video
- ☐ Programmable character blink rate

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Programmable cursor blink rate
- ☐ On chip data and attribute latches
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS n-Channel silicon gate COPLAMOS® process
- ☐ Compatible with CRT 5037 VTAC®; CRT 9007 VPAC™

GENERAL DESCRIPTION

The SMC CRT 9021 Video Attributes Controller (VAC) is an n-channel COPLAMOS MOS/LSI device containing Graphics logic, attributes logic, data and attributes latches, cursor control, and a high speed video shift register. The CRT 9021, a character generator ROM and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9021 serial video output may be connected directly to a CRT monitor's video input. The maximum video shift register frequency of 28.5 MHz or 30 MHz allows for CRT displays of up to 132 characters per data row.

The CRT 9021 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition, when used in conjunction with the CRT 9007 VPAC,™ the CRT 9021 will provide double height or double width characters.

Four programmable cursor modes are provided on the CRT 9021. They are: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the CRT 9021 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

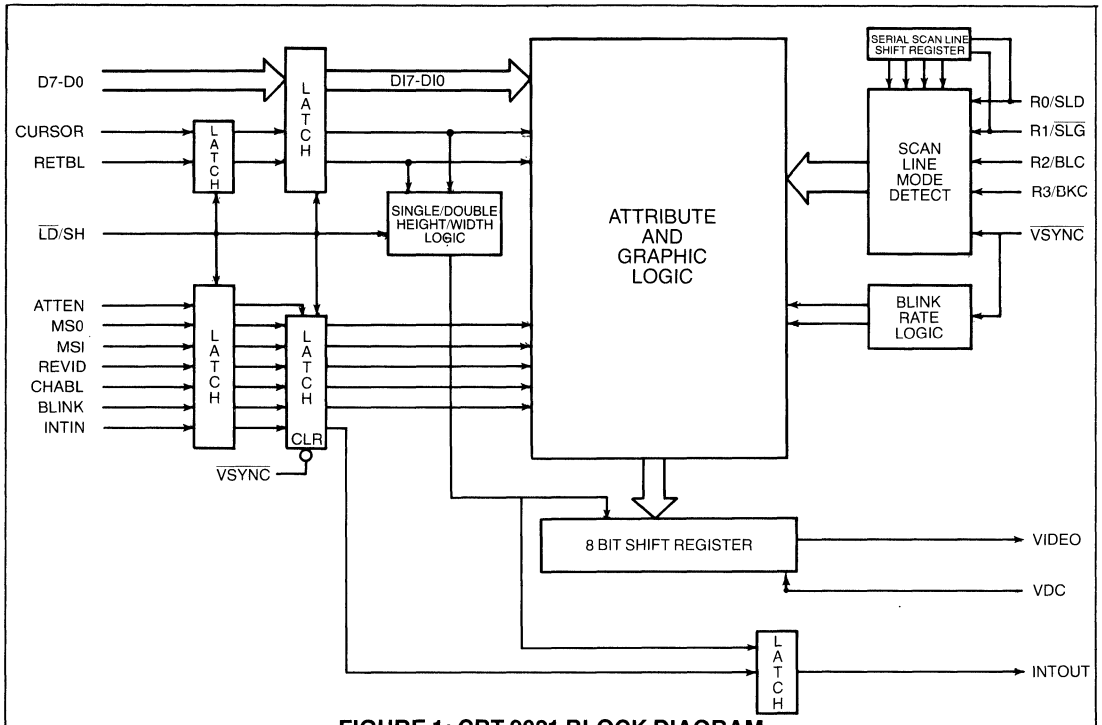


FIGURE 1: CRT 9021 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1, 28, 27, 26, 25, 24, 23, 22	Data	D7-D0	In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the LD/SH input goes low. In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Figures 2 and 3 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0
2 3	Mode Select 0 Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the CRT 9021 as follows: MS1, MS0 = 00; Wide graphics mode = 10; Thin graphics mode = 01; Character mode without underline = 11; Character mode with underline See section entitled Display Modes for details.
4	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register.
5	Character blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block.
6	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75/25 (on/off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink.
7	Intensity In	INTIN	The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity".

DESCRIPTION OF PIN FUNCTIONS CONT'D

PIN NO.	NAME	SYMBOL	FUNCTION
8	Supply Voltage	+5V	+5 volt power supply
9	Attribute Enable	ATTEN	When this input is high, the internal attribute latch is updated at the positive going edge of the LD/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes)..
10	Intensity Out	INTOUT	This output is used in conjunction with the INTIN input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7).
11	Cursor	CURSOR	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9021 enters the double width mode. See section entitled cursor formats for details.
12	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next LD/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time.
13	Load/Shift	LD/SH	The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of LD/SH.
14	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of the LD/SH input will determine the number of backfill dots. See figure 5.
15	Video Dot Clock	VDC	This input clock controls the rate at which video is shifted out on the VIDEO output.
16	Scan line 3/Block Cursor	SL3/BKC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the most significant bit of the binary scan line row address. *Serial scan line mode*—This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed.
17	Scan line 2/Blink Cursor	SL2/BLC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the second most significant bit of the binary scan line row address. *Serial scan line mode*—This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking.
18	Scan Line 1/Scan Line Gate	SL1/SLG	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the next to the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more LD/SH pulses, the CRT 9021 will assume the parallel input scan line row address mode.
19	Scan line 0/Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. Refer to figure 6. *Parallel scan line mode*—This input is the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will present the scan line information in serial form (least significant bit first) to the CRT 9021 and permits the proper scan line information to enter the serial scan line shift register during the LD/SH pulses framed by SLG (pin 18).
20	Ground	GND	Ground
21	Vertical Sync	VSYNC	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The VSYNC input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".

ATTRIBUTES FUNCTION

Retrace Blank —The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video —The REVID input causes inverted data to be loaded into the video shift register.

Character Blank —The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline —MS1, MS0 = 1, 1 forces the video to go to the inverse of the background level for the scan line(s) programmed for underline.

Blink —The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) —The INTiN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the CRT 9021. An external mixer can be used to combine VIDEO and INTOUT to create the desired video level. See figure 8.

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

TABLE 1: CRT 9021 ATTRIBUTE COMBINATIONS

CURSOR FORMAT	CRT 9021 INPUTS					VIDEO SHIFT REGISTER LOADED WITH:	
	RETBL	CURSOR	REVID	CHABL	UNDLN		
X	1	X	X	X	X	**all zero's**	
	0	0	0	0	0	data	
	0	0	0	0	1	One's for selected scan line(s); Data for all other scan lines.	
	0	0	0	1	X	All zero's	
	0	0	1	0	0	$\overline{\text{data}}$	
	0	0	1	0	1	Zero's for selected scan line(s); $\overline{\text{data}}$ for all other scan lines.	
	0	0	1	1	X	One's for all scan lines.	
UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) for cursor; data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) for cursor; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) for cursor; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) for cursor; one's for all other scan lines.	
BLINKING[3] UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) blinking; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) blinking; one's for all other scan lines.	
REVID BLOCK	0	1	0	0	0	$\overline{\text{Data}}$ for all scan lines.	
	0	1	0	0	1	Zero's for selected scan line(s) for underline; data for all other scan lines.	
	0	1	0	1	X	One's for all scan lines.	
	0	1	1	0	0	Data for all scan lines	
	0	1	1	0	1	One's for selected scan line(s) for underline; data for all other scan lines.	
	0	1	1	1	X	Zero's for all scan lines.	
BLINKING[3] REVID BLOCK	0	1	0	0	0	On Data for all scan lines.	Off Data for all scan lines.
	0	1	0	0	1	Zero's for selected scan line(s) for underline; Data for all other scan lines.	One's for selected scan line(s) for underline; Data for all other scan lines.
	0	1	0	1	X	One's for all scan lines.	Zero's for all scan lines.
	0	1	1	0	0	Data for all scan lines.	$\overline{\text{Data}}$ for all scan lines.
	0	1	1	0	1	One's for selected scan line(s); Data for all other scan lines.	Zero's for selected scan line(s); Data for all other scan lines.
	0	1	1	1	X	Zero's for all scan lines.	One's for all scan lines.

1 - if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence; otherwise both are displayed.
2 - at programmed scan line(s) for underline
3 - at cursor blink rate
Note—cursor blink rate overrides character blink rate.

DISPLAY MODES

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 8a and 8b illustrate a typical CRT 9021 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 —Wide Graphics Mode. In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 2. Note that individual bits in D7-D0 will illuminate particular portions of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

MS1, MS0 = 10 —Thin Graphics Mode. In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 3. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.

MS1, MS0 = 01 —Character Mode Without Underline. In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 8a and 8b.

MS1, MS0 = 11 —Character Mode With Underline. Same operation as MS1, MS0 = 01 with the underline attribute appearing on the scan line(s) mask programmed.

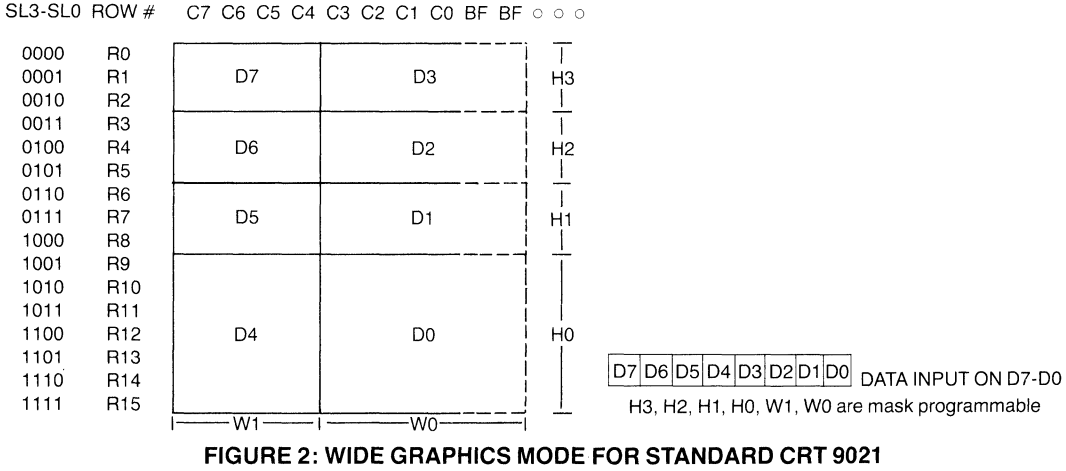


FIGURE 2: WIDE GRAPHICS MODE FOR STANDARD CRT 9021

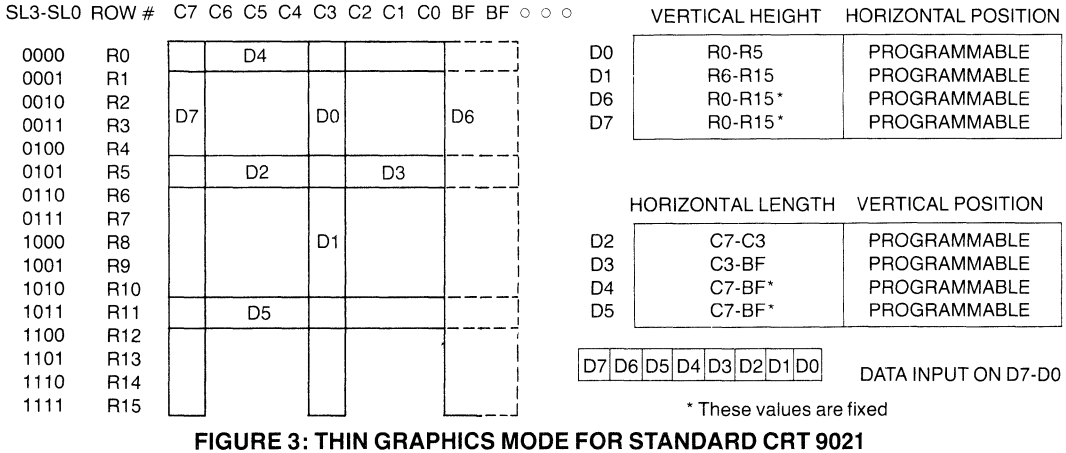


FIGURE 3: THIN GRAPHICS MODE FOR STANDARD CRT 9021

BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyond 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

CURSOR FORMATS

Four cursor formats are possible with the CRT 9021. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 5. The four cursor modes are as follows:

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse video block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

Scan Line Input Mode	Pin 17	Pin 16	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	X	X	Mask programmable Only

TABLE 5: CURSOR FORMATS

DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the CRT 9021, no distinction between double width and double height display is necessary. Figure 4 illustrated timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the CURSOR signal as required by the CRT 9021 with no additional hardware.

SCAN LINE INPUT MODES

Scan line information can be introduced into the CRT 9021 in parallel format or serial format. Table 6 illustrates the pin definition as a function of the scan line input mode. The CRT 9021 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two conditions occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$/SH periods. Refer to figure 7 for timing details.

Scan Line Input Mode	CRT 9021 Pin Number			
	19	18	17	16
Serial	SLD	$\overline{SLG}$	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

TABLE 6: PIN DEFINITION FOR PARALLEL AND SERIAL SCAN LINE MODES

PROGRAM OPTIONS

The CRT 9021 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 4 illustrates the range of the miscellaneous mask programmed options. In addition, Tables 2, 3 and 4 show the mask programmed options for the standard CRT 9021.

1 - Attributes include MS0 , MSI, BLINK, CHABL, INTENSITY, REVID

FIGURE 4: CRT 9021 FUNCTIONAL I/O TIMING

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	.15V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	All inputs except VDC, $\overline{LD}$/SH
Low Level V_{IL}			0.65	V	For VDC, $\overline{LD}$/SH inputs
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, $\overline{LD}$/SH input
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 0.4 mA
High Level V_{OH}	2.4			V	I_{OH} = 100μA
INPUT LEAKAGE CURRENT					
Leakage I_{L1}			10	μA	$0 \leq V_{IN} < V_{CC}$; excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leq V_{IN} \leq V_{CC}$; for VDC $\overline{LD}$/SH
INPUT CAPACITANCE					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		20		pf	For $\overline{LD}$/SH
C_{IN3}		25		pf	For VDC
POWER SUPPLY CURRENT					
I_{CC}		50		mA	

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VDC[1]					
$1/t_{CY1}$ VDC frequency	10.0		30.0	MHZ	CRT 9021A; see note 1
	10.0		28.5	MHZ	CRT 9021B
1_{CKL} VDC low	10				
t_{CKH} VDC high	10			ns	
t_{CKR} VDC rise time			10	ns	Measured from 10% to 90% points
t_{CKF} VDC fall time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	290			ns	CRT 9021A; see note 1
	315			ns	CRT 9021B
t_{S1}	7			ns	
t_{H1}	0			ns	
INPUT SETUP AND HOLD					
t_{S2}	35			ns	
t_{H2}	0			ns	
MISCELLANEOUS TIMING					
t_{PD}			35	ns	C_L = 15 pf
t_{DW}	t_{CY2}				

1-These parameters are Preliminary.

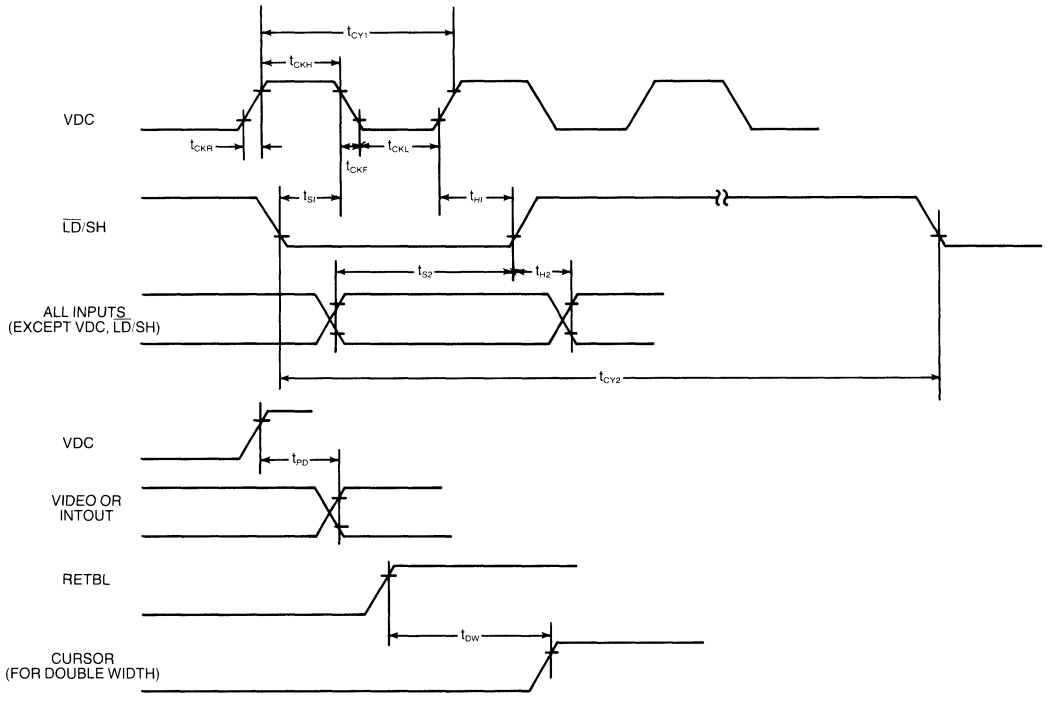


FIGURE 5: CRT 9021 INPUT/OUTPUT TIMING

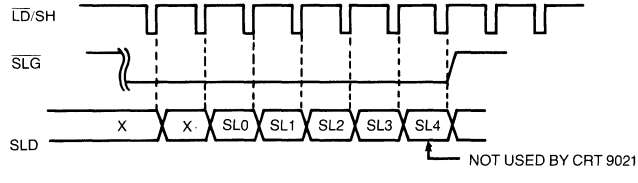


FIGURE 6: SERIAL SCAN LINE MODE TIMING

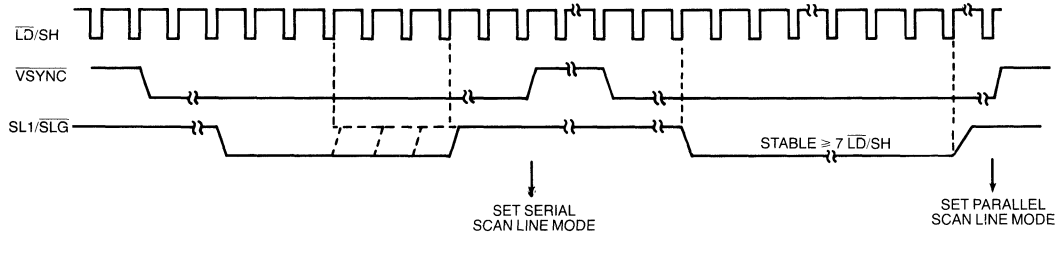


FIGURE 7: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING

TABLE 2
WIDE GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Height of graphic block*		
D7 and D3	any scan line(s)	R0, R1, R2
D6 and D2	any scan line(s)	R3, R4, R5
D5 and D1	any scan line(s)	R6, R7, R8
D4 and D0	any scan line(s)	R9, R10, R11, R12, R13, R14, R15
Width of D7, D6, D5, D4**	any number of dots 0 to 8	C7, C6, C5, C4
Width of D3, D2, D1, D0**	any number of dots 0 to 8	C3, C2, C1, C0, BF

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

TABLE 3
THIN GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill	C1 or C0	C0
Horizontal position for		
D2 and D3	any scan line(s) R0-R15	R5
D4	any scan line(s) R0-R15	R0
D5	any scan line(s) R0-R15	R11
Horizontal length for		
D2[2]	any continuous dots C7-C0, BF	C7-C3
D3[2]	all dots not covered by D2	C3-BF
Blanked dots for serrated horizontal lines		
D2	any dot(s) C7-C0, BF	none
D3	any dot(s) C7-C0, BF	none
D4 and D5	any dot(s) C7-C0, BF	none
Vertical position for		
D0 and D1	any dot(s) C7-C0, BF	C3
D6[1]	any dot(s) C6-C0, BF	BF
D7[1]	any dot(s) C7-C0	C7
Vertical length for		
D0	any scan line(s)	R0 to R5
D1	all scan lines not used by D0	R6 to R15
D6	no choice; always R0-R15	R0 to R15
D7	no choice; always R0-R15	R0 to R15

1-D7 must always come before D6 with no overlap; otherwise D6 is lost.
2-D2 and D3 must always overlap by one and only one dot.

TABLE 4
MISCELLANEOUS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill in character mode	C7 or C0	C7
Character blink rate (division of $\overline{\text{VSYNC}}$ frequency)	8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1]	32 (1.875 Hz)[1]
Cursor blink rate[2]	Twice the character blink rate	16 (3.75 Hz)[1]
character underline position	any scan line(s) R0-R15	R11
cursor underline[3]	any scan line(s) R0-R15	not applicable
cursor format[4]	underline Blinking underline Reverse video block Blinking reverse video block	Blinking reverse video block

1 - Assumes $\overline{\text{VSYNC}}$ input frequency of 60 Hz.
2 - Valid only if the cursor is formatted to blink.
3 - Valid only if the cursor is formatted for underline.
4 - Valid for the parallel scan line mode only.

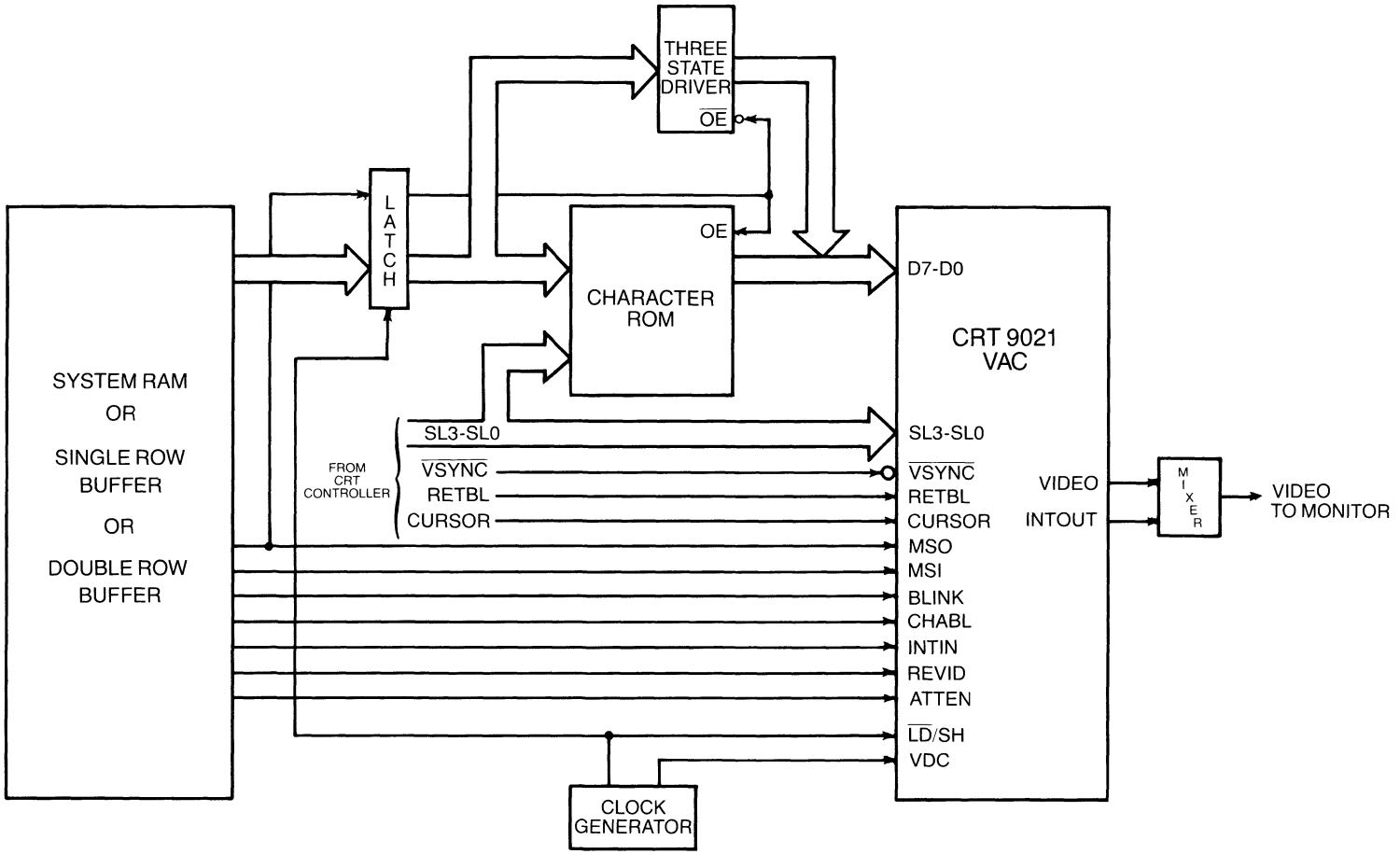


FIGURE 8a: CRT 9021 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE

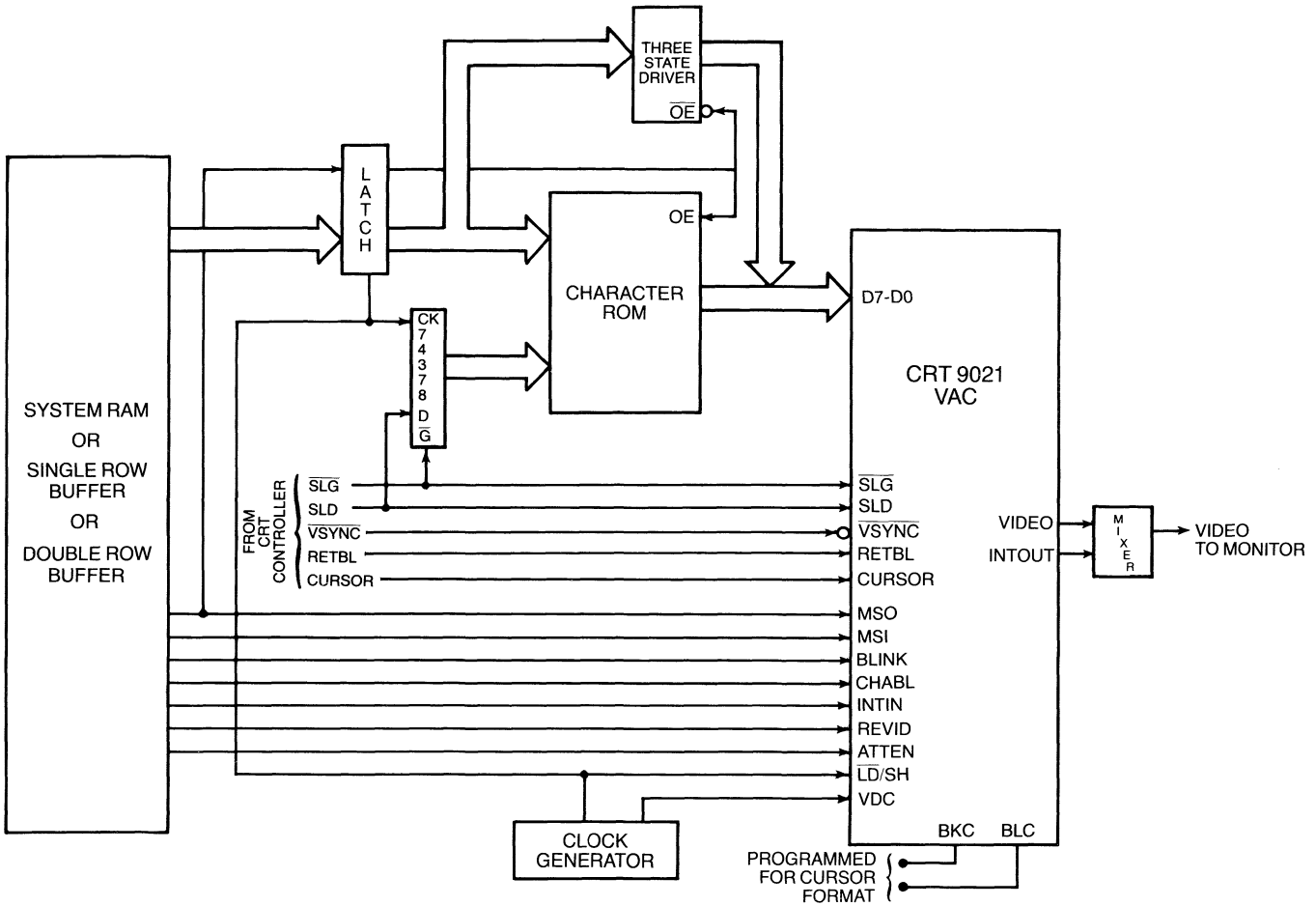


FIGURE 8b: CRT 9021 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE

STANDARD MICROSYSTEMS CORPORATION

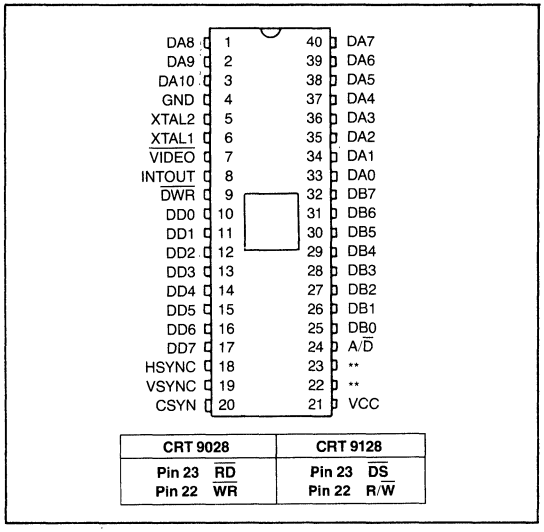
CRT 9028
CRT 9128

VTLC
Video Terminal Logic Controller

FEATURES

- ☐ Built-in High Frequency (4-14 MHz) Oscillator
- ☐ Built-in Video Shift Register
- ☐ Built-in Character Generator
- ☐ Bi-Directional Smooth Scroll Capability
- ☐ Visual Attributes Include Reverse Video, Intensity Control, Underline and Character Blank
- ☐ Separate HSYNC, VSYNC and VIDEO Outputs
- ☐ Composite Sync (RS170 Compatible) Output
- ☐ Absolute (RAM address) Cursor Addressing
- ☐ MASK Programmable Video Parameters:
  - Dots Per Character Block (6-8)
  - Raster Scans Per Data Row (8-12)
  - Characters Per Data Row (32, 48, 64, 80)
  - Data Rows Per Page (8,10,12,16,20,24 or 25)
  - Horizontal Blanking (8-64 Characters)
  - Horizontal Sync Front Porch (0-7 Characters)
  - Horizontal Sync Duration (1-64 Characters)
  - Horizontal Sync Polarity
  - Two Values of Vertical Blanking
  - Two Values of Vertical Sync Front Porch (0-63 Scan Lines)
  - Two Values of Vertical Sync Duration (1-16 Scan Lines)
  - Vertical Sync Polarity
  - Internal 128 Character 5x8 Dot Font
  - Character/Cursor Underline Position
  - Scan Row and Column for Thin Graphics Entity Segments
  - Scan Rows and Columns for Wide Graphics Entity Elements
- ☐ Software Enabled Non-Scrolling 25th Data Row Available with 25 Data Row/Page Display
- ☐ Non-Interlace Display Format
- ☐ Separate Display Memory Bus Eliminates Contention Problems
- ☐ Fill (Erase) Screen Capability
- ☐ Standard 8-bit Data Bus Microprocessor Interface
- ☐ Wide Graphics with Six Independently Addressable Segments Per Character Space
- ☐ Thin Graphics with Four Independently Addressable Segments Per Character Space
- ☐ Single +5V Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ TTL Compatible

PIN CONFIGURATION



CRT 9028	CRT 9128
Pin 23 RD	Pin 23 DS
Pin 22 WR	Pin 22 R/W

GENERAL DESCRIPTION

The CRT 9028 VTLC and CRT 9128 VTLC are mask programmable 40 pin COPLAMOS® n-channel MOS/LSI Video Display Controller Chips that combine video timing, video attributes, alphanumeric and graphics generation, smooth scroll and screen buffer interface functions.

The VTLC incorporates many of the features (previously requiring a number of external components) required in building a low cost yet versatile display interface. An internal mask programmable 128 character font provides for a full ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

Two pinout configurations enhance the versatility of the VTLC. The CRT 9028 controls data flow over the processor system data bus through separate read ($\overline{RD}$) and write ($\overline{WR}$) strobes for use with the 8085, 8051, Z80®, 8086, and similar microprocessors or microcomputers. The CRT 9128 regulates the data flow with a data strobe ($\overline{DS}$) and read/write (R/$\overline{W}$) enable signals for use with the 6500, Z8™, 68000 and similar microprocessors or microcomputers.

The VTLC provides two independent data buses; one bus that interfaces to the processor and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the VTLC eliminating contention problems and the need for a separate row buffer.

The VTLC has an internal crystal oscillator requiring only an external crystal to operate. Masked constants for critical video timing simplify programming, operation and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

*Z80 is a registered trademark of Zilog Corporation.
Z8 is a trademark of Zilog Corporation.

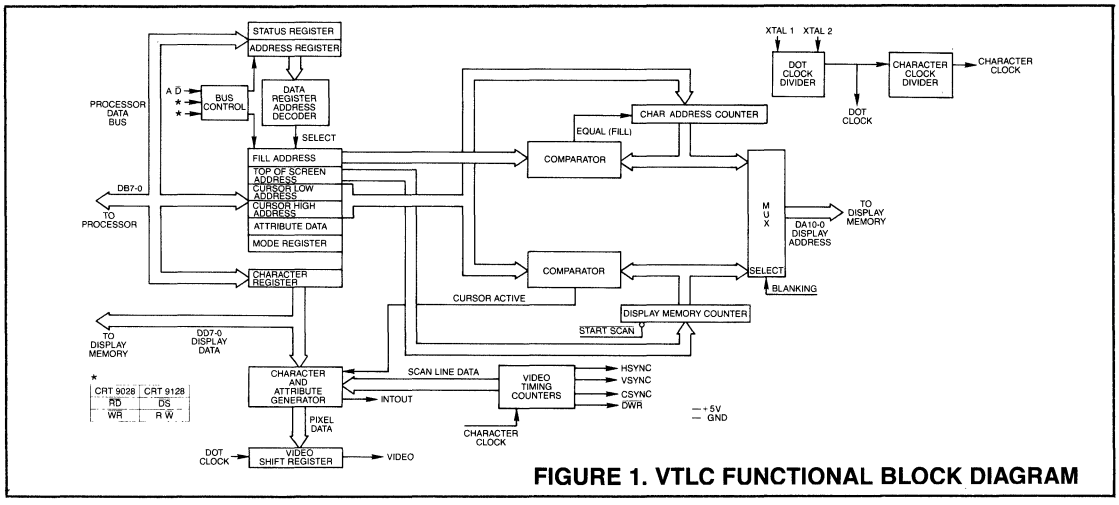


FIGURE 1. VTLC FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	NAME	DESCRIPTION
3-1, 40-33	DA10-0	O	Display Address	11 bit address bus to display memory
4	GND		Ground	Ground Connection
5,6	XTAL2,1	I	Crystal 2,1	External Crystal An external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating).
7	$\overline{\text{VIDEO}}$	O	$\overline{\text{Video Output}}$	This output is a digital TTL waveform used to develop the VIDEO and composite VIDEO signals to the monitor. The polarity of this signal is: HIGH = BLACK LOW = WHITE
8	INTOUT	O	Intensity Output	This pin is the intensity level modification attribute bit (synchronized with the video data output).
9	$\overline{\text{DWR}}$	O	$\overline{\text{Display Write}}$	Write strobe to display memory
17-10	DD7-0	I/O	Display Data	8-bit bidirectional data bus to display memory
18	HSYNC	O	Horizontal Sync	Horizontal sync signal to monitor
19	VSYNC	O	Vertical Sync	Vertical sync signal to monitor
20	CSYNC	O	Composite Sync	This output is used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor.
21	V_{cc}		Power	5.0 V power connection
			CRT 9028	
22	$\overline{\text{WR}}$	I	$\overline{\text{Write Strobe}}$	Causes data on the microprocessor data bus to be strobed into the VTLC
23	$\overline{\text{RD}}$	I	$\overline{\text{Read Strobe}}$	Causes data from the VTLC to be strobed onto the microprocessor data bus
			CRT 9128	
22	R/$\overline{\text{W}}$	I	Read/$\overline{\text{Write}}$ Select	Determines whether the processor is reading data from or writing data into the VTLC (high for read, low for write)
23	$\overline{\text{DS}}$	I	$\overline{\text{Data Strobe}}$	Causes data to be strobed into or out of the VTLC from the microprocessor data bus depending on the state of the R/W signal
24	A/$\overline{\text{D}}$	I	Register Select	The state of this input pin will determine whether the data is being read from, or written to, the address or status register, or a data register.
32-25	DB7-0	I/O	Processor Data Bus	8-bit bi-directional processor data bus

DESCRIPTION OF OPERATION*

THE VTLC INTERNAL REGISTERS

CRT 9028

Addressing of the internal VTLC data registers of the CRT 9028 is accomplished through the use of the A/$\overline{D}$ select input qualified by the $\overline{RD}$ and $\overline{WR}$ strobes.

A/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	REGISTER OPERATION
0	1	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	1	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

CRT 9128

Addressing of the internal VTLC data registers of the CRT 9128 is accomplished through use of the A/$\overline{D}$ and R/$\overline{W}$ select inputs qualified by the $\overline{DS}$ strobe.

A/$\overline{D}$	$\overline{DS}$	R/$\overline{W}$	REGISTER OPERATION
0	0	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	0	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

The contents of the seven processor programmable registers located in the upper left hand side of the Functional Block Diagram of figure 1 indicate the memory locations from which screen data is to be fetched and displayed as well as the selected modes of display operation. These registers are addressed indirectly via the Address Register.

To access one of the seven eight-bit registers, the processor must first load the Address Register with the three-bit address of the selected data register. The next read or write to a data register will then cause the data register pointed to by the Address Register to be accessed. The Line A/$\overline{D}$ controls whether writing is occurring to the Address Register or to a data register. When a read operation is performed, A/$\overline{D}$ controls access to either the Status Register or to the data register selected by the Address Register.

REGISTER DESCRIPTION

ADDRESS REGISTER

Writing a byte to the ADDRESS register will select the specified register the next time the processor writes to or reads the VTLC data registers. The data register addresses are as follows:

STATUS REGISTER

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register. This bit is used to synchronize data transfers between the processor and the VTLC. The VTLC will set the DONE bit to a logic one after completing a byte transfer command or a FILL operation. The DONE bit is set to a logic zero by reading from, or writing to, the CHARACTER register. The processor must wait until the DONE bit is 1 before attempting to change the CURSOR ADDRESS, in order to write a character to, or read a character from, the CHARACTER register.

STATUS REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DONE	X	X	X	X	X	X	X

DONE = 1 signifies that external processor is allowed to access cursor ADDRESS and/or CHARACTER registers.

DONE = 0 signifies that external processor must wait until VTLC completes transfer of data between display memory and CHARACTER register.

DATA REGISTERS

FILADD (Fill Address) This register contains the RAM address of the character following the last address to be filled. Writing to this register will enable the VTLC "fill" circuitry. The FILL operation will then be triggered by the next processor write to the CHARACTER register. The FILL operation will write the character in the CHARACTER register to every location in display memory starting with the address specified in the CURLO and CURHI registers through the location preceeding the address specified in the FILADD register. The cursor position is not changed after a FILL operation. Note that the address bits DA3-DA0 are internally forced to 0 forcing the FILADD address to be 00, 16, 32, etc. to 1920. The CURLO and CURHI registers will not be changed by this operation. Writing to the CHARACTER register will cause the VTLC to reset DB7 of the STATUS register to "0". Bit 7 will be set to 1 after the VTLC has filled the last memory location specified.

FILADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DA10	DA9	DA8	DA7	DA6	DA5	DA4

ADDRESS								TYPE	REGISTER
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
X	X	X	X	0	1	1	0	Write	CHIP RESET
X	X	X	X	1	0	0	0	Write	TOSADD
X	X	X	X	1	0	0	1	Write	CURLO
X	X	X	X	1	0	1	0	Write	CURHI
X	X	X	X	1	0	1	1	Write	FILADD
X	X	X	X	1	1	0	0	Write	ATTDAT
X	X	X	X	1	1	0	1	RD/WR	CHARACTER
X	X	X	X	1	1	1	0	Write	MODE REGISTER

(X = don't care)

*NOTE: Chip Reset is required before starting operation.

TOSADD (Top of Screen Address) This register contains the RAM address of the first character displayed at the top of the video monitor screen. In addition, this register controls selection of either of two mask programmable vertical scan rates.

TOSADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TIM	DA10	DA9	DA8	DA7	DA6	DA5	DA4

Note that address bits DA3-DAO are internally forced to 0 forcing the first address at the beginning of each row to be 00, 16, 32, etc. to 1920.

The most significant bit of this register (TIM) is used to select between the two mask programmed sets of vertical retrace parameters (scan A and scan B). This allows software selection of, for example, 50/60 HZ.

TIM = 0 enable raster scan A (60 Hz)
TIM = 1 enable raster scan B (50 Hz)

CURLO (Cursor Low) This register contains the eight lower order address bits of the RAM cursor address. All FILL screen and character transfer operations begin at the memory location pointed to by this address.

CURLO REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

CURHI (Cursor High) This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8). All FILL screen and character transfer operations begin at the memory location pointed to by this address. In addition, this register contains the Smooth Scroll Offset Values SS3-SS0 which determine the number of scan lines that the data is shifted on the screen. The MSB of this register (SLE-status line enable) is the enable for the non-scrolling status line (this feature is available only on a part programmed for 25 data rows).

CURHI REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SLE	SS3	SS2	SS1	SS0	DA10	DA9	DA8

SLE = 1 enables non-scrolling 25th status line
SLE = 0 disables and blanks non-scrolling status line

SS3-SS0 Smooth Scroll Offset Value

ATTDAT (Attribute Data) This register specifies the visual attributes of the video data and the cursor presentation. The visual attributes specified in the ATTDAT register (DB3-DB0) are enabled or disabled by a TAG bit that is appended to the ASCII character written to the CHARACTER register. Every character on the screen with its TAG bit set is displayed with the same attribute. Changing the Attribute register will change the attribute of every "tagged" character on the screen. The functions of the remaining bits in the ATTDAT register are not affected by the display character's TAG bit.

There are two display modes, "alphanumerics" and "graphics". In the alphanumeric mode, visual attributes may be selected by the TAG bit. In the graphics mode, a tagged character will be a normal alphanumeric character. This allows a screen to display a mix of graphic and alphanumeric characters or visually attributed alphanumeric characters. The display variations of the alphanumerics and graphics modes are summarized by the following:

ATTDAT REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

DB7	MODE SELECT	DB7 = 1	enables graphics mode display (No attributes allowed)
		DB7 = 0	enables alpha mode display
DB6	CURSOR SUPPRESS	DB6 = 1	inhibits VIDEO display at cursor time by forcing the VIDEO output to background level during cursor display time
		DB6 = 0	enables VIDEO display at cursor time Note: a blinking cursor display can be achieved by toggling this bit under processor control.
DB5	CURSOR DISPLAY	DB5 = 1	enables underline cursor display
		DB5 = 0	enables block cursor display Note: An underline cursor in an underline character attribute field will be dashed.
DB4	SCREEN	DB4 = 1	for white screen and black characters
		DB4 = 0	for black screen and white characters Note: this is a screen attribute (versus character attribute) bit and sets the default Video background level.

ENABLED OR DISABLED BY TAG BIT

DB3	CHARACTER SUPPRESS	DB3 = 1	to enable Video suppress
		DB3 = 0	to inhibit Video suppress This bit allows character blinking and blanking under processor control
DB2	INTENSITY	DB2 = 1	allows the INTOUT output pin to go high for the character time
		DB2 = 0	inhibits the INTOUT output pin from going high
DB1	UNDERLINE	DB1 = 1	will cause the character to be underlined
		DB1 = 0	will inhibit the underline
DB0	REVERSE VIDEO	DB0 = 1	will cause the standard foreground and background Video levels (selected with DB4) to be reversed for the character time
		DB0 = 0	will inhibit reverse video

MODE

The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the VTLC after every read/write of the CHARACTER register. Note: The visible cursor position is not affected.

MODE REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AUTO INC	X	X	X	X	X	X	X

DB7 AUTO INCREMENT

DB7 = 1 to enable automatic character address
The RAM address is incremented after the VTLC completes a display memory access initiated by a processor to RAM or RAM to processor character transfer.

DB7 = 0 to disable automatic increment

CHARACTER

This register allows access to the display memory for both byte transfers and FILL operations. In BYTE Transfer Write Mode, the processor first writes a character to this register. The VTLC takes that character and stores it in the display memory in the location specified by the CURLO and CURHI registers. In Byte Transfer Read Mode, the processor reads this register causing the VTLC to fetch the character whose address is specified in the CURLO and CURHI registers from the display memory and place it in the CHARACTER register. The processor then reads the character and initiates another fetch from memory cycle. In FILL mode, writing a byte to this register will initiate a FILL operation. All VTLC/memory data transfers take place during horizontal and vertical video retrace blank time.

CHARACTER REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG BIT + 7 BIT ASCII CHARACTER							

CHARACTER SET

Using the DB7-DB0 data bus I/O pins and the MOD SEL bit in the ATTDAT register, the user can address 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity. Included in the 128 mask programmable characters can be the 96 standard ASCII characters and 32 special characters.

A. (MODE SEL = 1) GRAPHICS MODE

This mode allows an intermix of alpha-numeric and graphics characters. No attributes are permitted in this mode. If TAG BIT = 1, the character will be an alpha-numeric. If TAG BIT = 0, the character will be a graphics character.

CHARACTER REGISTER

ALPHANUMERIC: TAG BIT = 1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG = 1	⟵ ALPHA-NUMERIC CHARACTER ⟶						

DB6-DB0 Specify character

CHARACTER REGISTER

GRAPHICS: TAG BIT = 0

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG=0	W/T	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

DB6 W/T = 1 specifies a wide graphics character
W/T = 0 specifies a thin graphics character

WIDE GRAPHICS ONLY:

DB5-4 SEG6-5 = 1 to turn on graphics entity segment
SEG6-5 = 0 to turn off graphics entity segment

Note that DB5 and DB4 have no meaning in the thin graphics entity.

SECTION V

WIDE AND THIN GRAPHICS:

DB3-0 SEG4-1 if any bit = 1, corresponding graphics entity segment ON

It any bit = 0, corresponding graphics entity segment OFF

B. (MOD SEL = 0) ALPHA-NUMERICS MODE

This mode allows display of alpha-numeric characters with attributes. If DB7 is set to a logical one, the attribute(s) specified in the ATTDAT register will be enabled for that character. If TAG BIT is cleared, attributes will not be enabled for that character.

CHARACTER REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG	← ALPHA-NUMERIC CHARACTER →						

DB7 = 1 to enable attribute(s) for character.
DB7 = 0 to disable attribute(s) for character.

DB6-DB0 Specify character

SEGMENT 6	SEGMENT 3
SEGMENT 5	SEGMENT 2
SEGMENT 4	SEGMENT 1

WIDE GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

	SEGMENT 3
SEGMENT 4	SEGMENT 2 SEGMENT 1

THIN GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

DESCRIPTION OF SYSTEM OPERATION

The VTLC circuitry provides two control functions. One function interprets and controls data from the system processor interface through the data bus DB7-DB0 as shown in the Processor Timing of figure 3. The other function generates and refreshes the video image on the screen through the DD7-DD0 data bus as shown in the Display Memory Timing of figure 2. Because the system data bus is isolated from the display data bus, the VTLC maintains complete control over access to display memory. All data flow between display RAM and the processor or the VTLC takes place through the VTLC. Refer to the VTLC Display Memory Access Timing of figure 7.

DISPLAY MEMORY ACCESS

Processor/display memory access is accomplished through the CHARACTER register of the VTLC. All processor transfers to or from the CHARACTER register take place only when the DONE bit is high. The DONE bit is used to synchronize data transfers between the VTLC and the processor as shown in the Typical Processor To Display Memory Transfer of figure 6. When the processor needs to store a byte of data in the display memory, it will write the byte to the CHARACTER register of the VTLC. The VTLC will immediately reset the DONE bit indicating that the transfer hardware is busy. At the next blanked Video time, the VTLC will store the byte in the display memory, increment the character address, (if auto increment is enabled) and set the DONE bit. When the processor needs to read a byte of data from the display memory, it will read the CHARACTER register. The VTLC will fetch the desired byte from the display memory during the next blanked VIDEO time, increment the character address (if enabled), and set the DONE bit. When the processor detects that the DONE bit is set, it will read the CHARACTER register to get the data byte from the VTLC. This read will reset the DONE bit and cause the VTLC to fetch the next byte of data from the memory.

If auto increment is not enabled, the processor must set the cursor address in the CURLO and CURHI register to the address of the memory location being read from, or written into, before every access to the CHARACTER register.

It should be noted that Auto Increment does not affect the visible cursor location. If auto-increment is enabled, the current character location will equal the cursor position only for the first character transfered following an update of the CURLO and CURHI registers. Note that the DONE bit must be high before attempting to update the cursor registers because the loading of the cursor registers will reset the character position counters to the cursor position.

SMOOTH SCROLL

The VTLC may be programmed to do either "jump" or "smooth" scrolling. Jump scrolling moves the data up or down the monitor screen one data row at a time. Smooth scrolling moves the data up the monitor screen one scan line at a time. The number of scan lines and the rate they move up the screen is under processor control.

Smooth scroll is controlled through manipulation of the SS3-SS0 bits of the CURHI register. These bits represent the binary address of the first scan line of the first data row displayed on the monitor screen (the data row whose beginning address is in the TOSADD register). When the value represented by these bits is incremented, the video data on the monitor screen moves up by the same number of scan lines. After the address of the last scan line of the data row is loaded into the CURHI register and the VIDEO data has moved up the last scan line of the data row, the processor resets the SS3-SS0 address to point to scan line

0 and does a jump scroll. Jump scroll is accomplished by incrementing the RAM address in the TOSADD register by a data row length (so that it points to the address of the first character of the new top data row on the monitor).

When programmed for a data row of 80 characters/data row display (1920 data words), for example, the display RAM contains 25 actual rows of data (2000 RAM locations). If the smooth scroll offset equals zero, the VTLC will display the 1919 RAM locations following the top of screen address when displaying data. The first data row is partially scrolled off the screen and the 25th data row is scrolled onto the screen when the smooth scroll offset is incremented. The VTLC will now display the 1999 RAM locations following the top of screen address (wrapping to 0 after address 1999). After the VTLC does a jump scroll, the processor will program it to erase the line just scrolled off the screen (preparing it to be scrolled onto the screen). This line now becomes the non-displayed 25th data row.

NON-SCROLLING STATUS LINE

The non-scrolling status line is only functional on a VTLC that has been programmed for 25 data rows. This data row will remain stationary at the bottom of the screen and will not move up the screen when the remainder of the display data is scrolled. Otherwise, VIDEO data on the status line may be manipulated as though it were normal display data. The smooth scroll offset will not function properly when the status line is enabled. The memory address of the characters on the status line are always characters 1920–1999.
NOTE: If the part is programmed for 25 data rows an additional mask option must be specified which makes the 25th data row either fixed (always displayed) or a status row (enabled/disabled by the SLE bit).

CHIP RESET

The CRT 9028 and CRT 9128 Chip Reset requires two steps. The system processor first writes the reset address to the address register of the VTLC. The system processor then writes a dummy character to the VTLC Data register. Writing to the Data register resets the chip. The only state affected by the reset function is the setting of the DONE bit in the STATUS register.

ROM CHARACTER BLOCK FORMAT

COLUMN DOT ->	C7	C6	C5	C4	C3	C2	C1	C0
SCAN LINE 0 ->	0	0	0	0	0	0	0	0
SCAN LINE 1 ->	0						0	0
SCAN LINE 2 ->	0						0	0
SCAN LINE 3 ->	0			MASK PROGRAMMABLE			0	0
SCAN LINE 4 ->	0			CHARACTER BLOCK (FONT) 5 X 8			0	0
SCAN LINE 5 ->	0						0	0
SCAN LINE 6 ->	0						0	0
SCAN LINE 7 ->	0						0	0
SCAN LINE 8 ->	0						0	0
SCAN LINE 9 ->	0	0	0	0	0	0	0	0
SCAN LINE 10 ->	0	0	0	0	0	0	0	0
SCAN LINE 11 ->	0	0	0	0	0	0	0	0

Mask programmable options–The ROM character block format above shows the 5X8 mask programmable character font within the character cell as defined by dots C7 through C0 and scan lines 0 through 11.

Dots/Character: 6 dots/character cell => C7 - C2 displayed
7 dots/character cell => C7 - C1 displayed
8 dots/character cell => C7 - C0 displayed

Column dots C0 and C1 will be the same as column dot C7 when more than 6 dots/character cell are specified when generating alpha-numerics.

NOTE: The maximum dot clock crystal frequency is dependent on the dots/character programmed:

DOTS/CHARACTER	MAX XTAL FREQ
6 dots	10.5 MHz max*
7 dots	12.25 MHz max*
8 dots	14.0 MHz max*

*These values are preliminary

Scan Lines per Character: 8 scan lines/character => SL0 - SL7 displayed
9 scan lines/character => SL0 - SL8 displayed
10 scan lines/character => SL0 - SL9 displayed
11 scan lines/character => SL0 - SL10 displayed
12 scan lines/character => SL0 - SL11 displayed

Thin and Wide Graphics: Dots mask programmed for vertical column C2 will be the same as backfill Columns 0 and 1 when generating wide and thin graphics.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

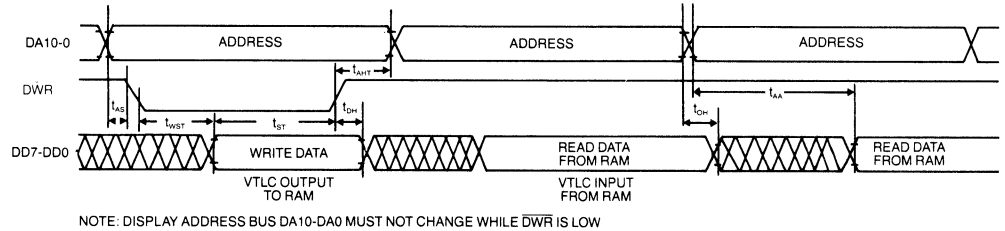
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{cc} = +5V ±5%, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, Vil			0.8	V	
High-Level, Vih	2.2			V	
OUTPUT VOLTAGE LEVELS					
Low-level, Vol			0.4	V	All outputs except $\overline{\text{VIDEO}}$, CSYNC, INTOUT, HSYNC, $\overline{\text{VSYNC}}$; Iol = 1.6 mA
Low-level, Vol			0.4	V	$\overline{\text{VIDEO}}$, CSYNC, INTOUT, HSYNC, $\overline{\text{VSYNC}}$; Iol = 0.4 mA
High-level, Voh	2.4			V	All outputs except $\overline{\text{VIDEO}}$, CSYNC, INTOUT, HSYNC, $\overline{\text{VSYNC}}$; Ioh = −40 µA
High-level, Voh	2.4			V	$\overline{\text{VIDEO}}$, CSYNC, INTOUT, HSYNC, $\overline{\text{VSYNC}}$; Ioh = −20 µA
INPUT LEAKAGE CURRENT					
High-level, Iih			10	µA	All inputs; Vin = Vcc
Low-level, Iil			−10	µA	All inputs except $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$; Vin = .04V
Low-level, Iil			−200	µA	$\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$; Vin = 0.4V
INPUT CAPACITANCE					
All inputs, Cin			15	pF	
OUTPUT LOAD					
C_L			15	pF	Except DB7-0
C_L			100	pF	DB7-0
POWER SUPPLY CURRENT					
Icc		125		mA	
AC CHARACTERISTICS					
CLOCK FREQUENCY, fin	1.0		14.0	MHz	
DISPLAY MEMORY TIMING					
Address Set-up Time					
t_{AS}	20			ns	
Write Strobe Set-up Time					
t_{WST}	80			ns	
Data Set-up Time					
t_{ST}	80			ns	
Data Hold Time					
t_{DH}	10		25	ns	

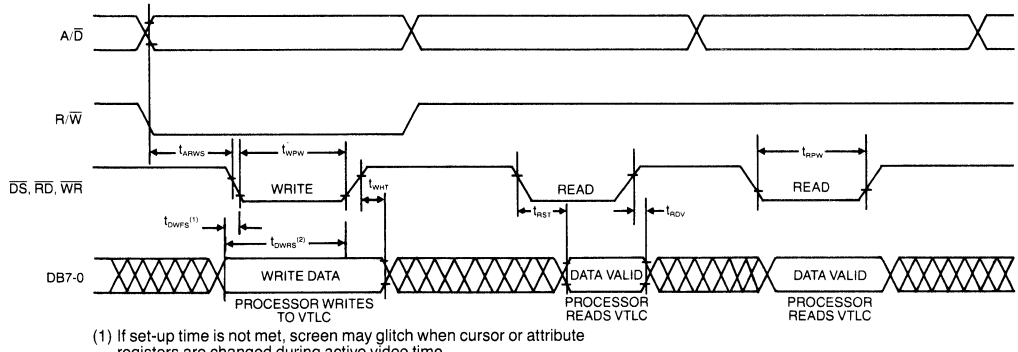
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Address Hold Time t_{AHT}	25			ns	
Output Hold From Address Change t_{OH}	15			ns	
Address Access Time t_{AA}			250	ns	
PROCESSOR TIMING					
Address Read/Write Set-up t_{ARWS}	160			ns	
Write Pulse Width t_{WPW}	160			ns	
Write Hold Time t_{WHT}	15			ns	
Read Set-up Time t_{RST}			200	ns	
Read Data Valid T_{RDV} ·	0			ns	
Read Pulse Width t_{RPW}	250			ns	
Data Write Falling Set-up t_{DWFS}	120			ns	
Data Write Rising Set-up t_{DWRS}	160			ns	

Crystal specification (Applies for 4-14 MHz):
- Series Resonant
- 50 ohms max series resistance
- 1.5 pf typ parallel capacitance
- Operation below 4 MHz requires external crystal oscillator



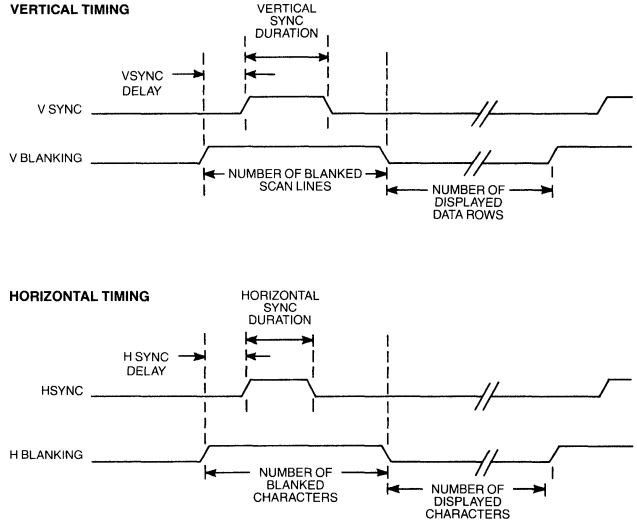
NOTE: DISPLAY ADDRESS BUS DA10-DA0 MUST NOT CHANGE WHILE $\overline{DWR}$ IS LOW

FIGURE 2. DISPLAY MEMORY TIMING



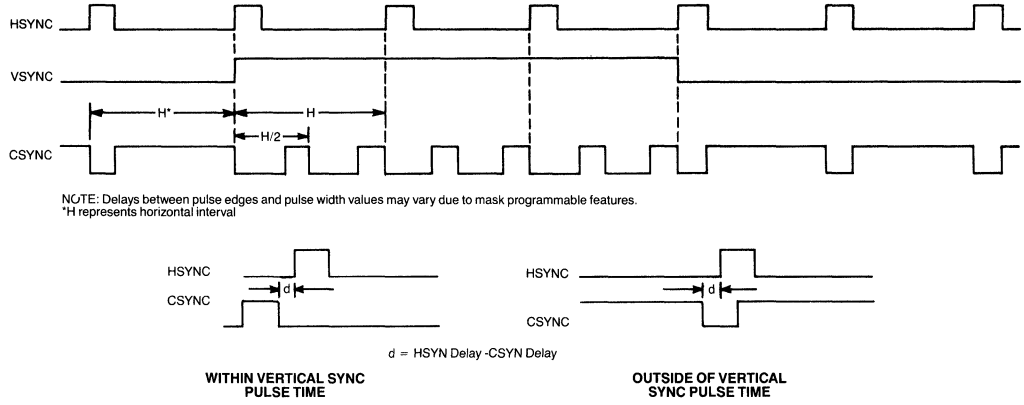
(1) If set-up time is not met, screen may glitch when cursor or attribute registers are changed during active video time.
(2) Minimum set-up time to ensure valid data into VTLC internal registers.

FIGURE 3. PROCESSOR TIMING



NOTE: Video parameters above are mask programmable

FIGURE 4. VERTICAL AND HORIZONTAL SYNC TIMING



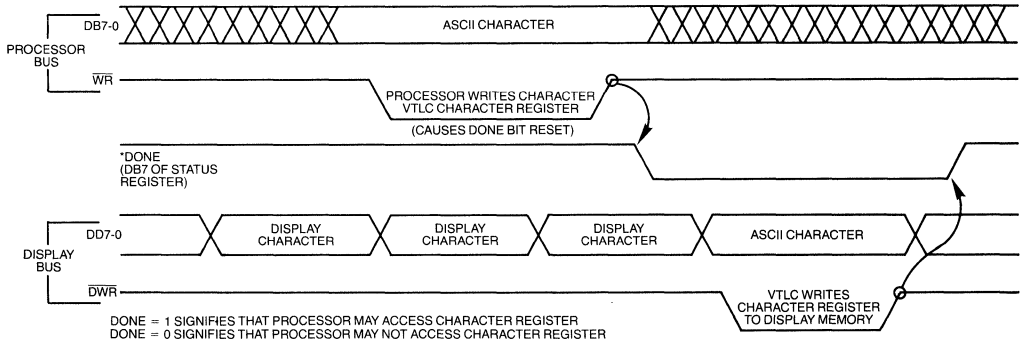
NOTE: Delays between pulse edges and pulse width values may vary due to mask programmable features.
*H represents horizontal interval

d = HSYN Delay -CSYN Delay

WITHIN VERTICAL SYNC PULSE TIME

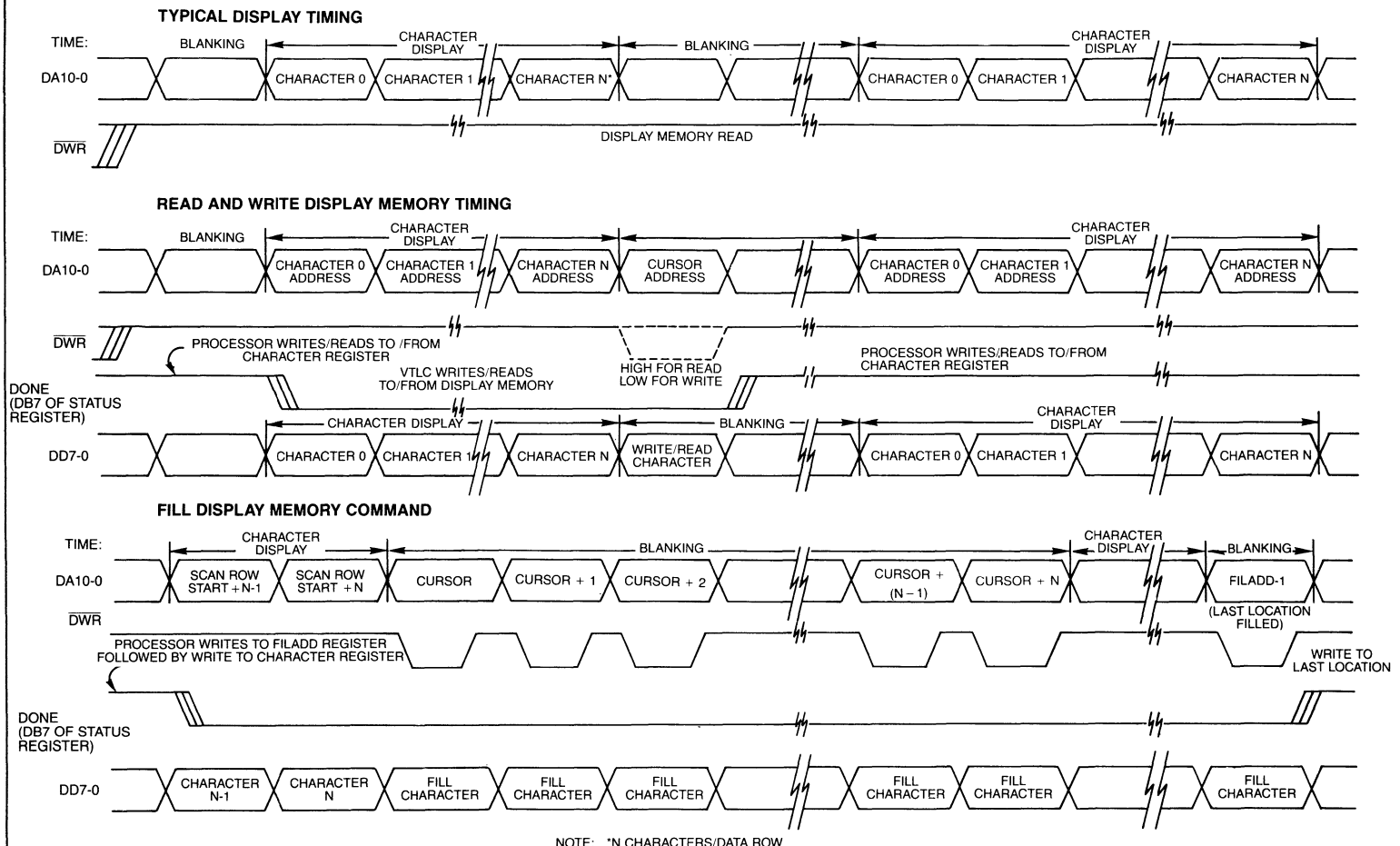
OUTSIDE OF VERTICAL SYNC PULSE TIME

FIGURE 5. VIDEO SIGNAL TIMING



DONE = 1 SIGNIFIES THAT PROCESSOR MAY ACCESS CHARACTER REGISTER
DONE = 0 SIGNIFIES THAT PROCESSOR MAY NOT ACCESS CHARACTER REGISTER

FIGURE 6. TYPICAL PROCESSOR TO DISPLAY MEMORY TRANSFER



NOTE: *N CHARACTERS/DATA ROW

FIGURE 7. VTLC DISPLAY MEMORY ACCESS TIMING

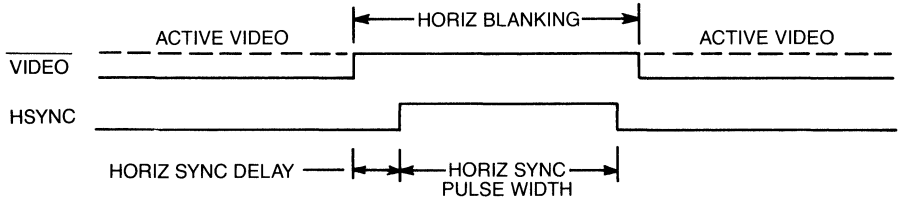
I. ROM CHARACTER BLOCK FORMAT:

COLUMN DOT –>	C7	C6	C5	C4	C3	C2	C1
SCAN LINE 0 –>	0	0	0	0	0	0	0
SCAN LINE 1 –>	0						0
SCAN LINE 2 –>	0						0
SCAN LINE 3 –>	0		CHARACTER BLOCK 5 X 8 CELL				0
SCAN LINE 4 –>	0						0
SCAN LINE 5 –>	0						0
SCAN LINE 6 –>	0						0
SCAN LINE 7 –>	0						0
SCAN LINE 8 –>	0						0
SCAN LINE 9 –>	0	0	0	0	0	0	0

DOTS PER CHARACTER: 7
DOT CLOCK XTAL FREQUENCY (MHz): 10.92

II. HORIZONTAL TIMING (IN CHARACTER TIMES):

CHARACTERS PER DATA ROW: 80
HORIZONTAL BLANKING: 20
HORIZONTAL SYNC DELAY: 4
HORIZONTAL SYNC PULSE WIDTH: 8
HORIZONTAL SYNC POLARITY: NEGATIVE ACTIVE

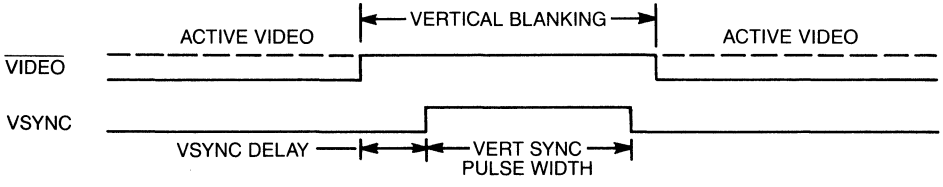


III. VERTICAL TIMING:

CHARACTER ROWS: 24
SCAN LINES PER CHARACTER: x 10
TOTAL VISIBLE SCAN LINES: 240
VERTICAL SYNC POLARITY: NEGATIVE ACTIVE

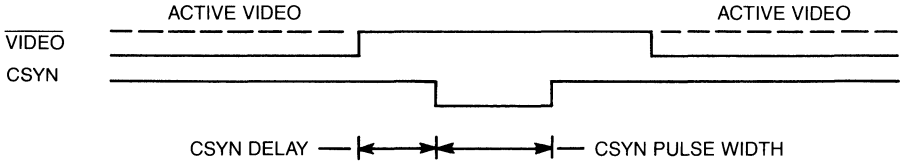
IV. VERTICAL SYNC TIMING (IN SCAN LINES):

60 Hz VERTICAL BLANKING: 20
60 Hz VERTICAL SYNC DELAY: 4
60 Hz VERTICAL SYNC PULSE WIDTH: 8
ALTERNATE (50 Hz) VERTICAL BLANKING: 72
ALTERNATE (50 Hz) VERTICAL SYNC DELAY: 30
ALTERNATE (50 Hz) VERTICAL SYNC PULSE WIDTH: 10



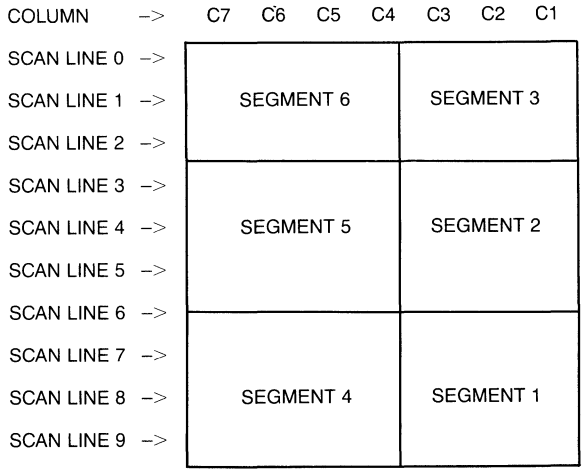
V. COMPOSITE SYNC OUTPUT (IN CHARACTER TIMES):

COMPOSITE SYNC DELAY: 2
COMPOSITE SYNC PULSE WIDTH: 8

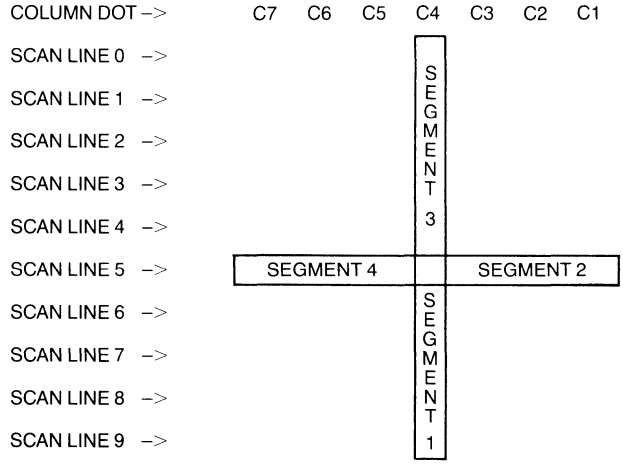


VI. UNDERLINE ATTRIBUTE AND CURSOR LINE: SCAN LINE 9

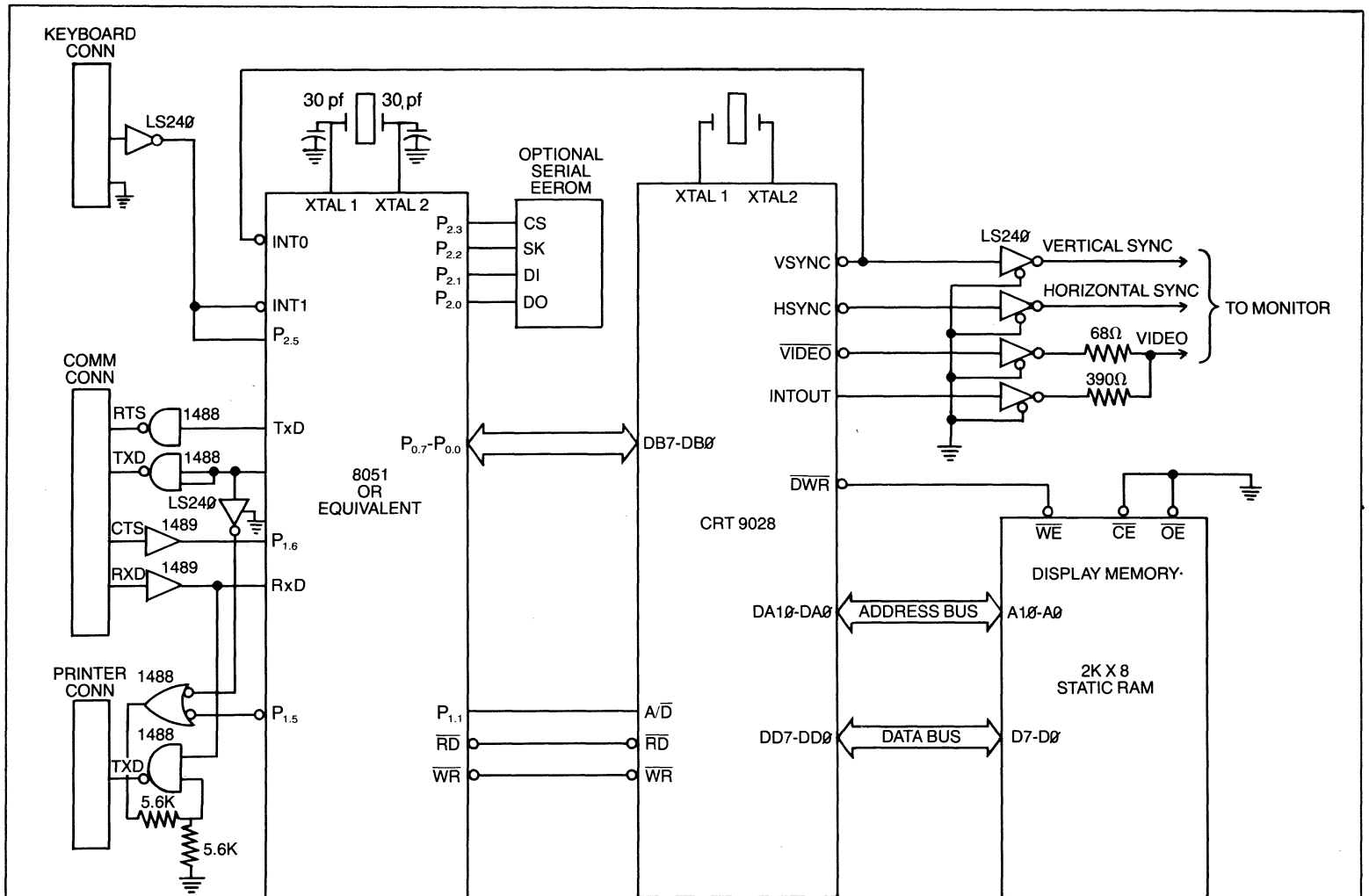
VII. WIDE GRAPHICS FIGURE DEFINITION:



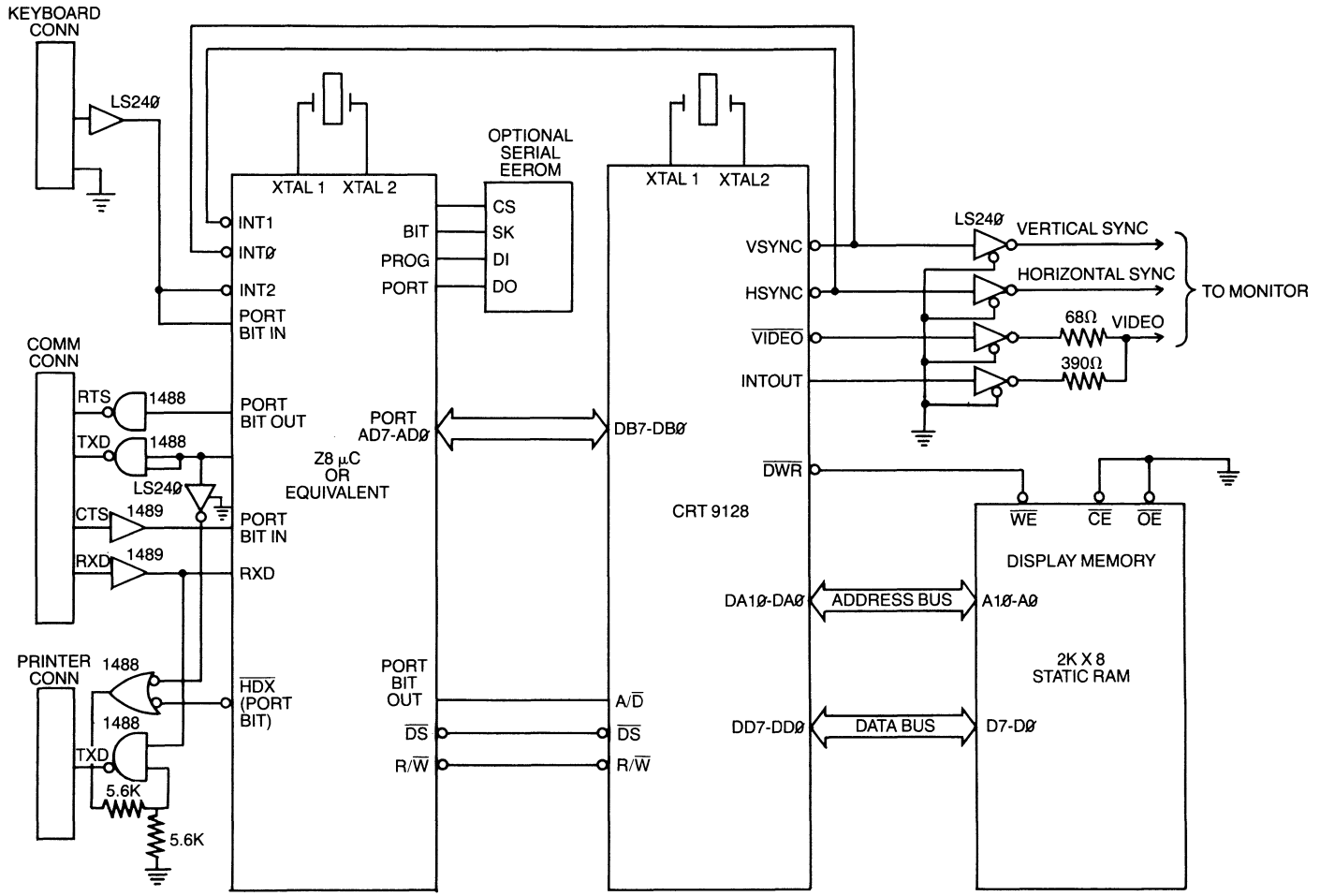
VIII. THIN GRAPHICS FIGURE DEFINITION:



SEGMENT 4 = SCAN LINE 5; C7, C6, C5, C4
SEGMENT 3 = C4; SCAN LINES 0, 1, 2, 3, 4, 5
SEGMENT 2 = SCAN LINE 5; C4, C3, C2, C1
SEGMENT 1 = C4; SCAN LINES 5, 6, 7, 8, 9



CRT 9028
TYPICAL APPLICATION



CRT 9128
TYPICAL APPLICATION

CRT 9028/9128-000

DD6...DD4 \ DD3...DD0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2
000	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
001	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
010	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
011	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
100	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
101	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
110	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
111	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL

STANDARD MICROSYSTEMS CORPORATION

CRT 9041A
CRT 9041B
CRT 9041C

CRT Video Attributes Controller VAC

FEATURES

- ☐ On chip 12 bit shift register
  - 3 speed versions:
    - CRT 9041A -33MHz
    - CRT 9041B -30MHz
    - CRT 9041C -28.5MHz
- ☐ On chip attributes logic
  - Reverse video
  - Character blank
  - Character blink to blank
  - Character blink between any two of four video intensity levels
  - Two independent underline attributes
  - Four video intensity levels
  - Two general purpose attributes
- ☐ Wide graphics mode
- ☐ Thin graphics mode
- ☐ Reverse screen input
- ☐ On chip logic for double height/double width data rows
- ☐ Accepts scan line information in parallel or serial format
- ☐ Supports multiple cursors
- ☐ Four cursor modes dynamically selectable via 2 input pins
  - Underline
  - Blinking underline
  - Reverse video block
  - Blinking reverse video block
- ☐ Mask programmable cursor blink rate and duty cycle

PIN CONFIGURATION

CURS	1	40	Vcc
RETBL	2	39	GP2O
$\overline{LD}$/SH	3	38	GP1O
VDC	4	37	HINTO
VIDEO	5	36	BOLDO
DST	6	35	ATTEN
D11	7	34	CHABL
D10	8	33	UL2/GP2I
D9	9	32	XCURS/GP1I
D8	10	31	HINTI
D7	11	30	BOLDI
D6	12	29	BLINK
D5	13	28	RS
D4	14	27	REVID
D3	15	26	MS1
D2	16	25	MSØ
D1	17	24	$\overline{VSYNC}$
D0	18	23	SL0/SLD
SL3/BKC	19	22	SL1/$\overline{SLG}$
GND	20	21	SL2/BLC

- ☐ Mask programmable character blink rate and duty cycle
- ☐ On chip data and attribute latches
- ☐ Externally multiplexible for higher video rates
- ☐ Dot stretch on a character basis
- ☐ + 5 volt operation
- ☐ TTL compatible
- ☐ MOS n-channel silicon gate COPLAMOS® process
- ☐ Compatible with the CRT 5037 and CRT 9007

SECTION V

GENERAL DESCRIPTION

The SMC CRT 9041 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device containing graphics logic, attributes logic, data and attribute latches, cursor control, and a high speed video shift register. The CRT 9041, a character generator ROM, and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9041 serial video output may be connected directly to a CRT monitor's video input. The CRT 9041 is available in three speed versions: 28.5 MHZ (9041C), 30 MHZ (9041B) and 33 MHZ (9041A).

The CRT 9041 attributes include: reverse video, 2 underlines, character blank, and character blink. Character blink may be to background, or between any 2 of 4 possible video intensity levels. Two output pins define 4 video levels: half, three quarters, full, and bold. When used in conjunction with the CRT 9007 VPAC™, the CRT 9041 will provide double height or double width data row display.

Two cursor input pins allow simultaneous display of two cursors. Each of these cursors can be displayed in one of 4 display formats: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, each cursor may be displayed in any of the 4 cursor display modes as selected via the two input pins. When used in the parallel scan line input mode, each cursor display mode is mask programmable and fixed at the time of manufacture.

The cursor format or the parallel scan line information can be changed on a character by character basis to allow different cursor formats on separate areas of the screen or for superscripted or subscripted characters.

Two graphics modes are provided. In the wide graphics mode, the CRT 9041 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms. In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided through the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal lines.

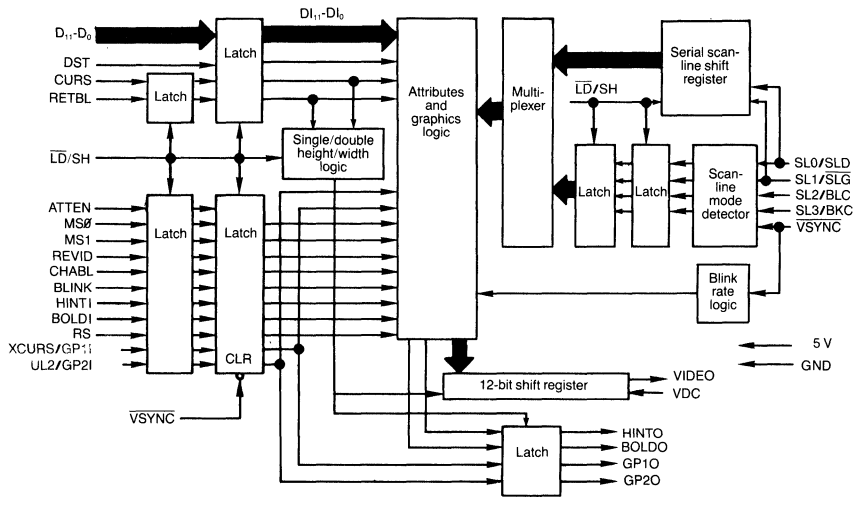


FIGURE 1: CRT 9041 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Cursor	CURS	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9041 enters the double width mode. See section entitled "Cursor Formats" for details.
2	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next $\overline{LD}$/SH pulse. This forces the Video output to a low voltage level, independent of all attributes for blanking the CRT during horizontal and vertical retrace time.
3	$\overline{Load}$/Shift	$\overline{LD}$/SH	The 12 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of $\overline{LD}$/SH. If the period of this signal is greater than 12 dots, video information will be supplied in the form of backfill dots as specified in the mask programmed options.
4	Video Dot Clock	VDC	This input clock controls the rate at which video data is shifted out on the VIDEO output.
5	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video data is shifted out on the rising edge of the video dot clock VDC. The timing of the $\overline{LD}$/SH input will determine the number of backfill dots.
6	Dot Stretch	DST	This input determines if all dots in the video stream will be stretched by one dot. In normal video, all 1's are stretched and in reverse video all 0's are stretched. This input enters the CRT 9041 along with D11-D0 with one $\overline{LD}$/SH delay. Updating can occur each $\overline{LD}$/SH to allow selected dot stretching on a character by character basis. A high voltage will cause the dot stretch and a low voltage will inhibit the dot stretch mechanism. See section entitled "Dot Stretch" for details.
7-18	Data	D11-D0	In the character mode, the data on these inputs are passed through the attributes logic into the 12 bit high speed video shift register. The binary information on D11 will be the first bit output after the $\overline{LD}$/SH input goes low. In the thin or wide graphics mode only the D11 through D4 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Tables 5 and 6 illustrate the wide and thin graphics modes respectively and their relationships to D11-D4.

PIN NO.	NAME	SYMBOL	FUNCTION
19	Scan line 3/ Block Cursor	SL3/BKC	Information on this input is delayed 2 $\overline{LD}$/SH cycles before entering the Attribute and Graphics Logic. As a result, this input can be changed on a character basis to allow the cursor format to enter the CRT 9041 as an attribute or to allow the parallel scan line information to change on a character basis. This input has two separate functions depending on the way scan line information is presented to the CRT 9041. In the Parallel Scan Line Mode, this input is the most significant bit of the binary scan line row address. In the Serial Scan Line Mode, this input controls the cursor's physical dimensions. If high, the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed. (See Table 4.)
20	Ground	GND	Ground
21	Scan line 2/ Blink Cursor	SL2/BLC	Information on this input is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic. As a result, this input can be changed on a character basis to allow the cursor format to enter the CRT 9041 as an attribute or to allow the parallel scan line information to change on a character basis. This input has two separate functions depending on the way scan line information is presented to the CRT 9041. (See Table 4.)
22	$\overline{\text{Scan Line 1/}}$ $\overline{\text{Scan Line Gate}}$	SL1/$\overline{SLG}$	This input has two separate functions depending on the way scan line information is presented to the CRT 9041. In the Parallel Scan Line Mode this input is the next to the least significant bit of the binary scan line row address. In this mode the information presented is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic to allow the scan line information to be changed on a character basis. In the Serial Scan Line Mode this input will be low for 5 or 6 $\overline{LD}$/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more $\overline{LD}$/SH pulses, the CRT 9041 will assume the parallel input scan line row address mode.
23	Scan line 0/ Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the CRT 9041. Refer to Table 4. In the Parallel Scan Line Mode this input is the least significant bit of the binary scan line row address. The information presented in this mode is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic to allow the scan line information to be changed on a character basis. In the Serial Scan Mode this input will present the scan line information in serial form (least significant bit first) to the CRT 9041 and permits the proper scan line information to enter the serial scan line shift register during the $\overline{LD}$/SH pulses framed by $\overline{SLG}$.
24	$\overline{\text{Vertical}}$ $\overline{\text{Sync}}$	$\overline{VSYNC}$	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the on-chip mask programmable blink rate dividers. The cursor blink rate can be a multiple or submultiple of the character blink which is selectable as a mask program option (see Table 10.) In addition, the internal attributes are reset when this input is low. The $\overline{VSYNC}$ input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".
25 26	Mode Select 0 Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the CRT 9041 as follows: MS1 / MS0 / MODE 0 / 0 / Wide graphics mode 1 / 0 / Thin graphics mode 0 / 1 / Character mode without underline one 1 / 1 / Character mode with underline one See section entitled Display Modes for details.
27	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics Logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics Logic will invert the data before presenting it to the video shift register.
28	Reverse Screen	RS	This input defines the base background level of the screen. A low on this input will cause normal (non-reverse) video to appear white with a black background. A high on this input will cause normal (non-reverse) video to appear black with a white background.

PIN NO.	NAME	SYMBOL	FUNCTION
29	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. This input allows a character to blink between 2 of 4 levels of video or to the background level according to one of the 3 mask programmable blink tables (Tables 1, 2 and 3). The duty cycle for the character blink is mask programmable at either 75/25 (off/on) or 50/50.
30	Bold in	BOLDI	The BOLDI input along with the BOLDO output provides a user with a Bold (high intensity) attribute on a character by character basis. Data input on BOLDI will appear at BOLDO with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise the voltage level of the video output to produce the bold attribute.
31	Half intensity in	HINTI	The HINTI input along with the HINTO output provides a user with a half intensity attribute on a character by character basis. Data input on HINTI will appear at HINTO with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to lower the voltage level of the video output to produce the half intensity attribute.
32	Extra Cursor/ General Purpose Attribute 1 In	XCURS/ GP1I	This input has a dual function. It can produce a second cursor with either a dynamically selectable format or a masked programmed format. If no scan line(s) are programmed for the XCURS format (or if the programmed scan lines are beyond the range of the actual scan lines), this input will simply be pipelined through the CRT 9041 to produce a user controlled general purpose attribute. Data appearing on this input is pipelined to the GP1O with the same delay as that from any other attribute input and can affect the video as desired. Whether XCURS is used or not, data appearing on this input will be pipelined to the GP1O output.
33	Underline 2 General Purpose Attribute 2 In	UL2/ GP2I	This input has a dual function. It can produce a second underline (UL2) at the masked programmed scan line(s). If no scan line(s) are programmed for underline 2, this input will simply be pipelined through the CRT 9041 to produce a user controlled general purpose attribute. Data appearing on this input is pipelined to the GP2O with the same delay as that from any other attribute input and can affect the video as desired. Whether UL2 is used or not, data appearing on this input will be pipelined to the GP2O output. Note that underline 1 is selected via the MS0 and MS1 inputs.
34	Character Blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID and RS) thus providing a constant video level for the entire length of the character block. Only the cursor is visible in a character blank field.
35	Attribute Enable	ATTEN	When this input is high, the internal attribute latch is updated at the positive going edge of the $\overline{LD}$/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK, BOLDI, HINTI, UL2/GP2I, DST RS, and XCURS/GP1I inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tying this input high (thus allowing "invisible" attributes). All attributes are reset by the $\overline{VSYNC}$ input.
36	Bold out Out	BOLDO	This output is used in conjunction with the BOLDI input to provide a three character pipeline delay when creating a high intensity effect on the video bit stream. In addition, this output is activated independent of the BOLDI signal during certain character and cursor blink operations according to Tables 1, 2 and 3.
37	Half Intensity Out	HINTO	This output is used in conjunction with the HINTI input to provide a three character pipeline delay when creating a half intensity effect on the video bit stream. In addition, this output is activated independent of the HINTI signal during certain character and cursor blink operations according to Tables 1, 2 and 3.
38	General Purpose Attribute 1 out	GP1O	This output is used in conjunction with the XCURS/GP1I input and provides a three character pipeline delay to allow for general purpose attributes to be implemented.
39	General Purpose Attribute 2 out	GP2O	This output is used in conjunction with the UL2/GP2I input and provides a three character pipeline delay to allow for general purpose attributes to be implemented.
40	Supply Voltage	Vcc	+ 5 volt power supply.

ATTRIBUTES FUNCTIONS

Reverse Video – The REVID input causes inverted data to be loaded into the video shift register.

Character Blank – The CHABL input forces the video to go to the current background level as defined by Reverse Video and Reverse screen. This attribute blanks all video with the exception of both cursor displays.

Underline – MS1, MS0 = 1,1 or UL2 = 1: either condition forces the video to the inverse of the background level (all 1's or all 0's) for all scan line(s) programmed for underline. The two underlines are independent.

Half Intensity – The HINTI input and the HINTO output allow a half intensity attribute to be carried through the pipeline of the CRT 9041. An external mixer can be used to combine VIDEO and HINTO to create a decreased white level in the video.

Retrace Blank – The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Bold – The BOLDI input and the BOLDO output allow a bold (high intensity) attribute to be carried through the pipeline of the CRT 9041. An external mixer can be used to combine VIDEO and BOLDO to create an increased white level in the video.

Blink – The BLINK input will cause characters to blink in a number of mask programmable ways. Referring to Tables 1, 2 or 3, video can be made to blink between 2 or 4 possible video levels with either a 50/50 on/off or a 75/25 on/off duty cycle. The tables also illustrate that the blink levels can be programmed to be a function of the reverse video input attribute. A blinking cursor overrides the character blink for the scan lines programmed for cursor. The CRT 9041 can implement character blinking in several different mask programmable visual formats as shown in the Tables. The blink function illustrated in Table 2 implements CRT 9021 compatibility blinking.

The CRT 9041 may be mask programmed for one of three combinations of blinking operation. These are illustrated respectively in Tables 1, 2, and 3. Since 4 levels of video are possible, Tables 1 and 3 define the video blinking between 2 video levels and Table 2 defines the video blinking to the background level making this table compatible with the CRT 9021.

The Non-blink Option Table 1A shows the state of the video DATA (DATA = non inverted video, $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 1A result in a non-character blink display as compared to the video DATA shown in the Blink Combinations Option Table 1B.

(1) Reverse video = (REVID) and ($\overline{RS}$) or ($\overline{REVID}$) and (RS)

TABLE 1A: NON-BLINK COMBINATIONS OPTION TABLE

INPUTS					OUTPUTS	
BLINK	REVERSE VIDEO (1)	BOLDI	HINTI	VIDEO	BOLDO	HINTO
0	0	0	0	DATA	0	0
0	0	0	1	DATA	0	1
0	0	1	0	DATA	1	0
0	0	1	1	DATA	1	1
0	1	0	0	$\overline{DATA}$	0	1
0	1	0	1	$\overline{DATA}$	0	1
0	1	1	0	$\overline{DATA}$	0	0
0	1	1	1	$\overline{DATA}$	1	1

TABLE 1B: BLINK COMBINATIONS OPTION TABLE

INPUTS				CHARACTER BLINK WITHOUT CURSOR (2)		OUTPUTS			
BLINK	REVERSE VIDEO (1)	BOLDI	HINTI			BOLDO		HINTO	
				A*	B*	A*	B*	A*	B*
1	0	0	0	DATA	DATA	0	0	0	1
1	0	0	1	DATA	DATA	0	0	1	0
1	0	1	0	DATA	DATA	1	0	0	0
1	0	1	1	DATA	DATA	1	0	1	0
1	1	0	0	$\overline{DATA}$	$\overline{DATA}$	0	0	0	1
1	1	0	1	$\overline{DATA}$	$\overline{DATA}$	0	0	0	1
1	1	1	0	$\overline{DATA}$	$\overline{DATA}$	0	1	0	0
1	1	1	1	$\overline{DATA}$	$\overline{DATA}$	0	1	0	1

The Blink Combinations Option Table 1B shows the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 1B result in a blinking character display as compared to the non-blinking video DATA shown in the Non-blink Combinations Option Table 1A. Since 4 levels of video are possible, Table 1B defines video blinking between 2 video levels. This is shown in the explanation Table 1C below. It should be noted that the designation NORMAL, ½ INTENSITY, ¾ INTENSITY and BOLD have been used arbitrarily. The actual video levels caused by the BOLDO and HINTO are defined by the external video mixing circuit.

TABLE 1 C

BOLDO	HINTO	INTENSITY LEVEL	BLINK BETWEEN THESE 2 LEVELS (OFF-ON) NON REVERSE VIDEO	REVERSE VIDEO
0	0	NORMAL (N)	N - ½	N - ½
0	1	½ INTENSITY (½)	½ - N	N - ½
1	0	BOLD (B)	B - N	N - B
1	1	¾ INTENSITY (¾)	¾ - N	N - ¾

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(2) The combinations in Table 1 allow the user to define the cursor and the character blink interaction. A non-blinking cursor adds one more inversion to either a non-blinking character or a blinking character. A blinking cursor overrides a character blink for the scan lines programmed for cursor. A blinking cursor will introduce and then remove one more inversion to either a non-blinking character or a blinking character.

TABLE 2A: ALTERNATE NON-BLINK COMBINATIONS FOR CRT 9021 COMPATIBILITY

INPUTS					OUTPUTS	
BLINK	REVERSE VIDEO	BOLDI	HINTI	VIDEO	BOLDO	HINTO
0	0	0	0	DATA	0	0
0	0	0	1	DATA	0	1
0	0	1	0	DATA	1	0
0	0	1	1	DATA	1	1
0	1	0	0	$\overline{DATA}$	0	0
0	1	0	1	$\overline{DATA}$	0	1
0	1	1	0	$\overline{DATA}$	1	0
0	1	1	1	$\overline{DATA}$	1	1

The Alternate Non-blink Combinations for CRT 9021 Compatibility Table 2A show the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 2A result in a non-character blink display as compared to video DATA shown in Alternate Blink Combinations for CRT 9021 Compatibility Table 2B.

TABLE: 2B BLINK COMBINATIONS OPTION TABLE

INPUTS				CHARACTER BLINK WITHOUT CURSOR (1)	OUTPUTS			
BLINK	REVERSE VIDEO	BOLDI	HINTI		BOLDO		HINTO	
					A*	$\overline{B^*}$	A*	$\overline{B^*}$
1	0	0	0	DATA 0	0	0	0	0
1	0	0	1	DATA 0	0	0	1	1
1	0	1	0	DATA 0	1	1	0	0
1	0	1	1	$\overline{DATA}$ 0	1	1	1	1
1	1	0	0	$\overline{DATA}$ 1	0	0	0	0
1	1	0	1	$\overline{DATA}$ 1	0	0	1	1
1	1	1	0	$\overline{DATA}$ 1	1	1	0	0
1	1	1	1	$\overline{DATA}$ 1	1	1	1	1

The Alternate Blink Combinations for CRT 9021 Compatability Table 2B show the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 2B result in a blinking character display as compared to the non-blinking video DATA shown in the Alternate Non-Blink Combinations for CRT Compatibility Table 2A. In this table, the BOLDO and HINTO attributes are controlled by the BOLDI and HINTI attributes making them truly general purpose.

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(1) The combinations in Table 2 allow the user to define the cursor and the character blink interaction. A non-blinking cursor adds one more inversion to either a non-blinking character or a blinking character. In both cases the character blinks to the background video level. A blinking cursor overrides a character blink for the scan lines programmed for cursor. A blinking cursor will introduce and then remove one more inversion to either a non-blinking cursor or a blinking character.

TABLE 3A: NON-BLINK COMBINATIONS FOR THE STANDARD CRT 9041 (CRT 9041-004)

INPUTS					OUTPUTS	
BLINK	REVERSE VIDEO	BOLDI	HINTI	VIDEO	BOLDO	HINTO
0	0	0	0	DATA	0	0
0	0	0	1	DATA	0	1
0	0	1	0	DATA	1	0
0	0	1	1	DATA	1	1
0	1	0	0	$\overline{DATA}$	0	0
0	1	0	1	$\overline{DATA}$	0	1
0	1	1	0	$\overline{DATA}$	1	0
0	1	1	1	$\overline{DATA}$	1	1

The Non-blink Combinations for the Standard CRT 9041 of Table 3A shows the state of the video data (DATA = non inverted video; $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 3A result in a non-character blink display as compared to video DATA shown in the Blink Combinations for the Standard CRT 9041 of Table 3B.

TABLE 3B: BLINK COMBINATIONS FOR THE STANDARD CRT 9041 (CRT 9041-004)

INPUTS					OUTPUTS			
BLINK	REVERSE	BOLDI	HINTI	NON-CURSOR(2)	BOLDO		HINTO	
					A*	$\overline{B^*}$	A*	$\overline{B^*}$
1	0	0	0	DATA	DATA	0	0	0	1
1	0	0	1	DATA	DATA	0	1	1	1
1	0	1	0	DATA	DATA	1	0	0	0
1	0	1	1	DATA	DATA	1	0	1	0
1	1	0	0	$\overline{DATA}$	$\overline{DATA}$	0	0	0	1
1	1	0	1	$\overline{DATA}$	$\overline{DATA}$	0	1	1	1
1	1	1	0	$\overline{DATA}$	$\overline{DATA}$	1	0	0	0
1	1	1	1	$\overline{DATA}$	$\overline{DATA}$	1	0	1	0

The Blink Combinations for the Standard CRT 9041 of Table 3B shows the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 3B result in the blinking character display as compared to the non-blinking video DATA shown in the Non-Blink Combinations for the Standard CRT 9041 Table 3A. Since 4 levels of video are possible, Table 3B defines video blinking between 2 video levels. This is shown by the explanation Table 3C below. It should be noted that the designation NORMAL, ½ INTENSITY, ¾ INTENSITY and BOLD have been used arbitrarily. The actual video level caused by the BOLDO and HINTO are defined by the external video mixing circuit.

TABLE 3C

BOLDO	HINTO	INTENSITY LEVEL	BLINK BETWEEN THESE 2 LEVELS (OFF-ON) NON REVERSE VIDEO	REVERSE VIDEO
0	0	NORMAL (N)	N - ½	N - ½
0	1	½ INTENSITY (½)	½ - ¾	½ - ¾
1	0	BOLD (B)	B - N	B - N
1	1	¾ INTENSITY (¾)	¾ - N	¾ - N

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(2)The scan lines programmed for a non-blinking cursor force a non-blinking or blinking character to a normal video level and introduce one more level of inversion. A blinking cursor adds one more level of inversion to the video during the blink time to a non-blinking or blinking character.

CURSOR FORMATS

Four cursor formats are possible with the CRT 9041. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option for each cursor independently. If the serial scan line input is used, the cursor format is dynamically selectable on a character by character basis via input pins 21 and 19 (SL2/BLC, SL3/BKC). See Table 4. The four cursor formats are as follows:

Underline – The cursor will appear as an underline. The position and width of the cursor underline is mask programmed. An underline cursor will add one more level of inversion to the video on the programmed scan line(s) for underline cursor.

Blinking Underline – The cursor will appear as an underline and introduce and then remove one more level of inversion to the video on the programmed scan line(s) for cursor underline. The cursor blink rate and duty cycle is mask programmable as outlined in Tables 1, 2 or 3.

Reverse Video Block – The cursor will appear as a reverse video block. The block cursor will add one more level of inversion to the video for all scan lines in the character cell.

Blinking Reverse Video – The cursor will appear as a blinking reverse video block. The cursor will introduce and then remove one more level of inversion to the video for all scan lines in the character cell. The cursor blink rate and duty cycle is mask programmable as outlined in Tables 1, 2 or 3.

In the parallel scan line mode it is possible to change the scan line count on a character by character basis. If the scan inputs are stable a time TS2 (figure 2) prior to the next rising edge of the LD/SH input the scan line count will enter the delay latch of the CRT 9041. In the serial scan line mode, it is possible to change the cursor format on a character by character basis with the timing identical to that described in the parallel scan line mode (TS2). This timing is shown in the AC timing diagram, Figure 2.

TABLE 4: CURSOR FORMATS

Scan Line Input Mode	(PIN21) SL2/BLC	(PIN19) SL3/BKG	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	X	X	Mask programmable only

DISPLAY MODES

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 6a and 6b illustrate a typical CRT 9041 configuration which operates in all display modes for the parallel and serial scan line modes respectively.

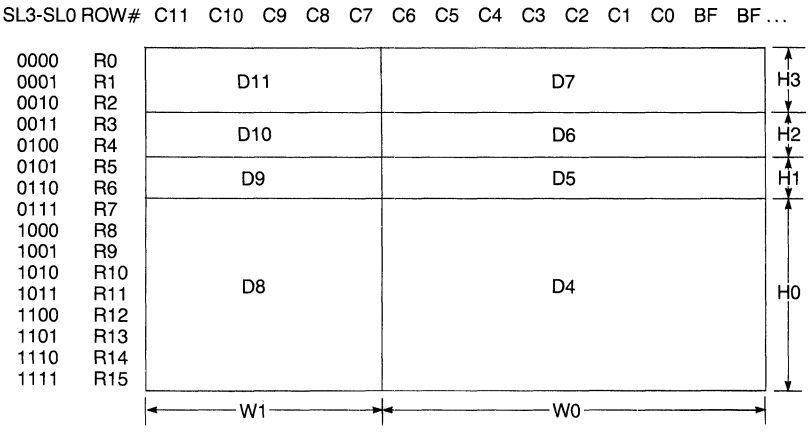
MS1,MS0 = 00–Wide Graphics Mode.
In this display mode, inputs D11-D4 define a graphic entity as illustrated in Table 5. Note that individual bits in D11-D4 will illuminate particular portions of the character block. Table 5 shows all programming ranges possible when defining the wide graphics boundaries. Only underline 2 is possible in this display mode.

MS1,MS0 = 10–Thin Graphics Mode.
In this display mode inputs D11-D4 define a graphic entity as illustrated in Table 6. Note that individual bits in D11-D4 will illuminate particular horizontal or vertical line segments within the character block. Table 6 shows all programming ranges possible when defining the thin graphics boundaries. Only underline 2 is possible in this display mode.

MS1,MS0 = 01–Character Mode without Underline 1.
In this display mode, inputs D11-D4 go directly from the input latch to the video shift register via the Attributes and Graphics Logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixel on the CRT) or a character generator as shown in Figures 6a and 6b. Underline 2 is available in this display mode.

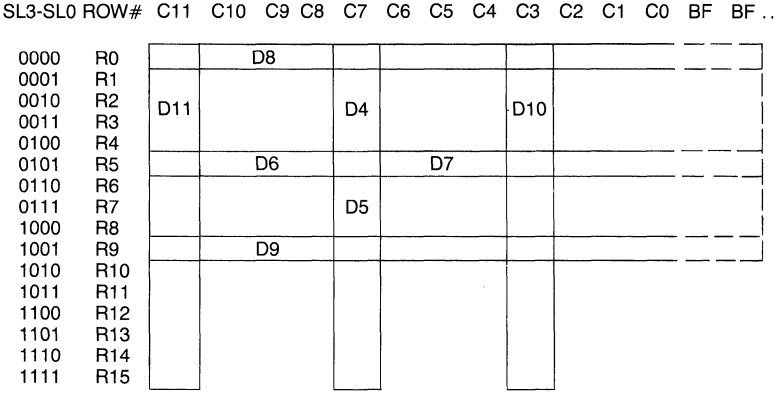
MS1,MS0 = 11–Character Mode with Underline 1.
Same operation as MS1, MS0 = 01 with the underline attribute byte appearing on the scan line(s) mask programmed. Underline 2 is available in this display mode.

TABLE 5: WIDE GRAPHICS MODE



H0, H1, H2, H3, W0, W1, are mask programmable.
The values shown are for the CRT 9041-004.

TABLE 6: THIN GRAPHICS MODE



	VERTICAL HEIGHT	HORIZONTAL POSITION
D4	R0-R5	PROGRAMMABLE
D5	R6-R15	PROGRAMMABLE
D10	R0-R15*	PROGRAMMABLE
D11	R0-R15*	PROGRAMMABLE

	HORIZONTAL LENGTH	VERTICAL POSITION
D6	C11-C7	PROGRAMMABLE
D7	C7-BF	PROGRAMMABLE
D8	C11-BF*	PROGRAMMABLE
D9	C11-BF*	PROGRAMMABLE

The height of D4 and D5, the length of D6 AND D7, and the position of D4-D11 are mask programmable. The values shown are for the CRT 9041-004.
*These values are fixed

DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. Figure 5 illustrates timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the cursor signal as required by the CRT 9041 with no additional hardware. It should be noted that the XCURSOR input will not affect the double width logic on the CRT 9041 in any way.

SCAN LINE INPUT MODES

Scan line information can be introduced into the CRT 9041 in parallel format or serial. Table 7 illustrates the pin definition as a function of the scan line input mode. The CRT 9041 will automatically recognize the scan line mode by observing the activity on pin 22. In parallel mode, this input will be active low for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 22 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next frame. The parallel scan line input mode will be selected for the next frame if the following two conditions occur during the VSYNC low time. First, at least one positive transition must occur on pin 22 and second, pin 22 must be low for seven or more $\overline{LD}$/SH periods. Refer to Figure 4 for timing details. Whenever the CRT 9041 detects a change of scan line modes (from parallel to serial or visa versa), the internal blink counter will be initialized to a known count value. This allows the user to achieve phase synchronization of the blink rates from two or more CRT 9041's. This is useful if one multiplexes alternate dots from two CRT 9041's to double the allowable video dot rate.

TABLE 7: PIN DEFINITION FOR PARALLEL

Scan Line Input Mode	CRT 9041 Pins			
	23	22	21	19
Serial	SLD	SLG	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

DOT STRETCH

Dot stretch is a mechanism whereby a single illuminated dot will never stand alone in the video stream. This eliminates the intensity variation otherwise found between single and multiple dots by raising the intensity level of single dots up to the level of consecutively displayed dots. To accomplish this, each illuminated dot (represented by a logic "1") will be extended into the next dot position. The following example illustrates the dot stretch mechanism.

Input bit pattern (D11-D0)	100101100100
Output bit pattern	110111110110

For reverse video, logic "0"'s are stretched (logic "1" represents the background of the reverse video character). The following example illustrates the mechanism in reverse video.

Input bit pattern (D11-D0)	010011001000
Reverse video pattern	101100110111
Output bit pattern	100100010011

In all cases, the next load of the shift register will always load the D11 bit to the output regardless of the value of the video output prior to the load. This dot stretch mechanism can be enabled on a character by character basis (or scan line by scan line) and is controlled by the DST input which is updated each $\overline{LD}$/SH period. The dot stretch signal enters the CRT 9041 with the D11-D0 inputs. In all cases, backfill (BF) is not affected by the dot stretch input.

BACKFILL

Backfill is a mechanism that allows a character width of greater than 12 dots and provides dot information (usually blanks) for all dots beyond 12. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the end of the character by two methods which are mask programmable.

Method A– The backfill (BF) dots will be the same as the dot displayed in position C11.

Method B– The backfill (BF) dots will be the same as the dots displayed in position C0.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature in Range ..... 0° C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{cc} = +5V ±5%, unless otherwise noted)

DC CHARACTERISTICS

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	All inputs except VDC, $\overline{LD}$/SH
Low Level V_{IL}			0.65	V	For VDC, $\overline{LD}$/SH input
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, $\overline{LD}$/SH input
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OH} = 0.4 mA
High Level V_{OH}	2.4			V	I_{OH} = 100μA
INPUT LEAKAGE CURRENT					
Leakage I_{L1}			10	μA	$0 \leq V_{IN} < V_{cc}$; excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leq V_{IN} \leq V_{cc}$; for VDC, $\overline{LD}$/SH
INPUT CAPACITANCE					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		35		pf	$\overline{LD}$/SH
C_{IN3}		35		pf	VDC
POWER SUPPLY CURRENT					
I_{CC}		95		mA	

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VDC	1.0		33.0	MHZ	CRT9041A
$1/t_{CY1}$ VDC frequency	1.0		30.0	MHZ	CRT9041B
	1.0		28.5	MHZ	CRT9041C
t_{CKL} VDC low	10			ns	
t_{CKH} VDC high	10			ns	
t_{CKR} VDC rise time			10	ns	Measured from 10% to 90% points
t_{CKF} VDC fall time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	250			ns	CRT9041A (1)
	270			ns	CRT9041B (1)
	300			ns	CRT9041C (1)
t_{S1}	7			ns	
t_{H1}	0			ns	
INPUT SETUP AND HOLD					
t_{S2}	60			ns	CRT9041A } For inputs $\overline{SLG}$, SLD,
	80			ns	CRT9041B } $\overline{VSYNC}$
	110			ns	CRT9041C }
	35			ns	For all other inputs except VDC, $\overline{LD}$/SH, $\overline{SLG}$, SLD, $\overline{VSYNC}$
t_{H2}	10			ns	For inputs $\overline{SLG}$, SLD, $\overline{VSYNC}$
	0			ns	For all inputs except VDC, $\overline{LD}$/SH, $\overline{SLG}$, SLD, $\overline{VSYNC}$
MISCELLANEOUS TIMING					
t_{PD}			30	ns	CRT9041A
			33	ns	CRT9041B
			35	ns	CRT9041C
t_{DW}	t_{CY2}				

(1) When mask programmed for CRT 9021 compatibility TCY2 will be slower.

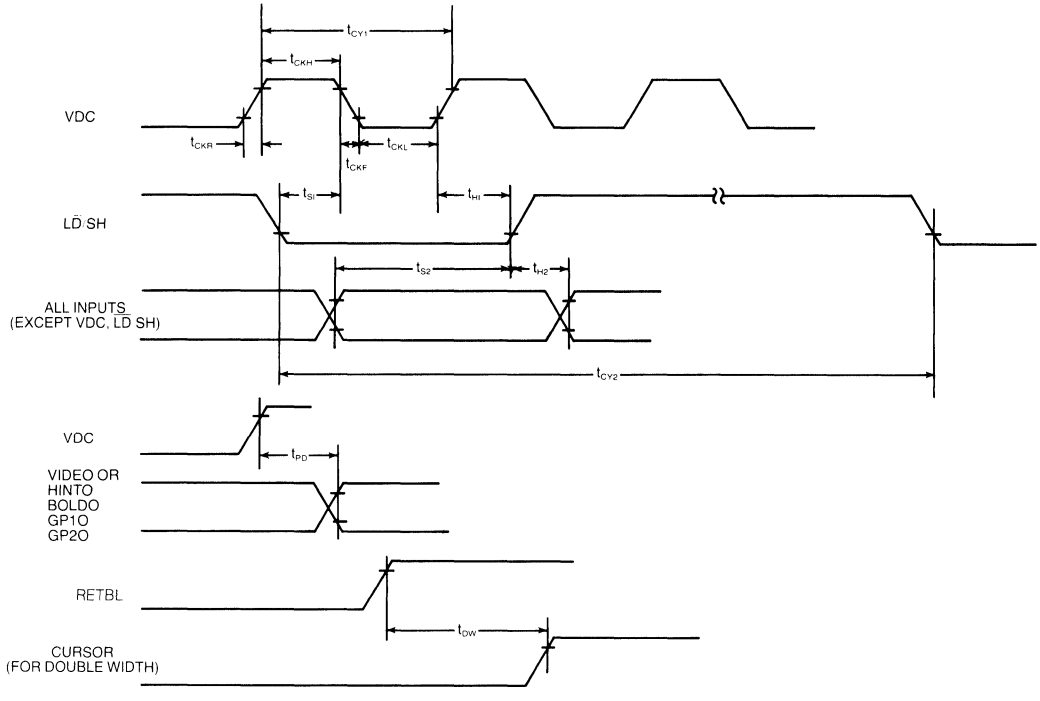


FIGURE 2: CRT 9041 INPUT/OUTPUT TIMING

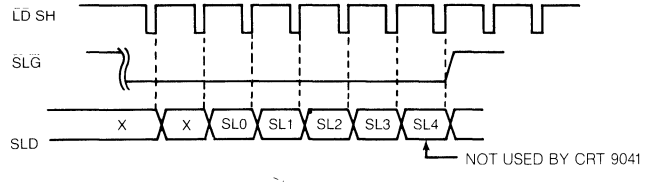


FIGURE 3: SERIAL SCAN LINE MODE TIMING

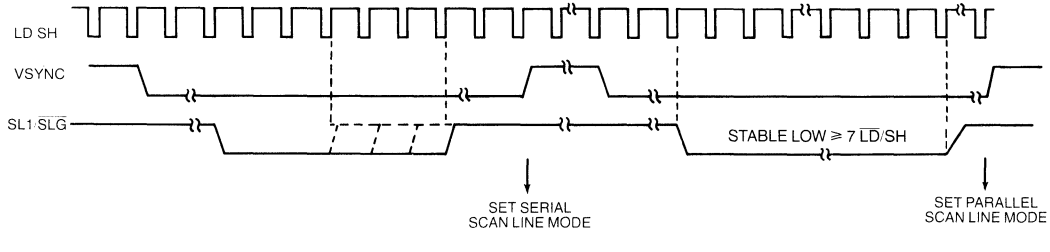
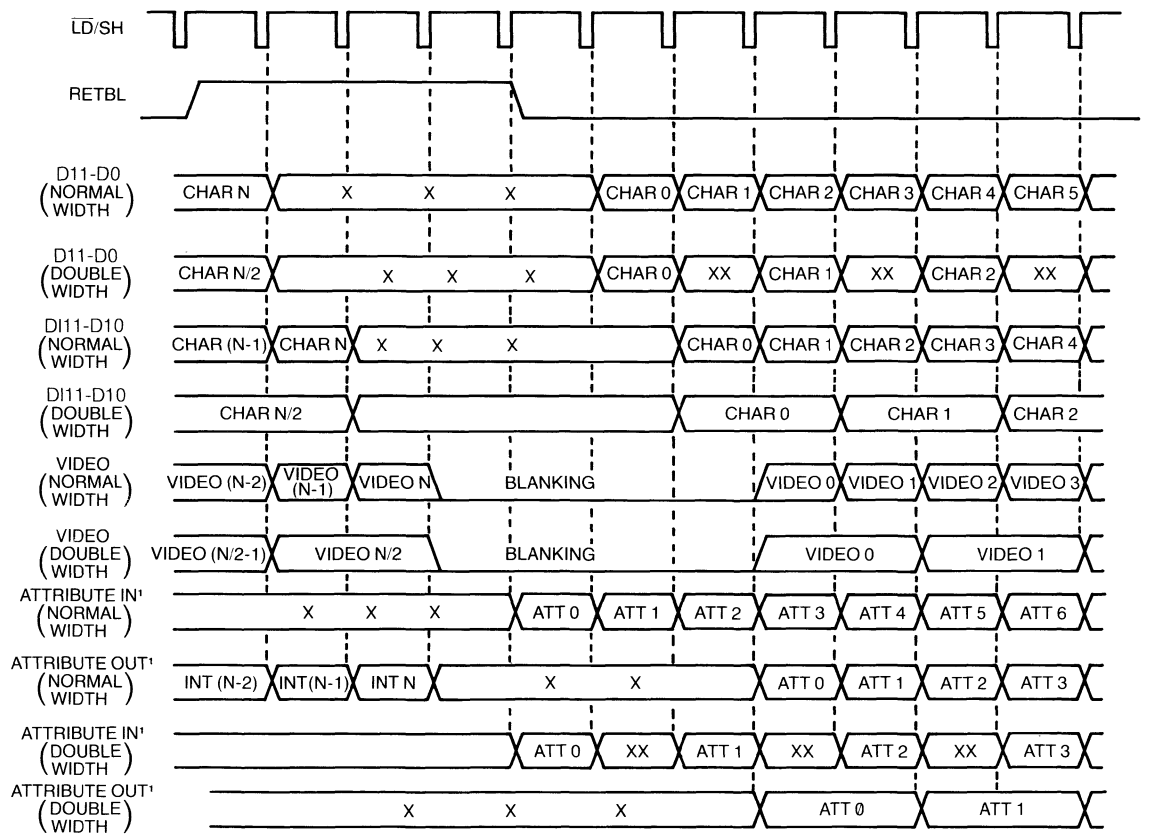


FIGURE 4: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING

SECTION V



1-Attributes include MS0, MS1, BLINK, CHABL, HINT, BOLD, REVID and XCURS

FIGURE 5: CRT 9041 FUNCTIONAL I/O TIMING

PROGRAM OPTIONS

The CRT 9041 has a variety of mask programmed options. Tables 8 and 9 illustrate the range of these options for the wide and thin graphics modes respectively. Table 10 illustrates the range of the miscellaneous other mask programmed options. In addition, Tables 8, 9 and 10 show the mask programmed options for the CRT 9041-004.

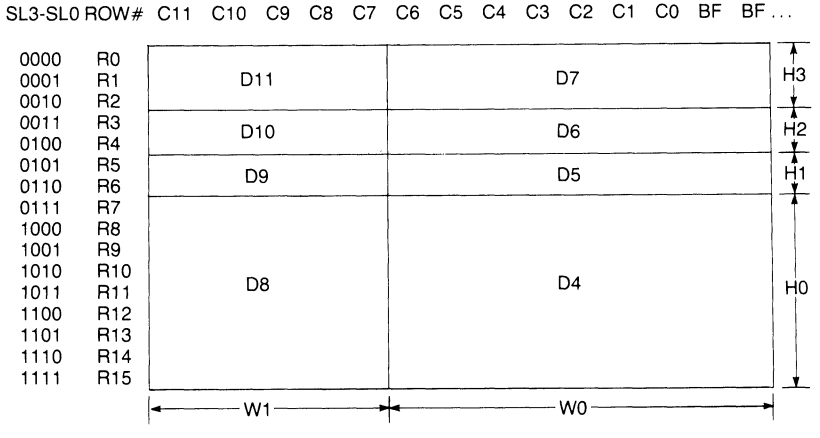
TABLE 8: WIDE GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	CRT 9041-004
Height of Graphic block*		
D11 AND D7	any scan line(s)	R0,R1,R2
D10 AND D6	any scan line(s)	R3,R4
D9 AND D5	any scan line(s)	R5,R6
D8 AND D4	any scan line(s)	R7 thru R15
Width of graphic block**	any consecutive dots	C11 thru C7
D11,D10,D9,D8	C11 thru C0	
D7,D6,D5,D4	all remaining dots not specified above	C6 thru C0 plus BF

*Any graphic block pair can be removed by programming for zero scan lines.

**Total number of dots for both must be equal to the total dots per character with no overlap. D11,D10,D9 and D8 must always be to the left of D7-D4.

WIDE GRAPHICS



H0, H1, H2, H3, W0, W1, are mask programmable.
The values shown are for the CRT 9041-004.

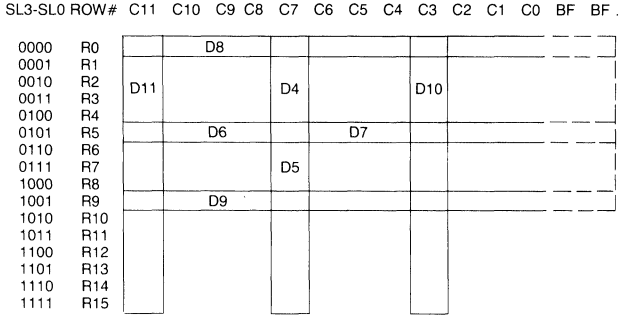
SECTION V

TABLE 9: THIN GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9041-004
Backfill	any dot(s) within the programmed D7 range to the right of the programmed column(s) for D11.	C0
Horizontal position for		
D6 and D7	any scan line(s) R0-R15	R5
D8	any scan line(s) R0-R15	R0
D9	any scan line(s) R0-R15	R9
Horizontal length for		
D6 (1)	any consecutive dots	C11 thru C7
D7 (1)	all dots not covered by D6 with one dot overlapping.	C7 thru BF
Blanked dots for serrated horizontal lines		
D6	any dot(s), BF programmed	none
D7	any dot(s), BF programmed	none
D8, D9	any dot(s), BF programmed	none
Vertical position for:		
D4 and D5	any dot(s) C11-C0,BF	C7
D10 (2)	any dot(s) C10-C0,BF	C3
D11 (2)	any dot(s) C11-C0	C11
Vertical length for:		
D4	any scan line(s)	R0 thru R5
D5	any scan lines not in D4	R6 thru R15
D10	no choice; always R0 thru R15	R0 thru R15
D11	no choice; always R0 thru R15	R0 thru R15

(1) D6 and D7 must always overlap by 1 dot. This overlap may be blanked by specifying the proper column(s) in the serration program line. D7 must always be to the right of D6.
(2) D11 must always come before D10 with no overlap: otherwise D10 is lost.

THIN GRAPHICS



	VERTICAL HEIGHT	HORIZONTAL POSITION
D4	R0-R5	PROGRAMMABLE
D5	R6-R15	PROGRAMMABLE
D10	R0-R15	PROGRAMMABLE
D11	R0-R15*	PROGRAMMABLE

	HORIZONTAL LENGTH	VERTICAL POSITION
D6	C11-C7	PROGRAMMABLE
D7	C7-BF	PROGRAMMABLE
D8	C11-BF*	PROGRAMMABLE
D9	C11-BF*	PROGRAMMABLE

The height of D4 and D5, the length of D6 AND D7, and the position of D4-D11 are mask programmable. The values shown are for the CRT 9041-004.
*These values are fixed

TABLE 10: MISCELLANEOUS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	"STANDARD" CRT 9041-004
Backfill in character mode	C11 or C0	C11
Character blink rate (division of VSYNC frequency)	7.5 Hz to 0.5 Hz (1) (1)	1.25Hz (1)
Cursor blink rate (2)	same as, half, or twice the character blink rate	2.50 Hz (1)
Character blink duty cycle	50/50 or 75/25	50/50
Cursor blink duty cycle	50/50 or 75/25	50/50
Character underline 1 position	any scan line(s) R0 thru R15	R8
Character underline 2 position	any scan line(s) R0 thru R15	R10
Cursor underline position	any scan line(s) R0 thru R15	R9
Extra cursor underline position	any scan line(s) R0 thru R15	R11
Cursor format (3)	underline blinking underline reverse video block blinking reverse video block	blinking reverse video block
Extra cursor format (3)	underline blinking underline reverse video block blinking reverse video block	blinking underline
Blink table	Table 1 Table 2 Table 3	Table 3
CURSOR or XCURSOR effect on BOLDO and HINTO	no effect or force to zero at cursor position	force to zero at cursor position.

(1) Assumes VSYNC input frequency of 60 HZ.
(2) Valid only if the cursor is formatted to blink.
(3) Valid for the parallel scan line mode only.

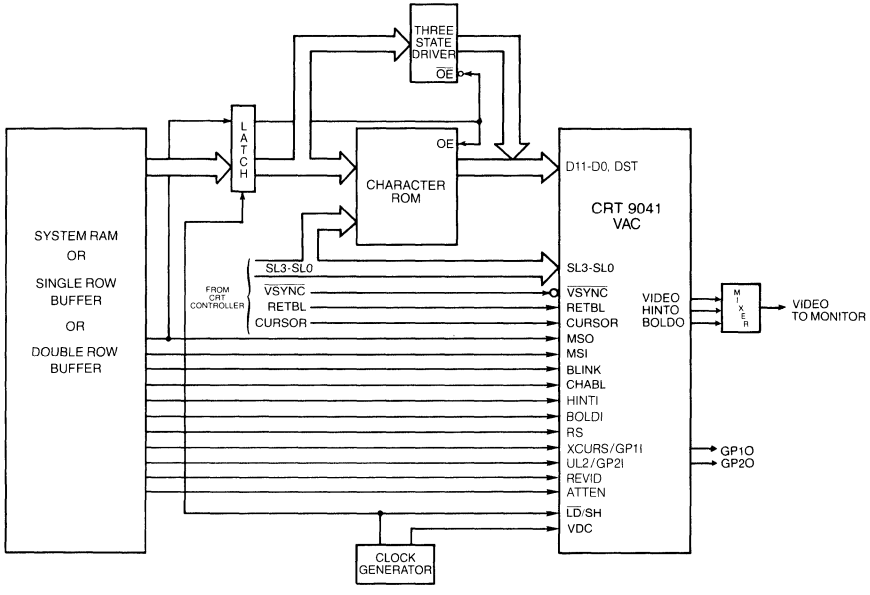


FIGURE 6a: CRT 9041 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE

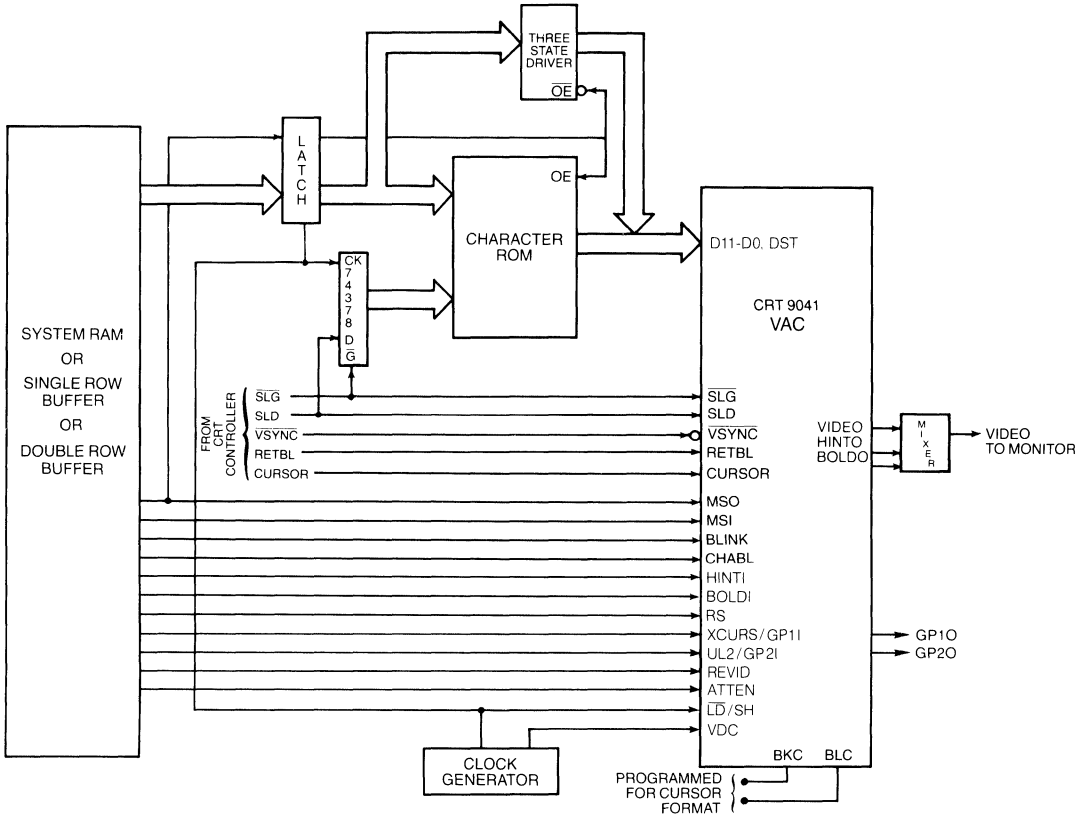


FIGURE 6b: CRT 9041 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE

STANDARD MICROSYSTEMS CORPORATION

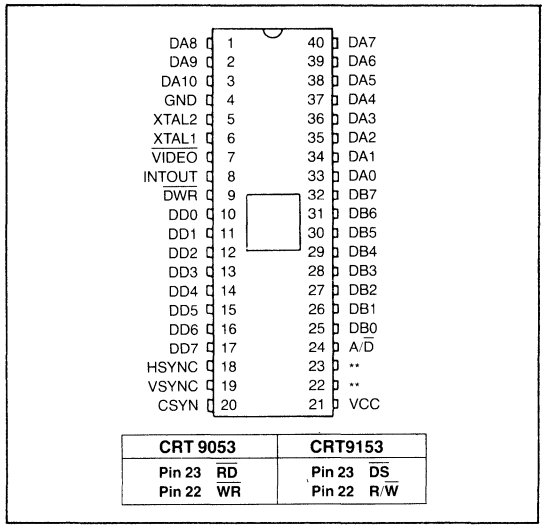
CRT 9053
CRT 9153

EVTLC
Enhanced Video Terminal Logic Controller

FEATURES

- ☐ Built-in High Frequency (4-18.7 MHz) Oscillator
- ☐ Built-in Video Shift Register
- ☐ Built-in Character Generator (128 Characters, 7x11 Dot Font)
- ☐ Bi-Directional Smooth Scroll Capability
- ☐ Visual Attributes Include Reverse Video, Intensity Control, Underline, and Character Blank and Blink
- ☐ Separate HSYNC, VSYNC and VIDEO Outputs
- ☐ Composite Sync (RS170 Compatible) Output
- ☐ Absolute (RAM address) Cursor Addressing
- ☐ MASK Programmable Video Parameters:
  - Dots Per Character Block (8-9)
  - Raster Scans Per Data Row (11-13)
  - Characters Per Data Row (32, 48, 64, 80)
  - Data Rows Per Page (8, 10, 12, 16, 20, 24 or 25)
  - Horizontal Blanking (8-64 Characters)
  - Horizontal Sync Front Porch (0-7 Characters)
  - Horizontal Sync Duration (1-64 Characters)
  - Horizontal Sync Polarity
  - Two Values of Vertical Blanking
  - Two Values of Vertical Sync Front Porch (0-63 Scan Lines)
  - Two Values of Vertical Sync Duration (1-16 Scan Lines)
  - Vertical Sync Polarity
  - Internal 128 Character 7x11 Dot Font
  - Character/Cursor Underline Position
  - Character/Cursor Blink Rate
  - Scan Row and Column for Thin Graphics Entity Segments
  - Scan Rows and Columns for Wide Graphics Entity Elements
- ☐ Software Enabled Non-Scrolling 25th Data Row Available with 25 Data Row/Page Display
- ☐ Non-Interlace Display Format

PIN CONFIGURATION



CRT 9053	CRT9153
Pin 23 RD	Pin 23 DS
Pin 22 WR	Pin 22 R/W

- ☐ Embedded Attribute or Tag Bit Attribute Capability
- ☐ Separate Display Memory Bus Eliminates Contention Problems
- ☐ Fill (Erase) Screen Capability
- ☐ Standard 8-bit Data Bus Microprocessor Interface
- ☐ Wide Graphics with Six Independently Addressable Segments Per Character Space
- ☐ Thin Graphics with Four Independently Addressable Segments Per Character Space
- ☐ Single + 5V Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ TTL Compatible

GENERAL DESCRIPTION

The CRT 9053 EVTLC and CRT 9153 EVTLC are mask programmable 40-pin COPLAMOS® n-channel MOS/LSI Video Display Controller Chips that combine video timing, video attributes, alphanumeric and graphics generation, smooth scroll and screen buffer interface functions.

The EVTLC incorporates many of the features (previously requiring a number of external components) required in building a low cost yet versatile display interface. An internal mask programmable 128 character font provides for a full ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

Two pinout configurations enhance the versatility of the EVTLC. The CRT 9053 controls data flow over the processor system data bus through separate read ($\overline{RD}$) and write ($\overline{WR}$) strobes for use with the 8085, 8051, Z80®, 8086, and similar microprocessors or microcomputers. The CRT 9153 regulates the data flow with a data strobe ($\overline{DS}$) and read/write (R/$\overline{W}$) enable signals for use with the 6500, Z8™, 68000 and similar microprocessors or microcomputers.

The EVTLC provides two independent data buses; one bus that interfaces to the processor and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the EVTLC eliminating contention problems and the need for a separate row buffer.

The EVTLC has an internal crystal oscillator requiring only an external crystal to operate. Masked constants for critical video timing simplify programming, operation and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

*Z80 is a registered trademark of Zilog Corporation.
Z8 is a trademark of Zilog Corporation.

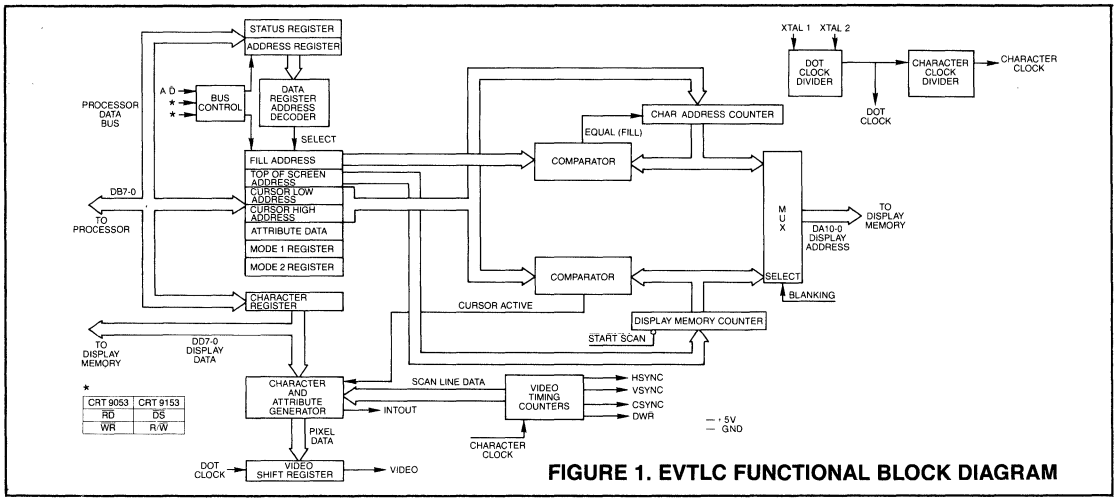


FIGURE 1. EVTLC FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	NAME	DESCRIPTION
3-1, 40-33	DA10-0	O	Display Address	11 bit address bus to display memory
4	GND		Ground	Ground Connection
5,6	XTAL2,1	I	Crystal 2,1	External Crystal An external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating).
7	$\overline{\text{VIDEO}}$	O	$\overline{\text{Video Output}}$	This output is a digital TTL waveform used to develop the VIDEO and composite VIDEO signals to the monitor. The polarity of this signal is: HIGH = BLACK LOW = WHITE
8	INTOUT	O	Intensity Output	This pin is the intensity level modification attribute bit (synchronized with the video data output).
9	$\overline{\text{DWR}}$	O	$\overline{\text{Display Write}}$	Write strobe to display memory
17-10	DD7-0	I/O	Display Data	8-bit bidirectional data bus to display memory
18	HSYNC	O	Horizontal Sync	Horizontal sync signal to monitor
19	VSYNC	O	Vertical Sync	Vertical sync signal to monitor
20	CSYNC	O	Composite Sync	This output is used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor.
21	V_{cc}		Power	5.0 V power connection
			CRT 9053	
22	$\overline{\text{WR}}$	I	$\overline{\text{Write Strobe}}$	Causes data on the microprocessor data bus to be strobed into the EVTLC
23	$\overline{\text{RD}}$	I	$\overline{\text{Read Strobe}}$	Causes data from the EVTLC to be strobed onto the microprocessor data bus
			CRT9153	
22	R/$\overline{\text{W}}$	I	Read/$\overline{\text{Write}}$ Select	Determines whether the processor is reading data from or writing data into the EVTLC (high for read, low for write)
23	$\overline{\text{DS}}$	I	$\overline{\text{Data Strobe}}$	Causes data to be strobed into or out of the EVTLC from the microprocessor data bus depending on the state of the R/W signal
24	A/$\overline{\text{D}}$	I	Register Select	The state of this input pin will determine whether the data is being read from, or written to, the address or status register, or a data register.
32-25	DB7-0	I/O	Processor Data Bus	8-bit bi-directional processor data bus

THE EVTLC INTERNAL REGISTERS

CRT 9053

Addressing of the internal EVTLC data registers of the CRT 9053 is accomplished through the use of the A/$\overline{D}$ select input qualified by the $\overline{RD}$ and $\overline{WR}$ strobes.

A/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	REGISTER OPERATION
0	1	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	1	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

CRT9153

Addressing of the internal EVTLC data registers of the CRT 9153 is accomplished through use of the A/$\overline{D}$ and R/$\overline{W}$ select inputs qualified by the $\overline{DS}$ strobe.

A/$\overline{D}$	$\overline{DS}$	R/$\overline{W}$	REGISTER OPERATION
0	0	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	0	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

The contents of the eight processor programmable registers located in the upper left hand side of the Functional Block Diagram of figure 1 indicate the memory locations from which screen data is to be fetched and displayed as well as the selected modes of display operation. These registers are addressed indirectly via the Address Register.

To access one of the eight eight-bit registers, the processor must first load the Address Register with the three-bit address of the selected data register. The next read or write to a data register will then cause the data register pointed to by the Address Register to be accessed. The Line A/$\overline{D}$ controls whether writing is occurring to the Address Register or to a data register. When a read operation is performed, A/$\overline{D}$ controls access to either the Status Register or to the data register selected by the Address Register.

REGISTER DESCRIPTION

ADDRESS REGISTER

Writing a byte to the ADDRESS register will select the specified register for the next time the processor writes to or reads the EVTLC data registers. The data register addresses are as follows:

ADDRESS								TYPE	REGISTER
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
X	X	X	X	0	1	1	0	Write	CHIP RESET
X	X	X	X	1	0	0	0	Write	TOSADD
X	X	X	X	1	0	0	1	Write	CURLO
X	X	X	X	1	0	1	0	Write	CURHI
X	X	X	X	1	0	1	1	Write	FILADD
X	X	X	X	1	1	0	0	Write	ATTDAT
X	X	X	X	1	1	0	1	RD/WR	CHARACTER
X	X	X	X	1	1	1	0	Write	MODE1 REGISTER
X	X	X	X	1	1	1	1	Write	MODE2 REGISTER

(X = don't care) NOTE: Chip Reset is required before starting operation.

STATUS REGISTER

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register. This bit is used to synchronize data transfers between the processor and the EVTLC. The EVTLC will set the DONE bit to a logic one after completing a byte transfer command or a FILL operation. The DONE bit is set to a logic zero by reading from, or writing to, the CHARACTER register. The processor must wait until the DONE bit is 1 before attempting to change the CURSOR ADDRESS, in order to write a character to, or read a character from, the CHARACTER register.

STATUS REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DONE	X	X	X	X	X	X	X

DONE = 1 signifies that external processor is allowed to access CURSOR ADDRESS and/or CHARACTER registers.

DONE = 0 signifies that external processor must wait until EVTLC completes transfer of data between display memory and CHARACTER register.

DATA REGISTERS

FILADD (Fill Address) This register contains the RAM address of the character following the last address to be filled. Writing to this register will enable the EVTLC "fill" circuitry. The FILL operation will then be triggered by the next processor write to the CHARACTER register. The FILL operation will write the character in the CHARACTER register to every location in display memory starting with the address specified in the CURLO and CURHI registers through the location preceding the address specified in the FILADD register. The cursor position is not changed after a FILL operation. Note that the address bits DA3-DA0 are internally forced to 0 forcing the FILADD address to be 00, 16, 32, etc. to 1920. The CURLO and CURHI registers will not be changed by this operation. Writing to the CHARACTER register will cause the EVTLC to reset DB7 of the STATUS register to "0". Bit 7 will be set to 1 after the EVTLC has filled the last memory location specified.

FILADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DA10	DA9	DA8	DA7	DA6	DA5	DA4

TOSADD (Top of Screen Address) This register contains the RAM address of the first character displayed at the top of the video monitor screen. In addition, this register controls selection of either of two mask programmable vertical scan rates.

TOSADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TIM	DA10	DA9	DA8	DA7	DA6	DA5	DA4

Note that address bits DA3-DAO are internally forced to 0 forcing the first address at the beginning of each row to be 00, 16, 32, etc. to 1920.

The most significant bit of this register (TIM) is used to select between the two mask programmed sets of vertical retrace parameters (scan A and scan B). This allows software selection of, for example, 50/60 HZ.

TIM = 0 enable raster scan A (60 Hz)

TIM = 1 enable raster scan B (50 Hz)

CURLO (Cursor Low) This register contains the eight lower order address bits of the RAM cursor address. All FILL screen and character transfer operations begin at the memory location pointed to by this address.

CURLO REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

CURHI (Cursor High) This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8). All FILL screen and character transfer operations begin at the memory location pointed to by this address. In addition, this register contains the Smooth Scroll Offset Values SS3-SS0 which determine the number of scan lines that the data is shifted on the screen. The MSB of this register (SLE-status line enable) is the enable for the non-scrolling status line.

CURHI REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SLE	SS3	SS2	SS1	SS0	DA10	DA9	DA8

SLE = 1 enables non-scrolling 25th status line
SLE = Ø disables and blanks non-scrolling status line

SS3-SS0 Smooth Scroll Offset Value

ATTDAT (Screen Attribute Data) Two attribute modes are provided. In the "tag bit" attribute mode, the MSB of each character is used to "tag" those characters which are to be enhanced with the attribute specified by the ATTDAT register. This allows individual characters to be attributed, but with the limitation that only one attribute style may be enabled for a specific screen. This is compatible with the CRT9028/9128, and is specified as the 9x28 operation mode. In the "embedded attribute" mode, multiple attributes may be displayed on one screen. This is specified as the 9x53 operation mode. See "MODE 2" register for selection of 9x28 and 9x53 modes.

The ATTDAT register specifies the visual attributes of the video data, in 9x28 operation mode, and the cursor presentation. The visual attributes specified in the ATTDAT register (DB3-DB0) are enabled or disabled by a TAG bit that is appended to the ASCII character written to the CHARACTER register. Every character on the screen with its TAG bit set is displayed with the same attribute. Changing the Attribute register will change the attribute of every "tagged" character on the screen. Character attributes in the 9x53 mode are determined by specific attribute characters embedded in the character data stream as explained below in the section titled CHARACTER SETS. The functions of the remaining bits in the ATTDAT register are not affected by the display character's TAG bit. NOTE: All 8 bits are valid for the 9x28 mode. In the 9x53 mode the only bits that are recognized are DB6, 5 and 4.

ATTDAT REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

DB7 (1) MODE SELECT
- DB7 = 1 enables graphics mode display (No attributes allowed)
- DB7 = 0 enables alpha mode display

Note: See CHARACTER SETS for definition of characters available in each mode.

DB6 CURSOR SUPPRESS
- DB6 = 1 inhibits VIDEO display at cursor time by forcing the VIDEO output to background level during cursor display time
- DB6 = 0 enables VIDEO display at cursor time

Note: A blinking cursor display can be achieved by toggling this bit under processor control.

DB5 CURSOR DISPLAY
- DB5 = 1 enables underline cursor display
- DB5 = 0 enables block cursor display

Note: An underline cursor in an underline character attribute field will be dashed.

DB4 SCREEN
- DB4 = 1 for white screen and black characters
- DB4 = 0 for black screen and white characters

Note: This is a screen attribute (versus character attribute) bit and sets the default video background level.

ENABLED OR DISABLED BY TAG BIT (9x28 MODE ONLY)

DB3[1] CHARACTER SUPPRESS
- DB3 = 1 to enable Video suppress
- DB3 = 0 to inhibit Video suppress

Note: This bit allows character blinking and blanking under processor control

DB2[1] INTENSITY
- DB2 = 1 allows the INTOUT output pin to go high for the character time
- DB2 = 0 inhibits the INTOUT output pin from going high

DB1[1] UNDERLINE
- DB1 = 1 will cause the character to be underlined
- DB1 = 0 will inhibit the underline

DB0[1] REVERSE VIDEO
- DB0 = 1 will cause the standard foreground and background Video levels (selected with BIT 4) to be reversed for the character time
- DB0 = 0 will inhibit reverse video

[1] These bits not recognized in 9x53 mode and represent don't care states.

MODE 1 The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the EVTLC after every read/write of the CHARACTER register. Note: The visible cursor position is not affected.

MODE 1 REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AUTO INC	X	X	X	X	X	X	X

DB7 AUTO INCREMENT
- DB7 = 1 to enable automatic character address

The RAM address is incremented after the EVTLC completes a display memory access initiated by a processor to RAM or RAM to processor character transfer.

- DB7 = 0 to disable automatic increment.

MODE 2 This register contains two bits which control operational modes of the device. DB0 controls whether the device operates as a 9x53 or emulates the 9x28. In the 9x28 mode the device is fully compatible with the CRT 9028/9128 with the exception of the higher density character set. DB1 enables the cursor blink function where the blink rate is a mask programmable feature (see CRT 9053/9153 coding sheet.) This function is automatically disabled when in 9x28 mode.

MODE 2 REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	X	X	CUR BLINK ENBL	9x53

DB1 CURSOR BLINK
- DB1 = 1 will enable blinking cursor.
- DB1 = 0 will disable blinking cursor and state of cursor is controlled by DB6 in ATTDAT register.

DB0 9x53 ENABLE
- DB0 = 1 will enable operation as a 9053/9153.
- DB = 0 will enable operation as 9028/9128.

CHARACTER This register allows access to the display memory for both byte transfers and FILL operations. In BYTE Transfer Write Mode, the processor first writes a character to this register. The EVTLC takes that character and stores it in the display memory in the location specified by the CURLO and CURHI registers. In Byte Transfer Read Mode, the processor reads this register causing the EVTLC to fetch the character whose address is specified in the CURLO and CURHI registers from the display memory and place it in the CHARACTER register. The processor then reads the character and initiates another fetch from memory cycle. In FILL mode, writing a byte to this register will initiate a FILL operation. All EVTLC/memory data transfers take place during horizontal and vertical video retrace blank time.

CHARACTER REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
8 BIT CHARACTER[2]							

[2] See next section, CHARACTER SETS, for definition of 8 bit characters.

CHARACTER SETS

The character set consists of 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity. Included in the 128 mask programmable characters can be the 96 standard ASCII characters and 32 special characters.

9x28 OPERATION MODE (MODE 2: DB0 = 0)

A. GRAPHICS MODE – (ATTDAT: DB7 = 1)

This mode allows an intermix of alphanumeric and graphics characters. No attributes are permitted in this mode. If DB7 = 1, the character will be alphanumeric. If DB7 = 0, the character will be a graphics character. DB7 is "tag bit".

ENTITY	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CHARACTER	1	← CHARACTER DATA →						
THIN[1] GRAPHICS	0	0	X	X	SEG4	SEG3	SEG2	SEG1
WIDE[1] GRAPHICS	0	1	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

B. ALPHANUMERICS MODE – (ATTDAT: DB7 = 0)

This mode allows display of alphanumeric characters with attributes. If DB7 is set to a logical one, the attribute(s) specified in the ATTDAT register will be enabled for that character. If DB7 is cleared, attributes will not be enabled for that character. DB7 is "tag bit".

ENTITY	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CHARACTER (Attr enabled)	1	← CHARACTER DATA →						
CHARACTER (No attribute)	0	← CHARACTER DATA →						

9x53 OPERATION MODE (MODE 2: DB0 = 1)

This mode allows the use of embedded field attributes where the desired attribute for any given string of one or more consecutive characters is defined by an attribute character which is part of the character data stream and is located immediately in front of the characters to be attributed. A second attribute character should be located immediately following the string of attributed characters to restore the normal display mode. Since the specific attribute characters occupy character positions, they are actually displayed as spaces.

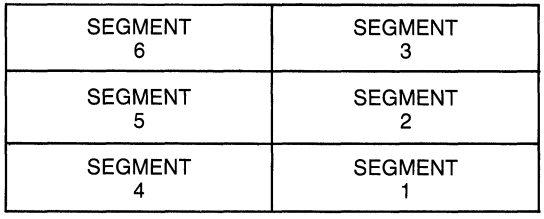
ENTITY	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CHARACTER	0	← CHARACTER DATA →						
ATTRIBUTE[2] CHARACTER	1	0	0	BLANK	BLINK	INT	UNDLN	RV
THIN[1] GRAPHICS	1	0	1	X	SEG4	SEG3	SEG2	SEG1
WIDE[1] GRAPHICS	1	1	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

[1] Graphics segments are turned on when bit is set to a "1".

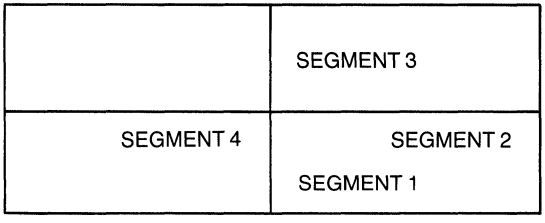
[2] A specific field attribute is enabled by setting the appropriate bit and disabled by resetting the bit. Attributes can be mixed. The following defines the available attributes indicated in the ATTRIBUTE CHARACTER.

DB4 (BLANK)–Suppresses character video output.
DB3 (BLINK)–Causes character to blink at mask programmed rate.
DB2 (INTENSITY)–Controls INTOUT output pin.
DB1 (UNDERLINE)–Causes character to be underlined.
DB0 (REVERSE VIDEO)–Reverses foreground/background video levels.

GRAPHICS CHARACTERS[3]



WIDE GRAPHICS ENTITY



THIN GRAPHICS ENTITY

[3] Scan line and column of segment locations are mask programmable.

DESCRIPTION OF SYSTEM OPERATION

The EVTLC circuitry provides two control functions. One function interprets and controls data from the system processor interface through the data bus DB7-DB0 as shown in the Processor Timing of figure 3. The other function generates and refreshes the video image on the screen through the DD7-DD0 data bus as shown in the Display Memory Timing of figure 2. Because the system data bus is isolated from the display data bus, the EVTLC maintains complete control over access to display memory. All data flow between display RAM and the processor or the EVTLC takes place through the EVTLC. Refer to the EVTLC Display Memory Access Timing of figure 7.

DISPLAY MEMORY ACCESS

Processor/display memory access is accomplished through the CHARACTER register of the EVTLC. All processor transfers to or from the CHARACTER register take place only when the DONE bit is high. The DONE bit is used to synchronize data transfers between the EVTLC and the processor as shown in the Typical Processor To Display Memory Transfer of figure 6. When the processor needs to store a byte of data in the display memory, it will write the byte to the CHARACTER register of the EVTLC. The EVTLC will immediately reset the DONE bit indicating that the transfer hardware is busy. At the next blanked Video time, the EVTLC will store the byte in the display memory, increment the character address, (if auto increment is enabled) and set the DONE bit. When the processor needs to read a byte of data from the display memory, it will read the CHARACTER register. The EVTLC will fetch the desired byte from the display memory during the next blanked VIDEO time, increment the character address (if enabled), and set the DONE bit. When the processor detects that the DONE bit is set, it will read the CHARACTER register to get the data byte from the EVTLC. This read will reset the DONE bit and

cause the EVTLC to fetch the next byte of data from the memory.

If auto increment is not enabled, the processor must set the cursor address in the CURLO and CURHI register to the address of the memory location being read from, or written into, before every access to the CHARACTER register.

It should be noted that Auto Increment does not affect the visible cursor location. If auto-increment is enabled, the current character location will equal the cursor position only for the first character transfered following an update of the CURLO and CURHI registers. Note that the DONE bit must be high before attempting to update the cursor registers because the loading of the cursor registers will reset the character position counters to the cursor position.

SMOOTH SCROLL

The EVTLC may be programmed to do either "jump" or "smooth" scrolling. Jump scrolling moves the data up or down the monitor screen one data row at a time. Smooth scrolling moves the data up the monitor screen one scan line at a time. The number of scan lines and the rate they move up the screen is under processor control.

Smooth scroll is controlled through manipulation of the SS3-SS0 bits of the CURHI register. These bits represent the binary address of the first scan line of the first data row displayed on the monitor screen (the data row whose beginning address is in the TOSADD register). When the value represented by these bits is incremented, the video data on the monitor screen moves up by the same number of scan lines. After the address of the last scan line of the data row is loaded into the CURHI register and the VIDEO data has moved up the last scan line of the data row, the processor resets the SS3-SS0 address to point to scan line 0 and does a jump scroll. Jump scroll is accomplished by incrementing the RAM address in the TOSADD register by a data row length (so that it points to the address of the first character of the new top data row on the monitor).

When programmed for a data row of 80 characters/data row display (1920 data words), for example, the display RAM contains 25 actual rows of data (2000 RAM locations). If the smooth scroll offset equals zero, the EVTLC will display the 1919 RAM locations following the top of screen address when displaying data. The first data row is partially scrolled off the screen and the 25th data row is scrolled onto the screen when the smooth scroll offset is incremented. The EVTLC will now display the 1999 RAM locations following the top of screen address (wrapping to 0 after address 1999). After the EVTLC does a jump scroll, the processor will program it to erase the line just scrolled off the screen (preparing it to be scrolled onto the screen). This line now becomes the non-displayed 25th data row.

NON-SCROLLING STATUS LINE

The non-scrolling status line is only functional on a EVTLC that has been programmed for 25 data rows. This data row will remain stationary at the bottom of the screen and will not move up the screen when the remainder of the display data is scrolled. Otherwise, VIDEO data on the status line may be manipulated as though it were normal display data. The smooth scroll offset will not function properly when the status line is enabled. The memory address of the characters on the status line are always characters 1920–1999.
NOTE: If the part is programmed for 25 data rows an additional mask option must be specified which makes the 25th data row either fixed (always displayed) or a status row (enabled/disabled by the SLE bit).

CHIP RESET

The CRT 9053 and CRT 9153 Chip Reset requires two steps. The system processor first writes the reset address to the address register of the EVTLC. The system processor then writes a dummy character to the EVTLC Data register. Writing to the Data register resets the chip. See the DONE timing in figure 6. This reset process causes the MODE 2 register to be set to the "00" state which disables the blinking cursor and enables the 9x28 operation mode.

ROM CHARACTER BLOCK FORMAT

COLUMN DOT ->	C8	C7	C6	C5	C4	C3	C2	C1	C0
SCAN LINE 0 ->	0	0	0	0	0	0	0	0	0
SCAN LINE 1 ->	0								0
SCAN LINE 2 ->	0								0
SCAN LINE 3 ->	0								0
SCAN LINE 4 ->	0								0
SCAN LINE 5 ->	0								0
SCAN LINE 6 ->	0			MASK PROGRAMMABLE CHARACTER BLOCK (FONT) 7 X 11					0
SCAN LINE 7 ->	0								0
SCAN LINE 8 ->	0								0
SCAN LINE 9 ->	0								0
SCAN LINE 10 ->	0								0
SCAN LINE 11 ->	0								0
SCAN LINE 12 ->	0	0	0	0	0	0	0	0	0

Dots/Character: 8 dots/character cell => C8 - C1 displayed
9 dots/character cell => C8 - C0 displayed

Column dot C0 will be the same as column dot C8 when more than 8 dots/character cell are specified when generating alpha-numerics.

NOTE: The maximum dot clock crystal frequency is dependent on the dots/character programmed:

DOTS/CHARACTER	MAX XTAL FREQ
8 dots	16.62 MHz max*
9 dots	18.7 MHz max*

*These values are preliminary

Scan Lines per Character:
11 scan lines/character => SL0-SL10 displayed
12 scan lines/character => SL0-SL11 displayed
13 scan lines/character => SL0-SL12 displayed

Thin and Wide Graphics: Dots mask programmed for vertical column C1 will be the same as backfill Columns 0 when generating wide and thin graphics.

Mask programmable options–The ROM character block format above shows the 7X11 mask programmable character font within the character cell as defined by dots C8 through C0 and scan lines 0 through 12.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

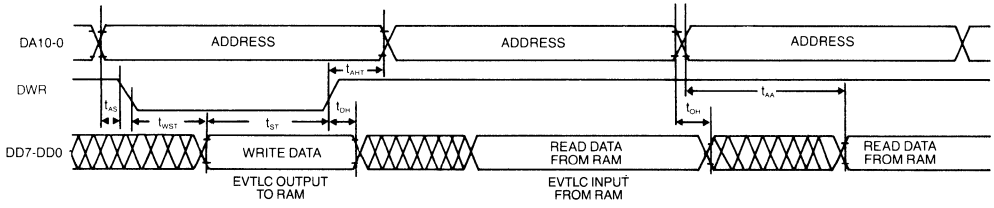
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($TA = 0°C$ to 70°C, $V_{cc} = +5V \pm 5\%$, unless otherwise noted.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, Vil			0.8	V	
High-Level, Vih	2.2			V	
OUTPUT VOLTAGE LEVELS					
Low-level, Vol			0.4	V	All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, $\overline{VSYNC}$; Iol = 1.6 mA
Low-level, Vol			0.4	V	$\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 0.4 mA
High-level, Voh	2.4			V	All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −40μa
High-level, Voh	2.4			V	$\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −20μA
INPUT LEAKAGE CURRENT					
High-level, Ilh			10	μA	All inputs; Vin = Vcc
Low-level, Iil			−10	μA	All inputs except $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V
Low-level, Iil			−200	μA	$\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V
INPUT CAPACITANCE					
All inputs, Cin			15	pF	
OUTPUT LOAD					
C_L			15	pF	Except DB7-0
C_L			100	pF	DB7-0
POWER SUPPLY CURRENT					
Icc		125		mA	
AC CHARACTERISTICS					
CLOCK FREQUENCY, fin	1.0		18.7	MHz	
DISPLAY MEMORY TIMING					
Address Set-up Time t_{AS}	20			ns	
Write Strobe Set-up Time t_{WST}	100			ns	
Data Set-up Time t_{ST}	80			ns	
Data Hold Time t_{DH}	10		50	ns	

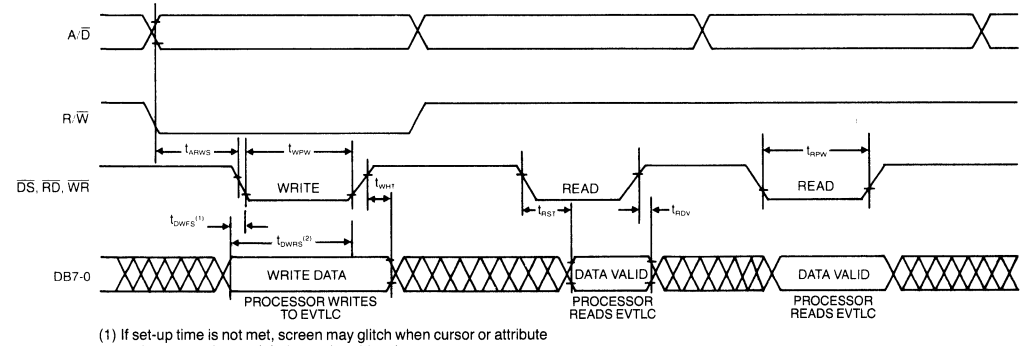
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Address Hold Time t_{AHT}	50			ns	
Output Hold From Address Change t_{OH}	15			ns	
Address Access Time t_{AA}			250	ns	
PROCESSOR TIMING					
Address Read/Write Set-up t_{ARWS}	160			ns	
Write Pulse Width t_{WPW}	160			ns	
Write Hold Time t_{WHT}	15			ns	
Read Set-up Time t_{RST}			200	ns	
Read Data Valid T_{RDV}	0			ns	
Read Pulse Width t_{RPW}	250			ns	
Data Write Falling Set-up t_{DWFS}	120			ns	
Data Write Rising Set-up t_{DWRS}	160			ns	

Crystal specification (Applies for 4-18.7 MHz):
- Series Resonant
- 50 ohms max series resistance
- 1.5 pf typ parallel capacitance
- Operation below 4 MHz requires external crystal oscillator



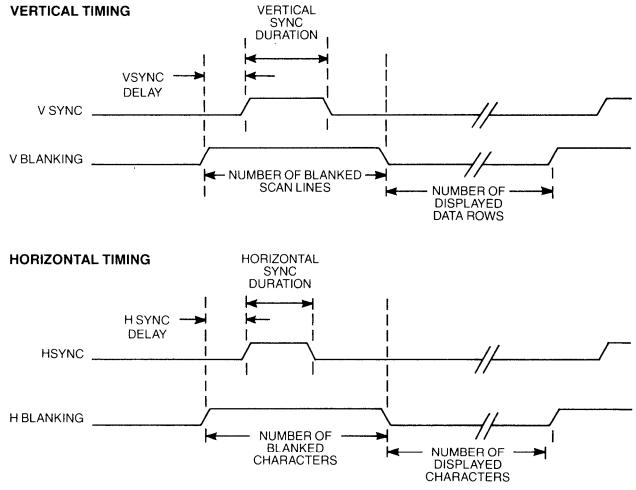
NOTE: DISPLAY ADDRESS BUS DA10-DA0 MUST NOT CHANGE WHILE $\overline{DWR}$ IS LOW

FIGURE 2. DISPLAY MEMORY TIMING



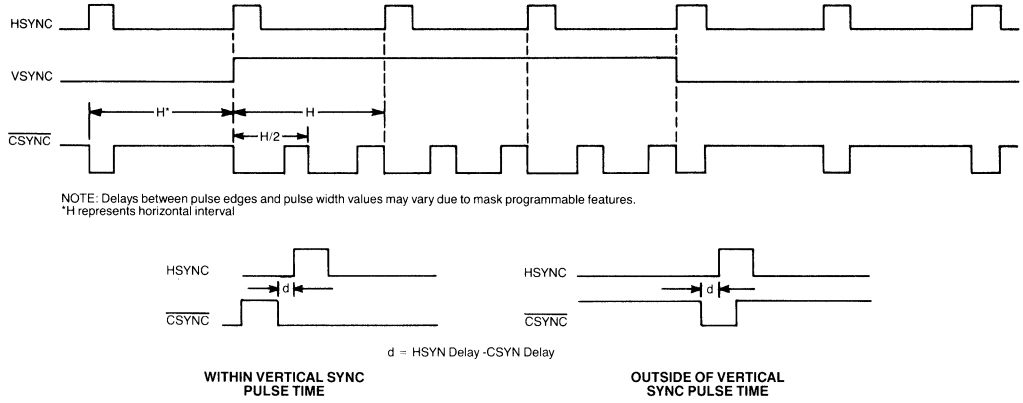
(1) If set-up time is not met, screen may glitch when cursor or attribute registers are changed during active video time.
(2) Minimum set-up time to ensure valid data into EVTLC internal registers.

FIGURE 3. PROCESSOR TIMING



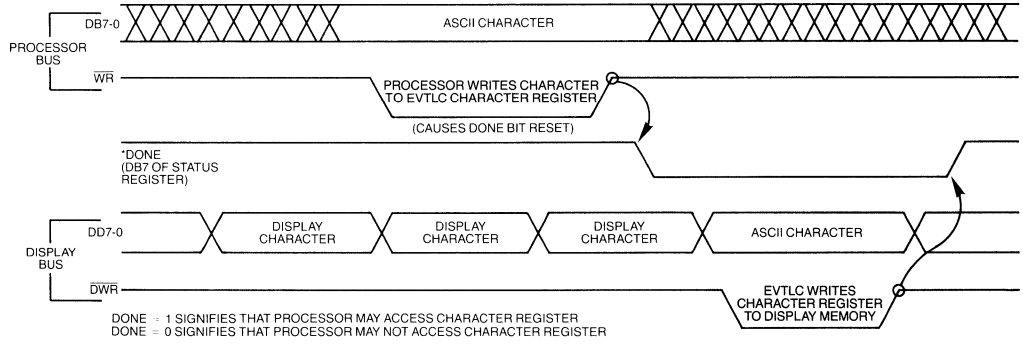
NOTE. Video parameters above are mask programmable

FIGURE 4. VERTICAL AND HORIZONTAL SYNC TIMING



NOTE: Delays between pulse edges and pulse width values may vary due to mask programmable features.
*H represents horizontal interval

FIGURE 5. VIDEO SIGNAL TIMING



DONE = 1 SIGNIFIES THAT PROCESSOR MAY ACCESS CHARACTER REGISTER
DONE = 0 SIGNIFIES THAT PROCESSOR MAY NOT ACCESS CHARACTER REGISTER

FIGURE 6. TYPICAL PROCESSOR TO DISPLAY MEMORY TRANSFER

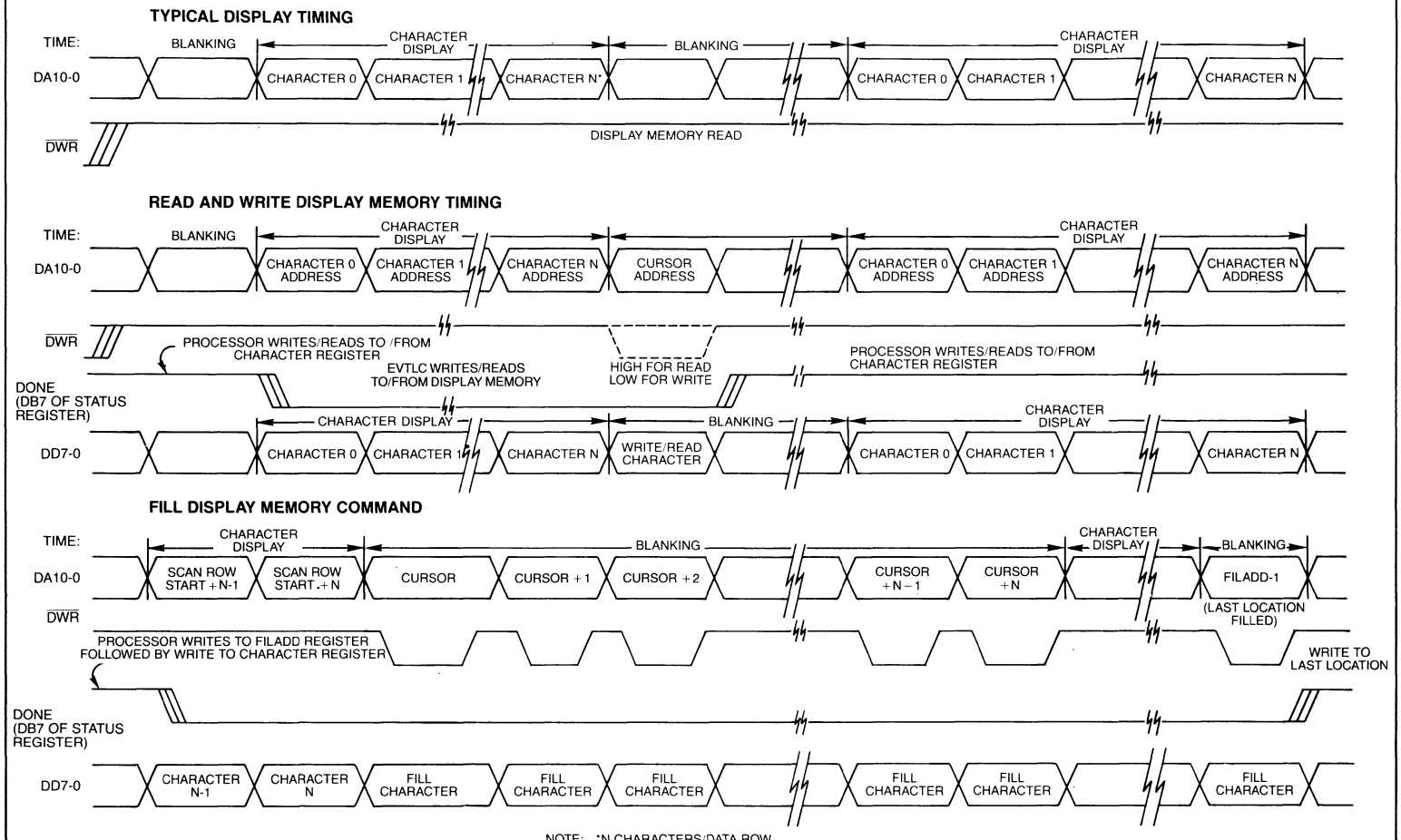


FIGURE 7. EVTLC DISPLAY MEMORY ACCESS TIMING

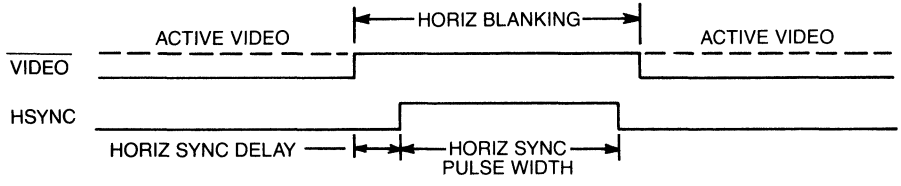
I. ROM CHARACTER BLOCK FORMAT:

COLUMN DOT	–>	C8	C7	C6	C5	C4	C3	C2	C1	C0
SCAN LINE 0	–>	0	0	0	0	0	0	0	0	0
SCAN LINE 1	–>	0								0
SCAN LINE 2	–>	0								0
SCAN LINE 3	–>	0								0
SCAN LINE 4	–>	0								0
SCAN LINE 5	–>	0								0
SCAN LINE 6	–>	0	CHARACTER BLOCK 7X11 CELL							0
SCAN LINE 7	–>	0								0
SCAN LINE 8	–>	0								0
SCAN LINE 9	–>	0								0
SCAN LINE 10	–>	0								0
SCAN LINE 11	–>	0								0

DOTS PER CHARACTER: 9
DOT CLOCK XTAL FREQUENCY (MHz): 17.1072

II. HORIZONTAL TIMING (IN CHARACTER TIMES):

CHARACTERS PER DATA ROW: 80
HORIZONTAL BLANKING: 19
HORIZONTAL SYNC DELAY: 4
HORIZONTAL SYNC PULSE WIDTH: 8
HORIZONTAL SYNC POLARITY: NEGATIVE ACTIVE

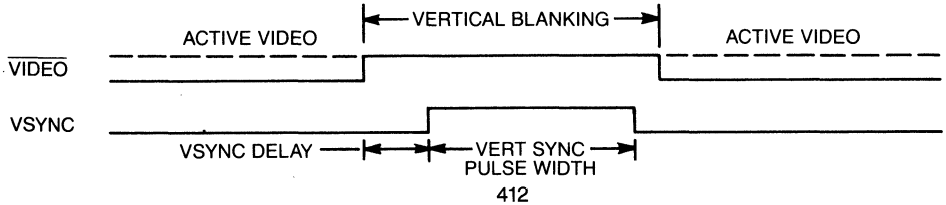


III. VERTICAL TIMING:

CHARACTER ROWS: 25
SCAN LINES PER CHARACTER: x 12
TOTAL VISIBLE SCAN LINES: 300
VERTICAL SYNC POLARITY: NEGATIVE ACTIVE

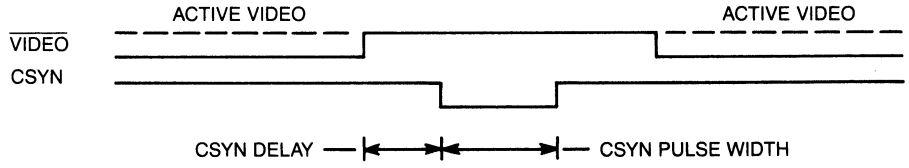
IV. VERTICAL SYNC TIMING (IN SCAN LINES):

60 Hz VERTICAL BLANKING: 20
60 Hz VERTICAL SYNC DELAY: 4
60 Hz VERTICAL SYNC PULSE WIDTH: 8
ALTERNATE (50 Hz) VERTICAL BLANKING: 84
ALTERNATE (50 Hz) VERTICAL SYNC DELAY: 17
ALTERNATE (50 Hz) VERTICAL SYNC PULSE WIDTH: 34



V. COMPOSITE SYNC OUTPUT (IN CHARACTER TIMES)

COMPOSITE SYNC DELAY: 2
COMPOSITE SYNC PULSE WIDTH: 8



VI. BLINK RATES (@ 60 Hz VSYNC):

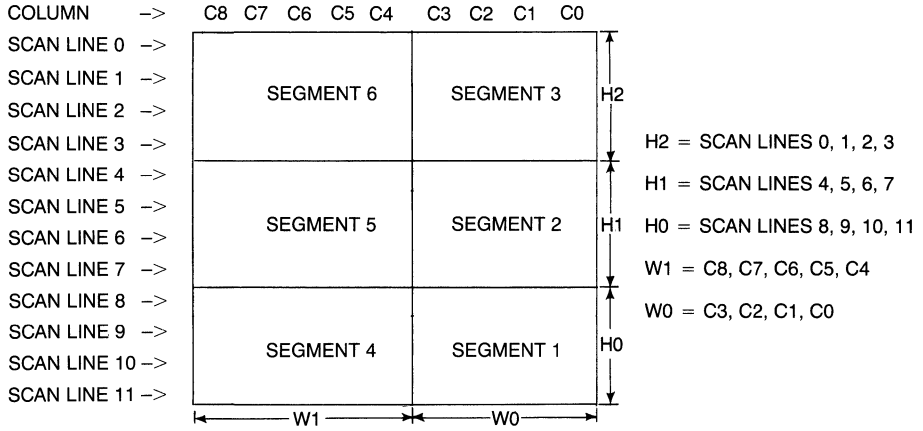
CHARACTER—
BLINK RATE: 1.25 Hz
DUTY CYCLE: 75/25

CURSOR—
BLINK RATE: 2.5 Hz
DUTY CYCLE: 50/50

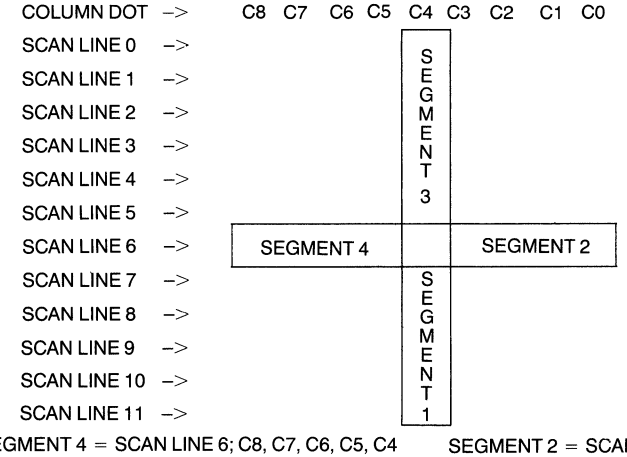
VII. UNDERLINE ATTRIBUTE:

CHARACTER UNDERLINE: SCAN LINE 11
CURSOR UNDERLINE: SCAN LINE 11

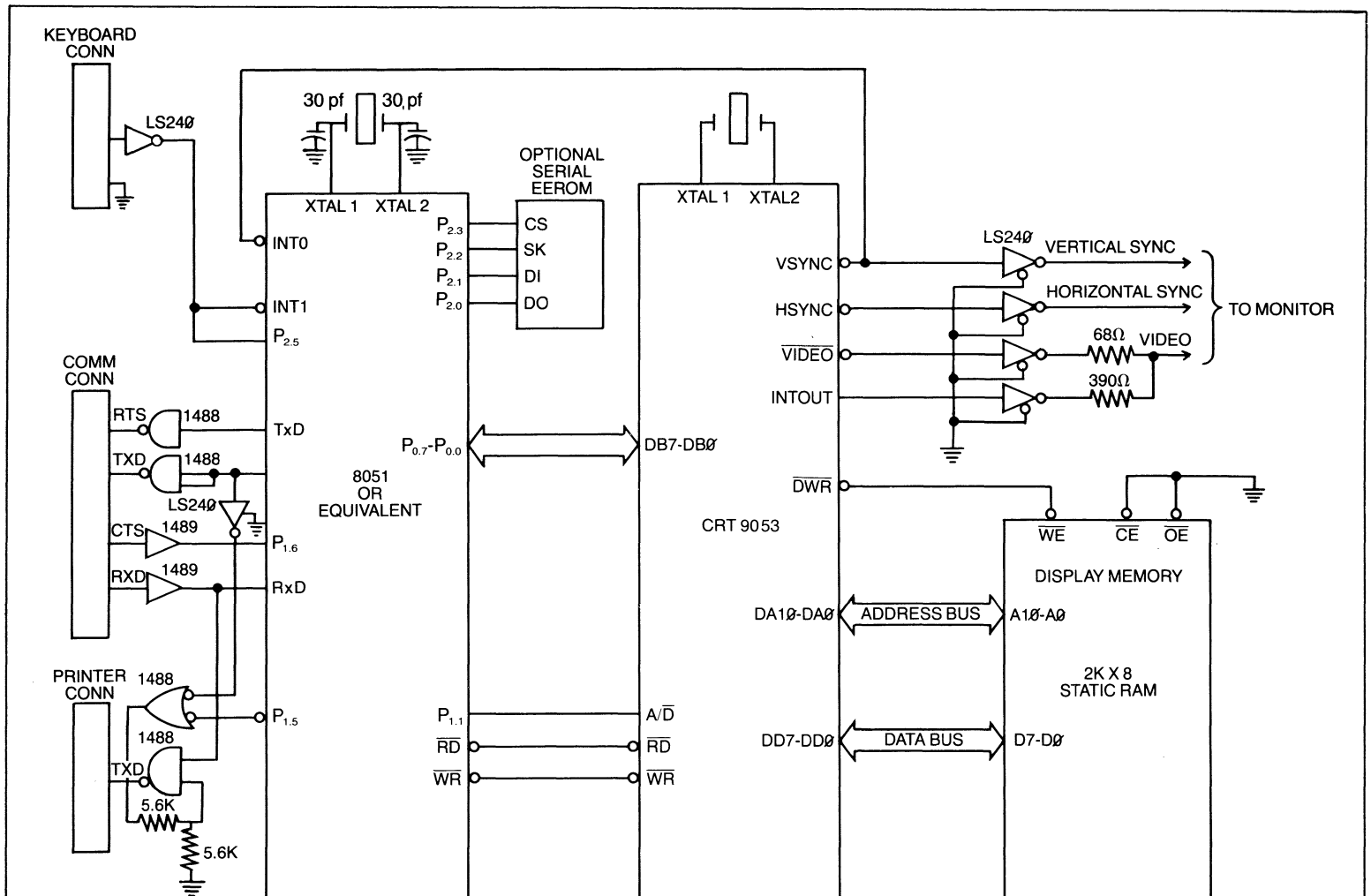
VIII. WIDE GRAPHICS FIGURE DEFINITION:



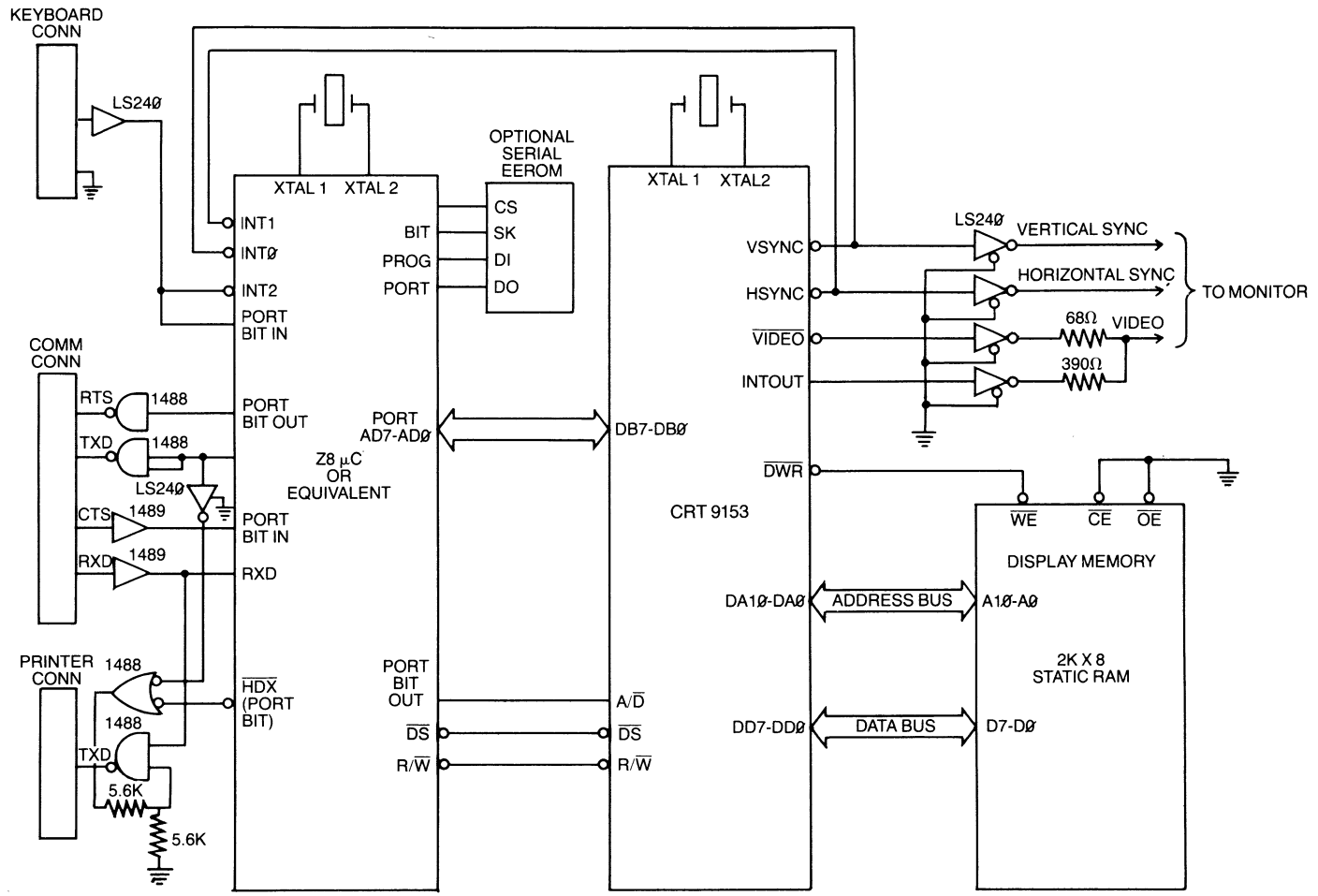
IX. THIN GRAPHICS FIGURE DEFINITION:



SEGMENT 4 = SCAN LINE 6; C8, C7, C6, C5, C4
SEGMENT 3 = C4; SCAN LINES 0, 1, 2, 3, 4, 5, 6
SEGMENT 2 = SCAN LINE 6; C4, C3, C2, C1, C0
SEGMENT 1 = C4; SCAN LINES 6, 7, 8, 9, 10, 11



CRT 9053
TYPICAL APPLICATION



CRT 9153
TYPICAL APPLICATION

CRT 9053/9153-000

DD6 DD4 \ DD3 DD0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1	C7 C1
000	SL1																
	SL11																
001	SL1																
	SL11																
010	SL1																
	SL11																
011	SL1																
	SL11																
100	SL1																
	SL11																
101	SL1																
	SL11																
110	SL1																
	SL11																
111	SL1																
	SL11																

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

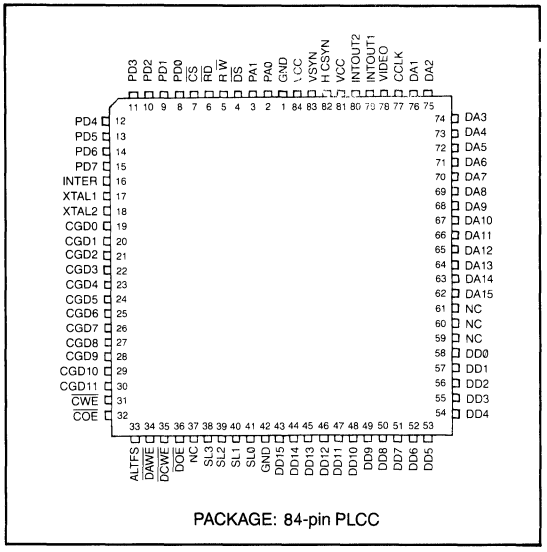
CRT92C07
PRELIMINARY

Advanced Terminal Logic Controller ATLC

FEATURES:

- ☐ Internal 12 Bit 42 MHz Video Shift Register.
- ☐ Internal Oscillator (10 MHz to 42 MHz) or External TTL Clock.
- ☐ Internal Clock Divider to Generate 80/132 columns.
- ☐ Separate 16 Bit Wide Private Display Memory Bus Resolves Memory Contention.
- ☐ Row Table Indirect Video Memory Addressing.
- ☐ X-Y Cursor Addressing.
- ☐ Multiple Bi-Directional Partial Page Smooth Scroll Regions.
- ☐ Line Lock Capability.
- ☐ Programmable Interrupt Generation.
- ☐ Programmable Display Format:
  Dots per character (9-12)
  Characters per Data Row (64-132)
  Data Rows per Frame (24-64)
  Raster Scans per Data Row (10-16)
- ☐ Programmable Sync Format:
  Horizontal Blanking Time (8-128 Characters)
  Horizontal Sync Delay (0-64 Characters)
  Horizontal Sync Pulse (1-64 Characters)
  Vertical Blanking Time (8-255 Scan Lines)
  Vertical Sync Delay (0-63 Scan Lines)
  Vertical Sync Pulse (1-63 Scan Lines)
- ☐ Programmable Attribute Features:
  Character Underline Position
  Cursor Underline Position
  Character Blink Rate and Duty Cycle
  Cursor Blink Rate and Duty Cycle
  Blink Mode
  Four Level Intensity Control

PIN CONFIGURATION



PACKAGE: 84-pin PLCC

- ☐ Mask Programmable Features:
  Vertical Sync Polarity
  Horizontal Sync Polarity
  Video Output Polarity
- ☐ Parallel and Tag Character Video Attributes.
- ☐ External Character Generator—Loadable thru the ATLC.
- ☐ CMOS Technology for Low Power Consumption.
- ☐ All Inputs and Outputs TTL Compatible.

SECTION V

GENERAL DESCRIPTION

The CRT92C07 Advanced Terminal Logic Controller (ATLC) is a CMOS VLSI implementation of all the logic functions required for generation of the timing and video outputs for a terminal design.

The ATLC incorporates all of the functions associated with a CRT controller and an attributes controller. These functions include register programmability of all timing parameters, positioning of cursor, addressing of display memory, control of screen partitions, generation of video and timing signals and application of attributes.

The ATLC provides three independent bus interfaces—the system processor, display memory, and character generator memory. Data is transferred from the processor to the display memory and character generator memory through the ATLC. The double speed architecture of the ATLC provides access to display memory at the character rate for both display refresh and data update functions. The external character generator can be implemented with either EPROM or static RAM (for soft font implementations).

A row table addressing method is used to access character data from display memory. This method provides the capability to create multiple split screens and to smooth scroll each screen region simultaneously and independently. The use of a link within the row table allows flexible manipulation of the sequence of character rows on screen.

The built in attributes controller, equivalent to the CRT9041 Video Attributes Controller, can support parallel, embedded, or tag attributes. All commonly used video terminal attributes are supported; in particular those required for DEC VT100/220 emulation.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
DISPLAY MEMORY INTERFACE			
62-76	Display Memory Address	DA15-1	Output. Fifteen bit Display Memory Address bus. DA15 is the MSB and DA1 is the LSB.
43-58	Display Memory Data	DD15-0	Input/Output. Sixteen bit bi-directional Display Memory Data bus. Character data is transferred on DD7-0 and attribute data on DD15-8. DD15 is the MSB and DD0 is the LSB.
35	Display Memory Character Write Enable	$\overline{\text{DCWE}}$	Output. Active low write strobe to Display Memory. This signal is active when character data is being written to the display memory.
34	Display Memory Attribute Write Enable	$\overline{\text{DAWE}}$	Output. Active low write strobe to Display Memory. This signal is active when attribute data is being written to the display memory.
36	Display Memory Output Enable	$\overline{\text{DOE}}$	Output. Active low output enable strobe to Display Memory. This signal is active whenever character and/or attribute data is read from memory.
CHARACTER GENERATOR MEMORY INTERFACE			
77	Character Clock	CCLK	Output. This output defines the rate at which characters are output to the screen. This signal is also used to externally latch the 8 address bits output from DA7-0 for the external character generator. This clock output does not stop as a result of the RESET or Stop commands.
33	Alternate Font Select	ALTFS	Output. This signal reflects the state of the Underline 2/Alternate Font Select attribute bit (DD0) or the Font Select bit in the Mode 4 register. When it reflects the state of the attribute bit, it is internally pipelined such that it is output at the same time that the associated character data is presented to the address inputs of the character generator. This output is typically connected to the MSB of the address bus to the character generator.
38-41	Scan Line Data	SL3-0	Output. These signals represent scan line data that are used to provide the four LSB's of the character generator address. SL3 is the MSB and SL0 is the LSB.
30-19	Character Generator Data	CGD11-0	Input/Output. Twelve bit bi-directional data bus to the Character Generator memory.
31	Character Generator Write Enable	$\overline{\text{CWE}}$	Output. Active low write strobe to the external character generator memory. This signal is active when the processor is writing pattern data to the Character Generator memory.
32	Character Generator Output Enable	$\overline{\text{COE}}$	Output. Active low output enable strobe to Character Generator Memory. This output is active whenever character pattern data is read from memory.
PROCESSOR INTERFACE			
3-2	Processor Address	PA1-0	Input. These signals represent a 2-bit address bus from the processor which is used to access either the Status, Pointer, Character Data, RAM Address registers or the internal registers pointed to by the Pointer Register.
15-8	Processor Data	PD7-0	Input/Output. Eight bit bi-directional Processor Data bus. PD7 is the MSB and PD0 is the LSB.
6	Read Strobe	$\overline{\text{RD}}$	Input. This signal is used to gate data from the ATLC onto the processor bus. A design using $\overline{\text{DS}}$ and R/$\overline{\text{W}}$ should tie $\overline{\text{RD}}$ to ground. A design using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should tie $\overline{\text{DS}}$ to ground.
5	Read/Write Select	R/$\overline{\text{W}}$	Input. This signal determines if the processor is reading or writing to the ATLC. A design using $\overline{\text{DS}}$ and R/$\overline{\text{W}}$ should tie $\overline{\text{RD}}$ to ground. A design using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should tie $\overline{\text{DS}}$ to ground.
4	Data Strobe	$\overline{\text{DS}}$	Input. This signal causes data to be strobed into or out of the ATLC from the Processor Data bus depending on the state of the R/$\overline{\text{W}}$ signal. A design using $\overline{\text{DS}}$ and R/$\overline{\text{W}}$ should tie $\overline{\text{RD}}$ to ground. A design using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should tie $\overline{\text{DS}}$ to ground.
7	Chip Select	$\overline{\text{CS}}$	Input. This signal is active low and enables all read and write operations between the processor and the ATLC.
16	Interrupt	INTER	Output. This signal is active high and occurs when the ATLC encounters an enabled interrupt causing condition. This signal is reset by reading the Interrupt Status register or a Reset command.

VIDEO INTERFACE			
PIN NO.	NAME	SYMBOL	FUNCTION
82	Horizontal/ Composite Sync	H/CSYN	Input/Output. This signal provides either a horizontal or composite synchronization output. It can also be driven as an input to allow synchronization of horizontal sync to an external source. The function of this signal is register programmable. After reset, this signal defaults to the input mode. The polarity of the signal is mask programmable.
83	Vertical Sync	VSYN	Input/Output. This signal provides either a vertical synchronization output. It can also be driven as an input to allow synchronization of vertical sync to an external source. After reset, this signal defaults to the input mode. The polarity of the signal is mask programmable.
78	Video	VIDEO	Output. This signal provides the serial dot stream for the video interface. The polarity of this signal is mask progammable.
79-78	Intensity Out	INTOUT2-1	Output. These signals provide the two bits of the intensity attribute for use with an external mixing circuit to create variable intensity on screen. This signal is modified at the character rate and is synchronized with the VIDEO output.
MISCELLANEOUS			
17-18	Crystal Input	XTAL1-2	Input. These inputs are used for direct connection to a crystal. An external TTL level clock may be used to drive XTAL1, in which case XTAL2 should be left floating.
81, 84	Power	VCC	5.0 volt power connection.
1, 42	Ground	GND	Ground connection.

SYSTEM DESCRIPTION

The system diagram shown in Figure 1 illustrates the minimum hardware required to implement the display interface for a terminal design using the ATLC. There are three bus interfaces, the video interface and the clock inputs. The only external logic required is a decoder for generating the chip select on the processor bus and an 8 bit latch between the Character Generator RAM and the Display Character RAM.

Processor Bus

The processor bus consists of a 2 bit address bus (PA1-0), 8 bit data bus (PD7-0) and three control signals. The MSB's of the processor address bus are decoded to generate the Chip Select ($\overline{CS}$) signal for the ATLC. Three control signals are available as inputs to the ATLC for data transfers over the bus—Read Strobe ($\overline{RS}$), Data Strobe ($\overline{DS}$) and Read/ Write Select (R/$\overline{W}$). Only two of these three signals will typically be used depending on the type of system processor being used. One option would be $\overline{RD}$ and R/$\overline{W}$, where R/$\overline{W}$ would serve as a write strobe input ($\overline{DS}$ must be grounded), and the other option would be $\overline{DS}$ and R/$\overline{W}$ ($\overline{RD}$ must be grounded).

There are five directly accessible registers in the ATLC which are selected by two address inputs (PA1-0). All other registers in the ATLC are indirectly accessible via one of the direct registers, the Register Pointer. There is also an Interrupt (INTER) output provided identifying key internal events.

Display Memory Bus

The display memory bus consists of a 15 bit address bus (DA15-1), a 16 bit data bus (DD15-0) and three control signals. The 15 bit Display Memory Address bus provides access to a maximum of 32K, 16 bit words which are divided into 8 bits for character data and 8 bits for attribute data. The last 256 memory locations (highest memory addresses) are used to store the row table. The 8 MSB's of the Display Memory Data bus are the attribute data and are used by the ATLC to generate unique attributes for each character output to the screen. The 8 LSB's of the Display Memory Data bus are the character data and this data is latched externally, as shown in Figure 1, to provide 8 of the 13 bits of the address for the character generator memory. There are three control signals—separate write enables for the character and attribute RAM's and an output enable when reading from the RAM's.

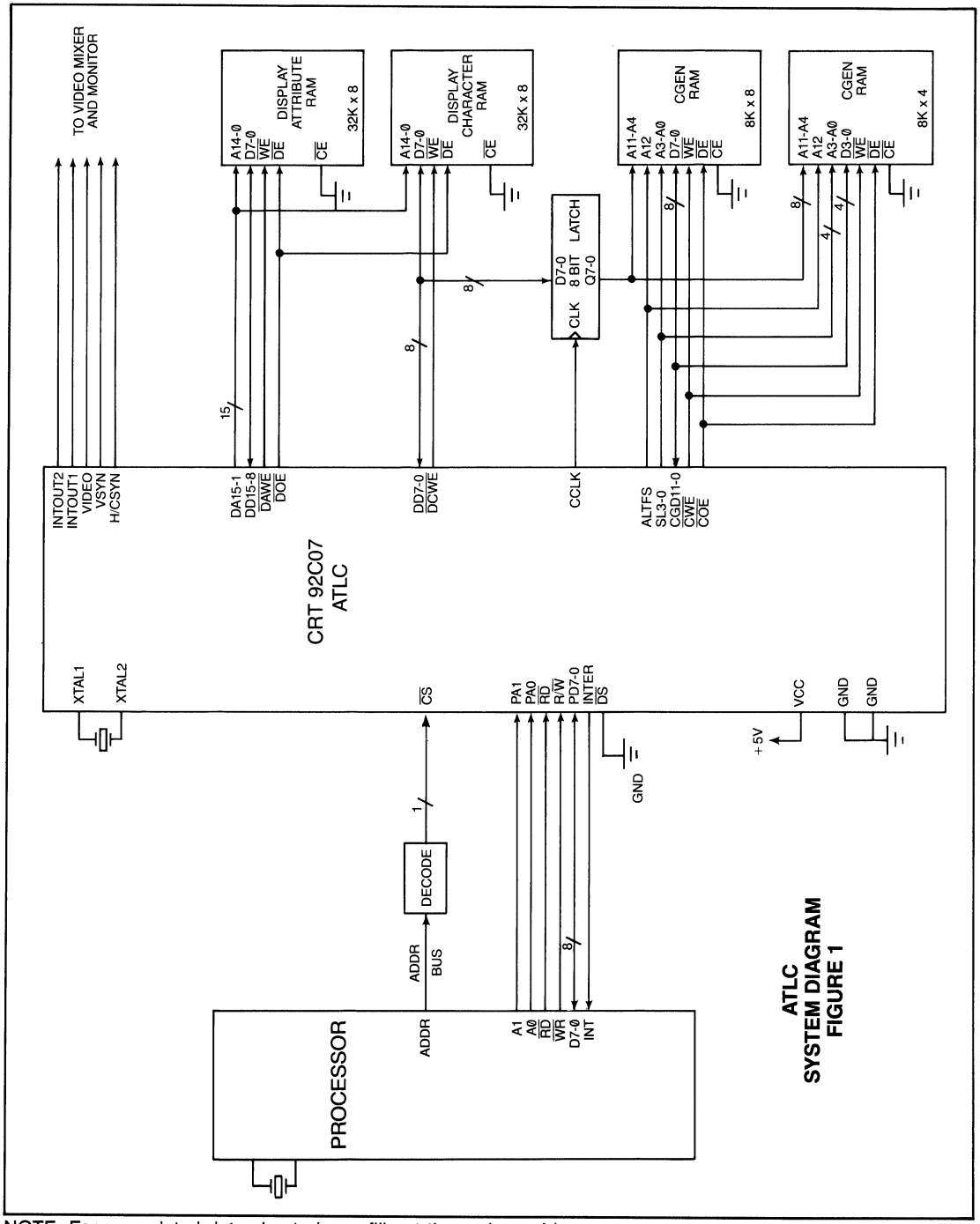
The processor can access the display memory through the ATLC. The processor writes an address to the RAM Address Register which serves as a pointer to the display memory location to be accessed. Next the processor either reads data from or writes data to the display memory through the Character Data register. The ATLC actually performs the transfer with the display memory using a Busy status bit as a flag to indicate when the transfer has been completed. The ATLC is capable of performing two display memory accesses during each character period. One access is for refresh of the screen (during visible scan time) and the other is for data transfers from the processor (at any time). This architecture eliminates the memory contention problem and provides maximum throughput from the processor to display memory.

Character Generator Memory Bus

The character generator memory bus consists of a 13 bit address bus, a 12 bit data bus (CGD11-0) and two control signals. Five of the 13 address bits are output by the ATLC (ALTFS, SL3-0) while the other eight come from the external latch that stores the ASCII character data coming from the Display Character RAM. The 12 bits of pixel data are transferred to the ATLC, processed by the attribute logic and converted to serial form for output on the Video signal. The character generator memory can be implemented with either EPROM or RAM. If RAM is used then the processor can make use of character data and address registers in the ATLC to download the character font. The control signals provided are a write enable and an output enable.

Video Interface

The ATLC outputs all the signals required by the video interface. These include the serial video data signal, two intensity signals and the vertical sync and horizontal/ composite sync signals. The dot clock can be generated by a crystal oscillator internal to the ATLC. The crystal placed on the XTAL1/XTAL2 inputs should be that required for the dot clock used for a 132 column display. When switching between 80 and 132 column displays, the ATLC will automatically perform a divide by 2/3 of the dot clock internally. There is also the option of driving the XTAL1 input with a TTL clock.



ATLC
SYSTEM DIAGRAM
FIGURE 1

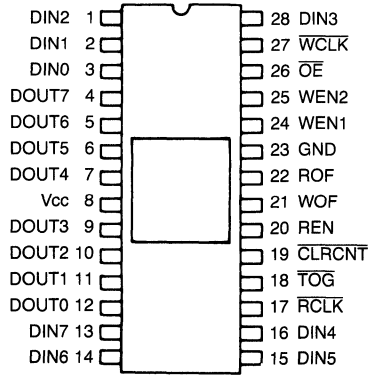
NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

Double Row Buffer DRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

SECTION V

GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

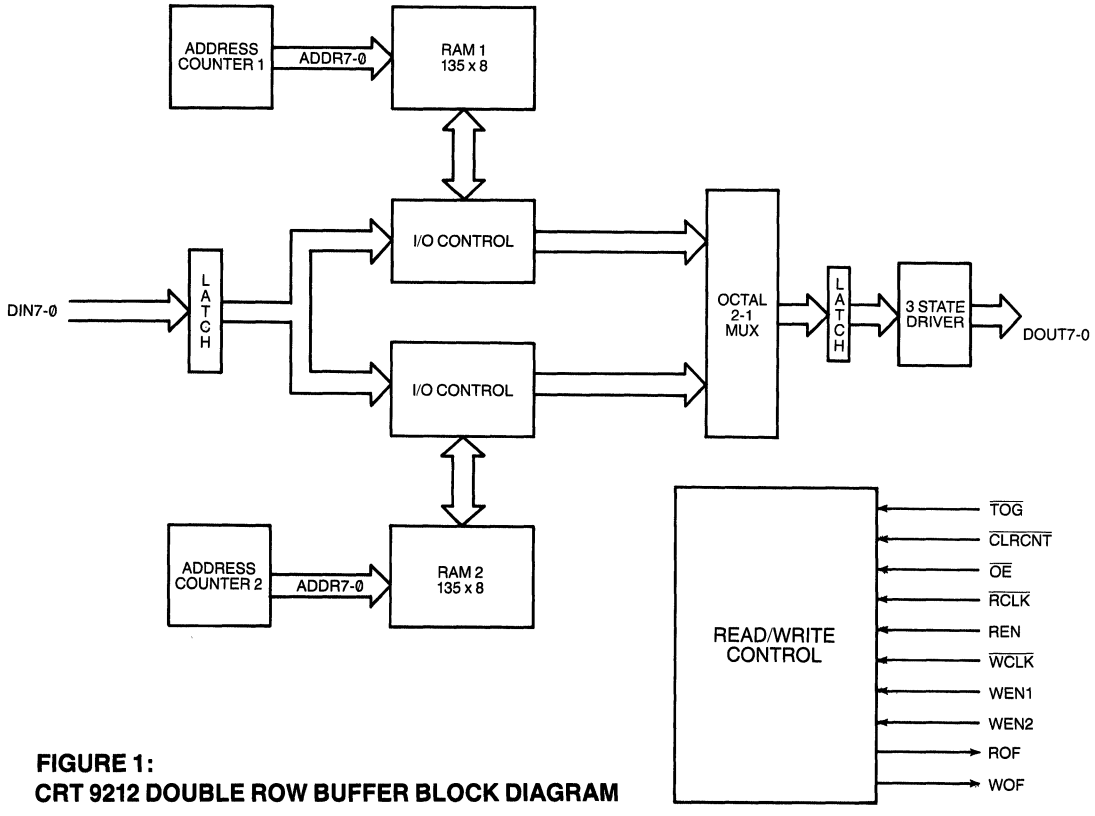


FIGURE 1:
CRT 9212 DOUBLE ROW BUFFER BLOCK DIAGRAM

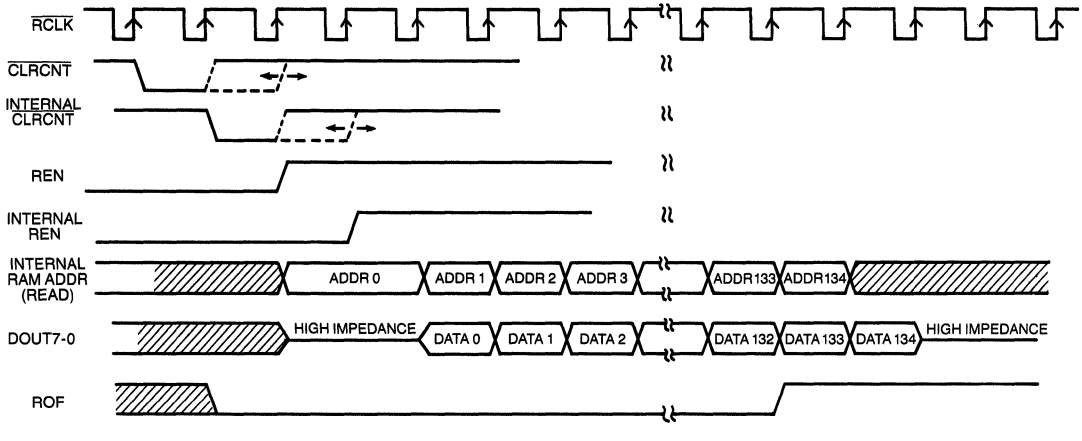


FIGURE 2: CRT 9212 DOUBLE ROW BUFFER READ TIMING

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	Toggle Signal	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and CLRCNT are low.
19	Clear Counter	$\overline{CLRCNT}$	Clear Counter clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4.
24, 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	$\overline{OE}$	When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	WEN1
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

AC CHARACTERISTICS[1]

t_{CYW}	300			ns	Write clock period
t_{CYR}	300			ns	Read clock period
t_{CKH}	247		DC	ns	
t_{CKL}	33			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{RCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30 pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

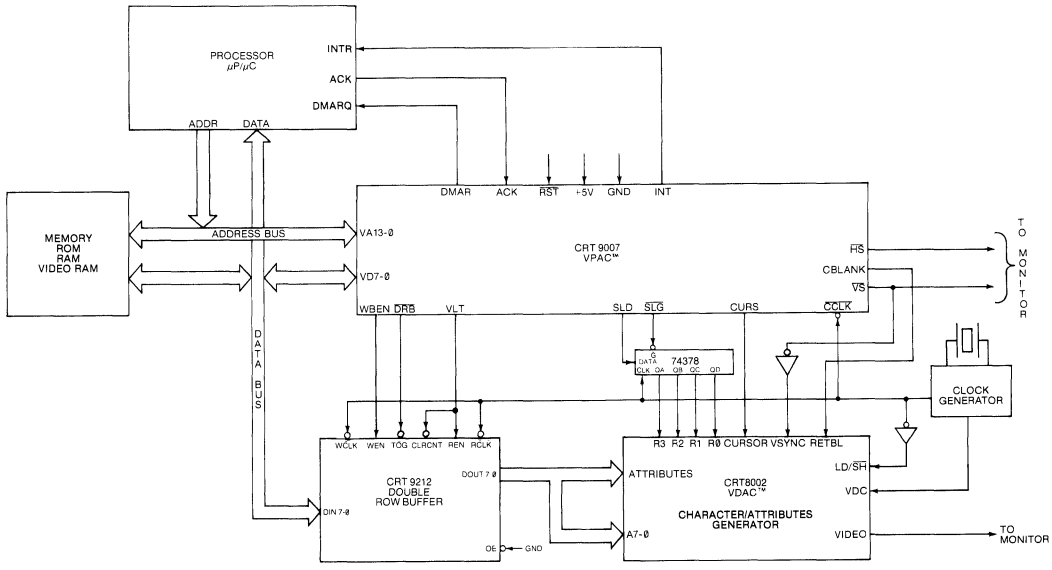


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

SECTION V

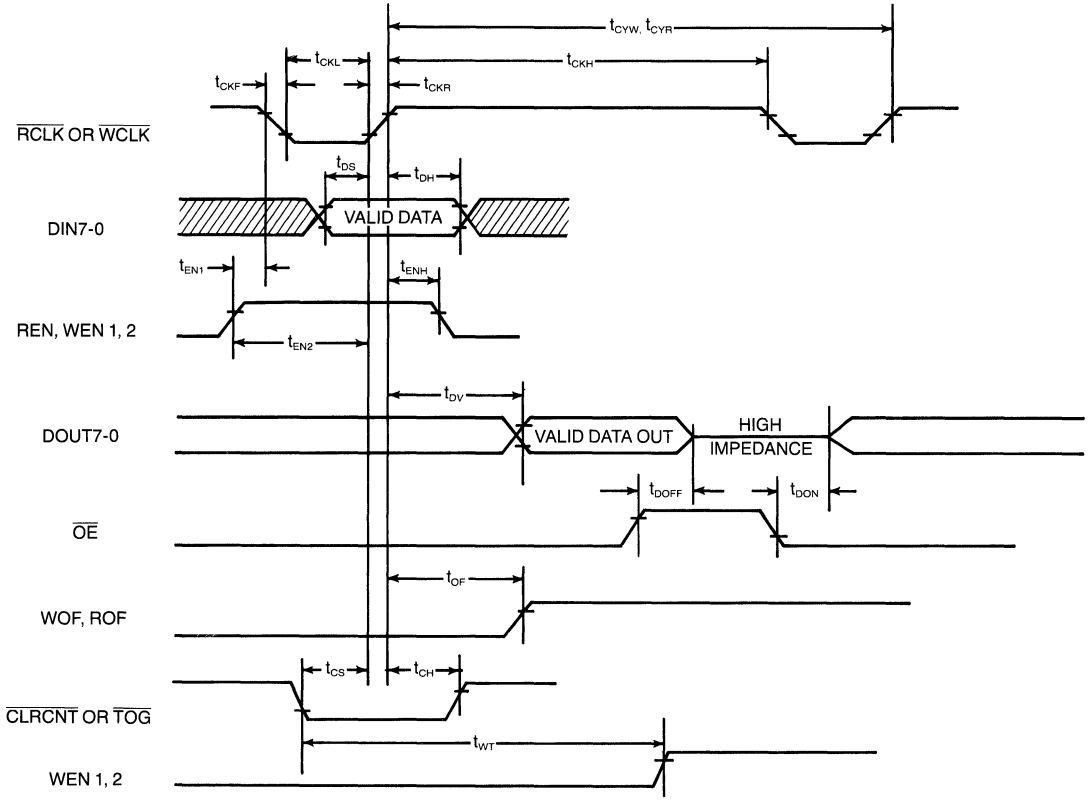
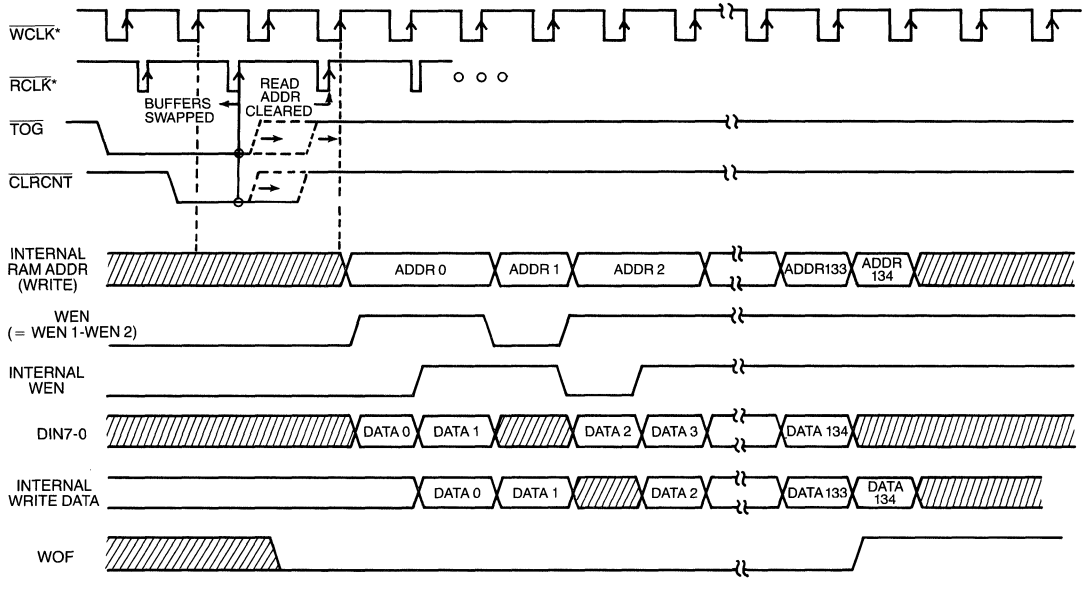


FIGURE 6: CRT 9212 I/O TIMING



* in general $\overline{\text{WCLK}}$ and $\overline{\text{RCLK}}$ can be different

FIGURE 3: CRT 9212 DOUBLE ROW BUFFER WRITE TIMING

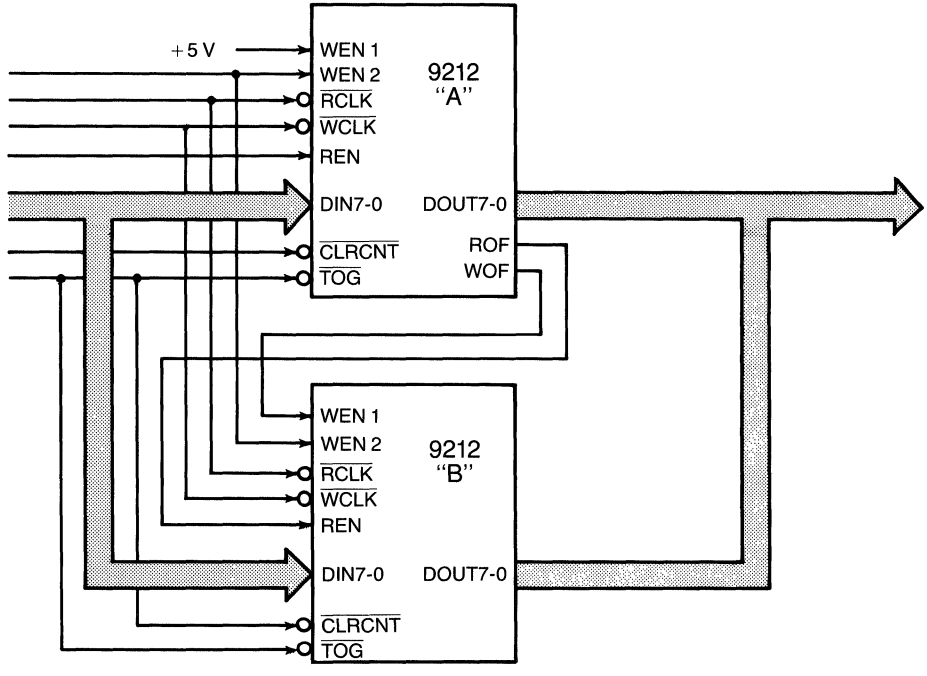


FIGURE 4: CRT 9212 CASCADED CONFIGURATION FOR DATA ROW LENGTHS UP TO 270 CHARACTERS

STANDARD MICROSYSTEMS CORPORATION

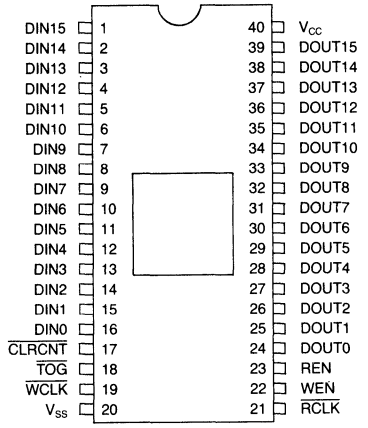
CRT 94C12
PRELIMINARY

Quad Row Buffer
QRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Row Buffer Architecture Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits
- ☐ Supports Both Double Row Buffer and Attribute Assemble Modes of the CRT 9007
- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 9007
- ☐ 40 Pin Dual-In-Line Package
- ☐ Low Power CMOS Technology
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

PIN CONFIGURATION



PACKAGE 40-pin D.I.P.

GENERAL DESCRIPTION

The CRT 94C12 Quad Row Buffer (QRB) is a CMOS VLSI device which provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems yet provides a maximum performance solution when combined with the CRT 9007 and the CRT 9041 VPAC family components.

The CRT 94C12 QRB is a RAM-based buffer which provides four rows of buffering. It appears to the system as two pairs of octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 94C12 can support both the double row buffer and the attribute assemble operation modes of the CRT 9007. These operation modes permit the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data. In addition the attribute assemble mode allows an 8-bit data bus to be used when implementing parallel attributes.

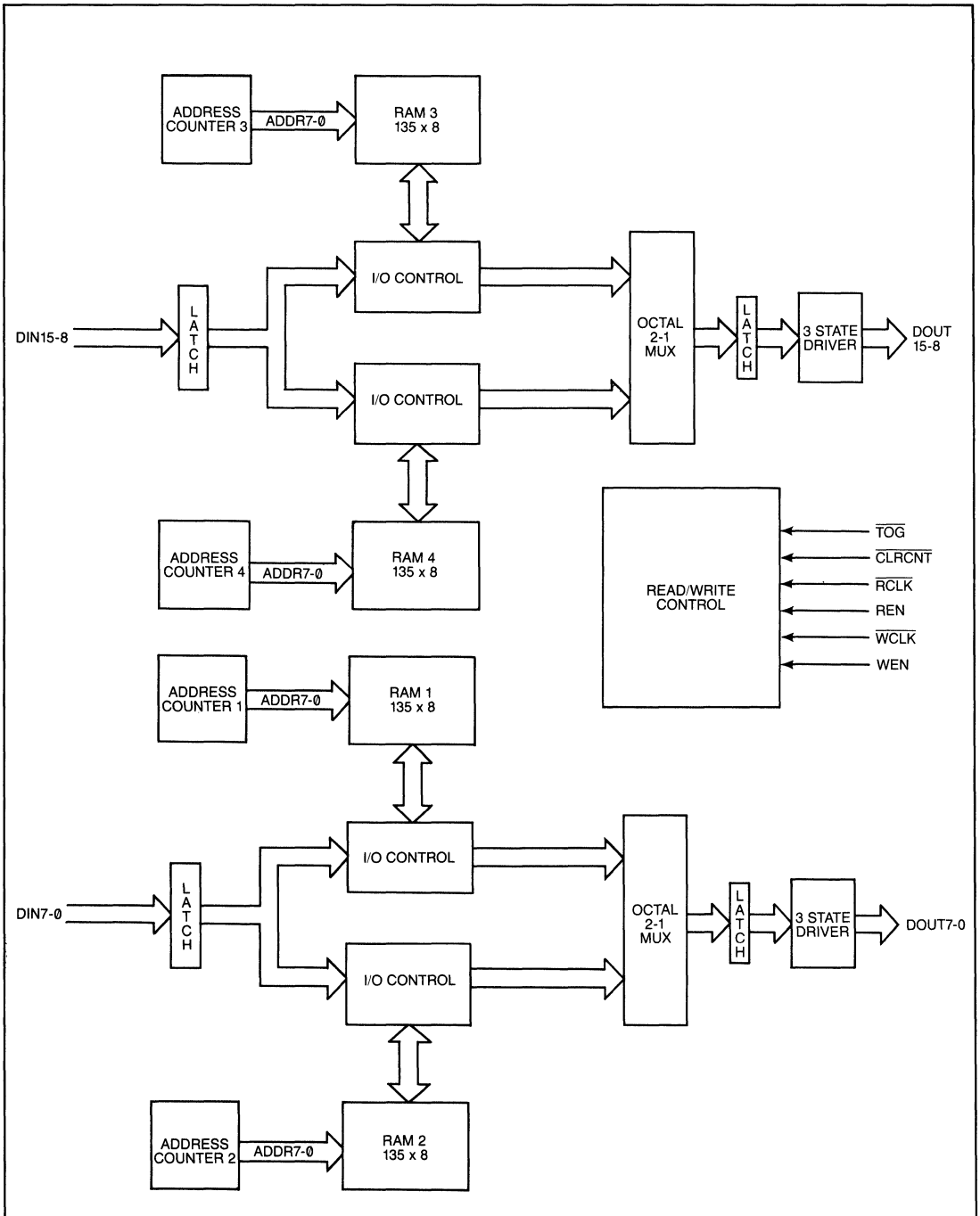


FIGURE 1: CRT 94C12 QUAD ROW BUFFER BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-16	Data inputs	DIN15-DIN0	DIN15-DIN0 are the data inputs from the system memory.
24-39	Data outputs	DOUT15-DOUT0	DOUT15-DOUT0 are the data outputs from the CRT 94C12 internal data output latch. Valid information will appear on DOUT0-DOUT15 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
21	$\overline{Read\ Clock}$	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	$\overline{Toggle\ Signal}$	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and $\overline{CLRCNT}$ are low.
17	$\overline{Clear\ Counter}$	$\overline{CLRCNT}$	$\overline{Clear\ Counter}$ clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
23	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when $\overline{Read\ Clock}$ is active.
22	Write Enable	WEN	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. WEN has an internal pullup resistor allowing it to assume a high if pin 22 is left open.
19	$\overline{Write\ Clock}$	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN is high.
40	Power Supply	V_{CC}	+5 Volt supply
20	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 94C12. It contains 135 bytes of RAM in each of its four buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When Write Enable (WEN) goes high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 94C12 and internal "read" address counter.

Figures 2 and 3 illustrate the functional timing for reading from and writing to the CRT 94C12. The CRT 94C12 is compatible with the VPAC family of devices (CRT 9007, CRT 8002, CRT 9021 and the CRT 9041) and provides up to sixteen bits per character of row buffering with a single device. The sixteen bits can be divided between character data and attributes as required allowing the support of character-by-character, or invisible, attributes. This capability can be implemented using a 16-bit data bus with the double row buffer operation mode of the CRT 9007 or an 8-bit data bus using the attribute assemble operation mode. Typical configurations employing the VPAC family of parts are illustrated in Figures 5 and 6.

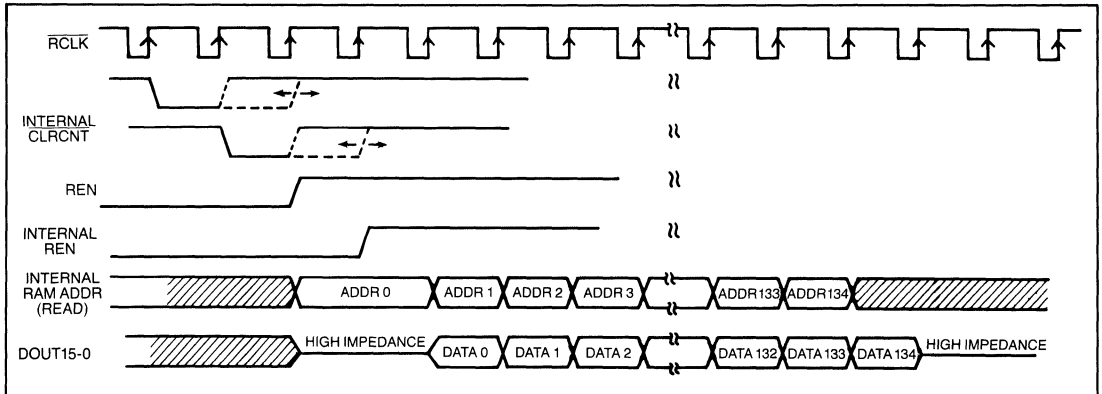
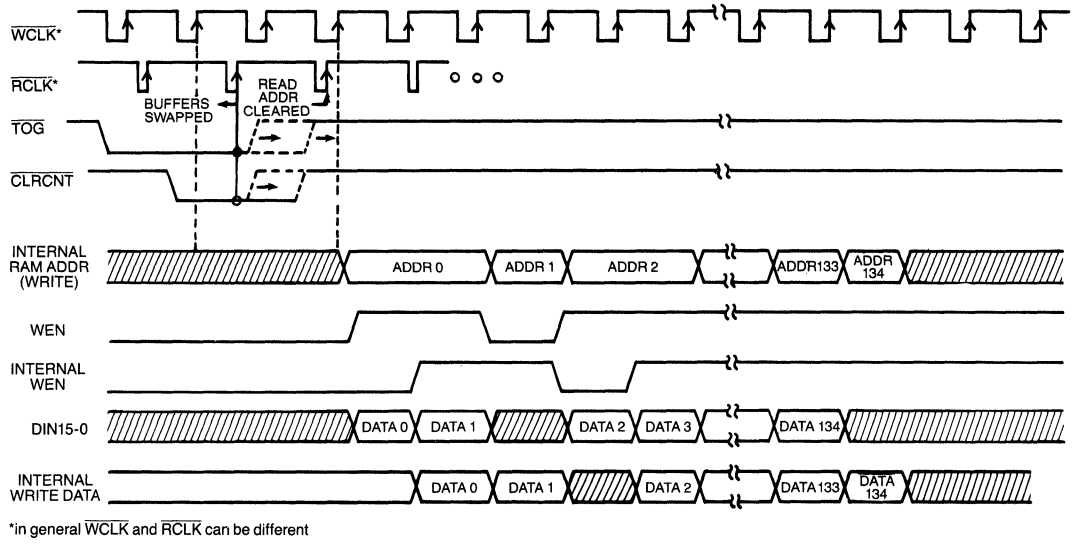


FIGURE 2: CRT 94C12 QUAD ROW BUFFER READ TIMING



*in general WCLK and RCLK can be different

FIGURE 3: CRT 94C12 QUAD ROW BUFFER WRITE TIMING

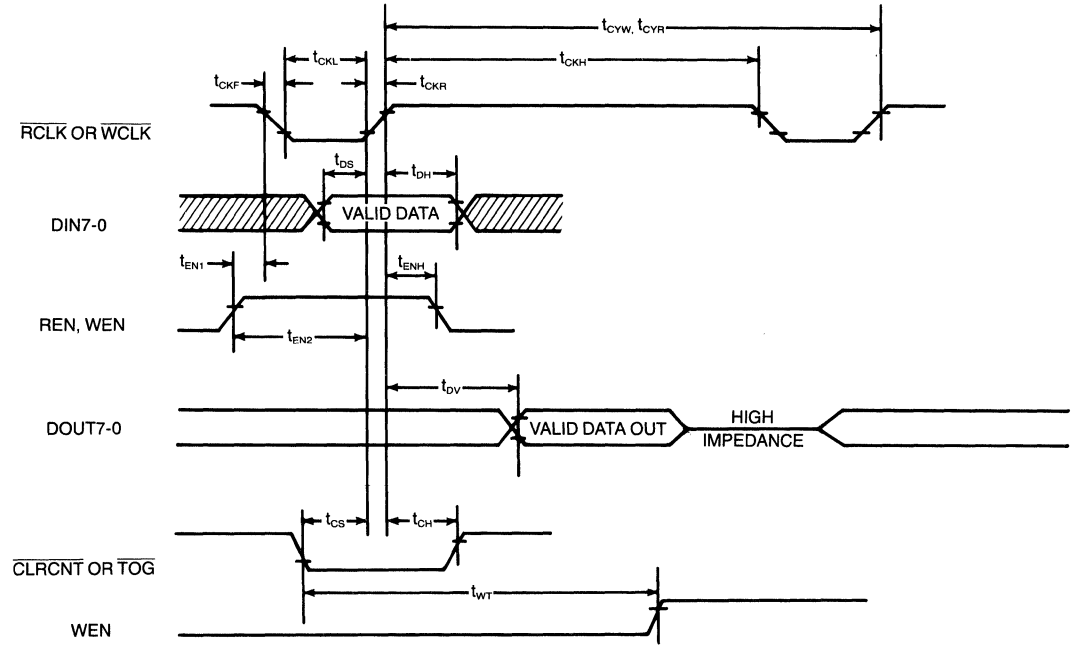


FIGURE 4: CRT 94C12 I/O TIMING

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Maximum V_{CC} ..... +7.0 V
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.3 V
Negative Voltage on any Pin, with respect to Ground ..... −0.5 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 2mA
High Level V_{OH}	2.4			V	I_{OH} = 100 µA
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	$\overline{WEN1}$
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}			40	mA	

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
AC CHARACTERISTICS[1]					
t_{CYW}	250			ns	Write clock period
t_{CYR}	250			ns	Read clock period
t_{CKH}	100		DC	ns	
t_{CKL}	100			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{RCLK}$
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[3]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

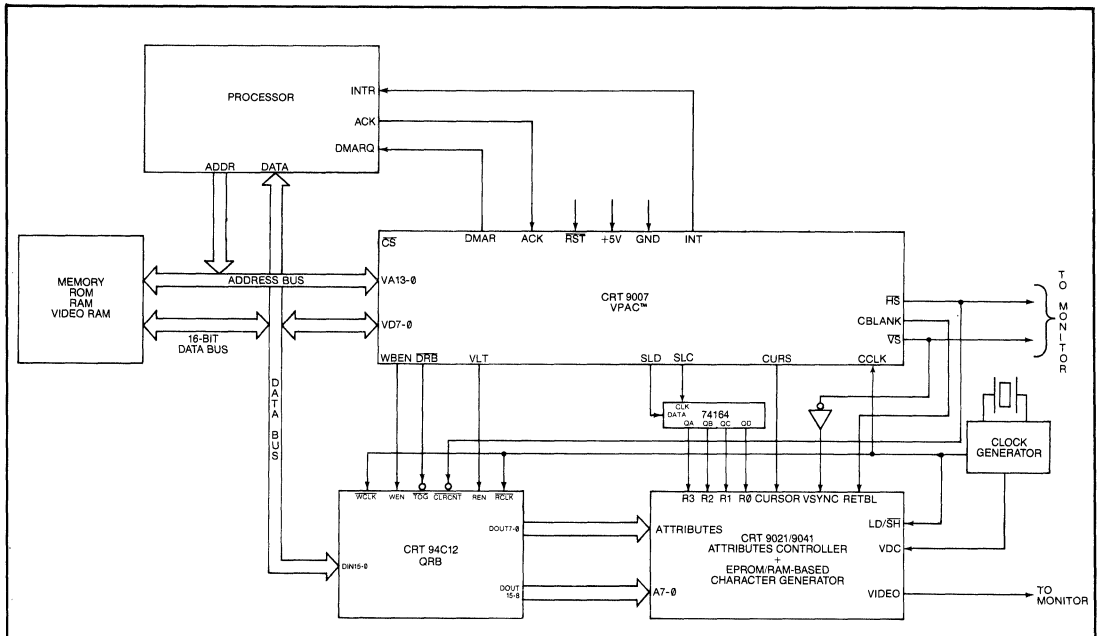


Figure 5. VPAC Configuration With Quad Row Buffer

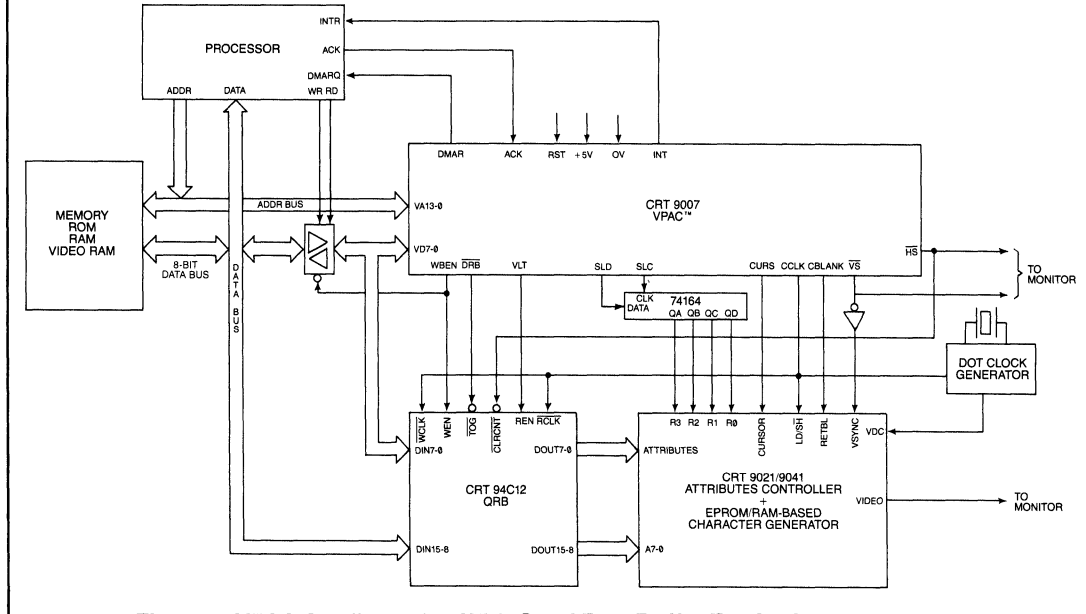


Figure 6. VPAC Configuration With Quad Row Buffer For Attribute Assembly

STANDARD MICROSYSTEMS CORPORATION

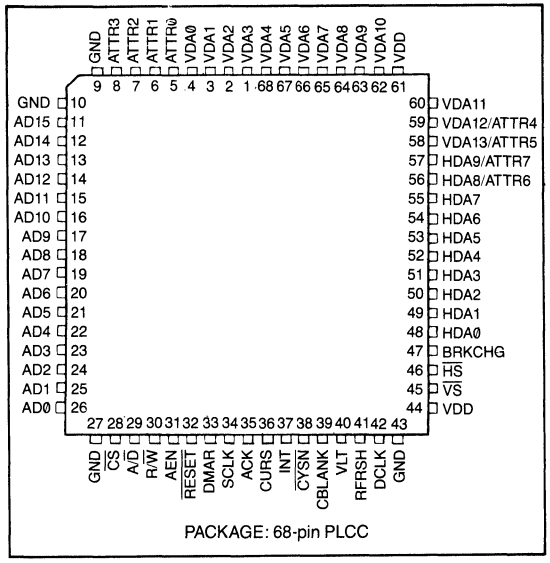
CRT97C11
PRELIMINARY

Video Engine For Windows VIEW

FEATURES:

- ☐ 127 Independent Windows Max per Screen.
- ☐ Windows Specified Relative to Screen:
  - Window Number
  - X-Y Start/End Screen Coordinate
  - X-Y Display Memory Start Address
- ☐ Attributes can be Specified on a per Window Basis:
  - Window Priority
  - Up to 8 Parallel Attributes/Window Output by VIEW
  - Background windows
- ☐ Three Internal Break Address Buffers.
- ☐ 32 Max Visible Horizontal Breaks per Scan Line.
- ☐ Capable of Generating Screen Resolutions as High as 4K x 4K Pixels (assuming a 16 bit wide display memory).
- ☐ Private Display and System Buses:
  - 20 Bit X-Y Display Memory Address Bus + 4 Bit Extended Bus
  - 16 Bit Address/Data Bus to System Memory
- ☐ Separate Clocks for Display and System Buses.
- ☐ DMA Master Capability for Interfacing to System Memory.
- ☐ Automatic and Transparent Dynamic RAM Refresh for Display Memory.
- ☐ Programmable Cursor Output.
- ☐ Fully Programmable Display Format.
- ☐ Normal or Interlaced Video Output.

PIN CONFIGURATION



PACKAGE: 68-pin PLCC

- ☐ Horizontal and Vertical Drive Signals may be Externally Synchronized.
- ☐ Compatible with 680X0 and 80X86 Processors.
- ☐ Low Power CMOS Technology.

SECTION V

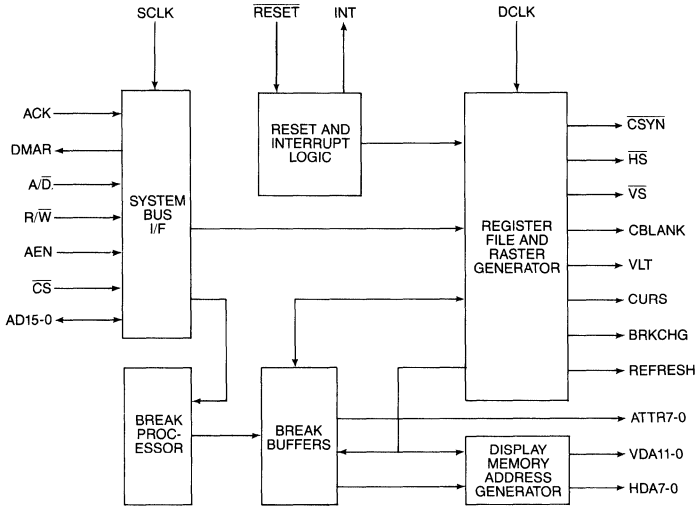
GENERAL DESCRIPTION

The CRT97C11 VIdeo Engine for Windows (VIEW) is a 3rd generation CRT controller following the CRT50x7 family (1st generation) and the CRT9007 (2nd generation). The VIEW is designed to support both bit-mapped graphics and alphanumeric types of CRT displays. This device allows real time manipulation of independent, overlapping windows on the screen with a minimum of processor intervention.

The VIEW architecture provides the system designer with a very high performance and extremely flexible method for supporting the generation of windows on screen. The performance advantage over designs which manipulate windows via software is significant. Windows on screen are defined via a window list maintained in system memory by the system microprocessor and accessed by the VIEW chip. The VIEW chip is also able to access display memory data via a separate memory bus which can be as wide as 24 bits providing a 16M word address range.

The VIEW generates display memory addresses by correlating the X and Y screen coordinates at which the windows start and end with the X and Y display memory addresses. The VIEW stores this information in its three internal break buffers. As the VIEW generates the display memory addresses for the windows, it automatically resolves priority conflicts that arise when two or more windows overlap.

Control of window position on screen, its size and priority relative to other windows and the visible contents of the window are all accomplished via the simple manipulation of data in the window list in system memory. The VIEW buffers and outputs general purpose attribute bits for each window as it generates that window's display memory addresses. The VIEW automatically generates dynamic RAM refresh addresses during the horizontal and vertical retrace intervals.



VIEW FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

DISPLAY MEMORY BUS SIGNALS			
PIN NO.	NAME	SYMBOL	FUNCTION
55-48	Horizontal Display Memory Address	HDA7-0	Output. Eight bits of the Display Memory Address corresponding to the X portion of the window's data address in display memory. HDA7 is the MSB and HDA0 is the LSB.
60 62-68 1-4	Vertical Display Memory Address	VDA11-0	Output. Twelve bits of the Display Memory Address corresponding to the Y portion of the window's data address in display memory. VDA11 is the MSB and VDA0 is the LSB.
42	Display Clock	DCLK	Input. This signal is used to generate all Display Memory Bus cycles. A minimum high voltage of 4.0V must be reached for proper operation.
40	Visible Line Time	VLT	Output. This signal is active high for the visible (non-blanked) portion of every horizontal period including the vertical retrace period.
8-5 58-59 57-56	Attributes	ATTR3-0 ATTR5-4/ VDA13-12 ATTR7-6/ HDA9-8	Outputs. Four of these outputs (ATT3-0) are used as general purpose attributes which are unique to each window being displayed. The other four outputs (ATT7-4) are used as either four additional attribute outputs or as address extension bits for the Horizontal Display Memory Address (ATT7-6/HDA9-8) or the Vertical Display Memory Address (ATT5-4/VDA13-12). The functions served by ATT7-4 are determined by the contents of the Interrupt Enable/Mode Register (R17[1,0]).
41	Refresh	RFRSH	Output. This signal is active high when the VIEW is generating dynamic RAM refresh addresses for the display memory. The refresh address is output on the Vertical Display Memory Address bus during the portion of the horizontal period in which the video is blanked (when VLT is low).
47	Break Change	BRKCHG	Output. The active high state of this signal indicates that the next Display Clock generates a new visible horizontal break.

VIDEO DRIVE SIGNALS			
PIN NO.	NAME	SYMBOL	FUNCTION
46	Horizontal Sync	$\overline{HS}$	Input/Output. This signal initiates a horizontal retrace. Its position and pulse width are programmable. After a hardware or software reset this signal will behave as an input. Programming this signal as an input allows the horizontal scan rate to be synchronized to an external source. An external pullup resistor will be required to guarantee that this signal is inactive high after power-up.
45	Vertical Sync	$\overline{VS}$	Input/Output. This signal initiates a vertical retrace. Its position and pulse width are programmable. After a hardware and software reset this signal will behave as an input. Programming this signal as an input allows the vertical scan rate to be synchronized to an external source. An external pullup resistor will be required to guarantee that this signal is inactive high after power-up.

VIDEO DRIVE SIGNALS			
PIN NO.	NAME	SYMBOL	FUNCTION
39	Composite Blank	CBLANK	Output. This signal goes active high when a vertical or horizontal retrace is going to be initiated. The signal stays active for the entire retrace. CBLANK is used to blank the video to the CRT. The CBLANK signal can be skewed 0 to 3 DCLK's with respect to the Display Memory Address and Attribute bus timings.
38	Composite Sync	$\overline{\text{CSYN}}$	Output. This signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and non-interlace formats. Figure 14 under Functional Description illustrates the $\overline{\text{CSYN}}$ output in both modes.
36	Cursor	CURS	Output. This signal is active high for the programmed number of DCLK periods on each of the programmed scan lines (see descriptions of R11 thru R15). The CURS output can be skewed 0 to 3 DCLK's from the Display Memory Address and Attribute bus timing.
SYSTEM BUS SIGNALS			
11-26	System Address/Data Bus	AD15-0	Input/Output. These 16 signals are used by the system processor to access the internal registers of the VIEW chip when it is in the peripheral mode. When in the master mode then the VIEW chip controls the bus in order to access the window list in system memory. Following a hardware or software reset the VIEW chip will be in the peripheral mode.
28	Chip Select	$\overline{\text{CS}}$	Input. If VIEW is not performing a DMA cycle, the active low state of this input will allow the system to clock data into or read data out of the internal VIEW registers while the inactive high state of this signal will force AD15-0 into an input (high impedance) state. A minimum high voltage of 4.0V must be output for proper operation.
31	Address Enable	AEN	Input. When the VIEW is operating as bus master and performing a DMA cycle, the active high state of this signal will enable the VIEW to output the System Memory Address on AD15-0. The VIEW is not affected by the state of this input unless it has received ACK and is performing a DMA cycle.
30	Read/Write	R/$\overline{\text{W}}$	Input. This signal is used to qualify the $\overline{\text{CS}}$ input and determines whether the system is writing data into (low state) or reading data from (high state) the VIEW registers.
33	DMA Request	DMAR	Output. This signal is driven active high by VIEW to request use of the System Address/Data bus. It will only become active if the DMA Acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
35	DMA Acknowledge	ACK	Input. This active high signal acknowledges a DMA request. It is used to enable the VIEW's DMA mechanism. The system should drive ACK inactive low after DMAR is negated. The state of this signal will not affect VIEW operation unless DMAR is being driven active high.
37	Interrupt	INT	Output. This signal is driven active high when VIEW encounters an enabled interrupt causing condition. This output is reset by reading the Interrupt Status register or a hardware reset. NOTE: This signal should be connected to a level sensitive interrupt input as no edge can be guaranteed between successive interrupts. This output will be reset one full DCLK period after $\overline{\text{CS}}$ goes high after an Interrupt Status 1 register read.
34	System Clock	SCLK	Input. This signal is used to generate all system DMA bus cycles. The rising edge of this signal is used by the VIEW to clock in data from the system memory during a DMA cycle. This signal may be "stretched" by the system to generate long read cycles. A minimum high voltage of 4.0V must be output for proper operation.
29	Address/Data	A/$\overline{\text{D}}$	Input. When the VIEW is in the peripheral mode, this signal selects whether a system bus access is to the Register Pointer Latch or to the register file.
32	Reset	RESET	Input. This active low signal puts the VIEW in a known, inactive state and resets all raster counters. Activating this input has the same effect as executing the software Reset command. The following VIEW signals will be left in the indicated states: $\overline{\text{VS}}$ —Input HS —Input VLT —Inactive Low $\overline{\text{CSYN}}$ —Inactive High CURS —Inactive Low RFRSH —Inactive Low AD15-0 —Inputs DMAR —Inactive Low INT —Inactive Low CBLANK—Active High

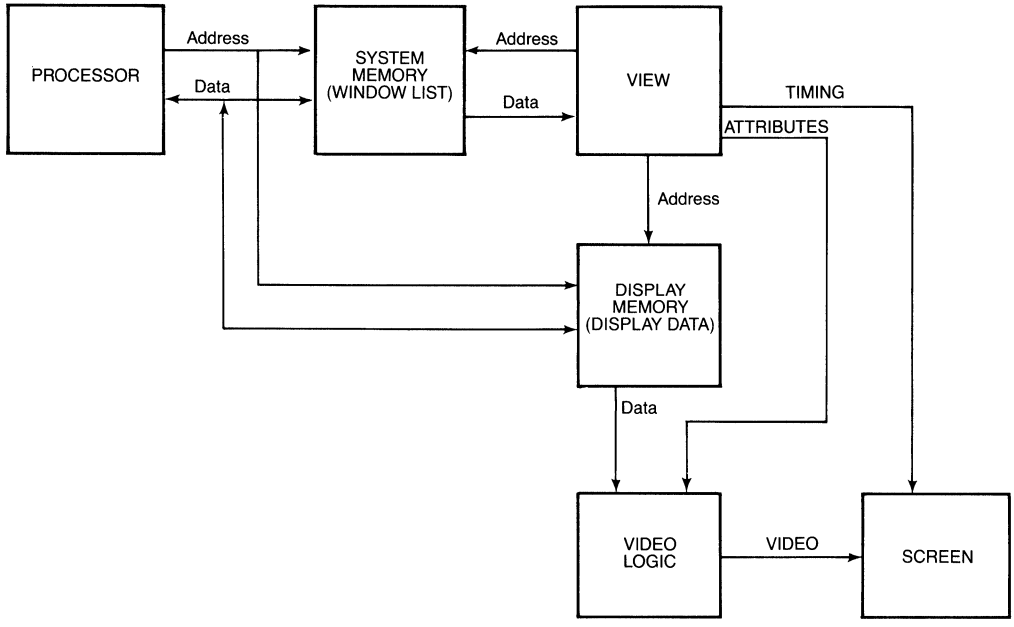


FIGURE 1—SYSTEM ELEMENTS

FUNCTIONAL DESCRIPTION

SYSTEM FUNCTIONS

A display system based on the VIEW must have a minimum set of elements as described in the following sections. The block diagram in Figure 1 provides a simple conceptual illustration of the interconnection of these elements. The sections below will define the purpose of these major elements and also describe how they interact with each other. The VIEW does not restrict the architecture chosen in any particular way and choices made will be determined by the overall system performance goals and cost guidelines.

System Elements

The six blocks shown in Figure 1 are described below in more detail. The interconnection of the blocks are depicted in terms of the address/data buses or other primary inputs or outputs. The details of the interconnection will be determined by the memory arbitration methods implemented and are not being shown here.

a) Processor—The processor can be a system microprocessor (such as the 8088, 80X86, 680X0, etc.) that is responsible for all system functions or a microprocessor dedicated to handling all display and drawing related functions. The processor is responsible for maintaining the window list in system memory and the display data in display memory. For bit mapped graphics applications, overall performance could be improved if a special purpose coprocessor is added to handle the drawing related functions.

b) Window List—The window list is maintained in system memory by the processor. For a definition of the window list and its contents see the section on Screen Management below. The VIEW accesses the window list in order to determine the display memory address sequencing required to generate the windowing effect on screen.

c) VIEW—The VIEW accesses data from the window list, processes it and stores it in internal buffers. The VIEW chip performs all display memory addressing in accordance with the data accessed from the window list. The VIEW can perform both window list and display memory access simultaneously. In addition the VIEW generates video synchronization signals which define the overall video format.

d) Display Data—The VIEW outputs addresses to display memory in a sequence defined by the window list which automatically takes into consideration the overlapping of windows. Display data is stored in memory by the processor in individually allocated areas for each image. Display data can consist of either bit-mapped images or ASCII-based character data. Bit-mapped images may be either single-plane monochrome or multi-plane color. Contention between the VIEW and the processor for access to display memory must be supported at the system design level.

e) Video Logic—This block performs all operations necessary on the data output from display memory before being output as a video signal to the screen. If the data represents bit-mapped images then some typical operations might be serial-to-parallel conversion, color look-up and conversion to RGB output, and other shift operations that may be

required to move images within a window. If the data represents ASCII characters in an alphanumeric only system then some typical functions would include a character generator and attributes controller. In addition the VIEW can output up to 8 attribute signals which are unique to each window and may be used to control specific visual effects.

f) Screen—The output display device can be a CRT or flat panel screen. The VIEW provides all the timing signals required to synchronize the display. See Video Output section below for a more detailed description of these outputs.

System Interaction and Timing

In order to address the problem of memory contention between the processor, VIEW, system memory and display memory, an understanding of the interaction between these elements and their relative timing is important. Whereas the processor can access only one memory (system or display) at a time (unless two processors are used in the system design), the VIEW is capable of performing both memory accesses simultaneously. Refer to Figure 1 while reading this section.

Processor and system memory—Updates of the window list will require activity on the bus between the processor and system memory. This can occur at any time due to operator input or commands received over communications networks which are asynchronous to the screen refresh process. Resolving contention between the processor and the VIEW for access to system memory can make use of the DMA handshake signals provided by the VIEW (see the section on System Interfaces below) or through the use of dual port RAM's.

VIEW and system memory—VIEW accesses the window list whenever it needs to fill its break buffers. This is a periodic process only with reference to the refresh rate. During a given frame refresh the actual timing of these events is determined primarily by a Break Processing Delay parameter and the spacing and number of vertical breaks on the screen. These events always occur before data is needed for screen refresh. See the section on Break Processing below.

Processor and display memory—As in the case with activity between the processor and system memory, update of display data is also driven by commands received via operator input or over communications networks. These events are asynchronous to the screen refresh process. Support for resolving memory contention must be implemented in external logic.

VIEW and display memory—VIEW accesses display memory for the purpose of refreshing the screen image. Therefore this activity is completely synchronous with the video timing and is normally considered the highest priority process within the system.

DISPLAY OUTPUT AND STORAGE

The window list in system memory is used to define and manage windows on screen and specify the data displayed within the windows. The following sections describe the parameters used and how screens and display memory are organized.

Screen Management

The positioning and sizing of windows on a display screen is defined through the use of X and Y coordinates (0, 0 is defined as the upper left corner of the screen). The maximum values of these coordinates is determined by the screen resolution which is defined by the contents of the timing registers (see Operational Description). The absolute maximum values, as determined by the sizes of the coordinate fields in the window list, are 256 for the X coordinate and 4096 for the Y coordinate. Figure 2 shows a screen with a single window in place. The actual location of a window on the screen is determined by a set of 4 coordinates. The left and right edges of the window are defined by XSTART and XEND coordinates and the top and bottom edges of the window are defined by YSTART and YEND coordinates. The width and height of the window is automatically determined from these coordinates. The XSTART and XEND coordinates are called horizontal breaks and the YSTART and YEND coordinates are called vertical breaks (see Break/Link Concept below). These coordinates are stored in the window list data for each window. Horizontally, the spacing of each coordinate is determined by the display data bus width, and vertically, the spacing of each coordinate is one pixel (see the next two sections on Display Memory Management and the Window List).

Display Memory Management

The images viewed through windows on the display screen are determined by a two segment address. This address points to a display memory location which represents the upper left hand corner of the image that appears in the window. The two segment address consists of an X MEMORY ADDRESS and a Y MEMORY ADDRESS. The amount of display memory required is dependent on the application and is a function of the number of independent images to be maintained in memory at the same time and the image sizes to be stored. The VIEW limits the X and Y addressing ranges to 8 bits and 12 bits respectively. Each address segment can be extended by 2 bits. Figure 3a shows a rectangular view of display memory with the unextended limits of addressing indicated. An image area is defined that occupies memory from addresses (0,0) through (X1,Y1). In order to determine what portion of this image will be shown in a window on the screen, an address pointer (X2,Y2) is defined that identifies the upper left corner of the image data to be displayed. This pointer is the X MEMORY ADDRESS and Y MEMORY ADDRESS data stored in the window list. As shown in Figure 3b, each memory location stores N bits of data which is determined by the display memory data bus width.

Window List

The window list (described in detail below under Window Management) contains 6 fields of information that define the relationship between the window on screen and the portion of the display memory image that is shown in the window. As described above, four of the fields are XSTART, XEND, YSTART and YEND which define the position and size of the window on screen. A display memory location (X MEMORY ADDRESS and Y MEMORY ADDRESS) is defined for the upper left corner of the window and all other memory locations are mapped in direct correlation to the width and height of the window. Figure 4 illustrates this relationship. The example shows that the location of the window on screen and the location of the image in memory are independent of each other. The VIEW uses the X MEMORY ADDRESS and the Y MEMORY ADDRESS plus the width and height (ΔX, ΔY) to determine the range of display memory addresses to be generated. Figure 4 assumes N = 8 for the display data bus width which results in a screen size of 1K x 1K pixels and a window size of 256 x 256 pixels.

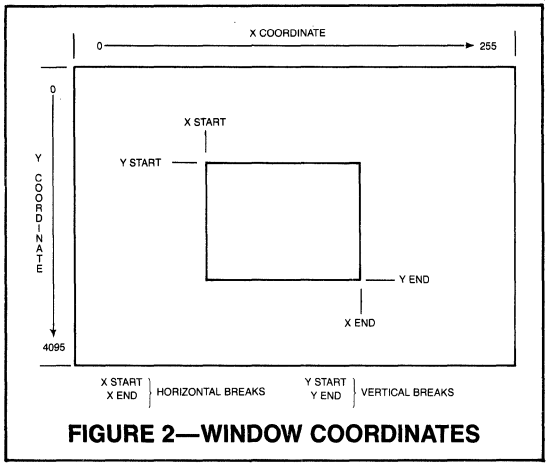


FIGURE 2—WINDOW COORDINATES

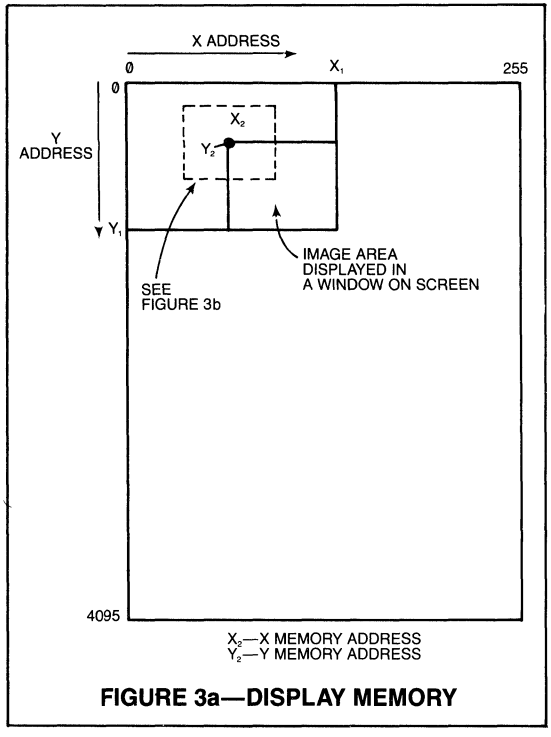


FIGURE 3a—DISPLAY MEMORY

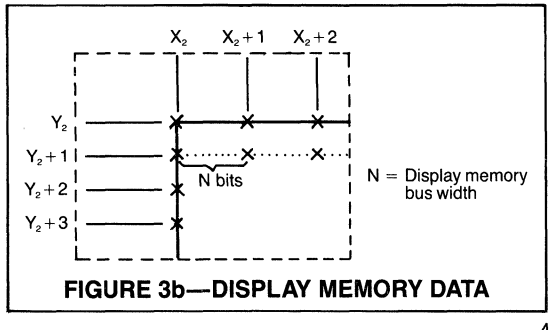


FIGURE 3b—DISPLAY MEMORY DATA

WINDOW MANAGEMENT

The window list is a contiguous set of 16 word blocks of memory which define all parameters associated with each window. A maximum of 127 windows can be defined in a given window list. Up to 32 independent window lists can be maintained in memory at the same time (see R16[7,3] in Operational Description section).

Window List Contents

Each window requires the definition of the following parameters (see Figure 5 for the format):

W0: D15-D12—General Purpose Attribute Bits

The four attribute bits, D15 thru D12, are output on the ATTR3 thru ATTR0 pins. These signals are general purpose and are active during the time the VIEW is generating display memory addresses for the window to which these attributes are assigned.

W0: D10—Background Window Tag Bit

If this bit is set to a one, the associated window is displayed as a background window. The VIEW will generate the same display memory address for every memory access in the window. The address generated is that specified for the X and Y MEMORY ADDRESS described below. If this bit is set to a zero, then all addresses for this window are generated in the normal incrementing manner.

W0: D9-D8—General Purpose Attribute/X Address Extension Bits

Depending on the programming of R17[0] these bits are either General Purpose Attribute bits or X Address Extension bits. When they are programmed to be X Address Extension bits, they function as the X Memory Address MSB's (D9 is the MSB and D8 is the LSB). When they are General Purpose Attributes, D9 is output on ATTR7 and D8 is output on ATTR6.

W0: D7-D0—X Memory Address

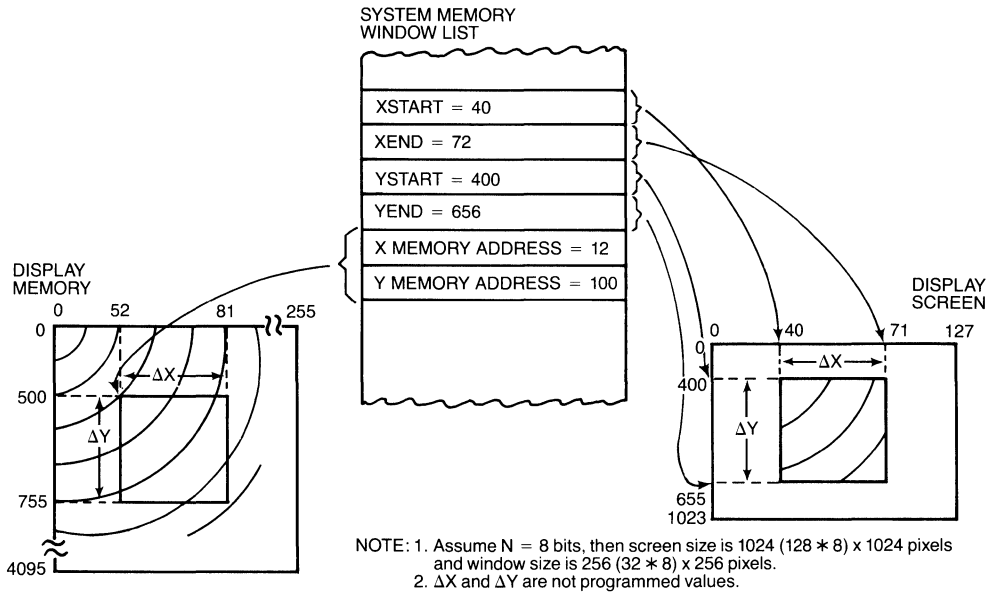
These 8 bits correspond to the X portion of the window's beginning address in display memory. D7 is the MSB and D0 is the LSB. The actual value that is stored in this field depends on the type of window being displayed (normal or background). For a normal window a value equal to [X Memory Address—X Start Break] should be stored (see Figure 4) and for background windows the value stored should be equal to [X Memory Address]. Note that if the X Address Extension is used, then the calculation should be performed using the 10-bit value for X Memory Address and both this field and the X Address Extension field should be programmed with the result. Negative results should be represented in 2's complement form.

W1: D13-D12—General Purpose Attribute/Y Address Extension Bits

Depending on the programming of R17[1] these bits are either General Purpose Attribute bits or Y Address Extension bits. When they are programmed to be Y Address Extension bits, they function as the Y Memory Address MSB's (D13 is the MSB and D12 is the LSB). When they are General Purpose Attributes, D13 is output on ATTR5 and D12 is output on ATTR4.

W1: D11-D0—Y Memory Address

These 12 bits correspond to the Y portion of the window's beginning address in display memory. D11 is the MSB and D0 is the LSB. The actual value that is stored in this field depends on the type of window being displayed (normal or background). For a normal window a value equal to [Y Memory Address—Y Start Break] should be stored (see Figure 4) and for background windows the value stored should be equal



NOTE: 1. Assume N = 8 bits, then screen size is 1024 (128 * 8) x 1024 pixels and window size is 256 (32 * 8) x 256 pixels.
2. ΔX and ΔY are not programmed values.

FIGURE 4—MAPPING MEMORY TO SCREEN

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W0	AT3	AT2	AT1	AT0	0	BK	X EXT/AT7,6		X MEMORY ADDRESS							
W1	0	0	Y EXT/AT5,4						Y MEMORY ADDRESS							
W2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W3	0	INT	0	0					Y START BREAK							
W4	0		WINDOW #						0	0	0	PRIORITY				
W5	X	X	X	X	X	X	X	X				Y LINK				S/E
W6	0			WINDOW #								X START BREAK				
W7	X	X	X	X	X	X	X	X				X LINK				S/E
W8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W11	0	INT	0	0					Y END BREAK							
W12	0		WINDOW #						0	0	0	PRIORITY				
W13	X	X	X	X	X	X	X	X				Y LINK				S/E
W14	0				WINDOW #							X END BREAK				
W15	X	X	X	X	X	X	X	X				X LINK				S/E

FIGURE 5—FORMAT FOR WINDOW LIST

to [Y Memory Address]. Note that if the Y Address Extension is used, then the calculation should be performed using the 14-bit value for Y Memory Address and both this field and the Y Address Extension field should be programmed with the result. Negative results should be represented in 2's complement form.

W3: D14, W11: D14—Window Display Interrupt Tag Bit
If this bit is a one, the VIEW will generate an interrupt (if enabled) during the blanking interval preceding the scan line defined as the YSTART break or the YEND break. W3:D14 provides an interrupt prior to the start of a window on screen and W11:D14 provides an interrupt after the end of a window on screen.

W3: D11-D0, W11: D11-D0—Y Start/End Break Coordinate
This 12-bit value defines a vertical coordinate which corresponds to the scan line on which a window starts or ends on screen. W3: D11-D0 points to the start of a window (YSTART = 400 in Figure 4), while W11: D11-D0 points to the scan line after the end of a window (YEND = 656 in Figure 4). D11 is the MSB and D0 is the LSB. The first break at the top of the screen is 00H and the last is FFFH (assuming the full 12 bit coordinate range is used). With a maximum value of FFFH, the last displayable scan line for a window on screen would be FFEH.

W4: D14-D8, W6: D14-D8, W12: D14-D8, W14: D14-D8—Window Number

This 7-bit value corresponds to the break's window number and represents an offset into the full window list at which all data relating to this window can be found. D14 is the MSB and D8 is the LSB. The contents of these four fields should be the same. Window number 00H is reserved. See the section entitled Window List Addressing for more details.

W4: D4-D0, W12: D4-D0—Priority

This 5-bit value represents this window's priority relative to the other windows. This value is used by VIEW to resolve which of two or more overlapping windows will be displayed on a coordinate by coordinate basis. The contents of these two fields should be the same. D4 is the MSB and D0 is the LSB. NOTE: Two windows with the same priority cannot exist on the same scan line. This presents the restriction that no more than 32 windows can overlap.

W5: D15-D8, W7: D15-D8, W13: D15-D8, W15: D15-D8—Backward Link

This 8-bit value (marked by X's in Figure 5) is not used by the VIEW and therefore could be used by the system software for the purpose of defining a Backward Link. The format of this parameter could be similar to that of the X/Y Link and Start/End Tag parameters defined below (8 bits are reserved) or any other format dictated by the system software. These bits are reserved for this purpose and future versions of the VIEW will not make use of them.

W5: D7-D1, W7: D7-D1, W13: D7-D1, W15: D7-D1—X/Y Link

This 7-bit value is a pointer to the next break in ascending coordinate sequence. The X/Y link is actually a window number which represents the next window encountered when sequencing through the windows along the coordinate axis. This value when combined with the associated Start/End Tag bit uniquely identifies the next break. D7 is the MSB and D1 is the LSB. See section on Break/Link Concept for more detail.

W5: D0, W7: D0, W13: D0, W15: D0—Start/End Tag Bit

This one bit value indicates whether the window break defined in the associated X/Y Link is the start or the end of the window. A value of "1" indicates the end of a window and a value of "0" indicates the start of the window.

W6: D7-D0, W14: D7-D0—X Start/End Break Coordinate

This 8-bit value defines a horizontal coordinate which corresponds to the column at which a window starts or ends on screen. W6: D7-D0 points to the start of a window (XSTART = 40 in Figure 4) while W14: D7-D0 points to the memory word after the end of a window (XEND = 72 in Figure 4). D7 is the MSB and D0 is the LSB. The first break at the left of the screen is 00H and the last is FFH. With a maximum value of FFH, the last displayable memory word for a window on screen would be FEH.

NOTE: The contents of words W2, W8, W9 and W10 are not used by the VIEW and may be utilized by the system processor to store other window related information.

Break/Link Concept

The VIEW accesses the window list in order to determine the exact sequence of display memory addresses to be generated to create the desired windowing effect on screen. The VIEW makes use of both break and link information contained in the window list in order to traverse the list in the correct sequence. As the VIEW traverses the list, it checks the priority and location of each window to determine whether it is active for a given region of the screen. A region is defined as that portion of a screen between two vertical breaks. For each active window the VIEW accesses the address information found in the window list, performs calculations on it and stores it in one of three internal break buffers. The contents of the break buffers are then accessed sequentially to generate the display memory addresses required during the screen refresh period.

Breaks—Breaks are the screen coordinates, both vertical and horizontal, at which windows start or end. Figure 6 provides an illustration. Four windows are shown with the X START and END COORDINATES (horizontal breaks) identified at the top—0, 5, 9, 23, 35, 42, 60 and 100. The Y START and END COORDINATES (vertical breaks) are identified at the left—0, 70, 130, 290, 360, 440, 500.

Links—When processing the window list, the VIEW makes use of a series of pointers that link the breaks together in sequential order. The window list contains two linked lists—one for vertical breaks and one for horizontal breaks. The link parameter contains two data items—a window number and a tag bit. The

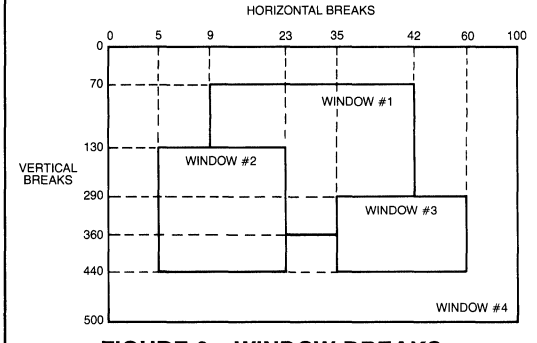


FIGURE 6—WINDOW BREAKS

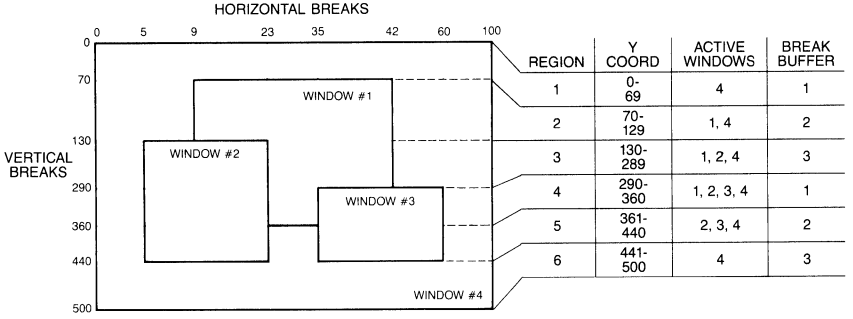
	X START		X END		Y START		Y END	
	COORD	LINK	COORD	LINK	COORD	LINK	COORD	LINK
WINDOW #1	9	2E	43	3E	70	2S	361	3E
WINDOW #2	5	1S	24	3S	130	3S	441	4E
WINDOW #3	35	1E	61	4E	290	1E	441	2E
WINDOW #4	0	2S	101	00	0	1S	501	00

FIGURE 7—WINDOW LINKS

window number identifies which window is encountered next when sequencing through the breaks. The tag bit identifies whether it is the start ("S") or end ("E") of the window. (See the section under Window List Contents for a definition of these data items.) Figure 7 lists all the breaks and links for the example shown in Figure 6. End breaks in Figure 6 represent actual coordinates of last scan line or last display memory word for each window while in Figure 7 each end break value stored in the window list is one more than defined in Figure 6. The VIEW starts processing breaks at the upper left corner of the screen (see Break Processing below), which in this example is window 4. The following list describes the breaks and links along the horizontal axis for this example.

- Break "0"—Coordinate for start of window 4.
- Link "2S"—Pointer to the start of window 2.
- Break "5"—Coordinate for start of window 2.
- Link "1S"—Pointer to the start of window 1.
- Break "9"—Coordinate for start of window 1.
- Link "2E"—Pointer to the end of window 2.
- Break "24"—Coordinate for end of window 2.
- Link "3S"—Pointer to the start of window 3.
- Break "35"—Coordinate for start of window 3.
- Link "1E"—Pointer to the end of window 1.
- Break "43"—Coordinate for end of window 1.
- Link "3E"—Pointer to the end of window 3.
- Break "61"—Coordinate for end of window 3.
- Link "4E"—Pointer to the end of window 4.
- Break "101"—Coordinate for end of window 4.
- Link "00"—Terminator for end of horizontal breaks.

As shown, a special link, or terminator, equal to "00" is used to indicate the last break in the sequence. A similar sequence exists for the vertical breaks. The VIEW uses the two independently linked lists to perform the break processing described in the next section. It is the responsibility of the window management software to create and maintain these links in the window list in system memory when manipulating windows on screen.



REGION	Y COORD	ACTIVE WINDOWS	BREAK BUFFER
1	0-69	4	1
2	70-129	1, 4	2
3	130-289	1, 2, 4	3
4	290-360	1, 2, 3, 4	1
5	361-440	2, 3, 4	2
6	441-500	4	3

FIGURE 8—BREAK PROCESSING EXAMPLE

	FRAME REFRESH	BUFFER USED		BREAK PROCESSING	BUFFER USED	ACCESS TIME
				REGION 6	3	39 SCLK's
FRAME REFRESH				① LAST BREAK PROCESSED		10 SCLK's
				BREAK DELAY (R10)		
VERTICAL RETRACE				② REGION 1	1	44 SCLK's
				REGION 2 ③	2	39 SCLK's
				REGION 3	3	39 SCLK's
			④ 0			
FRAME REFRESH	REGION 1	1	70	REGION 4 ⑤	1	39 SCLK's
	REGION 2	2	130	REGION 5 ⑥	2	42 SCLK's
	REGION 3	3	290	REGION 6 ⑥	3	39 SCLK's
	REGION 4	1	360			
	REGION 5	2	440	⑦ LAST BREAK PROCESSED ⑥		10 SCLK's
	REGION 6	3	500	BREAK DELAY (R10)		
				REGION 1	1	39 SCLK's

FIGURE 9—BREAK PROCESSING TIMING

Break Processing

For each screen refresh, the VIEW accesses the window list by reading all vertical breaks for each region of the screen (more than one vertical break in a region is possible if multiple windows either end or start on the same scan line) and then reading all horizontal breaks. When reading the horizontal breaks, the VIEW processes the address and attribute data for each active window and stores this data in the next available break buffer.

Figure 8 and 9 will be used to illustrate this process. Figure 8 repeats the same screen layout as shown in Figure 6 and adds four columns which identify the region, the range of Y coordinates for that region, active windows in that region, and the break buffer used to store data for that region. Figure 9 illustrates the timing of the window list accesses and the break buffer activity for a single frame refresh period.

During a given frame refresh, the Last Break Processed interrupt will occur when the vertical break for the end of the screen is processed ①. At this time the VIEW will not attempt to start break processing for the next frame refresh until after the Start Delay (see R10[5,0]) timeout has terminated ②. This timeout may occur before or after the start of vertical retrace and is strictly a function of the Start Delay parameter and when the Last break Processed interrupt occurs. This delay allows time for the processor to manipulate the window list. At this time the VIEW will request access to the system bus by activating the DMAR signal. When the ACK signal is activated, the VIEW will process the first four vertical breaks which provides all the data needed to refresh these regions on screen ③. When frame refresh starts, the VIEW will make use of the data in break buffer 1 to refresh the first region on screen ④. At the completion of this period, the contents of break buffer 1 are no longer needed and the VIEW processes the next vertical break (between vertical coordinates 29 and 36—region 4). The data for refreshing region 4 is now placed in break buffer 1 ⑤. Similarly, at the completion of the refresh of regions 2, 3 and 4, break buffers 2, 3 and 1 become available and the VIEW processes the breaks for regions 5 and 6 and stores this data in break buffers 2 and 3 and then processes the last break, represented by the Y break at coordinate 500 (no break buffer is required in this case) ⑥. Once again the VIEW will generate the Last Break Processed interrupt and the entire cycle will start again ⑦.

Figure 9 also shows the amount of time that the VIEW takes to perform the break processing. This time is measured in SCLK's. The formula to calculate this timing is as follows—

$$8W + 3Y + 4$$

where W = Number of total windows (for the example in Figure 6, W would equal 4 for all regions).

Y = Number of vertical breaks with the same break coordinate (start or end) for a given region. For the example in Figure 6, Y equals 1 for regions 1, 2, 3, 4, 6 and Y equals 2 for region 5. Y = 2 for region 5 because windows 2 and 3 end on the same scan line (same Y break coordinate).

Three special conditions exist with respect to the above calcuation—

1) If the break being processed is the final break (break which represents the last scan line on the screen), then the formula is modified as follows—

$$3Y + 7$$

2) If the break being processed is the first break (break which represents the first scan line on the screen—Region 1 in the example), then the formula is modified as follows—

$$8W + 3Y + 9$$

3) If the break being processed is the first break after the VIEW has been given a Start command, then an additional 2 SCLK's should be added to the result.

Window List Addressing

As indicated above, each window is defined by the parameters stored in a 16 word block of system memory. In addition to the 127 blocks of system memory required to define all possible windows (numbered 1 through 127), there is also a block reserved for window # 0 that serves a special purpose. When the VIEW processes breaks for the next frame refresh, it starts with the block that defines the first window to be encountered at the upper left corner of the screen. The pointer to that block is found in the first two words of the block for window # 0. Figure 10 shows the contents of this special block of data. The LSB of the first word identifies the X START LINK and S/E tag bit and the LSB of the second word identifies the Y START LINK and S/E tag bit. All other bits in this block of memory should be reset. These two link parameters define the entry points to the linked lists for vertical and horizontal breaks.

The address generated by the VIEW for accessing the window list consists of three segments (see Figure 11). The 5 MSB's (AD15-11) are defined by the contents of the Window List Start Address found in register (R16[7,3]). This base address allows the VIEW to access up to 32 independent window lists. The next 7 bits (AD10-4) are defined by the specific window number which is included in the data accessed from the window list. The 4 LSB's (AD3-0) are the offset within each window list which points to a specific data item.

SYSTEM INTERFACES

System Memory

The VIEW operates in two modes—peripheral and master. Following a hardware $\overline{\text{RESET}}$ or a software Reset command, the VIEW will be in peripheral mode. In this mode, the processor can access the VIEW's internal registers by means of the $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ inputs. After a Start command, the VIEW will begin to generate DMA requests. When it receives a DMA acknowledge from the processor, the VIEW will operate in bus master mode (see Figure 12). In this mode, the VIEW will use its DMA circuitry to request the use of the system bus from the permanent master (typically the system processor) when it needs to fill its break buffers. When the VIEW disables its DMA request, it will again revert to peripheral mode (see Figure 13). Table 1 defines the activity on the System Address/Data Bus for the control signal states shown.

After processing the last break for a given frame refresh, the VIEW will wait the period of time specified in the Start Delay register before it starts to access system memory again. After this time, the VIEW will start to load the break buffers for the first break of the next frame refresh. This feature prevents system memory access conflicts as it provides the processor with a window of programmable length in which it can address the VIEW as a peripheral, disable the VIEW's DMA mechanism, access the internal registers and access the window list in system memory.

ADDRESS	WINDOW ϕ DATA															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	X START LINK							S/E [1]
1	0	0	0	0	0	0	0	0	Y START LINK							S/E [1]
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIGURE 10—WINDOW ϕ CONTENTS

NOTE: [1] Both S/E tag bits should be set equal to zero because the first window boundaries encountered will always be the start of a window.

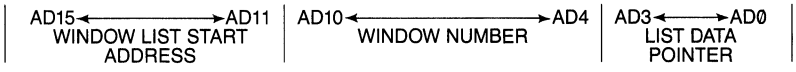


FIGURE 11—WINDOW LIST ADDRESSING

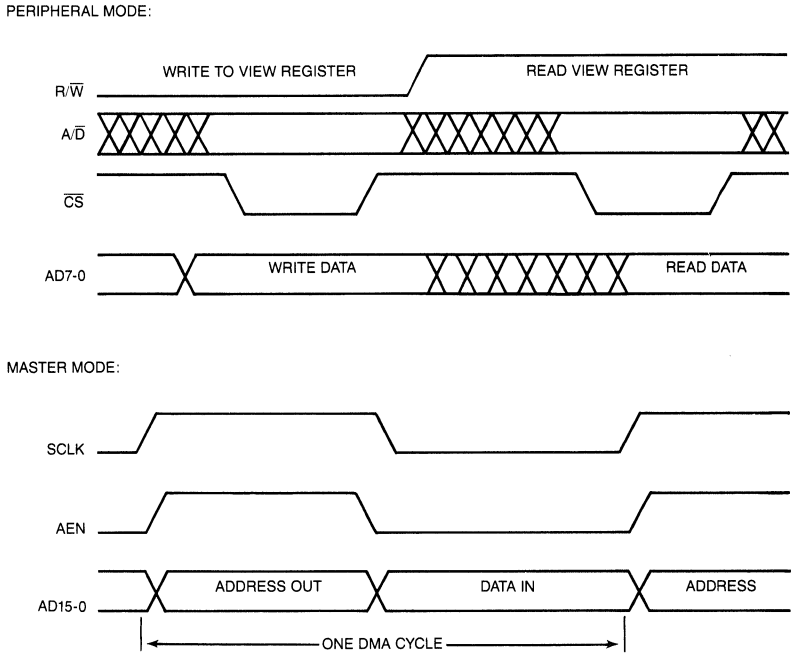


FIGURE 12—VIEW PERIPHERAL/MASTER MODE

The VIEW will tri-state its System Address/Data bus (AD15-0) when it is not performing a DMA cycle and when it is not selected ($\overline{CS}$ in its inactive state) for register access. The processor can also disable the DMA mechanism by issuing a STOP command. In this case the VIEW will not access system memory again until a START command is issued. However, the VIEW will continue to refresh the display memory if transparent refresh is enabled.

Display Memory

The VIEW addresses display memory as a rectangular memory space with a two segment address—8 bits for the horizontal range (HDA7-0) and 12 bits for the vertical range (VDA11-0). Each segment can be independently extended by two bits (see description of General Purpose Attribute Bits below). The logic required to support the RAS/CAS address generation (required when using DRAM's) and to arbitrate display memory accesses must be implemented externally.

If display memory is implemented using DRAM's, then the VIEW supports the refresh of memory through the use of an internal twelve bit binary counter. The outputs of this counter are used to drive the Vertical Display Memory Address bus (VDA11-0) during the portion of the horizontal period in which the video is blanked (when VLT is low). The counter is incremented by the DCLK signal the number of times specified by the Memory Refresh Count register during each horizontal blanking interval (for the entire vertical period). The counter is set to zero (counting is inhibited) by a software Reset command or a hardware RESET. The counter can also be disabled at any time by setting the Memory Refresh Count register to zero. The counter will not initiate the counting sequence until the VIEW receives a Start command. The VIEW drives the RFRSH output active high when it is driving the VDA11-0 bus with the counter output. To take advantage of the VIEW's refresh function, the VDA11-0 bits should be used for the DRAM row address.

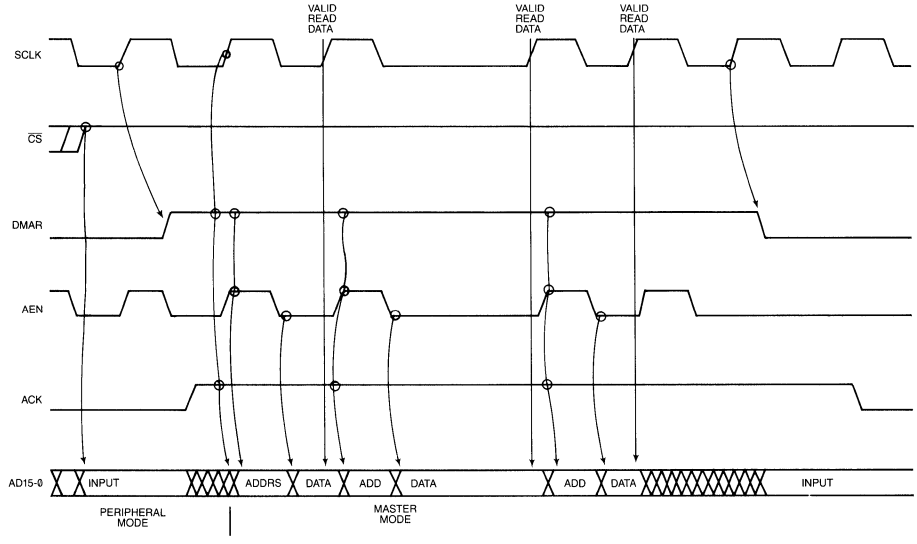


FIGURE 13—VIEW DMA CYCLE

MODE	R/W*	CS*	ADR	DMAR	ACK	AEN	AD15 – AD8	AD7 – AD0
PERIPHERAL	1	0	0	0	X	X	X	READ REG FILE
PERIPHERAL	1	0	1	0	X	X	X	READ REG POINTER
PERIPHERAL	0	0	0	0	X	X	X	WRITE REG FILE
PERIPHERAL	0	0	1	0	X	X	X	WRITE REG POINTER
PERIPHERAL	1	0	0	X	0	X	X	READ REG FILE
PERIPHERAL	1	0	1	X	0	X	X	READ REG POINTER
PERIPHERAL	0	0	0	X	0	X	X	WRITE REG FILE
PERIPHERAL	0	0	1	X	0	X	X	WRITE REG POINTER
PERIPHERAL	X	1	X	0	X	X	HIGH IMPEDANCE (INPUT) STATE	
PERIPHERAL	X	1	X	X	0	X	HIGH IMPEDANCE (INPUT) STATE	
MASTER	X	1	X	1	1	0	HIGH IMPEDANCE (INPUT) STATE	
MASTER	X	1	X	1	1	1	DMA ADDRESS (OUTPUT)	

SYSTEM ADDRESS/DATA BUS
TABLE 1

Video Output

Cursor Control

The VIEW provides a cursor output (CURS—pin 36) with separate programmable X and Y start and duration values. The cursor output will become active when the value programmed in the Horizontal Cursor Position register is equal to the X component of the raster counter and the value programmed in the Vertical Cursor Position register is equal to the Y component of the raster counter. It will remain active for the number of DCLK periods specified in the Horizontal Cursor Duration register before returning to its inactive state. The cursor output's action will be repeated on the scan lines following the one specified in the Vertical Cursor Position register for the number of scan lines specified in the Vertical Cursor Duration register.

As the Horizontal and Vertical Cursor Position registers are changed, the information read from the Interrupt Status register will indicate in which window the cursor resides. This is determined by the location of the upper left corner of the cursor block as specified in the Horizontal and Vertical Cursor Position registers. If the cursor position registers place the cursor simultaneously in two or more overlapping windows, the status will report it as being in the window with the highest priority.

Window Attributes

Unique attributes can be specified for each window. Two types of attributes are used internally by the VIEW—the window interrupt tag bits and a background window tag bit. There are also eight general purpose attribute bits. All of these bits are accessed by the VIEW during break processing and stored internally in break buffers.

Window Interrupt Tag Bits

Two interrupt tag bits are assigned to each window. When either of these bits are set and the Y Break Interrupt Enable bit (R17[4]) is set, an appropriate interrupt will be generated by the VIEW during the horizontal retrace period. The tag bit associated with the Y Start break will cause an interrupt to be generated during the horizontal retrace period prior to the first scan line of the window. The tag bit associated with the Y End Break will cause an interrupt to be generated during the horizontal retrace period following the last scan line of the window. The timing of these interrupts is independent of whether the first or last scan lines of the window are obscured by a higher priority window. See discussion of R17[4] in Register Descriptions section and W3: D14 and W11: D14 in the Window List section.

Background Window Tag Bit

See description of this bit (W0: D10) in the section on the Window List.

General Purpose Attribute Bits

The eight general purpose attribute bits do not affect the internal operations of the VIEW, however they are read and output on the ATTR7-0 pins during the time the VIEW is generating display memory addresses associated with that window. The functionality of four of the eight attribute bits can be programmed by the Attribute Select bits in R17[1,0] (see Register Descriptions section). Independently, two of the bits can be programmed to extend the Horizontal Display Memory Address and the other two can be programmed to extend the Vertical Display Memory Address.

Horizontal and Vertical Sync

The horizontal and vertical synchronization outputs are programmable with respect to their pulse width and position relative to the horizontal and vertical visible display times. See Figure 14 for typical waveforms in interlaced and non-interlaced modes. They can also be configured so as to allow external signals to initiate horizontal and vertical retrace cycles. If the external horizontal sync is enabled and an external signal drives the $\overline{HS}$ input low, the VIEW will initiate a horizontal retrace cycle on the leading edge of the second DCLK pulse following $\overline{HS}$ going low. This will lock the VIEW's horizontal frequency to that of the external signal. If the external vertical sync is enabled and an external signal drives the $\overline{VS}$ input low, the VIEW will initiate a vertical retrace cycle on the leading edge of the next $\overline{HS}$ pulse. This will lock the VIEW's vertical frequency to that of the external signal. When external sync is enabled, the vertical and horizontal periods must be programmed to be the same as the master sync generator. Note that it is possible for the first frame to be out of sync in interlace mode.

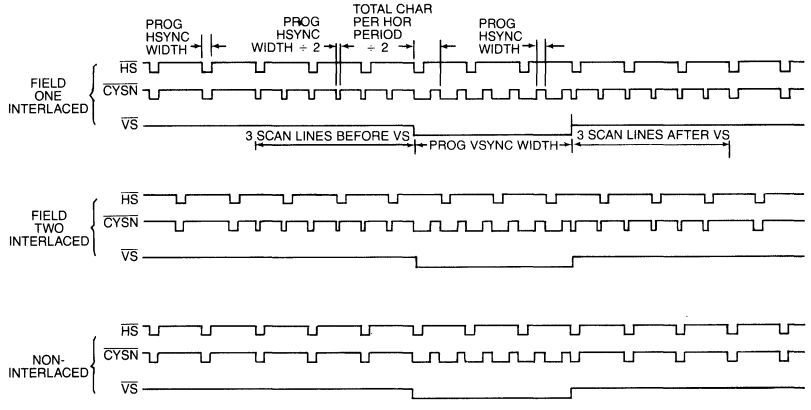


FIGURE 14—TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

OPERATIONAL DESCRIPTION

REGISTER ACCESSIBILITY

Figures 16 and 17 illustrate the bit layout of all addressable registers within the VIEW. Access to these registers takes place over the System Address/Data Bus (AD15-0). Specific registers are selected for reading and writing by means of a Register Pointer Latch. Data transfers to and from the registers takes place over the 8 LSB's of the address/data bus (AD7-AD0, see Table 1). Control over the access to both the registers and the Register Pointer Latch is accomplished via the A/$\overline{D}$, R/$\overline{W}$ and $\overline{CS}$ inputs (see Table 2). These registers should not be accessed during a DMA cycle (DMAR and ACK both active).

A/$\overline{D}$	R/$\overline{W}$	FUNCTION
0	0	Write to register in register file
0	1	Read register in register file
1	0	Write to Register Pointer Latch
1	1	Read from Register Pointer Latch

TABLE 2—ACCESS TO VIEW REGISTERS

The Register Pointer Latch is 8 bits wide (Fig. 15). The five LSB's are used to select the desired register. The three MSB's are used to initiate Start, Stop and Reset commands via software. The allowable combinations of bit settings for the Register Pointer Latch are shown in Fig. 15.

D7	D6	D5	D4 D3 D2 D1 D0	
RESET	STOP	START	REGISTER NUMBER	FUNCTION
1	0	0	X X X X X	RESET
0	1	0	X X X X X	STOP
0	0	1	X X X X X	START
0	0	0	←——N——→	ACCESS REGISTER N

X—Don't care N—Register address

FIGURE 15—REGISTER POINTER LATCH

Executing one of the three commands requires the exclusive setting of one of the three MSB's. When accessing a register all three MSB's must be reset. Execution of the commands causes the following actions to take place:

RESET: Writing this command will cause the VIEW to respond exactly as though the Reset pin was strobed. All raster counters will be reset and the signals listed below will be left in the states indicated:

$\overline{VS}$	—Input
$\overline{HS}$	—Input
$\overline{VLT}$	—Inactive Low
$\overline{CSYN}$	—Inactive High
CURS	—Inactive Low
RFRSH	—Inactive Low
AD15-0	—Inputs
DMAR	—Inactive Low
INT	—Inactive Low
CBLANK	—Active High

STOP: Writing this command will cause the VIEW to disable its DMA circuitry and drive its CBLANK signal active high. The VIEW will not initiate a DMA request again or drive the System Address/Data bus until it receives a new Start command. Horizontal and vertical sync generation will not be affected.

START: Writing this command will cause the VIEW to initiate its internal operations by starting its raster counters and filling its break buffers. The VIEW always generates even field raster addresses following a Reset command.

NOTE: A minimum delay of 4 full SCLK periods is required between a Stop, Start, or Reset command or a hardware Reset and writing to the VIEW registers. The clock periods are counted starting with the first rising edge of SCLK following the rising edge of $\overline{CS}$.

	D7	D6	D5	D4	D3	D2	D1	D0
R0	HORIZONTAL CYCLE MSB'S							
R1	HOR CY LSB	HORIZONTAL SYNC WIDTH						
R2	INTER MODE	HORIZONTAL DELAY						
R3	HORIZONTAL VISIBLE							
R4	VERTICAL CYCLE LSB'S						SCAN MODE	EXT SYNC ENABLE
R5	VERTICAL CYCLE MSB'S							
R6	VERTICAL SYNC WIDTH							
R7	VERTICAL DELAY							
R8	VERTICAL VISIBLE LSB'S							
R9	VERTICAL VISIBLE MSB'S						MEMORY REFRESH COUNT	
R10	BLANK SKEW	START DELAY						
R11	CURS SKEW	V CUR DUR MSB	HORIZ CURSOR DURATION					
R12	VERTICAL CURSOR DURATION LSB'S							
R13	HORIZONTAL CURSOR POSITION							
R14	VERT CURSOR POS MSB'S							
R15	VERTICAL CURSOR POSITION LSB'S							
R16	WINDOW LIST START ADDRESS						0	0 0
R17	INTERRUPT ENABLE							ATTR SEL

FIGURE 16—VIEW REGISTERS (WRITE)

	D7	D6	D5	D4	D3	D2	D1	D0
RR17	INTERRUPT STATUS 1							
RR18	INTERRUPT STATUS 2							
RR13	HORIZONTAL CURSOR POSITION							
RR14	VERT CURSOR POS MSB'S							
RR15	VERTICAL CURSOR POSITION LSB'S							

FIGURE 17—VIEW REGISTERS (READ)

REGISTER DESCRIPTIONS

HORIZONTAL TIMING—

HORIZONTAL CYCLE (9 Bits—R0[7,0], R1[7])—Write only.

Defines the horizontal period length (visible and blanking time). This field should be programmed with the total number of DCLK periods in the entire horizontal period minus four times the number of DCLK periods specified for the Horizontal Sync Width (see Figure 18).

HORIZONTAL SYNC WIDTH (7 Bits—R1[6,0])—Write only.

Defines the duration of the Horizontal Sync signal ($\overline{HS}$). This field should be programmed with the number of DCLK periods that compose the horizontal synchronization pulse (see Figure 18). The minimum value is 3.

HORIZONTAL DELAY (7 Bits—R2[6,0])—Write only. Defines the delay between the start of the Horizontal Sync signal and the start of the next visible scan line. This field should be programmed with N − 3 where N is the number of DCLK periods between the beginning

of the $\overline{HS}$ signal and the leading edge of the VLT signal. If this register is programmed with a value that is greater then the horizontal blank interval, the horizontal sync pulse will begin before the horizontal blank interval yielding a negative "front porch" (see Figure 18). The minimum value is 1.

HORIZONTAL VISIBLE (8 Bits—R3[7,0])—Write only. Defines the length of the visible portion of the total horizontal period. This field should be programmed with N – 1 where N is the number of DCLK periods that the display is not blanked during the horizontal period (see Figure 18).

NOTE: VIEW requires that the display must be blanked a minimum of 11 DCLK periods (interlaced display) or 7 DCLK periods (noninterlaced display) in a Horizontal Cycle.

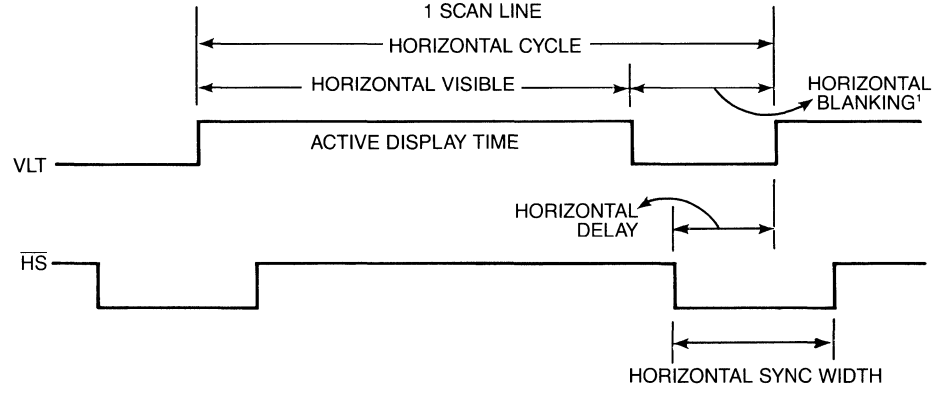
VERTICAL TIMING—

VERTICAL CYCLE (13 Bits—R5[7,0], R4[7,3])—Write only. Defines the vertical period length (visible and blanking time). This field should be programmed with 6 less than the total number of scan lines in the total vertical period (see Figure 19).

VERTICAL SYNC WIDTH (8 Bits—R6[7,0])—Write only. Defines the duration of the Vertical Sync signal ($\overline{VS}$). This field should be programmed with the number of horizontal periods (scan lines) that compose the vertical synchronization pulse (see Figure 19).

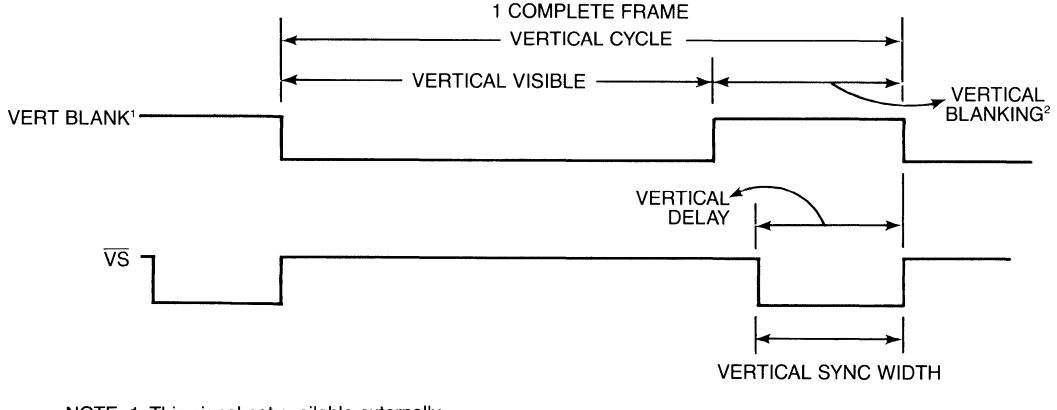
VERTICAL DELAY (8 Bits—R7[7,0])—Write only. Defines the delay between the beginning of the Vertical Sync signal and the end of the vertical blanking interval. This field should be programmed with N – 2 where N is the number of horizontal periods (scan lines) between the beginning of $\overline{VS}$ and the falling edge of vertical blanking (see Figure 19).

VERTICAL VISIBLE (12 Bits—R9[7,4], R8[7,0])—Write only. Defines the length of the visible portion of the total vertical period. This field should be programmed with N – 1 where N is the number of horizontal periods (scan lines) that the display is not blanked during the vertical period (see Figure 19).



NOTE: 1. This value is not programmed, however it can be calculated from the other programmed parameters.

FIGURE 18—VIEW HORIZONTAL TIMING



NOTE: 1. This signal not available externally.
2. This value is not programmed, however it can be calculated from the other programmed parameters.

FIGURE 19—VIEW VERTICAL TIMING

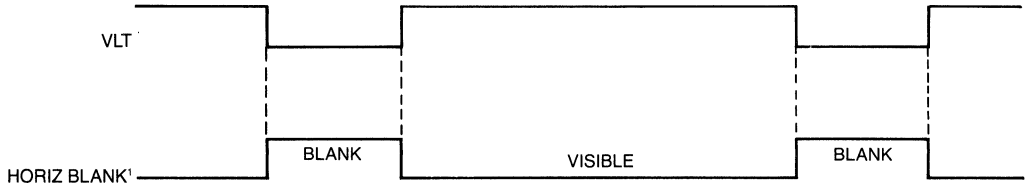
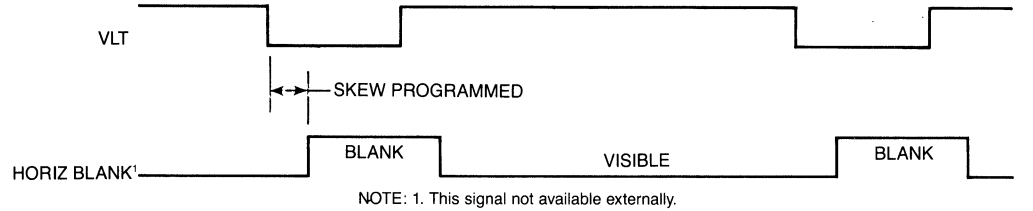


FIGURE 20a—HORIZONTAL TIMING: SKEW = 0



NOTE: 1. This signal not available externally.

FIGURE 20b—HORIZONTAL TIMING: SKEW ≠ 0

CURSOR CONTROL—

HORIZONTAL CURSOR DURATION (5 Bits—R11[4,0])—Write only.
Defines the active time per scan line of the Cursor (CURS) output pulse. This field should be programmed with the number of DCLK periods that the output is active high. The specific scan lines on which the CURS signal will be activated is determined by the contents of the Vertical Cursor Duration and Position fields. This parameter defines the width of the cursor rectangle on the screen.

VERTICAL CURSOR DURATION (9 Bits—R11[5], R12[7,0])—Write only.
Defines the active time per vertical period of the Cursor (CURS) output pulse. This field should be programmed with the number of scan lines that the output is active high. This parameter determines the height of the cursor rectangle on the screen.

HORIZONTAL CURSOR POSITION (8 Bits—R13[7,0], RR13[7,0])—Read/Write.
Defines the absolute horizontal coordinate relative to the visible portion of the screen when the Cursor (CURS) output will go active high. This field should be programmed with the X coordinate of the upper left corner of the cursor rectangle.

VERTICAL CURSOR POSITION (12 Bits—R14[7,4], R15[7,0], RR14[7,4], RR15[7,0])—Read/Write.
Defines the absolute vertical coordinate relative to the visible portion of the screen when the Cursor (CURS) output will go active high. This field should be programmed with the Y coordinate of the upper left corner of the cursor rectangle.

CURSOR SKEW (2 Bits—R11[7,6])—Write Only.
These bits define the number of DCLK periods that the CURS output signal is delayed (skewed) from the Display Memory Address corresponding to the cursor position. If zero skew is specified, the CURS output will be active when the VIEW generates the addresses in direct relation to the cursor position. The maximum cursor skew is three.

MISCELLANEOUS CONTROL—

BLANKING SKEW (2 Bits—R10[7,6])—Write only.
These bits define the number of DCLK periods that the horizontal blank component of the CBLANK signal is delayed (skewed) from the VLT signal as shown in Figure 20b. If, as shown in Figure 20a, zero skew is specified, the edges of the horizontal component of CBLANK will coincide with the edges of VLT. The maximum blanking skew is three.

WINDOW LIST START ADDRESS (5 Bits—R16[7,3])—Write only.
Defines the 5 MSB's of the memory address generated by the VIEW to access the Window List in system memory. This base address allows the VIEW to maintain up to 32 Window Lists in memory at the same time.

SCAN MODE (1 Bit—R4[2])—Write only.
Defines which scan mode will be used by the VIEW for generation of timing signals and Display Memory Addresses. If this bit is reset then non-interlaced mode (even and odd scan lines displayed sequentially in one field) will be used and if set then the interlaced mode (see Interlace Mode register) will be used.

INTERLACE MODE (1 Bit—R2[7])—Write only.
Defines which interlace mode will be used when the Scan Mode bit is set (R4[2] = 1). If this bit is reset (R2[7] = 0) then the normal interlaced mode is enabled which will cause the odd scan lines to be displayed in odd fields and even scan lines to be displayed in even fields. If this bit is set (R2[7] = 1) then the enhanced interlace mode is enabled which will cause the even and odd scan lines to be repeated on successive scan lines for both even and odd fields.

EXTERNAL SYNC ENABLE (2 Bits—R4[1,0])—Write only.
Defines whether sync outputs are generated internally or triggered by external signals. R4[1] defines the source of the Vertical Sync signal (R4[1] = 0 – internal, R4[1] = 1 – external). R4[0] defines the source of the Horizontal Sync signal (R4[0] = 0 – internal, R4[0] = 1 – external).

MEMORY REFRESH COUNT (4 Bits—R9[3,0])—Write only.

Defines how many sequential Display Memory addresses will be generated by VIEW for transparent refresh of dynamic RAM's during the horizontal retrace interval (when the VLT output is inactive low). Bit 3 is the MSB and bit 0 is the LSB. Setting these bits to zero will disable the refresh counter. These bits are reset by a hardware Reset or software Reset command.

START DELAY (6 Bits—R10[5,0])—Write only.

Defines the number of scan lines the VIEW will wait after accessing the Window List in system memory for the last break. The VIEW will not access the Window List again until this count expires at which time the VIEW will begin processing data again for the first break of the next frame refresh. Bit 5 is the MSB and bit 0 is the LSB. See section on Break Processing under Functional Description.

ATTRIBUTE SELECT (2 Bits—R17[1,0])—Write only.

Defines the functionality of the VIEW's ATTR7-4 general purpose Attribute output pins. The programming of these bits will determine whether these outputs function as attribute information or as extension bits to the Display Memory Address bus. See Table 3 for programming of these bits and the Functional Description section for an explanation of functions associated with these outputs.

VIEW OUTPUT	ATTRIBUTE SELECT R17[0] = 1	ATTRIBUTE SELECT R17[0] = 0
ATTR7 ATTR6	X ADDR EXT MSB X ADDR EXT LSB	GP ATTRIBUTE GP ATTRIBUTE
	R17[1] = 1	R17[1] = 0
ATTR5 ATTR4	Y ADDR EXT MSB Y ADDR EXT LSB	GP ATTRIBUTE GP ATTRIBUTE

ATTRIBUTE SELECT PROGRAMMING TABLE 3

INTERRUPT ENABLE (7 Bits—R17[7,5,4,3,2])—Write only.

These bits, when set, enable the VIEW to generate an interrupt when the appropriate conditions exist. These bits are reset to zero by a hardware Reset or a software Reset command. The following defines the specific conditions associated with each of the bits in this register.

Bit 7 (Interrupt Enable)
This bit, when set, will allow the VIEW to drive its INT pin high whenever the Interrupt Pending bit in the Interrupt Status 2 register goes high. When reset, the VIEW cannot drive the INT pin high. This bit is a global interrupt enable and has higher priority than the other enable bits in this register.

Bit 5 (Cursor Window Interrupt Enable)
This bit, when set, will allow the VIEW to set the Interrupt Pending bit after the last break has been processed whenever the cursor position (upper left corner of the cursor area) is moved into another window. When reset, this condition will be ignored.

Bit 4 (Y Break Interrupt Enable)
This bit, when set, will allow the VIEW to set the Interrupt Pending bit whenever a Y break with the Interrupt Tag bit set is encountered when generating Display Memory Addresses. The same interrupt will be generated for both even and odd fields. When reset, this condition will be ignored.

Bit 3 (Last Break Processed Interrupt Enable)
This bit, when set, will allow the VIEW to set the Interrupt Pending bit whenever the VIEW retrieves a Y break with a terminator window number followed by an X break with a terminator window number. When reset, this condition will be ignored.

Bit 2 (Vertical Retrace Interrupt Enable)
This bit, when set, will allow the VIEW to set the Interrupt Pending bit at the start of vertical blanking time. When reset, this condition will be ignored.

INTERRUPT STATUS 1 (5 Bits—RR17[6, 5, 4, 3, 2])—Read only.

These bits act as flags to indicate which condition/s are causing an interrupt. With the exception of bit 6 (Odd/Even status), these bits are reset by reading the Interrupt Status 1 register, a hardware Reset, or a software Reset command. They can only be driven active when they are enabled in the Interrupt Enable register. This register should not be read unless the Interrupt Pending bit in the Interrupt Status 2 register is high or the VIEW has driven its INT output active.

Bit 6 (Odd/Even)
This bit is set when the next field to be displayed is the odd field and is reset when the next field to be displayed is the even field. This status bit becomes valid shortly before the Vertical Retrace Interrupt occurs and remains valid for the vertical period.

Bit 5 (Cursor Window Interrupt)
This bit is set whenever the cursor position (upper left corner of the cursor area) is moved into a new window.

Bit 4 (Y Break Interrupt)
This bit is set during the retrace period preceeding the display of a window that has its Interrupt Tag bit set.

Bit 3 (Last Break Processed Interrupt)
This bit is set whenever the VIEW retrieves a Y break with a terminator window number followed by an X break with a terminator window number. The purpose of this condition is to indicate that the VIEW will not access system memory again until the Start Delay count has expired. This can be used to give the system processor an opportunity to access the window list in memory. See section on Break Processing under Functional Description.

Bit 2 (Vertical Retrace Interrupt)
This bit is set when the vertical retrace interval begins.

INTERRUPT STATUS 2 (8 Bits—RR18[7,0])—Read only.

Bit 7 (Interrupt Pending)
This bit is set when any of the enabled interrupt causing conditions has occurred. This bit is reset by reading the Interrupt Status 1 register, a hardware Reset, or a software Reset command.

Bit 6-0 (Cursor Window Number)
These bits represent the window number that the VIEW cursor is currently resident in. This is determined with respect to the location of the upper left corner of the cursor block as specified in the Horizontal and Vertical Cursor Position registers. Bit 6 is the MSB and bit 0 is the LSB. If the cursor is resident in more than one window, the window number with the highest priority is reported here. The data in this register is valid from the time the Last Break Processed Interrupt occurs until the Start Delay count expires.

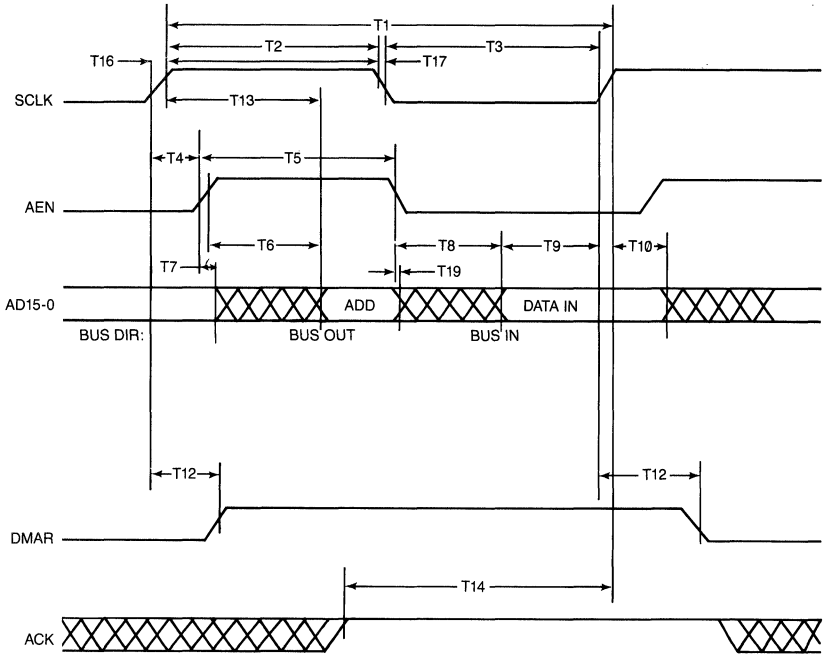


FIGURE 21—SYSTEM BUS MASTER TIMING

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to + 150°C
Lead Temperature (Soldering, 10 sec) ..... + 300°C
Positive voltage on any pin (WRT ground) ..... Vcc + 0.3V
Negative voltage on any pin (WRT ground) ..... -0.3V
Maximum Vcc ..... + 7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage:					
V_{IL}	Low			0.8	V	All inputs except DCLK, SCLK, and $\overline{CS}$
V_{IH}	High	2.0			V	
V_{IL}	Low			1.0	V	DCLK, SCLK, $\overline{CS}$ with $V_{CC} = 5.0V$
V_{IH}	High	4.0			V	See NOTE 1.
	Output voltage:					
V_{OL}	Low			0.4	V	$I_{OL} = 1.6$ mA
V_{OH}	High	2.4			V	$I_{OH} = -40$ μA
	Input leakage current:					
I_{IL}				10	μA	
I_{IH}				10	μA	
	Input/Output capacitance:					
C_{IN}				25	pF	All inputs
C_{OUT}				50	pF	All outputs
	Power supply current:					
I_{CC}				30	mA	

NOTES: 1. The V_{IH} MIN and V_{IL} MAX of SCLK, $\overline{CS}$, and DCLK are 80% and 20% of V_{CC} respectively.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	System Bus:					
T1	SCLK period	200		10,000	ns	
T2	SCLK high	70		5,000	ns	
T3	SCLK low	70		5,000	ns	
T16	SCLK rise time			10	ns	
T17	SCLK fall time			10	ns	
T4	SCLK to AEN delay	0			ns	
T5	AEN pulse width	50			ns	
T6	AEN active to address valid delay			50	ns	
T7	AEN high to AD bus drive delay	0			ns	
T8	AEN low to AD bus float delay			50	ns	
T9	Data valid to SCLK setup time	35			ns	
T10	Data hold time from SCLK high	0			ns	
T12	SCLK to DMAR delay			65	ns	
T13	SCLK rising edge to address valid delay	50			ns	
T14	ACK to SCLK setup	35			ns	
T19	Address hold from $\overline{\text{AEN}}$ low	0			ns	
T18	$\overline{\text{RESET}}$ pulse width	200			ns	
T60	$\overline{\text{CS}}$ read pulse width	125			ns	
T61	$\overline{\text{CS}}$ write pulse width	75			ns	
T62	$\overline{\text{CS}}$ active to data valid delay			75	ns	
T63	$\overline{\text{CS}}$ active to AD bus drive delay	0			ns	
T64	$\overline{\text{CS}}$ inactive to AD bus float delay			75	ns	
T65	Write data setup time to $\overline{\text{CS}}$ inactive	40			ns	
T66	Write data hold time from $\overline{\text{CS}}$ inactive	0			ns	
T67	R/$\overline{\text{W}}$ and A/$\overline{\text{D}}$ to $\overline{\text{CS}}$ active setup time	30			ns	
T68	R/$\overline{\text{W}}$ and A/$\overline{\text{D}}$ to $\overline{\text{CS}}$ active hold time	0			ns	
T69	$\overline{\text{CS}}$ rise time			10	ns	
T70	$\overline{\text{CS}}$ fall time			10	ns	
T71	$\overline{\text{CS}}$ inactive between processor access	200			ns	
T72	Data hold time from $\overline{\text{CS}}$ inactive	0			ns	
	Display Bus:					
T30	DCLK period	100		5,000	ns	
T31	DCLK high	40		2,500	ns	
T32	DCLK low	40		2,500	ns	
T43	DCLK rise time			10	ns	
T44	DCLK fall time			10	ns	
T33	DCLK high to signal[1] valid delay			75	ns	
T34	Signal[1] hold time to DCLK rising edge	0			ns	
T45	Ext $\overline{\text{VS}}$/$\overline{\text{HS}}$ active to DCLK rising edge setup time	35			ns	
T46	DCLK high to Ext $\overline{\text{VS}}$/$\overline{\text{HS}}$ inactive hold time	0			ns	

NOTE: 1. Signal refers to following—ATTR7-0, CURS, HDA7-0, VDA11-0, CBLANK, $\overline{\text{CYSN}}$, RFRSH, BRKCHG, VLT, INT, $\overline{\text{VS}}$ and $\overline{\text{HS}}$ ($\overline{\text{VS}}$ and $\overline{\text{HS}}$ only when programmed as outputs).

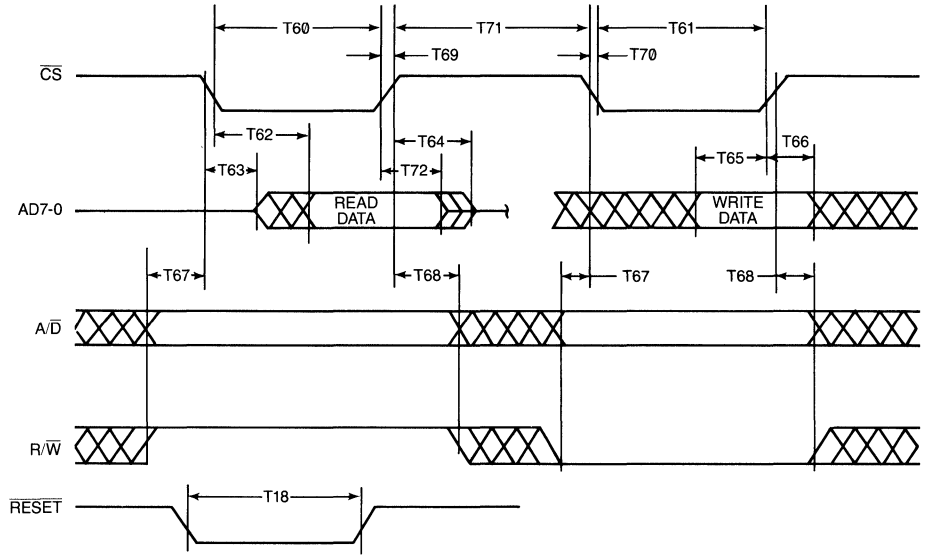
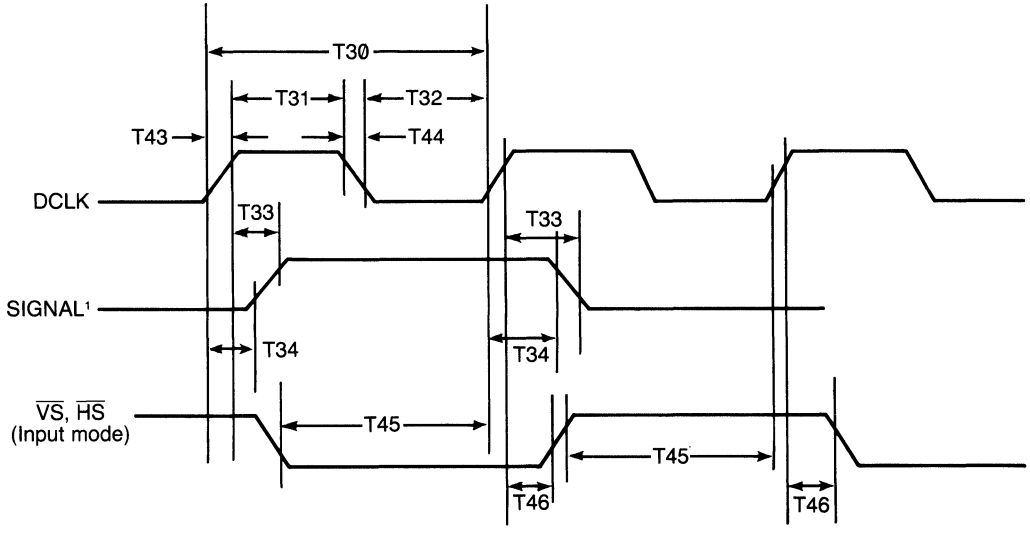


FIGURE 22—SYSTEM BUS PERIPHERAL TIMING



NOTE: [1] SIGNAL above refers to ATTR7-0, CURS, HDA7-0, VDA11-0, CBLANK, CSYN, RFRSH, BRKCHG, VLT, INT, VS and HS (VS and HS only when programmed as outputs).

FIGURE 23—DISPLAY BUS TIMING

Floppy Disk

Part Number	Software Compatability	Max. Recommended Disk Data Transfer Rate	Data Separator	Power Supply	Package	Page
FDC 9268	IBM® PC/AT®, PC/XT, PS/2®	500 Kb/sec	16 MHz Digital	+5V	40 DIP, 44 PLCC	541-556
FDC 9266	IBM® PC/AT®, PC/XT, PS/2®	250 Kb/sec	8 MHz Digital	+5V	40 DIP, 44 PLCC	525-540
FDC 765A, 765A-2, 7265	IBM® PC/AT®, PC/XT, PS/2®	500 Kb/sec	external	+5V	40 DIP, 44 PLCC	455-470
FDC 72C65, 72C66	IBM® PC/AT®, PC/XT, PS/2®	Up to 1 Mb/sec	external	+5V	40 DIP, 44 PLCC	473-496
FDC 92C81	IBM® PC/AT®, PC/XT, PS/2®	Up to 1 Mb/sec	Dual Gain Analog	+5V	24 DIP, 28 PLCC	557-564
FDC 91C36/B, 92C36/B	IBM® PC/AT®, PC/XT, PS/2®	250/500 Kb/sec	16 MHz Digital	+5V	8 DIP	497-500
FDC 92C38/B	IBM® PC/AT®, PC/XT, PS/2®	250/500/500/250 Kb/sec	16 MHz Digital	+5V	14 DIP	513-516
FDC 92C39/B/BT/T	IBM® PC/AT®, PC/XT, PS/2®	250/500/500/250 Kb/sec	16 MHz Digital	+5V	20 DIP, 28 PLCC	517-524
FDC 9229T/BT	IBM® PC/AT®, PC/XT, PS/2®	125/250 Kb/sec	8 MHz Digital	+5V	20 DIP, 28 PLCC	505-512
FDC 9216/B	IBM® PC/AT®, PC/XT, PS/2®	125/250 Kb/sec	8 MHz Digital	+5V	8 DIP	501-504
FDC 9791, 9793, 9795, 9797	179X	250 Kb/sec	external	+5V	40 DIP, 44 PLCC	565-566
FDC 1791, 1793, 1795, 1797	179X	250 Kb/sec	external	+5V, +12V	40 DIP, 44 PLC	471-472

STANDARD MICROSYSTEMS CORPORATION

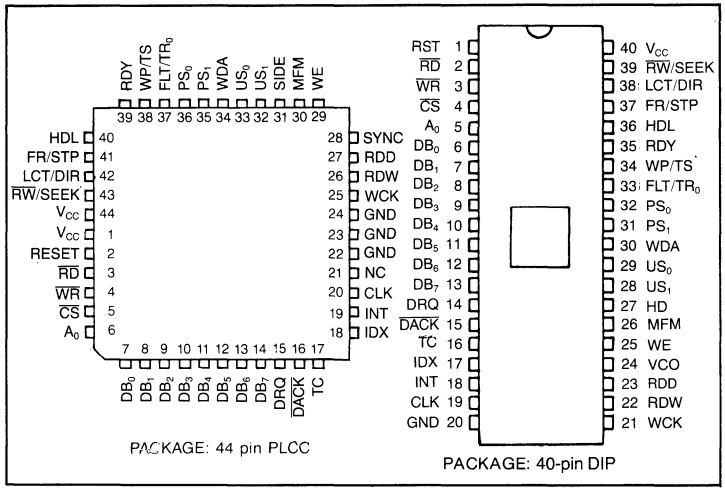
FDC765A/765A-2
FDC 7265/7265-2

Single/Double Density Floppy Disk Controller

FEATURES

- ☐ IBM Compatible in both Single and Double Density Recording Formats (FDC765A)
- ☐ Sony (EMCA) Compatible Recording Format (FDC7265)
- ☐ Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- ☐ Multi-Sector and Multi-Track Transfer Capability
- ☐ Drive up to 4 Floppy Disks
- ☐ Data Scan Capability—will scan a Single Sector or an entire cylinder's worth of data fields, comparing on a Byte by Byte Basis, data in the Processor's Memory with data read from the Diskette
- ☐ Data Transfers in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on up to four drives
- ☐ Compatible with Most Microprocessors
- ☐ Single Phase 8 MHz Clock
- ☐ Single +5 Volt Power Supply

PIN CONFIGURATION



- ☐ COMPLAMOS® n-Channel Silicon Gate Technology
- ☐ Available in 40-Pin Dual-in-Line Package

SECTION VI

GENERAL DESCRIPTION

The FDC765A is an LSI floppy disk controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The FDC765A provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The FDC7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppydisk® drive. The FDC7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The FDC7265 can read a diskette that has been formatted by the FDC765A.

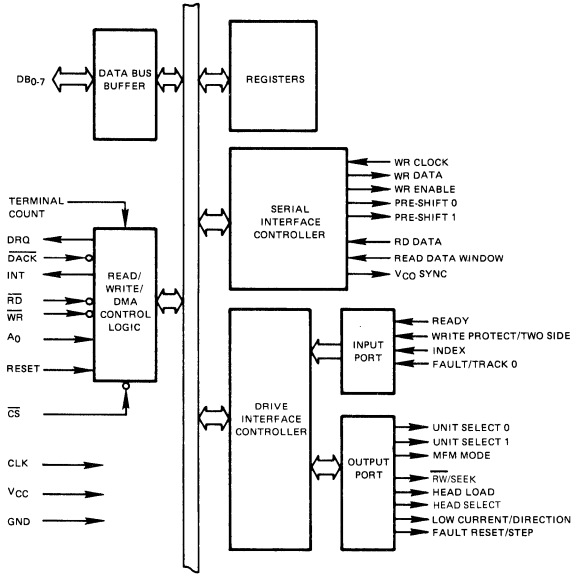
Each of these devices is also available in a -2 version. The -2 versions represent a reduction from 4-micron to 3-micron design rule. Functionally is the same. Minor differences between the two versions are detailed in the AC Characteristics table. The -2 versions are only available in the plastic package at this time.

Hand-shaking signals are provided in the FDC765A/FDC7265 which make DMA operation easy to incorporate with the aid of an external DMA controller chip. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

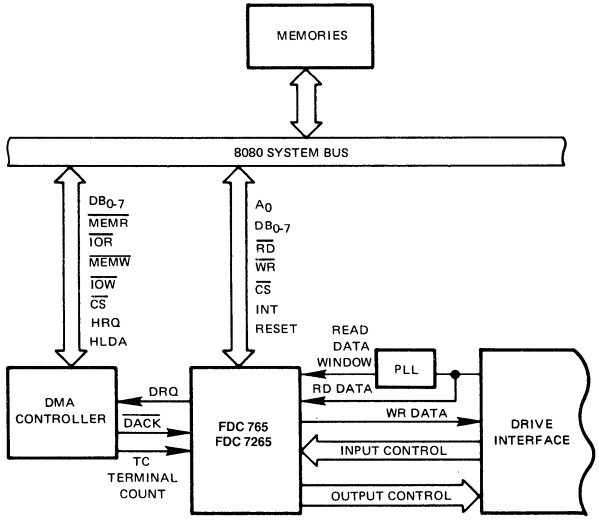
There are 15 commands which the FDC765A/FDC7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Format Track
Read Track	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
	Sense Drive Status

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The FDC765A/FDC7265 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.



BLOCK DIAGRAM



SYSTEM CONFIGURATION

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input①	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input①	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input①	Processor	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input① Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1."
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high). Head 2 selected when "0" (low).
28, 29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31, 32	PS_1, PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/ write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks $\geq$ 42 in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/ Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: ① Disabled when CS = 1.

DESCRIPTION OF INTERNAL REGISTERS

The FDC765A/7265 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC.

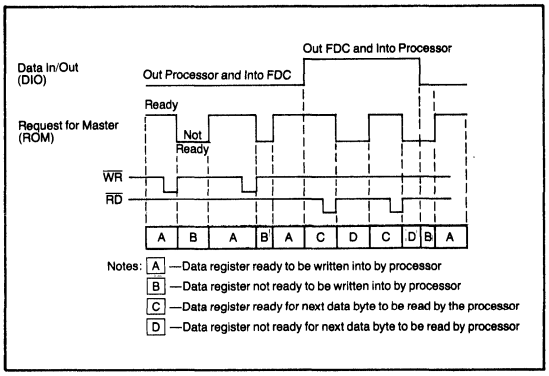
The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



COMMAND SEQUENCE

The FDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

INSTRUCTION SET ① ②

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

INSTRUCTION SET (CONT.)

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior
	W	———			H				———	Command execution
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after
	R	———			ST 1				———	Command execution
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after
	R	———			H				———	Command execution
	R	———			R				———	
	R	———			N				———	
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior
	W	———			H				———	Command execution
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after
	R	———			ST 1				———	Command execution
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after
	R	———			H				———	Command execution
	R	———			R				———	
	R	———			N				———	

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———			STO				———	Status information at the end
	R	———			PCN				———	of seek-operation about the FDC
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	——	SRT	——►				◄——	HUT	——
	W	———	HLT	——►					ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	———			ST 3				———	Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			NCN				———	
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	———			Invalid Codes				———	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	———			ST 0				———	ST 0 = 80 (16)

FUNCTIONAL DESCRIPTION OF COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

SECTION VI

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

Format	Sector Size	N	SC	GPL①	GPL②③
8″ Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode ④	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼″ Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode ④	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½″ Sony Micro Floppydisk®					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode ④	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Table 3

Notes: ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END	INTERRUPT CODE		
BITS 5	BIT 6	BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC765A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT			
NO.	NAME	SYMBOL	DESCRIPTION
D_7 D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	

BIT NO.	NAME	SYMBOL	DESCRIPTION
			STATUS REGISTER 1(CONT.)
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Errror	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
			STATUS REGISTER 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			STATUS REGISTER 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC is in the NON-DMA Mode, then the receipt of each data byte (if FDC is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The FDC contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the FDC to form the Command Phase, and are read out of the FDC in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC is ready for a new command.

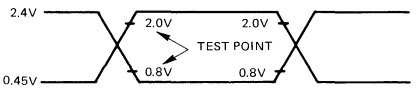
POLLING FEATURE OF THE FDC765A/7265

After the Specify command has been sent to the FDC, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

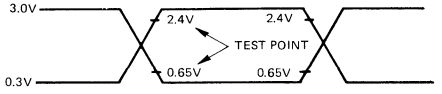
SECTION VI

AC TEST CONDITION

INPUT/OUTPUT



CLOCK



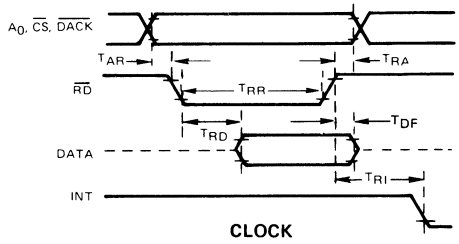
AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

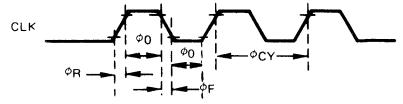
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

TIMING DIAGRAMS

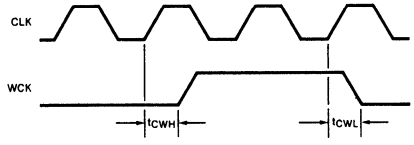
PROCESSOR READ OPERATION



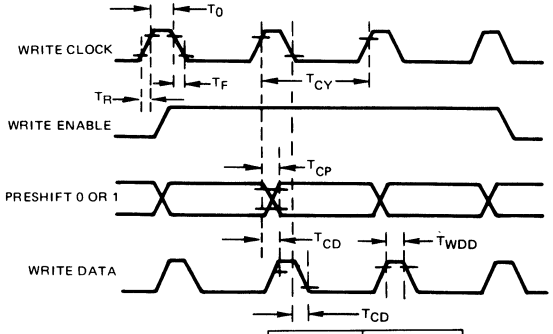
CLOCK



WRITE CLOCK



FDD WRITE OPERATION



	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −55°c to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −200 μA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\phi)}$	−0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				−10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = +0.45V

NOTE: ①Typical values for T_a = 25°C and nominal supply voltage.

CAPACITANCE T_a = 25°C; f_c = 1 MHz; V_{CC} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS $T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

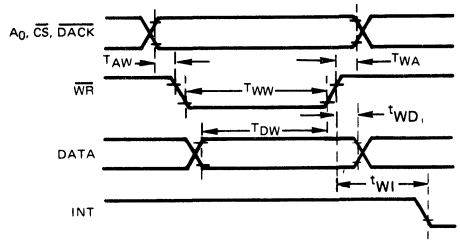
PARAMETER	SYMBOL	LIMITS 765A, 7265 MIN	TYP①	MAX	765A-2, 7265-2 MIN	TYP①	MAX	UNIT	TEST CONDITIONS
Clock Period	ϕ_{CY}	120	125	500	120	125	500	ns	
Clock Active (High, Low)	ϕ_0	40			40			ns	
Clock Rise Time	ϕ_r			20			20	ns	
Clock Fall Time	ϕ_f			20			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}\downarrow$	T_{AR}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}\uparrow$	T_{RA}	0			0			ns	
$\overline{RD}$ Width	T_{RR}	250			200			ns	
Data Access Time from $\overline{RD}\downarrow$	T_{RD}			200			140	ns	$C_L = 100$ pF
DB to Float Delay Time from $\overline{RD}\uparrow$	T_{DF}	20		100	10		85	ns	$C_L = 100$ pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}\downarrow$	T_{AW}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}\uparrow$	T_{WA}	0			0			ns	
$\overline{WR}$ Width	T_{WW}	250			200			ns	
Data Set Up Time to $\overline{WR}\uparrow$	T_{DW}	150			100			ns	
Data Hold Time from $\overline{WR}\uparrow$	T_{WD}	5			0			ns	
INT Delay Time from $\overline{RD}\uparrow$	T_{RI}			500			400	ns	
INT Delay Time from $\overline{WR}\uparrow$	T_{WI}			500			400	ns	
DRQ Cycle Time	T_{MCY}	13			13			µs	
DRQ Delay Time from $\overline{DACK}\downarrow$	T_{AM}			200			140	ns	
DRQ $\uparrow$ to $\overline{DACK}\downarrow$ Delay	T_{MA}	2			2			ϕ_{CY}	
$\overline{DACK}$ width	T_{AA}	2			2			ϕ_{CY}	
TC Width	T_{TC}	1			1			ϕ_{CY}	
Reset Width	T_{RST}	14			14			ϕ_{CY}	
WCK CYCLE TIME	T_{WCKCY}		16 8			16 8		ϕ_{CY}	MFM = 0 5¼″ MFM = 1 5¼″
			8 4			8 4			MFM = 0 8″ MFM = 1 8″
			8 4			8 4			MFM = 0 3½″ ⑤ MFM = 1 3½″ ⑤
			16 8			16 8			MFM = 0 3½″ ⑥ MFM = 1 3½″ ⑥
WCK Active Time (High)	T_0	80	250	350	80	250	350	ns	
CLK $\uparrow$ to WCK $\uparrow$ Delay	T_{CWH}	0		40	0		40	ns	
CLK $\uparrow$ to WCK $\downarrow$ Delay	T_{CWL}	0		40	0		40	ns	
WCK Rise Time	T_r			20			20	ns	
WCK Fall Time	T_f			20			20	ns	
Pre-Shift Delay Time from WCK $\uparrow$	T_{CP}	20		100	20		100	ns	
WDA Delay Time from WCK $\uparrow$	T_{CD}	20		100	20		100	ns	
RDD Active Time (High)	T_{RDD}	40			40			ns	
Window Cycle Time	T_{WCY}		2.0 1.0			2.0 1.0		µs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	15			15			ns	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK $\uparrow$	T_{US}	12			12			µs	
SEEK/$\overline{RW}$ Hold Time to LOW CURRENT/DIRECTION $\uparrow$	T_{SD}	7			7			µs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP $\uparrow$	T_{DST}	1.0			1.0			µs	8 MHz Clock Period
$US_{0,1}$ Hold Time from FAULT RESET/STEP $\uparrow$	T_{STU}	5.0			5.0			µs	
STEP Active Time (High)	T_{STP}	6.0	7.0	8.0	6.0	7.0	8.0	µs	
STEP Cycle Time	T_{SC}	33	③	③	33	③	③	µs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	8.0		10.0	µs	
Write Data Width	T_{WDD}	T_0-50			T_0-50			ns	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			15			µs	
Seek Hold Time from DIR	T_{DS}	30			30			µs	8 MHz Clock Period
DIR Hold Time after STEP	T_{STD}	24			24			µs	
Index Pulse Width	T_{IDX}	10			4			ϕ_{CY}	
$\overline{RD}\downarrow$ Delay from DRQ	T_{MR}	800			800			ns	
$\overline{WR}\downarrow$ Delay from DRQ	T_{MW}	250			250			ns	8 MHz Clock Period
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ $\uparrow$	T_{MRW}			12			12	µs	

NOTES: ① µ Typical values for $T_a = 25°C$ and nominal supply voltage.
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.
③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.
④ For mini-floppy applications, ϕ_{CY} must be 4 mHz.
⑤ Sony microfloppy 3½″ drive (8″ compatible).
⑥ Sony microfloppy 3½″ drive (5¼″ compatible).

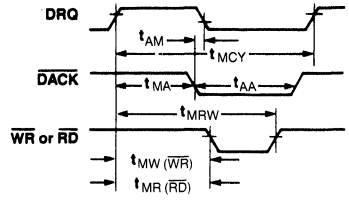
SECTION VI

TIMING DIAGRAMS

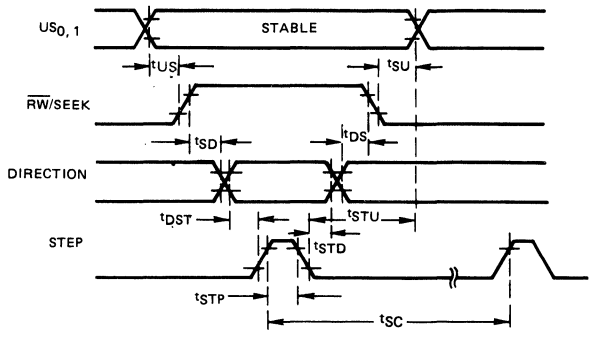
PROCESSOR WRITE OPERATION



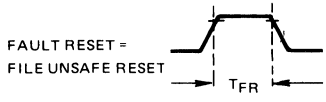
DMA OPERATION



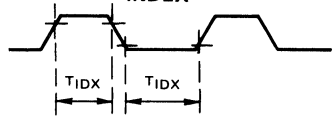
SEEK OPERATION



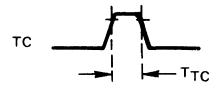
FLT RESET



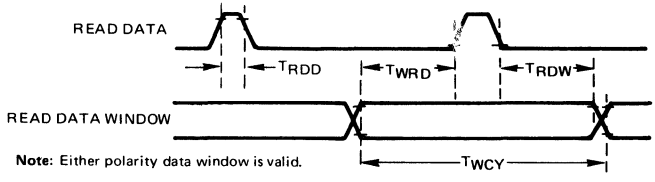
INDEX



TERMINAL COUNT

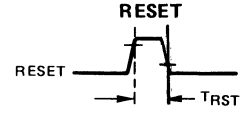


FDD READ OPERATION



Note: Either polarity data window is valid.

RESET



STANDARD MICROSYSTEMS CORPORATION

FDC 1791-02
FDC 1792-02
FDC 1793-02
FDC 1794-02
FDC 1795-02
FDC 1797-02

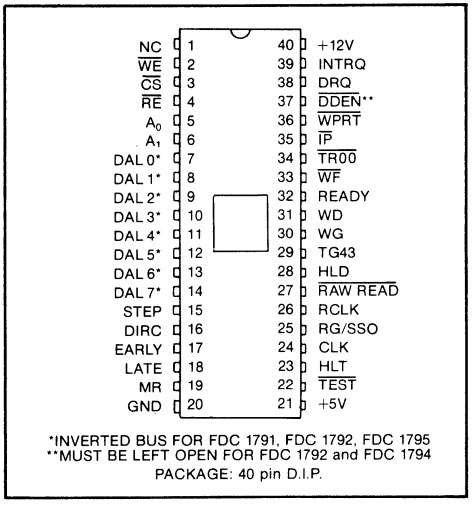
Floppy Disk Controller/Formatter FDC

μPC FAMILY

FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1795, FDC 1797)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



*INVERTED BUS FOR FDC 1791, FDC 1792, FDC 1795
**MUST BE LEFT OPEN FOR FDC 1792 and FDC 1794
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into six specific parts: FDC 1791, FDC 1792, FDC 1793, FDC 1794, FDC 1795, and the FDC 1797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The FDC 1792 operates in the single density mode only. Pin 37 (DDEN) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses. The FDC 1795 adds side select logic to the FDC 1791. The FDC 1797 adds the side select logic to the FDC 1793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

SECTION VI

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

FDC72C65/66

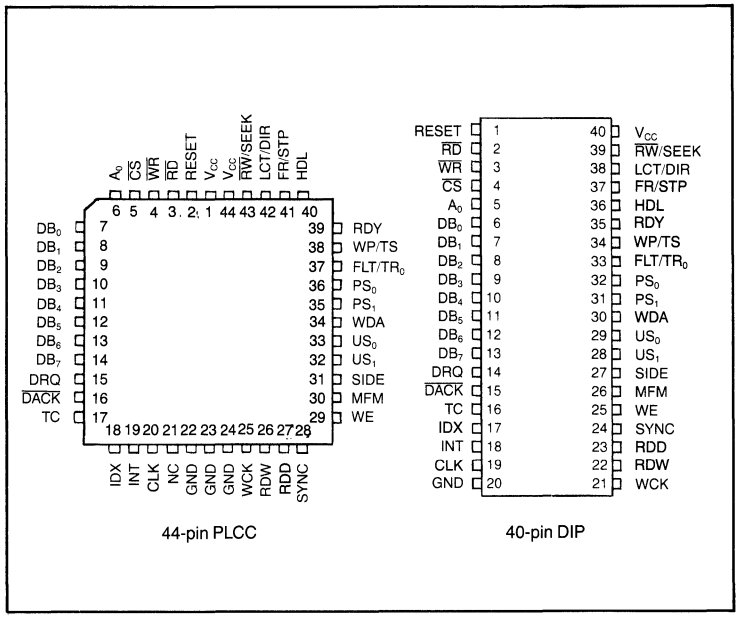
PRELIMINARY

Single/Double Density Floppy Disk Controller

FEATURES

- ☐ IBM-compatible format (single, double and quad density) (FDC72C65)
- ☐ Sony (EMCA)-compatible recording format (FDC72C66)
- ☐ Multi-sector and multi-track transfer capability
- ☐ Drive Up to 4 floppy or micro floppydisk drives
- ☐ Data scan capability–will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Programmable stepping rate, head load and head unload times
- ☐ Parallel seek operations on up to four drives
- ☐ Compatible with μPD8080/85, μPD8086/88, μPD80186/286/386 and Z80® microprocessors
- ☐ Single-phase clock 8 MHz (standard floppy) or 4 MHz (minifloppy)
- ☐ CMOS technology
- ☐ Single +5V ±10% power supply.

PIN CONFIGURATION



44-pin PLCC

40-pin DIP

GENERAL DESCRIPTION

The FDC72C65 is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The FDC 72C65 provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The FDC72C66 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppy-disk® drive. The FDC72C66 is pin-compatible and electrically equivalent to the 72C65 but utilizes the Sony recording format. The FDC72C66 can read a diskette that has been formatted by the FDC72C65.

Hand-shaking signals are provided in the FDC72C65/FDC72C66 which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

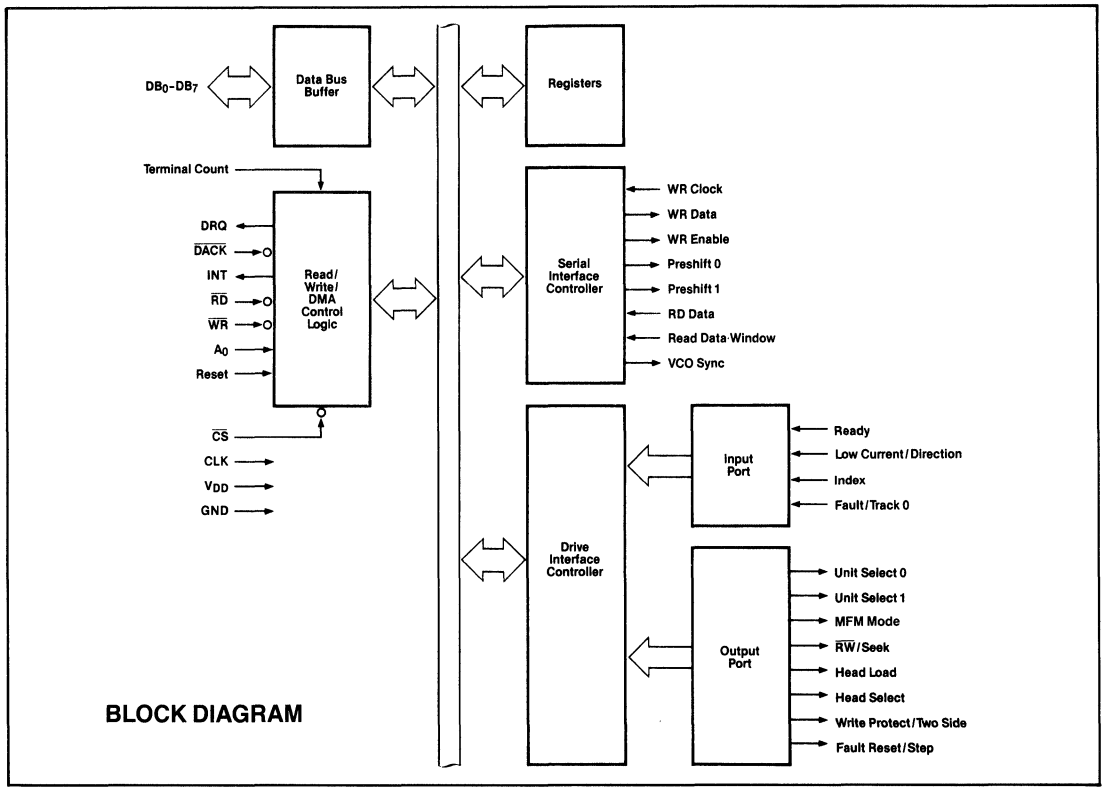
The FDC is designed using CMOS technology. In addition to a low normal operating current, a standby mode can be software-enabled to provide minimal current drain when the FDC is not in use.

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The FDC72C65/FDC72C66 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

There are 18 commands which the FDC72C65/FDC72C66 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Format Track
Read Track	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
Set Standby	Sense Drive Status
Reset Standby	Software Reset

SECTION VI



BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
1	RESET	Reset	Input	Processor	A high input places the FDC72C65/72C66 in standby mode and sets drive interface outputs to low level (except PS_0, PS_1, and WDATA). In the main system, INT and DRQ are set to low level, and DB_0-DB_7 are set as inputs.
2	$\overline{RD}$	Read control	Input	Processor	The $\overline{RD}$ input allows the transfer of data from the FDC to the data bus when low. Disabled when $\overline{CS}$ is high.
3	$\overline{WR}$	Write control	Input	Processor	The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.
4	$\overline{CS}$	Chip select	Input	Processor	The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$, $\overline{WR}$, and A_0.
5	A_0	Data or status select	Input	Processor	The A_0 input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be sent to the data bus.
6-13	DB_0-DB_7	Bidirectional data bus	Input Output	Processor	DB_0-DB_7 are a bidirectional three-state 8-bit data bus. Disabled when $\overline{CS}$ is high.
14	DRQ	DMA request	Output	DMA	The FDC asserts the DRQ output high to request a DMA transfer.
15	$\overline{DACK}$	DMA acknowledge	Input	DMA	When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.
16	TC	Terminal count	Input	DMA	When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
17	IDX	Index	Input	FDD	The IDX input goes high at the beginning of a disk track.
18	INT	Interrupt request	Output	Processor	The INT output is FDC's interrupt request.
19	CLK	Clock	Input	Clock	CLK is the input for the FDC's single-phase, 8 MHz (standard floppy) or 4 MHz (mini floppy) clock.
20	GND	Ground			Ground.
21	WCK	Write clock	Input	Data Separator or Clock Generator	The WCK input sets the data read and write rate. Synchronize the rising edge of WCK with the rising edge of CLK. FM = 16 CLK cycles; MFM = 8 CLK cycles.
22	RDW	Read data window	Input	Phase Lock Loop	The RDW input is generated by the VFO circuit. It is used to sample clock and data bits of RDD.
23	RDD	Read data	Input	FDD	The RDD input is the read data from the FDD, containing clock and data bits. Input RDD and RDW during a data read, or the FDC will enter a deadlock state.
24	SYNC	VCO sync	Output	Phase Lock Loop	SYNC outputs the functional mode of the FDC. A high output indicates read and a low output inhibits read.
25	WE	Write enable	Output	FDD	The WE output enables write data into the FDD.
26	MFM	MFM	Output	Phase Lock Loop	The MFM output shows the FDC's mode. It is high for MFM, low for FM.
27	SIDE	Side select	Output	FDD	Head 1 is selected when the SIDE output is 1 (high), head 0 is selected when SIDE is 0 (low).
28, 29	US_0, US_1	FDD unit select	Output	FDD	The US_0 and US_1 outputs select the floppy disk drive unit.
30	WDA	Write data	Output	FDD	WDA is the serial clock and data output to the FDD.
31, 32	PS_0, PS_1	Preshift	Output	FDD	The PS_0 and PS_1 outputs are the write precompensation status for MFM mode. They determine early, late, and normal times.
33	FLT/TR_0	Fault/track zero	Input	FDD	In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TR_0 detects track 0.
34	WP/TS	Write protect/two side	Input	FDD	In the read/write mode, the WP input senses write protected status. In the seek mode, TS senses two-sided media.
35	RDY	Ready	Input	FDD	The RDY input indicates that the FDD is ready to receive.
36	HDL	Head load	Output	FDD	The HDL output is the command which causes the read/write head in the FDD to contact the diskette.
37	FR/STP	Fault reset/step	Output	FDD	In the read/write mode, the FR output resets the fault flip-flop in the FDD. In the seek mode, STP outputs step pulses to move the head to another cylinder. A fault reset pulse (FR) is issued at the beginning or each Read or Write command prior to the HDL signal.
38	LCT/DIR	Low current/direction	Output	FDD	When RW/SEEK specifies RW, this output becomes LCT, indicating the read/write head of the drive is selecting a cylinder beyond the 43rd cylinder. When RW/SEEK specifies SEEK, this pin becomes DIR, specifying the direction of the seek operation. A low signal indicates output and a high signal indicates input.
39	$\overline{RW}$/ SEEK	Read/write/seek	Output	FDD	The $\overline{RW}$/SEEK output specifies the read/write mode when low, and the seek mode when high.
40	V_{CC}	DC power		Power Supply	+5V power supply.

Internal Registers

The FDC72C65/FDC72C66 contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0-ST3, in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and FDC72C65/FDC72C66.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in table 1.

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the main status register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC busy) goes low is 12 μs. See figure 1.

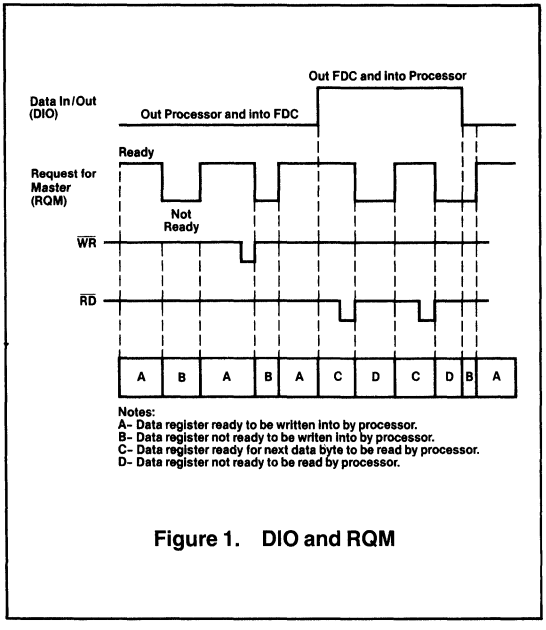


Figure 1. DIO and RQM

Table 1. Status/Data Register Addressing

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read main status register
0	1	0	Reset commands
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from data register
1	1	0	Write into data register

The bits in the main status register are defined in table 2.

Table 2. Main Status Register

Pin No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_4	CB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB_6	DIO (Data Input/ Output)	Indicates direction of data transfer between the processor and data register. If DIO = 1, then transfer is from data register to the processor. If DIO = 0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

Table 3. Status Register Identification

Pin No.	Pin Name	Symbol	Function
			Status Register 0
D_7, D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal termination of command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
			D_7 = 1 and D_6 = 0 Invalid command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at interrupt.
D_1	Unit Select 1	US_1	This flag is used to indicate a drive unit number at interrupt.
D_0	Unit Select 0	US_0	This flag is used to indicate a drive unit number at interrupt.
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit is always 0 (low).
D_2	No Data	ND	During execution of Read Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
			During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the Read A Cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the data address mark or deleted data address mark, this flag is set. Also at the same time, the MD (missing address mark in data field) of status register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Status Register 3			
D_7	Fault	FT	This bit is used to indicate the status of the fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	Two-Side	TS	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the side select signal to the FDD.
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Note:

(1) CRC = Cyclic Redundancy Check

(2) IDR = Internal Data Register

(3) Cylinder (C) is described more fully in the Command Symbol Description.

Standby Mode

The FDC72C65/FDC72C66 can be placed in a low-power standby mode by issuing the SET STANDBY command. During standby mode, the main status register will contain all zeros. After standby mode is disabled, RQM (Request for Master) in the main status register will be set to 1, indicating that the FDC72C65/72C66 is available for use. During standby mode, it is only necessary to maintain clock on pin 19. All disk control signals will be inactive.

To further reduce system power dissipation, it is possible to stop the clock on pin 19 as well by the following procedure.

(1) Issue SET STANDBY command.

(2) Wait for 32 clock periods, minimum.

(3) The clock may then be stopped.

To resume normal operation, the clock must be re-started. After 24 clock periods, the RESET STANDBY command may be issued.

All internal registers and I/O ports are held constant. V_{DD} must be maintained at normal levels.

Command Sequence

The FDC72C65/FDC72C66 is capable of performing 18 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the FDC72C65/FDC72C66 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbreviations used in table are given in the Command Symbol Description table.

NOTES:

Command Symbol Description

Pin		Function
Name	**Symbol**	
Address Line 0	A_0	A_0 controls selection of main status register (A_0 = 0) or data register (A_0 = 1).
Cylinder Number	C	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
Data	D	D stands for the data pattern which is going to be written into a sector.
Data Bus	D_7-D_0	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
Data Length	DTL	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
End of Track	EOT	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
Gap Length	GPL	GPL stands for the length of gap 3. During Read/Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
Head Address	H	H stands for head number 0 or 1, as specified in ID field.
Head	HD	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
Head Load Time	HLT	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments.)
Head Unload Time	HUT	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments.)
FM or MFM Mode	MF	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
Multitrack	MT	If MT is high, a multitrack operation is performed. If MT = 1 after finishing read/write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
Number	N	N stands for the number of data bytes written in a sector.
New Cylinder Number	NCN	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
Non-DMA Mode	ND	ND stands for operation in the non-DMA mode.
Present Cylinder Number	PCN	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
Record	R	R stands for the sector number which will be read or written.
Read/Write	R/W	R/W stands for either Read (R) or Write (W) signal.
Sector	SC	SC indicates the number of sectors per cylinder.
Skip	SK	SK stands for skip deleted data address mark.
Step Rate Time	SRT	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
Status 0-3	ST0-ST3	ST0-ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contains information relevant to that particular command.
	STP	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
Unit Select	US_0, US_1	US stands for a selected drive number 0 or 1.

NOTES:

Table 4. Instruction Set

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command
	W	←				H			→	execution. The 4 bytes are compared against
	W	←				R			→	header on floppy disk.
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execu-
	W	←				H			→	tion. The 4 bytes are compared against header on
	W	←				R			→	floppy disk.
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execu-
	W	←				H			→	tion. The 4 bytes are compared against header on
	W	←				R			→	floppy disk.
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the main system and FDD
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	←			ST0				→	Status information about the FDC at the end of
	R	←			PCN				→	seek operation
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	←	SRT	→	←	HUT	→			
	W	←		HLT		→	ND			
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←			ST3				→	Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			NCN				→	
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	←			Invalid Codes				→	Invalid Command codes (No op—FDC goes into standby state)
Result	R	←			ST0				→	ST0 = 80H
Set Standby										
Command	W	0	0	1	1	0	1	0	1	Command codes
Execution										Enter standby mode
Reset Standby										
Command	W	0	0	1	1	0	1	0	0	Command codes
Execution										Disable standby mode
Software Reset										
Command	W	0	0	1	1	0	1	1	0	Command codes
Execution										Same as hardware reset
Read a Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information read during execution phase from floppy disk.
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Format a Track										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				N			→	Bytes/sector
	W	←				SC			→	Sectors/track
	W	←				GPL			→	Gap 3
	W	←				D			→	Filler byte
Execution										FDC formats an entire track.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	In this case, the ID information has no meaning
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				STP			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:

(1) In the Instruction Code, X = don't care (usually set to 0).

(2) A_0 should be 0 for SET STANDBY, RESET STANDBY, and SOFTWARE RESET commands and 1 for all other commands.

NOTES:

System Configuration

Figure 2 shows an example of a system using a FDC72C65/FDC72C66.

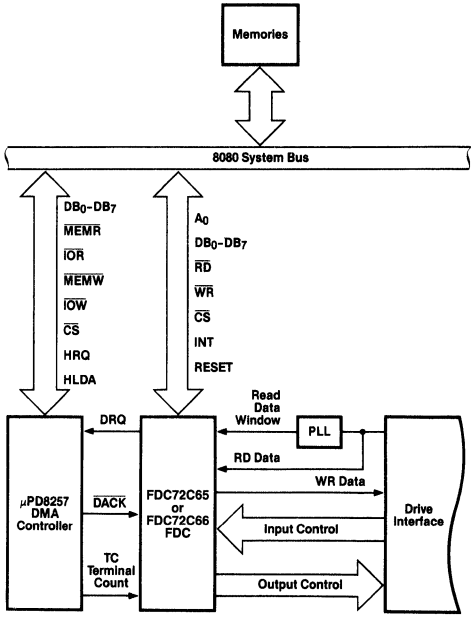


Figure 2. System Configuration

Processor Interface

During command or result phases the main status register (described earlier) must be read by the processor before each byte of information is written into or read from the data register. After each byte of data is read or written to the data register, the CPU should wait for 12μs before reading the main status register. Bits D_6 and D_7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the FDC72C65/FDC72C66. Many of the commands require multiple bytes and, as a result, the main status register must be read prior to each byte transfer to the FDC72C65/FDC72C66. On the other hand, during the result phase, D_6 and D_7 in the main status register must both be 1's ($D_6 = 1$ and $D_7 = 1$) before reading each byte from the data register. Note that this reading of the main status register before each byte transfer to the FDC72C65/FDC72C66 is required only in the command and result phases, and *not* during the execution phase.

During the execution phase, the main status register need not be read. If the FDC72C65/FDC72C66 is in the non-DMA mode, then the receipt of each data byte (if FDC72C65/FDC72C66 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a read signal ($\overline{RD} = 0$) or write signal ($\overline{WR} = 0$) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the main status register and bit D_7 (RQM) functions as the interrupt signal. If a write command is in the process then the $\overline{WR}$ signal negates the reset to the interrupt signal.

Note that in the non-DMA mode it is necessary to examine the main status register to determine the cause of the interrupt, since it could be a data interrupt of a command termination interrupt, either normal or abnormal.

If the FDC72C65/FDC72C66 is in the DMA mode, no interrupts are generated during the execution phase. The FDC72C65/FDC72C66 generates DRQs (DMA requests) when each byte of data is available. The DMA controller responds to this request with both a $\overline{DACK} = 0$ (DMA acknowledge) and an $RD = 0$ (read signal). When the DMA acknowledge signal goes low ($\overline{DACK} = 0$), then the DMA request is cleared ($DRQ = 0$). If a write command has been issued, then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the execution phase has been completed (terminal count has occurred) or the EOT sector read/written, then an interrupt will occur (INT = 1). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

It is important to note that during the result phase all bytes shown in the instruction set (table 4) must be read. The read data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The FDC72C65/FDC72C66 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

The FDC72C65/FDC72C66 contains five status registers. The main status register mentioned above may be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the FDC72C65/FDC72C66 to form the command phase and are read out of the FDC72C65/FDC72C66 in the result phase must occur in the order shown in table 4. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the FDC72C65/FDC72C66, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the FDC72C65/FDC72C66 is ready for a new command.

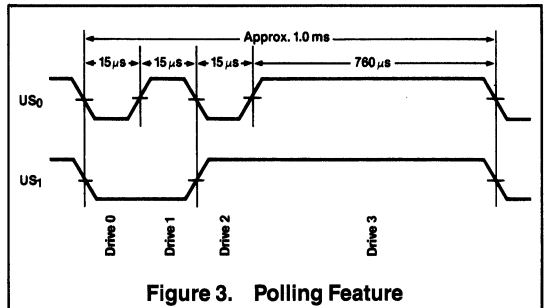


Figure 3. Polling Feature

Polling

After reset has been sent to the FDC72C65/FDC72C66, the unit select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the FDC72C65/FDC72C66 polls all four FDDs looking for a change in the ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the FDC72C65/FDC72C66 will generate an interrupt. When status register 0(ST0) is read (after Sense Interrupt Status is issued), not ready (NR) will be indicated. The polling of the ready line by the FDC72C65/FDC72C66 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms. See figure 3.

Read Data

A set of nine (9) byte words are required to place the FDC into the read data mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID address marks and ID fields. When the current sector number (R) stored in the ID register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the sector number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a multi-sector read operation. The Read Data command may be terminated by the receipt of a terminal count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (cyclic redundancy count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 5 shows the transfer capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTl defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus. The FDC reads (internally) the complete sector performing the CRC check and, depending upon the manner of command termination, may perform a multi-sector read operation. When N is non-zero, then DTL has no meaning and should be set to FFH.

At the completion of the Read Data command, the head is not unloaded until after head unload time interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the index hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No data) flag in status register 1 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

After reading the ID and data fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (data error) flag in status register 1 to a 1 (high), and if a CRC error occurs in the data field, the FDC also sets the DD (data error in data field) flag in status register 2 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

If the FDC reads a deleted data address mark off the diskette, and the SK bit (bit D_5 in the first command word) is not set (SK = 0), then the FDC sets the CM (control mark) flag in status register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the deleted data address mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27μs in the FM mode, and every 13μs in the MFM mode, or the FDC sets the OR (Overrun) flag in status register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Table 6 shows the values for C, H, R, and N, when the processor terminates the command.

Functional Description of Commands

Write Data

A set of nine (9) bytes is required to set the FDC into the write data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C,H,R,N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD. See table 6.

After writing data into the current sector, the sector number stored in R is incremented by one, and the next data field is written into. The FDC continues this multisector write operation until the issuance of a terminal count signal. If a terminal count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the terminal count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at side 0
0	1	01	(256) (26) = 6,656	or 26 at side 1
1	0	00	(128) (52) = 6,656	26 at side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at side 0
0	1	02	(512) (15) = 7,680	or 15 at side 1
1	0	01	(256) (30) = 7,680	15 at side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at side 0
0	1	03	(1024) (8) = 8,192	or 8 at side 1
1	0	02	(512) (16) = 8,192	8 at side 1
1	1	03	(1024) (16) = 16,384	

Table 6. Command Description

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=01	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=01	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=1	NC

Note: (1) NC (No Change): The same value as the one at the beginning of command execution.

(2) LSB (Least Significant Bit): The least significant bit of H is complemented.

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (end of cylinder) flag
- ND (no data) flag
- Head unload time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the write data mode, data transfers between the processor and FDC, via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the OR (overrun) flag in status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Write Deleted Data

This command is the same as the Write Data command except a deleted data address mark is written at the beginning of the data field instead of the normal data address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a data address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in status register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the data address mark and reads the next sector.

Read a Track

This command is similar to the Read Data command except that this is a continuous read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID address mark on the diskette after it senses the index hole for the second time, it sets the MA (missing address mark) flag in status register 1 to a 1 (high) and terminates the command. (Status register 0 has bits 7 and 6 set to 0 and 1, respectively).

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the

first ID field it is able to read. If no proper ID address mark is found in the diskette before the index hole is encountered for the second time, then the MA (missing address mark) flag in status register 1 is set to a 1 (high), and if no data is found then the ND (No data) flag is also set in status register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in status register 0 set to 0 and 1, respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format a Track command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; gaps, address marks, ID fields, and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format, are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number), and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C,H,R, and N to the FDC72C65/FDC72C66 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R reg-

Table 7. Sector Size

Format	Sector Size	N	SC	GPL (1)	GPL (2,3)
8″ Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode (Note 4)	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼″ Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode (Note 4)	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½″ Sony Micro Floppydisk					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode (Note 4)	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Note:

(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.

(2) Suggested values of GPL in format command.

(3) All values except sector size are hexidecimal.

(4) In MFM mode FDC cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00).

ister are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a fault signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of status register 0 to 0 and 1, respectively. Also, the loss of a ready signal at the beginning of a command execution phase causes bits 7 and 6 of status register 0 to be set to 0 and 1, respectively.

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP→R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (scan hit) flag of status register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (scan not satisfied) flag of status register 2 to a 1 (high) and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 8 shows the status of bits SH and SN under various conditions of Scan.

Table 8. Scan Conditions

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a deleted data address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (control mark) flag of status register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the deleted address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (control mark) flag of status register 2 to a 1 (high) in order to show that a deleted sector has been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (overrun) flag set in status register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an overrun occurs, the FDC ends the command with bits 7 and 6 of status register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent present cylinder registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (present cylinder number) which is the current head position with the NCN (new cylinder number), and if there is a difference, performs the following operations:

PCN<NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step in)

PCN>NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step out)

The rate at which step pulses are issued is controlled by SRT (stepping rate time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (seek end) flag is set in status register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $D_0B - D_3B$ in the main status register are set during the seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the seek operation the FDC is in the FDC busy state, but during the execution phase it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the NR (not ready) flag is set in status register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

If the time to write three bytes of Seek command exceeds 150 μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the track 0 signal from the FDD. As long as the track 0 signal is low, the direction signal remains 0 (low) and step pulses are issued. When the track 0 signal goes high, the SE (seek end) flag in status register 0 is set to a 1 (high) and the command is terminated. If the track 0 signal is still low after 256 step pulses have been issued, the FDC sets the SE (seek end) and EC (equipment check) flags of status register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

The ability to do overlapping Recalibrate commands to multiple FDDs and the loss of the ready signal, as described in the Seek command, also applies to the Recalibrate command.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

(1) Upon entering the result phase of:
  (a) Read Data command
  (b) Read a Track command
  (c) Read ID command
  (d) Read Deleted Data command
  (e) Write Data command
  (f) Format a Cylinder command
  (g) Write Deleted Data command
  (h) Scan commands
(2) Ready line of FDD changes state
(3) End of Seek or Recalibrate command
(4) During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, DB_5 in the main status register is high. Upon entering the result phase this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by reading/writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and, via bits 5, 6, and 7 of status register 0, identifies the cause of the interrupt. See table 9.

Table 9. Interrupt Status

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready line changed state, either polarity
1	0	0	Normal termination of Seek or Recalibrate command
1	1	0	Abnormal termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the FDC72C65/FDC72C66 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be seek end or a change in ready status from one of the drives. A graphic example is shown in figure 4.

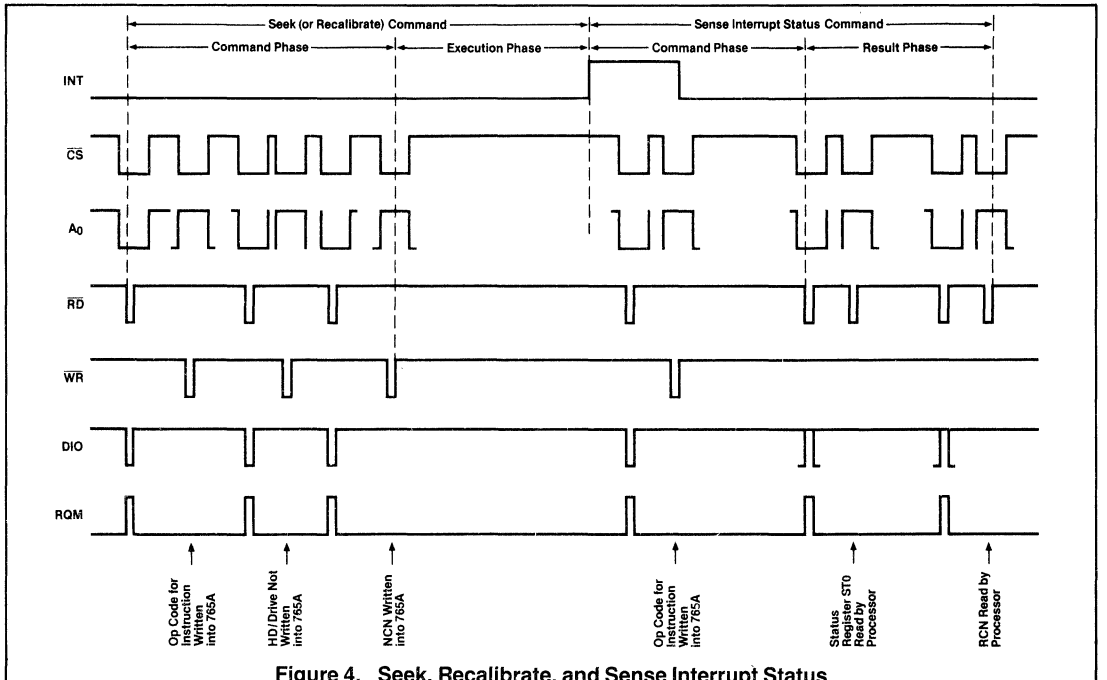


Figure 4. Seek, Recalibrate, and Sense Interrupt Status

Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (head unload time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OFH = 240 ms). The SRT (step rate time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (head load time) defines the time between when the head load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock was reduced to 4 MHz (minifloppy application), then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (non-DMA) bit. When this bit is high (ND = 1) the non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status register 3 contains the drive status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of status register 0 are set to 1 and 0, respectively. No interrupt is generated by the FDC72C65/FDC72C66 during this condition. Bits 6 and 7 (DIO and RQM) in the main status register are both 1 (high), indicating to the processor that the FDC72C65/FDC72C66 is in the result phase and the contents of status register 0 (ST0) must be read. When the processor reads status register 0 it will find an 80H, indicating an invalid command was received.

A Sense Interrupt Status command must be sent after a seek or recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid command. In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or no operation state.

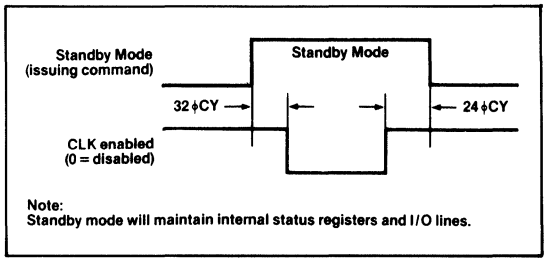
CMOS Reset Commands

Commands that are available in the FDC72C65/FDC72C66 which are enhancements over the FDC765A/FDC7265 are the CMOS reset commands. They are initiated as follows:

	AO	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Set standby	0	1	0	0	0	1	1	0	1	0	1
Reset standby	0	1	0	0	0	1	1	0	1	0	0
Software reset	0	1	0	0	0	1	1	0	1	1	0

The software reset command is identical to the hardware reset described previously.

The set standby command reduces power consumption (P_D) from 10mW to 10μW. Pin 19 (CLK) must be active when setting or resetting standby mode. All other clocks (i.e. WCK, etc.) can be inactive. The supply voltage must be maintained at 5 V during standby. The clock to pin 19 may be disabled during standby provided the following set-up and hold conditions are met:



Note:
Standby mode will maintain internal status registers and I/O lines.

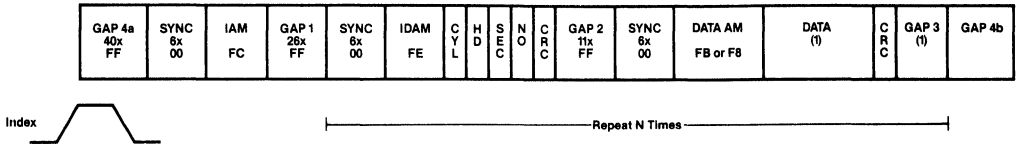
Differences Between the FDC72C65/72C66 and FDC765A/7265

Parameter	FDC72C65	FDC72C66	FDC765A	FDC7265
Track format	IBM	ECMA/ISO	IBM	EMCA/ISO
Tracks to be recalibrated	255		77	255
Skipping time after detection of index pulses	0.2ms (at 4 MHz)		about 1.2 ms (at 4 MHz)	about 0.2 ms (at 4 MHz)
DRQ ↑ $\overline{RD}$ ↓ TE response time	125 ns at 4MHz 250 ns at 8MHz		0.8 μs 1.6 μs	
FDD response latency after unit select signal output	2.5μs at 4MHz 5.0μs at 8MHz		0.5μs 1.0μs	
Multitrack write by tunnel erase head	Yes		No	
Standby function (standby command)	Yes		No	
Software reset command	Yes		No	

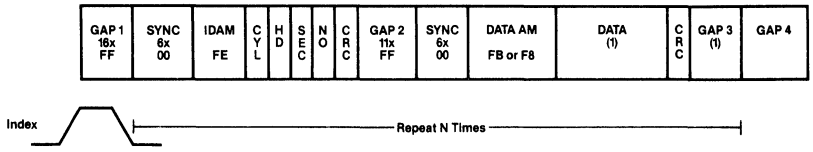
Data Format

Figure 5 shows the data transfer format for the FDC72C65 and FDC72C66 in various modes.

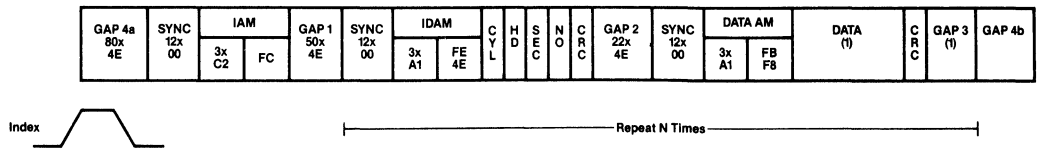
FDC72C65 (FM Mode)



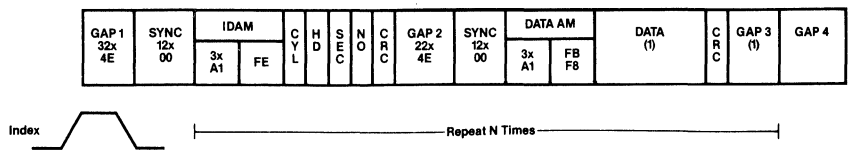
FDC72C66 (FM Mode)



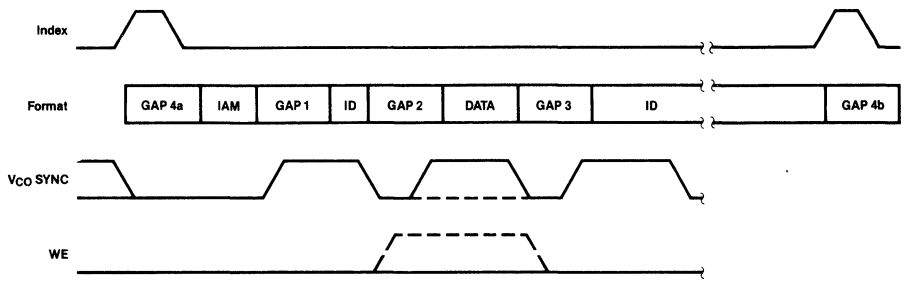
FDC72C65 (MFM Mode)



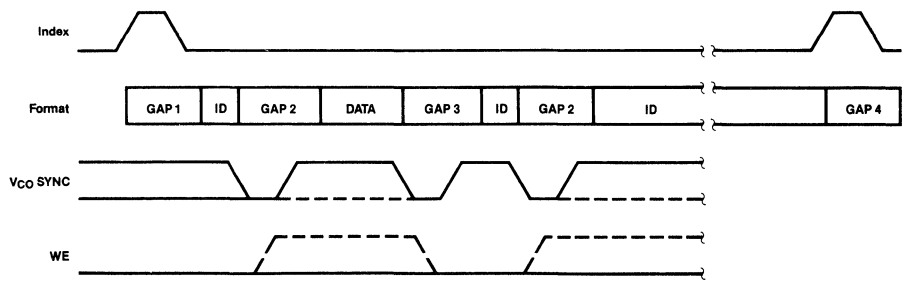
FDC72C66 (MFM Mode)



FDC72C65



FDC72C66



Note:
Read
Write

Figure 5. Data Format

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

Power supply voltage, V_{CC} ..... −0.3V to +7V
Input voltage, V_I ..... −0.3V to V_{CC} +0.3V
Output voltage, V_O ..... −0.3V to V_{CC} +0.3V
Operating temperature, T_{OPT} ..... 0°C to +70°C
Storage temperature, T_{STG} ..... −55°C to +125°C
Power dissipation, P_D 50mW

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE $T_A = 25°C$, $f_C = 1MHz$, $V_{CC} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input clock capacitance	$C_{IN}(\phi)$			20	pF	(Note 1)
Input capacitance	C_{IN}			10	pF	(Note 1)
Output capacitance	C_{OUT}			20	pF	(Note 1)

Note:
(1) All pins except pin under test tied to AC ground

DC CHARACTERISTICS

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2.2		V_{CC} +0.5	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200\ \mu A$
Supply current (V_{CC})	I_{DD} I_{DD1}		3 0.7	10 2	mA mA	
Input load current high	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input load current low	I_{LIL}			−10	μA	$V_{IN} = 0V$
Output leakage current high	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Output leakage current low	I_{LOL}			−10	μA	$V_{OUT} = +0.45$ V

AC CHARACTERISTICS

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock period	ϕ_{CY}	120	125 125 250 125	500	ns ns ns ns	(Note 4) 8″ FDD 5¼″ FDD 3½″ Sony (Note 3)
Clock active (high, low)	ϕ_0	40			ns	
Clock rise time	ϕ_r			20	ns	
Clock fall time	ϕ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}\downarrow$	t_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}\uparrow$	t_{RA}	0			ns	
$\overline{RD}$ width	t_{RR}	200			ns	
Data access time from $\overline{RD}\downarrow$	t_{RD}			140	ns	$C_L = 100$ pF
DB to float delay time from $\overline{RD}\uparrow$	t_{DF}	10		85	ns	$C_L = 100$ pF
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}\downarrow$	t_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}\uparrow$	t_{WA}	0			ns	
$\overline{WR}$ width	t_{WW}	200			ns	
Data setup time to $\overline{WR}\uparrow$	t_{DW}	100			ns	
Data hold time from $\overline{WR}\uparrow$	t_{WD}	0			ns	
INT delay time from $\overline{RD}\uparrow$	t_{RI}			400	ns	

AC CHARACTERISTICS CONTINUED

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
INT delay time from $\overline{WR}\uparrow$	t_{WI}			400	ns	
DRQ cycle time	t_{MCY}	13			µs	ϕ_{CY} = 125 ns (Note 4)
$\overline{DACK}\downarrow \rightarrow DRQ\downarrow$ delay	t_{AM}			140	ns	
$DRQ\uparrow \rightarrow \overline{DACK}\downarrow$ delay	t_{MA}	200			ns	ϕ_{CY} = 125 ns (Note 4)
$\overline{DACK}$ width	t_{AA}	2			ϕ_{CY}	
TC width	t_{TC}	1			ϕ_{CY}	
Reset width	t_{RST}	14			ϕ_{CY}	
WCK cycle time	t_{CY}		16 8 8 4 8 4		ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY}	MFM = 0, 5¼″ MFM = 1, 5¼″ MFM = 0, 8″ MFM = 1, 8″ MFM = 0, 3½″ (Note 3) MFM = 1, 3½″ (Note 3)
WCK active time (high)	t_0		2		ϕ_{CY}	
$CLK\uparrow \rightarrow WCK\uparrow$ delay	t_{CWH}	0		40	ns	
$CLK\uparrow \rightarrow WCK\downarrow$ delay	t_{CWL}	0		40	ns	
WCK rise time	t_R			20	ns	
WCK fall time	t_f			20	ns	
Preshift delay time from $WCK\uparrow$	t_{CP}	10		80	ns	
$WCK\uparrow \rightarrow WE\uparrow$ delay	t_{CWE}	10		80	ns	
WDA delay time from $WCK\uparrow$	t_{CD}	10		80	ns	
RDD active time (high)	t_{RDD}	40			ns	
Window cycle time	t_{WCY}		4 2 2 1 2 1		µs µs µs µs µs µs	MFM = 0, 5¼″ MFM = 1, 5¼″ MFM = 0, 8″ MFM = 1, 8″ MFM = 0, 3½″ (Note 3) MFM = 1, 3½″ (Note 3)
Window hold time to RDD	t_{RDW}	15			ns	
Window hold time from RDD	t_{WRD}	15			ns	
$US_{0,1}$ hold time to $\overline{RW}$ / $seek\uparrow$	t_{US}	12			µs	8 MHz clock period (Note 4)
$\overline{RW}$ / seek hold time to low current / $direction\uparrow$	t_{SD}	7			µs	8 MHz clock period (Note 4)
Low current / direction hold time to fault reset / $step\uparrow$	t_{DST}	1.0			µs	8 MHz clock period (Note 4)
$US_{0,1}$ hold time from fault reset / step 1	t_{STU}	5.0			µs	8 MHz clock period (Note 4)
Step active time (high)	t_{STP}	6	7	8	µs	(Note 4)
Step cycle time	t_{SC}	33	(2)	(2)	µs	(Note 4)
Fault reset active time (high)	t_{FR}	8.0		10	µs	(Note 4)
Write data width	t_{WDD}	t_0-50			ns	
$US_{0,1}$ hold time after seek	t_{SU}	15			µs	8 MHz clock period (Note 4)
Seek hold time from DIR	t_{DS}	30			µs	8 MHz clock period (Note 4)
DIR hold time after step	t_{STD}	24			µs	8 MHz clock period (Note 4)
Index pulse width	t_{IDX}	10			ϕ_{CY}	
$\overline{RD}\downarrow$ delay from DRQ	t_{MR}	1			ϕ_{CY}	8 MHz clock period (Note 4)
$\overline{WR}\downarrow$ delay from DRQ	t_{MW}	250			ns	8 MHz clock period (Note 4)
WE or $\overline{RD}$ response time from $DRQ\uparrow$	t_{MRW}			12	µs	8 MHz clock period (Note 4)

Note:

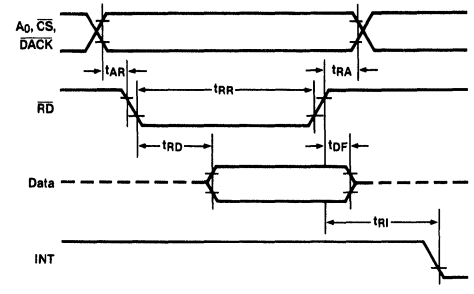
(1) Typical values for T_A = 25°C and nominal supply voltage.

(2) Under software control. The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 ms to 32 ms at 4 MHz clock period.

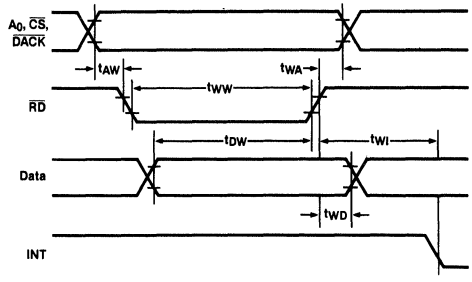
(3) Sony Micro Floppydisk 3½″ drive.

(4) Double these values for a 4 MHz clock period.

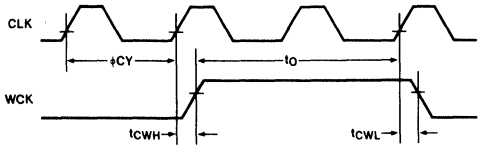
Timing Waveforms



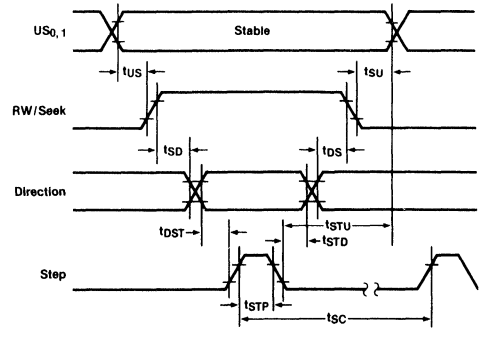
Processor Read Operation



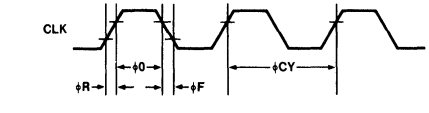
Processor Write Operation



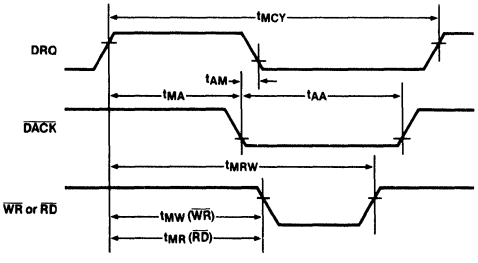
ϕ, WCK Timing



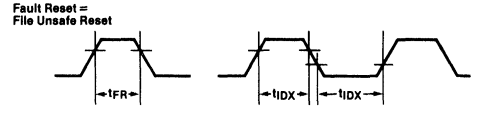
Seek Operation



Clock

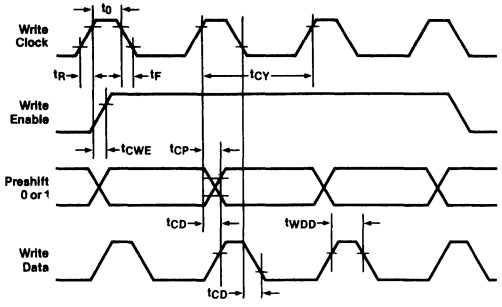


DMA Operation



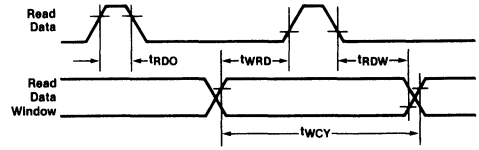
FLT Reset

Timing Waveforms



	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

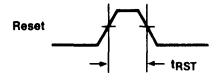
FDD Write Operation



Note: Either polarity data window is valid.

FDD Read Operation

Terminal Count



Reset

SECTION VI

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273 3100 TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

FDC91C36/ FDC92C36

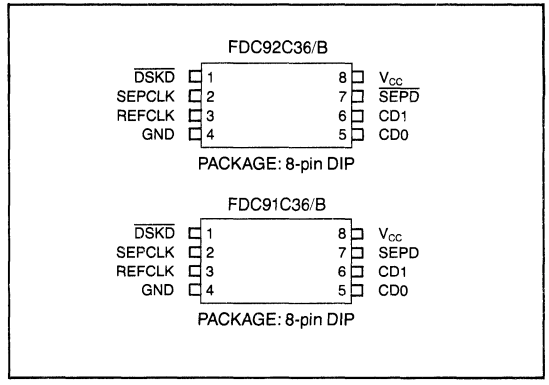
PRELIMINARY

CMOS Floppy Disk Data Separator

FEATURES

- ☐ High Performance Digital Data Separator
- ☐ Pin Replacement for FDC9216 (FDC92C36)
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Single +5 Volt Supply
- ☐ Fully TTL compatible
- ☐ Fabricated in power saving CMOS
- ☐ Compatible with 3.5″, 5.25″ and 8″ drives and data rates up to 500 Kb/s
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC92C36 is a direct high performance CMOS pin for pin replacement for the FDC9216 in systems using data transfer rates of 250Kb/s or 125Kb/s.

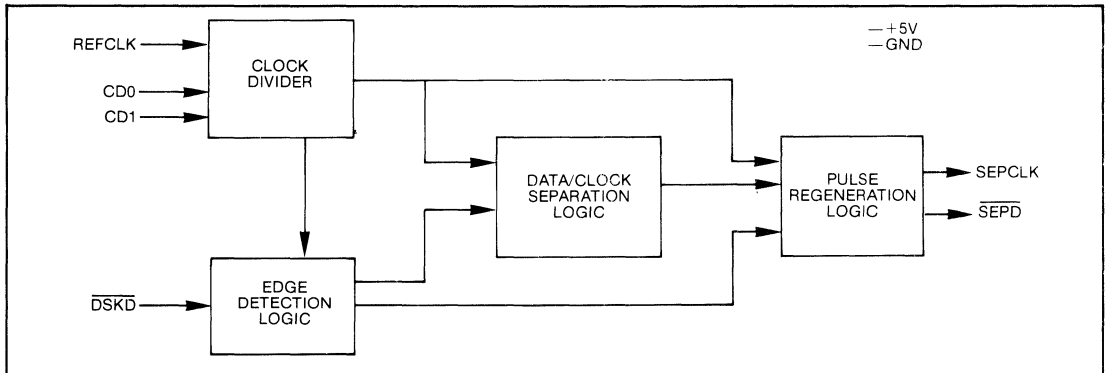
The FDC92C36B can be used in systems having a 500Kb/s data transfer rate by applying a 16MHz input clock to pin 3 and applying a low level to pin 6 and a high level to pin 5.

The FDC91C36/B is designed for use with the FDC765A, 8272A or FDC72C65 floppy disk controller. The FDC91C36/B provides an active high SEPD output, eliminating the inverter required when using the FDC9216/B.

The FDC91C36/FDC92C36 incorporates a high performance, synthetic phase locked loop digital data separator in a 300 mil wide 8 pin package.

The use of a high performance synthetic phase locked loop allows the system designer to replace a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC92C36 and the FDC91C36 are available in two versions: the parts without a "B" suffix (FDC92C36, FDC91C36) are intended for 5.25″ drives using data rates of 250 Kb/s, and the parts with a "B" suffix (FDC92C36B, FDC91C36B) are intended for 3.5″, 5.25″ and 8″ drives using data rates of 500 Kb/s.



FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Disk Data	$\overline{DSKD}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. Refer to Table 1.
7	Separated Data Separated Data	SEPD $\overline{SEPD}$	(FDC91C36) (FDC92C36) This output is the regenerated data pulse derived from the raw data input. This output is positive for the FDC91C36 and negative for the FDC92C36.
8	Power Supply	V_{DD}	+5 volt power supply

OPERATION

A reference clock (REFCLK) of 8 or 16 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/32 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 16 to a minimum of 12 and a maximum of 21 internal clock cycles.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1

CD1	CD0	8MHz REFCLK	9.6 MHz	16MHz REFCLK	DIVISOR f(REFCLK)/f(INTCLK)
0	0	not used	not used	5 1/4" SD 3 1/2" SD①	4
0	1	8" SD 5 1/4" DD 3 1/2" DD①	5 1/4" QD②	8" DD 5 1/4" QD	1
1	0	5 1/4" SD 3 1/2" SD①	not used	8" SD 5 1/4" DD 3 1/2" DD①	2
1	1	Illegal	Illegal	Illegal	Illegal

NOTES: ①Some 3 1/2" drives are 8" compatible (instead of 5 1/4" as assumed in Table 1). For these drives, use 8" values.
②9.6 MHz clock is used to read or write a 5 1/4" double density diskette on a quad density drive.

PERFORMANCE SPECIFICATIONS

PARAMETER		MFM 500KHZ	MFM 250KHZ	UNITS
BIT JITTER				
	NOMINAL SPEED	+/−260	+/−540	nsec
	+5% SPEED	+/−260	+/−480	nsec
	−5% SPEED	+/−320	+/−640	nsec
WINDOW MARGIN	EARLY	500	980	nsec
	LATE	500	980	nsec
	COMBINED	+/−400	+/−740	nsec

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... V_{CC} +0.3V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Power Dissipation 0.75W
Maximum Voltage on V_{CC} Pin, with respect to ground 7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

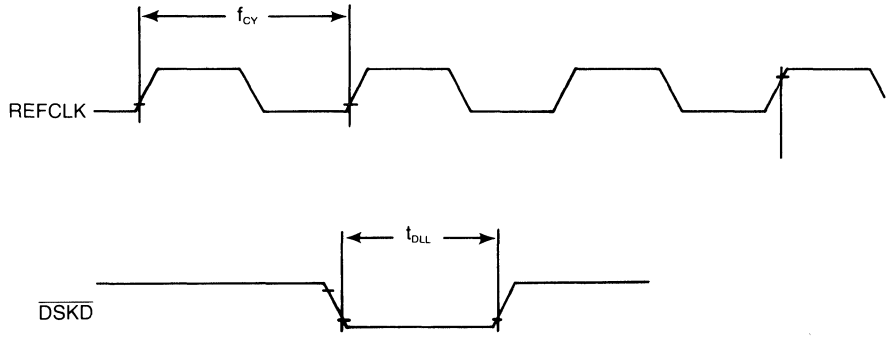
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to 70°C, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

Parameter	SYMBOL	Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	$I_{OL} = 1.6mA$
High Level V_{OH}		2.4			V	$I_{OH} = -100\ \mu A$
INPUT CURRENT						
Leakage I_{IL}				10.0	μA	$0 < V_{IN} < V_{DD}$
INPUT CAPACITANCE						
All Inputs				10.0	pF	
POWER SUPPLY CURRENT						
I_{DD}				20.0	mA	
A.C. CHARACTERISTICS						
REFCLK Frequency	f_{cy}	1.0	8.0	8.1	MHz	FDC 92C36/FDC 91C36
REFCLK Frequency	f_{cy}	1.0	16.0	16.2.	MHz	FDC 92C36B/FDC 91C36B
$\overline{DSKD}$ Active Low Time	t_{DLL}	0.05		100.0	μs	
CLKIN Duty Cycle		40		60	%	

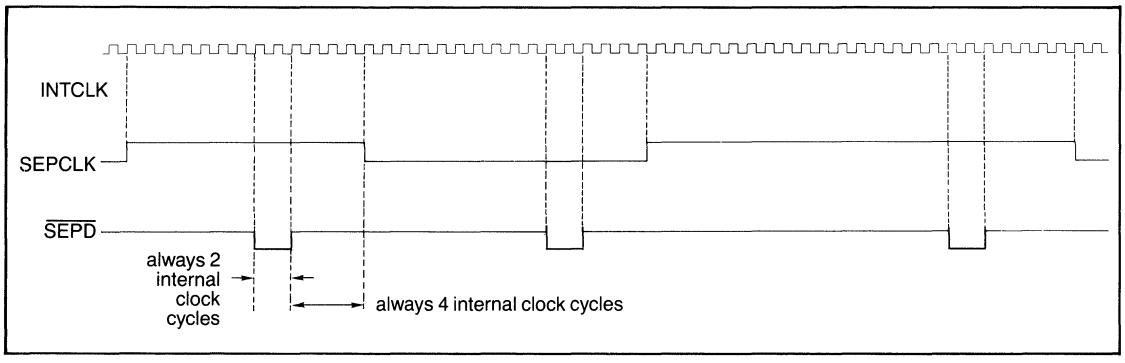
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

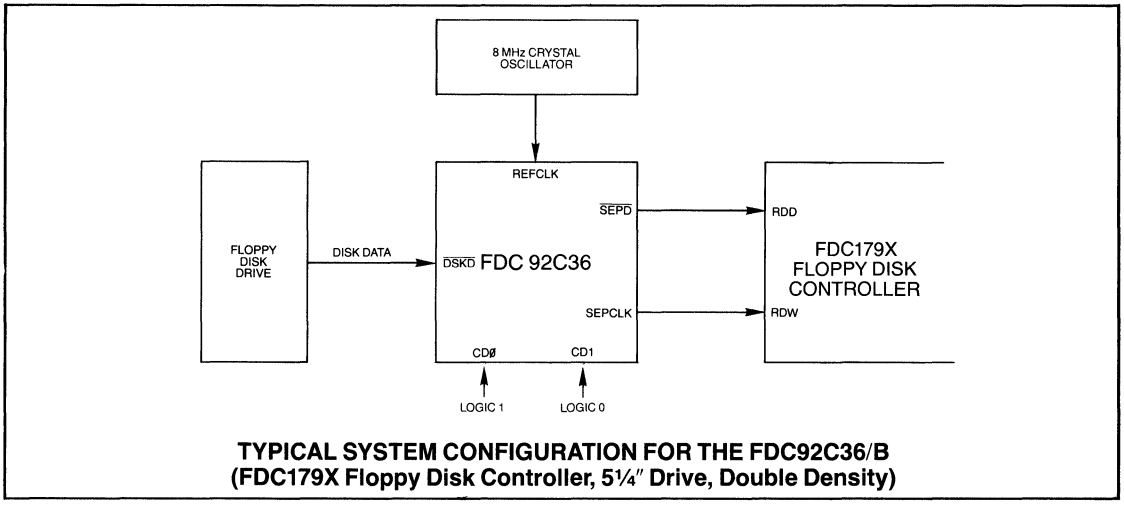
*All times assume XTAL/CLKIN = 16 MHz unless otherwise specified.



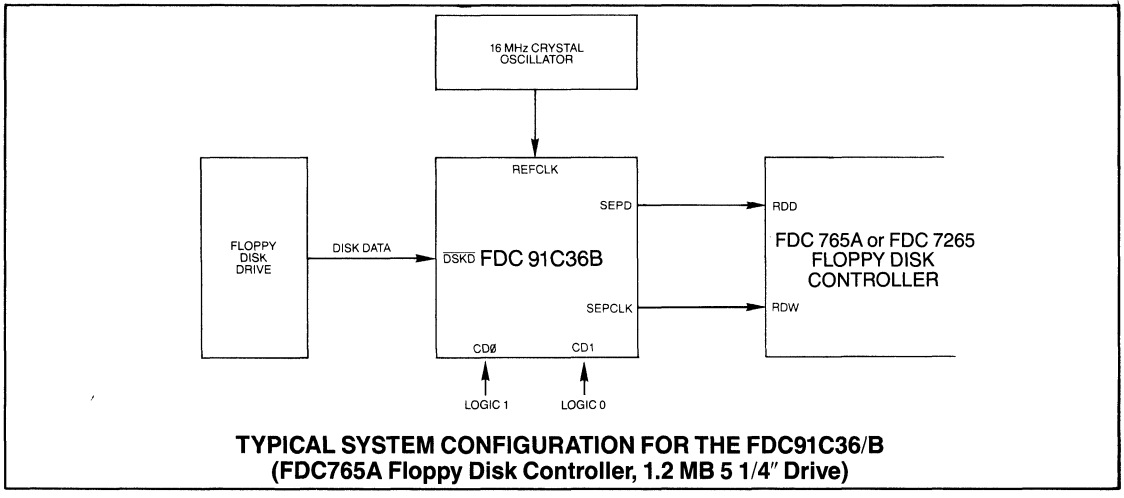
AC CHARACTERISTICS

SECTION VI





TYPICAL SYSTEM CONFIGURATION FOR THE FDC92C36/B
(FDC179X Floppy Disk Controller, 5¼″ Drive, Double Density)



TYPICAL SYSTEM CONFIGURATION FOR THE FDC91C36/B
(FDC765A Floppy Disk Controller, 1.2 MB 5 1/4″ Drive)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge, N.Y. 11788
(516) 273-3100 TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

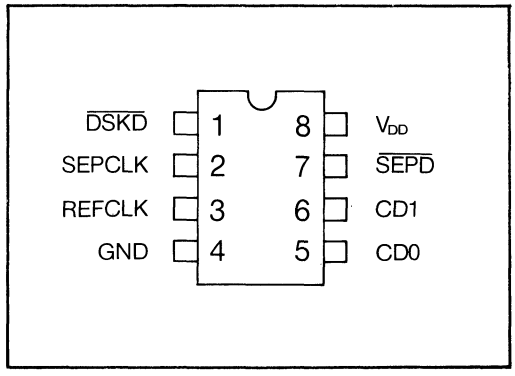
FDC 9216
FDC 9216B
μPC FAMILY

Floppy Disk Data Separator
FDDS

FEATURES

- ☐ PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- ☐ SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ☐ ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- ☐ NO CRITICAL ADJUSTMENTS REQUIRED
- ☐ COMPATIBLE WITH STANDARD MICROSYSTEMS' FDC 1791, FDC 1793 AND OTHER FLOPPY DISK CONTROLLERS
- ☐ SMALL 8-PIN DUAL-IN-LINE PACKAGE
- ☐ +5 VOLT ONLY POWER SUPPLY
- ☐ TTL COMPATIBLE INPUTS AND OUTPUTS

PIN CONFIGURATION



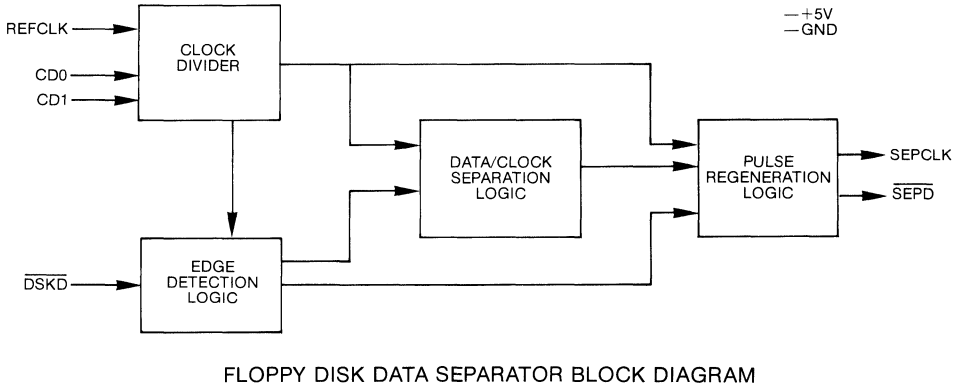
SECTION VI

GENERAL DESCRIPTION

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The FDC 9216 is available in two versions; the FDC 9216, which is intended for 5¼" disks and the FDC 9216B for 5¼" and 8" disks.

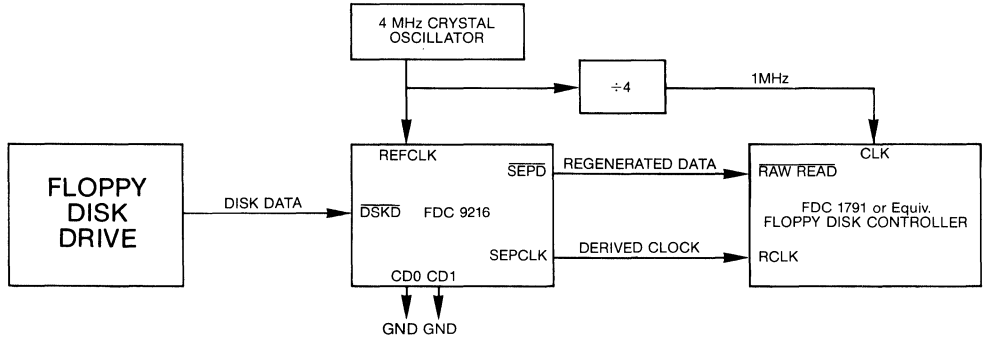


FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5, 6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

FIGURE 1
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

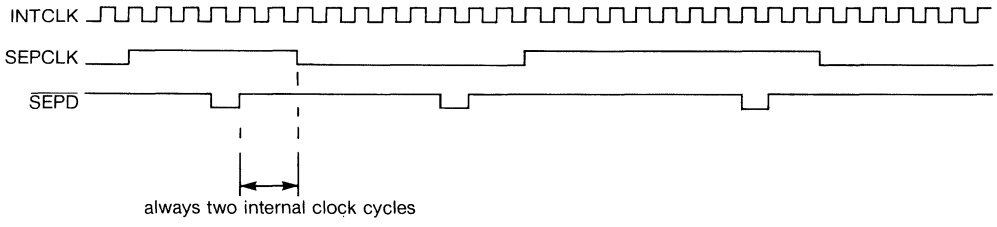
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5¼")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	Select any one
5¼	SD	2	0	0	

FIGURE 2



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

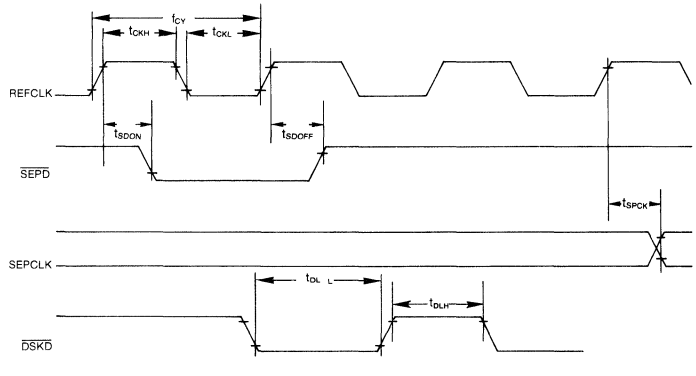
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{DD}=+5V±5%, unless otherwise noted)

Parameter		Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL}=1.6mA
High Level V_{OH}		2.4			V	I_{OH}=−100 μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$O \leq V_{IN} \leq V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				60	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{cy}	REFCLK Frequency	0.2		4.3	MHz	FDC 9216
f_{cy}	REFCLK Frequency	0.2		8.3	MHz	FDC 9216B
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay	25	100	250	ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay	25	100	250	ns	
t_{SPCK}	REFCLK to SEPCLK Delay	35			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

FIGURE 3: AC CHARACTERISTICS



STANDARD MICROSYSTEMS CORPORATION

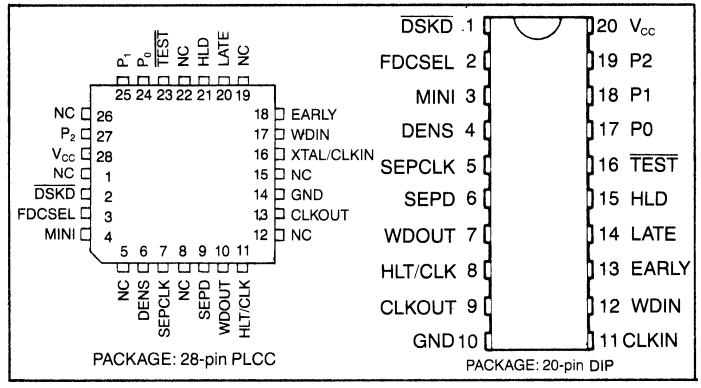
FDC 9229T
FDC 9229BT

FLOPPY DISK INTERFACE CIRCUIT

FEATURES

- ☐ Digital Data Separator
  Performs complete data separation function for floppy disk drives
  Separates FM and MFM encoded data
  No critical adjustments necessary
  5¼" and 8" compatible
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator Circuit
- ☐ Track-Selectable Write Precompensation
- ☐ Retriggerable Head-Load Timer
- ☐ Compatible with the FDC 179X, 765, and other standard Floppy Disk Controllers
- ☐ COPLAMOS® n-channel MOS Technology
- ☐ Single +5 Volt Supply
- ☐ TTL Compatible

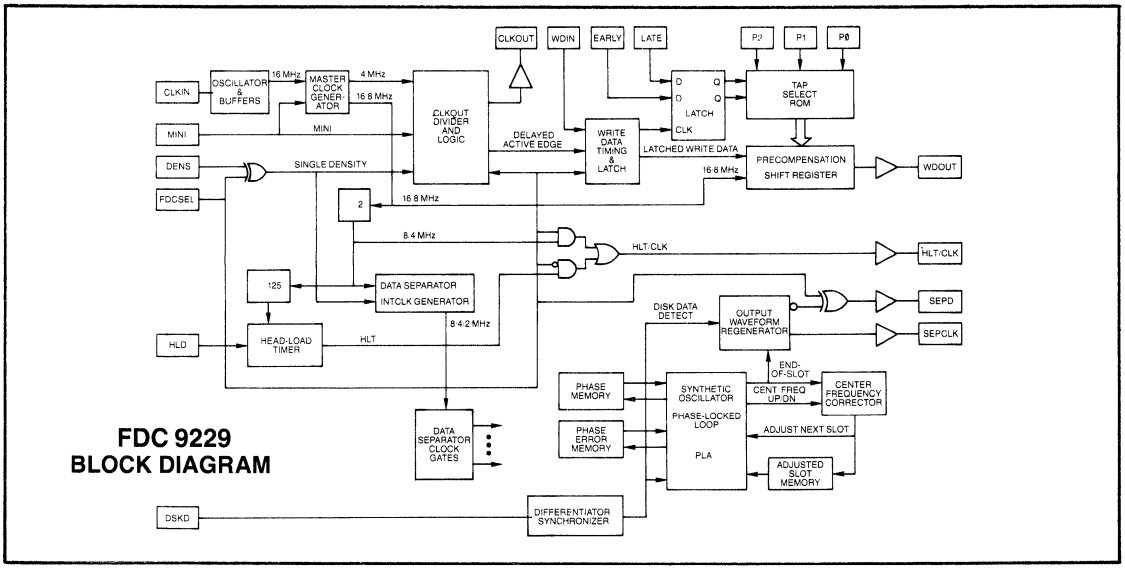
PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC 9229 is an MOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9229 provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9229 operates from a + 5V supply and simply requires that a TTL-level clock be connected to the CLKIN pin. All inputs and outputs are TTL compatible.

The FDC 9229 is available in two versions: The FDC 9229/T are intended for 5¼" drives and the FDC 9229B/T for 5¼" and 8" drives.



FDC 9229
BLOCK DIAGRAM

SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{\text{DSKD}}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low, programs the FDC 9229 for a 179X type of LSI controller. When FDCSEL is high, the FDC 9229 is programmed for a 765 (8272) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the FDC 9229 is configured to support 8″ or 5¼″ floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the FDC 9229 is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{\text{DSKD}}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{\text{DSKD}}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occurred following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz single-phase TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.) In 765 mode, this pin should be left floating or grounded.
16	$\overline{\text{TEST}}$	I	This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

Data Separator

The CLKIN input clock is internally divided by the FDC 9229 to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

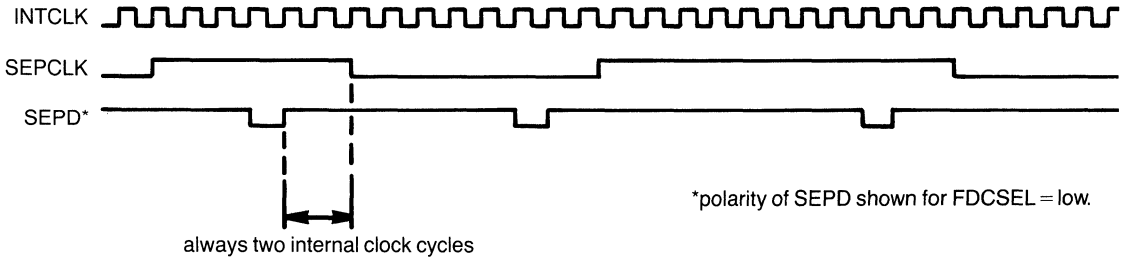
The FDC 9229 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

INPUTS			DIVISOR
FDCSEL	DENS	MINI	f(CLKIN)/f(INTCLK)
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

FIG. 1



Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9229 as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION

Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9229 goes high before starting a read or write operation.

INPUTS			OUTPUTS	
FDCSEL	DENS	MINI	CLKOUT	HLT/CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

*May be mask programmed at factory to any value from 1 to 512 ms in 15.625 μs increments (MINI low) or 1 to 1024 ms in 31.25 μs increments (MINI high).

FIG. 3 CLOCK AND HEAD LOAD TIME DELAY SELECTION

INPUTS			FLOPPY DISK	FLOPPY DISK	FLOPPY DISK
FDCSEL	DENS	MINI	DRIVE TYPE	DRIVE DENSITY	CONTROLLER TYPE
0	0	0	8" DRIVE	DOUBLE	179X
0	0	1	5¼" DRIVE	DOUBLE	179X
0	1	0	8" DRIVE	SINGLE	179X
0	1	1	5¼" DRIVE	SINGLE	179X
1	0	0	8" DRIVE	SINGLE	765 (8272)
1	0	1	5¼" DRIVE	SINGLE	765 (8272)
1	1	0	8" DRIVE	DOUBLE	765 (8272)
1	1	1	5¼" DRIVE	DOUBLE	765 (8272)

FIG. 4 FLOPPY DISK DRIVE AND CONTROLLER SELECTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+8.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low Level V_{IL}	−0.3		0.8	V	Except CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
CLKIN INPUT VOLTAGE					
Low Level	−0.3		0.8	V	
High Level	2.4		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100 µA except HLT/CLK
					I_{OH} = −400 µA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURRENT					
I_{IL}			10	µA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

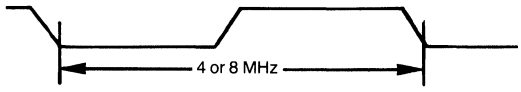
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
AC ELECTRICAL CHARACTERISTICS	All times assume CLKIN = 16 MHz unless otherwise specified)				
CLKIN frequency	3.95	16	16.2	MHz	FDC 9229B
	3.95	8	8.1	MHz	FDC 9229
CLKIN DUTY CYCLE	25		75	%	
t_{clkoh}	465	500	515	ns	FDCSEL = low; MINI = high.
	215	250	265	ns	FDCSEL = low; MINI = low.
	90	125	140	ns	FDCSEL = high.
t_{wdo}	280	312.5	350	ns	Time Doubles with MINI = 1
t_d	50		400	ns	
t_{dNEC}	0		400	ns	
t_{wdE}	500	562.5	625	ns	9 clock times ± 1 clock time
t_{wdN}		precomp value			See fig. 2
t_{wdL}		2x precomp value			See fig. 2
t_s	1.0			µs	

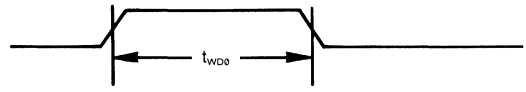
SECTION VI

AC TIMING CHARACTERISTICS

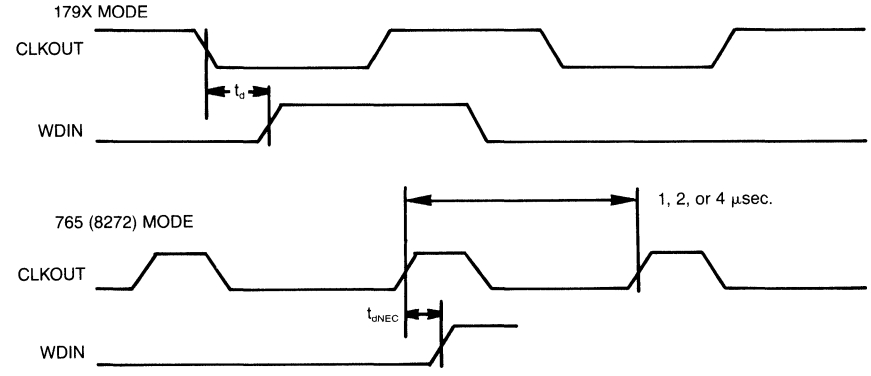
HLT/CLK (765 MODE)



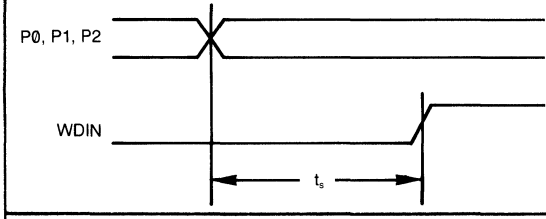
WDOUT PULSE WIDTH



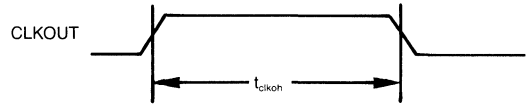
CLKOUT VS. WDIN TIMING



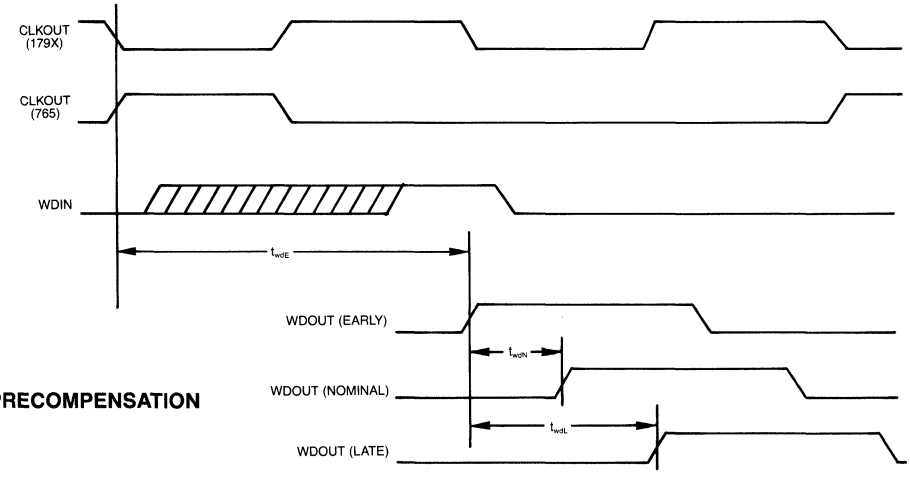
SET-UP TIME PØ, P1 AND P2 TO WDIN



CLKOUT

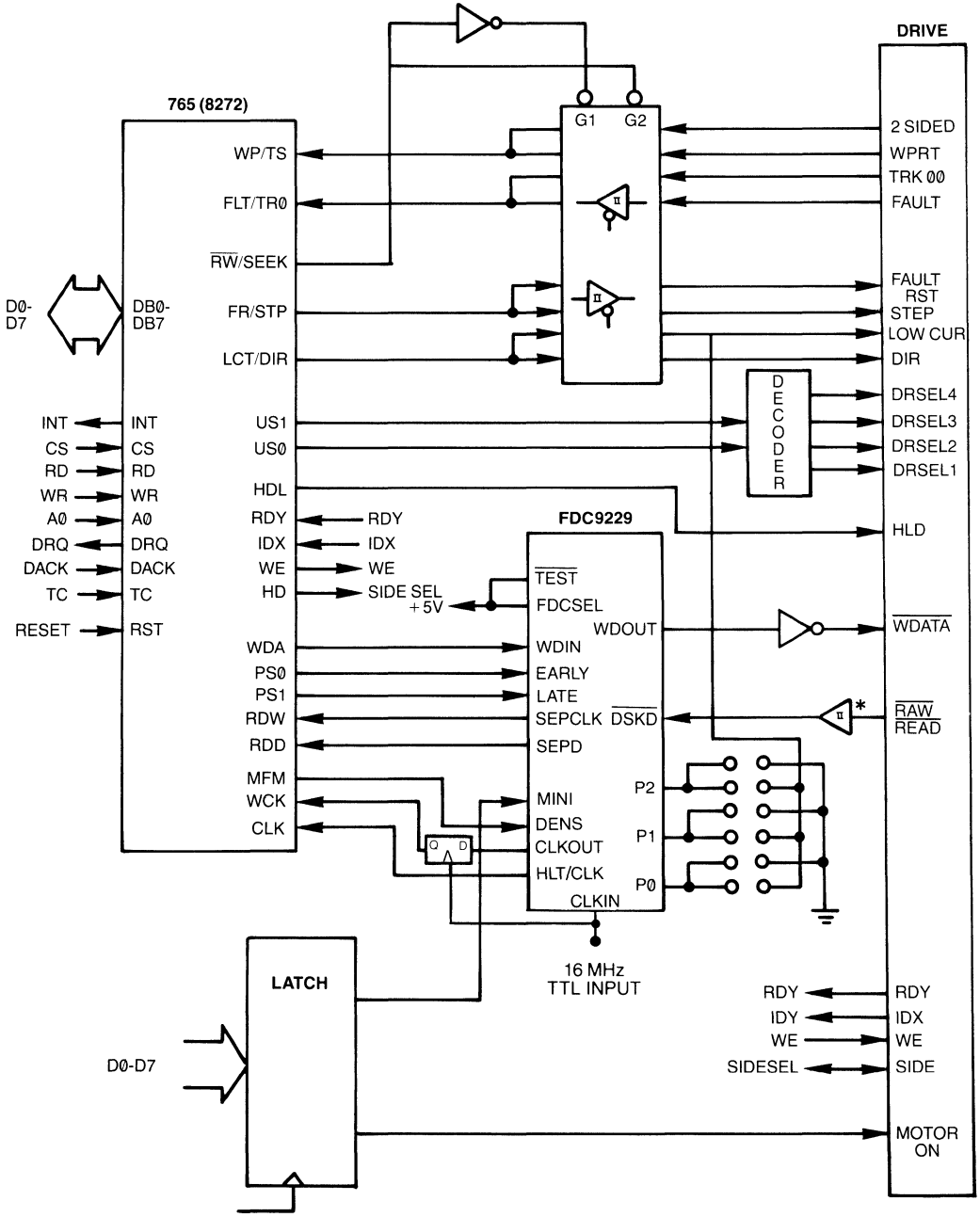


PRECOMPENSATION



Ref. to Fig. 2 for t_p (precompensation) value

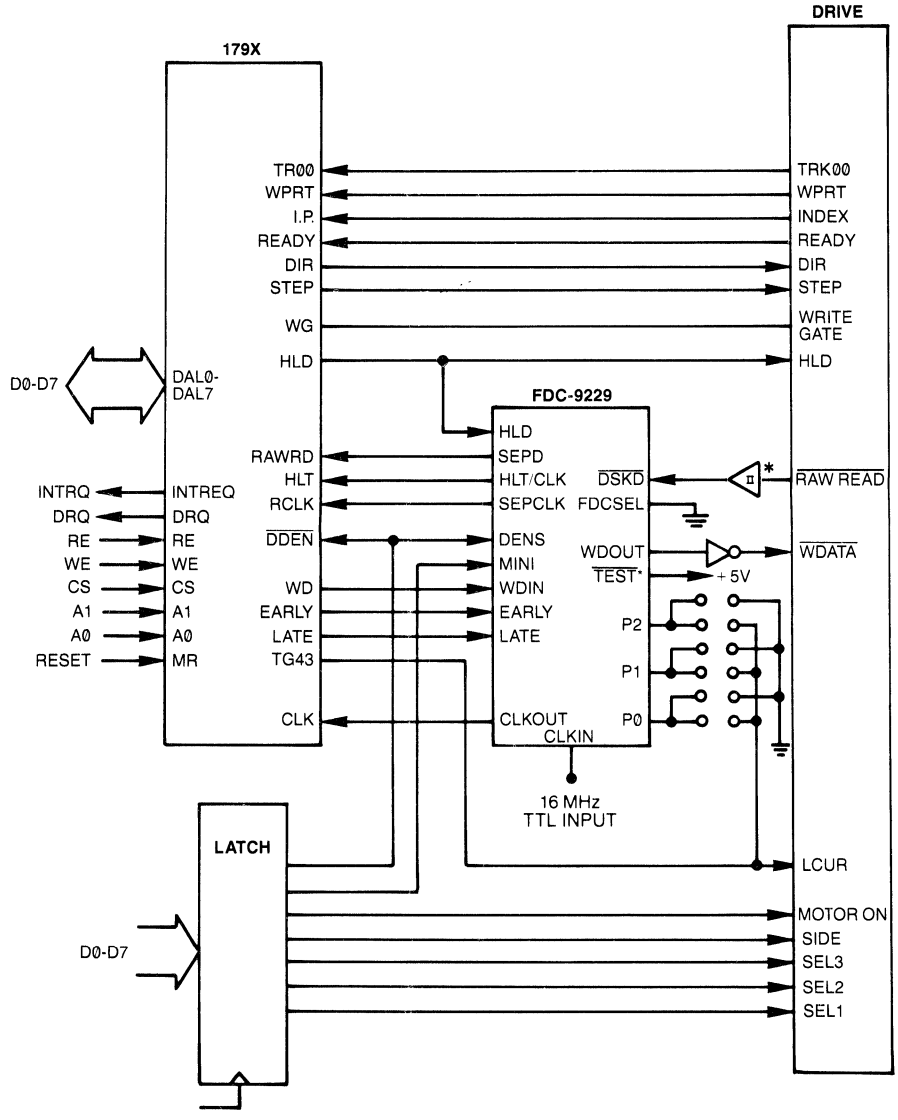
TYPICAL SYSTEM IMPLEMENTATION—765 (8272) FDC



*The FDC9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

TYPICAL SYSTEM IMPLEMENTATION—179X FDC



*The FDC9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

FDC 92C38/92C38B
FDC 92C38T/92C38BT

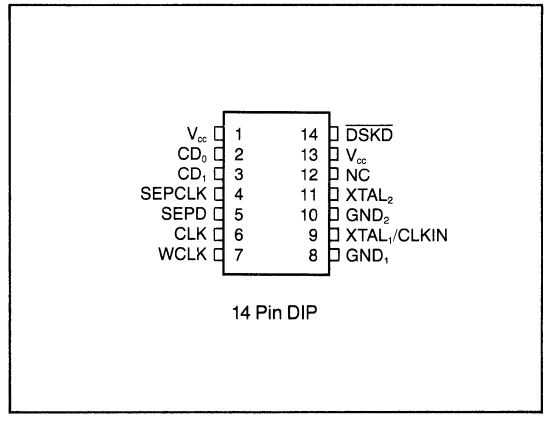
PRELIMINARY

CMOS Floppy Disk Data Separator and Clock Generator

FEATURES

- ☐ High Performance Digital Data Separator with Synthetic Oscillator and Phase Lock Loop for industry standard FDC 765A and FDC 7265
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Compatible with 3.5″, 5.25″ and 8″ drives and data rates up to 500 KBs
- ☐ Internal Crystal Oscillator Circuit provides all clocks required by FDC 765A and FDC 7265
- ☐ Fabricated in power saving CMOS
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs
- ☐ Single +5 Volt supply
- ☐ Fully TTL compatible

PIN CONFIGURATION



14 Pin DIP

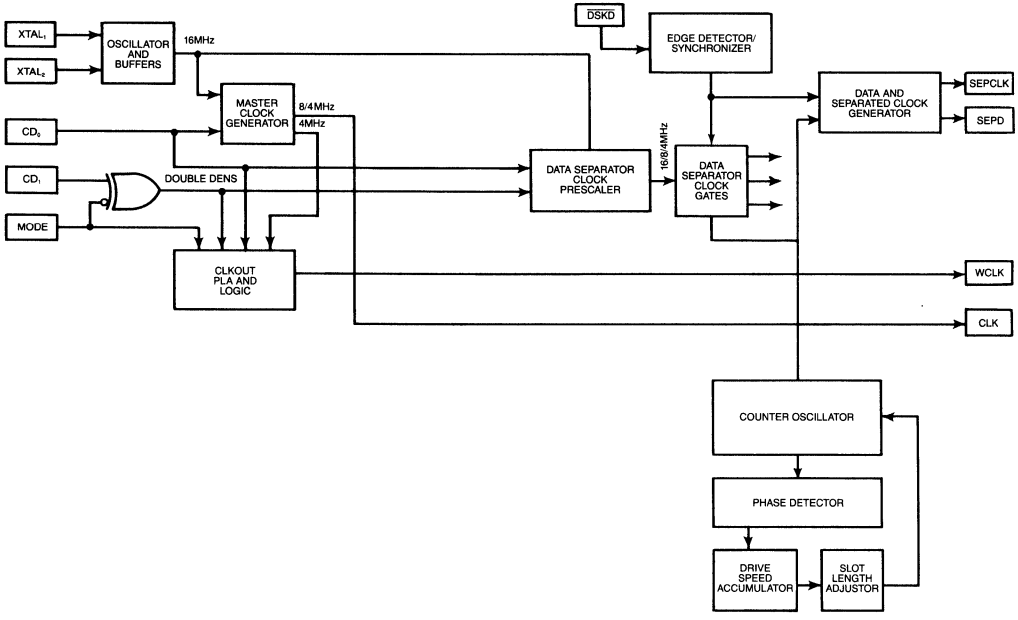
SECTION VI

FUNCTIONAL DESCRIPTION

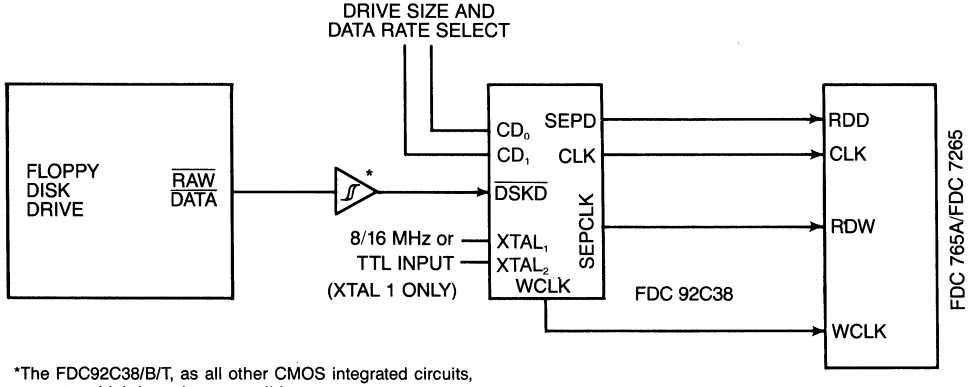
The FDC 92C38 is a CMOS integrated circuit designed to complement the FDC 765A (8272A) or the FDC 7265 floppy disk controller. It incorporates a high performance, synthetic phase locked loop digital data separator and clock generator in one 0.3 inch wide 14 pin package.

The use of a high performance synthetic phase locked loop data separator allows the system designer to replace (without sacrificing performance) a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC 92C38 is available in four versions: the FDC 92C38/T which is intended for disk transfer rates up to 250 kilobits per second and the FDC 92C38B/T is intended for disk transfer rates up to 500 kilobits per second.



FDC 92C38 BLOCK DIAGRAM



*The FDC92C38/B/T, as all other CMOS integrated circuits, presents a high impedance on all inputs

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{DSKD}$ input to the FDC92C38/B/T.

TYPICAL SYSTEM IMPLEMENTATION

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	V_{cc}	I	This pin MUST be tied to V_{cc}.
2,3	CD_0,CD_1	I	These inputs select the appropriate internal clock divisor for the data rate of the disk data, the CLK output to the FDC and the WCLK output to the FDC. Refer to Table 1.
4	SEPCLK	0	A Square wave window clock signal output derived from the $\overline{DSKD}$ input.
5	SEPD	0	This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). To insure complete compatibility with the FDC 765A and FDC 7265, this output is positive going.
6	CLK	0	This output provides the clock signal for the FDC 765A or FDC 7265.
7	WCLK	0	This output provides the write clock signal for the FDC 765A or FDC 7265.
8	GND_1		Ground
9	$XTAL_1$/CLKIN	I	This input is for direct connection to an 8 or 16 MHz single-phase TTL level clock, or one lead from an 8 or 16 MHz crystal.
10	GND_2	I	This pin must be tied to ground.
11	$XTAL_2$	I	In the FDC 92C38 and FDC 92C38B, the second lead from an 8 or 16 MHz crystal is connected to this pin. In the FDC 92C38T and FDC 92C38BT, this pin should be left floating.
12	NC		No connection should be made to this pin.
13	V_{cc}	I	+5 Volts
14	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)

SECTION VI

OPERATION

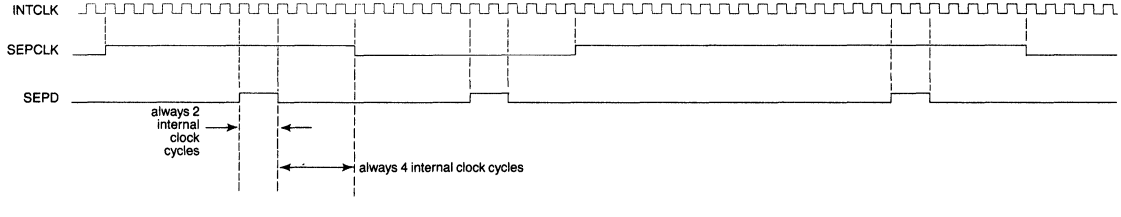
The high performance digital data separator incorporated in the FDC 92C38 will accept data from the floppy disk drive at 125 KHz, 250 KHz, or 500 KHz data rates and output the appropriate regenerated clock and data signals.

The heart of the digital floppy disk data separator section is a synthetic oscillator phase locked loop. One half-bit cell of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of 16 phase slices. The circuit, therefore, needs a phase slice clock with a frequency of 16 times the half-bit cell time.

Detection of an input pulse away from the center of its half-bit "slot" causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit slot closer to the pulse.

The end-of-cycle signal from the synthetic oscillator defines the derived clock waveform and the duration of each half-bit slot. If there is a flux transition during the half-bit slot, it is remembered and used to regenerate the data waveform pulses immediately following the end-of-cycle.

A short history of input pulse detections (which induce phase corrections by the FDC 92C38) is kept. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency, and helps compensate for drive speed variations. This, along with separate short term and long term correction algorithms, assures accurate floppy disk data separation.



MAXIMUM GUARANTEED RATINGS

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 300°C
Positive Voltage on any I/O Pin, with respect to ground	V_{CC} + 0.3V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Maximum V_{CC}	+ 7V
Power Dissipation	0.25W

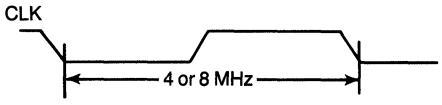
Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

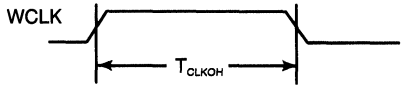
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low (V_{IL})	−0.3		0.8	V	Except XTAL/CLKIN
High (V_{IH})	2.0		V_{cc}		
XTAL/CLKIN INPUT VOLTAGE					
Low (V_{IL})	−0.3		1.5	V	
High (V_{IH})	3.2		V_{cc}	V	
OUTPUT VOLTAGE					
Low (V_{OL})			0.4	V	L_{OL} = 1.6 ma, except CLK
					L_{OL} = 0.4 ma, CLK only
					L_{OH} = − 100µa, except CLK
High (V_{OH})	2.4				L_{OH} = − 400µa, CLK only
POWER SUPPLY CURRENT					
I_{cc}		TBD			
INPUT LEAKAGE CURRENT					
I_{IL}		TBD			
INPUT CAPACITANCE					
C_{IN}		TBD			
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
CLKIN Frequency	3.95	16	16.2	MHz	FDC 92C38B/BT
	3.95	8.0	8.1	MHz	FDC 92C38/T
CLKIN Duty Cycle	40		60	%	
T_{CLKOH}	90	125	140	ns	



XTAL	Inputs CD_1	Inputs CD_0	DISK DATA RATE	CLK	WCLK	ENCODING
16MHz	0	0	250KHz	8MHz	500KHz	FM
16MHz	1	0	500KHz	8MHz	1MHz	MFM
16MHz	0	1	125KHz	4MHz	250KHz	FM
16MHz	1	1	250KHz	4MHz	500KHz	MFM
8MHz	0	0	125KHz	4MHz	250KHz	FM
8MHz	1	0	250KHz	4MHz	500KHz	MFM
8MHz	0	1	Not Used			
8MHz	1	1	Not Used			

TABLE 1



STANDARD MICROSYSTEMS CORPORATION

FDC 92C39/92C39B 92C39T/92C39BT

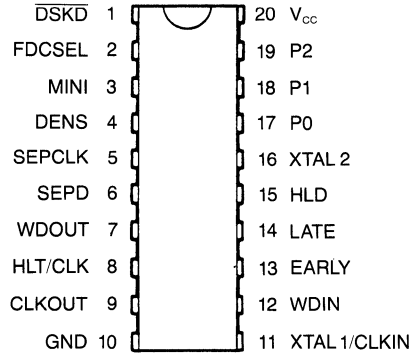
PRELIMINARY

ENHANCED FLOPPY DISK INTERFACE CIRCUIT

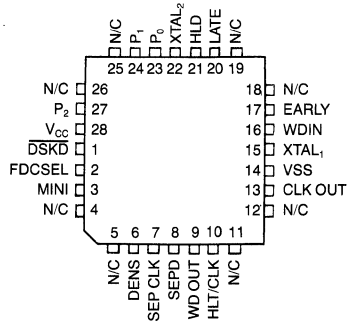
FEATURES

- ☐ Digital Data Separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 3½", 5¼" and 8" compatible
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator Circuit
- ☐ Track-Selectable Write Precompensation
- ☐ Retriggerable Head-Load Timer
- ☐ Fully compatible with FDC 179X, FDC 765A and FDC 7265
- ☐ 16-Bit Cell Divide Algorithm Improves Performance
- ☐ Fabricated in Low Power CMOS
- ☐ Single +5 Volt Supply
- ☐ TTL Compatible; Fully Compatible with the FDC 9229

PIN CONFIGURATION



PACKAGE: 20-pin D.I.P.



PACKAGE: 28-pin PLCC

SECTION VI

FUNCTIONAL DESCRIPTION

The FDC 92C39 is a CMOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 92C39 provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 92C39 operates from a +5V supply.

The FDC 92C39 is available in four versions: the FDC 92C39/T which is intended for 5¼" drives and the FDC 92C39B/T for 3½", 5¼", and 8" drives. (The /T versions require a TTL clock input.)

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{\text{DSKD}}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low, programs the FDC 92C39 for a 179X type of LSI controller. When FDCSEL is high, the FDC 92C39 is programmed for a 765 (8272) or 7265 floppy disk controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the FDC 92C39 is configured to support 8″ or 5¼″ floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the FDC 92C39 is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{\text{DSKD}}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{\text{DSKD}}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL 1/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz single-phase TTL-level clock, or one lead from an 8 MHz or 16 MHz crystal.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state MINI output. (See fig. 3.) In 765 mode this pin must not be forced high.
16	XTAL 2	I	The second lead from an 8 MHz or 16 MHz crystal is connected to this pin. In those applications, using a TTL clock, this pin should be left floating.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

Data Separator

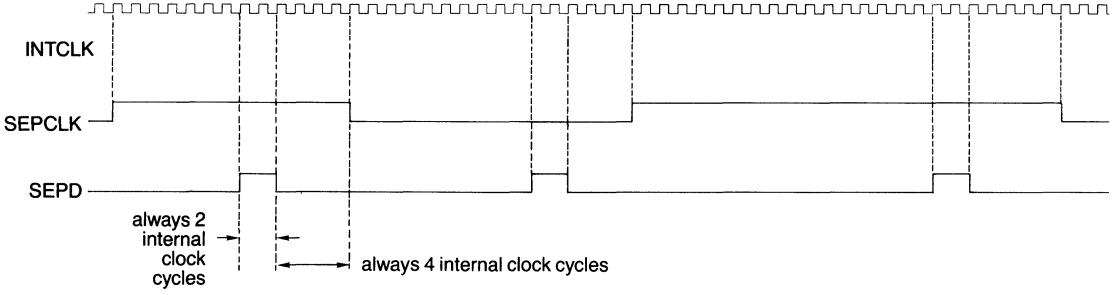
The CLKIN input clock is internally divided by the FDC 92C39 to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

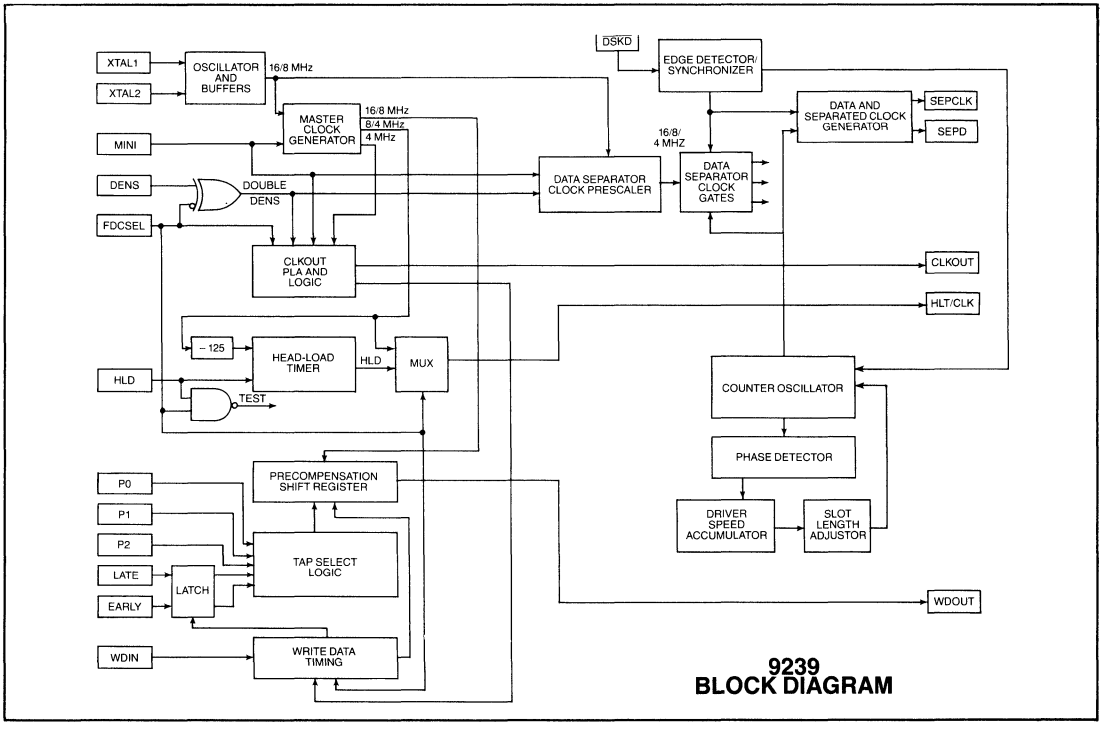
The FDC 92C39 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/32 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 16 to a minimum of 12 and a maximum of 21 internal clock cycles.

INPUTS			DIVISOR
FDCSEL	DENS	MINI	f(CLKIN)/f(INTCLK)
0	0	0	1
0	0	1	2
0	1	0	2
0	1	1	4
1	0	0	2
1	0	1	4
1	1	0	1
1	1	1	2





9239 BLOCK DIAGRAM

SECTION VI

Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 92C39 as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 or 7265 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 92C39 goes high before starting a read or write operation.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION

INPUTS			OUTPUTS				
FDCSEL	DENS	MINI	CLKOUT	HLT/CLK	16 MHZ INPUT CLOCK	8 MHZ INPUT CLOCK	CONTROLLER
0	0	0	2 MHz	40 ms*	8" Double Density	5¼" Double Density	179X
0	0	1	1 MHz	80 ms*	5¼" Double Density	Not Permitted	179X
0	1	0	2 MHz	40 ms*	8" Single Density	5¼" Single Density	179X
0	1	1	1 MHz	80 ms*	5¼" Single Density	Not Permitted	179X
1	0	0	500 KHz	8 MHz	8" Single Density	5¼" Single Density	765 (8272)
1	0	1	250 KHz	4 MHz	5¼" Single Density	Not Permitted	765 (8272)
1	1	0	1 MHz	8 MHz	8" Double Density	5¼" Double Density	765 (8272)
1	1	1	500 KHz	4 MHz	5¼" Double Density	Not Permitted	765 (8272)

NOTE: 3½" drive users should consult drive specifications to determine if drive data rate equals 5.25" or 8" standards.

*NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

FIG. 3 CLOCK/HEAD LOAD TIME DELAY AND FLOPPY DISK DRIVE/CONTROLLER SELECTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 300°C
Positive Voltage on any I/O Pin, with respect to ground	V_{CC} + 0.3V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Maximum V_{CC}	+ 7V
Power Dissipation	0.25W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low Level V_{IL}	−0.3		0.8	V	Except CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL/CLKIN INPUT VOLTAGE					
Low (V_{IL})	−0.3		1.5	V	
High (V_{IH})	3.2		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100 µA except HLT/CLK
					I_{OH} = −400 µA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			20	mA	
INPUT LEAKAGE CURRENT					
I_{IL}			10	µA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE				pF	Except CLKIN
C_{IN}		TBD		pF	CLKIN only

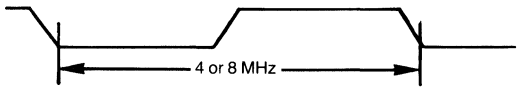
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
CLKIN frequency	3.95	16	16.2	MHz	FDC 92C39B
	3.95	8	8.1	MHz	FDC 92C39
CLKIN DUTY CYCLE	40		60	%	
t_{clkoh}	465	500	515	ns	FDCSEL = low; MINI = high
	215	250	265	ns	FDCSEL = low; MINI = low
	90	125	140	ns	FDCSEL = high
t_{wdo}	150	312.5	350	ns	Time Doubles with MINI-1
t_d	50		400	ns	
t_{dNEC}	0		400	ns	
t_{wdE}	500	562.5		ns	9 clock times ± 1 clock time
t_{wdN}		precomp value			See fig. 2
t_{wdL}		2 x precomp value			See fig. 2
t_s	1.0			µs	

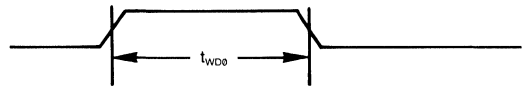
SECTION VI

AC TIMING CHARACTERISTICS

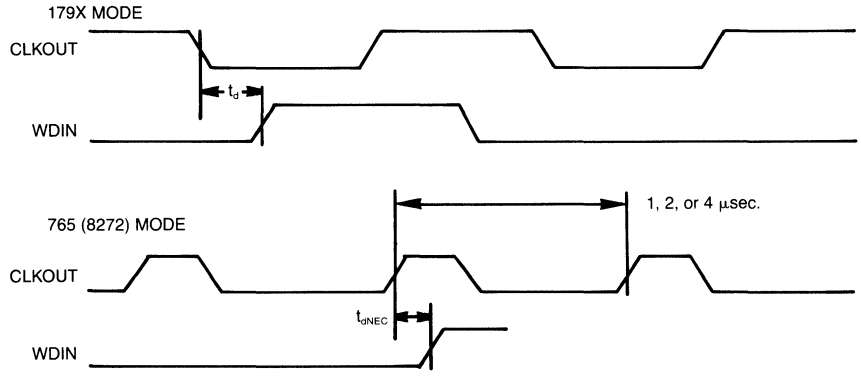
HLT/CLK (765 MODE)



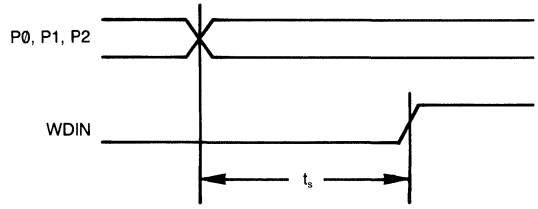
WDOUT PULSE WIDTH



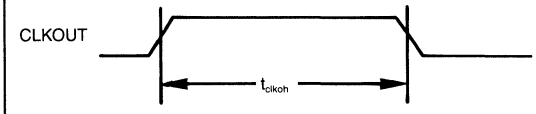
CLKOUT VS. WDIN TIMING



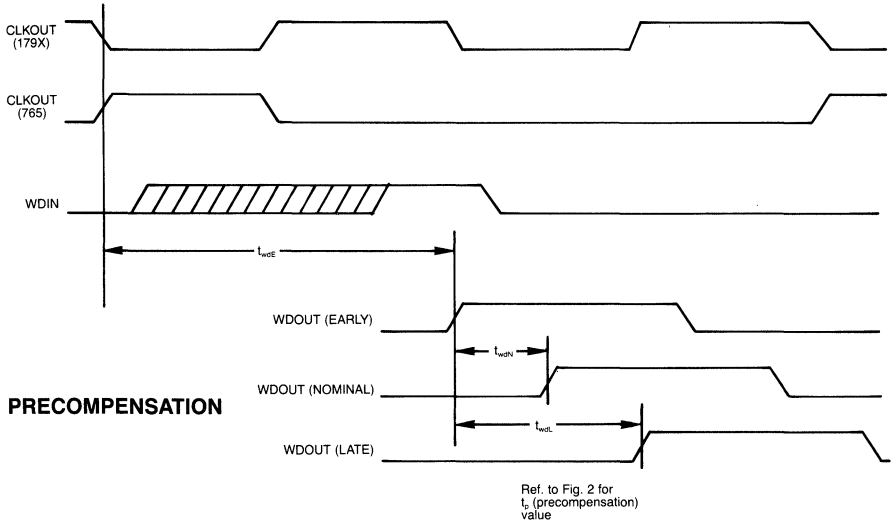
SET-UP TIME P0, P1 AND P2 TO WDIN



CLKOUT

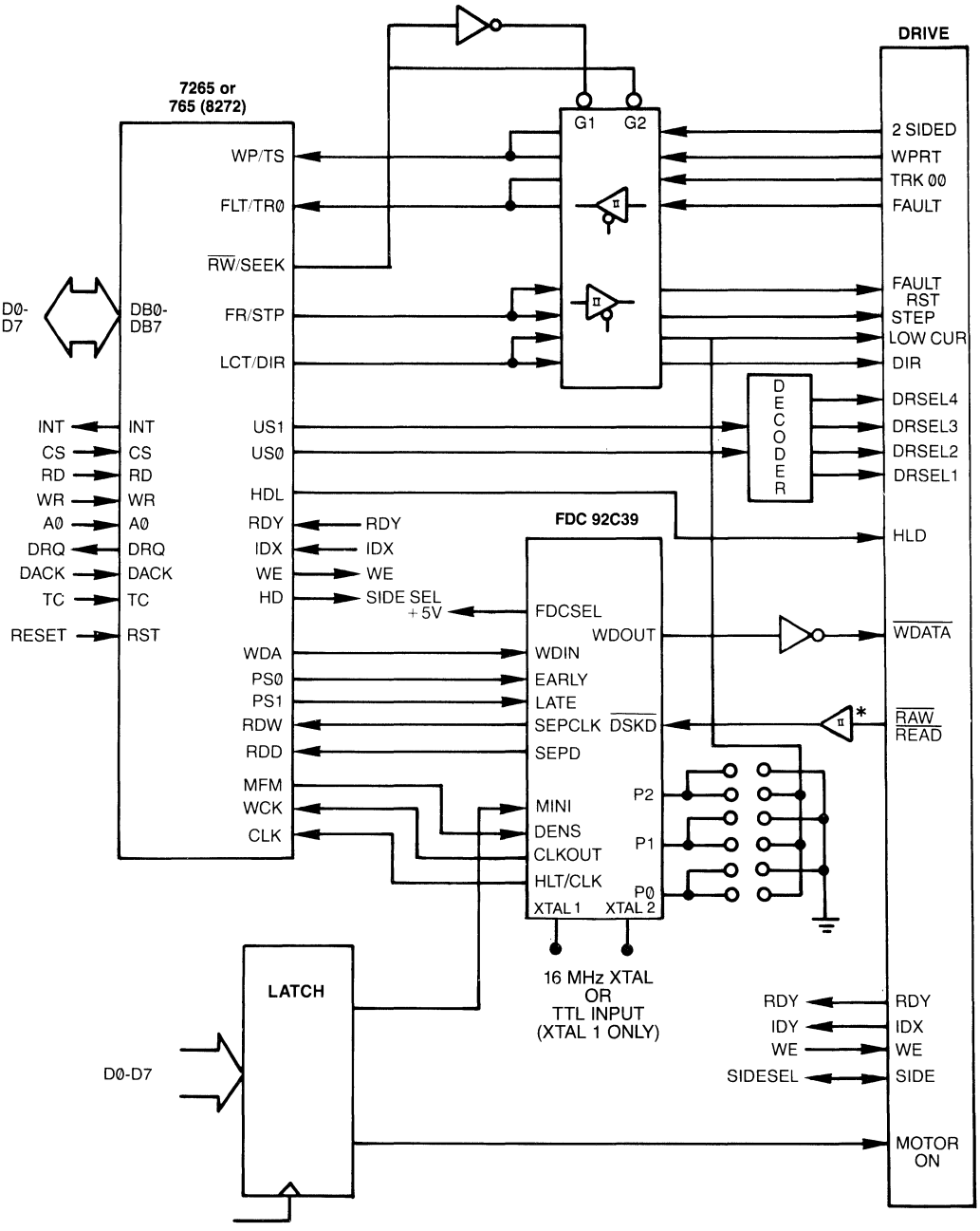


PRECOMPENSATION



Ref. to Fig. 2 for t_p (precompensation) value

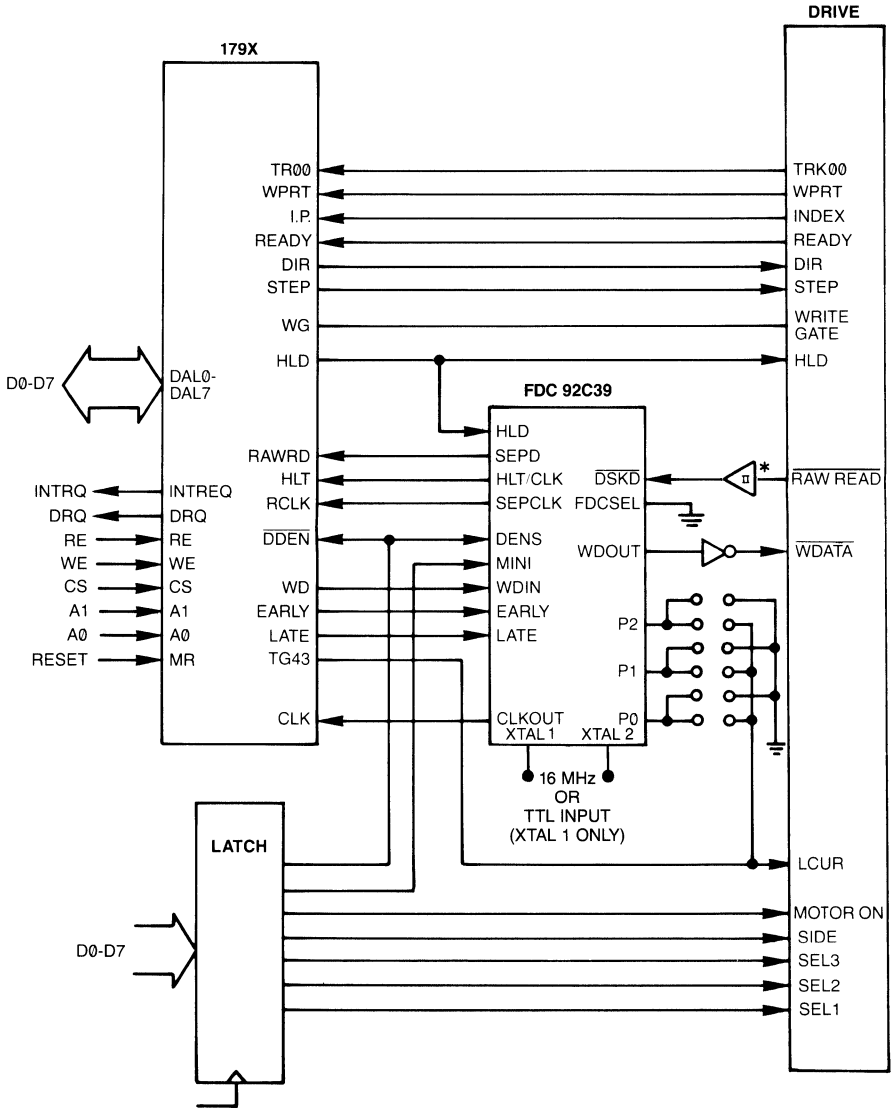
TYPICAL SYSTEM IMPLEMENTATION—765 (8272) FDC OR 7265 FDC



*The FDC 92C39/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{\text{DSKD}}$ input to the FDC 92C39/B.

TYPICAL SYSTEM IMPLEMENTATION—179X FDC OR 979X FDC



*The FDC 92C39/B, as all other CMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{\text{DSKD}}$ input to the FDC 92C39/B.

STANDARD MICROSYSTEMS CORPORATION

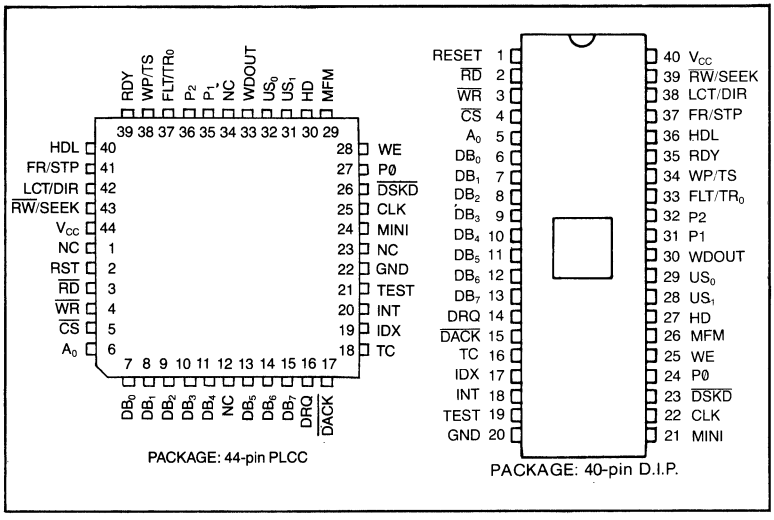
FDC 9266

Single/Double Density Enhanced Floppy Disk Controller

FEATURES

- ☐ Combination Floppy Disk Controller and Floppy Disk Interface
- ☐ Software compatible with industry standard FDC 765A
- ☐ On chip digital data separator eliminates critical analog adjustments
- ☐ On-chip drive control logic reduces component count.
- ☐ IBM compatible in both single and double density recording formats
- ☐ Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- ☐ Multi-sector and multi-track transfer capability
- ☐ Controls up to 4 floppy disk drives
- ☐ Data Scan Capability–will scan a single sector or entire track's worth of data fields, comparing on a byte by byte basis, data in the processor's memory with the data read from the diskette
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Single 8 MHz TTL clock input
- ☐ Single +5 Volt power supply
- ☐ Parallel Seek operations on up to four drives
- ☐ Compatible with most microprocessors
- ☐ COPLAMOS® n-channel silicon gate technology
- ☐ Available in 40-pin Dual-in-Line package and 44-pin PLCC

PIN CONFIGURATION



GENERAL DESCRIPTION

The FDC 9266 is a monolithic combination of the industry standard FDC 765A Floppy Disk Controller and the FDC 9229 Floppy Disk Interface Circuit. It preserves all of the processor hardware and software interfaces to the FDC 765A, and contains on-chip circuitry to simplify drive interfacing.

These on-chip enhancements include a digital data separator, compatible with 5.25″ and 8″ drives. The data separator separates both FM (Single Density) and MFM (Double Density) encoded data, and requires no external adjustments.

The FDC 9266 also allows variable write precompensation, which is track selectable.

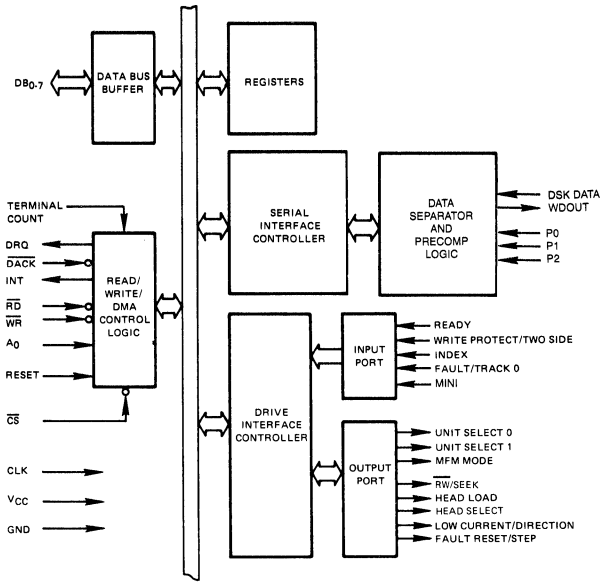
These enhancements greatly reduce the number of components required to interface floppy disks to a microprocessor system.

There are 15 separate commands which the FDC 9266 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

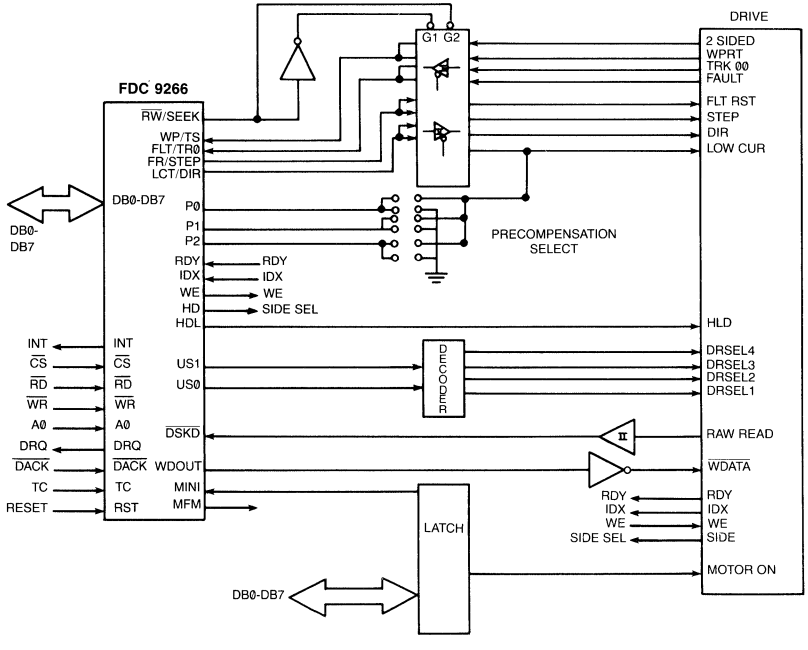
Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC which simplifies the read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The FDC 9266 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

SECTION VI



BLOCK DIAGRAM



TYPICAL APPLICATION

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.①	SYMBOL	NAME			
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input②	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input②	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input②	Processor	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input② Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	TEST	Test	Input		This pin is for test purposes only. Should be left tied high in normal operation.
20	GND	Ground			D.C. Power Return.
21	MINI	Mini	Input	Processor	This input, when set to "1" (high), configures the FDC for operation with 5.25" floppies. If reset to "0" (low), then the FDC is configured for 8" drive operation.
22	CLK	8 MHz TTL Clock	Input		Device clock.
23	$\overline{DSKD}$	Raw Data	Input	FDD	Raw data from drive.
24,31,32	P0, P1, P2	Precompensation Select	Input	Processor	These pins select the amount of precompensation applied to the write data.
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output		MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high). Head 2 selected when "0" (low).
28, 29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WD OUT	Write Data Out	Output	FDD	Serial clock and data bits to FDD.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.

NOTES: ① For DIP package.
② Disabled when $\overline{CS}$=1.

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO. ①	SYMBOL	NAME			
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/ write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Stop	Output	FDD	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on tracks $\geq$42 in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/ Write mode selected.
40	V_{CC}	+5V			DC Power.

NOTES: ① For DIP package. ② Disabled when $\overline{CS}$=1.

DESCRIPTION OF INTERNAL REGISTERS

The FDC 9266 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC 9266.

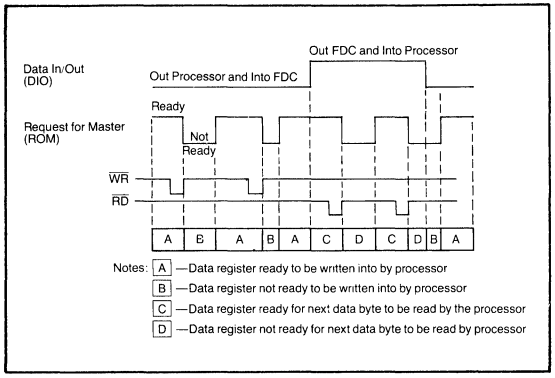
The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



COMMAND SEQUENCE

The FDC 9266 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC 9266 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

INSTRUCTION SET ① ②

READ DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

WRITE DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ ID

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								

FORMAT A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								

SCAN EQUAL

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

INSTRUCTION SET (CONT.)

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior
	W	H	Command execution
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after
	R	ST 1	Command execution
	R	ST 2	
	R	C	Sector ID information after
	R	H	Command execution
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X 'X X X HD US1 US0	
	W	C	Sector ID information prior
	W	H	Command execution
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after
	R	ST 1	Command execution
	R	ST 2	
	R	C	Sector ID information after
	R	H	Command execution
	R	R	
	R	N	

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	STO	Status information at the end
	R	PCN	of seek-operation about the FDC
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT → ← HUT	
	W	HLT → ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

FUNCTIONAL DESCRIPTION OF COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

SECTION VI

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

Format	Sector Size	N	SC	GPL①	GPL②③
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode ④	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode ④	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF

Table 3

Notes: ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC 9266 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BITS 5	INTERRUPT CODE BIT 6	INTERRUPT CODE BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms).The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC 9266 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC 9266 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

SECTION VI

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
D_7 D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	

BIT NO.	NAME	SYMBOL	DESCRIPTION
			STATUS REGISTER 1(CONT.)
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Errror	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
			STATUS REGISTER 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			STATUS REGISTER 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC 9266. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC 9266. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC 9266 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC 9266 is in the NON-DMA Mode, then the receipt of each data byte (if FDC 9266 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC 9266 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC 9266 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC 9266 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The FDC 9266 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

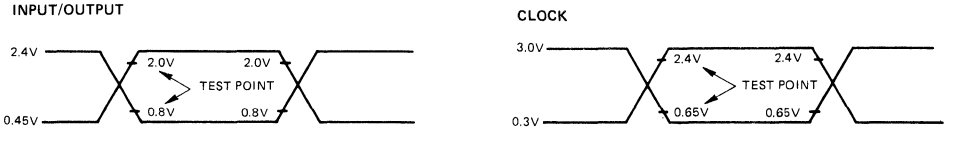
The bytes of data which are sent to the FDC 9266 to form the Command Phase, and are read out of the FDC 9266 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC 9266, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC 9266 is ready for a new command.

POLLING FEATURE OF THE FDC 9266

After the Specify command has been sent to the FDC 9266, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC 9266 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC 9266 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC 9266 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

SECTION VI

AC TEST CONDITION



AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

PRECOMPENSATION

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive.

P2	P1	P0	PRECOMP VALUE
0	0	0	0 NS
0	0	1	125 NS
0	1	0	250 NS
0	1	1	375 NS*
1	0	0	500 NS*

WRITE PRECOMPENSATION VALUE SELECTION

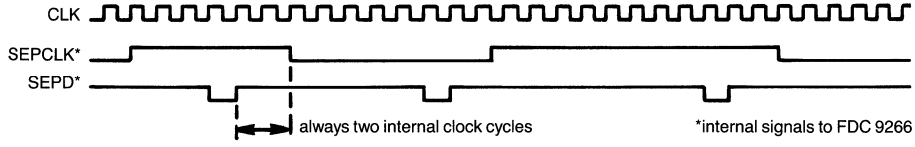
*NOTE: Precomp values of 375 ns and 500 ns are valid only with 5¼" drives.

DATA SEPARATOR

The FDC 9266 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the internal SEPCLK signal.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the CLK frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −200 µA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\phi)}$	−0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			200	mA	
Input Load Current (All Input Pins)	I_{LI}			10	µA	V_{IN} = V_{CC}
				−10	µA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	µA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	µA	V_{OUT} = +0.45V

NOTE: ①Typical values for T_a = 25°C and nominal supply voltage.

DC CHARACTERISTICS T_a = 25°C; f_c = 1 MHz; V_{CC} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

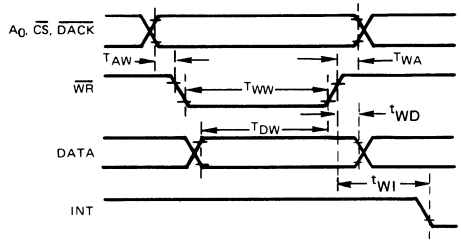
AC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Clock Period	ϕ_{CY}	120	125	130	ns	
Clock Active (High, Low)	ϕ_0	40			ns	
Clock Rise Time	ϕ_r			20	ns	
Clock Fall Time	ϕ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pF
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			µs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	1			ϕ_{CY}	
Reset Width	T_{RST}	14			ϕ_{CY}	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			µs	8 Mhz Clock Period Mini=0 16 MHz Clock Period Mini=1
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			µs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			µs	
$US_{0,1}$ Hold Time from FAULT RESET/ STEP ↑	T_{STU}	5.0			µs	
STEP Active Time (High)	T_{STP}	6.0	7.0		µs	
STEP Cycle Time	T_{SC}	33	②	②	µs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	µs	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			µs	8 MHz Clock Period Mini=0 16 MHz Clock Period Mini=1
Seek Hold Time from DIR	T_{DS}	30			µs	
DIR Hold Time after STEP	T_{STD}	24			µs	
Index Pulse Width	T_{IDX}	10			ϕ_{CY}	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	8 MHz Clock Period Mini=0 16 MHz Clock Period Mini=1
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	µs	

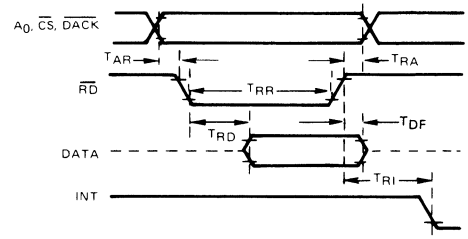
NOTES: ① Typical values for T_a = 25°C and nominal supply voltage.
② Under Software Control. The range is from 1 ms to 16 ms for 8" floppies, and 2 to 32 ms for 5¼" floppies.

TIMING DIAGRAMS

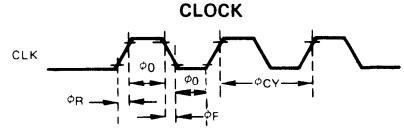
PROCESSOR WRITE OPERATION



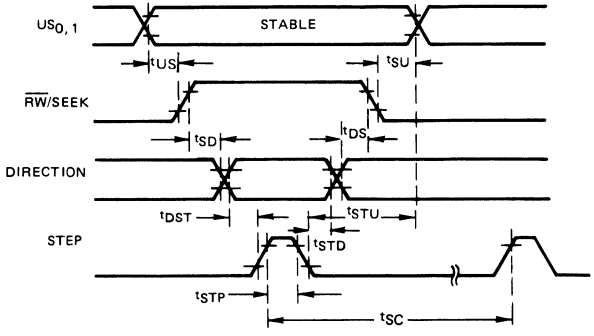
PROCESSOR READ OPERATION



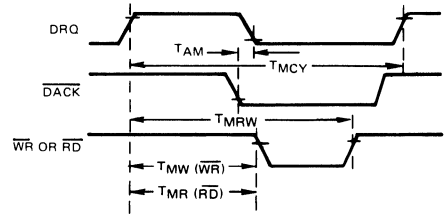
CLOCK



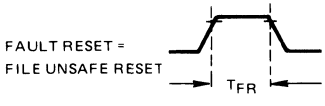
SEEK OPERATION



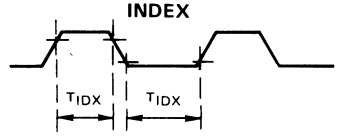
DMA OPERATION



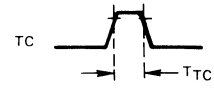
FLT RESET



INDEX



TERMINAL COUNT



RESET

For more information, please consult:
Technical Note 6-1 (Digital Data Separation)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

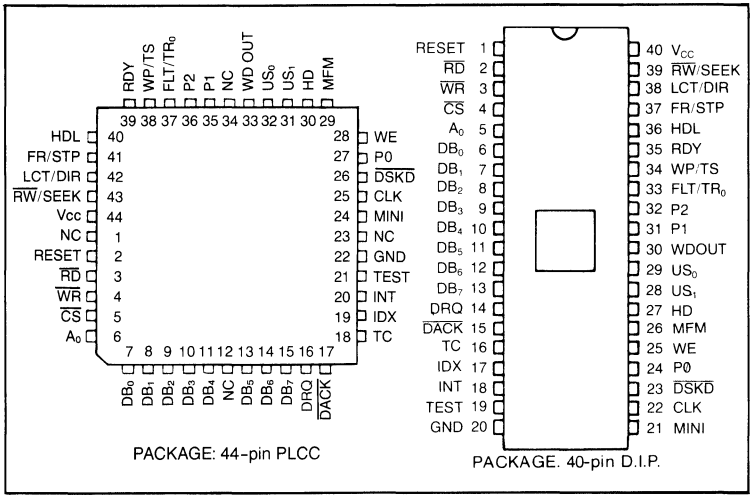
FDC 9268

Quad Density Integrated Floppy Disk Controller

FEATURES

- ☐ Combination Floppy Disk Controller, Data Separator and Precompensation Generator
- ☐ Software compatible with industry standard FDC 765A
- ☐ On chip high resolution digital data separator eliminates critical analog adjustments
- ☐ 500, 300, 250, 125 Kb/s Data Rates
- ☐ IBM compatible in both single, double and quad density recording formats
- ☐ Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- ☐ Multi-sector and multi-track transfer capability
- ☐ Controls up to 4 floppy disk drives
- ☐ Data Scan Capability—will scan a single sector or entire track's worth of data fields, comparing on a byte by byte basis, data in the processor's memory with the data read from the diskette
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Single 16 MHz TTL clock input
- ☐ Parallel Seek operations on up to four drives

PIN CONFIGURATION



- ☐ Compatible with most microprocessors
- ☐ COPLAMOS® n-channel silicon gate technology
- ☐ Single +5 Volt power supply
- ☐ Available in 40-pin Dual-In-Line and 44-pin PLCC packages.

SECTION VI

GENERAL DESCRIPTION

The FDC 9268 is a monolithic combination of the industry standard FDC 765A Floppy Disk Controller and the FDC 9239, a high performance Data Separator and Precompensation Generator. It preserves all of the processor hardware and software interfaces to the FDC 765A, and contains on-chip circuitry to simplify drive interfacing. The FDC 9268 contains the circuitry and control functions for interfacing a processor to four 3.5", 5.25", and 8" floppy-disk drives. It is capable of supporting either IBM 3740 single density format (FM), IBM System 34 Double Density format (MFM) or IBM quad density format, including double-sided recording. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the FDC 9268 which make DMA operation easy to incorporate with the aid of an external DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC 9268.

The FDC 9268 enhancements greatly reduce the number of components required to interface floppy disks to a microprocessor system. These on-chip enhancements include a digital data separator, compatible with 3.5", 5.25", and 8" floppy disk drives. The FDC 9268 separates both FM (Single Density) and MFM (Double Density) encoded data. The FDC uses a high performance 16-bit cell divide algorithm which produces significant improvements in soft error rates over existing designs. The FDC 9268's high performance is achieved without any external adjustments.

The FDC 9268 also allows variable write precompensation, which is track selectable.

There are fifteen separate commands which the FDC 9268 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC which simplifies the read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The FDC 9268 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

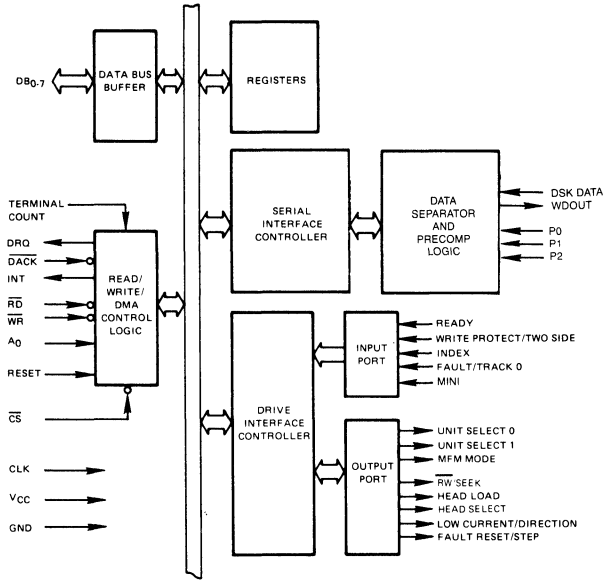


FIGURE 1: BLOCK DIAGRAM

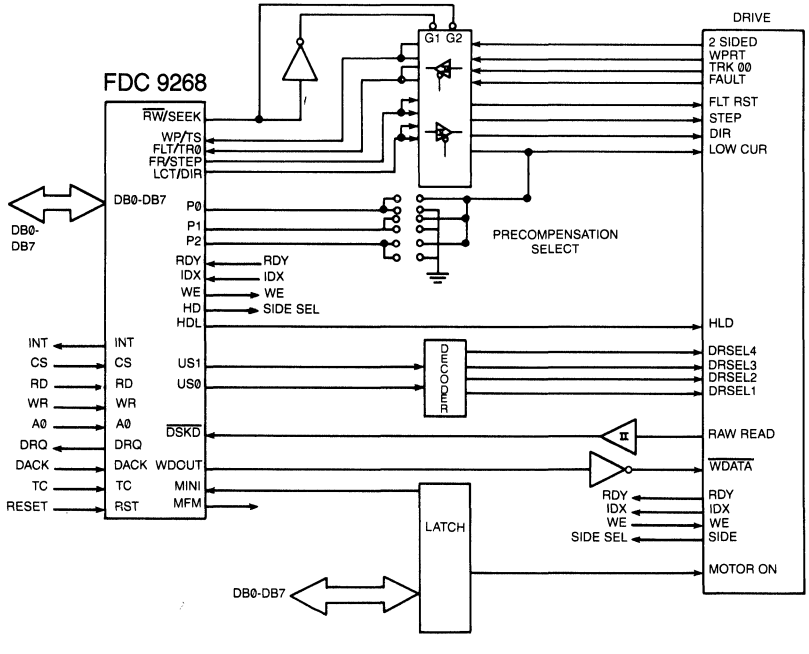


FIGURE 2: TYPICAL APPLICATION

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input①	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input①	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input①	Processor	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input① Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRW = "1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	TEST	Test	Input		This pin is for test purposes only. Should be left tied high in normal operation.
20	GND	Ground			D.C. Power Return.
21	MINI	Mini	Input	Processor	This input, when set to "1" (high), configures the FDC for operation with 250 Kb/s. If reset to "0" (low), then the FDC is configured for 500 Kb/s operation (MFM mode).
22	CLK	16 MHz TTL Clock	Input		Device clock.
23	$\overline{DSKD}$	Raw Data	Input	FDD	Raw data from drive.
24,31,32	P0, P1, P2	Precompensation Select	Input	Processor	These pins select the amount of precompensation applied to the write data.
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output		MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high). Head 2 selected when "0" (low).
28, 29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WD OUT	Write Data Out	Output	FDD	Serial clock and data bits to FDD.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/ write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Stop	Output	FDD	Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks $\geq$ 42 in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/ Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: ① Disabled when CS = 1.

DESCRIPTION OF INTERNAL REGISTERS

The FDC 9268 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC 9268.

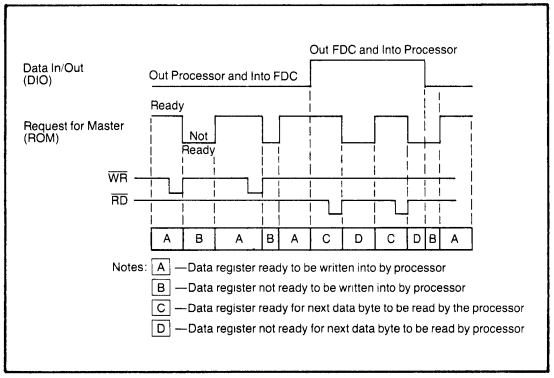
The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



COMMAND SEQUENCE

The FDC 9268 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC 9268 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	Number of data bytes written in a Sector = $128 * 2^N$.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

INSTRUCTION SET ① ②

READ DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

WRITE DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

READ ID

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								

FORMAT A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								

SCAN EQUAL

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

INSTRUCTION SET (CONT.)

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior
	W	H	Command execution
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after
	R	ST 1	Command execution
	R	ST 2	
	R	C	Sector ID information after
	R	H	Command execution
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior
	W	H	Command execution
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after
	R	ST 1	Command execution
	R	ST 2	
	R	C	Sector ID information after
	R	H	Command execution
	R	R	
	R	N	

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	STO	Status information at the end
	R	PCN	of seek operation about the FDC
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT → HUT	
	W	HLT → ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

FUNCTIONAL DESCRIPTION OF COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

For more information, please consult: Technical Note 6.6 (Programming the FDC 765A, 9266, 9267, 9268)

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

Format/ Transfer Rate	Sector Size	N	SC	GPL①	GPL ②③
8" Standard Floppy					
	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
FM Mode	512	02	08	1B	3A
250 KB/s	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	256	01	1A	0E	36
	512	02	0F	1B	54
MFM	1024	03	08	35	74
Mode ④	2048	04	04	99	FF
500 KB/s	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
	128 bytes/sector	00	12	07	09
	128	00	10	10	19
FM Mode	256	01	08	18	30
125 KB/s	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
	256	01	12	0A	0C
	256	01	10	20	32
MFM	512	02	08	2A	50
Mode ④	1024	03	04	80	F0
250 KB/s	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk®					
	128 bytes/sector	0	0F	07	1B
FM Mode	256	1	09	0E	2A
125 KB/s	512	2	05	1B	3A
MFM	256	1	0F	0E	36
Mode ④	512	2	09	1B	54
250 KB/s	1024	3	05	35	74

TABLE 3

Notes: ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC 9268 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END	INTERRUPT CODE		
BITS 5	BIT 6	BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms).The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 22). Times indicated above are for an 16 MHz clock, if the clock was reduced to 8 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC 9268 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC 9268 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
D_7 D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	

BIT NO.	NAME	SYMBOL	DESCRIPTION
			STATUS REGISTER 1(CONT.)
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Errror	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
			STATUS REGISTER 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			STATUS REGISTER 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC 9268. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC 9268. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC 9268 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC 9268 is in the NON-DMA Mode, then the receipt of each data byte (if FDC 9268 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC 9268 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC 9268 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC 9268 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The FDC 9268 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the FDC 9268 to form the Command Phase, and are read out of the FDC 9268 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC 9268, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC 9268 is ready for a new command.

POLLING FEATURE OF THE FDC 9268

After the Specify command has been sent to the FDC 9268, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC 9268 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC 9268 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC 9268 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

SECTION VI

AC TEST CONDITION

AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

FDC 9268 COMPATIBILITY

The FDC9268 is software and hardware compatible with the FDC9266 with the following qualifications pertaining to Precomp and clock input.

-A 16 MHz clock is used on the FDC9268.

-The precomp specifications for the FDC9267 and FDC9266 can be used for the FDC9268 with the following qualification. Whenever the precomp select line P_2 is active, the FDC9268 uses the maximum precomp available in that mode (i.e. 375 nsec in the 250 Kb/s mode and 187.5 nsec in the 500 Kb/s mode).

MINI	P_2	P_1	P_0	PRECOMP VALUE (nsec)
1	0	0	0	0
1	0	0	1	125.0
1	0	1	0	250.0
1	0	1	1	375.0
1	1	0	0	375.0
1	1	0	1	375.0
1	1	1	0	375.0
1	1	1	1	375.0
0	0	0	0	0
0	0	0	1	62.5
0	0	1	0	125.0
0	0	1	1	187.5
0	1	0	0	187.5
0	1	0	1	187.5
0	1	1	0	187.5
0	1	1	1	187.5

Write Precompensation Value Selection

ELECTRICAL CHARACTERISTICS

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −200 µA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\phi)}$	−0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			200	mA	
Input Load Current (All Input Pins)	I_{LI}			10	µA	V_{IN} = V_{CC}
				−10	µA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	µA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	µA	V_{OUT} = +0.45V

NOTE: ①Typical values for T_a = 25°C and nominal supply voltage.

DC CHARACTERISTICS T_a = 25°C; f_c = 1 MHz; V_{CC} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	COMMENTS
Clock Period	ϕ_{CY}	60	62.5	250	ns	
Clock Active (High, Low)	ϕ_0	20			ns	
Clock Rise Time	ϕ_r			10	ns	
Clock Fall Time	ϕ_f			10	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pF
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			µs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	2 ③			ϕ_{CY}	
Reset Width	T_{RST}	28 ③			ϕ_{CY}	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			µs	16 MHz Clock Period
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			µs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			µs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	5.0			µs	
STEP Active Time (High)	T_{STP}	6.0	7.0		µs	
STEP Cycle Time	T_{SC}	33	②	②	µs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	µs	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			µs	16 MHz Clock Period
Seek Hold Time from DIR	T_{DS}	30			µs	
DIR Hold Time after STEP	T_{STD}	24			µs	
Index Pulse Width	T_{IDX}	20 ③			ϕ_{CY}	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	16 MHz Clock Period
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	µs	

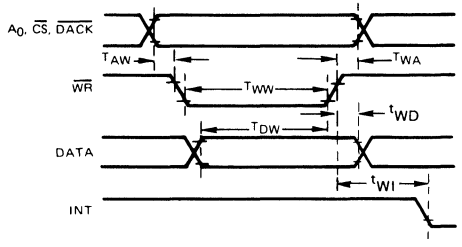
NOTES: 1 Typical values for T_0 = 25°C and nominal supply voltage.
2 Under Software Control. The range is from 1 ms to 16 ms for 500 Kb/s data rates, and 2 to 32 ms for 250 Kb/s data rates
3 When mini is active, (pin 21), these periods are doubled.

Data Separator Performance Specifications:

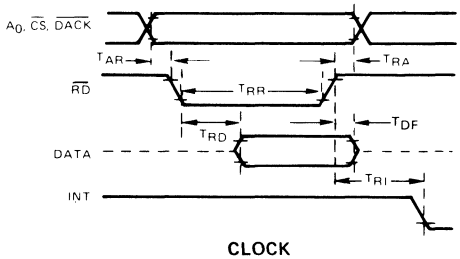
PARAMETER	MFM 500 KHz	MFM 250 KHz	UNITS
Bit Jitter			
Nominal Speed	±260	±540	nsec
+5% Speed	±260	±480	nsec
-5% Speed	±320	±640	nsec
Window Margin Early	490	980	nsec
Late	490	980	nsec

TIMING DIAGRAMS

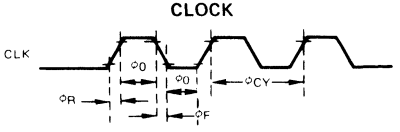
PROCESSOR WRITE OPERATION



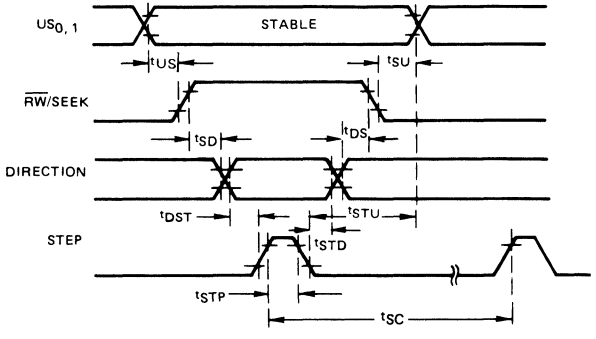
PROCESSOR READ OPERATION



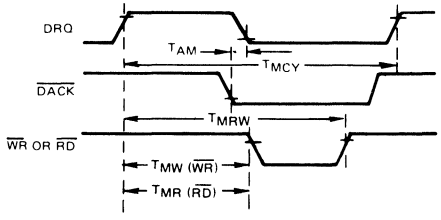
CLOCK



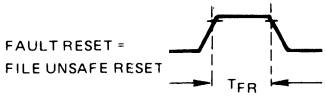
SEEK OPERATION



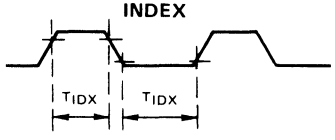
DMA OPERATION



FLT RESET

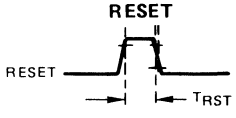


INDEX



TERMINAL COUNT

RESET



For more information, please consult:
Technical Note 6-1 (Digital Data Separation)
Technical Note 6-6 (Programming the FDC 765, 9266, 9267, 9268)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

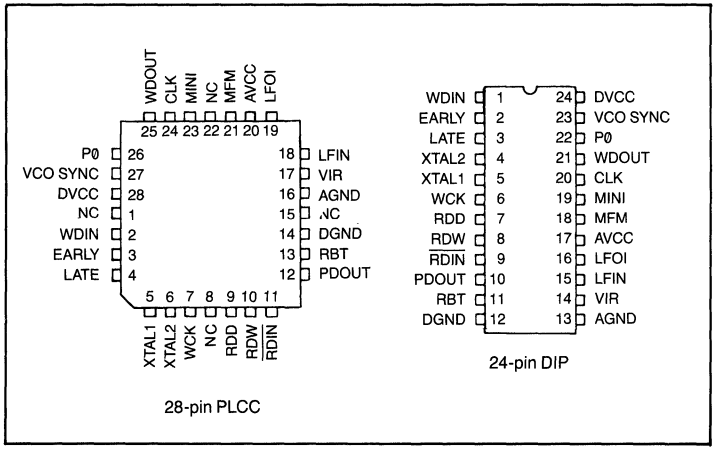
FDC92C81
PRELIMINARY

Self Tuning Analog Floppy Disk Data Separator (AFDDS)

FEATURES

- ☐ 1 Mb/s, 750, 500, 300, 250 and 125 Kb/s disk data rates
- ☐ Analog Data Separator performs complete data separation for floppy disk drives. Separates FM or MFM encoded data. 3½", 5¼" and 8" compatible.
- ☐ No adjustments necessary
- ☐ Provides clock for FDC765A
- ☐ High Performance Dual Gain Analog Phase Locked Loop
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator
- ☐ 300 Kb/s with clock frequency change and no filter change
- ☐ On-chip VCO
- ☐ Fabricated in Low Power CMOS
- ☐ TTL Compatible I/O
- ☐ Single +5V Supply

PIN CONFIGURATION

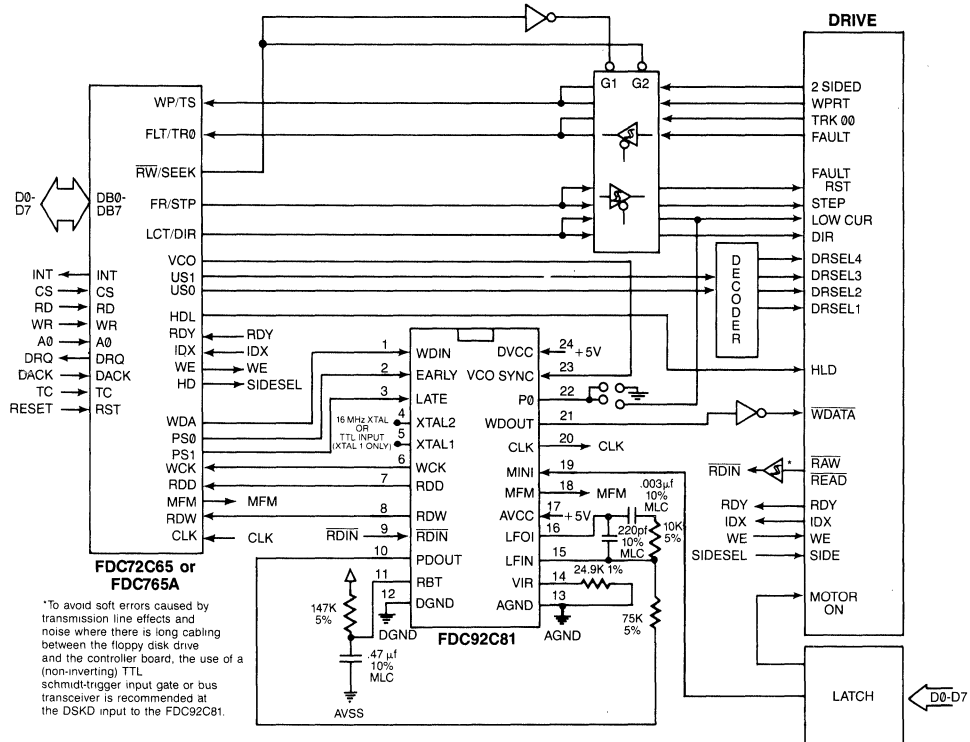


GENERAL DESCRIPTION

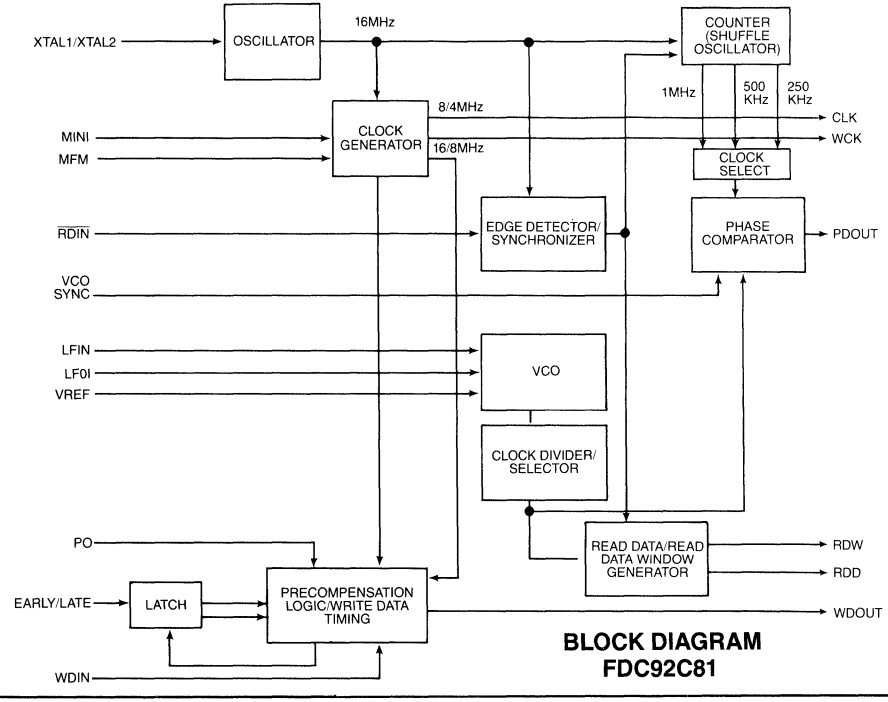
The FDC92C81 is a high performance CMOS Dual Gain Analog Floppy Disk Data Separator (AFDDS). The FDC92C81 is compatible with 3.5", 5.25" and 8" floppy disk drives, and provides all clocks required by the industry standard FDC765A and FDC72C65 floppy disk controllers.

The FDC92C81 incorporates all the active components necessary to implement analog floppy disk data separation, eliminating the need for discrete transistors. Only a crystal and a few external resistors and capacitors are required. Using the FDC92C81 and a floppy disk controller chip, a system designer can build a highly reliable, cost efficient double or single density floppy disk subsystem requiring no tuning adjustments.

Three different user selectable values for write precompensation assure reliable positioning of data when writing to disk.



TYPICAL SYSTEM IMPLEMENTATION



BLOCK DIAGRAM FDC92C81

TABLE 1—FDC92C81 DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	I/O	DESCRIPTION
1	Write Data In	WDIN	I	This input contains the serial clock and data bits which may be precompensated and output to the drive.
2	Early	EARLY	I	Used for precompensation. When high, the write data bit will be written early. Refer to table below.
3	Late	LATE	I	Used for precompensation. When high, the write data bit will be written late. EARLY LATE PULSE POSITION 0 0 nominal 1 0 early 0 1 late 1 1 not used
4 5	Crystal Crystal	XTAL2 XTAL1	O I	A 16.000 MHz parallel resonant crystal may be connected between XTAL1 and XTAL2. If a TTL signal is used in place of a crystal, the signal should be connected to XTAL1 while XTAL2 is left unconnected.
6	Write Clock	WCK	O	This output contains the clock which controls the rate at which data is written to the drive. See table for MINI pin.
7	Read Data	RDD	O	This output contains the reclocked encoded bit stream from the drive.
8	Read Data Window	RDW	O	This output is a function of the internal VCO frequency which tracks and properly frames the encoded drive bit stream for reliable clocking into the floppy disk controller.
9	Read Data In	$\overline{\text{RDIN}}$	I	This input is the read data from the floppy disk drive. The input is active low. The leading edge (high to low transition) is used for all frequency tracking operations.
10	Phase Detect Out	PDOUT	O	The output of the phase detect circuit. A 75K 5% resistor is connected between this output and LFIN.
11	Bias Reference	RBT	I	An external 147K 5% resistor connected between this pin and AVCC establishes a bias reference current for the VCO. This input should not be forced low.
12	Digital Ground	DGND		Digital Ground
13	Analog Ground	AGND		Analog Ground
14	Voltage to Current Reference	VIR	I	A 24.9K 1% metal film resistor connected between this pin and AVSS establishes a current reference for the on-chip voltage to current converter which is part of the VCO.
15	Low-pass Filter In	LFIN	I	This is the input to the low pass filter amplifier. A resistor is connected between this input and PDOUT and a low pass filter is connected between this input and LFOI.
16	Low-pass Filter	LFOI	I/O	This pin is the output of the low pass filter amplifier and the input to the VCO.
17	Analog Vcc	AVCC		+5V analog power supply
18	MFM Mode	MFM	I	When this input is high, the chip is in MFM mode. When low, the chip is in the FM mode.
19	MINI	MINI	I	This input, along with the input PØ specifies the amount of precompensation to be used. See table for the PØ pin. This input along with MFM controls the CLK and WCK outputs. MFM MINI WCK CLK 0 0 500KHz 8MHz 0 1 250KHz 4MHz 1 0 1MHz 8MHz 1 1 500KHz 4MHz
20	Clock	CLK	O	This output is a 4MHz or 8MHz clock. See table above.
21	Write Data Out	WDOUT	O	This output is the precompensated serial write data to the floppy disk drive.

TABLE 1—FDC92C81 DESCRIPTION OF PIN FUNCTIONS CONTINUED

PIN NO.	NAME	SYMBOL	I/O	DESCRIPTION
22	Precompensation	PØ	I	This input along with the MINI input specifies the amount of precompensation to be used. MINI PO PRECOMP 0 0 0.0ns 0 1 62.5ns 1 0 0.0ns 1 1 125.0ns
23	VCO Sync	VCO SYNC	I	VCO locks to clock when low and to data when high.
24	Digital Vcc	DVCC		+5V digital power supply.

MODE GAIN IMPLEMENTATION

The phase locked loop gain of the FDC92C81 is controlled by switching between two modes of operation, shuffle oscillator and arm on data. The mode change is via VCO SYNC. The shuffle oscillator mode is considered the high gain mode and the arm on data mode is considered the low gain mode.

Arm On Data Mode

The purpose of the arm on data mode is to reduce the gain so that the chip can handle higher amounts of bit jitter. In this mode, each code bit received from the drive resets the phase compare circuits and a counter (shuffle oscillator). The phase compare circuits are only armed for one compare cycle after each code bit. The counter is set such that ¼ bit cell after the phase compare reset has gone away, it creates an edge. (Only one compare is performed until the next code bit is received.) This edge is compared against the edges of the VCO by the phase compare circuits. The relationship between these edges is used to generate one pump-up or pump-down signal. Therefore, in this mode, each code bit causes only one update to the loop.

Shuffle Oscillator Mode

The shuffle oscillator mode allows for a fast lock to data time when attempting to acquire data synchronization. In this mode, each code bit received from the drive resets the phase compare circuits and a counter (shuffle oscillator). The phase compare circuits are always armed. The counter is set such that ¼ bit cell after the phase compare reset has gone away, it creates an edge. Each ½ bit cell thereafter creates an edge until reset by another code bit. This edge is compared against the edges of the VCO by the phase compare circuits. The relationship between these edges is used to generate pump-up/pump-down signals. In MFM codes, the minimum spacing between code bits is one bit cell, the maximum spacing is two bit cells. Therefore, in this mode, each code bit can cause up to four updates to the loop. This is how the gain of the loop is increased.

TYPICAL PERFORMANCE SPECIFICATIONS

PARAMETER	500KHz	300KHz	250KHz	UNITS
Bit Jitter				
Nominal Speed	380	620	760	nsec
+5% Speed	360	600	740	nsec
−5% Speed	380	660	840	nsec
Window Margin				
Early	480	800	860	nsec
Late	400	720	820	nsec

Lock to Encoded Data	less than 3 bytes

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.3V
Negative Voltage on any Pin, with respect to Ground ..... −0.3V
Power Dissipation 0.25W
Positive Voltage on V_{CC} Pin, with respect to Ground 7.0V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power supply line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS TA = 0°C to 70°C, V_{CC} = 5.0V ±5% unless otherwi

PARAMETERS	MIN	TYP	MAX	UNITS	COMME
INPUT VOLTAGE					WDIN, EARLY, LATE, RDIN, PØ, SYNC
High Level V_{IL}	−0.3		0.8	V	
High Level V_{IH}	2.0		(VCC)	V	
INPUT VOLTAGE					XTAL 1, XTAL 2
Low level V_{IL}	−0.3		0.8	V	
High Level V_{IH}	3.2		(VCC)	V	
OUTPUT VOLTAGE					CLK, WCK, RDD, RDW, MFM, MINI, WDOUT
Low Level V_{OL}			0.4	V	I_{OL} = 1.6mA except CLK
					I_{OL} = 0.4mA, CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100uA except CLK
					I_{OH} = −400uA, CLK only
POWER SUPPLY CURRENT I_{CC}			TBD	mA	
INPUT LEAKAGE CURRENT I_{IL}			TBD	uA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE					WDIN, EARLY, LATE, RDIN, PØ, SYNC, XTAL 1
C_{IN}		TBD		pF	

AC ELECTRICAL CHARACTERISTICS TA = 0°C to 70°C, V_{CC} = 5.0V ±5% unless otherw

PARAMETERS	SMBL	MIN	TYP	MAX	UNIT	LOAI	
Read data width	T_1	40			ns	20pf	
Window setup time	T_2	15			ns	20pf	
Window hold time	T_3	15			ns	20pf	
Window cycle time	T_4		2		us	20pf	MFM = 0 MINI = 0
			1		us		MFM = 1 MINI = 0
			4		us		MFM = 0 MINI = 1
			2		us		MFM = 1 MINI = 1
WCK high	T_5	80	250	350	ns	20pf	
WCK cycle time	T_6		4		us	20pf	125KHz data rate
			2		us	20pf	250KHz data rate
			1		us	20pf	500KHz data rate
CLK high	T_7	40			ns	20pf	
CLK low	T_8	40			ns	20pf	
CLK period	T_9	120		500	ns	20pf	
WDOUT width	T_{9a}	250	315	350	us	20pf	x2 if mini = 1
CLK ↑ to WCK ↑ delay	T_{10}	0		40	ns		

SECTION VI

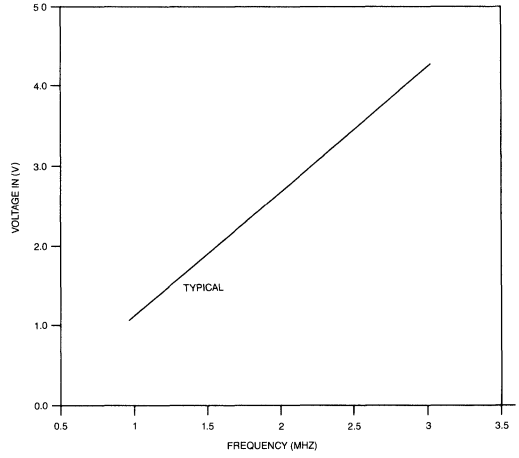
AC ELECTRICAL CHARACTERISTICS CONTINUED

PARAMETERS	SMBL	MIN	TYP	MAX	UNIT	LOAD	COM.
CLK ↑ to WCK ↓ delay	T_{11}	0		40	ns		
WDOUT early rising edge to WDOUT nom. rising edge	T_{12}	Desired Precomp Value					see table for pin 22
WDOUT nom. rising edge to WDOUT late rising edge	T_{13}	Desired Precomp Value					see table for pin 22
Pre-shift delay time from WCK positive edge	T_{14}	20		100	ns		
WDIN delay time rising edge of WCK to rising edge of WDIN, falling edge of WCK to falling edge of WDIN	T_{15}	20		100	ns		
WDIN width	T_{16}	30	200	300	ns		
Read data width	T_{17}	100			ns		
Read data cycle time	T_{18}		2 2 4 4		us us us us		500 Kb/s MFM, 250 Kb/s FM 250 Kb/s MFM, 125 Kb/s FM

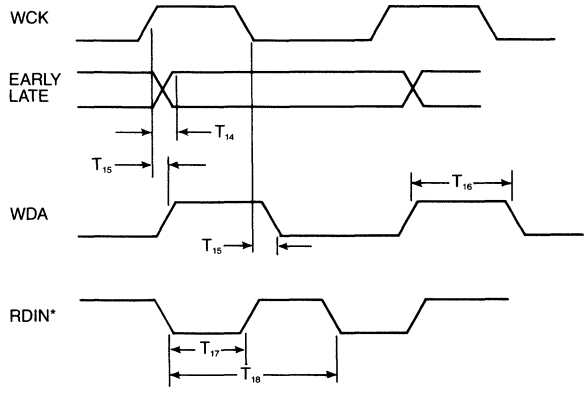
The following inputs are DC levels: MFM, MINI, P_0.

TYPICAL VCO VOLTAGE IN VS. FREQUENCY

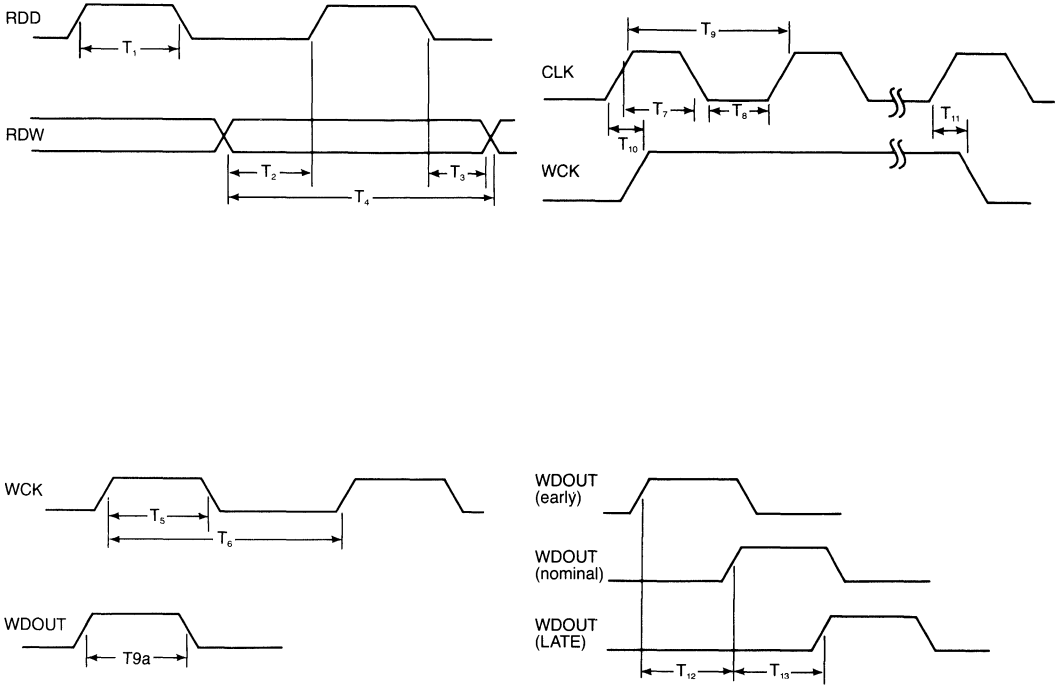
FDC92C81



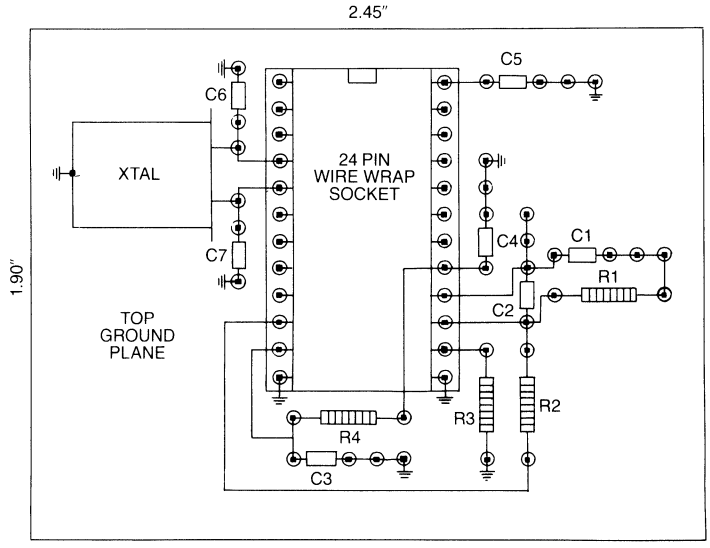
INPUT TIMING



OUTPUT TIMING



NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

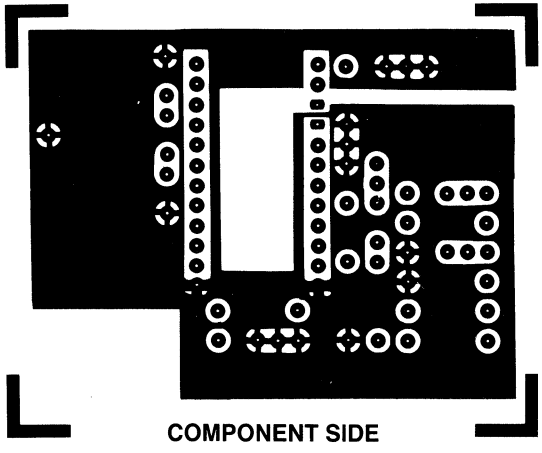


RESISTOR VALUES	
R1	10K 5%
R2	75K 5%
R3	24.9K 1% metal film
R4	147K 5%

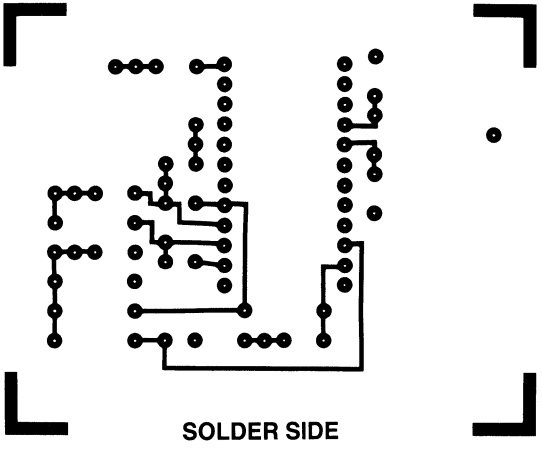
CAPACITOR VALUES	
C1	.003 uf 10% MLC
C2	220 pf 10% MLC
C3	.47 uf 10% MLC
C4	.22 uf 10%
C5	.22 uf 10%
C6	60 pf 10%
C7	60 pf 10%

REDUCE TO 2.500 ±.005"

REDUCE TO 2.500 ±.005"



COMPONENT SIDE



SOLDER SIDE

NOTE: The printed circuit board artwork shown above is included for illustration only. Camera ready artwork is available through your SMC representative or regional sales office.

Blank PC boards (based on the illustrations above) are also available to facilitate evaluation and design. Contact your SMC representative or regional sales office for more information.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge N.Y. 11788
(516) 273 3100 TWX 510 227 8698

STANDARD MICROSYSTEMS CORPORATION

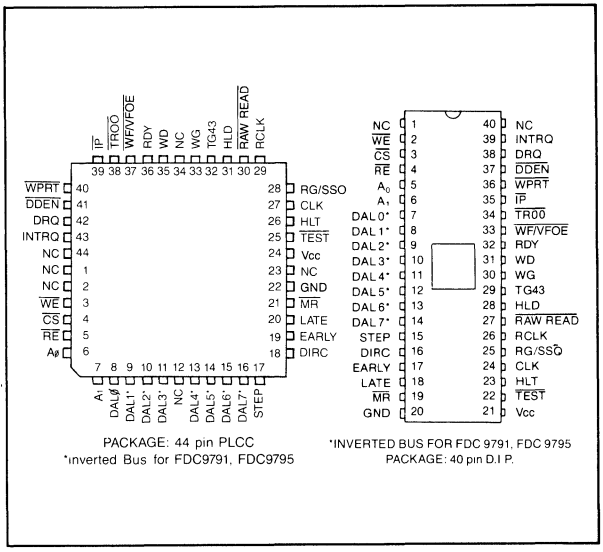
FDC 9791
FDC 9793
FDC 9795
FDC 9797
μPC FAMILY

Floppy Disk Controller/Formatter FDC

FEATURES

- ☐ +5 VOLT ONLY VERSION OF FDC179X-02
- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 9795, FDC 9797)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



PACKAGE: 44 pin PLCC
*inverted Bus for FDC9791, FDC9795

*INVERTED BUS FOR FDC 9791, FDC 9795
PACKAGE: 40 pin D.I P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FDC 179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 979X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 979X chip design has evolved into four specific parts: FDC 9791, FDC 9793, FDC 9795, and the FDC 9797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

The FDC 9791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 9791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 9793 is identical to the FDC 9791 except the DAL lines are TRUE for systems that utilize true data busses.

The FDC 9795 adds side select logic to the FDC 9791. The FDC 9797 adds the side select logic to the FDC 9793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

SECTION VI

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Hard Disk

Part Number	Disk Format	Data Encoding	Max. Disk Data Transfer Rate	Hard Disk Data Separator	Power Supply	Package	Page
MSD 95C00	SCSI	RLL 2,7/MFM/NRZ/GCR	20 Mb/sec	external	+5V	68 PLCC	681-692
MSD 95C02	User Defined	RLL 2,7/MFM/NRZ/GCR	24 Mb/sec	external	+5V	68 PLCC	693-736
MSD 7262	ESDI	NRZ	18 Mb/sec	external	+5V	40 DIP	677-680
HDC 9234	IBM® PC/AT®, ST-506	MFM, FM	5 Mb/sec	external	+5V	40 DIP, 44 PLCC	637-676
HDC 92C26	ST-506	MFM, FM	5 Mb/sec	Analog, external VCO	+5V	24 DIP, 28 PLCC	627-634
HDC 9223	ST-506	MFM, FM	5 Mb/sec	VCO only	+5V	14 DIP	585-588
HDC 9224	DEC VAX®, MICROVAX®, ST-506	MFM, FM	5 Mb/sec	external	+5V	40 DIP, 44 PLCC	589-624
HDC 92C27	ST-506	MFM, FM	5 Mb/sec	Analog, external VCO	+5V	28 DIP, 28 PLCC	635-636
HDC 92C25	ST-506	MFM, FM	5 Mb/sec	external	+5V	48 DIP	625-626
HDC 7261	NEC ST-506	MFM, FM	12 Mb/sec	external	+5V	40 DIP	583-584
HDC 7260	NEC ST-506	MFM, FM	6 Mb/sec	external	+5V	40 DIP	579-582
HDC 1100-01, -12, -03, -05	SA1000, ST-506	NRZ, MFM, FM	5 Mb/sec	external	+5V	20 DIP	569-578

STANDARD MICROSYSTEMS CORPORATION

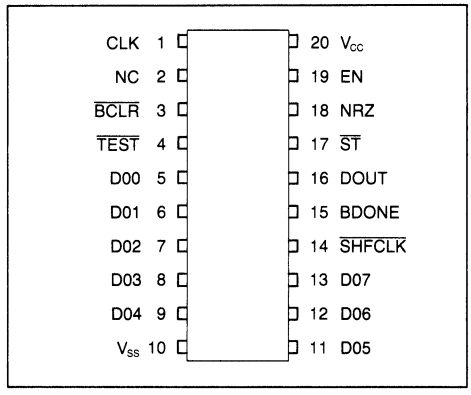
HDC 1100-01
PRELIMINARY

Hard Disk Serial to Parallel Converter

FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 MBit Shift Rate
- ☐ Serial Input/Parallel Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

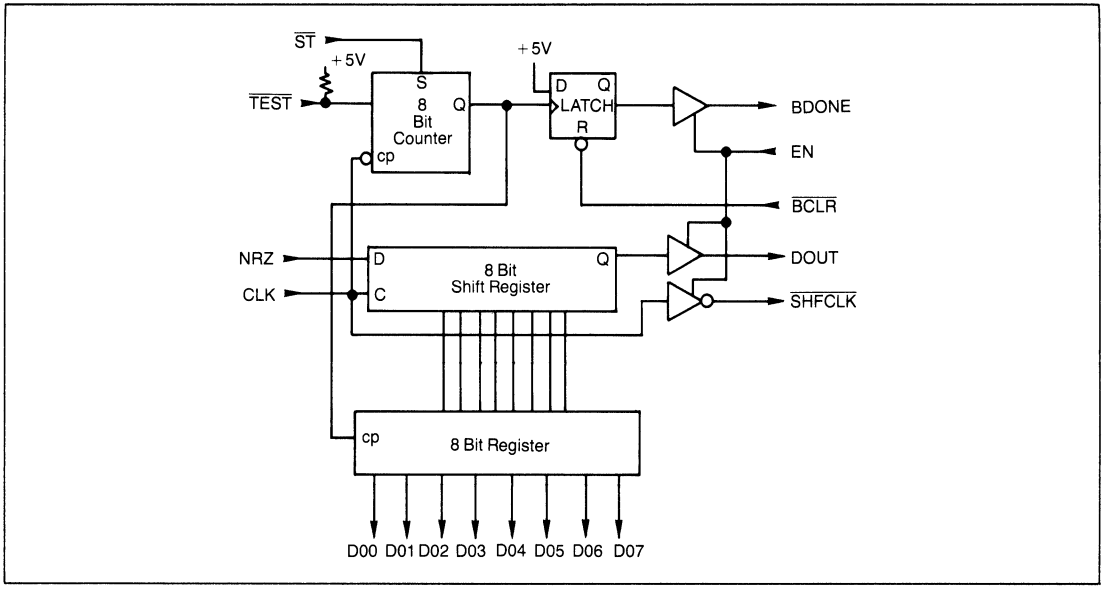
PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-01 converts NRZ data from a Winchester disk drive into eight bit parallel form. Additional inputs are provided to initiate the conversion process, as well as output strobes to indicate the completion.

The HDC 1100-01 contains two sets of 8 bit registers. This allows one register to be read (in parallel) while serial data is being shifted into the other.



SECTION VII

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd · Hauppauge N.Y. 11788
(516) 273-3100 · TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

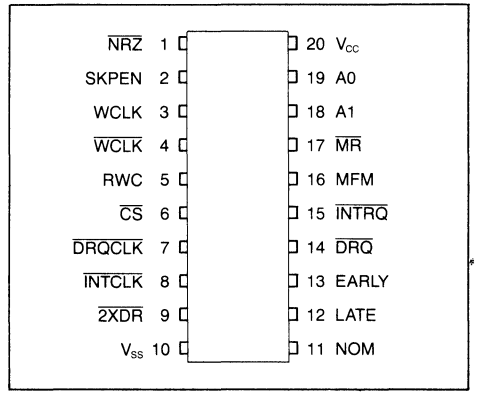
HDC 1100-12
PRELIMINARY

Hard Disk Improved MFM Generator

FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Write Precompensation
- ☐ Address Mark Generation
- ☐ 5 Mbit Data Rate
- ☐ Converts NRZ to MFM
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION

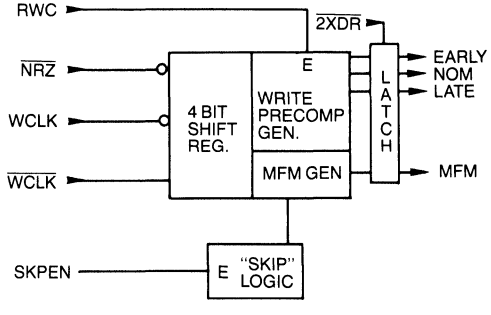


GENERAL DESCRIPTION

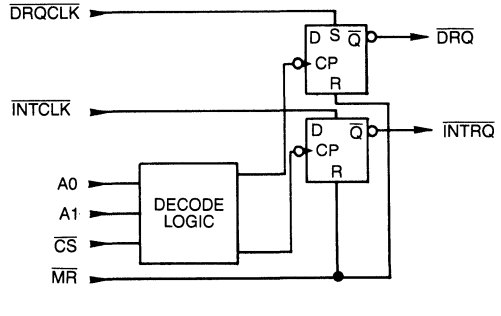
The HDC 1100-12 "improved" MFM Generator converts serial NRZ data into an MFM (Modified Frequency Modulated) data stream. The MFM signal may be used to record information on a Winchester Disk.

In addition, the HDC 1100-12 generates Write Precompensation signals required to compensate for bit shift effects on the recording medium.

The HDC 1100-12 has the ability to delete clock pulses in the outgoing data stream in order to record Address Marks.



MFM GENERATOR



INTERRUPT CONTROLLER

SECTION VII

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

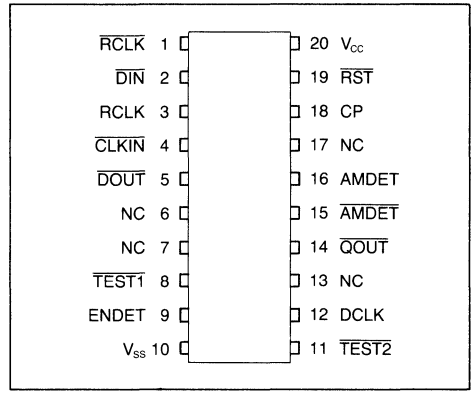
HDC 1100-03
PRELIMINARY

Hard Disk Address Mark Detector

FEATURES

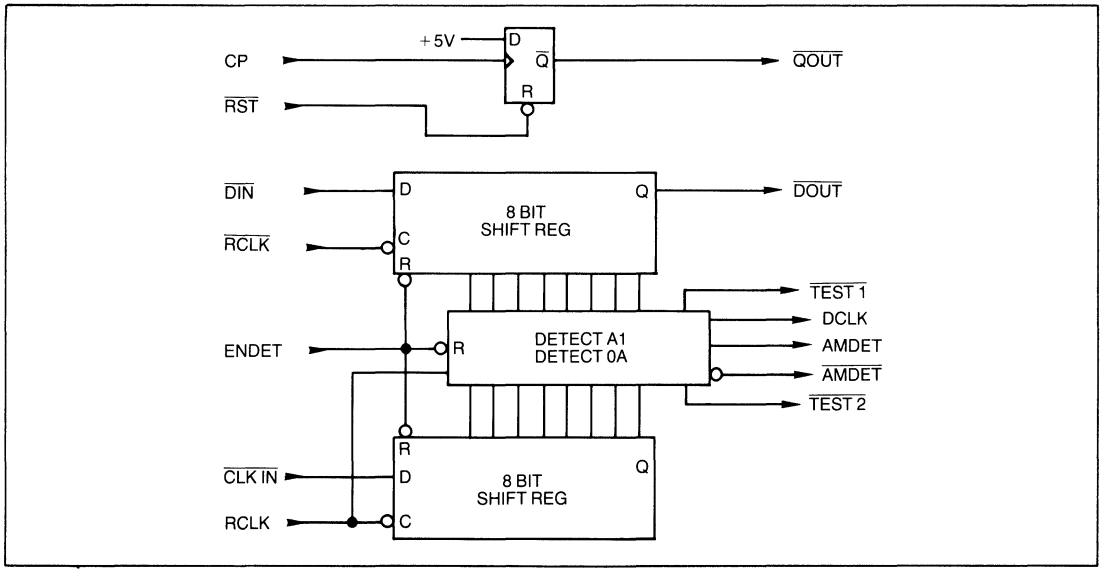
- ☐ Single +5 Volt Power Supply
- ☐ Decodes A1-0A
- ☐ Synchronous Clock/Data Outputs
- ☐ 5 MBit Data Rate
- ☐ Address Mark Detection
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-03 Address Mark Detector Provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM clocks and data are fed to the device along with a window clock generated by an external data separator. The HDC 1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces and AM DET signal when the pattern has been found. NRZ data is output from the device for driving a serial/parallel converter. An uncommitted latch is also provided for use by the data separator circuitry if required.



SECTION VII

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

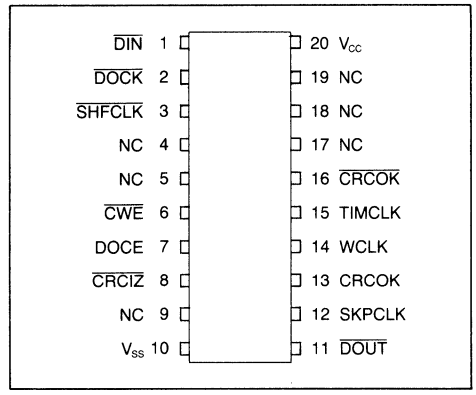
HDC 1100-04
PRELIMINARY

Hard Disk CRC Checker/Generator

FEATURES

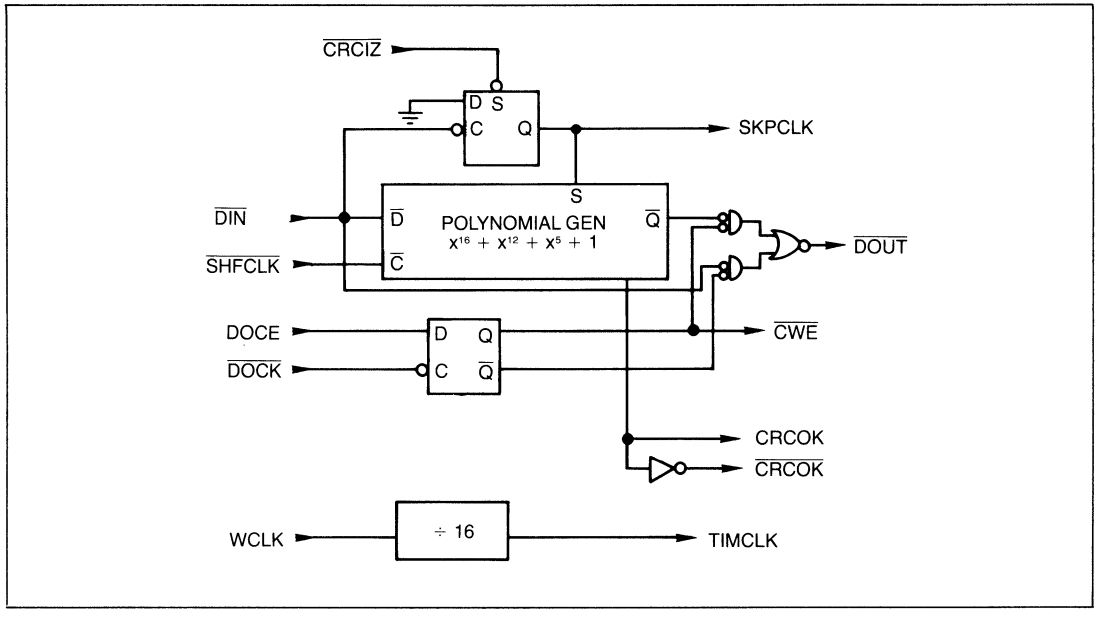
- ☐ Single +5 Volt Power Supply
- ☐ Generates/Checks CRC
- ☐ Latched Error Outputs
- ☐ CCITT-16 CRC
- ☐ Automatic Preset
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-04 CRC Checker/Generator generates a Cyclic Redundancy Checkword from a serial data stream, and checks for the proper CRC in a received serial data stream. In addition to the transmitted CRC output, complimentary latched "CRCOK" outputs are provided to indicate CRC errors in the check mode.



SECTION VII

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

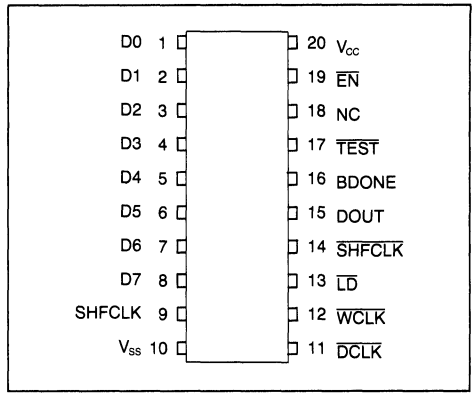
HDC 1100-05
PRELIMINARY

Hard Disk Parallel to Serial Converter

FEATURES

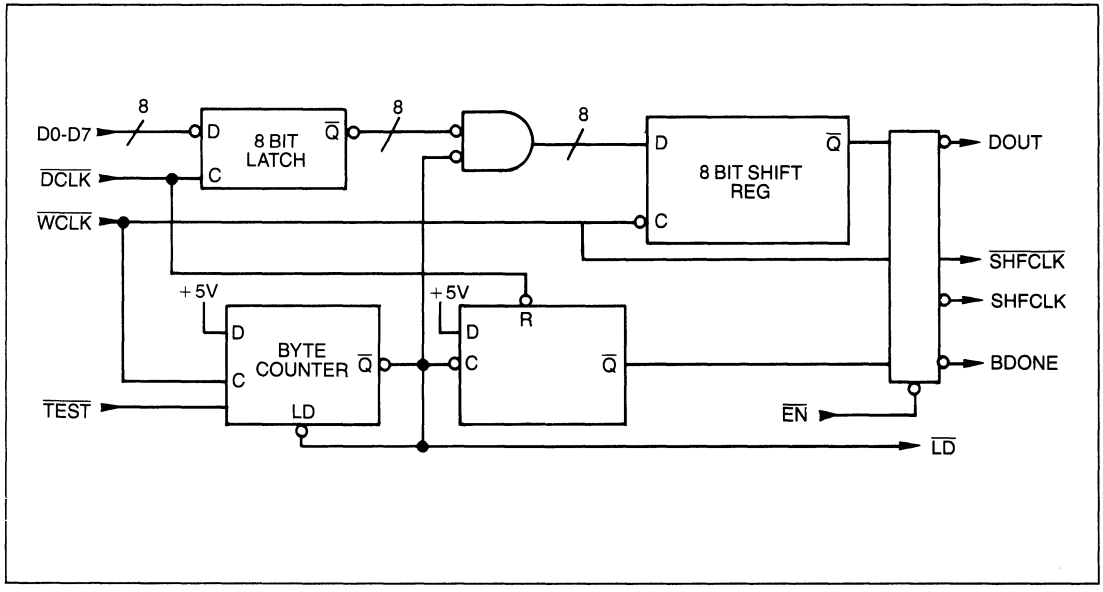
- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 Mbit Data Rate
- ☐ Parallel In/Serial Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-05 converts bytes of parallel data to a serial data stream for writing to disk memories or other serial devices. Parallel data is entered via the D0-D7 lines. A synchronous byte counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.



SECTION VII

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

HDC7260
PRELIMINARY

Universal Disk Controller

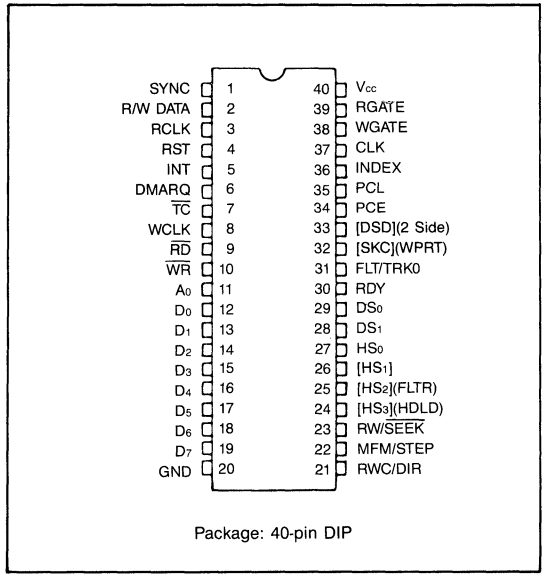
FEATURES

- ☐ Hard and floppy disk interface
- ☐ Controls four drives (any combination) simultaneously
- ☐ Programmable track format
- ☐ Transfer rate 6 MHz maximum
- ☐ High Level Commands, Including:

Check	Sense Intr. Status
Detect Error	Sense Status
Read Data	Specify1
Read Diagnostic	Specify2
Read ID	Verify Data
Recalibrate	Verify ID
Scan	Write Data
Seek	Write Format

- ☐ Parallel seek capability
- ☐ Multi-sector, -track, -cylinder read/write capability
- ☐ Implied seek function
- ☐ CRC error detection
- ☐ ECC error detection and correction
- ☐ DMA data transfer
- ☐ Single +5 volt supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

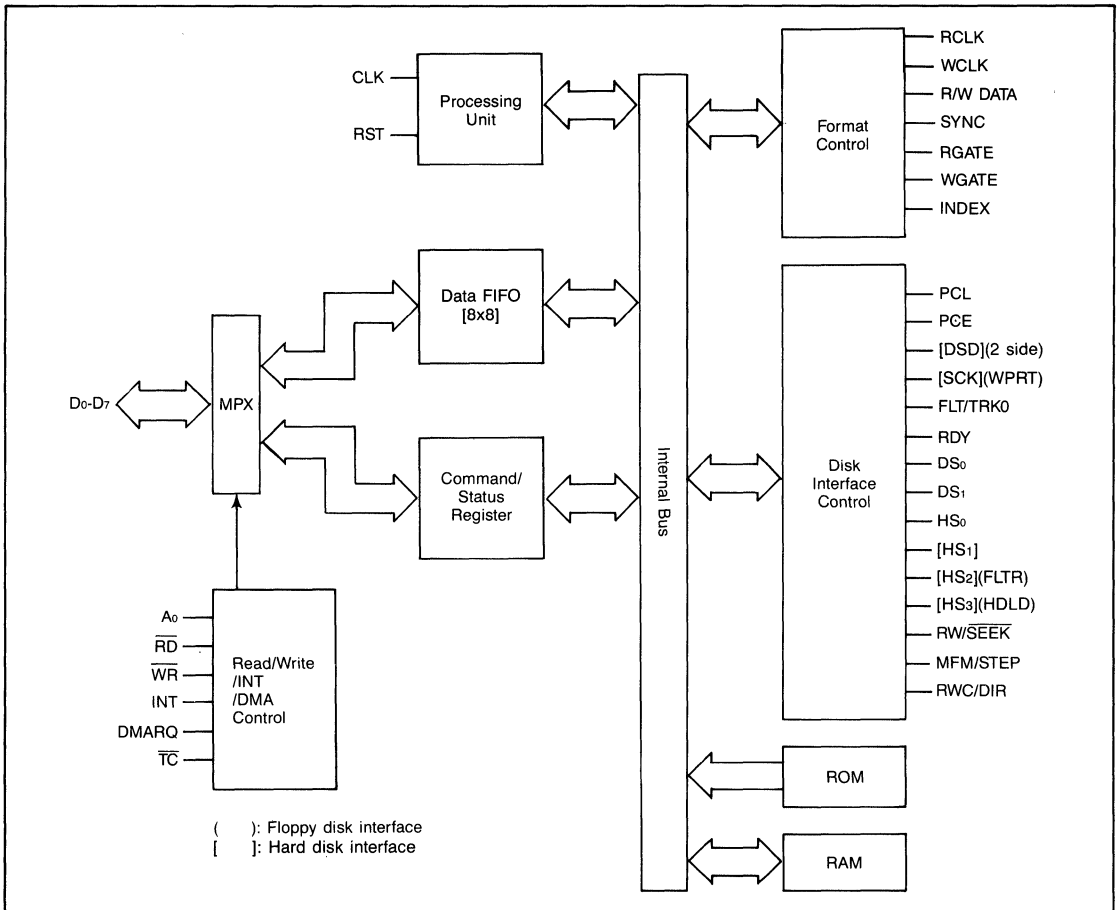
PIN CONFIGURATION



Package: 40-pin DIP

GENERAL DESCRIPTION

The HDC7260 is a single-chip disk controller that is capable of interfacing to a maximum of four floppy or hard disks in any combination. The chip utilizes the ST-506 defacto standard for the Winchester disks and is compatible with 8-inch, 5¼-inch and 3½-inch floppy disks. The HDC7260 is based on the HDC7261A architecture, but with changes to enhance performance and flexibility. The HDC7260 can generate both IBM- and ECMA-compatible floppy disks and hard disks with the standard format. ECC and CRC capabilities along with many high-level commands provide excellent system throughput, and the single-chip design provides for efficient board space utilization.



HDC7260 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	PLL SYNC	SYNC	PLL synchronization output
2	Read/Write Data	R/W DATA	Read data input or write data output
3	Read Clock	RCLK	Read clock input
4	Reset	RST	System reset input from host computer
5	Interrupt	INT	Interrupt request output
6	DMA Request	DMARQ	DMA request output
7	Terminal Count	$\overline{TC}$	Terminal count input from DMA
8	Write Clock	WCLK	Write clock input
9	Read	$\overline{RD}$	Host computer read control input
10	Write	$\overline{WR}$	Host computer write control input
11	Data/Status Reg Select	A_0	Status/command register or FIFO select pin
12-19	Data Bus	D_0-D_7	System data bus connections
20	Ground	GND	System ground
21	Read Write Current/Direction	RWC/DIR	If RW/$\overline{SEEK}$ = 1, outputs read/write current decrease signal. If RW/$\overline{SEEK}$ = 0, outputs the direction RW head is to move.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
22	MFM Step	MFM/STEP	If RW/$\overline{SEEK}$ = 1, outputs MFM signal to VCO circuit. If RW/$\overline{SEEK}$ = 0, outputs STEP signal to move RW head.
23	Read Write/$\overline{SEEK}$	RW/$\overline{SEEK}$	Output signal that specifies function of some multiplexed signals
24	Head Select 3 (Hold)	HS^3 (HDLD)	For hard disk, head select 3 output. For floppy disk, head load output.
25	Head Select 2 (Fault Reset)	HS_2 (FLTR)	For hard disk, head select 2 output. For floppy disk, output to clear drive fault state.
26	Head Select 1	HS_1	Head select output to disk drive.
27	Head Select 0	HS_0	Head select output to disk drive.
28-29	Drive Select	DS_1-DS_0	Drive select outputs.
30	Ready	RDY	Ready input from disk drive.
31	Fault/Track Zero	FLT/TRKØ	If RW/$\overline{SEEK}$ = 1, inputs a fault flag from the disk drive. If RW/$\overline{SEEK}$ = 0, inputs a signal indicating R/W head is over cylinder zero.
32	Seek Complete (Write Protect)	SKC (WPRT)	Seek complete input from hard disk drive, or write protected input from floppy disk drive.
33	Drive Select (double-sided)	DSD (2 Side)	Drive selected input from hard disk drive, or double-sided disk input from floppy disk drive.
34-35	Precompensation Entry, Late	PCE, PCL	Precompensation early/late output to disk drive.
36	Index	INDEX	Index hole detect input from disk drive
37	Clock	CLK	System clock input from host computer
38	Write Gate	WGATE	Write gate output to disk drive
39	Read Gate	RGATE	Read gate output to disk drive
40	Power Supply	V_{CC}	+5 V (typical)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge NY 11788
(516) 273 3100 TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

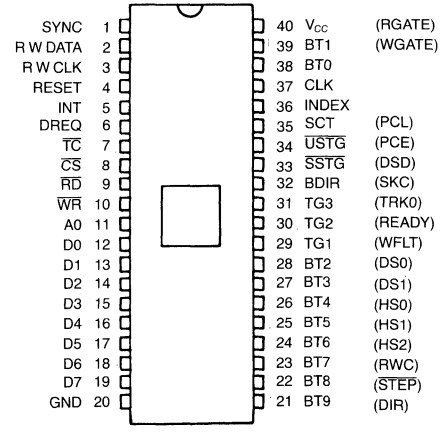
HDC 7261A
PRELIMINARY

Hard Disk Controller

FEATURES

- ☐ Flexible interface to various types of Hard Disk Drives
- ☐ Programmable Track Format
- ☐ Controls up to 8 Drives
- ☐ Parallel Seek Operation Capability
- ☐ Multi-sector and Multi-track Transfer Capability
- ☐ Data Scan and Data Verify Capability
- ☐ High Level Commands, Including:
  - READ DATA
  - READ ID
  - WRITE DATA
  - WRITE ID
  - SCAN DATA
  - VERIFY DATA
  - VERIFY ID
  - CHECK
  - SEEK (Normal or Buffered)
  - RECALIBRATE (Normal or Buffered)
  - READ DIAGNOSTIC (SMD Only)
  - SPECIFY
  - SENSE INTERRUPT STATUS
  - SENSE DRIVE STATUS
  - DETECT ERROR
- ☐ NRZ, FM, or MFM Data Format
- ☐ Maximum Data Transfer Rate: 12MHz
- ☐ Error Detection and Correction Capability
- ☐ Simple I/O Structure: Compatible with Most Microprocessors
- ☐ All Inputs and Outputs except Clock Pins are TTL-Compatible (Clock Pins Require Pull-up)
- ☐ Single +5V Power Supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

Note: Signals shown in parentheses are used when the HDC7261 is in the floppy-like mode.

SECTION VII

GENERAL DESCRIPTION

The HDC7261 Hard Disk Controller is an intelligent microprocessor peripheral designed to control a number of different types of disk drives. It is capable of supporting either hard-sector or soft-sector disks and provides all control signals that interface the controller with either SMD disk interfaces or Seagate floppy-like drives. Its sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the HDC7261 and all the data transfers associated with read, write, or format operations are done by the HDC7261 and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The HDC7261 provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

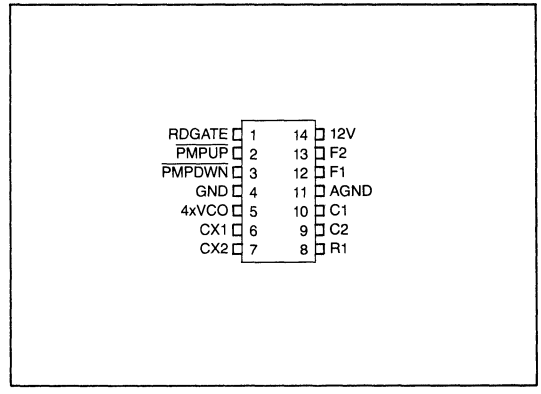
HDC 9223
PRELIMINARY

High Performance Analog Data Separator Support Circuit (ADSSC) For Hard Disk

FEATURES

- ☐ Significantly reduces component count in hard disk systems
- ☐ Completely compatible with the HDC 9226 Hard Disk Data Separator and the HDC 9224 Universal Disk Controller
- ☐ Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- ☐ Eliminates costly critical "tune up" adjustments
- ☐ Space saving 14 pin package
- ☐ Monolithic analog solution reduces critical pc board layout
- ☐ Single + 12V power supply
- ☐ Printed Circuit Board Artwork available to facilitate prototyping and evaluation

PIN CONFIGURATION



SECTION VII

GENERAL DESCRIPTION

The HDC 9223 Analog Data Separator Support Circuit (ADSSC) is a 14 pin device, which when used with the HDC 9224 Universal Disk Controller and the HDC 9226 Hard Disk Data Separator significantly simplifies the design of a high performance hard disk data separator.

The HDC 9223, combined with the HDC 9226 and a few resistors and capacitors, forms a phase locked loop which performs phase and frequency locking onto either the MFM or FM data stream output by ST506 or ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9223 and HDC 9226 simplify the task of the designer.

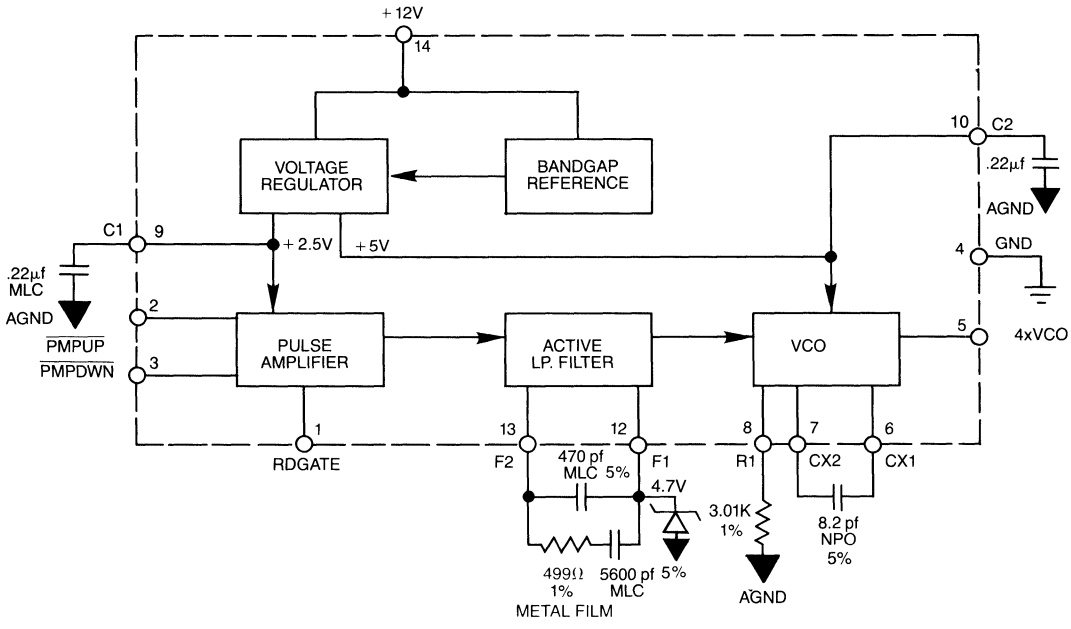


FIGURE 1: HDC 9223 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Read Gate	RDGATE	This active high input controls the gain of the loop. A high level decreases the gain and a low level increases the gain.
2	$\overline{\text{Pump Up}}$	$\overline{\text{PMPUP}}$	This active low input causes the VCO to increase its frequency.
3	$\overline{\text{Pump Down}}$	$\overline{\text{PMPDWN}}$	This active low input causes the VCO to decrease its frequency.
4	Digital Ground	GND	This is the ground connection for the digital circuitry within the HDC 9223.
5	Four Times VCO	4xVCO	This is the VCO output. It will vary from 18 to 22 MHz as a function of the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ input signals.
6	External Capacitor Connection 1	CX1	An 8.2 pf external NPO capacitor is connected across pins 6 and 7.
7	External Capacitor Connection 2	CX2	
8	External Resistor Connect	R1	A 3.01K 1% resistor is connected from this pin to Analog Ground.
9	External Filter Cap Connection 1	C1	A .22µf MLC capacitor is connected from this pin to Analog Ground.
10	External Filter Cap Connection 2	C2	A .22µf MLC capacitor is connected from this pin to Analog Ground.
11	Analog Ground	AGND	This is the ground connection for the analog circuitry within the HDC 9223.
12	External Filter Connection 1	F1	A filter network should be connected to this pin as shown in Figure 4.
13 •	External Filter Connection 2	F2	A filter network should be connected to this pin as shown in Figure 4.
14	+12 Volts	12V	Connect the power supply to this pin. A .22µf bypass capacitor should also be connected from this pin to Analog Ground.

DESCRIPTION OF OPERATION

The functional block diagram of the HDC 9223 is shown in Figure 1. The major functional blocks within the HDC 9223 are a voltage controlled oscillator (VCO), an active loop filter, and a pulse amplifier. The gain of the pulse amplifier is controlled by the RDGATE logic input.

The voltage controlled ocsillator generates the 4xVCO output (nominally 20 MHz). The frequency of this output is determined by the signals on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ inputs to the HDC 9223. Since the half bit time for data from the disk is 100ns, the HDC 9226 divides the frequency of the 4xVCO signal in half, and compares the phase and frequency of the resulting 10 MHz signal to that of the incoming data. The HDC 9226 then varies the pulse width on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ lines to adjust the output frequency of the VCO on the HDC 9223, closing the loop.

A voltage regulator and bandgap voltage reference ensure power supply rejection and stable VCO operation.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 to +150 C
Lead Temperature (soldering, 10 sec) ..... +300 C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} +0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibly exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS

(TA = 0C to 70C, V_{CC} = 12.0V ± 5%)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT				
I_{CC}		60	mA	
SUPPLY VOLTAGE				
V_{CC}	11.4	12.6	V	12V ± 5%
INPUT VOLTAGE				
V_{IL}		2.4	V	I_{OL} = 2.0mA
V_{IH}	3.6		V	I_{OH} = −400μA
OUTPUT VOLTAGE				
V_{OL}		1.2	V	I_{OL} = 2.0mA
V_{OH}	4.1		V	I_{OH} = −400μA
INPUT CURRENT				
I_{IL}		−10	μA	V_{IL} = 0.8V
I_{IH}		40	μA	V_{IH} = 3.0V

AC ELECTRICAL CHARACTERISTICS

(TA = 0C to 70C, V_{CC} = 12.0V ± 5%)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Parameter	Symbol	Min.	Max.	Units	Comments
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ pulse width	t_{PW}	15	125	ns	Measured at 50% amplitude (Fig. 2)
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ rise time	t_{IR}		10	ns	Measured between 0.6 and 1.8V (Fig. 2)
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ fall time	t_{IF}		10	ns	Measured between 0.6 and 1.8V (Fig. 2)
Output Frequency (when locked)		18	22	MHz	
4xVCO rise time	t_{OR}		15	ns	Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3)
4xVCO fall time	t_{OF}		15	ns	Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3)
4xVCO pulse width high	t_{OH}	16		ns	Fig. 3 Measured at 2.5V
4xVCO pulse width low	t_{OL}	16		ns	Fig. 3 Measured at 2.5V

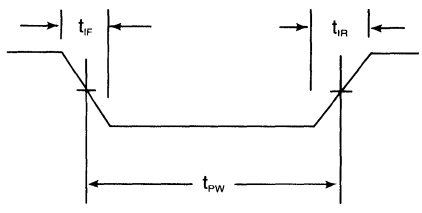


FIGURE 2:
$\overline{\text{PMPUP}}$/$\overline{\text{PMPDWN}}$ TIMING

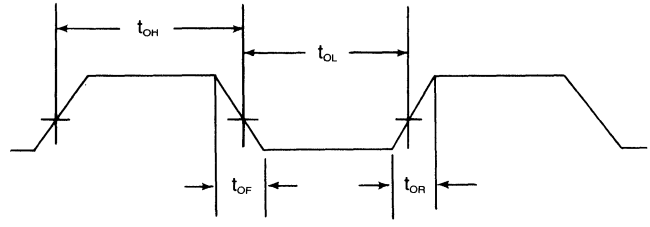


FIGURE 3: 4xVCO TIMING

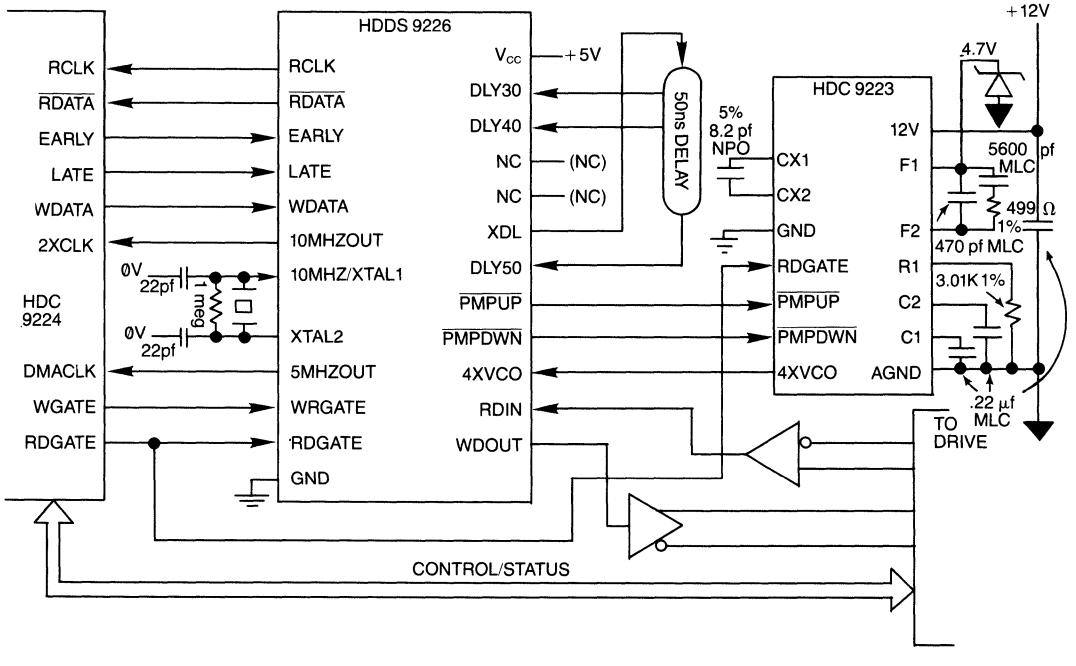


FIGURE 4: TYPICAL CIRCUIT CONFIGURATION

STANDARD MICROSYSTEMS CORPORATION

HDC 9224

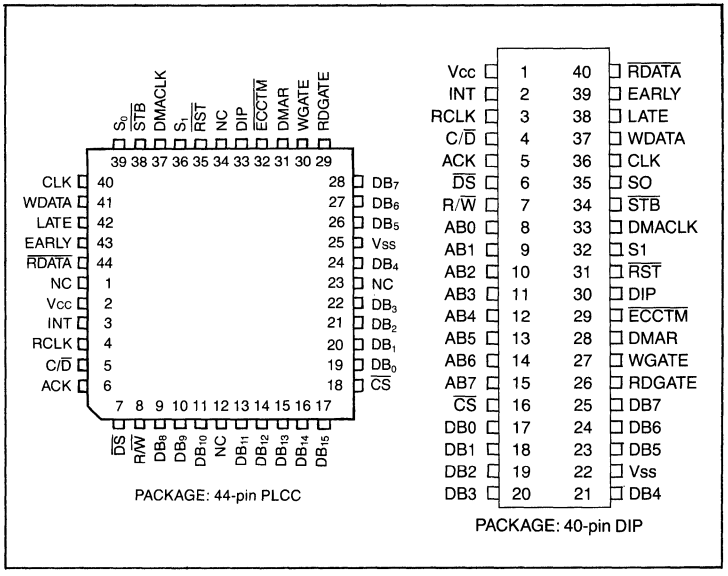
Universal Disk Controller

FEATURES

Programmable Disk Drive Interface and Formats

- ☐ Seagate (ST506) or user definable Hard Disk Formats
- ☐ IBM Compatible Single or Double Density Floppy Disk Formats
- ☐ Controls 8″, 5.25″, and 3.5″ drives
- ☐ Controls tape drives for tape backup of disks
- ☐ Full CRC generation and checking
- ☐ Internal or External Error detection
- ☐ Programmable user-transparent Error correction
- ☐ Programmable automatic retry option
- ☐ Programmable internal write precompensation logic
- ☐ Read/Write commands with automatic seek
- ☐ Multiple sector read/write transfers
- ☐ Sector interleave capability
- ☐ Internal address mark generation and detection
- ☐ Programmable track step rates
- ☐ Supports both buffered and unbuffered seeks
- ☐ Polling command allows overlapping seeks
- ☐ Powerful, high level command set
- ☐ Controls up to 4 drives with
  - ☐ up to 16 heads per drive
  - ☐ up to 2048 cylinders per drive
  - ☐ up to 256 sectors per track

PIN CONFIGURATION



Flexible System Interface

- ☐ Built-in DMA controller capable of addressing up to 16 MBytes
- ☐ Supports either private or virtual buffer memory addressing schemes
- ☐ User readable Interrupt, Chip Status, and Drive Status registers
- ☐ Programmable Interrupt Mask
- ☐ TTL compatible
- ☐ Standard 40 pin DIP package
- ☐ Single +5 volt supply

SECTION VII

GENERAL DESCRIPTION

The HDC 9224 Universal Disk Controller (UDC) is a 40 pin, n-channel MOS/LSI device capable of interfacing up to 4 Winchester-type hard disks and/or industry standard floppy disks to a processor. The chip is programmable to support both the Seagate (ST506) and user defined hard disk formats, as well as IBM compatible 8″, 5.25″ and 3.5″ single and double density formats.

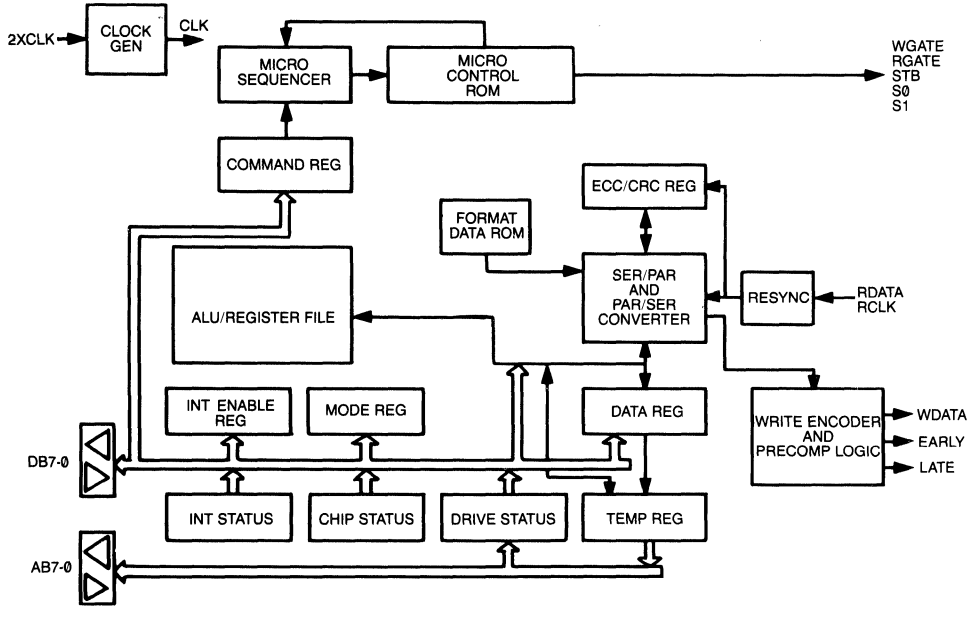
A powerful and sophisticated command set reduces the software overhead required to implement a combined hard disk/floppy disk controller. These commands include:

Drive Select	Seek to cylinder and read ID
Step out 1 cylinder	Step in 1 cylinder
Restore Drive	Read Logical Sectors
Read Physical Sectors	Read Entire Track
Write Logical Sectors	Write Physical Sectors
Chip Reset	Deselect Drive
Poll Drives for Ready	Set Register Pointer
Tape Back-up	Format current track

The HDC 9224 can use both private memory or shared memory buffers with the chip's internal DMA controller providing up to 24 bit addresses over an 8 bit data bus. This enables the HDC 9224 to address up to 16 megabytes of memory, and allows the hardware designer tremendous flexibility in system design.

Several techniques of error detection and correction are implemented on the HDC 9224. One user selected method allows the chip to detect and transparently correct a read error in the data-stream, without external logic. Another technique allows the designer complete control over the ECC algorithm, by using external logic or system software to detect and correct the error. As a further aid in error handling, the HDC 9224 allows the user to specify the number of read retries to be attempted before an error is reported to the host processor by the HDC 9224.

The HDC 9224 features a versatile track format command which allows formatting with interleaved sectors. The chip needs only 3 or 4 bytes of external memory space per sector (depending on format selected). This feature allows the designer to optimize sector interleaving for optimum throughput.



BLOCK DIAGRAM OF DATA PATH IN HDC 9224

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Power	V_{CC}	+5 volt power supply pin
22	Ground	V_{SS}	System ground
16	$\overline{\text{Chip Select}}$	$\overline{CS}$	This signal (when active) selects the HDC 9224 for communications with the host processor. This signal is normally derived by decoding the high order address bits. It is active low.
17,18 19,20 21,23 24,25	Data Bus 7-0	DB7-0	All system processor reads and writes, (including status reads, initialization, disk parameters, and commands) are 8 bit transfers which utilize these lines. When the UDC is accessing memory, data is input or output on these lines. Data on these lines is valid only when $\overline{\text{DATA STROBE}}$ ($\overline{DS}$) is active low.
8-15	Aux Bus 7-0	AB7-0	These 8 pins are used to output drive control signals and DMA Address information. Additionally, these pins are used to input drive status information.
4	Command/$\overline{\text{Data}}$	C/$\overline{D}$	During processor to UDC communications, this input is used to indicate whether a command or data transfer will follow. If this pin is low, data may be written to, or read from, the internal data registers. If this pin is high, the processor may write commands or read command results from the UDC.
7	Read/$\overline{\text{Write}}$	R/$\overline{W}$	When the processor is communicating to the UDC, a high on this input line indicates a (processor) request for a UDC read operation, and a low indicates a (processor) request for a write operation. R/$\overline{W}$ C/$\overline{D}$ Operation 0 0 Write to register file 0 1 Write to command reg. 1 0 Read from register file 1 1 Read Interrupt Status Register During UDC initiated operations, this pin becomes an output, and is used to indicate a read operation (logic 1) or write operation (logic 0) to external memories.

PIN NO.	NAME	SYMBOL	DESCRIPTION
6	$\overline{\text{Data Strobe}}$	$\overline{\text{DS}}$	This active low pin functions as both an input and output. When the processor is writing to the UDC, the trailing edge of an active (low) signal applied to this pin indicates that the data on DB7-0 is valid, and the data is latched into the appropriate UDC register on the rising edge. When the processor is reading from the UDC, the trailing edge of an active (low) signal applied to this pin is used to clock out the desired UDC register on to DB7-0. During UDC initiated DMA operations, the UDC drives this pin low to either read or write data from memory. On DMA read cycles, data is clocked in on the trailing edge. On DMA write operations, the data on DB7-0 is valid anytime this pin is active (low). When this pin is high (logic 1), DB7-0 return to a high impedance state.
2	Interrupt	INT	This active high output is used by the UDC whenever it wants to interrupt the processor. The interrupt pin is reset to its inactive (low) state when the UDC interrupt status register is read.
30	DMA In Progress	DIP	This active high output becomes active whenever the UDC is actually performing a DMA operation.
28	DMA Request	DMAR	This active high output becomes active whenever the UDC requires the system bus to perform a memory cycle, and ACK is inactive. During hard disk operations, it remains active until the sector transfer is complete. During floppy disk operations, it is active for 1 byte transfer time. The UDC shows that is has released the system bus by resetting this signal to its inactive (low) state.
5	Acknowledge	ACK	This active high signal from the processor tells the UDC that the processor has released the system bus and the UDC may access system memory.
37	Write Data	WDATA	This pin is used to output serial data from the UDC to the drive, in either FM or MFM format. In both cases, data is output with the most significant bit first.
38	Late	LATE	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written late.
39	Early	EARLY	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written early.
27	Write Gate	WGATE	This output (when active high) indicates the drive should allow a write operation.
40	$\overline{\text{Read Data}}$	$\overline{\text{RDATA}}$	This input pin contains the serial bit stream read from the drive, in either FM or MFM format. Media flux reversals are indicated by a negative transition.
3	Read Clock	RCLK	This input is generated by the external data separator. Its frequency should self-adjust to the variations in bit width in the data stream from the drive. This clock supplies a window to indicate half-bit-cell boundaries.
26	Read Gate	RDGATE	This output pin is used to enable the external data separator, compensate for write to read recovery time of the drive, and filter out the write splice in gaps 2 and 3. The timing of this signal is dependent upon the type of drive (hard or floppy) being used. RDGATE is inactive at all times except when the UDC is actually performing a read operation or an internal ECC operation.
29	$\overline{\text{ECC Time}}$	$\overline{\text{ECCTM}}$	When the UDC is used in external ECC mode, this output pin becomes active (low) during the time the UDC is reading the ECC bytes from memory or external ECC chip, when executing a WRITE command. It is also active during internal ECC correction operations, and for either one (write) or two (read) byte times after DIP (pin 30) becomes inactive following a sector transfer. This shows the system processor when it should service the UDC buffer.
32,35	Select 1,0	S1,S0	These active high outputs are used by external logic to select either the source or destination for data transfers occuring via AB7-0. The following table defines the specific transfer being called for by the UDC. (Note that S1-0 are valid only when $\overline{\text{STB}}$ is active low.)

$\overline{\text{STB}}$	S1	S0	AB7-0 Activity
1	X	X	S1,S0 Invalid
0	0	0	UDC inputs Drive Status Signals
0	0	1	UDC outputs DMA address bytes
0	1	0	UDC outputs OUTPUT 1 signals
0	1	1	UDC outputs OUTPUT 2 signals

PIN NO.	NAME	SYMBOL	DESCRIPTION
34	$\overline{\text{Strobe}}$	$\overline{\text{STB}}$	This active low output indicates when the host processor should read or write to AB7-0, as indicated by S1-0. When AB7-0 are used as outputs from the UDC, data is valid anytime this signal is active (low). When AB7-0 are used as inputs to the UDC, data is clocked in on the rising edge of this signal.
36	DEVICE CLOCK	CLK	This input is the double frequency clock used by the UDC for all internal timing operations. Eight inch hard disk drives (with a nominal bit time of 230 ns) require an input of 8.696 MHz (115 ns period). 5.25″ hard disks (with a nominal bit time of 200 ns) require a 10 MHz input (100 ns period). Eight inch, 5.25″ and 3.5″ floppy drives all require a 10 MHz clock, which is internally prescaled by the UDC to the correct frequency, as determined from the Drive Select command and MODE register. This input requires an external pull-up resistor, as it is not TTL-level compatible. See figure 2.
31	$\overline{\text{Reset}}$	$\overline{\text{RST}}$	This active low input will force the UDC into the following known state: INT–Inactive low $\overline{\text{WDATA}}$–Inactive low $\overline{\text{ECCTM}}$–Inactive high DMAR–Inactive low EARLY–Inactive low C/$\overline{\text{D}}$–Input AB7-0–Input $\overline{\text{LATE}}$–Inactive low R/$\overline{\text{W}}$–Input DB7-0–Input WGATE–Inactive low DIP–Inactive low $\overline{\text{RDGATE}}$–Inactive low $\overline{\text{DS}}$–Input An active low on this pin has the same effect as a RESET Command.
33	DMA Clock	DMACLK	All UDC DMA operations will be synchronized to this clock input. Three DMACLK periods are required for each DMA byte transfer.

OVERVIEW OF UDC REGISTERS

The HDC 9224 has three types of internal, processor addressable registers; Read/Write, Read Only, and Write Only. These registers are addressed by an internal register pointer that is set by the SET REGISTER POINTER command.

All register data is passed to and from the UDC via the data bus (DB7-0).

The internal register pointer is automatically incremented with each register access until it points to the DATA Register. This insures that all subsequent register accesses will address the DATA register.

PROCESSOR ACESSIBLE REGISTERS

REGISTER ADDR	WRITE	READ
0	DMA7-0	DMA7-0
1	DMA15-8	DMA15-8
2	DMA23-16	DMA23-16
3	Desired Sector	Desired Sector
4	Desired Head	Current Head
5	Desired Cylinder	Current Cylinder
6	Sector Count	Temporary Storage
7	Retry Count	Temporary Storage
8	Mode	Chip Status
9	Interrupt/Command Terminator	Drive Status
A	Data/Delay	Data
COMMAND	Current Command	Interrupt Status

Three internal registers (OUTPUT 1, OUTPUT 2, and INPUT DRIVE STATUS) which are not directly addressable by the processor are accessed by the UDC. The information contained in these registers is used in disk interfacing and is input or output on UDC Pins AB7-0. The following table describes these registers and the signals they output or input on AB7-0.

UDC ADDRESSABLE REGISTERS

DRIVE STATUS REGISTER (input)	**Select Pins S1 = 0, S0 = 0**
AB7—ECC Error	AB6—Index Pulse
AB5—Seek Complete	AB4—Track 00
AB3—User Defined	AB2—Write Protect
AB1—Drive Ready	AB0—Write Fault

OUTPUT 1 (Output)	**Select Pins S1 = 1, S0 = 0**
AB7—Drive Select 3	AB6—Drive Select 2
AB5—Drive Select 1	AB4—Drive Select 0
AB3—Programmable Outputs (see text)	AB2—Programmable Outputs
AB1—Programmable Outputs	AB0—Programmable Outputs

OUTPUT 2 (Output)	**Select Pins S1 = 1, S0 = 1**
AB7—Drive Select 3	AB6—Reduce Write Current
AB5—Step Direction	AB4—Step Pulse
AB3—Desired Head (Bit 3)	AB2—Desired Head (Bit 2)
AB1—Desired Head (Bit 1)	AB0—Desired Head (Bit 0)

Additionally, several registers (DMA7-0, DMA15-8, DMA23-16, DESIRED SECTOR, DESIRED CYLINDER, SECTOR COUNT, and RETRY COUNT) serve an alternate purpose. These registers are used by the FORMAT TRACK command to hold parameters. This alternate register utilization is described in detail under the FORMAT TRACK command.

DESCRIPTION OF UDC REGISTERS

DMA 7-0 (R/W Register; Address 0)
This 8-bit read/write register is loaded with the low order byte (MSB in bit 7) of the DMA buffer memory starting address.

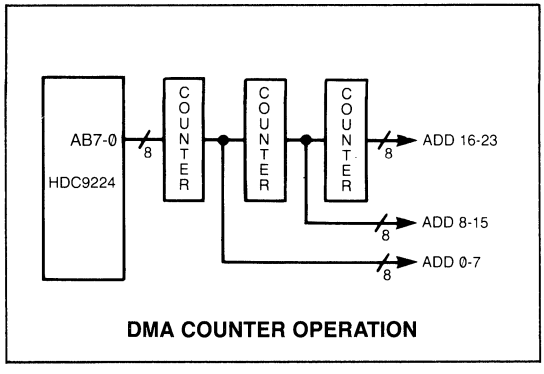
DMA 15-8 (R/W Register; Address 1)
This 8-bit read/write register is loaded with the middle order byte (MSB in bit 7) of the DMA buffer memory starting address.

DMA 23-16 (R/W Register; Address 2)
This 8 bit read/write register is loaded with the high order byte (MSB in bit 7) of the DMA buffer memory starting address.

Prior to the data transfer portion of a read or write command, the UDC writes the contents of the DMA registers to an external counter. This transfer (from the registers to the external counter) is accomplished by the UDC with 3 separate outputs on AB7-0, with the contents of DMA 24-16 being transfered first. (In memory areas that require less than 24 bit addressing, the higher order bits are overwritten. The external counter must be incremented with the UDC's $\overline{DS}$ signal after each byte transfer.

If, during read operations, an error is detected during the data transfer, a retry will occur (if so programmed), and the three DMA registers will re-initialize the external counter to the original starting address.

During multiple sector read/write operations, the DMA address contained in the DMA registers will be incremented by the size of the sector selected at each sector boundary. This ensures that during read operations the address contained in the DMA registers always corresponds to the proper memory starting address of the sector currently being read.



DMA COUNTER OPERATION

DESIRED SECTOR REGISTER (R/W Register; Address 3)
This 8-bit read/write register is loaded with the starting sector number of a multiple sector read/write operation. Except for the last sector of the operation, this register is incremented after each sector is written or read without error.

If the UDC terminates a command because of an error, this register will normally contain the bad sector number, and may be read by the processor.

DESIRED HEAD REGISTER (Write Register; Address 4)
This 8-bit write only register is loaded with the 4-bit head number, and the upper 3 bits of the desired cylinder number.

BIT 7 ALWAYS 0
BITS 6-4 MSBs of the Desired Cylinder number
BITS 3-0 Desired Head Number.

The desired head number is output on AB3-0 during OUTPUT 2 times.

DESIRED CYLINDER REGISTER (Write Register; Address 5)
This 8-bit write only register is loaded with the 8 low order bits of the desired cylinder (MSB in Bit 7). Combined with the 3 high order bits loaded into the DESIRED HEAD REGISTER, these 11 bits form the desired cylinder number, which is checked by read and write operations during the Check ID portion of the command.

SECTOR COUNT REGISTER (Write Register; Address 6)
This 8-bit write only register is loaded with the number of sectors to be operated on by the read or write command. This allows multiple sectors on the same cylinder to be either written or read.

RETRY COUNT REGISTER (Write Register; Address 7)
This 8-bit write only register is loaded with the number of times the UDC should retry to read a data field before reporting an error. Additionally, this register is loaded with the user programmable output signals that the UDC outputs on AB0-3 during OUTPUT 1 times.

The retry count is loaded (in 1's complement format) into the 4 most significant bits of this register.

The user programmable output signals are loaded into the 4 least significant bits of the register.

BITS 7-4 Desired Retry Count (in 1's complement format)
BITS 3-0 User Programmable Output Signals

MODE REGISTER (Write Register; Address 8)
This 8-bit write only register defines the operating mode of the UDC as follows:

BIT 7 (DRIVE DATA TYPE)
This bit determines how the UDC decodes data from the drive.

BIT 7 = (1): UDC configured for hard disk use. (Level transitions)
BIT 7 = (0): UDC configured for floppy use. (Pulse inputs)

BITS 6,5 (CRC/ECC Enable Code)
These bits determine the error detection/correction code generated and checked by the UDC.

DB6	DB5	CODE GENERATED/CHECKED
0	0	CRC
0	1	External ECC
1	0	Internal 32 bit ECC without correction
1	1	Internal 32 bit ECC with correction

With internal ECC selected the UDC will transfer 4 extra bytes during reads and writes. Normal CRC checking is still done on all ID fields.

With external ECC selected the UDC will flag an ECC error via BIT 7 of the DRIVE STATUS REGISTER. Normal CRC checking is still done on all ID fields.

If neither internal or external ECC is selected, then the UDC will perform CRC checks on both data and ID fields.

STEP RATES FOR DOUBLE DENSITY (MFM) OPERATION **(Mode Bit 4 = 0)**

DRIVE TYPE			5.25" HARD DISK	8" FLOPPY	5.25" FLOPPY
DB2	DB1	DB0	STEP RATE	STEP RATE	STEP RATE
1	1	1	12.8 ms	128 ms	256 ms
1	1	0	6.4 ms	64 ms	128 ms
1	0	1	3.2 ms	32 ms	64 ms
1	0	0	1.6 ms	16 ms	32 ms
0	1	1	0.8 ms	8 ms	16 ms
0	1	0	0.4 ms	4 ms	8 ms
0	0	1	0.2 ms	2 ms	4 ms
0	0	0	17.6 us *	176 us *	352 us *
0	0	0	21.8 us **	218 us **	436 us **
Pulse Width:			11.2 us	112 us	224 us

*This rate applies for SEEK commands only
**This rate applies for RESTORE commands only

(DOUBLE ALL OF THE ABOVE TIMES FOR SINGLE DENSITY (FM) OPERATIONS.)

BIT 4 (Single or Double Density)
This bit determines whether the UDC will perform its operations in either single or double density.

BIT 4 = (1) Single Density (FM) Format
BIT 4 = (0) Double Density (MFM) Format

BIT 3 (ALWAYS 0)

BITS 2,1,0 (Step Rate Select)
These bits are programmed to select the desired drive step rate. Note that all step rates are determined by the type of drive and density selected, and are scaled from the CLK input.

The UDC can output extremely rapid step rate pulses if these bits are set to 000. This is useful when the UDC is controlling drives which support buffered seeks. For other speeds, please refer to the table above.

INTERRUPT/COMAND TERMINATION REGISTER (Write Register; Address 9)

This 8-bit write only register allows the programmer to mask out a number of conditions that would cause termination of a command. (Such termination occurs when the DONE bit in the INTERRUPT STATUS register is set.) One bit in this register also controls the generation of interrupts when either the DONE bit or the READY CHANGE bit in the INTERRUPT STATUS register go active.

BIT 7 (CRC PRESET)
Setting this bit to "1" will cause the CRC register to preset to 1 for CRC generation and checking. Setting this bit to "0" will cause the CRC register to preset to 0 for CRC generation and checking.

ID field CRC and data field CRC or ECC are generated and tested from the first A1 HEX byte in the ID field.

BIT 6 (ALWAYS "0")
This bit should always be set to "0" by the user. Failure to do this may result in unreliable operation.

BIT 5 (INT ON DONE)
If this bit is set (to "1"), an interrupt will occur when the DONE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

BIT 4 (DELETED DATA MARK)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the DELETED DATA MARK bit in the CHIP STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 3 (USER DEFINED)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the USER DEFINED status bit in the DRIVE STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 2 (WRITE PROTECT)
If this bit is set to (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE PROTECT bit in the DRIVE STATUS register goes active.

BIT 1 (READY CHANGE)
If this bit is set (to "1"), an interrupt will occur when the READY CHANGE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

The user should note that as a drive is selected or deselected, it is possible for the ready line from the drive to change state, and care should be taken in the design of the interrupt handler.

BIT 0 (WRITE FAULT)
If this bit is set (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE FAULT status bit in the DRIVE STATUS register is set. The command in progress will terminate when the current sector operation is completed.

DATA/DELAY REGISTER (R/W Register; Address 0AH)

This 8-bit read /write register serves a dual purpose. During UDC writes, data is placed in this register for recording to the disk. During UDC reads, recovered data is fetched from this register for storage into memory. All transfers occur via DB7-0, under DMA control.

Additionally, this register is loaded with the HEAD LOAD TIMER COUNT when the Drive Select command is issued. (Note that the actual amount of head load time is this value, times a value predetermined by the UDC, based on the type of drive selected. For more information, please see the Drive Select command description.)

COMMAND REGISTER (Write Register)

This 8-bit write only register is used to pass commands to the UDC. Valid commands are given to the UDC by setting C/$\overline{D}$ high and R/$\overline{W}$ active high, while strobing $\overline{DS}$ active (low).

CURRENT HEAD REGISTER Read Register; Address 4)

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register contains the actual head number, bad sector flag, and the 3 most significant bits of the cylinder number, as specified during formatting.

BIT 7 = (1) Last sector read had BAD SECTOR bit set
BIT 7 = (0) Last sector read had BAD SECTOR bit reset.

BITS 6-4 Three most significant bits of the current cylinder. (Most significant bit in Bit 6.)

BITS 3-0 Current Head Number (MSB in bit 3).

CURRENT CYLINDER REGISTER (Read Register; Address 5)

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register will contain the 8 least significant bits of the cylinder ID number, as specified during formatting. (The 3 most significant bits of the 11 bit cylinder ID number are contained as part of the CURRENT HEAD REGISTER.)

INTERRUPT STATUS REGISTER (Read Register)

This 8-bit read only register contains status information associated with interrupt conditions and errors that occur during disk operation. This register is read by setting C/$\overline{D}$ high, and R/$\overline{W}$ high.

When the Interrupt Status register is read, the INT output signal from the UDC will be reset (to an inactive low level).

BIT 7 (INTERRUPT PENDING)
A "1" indicates that either DONE bit or READY CHANGE bit has gone active. The user may disable these interrupts by setting the appropriate bits in the INTERRUPT/COMMAND TERMINATION, REGISTER. This bit is reset (to "0") by reading the Interrupt Status register.

BIT 6 (DMA REQUEST)
A "1" indicates that the UDC requires a data transfer either to or from its data register. This bit is reset (to "0") by the data transfer.

BIT 5 (DONE)
A "1" indicates that the current command is completed. This bit is reset (to "0") when a new command is issued.

BIT 4,3 (COMMAND TERMINATION CODE)
(Valid only when DONE is set)
These two bits indicate the command termination conditions:

BIT 4	BIT 3	CONDITIONS
0	0	Successful command termination
0	1	Execution error in READ ID Sequence
1	0	Execution error in SEEK Sequence
1	1	Execution error in DATA field

More detailed command termination error information is obtained by reading the Chip Status register.

BIT 2 (READY CHANGE)
A "1" indicates that the "ready" signal from the drive has experienced a low-to-high or high-to-low transition. (This shows that the drive has either become ready or become not ready.) This bit is reset (to "0") by reading the Interrupt Status register.

BIT 1 (OVERRUN/UNDERRUN)
A "1" indicates that a overrun or underrun condition has occured during a read or write command. These conditions occur when the UDC does not receive an acknowledge (to a DMA request) by the time a byte is ready for transfer to or from the processor.

This bit can only be reset (to "0") with a RESET command or a high on the RESET pin.

BIT 0 (BAD SECTOR)
A "1" indicates that a bad sector (as indicated from the MSB of the head ID byte in the ID field) has been encountered. This bit is reset when a new command is issued, or a good sector is read.

CHIP STATUS REGISTER (Read Register; Address 8)

This 8-bit read only register supplies additional chip status information. The information in this register is only valid between the time that the DONE bit is set in the INTERRUPT STATUS register and the time when the next command is issued to the UDC.

BIT 7 (RETRY REQUIRED)
If a retry was attempted by the UDC during the execution of any read or write command, this bit is set (to "1").

BIT 6 (ECC CORRECTION ATTEMPTED)
If the internal ECC circuitry has attempted to correct a bad sector, this bit is set (to "1").

BIT 5 (CRC/ECC ERROR)
If the UDC detects a CRC error or an ECC error, this bit is set (to "1").

BIT 4 (DELETED DATA MARK)
If the UDC reads a deleted data mark in the ID field, this bit is set (to "1"), otherwise it is reset (to "0").

BIT 3 (SYNC ERROR)
If the UDC does not find a sync mark when it is attempting to read either an ID or data field, then this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 2 (COMPARE ERROR)
If the information contained in the DESIRED HEAD and DESIRED CYLINDER registers does not match that contained in an ID field on the disk, this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 1,0 (PRESENT DRIVE SELECTED)
These two binary encoded bits represent the drive currently selected and correspond to the Drive Select bits set in the Output 1 and Output 2 latches.

BIT 1	BIT 0	DRIVE SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

DRIVE STATUS REGISTER (Read Register; Address 9)

This 8-bit read only register contains status information generated by the drives, external ECC Chip (if any), and a user definable input to the UDC from the drive.

To save pins on the UDC, the 8 status lines are input on AB7-0 and are latched in this internal register. The UDC will update this register whenever it is not using AB7-0 to output DMA counter values, OUTPUT 1, or OUTPUT 2 data. When configured as described below, the UDC will input drive status signals and interpret them as follows. In all cases, a logic "1" is considered the active input.

BIT 7 (ECC ERROR)
This bit is set (to "1") when the ECC ERROR signal is generated by an external ECC chip. This signal is input to the UDC on AB7.

BIT 6 (INDEX)
This bit is set (to "1") when the INDEX signal from the selected drive is active. Typically, index pulses from the drives are active for 10us-100us for each disk revolution. This signal is input to the UDC on AB6.

BIT 5 (SEEK COMPLETE)
This bit is set (to "1") when the SEEK COMPLETE signal from the selected drive is active. This bit will go active when the heads of the selected drive have settled over the desired track (at the completion of a seek).

When a drive supplies this signal, reading and writing should not be attempted until SEEK COMPLETE is set (to "1"). This signal is input on AB5.

For floppy disk operation, where the drives normally do not provide this signal, a retriggerable one shot could be used to generate a SEEK COMPLETE signal (if desired).

BIT 4 (TRACK 00)
This bit is set (to "1") when the TRACK 00 signal from the selected drive is active. This indicates that the heads on the selected drive are positioned over track 0. This signal is input on AB4.

BIT 3 (USER DEFINED)
This bit is set (to "1") when the USER DEFINED signal is active. This signal is input on AB3.

BIT 2 (WRITE PROTECT)
This bit is set (to "1") when the WRITE PROTECT signal from the selected drive is active. When set, this bit indicates that the disk in the selected drive is write protected. This signal is input on AB2.

BIT 1 (READY)
This bit is set (to "1") when the READY signal from the selected drive is active. When set, this bit indicates that the drive is ready to execute commands. This signal is input on AB1.

BIT 0 (WRITE FAULT)
This bit is set (to "1") when the WRITE FAULT signal from the selected drive is active. This signal, when active, indicates that a condition exists at the drive that would cause improper writing on the disk. This signal is input to the UDC on AB0.

TEMPORARY STORAGE REGISTERS

The UDC contains two temporary storage registers, used by the UDC for internal operations. The host processor should not attempt to read or modify these registers, as unpredictable results may occur.

UDC COMMAND OVERVIEW

The HDC 9224 has 16 high-level commands that provide the user with a high degree of flexibility and control. All of the commands for the UDC can be thought of as falling into one of two basic groups.

The first group handles the "housekeeping" required by the drives and the UDC itself. These commands are:

RESET	STEP OUT 1 CYLINDER
STEP IN 1 CYLINDER	SET REGISTER POINTER
DRIVE SELECT	RESTORE DRIVE
DESELECT DRIVES	POLL DRIVES

The second group comprises the "READ/WRITE" functions required in a magnetic disk subsystem. These commands are:

SEEK/READ ID	TAPE BACKUP (READ/
FORMAT TRACK	WRITE)
READ TRACK	READ SECTORS LOGICAL
READ SECTORS PHYSICAL	
WRITE SECTORS LOGICAL	

An internal status byte, which contains the BAD SECTOR, DELETED DATA and OVER/UNDER RUN bits, along with the current state of the READY, WRITE PROTECT, WRITE FAULT, and USER DEFINED lines, is checked at various times during command execution.

This internal status byte is examined before the execution of all READ/WRITE commands, and is also checked just prior to the completion of all commands (except for RESET, where its values would be meaningless.)

This byte is also checked by the UDC between sector operations during the execution of READ LOGICAL, READ PHYSICAL, WRITE LOGICAL and WRITE PHYSICAL commands.

The UDC makes decisions regarding command termination and interrupt generation based on the contents of this status byte, and the state of the bits in the INTERRUPT/COMMAND TERMINATION register. (Note that "write protect" and "write fault" status may cause command termination only during write and format operations.)

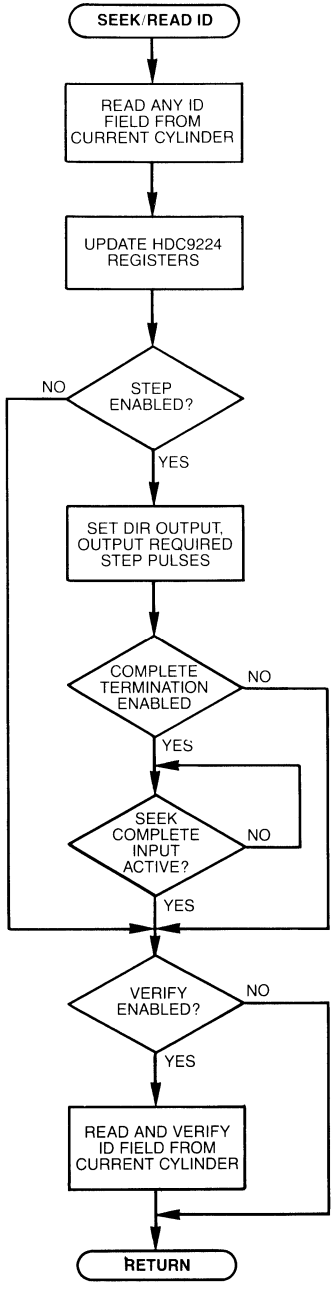
All commands (except RESET) terminate with the DONE bit in the INTERRUPT STATUS register being set. This bit may also be considered to be an inverted "busy" line, as the UDC resets it upon receipt of a valid command.

During all READ/WRITE group commands (except FORMAT TRACK and BACKUP), the UDC utilizes some common command execution sequences. Prior to entering each sequence the UDC sets the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to a known state. If a command fails to execute properly, these bits may then be used to determine where the command aborted.

The sequences common to the READ/WRITE group commands are as follows:

1. READ ID FIELD (Command Termination Code = 0-1)
   First, the UDC attempts to find an ID Field Sync mark. If no sync mark is found within 33,792 byte times (byte time = time to read one byte from the type of drive selected), the SYNC ERROR bit (in the CHIP STATUS register) is set (to "1"), and the command is terminated.

   During this phase, the UDC will raise and drop RDGATE up to 256 times (as it attempts to read each sector on the cylinder).



SEEK/READ ID OPERATION

After the ID Field is found, the UDC reads it and updates it CURRENT HEAD and CURRENT CYLINDER registers. This information was written to the disk during formatting.

Next, the UDC checks the CRC of the ID field which was read. If it is incorrect, the UDC sets (to "1") the CRC ERROR status bit (in the CHIP STATUS register) and terminates the command.

If the CRC is correct, the UDC then calculates the direction and number of step pulses required to move the head from the current cylinder to the cylinder specified in the DESIRED HEAD REGISTER. These pulses, and the direction bit are output during the OUTPUT 2 times.

If a command should terminate while in the sequence, the COMMAND TERMINATION bits will be set to 0-1.

2. VERIFY (Command Termination Code = 1-0)

After the UDC has read the ID Field, it attempts to verify that it has found the correct cylinder. To do this, the UDC tries to find an ID Field sync mark on the selected disk. If the UDC is unable to find an ID Field sync mark within 33,792 byte times, the SYNC ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

The UDC, after finding the ID Field sync mark, then reads the ID field and compares the information on the disk to the information contained in the DESIRED CYLINDER, DESIRED HEAD and DESIRED SECTOR registers.

The UDC will hunt for sync marks and read ID fields until the desired sector is found. If the desired sector is not located within 33,792 byte times, then the COMPARE ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

After the correct sector is found, the UDC checks the CRC for the sector ID Field. If this is found to be incorrect, the UDC sets to "1" the CRC/ECC ERROR bit in the CHIP STATUS register, and the command is terminated.

(When the UDC is executing a READ PHYSICAL or WRITE PHYSICAL command, ID Fields are checked only until the first sector to be transfered is found. No ID Field checking is performed on subsequent sectors, although CRC checking is done.)

If a command should terminate while in this sequence, the COMMAND TERMINATION bits will be set to 1-0.

3. DATA TRANSFER (Command Termination Code = 1-1)

If a READ PHYSICAL or READ LOGICAL command is being executed, the UDC will try to find a data sync mark (FBhex or F8hex) on the disk. If the sync mark found is F8h, then the UDC will set the DELETED DATA MARK bit in the CHIP STATUS register.

After a data sync mark is found, the UDC then updates its CURRENT HEAD and CURRENT CYLINDER registers from the information found on the disk and initiates a DMA request. If the host processor does not respond to the request within 1 byte time, then the UDC will set to "1" the OVER/UNDERRUN status bit in the INTERRUPT STATUS register, and the command will terminate.

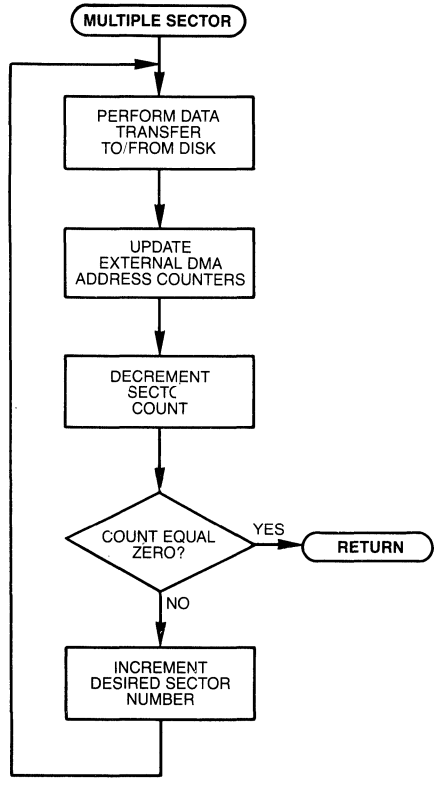
Using DMA, the UDC transfers a sector's worth of data, and then reads the ECC and/or CRC bytes. If a CRC error or uncorrectable ECC error is detected, the UDC will decrement the RETRY REGISTER, set the RETRY REQUIRED status bit (in the CHIP STATUS

register), and return to the VERIFY sequence.

If the UDC cannot read the sector, and the count in the ENTRY COUNT register has expired, then the CRC/ECC Error bit (in the CHIP STATUS register) is set, and the command terminates.

During a multi-sector transfer, the UDC updates the DMA registers after all sector operations, including the last one, and the SECTOR COUNT register is decremented. If the SECTOR COUNT register equals 0, then the command is terminated. If the SECTOR COUNT register is not equal to 0, then the UDC will increment the DESIRED SECTOR register, re-initialize the RETRY COUNT register (to its original value) and return to the VERIFY sequence.

If a command should terminate while in this sequence, the command termination bits will be set to 1-1.



MULTIPLE SECTOR READ OPERATIONS

COMMAND DESCRIPTION

RESET **(Hex Value = 00)**

This command causes the UDC to return to a known state. This command allows the system software to reset the chip, and has the same effect as $\overline{RST}$ input becoming active.

DESELECT DRIVE **(Hex Value = 01)**

This command causes all of the drive select bits (Drive Select 0-3) in the OUTPUT 1 and OUTPUT 2 registers to become inactive.

RESTORE DRIVE **(Hex Values = 02, 03)**

This command will cause the HDC 9224 to output step pulses to the selected drive, so as to move the head back to Track 00. Before each step pulse, the UDC first checks the TRK00 and READY bits in the DRIVE STATUS register. If TRK00 is active (high) or READY is inactive (low), then the UDC will terminate the command.

The UDC will output up to 4096 step pulses. If the drive does not respond with an active (high) TRK00 signal within this period, the UDC will terminate the command with the DONE bit set (to "1") and the COMMAND TERMINATION CODE bits set to 1-0. (These bits are contained in the INTERRUPT STATUS register.)

This command takes two forms:

COMMAND BYTE	RESULT
02	The command will terminate, and an interrupt generated after the UDC has issued the step pulses.
03	The command will terminate, and an interrupt generated after the drive has provided a SEEK COMPLETE signal to the UDC. (This is useful in systems with "buffered seek" drives.)

This command uses the step rate value loaded into the MODE register.

STEP IN 1 CYLINDER **(Hex Values = 04, 05)**

This command will cause the HDC 9224 to issue one step pulse towards the inner most track. This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
04	The command will terminate, and an interrupt generated after the UDC issues the step pulse.
05	The command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of SEEK COMPLETE the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE register.

STEP OUT 1 CYLINDER **(Hex Values = 06, 07)**

This command will cause the HDC 9224 to issue one step pulse towards the outer most track (Track 00). This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
06	This command will terminate, and an interrupt generated after the UDC issues the step pulse.
07	This command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of the SEEK COMPLETE, the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE Register.

POLL DRIVES (Hex Values = 10 thru 1F)

This command polls the drives for a SEEK COMPLETE signal allowing the user to perform simultaneous seeks on up to four drives. Polling is enabled by setting (to 1) the appropriate bit in the command word: bit 0 for drive 0 thru to bit 3 for drive 3.

This command executes as follows:

The UDC will output a drive select for the first drive in the polling sequence and look for a SEEK COMPLETE status input from the polled drive. If the polled drive has not completed a seek, then this line remains low (logic 0), and the UDC selects the next drive in the polling sequence. This continues until the UDC detects a SEEK COMPLETE signal from a drive, which causes the DONE bit in the Interrupt Status register to be set, and the command terminates.

The UDC will continue to select the drive that produced the SEEK COMPLETE signal, allowing the user to read the DRIVE STATUS register to determine which drive caused the command termination.

The POLL DRIVES command must be preceeded by DESELECT.

DRIVE SELECT (Hex Values = 20 thru 3F)

This command will cause one of (up to) four drives to be selected for operation. Any previously selected drive is deselected by this command. Bits 0 and 1 in the command word indicate (in binary form) which of the (up to) four drives has been selected.

COMMAND WORD		DRIVE SELECTED
DB1	DB0	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

Decoded drive select signals are then placed on the data bus (via AB7-AB4) during OUTPUT 1 times and should be latched externally.

Since the HDC 9224 can interface both hard disks and floppy disks to a processor, the Drive Select command needs to also specify the type of drive being selected. Bits 2 and 3 in the command word are used to pass this information to the chip, and take the following form:

COMMAND WORD		TYPE OF DRIVE
DB3	DB2	
0	0	Hard disk with ST506 (Seagate) compatible format—256 byte data field and 3 byte ID field per sector. No internal clock prescaling performed.
0	1	Hard disk with user defineable format. This format allows a data field length of 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes with 4 byte ID field per sector. No internal clock pre-scaling is performed.
1	0	8 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 1 MHz clock to be compatible with standard disk data rates.
1	1	5.25 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 500 KHz clock to be compatible with standard disk data rates.

NOTE: Microfloppy system designers should determine whether the drive they have chosen to use in the system is compatible with 8″ floppy drives or 5.25″ floppy drives, and use the appropriate values from the table above.

Note that eight inch Winchester-type drives require an 8.696 MHz system clock. All other drives require a 10 MHz system clock. It is not possible for the UDC to derive internally the clocks required for floppy disk operation from the 8.696 MHz clock required by 8 inch Winchester drives.

To insure compatibility with various drives, the HDC 9224 features a programmable head load timer. Head load delay may be inhibited by resetting the Delay Bit (Bit 4) in the Drive Select command word to 0. If Bit 4 is set (to 1), then the head load delay timer is configured with the value in the DATA/DELAY register (Register A), multiplied by value shown below:

DRIVE AND FORMAT SELECTED	HEAD LOAD TIMER INCREMENT (BIT 4 = 1 = Delay Enabled)	
5.25″ HARD DISK (Double Density)	200 usec	
5.25″ HARD DISK (Single Density)	400 usec	
8″ FLOPPY (Double Density)	2 msec	(The HEAD LOAD TIMER is set to a value equal to this increment times the number in the DATA/DELAY register.)
8″ FLOPPY (Single Density)	4 msec	
5.25″ FLOPPY (Double Density)	4 msec	
5.25″ FLOPPY (Single Density	8 msec	

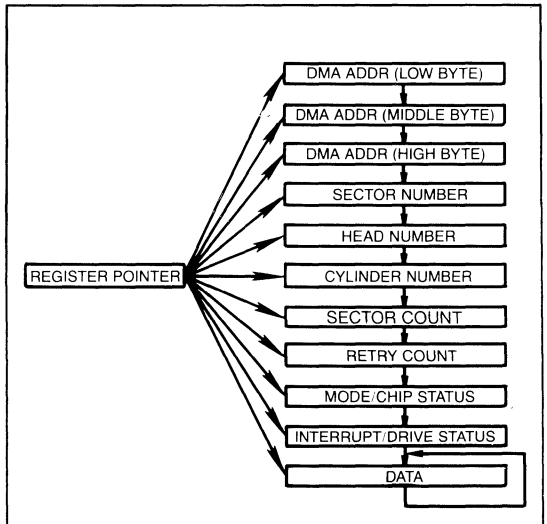
The Drive Select command also optimizes certain characteristics of the HDC 9224 for the type of drive selected.

IF HARD DISK SELECTED:

–DMA mechanism works in burst mode and the bus is held for the entire sector transfer.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.



SET REGISTER POINTER COMMAND

IF FLOPPY DISK SELECTED:

–DMA mechanism transfers an 8-bit byte, and releases the bus.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.

–The CLK input clock is prescaled (internally) to create an internal clock compatible with the floppy disk data rates.

SET REGISTER POINTER (Hex Values = 40 to 4A)
This command causes the register pointer to point to a register. The desired register number is loaded into the 4 least significant bits of the command word. (MSB in BIT 3).

The register pointer is incremented by the UDC on each register access, until it points to the DATA register. This reduces the number of times the user must set the register pointer during read and write operation.

Care should be taken to ensure that only valid register values are loaded into the command word. (Valid register numbers are 0 thru OAH.)

SEEK/READ ID (Hex Values = 50 to 57)
This command will cause the UDC to read the first sector ID field found from the currently selected drive, head, and cylinder. The MODE register should contain the correct value for step rate and density options.

After reading the ID field the UDC will examine the command word and execute the specified options. Bits 2 thru 0 in the command word are used to specify the following options:

BIT 2 = 1 STEP ENABLE. The UDC will execute the step sequence, and position the head on the track specified by the DESIRED CYLINDER register.

BIT 2 = 0 STEP DISABLE. No step pulses will be issued by the UDC.

BIT 1 = 1 WAIT FOR COMPLETE. The UDC will proceed to the verify sequence only after the drive has issued a SEEK COMPLETE signal.

BIT 1 = 0 DO NOT WAIT FOR COMPLETE. The UDC will proceed to the verify sequence after the last step pulse has been issued.

BIT 0 = 1 VERIFY ID. The UDC will execute the VERIFY sequence after operations selected by the previous options have finished.

BIT 0 = 0 DISABLE VERIFY ID. The UDC will not enter the VERIFY sequence. Instead, the command will terminate.

The order in which these options execute is: STEP, COMPLETE, VERIFY ID. Any combination of these option bits may be specified in the command word.

READ SECTORS PHYSICAL (Hex Values = 58 and 59)
This command will cause the UDC to read up to a full track from the disk. The user specifies the MODE, DESIRED CYLINDER, DESIRED HEAD, and DESIRED SECTOR along with the SECTOR COUNT. The UDC will find the requested cylinder and sector and set up to begin the data transfer.

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

If a BAD SECTOR bit is read (from the sector ID field) the UDC will set the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to 1-0, and set the DONE bit (in the INTERRUPT STATUS register) to 1, and terminate the command.

After each sector is successfully read, the SECTOR COUNT register is decremented. If the SECTOR COUNT register is not yet equal to 0 the process is repeated for the next physical sector on the track. This command also will terminate if the Index pulse is received from the drive.

(Note that after the first sector is found, no further comparison is made against sector numbers found on the disk as the DESIRED SECTOR register value may not correspond to the next physical sector on the disk because of sector interleaving.)

This command takes two forms allowing the user to specify the desired transfer option. The options are specified by Bit 0 in the command word, and are:

BIT 0 = 1 TRANSFER ENABLE. The UDC will transfer the data fields to (external) memory, using DMA.

BIT 0 = 0 TRANSFER DISABLE. The UDC will NOT transfer any data to (external) memory, but all error detection circuitry will be enabled and errors reported. This is useful in detecting bad sectors and tracks on the disk.

Before executing this command, the user must set the RETRY COUNT to 0. This is done by loading the high order nybble in the RETRY COUNT register to "1111" (zero in 1's complement format). Failure to do this will result in unpredictable performance because the DESIRED SECTOR register value may not correspond to the next physical sector on the disk.

READ TRACK (Hex Values = 5A and 5B)
When this command is issued, the UDC will read the data from the entire track on which the selected drive is currently sitting. The UDC will begin reading when it detects the leading edge of an index mark signal from the drive, and terminate reading when it detects the next leading edge of an index mark signal. Sync detect is performed for the ID field, but no error checking is done on the data field.

This command allows the user to specify a data transfer option, using Bit 0 in the command word. These options are:

BIT 0 = 1 TRANSFER ALL DATA. The UDC will transfer the ID field and data fields to (external) memory.

BIT 0 = 0 TRANSFER ONLY IDs. The UDC will transfer only ID fields to the (external) memory. This is useful during tape backup operations.

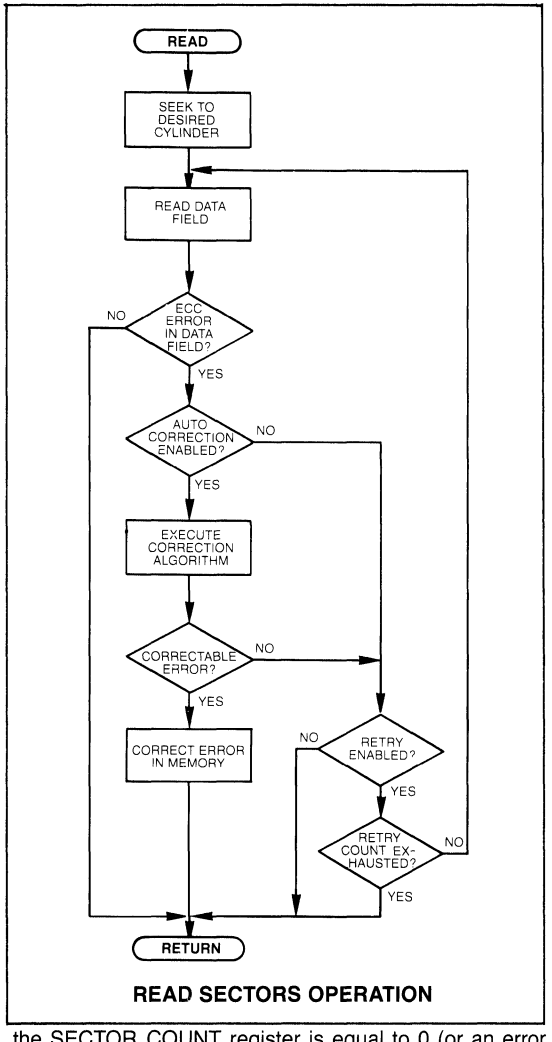
READ SECTORS LOGICAL (Hex Values = 5C to 5F)
When this command is issued, the UDC will read up to a full track from the selected drive. Prior to reading the data from the disk, the UDC will use the information in the MODE, DESIRED CYLINDER, DESIRED SECTOR and DESIRED HEAD registers to locate the correct track, sector and drive surface (using the previously described VERIFY sequence).

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

Before the command is issued, the system processor must also load the desired values into the MODE, SECTOR COUNT, RETRY COUNT and the three DMA registers.

When reading multiple sectors, the read command must be configured with ECC correction disabled. If a hard error is detected, the sector count must be set to one, retry count to zero, and ECC correction enabled. The sector can then be read and corrected. After the error has been corrected, ECC correction can be disabled, retry can be re-enabled, and the remainder of the data can be read.

After the desired track and sector is found and verified, the DATA TRANSFER sequence begins. After each successful sector transfer, the UDC increments the DESIRED SECTOR register (except after the last sector is transferred), decrements the SECTOR COUNT register, and re-enters the VERIFY sequence. This process continues until



READ SECTORS OPERATION

the SECTOR COUNT register is equal to 0 (or an error occurs).

This command has four options, which are specified by Bit 1 and Bit 0 of the command word. The four options are:

BIT 1 = 1 BAD SECTOR BYPASS. If, during the read, the UDC finds a sector with the BAD SECTOR bit set (from the sector ID field on the disk), the sector be skipped, the sector count will not be decremented, and the sector number will not be changed.

BIT 1 = 0 BAD SECTOR TERMINATE. If, during a read, the UDC finds a sector with the BAD SECTOR bit set, the UDC will set the COMMAND TERMINATION CODE to 1-0, set the BAD SECTOR status bit and the DONE status bit, and terminate the command (with an interrupt, if enabled). All of the above named status bits are contained in the INTERRUPT STATUS register.

BIT 0 = 1 TRANSFER ENABLED. The UDC will transfer data from the disk to the system. The DMA REQUEST status bit (in the INTERRUPT STATUS register) will be set when the UDC requires servicing.

BIT 0 = 0 TRANSFER DISABLED. The UDC will not transfer data read from the disk, but all error checking circuitry will be enabled.

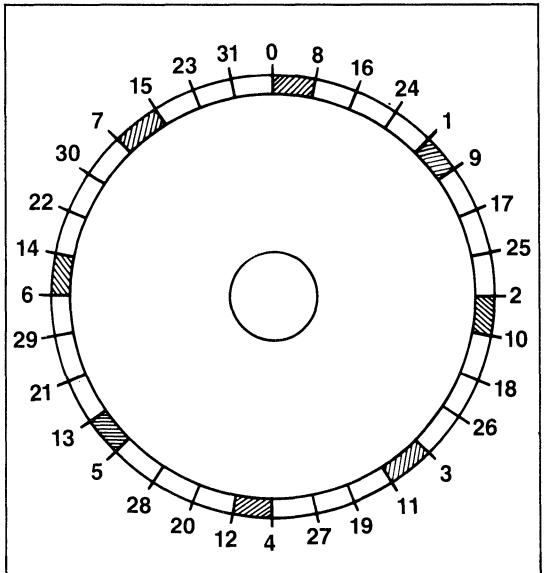
FORMAT TRACK (Hex Values 60 to 7F)

This command causes the UDC to format the current cylinder from the leading edge of one index mark to the leading edge of the next index mark. The format chosen is dependent on the Drive Select command.

During execution of the FORMAT TRACK command, the UDC will fetch all required ID field data from external memory, and write it to the disk, along with format constants supplied automatically by the UDC. This reduces the number of bytes required to format a sector to 3 or 4, depending on the format chosen.

Before the FORMAT TRACK command can be given, the system processor must:

1. Generate an ID Field table for the track in UDC memory area. This ID Field Table consists of:
   CYLINDER BYTE
   HEAD BYTE
   SECTOR NUMBER BYTE
   SECTOR SIZE/ECC SIZE BYTE (not required for ST-506 formats) repeated for each sector on the track.



INTERLEAVED SECTORS

The UDC can format a track with interleaved sectors by staggering the sector numbers. For example, to format a 32 sector track, with a sector interleave factor of 4, the system processor would set up the ID Field table sector numbers as follows:
0,8,16,24,1,9,17,25,2,10,18,26,3,11,19,
27...7,15,23,31.

(Note that when formatting in ST506 mode, only three bytes are required for each sector, while four bytes are needed for IBM or user defineable formats. Also note that sector numbers start with zero (0) on ST506 compatible format, and start with one (1) on IBM formatted floppy diskettes.)

2. Load the UDC DMA registers with the starting address of the external memory buffer containing the ID Field data just created.

3. Issue the DRIVE SELECT command, which moves the DMA registers to the CURRENT HEAD, CURRENT CYLINDER, and a TEMPORARY REGISTER. (This is necessary because the UDC will now re-use the DMA registers to hold format parameters).

   When formatting multiple cylinders, the system processor does not need to re-issue DRIVE SELECT between cylinders as the STEP IN and STEP OUT commands preserve the DMA addresses and format parameters. It is necessary, however, to update the ID Field table, described in #1, above.

4. Load the DESIRED HEAD register with the proper value.
5. Load the following values (in the format shown) into the registers indicated below:

PARAMETER	FORMAT	REGISTER
GAP 0 Size	two's complement format	DMA 7-0
GAP 1 Size	two's complement format	DMA 15-8
GAP 2 Size	two's complement format	DMA 23-16
GAP 3 Size	two's complement format	Desired Sector
Sync Size	one's complement format	Desired Cylinder
Sector Count	one's complement format	Sector Count
Sector Size Mult.	one's complement format	Retry Count

FORMAT PARAMETERS TABLE

When using ST506/PC (fixed length) hard disk format, the values for GAP 0 and GAP 1 must both be set to the same number, and loaded into the appropriate DMA register.

The Sector Size Multiple programs the UDC to format with a sector size that is a multiple of 128 data field bytes. For example, to format a track with a sector data field size of 512 bytes, then the Sector Size Multiple would be set to FB hex, which is "4" in one's complement notation.

In ST506/PC format, the sector size is fixed at 512 bytes. In IBM floppy disk format, the sector sizes allowed are 128, 256, 512, or 1024 bytes. With user defineable hard disk formats, allowed sector sizes are 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes.

6. Load the MODE register to specify the step rate, single or double density option, and CRC/ECC options.
7. Step to the desired track. For the first track, this is normally done by issuing a RESTORE DRIVE command, to return the heads to Cylinder 000, then use the STEP IN 1 or STEP OUT 1 commands to move the head to subsequent cylinders on the disk.
8. Issue the FORMAT TRACK command. All data fields on the disk will be filled with E5 hex. In double density recording (MFM) all gaps will be filled with 4E hex, while in single density (FM) all gaps will be filled with FF hex. This format is compatible for IBM specifications for floppy disks.
9. To Format additional tracks, it is only necessary to update the ID Field table (step 1) and repeat steps 7 and 8. Do NOT modify the DESIRED HEAD register when formatting additional tracks with the same head. If it is necessary to change the DESIRED HEAD register, the system processor must repeat all steps described above.

   The FORMAT TRACK command allows the user to specify several options. These options are specified by setting the appropriate low order bits in the command word. The bit mapping for these options are:

BIT 4 = 1 Write Deleted Data Mark. During the format process, the UDC will write the deleted data mark (F8 hex) for the data address field.

BIT 4 = 0 Write Normal Data Mark. During the format process, the UDC will write the normal data field address mark (FB hex).

BIT 3 = 1 Write with Reduced Current. When this bit is set, the Reduced Write Current Output will go high (active) during the Output 2 time slot.

BIT 3 = 0 Write with Normal Current. When this bit is reset, the Reduced Write Current Output wil remain low (inactive) during the Output 2 time slot.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during the format of disks. The following table specifies these values:

SECTOR SIZE FIELD BITS

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	track number							
HEAD	side number							
SECTOR	sector number							
SECTOR SIZE							sector size (2 bits)	

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	cyl # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	cyl # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							
SECTOR SIZE	ECC type				X		sector size (3 bits)	

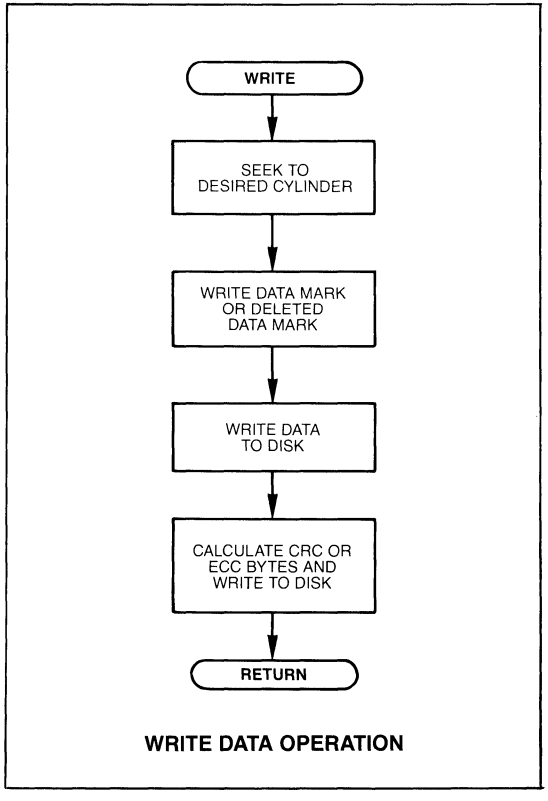
BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

WRITE SECTORS LOGICAL (Hex Values A0 thru BF, E0 thru FF)

This command will cause the UDC to write logically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).



WRITE DATA OPERATION

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register.

Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next logical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flag set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 1 WRITE LOGICAL COMMAND BIT (Always set to "1" for Write logical command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: For hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

WRITE SECTORS PHYSICAL (Hex Values 80 thru 9F, C0 thru DF)

This command will cause the UDC to write physically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and

verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register. Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next physical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flat set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 0 WRITE PHYSICAL COMMAND BIT (Reset to "0" for Write Physical Command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to floppy disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: for hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

TAPE BACK-UP (Hex Values = 08 to 0F)

The TAPE BACK-UP command set provides the system with the capability of transferring data to and from a tape drive in continuous blocks. TAPE BACK-UP utilizes the UDC's DMA, data conversion, error detection/correction and sector count circuitry.

Because of the mechanical and electronic differences between tape drives and disk drives, some of the register bits described earlier in this data sheet change functions when the UDC is executing the TAPE BACKUP COMMAND. In many cases, the CLK input to the UDC will also need to be changed to compensate for the slower data rate from tape drives.

TAPE BACKUP REGISTER DESCRIPTION

The following bits in the UDC's register file assume the functions listed below when executing the BACK-UP command and should be programmed accordingly.

The following tables describe the differences in register usage when the UDC is executing the TAPE BACKUP command. (Complete TAPE BACKUP register bit maps are located in rear of the data sheet.)

MODE REGISTER

Bit 2 = 1 16 byte sync detect delay enable
= 0 16 byte sync detect delay disabled

Bit 1 = 1 TAPE BACKUP Write Enable (writing)
= 0 TAPE BACKUP Write Disable (reading)

Bit 0 = 1 Tape mark enable (short block)
= 0 Tape mark disable (long block)

RETRY COUNT REGISTER

Bits 7-4 Retry should be disabled, by setting these bits to "1". (Retry Disabled)

Bits 3-0 program outputs (user controlled). Bit 3 is typically used for write enable to the tape drive.

Bits 0 and 1 are typically used for tape driven motion control as per drive manufacturer's specification.

DESIRED CYLINDER

Bits 7-4 ECC Type Field:

DB7	DB6	DB5	DB4	ECC TYPE
0	0	0	0	4 ECC bytes generated/ checked
1	1	1	1	5 ECC bytes generated/ checked
1	1	1	0	6 ECC bytes generated/ checked
1	1	0	1	7 ECC bytes generated/ checked

note: 5, 6, 7 byte ECCs are generated and checked by hardware external to the UDC.

DESIRED CYLINDER

Bit 3 Always 1

Bits 2-0 Data Block Size:

DB2	DB1	DBO	DATA BLOCK SIZE
0	0	0	128 bytes
0	0	1	256 bytes
0	1	0	512 bytes
0	1	1	1024 bytes
1	0	0	2048 bytes
1	0	1	4096 bytes
1	1	0	8192 bytes
1	1	1	16,384 bytes

Remember that the UDC internal ECC code can correct up to a 4K byte long Data Block, but that the larger the Data Block the greater the probability of a miscorrection.

Also, when executing the TAPE BACKUP command, the DRIVE SELECT command is altered slightly, as illustrated below:

DRIVE SELECT COMMAND								
Bit #	7	6	5	4	3	2	1	0
Drive Select	0	0	1	Ramp Up/Down delay enable	1	CLK divisor	1	1

DB2	CLOCK DIVISOR FOR TAPE
0	CLK is divided by 10 (similar to 8" floppy divisor).
1	CLK is divided by 20 (similar to 5.25" floppy divisor).

These bits, in conjunction with Bits 4 and 7 of the MODE register, will allow selection of both FM and MFM recording on tape, with a tape format that resembles IBM compatible floppy disk formats.

Setting the Drive Type bits to 1,0 or 1,1 will also cause the UDC to take on the following characteristics:

- –DMA mechanism transfers a byte (8 bits) and relinquishes the bus.
- –The RDGATE and WRGATE output signals have timing characteristics as shown in Figures 12A and 12B of the UDC spec.
- –The gap lengths are as illustrated in Table 1 or the UDC spec.
- –Tape format parameters will be as per Table 1 of the UDC spec.

COMMAND EXECUTION OVERVIEW

The tape backup command allows the user a convenient method of backing up either floppy or hard disks to tape. The UDC may be interfaced to either cartridge or cassette type tape drives, working in either streaming or start/stop mode.

Read and Write functions of TAPE BACKUP share a common command byte. The three LSB's of the MODE register are also used by the TAPE BACKUP command to specify user options, and to select between tape read or tape write mode.

Two kinds of blocks may be specified when reading or writing dependent on the state of the TAPE MARK ENABLE bit in the MODE register:

1. DATA BLOCK. The length of the data block (also called a long block) is equal to:

   2^n* 128 bytes where n is an integer between 0 and 7 inclusive. The desired length of the data block (2^n) is programmed into the desired cylinder register.

2. TAPE MARK. The minimum length of the tape mark (also called a short block) is 3 bytes. The maximum length of the tape mark is 257 bytes. The desired length is programmed into the sector count register.

Multiple data block transfers are accomplished by programming the 1's complement of the desired number of data blocks to be transferred into the sector count register.

The three LSB's of the MODE register function as part of the BACK-UP command word. The WRITE ENABLE bit determines whether loading the BACK-UP command into the UDC will initiate execution of a BACK-UP READ or BACK-UP WRITE sequence. The TAPE MARK ENABLE bit determines whether the UDC will write a short or long block of data on the tape and the DELAY ENABLE bit determines whether or not the RDGATE signal is stretched when it coincides with a sync mark when reading the tape. The remaining bits in the command word are as follows:

COMMAND	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BACK-UP (READING)	0	0	0	0	1	0	0	xfer enable
BACK-UP (WRITING)	0	0	0	0	1	precomp value		

BACK-UP READ

When reading a short block, only CRC is checked. When reading a long block, CRC or ECC will be checked, depending on the CRC/ECC bits in the Mode register.

Bit 0 = 1 Data transfer enabled, error checking enabled
= 0 Data transfer disabled, error checking enabled

BACK-UP WRITE

When writing, the precompensation value is derived from the CLK frequency as follows:

Bit 2	Bit 1	Bit 0	Precompensation
0	1	0	None, enable EARLY and LATE
1	0	1	6 CLK cycle periods
0	1	1	5 CLK cycle periods
1	1	1	4 CLK cycle periods
1	1	0	3 CLK cycle periods
1	0	0	2 CLK cycle periods
0	0	1	1 CLK cycle period
0	0	0	None, suppress EARLY and LATE
PRECOMPENSATION SELECT FOR BACK-UP COMMAND			

TAPE BACKUP SYSTEM CONFIGURATION NOTES

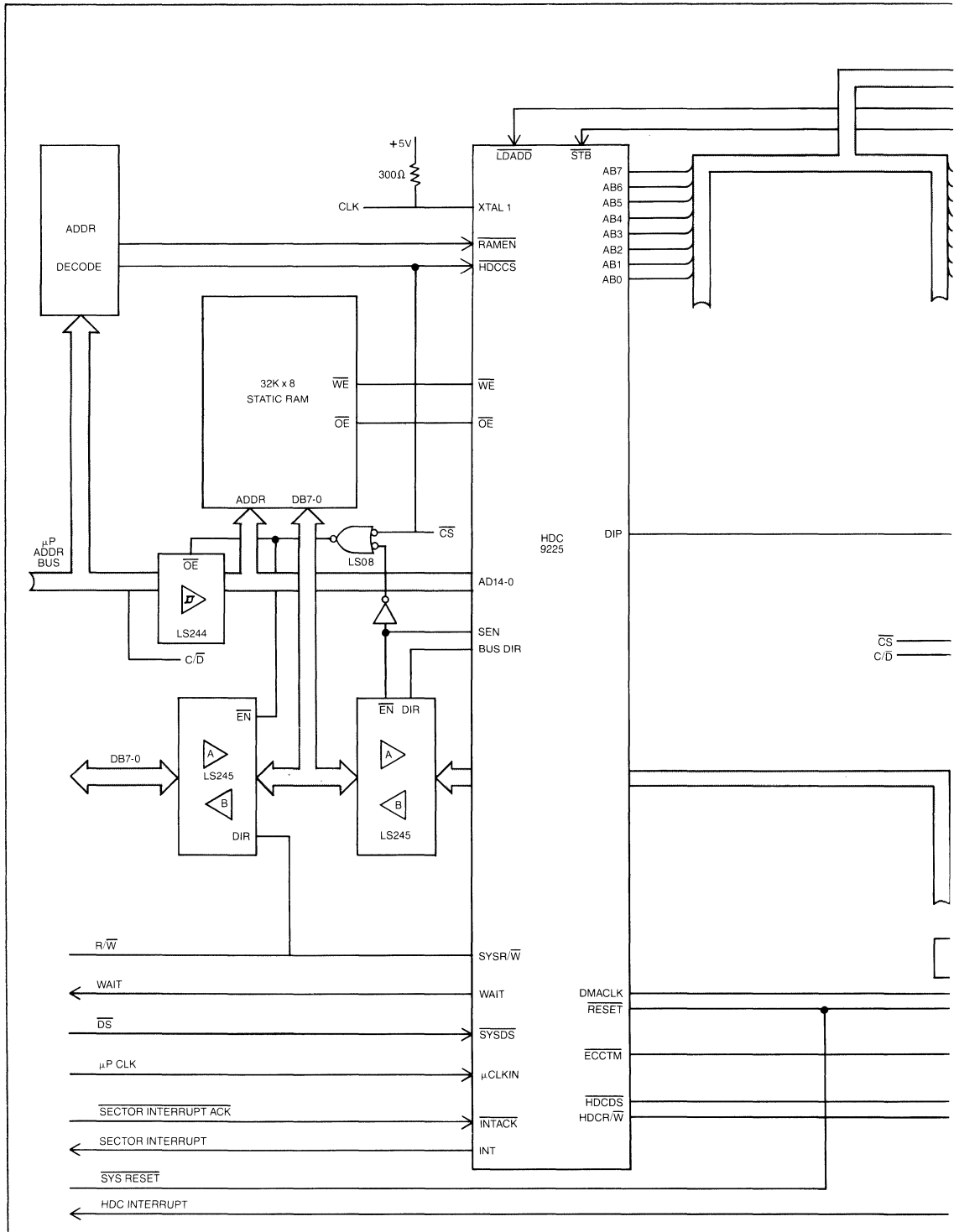
(A schematic showing a typical system implementation using the TAPE BACKUP feature is contained in Schematic Diagram 2.)

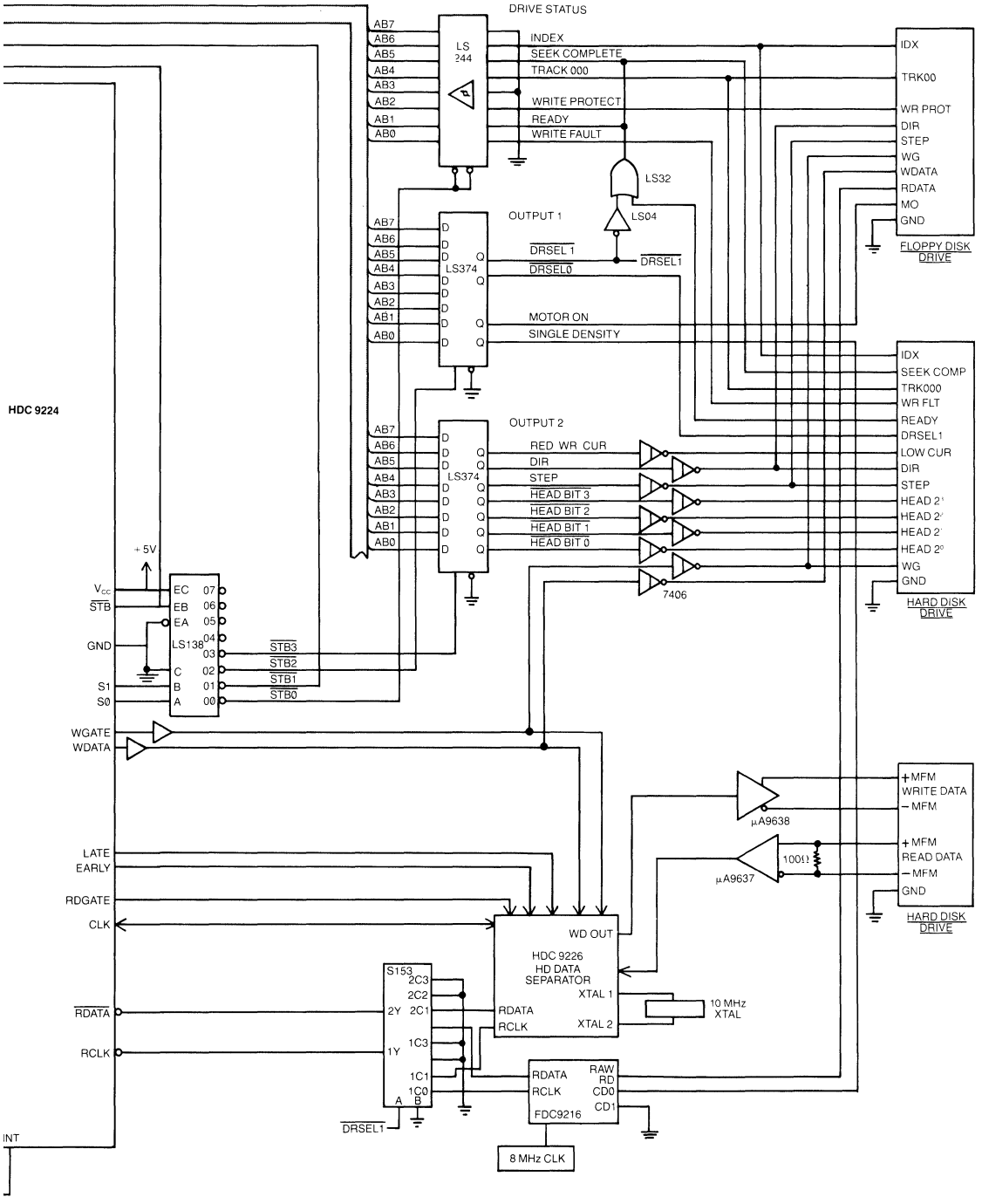
1. Proper operation of the TAPE BACKUP command requires that the tape drive be addressed as DRIVE #3 by the UDC.
2. During the UDC's OUTPUT 2 period external circuitry must enable a separate latch to receive the user defined IO bits and tape track number bits. This latch should use the DRIVE SELECT 3 signal (output during the OUTPUT 2 period) so that the contents of the latch may only be changed when the tape drive is selected.

   Four additional drive control signals may be loaded into the four LSB's of the RETRY COUNT register. These additional outputs are latched externally during OUTPUT 1 times for use by the tape drive. These outputs would normally be used to control tape drive Write Enable logic (bit 3) and tape motion (bits 0 and 1), and tape motor on and off (bit 2).

3. It is important to consider the time required for a tape drive to come up to operating speed when using the TAPE BACKUP command. Also, to insure adequate spacing between tape blocks, a delay is frequently required before stopping tape motion. The UDC has a programmable Ramp Up and Ramp Down timer to allow for easier implementation. The desired delay is programmed into the DATA/DELAY register before issuing the DRIVE SELECT "3" command.

CLOCK DIVISOR BIT	DENSITY BIT MODE REGISTER BIT 4	TIME IN SECONDS PER DELAY REGISTER COUNT
1	1 (Single)	1 CLK Cycle * 80000
1	0 (Double)	1 CLK Cycle * 40000
0	1 (Single)	1 CLK Cycle * 40000
0	0 (Double)	1 CLK Cycle * 20000


+5V
300Ω
CLK
XTAL 1
LDADD
STB
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
ADDR
DECODE
RAMEN
HDCCS
32K x 8
STATIC RAM
WE
OE
ADDR
DB7-0
CS
HDC
9225
DIP
μP
ADDR
BUS
OE
LS08
AD14-0
LS244
C/D
SEN
BUS DIR
EN
EN DIR
DB7-0
A
B
LS245
DIR
R/W
SYSR/W
WAIT
DS
SYSDS
μP CLK
μCLKIN
SECTOR INTERRUPT ACK
INTACK
SECTOR INTERRUPT
INT
SYS RESET
HDC INTERRUPT
DMACLK
RESET
ECCTM
HDCDS
HDCR/W


DRIVE STATUS
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
LS 244
INDEX
SEEK COMPLETE
TRACK 000
WRITE PROTECT
READY
WRITE FAULT
LS32
LS04
IDX
TRK00
WR PROT
DIR
STEP
WG
WDATA
RDATA
MO
GND
FLOPPY DISK DRIVE
OUTPUT 1
LS374
DRSEL 1
DRSEL0
DRSEL1
MOTOR ON
SINGLE DENSITY
HDC 9224
OUTPUT 2
RED WR CUR
DIR
STEP
HEAD BIT 3
HEAD BIT 2
HEAD BIT 1
HEAD BIT 0
7406
IDX
SEEK COMP
TRK000
WR FLT
READY
DRSEL1
LOW CUR
DIR
STEP
HEAD 2¹
HEAD 2²
HEAD 2³
HEAD 2⁰
WG
GND
HARD DISK DRIVE
+5V
Vcc
STB
GND
S1
S0
LS138
EC 07
EB 06
EA 05
04
03
C 02
B 01
A 00
STB3
STB2
STB1
STB0
WGATE
WDATA
LATE
EARLY
RDGATE
CLK
RDATA
RCLK
INT
μA9638
μA9637
100Ω
+MFM WRITE DATA
−MFM
+MFM READ DATA
−MFM
GND
HARD DISK DRIVE
WD OUT
HDC 9226
HD DATA SEPARATOR
XTAL 1
XTAL 2
10 MHz XTAL
RDATA
RCLK
S153
2C3
2C2
2Y 2C1
1C3
1Y
1C1
1C0
A B
DRSEL1
RDATA
RCLK
FDC9216
RAW RD
CD0
CD1
8 MHz CLK

SECTION VII

The UDC will issue a normal interrupt (with the command termination code set to 0-0) when the RAMP UP or RAMP DOWN timer has expired.

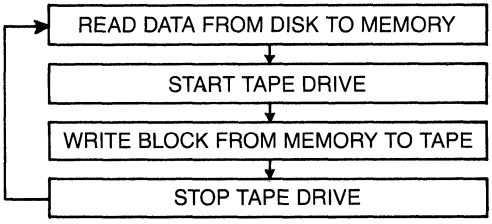
4. BACK-UP WRITE. The user will first request the UDC to perform a disk READ TRACK command, with the TRANSFER ENABLE bit in the command word reset. This will cause the UDC to transfer only the ID field information to memory.

   The TAPE BACKUP command will then be issued causing the UDC to write this ID information to the tape as a tape mark (typically 96 bytes for a drive formatted with a 3 byte/sector ID field or 128 bytes for a drive formatted with a four byte/sector ID field. The data fields should then be transferred to the tape in a similar manner.

   The UDC may be used with either "Streaming" or "Start/Stop" type tape drives. This is illustrated by the following examples:

   A. START/STOP TAPE DRIVE:

   typically transfers ½ or 1 disk track at a time as illustrated by the following flow chart:



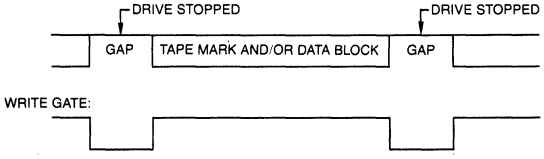
   When controlling a start/stop tape drive, the UDC will write the data "block by block". The system will issue a Drive Select command to the UDC with the Tape Motion, Motor On and Write Enable bits set to start and write data to the tape.

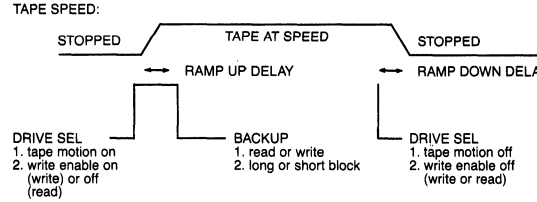
   The UDC will interrupt the system after the completion of the Ramp Up Delay indicating that the tape drive is up to speed. This interrupt is distinguished by the Command Termination Code of 0-0 (normal completion of command).

   The System then outputs the Write command (for a long or short block) and waits for the command termination interrupt. The UDC will write the Sync mark and tape mark or data block on the tape.

   When the System receives the interrupt indicating completion of the Write command, it will issue another drive select command with the Motor On and Write Enable bits set to stop the drive. The UDC will interrupt the system after completion of the Ramp Down Delay indicating that the tape has stopped moving.

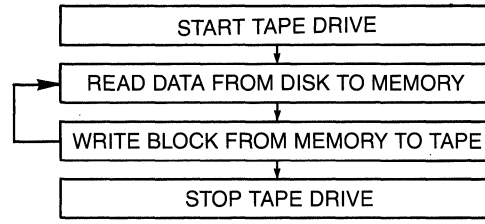
   The UDC will turn the Write Gate signal on when it is writing data and off when it is not, without regard to the tape motion. The Write Gate signal is used to generate "gaps" on the tape between the data blocks. This is done by externally forcing the two Data outputs with the Write Gate signal such that the Data + signal is high and the Data − signal is low when the UDC is not writing data to the tape (Write Gate is off):





   B. STREAMING TAPE DRIVE:

   typically transfers 1 sector at a time as illustrated by the following flow chart:



   Control of a streaming tape drive is similar to that of a start/stop drive. The tape is started at the beginning of the data transfer and stopped after the last block is written to the tape. The tape is not stopped in between blocks. The UDC will however turn the Write Gate signal on when it is writing data and off when it is not so that gaps will be written (with external hardware) on the tape between the data blocks.

5. BACK-UP READ. The data is read from the tape (in either start/stop or streamer mode) and buffered in memory. The disk track is then reconstructed from the data.

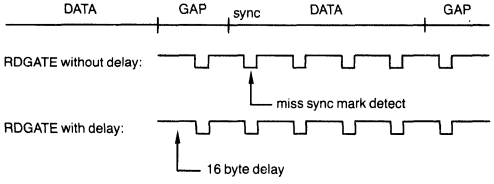
   The start/stop drive typically has a track (or half a track) of disk data stored as a block. It is therefore expedient to read in the data "block by block". When reading data from a streamer drive use can be made of the SECTOR COUNT register and a track's worth of data blocks may be read from the tape before generating the track on the disk.

   Tape motion control is similar to that described above except that the Write Enable Bit is off to inhibit writing to the tape. The UDC reads the tape until it detects a sync mark. After detecting a sync mark the UDC will transfer the data found on the tape to memory.

6. The search count is used when reading the tape. It specifies a maximum number of blocks of 128 bytes between adjacent data blocks. If the search count expires before sync is detected, the command is terminated.

   For example, if a search count of two is specified by loading the Desired Sector register with FD (hex), the UDC will search for 256 byte times before terminating the command. This will prevent the UDC from accidentally skipping a block. The search count is typically about the size of one block length. In the following figure, TM1 and TM2 are two tape marks and DB1, DB2, DB3 etc. are their associated Data Blocks:

7. 16 BYTE DELAY. Provision is made to shift the RDGATE pulse in the event that it coincides with the data block sync mark. If a tape cannot be read (sync is never detected) the tape can be re-read with the 16 byte delay enabled.



8. The DRIVE STATUS bits may be used by the tape drive if they are enabled (on the drive) by DRIVE SELECT 3. The ready change interrupt is especially handy for detecting start of tape (SOT) and end of tape (EOT) as a UDC command can be terminated by a change in state of the READY input.
9. The DATA FORMAT is as follows:

PRE	TMSYNC	TAPE MARK	POST GAP	PRE	DBSYNC	DATA BLOCK	POST GAP

The Tape Mark sync mark (TMSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FE (Hex). The Data Block sync mark (DBSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FB (Hex). A1 (Hex) is encoded with the standard missing clock pattern.

The sync mark is preceeded by a "preamble" consisting of bytes of 00 as per figure 2 of the UDC spec (this is required to synchronize the data separator when reading the tape). The Tape Mark and Data Block (including CRC or ECC bytes) are followed by a "postamble" consisting of one byte of 00.

Note that the postamble is not included in the Floppy Disk formats. The GAP sizes are dependent on the type of drive (start/stop or streamer) and the specific mechanical tape drive specifications.

10. Use can be made of the Sector Count register when doing a "file" (versus a "mirror image") backup on a start/stop tape drive. Instead of transferring the entire disk track to the tape in one long block, the data is moved file by file.

    If, for example, it is desired to back up a file consisting of five 256 byte long Hard Disk sectors, a 2048 byte long Data Block would have to be used for an image backup (the Data Block size is specified as $2^n * 128$ restricting blocks to 128, 256, 512 etc.). This would result in a lot of wasted space on the tape.

    If file backup is used and the Sector Count is set to five, 256 byte long Data Blocks can be used. Gaps will be generated on the tape corresponding to the time required to get the data from the disk drive (corresponding to DMA delays and the disk interleave factor).

    The tape will not be stopped until the entire file is transferred. When using sector count, the UDC internal programming will create inter-block gaps of about 30 to 32 bytes on the tape in both single (FM) and double (MFM) density modes.

SYSTEM CONFIGURATION NOTES

A simplified UDC schematic is shown in Schematic 1. The following notes may be helpful in implementation of the UDC.

1. In systems using a private memory area, it is important to know when the buffer needs servicing from the host processor. A second interrupt signal (INT2) signals the processor that servicing is needed. INT2 is generated by externally ANDING the ECCTM signal with STB1 signal. (The STB1 signal is active when the UDC is outputing the DMA address data, and occurs when STB is active (low), S0 is active (high) and S1 is inactive (low)).

   This "interrupt" occurs only when the UDC needs the system processor to either read from or write to the buffer memory. When reading from the disk, the system processor should empty the memory buffer each time this signal becomes active. (If an ECC error is detected, and error correction is enabled, this signal will not become active until the UDC has attempted to correct the error.)

   When writing data to the disk, the system processor must fill the buffer each time this signal becomes active.
2. The DIP (DMA in Progress) signal is used to isolate the buffer memory from the main system memory. If 74LS244 and 74LS245 address buffers are used in the memory addressing circuits, then this signal should be used to enable or disable the address buffers, as required. This eliminates the possibility of memory contention problems.
3. Write precompensation (for floppy disks) is handled internally by the UDC. For hard disks, the LATE and EARLY signals are connected to a multiplexer which, in turn is connected to a 24 ns delay line. The EARLY and LATE signals will toggle in response to the data pattern being written. This will allow the data being written to the shifted ± 12 ns from the nominal 12 ns delay specified by hard disk manufacturers.
4. The interface to the hard disk drive data inputs and outputs requires RS-422 data tranceivers. Other disk drive interface circuits (including floppy disk data inputs and outputs) may be 74LS series devices.
5. Since the UDC uses its Aux Bus for multiple functions, the system designer must be able to determine which function is occuring on the Aux Bus at any given time. The S0 and S1 signals, when combined with STB signal are decoded (using a 74LS138 or equivalent) to provide STB0-3 signals.

   These generated signals and their respective functions are:

STB0	Drive Status Input Time Slot
STB1	External DMA Address Counters Time Slot
STB2	Output 1 Time Slot
STB3	Output 2 Time Slot

6. The clocks required by the UDC are not TTL-level compatible. Pullup resistors (typically 390 ohms) should be used with Schottky drivers to insure that the clock signals reach the proper Input (high) level, with acceptable rise and fall times.
7. The UDC features a built-in DMA controller that requires connection to external counters. These counters are configured so that they are incremented after each byte is transferred. (The UDC's internal DMA circuits transfer the starting memory address for each read or write operation.) 74LS161 Counters are typically used in this area.
8. The DMACLK input should be tied to the master system clock, through a bus buffer. It is important to remember that three DMACLK periods are required for each DMA transfer.
9. The system design may be simplified, and costs reduced, by using the FDC 9216B Floppy Disk Data Separator, to separate raw data from the floppy disk drive into RDATA and RCLK.

ERROR CHECKING AND CORRECTION CIRCUIT (ECC) OPERATING PRINCIPLES

The UDC will automatically detect and correct errors in the data read from the disk. Error checking may be done using industry standard CRC or ECC encoding. Error correction may be done using either internal or external ECC encoding. This section will explain ECC operation, as implemented on the UDC.

The UDC contains two 16-bit registers used by the CRC/ECC circuits. CRC logic uses only one of these registers, while the logic for ECC uses both registers, implementing a full 32-bit algorithm.

These registers may be preset to either one or zero, using the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION register. (This allows compatibility with existing disk controllers and external ECC chips.) Both ECC and CRC are calculated beginning with the sync mark of the address (CRC) or data (ECC) field.

CRC/ECC GENERATION

The UDC uses the following industry standard polynomials in computing the CRC and ECC check bytes:

CRC: $x^{16} + x^{12} + x^5 + 1$

ECC: $x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$

As the UDC writes data to the disk drive, it first passes this data thru the CRC (and, if enabled, ECC) registers. After all data has been written, the remaining two (CRC) or four (ECC) bytes remaining in these registers are written to the appropriate address or data field.

CRC/ECC CHECKING

When CRC or ECC checking is initiated, the internal CRC/ECC registers are set to either zero or one, as required by the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION REGISTER. Data read from the disk is simultaneously shifted thru the CRC/ECC registers, and transferred to external memory.

After the CRC or ECC check bytes have been shifted thru the CRC/ECC registers, the remainder in these registers should be zero, else an error has occurred in the address or data block.

If CRC or ECC (without correction) is enabled, automatic retry (if enabled) or command termination will occur. If internal ECC with automatic correction is enabled, the correction algorithm will be executed. If the internal ECC algorithm is unable to correct the error (in one attempt), then automatic retry (if enabled) or command termination will occur.

ECC CORRECTION

Error Correction consists of three distinct parts:

1. The CRC/ECC registers are normalized by shifting zeros thru the register. This sets up a data block which is 42,987 bits long, which corresponds to the "natural message length" of the generation polynomial. The actual number of zeros shifted through the registers depends on the difference between the natural message length of the generator polynomial and the actual length of the data block being checked. The longest data block that can be corrected (using the internal ECC algorithm) is 4K bytes.
2. The data input to the CRC/ECC registers is then disabled and the DMA counters are re-initialized to the starting address for this data block. The contents of the CRC/ECC registers are then "ring-shifted" until 21 consecutive zeros are detected. The remaining bits in the CRC/ECC registers compose the error syndrome. As the CRC/ECC registers are shifted, the UDC generates $\overline{DS}$ signals, causing the external DMA counters to be incremented. When the 21 consecutive zeros are detected, the DMA counters are pointing to the corrupt data.

   If the error syndrome is not found within the data block the error is judged to be uncorrectable and the correction algorithm is terminated. (The data block is the length of the data field in the sector and the 4 ECC bytes. A format with a sector size of 256 bytes would have a data block size of 260 bytes.)
3. When the error syndrome is detected, the UDC will enable its $\overline{ECCTM}$ output, read the next byte from memory, exclusive-or it with the first byte of the three byte error syndrome, disable the $\overline{ECCTM}$ output and write the corrected byte back to memory. The correction process is then repeated for the next two bytes in memory.

   When using internal ECC (with correction enabled), the $\overline{ECCTM}$ output is used by the external DMA counters to inhibit the counters from incrementing their addresses when correcting the erroneous bytes. When using external ECC, the $\overline{ECCTM}$ output goes active (low) when the UDC is requesting the ECC Check Bytes from the external ECC chip prior to writing them to the disk.

   After a correction is completed, the UDC will then attempt to read the next sector on the disk (if the SECTOR COUNT register is still greater than zero). Anytime ECC correction has been attempted, (even if unsuccessful), the CORRECTION ATTEMPTED bit in the CHIP STATUS register will be set.

The maximum time required for one ECC Correction Cycle (using the internal algorithm) is:

1) $\frac{\text{(Natural Message Length [Bits])}}{8} + 4 = \text{ECC Cycle Time (in Byte times)}$

2) Maximum ECC Time = ECC Cycle Time + 30 byte times

Since the internal algorithm has a natural message length of 42,987 bits the ECC Cycle time is 5,377 byte times. Since a period of about 30 byte times must be allowed for the read-modify-write operations, the Maximum ECC Time equals 5,407 byte times.

One byte time equals the amount of time required to read one byte for the type of drive selected. For Hard Disks, this is about 1 microsecond. This equates to approximately 1 revolution (maximum) for either 8″ floppy disk (running in double density) or 5.25″ hard disk.

During the entire operation, the RDGATE signal is kept active.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to +70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any Pin, with respect to ground ..... +8 V
Negative Voltage on any Pin, with respect to ground ..... −0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

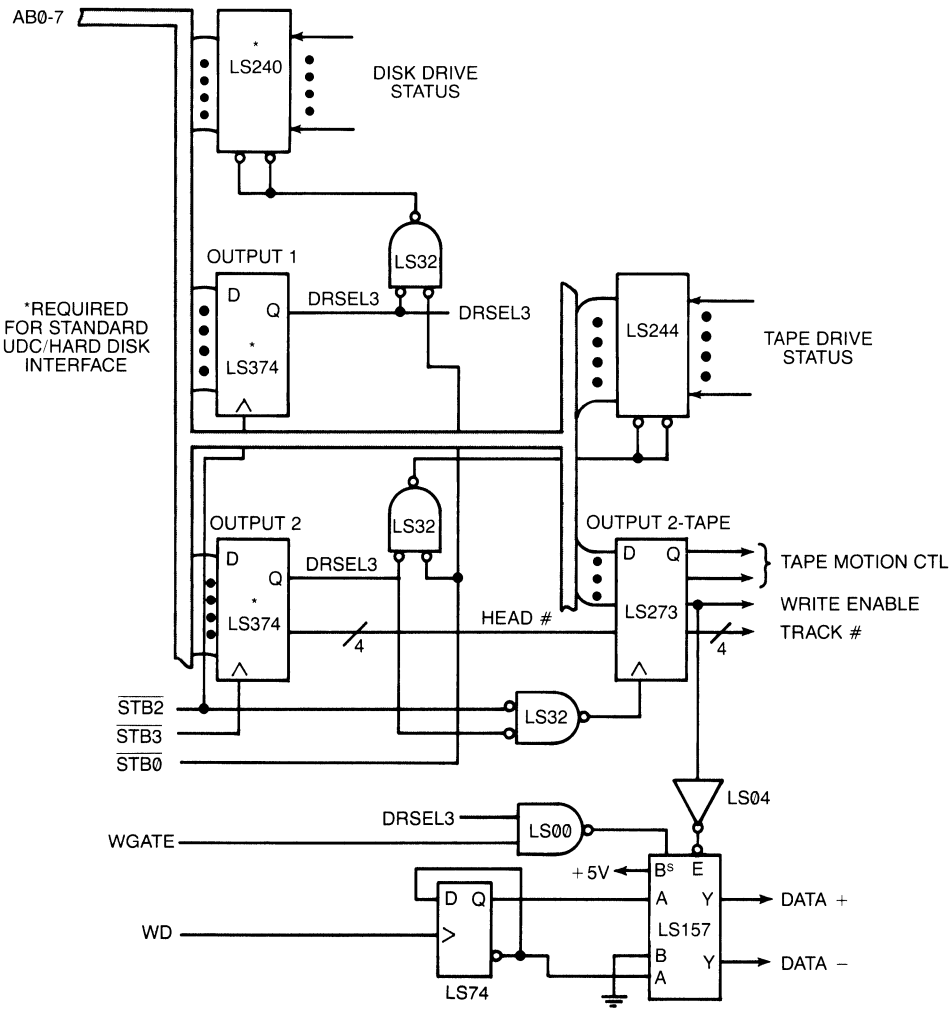
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
Input Voltage						
V_{IL} Low			0.8	V		
V_{IH1} High	2.0			V	all inputs except CLK and DMACLK	
V_{IH2} High	4.2			V	CLK and DMACLK input	
Output Voltage						
V_{OL1} Low			0.4	V	all outputs except WDATA, Early and Late. (Drive 1 TTL load into 50 pf)	I_{OL1} = 1.6 mA
V_{OH1} High	2.4			V		I_{OH1} = 40μA
V_{OL2} Low			0.5	V	WDATA, EARLY and LATE outputs. (Will drive 1 Schottky load into 15 pf.)	I_{OL2} = 2mA
V_{OH2} High	2.7			V		I_{OH2} = 50μA
V_{OL3} Low			0.4	V	DMAR and INT	I_{OL3} = 0.4 mA
V_{OH3} High	2.4			V	DMAR and INT	I_{OH3} = 20μA
Input Leakage Current					0.4V to 3.5V	
I_L			±10	uA		
I_{LC} (Clock)			−600	μA	0V	
Input Capacitance						
C_{IN}			25	pf		
Power Supply Current						
Icc			200	ma		

AC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
PROCESSOR WRITE CYCLE						
C/D, R/W, CS Setup time to DS↓	T_{DSB}	110			ns	FIGURE 3
C/D, R/W, CS Hold time to DS↑	T_{DSB}	0			ns	
DS Pulse Width	T_{DSL}	150			ns	
DS Pulse High Time	T_{DSH}	850			ns	
Data Bus In Setup time to DS↑	T_{DIB}	100			ns	
Data Bus In Hold time to DS↑	T_{DIA}	0			ns	
PROCESSOR READ CYCLE						
Data Access time from DS↓	T_{DOB}	75			ns	FIGURE 3
Data Hold time from DS↑	T_{DOA}	10			ns	
UDC TO MEMORY TIMING (BUS MASTER) (based on 10 Mhz DMACLK Input)						
Write Setup time to DS↓	T_{WB}	110			ns	FIGURE 4
Write Data Strobe Width	T_{WDS}	180			ns	
Write Hold time from DS↑	T_{WA}	110			ns	
Data Strobe Falling Edge	T_{DSF}			15	ns	
Data Strobe Rising Edge	T_{DSR}			20	ns	
Write Data Valid before DS↑	T_{WDB}			90	ns	
Write Data Hold time after DS↑	T_{WDA}	10			ns	
Memory Access Time	T_W		200		ns	

SECTION VII

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Read Setup time to $\overline{DS}\downarrow$	T_{RB}	110			ns	FIGURE 4
Read Hold time after $\overline{DS}\uparrow$	T_{RA}	110			ns	
Read Data Strobe Pulse Width	T_{RDS}	180			ns	
Read Data Setup time to $\overline{DS}\uparrow$	T_{RDB}	50			ns	
Read Data Hold time from $\overline{DS}\uparrow$	T_{RDA}	0			ns	
DMACLK$\uparrow$ to $\overline{DS}\downarrow$	T_{DDD}			100	ns	
DMACLK$\uparrow$ to $\overline{DS}\uparrow$	T_{DDA}			100	ns	
S0, S1, AND $\overline{STB}$ TIMING						
$\overline{STB}$ Width	T_{SW}	800			ns	FIGURE 7
S0, S1 Hold time after $\overline{STB}\uparrow$	T_{SD}	100			ns	
Data In Setup time to $\overline{STB}\uparrow$	T_{DIS}	700			ns	
Data In Hold time after $\overline{STB}\uparrow$	T_{DIH}	0			ns	
S0, S1 Setup time to $\overline{STB}\downarrow$	T_{SST1}	100			ns	
Aux Bus Setup time to $\overline{STB}\downarrow$	T_{SST2}	100			ns	
Aux Bus Hold time after $\overline{STB}\uparrow$	T_{SST3}			100	ns	
INPUT CLOCK TIMING (10 MHz Input)						
Clock Rise Time	T_{RT}			10	ns	FIGURE 2
Clock Fall Time	T_{RF}			10	ns	
Clock Cycle High Time	T_{CH}	40			ns	
Clock Cycle Low Time	T_{CL}	40			ns	
Clock Cycle Time	T_{CYC}	95	100	105	ns	
PRECOMPENSATION TIMING						
Early, Late Setup time (Before WDATA$\uparrow$)	T_{PB}	0			ns	FIGURE 9
Early, Late Hold Time (after WDATA$\downarrow$)	T_{PB}	50			ns	
FLOPPY INPUT DATA TIMING						
Window Setup time to RDCLK	T_{FRB}	50			ns	FIGURE 10
Window Hold time from $\overline{RDDATA}\uparrow$	T_{FRA}	50			ns	
HARD DISK INPUT DATA TIMING						
Data Setup time to RCLK$\downarrow$	T_{HRB}	60			ns	FIGURE 10
Data Hold time after RCLK$\downarrow$	T_{HRA}	10			ns	
Clock Setup time to RCLK$\uparrow$	T_{HCB}	60			ns	
Clock Hold time from RCLK$\uparrow$	T_{HCA}	10			ns	
ECCTIM TIMING						
$\overline{ECCTM}$ Setup to $\overline{DS}\downarrow$	T_{EDS}	50				FIGURE 10
$\overline{ECCTM}$ Hold after $\overline{DS}\uparrow$	T_{EDH}	100			ns	
RESET TIMING						
$\overline{RST}$ Pulse Width		1			µs	



SCHEMATIC 2: UDC/TAPE DRIVE INTERFACE CIRCUIT

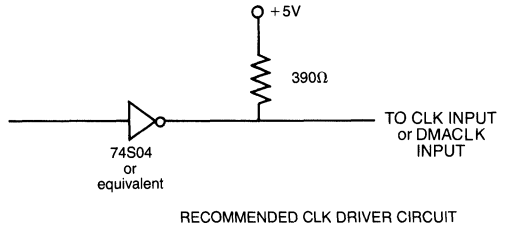


FIGURE 1: RECOMMENDED CLK/DMACLK INPUT

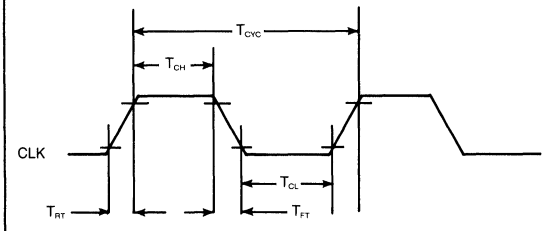


FIGURE 2: INPUT CLOCK TIMING (10MHz)

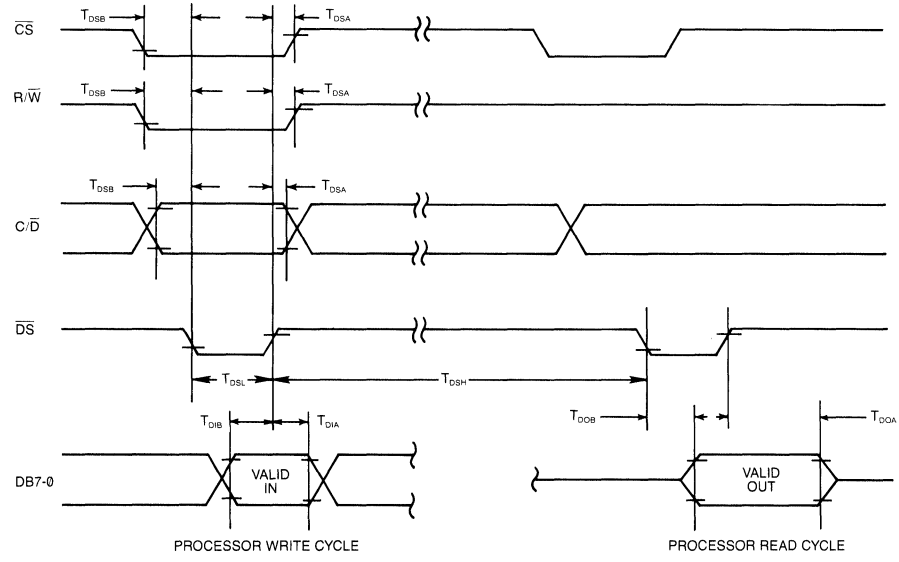


FIGURE 3: SYSTEM PROCESSOR TO UDC TIMING

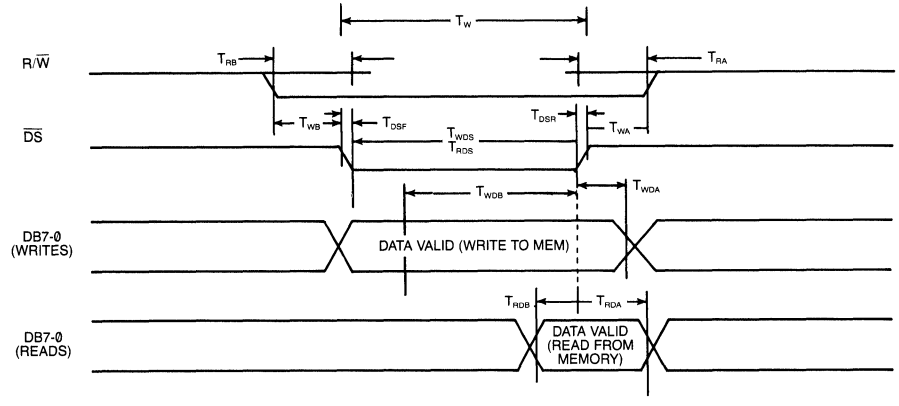


FIGURE 4: UDC TO MEMORY TIMING (BUS MASTER)

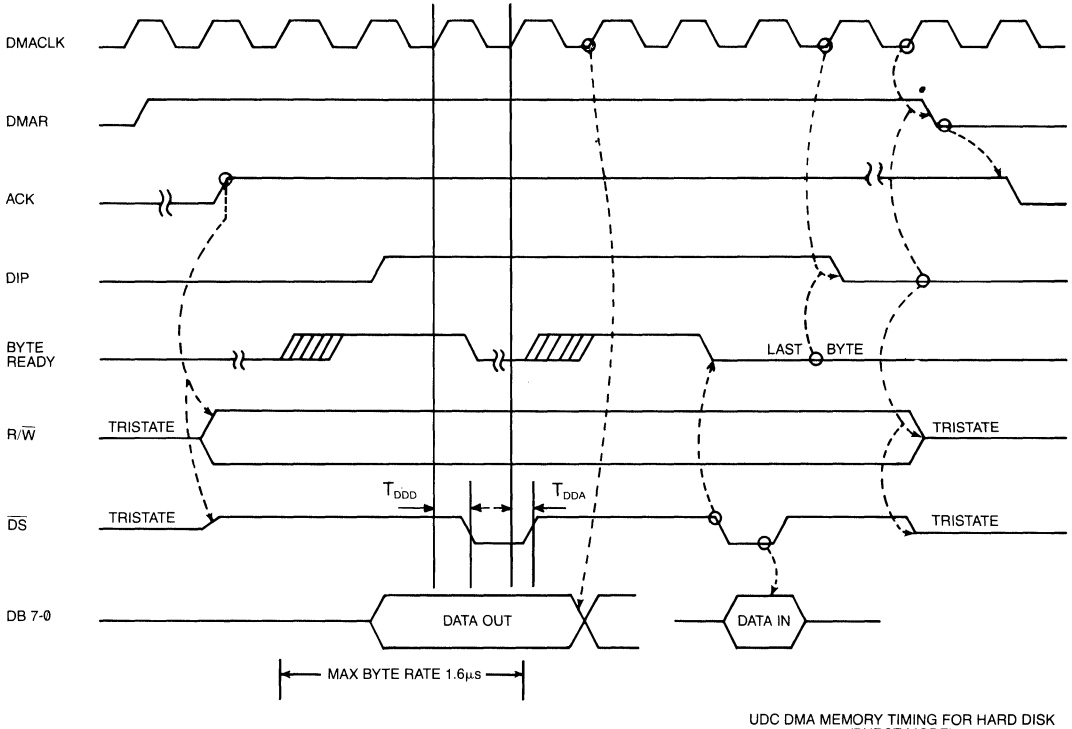


FIGURE 5: UDC DMA MEMORY TIMING FOR HARD DISK (BURST MODE)

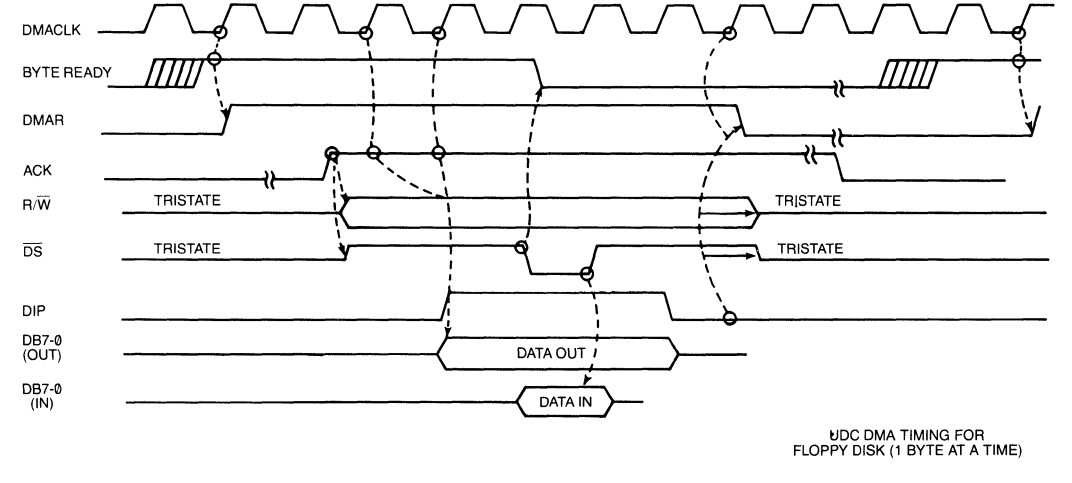


FIGURE 6: UDC DMA TIMING FOR FLOPPY DISK (1 BYTE AT A TIME)

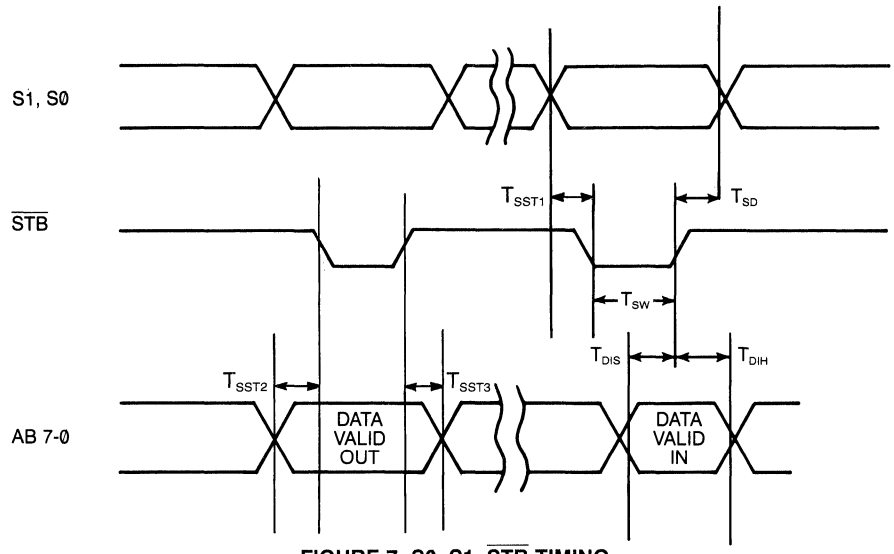


FIGURE 7: S0, S1, STB TIMING

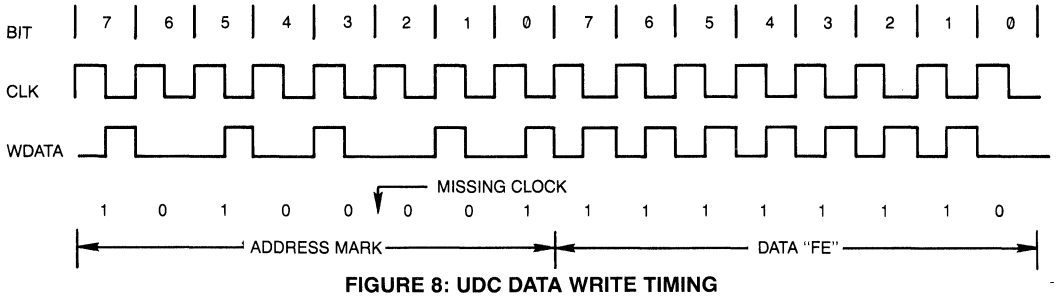
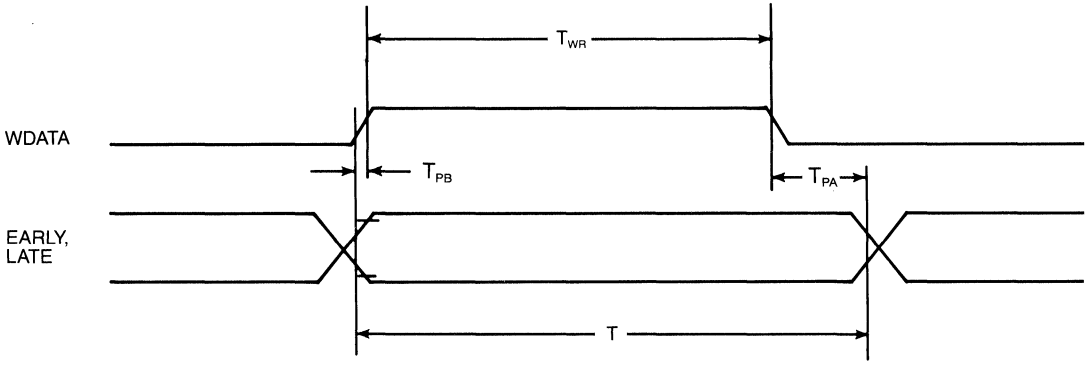
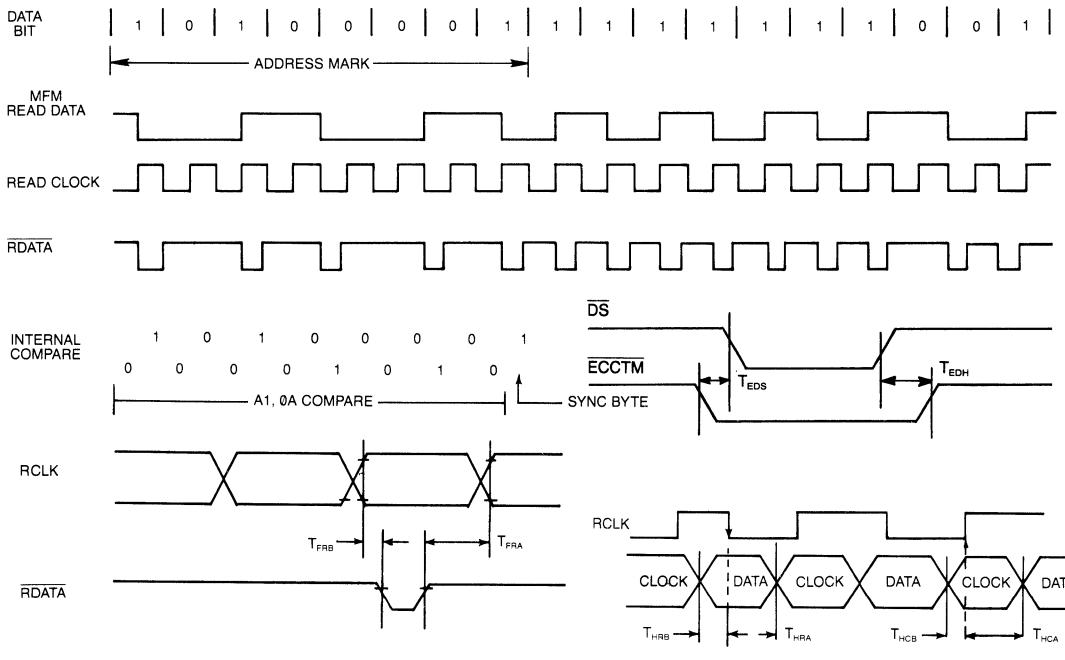


FIGURE 8: UDC DATA WRITE TIMING



DRIVE TYPE	T (typ)	T_{WR} (typ)
HARD DISK	200 NS	100 NS
8" MFM FLOPPY	2 µs	300 NS
8" FM FLOPPY	—	300 NS
5¼" MFM FLOPPY	4µs	300 NS
5¼" FM FLOPPY	—	300 NS

FIGURE 9: PRECOMPENSATION TIMING



FLOPPY INPUT DATA TIMING (HARD DISK BIT = 0)

HARD DISK INPUT DATA TIMING (HARD DISK BIT = 1)

FIGURE 10

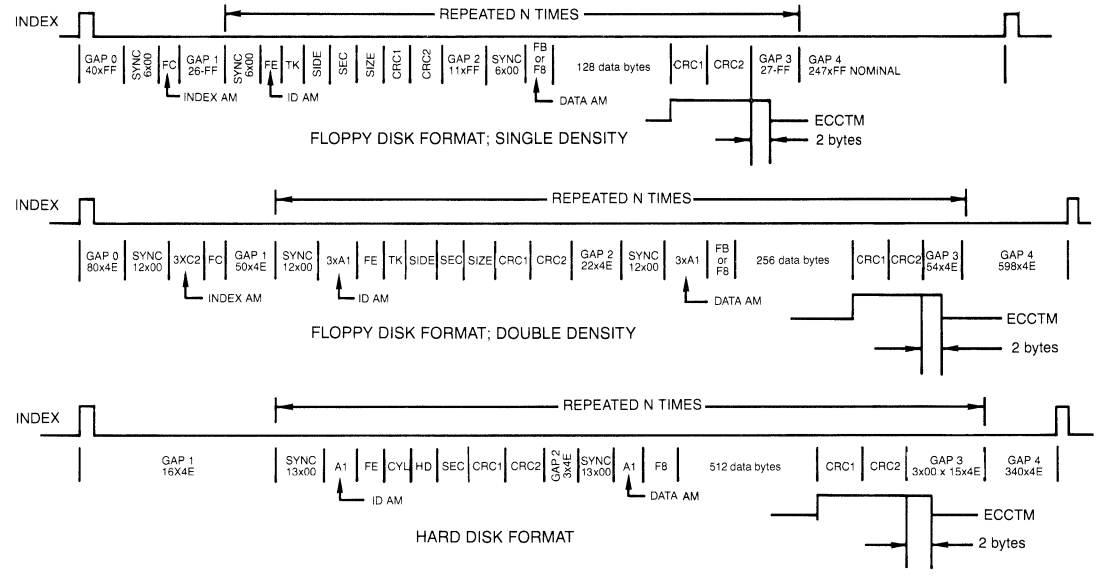


FIGURE 11: DISK FORMATS

SECTION VII

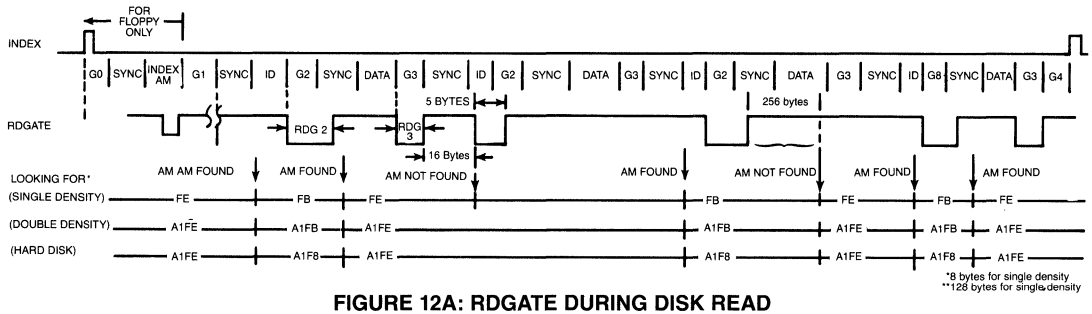


FIGURE 12A: RDGATE DURING DISK READ

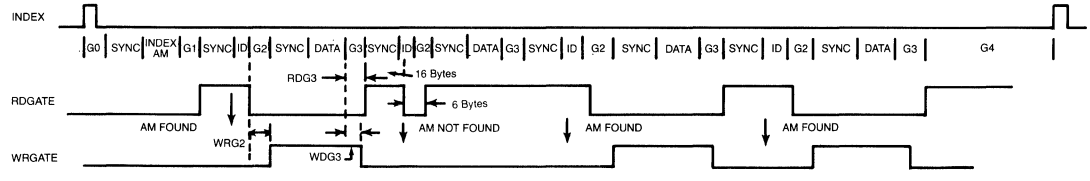


FIGURE 12B: RDGATE AND WRITE GATE TIMING

STANDARD FORMAT PARAMETERS			
PARAMETER	HARD DISK***	SINGLE DEN. FLOPPY	DOUBLE DEN. FLOPPY
GAP Ø *	16	40	80
GAP 1 *	16	26	50
GAP 2 *	3	11	22
GAP 3 *	18**	27	54
SYNC SIZE *	13	6	12
SECTOR COUNT *	user selectable	user selectable	user selectable
SECT. SIZE MULT *	user selectable	user selectable	user selectable
RDG 1	16	73	NA
RDG 2	6	13	24
RDG 3	25	27	24
WDG 2	5	11	23
WDG 3	3	11	3

* = PARAMETER USED BY FORMAT COMMAND
** = GAP 3 VARIES WITH SECTOR SIZE
*** = ALL VALUES APPLY TO 512 BYTES/SECTOR

TABLE 1: STANDARD FORMAT PARAMETERS

REGISTER BIT DEFINITIONS

	7	6	5	4	3	2	1	0
DMA 7-0 (REGISTER 0)	(MSB)			LOW ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 15-8 (REGISTER 1)	(MSB)			MIDDLE ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 23-16 (REGISTER 2)	(MSB)			HIGH ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)			DESIRED SECTOR NUMBER				(LSB)
DESIRED HEAD (REGISTER 4)	ALWAYS Ø		HIGH ORDER BITS OF DESIRED CYLINDER (MSB)		DESIRED HEAD NUMBER (MSB)			(LSB)
DESIRED CYLINDER (REGISTER 5)	(MSB)			LOW ORDER BITS OF DESIRED CYLINDER				(LSB)
SECTOR COUNT (REGISTER 6)	(MSB)			NUMBER OF SECTORS TO BE OPERATED ON BY COMMAND				(LSB)
RETRY COUNT (REGISTER 7)				RETRY COUNT (1'S COMPLEMENT)			PROGRAMMABLE OUTPUTS	
MODE (REGISTER 8)	HARD DISK		CRC/ECC ENABLE		SINGLE DENSITY	ALWAYS Ø	STEP RATE	SELECT
INTERRUPT/ COMMAND TERM. (REGISTER 9)	CRC PRESET 1 = Set to 1 0 = Set to Ø	ALWAYS Ø	INTERRUPT ON DONE		FLAG DELETED DATA MARK	USER DEFINED FLAG	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT
DATA/DELAY (REGISTER A)	(MSB)			HEAD LOAD DELAY MULTIPLE IS LOADED INTO THIS REGISTER DATA IS LOADED TO OR READ FROM THIS REGISTER				(LSB)
CURRENT HEAD (READ REGISTER 4)	BAD SECTOR FLAG		HIGH ORDER BITS OF CURRENT CYLINDER (MSB)		CURRENT HEAD NUMBER (MSB)			(LSB)
CURRENT CYLINDER (READ REGISTER 5)	(MSB)			LOW ORDER BITS OF CURRENT CYLINDER NUMBER				(LSB)
CHIP STATUS (READ REGISTER 8)	RETRY REQUIRED	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	DELETED DATA MARK READ	SYNC ERROR	COMPARE ERROR	PRESENT DRIVE SELECTED	
DRIVE STATUS (READ REGISTER 9)	ECC ERROR	INDEX	SEEK COMPLETE	TRACK ØØ	USER DEFINED ACTIVE	WRITE PROTECT ACTIVE	DRIVE READY	WRITE FAULT
INTERRUPT STATUS (COMMAND READ)	INTERRUPT PENDING	DMA REQUEST	DONE	COMMAND TERMINATION CODE		READY CHANGE	OVERRUN/ UNDERRUN	BAD SECTOR

TABLE 2: REGISTER BIT MAPS

UDC WRITE REGISTERS (APPLIES DURING TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BUTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT) (1)						(LSB)
DESIRED HEAD (REGISTER 4)	0	0	0	0	TRK # BIT 3	TRK # BIT 2	TRK # BIT 1	TRK # BIT 0
DESIRED CYLINDER (REGISTER 5)	ECC TYPE				ALWAYS 1	DATA BLOCK SIZE		
SECTOR COUNT (REGISTER 6)	TAPE MARK BLOCK SIZE (IN 2'S COMPLEMENT +1) (MODULO 256) (2)			OR	DATA BLOCK COUNT (IN 1'S COMPLEMENT) (3)			
RETRY COUNT (REGISTER 7)	1	1	1	1	USER DEFINED OUTPUTS			
MODE (REGISTER 8)	ALWAYS "Ø" FOR TAPE	CRC/ECC ENABLE CODE		SINGLE/ DOUBLE DENSITY	ALWAYS Ø	SYNC DELAY ENABLE	WRITE ENABLE	TAPE MARK ENABLE
INTERRUPT/ COMMAND TERMINATOR (REGISTER 9)	CRC PRESET	ALWAYS Ø	INTERRUPT ON DONE	ALWAYS 1	USER DEFINED	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT

NOTES: (1) The maximum search count is composed of:
130 byte inner loop (RDGATE high 128, 2 byte times)
times the number programmed (maximum of 33,150 byte times
(2) Tape mark operation
(3) Data block operation

TABLE 3: TAPE BACKUP REGISTER BIT MAPS

UDC READ REGISTERS (APPLIES TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BYTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT)						(LSB)
CURRENT HEAD (REGISTER 4)	X	X	X	X	X	X	X	X
CURRENT CYLINDER (REGISTER 5)	X	X	X	X	X	X	X	X
CHIP STATUS (REGISTER 8)	X	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	X	X	X	PRESENT DRIVE SELECTED	
DRIVE STATUS (REGISTER 9)	USER DEFINED	USER DEFINED	SEEK COMP	USER DEFINED	USER DEFINED	WRITE PROTECT	READY	WRITE FAULT
DATA (REGISTER A)	READ DATA							
INTERRUPT STATUS (COMMAND READ)	INT PENDING	DMA REG	DONE	COMMAND TERMINATION CODE (1)		READY CHANGE	OVER/ UNDER RUN	X

NOTES: (1) Command termination bits set to:
11 for data transfer error
10 for sync error
00 for successful termination
X Don't care

TABLE 4: TAPE BACKUP REGISTER BIT MAPS

COMMAND BIT DEFINITIONS

	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0
DESELECT DRIVES	0	0	0	0	0	0	0	1
RESTORE DRIVE	0	0	0	0	0	0	1	1 = Buffered Seek 0 = Normal Seek
STEP IN 1 CYLINDER	0	0	0	0	0	1	0	1 = Buffered Seek 0 = Normal Seek
STEP OUT 1 CYLINDER	0	0	0	0	0	1	1	1 = Buffered Seek 0 = Normal Seek
POLL DRIVES	0	0	0	1	1 = Poll Drive 3 0 = Don't Poll	1 = Poll Drive 2 0 = Don't Poll	1 = Poll Drive 1 0 = Don't Poll	1 = Poll Drive 0 0 = Don't Poll
SELECT DRIVE	0	0	1	1 = Head Load Delay Enabled 0 = Delay Disabled	TYPE OF DRIVE		DRIVE UNIT SELECTED	
SET REGISTER POINTER	0	1	0	0	REGISTER		NUMBER	
SEEK/READ ID	0	1	0	1	0	Step Enable	Wait For Complete	Verify ID
READ SECTORS PHYSICAL	0	1	0	1	1	0	0	Enable Transfer
READ TRACK	0	1	0	1	1	0	1	1 = Transfer All 0 = Transfer ID
READ SECTORS LOGICAL	0	1	0	1	1	1	1 = Bad Sector Bypass 0 = Bad Sector Terminate	Enable Transfer
FORMAT TRACK	0	1	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS PHYSICAL	1	1 = Bad Sector Bypass 0 = Bad Sector Termination	0	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS LOGICAL	1	1 = Bad Sector Bypass 0 = Bad Sector Terminate	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
TAPE BACKUP	0	0	0	0	1	WRITE:	PRECOMPENSATION VALUE	
						READ:	0 0	Transfer Enable

TABLE 5: COMMAND WORD BIT MAPS

SECTOR SIZE FIELD BITS

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	track number							
HEAD	side number							
SECTOR	sector number							
SECTOR SIZE							sector size (2 bits)	

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	cyl # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	hd # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							
SECTOR SIZE	ECC type				X		sector size (3 bits)	

DISK FORMATS

TABLE 6

For additional information, please consult the following:

Technical Note 6-2 (9224 Overview)
Technical Note 6-5 (Programmer's Reference Manual)
HDC 9225 Data Sheet
HDC 9226 Data Sheet
HDC 9224 Programmer's Quick Reference Card

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

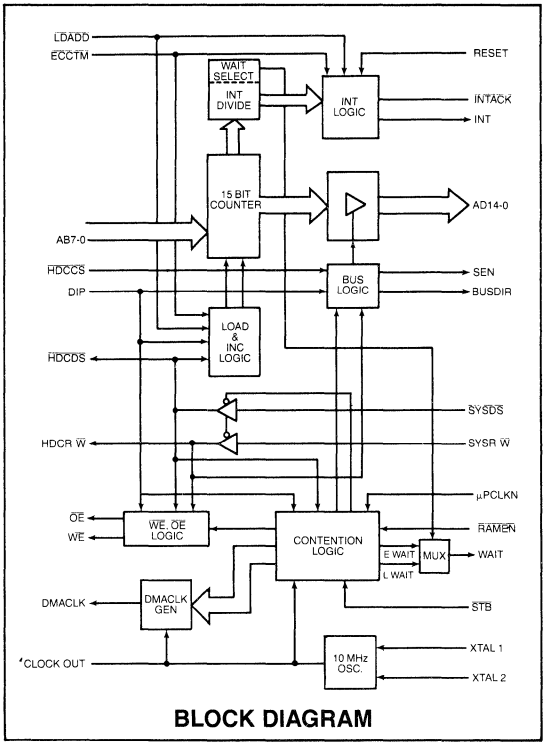
STANDARD MICROSYSTEMS CORPORATION

HDC 9225

DISK BUFFER MANAGEMENT UNIT "DBMU"

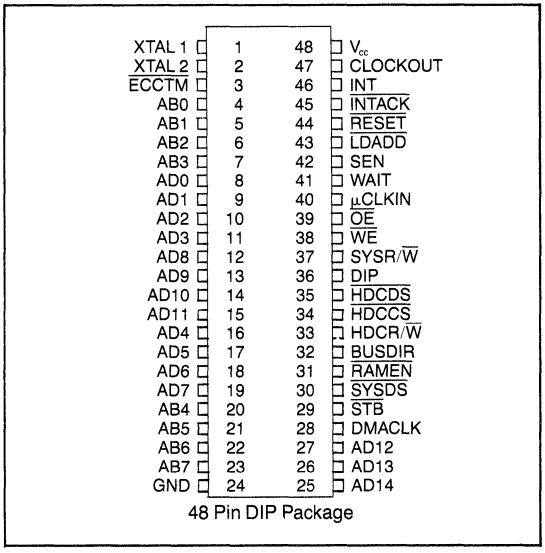
FEATURES

- ☐ Significantly reduces chip count in hard disc systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Creates a dual-port disk buffer (up to 32K in size) using low cost static ram
- ☐ Programmable sector interrupt counter allows host processor rapid access to data
- ☐ On board 10 MHz oscillator simplifies clock generation
- ☐ Allows disk interleave factor of 1, improving system performance
- ☐ Fabricated in low power CMOS; fully TTL compatible



BLOCK DIAGRAM

PIN CONFIGURATION



48 Pin DIP Package

GENERAL DESCRIPTION

The HDC 9225 Disk Buffer Management Unit (DBMU) is a 48 pin CMOS/LSI device which, when used with the HDC 9224 Universal Disk Controller, significantly reduces the total number of chips required to build a hard and floppy disk controller.

The DBMU allows low cost static rams to be used in a dual-ported configuration. This allows both the system processor and the HDC 9224 Universal Disk Controller to share a common disk buffer local memory area, while eliminating system memory contention problems. This feature greatly improves overall system performance, while simplifying design.

SECTION VII

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

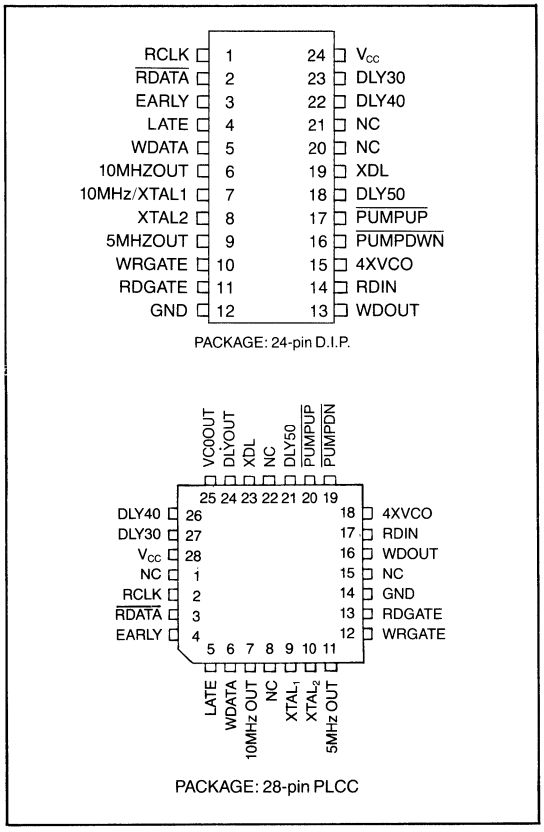
HDC 92C26
PRELIMINARY

HIGH PERFORMANCE HARD DISK DATA SEPARATOR "HDDS"

FEATURES

- ☐ Significantly reduces component count in hard disk systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- ☐ Built-in write precompensation logic
- ☐ Eliminates costly critical "tune up" adjustments
- ☐ Space saving 24 pin package saves board space and reduces critical layout problems.
- ☐ Printed Circuit Board Artwork available to facilitate prototyping and evaluation

PIN CONFIGURATION



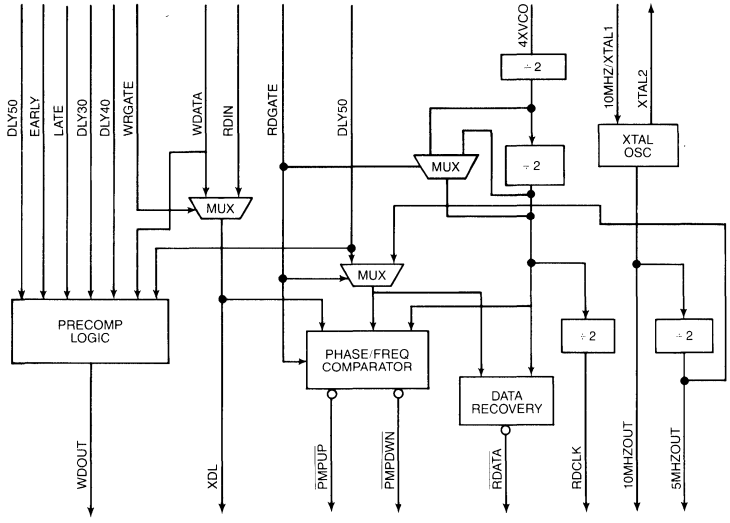
GENERAL DESCRIPTION

The HDC 92C26 Hard Disk Data Separator (HDDS) is a 24 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of a high performance hard disk data separator.

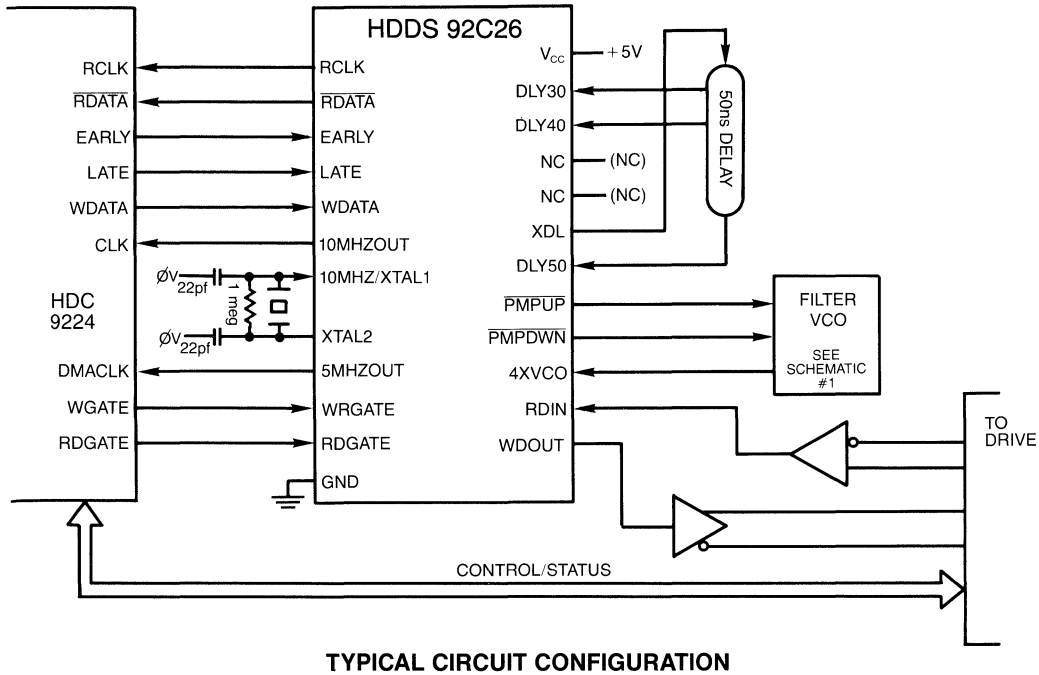
The HDC 92C26, combined with a few discrete components, form a phase locked loop which performs phase and frequency locking onto either the FM or MFM data stream output by ST506/ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 92C26 simplifies the task of the designer.

SECTION VII



HDC 92C26
BLOCK DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

DESCRIPTION OF PIN FUNCTIONS

PIN. NO.	NAME	SYMBOL	DESCRIPTION
1	Read Clock	RCLK	Read clock output with nominal frequency of 5 MHz which defines the half bit boundaries of the $\overline{\text{RDATA}}$ output.
2	Read Data	$\overline{\text{RDATA}}$	This output is the regenerated raw read data from the drive. This signal conforms to all timing requirements of the UDC.
3	Early	EARLY	This input is connected to the HDC 9224, and causes the HDDS to send out the write data early.
4	Late	LATE	This input is connected to the HDC 9224, and causes the HDDS to send out the write data late.
5	Write Data	WDATA	This input is connected to the HDC 9224, and is the MFM encoded write data signal. This signal is passed through the HDDS and is delayed according to the write precompensation inputs EARLY and LATE.
6	10 Mhz Out	10MHZOUT	This output is normally connected to the CLK input on the HDC 9224.
7, 8	Crystal 1, 2	XTAL 1,2	A 10 Mhz crystal may be connected between these two inputs. If a TTL signal is used in place of a crystal, the TTL signal (with pullup) should be connected to the XTAL 1 and the XTAL 2 input should be left open.
9	5 Mhz Out	5MHZOUT	This output is normally tied to the HDC 9224 DMACLK pin in systems that do not use the HDC 9225 Disk Buffer Management Unit.
10	Write Gate	WRGATE	This input is connected to the WRGATE output of the HDC 9224. When low the RDIN input is selected and is output to the delay line via the XDL pin. When in write mode (WRGATE active), the WDATA input is selected and output to the delay line via the XDL pin for precompensation.
11	Read Gate	RDGATE	This input signal, when active, allows the external VCO to begin locking on the incoming data from the drive. When this signal is inactive, the VCO will lock on to the 5 MHz output signal.
12	Ground	GND	This is the ground pin for the device
13	Write Data Out	WDOUT	This output is the precompensated version of the WDATA input. This output is normally connected to the write data signal of the hard disk drive.
14	Read Data In	RDIN	This input is normally connected to the Disk Data output of the drive. The leading edge of this input arms the internal phase comparator, and then also asserts the $\overline{\text{PMPUP}}$ output 50 ns later.
15	4 Times VCO	4XVCO	This input is connected to the external VCO and runs at a frequency of 4 times the data rate with RDGATE asserted. This signal is internally divided by 2 and feeds the phase comparator to generate the $\overline{\text{PMPDN}}$ signal. 4XVCO is also divided by four and output as the RCLK signal.
16	Pump Down	$\overline{\text{PMPDN}}$	When active (low) this output will decrease the frequency of the VCO.
17	Pump Up	$\overline{\text{PMPUP}}$	When active (low) this output will increase the frequency of the VCO.
18	Delay 50 ns	DLY50	This is the 50 ns delay of the XDL signal. The 50 ns tap is used to arm the phase detector and create a reclocked version of the raw read data from the drive.
19	Excite Delay Line	XDL	During write operations, when WRGATE is active, this output is identical to WDATA, and is output to the delay line, creating precise delays which are used to perform write precompensation. When WRGATE is inactive, this output is the image of the raw read data the RDIN input. XDL is output to the delay line and is used to provide proper arming for the phase comparator and clocking for the data recovery circuitry.
20, 21	No Connect	NC	No connection should be made to these pins.
22 23	Delay 40 Delay 30	DLY40 DLY30	These inputs are delays of 30 and 40 ns of the XDL signal, and come from the external delay line. These signals are used for the nominal, late and early positioning of the databits in the WDOUT data stream.
24	V_{CC}	V_{CC}	+5V supply connected to this pin.

DESCRIPTION OF OPERATION

DATA SEPARATION

The HDC 92C26, in conjunction with an external VCO, tapped delay line and filter, allows the system designer to implement a high performance phase locked loop circuit to perform phase and frequency locking onto either an MFM or FM encoded data stream (from an ST-506 style disk drive.)

In most applications, the data on the hard disk is recorded in double density (MFM). In MFM mode, an input pulse on RDIN indicates not a 1 or 0 but rather a flux transition on the media and (by definition) these flux transitions may be spaced at T, 1.5T or 2T time intervals, where T equals the inverse of the bit data rate. For the standard ST-506 drive, these time intervals are 200 ns, 300 ns, and 400 ns.

Due to the nature of magnetic storage phenomena, the bit spacing found on the hard disk is not constant, but instead will modulate due to magnetic effects and drive rotational speed variations. The HDC 92C26 compensates for these shifts in the RDIN signal coming from the drive and regenerates $\overline{\text{RDATA}}$ and RCLK.

The RCLK signal is derived from the VCO which changes its period as a function of the variations in the raw disk data and permits the data from the drive to be correctly clocked into the HDC 9224 Universal Disk Controller, independent of the bit spacing variations found in the raw data coming from the drive.

The VCO normally runs at 20 Mhz. Since the half bit time (for data from the disk) is 100 ns, the HDC 92C26 divides the 4XVCO signal in half and compares the phase and frequency of the VCO with the incoming data. The read data signal is regenerated by the HDC 9266 and is placed correctly within the RCLK window so as to satisfy the input timing requirements of the HDC 9224 Universal Disk Controller.

WRITE PRECOMPENSATION GENERATOR

The HDC 92C26 also performs write precompensation which is needed because of tendency of written data to "re-align" itself on the magnetic media.

Certain bit patterns, when written, and later read back, will cause a phenomena known as "peak" or "bit" shift. Since this shifting is predictable, it is common when writing to magnetic media to intentionally pre-shift when these bits are to be written. This intentional "pre-shifting" minimizes the amount of shifting which occurs when the data is read back, and facilitates proper data recovery.

The HDC 9224 recognizes those patterns which require "pre-shifting" or precompensation, and outputs EARLY and LATE signals to alert the HDC 92C26 to the need for precompensation.

Typical ST-506 applications may require "pre-shifting" the data bits by approximately 10 ns (either early or late). Three taps of the delay line (DLY30, DLY40, DLY50) are normally used to implement precompensation. The HDC 92C26 then outputs the precompensated data via the WDOUT pin.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec) ..... +325 C
Maximum V_{CC} ..... +7.0 V
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} + 0.3 V
Negative Voltage on any Pin, with respect to Ground ..... −0.3 V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, V_{CC} = 5.0V, ± 5%)

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT				
I_{CC}		30	mA	
OUTPUT VOLTAGE				
V_{OH} (1)	2.4		V	I_{OH} = 400 uA
V_{OH} (2)	4.3		V	I_{OH} = 400 uA
V_{OL}		0.4	V	I_{OL} = 2.0 mA
INPUT VOLTAGE				
V_{IH} (3)	2.0		V	
V_{IL} (3)		0.8	V	
V_{IH} (4)	3.5		V	
V_{IL} (4)		1.5	V	
INPUT CURRENT				
I_{IH}		10	uA	V_{IH} = 2.0V
I_{IL}		2.0	mA	V_{IL} = 0.4V

Notes:
(1) For all outputs except 10MHzOUT and 5MHzOUT
(2) For 10MHzOUT and 5MHzOUT
(3) For all inputs except XTAL 1 and 4XVCO
(4) For XTAL1 and 4XVCO

AC ELECTRICAL CHARACTERISTICS (TA = 0 C to +70 C, V_{CC} = 5.0V, ± 5%)

Symbol	Min.	Typ.	Max.	Unit	Comments
T_1			70	ns	figure 1
T_2			80	ns	figure 1
T_3	60			ns	figure 2
T_4	10			ns	figure 2
T_5	60			ns	figure 2
T_6	10			ns	figure 2
T_7			65	ns	figure 3
T_8			65	ns	figure 3
T_9			65	ns	figure 3
T_{10}			65	ns	figure 3
T_{11}	45	50	55	ns	figure 4
T_{12}		50		ns	figure 5
T_{13}		50		ns	figure 6
T_{14}	6			ns	figure 7
T_{15}	50			ns	figure 7

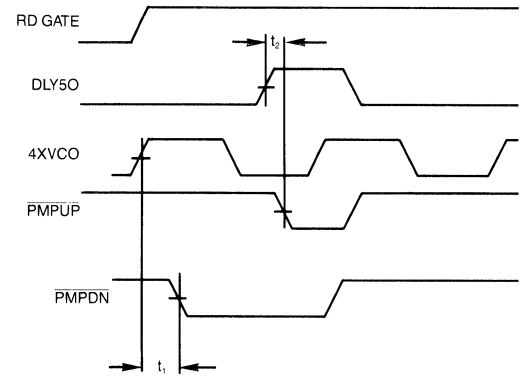


FIGURE 1

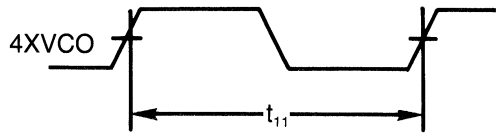


FIGURE 4

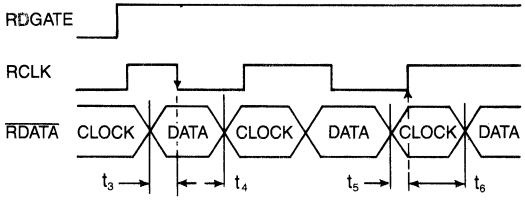


FIGURE 2

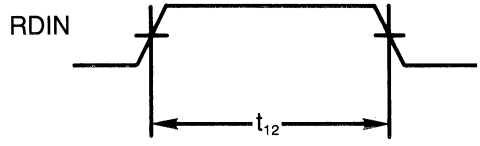


FIGURE 5

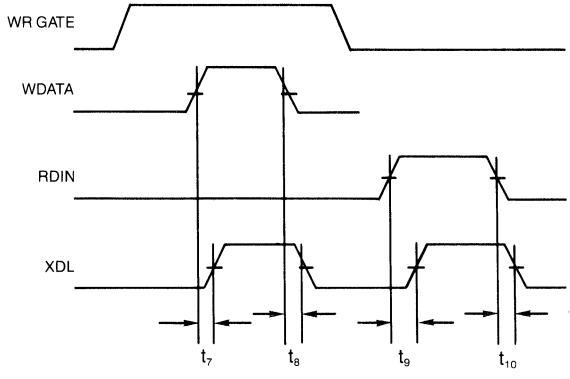


FIGURE 3

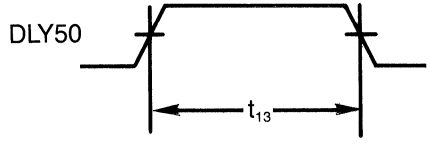


FIGURE 6

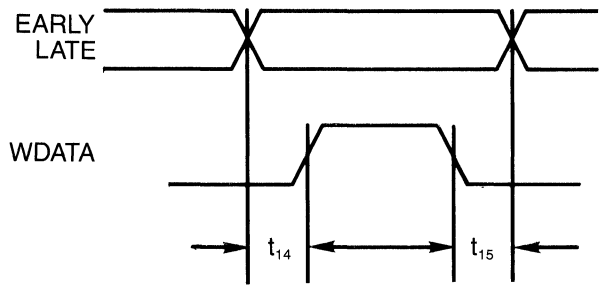
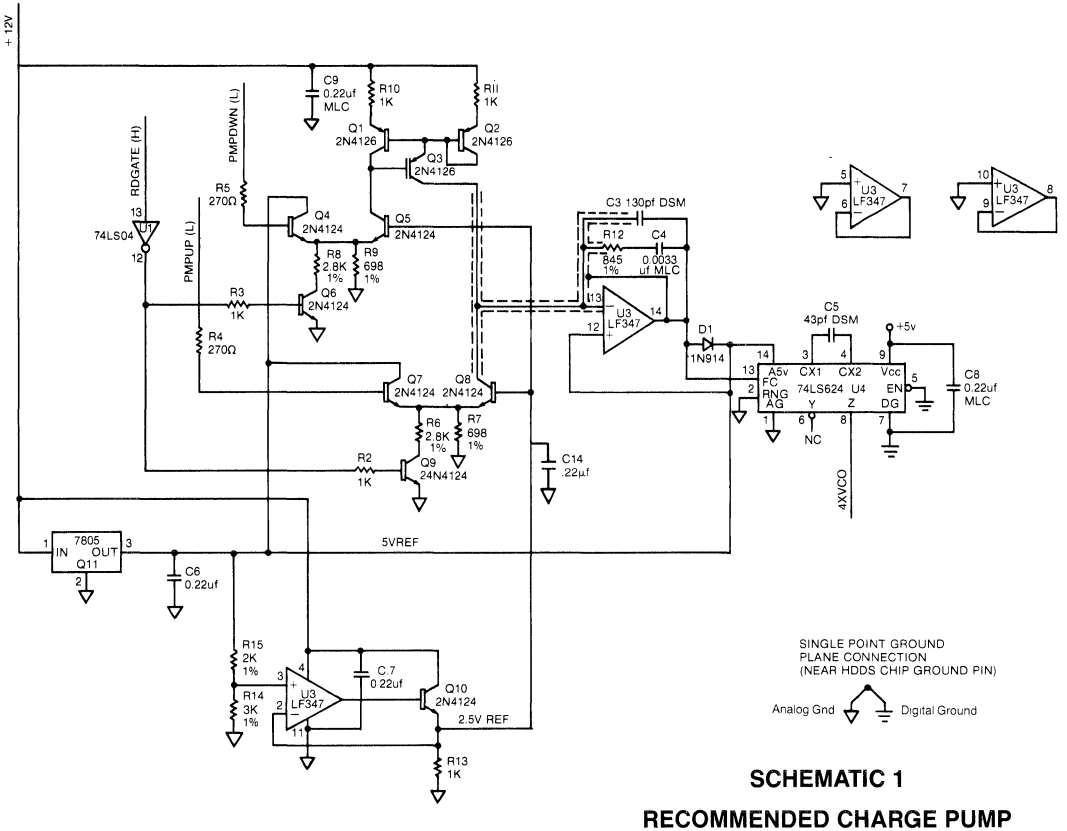


FIGURE 7

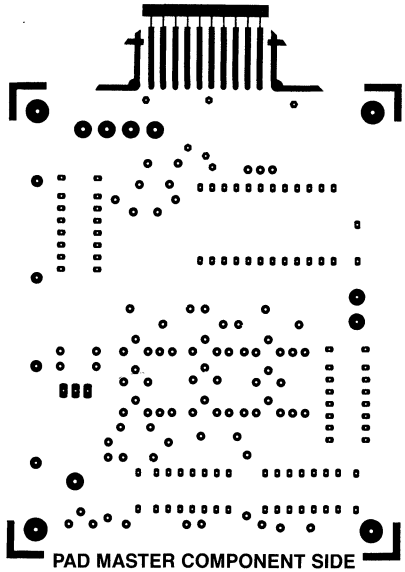


SCHEMATIC 1

RECOMMENDED CHARGE PUMP LOOP FILTER AND VCO

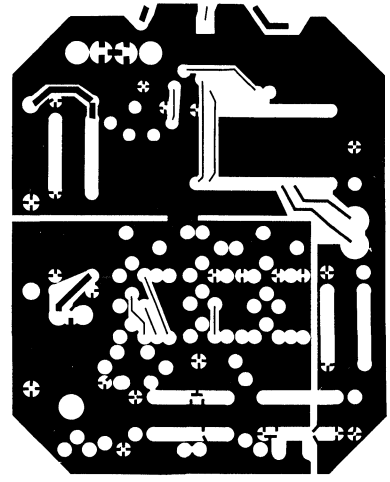
SECTION VII

PC 1



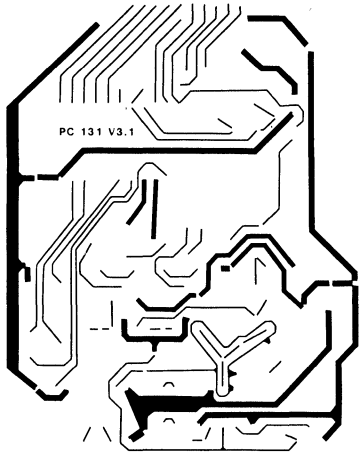
PAD MASTER COMPONENT SIDE

PC 2



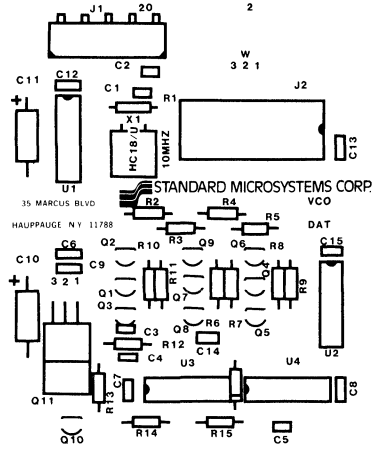
COMPONENT SIDE

PC 3



CIRCUIT SIDE

PC 4



SILK SCREEN

NOTE: The printed circuit board artwork shown above is included for illustration only. Camera ready artwork is available at no charge. Contact your SMC representative or regional sales office, and ask for Technical Note TN 6-4.

Blank PC boards (based on the illustrations above) are also available to facilitate evaluation and design. Contact your SMC representative or regional sales office for more information.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

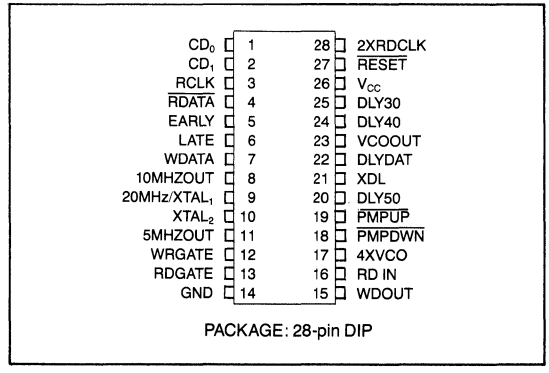
HDC 9227
PRELIMINARY

High Performance Dual (Hard/Floppy Disk) Data Separator DDS

FEATURES

- ☐ Single chip combines high performance analog hard disk data separator and high resolution digital floppy disk data separator
- ☐ Significantly reduces component count in hard disk and floppy systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Eliminates all tuning and tweaking normally required by analog data separators
- ☐ Built-in hard disk write precompensation logic
- ☐ Fabricated in CMOS technology
- ☐ Single +5V supply
- ☐ TTL Compatible

PIN CONFIGURATION



PACKAGE: 28-pin DIP

SECTION VII

GENERAL DESCRIPTION

The HDC 9227 Universal Disk Data Separator (UDDS) is a 28 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of the hard disk/floppy disk sub-system.

Internally, a precision floppy disk digital data separator is combined with the digital portion of a high performance, self tuning analog hard disk data separator.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9227 simplifies the task of the system designer.

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8888

STANDARD MICROSYSTEMS CORPORATION

HDC 9234
PRELIMINARY

Universal Disk Controller

FEATURES

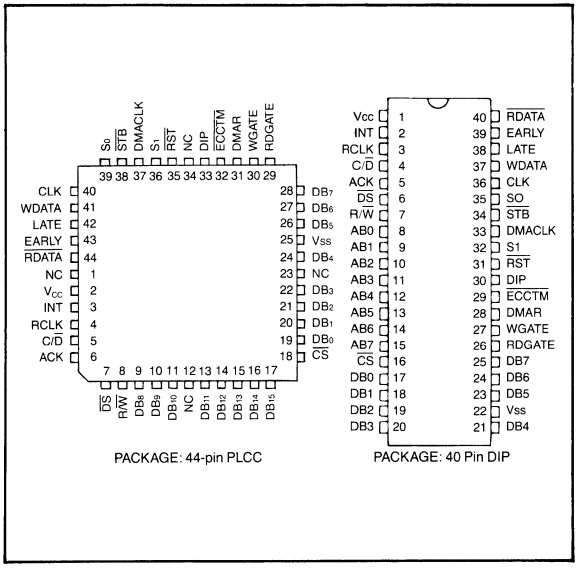
Programmable Disk Drive Interface and Formats

- ☐ IBM® PC-AT® ST506/412 or user definable hard disk formats
- ☐ IBM® PC-AT® compatible ECC algorithm
- ☐ IBM Compatible Single or Double Density Floppy Disk Formats
- ☐ Controls 8″, 5.25″, and 3.5″ drives
- ☐ Controls tape drives for tape backup of disks
- ☐ Full CRC generation and checking
- ☐ Internal or External Error detection
- ☐ Programmable user-transparent Error correction
- ☐ Programmable automatic retry option
- ☐ Programmable internal write precompensation logic
- ☐ Read/Write commands with automatic seek
- ☐ Multiple sector read/write transfers
- ☐ Sector interleave capability
- ☐ Internal address mark generation and detection
- ☐ Programmable track step rates
- ☐ Supports both buffered and unbuffered seeks
- ☐ Polling command allows overlapping seeks
- ☐ Powerful, high level command set
- ☐ Controls up to 4 drives with
  - ☐ up to 16 heads per drive
  - ☐ up to 2048 cylinders per drive
  - ☐ up to 256 sectors per track

Flexible System Interface

- ☐ Built-in DMA controller capable of addressing up to 16 MBytes
- ☐ Supports either private or virtual buffer memory addressing schemes
- ☐ User readable Interrupt, Chip Status, and Drive Status registers
- ☐ Programmable Interrupt Mask
- ☐ TTL compatible
- ☐ Standard 40 pin DIP package
- ☐ Single +5 volt supply

PIN CONFIGURATION



SECTION VII

GENERAL DESCRIPTION

The HDC 9234 Universal Disk Controller (UDC) is a 40 pin, n-channel MOS/LSI device capable of interfacing up to 4 Winchester-type hard disks and/or industry standard floppy disks to a processor. The chip is programmable to support IBM® PC-AT® ST506/412 and user defined hard disk formats, as well as IBM compatible 8″, 5.25″ and 3.5″ single and double density formats.

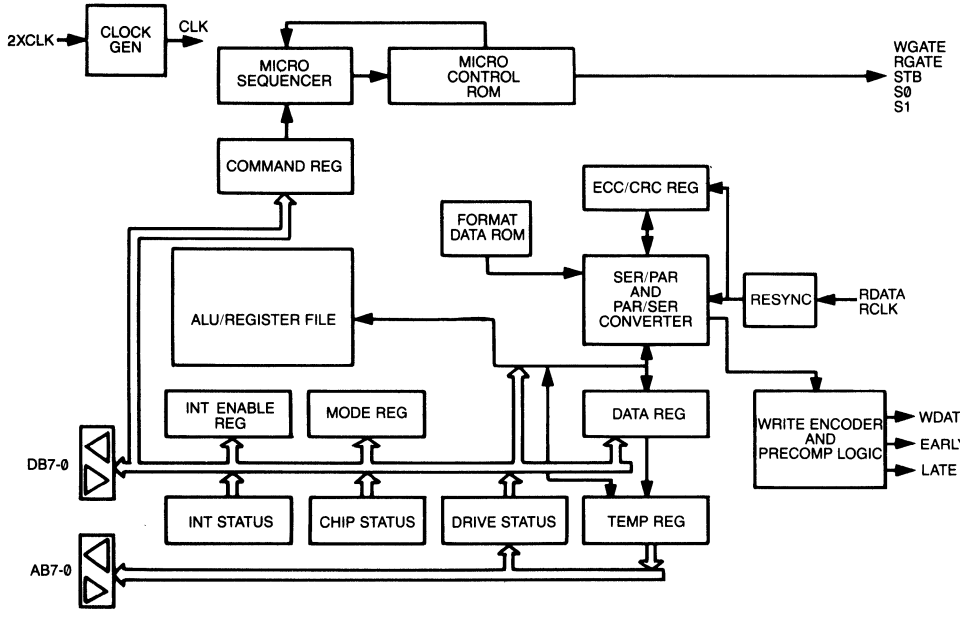
A powerful and sophisticated command set reduces the software overhead required to implement a combined hard disk/floppy disk controller. These commands include:

Drive Select	Seek to cylinder and read ID
Step out 1 cylinder	Step in 1 cylinder
Restore Drive	Read Logical Sectors
Read Physical Sectors	Read Entire Track
Write Logical Sectors	Write Physical Sectors
Chip Reset	Deselect Drive
Poll Drives for Ready	Set Register Pointer
Tape Back-up	Format current track

The HDC 9234 can use both private memory or shared memory buffers with the chip's internal DMA controller providing up to 24 bit addresses over an 8 bit data bus. This enables the HDC 9234 to address up to 16 megabytes of memory, and allows the hardware designer tremendous flexibility in system design.

Several techniques of error detection and correction are implemented on the HDC 9234. One user selected method allows the chip to detect and transparently correct a read error in the data-stream, without external logic. Another technique allows the designer complete control over the ECC algorithm, by using external logic or system software to detect and correct the error. As a further aid in error handling, the HDC 9234 allows the user to specify the number of read retries to be attempted before an error is reported to the host processor by the HDC 9234.

The HDC 9234 features a versatile track format command which allows formatting with interleaved sectors. The chip needs only 4 or 5 bytes of external memory space per sector (depending on format selected). This feature allows the designer to optimize sector interleaving for optimum throughput.



BLOCK DIAGRAM OF DATA PATH IN HDC 9234

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Power	V_{CC}	+5 volt power supply pin
22	Ground	V_{SS}	System ground
16	Chip Select	$\overline{CS}$	This signal (when active) selects the HDC 9234 for communications with the host processor. This signal is normally derived by decoding the high order address bits. It is active low.
17,18 19,20 21,23 24,25	Data Bus 7-0	DB7-0	All system processor reads and writes, (including status reads, initialization, disk parameters, and commands) are 8 bit transfers which utilize these lines. When the UDC is accessing memory, data is input or output on these lines. Data on these lines is valid only when DATA STROBE ($\overline{DS}$) is active low.
8-15	Aux Bus 7-0	AB7-0	These 8 pins are used to output drive control signals and DMA Address information. Additionally, these pins are used to input drive status information.
4	Command/$\overline{Data}$	C/$\overline{D}$	During processor to UDC communications, this input is used to indicate whether a command or data transfer will follow. If this pin is low, data may be written to, or read from, the internal data registers. If this pin is high, the processor may write commands or read command results from the UDC.
7	Read/$\overline{Write}$	R/$\overline{W}$	When the processor is communicating to the UDC, a high on this input line indicates a (processor) request for a UDC read operation, and a low indicates a (processor) request for a write operation. R/$\overline{W}$ C/$\overline{D}$ Operation 0 0 Write to register file 0 1 Write to command reg. 1 0 Read from register file 1 1 Read Interrupt Status Register During UDC initiated operations, this pin becomes an output, and is used to indicate a read operation (logic 1) or write operation (logic 0) to external memories.

PIN NO.	NAME	SYMBOL	DESCRIPTION
6	Data Strobe	$\overline{DS}$	This active low pin functions as both an input and output. When the processor is writing to the UDC, the trailing edge of an active (low) signal applied to this pin indicates that the data on DB7-0 is valid, and the data is latched into the appropriate UDC register on the rising edge. When the processor is reading from the UDC, the trailing edge of an active (low) signal applied to this pin is used to clock out the desired UDC register on to DB7-0. During UDC initiated DMA operations, the UDC drives this pin low to either read or write data from memory. On DMA read cycles, data is clocked in on the trailing edge. On DMA write operations, the data on DB7-0 is valid anytime this pin is active (low). When this pin is high (logic 1), DB7-0 return to a high impedance state.
2	Interrupt	INT	This active high output is used by the UDC whenever it wants to interrupt the processor. The interrupt pin is reset to its inactive (low) state when the UDC interrupt status register is read.
30	DMA In Progress	DIP	This active high output becomes active whenever the UDC is actually performing a DMA operation.
28	DMA Request	DMAR	This active high output becomes active whenever the UDC requires the system bus to perform a memory cycle, and ACK is inactive. During hard disk operations, it remains active until the sector transfer is complete. During floppy disk operations, it is active for 1 byte transfer time. The UDC shows that it has released the system bus by resetting this signal to its inactive (low) state.
5	Acknowledge	ACK	This active high signal from the processor tells the UDC that the processor has released the system bus and the UDC may access system memory.
37	Write Data	WDATA	This pin is used to output serial data from the UDC to the drive, in either FM or MFM format. In both cases, data is output with the most significant bit first.
38	Late	LATE	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written late.
39	Early	EARLY	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written early.
27	Write Gate	WGATE	This output (when active high) indicates the drive should allow a write operation.
40	Read Data	$\overline{RDATA}$	This input pin contains the serial bit stream read from the drive, in either FM or MFM format. Media flux reversals are indicated by a negative transition.
3	Read Clock	RCLK	This input is generated by the external data separator. Its frequency should self-adjust to the variations in bit width in the data stream from the drive. This clock supplies a window to indicate half-bit-cell boundaries.
26	Read Gate	RDGATE	This output pin is used to enable the external data separator, compensate for write to read recovery time of the drive, and filter out the write splice in gaps 2 and 3. The timing of this signal is dependent upon the type of drive (hard or floppy) being used. RDGATE is inactive at all times except when the UDC is actually performing a read operation or an internal ECC operation.
29	ECC Time	$\overline{ECCTM}$	When the UDC is used in external ECC mode, this output pin becomes active (low) during the time the UDC is reading the ECC bytes from memory or external ECC chip, when executing a WRITE command. It is also active during internal ECC correction operations, and for either one (write) or two (read) byte times after DIP (pin 30) becomes inactive following a sector transfer. This shows the system processor when it should service the UDC buffer.
32,35	Select 1,0	S1,S0	These active high outputs are used by external logic to select either the source or destination for data transfers occuring via AB7-0. The following table defines the specific transfer being called for by the UDC. (Note that S1-0 are valid only when $\overline{STB}$ is active low.)

$\overline{STB}$	S1	S0	AB7-0 Activity
1	X	X	S1,S0 Invalid
0	0	0	UDC inputs Drive Status Signals
0	0	1	UDC outputs DMA address bytes
0	1	0	UDC outputs OUTPUT 1 signals
0	1	1	UDC outputs OUTPUT 2 signals

PIN NO.	NAME	SYMBOL	DESCRIPTION
34	Strobe	STB	This active low output indicates when the host processor should read or write to AB7-0, as indicated by S1-0. When AB7-0 are used as outputs from the UDC, data is valid anytime this signal is active (low). When AB7-0 are used as inputs to the UDC, data is clocked in on the rising edge of this signal.
36	DEVICE CLOCK	CLK	This input is the double frequency clock used by the UDC for all internal timing operations. Eight inch hard disk drives (with a nominal bit time of 230 ns) require an input of 8.696 MHz (115 ns period). 5.25" hard disks (with a nominal bit time of 200 ns) require a 10 MHz input (100 ns period). Eight inch, 5.25" and 3.5" floppy drives all require a 10 MHz clock, which is internally prescaled by the UDC to the correct frequency, as determined from the Drive Select command and MODE register. This input requires an external pull-up resistor, as it is not TTL-level compatible. See figure 2.
31	Reset	RST	This active low input will force the UDC into the following known state: INT–Inactive low WDATA–Inactive low ECCTM–Inactive high DMAR–Inactive low EARLY–Inactive low C/D–Input AB7-0–Input LATE–Inactive low R/W–Input DB7-0–Input WGATE–Inactive low DIP–Inactive low RDGATE–Inactive low DS–Input An active low on this pin has the same effect as a RESET Command.
33	DMA Clock	DMACLK	All UDC DMA operations will be synchronized to this clock input. Three DMACLK periods are required for each DMA byte transfer.

OVERVIEW OF UDC REGISTERS

The HDC 9234 has three types of internal, processor addressable registers; Read/Write, Read Only, and Write Only. These registers are addressed by an internal register pointer that is set by the SET REGISTER POINTER command.

All register data is passed to and from the UDC via the data bus (DB7-0).

The internal register pointer is automatically incremented with each register access until it points to the DATA Register. This insures that all subsequent register accesses will address the DATA register.

PROCESSOR ACESSIBLE REGISTERS

REGISTER ADDR	WRITE	READ
0	DMA7-0	DMA7-0
1	DMA15-8	DMA15-8
2	DMA23-16	DMA23-16
3	Desired Sector	Desired Sector
4	Desired Head	Current Head
5	Desired Cylinder	Current Cylinder
6	Sector Count	Temporary Storage
7	Retry Count	Temporary Storage
8	Mode	Chip Status
9	Interrupt/Command Terminator	Drive Status
A	Data/Delay	Data
COMMAND	Current Command	Interrupt Status

Three internal registers (OUTPUT 1, OUTPUT 2, and INPUT DRIVE STATUS) which are not directly addressable by the processor are accessed by the UDC. The information contained in these registers is used in disk interfacing and is input or output on UDC Pins AB7-0. The following table describes these registers and the signals they output or input on AB7-0.

UDC ADDRESSABLE REGISTERS

DRIVE STATUS REGISTER (input)	Select Pins S1 = 0, S0 = 0
AB6—Index Pulse	AB4—Track 00
AB5—Seek Complete	AB3—User Defined
AB1—Drive Ready	AB7—ECC Error
AB0—Write Fault	AB2—Write Protect

OUTPUT 1 (Output)	Select Pins S1 = 1, S0 = 0
AB7—Drive Select 3	AB6—Drive Select 2
AB5—Drive Select 1	AB4—Drive Select 0
AB3—Programmable Outputs (see text)	AB2—Programmable Outputs
AB1—Programmable Outputs	AB0—Programmable Outputs

OUTPUT 2 (Output)	Select Pins S1 = 1, S0 = 0
AB7—Drive Select 3	AB6—Reduce Write Current
AB5—Step Direction	AB4—Step Pulse
AB3—Desired Head (Bit 3)	AB2—Desired Head (Bit 2)
AB1—Desired Head (Bit 1)	AB0—Desired Head (Bit 0)

Additionally, several registers (DMA7-0, DMA15-8, DMA23-16, DESIRED SECTOR, DESIRED CYLINDER, SECTOR COUNT, and RETRY COUNT) serve an alternate purpose. These registers are used by the FORMAT TRACK command to hold parameters. This alternate register utilization is described in detail under the FORMAT TRACK command.

DESCRIPTION OF UDC REGISTERS

DMA 7-0 (R/W Register; Address 0)
This 8-bit read/write register is loaded with the low order byte (MSB in bit 7) of the DMA buffer memory starting address.

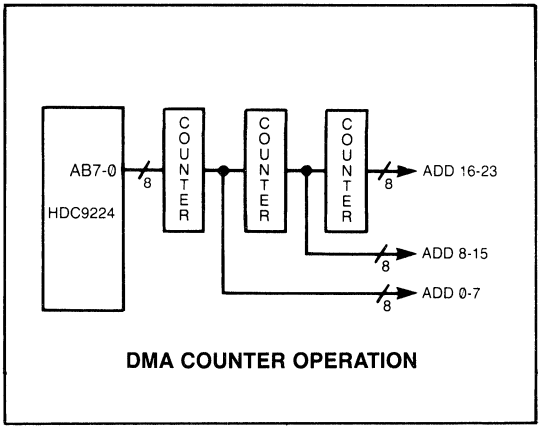
DMA 15-18 (R/W Register; Address 1)
This 8-bit read/write register is loaded with the middle order byte (MSB in bit 7) of the DMA buffer memory starting address.

DMA 23-16 (R/W Register; Address 2)
This 8 bit read/write register is loaded with the high order byte (MSB in bit 7) of the DMA buffer memory starting address.

Prior to the data transfer portion of a read or write command, the UDC writes the contents of the DMA registers to an external counter. This transfer (from the registers to the external counter) is accomplished by the UDC with 3 separate outputs on AB7-0, with the contents of DMA 24-16 being transfered first. In memory areas that require less than 24 bit addressing, the higher order bits are overwritten. The external counter must be incremented with the UDC's $\overline{DS}$ signal after each byte transfer.

If, during read operations, an error is detected during the data transfer, a retry will occur (if so programmed), and the three DMA registers will re-initialize the external counter to the original starting address.

During multiple sector read/write operations, the DMA address contained in the DMA registers will be incremented by the size of the sector selected at each sector boundary. This ensures that during read operations the address contained in the DMA registers always corresponds to the proper memory starting address of the sector currently being read.



DMA COUNTER OPERATION

DESIRED SECTOR REGISTER (R/W Register; Address 3)
This 8-bit read/write register is loaded with the starting sector number of a multiple sector read/write operation. Except for the last sector of the operation, this register is incremented after each sector is written or read without error.

If the UDC terminates a command because of an error, this register will normally contain the bad sector number, and may be read by the processor.

DESIRED HEAD REGISTER (Write Register; Address 4)
The contents of this register are compared to the disk sector's ID Field when verifying a seek operation.

For the PC/AT format, this register is loaded with a 2-bit sector size, and 4-bit head number.

BIT 7 Bad Block Mark (always 0)
BITS 6,5 Sector Size

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

BIT 4 Always 0
BIT 3-0 Desired Head Number

For the SMC format, this 8-bit write only register is loaded with the 4-bit head number and the upper 3-bits of the desired cylinder number.

BIT 7 Bad Block Mark (always 0).
BITS 6-4 MSBs of the Desired Cylinder number.
BITS 3-0 Desired Head Number.

The desired head number is output on AB3-0 during OUTPUT 2 times.

DESIRED CYLINDER REGISTER (Write Register; Address 5)
This 8-bit write only register is loaded with the 8 low order bits of the desired cylinder (MSB in Bit 7). Combined with the 3 high order bits loaded into the DESIRED HEAD REGISTER, these 11 bits form the desired cylinder number, which is checked by read and write operations during the Check ID portion of the command.

SECTOR COUNT REGISTER (Write Register; Address 6)
This 8-bit write only register is loaded with the number of sectors to be operated on by the read or write command. This allows multiple sectors on the same cylinder to be either written or read.

RETRY COUNT REGISTER (Write Register; Address 7)
This 8-bit write only register is loaded with the number of times the UDC should retry to read a data field before reporting an error. Additionally, this register is loaded with the user programmable output signals that the UDC outputs on AB0-3 during OUTPUT 1 times.

The retry count is loaded (in 1's complement format) into the 4 most significant bits of this register.

The user programmable output signals are loaded into the 4 least significant bits of the register.

BITS 7-4 Desired Retry Count (in 1's complement format)
BITS 3-0 User Programmable Output Signals

MODE REGISTER (Write Register; Address 8)
This 8-bit write only register defines the operating mode of the UDC as follows:
BIT 7 (DRIVE DATA TYPE)
This bit determines how the UDC decodes data from the drive.

BIT 7 = (1): UDC configured for hard disk use. (Level transitions)
BIT 7 = (0): UDC configured for floppy use. (Pulse inputs)

STEP RATES FOR DOUBLE DENSITY (MFM) OPERATION **(Mode Bit 4 = 0)**

DRIVE TYPE			5.25″ HARD DISK	8″ FLOPPY	5.25″ FLOPPY
DB2	DB1	DB0	STEP RATE	STEP RATE	STEP RATE
1	1	1	3.2 ms	32 ms	64 ms
1	1	0	1.6 ms	16 ms	32 ms
1	0	1	0.8 ms	8 ms	16 ms
1	0	0	0.4 ms	4 ms	8 ms
0	1	1	0.2 ms	2 ms	4 ms
0	1	0	0.1 ms	1 ms	2 ms
0	0	1	0.05 ms	0.5 ms	1 ms
0	0	0	21.8 us	218 us	436 us
Pulse Width:			11.2 us	112 us	224 us

(DOUBLE ALL OF THE ABOVE TIMES FOR SINGLE DENSITY (FM) OPERATIONS.)

BITS 6,5 (CRC/ECC Enable Code)
These bits determine the error detection/correction code generated and checked by the UDC. In addition, they enable the Write Long command.

DB6	DB5	CODE GENERATED/CHECKED
0	0	CRC
0	1	Enable Write Long
1	0	Internal 32 bit ECC without correction
1	1	Internal 32 bit ECC with correction

With internal ECC selected the UDC will transfer 4 extra bytes during reads and writes. Normal CRC checking is still done on all ID fields.

If ECC is not selected, then the UDC will perform CRC checks on both data and ID fields.

BIT 4 (Single or Double Density)
This bit determines whether the UDC will perform its operations in either single or double density.

BIT 4 = (1) Single Density (FM) Format

BIT 4 = (0) Double Density (MFM) Format

BIT 3 (ALWAYS 0)

BITS 2,1,0 (Step Rate Select)
These bits are programmed to select the desired drive step rate. Note that all step rates are determined by the type of drive and density selected, and are scaled from the CLK input.

The UDC can output extremely rapid step rate pulses if these bits are set to 000. This is useful when the UDC is controlling drives which support buffered seeks. For other speeds, please refer to the table above.

INTERRUPT/COMAND TERMINATION REGISTER
(Write Register; Address 9)

This 8-bit write only register allows the programmer to mask out a number of conditions that would cause termination of a command. (Such termination occurs when the DONE bit in the INTERRUPT STATUS register is set.) One bit in this register also controls the generation of interrupts when either the DONE bit or the READY CHANGE bit in the INTERRUPT STATUS register go active.

BIT 7 (ALWAYS "1")
Setting this bit to "1" will cause the CRC register to preset to 1 for CRC generation and checking.

In the IBM® PC-AT mode, this bit should always be set to "1". Failure to do so may result in unreliable operation.

ID field CRC and data field CRC or ECC are generated and tested from the first A1 HEX byte in the ID field.

BIT 6 (ALWAYS "0")
This bit should always be set to "0" by the user. Failure to do this may result in unreliable operation.

BIT 5 (INT ON DONE)
If this bit is set (to "1"), an interrupt will occur when the DONE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

BIT 4 (DELETED DATA MARK)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the DELETED DATA MARK bit in the CHIP STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 3 (USER DEFINED)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the USER DEFINED status bit in the DRIVE STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 2 (WRITE PROTECT)
If this bit is set (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE PROTECT bit in the DRIVE STATUS register goes active.

BIT 1 (READY CHANGE)
If this bit is set (to "1"), an interrupt will occur when the READY CHANGE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

The user should note that as a drive is selected or deselected, it is possible for the ready line from the drive to change state, and care should be taken in the design of the interrupt handler.

BIT 0 (WRITE FAULT)
If this bit is set (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE FAULT status bit in the DRIVE STATUS register is set. The com-

mand in progress will terminate when the current sector operation is completed.

DATA/DELAY REGISTER (R/W Register; Address 0AH)

This 8-bit read/write register serves three purposes. During UDC writes, data is placed in this register for recording to the disk. During UDC reads, recovered data is fetched from this register for storage into memory. All transfers occur via DB7-0, under DMA control.

Additionally, this register is loaded with the HEAD LOAD TIMER COUNT when the Drive Select command is issued. (Note that the actual amount of head load time is this value, times a value predetermined by the UDC, based on the type of drive selected. For more information, please see the Drive Select command description.)

Finally, in the IBM® PC-AT mode, this register is used for a third purpose. If Implied Seek is enabled, this register is used by Seek/Read ID and Read/Write commands to control the UDC seek operation. The data in the Data/Delay Register and the Current Cylinder Register are used to calculate the direction and step count for a seek.

Please note, the MSB's of the Desired Cylinder Number does not correspond to those written in the Disk ID field.

BITS 7,6 Always 0
BITS 5,4 Actual Sector Size

5	4	Sector Size
0	0	128
0	1	256
1	0	512
1	1	1024

BITS 3,2 Always 0
BITS 1,0 MSB's of Cylinder Number

1	0	Cylinder Number
0	0	0 - 255
0	1	256 - 511
1	0	512 - 767
1	1	768 - 1023

COMMAND REGISTER (Write Register)

This 8-bit write only register is used to pass commands to the UDC. Valid commands are given to the UDC by setting C/$\overline{D}$ high and R/$\overline{W}$ active high, while strobing $\overline{DS}$ active (low).

CURRENT HEAD REGISTER (Read Register)

This 8-bit read only register is updated from the disk when valid ID field sync mark is found while executing a SEEK/READ ID command.

IBM® PC-AT MODE

BIT 7 = 1 Last Sector read had BAD SECTOR bit set.
= 0 Last Sector read had BAD SECTOR bit reset.
BIT 6,5 Sector Size

6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

BIT 4 Always 0
BIT 3-0 Current Head Number (MSB in BIT 3)

SMC AND FLOPPY MODES

BIT 7 = 1 Last sector read had BAD SECTOR bit set.
= 0 Last sector read had BAD SECTOR bit reset.
BITS 6-4 Three most significant bits of the current cylinder. (Most significant bit in BIT 6).
BITS 3-0 Current Head Number (MSB in bit 3).

CURRENT CYLINDER REGISTER (Read Register; Address 5)

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register will contain the 8 least significant bits of the cylinder ID number, as specified during formatting. (The 3 most significant bits of the 11 bit cylinder ID number are contained as part of the CURRENT HEAD REGISTER.)

CURRENT IDENT BYTE REGISTER (Read Register; Address 6)

This 8-bit read only register reads the Ident Byte from the disk during the Read ID command sequence. The Current Ident Byte is written to the disk during the format, changing as specified below.

IDENT BYTE	CYLINDER NUMBERS
FE	0 - 255
FF	256 - 511
FC	512 - 767
FD	768 - 1023

INTERRUPT STATUS REGISTER (Read Register)

This 8-bit read only register contains status information associated with interrupt conditions and errors that occur during disk operation. This register is read by setting C/$\overline{D}$ high, and R/$\overline{W}$ high.

When the Interrupt Status register is read, the INT output signal from the UDC will be reset (to an inactive low level).

BIT 7 (INTERRUPT PENDING)
A "1" indicates that either DONE bit or READY CHANGE bit has gone active. The user may disable these interrupts by setting the appropriate bits in the INTERRUPT/COMMAND TERMINATION, REGISTER. This bit is reset (to "0") by reading the Interrupt Status register.

BIT 6 (DMA REQUEST)
A "1" indicates that the UDC requires a data transfer either to or from its data register. This bit is reset (to "0") by the data transfer.

BIT 5 (DONE)
A "1" indicates that the current command is completed. This bit is reset (to "0") when a new command is issued.

BIT 4,3 (COMMAND TERMINATION CODE–
(Valid only when DONE is set)
These two bits indicate the command termination conditions:

BIT 4	BIT 3	CONDITIONS
0	0	Successful command termination
0	1	Execution error in READ ID Sequence
1	0	Execution error in SEEK Sequence
1	1	Execution error in DATA field

More detailed command termination error information is obtained by reading the Chip Status register.

BIT 2 (READY CHANGE)
A "1" indicates that the "ready" signal from the drive has experienced a low-to-high or high-to-low transition. (This shows that the drive has either become ready or become not ready.) This bit is reset (to "0") by reading the Interrupt Status register.

BIT 1 (OVERRUN/UNDERRUN)
A "1" indicates that a overrun or underrun condition has

occured during a read or write command. These conditions occur when the UDC does not receive an acknowledge (to a DMA request) by the time a byte is ready for transfer to or from the processor.

This bit can only be reset (to "0") with a RESET command or a high on the RESET pin.

BIT 0 (BAD SECTOR)
A "1" indicates that a bad sector (as indicated from the MSB of the head ID byte in the ID field) has been encountered. This bit is reset when a new command is issued, or a good sector is read.

CHIP STATUS REGISTER (Read Register; Address 8)

This 8-bit read only register supplies additional chip status information. The information in this register is only valid between the time that the DONE bit is set in the INTERRUPT STATUS register and the time when the next command is issued to the UDC.

BIT 7 (RETRY REQUIRED)
If a retry was attempted by the UDC during the execution of any read or write command, this bit is set (to "1").

BIT 6 (ECC CORRECTION ATTEMPTED)
If the internal ECC circuitry has attempted to correct a bad sector, this bit is set (to "1").

BIT 5 (CRC/ECC ERROR)
If the UDC detects a CRC error or an ECC error this bit is set (to "1").

BIT 4 (DELETED DATA MARK)
If the UDC reads a deleted data mark in the ID field, this bit is set (to "1"), otherwise it is reset (to "0").

BIT 3 (SYNC ERROR)
If the UDC does not find a sync mark when it is attempting to read either an ID or data field, then this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 2 (COMPARE ERROR)
If the information contained in the DESIRED HEAD and DESIRED CYLINDER registers does not match that contained in an ID field on the disk, this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 1,0 (PRESENT DRIVE SELECTED)
These two binary encoded bits represent the drive currently selected and correspond to the Drive Select bits set in the Output 1 and Output 2 latches.

BIT 1	BIT 0	DRIVE SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

DRIVE STATUS REGISTER (Read Register; Address 9)

This 8-bit read only register contains status information generated by the drives, external ECC Chip (if any), and a user definable input to the UDC from the drive.

To save pins on the UDC, the 8 status lines are input on AB7-0 and are latched in this internal register. The UDC will update this register whenever it is not using AB7-0 to output DMA counter values, OUTPUT 1, or OUTPUT 2 data. When configured as described below, the UDC will input drive status signals and interpret them as follows. In all cases, a logic "1" is considered the active input.

BIT 7 (ECC ERROR)
This bit is set (to "1") when the ECC ERROR signal is generated by an external ECC chip. This signal is input to the UDC on AB7.

BIT 6 (INDEX)
This bit is set (to "1") when the INDEX signal from the selected drive is active. Typically, index pulses from the drives are active for 10us-100us for each disk revolution. This signal is input to the UDC on AB6.

BIT 5 (SEEK COMPLETE)
This bit is set (to "1") when the SEEK COMPLETE signal from the selected drive is active. This bit will go active when the heads of the selected drive have settled over the desired track (at the completion of a seek).

When a drive supplies this signal, reading and writing should not be attempted until SEEK COMPLETE is set (to "1"). This signal is input on AB5.

For floppy disk operation, where the drives normally do not provide this signal, a retriggerable one shot could be used to generate a SEEK COMPLETE signal (if desired).

BIT 4 (TRACK 00)
This bit is set (to "1") when the TRACK 00 signal from the selected drive is active. This indicates that the heads on the selected drive are positioned over track 0. This signal is input on AB4.

BIT 3 (USER DEFINED)
This bit is set (to "1") when the USER DEFINED signal is active. This signal is input on AB3.

BIT 2 (WRITE PROTECT)
This bit is set (to "1") when the WRITE PROTECT signal from the selected drive is active. When set, this bit indicates that the disk in the selected drive is write protected. This signal is input on AB2.

BIT 1 (READY)
This bit is set (to "1") when the READY signal from the selected drive is active. When set, this bit indicates that the drive is ready to execute commands. This signal is input on AB1.

BIT 0 (WRITE FAULT)
This bit is set (to "1") when the WRITE FAULT signal from the selected drive is active. This signal, when active, indicates that a condition exists at the drive that would cause improper writing on the disk. This signal is input to the UDC on AB0.

TEMPORARY STORAGE REGISTERS

The UDC contains two temporary storage registers, used by the UDC for internal operations. The host processor should not attempt to read or modify these registers, as unpredictable results may occur.

UDC COMMAND OVERVIEW

The HDC 9234 has 16 high-level commands that provide the user with a high degree of flexibility and control. All of the commands for the UDC can be thought of as falling into one of two basic groups.

The first group handles the "housekeeping" required by the drives and the UDC itself. These commands are:

RESET	STEP OUT 1 CYLINDER
STEP IN 1 CYLINDER	SET REGISTER POINTER
DRIVE SELECT	RESTORE DRIVE
DESELECT DRIVES	POLL DRIVES

The second group comprises the "READ/WRITE" functions required in a magnetic disk subsystem. These commands are:

SEEK/READ ID	TAPE BACKUP (READ/
FORMAT TRACK	WRITE)
READ TRACK	READ SECTORS LOGICAL
READ SECTORS PHYSICAL	
WRITE SECTORS LOGICAL	

An internal status byte, which contains the BAD SECTOR, DELETED DATA and OVER/UNDER RUN bits, along with the current state of the READY, WRITE PROTECT, WRITE FAULT, and USER DEFINED lines, is checked at various times during command execution.

This internal status byte is examined before the execution of all READ/WRITE commands, and is also checked just prior to the completion of all commands (except for RESET, where its values would be meaningless.)

This byte is also checked by the UDC between sector operations during the execution of READ LOGICAL, READ PHYSICAL, WRITE LOGICAL and WRITE PHYSICAL commands.

The UDC makes decisions regarding command termination and interrupt generation based on the contents of this status byte, and the state of the bits in the INTERRUPT/COMMAND TERMINATION register. (Note that "write protect" and "write fault" status may cause command termination only during write and format operations.)

All commands (except RESET) terminate with the DONE bit in the INTERRUPT STATUS register being set. This bit may also be considered to be an inverted "busy" line, as the UDC resets it upon receipt of a valid command.

During all READ/WRITE group commands (except FORMAT TRACK and BACKUP), the UDC utilizes some common command execution sequences. Prior to entering each sequence the UDC sets the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to a known state. If a command fails to execute properly, these bits may then be used to determine where the command aborted.

The sequences common to the READ/WRITE group commands are as follows:

1. READ ID FIELD (Command Termination Code = 0-1)
   First, the UDC attempts to find an ID Field Sync mark. If no sync mark is found within 33,792 byte times (byte time = time to read one byte from the type of drive selected), the SYNC ERROR bit (in the CHIP STATUS register) is set (to "1"), and the command is terminated.

   During this phase, the UDC will raise and drop RDGATE up to 256 times (as it attempts to read each sector on the cylinder).

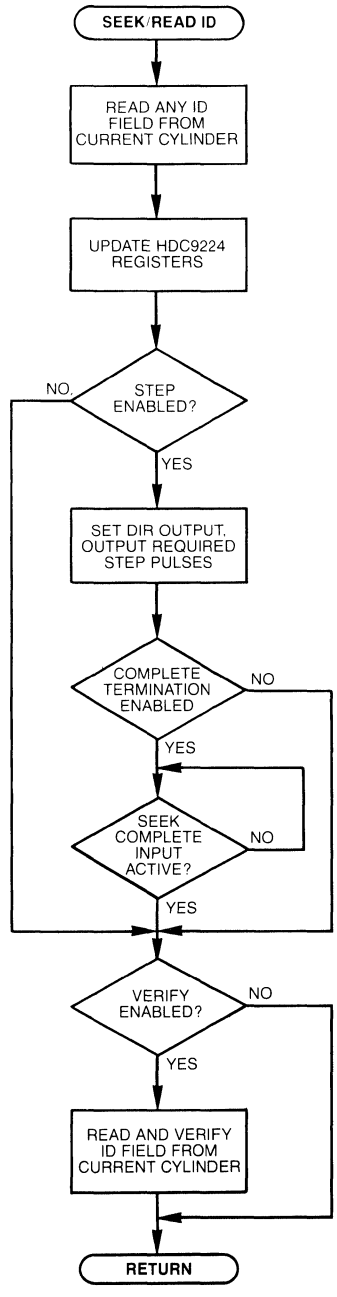
   After the ID Field is found, the UDC reads it and updates it CURRENT HEAD and CURRENT CYLINDER registers. This information was written to the disk during formatting.

   Next, the UDC checks the CRC of the ID field which was read. If it is incorrect, the UDC sets (to "1") the CRC ERROR status bit (in the CHIP STATUS register) and terminates the command.

   If the CRC is correct, the UDC then calculates the direction and number of step pulses required to move the head from the current cylinder to the cylinder specified in the DESIRED HEAD REGISTER. These pulses, and the direction bit are output during the OUTPUT 2 times.

   If a command should terminate while in the sequence, the COMMAND TERMINATION bits will be set to 0-1.

2. VERIFY (Command Termination Code = 1-0)
   After the UDC has read the ID Field, it attempts to verify that it has found the correct cylinder. To do this, the UDC tries to find an ID Field sync mark on the selected



SEEK/READ ID OPERATION

disk. If the UDC is unable to find an ID Field sync mark within 33,792 byte times, the SYNC ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

The UDC, after finding the ID Field sync mark, then reads the ID field and compares the information on the disk to the information contained in the DESIRED CYLINDER, DESIRED HEAD and DESIRED SECTOR registers.

The UDC will hunt for sync marks and read ID fields until the desired sector is found. If the desired sector is not located within 33,792 byte times, then the COMPARE ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

After the correct sector is found, the UDC checks the CRC for the sector ID Field. If this is found to be incorrect, the UDC sets to "1" the CRC/ECC ERROR bit in the INTERRUPT STATUS register, and the command is terminated.

(When the UDC is executing a READ PHYSICAL or WRITE PHYSICAL command, ID Fields are checked only until the first sector to be transfered is found. No ID Field checking is performed on subsequent sectors, although CRC checking is done.)

If a command should terminate while in this sequence, the COMMAND TERMINATION bits will be set to 1-0.

3. DATA TRANSFER (Command Termination Code = 1-1)

If a READ PHYSICAL or READ LOGICAL command is being executed, the UDC will try to find a data sync mark (FBhex or F8hex) on the disk. If the sync mark found is F8h, then the UDC will set the DELETED DATA MARK bit in the CHIP STATUS register.

After a data sync mark is found, the UDC then updates its CURRENT HEAD and CURRENT CYLINDER registers from the information found on the disk and initiates a DMA request. If the host processor does not respond to the request within 1 byte time, then the UDC will set to "1" the OVER/UNDERRUN status bit in the INTERRUPT STATUS register, and the command will terminate.

Using DMA, the UDC transfers a sector's worth of data, and then reads the ECC and/or CRC bytes. If a CRC error or uncorrectable ECC error is detected, the UDC will decrement the RETRY REGISTER, set the RETRY REQUIRED status bit (in the CHIP STATUS register), and return to the VERIFY sequence.

If the UDC cannot read the sector, and the count in the ENTRY COUNT register has expired, then the CRC/ECC Error bit (in the CHIP STATUS register) is set, and the command terminates.

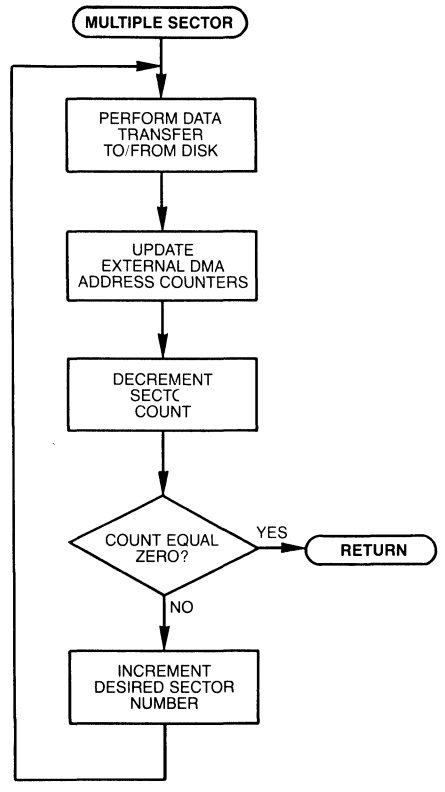
During a multi-sector transfer, the UDC updates the DMA registers after all sector operations, including the last one, and the SECTOR COUNT register is decremented. If the SECTOR COUNT register equals 0, then the command is terminated. If the SECTOR COUNT register is not equal to 0, then the UDC will increment the DESIRED SECTOR register, re-initialize the RETRY COUNT register (to its original value) and return to the VERIFY sequence.

If a command should terminate while in this sequence, the command termination bits will be set to 1-1.

COMMAND DESCRIPTION

RESET (Hex Value = 00)

This command causes the UDC to return to a known state. This command allows the system software to reset the chip, and has the same effect as $\overline{RST}$ input becoming active.



MULTIPLE SECTOR READ OPERATIONS

DESELECT DRIVE (Hex Value = 01)

This command causes all of the drive select bits (Drive Select 0-3) in the OUTPUT 1 and OUTPUT 2 registers to become inactive.

RESTORE DRIVE (Hex Values = 02, 03)

This command will cause the HDC 9234 to output step pulses to the selected drive, so as to move the head back to Track 00. Before each step pulse, the UDC first checks the TRK00 and READY bits in the DRIVE STATUS register. If TRK00 is active (high) or READY is inactive (low), then the UDC will terminate the command.

The UDC will output up to 4096 step pulses. If the drive does not respond with an active (high) TRK00 signal within this period, the UDC will terminate the command with the DONE bit set (to "1") and the COMMAND TERMINATION CODE

bits set to 1-0. (These bits are contained in the INTERRUPT STATUS register.)

This command takes two forms:

COMMAND BYTE	RESULT
02	The command will terminate, and an interrupt generated after the UDC has issued the step pulses.
03	The command will terminate, and an interrupt generated after the drive has provided a SEEK COMPLETE signal to the UDC. (This is useful in systems with "buffered seek" drives.)

This command uses the step rate value loaded into the MODE register.

STEP IN 1 CYLINDER (Hex Values = 04, 05)

This command will cause the HDC 9234 to issue one step pulse towards the inner most track. This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
04	The command will terminate, and an interrupt generated after the UDC issues the step pulse.
05	The command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of SEEK COMPLETE the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE register.

STEP OUT 1 CYLINDER (Hex Values = 06, 07)

This command will cause the HDC 9234 to issue one step pulse towards the outer most track (Track 00). This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
06	This command will terminate, and an interrupt generated after the UDC issues the step pulse.
07	This command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of the SEEK COMPLETE, the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE Register.

POLL DRIVES (Hex Values = 10 thru 1F)

This command polls the drives for a SEEK COMPLETE signal allowing the user to perform simultaneous seeks on up to four drives. Polling is enabled by setting (to 1) the appropriate bit in the command word: bit 0 for drive 0 thru to bit 3 for drive 3.

This command executes as follows:

The UDC will output a drive select for the first drive in the polling sequence and look for a SEEK COMPLETE status input from the polled drive. If the polled drive has not completed a seek, then this line remains low (logic 0), and the UDC selects the next drive in the polling sequence. This continues until the UDC detects a SEEK COMPLETE signal from a drive, which causes the DONE bit in the Interrupt Status register to be set, and the command terminates.

The UDC will continue to select the drive that produced the SEEK COMPLETE signal, allowing the user to read the DRIVE STATUS register to determine which drive caused the command termination.

The POLL DRIVES command must be preceeded by SEEK or DESELECT. In normal use, a SEEK command would precede the POLL DRIVES command. In those cases where another command (other than SEEK) has been issued to a drive in the polling sequence, it will be necessary to DESELECT that drive prior to issuing the POLL DRIVES command. This applies even if the selected drive was not included in the polling sequence.

DRIVE SELECT (Hex Values = 20 thru 3F)

This command will cause one of (up to) four drives to be selected for operation. Any previously selected drive is deselected by this command. Bits 0 and 1 in the command word indicate (in binary form) which of the (up to) four drives has been selected.

COMMAND WORD		DRIVE SELECTED
DB1	DB0	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

Decoded drive select signals are then placed on the data bus (via AB7-AB4) during OUTPUT 1 times and should be latched externally.

Since the HDC 9234 can interface both hard disks and floppy disks to a processor, the Drive Select command needs to also specify the type of drive being selected. Bits 2 and 3 in the command word are used to pass this information to the chip, and take the following form:

COMMAND WORD		TYPE OF DRIVE
DB3	DB2	
0	0	Hard disk with IBM® PC-AT compatible format—512 Byte data field and 4 byte ID field per sector. No internal clock prescaling performed.
0	1	Hard disk with user defineable format. This format allows a data field length of 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes with 5 byte ID field per sector. No internal clock pre-scaling is performed.
1	0	8 inch floppy disk, with standard 4 byte (FM) or 5 byte (MFM) ID field. An internal divider creates a 1 MHz clock to be compatible with standard disk data rates.
1	1	5.25 inch floppy disk, with standard 4 byte (FM) or 5 byte (MFM) ID field. An internal divider creates a 500 KHz clock to be compatible with standard disk data rates.

NOTE: Microfloppy system designers should determine whether the drive they have chosen to use in the system is compatible with 8" floppy drives or 5.25" floppy drives, and use the appropriate values from the table above.

Note that eight inch Winchester-type drives require an 8.696 MHz system clock. All other drives require a 10 MHz system clock. It is not possible for the UDC to derive internally the clocks required for floppy disk operation from the 8.696 MHz clock required by 8 inch Winchester drives.

To insure compatibility with various drives, the HDC 9234 features a programmable head load timer. Head load delay may be inhibited by resetting the Delay Bit (Bit 4) in the Drive Select command word to 0. If Bit 4 is set (to 1), then the head load delay timer is configured with the value in the

DATA/DELAY register (Register A), multiplied by value shown below:

DRIVE AND FORMAT SELECTED	HEAD LOAD TIMER INCREMENT (BIT 4 = 1 = Delay Enabled)	
5.25" HARD DISK (Double Density)	200 usec	
5.25" HARD DISK (Single Density)	400 usec	
8" FLOPPY (Double Density)	2 msec	(The HEAD LOAD TIMER is set to a value equal to this increment times the number in the DATA/DELAY register.)
8" FLOPPY (Single Density)	4 msec	
5.25" FLOPPY (Double Density)	4 msec	
5.25" FLOPPY (Single Density	8 msec	

The Drive Select command also optimizes certain characteristics of the HDC 9234 for the type of drive selected.

IF HARD DISK SELECTED:

–DMA mechanism works in burst mode and the bus is held for the entire sector transfer.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.

IF FLOPPY DISK SELECTED:

–DMA mechanism transfers an 8-bit byte, and releases the bus.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

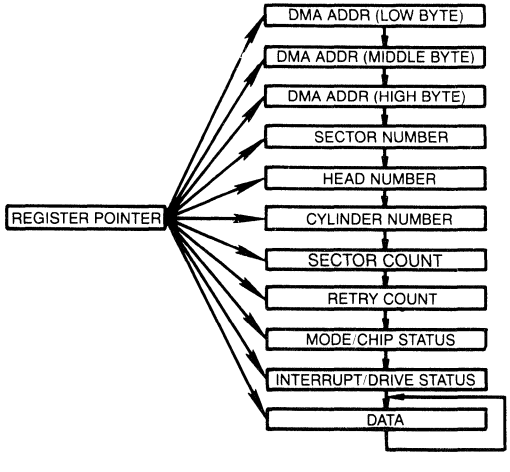
–The GAP lengths are as shown in Table 1.

–The CLK input clock is prescaled (internally) to create an internal clock compatible with the floppy disk data rates.

SET REGISTER POINTER (Hex Values = 40 to 4A)
This command causes the register pointer to point to a register. The desired register number is loaded into the 4 least significant bits of the command word. (MSB in BIT 3).

The register pointer is incremented by the UDC on each register access, until it points to the DATA register. This reduces the number of times the user must set the register pointer during read and write operation.

Care should be taken to ensure that only valid register values are loaded into the command word. (Valid register numbers are 0 thru OAH.)



SET REGISTER POINTER COMMAND

SEEK/READ ID (Hex Values = 50 to 57)
This command will cause the UDC to read the first sector ID field found from the currently selected drive, head, and cylinder. The MODE register should contain the correct value for step rate and density options.

After reading the ID field the UDC will examine the command word and execute the specified options. Bits 2 thru 0 in the command word are used to specify the following options:

BIT 2 = 1 STEP ENABLE. The UDC will execute the step sequence, and position the head on the track specified by the DESIRED CYLINDER register.

BIT 2 = 0 STEP DISABLE. No step pulses will be issued by the UDC.

BIT 1 = 1 WAIT FOR COMPLETE. The UDC will proceed to the verify sequence only after the drive has issued a SEEK COMPLETE signal.

BIT 1 = 0 DO NOT WAIT FOR COMPLETE. The UDC will proceed to the verify sequence after the last step pulse has been issued.

BIT 0 = 1 VERIFY ID. The UDC will execute the VERIFY sequence after operations selected by the previous options have finished.

BIT 0 = 0 DISABLE VERIFY ID. The UDC will not enter the VERIFY sequence. Instead, the command will terminate.

The order in which these options execute is: STEP, COMPLETE, VERIFY ID. Any combination of these option bits may be specified in the command word.

READ SECTORS PHYSICAL (Hex Values = 58 and 59)
This command will cause the UDC to read up to a full track from the disk. The user specifies the MODE, DESIRED CYLINDER, DESIRED HEAD, and DESIRED SECTOR along with the SECTOR COUNT. When using the IBM® PC-AT format, register A must also be initialized. The UDC will find the requested cylinder and sector and set up to begin the data transfer.

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

If a BAD SECTOR bit is read (from the sector ID field) the UDC will set the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to 1-0, and set the DONE bit (in the INTERRUPT STATUS register) to 1, and terminate the command.

After each sector is successfully read, the SECTOR COUNT register is decremented. If the SECTOR COUNT register is not yet equal to 0 the process is repeated for the next physical sector on the track. This command also will terminate if the Index pulse is received from the drive.

(Note that after the first sector is found, no further comparison is made against sector numbers found on the disk as the DESIRED SECTOR register value may not correspond to the next physical sector on the disk because of sector interleaving.)

This command takes two forms allowing the user to specify the desired transfer option. The options are specified by Bit 0 in the command word, and are:

BIT 0 = 1 TRANSFER ENABLE. The UDC will transfer the data fields to (external) memory, using DMA.

BIT 0 = 0 TRANSFER DISABLE. The UDC will NOT transfer any data to (external) memory, but all error detection circuitry will be enabled and errors reported. This is useful in detecting bad sectors and tracks on the disk.

Before executing this command, the user must set the RETRY COUNT to 0. This is done by loading the high order nybble in the RETRY COUNT register to "1111" (zero in 1's complement format). Failure to do this will result in unpredictable performance because the DESIRED SECTOR register value may not correspond to the next physical sector on the disk.

READ TRACK (Hex Values = 5A and 5B)

When this command is issued, the UDC will read the data from the entire track on which the selected drive is currently sitting. The UDC will begin reading when it detects the leading edge of an index mark signal from the drive, and terminate reading when it detects the next leading edge of an index mark signal. Sync detect is performed for the ID field, but no error checking is done on the data field.

This command allows the user to specify a data transfer option, using Bit 0 in the command word. These options are:

BIT 0 = 1 TRANSFER ALL DATA. The UDC will transfer the ID field and data fields to (external) memory.

BIT 0 = 0 TRANSFER ONLY IDs. The UDC will transfer only ID fields to the (external) memory. This is useful during tape backup operations.

READ SECTORS LOGICAL (Hex Values = 5C to 5F)

When this command is issued, the UDC will read up to a full track from the selected drive. Prior to reading the data from the disk, the UDC will (if enabled in command) use the information in the MODE, DESIRED CYLINDER, DESIRED SECTOR and DESIRED HEAD (and Register A for IBM® PC-AT mode) registers to locate the correct track, sector and drive surface (using the previously described VERIFY sequence).

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

Before the command is issued, the system processor must also load the desired values into the MODE, SECTOR COUNT, RETRY COUNT and the three DMA registers.

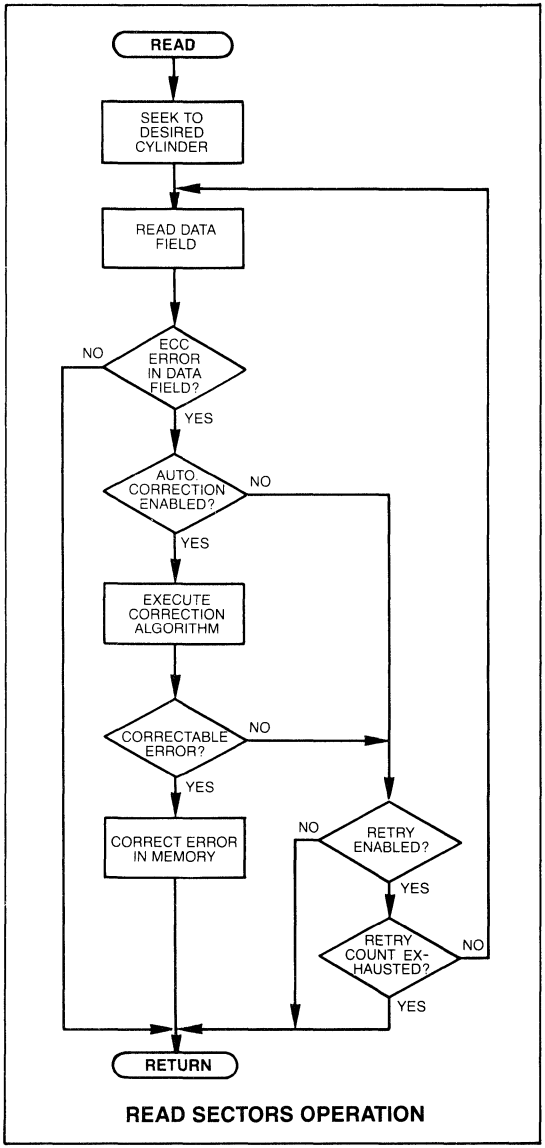
After the desired track and sector is found and verified, the DATA TRANSFER sequence begins. After each successful sector transfer, the UDC increments the DESIRED SECTOR register (except after the last sector is transferred), decrements the SECTOR COUNT register, and re-enters the VERIFY sequence. This process continues until the SECTOR COUNT register is equal to 0 (or an error occurs).

This command has four options, which are specified by Bit 1 and Bit 0 of the command word. The four options are:

BIT 1 = 1 IMPLIED SEEK DISABLED. The UDC will not update the CURRENT CYLINDER, CURRENT HEAD OR CURRENT SECTOR register and will not issue step pulses.

BIT 1 = 0 IMPLIED SEEK ENABLED. The UDC will update the CURRENT CYLINDER, CURRENT HEAD and CURRENT SECTOR register and will issue step pulses if requird.

BIT 0 = 1 TRANSFER ENABLED. The UDC will transfer data from the disk to the system. The DMA REQUEST status bit (in the INTERRUPT STATUS register) will be set when the UDC requires servicing.



READ SECTORS OPERATION

BIT 0 = 0 TRANSFER DISABLED. The UDC will not transfer data read from the disk, but all error checking circuitry will be enabled.

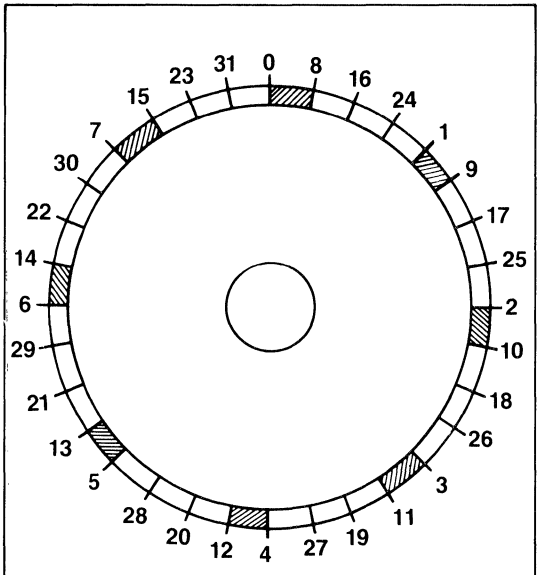
FORMAT TRACK (Hex Values 60 to 7F)

This command causes the UDC to format the current cylinder from the leading edge of one index mark to the leading edge of the next index mark. The format chosen is dependent on the Drive Select command.

During execution of the FORMAT TRACK command, the UDC will fetch all required ID field data from external memory, and write it to the disk, along with format constants supplied automatically by the UDC. This reduces the number of bytes required to format a sector to 3 or 4, depending on the format chosen.

Before the FORMAT TRACK command can be given, the system processor must:

1. Generate an ID Field Table for the track in UDC memory area. This ID Field Table consists of:
   IDENT BYTE (not required for floppy disk FM format)
   CYLINDER BYTE
   HEAD BYTE
   SECTOR NUMBER BYTE
   SECTOR SIZE/ECC SIZE BYTE (not required for IBM® PC-AT FORMAT) repeated for each sector on the track.



INTERLEAVED SECTORS

The UDC can format a track with interleaved sectors by staggering the sector numbers. For example, to format a 32 sector track, with a sector interleave factor of 4, the system processor would set up the ID Field table sector numbers as follows:
0,8,16,24,1,9,17,25,2,10,18,26,3,11,19,
27...7,15,23,31.

(Note that when formatting in IBM® PC-AT and floppy FM modes, only four bytes are required for each sector, while five bytes are needed for floppy MFM and user defineable formats. Also note that sector numbers start with zero (0) on IBM® PC-AT compatible format, and start with one (1) on IBM formatted floppy diskettes.)

2. Load the UDC DMA registers with the starting address of the external memory buffer containing the ID Field data just created.
3. Issue the DRIVE SELECT command, which moves the DMA registers to the CURRENT HEAD, CURRENT CYLINDER, and a TEMPORARY REGISTER. (This is necessary because the UDC will now re-use the DMA registers to hold format parameters).

   When formatting multiple cylinders, the system processor does not need to re-issue DRIVE SELECT between cylinders as the STEP IN and STEP OUT commands preserve the DMA addresses and format parameters. It is necessary, however, to update the ID Field table, described in #1, above.
4. Load the DESIRED HEAD register with the proper value.
5. Load the following values (in the format shown) into the registers indicated below:

PARAMETER	FORMAT	REGISTER
GAP 0 Size	two's complement format	DMA 7-0
GAP 1 Size	two's complement format	DMA 15-8
GAP 2 Size	two's complement format	DMA 23-16
GAP 3 Size	two's complement format	Desired Sector
Sync Size	one's complement format	Desired Cylinder
Sector Count	one's complement format	Sector Count
Sector Size Mult.	one's complement format	Retry Count

FORMAT PARAMETERS TABLE

When using the hard disk format, the values for GAP 0 and GAP 1 must both be set to the same number, and loaded into the appropriate DMA register.

The Sector Size Multiple programs the UDC to format with a sector size that is a multiple of 128 data field bytes. For example, to format a track with a sector data field size of 256 bytes, then the Sector Size Multiple would be set to FD hex, which is "2" in one's complement notation.

In IBM® PC/AT mode, the sector sizes allowed are 128, 256, 512, or 1024 bytes. In IBM® floppy disk format, the sector sizes allowed are 128, 256, 512, or 1024 bytes. With user defineable hard disk formats, allowed sector sizes are 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes.

6. Load the MODE register to specify the step rate, single or double density option, and CRC/ECC options.
7. Step to the desired track. For the first track, this is normally done by issuing a RESTORE DRIVE command, to return the heads to Cylinder 000, then use the STEP IN 1 or STEP OUT 1 commands to move the head to subsequent cylinders on the disk.
8. Issue the FORMAT TRACK command. All data fields on the disk will be filled with E5 hex. In double density recording (MFM) all gaps will be filled with 4E hex, while in single density (FM) all gaps will be filled with FF hex. This format is compatible for IBM specifications for floppy disks.
9. To Format additional tracks, it is only necessary to update the ID Field table (step 1) and repeat steps 7 and 8. Do NOT modify the DESIRED HEAD register when formatting additional tracks with the same head. If it is necessary to change the DESIRED HEAD register, the system processor must repeat all steps described above.

   The FORMAT TRACK command allows the user to specify several options. These options are specified by setting the appropriate low order bits in the command word. The bit mapping for these options are:

BIT 4 = 0 Write Deleted Data Mark. During the format process, the UDC will write the deleted data mark (F8 hex) for the data address field.

BIT 4 = 1 Write Normal Data Mark. During the format process, the UDC will write the normal data field address mark (FB hex).

BIT 3 = 1 Write with Reduced Current. When this bit is set, the Reduced Write Current Output will go high (active) during the Output 2 time slot.

BIT 3 = 0 Write with Normal Current. When this bit is reset, the Reduced Write Current Output wil remain low (inactive) during the Output 2 time slot.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during the format of disks. The following table specifies these values:

SECTOR SIZE FIELD BITS (IBM® FLOPPY AND USER SELECTABLE HARD DISK FORMATS)

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD (IBM® FLOPPY AND USER SELECTABLE HARD DISK FORMATS)

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM® MFM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT*			Ident Byte					
CYLINDER			track number					
HEAD			side number					
SECTOR			sector number				sector size	
SECTOR SIZE							(3 bits)	

IBM® FM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER			track number					
HEAD			side number					
SECTOR			sector number					
SECTOR SIZE	X	X	X	X	X		sector size	

HARD DISK FORMAT: IBM PC-AT FORMAT (512 BYTES)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT			Ident Byte					
CYLINDER			cylinder number (8 LSB's)					
HEAD	0	sctr bit 1	sctr bit 0	0	hd# bit 3	hd# bit 2	hd# bit 1	hd# bit 0
SECTOR			sector number					

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT*			Ident Byte					
CYLINDER			cylinder number (8 LSB's)					
HEAD	bad sctr flag	cyl# bit 10	cyl# bit 9	cyl# bit 8	hd# bit 3	hd# bit 2	hd# bit 1	hd# bit 0
SECTOR			sector number					
SECTOR SIZE			ECC type		X		sector size (3 bits)	

*for double density

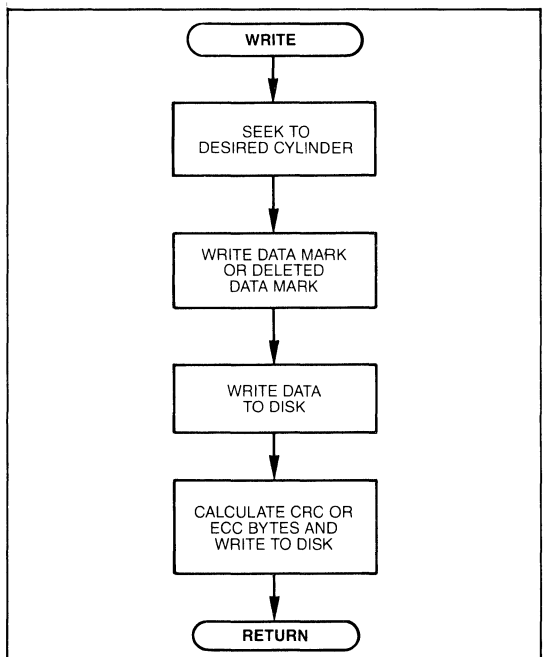
ID FIELD IDENT BYTE	CYLINDERS
FE	0 - 255
FF	256 - 511
FC	512 - 767
FD	768 - 1023

WRITE SECTORS LOGICAL (Hex Values A0 thru BF, E0 thru FF)

This command will cause the UDC to write logically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	REGISTER A (for IBM® PC-AT Mode)

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).



WRITE DATA OPERATION

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder (if enabled in command) and verify that has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register.

Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next logical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 IMPLIED SEEK DISABLED. The UDC will not update the CURRENT CYLINDER,

CURRENT HEAD OR CURRENT SECTOR register and will not issue step pulses.

BIT 6 = 0 IMPLIED SEEK ENABLED. The UDS will update the CURRENT CYLINDER, CURRENT HEAD and CURRENT SECTOR register and will issue step pulses if required.

BIT 5 = ALWAYS 1.

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to floppy disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: For hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

WRITE LONG

This command will cause the HDC9234 to transfer one sector of data and four ECC bytes from the buffer to the disk. The system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	REGISTER A (for IBM® PC-AT mode)

WRITE LONG can operate on only one sector per command. The sector slew register should be programmed to 1. The value in the retry counter is decremented by the HDC9234. It should, therefore, be programmed for each Write Long command.

This mode is enabled by programming the mode register (R8) bits 6 and 5 to 01. In this mode there is no retry. The retry counter register (R7) will be used as the ECC check byte length counter. The 1's complement value of the desired check byte length plus two should be programmed into these 4 bits, mapped as follows:

REGISTER 7	ECC LENGTH
1111	2
1110	3
1101	4
1100	5
1011	7
•	•
•	•
•	•

The system processor then issues the Read Sector Logic command. Signal $\overline{\text{ECCTM}}$ will not be activated in the WRITE LONG operation.

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder (if enabled in command) and verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data including the programmed number of ECC bytes using (DMA) for the memory area specified by the DMA register.

This command allows the user to specify several options. These options are specified by the bits in the command word, as follows:

BIT 6 = 1 IMPLIED SEEK DISABLED. The UDC will not update the CURRENT CYLINDER, CURRENT HEAD or CURRENT SECTOR register and will not issue step pulses.

BIT 6 = 0 IMPLIED SEEK ENABLE. The UDC will update the CURRENT CYLINDER, CURRENT HEAD and CURRENT SECTOR register and will issue step pulses if required.

BIT 5 = ALWAYS 1.

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCE WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensated value to be used during writes to disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: for hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

WRITE SECTORS PHYSICAL (Hex Values 80 thru 9F, C0 thru DF)

This command will cause the UDC to write physically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	REGISTER A (for IBM® PC-AT Mode)

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder (if enabled in command) and verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register. Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next physical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 IMPLIED SEEK DISABLED. The UDC will not update the CURRENT CYLINDER, CURRENT HEAD or CURRENT SECTOR register and will not issue step pulses.

BIT 1 = 0 IMPLIED SEEK ENABLED. The UDC will update the CURRENT CYLINDER, CURRENT HEAD and CURRENT SECTOR register and will issue step pulses if required.

BIT 5 = ALWAYS 0.

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to floppy disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: for hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

TAPE BACK-UP (Hex Values = 08 to 0F)

The TAPE BACK-UP command set provides the system with the capability of transferring data to and from a tape drive in continuous blocks. TAPE BACK-UP utilizes the UDC's DMA, data conversion, error detection/correction and sector count circuitry.

Because of the mechanical and electronic differences between tape drives and disk drives, some of the register bits described earlier in this data sheet change functions when the UDC is executing the TAPE BACKUP COMMAND. In many cases, the CLK input to the UDC will also need to be changed to compensate for the slower data rate from tape drives.

TAPE BACKUP REGISTER DESCRIPTION

The following bits in the UDC's register file assume the functions listed below when executing the BACK-UP command and should be programmed accordingly.

The following tables describe the differences in register usage when the UDC is executing the TAPE BACKUP command. (Complete TAPE BACKUP register bit maps are located in rear of the data sheet.)

MODE REGISTER

Bit 2 = 1 16 byte sync detect delay enable
= 0 16 byte sync detect delay disabled

Bit 1 = 1 TAPE BACKUP Write Enable (writing)
= 0 TAPE BACKUP Write Disable (reading)

Bit 0 = 1 Tape mark enable (short block)
= 0 Tape mark disable (long block)

RETRY COUNT REGISTER

Bits 7-4 Retry should be disabled, by setting these bits to "1". (Retry Disabled)

Bits 3-0 program outputs (user controlled) Bit 3 is typically used for write enable to the tape drive.

Bits 0 and 1 are typically used for tape driven motion control as per drive manufacturer's specification.

DESIRED CYLINDER

Bits 7-4 ECC Type Field:

DB7	DB6	DB5	DB4	ECC TYPE
0	0	0	0	4 ECC bytes generated/ checked
1	1	1	1	5 ECC bytes generated/ checked
1	1	1	0	6 ECC bytes generated/ checked
1	1	0	1	7 ECC bytes generated/ checked

note: 5, 6, 7 byte ECCs are generated and checked by hardware external to the UDC.

DESIRED CYLINDER

Bit 3 Always 1

Bits 2-0 Data Block Size:

DB2	DB1	DBO	DATA BLOCK SIZE
0	0	0	128 bytes
0	0	1	256 bytes
0	1	0	512 bytes
0	1	1	1024 bytes
1	0	0	2048 bytes
1	0	1	4096 bytes
1	1	0	8192 bytes
1	1	1	16,384 bytes

Remember that the UDC internal ECC code can correct up to a 4K byte long Data Block, but that the larger the Data Block the greater the probability of a miscorrection.

Also, when executing the TAPE BACKUP command, the DRIVE SELECT command is altered slightly, as illustrated below:

DRIVE SELECT COMMAND

Bit #	7	6	5	4	3	2	1	0
Drive Select	0	0	1	Ramp Up/Down delay enable	1	CLK divisor	1	0

DB2	CLOCK DIVISOR FOR TAPE
0	CLK is divided by 10 (similar to 8" floppy divisor).
1	CLK is divided by 20 (similar to 5.25" floppy divisor).

These bits, in conjunction with Bits 4 and 7 of the MODE register, will allow selection of both FM and MFM recording on tape, with a tape format that resembles IBM compatible floppy disk formats.

Setting the Drive Type bits to 1,0 or 1,1 will also cause the UDC to take on the following characteristics:

- –DMA mechanism transfers a byte (8 bits) and relinquishes the bus.
- –The RDGATE and WRGATE output signals have timing characteristics as shown in Figures 12A and 12B of the UDC spec.
- –The gap lengths are as illustrated in Table 1 or the UDC spec.
- –Tape format parameters will be as per Table 1 of the UDC spec.

COMMAND EXECUTION OVERVIEW

The tape backup command allows the user a convenient method of backing up either floppy or hard disks to tape. The UDC may be interfaced to either cartridge or cassette type tape drives, working in either streaming or start/stop mode.

Read and Write functions of TAPE BACKUP share a common command byte. The three LSB's of the MODE register are also used by the TAPE BACKUP command to specify user options, and to select between tape read or tape write mode.

Two kinds of blocks may be specified when reading or writing dependent on the state of the TAPE MARK ENABLE bit in the MODE register:

1. DATA BLOCK. The length of the data block (also called a long block) is equal to:
   2^n* 128 bytes where n is an integer between 0 and 7 inclusive. The desired length of the data block (2^n) is programmed into the desired cylinder register.
2. TAPE MARK. The minimum length of the tape mark (also called a short block) is 3 bytes. The maximum length of the tape mark is 257 bytes. The desired length is programmed into the sector count register.

Multiple data block transfers are accomplished by programming the 1's complement of the desired number of data blocks to be transferred into the sector count register.

The three LSB's of the MODE register function as part of the BACK-UP command word. The WRITE ENABLE bit determines whether loading the BACK-UP command into the UDC will initiate execution of a BACK-UP READ or BACK-UP WRITE sequence. The TAPE MARK ENABLE bit determines whether the UDC will write a short or long block of data on the tape and the DELAY ENABLE bit determines whether or not the RDGATE signal is stretched when it coincides with a sync mark when reading the tape. The remaining bits in the command word are as follows:

COMMAND	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BACK-UP (READING)	0	0	0	0	1	0	0	xfer enable
BACK-UP (WRITING)	0	0	0	0	1	precomp value		

BACK-UP READ

When reading a short block, only CRC is checked. When reading a long block, CRC or ECC will be checked, depending on the CRC/ECC bits in the Mode register.

Bit 0 = 1 Data transfer enabled, error checking enabled
= 0 Data transfer disabled, error checking enabled

BACK-UP WRITE

When writing, the precompensation value is derived from the CLK frequency as follows:

Bit 2	Bit 1	Bit 0	Precompensation
0	1	0	None, enable EARLY and LATE
1	0	1	6 CLK cycle periods
0	1	1	5 CLK cycle periods
1	1	1	4 CLK cycle periods
1	1	0	3 CLK cycle periods
1	0	0	2 CLK cycle periods
0	0	1	1 CLK cycle period
0	0	0	None, suppress EARLY and LATE

PRECOMPENSATION SELECT FOR BACK-UP COMMAND

TAPE BACKUP SYSTEM CONFIGURATION NOTES

(A schematic showing a typical system implementation using the TAPE BACKUP feature is contained in Schematic Diagram 2.)

1. Proper operation of the TAPE BACKUP command requires that the tape drive be addressed as DRIVE #3 by the UDC.
2. During the UDC's OUTPUT 2 period external circuitry must enable a separate latch to receive the user defined IO bits and tape track number bits. This latch should use the DRIVE SELECT 3 signal (output during the OUTPUT 2 period) so that the contents of the latch may only be changed when the tape drive is selected.

   Four additional drive control signals may be loaded into the four LSB's of the RETRY COUNT register. These additional outputs are latched externally during OUTPUT 1 times for use by the tape drive. These outputs would normally be used to control tape drive Write Enable logic (bit 3) and tape motion (bits 0 and 1), and tape motor on and off (bit 2).
3. It is important to consider the time required for a tape drive to come up to operating speed when using the TAPE BACKUP command. Also, to insure adequate spacing between tape blocks, a delay is frequently required before stopping tape motion. The UDC has a programmable Ramp Up and Ramp Down timer to allow for easier implementation. The desired delay is programmed into the DATA/DELAY register before issuing the DRIVE SELECT "3" command.

CLOCK DIVISOR BIT	DENSITY BIT MODE REGISTER BIT 4	TIME IN SECONDS PER DELAY REGISTER COUNT
1	1 (Single)	1 CLK Cycle * 80000
1	0 (Double)	1 CLK Cycle * 40000
0	1 (Single)	1 CLK Cycle * 40000
0	0 (Double)	1 CLK Cycle * 20000

   The UDC will issue a normal interrupt (with the command termination code set to 0-0) when the RAMP UP or RAMP DOWN timer has expired.

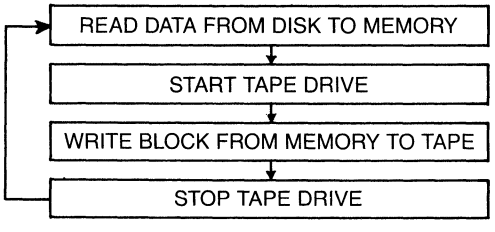
4. BACK-UP WRITE. The user will first request the UDC to perform a disk READ TRACK command, with the TRANSFER ENABLE bit in the command word reset. This will cause the UDC to transfer only the ID field information to memory.

   The TAPE BACKUP command will then be issued causing the UDC to write this ID information to the tape as a tape mark (typically 96 bytes for a drive formatted with a 3 byte/sector ID field or 128 bytes for a drive formatted with a four byte/sector ID field. The data fields should then be transferred to the tape in a similar manner.

   The UDC may be used with either "Streaming" or "Start/Stop" type tape drives. This is illustrated by the following examples:

A. START/STOP TAPE DRIVE:

typically transfers ½ or 1 disk track at a time as illustrated by the following flow chart:



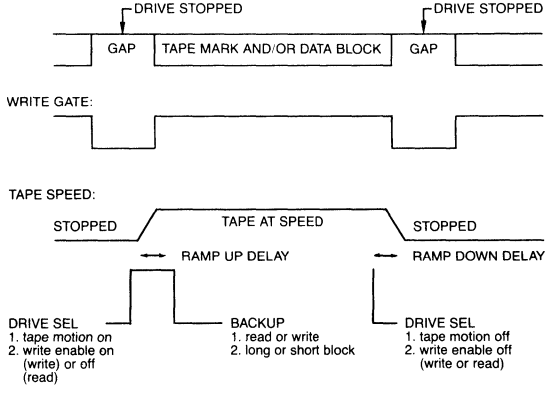
When controlling a start/stop tape drive, the UDC will write the data "block by block". The system will issue a Drive Select command to the UDC with the Tape Motion, Motor On and Write Enable bits set to start and write data to the tape.

The UDC will interrupt the system after the completion of the Ramp Up Delay indicating that the tape drive is up to speed. This interrupt is distinguished by the Command Termination Code of 0-0 (normal completion of command).

The System then outputs the Write command (for a long or short block) and waits for the command termination interrupt. The UDC will write the Sync mark and tape mark or data block on the tape.

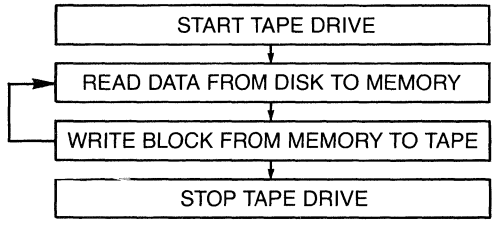
When the System receives the interrupt indicating completion of the Write command, it will issue another drive select command with the Motor On and Write Enable bits set to stop the drive. The UDC will interrupt the system after completion of the Ramp Down Delay indicating that the tape has stopped moving.

The UDC will turn the Write Gate signal on when it is writing data and off when it is not, without regard to the tape motion. The Write Gate signal is used to generate "gaps" on the tape between the data blocks. This is done by externally forcing the two Data outputs with the Write Gate signal such that the Data + signal is high and the Data − signal is low when the UDC is not writing data to the tape (Write Gate is off):

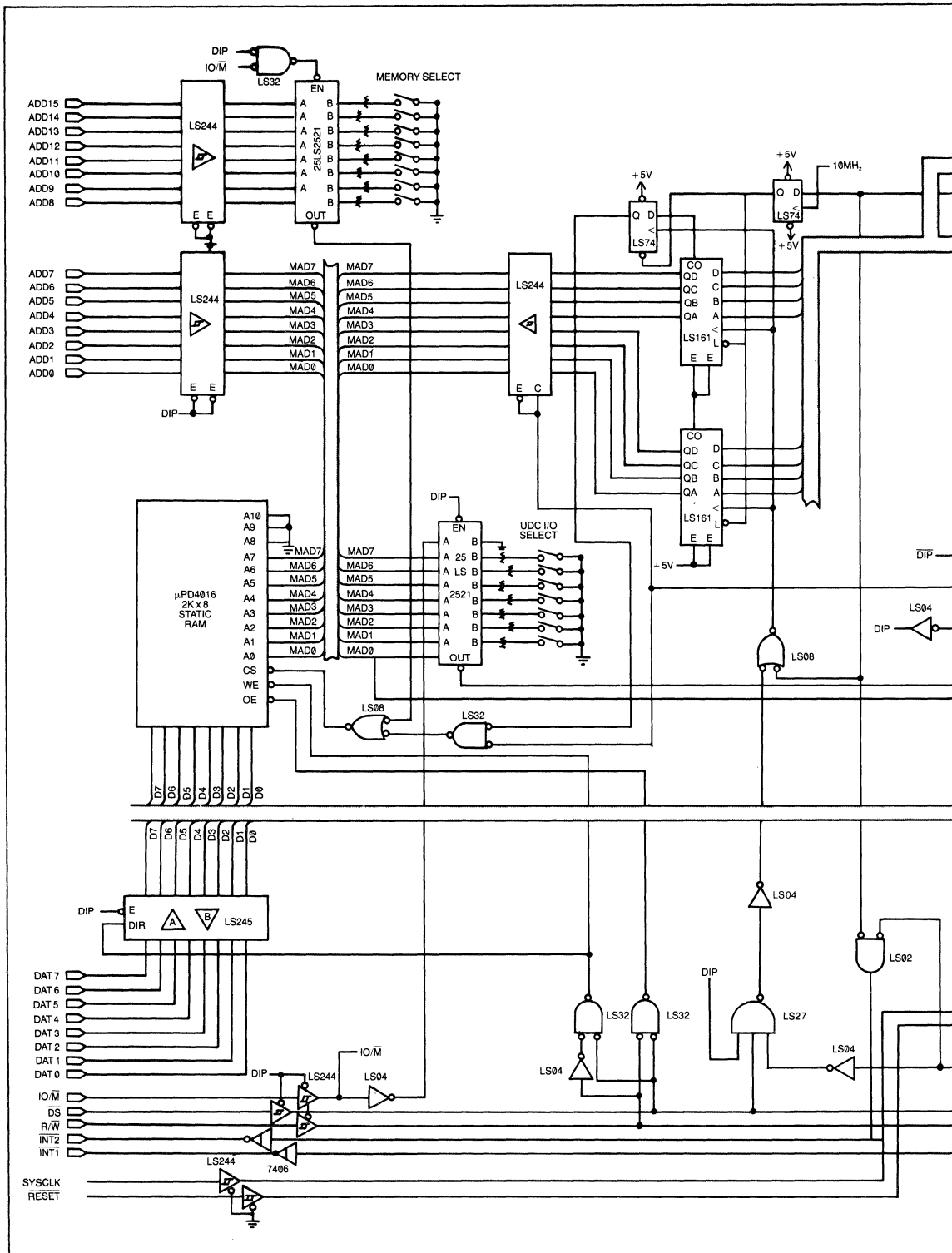


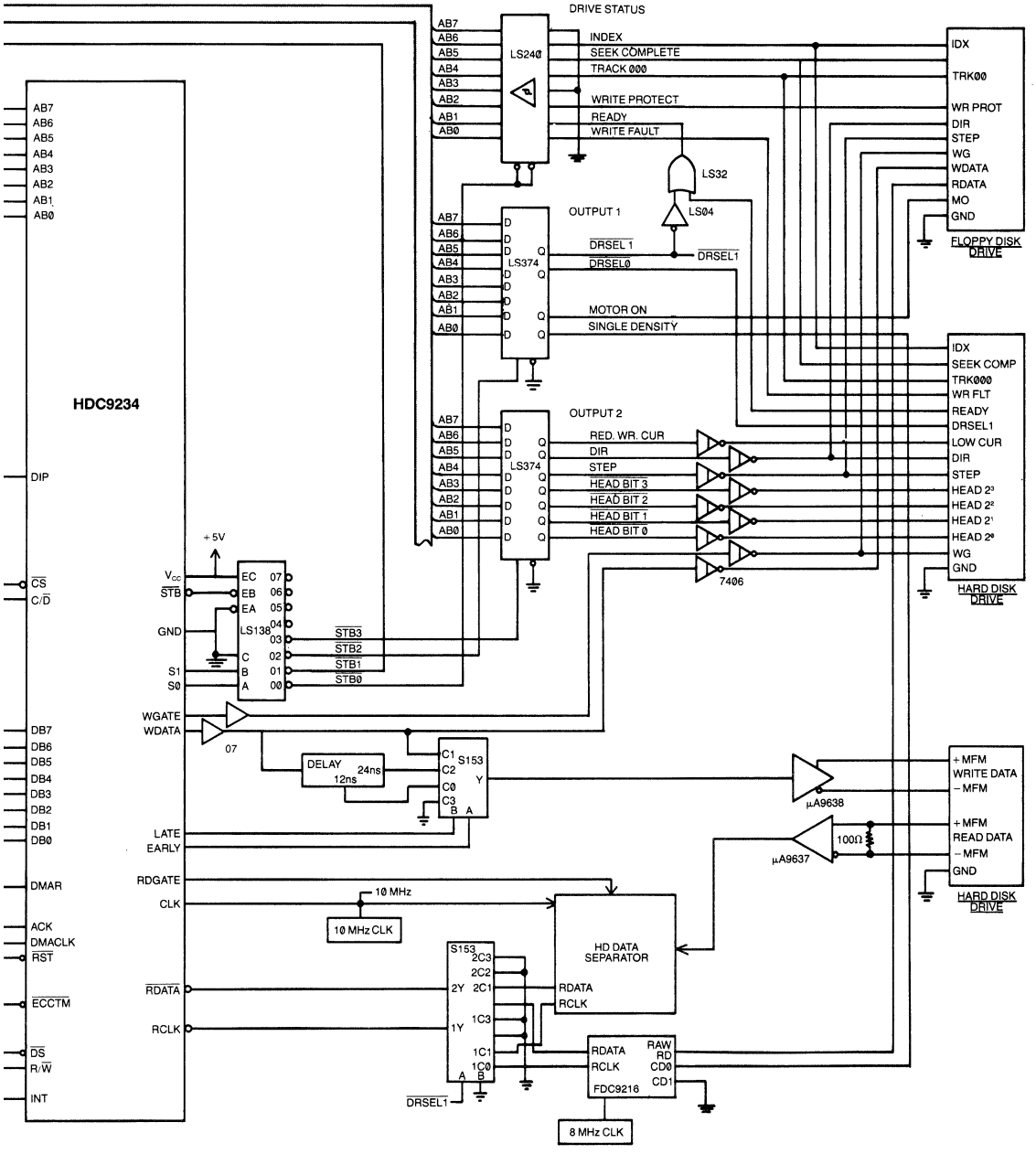
B. STREAMING TAPE DRIVE:

typically transfers 1 sector at a time as illustrated by the following flow chart:



Control of a streaming tape drive is similar to that of a start/stop drive. The tape is started at the beginning of the data transfer and stopped after the last block is written to the tape. The tape is not stopped in between blocks. The UDC will however turn the Write Gate sig-


DIP
IO/M
LS32
MEMORY SELECT
EN
ADD15
ADD14
ADD13
ADD12
ADD11
ADD10
ADD9
ADD8
LS244
25LS2521
OUT
+5V
10MHz
LS74
ADD7
ADD6
ADD5
ADD4
ADD3
ADD2
ADD1
ADD0
MAD7
MAD6
MAD5
MAD4
MAD3
MAD2
MAD1
MAD0
CO
QD
QC
QB
QA
LS161
UDC I/O SELECT
µPD4016
2K x 8
STATIC
RAM
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CS
WE
OE
LS08
LS32
LS04
LS02
LS27
LS245
DIR
DAT 7
DAT 6
DAT 5
DAT 4
DAT 3
DAT 2
DAT 1
DAT 0
DS
R/W
INT2
INT1
7406
SYSCLK
RESET


DRIVE STATUS
HDC9234
LS240
LS32
LS04
LS374
OUTPUT 1
OUTPUT 2
INDEX
SEEK COMPLETE
TRACK 000
WRITE PROTECT
READY
WRITE FAULT
DRSEL 1
DRSEL0
DRSEL1
MOTOR ON
SINGLE DENSITY
RED. WR. CUR
DIR
STEP
HEAD BIT 3
HEAD BIT 2
HEAD BIT 1
HEAD BIT 0
7406
IDX
TRK00
WR PROT
DIR
STEP
WG
WDATA
RDATA
MO
GND
FLOPPY DISK DRIVE
IDX
SEEK COMP
TRK000
WR FLT
READY
DRSEL1
LOW CUR
DIR
STEP
HEAD 2³
HEAD 2²
HEAD 2¹
HEAD 2⁰
WG
GND
HARD DISK DRIVE
+5V
LS138
STB3
STB2
STB1
STB0
WGATE
WDATA
DELAY 12ns 24ns
S153
LATE
EARLY
μA9638
μA9637
100Ω
+MFM WRITE DATA
−MFM
+MFM READ DATA
−MFM
GND
HARD DISK DRIVE
RDGATE
CLK
10 MHz
10 MHz CLK
HD DATA SEPARATOR
RDATA
RCLK
FDC9216
RAW RD
CD0
CD1
8 MHz CLK
DRSEL1

SECTION VII

nal on when it is writing data and off when it is not so that gaps will be written (with external hardware) on the tape between the data blocks.

5. BACK-UP READ. The data is read from the tape (in either start/stop or streamer mode) and buffered in memory. The disk track is then reconstructed from the data.

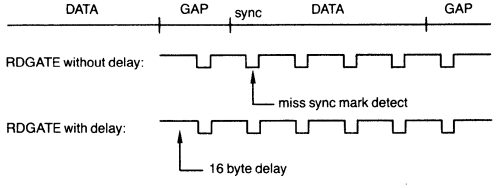
   The start/stop drive typically has a track (or half a track) of disk data stored as a block. It is therefore expedient to read in the data "block by block". When reading data from a streamer drive use can be made of the SECTOR COUNT register and a track's worth of data blocks may be read from the tape before generating the track on the disk.

   Tape motion control is similar to that described above except that the Write Enable Bit is off to inhibit writing to the tape. The UDC reads the tape until it detects a sync mark. After detecting a sync mark the UDC will transfer the data found on the tape to memory.

6. The search count is used when reading the tape. It specifies a maximum number of blocks of 128 bytes between adjacent data blocks. If the search count expires before sync is detected, the command is terminated.

   For example, if a search count of two is specified by loading the Desired Sector register with FD (hex), the UDC will search for 256 byte times before terminating the command. This will prevent the UDC from accidentally skipping a block. The search count is typically about the size of one block length. In the following figure, TM1 and TM2 are two tape marks and DB1, DB2, DB3 etc. are their associated Data Blocks:

7. 16 BYTE DELAY. Provision is made to shift the RDGATE pulse in the event that it coincides with the data block sync mark. If a tape cannot be read (sync is never detected) the tape can be re-read with the 16 byte delay enabled.



8. The DRIVE STATUS bits may be used by the tape drive if they are enabled (on the drive) by DRIVE SELECT 3. The ready change interrupt is especially handy for detecting start of tape (SOT) and end of tape (EOT) as a UDC command can be terminated by a change in state of the READY input.

9. The DATA FORMAT is as follows:

PRE	TMSYNC	TAPE MARK	POST GAP	PRE	DBSYNC	DATA BLOCK	POST GAP

   The Tape Mark sync mark (TMSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FE (Hex). The Data Block sync mark (DBSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FB (Hex). A1 (Hex) is encoded with the standard missing clock pattern.

   The sync mark is preceeded by a "preamble" consisting of bytes of 00 as per figure 2 of the UDC spec (this is required to synchronize the data separator when reading the tape). The Tape Mark and Data Block (including CRC or ECC bytes) are followed by a "postamble" consisting of one byte of 00.

   Note that the postamble is not included in the Floppy Disk formats. The GAP sizes are dependent on the type of drive (start/stop or streamer) and the specific mechanical tape drive specifications.

10. Use can be made of the Sector Count register when doing a "file" (versus a "mirror image") backup on a start/stop tape drive. Instead of transferring the entire disk track to the tape in one long block, the data is moved file by file.

    If, for example, it is desired to back up a file consisting of five 256 byte long Hard Disk sectors, a 2048 byte long Data Block would have to be used for an image backup (the Data Block size is specified as $2^n * 128$ restricting blocks to 128, 256, 512 etc.). This would result in a lot of wasted space on the tape.

    If file backup is used and the Sector Count is set to five, 256 byte long Data Blocks can be used. Gaps will be generated on the tape corresponding to the time required to get the data from the disk drive (corresponding to DMA delays and the disk interleave factor).

    The tape will not be stopped until the entire file is transferred. When using sector count, the UDC internal programming will create inter-block gaps of about 30 to 32 bytes on the tape in both single (FM) and double (MFM) density modes.

SYSTEM CONFIGURATION NOTES

A simplified UDC schematic is shown in Schematic 1. The following notes may be helpful in implementation of the UDC.

1. In systems using a private memory area, it is important to know when the buffer needs servicing from the host processor. A second interrupt signal (INT2) signals the processor that servicing is needed. INT2 is generated by externally ANDING the ECCTM signal with STB1 signal. (The STB1 signal is active when the UDC is outputing the DMA address data, and occurs when STB is active (low), S0 is active (high) and S1 is inactive (low)).

   This "interrupt" occurs only when the UDC needs the system processor to either read from or write to the buffer memory. When reading from the disk, the system processor should empty the memory buffer each time this signal becomes active. (If an ECC error is detected, and error correction is enabled, this signal will not become active until the UDC has attempted to correct the error.)

   When writing data to the disk, the system processor must fill the buffer each time this signal becomes active.

2. The DIP (DMA in Progress) signal is used to isolate the buffer memory from the main system memory. If 74LS244 and 74LS245 address buffers are used in the memory addressing circuits, then this signal should be used to enable or disable the address buffers, as required. This eliminates the possibility of memory contention problems.

3. Write precompensation (for floppy disks) is handled internally by the UDC. For hard disks, the LATE and EARLY signals are connected to a multiplexer which, in turn is connected to a 24 ns delay line. The EARLY and LATE signals will toggle in response to the data pattern being written. This will allow the data being written to the shifted ± 12 ns from the nominal 12 ns delay specified by hard disk manufacturers.

4. The interface to the hard disk drive data inputs and outputs requires RS-422 data tranceivers. Other disk drive interface circuits (including floppy disk data inputs and outputs) may be 74LS series devices.

5. Since the UDC uses its Aux Bus for multiple functions, the system designer must be able to determine which function is occuring on the Aux Bus at any given time. The S0 and S1 signals, when combined with STB signal are decoded (using a 74LS138 or equivalent) to provide STB0-3 signals.

   These generated signals and their respective functions are:

STB0	Drive Status Input Time Slot
STB1	External DMA Address Counters Time Slot
STB2	Output 1 Time Slot
STB3	Output 2 Time Slot

6. The clocks required by the UDC are not TTL-level compatible. Pullup resistors (typically 390 ohms) should be used with Schottky drivers to insure that the clock signals reach the proper Input (high) level, with acceptable rise and fall times.

7. The UDC features a built-in DMA controller that requires connection to external counters. These counters are configured so that they are incremented after each byte is transferred. (The UDC's internal DMA circuits transfer the starting memory address for each read or write operation.) 74LS161 Counters are typically used in this area.

8. The DMACLK input should be tied to the master system clock, through a bus buffer. It is important to remember that three DMACLK periods are required for each DMA transfer.

9. The system design may be simplified, and costs reduced, by using the FDC 9216B Floppy Disk Data Separator, to separate raw data from the floppy disk drive into RDATA and RCLK.

ERROR CHECKING AND CORRECTION CIRCUIT (ECC) OPERATING PRINCIPLES

The UDC will automatically detect and correct errors in the data read from the disk. Error checking may be done using industry standard CRC or ECC encoding. Error correction may be done using either internal or external ECC encoding. This section will explain ECC operation, as implemented on the UDC.

The UDC contains two 16-bit registers used by the CRC/ECC circuits. CRC logic uses only one of these registers, while the logic for ECC uses both registers, implementing a full 32-bit algorithm.

These registers may be preset to either one or zero, using the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION register. (This allows compatibility with existing disk controllers and external ECC chips.) Both ECC and CRC are calculated beginning with the sync mark of the address (CRC) or data (ECC) field.

CRC/ECC GENERATION

The UDC uses the following industry standard polynomials in computing the CRC and ECC check bytes:

CRC: $x^{16} + x^{12} + x^5 + 1$

ECC: $x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + ^1$

As the UDC writes data to the disk drive, it first passes this data thru the CRC (and, if enabled, ECC) registers. After all data has been written, the remaining two (CRC) or four (ECC) bytes remaining in these registers are written to the appropriate address or data field.

CRC/ECC CHECKING

When CRC or ECC checking is initiated, the internal CRC/ECC registers are set to either zero or one, as required by the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION REGISTER. Data read from the disk is simultaneously shifted thru the CRC/ECC registers, and transferred to external memory.

After the CRC or ECC check bytes have been shifted thru the CRC/ECC registers, the remainder in these registers should be zero, else an error has occurred in the address or data block.

If CRC or ECC (without correction) is enabled, automatic retry (if enabled) or command termination will occur. If internal ECC with automatic correction is enabled, the correction algorithm will be executed. If the internal ECC algorithm is unable to correct the error (in one attempt), then automatic retry (if enabled) or command termination will occur.

ECC CORRECTION

Error Correction consists of three distinct parts:

1. The CRC/ECC registers are normalized by shifting zeros thru the register. This sets up a data block which is 42,987 bits long, which corresponds to the "natural message length" of the generation polynomial. The actual number of zeros shifted through the registers depends on the difference between the natural message length of the generator polynomial and the actual length of the data block being checked. The longest data block that can be corrected (using the internal ECC algorithm) is 4K bytes.

2. The data input to the CRC/ECC registers is then disabled and the DMA counters are re-initialized to the starting address for this data block. The contents of the CRC/ECC registers are then "ring-shifted" until 21 consecutive zeros are detected. The remaining bits in the CRC/ECC registers compose the error syndrome. As the CRC/ECC registers are shifted, the UDC generates $\overline{DS}$ signals, causing the external DMA counters to be incremented. When the 21 consecutive zeros are detected, the DMA counters are pointing to the corrupt data.

   If the error syndrome is not found within the data block the error is judged to be uncorrectable and the correction algorithm is terminated. (The data block is the length of the data field in the sector and the 4 ECC bytes. A format with a sector size of 256 bytes would have a data block size of 260 bytes.)

3. When the error syndrome is detected, the UDC will enable its $\overline{ECCTM}$ output, read the next byte from memory, exclusive-or it with the first byte of the three byte error syndrome, disable the $\overline{ECCTM}$ output and write the corrected byte back to memory. The correction process is then repeated for the next two bytes in memory.

   When using internal ECC (with correction enabled), the $\overline{ECCTM}$ output is used by the external DMA counters to inhibit the counters from incrementing their addresses when correcting the erroneous bytes. When using external ECC, the $\overline{ECCTM}$ output goes active (low) when the UDC is requesting the ECC Check Bytes from the external ECC chip prior to writing them to the disk.

   After a correction is completed, the UDC will then attempt to read the next sector on the disk (if the SECTOR COUNT register is still greater than zero). Anytime ECC correction has been attempted, (even if unsuccessful), the CORRECTION ATTEMPTED bit in the CHIP STATUS register will be set.

The maximum time required for one ECC Correction Cycle (using the internal algorithm) is about equal to the time it takes to read 1 sector.

IMPLEMENTATION

Implementing ECC Correction consists of three steps:

1. Read with Auto-Correction disabled and Retry enabled.
2. When a sector with a hard ECC error is found, enable Read for one sector (sector count = 1) with Auto-Correction enabled and correct the error.
3. After the correction is completed, issue a new Read command with auto-correction disabled and retry disabled to transfer the balance of the data.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to +70 C
Shortage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any Pin, with respect to ground ..... +8 V
Negative Voltage on any Pin, with respect to ground ..... −0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

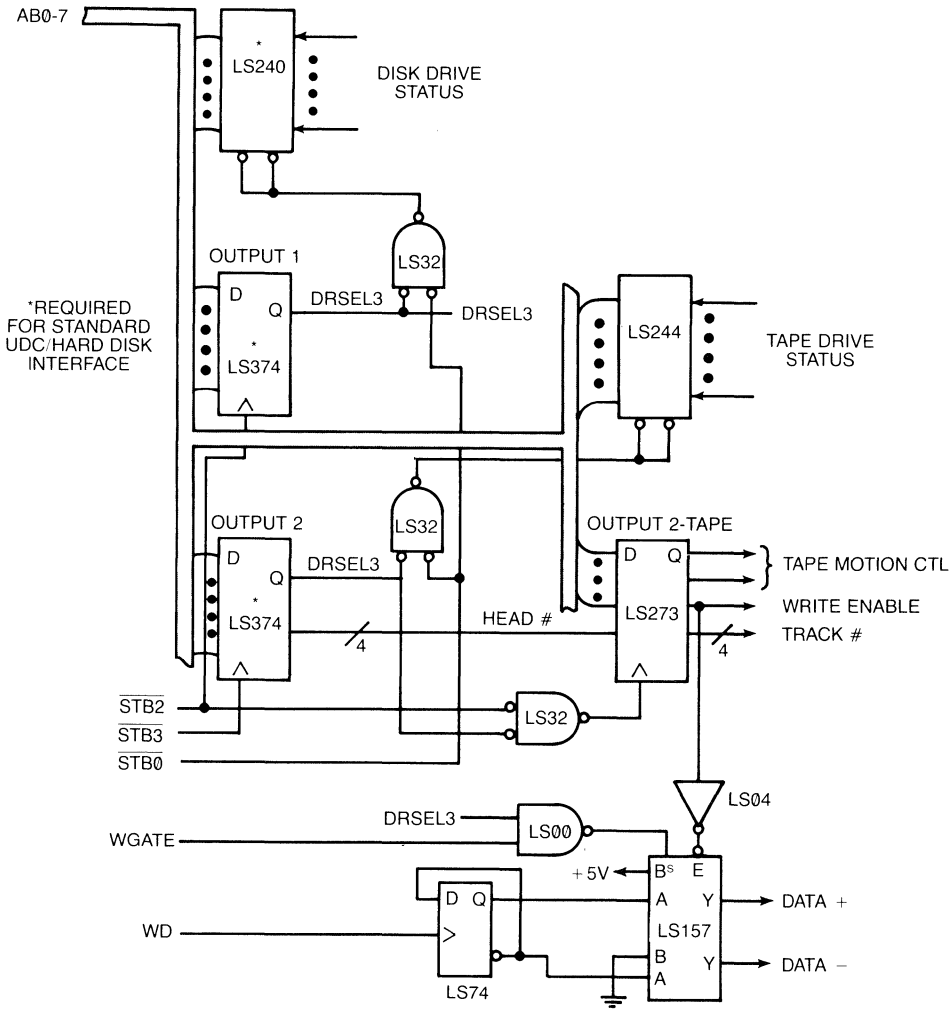
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Input Voltage					
Vi1 Low			0.8	V	
Vih1 High	2.0			V	all inputs except CLK
Vih2 High	4.2			V	CLK input
Output Voltage					
Vo11 Low			0.4	V	all outputs except WDATA,
Voh1 High	2.4			V	Early and Late. (Drive 1 TTL load into 50 pf)
Vo12 Low			0.4	V	WDATA, EARLY and LATE
Voh2 High	2.4			V	outputs. (Will drive 1 Schottky load into 15 pf.)
Input Leakage Current					
I1		10		uA	
Input Capacitance					
Cin		25		pf	
Power Supply Current		200			
Icc				ma	

AC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
PROCESSOR WRITE CYCLE						
C/$\overline{D}$, R/$\overline{W}$, $\overline{CS}$ Setup time to DS↓	T_{DSB}	110			ns	FIGURE 3
C/$\overline{D}$, R/$\overline{W}$, $\overline{CS}$ Hold time to DS↑	T_{DSB}	0			ns	
$\overline{DS}$ Pulse Width	T_{DSL}	150			ns	
$\overline{DS}$ Pulse High Time	T_{DSH}	850			ns	
Data Bus In Setup time to $\overline{DS}$↑	T_{DIB}	100			ns	
Data Bus In Hold time to $\overline{DS}$↑	T_{DIA}	0			ns	
PROCESSOR READ CYCLE						
Data Access time from $\overline{DS}$↓	T_{DOB}	75			ns	FIGURE 3
Data Hold time from $\overline{DS}$↑	T_{DOA}	10			ns	
UDC TO MEMORY TIMING (BUS MASTER) (based on 10 Mhz DMACLK Input)						
Write Setup time to $\overline{DS}$↓	T_{WB}	110			ns	FIGURE 4
Write Data Strobe Width	T_{WDS}	180			ns	
Write Hold time from $\overline{DS}$↑	T_{WA}	110			ns	
Data Strobe Falling Edge	T_{DSF}			15	ns	
Data Strobe Rising Edge	T_{DSR}			20	ns	
Write Data Valid before $\overline{DS}$↑	T_{WDB}			90	ns	
Write Data Hold time after $\overline{DS}$↑	T_{WDA}	10			ns	
Memory Access Time	T_W		200		ns	

SECTION VII

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Read Setup time to $\overline{DS}\downarrow$	T_{RB}	110			ns	FIGURE 4
Read Hold time after $\overline{DS}\uparrow$	T_{RA}	110			ns	
Read Data Strobe Pulse Width	T_{RDS}	180			ns	
Read Data Setup time to $\overline{DS}\uparrow$	T_{RDB}	50			ns	
Read Data Hold time from $\overline{DS}\uparrow$	T_{RDA}	0			ns	
DMACLK$\uparrow$ to $\overline{DS}\downarrow$	T_{DDD}			100	ns	
DMACLK$\uparrow$ to $\overline{DS}\uparrow$	T_{DDA}			100	ns	
S0, S1, AND $\overline{STB}$ TIMING						
$\overline{STB}$ Width	T_{SW}	800			ns	FIGURE 7
S0, S1 Hold time after $\overline{STB}\uparrow$	T_{SD}	100			ns	
Data In Setup time to $\overline{STB}\uparrow$	T_{DIS}	700			ns	
Data In Hold time after $\overline{STB}\uparrow$	T_{DIH}	0			ns	
S0, S1 Setup time to $\overline{STB}\downarrow$	T_{SST1}	100			ns	
Aux Bus Setup time to $\overline{STB}\downarrow$	T_{SST2}	100			ns	
Aux Bus Hold time after $\overline{STB}\uparrow$	T_{SST3}			100	ns	
INPUT CLOCK TIMING (10 MHz Input)						
Clock Rise Time	T_{RT}			10	ns	FIGURE 2
Clock Fall Time	T_{RF}			10	ns	
Clock Cycle High Time	T_{CH}	40			ns	
Clock Cycle Low Time	T_{CL}	40			ns	
Clock Cycle Time	T_{CYC}	95	100	105	ns	
PRECOMPENSATION TIMING						
Early, Late Setup time (Before WDATA$\uparrow$)	T_{PB}	0			ns	FIGURE 9
Early, Late Hold Time (after WDATA$\downarrow$)	T_{PB}	50			ns	
FLOPPY INPUT DATA TIMING						
Window Setup time to RDCLK	T_{FRB}	50			ns	FIGURE 10
Window Hold time from $\overline{RDDATA}\uparrow$	T_{FRA}	50			ns	
HARD DISK INPUT DATA TIMING						
Data Setup time to RDCLK$\downarrow$	T_{HRB}	60			ns	FIGURE 10
Data Hold time after RDCLK$\downarrow$	T_{HRA}	10			ns	
Clock Setup time to RDCLK$\uparrow$	T_{HCB}	60			ns	
Clock Hold time from RCLK$\uparrow$	T_{HCA}	10			ns	
ECCTIM TIMING						
$\overline{ECCTM}$ Setup to $\overline{DS}\downarrow$	T_{EDS}	50				FIGURE 10
$\overline{ECCTM}$ Hold after $\overline{DS}\uparrow$	T_{EDH}	100			ns	
RESET TIMING						
$\overline{RST}$ Pulse Width		1			µs	



SCHEMATIC 2: HDC9234 TAPE DRIVE INTERFACE CIRCUIT

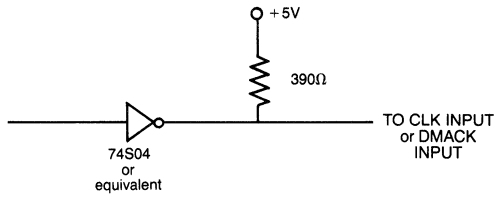


FIGURE #1 RECOMMENDED CLK DRIVER CIRCUIT

FIGURE 1: RECOMMENDED CLK/DMACLK INPUT

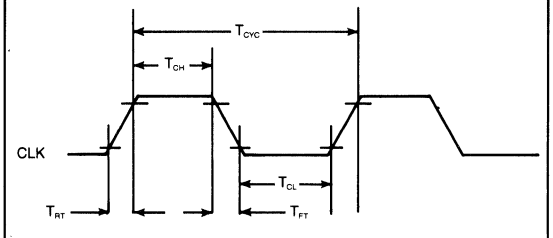


FIGURE 2: INPUT CLOCK TIMING (10MHz)

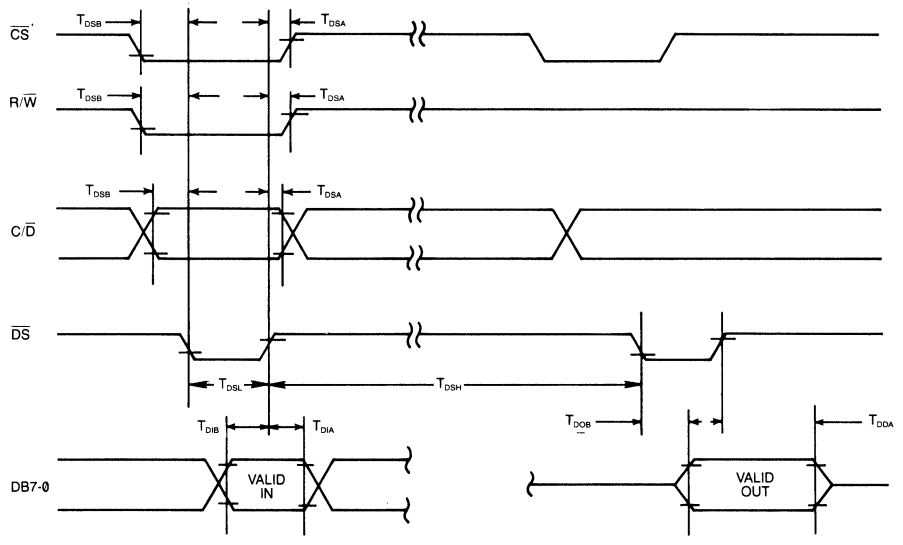


FIGURE 3

FIGURE 3: SYSTEM PROCESSOR TO UDC TIMING

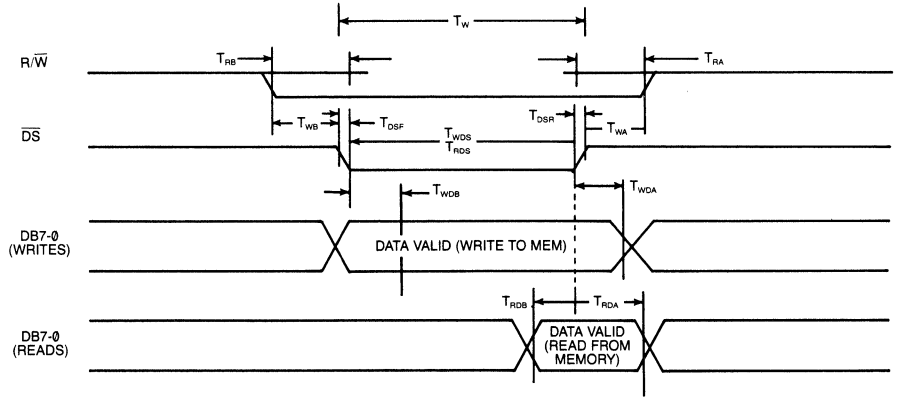


FIGURE 4: UDC TO MEMORY TIMING (BUS MASTER)

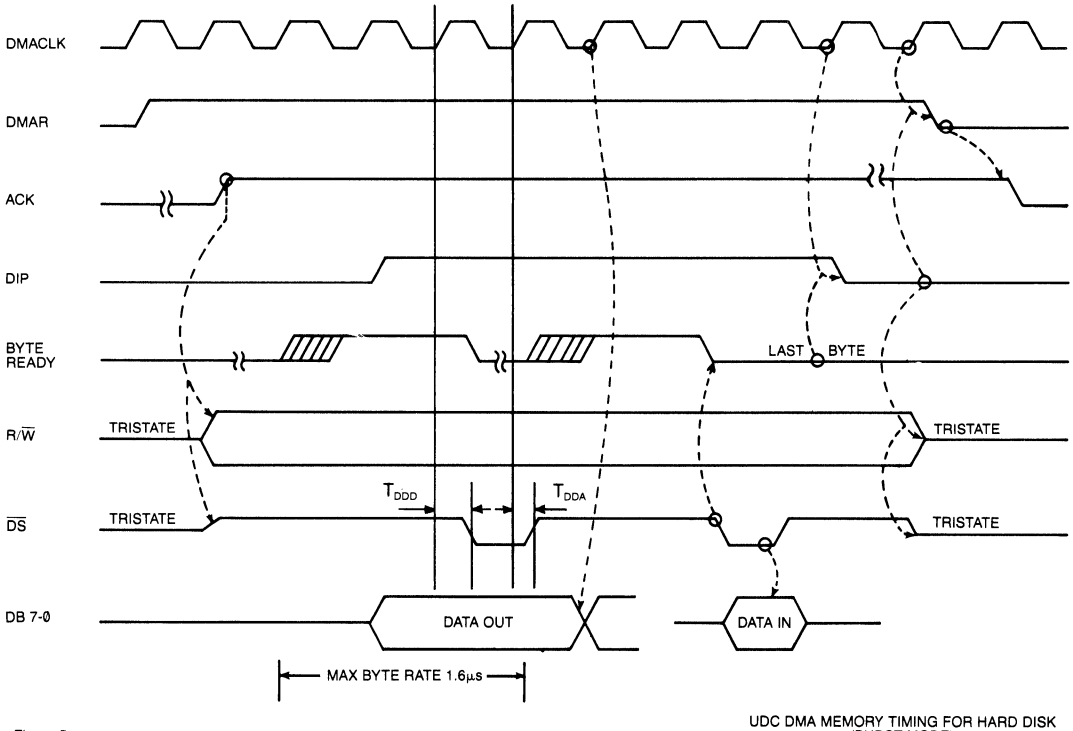
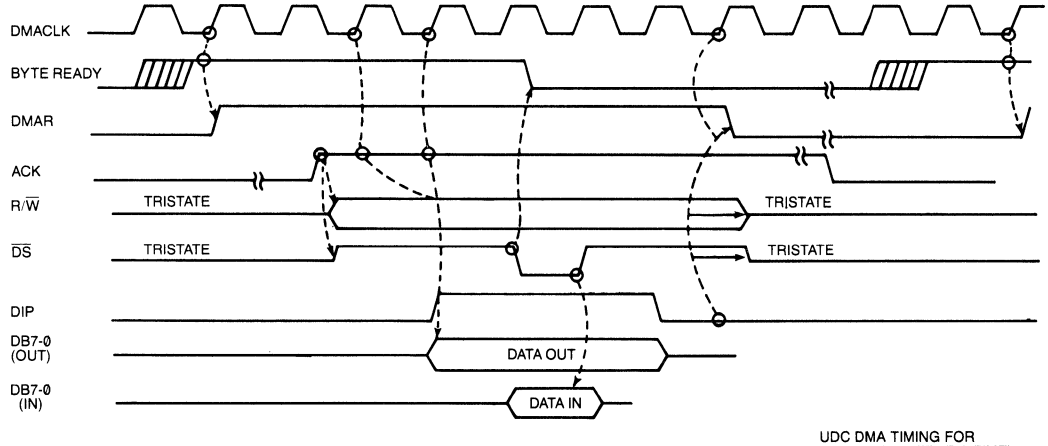


Figure 5

UDC DMA MEMORY TIMING FOR HARD DISK (BURST MODE)

FIGURE 5: UDC DMA MEMORY TIMING FOR HARD DISK (BURST MODE)



UDC DMA TIMING FOR FLOPPY DISK (1 BYTE AT A TIME)

FIGURE 6: UDC DMA TIMING FOR FLOPPY DISK (1 BYTE AT A TIME)

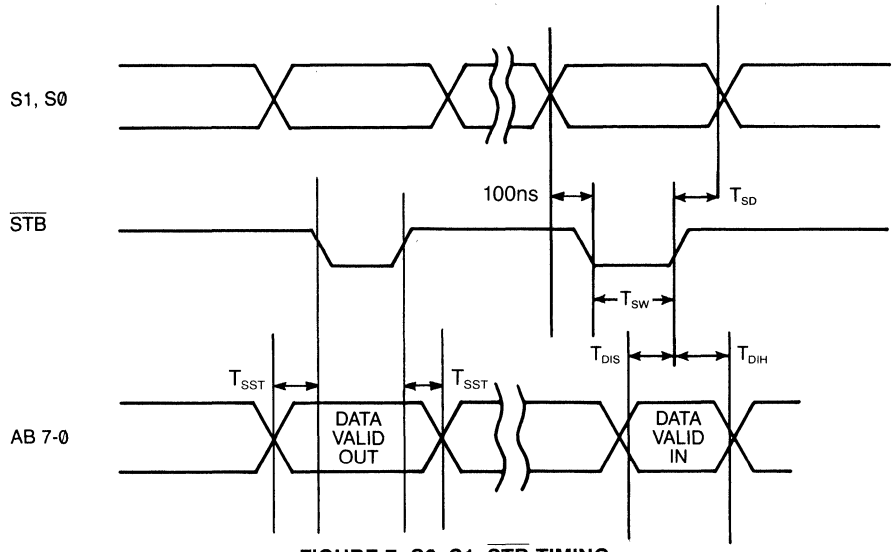


FIGURE 7: S0, S1, STB TIMING

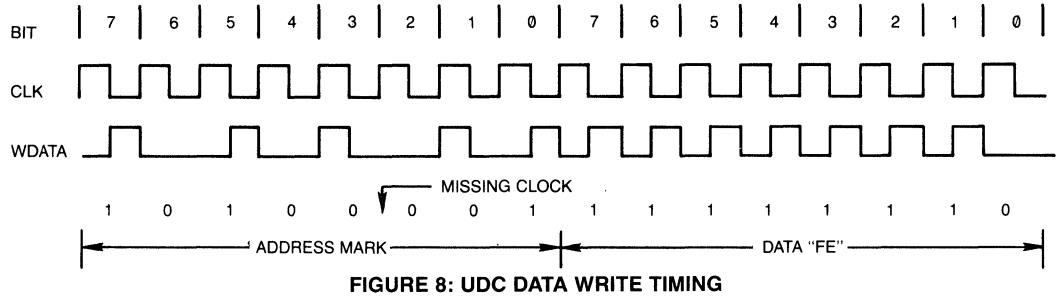
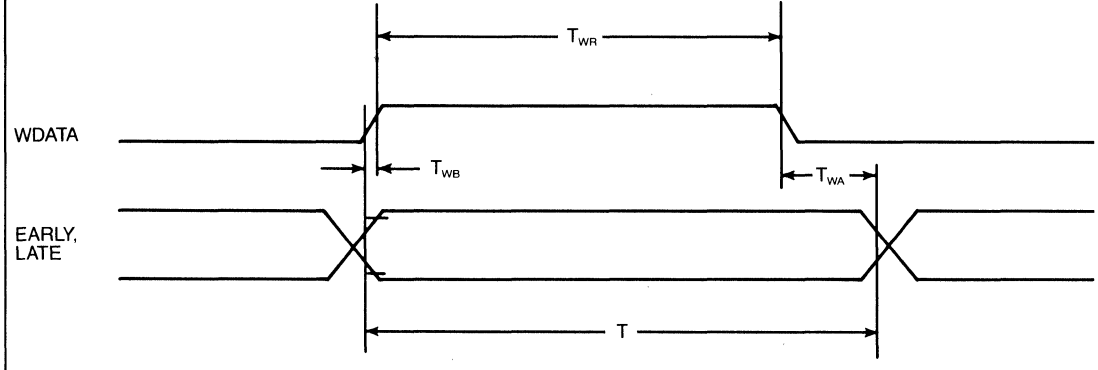
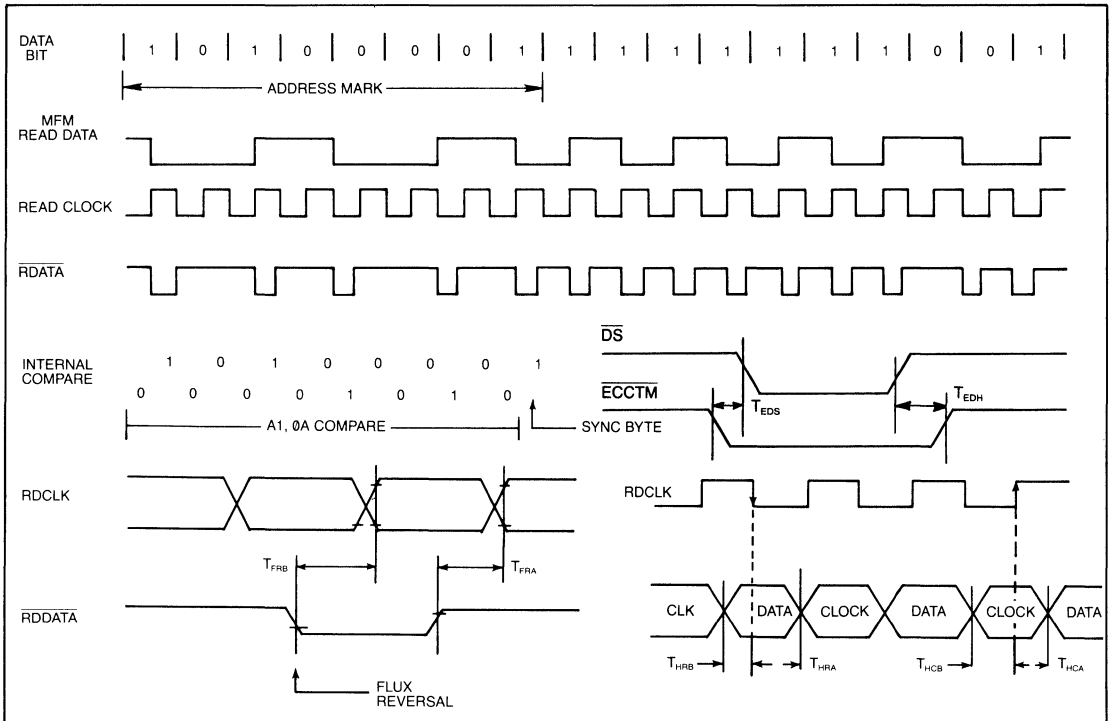


FIGURE 8: UDC DATA WRITE TIMING



DRIVE TYPE	T (typ)	T_{WR} (typ)
HARD DISK	200 NS	100 NS
8" MFM FLOPPY	2 µs	300 NS
8" FM FLOPPY	—	300 NS
5¼" MFM FLOPPY	4µs	300 NS
5¼" FM FLOPPY	—	300 NS

FIGURE 9: PRECOMPENSATION TIMING



FLOPPY INPUT DATA TIMING (HARD DISK BIT = 0)

HARD DISK INPUT DATA TIMING (HARD DISK BIT = 1)

FIGURE 10

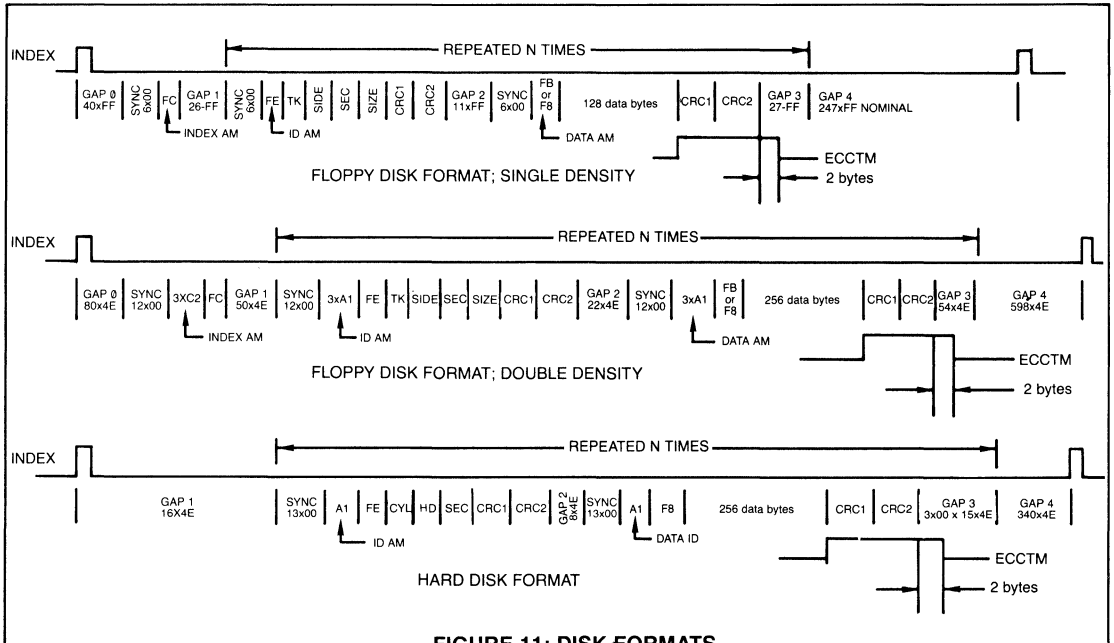


FIGURE 11: DISK FORMATS

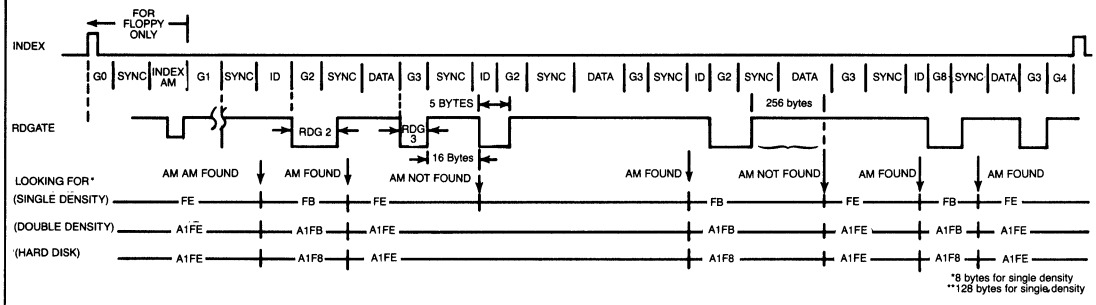


FIGURE 12A: RDGATE DURING DISK READ

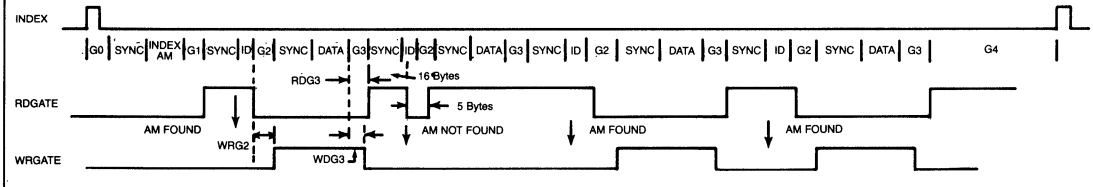


FIGURE 12B: RDGATE AND WRITE GATE TIMING

TYPICAL FORMAT PARAMETERS			
PARAMETER	HARD DISK***	SINGLE DEN. FLOPPY	DOUBLE DEN. FLOPPY
GAP Ø *	16	40	80
GAP 1 *	16	26	50
GAP 2 *	3	11	22
GAP 3 *	18**	27**	54**
SYNC SIZE *	13	6	12
SECTOR COUNT *	user selectable	user selectable	user selectable
SECT. SIZE MULT *	user selectable	user selectable	user selectable
RDG 1	16	73	NA
RDG 2	6	13	24
RDG 3	25	27	24
WDG 2	5	11	23
WDG 3	3	11	3

* = PARAMETER USED BY FORMAT COMMAND
** = CHANGES FOR DIFFERENT SECTOR SIZES
*** = 512 BYTES/SECTOR

TABLE 1: STANDARD FORMAT PARAMETERS

IBM® PC-AT HARD DISK FORMAT
REGISTER BIT DEFINITIONS

	7	6	5	4	3	2	1	0
DMA 7-0 (REGISTER 0)	(MSB)			LOW ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 15-8 (REGISTER 1)	(MSB)			MIDDLE ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 23-16 (REGISTER 2)	(MSB)			HIGH ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)			DESIRED SECTOR NUMBER				(LSB)
DESIRED HEAD (WRITE REGISTER 4)	ALWAYS 0	SECTOR SIZE		ALWAYS 0	DESIRED HEAD NUMBER (MSB)			(LSB)
DESIRED CYLINDER (REGISTER 5)	(MSB)			LOW ORDER BITS OF DESIRED CYLINDER				(LSB)
SECTOR COUNT (WRITE REGISTER 6)	(MSB)			NUMBER OF SECTORS TO BE OPERATED ON BY COMMAND				(LSB)
RETRY COUNT (REGISTER 7)	RETRY COUNT (1'S COMPLEMENT)				PROGRAMMABLE OUTPUTS			
MODE (REGISTER 8)	HARD DISK	CRC/ECC	ENABLE	SINGLE DENSITY	ALWAYS 0	STEP	RATE	SELECT
INTERRUPT/ COMMAND TERM. (REGISTER 9)	ALWAYS 1	ALWAYS 0	INTERRUPT ON DONE	FLAG DELETED DATA MARK	USER DEFINED FLAG	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT
DATA/DELAY (REGISTER A)	(MSB)			HEAD LOAD DELAY MULTIPLE IS LOADED INTO THIS REGISTER BEFORE SELECT COMMANDS				(LSB)
	(MSB)			DATA IS LOADED TO OR READ FROM THIS REGISTER FOR READ/WRITE/FORMAT COMMANDS DURING DATA TRANSFERS				(LSB)
	ALWAYS 0	ALWAYS 0	ACTUAL SECTOR SIZE		ALWAYS 0	ALWAYS 0	HIGH ORDER BITS OF DESIRED CYL NUMBER	
	BEFORE SEEK AND READ/WRITE COMMANDS WITH IMPLIED SEEK							
CURRENT HEAD (READ REGISTER 4)	BAD SECTOR FLAG	CURRENT SECTOR SIZE			ALWAYS 0	CURRENT HEAD NUMBER (MSB)		(LSB)
CURRENT CYLINDER (READ REGISTER 5)	(MSB)			LOW ORDER BITS OF CURRENT CYLINDER NUMBER				(LSB)
CURRENT IDENT (READ REGISTER 6)	IDENT BYTE FROM DISK FOR SEEK/READ ID COMMANDS ONLY							
CHIP STATUS (READ REGISTER 8)	RETRY REQUIRED	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	DELETED DATA MARK READ	SYNC ERROR	COMPARE ERROR	PRESENT DRIVE SELECTED	
DRIVE STATUS (READ REGISTER 9)	ECC ERROR	INDEX	SEEK COMPLETE	TRACK 00	USER DEFINED ACTIVE	WRITE PROTECT ACTIVE	DRIVE READY	WRITE FAULT
INTERRUPT STATUS (COMMAND READ)	INTERRUPT PENDING	DMA REQUEST	DONE	COMMAND TERMINATION CODE		READY CHANGE	OVERRUN/ UNDERRUN	BAD SECTOR

TABLE 2: REGISTER BIT MAPS

FLOPPY AND SMC HARD DISK FORMATS
REGISTER BIT DEFINITIONS

	7	6	5	4	3	2	1	0
DMA 7-0 (REGISTER 0)	(MSB)			LOW ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 15-8 (REGISTER 1)	(MSB)			MIDDLE ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 23-16 (REGISTER 2)	(MSB)			HIGH ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DESIRED SECTOR (WRITE REGISTER 3)	(MSB)			DESIRED SECTOR NUMBER				(LSB)
DESIRED HEAD (REGISTER 4)	ALWAYS Ø		HIGH ORDER BITS OF DESIRED CYLINDER (MSB)		DESIRED HEAD NUMBER (MSB)			(LSB)
DESIRED CYLINDER (REGISTER 5)	(MSB)			LOW ORDER BITS OF DESIRED CYLINDER				(LSB)
SECTOR COUNT (WRITE REGISTER 6)	(MSB)			NUMBER OF SECTORS TO BE OPERATED ON BY COMMAND				(LSB)
RETRY COUNT (REGISTER 7)	RETRY COUNT (1'S COMPLEMENT)				PROGRAMMABLE OUTPUTS			
MODE (REGISTER 8)	HARD DISK	CRC/ECC	ENABLE	SINGLE DENSITY	ALWAYS Ø	STEP	RATE	SELECT
INTERRUPT/ COMMAND TERM. (REGISTER 9)	CRC PRESET 1 = Set to 1 0 = Set to Ø	ALWAYS Ø	INTERRUPT ON DONE	FLAG DELETED DATA MARK	USER DEFINED FLAG	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT
DATA/DELAY (REGISTER A)	(MSB)			HEAD LOAD DELAY MULTIPLE IS LOADED INTO THIS REGISTER DATA IS LOADED TO OR READ FROM THIS REGISTER				(LSB)
CURRENT HEAD (READ REGISTER 4)	BAD SECTOR FLAG		HIGH ORDER BITS OF CURRENT CYLINDER (MSB)		CURRENT HEAD NUMBER (MSB)			(LSB)
CURRENT CYLINDER (READ REGISTER 5)	(MSB)			LOW ORDER BITS OF CURRENT CYLINDER NUMBER				(LSB)
CURRENT IDENT (READ REGISTER 6)	ALWAYS FE							
	FOR SEEK/READ ID COMMAND ONLY							
CHIP STATUS (READ REGISTER 8)	RETRY REQUIRED	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	DELETED DATA MARK READ	SYNC ERROR	COMPARE ERROR	PRESENT DRIVE SELECTED	
DRIVE STATUS (READ REGISTER 9)	ECC ERROR	INDEX	SEEK COMPLETE	TRACK ØØ	USER DEFINED ACTIVE	WRITE PROTECT ACTIVE	DRIVE READY	WRITE FAULT
INTERRUPT STATUS (COMMAND READ)	INTERRUPT PENDING	DMA REQUEST	DONE	COMMAND TERMINATION CODE		READY CHANGE	OVERRUN/ UNDERRUN	BAD SECTOR

TABLE 2: REGISTER BIT MAPS

HDC9234 WRITE REGISTERS (APPLIES DURING TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BUTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT) (1)						(LSB)
DESIRED HEAD (REGISTER 4)	0	0	0	0	TRK # BIT 3	TRK # BIT 2	TRK # BIT 1	TRK # BIT 0
DESIRED CYLINDER (REGISTER 5)	ECC TYPE				ALWAYS 1	DATA BLOCK SIZE		
SECTOR COUNT (REGISTER 6)	TAPE MARK BLOCK SIZE (IN 2'S COMPLEMENT + 1) (MODULO 256) (2)			OR	DATA BLOCK COUNT (IN 1'S COMPLEMENT) (3)			
RETRY COUNT (REGISTER 7)	1	1	1	1	USER DEFINED OUTPUTS			
MODE (REGISTER 8)	ALWAYS "Ø" FOR TAPE	CRC/ECC ENABLE CODE		SINGLE/ DOUBLE DENSITY	ALWAYS Ø	SYNC DELAY ENABLE	WRITE ENABLE	TAPE MARK ENABLE
INTERRUPT/ COMMAND TERMINATOR (REGISTER 9)	CRC PRESET	ALWAYS Ø	INTERRUPT ON DONE	ALWAYS 1	USER DEFINED	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT

NOTES: (1) The maximum search count is composed of:
130 byte inner loop (RDGATE high 128, 2 byte times)
times the number programmed (maximum of 33,150 byte times
(2) Tape mark operation
(3) Data block operation

TABLE 3–TAPE BACKUP REGISTER BIT MAPS

UDC READ REGISTERS (APPLIES TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BYTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT)						(LSB)
CURRENT HEAD (REGISTER 4)	X	X	X	X	X	X	X	X
CURRENT CYLINDER (REGISTER 5)	X	X	X	X	X	X	X	X
CHIP STATUS (REGISTER 6)	X	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	X	X	X	PRESENT DRIVE SELECTED	
DRIVE STATUS (REGISTER 7)	USER DEFINED (1)	USER DEFINED (2)	SEEK COMP	USER DEFINED (2)	USER DEFINED (1)	WRITE PROTECT	READY	WRITE FAULT
DATA (REGISTER 8)	READ DATA							
INTERRUPT STATUS (REGISTER 9)	INT PENDING	DMA REG	DONE	COMMAND TERMINATION CODE (3)		READY CHANGE	OVER/ UNDER RUN	X

NOTES: (1) Active level can generate interrupt.
(2) Active Level will not cause interrupt.
(3) Command termination bits set to:
11 for data transfer error
10 for sync error
00 for successful termination
X Don't care

TABLE 4: TAPE BACK UP REGISTER BIT MAPS

COMMAND BIT DEFINITIONS

	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0
DESELECT DRIVES	0	0	0	0	0	0	0	1
RESTORE DRIVE	0	0	0	0	0	0	1	1 = Buffered Seek 0 = Normal Seek
STEP IN 1 CYLINDER	0	0	0	0	0	1	0	1 = Buffered Seek 0 = Normal Seek
STEP OUT 1 CYLINDER	0	0	0	0	0	1	1	1 = Buffered Seek 0 = Normal Seek
POLL DRIVES	0	0	0	1	1 = Poll Drive 3 0 = Don't Poll	1 = Poll Drive 2 0 = Don't Poll	1 = Poll Drive 1 0 = Don't Poll	1 = Poll Drive 0 0 = Don't Poll
SELECT DRIVE	0	0	1	1 = Head Load Delay Enabled 0 = Delay Disabled	DRIVE TYPE		DRIVE UNIT SELECTED	
SET REGISTER POINTER	0	1	0	0	REGISTER		NUMBER	
SEEK/READ ID	0	1	0	1	0	Step Enable	Wait For Complete	Verify ID
READ SECTORS PHYSICAL	0	1	0	1	1	0	0	Enable Transfer
READ TRACK	0	1	0	1	1	0	1	1 = Transfer All 0 = Transfer ID
READ SECTORS LOGICAL	0	1	0	1	1	1	1 = Implied Seek Disabled 0 = Implied Seek Enabled	Enable Transfer
FORMAT TRACK	0	1	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS PHYSICAL	1	1 = Implied Seek Disabled 0 = Implied Seek Enabled	0	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS LOGICAL	1	1 = Implied Seek Disabled 0 = Implied Seek Enabled	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
TAPE BACKUP	0	0	0	0	1	WRITE:	PRECOMPENSATION VALUE	
						READ:	0 0	Transfer Enable

TABLE 5: COMMAND WORD BIT MAPS

IBM® FM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	track number							
HEAD	side number							
SECTOR	sector number							
SECTOR SIZE	X	X	X	X	X	sector size (3 bits)		

HARD DISK FORMAT:
IBM PC-AT FORMAT (512 BYTES)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT	Ident Byte							
CYLINDER	cylinder number (8 LSB's)							
HEAD	0	sctr bit 1	sctr bit 0	trk# bit 8	hd# bit 3	hd# bit 2	hd# bit 1	hd# bit 0
SECTOR	sector number							

HARD DISK FORMAT:
(USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT	Ident Byte							
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl# bit 10	cyl# bit 9	cyl# bit 8	hd# bit 3	hd# bit 2	hd# bit 1	hd# bit 0
SECTOR	sector number							
SECTOR SIZE	ECC type				X	sector size (3 bits)		

DISK FORMATS

TABLE 6

(continued)

SECTOR SIZE FIELD BITS

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM® MFM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IDENT			Ident Byte					
CYLINDER			track number					
HEAD			side number					
SECTOR			sector number					
SECTOR SIZE	X	X	X	X	X	sector size (3 bits)		

DISK FORMATS

TABLE 6

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

MSD7262
PRELIMINARY

Enhanced Small Device Interface Controller

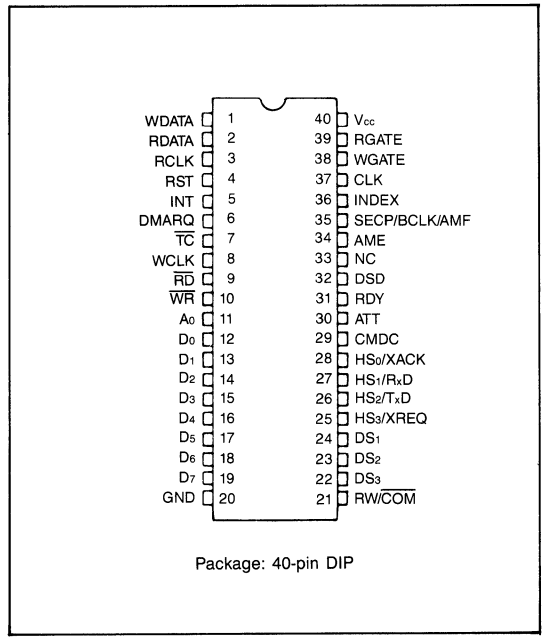
FEATURES

- ☐ Controls ESDI serial mode disks
- ☐ Controls up to seven disk drives
- ☐ Programmable soft and hard sector formats
- ☐ 18-MHz data transfer rate
- ☐ Multi-sector, -track, and -cylinder transfer capability
- ☐ Implied seek and parallel seek capability
- ☐ High Level Commands, Including:

Check	Read Diagnostic
Chip Reset	Read ID
Clear Command End Bit	Recalibrate
Clear Data FIFO	Scan
Detect Error	Send
Format Sector	Send Extended
Format Track	Sense Seek Status
Get Internal Information	Sense Unit Status
Group Assign	Specify1
Logical Seek	Specify2
Mask SRQ Interrupt	Verify Data
Physical Seek	Verify ID
Read Data	Write Data

- ☐ CRC error detection
- ☐ ECC error detection and correction
- ☐ Single +5 volt supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION

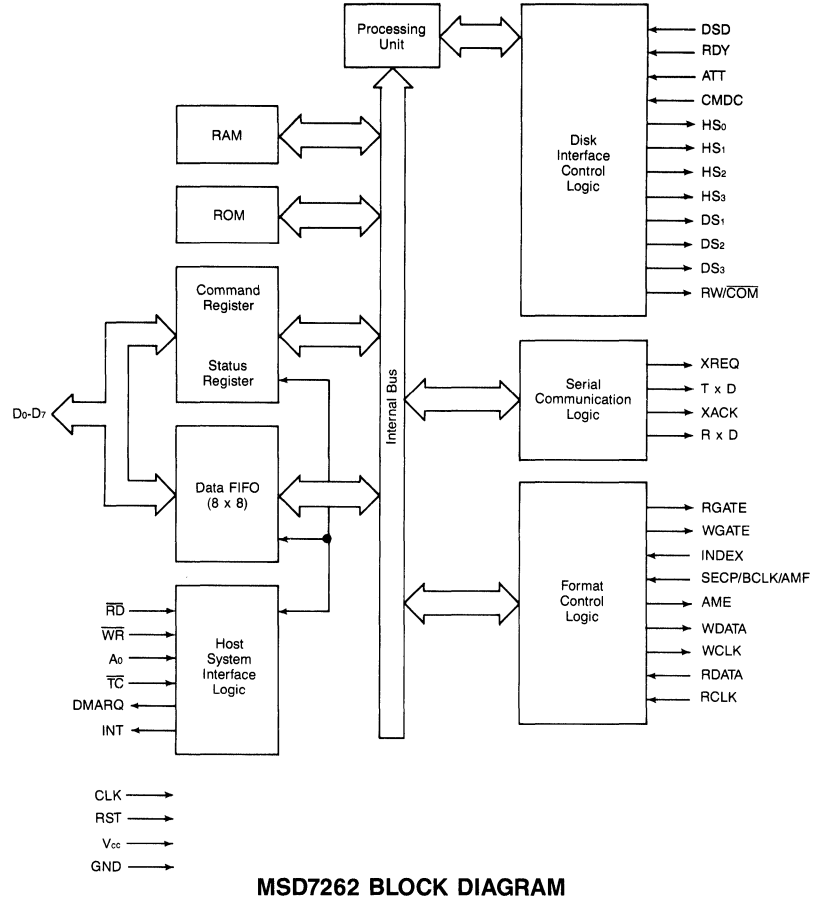


Package: 40-pin DIP

SECTION VII

GENERAL DESCRIPTION

The MSD7262 is a highly-integrated, single-chip controller for ESDI Winchester Disks. While conforming to the complete revision E of the ESDI specification, this device executes 22 high-level commands that provide flexibility and ease of usage. The MSD7262 is based on the proven HDC7261/HDC7260 architecture but adapted to the special requirements of this disk interface. It eliminates numerous ICs and gives complete access to all of the features implemented by the ESDI disk drive manufacturers.



MSD7262 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Write Data	WDATA	NRZ write data output to ESDI drive
2	Read Data	RDATA	NRZ read data input from ESDI drive
3	Read Clock	RCLK	Read/reference clock input from ESDI drive
4	Reset	RST	System reset input
5	Interrupt	INT	Interrupt request output
6	DMA Request	DMARQ	DMA request output
7	Terminal Count	$\overline{TC}$	Terminal count input from DMAC
8	Write Clock	WCLK	Write clock output to ESDI drive
9	Read	$\overline{RD}$	Read control input signal from host computer
10	Write	$\overline{WR}$	Write control input signal from host computer
11	Line Address 0	A_0	Address select input from host computer
12-19	Data Bus	D_0-D_7	Data bus from host computer
20	Ground	GND	System ground
21	Read Write/Command	RW/$\overline{COM}$	This output specifies the status of pins 25-28

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
22-24	Drive Select	DS_3-DS_1	Drive select outputs to ESDI drive
25 26 27 28	Head Select	HS_3/XREQ HS_2/TxD HS_1/RxD HS_0/XACK	If RW/COM = 1: head select (HS) outputs to ESDI drive. If RW/COM = 0 for serial data transfer to ESDI drive: transfer request (XREQ) output, transmit data (TxD) output, receive data (RxD) input, and transfer acknowledge (XACK) input.
29	Command Complete	CMDC	Command complete input from ESDI drive
30	Attention	ATT	Attention input from ESDI drive
31	Ready	RDY	Ready input from ESDI drive
32	Drive Select	DSD	Drive selected input from ESDI drive
33	No Connect	NC	Not connected; leave open
34	Address Mark Enable	AME	Address mark enable output from ESDI drive
35	Selector Pulse/ Byte Clock/ Address Mark	SECP/BCLK/ AMF	Sector pulse or byte clock or address mark found; input from ESDI drive (mutually exclusive)
36	Index	INDEX	Index detected input from ESDI drive
37	Clock	CLK	System clock input to MSD7262
38	Write Gate	WGATE	Write gate output to ESDI drive
39	Read Gate	RGATE	Read gate output to ESDI drive
40	Power Supply	V_{CC}	+5 V (Typical) input

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

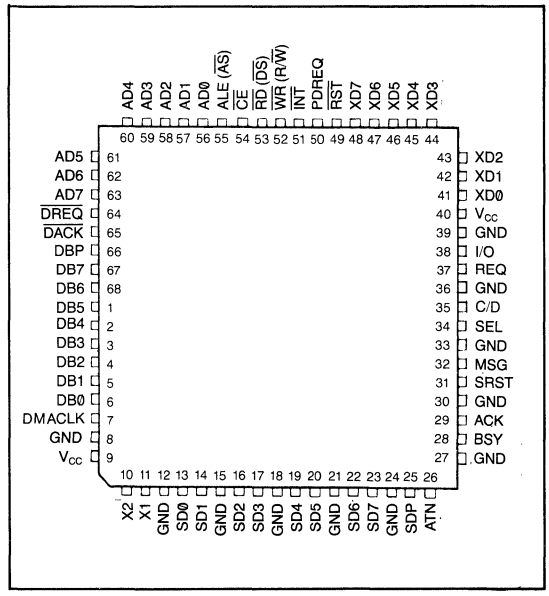
MSD95C00
PRELIMINARY

Small Computer System Interface (SCSI) Controller-SCSIC

FEATURES:

- ☐ Initiator and Target Operation.
- ☐ 5 MByte/Sec Synchronous and 3 MByte/Sec Asynchronous Data Transfers.
- ☐ Automatic Arbitration and (Re) Selection.
- ☐ Supports both Arbitration and Non-arbitration Applications.
- ☐ Separate Busses for Data and Microprocessor.
- ☐ Separate DMA for Processor and Data Channels.
- ☐ Burst Mode DMA Transfers on Data Bus.
- ☐ Programmed I/O or DMA Transfers on Processor Data Bus.
- ☐ Internal Twelve Byte Buffer.
- ☐ Internal 24-bit Byte Transfer Counter.
- ☐ Built-in 48ma High-Current SCSI Bus Drivers.
- ☐ Thru-Parity.
- ☐ User Selectable Selection Timeout.
- ☐ Eight Bit Bi-Directional General Purpose I/O Port.
- ☐ Bus Architecture allows caching.
- ☐ Compatible with MSD 95C02 Storage Controller.
- ☐ Low Power CMOS.
- ☐ TTL compatible inputs and outputs.

PIN CONFIGURATION



SECTION VII

GENERAL DESCRIPTION

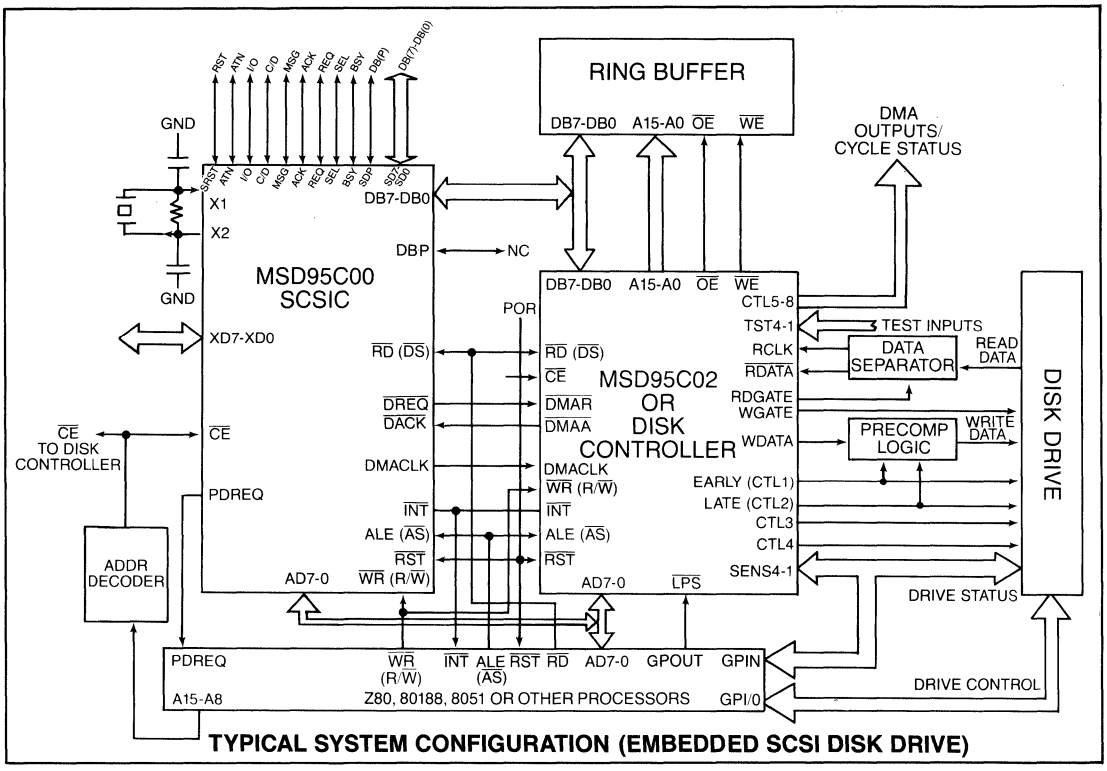
The MSD95C00 SCSI Controller is capable of negotiating for and supporting data transfer on an ANSI SCSI (Small Computer System Interface) compatible computer bus. The internal twelve byte buffer makes this device suitable for both peripheral and host adapter applications in systems that support both Asynchronous and Synchronous data transfer modes.

The MSD95C00 includes circuitry that automatically arbitrates for the SCSI bus and selects or reselects another device. This feature combined with the size of the internal buffer allows a selected Target device to transfer an entire command from an Initiator with a minimum of host processor intervention on either side.

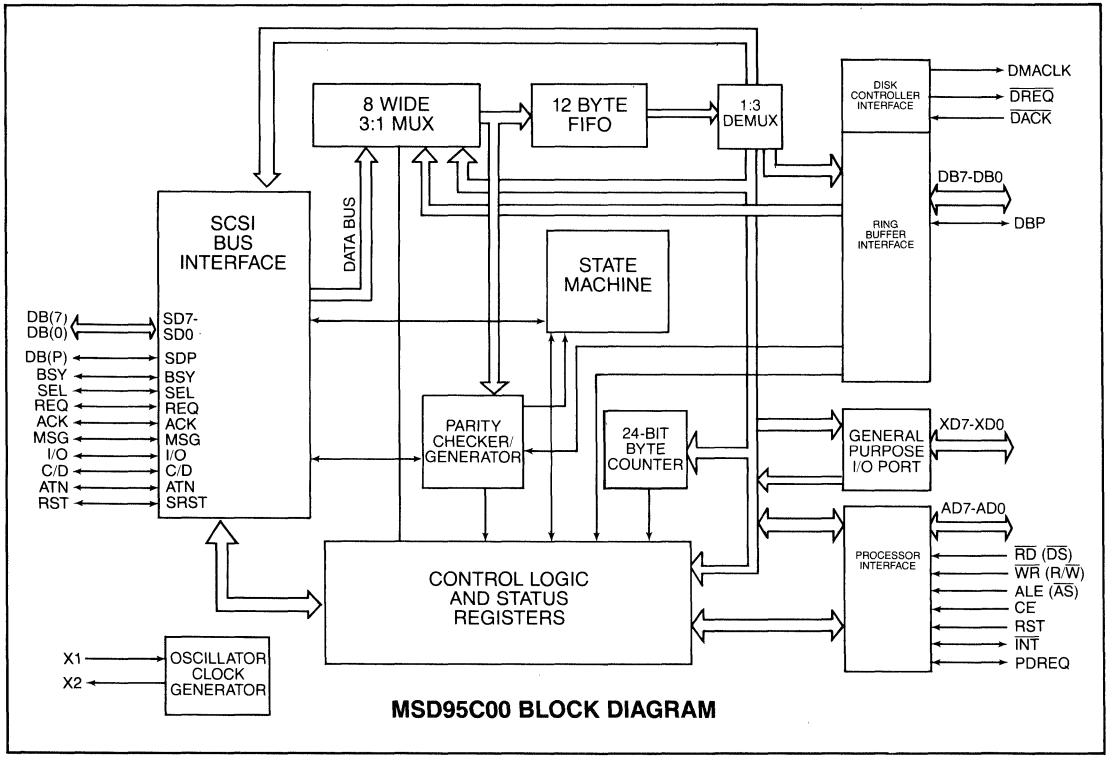
The MSD95C00 has three independent busses: one that connects to the local microprocessor (the System bus), one that connects to the data ring buffer (the Data bus) and the SCSI bus. Information transfers can be made between the SCSI bus and either of the other two busses. The Data bus supports burst mode DMA transfers and the System bus supports both programmed I/O and DMA transfers.

Accesses to the ring buffer are controlled via a DMA request/acknowledge handshake. Local processor transfers, as well as transfers to logical nodes (e.g., media transfers), are completely asynchronous with respect to transfers across the SCSI bus.

The MSD95C00 can be combined with the flexible MSD95C02 Storage Controller, a standard microprocessor, and off-the-shelf static RAM to support embedded SCSI peripheral applications with minimum component count and synchronous SCSI speeds of up to 5 megabytes per second.



TYPICAL SYSTEM CONFIGURATION (EMBEDDED SCSI DISK DRIVE)



MSD95C00 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
1-6 67, 68	RING BUFFER DATA BUS	DB0-DB7	I/O	These pins are the eight bi-directional data signals to/from the RING Buffer.
7	DMA CLOCK	DMACLK	O	This output is used by the DMA controller to time data transfers.
8, 12, 15, 18, 21 24, 27, 30, 33, 36, 39	GROUND	GND	P	Ground connection.
9, 40	POWER	V_{CC}	P	+5V Power connection.
11	CRYSTAL INPUT	X1	I	A 20 MHz. (max) crystal is connected to this output. Alternately a TTL clock may be the input to this pin.
10	CRYSTAL OUTPUT	X2	O	A 20 MHz. (max) crystal is connected to this output. Alternately, if a TTL is connected to X1, this input is left floating.
13, 14, 16, 17, 19, 20, 22, 23	SCSI DATA BUS	SD0-SD7	I/O	These pins are the eight bi-directional SCSI data signals to/from the SCSI bus. Their direction depends on the state of the I/O signal, except during arbitration.
25	SCSI PARITY	SDP	I/O	This pin is the bi-directional PARITY signal to/from the SCSI bus. Its direction depends on the state of the I/O signal.
26	ATTENTION	ATN	I/O	This pin is the bi-directional ATTENTION signal to/from the SCSI bus. It is an output when the controller is programmed as an initiator and an input when programmed as a target.
28	BUSY	BSY	I/O	This pin is the bi-directional BUSY signal to/from the SCSI bus.
29	ACKNOWLEDGE	ACK	I/O	This pin is the bi-directional ACKNOWLEDGE signal to/from the SCSI bus. It is an output when the controller is programmed as an initiator and an input when programmed as a target.
31	SCSI BUS RESET	SRST	I/O	A low on this bi-directional SCSI bus indicates an SCSI bus Reset.
32	MESSAGE	MSG	I/O	This pin is the bi-directional MESSAGE signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
34	SELECT	SEL	I/O	This pin is the bi-directional SELECT signal to/from the SCSI bus.
35	COMMAND/DATA	C/D	I/O	This pin is the bi-directional COMMAND/DATA signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
37	REQUEST	REQ	I/O	This pin is the bi-directional REQUEST signal to/from the SCSI bus. It is an input when the controller is programmed as an initiator and an output when programmed as a target.
38	INPUT/OUTPUT	I/O	I/O	This pin is the bi-directional INPUT/OUTPUT signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
41-48	BIDIRECTIONAL EXTERNAL DATA BUS	XD0-XD7	I/O	These pins are open drain general purpose I/O bus with internal 1K pullups.
49	$\overline{\text{RESET}}$	$\overline{\text{RST}}$	I	This active low input causes the MSD95C00 to reset to an initial state: All SCSI signals are deasserted. $\overline{\text{DREQ}}$ is inactive high. PDREQ is inactive low. $\overline{\text{INT}}$ is inactive high. AD7-0 are inputs. DB7-0 are inputs. Refer to individual register descriptions for the reset state of each register.

DESCRIPTION OF PIN FUNCTIONS

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
50	PROCESSOR DMA REQUEST	PDREQ	O	Output active high when data byte transfer to/from Processor RAM is required.
51	$\overline{\text{INTERRUPT}}$	$\overline{\text{INT}}$	O	This output is the interrupt signal to the local processor. This output is active low open drain and has an internal pullup.
52	$\overline{\text{WRITE STROBE}}$ ($\overline{\text{READ/WRITE}}$)	$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)	I	When the SCSIC is configured for ALE, this active low strobe is used to latch write data from the AD7-0 bus into the SCSIC. When the SCSIC is configured for $\overline{\text{AS}}$, the R/$\overline{\text{W}}$ input is used to qualify the $\overline{\text{DS}}$ for a read or write cycle.
53	$\overline{\text{READ STROBE}}$ ($\overline{\text{DATA STROBE}}$)	$\overline{\text{RD}}$ ($\overline{\text{DS}}$)	I	When the SCSIC is configured for ALE, this active low strobe is used to enable read data from the SCSIC onto the AD7-0 bus. When the SCSIC is configured for $\overline{\text{AS}}$, this active low signal is used to strobe data into or out of the SCSIC.
54	$\overline{\text{CHIP ENABLE}}$	$\overline{\text{CE}}$	I	This input, when low, enables the SCSIC's registers for reading and writing.
55	ADDRESS LATCH ENABLE ($\overline{\text{ADDRESS STROBE}}$)	ALE ($\overline{\text{AS}}$)	I	This signal is active when address data is valid on the AD7-0 bus. The local processor must read a SCSIC register to configure the chip for ALE or $\overline{\text{AS}}$.
56-63	LOCAL PROCESSOR ADDRESS/DATA BUS	AD0-AD7	I/O	These eight signals are the multiplexed address/ data bus to/from the local processor.
64	$\overline{\text{DMA REQUEST}}$	$\overline{\text{DREQ}}$	O	This active low output is used to request a DMA transfer between the SCSIC and its logical node across the RING Buffer data bus.
65	$\overline{\text{DMA}}$ $\overline{\text{ACKNOWLEDGE}}$	$\overline{\text{DACK}}$	I	This active low input is used to strobe data from the RING Buffer data bus during transfers between the SCSIC and its logical node.
66	SYSTEM DATA BUS PARITY	DBP	I/O	This pin is the parity bit for the RING Buffer Data Bus.

SYSTEM OPERATION

SCSI initiators and targets communicate using a protocol based on eight distinct phases. These phases are used to describe changes to the various conditions of the control lines and the data bus lines. In one possible order of execution, the phases of SCSI include:

BUS FREE phase: No signal lines are being driven by any target or initiator.

ARBITRATION phase: Arbitration is an optional phase where the initiator, or target if reselection is supported, tries to gain access to the bus by issuing its SCSI ID on the data bus. The initiator with the highest SCSI ID (closest to bit 7) wins the bus.

SELECTION phase or RESELECTION phase:

SELECTION phase: The selection phase allows the initiator to select a target for a given function (e.g., READ or WRITE command). NOTE: Once the target has been selected, it controls the bus until the end of MESSAGE phase.

RESELECTION phase: An optional phase that is the same as the selection phase, except that a target becomes an arbitrator during the arbitration phase. This phase is used when a target prematurely disconnects from an initiator, leaving a previous command unfinished.

MESSAGE phases: There are two MESSAGE phases (MESSAGE IN and MESSAGE OUT) used to provide for other communication between the initiator and the target. This phase allows for single byte messages such as COMMAND COMPLETE or multiple byte messages such as establishing data path management.

COMMAND phase: Allows the target to request a command from the initiator. The command might be to read data, write data, format the disk, etc. A command consists of several bytes called the COMMAND DESCRIPTOR BLOCK.

DATA phase: There are two data phases, the DATA IN phase and the DATA OUT phase. For the DATA IN phase, the Target requests that data be sent from the Target to initiator. The DATA OUT phase transfers data from the initiator to Target.

STATUS phase: The STATUS phase allows the target to send a byte of status to the initiator. Additional status can be requested with another command.

Automatic Selection And Reselection

This section describes how an Initiator selects a Target, a Target reselects an Initiator and a Target or Initiator becomes selected or reselected.

SELECTION AND RESELECTION

The Arbitration, Selection and Reselection phases are controlled by a state machine. When the MSD95C00 detects the SCSI Bus Free phase, it will perform the Arbitration, Selection or Reselection sequence required.

Issuing the Select command to the MSD95C00 will cause the internal Attempt Selection (ATMTSEL) latch to be set. The Destination ID must be loaded prior to issuing the Select command. Command execution will then be dependent on the settings of the Initiator/Target and Arbitration Enable/ Disable bits in the Mode register:

INIT/TARG	ARBITRATION ENABLE	Effect of Select Command
0	0	Illegal Condition
0	1	Initiate Arbitration for SCSI bus and Reselect Initiator when Arbitration won
1	0	Select Target without Arbitration
1	1	Initiate Arbitration for SCSI bus and Select Target when Arbitration won

In either case, the SCSIC will not begin the Arbitration or Selection phases until detection of Bus Free. The SCSIC will then either enter the Arbitration phase or go directly to the Selection or Reselection phase.

If it enters the Arbitration phase, the SCSIC will attempt to gain control of the SCSI bus. Following Arbitration, if it won the bus, the SCSIC will start the Selection or Reselection phase or if it lost the bus, begin looking for Bus Free phase.

BEING SELECTED OR RESELECTED

If enabled, the SCSIC may be Selected or Reselected by another SCSI device (depending on whether it is programmed as a Target or Initiator).

ENA RESEL	ENA SEL	Selection/Reselection
0	0	Device may not be selected or reselected
0	1	Device may be selected but not reselected
1	0	Device may be reselected but not selected
1	1	Device may be selected or reselected

The SCSIC will reset the ATMTSEL latch if 1) it detects that it is being selected, the selection is good and Selection is enabled or 2) it is being Reselected, the reselection is good and Reselection is enabled. For example, in the case in which the SCSIC attempted Arbitration (when ATMTSEL was set), lost Arbitration and was itself selected, the ATMTSEL latch will be reset. The ATMTSEL bit is also reset when the SCSIC wins Arbitration and completes Selection or Reselection either successfully or unsuccessfully. A Selection or Reselection is good if there are no more than two ID bits asserted (one of which corresponds to the one in the SCSI ID register) and the parity, if enabled, is good.

If a Selection or Reselection is not good, the SCSIC will not respond. If the Selection or Reselecion is good but not enabled, the Invalid (Re)Selection Status bit will be set. If the Selection or Reselection is good and enabled, either the Valid Selection or Valid Reselection status bit will be set.

When being selected or reselected the SCSIC will mask off its own ID bit when it latches the bus ID into the SCSI BUS ID register. The Processor can read the register after the Selection or Reselection is complete to determine the selecting or reselecting device.

Interrupt Mechanism

The processor should respond to an interrupt by reading the Interrupt Status register.

If the SCSI status bit is active high, the Processor reads the Status 1 register to determine the source of the interrupt. If the Selection Attempted or (Re)Selection Complete status bits are active high, the Processor should read the Status 2 register. The SCSIC resets Selection Attempted and (Re)Selection Complete status bits during the Status 2 register read.

If the Transfer Requested, Transfer Complete, Parity Error, SCSI Reset Change or SCSI ATN Change status bits are active high, the Processor should read the Status 3 register. In response, the SCSIC resets Transfer Requested, Transfer Complete, Parity Error, SCSI Reset Change and SCSI ATN Change status bits.

If the Condition Change status bit is active high, the Processor should read the Status 4 register, and the SCSIC resets the Condition Change status bit.

Byte Transfer Modes

INTERRUPT DRIVEN I/O:

The processor responds to an interrupt by reading the Interrupt Status register. If the SCSI status bit is active high, the Processor reads the Status 1 register to determine the source of the interrupt.

If the Transfer Requested status bit is active high, the Processor should read the Status 3 register. In response the SCSIC resets the Transfer Requested status bits.

If the Byte Available status bit is set, the Processor reads the SCSI Data Out register. Next, if no more data is found in buffer, the SCSIC clears the Byte Available status bit. If the Byte Available status bit is still set, the SCSIC then clears PDREQ and generates a new transfer Request interrupt.

If the Byte Requested status bit is set, the Processor writes a byte of data to the SCSI Data Out register. The SCSIC clears the Byte Requested status bit if no more SCSI REQs are pending or there is no more room in the buffer. Next, SCSI clears PDREQ and generates another Transfer Request interrupt if the Byte Requested status bit is still set.

DMA DRIVEN I/O:

DMA controller transfers Message bytes to Processor RAM in response to PDREQ active high. The SCSI Byte Available status bit is cleared if no more data is in the buffer. Next SCSI clears PDREQ (byte mode) and PDREQ (burst mode) if the Byte Available status bit is not active high. Another PDREQ is generated if the Byte Available status bit is still set.

DMA controller transfers Message bytes from the Processor RAM to the SCSI Data Out register in response to PDREQ active high. The SCSIC then 1) clears the Byte Requested status bit if no more SCSI REQs are pending or there is no more room in the Buffer, 2a) PDREQ is cleared (byte mode), 2b) PDREQ is cleared (burst mode) if the Byte Requested status bit is not active high and 3) another PDREQ is generated if the Byte Requested status bit is still set.

POLLED I/O:

The processor reads the Status 3 register to see if either the Byte Available or Byte Requested status bits are active high.

If Byte Available is active, the Processor transfers the byte from the SCSI Data In register to the Processor or the Processor RAM. If there is no more data in the buffer, the SCSIC clears the Byte Available status bit.

If the Byte Requested is active, the Processor transfers the byte from the Processor or the Processor RAM to the SCSI Data Out register. If no SCSI REQs are pending or the Buffer is full, the Byte Requested status bit is cleared.

SCSI Parity Error Handling

Initiator (Status, Message In, Data In Phases):

If the Halt On Parity Error bit in the Control Register is set to one the SCSIC will halt and set the Halted and PE status

bits if data has even parity. If these bits are set, the SCSIC will generate a PE interrupt. If enabled, a Condition Change interrupt will also be generated. In response to the interrupt, the processor reads the Status registers and resets Parity Error and Condition Change Interrupts.

The processor asserts ATN to request Message Out phase in order to signal its desire to send either Message Reject or Message Parity Error. Then the processor issues a (Re)Start Command.

Target (Command, Message Out, Data Out Phases):

The SCSIC will set the PE status bit if data has even parity. If the PE bit is set, the SCSIC will generate a PE interrupt. In response to the interrupt, the processor reads the Status registers. Finally, the SCSIC resets the Parity Error Interrupts.

Note: The Halt On Parity Error bit in the Control Register does not affect Target operation.

COMMANDS

The SCSIC acts as an interface between the SCSI bus and the initiator/target unit. When acting as an initiator (or target supporting reselection), it controls the selection and arbitration process. As a target, it manages the receipt of the command packet from the initiator. All other operations are managed by an outside processor. The typical flow of control progresses as follows:

1) The initiator's processor builds the command block.
2) The processor then instructs the initiating SCSIC to begin Selection. Arbitration, if enabled, is handled by the chip.
3) Once the target unit is selected, the target's processor instructs the target SCSIC to set up a command phase (other phases possible at this point include message, status or data phases).
4) The first byte is transmitted to the target.
5) The target SCSIC notifies its processor (through polling/interrupt) that it is holding the byte. The processor reads the byte in order to determine the command length.
6) The target processor instructs its SCSIC to transfer the remaining bytes.
7) The command packet now resides in the target SCSIC's FIFO buffer.
8) The target SCSIC notifies its processor (through polling/interrupt) that the command packet is available.
9) The processor transfers the command packet into its own memory. The processor is now responsible for digesting and executing the command.
10) While the target's processor executes each command, the initiator and target SCSICs handle handshaking associated with the command.

TABLE 1—MSD95C00 COMMANDS

COMM CODE (HEX)	COMMAND	SCSI	CCS
00	Test Unit Ready	optional	mandatory
03	Request Sense	mandatory	mandatory
04	Format Unit	mandatory	mandatory
08	Read	mandatory	mandatory
0A	Write	mandatory	mandatory
01	Rezero Unit	optional	optional
05	Check Track Format	vender unique	
0B	Seek	optional	optional
12	Inquiry	extended	mandatory
1A	Mode Sense	optional	optional
25	Read Capacity	extended	mandatory
06	Format Track	Vender Unique	
0E	Assign Alt Track	Vender Unique	
15	Mode Select	optional	optional
16	Reserve Unit	optional	mandatory
17	Release Unit	optional	optional
1C	Receive Diag Result	optional	optional
1D	Send Diagnostics	optional	mandatory
2E	Write and Verify	optional	optional

REGISTER DESCRIPTION

RESET REGISTER
8-Bits Read Only (ADDRESS 00H)

Reading the Reset register address configures the chip to ALE or $\overline{AS}$ type timing. Reading the Reset register address a second time puts the MSD95C00 into the same state as driving the $\overline{RST}$ input low and simultaneously reads the general purpose input port. A write to any other MSD95C00 register will terminate the reset state as well as write to the desired register. Both the hardware and software resets will perform the same function as the Clear command in addition to resetting certain register bits as detailed below.

NEGOTIATION REGISTER
8-Bit Write Only (ADDRESS 00H)

The 4 MSB's of this eight bit write only register are used to program the Transfer Period for Synchronous Data transfer. The 4 LSB's are used to program the SCSI REQ/ACK offset. The 4 LSB's are reset to zero by a hard or soft System Reset.

Bits 3-0 REQ/ACK Offset.
= 0 SCSI Asynchronous data transfer mode.
= 1-12 SCSI Synchronous data transfer mode.

These bits are used to program the MSD95C00 with the REQ/ACK offset. The maximum number of offsets the MSC95C00 can support is 12. These bits should be programmed with the REQ/ACK Offset regardless of whether the chip is operating in Initiator or Target mode.

Bits 7-4 Transfer Period

These bits are used to program the MSD95C00 with the Transfer Period for the SCSI Synchronous Data transfer operations. The transfer period will be (2 + N) T where T is twice the clock period. For a 20 Mhz crystal 1 is (2 + 0) 100ns = 200ns = 5mhz.

REGISTER BIT MAPS

NEGOTIATION REGISTER (WRITE REGISTER—ADDRESS 00H)

TRANSFER PERIOD	REQ/ACK OFFSET

MODE REGISTER (WRITE REGISTER—ADDRESS 01H)

RESERVED	SELECTION TIMEOUT bit 1	bit 0	PDREQ LEVEL/ PULSED	DREQ MULTIPLE/ SINGLE PULSE	PARITY CHECK ENABLE/ DISABLE	ARBITRATE ENABLE/ DISABLE	INITIATOR/ TARGET

BYTE COUNTER HIGH REGISTER (WRITE REGISTER-ADDRESS 02H)

MOST SIGNIFICANT BYTE OF BYTE COUNT REGISTER (1's compliment)

BYTE COUNTER MIDDLE REGISTER (WRITE REGISTER—ADDRESS 03H)

MIDDLE BYTE OF BYTE COUNT REGISTER (1's compliment)

BYTE COUNTER LOW REGISTER (WRITE REGISTER—ADDRESS 04H)

LEAST SIGNIFICANT BYTE OF BYTE COUNT REGISTER (1's compliment)

I/O REGISTER (WRITE REGISTER—ADDRESS 05H)

LATCHED DATA TO XD7 TO XD0 PINS

INTERRUPT ENABLE 1 REGISTER (WRITE REGISTER—ADDRESS 06H)

CONDI-TION CHANGE	ATN or RESET CHANGE	SYSTEM PARITY ERROR	SCSI PARITY ERROR	TRANSFER COMPLETE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION ATTEMPT-ED

INTERRUPT ENABLE 2 REGISTER (WRITE REGISTER—ADDRESS 07H)

SCSI MASTER INTER-RUPT	BUS FREE DETECT	HALT INTERRUPT	TRANSFER DONE	SCSI TRANSFER COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELECT

CONTROL REGISTER (WRITE REGISTER—ADDRESS 08H)

ENABLE DREQ	ENABLE PDREQ	HALT ON PARITY ERROR	ALWAYS 0	ALWAYS 0	ENABLE RESELECT	ENABLE SELECT	AUTO ATTEN-TION ASSERT

COMMAND 1 REGISTER (WRITE REGISTER—ADDRESS 09H)

DISCON-NECT	SELECT	(RE)-START	CLEAR	NEGATE ATTEN-TION	ASSERT ATTEN-TION	NEGATE SCSI RESET SIGNAL	ASSERT SCSI RESET SIGNAL

COMMAND 2 REGISTER (WRITE REGISTER—ADDRESS 0AH)

SET MESSAGE IN	SET MESSAGE OUT	RESERVED	RESERVED	SET STATUS PHASE	SET COMMAND PHASE	SET DATA IN	RESERVED

RESERVED (WRITE REGISTER—ADDRESS 0BH)

(MSB)	RESERVED	(LSB)

RESERVED (WRITE REGISTER—ADDRESS 0CH)

(MSB)	RESERVED	(LSB)

DESTINATION ID REGISTER (WRITE REGISTER—ADDRESS 0DH)

(MSB)	DESTINATION ID	(LSB)

SCSI ID REGISTER (WRITE REGISTER—ADDRESS 0EH)

(MSB)	SCSI ID (NODE ID)	(LSB)

DATA OUT REGISTER (WRITE REGISTER—ADDRESS 0FH)

(MSB)	DATA TO BE OUTPUT TO THE SCSI BUS	(LSB)

RESET REGISTER (READ REGISTER—ADDRESS 00H)

XD7-XD0 (IN)

MODE REGISTER (READ REGISTER—ADDRESS 01H)

RESERVED	SELECTION TIMEOUT	PDREQ LEVEL/ PULSED	DREQ MULTIPLE/ SINGLE PULSE	PARITY CHECK ENABLE/ DISABLE	ARBITRA-TION ENABLE/ DISABLE	INITIATOR/ TARGET

BYTE COUNTER HIGH REGISTER (READ REGISTER-ADDRESS 02H)

(MSB)	MOST SIGNIFICANT BYTE	(LSB)

BYTE COUNTER MIDDLE REGISTER (READ REGISTER—ADDRESS 03H)

(MSB)	MIDDLE SIGNIFICANT BYTE	(LSB)

BYTE COUNTER LOW REGISTER (READ REGISTER—ADDRESS 04H)

(MSB)	LEAST SIGNIFICANT BYTE	(LSB)

I/O REGISTER (READ REGISTER—ADDRESS 05H)

(MSB)	LATCHED DATA FROM XD7-XD0 PINS (IN)	(LSB)

INTERRUPT ENABLE 1 REGISTER (READ REGISTER—ADDRESS 06H)

CONDI-TION CHANGE	ATN or RESET CHANGE	SYSTEM PARITY ERROR	PARITY ERROR	TRANSFER DONE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION ATTEMPT-ED

INTERRUPT ENABLE 2 REGISTER (READ REGISTER—ADDRESS 07H)

MASTER INTER-RUPT	BUS FREE DETECT	HALT INTERRUPT ENABLE	TRANSFER DONE	SCSI TRANSFER COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELEC-TION

CONTROL REGISTER (READ REGISTER—ADDRESS 08H)

ENABLE DREQ	ENABLE PDREQ	HALT ON PARITY ERROR	ALWAYS 0	ALWAYS 0	ENABLE RESELECT	ENABLE SELECT	AUTO ATTEN-TION ASSERT

INTERRUPT STATUS REGISTER (READ REGISTER—ADDRESS 09H)

RESERVED	SCSI INTER-RUPT	RESERVED

STATUS 1 REGISTER (READ REGISTER—ADDRESS 0AH)

CONDI-TION CHANGE	ATTN or RESET CHANGE	SYSTEM PARITY ERROR	SCSI PARITY ERROR	TRANSFER COMPLETE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION AT-TEMPTED

STATUS 2 REGISTER (READ REGISTER— ADDRESS 0BH)

SCSI ATTN SIGNAL	RESERVED	RESERVED	UNSUC-CESS (RE)-SELECT COMPLETE	SUC-CESSFUL (RE)-SELECT COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELEC-TION

STATUS 3 REGISTER (READ REGISTER—ADDRESS 0CH)

SCSI ATTN SIGNAL	SCSI RESET	SYSTEM PARITY ERROR	TRANSFER DONE	SCSI TRANSFER COMPLETE	SCSI PARITY ERROR	BYTE AVAILABLE	BYTE RE-QUESTED

STATUS 4 REGISTER (READ REGISTER—ADDRESS 0DH)

RESERVED	BUS FREE DETECTED	HALTED	ARBITRA-TION	RESERVED	ENCODED PHASE MSG	ENCODED PHASE C/D	ENCODED PHASE I/O

SCSI BUS ID REGISTER (READ REGISTER—ADDRESS 0EH)

(MSB)	SCSI BUS ID (NODE SOURCE ID)	(LSB)

DATA IN REGISTER (READ REGISTER—ADDRESS 0FH)

(MSB)	DATA FROM BUFFER	(LSB)

MODE REGISTER
8-Bits Read/Write (ADDRESS 01H)

This 8 bit Read/Write register defines the operating mode of the SCSIC. Refer to the System Operation section for a description of the operating modes. The bits in this register are reset to zero by a hard or soft System Reset.

Bit 0 Initiator/$\overline{\text{Target}}$

The state of this bit will not prevent the chip from being selected or reselected by another device. The state of this bit determines whether the select command will start either the select function or the reselect function.

Bit 1 Arbitration Enable/$\overline{\text{Disable}}$

When this bit is set to 1, the MSD95C00 will begin arbitration for SCSI bus after detecting bus free for selected commands. When set to 0, the arbitration phase will be bypassed and the chip will go directly to selection after detecting bus free.

Bit 2 Parity Check Enable
When this bit is "1", the MSD95C00 checks the parity of the SCSI bus during all phase except Bus Free and Arbitration. When this bit is "0", Parity will not be checked.

Bit 3 DREQ Multiple/Single Pulse Mode
When this bit is "1", the SCSIC can generate up to twelve DREQ pulses before receiving the first DACK. When this bit is "0", the SCSIC will expect one DACK for every DREQ pulse generated.

Bit 4 PDREQ Level/Pulsed
When this bit is "1", PDREQ will be high as long as there is received data in the buffer or there is room for more data in the buffer when sending data. When this bit is "0", the MSD95C00 will drive the PDREQ output inactive low after the Data In register is read or the Data Out register is written to regardless of the state of the buffer.

Bit 5, 6 Selection Timeout
These two bits are used to select the desired SCSI Selection Timeout:

Bit 6	Bit 5	Timeout Selected*
0	0	839ms
0	1	210ms
1	0	52ms
1	1	1.6ms

*based on 20 MHz crystal operation

Bit 7 Reserved

BYTE COUNTER HIGH REGISTER
8-Bit Read/Write (ADDRESS 02H)

This 8-bit Read/Write register holds the most significant byte that is to be loaded into the Byte Counter. The data is transferred from the Byte Counter High Register into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB. The Byte Counter registers are loaded with the 1's complement of the desired byte count.

BYTE COUNTER MIDDLE REGISTER
8-Bit Read/Write (ADDRESS 03H)

This 8-bit Read/Write register holds the middle byte of data that is to be loaded into the Byte Counter. The data is transferred from the Byte Counter Middle Register into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB.

The Byte Counter registers are loaded with the 1's complement of the desired byte count.

BYTE COUNTER LOW REGISTER
8-Bit Read/Write (ADDRESS 04H)

This 8-bit Read/Write register holds the least significant byte of data that is to be loaded into the Byte Counter. The data is transferred into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB. The Byte Counter registers are loaded with the 1's complement of the desired byte count.

I/O REGISTER
8-Bit Read/Write (ADDRESS 05H)

This 8-bit Read/Write register is an eight bit bi-directional I/O port available to the Processor. Data written to this register will be latched and available on the XD7-XD0 pins. Information present on the XD7-XD0 pins will be available to the Processor when this register is read. The XD7-XD0 I/O pins are open drain with internal pullup devices.

INTERRUPT ENABLE 1 REGISTER
8-Bit Read/Write (ADDRESS 06H)

This eight bit Read/Write register enables or disables certain interrupt causing conditions to the microcomputer. Reading this register reflects the states of the bits in it. The bits in this register are cleared to zero by a hard or soft System Reset.

Bit 0 Selection Attempted Interrupt
When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Selection Attempted bit in the Status 1 register is set to one. When this bit is "0", the Master Interrupt will not be driven active high for this condition.

Bit 1 (Re)Selection Complete Interrupt Enable
When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the (Re)Selection Complete bit in the Status 1 register is set to one. If this bit is "0", the Master Interrupt will not be driven active high for this condition.

Bit 2 Transfer Request Interrupt
When the bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Transfer Request bit in the Status 1 register is set to one. If this bit is "0", the Master Interrupt will not be driven high for this condition.

Bit 3 Transfer Complete Interrupt Enable
When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Transfer Complete Interrupt bit in the Status 1 register is set to one. The Master Interrupt will not be driven high for this condition.

Bit 4 Parity Error Interrupt Enable
When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Parity Error Interrupt bit in the Status 1 register is set to one. When this bit is "0", the Master Interrupt will not be driven active high for this condition.

Bit 5 System Parity Error Interrupt Enable
When this bit is "1", the SCSIC will drive the SCSI Master Interrupt bit active high when the System Parity Error Interrupt bit in the Status 1 register is set to one. When this bit is reset, the Master Interrupt will not be driven active high for this condition.

Bit 6 SCSI ATN or RESET Change Interrupt Enable
When this bit is set to "1", the MSD95C00 will drive the SCSI Master Interrupt bit active high when the SCSI ATN or RESET Change bit in the Status 1 register is set to 1. When this bit is set to "0", the Master Interrupt will not be driven active high for this condition.

Bit 7 Condition Change Interrupt Enable
When this bit is set to "1", the MSD95C00 will drive the SCSI Master Interrupt bit active high when the Condition Change bit in the Status 1 register is set to one. When this bit is set to "0", the Master Interrupt will not be driven active high for this condition.

INTERRUPT ENABLE 2 REGISTER
8-Bit Read/Write (ADDRESS 07H)

This eight bit Read/Write register enables or disables certain microcomputer interrupt causing conditions. Reading this register reflects the states of the bits in it. The bits in this register are cleared to zero by a hard or soft System Reset.

Bit 0 Valid Selection Interrupt Enable
When this bit is set to "1", the SCSIC will set the Selection Attempted bit in the Status 1 register to one when the Valid Selection bit in the Status 2 register is active high. When this bit is "0", the Selection Attempted bit cannot be set by this condition.

Bit 1 Valid Reselection Interrupt Enable
When this bit is set to "1", the SCSIC will set the Selection Attempted bit in the Status 1 register to one when the Valid

Reselection bit in the Status 2 register is active high. When this bit is set to "0", the Selection Attempted bit cannot be set by this condition.

Bit 2 Invalid (Re)Selection Interrupt Enable
Setting this bit to a one will cause the SCSIC to set the Selection Attempted bit in the Status 1 register to one when the Invalid (Re)Selection bit in the Status 2 register is active high. If this bit is "0", the Selection Attempted bit cannot be set by this condition.

Bit 3 SCSI Transfer Complete Interrupt Enable
Setting this bit to "1" will cause the SCSIC to set the Transfer Complete Interrupt bit in the Status 1 register to one when the SCSI Transfer Complete bit in the Status 3 register is active high. If this bit is "0", the Transfer Complete Interrupt bit cannot be set by this condition.

Bit 4 Transfer Done Interrupt Enable
Setting this bit to "1" will cause the MSD95C00 to set the Transfer complete Interrupt bit in the Status 1 register to one when the Transfer Done bit in the Status 3 register is active high. If this bit is "0", the Transfer Complete Interrupt bit cannot be set by this condition.

Bit 5 Halted Interrupt Enable
Setting this bit to "1" will cause the MSD95C00 to set the Condition Change bit in the Status 1 register to one when the Halted bit in the Status 4 register goes active high. If this bit is "0", the Condition Change bit cannot be set by this condition.

Bit 6 Bus Free Phase Detect Interrupt Enable
Setting this bit to "1" will cause the MSD95C00 to set the Condition Change bit in the Status 1 register to one when the Bus Free Phase Detect bit in the Status 4 register is active high. If this bit is "0", the Phase Change bit cannot be set by this condition.

Bit 7 SCSI Master Interrupt Enable
Setting this bit to "1" will cause the MSD95C00 to drive its $\overline{\text{INT}}$ output active low when an enabled condition causes one of the bits in the Status 1 register to go active high. If this bit is "0", the $\overline{\text{INT}}$ pin cannot be driven active.

CONTROL REGISTER
8-Bit Read/Write (ADDRESS 08H)

This 8 bit Read/Write register is used to control chip operation. The bits are reset to zero by a hard or soft System Reset.

Bit 0 Auto ATN Assert
When this bit is set to "1", the MSD95C00 will automatically assert the SCSI bus ATN signal before beginning the select part of one of the Select commands. When this bit is set to "0", ATN will not be asserted.

Bit 1 Enable Selection
When this bit is set to "1", the MSD95C00 will allow itselt to be selected by another SCSI device. When this bit is set to "0", the MSD95C00 will generate an interrupt when another SCSI device tries to select it. The state of this bit will not prevent the chip from attempting to select or reselect another SCSI device.

Bit 2 Enable Reselection
When this bit is set to "1", the MSD95C00 will allow itself to be reselected by another SCSI device. When this bit is set to "0", the MSD95C00 will generate an interrupt when another SCSI device tries to reselect it. The state of this bit will not prevent the chip from attempting to select or reselect another SCSI device.

Bit 3 Always 0

Bit 4 Always 0

Bit 5 Halt On Parity Error
When this bit is set to "1" and the MSD95C00 is operating in Initiator mode, the MSD95C00 will not assert SACK for bytes with bad parity during Status, Message In or Data In phase transfers. This bit does not affect operation in Target mode. When this bit is set to "0", the MSD95C00 will negate SACK regardless of parity.

Bit 6 Enable PDREQ
When this bit is set to "1", the SCSIC will be able to drive the PDREQ output active high. When this bit is set to "0", the PDREQ output will be forced low.

Bit 7 Enable DREQ
When this bit is set to "1", the MSD95C00 will be able to drive the $\overline{\text{DREQ}}$ output active low. When this bit is set to "0", the $\overline{\text{DREQ}}$ output will be forced high.

INTERRUPT STATUS
8-Bit Read Only (ADDRESS 09H)

This Read Only register contains information about the internal MSD95C00 operation.

Bits 0-1 Always 0

Bit 2 SCSI Interrupt
This bit is set to "1" when one of the enabled interrupt causing conditions causes a bit in the Status 1 register to go active high. It is reset to "0" when the interrupt causing condition(s) are cleared.

Bits 3-7 Always 0

COMMAND 1 REGISTER
8-Bit Write Only (ADDRESS 09H)

This Write Only register is used to initiate one of the Select or Reselect operations and to assert or negate the SCSI bus signals that are manipulated by the Processor software. Except for the Clear bit, the states of these bits are used to generate a strobe and are not latched in the MSD95C00. A hard or soft System Reset will cause the signals controlled by this register to be negated and the Clear bit to be reset to "0".

Bit 0 Assert SCSI Reset Signal
Setting this bit to "1" will cause the MSD95C00 to assert the SCSI bus reset signal (SRST).

Bit 1 Negate SCSI Reset Signal
Setting this bit to "1" will cause the MSD95C00 to negate the SCSI bus reset signal (SRST).

Bit 2 Assert ATN Signal
Setting this bit to "1" will cause the MSD95C00 to assert the SCSI bus ATN signal (ATN).

Bit 3 Negate ATN Signal
Setting this bit to "1" will cause the SCSI chip to negate the SCSI bus ATN signal (ATN).

Bit 4 Clear
Setting this bit to "1" will cause the chip to go into the Clear state and reset all of the internal counters, reset the latched status bits, reset the SCSI Master Interrupt Enable, reset the bits in the Command 2 Register, disconnect from the SCSI bus and negate the SCSI control signals. Setting this bit to "0" will terminate the Clear state. After setting this bit to "1", the Processor must wait a minimum of 1 μsec before clearing it.

Bit 5 (Re)Start
When the MSD95C00 is operating in the Initiator mode, writing a "1" to this bit will cause chip operation, that was interrupted by detection of a parity error on the SCSI data bus, to continue (this condition can only occur when the Halt On Parity Error bit in the Control register is set to "1"). Also, writing a "1" to this bit after the MSD95C00 was halted by

SREQ going active when the byte counter was equal to "0" will cause the MSD95C00 to respond with SACK. This will allow the Initiator to perform single byte transfers without loading the Byte Counter (data may be written to the buffer before or after writing to the Command register). This bit does not affect Target mode chip operation.

Bit 6 Select
Setting this bit to "1" will cause the MSD95C00 to initiate a Select operation, a Select with ATN asserted operation, an Arbitrate and Select operation, an Arbitrate and Select with ATN asserted operation or an Arbitrate and Reselect opration. The operation initiated depends on the state of the Target/Initiator and Arbitration Enable/Disable bits in the Mode register and the Auto-ATN Assert bit in the Control register.

Bit 7 Disconnect
Setting this bit to "1" will cause the MSD95C00 to stop driving all of the SCSI Data Bus and Control signals.

STATUS 1 REGISTER
8-Bit Read Only (ADDRESS 0AH)

This 8-bit Read Only register contains information about the internal MSD95C00 operation.

Bit 0 Selection Attempted
This bit is set to "1" by the active and enabled state of either the Valid Select, Valid Reselect or Invalid (Re)Select status bits in the Status 2 register. It is reset by reading the Status 2 register.

Bit 1 (Re)Selection Complete
This bit is set to "1" by the active state of either the Successful (Re)Selection Complete or Unsuccessful (Re)Selection Complete status bits in the Status 2 register. It is reset by reading the Status 2 register.

Bit 2 Transfer Request
This bit is set to "1" by the active state of either the Byte Available or Byte Requested status bits in the Status 3 register. It is reset by reading the Status 3 register. It will be set again after the Data Register is read if Byte Available or Byte Requested are still high.

Bit 3 Transfer Complete Interrupt
This bit is set to "1" when either the Transfer Done or SCSI Transfer Complete bits in the Status 3 register go active high. It is reset by reading the Status 3 register.

Bit 4 Parity Error Interrupt
This bit is set to "1" when the Parity Error bit in the Status 3 register goes active high. It is reset by reading the Status 3 register.

Bit 5 System Parity Error
This bit is set to "1" when the System Parity Error bit in the Status 3 register goes active high. It is reset by reading the Status 3 register.

Bit 6 SCSI ATN or RESET Change
This bit is set to "1" when either the SCSI ATN or RESET signal changes from the high to low or low to high state. It is reset by reading the Status 3 register.

Bit 7 Condition Change
This bit is set to "1" when either the (enabled) Bus Free Detected or Halted bits in the Status 4 register go active high. It is reset by reading the Status 4 register.

COMMAND 2 REGISTER
8-Bit Write Only (ADDRESS 0AH)

This Write Only register is used to initiate a new phase when the SCSIC is in Target mode. A hard or soft System Reset or a Disconnect command will clear all the bits in this register to "0". When the Initiator detects that the SCSI Data Bus is changing direction from out (the Initiator driving) to in (the Target driving) it will release the SCSI Data bus within a Data Release Time (400ns) of I/O being asserted. This condition can occur when the Target begins a Message In, Status or Data In phase.

When the Target switches the SCSI Data Bus direction from in (the Target driving) to out (the Initiator driving) it will release the SCSI Data bus within a Deskew delay (45ns) of negating I/O. This condition can occur when the Target begins a Message Out, Command or Data Out phase.

Note that the Processor must delay at least 800ns after issuing a Set Phase type command before writing to the byte counter. The phase will be generated upon writing to the LSB of the Byte Count register. Phases must not be changed unless the FIFO is empty.

Bit 1 Set Data In Phase
Setting this bit to "1" will cause the MSD95C00 to assert the I/O signal and negate the MSG and C/D signals.

Bit 2 Set Command Phase
Setting this bit to "1" will cause the MSD95C00 to assert the C/D signal and negate the I/O and MSG signals.

Bit 3 Set Status Phase
Setting this bit to "1" will cause the MSD95C00 to assert the C/D and I/O signals and negate the MSG signal.

Bits 4 and 5 Reserved
Must be set to "0" at all times.

Bit 6 Set Message Out Phase
Setting this bit to "1" will cause the MSD95C00 to assert the C/D and MSG signals and negate the I/O signal.

Bit 7 Set Message In Phase
Setting this bit to "1" will cause the MSD95C00 to assert the C/D, I/O and MSG signals.

Set Data Out Phase Setting bits 0-7 to "0" will cause the SCSIC to negate the MSG, I/O and C/D signals.

STATUS 2 REGISTER
8-Bit Read Only (ADDRESS 0BH)

This 8 bit Read Only register contains information about the internal MSD95C00 operation.

Bit 0 Valid Selection
This bit is set to "1" when the MSD95C00 has been selected by another SCSI device. In order to be selected, the Enable Selection bit in the Control Register must be in the correct state. This bit is reset by reading the Status 2 register.

Bit 1 Valid Reselection
This bit is set to "1" when the MSD95C00 has been reselected by another SCSI device. In order to be reselected, the Enable Reselection bit in the Control Register must be in the correct state. This bit is reset by reading the Status 2 register.

Bit 2 Invalid (Re)Selection
This bit is set to "1" when another SCSI device attempts to select or reselect the SCSIC and the corresponding enable bit in the Mode register is not in the correct state. This bit is reset by reading the Status 2 register.

Bit 3 Successful (Re)Selection Complete
This bit is set to "1" when the MSD95C00 has successfully selected or reselected another SCSI device and that device has responded by asserting BSY. Also, this bit is set to "1" at the trailing edge of SEL when a device has selected or reselected this device. This bit is reset by reading the Status 2 register.

Bit 4 Unsuccessful (Re)Selection Complete
This bit is set to "1" when the MSD95C00 has attempted to select or reselect another SCSI device and that device has

not responded by asserting BSY within the programmed Selection Timeout Delay. This bit is reset by reading the Status 2 register.

Bits 5 and 6 Reserved

Bit 7 SCSI ATN
This bit reflects the state of the ATN bit on the SCSI bus. It is active high when the ATN signal is asserted and active low when the ATN signal is deasserted.

STATUS 3 REGISTER
8-Bit Read Only (ADDRESS 0CH)

This 8 bit Read Only register contains information about the internal MSD95C00 operation.

Bit 0 Byte Requested
This signal is active high whenever there is room for more requested data in the internal buffer when transferring to the SCSI Data bus.

Bit 1 Byte Available
This signal is active high whenever there is data from the SCSI Data bus in the internal buffer for transfer to the Processor or Ring Buffer RAM.

Bit 2 Parity Error (PE)
This bit is set to "1" if parity checking is enabled and the SCSI chip detects even (bad) parity on received data transfers over the SCSI data bus during any Information phase. It is reset by reading the Status 3 register.

Bit 3 SCSI Transfer Complete (STC)
This status signal is active high when the Byte Counter End Count condition is active high and the last byte has been transferred from the SCSI bus into the internal buffer when the chip is operating in Target mode during Message Out, Command or Data Out phases. In all other cases, this status signal will function the same as Transfer Done.

Bit 4 Transfer Done (TD)
This status signal is active high when the Byte Counter End Count condition is active high and the last byte has been transferred out of the internal buffer to the SCSI Data bus, the Processor port or the ring buffer DMA port.

Bit 5 System Parity Error (SYPE)
This bit is set to "1" when the MSD95C00 detects even (bad) parity on the System Data Bus. It is reset by reading the Status 3 register.

Bit 6 SCSI RESET
This bit reflects the state of the RST bit on the SCSI bus. It is active high when the RST signal is asserted and active low when the RST signal is deasserted.

Bit 7 SCSI ATN
This bit reflects the state of the ATN bit on the SCSI bus. It is active high when the ATN signal is asserted and active low when the ATN signal is deasserted.

STATUS 4 REGISTER
8-Bit Read Only (ADDRESS 0DH)

This 8 bit Read Only register contains information about the internal SCSIC operation.

Bit 0-2 Encoded Phase
These bits are reflections of the SCSI MSG, I/O, and C/D signals. They identify the SCSI Information Transfer Phase.

Bit 2 MSG	Bit 1 C/D	Bit 0 I/O	INFORMATION PHASE
0	0	0	Data Out Phase
0	0	1	Data In Phase
0	1	0	Command Phase
0	1	1	Status Phase
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message Out Phase
1	1	1	Message In Phase

Bit 3 Busfrpx
This bit goes high four to five internal clock cycles after BSY and SEL are both continuously false. The bit remains high as long as the SCSI bus is free.

Bit 4 Busfree (window)
This bit goes high five to six internal clock cycles after BSY and SEL are both continuously false. The bit remains high three to four clock cycles after the bus is no longer free.

Bit 5 Halted
This status bit can only be set when the chip is operating in Initiator mode. It is set by SREQ going active when the Byte Counter is "0". It can also be set when a parity error is detected on the SCSI data bus. This bit is reset by reading the Status 4 register.

Bit 6 Bus Free Phase Detect
This status signal is the output of the Bus Free detection circuit. It is latched active high when the Bus Free phase as specified in the SCSI specification is detected on the SCSI Bus. This bit is reset by reading the STATUS 4 register.

DESTINATION ID REGISTER
8-Bit Write Only (ADDRESS 0DH)

This 8-bit register Write Only is used to hold the value of the SCSI ID of the device that is to be Selected or Reselected.

SCSI BUS ID REGISTER
8-Bit Read Only (ADDRESS 0EH)

This 8-bit Read Only register holds the ID that had been latched from the SCSI bus when an attempt was made to Select or Reselect this chip. This chip's SCSI ID is masked off.

SCSI ID REGISTER
8-Bit Write Only (ADDRESS 0EH)

This 8-bit Write Only register is used to hold the value of the MSD95C00's SCSI ID.

DATA IN REGISTER
8-Bit Read Only (ADDRESS 0FH)

This 8-bit Read Only register is used by the Processor during programmed I/O or Processor port DMA transfers. It allows you to read data received from the SCSI bus which is presently in the internal buffer.

DATA OUT REGISTER
8-Bit Write Only (ADDRESS 0FH)

This 8 bit Write Only register is used by the Processor during programmed I/O or Processor port DMA transfers. The data loaded into this register is output to the SCSI bus via the internal buffer.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516)273 3100 TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

MSD95C02
PRELIMINARY

Storage μ-Controller for Direct Access (Disk) or Serial Access (Tape) Devices — SμnDAe™

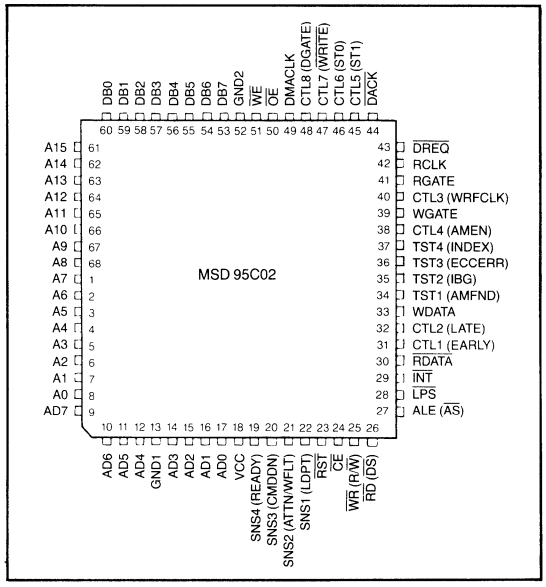
APPLICATIONS SUPPORTED:

- ☐ Embedded SCSI drives when used with companion MSD95C00 SCSI Controller
- ☐ Compatible with ESDI and SMD disk interfaces
- ☐ Interfaces to 8051, Z8 and 80188 microprocessors
- ☐ Supports 3-Sector Prefetch for Unix® applications
- ☐ Supports QIC-24 Tape:
  - 5 Mb/sec GCR data transfers
  - Read-after-write
- ☐ Controls Optical Disks with commonly available Error Correction IC's
- ☐ Supports Floppy Disk
- ☐ Modular design for easy adaption to special purpose applications

FEATURES:

- ☐ 24 Mb/sec NRZ OR 12 Mb/sec RLL, MFM, FM Disk Data Transfers
- ☐ Zero Latency read capability
- ☐ Choice of ECC:
  - Reed-Solomon ECC able to detect and correct a 41 bit burst error or two randomly spaced 17 bit burst errors without miscorrection; CRC extension to detect miscorrection of errors beyond that range, OR
  - 32-bit IBM® compatible ECC
- ☐ Register programmable data format via on-chip writeable microsequencer
- ☐ 3-Channel internal double-speed 64K (externally expandable) Ring Buffer DMA controller
- ☐ Cache buffer management allows disk data transfers without processor intervention

PIN CONFIGURATION



- ☐ Supports transparent "on-the-fly" error correction
- ☐ Low power CMOS with Standby Mode
- ☐ Available in 68 pin PLCC
- ☐ TTL compatible inputs and outputs

SECTION VII

GENERAL DESCRIPTION

The MSD95C02 is a high speed micro-programmable data path controller. It incorporates a triple channel DMA CONTROLLER, a RAM based MICROSEQUENCER, a sophisticated ECC generator/checker circuit, an RLL2, 7/MFM/FM/GCR Encoder/Decoder and a Parallel/Serial shift register in one 68 pin plastic package. The MSD95C02 can be combined in a circuit with standard local processor and static RAM chips to build a very high performance multi-media controller incorporating SCSI, ESDI, SMD, ST-506, QIC 24, and FLOPPY disk interfaces. The RAM based MICROSEQUENCER permits the user to build a mass storage controller that conforms with any currently available data format.

The addition of an SMC MSD95C00 SCSI CONTROLLER will provide a tightly coupled 2-chip set for high speed, high performance SCSI and "embedded SCSI" applications with minimum component count and synchronous SCSI speeds of up to 5 megabytes per second.

The DMA CONTROLLER section of the MSD95C02 controls and arbitrates up to 64K of external Ring Buffer memory built with standard off-the-shelf static RAM. The Ring Buffer size can be easily expanded beyond 64K with the addition of a few additional gates. Disk data transfers to and from this cache buffer are managed by the MSD95C02's internal DMA CONTROLLER and are performed without the need for processor intervention.

External Device (e.g., SCSI bus) accesses to the Ring Buffer are controlled via a DMA request/acknowledge handshake and are completely asynchronous with respect to disk and local processor transfers. This method of local buffer access combined with a powerful Reed Solomon error correcting code and CRC extension designed to virtually eliminate miscorrection, provides the user with on-the-fly error correction with no loss of disk revolutions.

Unix® is a registered trademark of AT&T Bell Labs.

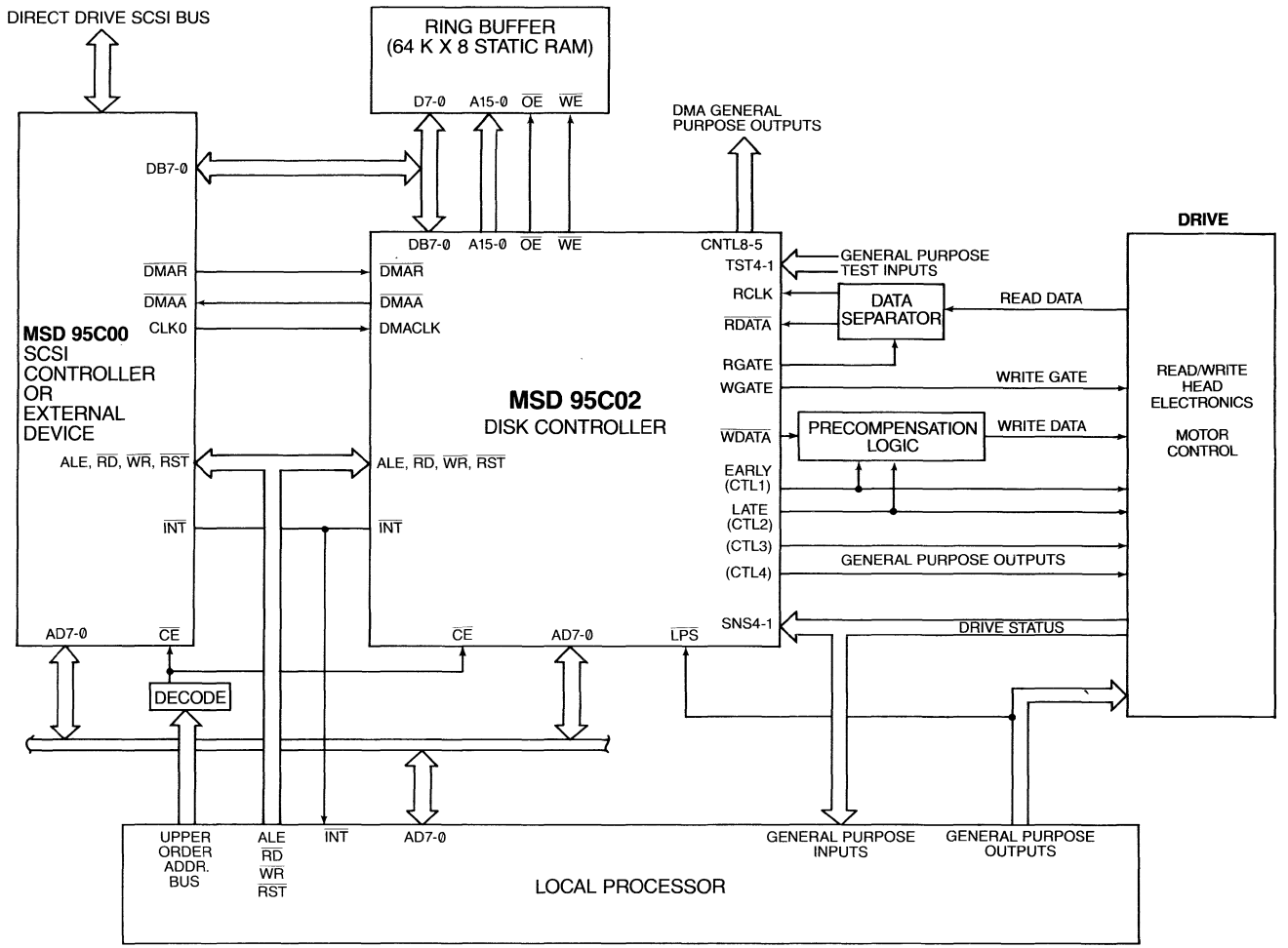


FIGURE 1: MSD 95C02 EMBEDDED SCSI SYSTEM

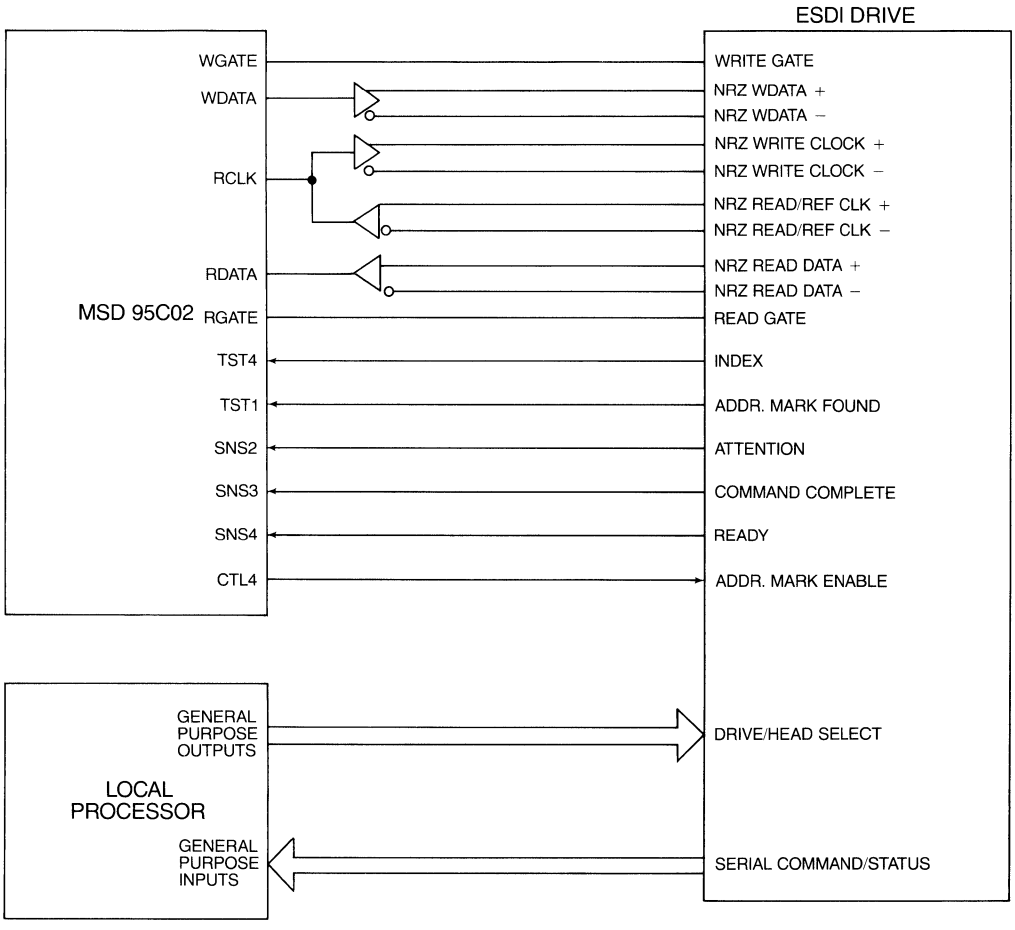


FIGURE 2: MSD95C02 TO ESDI INTERFACE

The MSD95C02 is built from a set of high level, function specific SuperCells™ that can be connected together in such a way as to adapt themselves to a special purpose customer requirement. The first set of SuperCells™ has been chosen to optimize the device for "EMBEDDED SCSI" and ESDI controller applications. Figure 1 illustrates the MSD95C02 used with its companion MSD95C00 SCSI chip to form an "EMBEDDED SCSI" system. Figure 2 illustrates the MSD95C02 used as an ESDI controller.

As can be seen from the system block diagrams, the interface to the external static RAM ring buffer requires no external circuitry. In an "EMBEDDED SCSI" environment, there are two external data buses used; one to permit data flow between the MSD95C00 SCSI controller and the ring buffer and another data bus to permit local processor to MSD95C00 SCSIC and MSD95C02 exchanges. The two data buses allow for uninterrupted data flow in and out of the ring buffer during local processor updates to the MSD95C00 and MSD95C02 devices. Ring buffer arbitration is controlled by the on-chip triple channel DMA CONTROLLER which arbitrates ring buffer accesses to and from the media, SCSI channel and local processor. Local processor accesses to the ring buffer are possible through directly addressable registers in the MSD95C02's DMA block.

The MSD95C02 contains several general purpose input/output pins which can be used to control and monitor external events. In addition, there are four general purpose test inputs and four latched sense inputs that may be used directly by the MICROSEQUENCER to perform conditional jumps.

The sense inputs, test inputs and control outputs of the MSD95C02 are used to efficiently handle ESDI drives with serial data rates up to 24 MHz.

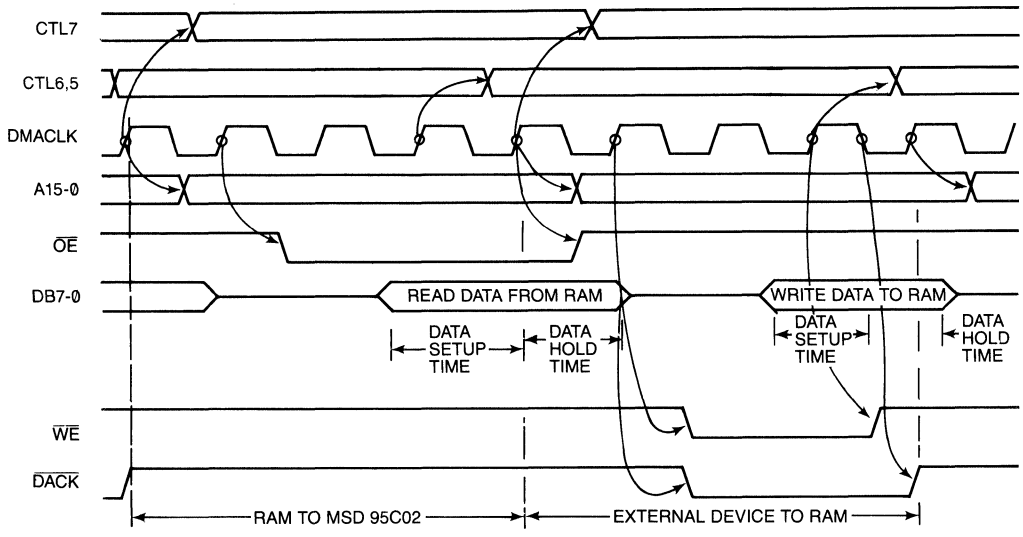


FIGURE 3: TYPICAL BUFFER TIMING (DISK WRITE)

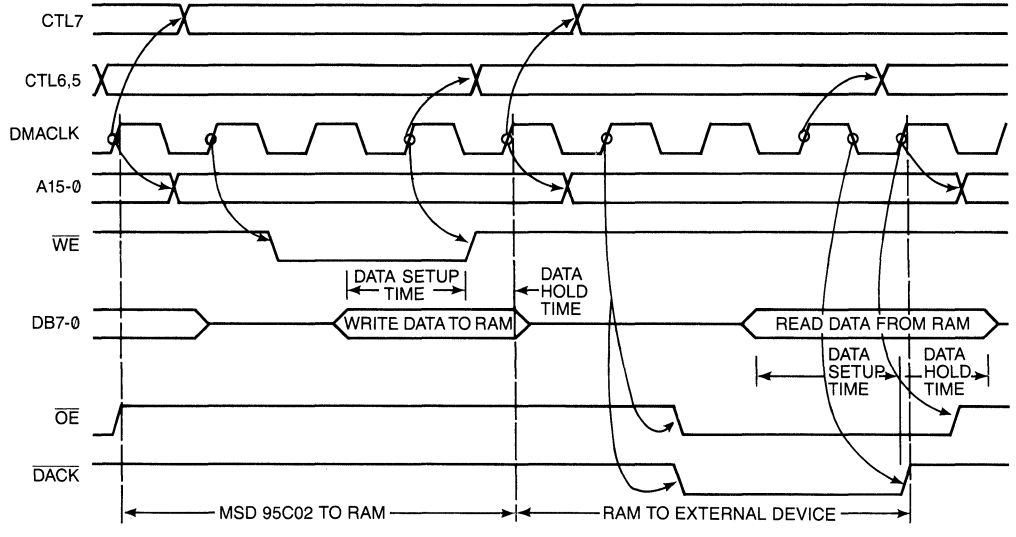


FIGURE 4: TYPICAL BUFFER TIMING (DISK READ)

PINOUT DESCRIPTION

RING BUFFER INTERFACE (Refer to Figures 3 and 4 for ring buffer timing):

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
53-60	DB7-0	I/O	Data Bus. Bi-directional data bus to the external ring buffer RAM. This bus is automatically put into a high impedance state during valid External Device DMA cycles.
61-68, 1-8	A15-0	O	Address Bus. These outputs are used to address the external ring buffer RAM.
50	$\overline{OE}$	O	$\overline{\text{Output Enable}}$. This active low output strobes the ring buffer RAM's data bus output drivers.
51	$\overline{WE}$	O	$\overline{\text{Write Enable}}$. Strobe. This active low output strobes write data from the data bus into the ring buffer RAM.
49	DMACLK	I	DMA Clock. This 20 MHz (maximum) input is used by the MSD95C02 to generate DMA cycles.
43	$\overline{DREQ}$	I	$\overline{\text{DMA Request}}$. This input is driven active low by an External Device to request a DMA cycle.
44	$\overline{DACK}$	O	$\overline{\text{DMA Acknowledge}}$. This output is driven active low by the MSD95C02 in response to $\overline{DREQ}$. During data transfer from the ring buffer to the External Device, the rising edge of this signal is used to strobe data into the External Device. During data transfer from the external device to the ring buffer, a low will enable data transfer from the External Device.
45 46	CTL5 (ST1) CTL6 (ST0)	O O	Control 5. Control 6. Depending on the programming of the MODE 1 Register, these bits can either reflect the data written to bits 4 and 5 of the Local Processor Output Register or they can be outputs that indicate the type MSD95C02 DMA controller cycle in progress: ST1 ST0 | CYCLE 0 0 | EXTERNAL DEVICE 0 1 | LOCAL PROCESSOR 1 0 | MICROSEQUENCER (DISK) 1 1 | RESERVED
47	CTL7 ($\overline{WRITE}$)	O	Control 7. Depending on the programming of the MODE 1 Register, this bit can either reflect the data written to bit 6 of the Local Processor Output Register or this bit can be an output signal indicating to the ring buffer that a WRITE or READ cycle is about to start. This output is low during a write cycle and high during a read cycle. CTL 7, 6, and 5, when programmed as $\overline{\text{WRITE}}$, ST0, ST1, can be used for interfacing to an external ECC chip.
48	CTL8 (DGATE)	O	Control 8. Depending on the programming of the MODE 1 Register, this bit can reflect the data written to bit 7 of the Local Processor Output Register. It may also be used as an output of the MICROSEQUENCER to be used as a "data valid" signal to indicate when data is being transferred on the DB7-0 bus for interface with an external ECC chip.

DRIVE INTERFACE:

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
30	$\overline{RDATA}$	I	$\overline{\text{Read Data}}$. This signal is the serial data from the disk or tape drive. It may be encoded as RLL2, 7, MFM, FM, GCR, or NRZ as selected in MODE Register bits 2-0.
41	RGATE	O	Read Gate. This output is typically used to enable the data separator to begin locking to data. Normally, it becomes active during the PLO sync field. This signal is controllable via microcode to allow specific read data search algorithms and conformance to unique drive formats.
42	RCLK	I	Read Clock (Read/Reference Clock). This input clock is used to frame the encoded RDATA bit stream from the drive. For NRZ input data, the Read/Reference Clock signal provides the timing necessary to synchronize the serial data transfer between the drive and the MSD95C02. RCLK is divided internal to the MSD95C02 and is used to run the MICROSEQUENCER. It is therefore necessary to continually provide a glitch-free clock into this input at all times.
33	WDATA	O	Write Data. This output is the serial NRZ, FM, MFM, GCR or RLL data being written to the drive.
39	WGATE	O	Write Gate. This output is controlled by the microsequencer and is active when the MSD95C02 is writing data to the drive.

PINOUT DESCRIPTION CONTINUED

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
31	CTL1 (EARLY)	O	Control 1. Depending on the programming of the MODE Register, this bit either reflects the data written to bit 0 of the Local Processor Output Register or indicates that the current disk Write Data bit should be externally precompensated early.
32	CTL2 (LATE)	O	Control 2. Depending on the programming of the MODE 3 Register, this bit either reflects the data written to bit 1 of the Local Processor Output Register or indicates that the current disk Write Data bit should be externally precompensated late.
40	CTL3 (WRFCLK)	I/O	Control 3. Depending on the programming of the MODE 3 Register, this bit either reflects the data written to bit 2 of the Local Processor Output Register or acts as a tape write reference clock input. In tape applications that require read after write capability, this pin must be programmed as an input (WRFCLK).
38	CTL4 (AMEN)	O	Control 4. Depending on the programming of the MODE 2 Register, this bit either reflects the data written to bit 3 of the Local Processor Output Register or acts as a MICROSEQUENCER output which may be used to write an Address Mark (WGATE active) or search for an address mark (WGATE, RGATE inactive) in ESDI drive applications.
19	SNS4 (READY)	I	Sense Input 4. The MSD95C02 can be programmed to generate any level change interrupt from this pin. This input may be used to sense READY status from the drive.
20	SNS3 (CMDDN)	I	Sense Input 3. The MSD95C02 can be programmed to generate a high-to-low level change interrupt from this pin. This input may be used to indicate a Command Complete status when using ESDI drives.
21	SNS2 (ATTN/WFLT)	I	Sense Input 2. The MSD95C02 can be programmed to generate a high-to-low level change interrupt from this pin. This input may be used to sense ATTENTION status from an ESDI drive or a WRITE FAULT status from an ST-506 drive.
22	SNS1 (LDPT)	I	Sense Input 1. The MSD95C02 can be programmed to generate a high-to-low level change interrupt from this pin. This input may be used to sense load point status for tape applications.
37	TST4 (INDEX)	I	Test Input 4. This input is used by the MICROSEQUENCER for conditional branching. Typically, the INDEX pulse from the drive is connected to this pin.
36	TST3 (ECCERR)	I	Test Input 3. This input is used by the MICROSEQUENCER for conditional branching. When used with an external ECC chip, this input may be used to indicate an ECC error.
35	TST2 (IBG)	I	Test Input 2. This input is used by the MICROSEQUENCER for conditional branching. An external signal indicating interblock gap for tape applications may be connected to this pin.
34	TST1 (AMFND)	I	Test Input 1. This input is used by the MICROSEQUENCER for conditional branching. Typically, an ESDI address mark found signal is connected this pin.

PROCESSOR INTERFACE:

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
9-12, 14-17	AD7-0	I/O	Address/Data Bus. Multiplexed bi-directional address/data bus to local processor.
27	ALE ($\overline{AS}$)	I	Address Latch Enable ($\overline{\text{Address Strobe}}$). This signal is active when an address is valid on the AD7-0 bus. The local processor reads the MSD95C02 RESET Register address either following a hard or prior to a soft reset to automatically configure the MSD95C02 to expect ALE or $\overline{AS}$ at this input.
29	$\overline{INT}$	O	$\overline{\text{Interrupt}}$. This open collector output is driven low when the MSD95C02 detects an enabled interrupt. This pin has an internal MOSFET which functions as a pull-up.
26	$\overline{RD}$ ($\overline{DS}$)	I	$\overline{\text{Read Strobe}}$ ($\overline{\text{Data Strobe}}$). When the MSD95C02 is configured for ALE, this active low strobe is used to enable read data from the MSD95C02 onto the AD7-0 bus. When the MSD95C02 is configured for $\overline{AS}$, this active low signal is used to strobe data into or out of the MSD95C02.
25	$\overline{WR}$ (R/$\overline{W}$)	I	$\overline{\text{Write Strobe}}$ (Read/$\overline{\text{Write}}$). When the MSD95C02 is configured for ALE, this active low strobe is used to latch write data from the AD7-0 bus into the MSD95C02. When the MSD95C02 is configured for $\overline{AS}$, the R/$\overline{W}$ input is used to qualify DS for a read or write cycle.

PINOUT DESCRIPTION CONTINUED

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
24	$\overline{CE}$	I	$\overline{Chip\ Enable}$. This input signal is used to qualify the $\overline{RD}$ and $\overline{WR}$ strobes for all accesses on the AD7-0 bus. This signal must be valid throughout the memory cycle.
28	$\overline{LPS}$	I	$\overline{Low\ Power\ Standby}$. A low level applied to this input signifies that the system is requesting the low power standby mode.
23	$\overline{RST}$	I	$\overline{Reset}$. A low level at this input will cause the MSD95C02 to be reset (hard reset) to a known state. Reset will cause the following I/O pins to be forced to the states indicated: $\overline{DB}$7-0 Input $\overline{OE}$ Inactive High $\overline{WE}$ Inactive High $\overline{DACK}$ Inactive High RGATE Inactive Low WGATE Inactive Low $\overline{AD}$7-0 Input $\overline{INT}$ Inactive High CTL1 (EARLY) Inactive Low CTL2 (LATE) Inactive Low CTL3 (WRFCLK) Input CTL4 (AMEN) Inactive Low
18	VCC	P	Power connection
13	GND1	P	Ground connection
52	GND2	P	Ground connection

OVERVIEW OF MSD95C02 REGISTERS

Figure 5 shows the MSD95C02 address map. The 256 locations are internally decoded from the lower 8 bits of the address bus. Valid decode space exists from address 40H to FFH as shown. Address 00H to 2FH is not decoded by the MSD95C02 and can be used as register space for the External Device. The MSD95C00 SCSIC uses address 00H to 0FH for its internal register space, allowing the MSD95C00 and the MSD95C02 to share the same chip select decoded from the upper address bits of the local processor's address bus.

The MSD95C02 address space accessible to the local processor can be broken into four sections as follows:

ADDRESS 40H-5FH

This address space contains the MSD95C02 working registers which include mode registers, setup registers, interrupt enable registers, status registers, and DMA parameter registers.

ADDRESS 60H-6FH

This address space contains an on-chip 16 byte register file referred to as the DESIRED REGISTER FILE. It is shared by the local processor and the MICROSEQUENCER and is typically loaded by the local processor and internally compared with data from the disk. Local processor access to this address space should only occur when the MICROSEQUENCER is not running.

ADDRESS 70H-7FH

This address space contains an on chip, 16 byte, register file referred to as the CURRENT REGISTER FILE. It is shared by the local processor and the MICROSEQUENCER and is typically loaded with data from the disk for examination later by the local processor. Local processor access to this address space is only allowed during certain MICROSEQUENCER initiated interrupts to the local processor.

ADDRESS 80H-FFH

This address space contains the 128 bytes of loadable microcode used by the MICROSEQUENCER. Internally, these bytes are arranged as 32 locations by 32 bits wide. Local processor address 80H corresponds to the least significant byte (D7-0) of word zero of the microcode RAM. This address space should not be accessed by the local processor while a microprogram is running.

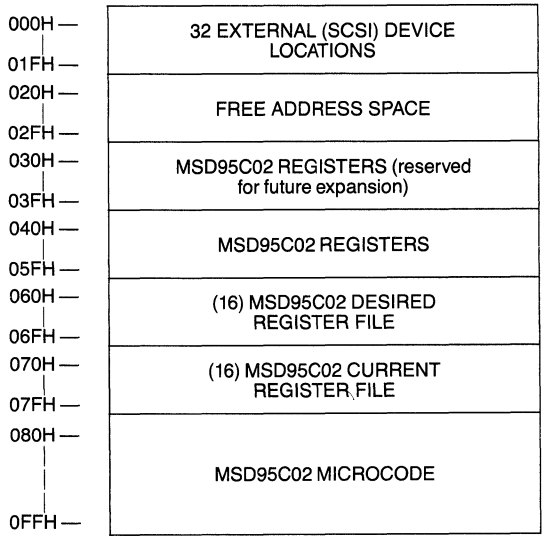


FIGURE 5: MSD95C02 ADDRESS MAP

Figure 6 shows the internal block diagram of the MSD95C02. The data flow through the chip occurs on the INBUS and the OUTBUS. The OUTBUS connects all data coming from the ring buffer to the drive and the INBUS connects all data from the drive to the ring buffer. There are six blocks that make up the MSD95C02 disk controller as shown in the block diagram. Each block will be described in detail in the following sections.

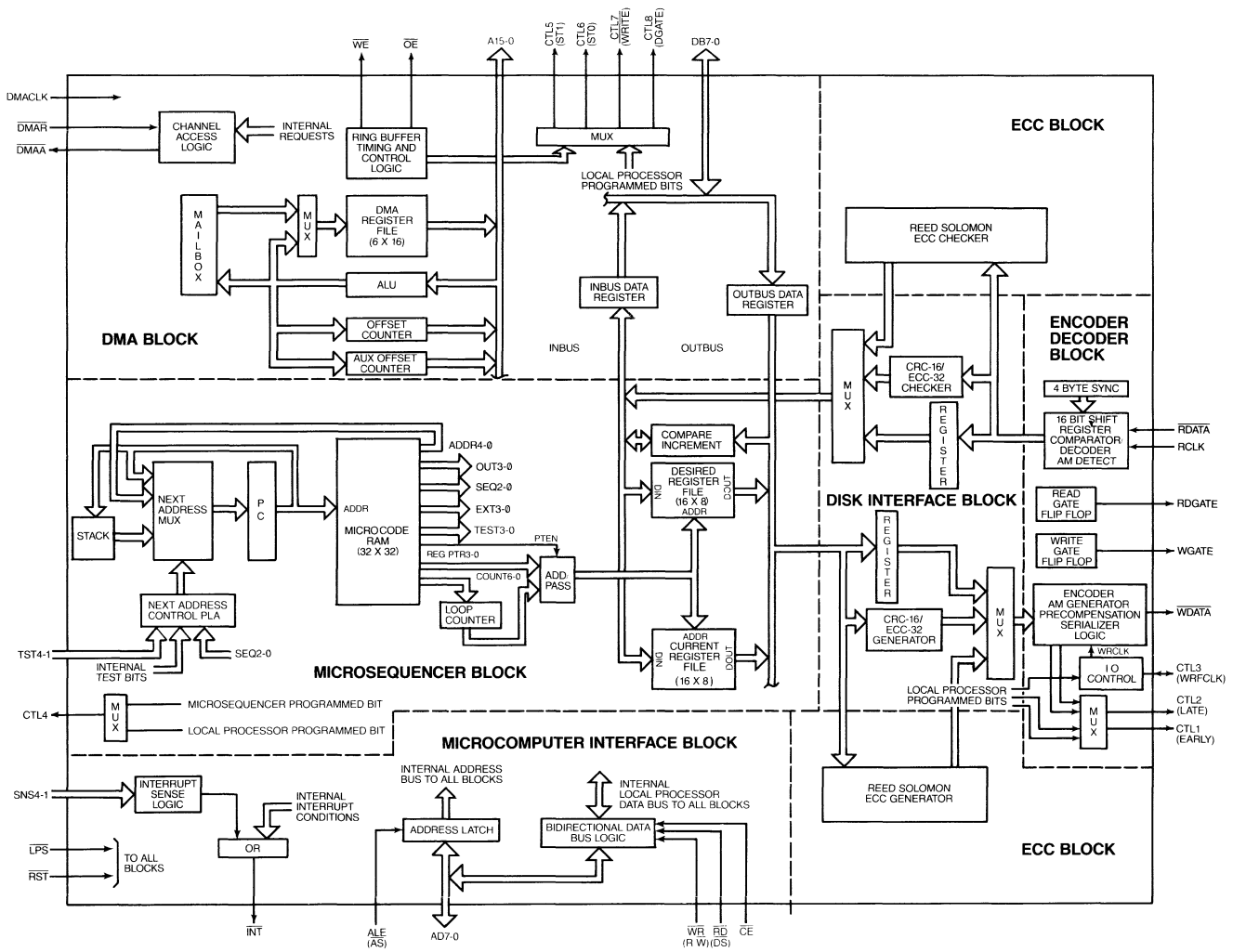
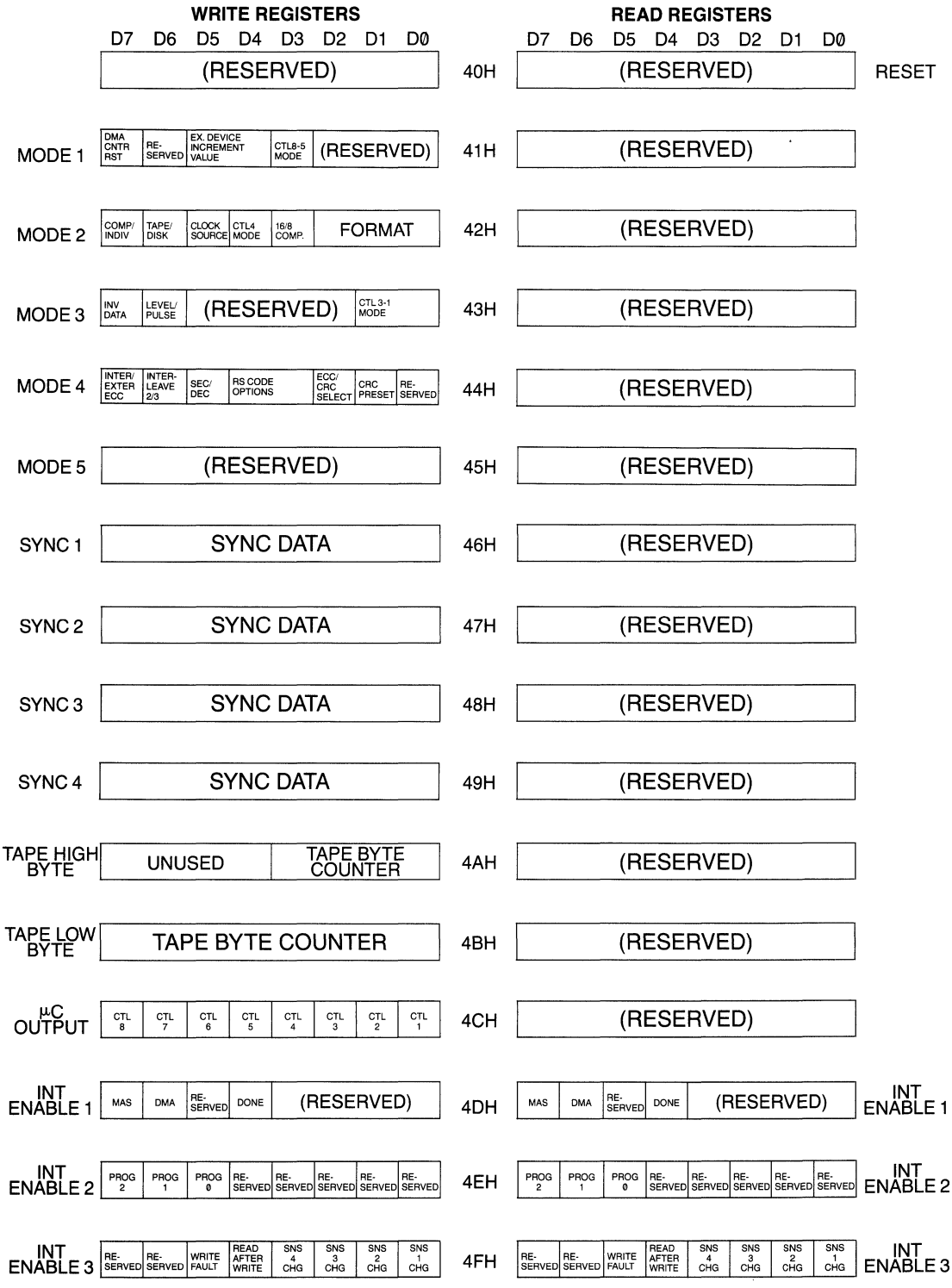
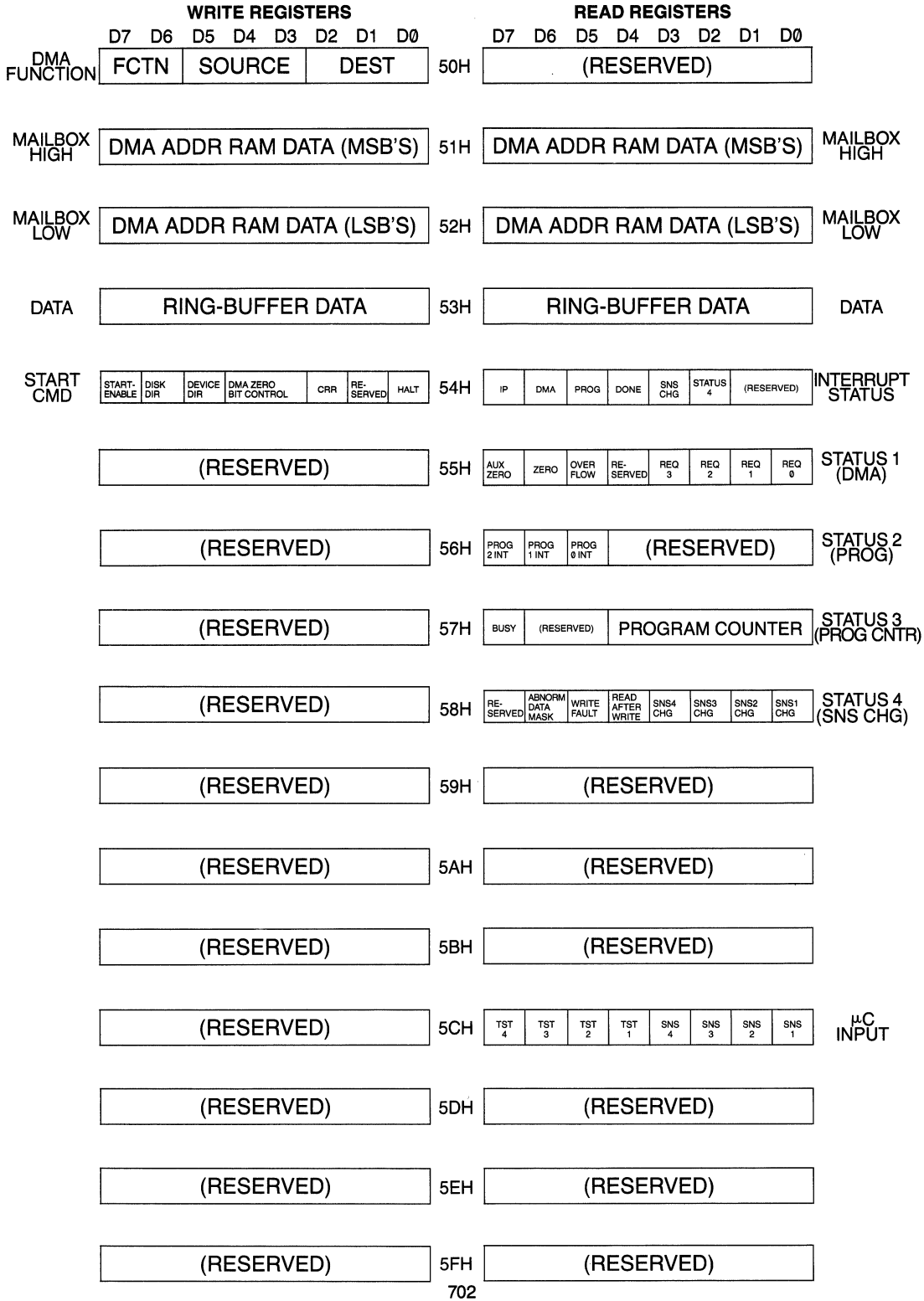


FIGURE 6: MSD95C02 INTERNAL BLOCK DIAGRAM

MSD95C02 REGISTERS




WRITE REGISTERS
READ REGISTERS
D7 D6 D5 D4 D3 D2 D1 D0
DMA FUNCTION
FCTN
SOURCE
DEST
50H
(RESERVED)
MAILBOX HIGH
DMA ADDR RAM DATA (MSB'S)
51H
DMA ADDR RAM DATA (MSB'S)
MAILBOX LOW
DMA ADDR RAM DATA (LSB'S)
52H
DMA ADDR RAM DATA (LSB'S)
DATA
RING-BUFFER DATA
53H
RING-BUFFER DATA
START CMD
START-ENABLE
DISK DIR
DEVICE DIR
DMA ZERO BIT CONTROL
CRR
RE-SERVED
HALT
54H
IP
DMA
PROG
DONE
SNS CHG
STATUS 4
(RESERVED)
INTERRUPT STATUS
(RESERVED)
55H
AUX ZERO
ZERO
OVER FLOW
RE-SERVED
REQ 3
REQ 2
REQ 1
REQ 0
STATUS 1 (DMA)
(RESERVED)
56H
PROG 2 INT
PROG 1 INT
PROG 0 INT
(RESERVED)
STATUS 2 (PROG)
(RESERVED)
57H
BUSY
(RESERVED)
PROGRAM COUNTER
STATUS 3 (PROG CNTR)
(RESERVED)
58H
RE-SERVED
ABNORM DATA MASK
WRITE FAULT
READ AFTER WRITE
SNS4 CHG
SNS3 CHG
SNS2 CHG
SNS1 CHG
STATUS 4 (SNS CHG)
(RESERVED)
59H
(RESERVED)
(RESERVED)
5AH
(RESERVED)
(RESERVED)
5BH
(RESERVED)
(RESERVED)
5CH
TST 4
TST 3
TST 2
TST 1
SNS 4
SNS 3
SNS 2
SNS 1
µC INPUT
(RESERVED)
5DH
(RESERVED)
(RESERVED)
5EH
(RESERVED)
(RESERVED)
5FH
(RESERVED)

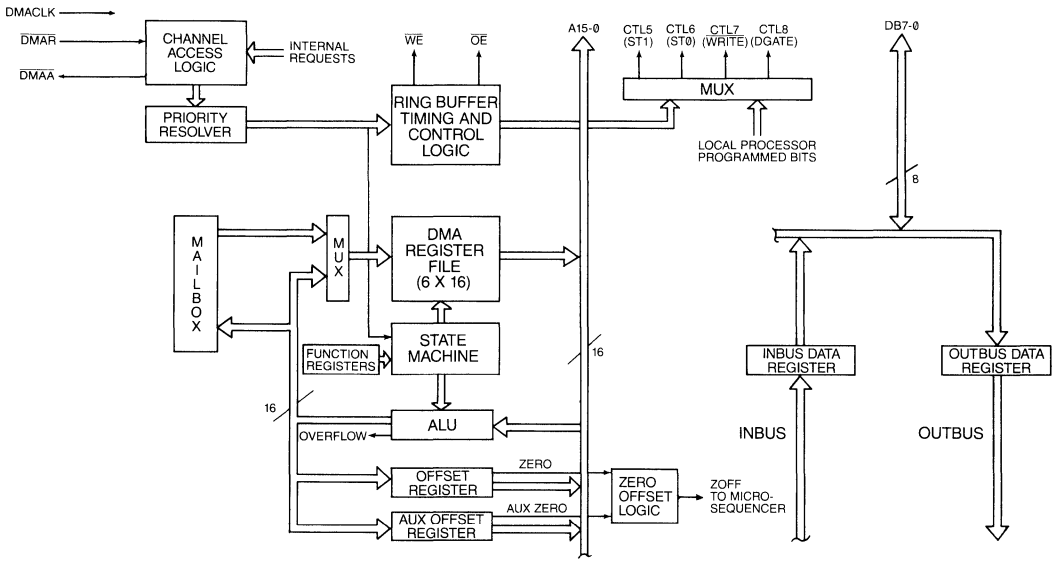


FIGURE 7: DMA BLOCK DIAGRAM

DESCRIPTION OF INDIVIDUAL BLOCKS

DMA CONTROLLER

The three channel DMA controller is composed of a 6 X 16 bit register file, two OFFSET COUNTERS for monitoring ring buffer full/empty status, a DMA FUNCTION Register to indirectly address the register file, a ring buffer DATA Register, and ALU to perform incrementing (by 1, 2, 3 or 4) and in addition, a 16 bit mailbox register, state controller and DMA request priority resolver.

Channel access to the ring buffer comes from three sources. The MICROSEQUENCER requests are initiated by the DISK INTERFACE block for every byte transferred to/from the MICROSEQUENCER and is given top priority. Local processor accesses to the ring buffer are initiated by direct operation of the local processor on the addressable registers within the DMA controller. The local processor is given second priority. External Device access (like SCSI) is initiated via a DMA request-acknowledge handshake and is given third priority.

ALU and Register function:

For each DMA channel, specific register manipulations are possible depending upon the operation required. Each channel will have different requirements on the way the address to the ring buffer is updated. For instance, during disk read operations, the channel must ensure that the starting address for a sector transfer is not updated until the data transferred into the ring buffer is known to be error free. The External Device, during a read operation from the ring buffer, must cause the address to be incremented for each byte transferred. It must also update the OFFSET COUNTER since there is a relationship between the value in the OFFSET COUNTER and the amount of available free space there is in the buffer and available error free data there is to transfer out on the External channel. The local processor channel might be required to perform read modify write routines during error correction operations.

Local Processor channel operation:

The local Processor can specify the address operation to be performed during its channel access via the DMA FUNCTION Register which is a write only local processor addressed register (assigned address 50HEX). This function register permits the loading of all registers in the register file which are not directly addressable from the external local processor.

The Local Processor can directly access four registers in the DMA controller. They are:

DMA FUNCTION Register (write only) address 50H
MAILBOX HIGH Register (read/write) address 51H
MAILBOX LOW Register (read/write) address 52H
DATA Register (read/write) address 53H

The local processor can indirectly access 6 additional 16 bit registers that make up the DMA register file. These registers are accessed by using the DMA FUNCTION Register. An example of their use is illustrated as follows:

CONSTANT 1—Normally used to hold the sector size and in calculating address updates and ring buffer status flags.

CONSTANT 2—Normally used to hold a number that is a function of the Ring Buffer size for generating Ring Buffer empty/full status.

LOCAL PROCESSOR ADDRESS Register—Holds the current address of a local processor to ring buffer data transfer.

EXTERNAL DEVICE ADDRESS Register—Holds the current address of an External Device to ring buffer data transfer.

DISK Register—Maintains the address of the first location of a MICROSEQUENCER initiated disk transfer until data integrity is established.

DISK ADDRESS Register—Holds the current address of a MICROSEQUENCER initiated disk ring buffer data transfer.

Refer to Appendix 2 for a description of how these registers are set up for particular DMA operations.

DMA FUNCTION Register:

BITS D7-D6. These bits specify the operation to be performed on the contents of a register in the internal register file:

D7	D6	FUNCTION
0	0	SOURCE + OFFSET COUNTER → DESTINATION (Note 1)
0	1	SOURCE + N → DESTINATION; DECREMENT OFFSET COUNTER
1	0	SOURCE → DESTINATION
1	1	SOURCE + N → DESTINATION

TABLE 1: DMA FUNCTION REGISTER OPERATION

N = 1 for disk and local processor data transfers
N specified by MODE 1 Register for External channel (SCSI) data transfers

Notes:

1. For this case, the only destinations that can be updated are the OFFSET COUNTER and the MAILBOX. All other destinations will cause the OVERFLOW flag to be updated as a function of the result out of the ALU, but will not update the destination.

2. When the controller changes the contents of the OFFSET and AUXILIARY OFFSET COUNTERS, it must set or clear the zero bit via the START COMMAND Register bits 4 and 3.

3. The OFFSET COUNTER cannot be used as a source. If it is used as a source, it will take on the value of zero. During error correction, it becomes necessary to use the OFFSET COUNTER as a source. See appendix 3 for a description of ERROR CORRECTION ON THE FLY for more detail.

BITS D5-D3. Source register file Address
BITS D2-D0. Destination register file Address

These bits select the register file address location(s) accessed by the operation specified by bits D7 and D6.

D5	D4	D3	
D2	D1	D0	REGISTER SELECTED
0	0	0	MAILBOX HIGH, LOW
0	0	1	OFFSET COUNTER
0	1	0	CONSTANT 1
0	1	1	CONSTANT 2
1	0	0	LOCAL PROCESSOR ADDRESS
1	0	1	EXTERNAL DEVICE ADDRESS
1	1	0	DISK REGISTER
1	1	1	DISK ADDRESS

TABLE 2: DMA FUNCTION REGISTER SOURCE/DEST

Disk Channel Access Operation:

Disk requests for data transfer are initiated by the MSD95C02's internal MICROSEQUENCER. For normal data transfer between the disk and the ring buffer, the MICROSEQUENCER causes the DISK ADDRESS in the DMA block to be incremented by one between ring buffer access cycles.

In addition, the MICROSEQUENCER may perform some housekeeping functions at each sector boundary if required. These housekeeping functions may include updating the OFFSET COUNTER, determining buffer full/empty status, etc.

In order to specify one of many housekeeping calculations, the MSD95C02's internal MICROSEQUENCER has the ability to specify the operation by loading a DISK DMA FUNCTION Register (different from the local processor addressable DMA FUNCTION Register). The bit definitions of this register are identical to the DMA FUNCTION Register as defined in Tables 1 and 2. The MICROSEQUENCER can load the DISK DMA FUNCTION Register by transferring a value previously stored in the DESIRED REGISTER FILE to the DMA block.

EXTERNAL DEVICE CHANNEL ACCESS OPERATION:

Upon an external DMA request, this channel will perform one hardwired function consisting of proper adjustment of the current ring buffer address as well as decrementing the OFFSET COUNTERs for current handling of ring buffer full/empty situations. The MSD95C02 can buffer a maximum of 12 DMA requests before issuing an acknowledgment without causing an overrun/underrun condition. The MSD95C02 uses the leading edge of DMA Request to post the EXTERNAL channel access. This permits the MSD95C02 to work with several REQ-ACK timing situations.

For External Device DMA operations, the DMA hardwired function performed is:

EXTERNAL DEVICE ADDRESS + N → EXTERNAL DEVICE ADDRESS.

N is used to permit various data bus widths between the ring buffer and the External Device as shown in table 3.

N	DATA BUS WIDTH
1	8 BITS
2	16 BITS
3	24 BITS
4	32 BITS

TABLE 3: EXTERNAL DEVICE BUS WIDTHS AS A FUNCTION OF N

The value N is programmed by the Local Processor in MODE 1 Register, bits 5 and 4.

OFFSET COUNTER:

The OFFSET COUNTER is part of the automatic housekeeping function of the DMA block and is used to keep track of buffer empty/full conditions.

During External Device to Ring Buffer to Disk operations (WRITE the disk), the OFFSET COUNTER keeps track of the number of free bytes left in the buffer. Whenever the Ring buffer size minus the OFFSET COUNTER is less than the sector size (indicating that there is less than a sector's worth of data in the ring buffer), the disk WRITE is temporarily held off. The throttling of the Disk DMA channel as a function of buffer space status is done automatically by the DMA controller without local processor intervention.

During Disk to Ring Buffer to External Device (READ the disk) operations, the OFFSET COUNTER keeps track of

the total data bytes left in the buffer. Whenever the Ring Buffer size minus the OFFSET COUNTER is less than the sector size (indicating that there is not enough room in the buffer to accept another sector), the disk READ is temporarily held off. The throttling of the Disk DMA channel as a function of buffer space status is done automatically by the DMA controller without local processor intervention.

Decisions by the MICROSEQUENCER regarding buffer empty/full status are made by interrogating the ZOFF flag whenever an ALU operation loads a zero into the OFFSET COUNTER.

AUXILIARY OFFSET COUNTER operation:

The AUXILIARY OFFSET COUNTER is loaded and modified along with the OFFSET COUNTER. It is required because data transferred from the disk into the Ring Buffer might contain errors. Because of this, the AUXILIARY OFFSET COUNTER might be different from the OFFSET COUNTER and is used to control the flow of data between the External Device and the Ring Buffer. During External Device to Ring Buffer transfers, the AUXILIARY OFFSET COUNTER keeps track of the number of free bytes left in the buffer. During Ring Buffer to External Device transfers, the AUXILIARY OFFSET COUNTER keeps track of the number of error free data bytes left in the buffer.

The OFFSET and AUXILIARY OFFSET COUNTERS are linked together until an error is detected on data read from the disk. When this occurs, only the OFFSET COUNTER is incremented as new data is transferred from the disk to the Ring Buffer. The AUXILIARY OFFSET COUNTER is not incremented until the error is corrected. Both counters are decremented when data is transferred from the Ring Buffer to the External Device. If the error is corrected before the AUXILIARY OFFSET COUNTER is decremented to zero, then the two counters are linked back together by transferring the contents of the OFFSET COUNTER into the AUXILIARY OFFSET COUNTER in response to a DMA FUNCTION Register command. If the AUXILIARY OFFSET COUNTER is decremented to zero before the error is corrected, the MSD95C02 will not respond to DMA requests from the external device until the AUXILIARY OFFSET COUNTER and OFFSET COUNTER are linked back together. See Appendix 4 for a further description of the OFFSET and AUXILIARY OFFSET COUNTERs during error correction on the fly.

Status Flags:

The DMA block will generate three status flags which can be used by the MICROSEQUENCER to test and make decisions on the microprogram flow. These three status flags, defined as follows, are also readable by the Local Processor in STATUS 1 Register (ADDR 55H):

OVERFLOW: This flag indicates the result of the current operation performed by the ALU; if the arithmetic yields an overflow, this bit will be set. This bit is available to the Local Processor in STATUS 1 Register, bit D5.

ZERO: This flag is set to a one when the OFFSET COUNTER is decremented to zero. This bit is available to the Local Processor in STATUS 1 Register, bit D6.

AUX ZERO: This flag is set to a one when the AUXILIARY OFFSET COUNTER is decremented to zero. This bit is available to the Local Processor in STATUS 1 Register, bit D7.

The ZERO and AUX ZERO flags are not set if the OFFSET and AUXILIARY OFFSET COUNTERS are loaded with a zero.

The MICROSEQUENCER can interrogate the logical OR of the ZERO and AUX ZERO flags via the test input ZOFF.

ECC ON THE FLY:

The three channel DMA arrangement provides the user with the ability to perform error correction on the fly without loss of a disk revolution. In general, upon disk read operations, one sector may be transferred from the Ring Buffer over the EXTERNAL channel, one sector may be operated on by the Local processor for error correction, and the third sector may be read from the disk and written into the Ring Buffer. Refer to Appendix 4 for further description of ECC on the fly.

MICROSEQUENCER

As shown in Figure 8, the MICROSEQUENCER consists of a 32 X 32 microcode RAM, a 7 bit loop counter, a one address STACK, a sophisticated next address generator and two 16 byte register files. During next address generation, the Program Counter can be loaded from the STACK, from the ADDRESS FIELD output by the microcode RAM (ADDR 4-0), or from the current or incremented value in the Program Counter.

The Local Processor can initiate Command execution (eg. a Read Command) by writing to the COMMAND START Register (ADDR 54 HEX). The MSD95C02 will then begin execution at address zero in the microcode RAM. From this time until the command terminates, program flow is dependent on which of the several sources are specified when the Program Counter is loaded. Selection of the next address is dependent on the Sequence control field (SEQ 2-0), and internal and external test points which are input to the Next Address Control PLA. Test points are chosen via the Test field (TEST 3-0) for interrogation and program flow of the MICROSEQUENCER.

Contained within the MICROSEQUENCER block are two, 16 byte register files named DESIRED and CURRENT REGISTER FILEs. In general, the MICROSEQUENCER reads the DESIRED REGISTER FILE and writes the CURRENT REGISTER FILE. The Local Processor can read or write either register file. Local Processor access to these register files are restricted and controlled by interrupts generated by the MICROSEQUENCER to the Local Processor. This limited access is required to resolve the access contentions to these register files by both the Local Processor and the MICROSEQUENCER.

In addition to the DESIRED and CURRENT REGISTER FILEs, there is a comparator structure set up to compare contents in the two register files as shown in Figure 8. Any information loaded by the local processor in the DESIRED REGISTER FILE may be compared with the data that is deposited in the CURRENT REGISTER FILE as it is filled with data read from the disk. The sequence and number of compares made are all initiated under MICROSEQUENCER control. Typically, the compares can be performed to determine whether a particular ID field had been encountered.

The contents of any DESIRED REGISTER FILE location can be incremented under MICROSEQUENCER control. Typically, this can be used to increment the sector number in the DESIRED REGISTER FILE location when performing consecutive logical sector operations.

In addition, the CURRENT REGISTER FILE can, under MICROSEQUENCER control, be loaded with the error syndrome bytes for examination by the Local Processor during an error correction operation.

In typical applications, the CURRENT REGISTER FILE holds data such as the current header information (head #, sector #, track #) and the writing to these registers is controlled by the MICROSEQUENCER as data is converted from serial to parallel in the DISK INTERFACE block. The

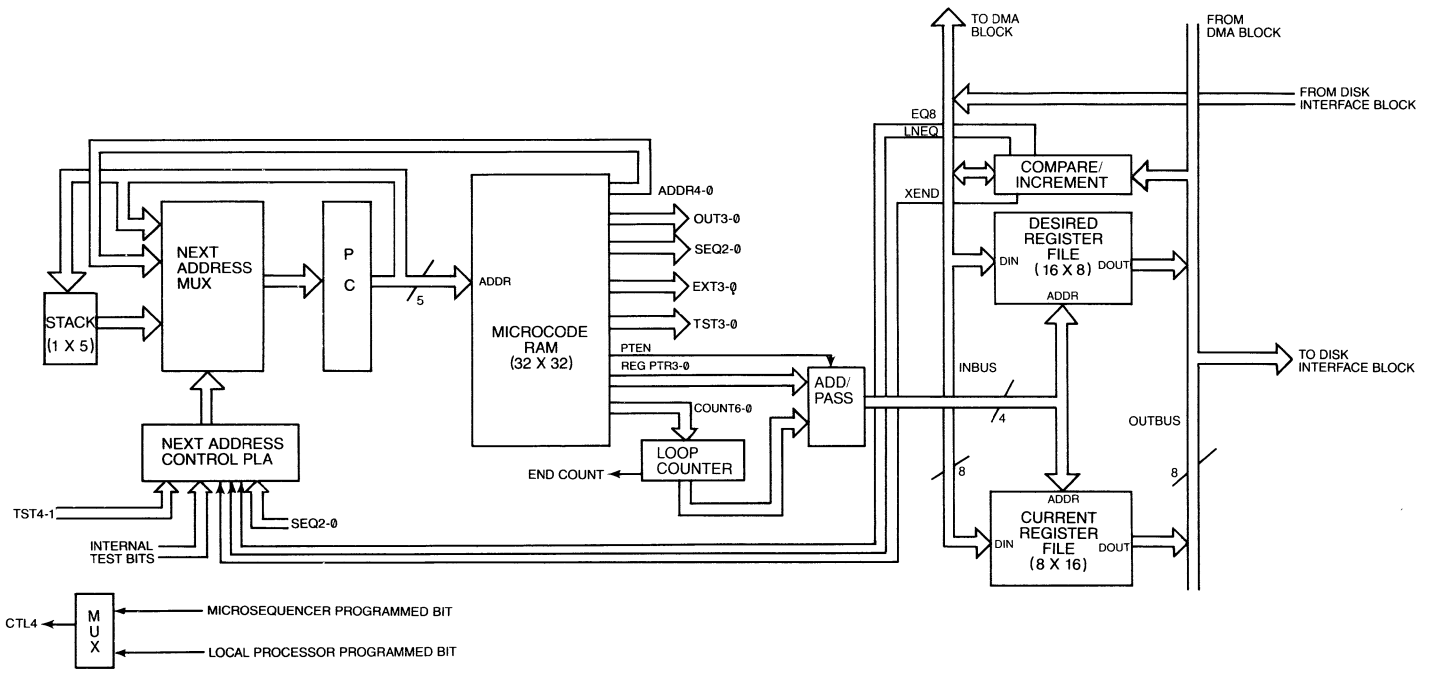


FIGURE 8: MICROSEQUENCER BLOCK DIAGRAM

DESIRED REGISTER FILE holds information such as the desired sector to be operated on in a READ or WRITE DISK operation. The desired header information, in this case is written into the DESIRED REGISTER FILE by the Local Processor prior to the execution of the READ OR WRITE command in an order that is consistent with the order in which the MICROSEQUENCER loads and compares the CURRENT REGISTER FILE.

The 32 bit microprogram word definition contains a total of 8 separate fields as shown in Figure 9.

DESCRIPTION OF INDIVIDUAL FIELDS:

SEQUENCE CONTROL FIELD (D31-29):

The SEQUENCE CONTROL FIELD determines the next address loaded into the PROGRAM COUNTER which feeds the MICROSEQUENCER RAM. Depending upon which SEQUENCE CONTROL FIELD is specified, the next address might remain at the current address, increment, use the value stored in the STACK, or use the value specified in the ADDRESS FIELD. In addition, it can cause the current value in the PROGRAM COUNTER to be pushed on the STACK. The STACK is one address deep. The END COUNT and TEST POINT can affect the next address generation and STACK operations in a number of ways. See section on the TEST FIELD and COUNT FIELD for a description of the various conditions that will produce a valid TEST POINT or END COUNT.

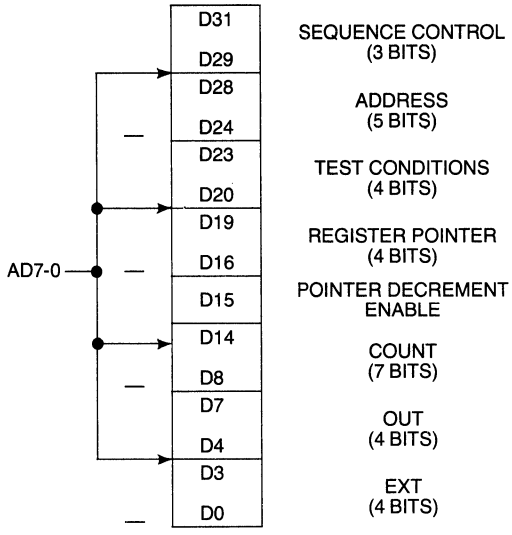


FIGURE 9: 32 BIT MICROSEQUENCER PROGRAM WORD DESCRIPTION

SEQUENCE CONTROL FIELD DEFINITION:

MNEMONIC	D31-29	OPERATION	TEST POINT END COUNT	1 1	1 0	0 1	0 0
SHLP (SHORT LOOP)	0 0 0	PC = STACK =		PC+1 D28-24	PC —	PC+1 —	PC —
LGLP (LONG LOOP)	0 0 1	PC = STACK =		PC+1 D28-24	PC —	PC+1 —	PC —
RC (RETURN OR CALL)	0 1 0	PC = STACK =		STACK —	PC —	D28-24 PC+1	PC —
CI (CALL OR INCREMENT)	0 1 1	PC = STACK =		D28-24 PC+1	PC —	PC+1 —	PC —
TSJ (TEST JUMP)	1 0 0	PC =		PC+1	PC+1	D28-24	PC
TSC (TEST CALL)	1 0 1	PC = STACK =		PC+1 —	PC+1 —	D28-24 PC+1	PC —
TSJL (TEST JUMP LONG)	1 1 0	PC =		PC+1	PC+1	D28-24	PC
TSCL (TEST CALL)	1 1 1	PC = STACK =		PC+1 —	PC+1 —	D28-24 PC+1	PC —

1. DS28-24 is the address as specified in the ADDR field of the microcode word.
2. — = no change.

ADDRESS FIELD (D28-24):

The Address Field bits in the microcode instruction may be directly loaded into the Program counter when executing "jump" and "call" instructions. When executing a call instruction, the current (or next) Program Counter value may be saved on a one address STACK. "Return" instructions can be implemented by loading the contents of the STACK back into the Program Counter. It should be noted that subroutines can only be nested one deep.

TEST CONDITIONS FIELD (D23-20):

The test condition field permits the MICROSEQUENCER to test one of 16 conditions for the purpose of conditional jumps and calls as specified in the SEQUENCE CONTROL FIELD. These 16 inputs originate in the MICROSEQUENCER block and other blocks and four of the test points are general purpose inputs from outside the MSD95C02 appearing on pins TST1-4.

TEST FIELD DEFINITION:

D23	D22	D21	D20	TEST POINT SELECTED	DEFINITION
0	0	0	0	FORCE ZERO	Forces the TEST input to a logic zero.
0	0	0	1	DC GAP	From the ENCODER/DECODER block indicating that no transitions have occurred on the RDATA input pin for 15 WRFCLKs.
0	0	1	0	SYNC	From the DISK INTERFACE block indicating a 16 bit high speed compare between disk data and the MICROSEQUENCER selected SYNC Register(s).
0	0	1	1	NDERR	From the DISK INTERFACE block indicating that a CRC-16, ECC-32 or Reed Solomon ECC data error has occurred. A zero indicates a data error.
0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	TST1 TST2 TST3 TST4	Input pin TST1. Input pin TST2. Input pin TST3. Input pin TST4.
1	0	0	0	EQ8	This input reflects the status of an 8 bit compare between the INBUS and the DESIRED REGISTER FILE.
1	0	0	1	LNEQ	Indicates that one of the previous 8 bit compares or the current 8 bit compare is not equal.
1	0	1	0	XEND	Indicates that the contents of a DESIRED REGISTER FILE location has been incremented to all zeros.
1	0	1	1	NTP2	This is an auxiliary test input which is the logical OR of three independent conditions. It is equal to either a HALT (local processor initiated via Register 54, bit 0), an ABNORMAL DATA MARK (Register 58H, bit 6) or a WRITE FAULT (Register 58H, bit 5). A zero indicates that one of the conditions is true.
1	1	0	0	CMD	Originates in the DMA block and indicates if the command loaded by the local processor is a READ or WRITE Command with respect to the Disk. This operation tests bit 6 inverted in the START COMMAND Register. A one is a disk write and a zero is a disk read.
1	1	0	1	NOVERFLOW	Originates from the DMA block. This test input is a logic one if the result of an ALU operation has not yielded an overflow and NTP2 is a logic one.
1	1	1	0	ZOFF	Originates from the DMA block and indicates when either the OFFSET or AUXILIARY OFFSET COUNTER is loaded with a zero as a result of an ALU operation.
1	1	1	1	ONE	Forces the TEST input to a logic ONE.

REGISTER POINTER FIELD (D19-16):

The REGISTER POINTER FIELD is associated with the DESIRED and CURRENT REGISTER FILES and specifies the address of the particular register file location to be operated on. The DESIRED and CURRENT REGISTER FILEs have a common address such that the same corresponding location in each file may be operated on at the same time.

POINTER DECREMENT FIELD (D15):

This one bit field permits one to access sequentially decrementing locations in the DESIRED and CURRENT REGISTER FILEs for multiple operations within these registers. If the Pointer Decrement enable bit is zero, the Register Address will be the value specified in the Register Pointer field. If the Pointer Decrement enable bit is one, the Register Address will be the value specified in the Register Pointer field added to the current contents of the Loop Counter. When accessing sequential register file locations, the Count field should be initialized to the number of sequential access required and the REGISTER POINTER FIELD should be initialized to the last sequential register file location to be accessed. At each MICROSEQUENCER clock, the loop counter in the instruction is decremented, thus permitting sequential access at the MICROSEQUENCER clock frequency.

COUNT FIELD (D14-8):

This field serves two functions. First, it is loaded into the loop counter for counting microinstruction loops. In this instance, the generation of an END COUNT status bit, will cause branching conditions as defined by the SEQUENCE CONTROL FIELD (D31-29). The END COUNT status bit will be set to a logic one when the loop counter is decremented to zero. The second function of this field is for accessing sequential locations of the DESIRED and CURRENT REGISTER FILEs as described in the POINTER DECREMENT ENABLE FIELD.

It should be noted that the count value is loaded into the loop counter as the microinstruction containing it is exited.

The loop counter is decremented every microinstruction clock or every 128th microinstruction clock for a short loop (SHLP) or a long loop (LGLP) respectively. To perform a count of N, the value N-1 should be specified in the previous instruction in the microcode since the loop counter gets loaded as an instruction is exited.

OUT FIELD (D7-4):

The out field is one of two control fields used to control internal and external operations during microprogram execution. This four bit field yields one of 16 control outputs as follows:

OUT FIELD DEFINITION:

MNEMONIC	D7-D4	OPERATION
NOP	0 0 0 0	No operation.
CNTRL4	0 0 0 1	To DISK INTERFACE block causing the output CTL 4 to change. This output is multiplexed with a programmable output controlled by the local processor. This signal may be used for an external address mark enable when interfacing with ESDI drives.
RDG	0 0 1 0	To the DMA block. This signal is a DMA request from the MICROSEQUENCER and enables disk data to get transferred to the DATA Register in the DMA block over the INBUS. It also can cause the output DG (Data Gate) to go active. The DG output is multiplexed with a programmable output controlled by the local processor.
	0 0 1 1	RESERVED FOR FUTURE USE.
WPRE	0 1 0 0	This signal allows the PLO SYNC (preamble) data stored in the DESIRED REGISTER FILE to be loaded into the ENCODER/DECODER/DISK INTERFACE block over the OUTBUS. In addition, it is used to preset all CRC and ECC generation logic.
WMISS	0 1 0 1	This signal allows the missing clock data pattern stored in the DESIRED REGISTER FILE to be loaded into the ENCODER/DECODER/DISK INTERFACE block over the OUTBUS and generate the missing clock pattern when shifting the data out to the disk. In addition, it is used to start all CRC and ECC generation logic.
FREG	0 1 1 0	This signal gates the data stored in the DESIRED REGISTER FILE on to the OUTBUS.
SNDRM	0 1 1 1	This signal gates the error syndrome (from the selected error checker) to the DESIRED REGISTER FILE.
PREQ1	1 0 0 0	This signal causes the contents of the DESIRED REGISTER FILE pointed to by the register pointer field to be loaded into the DISK DMA FUNCTION Register.
WCRC	1 0 0 1	This signal gates the check bytes (CRC-16, ECC-32 Reed Solomon ECC) out to the disk.
	1 0 1 0	RESERVED FOR FUTURE USE.
	1 0 1 1	RESERVED FOR FUTURE USE.
PINT0	1 1 0 0	This signal sets bit 5 of STATUS 2 Register (ADDR 56H) and will, if enabled, generate an interrupt to the Local Processor. In addition, this interrupt will permit the Local Processor to access the CURRENT REGISTER FILE. It also separates the OFFSET and the AUXILIARY OFFSET COUNTERS. Typically, this interrupt is used for error correction operations. See description of STATUS 2 Register.
PINT1	1 1 0 1	This signal sets bit 6 of STATUS 2 Register (ADDR 56H) and will, if enabled, generate an interrupt to the Local Processor. In addition, this interrupt will permit the Local Processor to access the CURRENT REGISTER FILE. Typically, this interrupt may be used to permit the Local Processor to read the current ID information that is stored in the CURRENT REGISTER FILE.
PINT2	1 1 1 0	This signal will, if enabled, generate an interrupt to the Local Processor. This interrupt is general purpose and can be generated upon recognition of any MICROSEQUENCER detectable condition. The generation of this interrupt will affect no additional hardware.
DNINT	1 1 1 1	This signal sets bit 4 of the interrupt STATUS 2 Register (ADDR 56 H) and will, if enabled, generate an interrupt to the Local Processor. Typically, this signal is invoked to inform the Local Processor that the current command executed by the MICROSEQUENCER has been completed. Generation of this signal will stop the MICROSEQUENCER, reset BUSY (STATUS 3 Register, Bit D7), and set done (INTERRUPT STATUS Register, Bit D4). In addition, this interrupt will permit the Local Processor to access the CURRENT REGISTER FILE.

EXT FIELD (D3-0):

The EXT field is one of two control fields used to control internal and external operations during microprogram execution. This four bit field yields one of 16 control outputs as follows:

EXT FIELD DEFINITION:

MNEMONIC	D3-D0	OPERATION
NOOP	0 0 0 0	No operation.
SWDG	0 0 0 1	This signal posts a DMA request for the MICROSEQUENCER to the DMA block and is used during disk write operations. The signal allows data to be transferred from the DATA Register in the DMA block to the DISK INTERFACE and ENCODER/DECODER blocks. It also generates the DG (Data Gate) signal.
SRCRC	0 0 1 0	This signal is used to inform the CRC-16 or ECC-32 CHECKER that the respective code is being transferred from the disk.
SRECC	0 0 1 1	This signal is used to inform the Reed Solomon ECC CHECKER that the ECC bytes are being transferred in from the disk.
SGAP	0 1 0 0	This signal enables the gap detect logic.
SPRE	0 1 0 1	This signal enables the compare between incoming data and the value programmed in the appropriate SYNC register(s). Normally, this comparison is used to detect a PLO SYNC (preamble) data pattern. The RGATE signal is also set.
SMC	0 1 1 0	This signal enables the compare between incoming data and the value programmed in the appropriate SYNC register(s). Normally, this comparison is used to detect a missing clock data pattern. The RGATE signal is also set.
SDM	0 1 1 1	This signal enables the compare between incoming data and the value programmed in the appropriate SYNC register(s). Normally, this comparison is used to detect a data mark data pattern. The RGATE signal is also set.
SGOFF (1)	1 1 0 0	This signal resets both RGATE and WGATE.

NOTE: The signals above describe operations to be performed as the instruction containing them is exited (The PC is changed). The following signals will be invoked when the instruction containing them is entered.

MNEMONIC	D3-D0	OPERATION
TREG	1 0 0 0	This signal gates the contents of the INBUS into the CURRENT REGISTER FILE as pointed to by the REGISTER POINTER FIELD.
	1 0 0 1	RESERVED FOR FUTURE USE.
CRC16	1 0 1 0	This signal presets the CRC-16 generation and detection logic.
ECC32	1 0 1 1	This signal presets the ECC-32 or the Reed Solomon generation and detection logic.
ZRCLR	1 1 0 1	This signal clears the ZERO and AUX ZERO flags in the DMA block.
INCE	1 1 1 0	This signal causes the contents of the DESIRED REGISTER FILE pointed to by the register pointer field to be incremented and placed back into the same DESIRED REGISTER location.
WGON	1 1 1 1	This signal sets WGATE on.

(1) The signal SGOFF is shown out of numerical sequence to permit it to be grouped accordingly.

DISK INTERFACE & ENCODER/DECODER BLOCK

This block interfaces to the rest of the chip via the INBUS and the OUTBUS which connects the serial to parallel/parallel to serial converters to the DESIRED and CURRENT REGISTER FILES and the appropriate data registers within the DMA block.

In addition to serialization and deserialization of data, this block will perform complex high speed compare logic that can sequentially compare a bit pattern read from the disk of up to 32 bits in length. Any and all compares can detect a predefined missing clock pattern. The sequence of comparisons made prior to declaring a valid synchronization with the rotating media, is fully programmable under MICROSEQUENCER control. During write disk operations, this block can generate fully programmable formats and complex missing clock data patterns completely under MICROSEQUENCER control.

The encoder/decoder section is local processor programmable to handle FM, MFM, RLL 2, 7 and GCR codes. Included in this block is the CRC-16 and IBM AT compatible 32 bit ECC generator and checker.

REED SOLOMON ERROR CORRECTION BLOCK

The REED SOLOMON ECC block has been optimized to permit single and double burst error correction while simultaneously reducing the probability of miscorrection and expanding the error detection capability dramatically.

FUNDAMENTALS OF REED-SOLOMON ERROR CORRECTING CODES

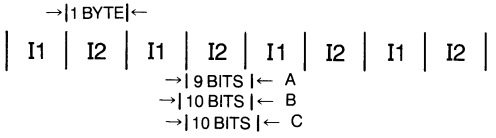
The error correction and detection capability of any Reed Solomon code always relates the number of symbols (bytes) that are allowed to be in error to permit valid correction and detection. In the simplest case, data is run through hardware one byte at a time and, depending on the complexity of the

hardware and the number of redundancy bytes (bytes appended to the data field) used, one can allow a certain number of these bytes to be in error and still recover the data via correction and or detection.

To minimize hardware and maximize the error detection and correction capability of the Reed Solomon code, several identical hardware constructions are employed in parallel; each with their individual limit on the number of symbols (bytes) that can be in error. This method is called interleaving. The interleaving method is set up such that the first byte goes into the first interleave, the second byte into the second interleave, etc. for the entire length of the data plus redundancy fields. The MSD95C02 can employ either two or three interleaves, each interleave containing a maximum of 255 bytes. Further, each interleave can be programmed to handle either 1 or 2 symbols in error. The combination of interleaves and allowable symbols in error per interleave, accounts for a variety of local processor programmable error detection and correction capabilities. A few examples will illustrate.

CASE 1:

Interleave of 2 and the ability to correct 1 byte per interleave



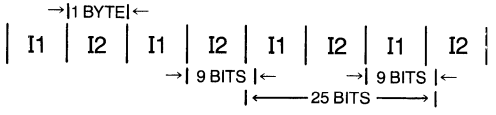
A: Any and all 9 bit bursts will never span more than one symbol per interleave. This arrangement permits correction of any single 9 bit burst error.

B: This 10 bit burst includes two symbols from interleave 1 and hence, cannot guarantee proper correction.

C: This 10 bit burst, because of its position, does not include more than one symbol per interleave and can be corrected properly.

CASE 2:

Interleave of 2 and the ability to correct 2 byte per interleave.



A: Any two randomly placed 9 bit bursts will never include more than two symbols per interleave. This arrangements permits correction of any two, 9 bit burst errors.

B: Any single burst error, 25 bits long or smaller, will never include more than two symbols per interleave. This arrangement permits correction of any single 25 bit burst error.

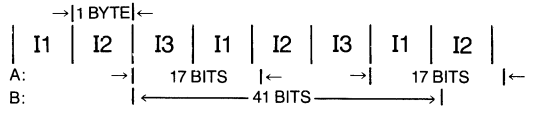
CASE 3:

Interleave of 3 and the ability to correct 1 symbol per interleave.

A: Any and all 17 bit bursts will never include more than one symbol per interleave. This arrangements permits correction of any single 17 bit burst error.

CASE 4:

Interleave of 3 and the ability to correct 2 symbols per interleave.



A: Any two randomly placed 17 bit bursts will never include more than two symbols per interleave. This arrangement permits correction of any two, 17 bit burst errors.

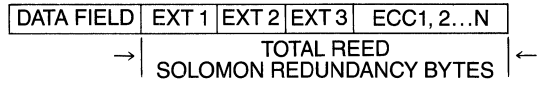
B: Any single burst error, 41 bits long or smaller, will never include more than two symbols per interleave. This arrangement permits correction of any single 41 bit burst error.

The MSD 95C02 has the ability to handle 2 or 3 interleaves and can be programmed to correct either single or double burst errors of varying length. Single or double burst error correction capability corresponds to 1 or 2 symbol errors per interleave.

The MSD 95C02 provides the user with an additional option used to control the range of the error detection capability. This is performed by including either an ECC extension field or a CRC addition field.

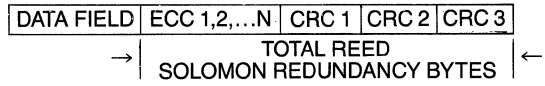
ECC EXTENSION FIELD:

An extension field can be added to the data block being processed to guarantee detection of an extra symbol per interleave. The extension field consists of either 2 (for an interleave of 2) or 3 (for an interleave of 3) additional bytes preceding the original ECC bytes as follows:



CRC ADDITION FIELD:

In place of the ECC EXTENSION FIELD, an additional 2 or 3 byte CRC field may be appended behind the ECC bytes. The inclusion of this field, which generates a unique 16 or 24 bit CRC sequence, ensures maximum data integrity on the data and ECC field. Since the CRC field incorporates all data independent of interleaves, far greater error detection capability is provided. In addition, this field is used to ensure that every correction performed is valid and hence eliminates any miscorrections going undetected. This requirement is suggested when performing "correction on the fly" without loss of a disk revolution. See Appendix 6 for a description of the software procedure used to ensure that an error was corrected properly. The CRC addition field consists of 2 bytes (for an interleave of 2) or 3 bytes (for an interleave of 3) following the ECC bytes as follows:



The number of redundancy bytes appearing at the end of the data field is a function of the number of interleaves, the programmed number of burst errors correctable (either 1 or 2) and the inclusion of the ECC extension or CRC addition fields.

CRC ADDITION:

INTER-LEAVES	TOTAL REDUNDANCY BYTES	CORR TYPE	MAXIMUM DATA BLOCK LENGTH
2	6 (= 4 R/S ECC + 2 CRC)	SEC, MED	504 BYTES
2	9 (= 7 R/S ECC + 2 CRC)	DEC, MED	501 BYTES
3	9 (= 6 R/S ECC + 3 CRC)	SEC, MED	756 BYTES
3	15 (= 12 R/S ECC + 3 CRC)	DEC, MED	750 BYTES

SEC = single error correction
DEC = double error correction
MED = multiple error detection as defined by the CRC extension used

ECC EXTENSION:

INTER-LEAVES	TOTAL REDUNDANCY BYTES	CORR TYPE	MAXIMUM DATA BLOCK LENGTH
2	6 (= 4 R/S ECC + 2 ECC EXT.)	SEC, DED	504 BYTES
2	9 (= 7 R/S ECC + 2 ECC EXT.)	DEC, TED	501 BYTES
3	9 (= 6 R/S ECC + 3 ECC EXT.)	SEC, DED	756 BYTES
3	15 (= 12 R/S ECC + 3 ECC EXT.)	DEC, TED	750 BYTES

SEC = single error correction
DEC = double error correction
TED = triple error detection

It is also possible to program the redundancy bytes to exclude both an ECC extension and a CRC addition. In this case the total redundancy bytes, etc. take on the following form:

INTER-LEAVES	TOTAL REDUNDANCY BYTES	CORR TYPE	MAXIMUM DATA BLOCK LENGTH
2	4	SEC	506 BYTES
2	7	DEC	503 BYTES
3	6	SEC	759 BYTES
3	12	DEC	753 BYTES

SEC = single error correction
DEC = double error correction

LOCAL PROCESSOR INTERFACE BLOCK

This block has been optimized to interface with Local Processors that have a multiplexed 8 bit Address/Data bus. The internal local processor data bus and address bus are distributed to all blocks within the MSD95C02. Each block has its own address decoder as described in the OVERVIEW OF THE MSD95C02 REGISTERS section.

In addition, this block employs a complex interrupt structure used to generate appropriate interrupt based on multiple internal and external conditions. The interrupts can occur from three sources, namely the MICROSEQUENCER, the DMA block and via the four external sense inputs (SNS4-1) to the MSD95C02. Figure 10 illustrates the interrupt structure of the MSD92C02 with all the corresponding status and interrupt enable registers.

REGISTER DESCRIPTIONS

All reserved bits are read as zero and all unused bits should be written as zero for compatibility with future options.

RESET (READ)—40H

Reading this register address will reset the MSD95C02. This is referred to as a "soft" reset. Soft and hard resets are indistinguishable. Reset will be terminated by a write to any MSD95C02 register.

MODE 1 Register (WRITE)—41H

This register space is not presently implemented.

MODE 1 Register (write)—41H

The bits in this register are cleared to "0" by a hard or soft reset. This Mode Register is used to control the DMA section.

BIT D7: DMA TRANSFER REQUEST COUNTER RESET

Writing a "1" to this bit causes the DMA transfer request counter to be reset. This bit does not have to be cleared between writing successive "1's."

BIT D6: RESERVED

BIT D5-4: EXTERNAL DEVICE DMA ADDRESS INCREMENT VALUE

These bits determine the value that the External Device's DMA address will be incremented for every External Device DMA cycle:

D5	D4	INCREMENT VALUE
0	0	1
0	1	2
1	0	3
1	1	4

BIT D3: CONTROL OUTPUTS MODE SELECT

These bits determine the function of the output pins CTL8-5:

D3 = 0: CTL8 is DGATE
CTL7 is WRITE
CTL6 is ST0
CTL5 is ST1

D3 = 1: CTL8-5 are local processor programmed outputs.

MODE 2 Register (WRITE)—42H

This Mode Register is used to control the Disk Interface and Encoder/Decoder section.

BIT D7: COMPOSITE/INDIVIDUAL SYNDROME

D7 = 0: The ECC uses individual syndrome.
D7 = 1: The ECC uses composite syndrome.

BIT D6: TAPE/DISK MODE

D6 = 0: Select disk mode.
D6 = 1: Select tape mode, perform Read after Write using CRC.

BIT D5: REFERENCE CLOCK SOURCE

This bit is used to select the clock source for the bit rate Read/Write circuitry used when the Read Gate is inactive. (This bit must be a "1" when using Read after Write for tape mode.)

D5 = 0: RCLK (COMBINED READ/REFERENCE CLOCK)
D5 = 1: WRITE REF CLOCK

BIT D4: CONTROL OUTPUTS MODE SELECT

These bits determine the function of the CTL4 pin:

D2 = 0: CTL4 is MICROSEQUENCER output (typically used for ESDI AM enable)
D2 = 1: CTL4 is Local Processor output pin

BIT D3: 16/8 BIT COMPARISON

This bit will choose the 16 or 8 bit compare mechanism in the ENCODER/DECODER block. The 8 bit compare is used when accepting data in NRZ format. The 16 bit compare is used when accepting data in an encoded mode typically to

establish bit synchronization. Refer to the SYNC Register description for a table of how the compares interact with this bit.

D3 = 0: Choose 8 bit compare.
D3 = 1: Choose 16 bit compare.

BITS D2-D0: FORMAT

These bits are used to control the Encoder and Decoder.

D2	D1	D0	TYPE OF ENCODING
0	0	0	FM
0	0	1	MFM
0	1	0	M²FM
0	1	1	MANCHESTER
1	0	0	RLL 2, 7 TYPE 1
1	0	1	RLL 2, 7 TYPE 2
1	1	0	GCR
1	1	1	NRZ

TABLE 4: ENCODER/DECODER SELECTION

Tables 5 and 6 show the correspondence mapping for RLL and GCR encoding respectively.

INPUT BIT STREAM	RLL 2, 7 TYPE 1	RLL 2, 7 TYPE 2
10	0100	0100
010	000100	100100
0010	001100100	00100100
11	1000	1000
011	001000	001000
0011	00001000	00001000
000	100100	000100

TABLE 5: RLL ENCODING MAPPING

INPUT BIT STREAM	GCR ENCODING
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

TABLE 6: GCR ENCODING MAPPING

MODE 3 Register (WRITE)—43H

This Mode Register is used to control the DISK INTERFACE and ENCODER/DECODER blocks.

BIT D7: INVERT DATA

Setting this bit to "1" will cause the disk data to be inverted before encoding and after decoding. If this bit is "0", the data will not be inverted.

BIT D6: LEVEL/PULSE

Setting this bit to "1" will cause the disk data to be decoded as hard disk data (level transitions). If this bit is "0", the data will be decoded as floppy disk (pulse) data.

BITS D5-D2: RESERVED

BITS D1-D0: CONTROL OUTPUTS MODE SELECT

These bits determine the function of the CTL3-1 pins:

D1 = 0: CTL3 is WRFCLK input
D1 = 1: CTL3 is Local Processor output pin
(Note: this bit is set to a "0" upon a hard or soft reset)
D0 = 0: CTL2 is LATE output
CTL1 is EARLY output
D0 = 1: CTL2 and 1 are Local Processor programmable outputs.

MODE 4 Register (WRITE)—44H

This Mode Register is used to control the ECC Interface section.

BIT D7: INTERNAL/EXTERNAL ECC

D7 = 1: Will disable all internal ECC/CRC circuitry.
D7 = 0: Will enable all selected ECC/CRC circuitry.

BIT D6: INTERLEAVE 2/3

D6 = 1: Indicates Interleave 2
D6 = 0: Indicates Interleave 3

BIT D5: SINGLE/DOUBLE ERROR CORRECTION SELECTION

D5 = 1: Correct single error
D5 = 0: Correct double error

BITS D4, D3: REED-SOLOMON CODE OPTIONS

These bits determine the optional ECC configurations and code capabilities.

D4	D3	OPTION
0	0	REED-SOLOMON DISABLED (USE ECC-32 OR CRC-16)
0	1	REED-SOLOMON only
1	0	REED-SOLOMON WITH ECC EXTENSION
1	1	REED-SOLOMON WITH CRC ADDITION (1)

TABLE 7: REED-SOLOMON CODE OPTIONS

(1) This is either a 16 bit CRC (for single error correction) or a 24 bit CRC (for double error correction) different than the standard CRC-16 code which can be used as defined by bit D2.

BIT D2: ALTERNATE ECC/CRC USAGE

D2 = 1: Attaches the IBM® PC/XT™/AT® compatible 32 bit ECC code to the end of the data field.
(X32 + X28 + X26 + X19 + X17 + X10 + X6 + X2 + 1)

D2 = 0: Attaches the standard floppy disk 16 bit CRC code to the end of the data field.
(X16 + X12 + X5 + 1)

BIT D1: CRC/PRESET

D1 = 1: Preset alternate ECC/CRC Register to "1" before computing.
D1 = 0: Preset alternate ECC/CRC Register to "0" before computing.

BIT D0: (RESERVED)

RESERVED REGISTER SPACE—45H

This register space is reserved for future expansion.

SYNC REGISTER 1-4 (WRITE)—ADDR 46H-49H.

The following four SYNC Registers are used to perform either 8 or 16 bit high speed compares on the incoming encoded data from the disk. The compares are executed via three signals in the microcode EXT field. The three signals, SPRE, SMC and SDM are typically used to look for PLO SYNC (preamble) data, missing clock pattern data, and data mark data respectively. The MICROSEQUENCER can check for a valid high speed compare via the signal SYNC in the test field of the microcode word. Tables 8 and 9 illustrate how the compares are used in conjunction with the four SYNC Registers as a function of the encoding scheme used and bit D3 (8/16 bit compare) of MODE 2 Register.

SYNC 1 Register (WRITE)—46H This register holds SYNC pattern 1.

SYNC 2 Register (WRITE)—47H This register holds SYNC pattern 2.

SYNC 3 Register (WRITE)—48H This register holds SYNC pattern 3.

SYNC 4 Register (WRITE)—49H This register holds SYNC pattern 4.

ENCODING SCHEME	SYNC 1 (47H)	SYNC 2 (48H)	SYNC 3 (48H)	SYNC 4 (49H)
FM	ADDRESS MARK DATA	DATA MARK DATA	PLO SYNC DATA	DATA MARK CLOCK
MFM	MISSING CLOCK DATA	PLO SYNC DATA	PLO SYNC CLOCK	MISSING CLOCK CLOCK
RLL (1)	MISSING CLOCK PATTERN 1	PLO SYNC DATA	PLO SYNC CLOCK	MISSING CLOCK PATTERN 2
RLL (2)	MISSING CLOCK DATA	PLO SYNC DATA	—	—
NRZ & GCR (3)	PATTERN 1	PATTERN 2		

TABLE 8: SYNC REGISTER DEFINITION AS A FUNCTION OF ENCODING SCHEME

(1) RLL SYNC Register setup for 16 bit compare (bit D3 of MODE 2 Register = 1)
(2) RLL SYNC Register setup for 8 bit compare (bit D3 of MODE 2 Register = 0)
(3) NRZ and GCR encoding should always use 8 bit compares (bit D3 of MODE 2 Register = 0)

MICROCODE SIGNAL	8/16 COMPARE	COMPARE BETWEEN DISK DATA AND SYNC REGISTER
SPRE	8	SYNC 2 (47H)
SPRE	16	SYNC 2 (47H) FOR DATA TRACK AND SYNC 3 (48H) FOR CLOCK TRACK
SMC	8	SYNC 1 (46H)
SMC	16	SYNC 1 (46H) FOR DATA TRACK AND SYNC 4 (49H) FOR CLOCK TRACK
SDM	8	SYNC 2 (47H)
SDM	16	SYNC 2 (47H) FOR DATA TRACK AND SYNC 4 (49H) FOR CLOCK TRACK

TABLE 9: SYNC REGISTER COMPARE MATRIX AS A FUNCTION OF MICROCODE SIGNALS

The following two registers represent a 12 bit TAPE BYTE counter. This counter is needed during tape Read/Write operating to inform the readback circuitry that the data block plus the two byte CRC field has been read. Only the CRC-16 can be used with the tape feature. It is loaded with the value equal to the number of bytes in the data block plus 2 (for the CRC-16 field).

TAPE BYTE COUNTER HIGH (WRITE)—4AH

This register holds the upper four bits of the twelve bit Tape Byte Counter. This counter is used to count the number of bytes used for CRC 2 during the Read after Write.

TAPE BYTE COUNTER LOW (WRITE)—4BH

This register holds the lower eight bits of the twelve bit Tape Byte Counter. This counter is used to count the number of bytes used for CRC 2 during the Read after Write.

LOCAL PROCESSOR OUTPUT Register (WRITE)—4CH

This register holds the data that is directly output on the CTL8-1 pins when they are configured as Local Processor outputs by bits in MODE 1, MODE 2 and MODE 3 Registers. Bit 7 is output on CTL8 and bit 0 is output on CTL1. These bits are cleared to zero by a hard or soft reset.

INTERRUPT ENABLE 1 Register (READ/WRITE)—4DH

The bits in this register are cleared to zero by a hard or soft reset.

BIT D7: MASTER INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to drive its $\overline{INT}$ output pin active when an enabled condition causes the Interrupt Pending status bit to go active high.

BIT D6: DMA INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending status bit when the DMA bit in the INTERRUPT STATUS Register goes active high.

BIT D5: (RESERVED)

BIT D4: DONE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending status bit when the DONE bit in the INTERRUPT STATUS Register goes active high.

BIT D3: (RESERVED)

BIT D2-D0: (reserved for future expansion)

INTERRUPT ENABLE 2 Register (READ/WRITE)—4EH

The bits in this register are cleared to zero by a hard or soft reset.

BIT D7: PROGRAM 2 INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Program status bits in the INTERRUPT STATUS Register when the PROG 2 bit in the STATUS 2 Register goes active high.

BIT D6: PROGRAM 1 INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Program status bits in the INTERRUPT STATUS Register when the PROG 1 bit in the STATUS 2 Register goes active high.

BIT D5: PROGRAM 0 INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Program status bits in the INTERRUPT STATUS Register when the PROG 0 bit in the STATUS 2 Register goes active high.

BITS D4-D0: (RESERVED)

INTERRUPT ENABLE 3 Register (READ/WRITE)—4FH

The bits in this register are cleared to zero by a hard or soft reset.

BITS D7-D6: MUST BE SET TO ZERO (RESERVED)

BIT D5: WRITE FAULT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Write Fault bit in the STATUS 4 Register and cause the test point "NTP2" to go active when the Sense 2 Change bit in the STATUS 4 Register goes active high. In tape mode, setting this bit will also cause test point "NTP2" to go active if Read After Write Enable is active and a CRC error occurs during a Read after Write.

BIT D4: READ AFTER WRITE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and STATUS 4 Interrupt bits in the INTERRUPT STATUS Register when the Read After Write Fault bit in the STATUS 4 Register goes active high.

BIT D3: SENSE 4 CHANGE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Sense Change bits in the INTERRUPT STATUS Register when the Sense 4 Change bit in the STATUS 4 Register goes active high.

BIT D2: SENSE 3 CHANGE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Sense Change bits in the INTERRUPT STATUS Register when the SENSE 3 Change bit in the STATUS 4 Register goes active high.

BIT D1: SENSE 2 CHANGE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Sense Change bits in the INTERRUPT STATUS Register when the SENSE 2 Change bit in the STATUS 4 Register goes active high.

BIT D0: SENSE 1 CHANGE INTERRUPT ENABLE
Setting this bit to "1" will cause the MSD95C02 to set the Interrupt Pending and Sense Change bits in the INTERRUPT STATUS Register when the SENSE 1 Change bit in the STATUS 4 Register goes active high.

DMA FUNCTION Register (READ)—50H

BITS D7-D6. These bits specify the operation to be performed on the internal register file by the Local Processor:

D7	D6	FUNCTION
0	0	SOURCE + OFFSET COUNTER → DESTINATION (Note 1)
0	1	SOURCE + N → DESTINATION; DECREMENT OFFSET COUNTER
1	0	SOURCE → DESTINATION
1	1	SOURCE + N → DESTINATION

N = 1 for disk and local processor data transfers
N specified for MODE 1 Register for External channel (SCSI) data transfers

TABLE 10: DMA FUNCTION REGISTER OPERATION

Notes:

1. For this case, the only destinations that can be updated are the OFFSET COUNTER and the MAILBOX. All other destinations will cause the OVERFLOW flag to be updated as a function of the result out of the ALU, but will not update the destination.

2. When the controller changes the contents of the OFFSET and AUXILIARY OFFSET COUNTERS, it must set or clear the zero bit via the START COMMAND Register bits 4 and 3.

3. The OFFSET COUNTER cannot be used as a source. If it is used as a source, it will take on the value of zero. During error correction, it becomes necessary to use the OFFSET COUNTER as a source. See appendix 3 for a description of ERROR CORRECTION ON THE FLY for more detail.

BITS D5-D3. Source register file address.
BITS D2-D0. Destination register file address.

These bits select the register file address location(s) accessed by the operation specified by bits D7 and D6.

D5 D2	D4 D1	D3 D0	REGISTER SELECTED
0	0	0	MAILBOX HIGH, LOW
0	0	1	OFFSET COUNTER
0	1	0	CONSTANT 1
0	1	1	CONSTANT 2
1	0	0	LOCAL PROCESSOR ADDRESS
1	0	1	EXTERNAL DEVICE ADDRESS
1	1	0	DISK REGISTER
1	1	1	DISK ADDRESS

TABLE 11: DMA FUNCTION REGISTER SOURCE/ DESTINATION

MAILBOX HIGH Register (READ/WRITE)—51H

BITS D7-D0: HIGH ORDER DMA ADDRESS BITS; A15-8

This register functions as a mailbox for transfer of the high order address bits to and from the DMA register file.

MAILBOX LOW Register (READ/WRITE)—52H

BITS D7-D0: LOW ORDER DMA ADDRESS BITS; A7-0

This register functions as a mailbox for transfer of the low order address bits to and from the DMA register file.

DATA Register (READ/WRITE)—53H

This register functions as a mailbox for data transfers between the Local Processor and the Ring Buffer. Local Processor read and writes to the Ring Buffer are funnelled through this register which resides in the DMA block. The Local Processor should poll STATUS 1 Register, bit 1 (REQUEST 1), to determine the status of local processor initiated DMA cycles.

START COMMAND Register (WRITE)—54H

Writing to this register initiates microprogram execution.

BIT D7: START ENABLE

Setting this bit to a logic "1" will set the BUSY bit in STATUS 3 Register and enable the start of microprogram execution.

BIT D6: DISK DMA DIRECTION
This bit selects the direction of DMA data transfer for the disk data channel:

D6 = 1 Disk to Ring Buffer (Disk READ)
D6 = 0 Ring Buffer to Disk (Disk WRITE)

BIT D5: EXTERNAL DEVICE DMA DIRECTION
This bit selects the direction of DMA data transfer for the EXTERNAL data channel:

D5 = 1 External Device to Ring Buffer.
D5 = 0 Ring Buffer to External Device.

BIT D4, D3: DMA ZERO BIT CONTROL
These bits can set or reset the zero output of the DMA OFFSET and AUXILIARY OFFSET COUNTERs:

D3	D4	RESULT
0	0	No change to zero indicator
0	1	Reset zero indicator
1	0	Set zero indicator
1	1	Undefined

TABLE 12: DMA ZERO BIT CONTROL

BIT D2: CRR (Current Register Read)
Writing a logic "1" to this register indicates that the microprocessor has finished reading the information in the CURRENT REGISTER FILE. This must be done after an interrupt has been caused by PROG0 or PROG1 to allow MICROSEQUENCER access to the CURRENT REGISTER FILE. Writing a logic zero will have no effect.

BIT D1: (RESERVED)

BIT D0: HALT
Writing a logic "1" to this register will cause "NTP2" to go active. The MICROSEQUENCER can test "NTP2" at certain times to determine if it should terminate execution of the present command. This bit is a way for the local processor to halt the microprogram at an appropriate time (for example; at the end of a sector read) by having the microprogram interrogate NTP2 at that time.

INTERRUPT STATUS Register (READ)—54H

This register is the master interrupt status register. It should be read after an interrupt is generated to determine which logical block generated the interrupt condition.

BIT D7: INTERRUPT PENDING
This bit is set to "1" when one of the enabled interrupt conditions occur. It is cleared to "0" when the interrupt causing condition(s) are cleared.

BIT D6: DMA INTERRUPT
This bit is set to "1" when the ZERO or AUXILIARY ZERO bits in the STATUS 1 (DMA) Register go active high. It is cleared to "0" by reading the STATUS 1 (DMA) Register, a hard or a soft reset.

BIT D5: PROGRAM INTERRUPT
This bit is set to "1" when one of the enabled PROG2-0 bits in the STATUS 2 Register goes active high. It is cleared to "0" by reading the STATUS 2 Register, a hard or a soft reset.

BIT D4: DONE INTERRUPT
This bit is set to "1" when the MSD95C02 completes a command. This interrupt is generated by the microcode and indicates that the internal MICROSEQUENCER has stopped. This bit is reset to "0" by reading STATUS 3 Register, or by a hard or soft reset.

BIT D3: SENSE CHANGE INTERRUPT
This bit is set to "1" when one of the enabled Sense 4-1 Change bits in the STATUS 4 Register goes active high. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D2: STATUS 4 Register INTERRUPT
This bit is set to "1" when the Read After Write interrupt in STATUS 4 Register goes active high. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BITS D1-D0: (RESERVED)

STATUS 1 Register (READ)—55H

This register contains status about the DMA block. Bits D3-D0 are cleared to zero following a hard or soft reset. Bits D7-D4 are unaffected by a hard or soft reset.

BIT D7: AUXILIARY ZERO
This bit reflects the state of the zero flag of the AUXILIARY OFFSET COUNTER. This bit is set by a hard or soft reset.

BIT D6: ZERO
This bit reflects the state of the zero flag of the

OFFSET COUNTER. This bit is set by a hard or soft reset.

BIT D5: OVERFLOW
This bit reflects the state of the overflow flag generated from the ALU in the DMA block.

BIT D4: (RESERVED)

BIT D3: REQUEST 3
This bit reflects the state of the MICROSEQUENCER housekeeping DMA cycle request latch. A logic "1" indicates that the DMA cycle request has either not been acknowledged or is in progress and a logic "0" indicates that the DMA cycle has been completed.

BIT D2: REQUEST 2
This bit reflects the state of the MICROSEQUENCER data transfer DMA cycle request latch. A logic "1" indicates that the DMA cycle request has either not been acknowledged or is in progress and a logic "0" indicates that the DMA cycle has been completed.

BIT D1: REQUEST 1
This bit reflects the state of the Local Processor channel DMA cycle request latch. A logic "1" indicates that the DMA cycle request has either not been acknowledged or is in progress and a logic "0" indicates that the DMA cycle has been completed.

BIT D0: REQUEST 0
This bit reflects the state of the External Device channel DMA cycle request latch. A logic "1" indicates that the DMA cycle request has either not been acknowledged or is in progress and a logic "0" indicates that the DMA cycle has been completed.

STATUS 2 Register (READ)—56H

This register contains status about the MICROSEQUENCER block. The Program Interrupt bits are set under MICROSEQUENCER control. The PROG2-0 bits are cleared to zero by reading the STATUS 2 Register, a hard or a soft reset.

BITS D7-D5: PROGRAMMABLE INTERRUPTS 2-0.
These bits are set to "1" under MICROSEQUENCER control. These bits are reset to "0" by reading the Status 2 Register, a hard or a soft reset.

BIT D7: PROGRAMMABLE INTERRUPT 2
This is a programmable interrupt that is set under a MICROSEQUENCER control. This is a general purpose interrupt that can be generated upon recognition of any MICROSEQUENCER detectable condition. The generation of this interrupt will affect no additional hardware.

BIT D6: PROGRAMMABLE INTERRUPT 1
This is a programmable interrupt that is set under MICROSEQUENCER control. This interrupt will allow the local processor to access the CURRENT REGISTER FILE. The MICROSEQUENCER will not be able to update the register file until the local processor has indicated that it has finished reading the register file by writing a "1" to bit D2 (CRR) of the START COMMAND Register. This interrupt may be used for ID field interrupt to permit the local processor to read the current ID information that is stored

BIT D5: PROGRAMMABLE INTERRUPT 0
This is a programmable interrupt that is set under MICROSEQUENCER control. This interrupt will allow the local processor to access the CURRENT REGISTER FILE. The MICROSEQUENCER will not be able to update the CURRENT REGISTER FILE until the local processor has indicated that it has finished reading the CURRENT REGISTER FILE by writing a "1" to bit D2 (CRR) of the START COMMAND Register. The generation of this interrupt will delink the OFFSET and AUXILIARY OFFSET COUNTERS in the DMA block. This interrupt is used to indicate an ECC error. Service would be required by having the Local Processor read the error syndrome residing in the CURRENT REGISTER FILE, correct the error and properly relink the AUXILIARY OFFSET and OFFSET COUNTERs in the DMA block back together. See Appendix 4 (ECC ON THE FLY) for further details.

BITS D4-D0: (RESERVED)

STATUS 3 Register (READ)—57H

This register contains status about the MICROSEQUENCER block. The values in bits D4-0 are valid when the Done Interrupt bit is active high.

BIT D7: BUSY
This bit indicates the state of the MICROSEQUENCER.
0 = MICROSEQUENCER is finished or reset.
1 = MICROSEQUENCER is executing a program.

BITS D6-D5: (RESERVED)

BITS D4-D0: PROGRAM COUNTER DATA
These bits will hold the address of the instruction executed prior to executing the instruction that generated the Done Interrupt via the signal DNINT in the OUT field of the MICROSEQUENCER RAM. They are valid after the Done status bit is set indicating that the MICROSEQUENCER has stopped running.

STATUS 4 Register (READ)—58H

This register contains status information.

BIT D7: RESERVED

BIT D6: ABNORMAL DATA MARK
This bit is set to "1" when the MICROSEQUENCER tests the data mark and it does not match the data mark in the DESIRED REGISTER. This bit being set will cause "NTP2" to become active. This bit is reset by the start of execution of a command.

BIT D5: WRITE FAULT
This bit is set to "1" when the SNS2 input undergoes a high-to-low level transition if the WRITE FAULT enable bit of the INTERRUPT ENABLE 3 Register is an active "1". This bit being set will cause "NTP2" to become active. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D4: READ AFTER WRITE ERROR
This bit is set to "1" when a CRC error occurs during a Read After Write while in the tape mode. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D3: SENSE 4 CHANGE
This bit is set to "1" when the SNS4 input undergoes a high-to-low or low-to-high level transition. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D2: SENSE 3 CHANGE
This bit is set to "1" when the SNS3 input undergoes a high-to-low level transition. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D1: SENSE 2 CHANGE
This bit is set to "1" when the SNS2 input undergoes a high-to-low level transition. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset.

BIT D0: SENSE 1 CHANGE
This bit is set to "1" when the SNS1 input undergoes a high-to-low level transition. This bit is reset to "0" by reading the STATUS 4 Register, a hard or a soft reset. When the Local Processor reads this register, this bit must not be reset before it is read.

REGISTERS (READ)—59H, 5AH, 5BH

These registers are reserved for future expansion.

DEVICE INPUTS Register (READ)—5CH

This register reflects the status of the external TEST and SENSE inputs. The MSD95C02 can be programmed to generate an interrupt from some of these input pins as follows:

BIT D7: TEST 4
This bit reflects the state of the TST4 input.

BIT D6: TEST 3
This bit reflects the state of the TST3 input.

BIT D5: TEST 2
This bit reflects the state of the TST2 input.

BIT D4: TEST 1
This bit reflects the state of the TST1 input.

BIT D3: SENSE 4
This bit reflects the state of the SNS4 input. The MSD95C02 can be programmed to generate an interrupt whenever this input transitions (level change interrupt).

BIT D2: SENSE 3
This bit reflects the state of the SNS3 input. The MSD95C02 can be programmed to generate an interrupt whenever this input transitions from high to low (negative edge triggered interrupt).

BIT D1: SENSE 2
This bit reflects the state of the SNS2 input. The MSD95C02 can be programmed to generate an interrupt whenever this input transitions from high to low (negative edge triggered interrupt).

BIT D0: SENSE 1
This bit reflects the state of the SNS1 input. The MSD95C02 can be programmed to generate an interrupt whenever this input transitions from high to low (negative edge triggered interrupt).

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} +0.3V
Negative Voltage on any Pin, with respect to Ground ..... −0.3V
Maximum Voltage on V_{CC} pin 7.0V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS TA = 0°C to 70°C, V_{CC} = 5.0V, ±5%)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
SUPPLY CURRENT					
I_{CC}				mA	V_{CC} = 5.25V
$I_{STANDBY}$				mA	V_{CC} = 5.25V
OUTPUT VOLTAGE					
High, V_{OH}	2.4			V	I_{OH} = −40µA
Low, V_{OL}			0.4	V	I_{OL} = 1.6mA
INPUT VOLTAGE					
High, V_{IH1}	2.0			V	Except DMACLK, RCLK, CTL3
High, V_{IH2}	3.5			V	DMACLK, RCLK, CTL3
Low, V_{IH1}			0.8	V	Except DMACLK, RCLK, CTL3
Low, V_{IH2}			1.5	V	DMACLK, RCLK, CTL3
INPUT LEAKAGE					
High, I_{IH}			10	µA	V_{IH} = 2.0V, Except DMACLK, RCLK, CTL3
Low, I_{IL}			10	µA	V_{IH} = 3.5V, DMACLK, RCLK, CTL3
					V_{IL} = 0.8V, Except DMACLK, RCLK, CTL3
					V_{IL} = 1.5V, DMACLK, RCLK, CTL3

AC ELECTRICAL CHARACTERISTICS

All minimum and maximum times are given assuming a 20MHz clock. If the time is clock dependent, then the equation is given under the comments column. This is to allow calculation of the time delays using slower clock rates.

AC ELECTRICAL SPECIFICATIONS TA = 0°C to 70°C, V_{CC} = 5.0V, ±5%)

DATA SYMBOL	PATH MIN	TIMING MAX	UNITS	COMMENTS
T_1		100	ns	ADDR TO DATA VALID (3xDMACLK) − 50 nsec
T_2	0		ns	READ DATA HOLD FROM ADDR CHNG
T_3	140		ns	$\overline{OE}$ PULSE WIDTH (3xDMACLK) − 10 nsec
T_4		75	ns	$\overline{OE}$ TO READ DATA VALID (3xDMACLK) − 75 nsec
T_5		35	ns	$\overline{OE}$ TO DATA HIGH IMPEDANCE (DMACLK) − 15 nsec
T_8	100		ns	$\overline{OE}$ TO TRAILING EDGE OF $\overline{DACK}$ (2.5xDMACLK) − 25 nsec
T_9	15		ns	TRAILING EDGE OF $\overline{DACK}$ TO TRAILING EDGE OF $\overline{OE}$ (0.5xDMACLK) − 10 nsec
T_{10}	0		ns	ADDR SETUP TIME TO $\overline{WE}$
T_{11}	25		ns	WRITE RECOVERY TIME (ADDR HOLD AFTER $\overline{WE}$ INACTIVE) (DMACLK − 25 nsec)
T_{12}	75		ns	$\overline{WE}$ PULSE WIDTH (2xDMACLK) − 25 nsec
T_{13}	40		ns	WRITE DATA SETUP TIME (DMACLK − 10 nsec)
T_{14}	25		ns	WRITE DATA HOLD TIME (DMACLK − 10 nsec)
T_{15}	85		ns	$\overline{DACK}$ TO TRAILING EDGE OF $\overline{WE}$ (2xDMACLK) − 15 nsec
T_{16}	10		ns	TRAILING EDGE OF $\overline{WE}$ TO TRAILING EDGE OF $\overline{DACK}$ (0.5xDMACLK) − 10 nsec
T_{17}	50		ns	$\overline{DACK}$ PULSE WIDTH HIGH (1.5xDMACLK) − 25 nsec
T_{18}	100		ns	$\overline{DACK}$ PULSE WIDTH LOW (2.5xDMACLK) − 25 nsec
T_{1a}	85		ns	S0, S1 HOLD AFTER $\overline{OE}$ ACTIVE (2xDMACLK) − 15 nsec
T_{1b}	85		ns	S0, S1 HOLD AFTER $\overline{WE}$ ACTIVE (2xDMACLK) − 15 nsec
T_{1c}	85	115	ns	S0, S1 VALID TO ADDRESS VALID (2xDMACLK) − 15 nsec (MIN) (2xDMACLK) + 15 nsec (MAX)
T_{1d}	185		ns	S0, S1 WIDTH (4xDMACLK) − 15 nsec
T_{2a}	135		ns	$\overline{WRITE}$ HOLD AFTER $\overline{OE}$ ACTIVE (3xDMACLK) − 15 nsec
T_{2b}	135		ns	$\overline{WRITE}$ HOLD AFTER $\overline{WE}$ ACTIVE (3xDMACLK) − 15 nsec
T_{2c}	35	65	ns	$\overline{WRITE}$ VALID TO ADDRESS VALID (1xDMACLK) − 15 nsec (MIN) (1xDMACLK) + 15 nsec (MAX)
T_{2d}	185		ns	$\overline{WRITE}$ WIDTH (4xDMACLK) − 15 nsec

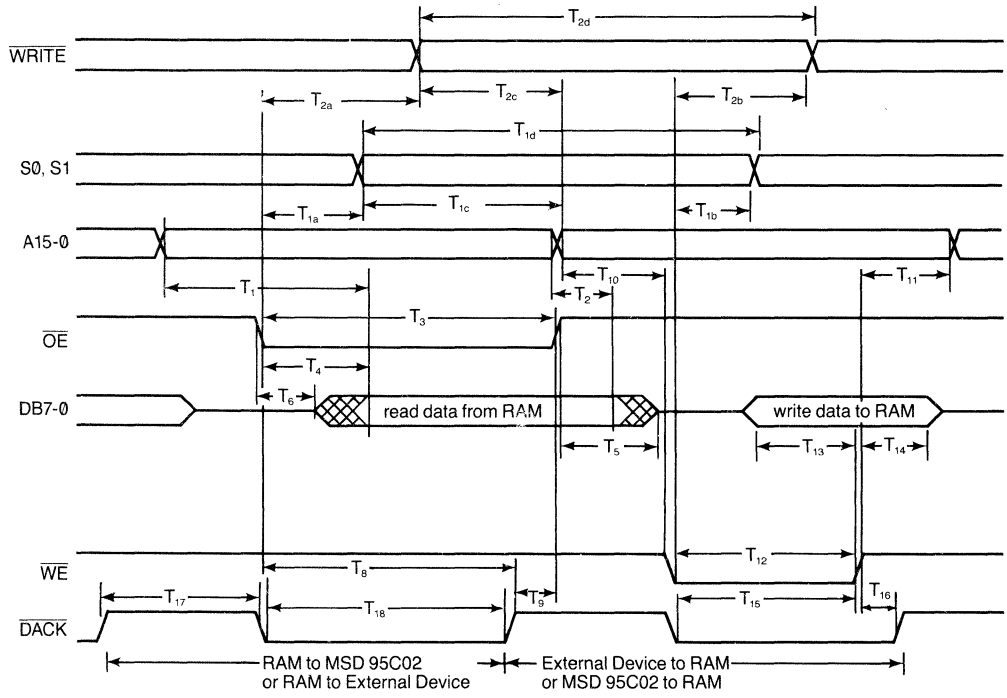


FIGURE 11: DATA PATH TIMING

DMA CLOCK and DMA REQUEST TIMING

SYMBOL	MIN	MAX	UNITS	COMMENTS
T_{20}	50	1000	nsec	DMACLK CYCLE TIME
T_{21}	20		nsec	DMACLK HIGH TIME
T_{22}	20		nsec	DMACLK LOW TIME
T_{23}		5	nsec	DMACLK RISE TIME
T_{24}		5	nsec	DMACLK FALL TIME
T_{25}	1.1xT20		nsec	DMAREQ CYCLE TIME (Note 1)
T_{26}	20		nsec	DMAREQ LOW TIME
T_{27}	20		nsec	DMAREQ HIGH TIME
T_{28}		5	nsec	DMAREQ RISE TIME
T_{29}		5	nsec	DMAREQ FALL TIME

NOTE 1: Can be 1XT21a if DMAREQ is synchronized to DMACLK.

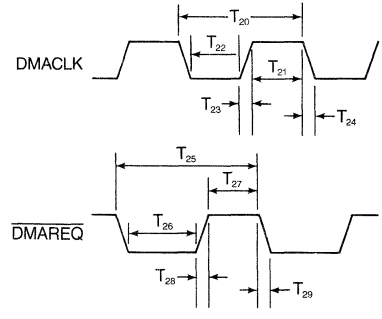


FIGURE 12: DMA CLOCK and DMA REQUEST TIMING

INTERRUPT TIMING

SYMBOL	MIN	MAX	UNITS	COMMENTS
T_{30}		100	nsec	INTERRUPT RESET FROM $\overline{RD}$ or $\overline{WR}$

FIGURE 13: INTERRUPT TIMING

DISK (Write Data) TIMING

SYMBOL	MIN	MAX	UNITS	COMMENTS
T_1	48		nsec	CYCLE TIME
T_2	0.40 T1		nsec	HIGH TIME
T_3	0.40 T1		nsec	LOW TIME
T_4		5	nsec	RISE TIME
T_5		5	nsec	FALL TIME
T_6	(TBD)		nsec	DATA SETUP TIME
T_7	(TBD)		nsec	DATA HOLD TIME
T_8	0.75 T1	1.25 T1	nsec	CYCLE TIME
T_9		10	nsec	WDATA VALID TO EARLY, LATE
T_{9a}		10	nsec	EARLY, LATE VALID TO WDATA VALID
T_{10}	0.5 T1		nsec	Hold from trailing edge of WDATA
T_{11}	2xT1-20		nsec	Active time

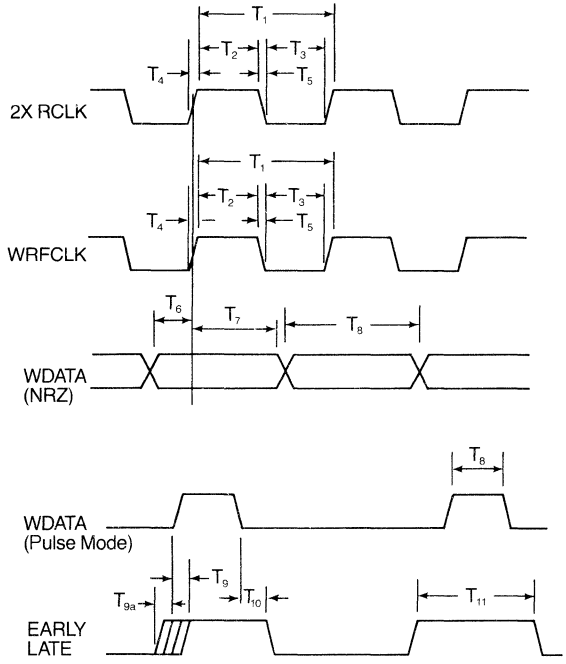


FIGURE 14: DISK (Write Data) TIMING

Microprocessor Interface Timing

SYMBOL	R/$\overline{W}$ $\overline{DS}$	$\overline{RD}$ $\overline{WR}$	UNITS	COMMENTS
T_1	45	45	nsec min	ALE ($\overline{AS}$) ACTIVE PULSE WIDTH
T_2	30	30	nsec min	ADDRESS VALID TO ALE INACTIVE
T_3	15	15	nsec min	ALE INACTIVE TO ADDRESS INVALID
T_4	120	120	nsec min	READ STROBE LOW PULSE WIDTH
T_5	70	115	nsec MAX	$\overline{RD}$ ($\overline{DS}$) ACTIVE TO READ DATA VALID
T_6	10	10	nsec min	READ DATA HOLD FROM $\overline{RD}$ ($\overline{DS}$) HIGH
T_7	110	110	nsec min	WRITE STROBE LOW PULSE WIDTH
T_8	135	135	nsec min	WRITE DATA VALID TO $\overline{WR}$ ($\overline{DS}$) INACTIVE
T_9	25	25	nsec min	WRITE DATA HOLD FROM $\overline{WR}$ ($\overline{DS}$) INACTIVE
T_{10}	20	20	nsec min	ALE ($\overline{AS}$) INACTIVE TO READ STROBE ACTIVE
T_{11}	20	20	nsec min	ALE ($\overline{AS}$) INACTIVE TO WRITE STROBE ACTIVE
T_{12}	0	0	nsec min	$\overline{RD}$ ($\overline{DS}$) INACTIVE TO ALE ACTIVE
T_{13}	0	0	nsec min	$\overline{WR}$ ($\overline{DS}$) INACTIVE TO ALE ACTIVE
T_{14}	0	0	nsec MAX	$\overline{CE}$ VALID TO $\overline{RD}$, $\overline{WR}$ OR $\overline{DS}$
T_{15}	0	0	nsec min	R/$\overline{W}$ VALID TO ALE ($\overline{AS}$) INACTIVE

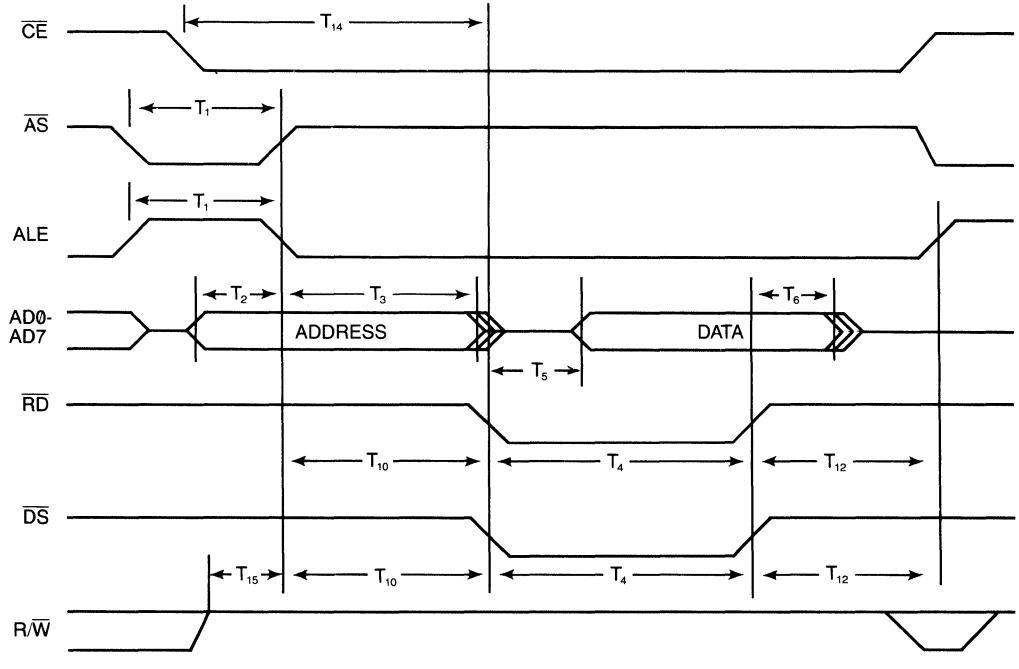


FIGURE 15: MICROPROCESSOR INTERFACE TIMING (READ)

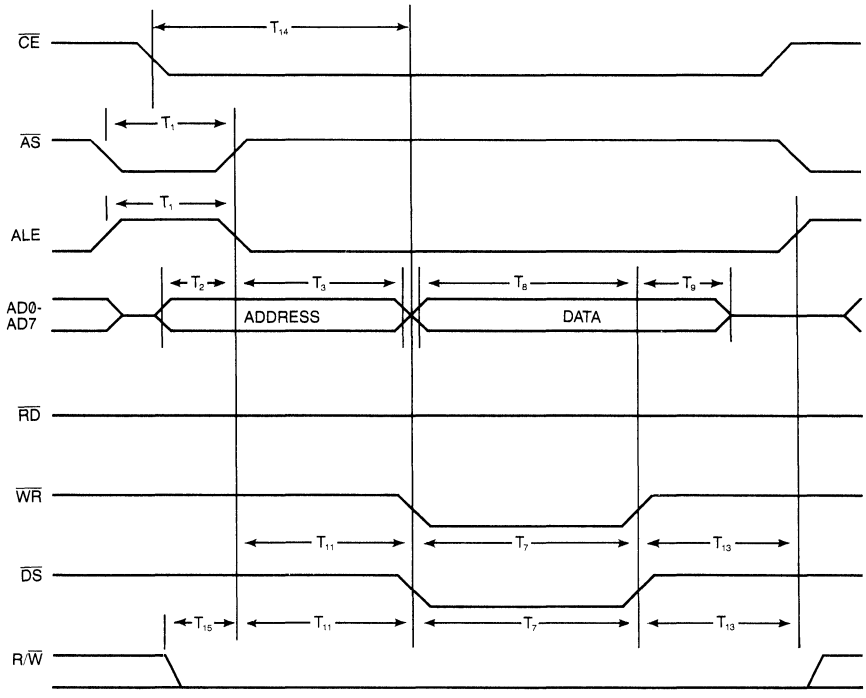


FIGURE 16: MICROPROCESSOR INTERFACE TIMING (WRITE)

DISK INTERFACE TIMING

SYMBOL	MIN	MAX	UNITS	COMMENTS
T_{40}	(TBD)		nsec	Write gate setup to AMENA
T_{40a}	8xWCLK		nsec	Write gate active time
T_{41}	(TBD)		nsec	Write gate hold after AMENA
T_{42}	8xWCLK		nsec	AMENA active time
T_{43}	50		nsec	Index active time
T_{44}	(TBD)		nsec	AMENA TO AMFND
T_{45}	(TBD)		nsec	AMENA inactive to AMFND inactive
T_{46}	50		nsec	AMFND active time
T_{47}	(TBD)		nsec	AMFND active to RGATE active
T_{49}	25		nsec	$\overline{\text{RDATA}}$ active time
T_{50}	12		nsec	$\overline{\text{RDATA}}$ setup to 2xRCLK
T_{51}	12		nsec	$\overline{\text{RDATA}}$ hold from 2xRCLK
T_{52}	25		nsec	SNS1 active time
T_{53}	25		nsec	TST3 active time
T_{54}	25		nsec	SNS2 active time
T_{55}	25		nsec	SNS3 active time
T_{56}	25		nsec	SNS4 active time
T_{57}	25		nsec	TST2 active time
T_{58}	1		µsec	$\overline{\text{RST}}$ active time
T_{59}	0		nsec	$\overline{\text{LPS}}$ active time (Note 1)
T_{60a}	8xWCLK		nsec	RGATE active time

NOTE 1

If the chip is at idle, then the time from $\overline{\text{LPS}}$ becoming active until the chip actually enters the low power mode is the longest of the following times:

1. (2 x (2XRCLK)) + 200nsec
2. (2 x (WRFCLK)) + 200nsec
3. (0.5 x (DMACLK)) + 200nsec

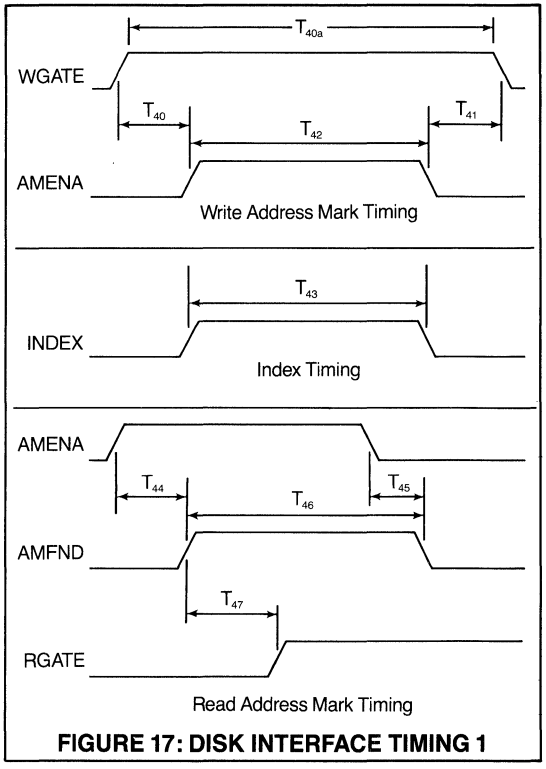


FIGURE 17: DISK INTERFACE TIMING 1

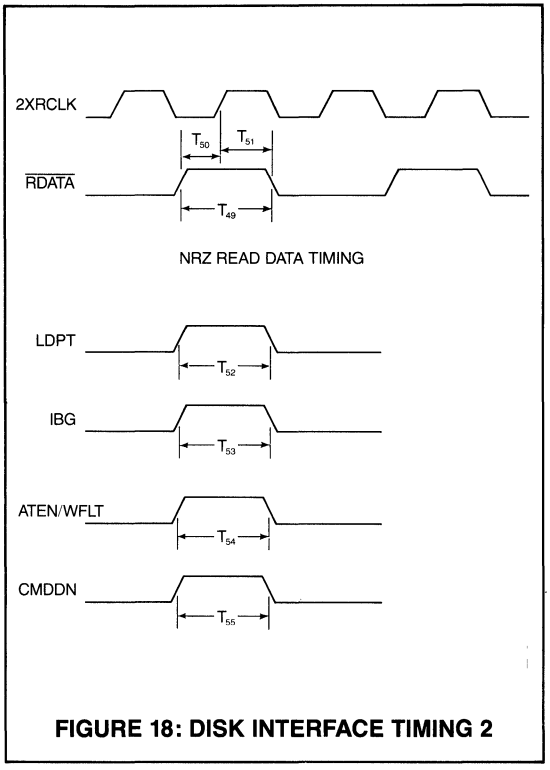


FIGURE 18: DISK INTERFACE TIMING 2

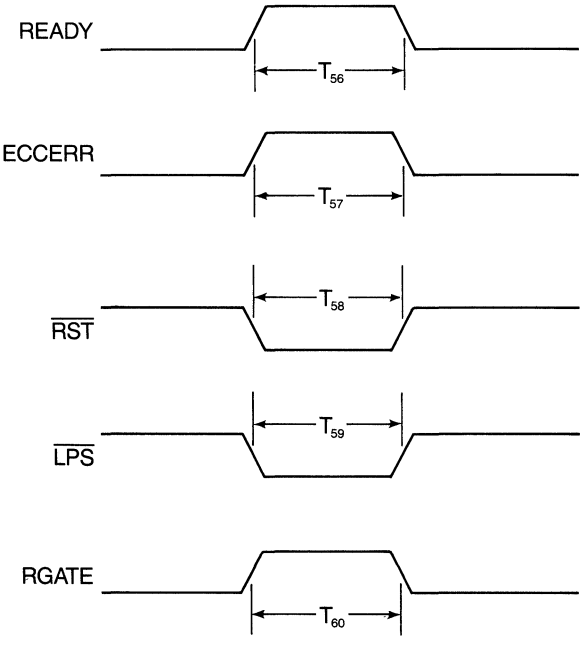
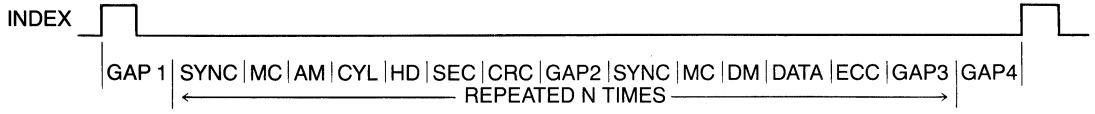


FIGURE 19: DISK INTERFACE TIMING 3

APPENDIX 1—SAMPLE MICROPROGRAMS:

1—FORMAT COMMAND

The following description and microprogram will format a Hard disk with the following format:



All of the following variables can contain any data and be microprogrammed for any length (in bytes).

GAP1—Post index gap.
SYNC—The PLO SYNC (preamble) field.
MC—Missing clock pattern.
AM—Address mark.
CYL—Cylinder number.
HD—Head number.
SEC—Sector number.
CRC—One of several selectable check bytes.
GAP2—Header to data gap.
DM—Data mark.
DATA—The data field.
ECC—One of 2 selectable ECC codes.
GAP3—Post data field gap.
GAP4—Pre index gap.
N—The number of sectors per track.

Prior to executing the format command with the defined microprogram written in the Microprogram RAM, the local processor should load the DESIRED REGISTER FILE with the data to be used in each of the defined fields in the format. The microprogram will point to these preloaded values, via the register pointer field, to permit the data to be transferred to the ENCODER/DECODER block and finally out to the disk. The Local Processor should also load the Ring Buffer with the TRACK, HEAD and SECTOR of all the sectors to be formatted in consecutive locations as follows:

RING BUFFER LOCATION	DATA
0000	TRACK #
0001	HEAD #
0002	SECTOR # FOR FIRST SECTOR AFTER INDEX
0003	TRACK #
0004	HEAD #
0005	SECTOR # FOR SECOND SECTOR AFTER INDEX
o	o
	o
	o
o	TRACK #
	HEAD #
	SECTOR # FOR LAST
o	SECTOR ON THE TRACK

This format table can start at any Ring Buffer memory address.

The Local Processor should also set the DISK ADDRESS Register in the DMA block to the first address in this ID format sequence. In this case it would be address 0000. The track number, head number and sector number may be merged into two bytes as a function of the disk format used.

For the microprogram shown below, the DESIRED REGISTER FILE is loaded as follows:

LABEL	DESIRED REGISTER ADDRESS	CONTENTS	COMMENTS
M(GAP 1)	0C HEX	4E HEX	DATA IN GAP 1
M(SYNC)	0A HEX	00 HEX	DATA IN SYNC FIELD
M(MC)	0B HEX	A1 HEX	MISSING CLOCK PATTERN
M(GAP 2)	0C HEX	4E HEX	DATA IN GAP 2
M(AM)	0E HEX	FE HEX	ADDRESS MARK DATA
SLEW	0F HEX	E0 HEX	2'S COMP. OF # OF SECTORS (16) TO BE WRITTEN
M(DM)	09 HEX	FB HEX	DATA MARK DATA
M(FDAT)	08 HEX	E5 HEX	FORMAT DATA
M(GAP 3)	0C HEX	4E HEX	DATA IN GAP 3
M(GAP 4)	0C HEX	4E HEX	DATA IN GAP 4

In addition, the following variables, which control the length of each field in the format command, are assigned the specified values for this microprogram:

VARIABLE	ASSIGNED VALUE	COMMENTS
GAP 1	10 HEX	LENGTH OF GAP 1
GAP 2	03 HEX	LENGTH OF GAP 2
GAP 3	12 HEX	LENGTH OF GAP 3
PLO	0D HEX	LENGTH OF PLO SYNC FIELD
DTFLD	04 HEX	LENGTH OF DATA FIELD (128 X 4 = 512)
CRC	02 HEX	LENGTH OF CRC FIELD (USES CRC-16)
ECC	04 HEX	LENGTH OF ECC FIELD (USES ECC-32)

This example assumes that the INDEX pulse from the drive is input on TST1.

The microcode is loaded by the local processor in byte address space 80H to FFH according to table 13.

LOCAL PROCESSOR ADDRESS (A7-A0)	DATA (D7-D0)
1XXXXX00	OUT 3-0, EXT 3-0
1XXXXX01	REGISTER DECREMENT (PEN), COUNT 6-0
1XXXXX10	TEST 3-0, REGISTER POINTER 3-0 (POINT)
1XXXXX11	SEQ 2-0, ADDR 4-0.

TABLE 13: LOCAL PROCESSOR TO MICROCODE ADDRESS MAPPING

MICROPROGRAM:

INST #	LABEL	SEQ	ADDR	TEST	POINT	PEN	COUNT	OUT	EXT
00	START	TSJ	START	ONE	0	0	4-1	0	SGOFF
01	WAIT	TSJ	WAIT	TST1	0	0	GAP1-1	0	0
02	BEGIN	SHLP	0	ZERO	M(GAP1)	0	PLO-1	FREG	WGON
03		SHLP	0	ZERO	M(SYNC)	0	1-1	WPRE	CRC16
04		SHLP	0	ZERO	M(MC)	0	1-1	WMISS	0
05		SHLP	0	ZERO	M(AM)	0	3-1	FREG	SWDG
06		SHLP	0	ZERO	0	0	CRC-2	0	0
07		SHLP	0	ZERO	SLEW	0	1-1	WCRC	INCE
08		SHLP	0	ZERO	0	0	GAP2-1	WCRC	0
09		SHLP	0	ZERO	M(GAP2)	0	PLO-1	FREG	ECC32
0A		SHLP	0	ZERO	M(SYNC)	0	1-1	WPRE	0
0B		SHLP	0	ZERO	M(MC)	0	1-1	WMISS	0
0C		SHLP	0	ZERO	M(DM)	0	DTFLD-1	FREG	0
0D		LGLP	0	ZERO	M(FDAT)	0	ECC-1	FREG	0
0E		SHLP	0	ZERO	0	0	1-1	WCRC	0
0F		CI	OUT	XEND	SLEW	0	1-1	FREG	0
10		TSJ	BEGIN	ZERO	M(SYNC)	0	GAP3-1	FREG	0
11	OUT	TSJ	OUT	TST1	M(GAP4)	0	1-1	FREG	0
12		SHLP	0	ZERO	M(GAP4)	0	1-1	FREG	SGOFF
13	LAST	CI	LAST	ONE	0	0	1-1	DNINT	SGOFF

COMMENTS:

D31-D0 is the actual assembled microcode loaded into the microprogram RAM.

INST #	D31-D0	COMMENTS
00	0C 03 F0 80	ENSURE THAT READ AND WRITE GATE ARE OFF.
01	00 0F 70 81	WAIT FOR INDEX AND THEN GO TO NEXT INSTRUCTION.
02	6F 0C 0C 00	RAISE WRITE GATE; WRITE GAP 1 DATA FOR GAP 1 TIME.
03	4A 00 0A 00	WRITE PLO SYNC (PREAMBLE) DATA FOR PLO TIME.
04	50 00 0B 00	WRITE MISSING CLOCK PATTERN USING MISSING CLOCK DATA FOR 1 BYTE TIME.
05	61 02 0E 00	WRITE ADDRESS MARK DATA FOR 1 BYTE TIME. PREPARE TRANSFER OF DATA FROM RING BUFFER TO DISK AT NEXT INSTRUCTION VIA SWDG.
06	00 00 00 00	TRANSFER TWO CONSECUTIVE BYTES FROM RING BUFFER AS SPECIFIED BY THE DISK ADDRESS REGISTER TO THE DISK; THESE TWO BYTES CONTAIN THE HEAD #, TRACK # AND SECTOR #.
07	9E 00 0F 00	WRITE THE FIRST BYTE OF THE CRC; INCREMENT CONTENTS OF THE DESIRED REGISTER LOCATION LABELED SLEW TO LATER CHECK FOR THE END OF THE FORMAT COMMAND.
08	90 02 00 00	WRITE SECOND BYTE OF THE CRC.
09	6B 0C 00 00	WRITE GAP 2 DATA FOR GAP 2 TIME; PRESET ECC GENERATOR.
0A	40 00 0A 00	WRITE PLO SYNC (PREAMBLE) DATA FOR PLO SYNC TIME.
0B	50 00 0B 00	WRITE MISSING CLOCK PATTERN USING MISSING CLOCK DATA FOR 1 BYTE TIME.
0C	60 03 09 00	WRITE DATA MARK DATA FOR 1 BYTE TIME.
0D	60 03 08 20	WRITE FORMAT DATA IN DATA FIELD FOR 512 BYTE TIMES.
0E	90 00 00 00	WRITE A FOUR BYTE ECC.
0F	60 00 AF 71	CHECK FOR END OF COMMAND VIA XEND; IF END, GO TO OUT; ELSE GO TO NEXT INSTRUCTION.
10	60 11 0A 82	WRITE 1 BYTE OF SYNC DATA AFTER ECC; GO TO BEGIN.
11	60 00 4C 91	WRITE A 4E UNTIL INDEX.
12	6C 00 0C 00	WRITE ONE MORE BYTE OF 4E; RESET WRITE GATE AS INSTRUCTION IS EXITED.
13	FC 00 F0 73	SET THE DONE INTERRUPT TO THE LOCAL PROCESSOR; THE MICROSEQUENCER WILL STOP HERE.

2—READ AND WRITE COMMANDS FOR ST-506 FORMATTED DISKS

Prior to executing a READ or WRITE command, using the defined microprogram written in the Microprogram RAM, the Local Processor should load the DESIRED REGISTER FILE with the parameters used during the execution of the microprogram. The microprogram will point to these preloaded values, via the register pointer field, to permit the data to be transferred to the ENCODER/DECODER block and finally out to the disk. The Local Processor should also set up the appropriate DMA address and function registers and specify disk direction, External Device direction, and initialize the zero status bit in the START COMMAND Register prior to execution of microprogram.

For the microprogram shown, the DESIRED REGISTER FILE is loaded as follows:

LABEL	DESIRED REGISTER ADDRESS	CONTENTS	COMMENTS
XFER	00 HEX	BE HEX	USED AS DISK DMA FUNCTION REGISTER DATA TO MOVE DISK ADDRESS REGISTER TO DISK ADDRESS IN DMA BLOCK.
ADDC1	01 HEX	11 HEX	USED AS DISK DMA FUNCTION REGISTER DATA TO ADD CONSTANT 1 TO OFFSET COUNTER IN THE DMA BLOCK.
ADDC2	02 HEX	1B HEX	USED AS DISK DMA FUNCTION REGISTER DATA TO CHECK FOR OVERFLOW OF THE SUM OFFSET COUNTER PLUS CONSTANT 2 IN THE DMA BLOCK.
M(DM)	03 HEX	FB HEX	DATA MARK DATA.
M(AM)	04 HEX	FE HEX	ADDRESS MARK DATA.
M(SYNC)	05 HEX	00 HEX	DATA IN SYNC FIELD.
M(MC)	06 HEX	A1 HEX	MISSING CLOCK PATTERN.
SIZE	07 HEX	—	NOT IMPLEMENTED BUT CAN INDICATE THE SIZE OF THE SECTOR (0, 1, 2, 3, FOR SECTOR SIZES OF 128, 256, 512 AND 1024 RESPECTIVELY).
RETRY	08 HEX	—	NOT IMPLEMENTED BUT CAN BE USED AS A RETRY COUNT WHEN ENCOUNTERING SOFT ERRORS DURING A READ COMMAND. LOADED WITH THE 2'S COMPLEMENT.
SLEW	09 HEX	—	VARIABLE LOADED BY THE LOCAL PROCESSOR INDICATING THE NUMBER OF SECTORS TO BE READ OR WRITTEN DURING THE COMMAND EXECUTION. LOADED WITH THE 2'S COMPLEMENT.
SSECT	0A HEX	—	INITIALIZED WITH THE STARTING SECTOR NUMBER IN THE TRANSFER.
HEAD	0B HEX	—	INITIALIZED WITH THE HEAD NUMBER TO BE OPERATED ON.
TRACK	0C HEX	—	INITIALIZED WITH THE TRACK NUMBER TO BE OPERATED ON.

In addition, the following variables, which are loaded into the loop counter to control the length of each instruction, are assigned the specified values for this microprogram:

VARIABLE	ASSIGNED VALUE	COMMENTS
PLO	0D HEX	LENGTH OF PLO SYNC FIELD
DTFLD	04 HEX	LENGTH OF DATA FIELD (128 X 4 = 512)
CRC	02 HEX	LENGTH OF CRC FIELD (USES CRC-16)
ECC	04 HEX	LENGTH OF ECC FIELD (USES ECC-32)
DTPAD	04 HEX	LENGTH OF DATA PAD AT END OF DATA FIELD

INST #	LABEL	SEQ	ADDR	TEST	POINT	PEN	COUNT	OUT	EXT
00	D1	TSJ	NEXT	ONE	0	0	1-1	0	CRC16
01	NEXT	TSJ	ID	ONE	0	0	6-1	0	SGOFF
02	ID	SHLP	RA	ONE	0	0	128-1	0	SPRE
03		TSJ	NEXT	SYNC	0	0	PLO-1	0	SMC
04		TSJ	NEXT	SYNC	0	0	1-1	0	0
05		TSJ	ID	EQ8	M(AM)	0	2-1	0	0
06		CI	STP	LNEQ	HEAD	1	1-1	0	TREG
07		TSJ	ID	EQ8	SSECT	0	CRC-1	0	SRCRC
08		SHLP	WT	CMD	0	0	1-1	0	SGOFF
09		RC	STP	NDERR	0	0	PLO-1	0	ECC32
0A	WT	SHLP	0	ZERO	M(SYNC)	0	1-1	WPRE	WGON
0B		SHLP	0	ZERO	M(MC)	0	1-1	WMISS	0
0C		SHLP	0	ZERO	M(DM)	0	4-1	FREG	SWDG
0D		LGLP	0	ZERO	0	0	ECC-1	0	0
0E		SHLP	0	ZERO	0	0	DTPAD-1	WCRC	0
0F		TSJ	HSKP	ZERO	M(SYNC)	0	1-1	FREG	SGOFF
10	RA	TSJ	0	ONE	0	0	2*PLO-1	0	SPRE
11		TSC	STP	SYNC	0	0	2*PLO-1	0	SMC
12		TSC	STP	SYNC	0	0	1-1	0	0
13		TSC	STP	EQ8	M(DM)	0	DTFLD-1	0	0
14		LGLP	0	ZERO	0	0	ECC-1	RDG	SRCRC
15		SHLP	0	ZERO	0	1	1-1	0	SGOFF
16		CI	HSKP	NDERR	3	0	ECC-2	SNDRM	0
17	XERR	SHLP	0	ZERO	0	1	1-1	SNDRM	0
18		TSJ	0	ONE	XFER	0	1-1	PREQ1	0
19		TSJ	0	ONE	0	0	1-1	PINT0	0
1A	HSKP	TSJ	0	ONE	SLEW	0	1-1	0	INCE
1B		SHLP	ID	ONE	ADDC1	0	1-1	PREQ1	ZRCLR
1C		CI	STP	XEND	SSECT	0	1-1	0	INCE
1D	CKFULL	TSJ	STP	NTP2	ADDC2	0	1-1	PREQ1	0
1E		RC	CKFULL	NOVFLW	0	0	6-1	0	0
1F	STP	TSJ	0	ZERO	0	0	0	DNINT	SGOFF

COMMENTS:

INST #	D31-D0	COMMENTS
00	0A 00 F0 81	PRESET THE CRC CHECKER.
01	0C 05 F0 82	SHUT READ GATE AND WRITE GATE OFF.
02	05 7F F0 10	WAIT HERE FOR 6 BYTE TIMES; PUT RA (INST #10) ON STACK. SET READ GATE AND START LOOKING FOR PLO SYNC (PREAMBLE) AS INSTRUCTION IS EXITED (VIA SPRE).
03	06 0C 20 80	LOOK FOR ALL 0'S; WAIT 128 BYTE TIMES; IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO NEXT (INST #1).
04	00 00 20 80	LOOK FOR THE MISSING CLOCK PATTERN FOR THE PLO TIME; IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO NEXT (INST #1).
05	00 01 84 82	LOOK FOR AN "FE" ADDRESS MARK VIA 8 BIT COMPARE (EQ8). IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO ID (INST #2).
06	08 80 9B 7F	LOOK FOR TRACK AND HEAD COMPARE; IF COMPARE, GO TO NEXT INSTRUCTION; ELSE, GO TO STP (INST #1F). THIS BRANCH MEANS THAT THE DISK IS ON THE WRONG TRACK. AT INSTRUCTION STP, THE LOCAL PROCESSOR WILL BE INTERRUPTED; READING THE PC REGISTER WILL TELL THE PROCESSOR THAT THE INTERRUPT WAS GENERATED BY THIS INSTRUCTION; A STEP ROUTINE WILL USUALLY BE EXECUTED BY THE LOCAL PROCESSOR. ALSO, THE TRACK AND HEAD NUMBER FROM THE DISK IS SAVED IN THE CURRENT REGISTER FILE.
07	02 01 8A 82	LOOK FOR SECTOR NUMBER COMPARE; IF COMPARE WITH DESIRED SECTOR (IN DESIRED REGISTER FILE), GO TO NEXT INSTRUCTION; ELSE, GO TO ID (INST #2).
08	0C 00 C0 0A	TEST FOR READ OR WRITE COMMAND. IF WRITE COMMAND, PUT WT (INST #0A) ON STACK (INST #02 PUT RA ON STACK PREVIOUSLY). AS INSTRUCTION IS EXITED, TURN OFF READ GATE. THE CRC IS CHECKED HERE.

COMMENTS:

INST #	D31-D0	COMMENTS
09	0B 0C 30 5F	CHECK FOR GOOD CRC. IF GOOD, LOAD THE STACK TO THE PC (GO TO EITHER RA OR WT). ELSE, GO TO STP (INST #F) TO END THE COMMAND. A RETRY CAN BE IMPLEMENTED IF DESIRED TO ATTEMPT TO READ THE ID A NUMBER OF TIMES.
0A	4F 00 05 00	THIS IS THE START OF THE WRITE ROUTINE; TURN WRITE GATE ON AND WRITE THE PLO SYNC (PREAMBLE) FIELD, PLO TIMES.
0B	50 00 06 00	WRITE THE MISSING CLOCK PATTERN.
0C	61 03 03 00	WRITE THE DATA MARK PATTERN. PREPARE DMA TRANSFER OF DATA FIELD FROM RING BUFFER AT NEXT INSTRUCTION.
0D	00 03 00 20	TRANSFER RING BUFFER DATA TO DISK FOR 4X128 TIMES.
0E	90 03 00 00	WRITE THE FOUR BYTE ECC FIELD.
0F	6C 00 05 9A	WRITE A FOUR BYTE DATA PAD AFTER THE ECC BYTES. GO TO HSKP (INST #1A; HOUSEKEEPING) FOR DMA UPDATES. TURN OFF WRITE GATE.
10	05 19 F0 80	THIS IS THE START OF THE READ COMMAND. PREPARE TO LOOK FOR ALL PLO SYNC FIELD. RAISE READ GATE AS INSTRUCTION IS EXITED.
11	06 19 20 BF	LOOK FOR PLO SYNC (PREAMBLE) FOR 2 X PLO TIME. IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO STP (INST #1F) WHICH WILL END THE COMMAND VIA A LOCAL PROCESSOR INTERRUPT. THE VALUE IN THE PC WILL INDICATE TO THE LOCAL PROCESSOR THAT A PLO SYNC (PREAMBLE) OF ALL 0'S WAS NOT FOUND IN THE ALLOTTED TIME AFTER A VALID ID WAS FOUND.
12	00 01 20 BF	LOOK FOR MISSING CLOCK PATTERN FOR 2 X PLO TIME. IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO STP (INST #1F) WHICH WILL END THE COMMAND VIA A LOCAL PROCESSOR INTERRUPT. THE VALUE IN THE PC WILL INDICATE TO THE LOCAL PROCESSOR THAT A MISSING CLOCK PATTERN WAS NOT FOUND IN THE ALLOTTED TIME AFTER A PLO SYNC (PREAMBLE) WAS FOUND.
13	00 03 83 BF	LOOK FOR "FB" DATA MARK. IF FOUND, GO TO NEXT INSTRUCTION; ELSE, GO TO STP (INST #1F) WHICH WILL END THE COMMAND VIA A LOCAL PROCESSOR INTERRUPT. THE VALUE IN THE PC WILL INDICATE TO THE LOCAL PROCESSOR THAT A DATA MARK WAS NOT FOUND AFTER A MISSING CLOCK PATTERN.
14	22 03 00 20	START THE TRANSFER OF DATA FROM THE DISK TO THE RING BUFFER VIA THE SIGNAL RDG WHICH REQUEST CHANNEL ACCESS TO THE RING BUFFER. THE DMA ADDRESS WILL AUTOMATICALLY BE INCREMENTED. START THE CHECKING OF THE ECC AS THIS INSTRUCTION IS EXITED.
15	0C 80 00 00	TRANSFER THE ECC BYTES TO THE CURRENT REGISTER FILE ADDRESSES 3, 2, 1 AND 0. TURN OFF READ GATE AS INSTRUCTION IS EXITED.
16	70 02 33 7A	CHECK FOR ECC ERROR. IF ERROR, GO TO NEXT INSTRUCTION; ELSE, GO TO HSKP (INST #1A; HOUSEKEEPING). TRANSFER FIRST ECC SYNDROME INTO CURRENT REGISTER FILE LOCATION 3.
17	70 80 00 00	THIS INSTRUCTION IS ENTERED IF AN ECC ERROR IS FOUND. TRANSFER THE REMAINING 3 BYTES OF ECC SYNDROME INTO CURRENT REGISTER LOCATIONS 2, 1, AND 0.
18	80 00 F0 80	SINCE DATA WAS BAD, REINITIALIZE THE DMA DISK ADDRESS REGISTER BACK TO THE BEGINNING OF THE SECTOR BY LOADING THE CONTENTS OF XFER (IN THE DESIRED REGISTER FILE), TO THE DMA DISK FUNCTION REGISTER CAUSING THE TRANSFER OF THE DISK REGISTER TO THE DISK ADDRESS.
19	C0 00 F0 80	GENERATE AN INTERRUPT TO THE LOCAL PROCESSOR VIA PINT0 WHICH IS USED FOR ECC ERROR INTERRUPTS. THIS INTERRUPT DELINKS THE OFFSET AND AUXILIARY OFFSET COUNTERS IN THE DMA BLOCK.
1A	0E 00 F9 80	THIS IS THE START OF THE DMA HOUSEKEEPING FUNCTION. THE LOCATION IN THE DESIRED REGISTER FILE LABELED SLEW IS INCREMENTED. LATER A TEST IS DONE TO DETERMINE IF ALL THE SECTORS IN THE COMMAND HAVE BEEN READ OR WRITTEN.
1B	8D 00 F1 02	ADD CONSTANT 1 REGISTER TO THE OFFSET COUNTER. PUT ADDRESS ID (INST #2) ON STACK; CLEAR ZERO FLAGS IN DMA BLOCK.
1C	0E 00 AA 7F	CHECK FOR END OF COMMAND VIA SLEW BEING INCREMENTED TO ZERO. IF END, GO TO STP (INST #1F); ELSE, GO TO NEXT INSTRUCTION. INCREMENT THE DESIRED REGISTER LOCATION CONTAINING THE SECTOR NUMBER TO BE OPERATED ON NEXT.

COMMENTS:

INST #	D31-D0	COMMENTS
1D	80 00 B2 9F	ADD CONSTANT 2 TO OFFSET COUNTER BUT DO NOT UPDATE THE OFFSET COUNTER. JUST UPDATE THE OVERFLOW BIT. IF TP2 IS A LOCIC ONE (NTP2 A ZERO), GO TO STP (INST #1F) BECAUSE A HALT, ABNORMAL DATA MARK OR DELETED DATA MARK HAS BEEN ENCOUNTERED. ELSE, GO TO NEXT INSTRUCTION.
1E	00 05 D0 5D	CHECK FOR OVERFLOW. IF OVERFLOW DURING WRITE, NO DATA IS CURRENTLY AVAILABLE TO WRITE; FOR READ, NO BUFFER SPACE IS AVAILABLE. IF OVERFLOW (NOVFLW = 0), GO TO CKFULL TO RECALCULATE THE OVERFLOW STATUS; IF NO OVERFLOW (NOVFLW = 1), PUT THE STACK (WHICH CONTAINS LOCATION ID; INST #02)INTO THE PC AND LOOK FOR THE NEXT ID.
1F	FC 00 00 80	THIS IS THE STOP LOCATION. A DONE INTERRUPT IS GENERATED TO THE LOCAL PROCESSOR AND THE READ AND WRITE GATES ARE TURNED OFF. THE MICROSEQUENCER IS STOPPED HERE BUT THE LOCAL PROCESSOR CAN READ THE PREVIOUS VALUE OF THE PC (THE LOCATION OF THE INSTRUCTION THAT BRANCHED TO HERE) VIA STATUS REGISTER 3 BITS D4-D0 TO DETERMINE HOW AND WHY THE COMMAND ENDED.

APPENDIX 2—DMA OPERATION EXAMPLES

It should be noted that a ">" indicates operations performed automatically by the MSD95C02.

EXAMPLE 1—LOCAL PROCESSOR LOADS DMA ADDRESS INTO DMA REGISTER FILE:

1. Write DMA FUNCTION Register to configure for MAILBOX → LOCAL PROCESSOR ADDR.

2a. Write DMA address MSB data to MAILBOX HIGH Register.

2b. Write DMA address LSB data to MAILBOX LOW Register.

This operation triggers the next event by setting the cycle request latch.

> transfer address data from Mailbox to DMA address register.

EXAMPLE 2—LOCAL PROCESSOR READS DMA ADDRESS:

1. Write DMA FUNCTION Register to configure for LOCAL PROCESSOR ADDR → MAILBOX.

The transfer will take place automatically after this step as follows:

> transfer address data from DMA address register to Mailbox.

Local processor may read DMA address data MSB's from the MAILBOX HIGH Register and DMA address data LSB's from the MAILBOX LOW Register. Bit 1 (REQUEST 1) of STATUS 1 Register can be used to determine when the operation is complete.

EXAMPLE 3—LOCAL PROCESSOR READS SEQUENTIAL RING BUFFER DATA:

The local processor will initialize the Address location in the DMA address register with the starting ring buffer address. The MSD95C02 will automatically fetch the data in that location and deposit it in the DATA Register. The Local Processor may program the MSD95C02 to increment the DMA address after every transfer via the DMA FUNCTION Register. This permits the Local Processor to read sequentially located data in the Ring Buffer without any address manipulation by the Local Processor.

1. Write DMA FUNCTION Register to configure for MAILBOX → LOCAL PROCESSOR ADDR.

2a. Write DMA address data to MAILBOX HIGH Register.

2b. Write DMA address data to MAILBOX LOW Register.

This operation triggers the following events by setting the cycle request latch.

> Transfer address data from the mailbox to the DMA ADDRESS Register.

> Output address data from LOCAL PROCESSOR ADDRESS Register to Ring Buffer.

> Fetch data from Ring Buffer, leave in DATA Register and reset the cycle request latch.

3. Write DMA FUNCTION Register to configure for LOCAL PROCESSOR ADDR. +1→LOCAL PROCESSOR ADDR.

4. Read DATA Register (set Cycle Request and Read latches) for data transfer.
   > MSD95C02 will output address data from LOCAL PROCESSOR ADDRESS Register to Ring Buffer.
   > MSD95C02 will increment address data in LOCAL PROCESSOR ADDRESS Register.
   > MSD95C02 will input data from Ring Buffer, store it in the DATA Register and reset the cycle request latch.

Data can be read sequentially by the local processor by continually reading the DATA Register. Each read of the DATA Register will automatically trigger a new ring buffer access cycle at the next sequentially located memory location.

EXAMPLE 4—LOCAL PROCESSOR WRITES SEQUENTIAL DATA TO RING BUFFER:

The Local Processor will initialize the address location in the DMA address register with the ring buffer address. The MSD95C02 will automatically fetch the data in that location and leave it in the DATA Register. The Local Processor may program the MSD95C02 to increment the DMA address after every transfer via the DMA FUNCTION Register. This permits the Local Processor to sequentially write data into the Ring Buffer without any address manipulation by the Local Processor.

1. Write DMA FUNCTION Register to configure for MAILBOX → LOCAL PROCESSOR ADDRESS.

2a. Write DMA address data to MAILBOX HIGH Register.

2. Write DMA address data to MAILBOX LOW Register.

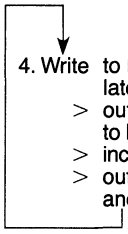
This operation triggers the next event by setting the cycle request latch.

> Transfer address data from Mailbox to DMA address register.

> Output address data from DMA address register to Ring Buffer.

> Fetch data from Ring Buffer and leave in DATA Register; Reset cycle request latch.

3. Write DMA FUNCTION Register to configure for LOCAL PROCESSOR ADDRESS +1 → LOCAL PROCESSOR ADDRESS.



4. Write to DATA Register (set Cycle Request and Write latches) for data transfer.
   > output address data from DMA address register to Ring Buffer.
   > increment address data in DMA address register.
   > output data from DATA Register to Ring Buffer and reset the cycle request latch.

Data can be written sequentially by the local processor by continually writing the DATA Register. Each write to DATA Register will automatically trigger a new ring buffer access cycle at the next sequentially located memory location.

EXAMPLE 5—DATA IS READ FROM THE DISK AND WRITTEN INTO THE RING BUFFER AND SIMULTANEOUSLY, DATA IS READ FROM THE RING BUFFER OUT OVER THE EXTERNAL CHANNEL (SCSI):

This function of filling the Ring Buffer from the disk data and emptying the Ring Buffer over the external channel involves two independent and simultaneous operations. The description of this example will explain the local processor's involvement in this example. It is the role of the local processor to set up the DMA controller block such that the two operations can take place. Once the external channel's DMA registers are set up, the operation involves a simple DMA request-acknowledge handshake to empty the buffer. Automatic throttling on the DMA acknowledge to the external channel will occur as described in the section on the DMA block operation.

In addition, there is a MICROSEQUENCER routine that is executed when the Local Processor causes a command to be started. The details of the MICROSEQUENCER routine is described in appendix 1.

It is the role of the Local Processor to initialize the OFFSET and AUXILIARY OFFSET COUNTERs, CONSTANT 1 and CONSTANT 2 Registers, as well as the starting ring buffer addresses for the disk and external channel data. The MICROSEQUENCER will assume that these registers are initialized and use then accordingly to calculate buffer full/empty status which is used to automatically throttle the DMA request coming from the disk, which are initiated and controlled by the MICROSEQUENCER, and the External Device DMA requests.

For this example, it is assumed that the sector size is 512, and the ring buffer size is 2K.

1. The Local Processor will set the DMA FUNCTION Register for a Mailbox to OFFSET COUNTER transfer and write 00H into the MAILBOX HIGH and LOW Registers (generating a dummy request).
   > Initialize OFFSET and AUXILIARY OFFSET COUNTERs with 00H and reset cycle request.
2. The Local Processor will set the DMA FUNCTION Register for a Mailbox to CONSTANT 1 location transfer and write a value of 512 (the sector size) into the MAILBOX HIGH and LOW Registers, generating a dummy request.
   > Transfer value 512 from Mailbox to CONSTANT 1 location and reset cycle request.
3. The Local Processor will set the DMA FUNCTION Register for a Mailbox to CONSTANT 2 location transfer and write the value 64K − 2K + 512 − 1 into the MAILBOX HIGH and LOW Registers. The General form for CONSTANT 2 is [64K − (BUFFER SIZE) + (SECTOR SIZE) − 1], generating a dummy request.
   > Transfer value 64K − 2K + 512 − 1 from Mailbox to CONSTANT 2 location and reset cycle request.
4. The Local Processor will set the DMA FUNCTION Register for a Mailbox to External Device Address location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.
   > Transfer start address from Mailbox to External Device Address location and reset cycle request.
5. The Local Processor will set the DMA FUNCTION Register for a Mailbox to DISK Address location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.
   > Transfer start address from Mailbox to disk address location and reset cycle request.
6. The Local Processor will set the DMA FUNCTION Register for a Mailbox to DISK Register location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.
   > Transfer start address from Mailbox to DISK Register location and reset cycle request.
7. Write the sector ID information and the number of sectors to be read (SLEW) into the appropriate locations in the DESIRED REGISTER FILE registers and issue a Start Command with the Disk Direction bit set to one and the External Device Direction bit set to zero. External device DMA requests can start at any time since they will not be acknowledged until one error free sector is deposited into the Ring Buffer. The MICROSEQUENCER routine will ensure that the OFFSET COUNTER is incremented by the sector size (512) when the MSD95C02 finishes transferring an error free sector into the Ring Buffer.
8. When the OFFSET COUNTER is greater than zero, the external channel's DMA requests will be acknowledged. The OFFSET COUNTER will be decremented by 1, 2, 3 or 4 (depending on the programming of MODE 1 Register) every time the external channel reads data from the Ring Buffer.
9. The MICROSEQUENCER will add the OFFSET COUNTER value and CONSTANT 2 together before beginning the next sector transfer into the Ring Buffer. This calculation is done to determine buffer full/empty status. This is done without altering the contents of the OFFSET COUNTER.
   > If ALU Overflow status is active, then the buffer is full.

> If the OFFSET COUNTER equals zero, then the buffer is empty.

If the buffer is full, the MSD95C02 will wait before transferring the next sector into it. If the buffer is empty, the External Channel's DMA requests will not be serviced.

EXAMPLE 6—DATA IS WRITTEN TO THE DISK BY SIMULTANEOUSLY WRITING TO THE RING BUFFER FROM THE EXTERNAL CHANNEL AND READING FROM THE RING BUFFER FOR DATA TRANSFER ON TO THE DISK.

This function of filling the Ring Buffer from the EXTERNAL CHANNEL and emptying the Ring Buffer for data transfer to the disk involves two independent and simultaneous operations. The description of this example will explain the Local Processor's involvement in this example. It is the role of the Local Processor to set up the DMA controller block such that the two operations can take place. Once the External Channel's DMA registers are set up, the operation involves a simple DMA request-acknowledge handshake to start filling the buffer. Automatic throttling on the DMA acknowledge to the External Channel will occur if the buffer becomes full.

In addition, there is a MICROSEQUENCER routine that is executed when the Local Processor causes a command to be started. The details of the MICROSEQUENCER routine is described in appendix 1.

It is the role of the Local Processor to initialize the OFFSET and AUXILIARY OFFSET COUNTERs, CONSTANT 1 and CONSTANT 2 Registers, as well as the starting ring buffer addresses for the disk and external channel data. The MICROSEQUENCER will assume that these registers are initialized and use then accordingly to calculate buffer full/empty status which is used to automatically throttle the DMA request coming from the disk, which are initiated and controlled by the MICROSEQUENCER, and the external channel's DMA requests.

For this example, it is assumed that the sector size is 512, and the Ring Buffer size is 2K.

1. The Local Processor will set the DMA FUNCTION Register for a Mailbox to Offset Counter transfer and write 512 into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   Initialize OFFSET and AUXILIARY OFFSET COUNTERs with 512 and reset cycle request.

2. The Local Processor will set the DMA FUNCTION Register for a Mailbox to Constant 1 location transfer and write a value of 512 (the sector size) into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   > Transfer value 512 from Mailbox to Constant 1 location and reset cycle request.

3. The Local Processor will set the DMA FUNCTION Register for a Mailbox to Constant 2 location transfer and write the value 64K − 2K + 512 − 1 into the MAILBOX HIGH and LOW Registers. The General form for CONSTANT 2 is [64K − (BUFFER SIZE) + (SECTOR SIZE) − 1], generating a dummy request.

   > Transfer value 64K − 2K + 512 − 1 from Mailbox to Constant 2 location and reset cycle request.

4. The Local Processor will set the DMA FUNCTION Register for Mailbox to External Device address location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   > Transfer start address from Mailbox to External Device Address location and reset cycle request.

5. The Local Processor will set the DMA FUNCTION Register for a Mailbox to DISK Address location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   > Transfer start address from Mailbox to disk address location and reset cycle request.

6. The Local Processor will set the DMA FUNCTION Register for a Mailbox to DISK Register location transfer and write the buffer starting address into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   > Transfer start address from Mailbox to DISK Register location and reset cycle request.

7. Start the transfer of sector data from the External Device to the Ring Buffer. Since the OFFSET COUNTER is decremented as information is deposited into the Ring Buffer from the external channel, and the OFFSET COUNTER is initialized to 512, it will hit zero after one sector is written into the Ring Buffer. Loading the OFFSET Register with 512 initially, ensures that there is at least 1 sector of data in the Ring Buffer before disk writing is started.

8. The Local Processor will set the DMA FUNCTION Register for a Mailbox to OFFSET COUNTER transfer and write 64K − 512 + 1 into the MAILBOX HIGH and LOW Registers, generating a dummy request.

   > Initialize OFFSET COUNTER with 64K − 512 + 1 and reset cycle request.

   The External Device is free to continue data transfer into the Ring Buffer.

9. Write the sector ID information and the number of sectors to be written (SLEW) into the appropriate locations in the DESIRED REGISTER FILE registers and issue a Start Command with the Disk Direction bit set to 0 and the External Device Direction bit set to 1. This starts a MICROSEQUENCER routine to transfer data from the Ring Buffer to the disk. The OFFSET COUNTER is incremented by 512 when the MSD95C02 finishes transferring a sector from the Ring Buffer to the disk.

10. Before transferring a sector to the disk, the MICROSEQUENCER will add the OFFSET COUNTER value and CONSTANT 2 (64K − 512 + 1). This calculation allows the MICROSEQUENCER to determine if at least 1 more sector resides in the Ring Buffer by checking the overflow flag in the DMA's ALU. This is done without altering the contents of the OFFSET COUNTER. If it is determined that the buffer is empty (overflow = 1), all DMA requests for data to the Ring Buffer, which are initiated by the MICROSEQUENCER, will be held off.

11. If the buffer is full (OFFSET COUNTER = zero), DMA requests from the External Device will not be serviced.

APPENDIX 3. ERROR CORRECTION ON THE FLY:

In order to perform error correction on the fly, a Reed Solomon ECC with CRC extension is recommended. When a disk read operation detects an error, the MICROSEQUENCER program will set Program Interrupt 0 (PROG 0) which automatically delinks the OFFSET the AUXILIARY OFFSET COUNTERs. Further, the microprogram will cause the error syndrome bytes to be transferred into designated sequential locations in the DESIRED REGISTER FILE. The generation of this interrupt will also permit the Local Processor access to the CURRENT REGISTER FILE. Transfer of data into the Ring Buffer from the disk and out of the Ring Buffer to the external channel will continue simultaneous to the error correction operation.

When the Local Processor gets an interrupt, it will read the error syndrome bytes out to the CURRENT REGISTER FILE and then immediately write a logic one to bit D2 (CRR) of the START COMMAND REGISTER (ADDR 54H). This permits the disk to regain access to the CURRENT REGISTER FILE to allow proper processing of the next sector. Next, the Local Processor should use the error syndrome bytes to calculate the error pattern and location. Once this is performed, a read modify write operation to the calculated Ring Buffer locations will correct the error.

While this is going on, data will continue to be read from the disk and transferred out over the external channel. As new error free sectors are read, only the OFFSET COUNTER is increased by the sector size. As the external channel reads data out of the Ring Buffer, both the OFFSET and AUXILIARY OFFSET COUNTERs are decremented together. If the AUXILIARY OFFSET COUNTER reaches zero, the external channel's DMA requests are temporarily held off. Buffer full status is determined as usual by the MICROSEQUENCER using the value in the OFFSET COUNTER and CONSTANT 2.

Once the error has been corrected, the OFFSET and AUXILIARY OFFSET COUNTERS must be linked back together again. This is accomplished by loading the DMA FUNCTION Register (ADDR 50H) with a value 09 H. This special function will load the value of the OFFSET COUNTER into the AUXILIARY OFFSET COUNTER and permit these counters to both increment and decrement together. This function will be performed when the Local Processor writes any value into the MAILBOX LOW Register (ADDR 52H).

It should be noted that when errors occur on multiple sectors, this special function must not be initiated until all bad sectors are corrected.

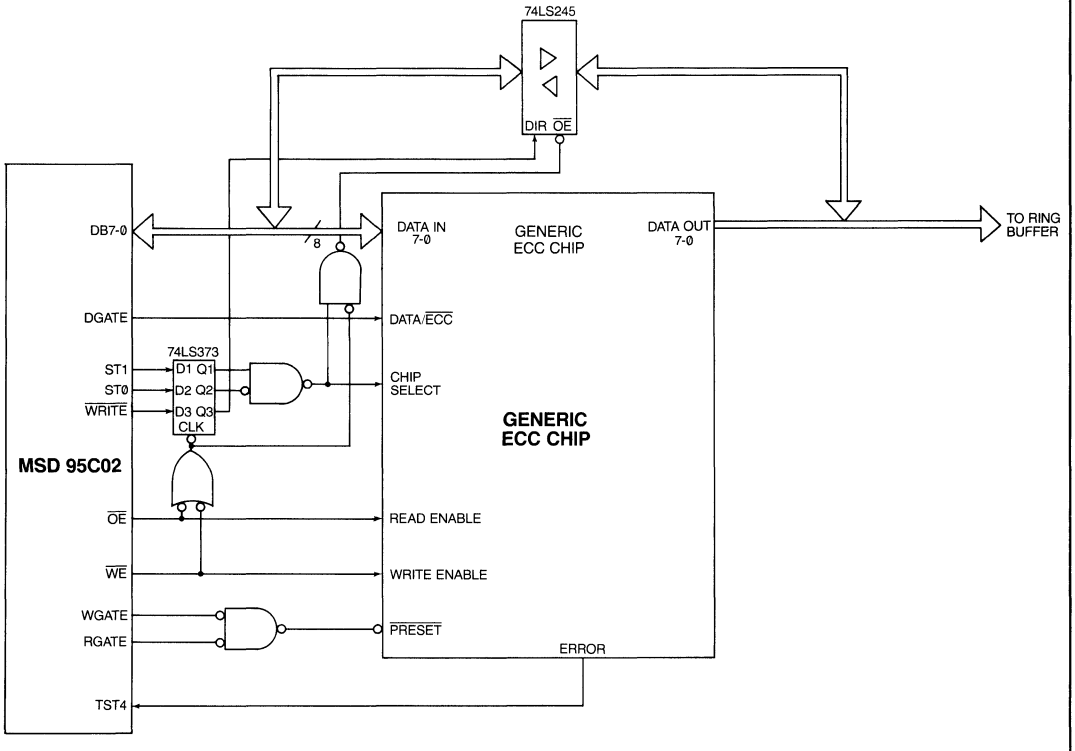


FIGURE 20: MSD 95C02 USED WITH OPTIONAL EXTERNAL ECC CHIP

APPENDIX 4—USE WITH AN EXTERNAL ECC CHIP

The MSD95C02 has been designed to allow operation with an external ECC chip. To allow this operation, it is necessary for the external ECC chip to be able to determine three situations.

1—The time when the MSD95C02 is performing a disk access cycle.

2—The disk access cycle is a read or write cycle.

3—The access cycle is for data transfer or ECC transfer.

Figure 20 shows connection to a generic ECC chip. The required information for proper operation is presented to the outside world via the signals DGATE, ST1, ST0 and $\overline{\text{WRITE}}$.

It should be noted that the DATA ERROR signal from the external ECC chip must be valid when it is checked by the MICROSEQUENCER.

APPENDIX 5—USE OF SYNC REGISTERS WITH RLL ENCODING:

For RLL encoding, two missing clock patterns are recommended.

1—For RLL 2, 7 type 1, a missing clock pattern of F0 is recommended along with a PLO SYNC pattern of 00. During the RLL encoding process, the PLO SYNC field of all zeros will encode on the disk as a repeating 100 pattern. If the PLO SYNC field is of such a length that an RLL encoding grouping ends at the 00 to F0 boundary, then reliable bit synchronization via missing clock pattern detection can occur. The length of the PLO SYNC field during disk writing can be controlled via microcode.

Loading 00 and F0 in DESIRED REGISTER FILE locations and outputting them to the disk via the microcode signal WPRE and WMISS, will produce a unique pattern on the disk. In order to read this unique pattern back and obtain bit synchronization via the high speed compare, the signal SMC is activated which will cause a compare between SYNC Registers 1 & 4 and the incoming decoded bit stream. For a valid compare, SYNC Registers 1 & 4 should be programmed with the following values:

SYNC 1 Register = F0
SYNC 4 Register = 0B

2—For RLL 2, 7 type 2, a missing clock pattern of 7A is recommended along with a PLO SYNC pattern of FF. During the RLL encoding process, the PLO SYNC field of all ones will encode on the disk as a repeating 1000 pattern. In this case, the length of the PLO SYNC field is not a critical parameter in obtaining reliable bit synchronization.

Loading FF and 7A in DESIRED REGISTER FILE locations and outputting them to the disk via the microcode signal WPRE and WMISS, will produce a unique pattern on the disk. In order to read this unique pattern back and obtain bit synchronization via the high speed compare, the signal SMC is activated which will cause a compare between SYNC Registers 1 & 4 and the incoming decoded bit stream. For a valid compare, SYNC Registers 1 & 4 should be programmed with the following values:

SYNC 1 Register = 7A
SYNC 4 Register = 00

The two cases above assume that bit D3 of MODE 2 Register (8/16 COMPARE) is set to select the 16 bit compare mode.

APPENDIX 6—OUTLINE OF REED SOLOMON ERROR CORRECTION AND VERIFICATION ROUTINES

The Reed Solomon ECC has been designed to permit the user correction of a maximum of two error bursts. The ability to correct two burst errors is generally associated with Reed Solomon codes. Using Reed Solomon alone, there is a finite probability of miscorrection if the error appearing in the data falls outside the capability of the Reed Solomon code used.

The MSD95C02 allows the user to attach an optional CRC field to the Reed Solomon ECC field to permit detection of virtually all miscorrected data.

The following steps should be performed to successfully correct a data error via Reed Solomon ECC and verify that the correction was performed properly:

1. If an error is detected, the MICROSEQUENCER will interrupt the Local Processor with the syndrome bytes (information used to correct the error) and the CRC field residing in the CURRENT REGISTER FILE.

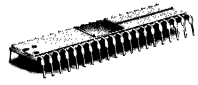
2. The Local Processor will read the syndrome and CRC bytes and use the syndrome bytes to calcuate the error pattern (exclusive OR mask) and error location (in the Ring Buffer memory). This calculation is performed via table lookup in software. For the Reed Solomon code implemented in the MSD95C02, three tables of 256 bytes each are required. These three tables are a Log, antilog and root table. The generation of the error pattern will require a maximum of 6 recursive table lookups and the generation of the error location will require a maximum of 3 recursive table lookups. It is this routine that will indicate if the error in the data is correctable or uncorrectable.

3. Once the error location and error pattern are determined, the Local Processor will set up the DMA block to perform the required read-modify-write operation to correct the error.

4. Once the error is corrected, the Local Processor should verify if the error was corrected properly. This is done by taking the error pattern generated in step 2 and performing another table lookup (uses the same antilog table as step 2) and taking this result and exclusive ORing it with one of the CRC bytes read in from the CURRENT REGISTER FILE in step 1. This is performed for each interleave. The result of these operations should yield zero if the error was corrected properly and yield a non zero if the error was not corrected properly.

Details of the three tables and actual software routines will be available in associated application notes.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX-510-227-8898



Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-9600 XX[1]	90	4	2 or N Key Rollover	-PRO -STD	Binary Sequential ASCII	+5	40 DIP/ 44 SMT	739-752
KR-9601 XX[1]	90	4	2 or N Key Rollover; caps-lock, auto-repeat	-STD -012[2]	Binary Sequential ASCII	+5	40 DIP/ 44 SMT	739-752
KR-9602 XX[1]	90	4	2 or N Key Rollover; caps-lock, auto-repeat, serial output	-STD -012[2]	Binary Sequential ASCII	+5	28 DIP/ 28 SMT	739-752

[1]May be custom mask programmed [2]For future release

STANDARD MICROSYSTEMS CORPORATION

KR9600
KR9601
KR9602

Keyboard Encoder Read Only Memory
KEM

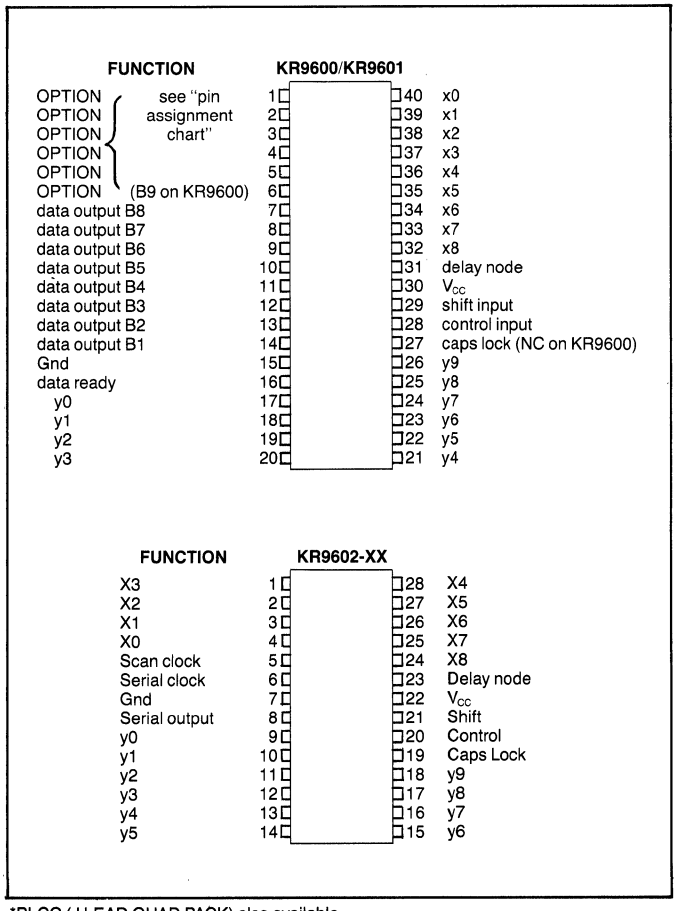
FEATURES

- ☐ On-chip "caps" lock (KR9601, KR9602)
- ☐ On-chip auto repeat (KR9601, KR9602)
- ☐ Contact bounce protection
- ☐ N Key Rollover or Lockout operation
- ☐ Hysteresis on keyboard matrix inputs
- ☐ Tri-state TTL compatible data outputs
- ☐ Serial output (on KR9602 only)
- ☐ Quad Mode (Normal, shift, control, shift-control)
- ☐ High frequency clock input
- ☐ Pin-compatible with KR3600 (KR9600)
- ☐ Static charge protection on all inputs and outputs
- ☐ +5 volt supply

EXTERNALLY SELECTABLE OPTIONS ON KR9600 AND KR9601

- ☐ Pulse or level data ready output signal
- ☐ External clock input
- ☐ On chip master/slave oscillator
- ☐ All 10 output bits available
- ☐ Lockout/Rollover external selection
- ☐ Chip enable external selection
- ☐ Data complement control
- ☐ Any Key Down output
- ☐ Selectable Auto-Repeat rate
- ☐ Programmable Auto-Repeat rate

PIN CONFIGURATION*



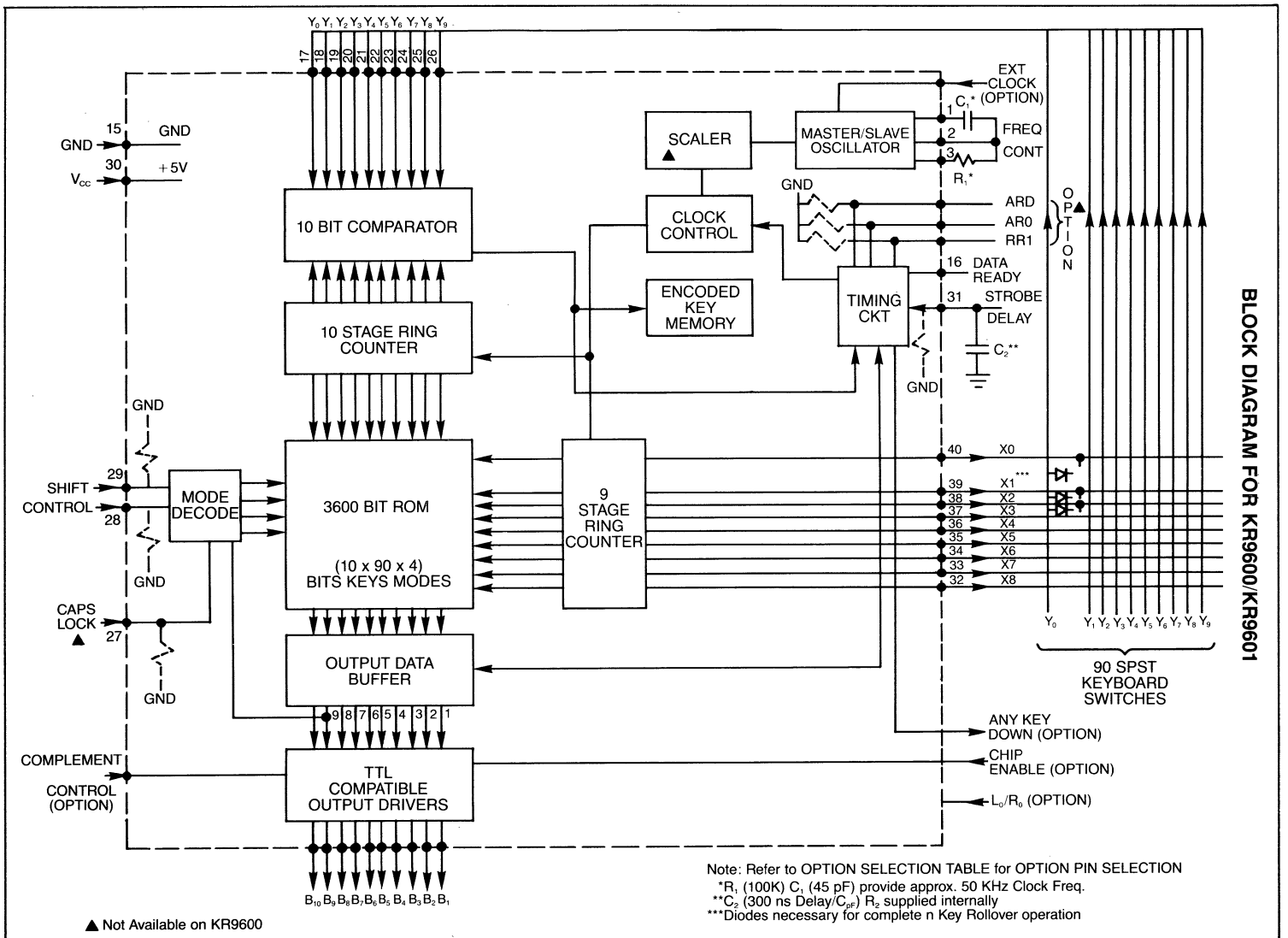
*PLCC (J LEAD QUAD PACK) also available.

GENERAL DESCRIPTION

The KR9600/1/2 is a keyboard encoder that contains all the logic necessary to debounce and encode SPST keyswitches into a fully decoded data output of up to 10 bits. The KR9600/1/2 contains a 3600 bit ROM, 9 stage and 10 stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for N key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer and TTL compatible output drivers.

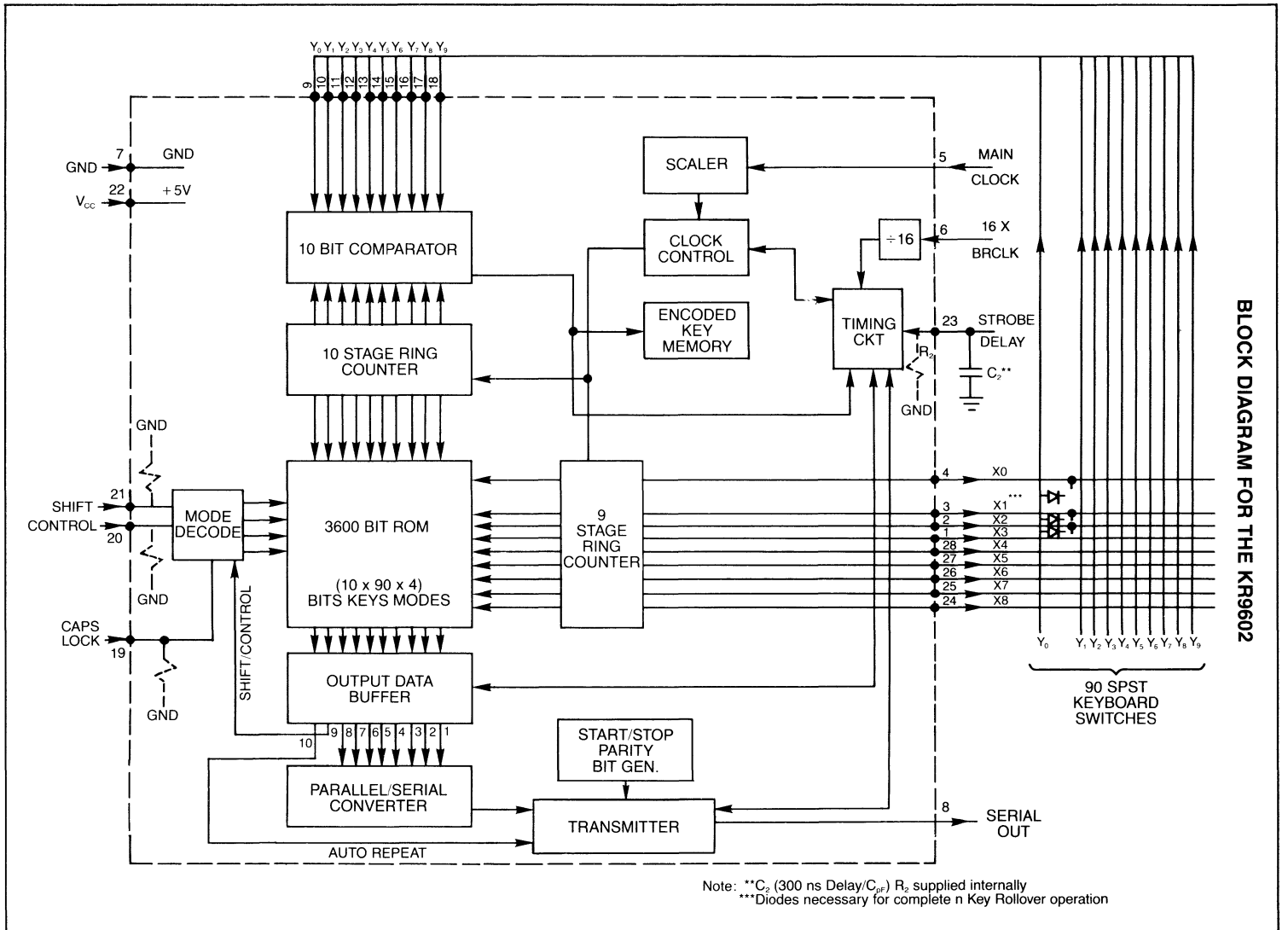
The KR9600 and the KR9601 provide a parallel data output in a 40 pin configuration with pin selectable options, while the KR9602 provides a serial asynchronous output in a 28 pin configuration with mask programmable options. (Ref. KR9600/1/2 custom coding information sheet).

SECTION VIII



Note: Refer to OPTION SELECTION TABLE for OPTION PIN SELECTION
*R_1 (100K) C_1 (45 pF) provide approx. 50 KHz Clock Freq.
**C_2 (300 ns Delay/C_{pF}) R_2 supplied internally
***Diodes necessary for complete n Key Rollover operation

▲ Not Available on KR9600



Note: **C_2 (300 ns Delay/C_{pF}) R_2 supplied internally
***Diodes necessary for complete n Key Rollover operation

BLOCK DIAGRAM FOR THE KR9602

DESCRIPTION OF PIN FUNCTIONS

NAME	SYMBOL	KR9600 PIN #	KR9601 PIN #	KR9602 PIN #	FUNCTION
X OUTPUTS	X0-X8	40-32	40-32	4-1 28-24	External outputs from the 9-stage ring counter to the keyboard to form X-Y matrix with the keyboard switches as the crosspoints.
Y INPUTS	Y0-Y9	17-26	17-26	9-18	External inputs from the keyboard X-Y matrix.
EXTERNAL CLOCK (see note)	***	1	1	5	External clock input.
SERIAL CLOCK	***	***	***	6	Serial input Baud rate clock, for KR9602.
DATA OUTPUTS	B8-B1	7-14	7-14	8	Data outputs B1-B8. Parallel outputs for the KR9600/9601, serial output for the KR9602.
DATA READY	DR	16	16	N/A	This output, which can be a level or a pulse, signals that a key closure has been detected and that data is available at the output port.
DELAY NODE INPUT	DELAY	31	31	23	Externally controllable delay network for eliminating the effect of switch contact bounce.
SHIFT INPUT	SHIFT	29	29	21	This input is used to select the shift mode data.
CONTROL INPUT	CNTRL	28	28	20	This input is used to select the control mode data. Simultaneous assertion of shift and control inputs will place the encoder into the shift-control mode.
CAPS LOCK	CAPS	see note	27	19	This input "ANDed" with bit B9 of the ROM will cause a mode shift. See "programming options".
POWER SUPPLY	V_{CC}	30	30	22	+5V power supply.
GROUND	Gnd	15	15	7	Ground.
OPTION PINS		see note	1-6	N/A	See option selection table for pin assignment.

Note: Caps Lock and Auto-Repeat are not available on KR9600.
See option selection table for pin assignment.

DESCRIPTION OF OPERATION

The main clocks for the KR9600 and KR9601 are derived from either an external clock source or the Internal oscillator. The KR9602 requires an external clock. The external clock is routed to a divider with a mask programmable division rate from 1 to 63 to generate the internal clock.

The keys are scanned in a nine output by ten input matrix, each key having a unique input-output combination connected to it. The inputs all go selectively to a level detector which has logically variable (1's and 0's) levels and hysteresis. The outputs are enabled one at a time from output X0 towards X8, at a rate of 10-100KHz, through a 9 stage ring counter. The 10 inputs are searched one at a time from Y0 to Y9, through a 10 stage ring counter, each time one of the outputs is enabled. The output and input pins all have pullups to V_{CC} and are precharged each clock even if the scan is stopped at one key. When a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10 stage ring counter and the key has not been encoded, the switch bounce delay network is enabled. The key down stroke is examined, without advance to the next key location, until the key has been stable for the length of the DELAY CAP pin to discharge. The code for the depressed key is transferred to the output data buffer and the data ready signal appears.

The scan has two modes as determined by the LOckout/Rollover option. Once a key is determined to be down the scan will not advance if in the LOckout mode. Consequently a new key closure is not detected until the previously depressed key is released. The scan sequence will resume upon key release and the output data buffer stores the code of the last key encoded. In the Rollover mode a "1" is stored in the encoded key memory and the scan sequence is resumed and the code for the last encoded key remains in the data output buffer. Each depressed key is encoded regardless of the state of the previously depressed keys. The internal keyboard ROM is 10 bits wide. Bits 1-8 are output via data outputs B1-B8. Bits 9 and 10 may be output as data and/or utilized respectively for Caps-lock and Auto-repeat select. This allows mask programmable selection of which keys will have caps-lock and auto-repeat. When selected, the auto repeat will commence with a "long" delay after key depression followed by "short" delays. The duration of the delays varying with the clock frequency and the state of the ARD, AR0, and AR1 signals.

A Chip Enable input is available to enable the parallel output buffer. Data Ready can be put in the high-impedance state with Chip Enable (CE) or can be open drain as a mask programmable option to facilitate wire-oring as an interrupt.

In the serial output version of KR9602, when a key is debounced and then called valid, the serial shift register is loaded with the data (8 bits B1-B8) from the ROM, the data from the parity generator, and the data from the start and stop bits generator. Bits B9 and B10 are internally used respectively for Caps-lock and Auto-repeat select. The data register is then allowed to shift data out at the rate of one bit per 16 clocks of the baud rate clock pin, on the negative edge of that clock. If the baud rate clock is too slow with respect to the internal clock, and the keyboard were allowed to continue scanning when the data register is loaded, then new data could be loaded on top of shifting-out data.

To avoid this, if a new key is depressed before the previous data is fully shifted out of the device, including the stop bits, the delay cap will be allowed to decay but the internal logic will delay its effect until the shift out of the previous data is completed. If the new key is released before the end of the extended delay time it will not be encoded.

OPTION SELECTION TABLE

Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to ten bits can be programmed into the KR9600/KR9601 ROM covering most popular codes such as ASCII, EBCDIC, SELECTRIC etc. as well as many specialized codes.*

Pin Assignment for KR9600/KR9601

The chip pins from pin #1 thru pin #6 are optionally connected to differing logic functions. Many of the functions are available on more than one pin.

PIN	FUNCTION (input unless noted)
1	Ext clock (opt. internal divisor of 1-63)**
1	Pin 1 of Internal oscillator.
2	Pin 2 of Internal oscillator.
2	Lo/Ro CC CE ARD** AR0** AR1**
3	Pin 3 of Internal oscillator.
3	Lo/Ro CC CE ARD** AR0** AR1**
4	AKO output
4	Lo/Ro CC CE ARD** AR0** AR1**
5	AKO or B10 output
5	Lo/Ro CC CE ARD** AR0** AR1**
6	B9 or AKO** output

Options Available for the KR9602:

The following options can be obtained on the KR9602 only with a mask program, and are not pin selectable:

Lo/Ro, CC, AUTO-REPEAT, LONG DELAY, SHORT DELAY, CLOCK DIVISOR 1,2,4,8,16,32,63; PARITY, 1 OR 2 STOP BITS.

Legend

CC = COMPLEMENT CONTROL
Lo/Ro = LOCKOUT/ROLLOVER
AKO = ANY KEY DOWN
CE = CHIP ENABLE
B10 = B10 (DATA) OUTPUT
B9 = B9 (DATA) OUTPUT
INTERNAL CLOCK = SELF CONTAINED OSCILLATOR (Not available in KR9602)
EXTERNAL CLOCK = EXTERNAL FREQUENCY SOURCE
ARD = INITIAL AUTO-REPEAT DELAY
AR0, AR1 = SECONDARY AUTO-REPEAT DELAY, OR NO AUTO-REPEAT WHEN BOTH ARE FALSE.

*Contact local sales office for custom coding sheet.
**Not available on the KR9600.

PROGRAMMING OPTIONS

The various options on the KR9600 and KR9601 are user selectable via externally programmable pins, but they are fixed, internally mask programmed, for the KR9602.

Oscillator:

The main clocks are derived from either an external clock source or from the Internal oscillator. The resultant signal is then routed to a divider with a mask programmable division rate from 2 to 63. If no division is required then the divider is bypassed. The external clock requires one pin (pin #1), while the Internal oscillator needs three pins (pins #1, 2, 3) for frequency selection via an external resistor and capacitor.

Lockout/Rollover: LO/RO

This option selects the operation of the key scan when a new key is detected. In Lockout the scan stops as long as the key is down. In Rollover the scan stops till the new key is debounced by the DELAY CAP and the key code is output. Then the key position is marked as down and the scan continues until another new key is seen. The option is selected either by an external pin or internally mask programmed, fixed in either state. The external LOckout selection is optionally hi or low active. A pulldown resistor to ground is optional.

Complement Control: CC

This option inverts the logic true state of the DATA OUTPUTS and can optionally additionally invert the logic true state of the DATA READY pin. The option can be internally fixed as true or false where true will output a high logic level. When externally selected the option can be either input high or low active true. The pulldown to ground is optional.

Data Ready:

The data ready pin is optionally either a pulse or level upon an output state ready to transfer. This transfer occurs when a new key is encoded or when the current key is repeating via the repeat logic. This output is individually capable of being disabled via CE or inverted via CC. To invert DATA READY is to have the pulse go logic low or the level fall to logic low active when the output is allowed to drive out of the chip.

Any Key Down: AKO output

The AKO output is an indicator to tell that there is at least one key determined to be depressed. The output is optionally logic high or low true. The CE can be separately used to set the output in the high impedance mode. AKO will reset one full keyboard scan time after the last key is released. AKO cannot be inverted by CC (complement control).

Chip Enable: $\overline{CE}$

The chip enable option can be internally fixed to true or

SECTION VIII

can be externally selected. When an external pin is used the true level is only low true. The true state means that the outputs connected to CE will go to the driven state from the high-impedance condition. Output pins B1-B10 are always affected by Chip Enable (CE), optional for Data Ready and Any Key Down. A pulldown to ground is optional.

Shift Control Lock: S C L

These three pins determine what will be output in response to a new key being detected. The Caps Lock pin is optional on the KR9601 and KR9602 but it is not available on the KR9600. All three pins have optional pulldown resistors to ground. The Lock option is allowed if data bit nine of the ten data bits is programmed as true. In other words the Rom is read with no lock logic allowed, but with the full influence of the Shift and Control pins. This determines the B9 output which is used to see if this key can be shifted (be it a control code or not) by modifying the effect of the Shift upon a second read of the rom. The operation of the allowed Lock follows this table:

L	B9	S	C	Result		
F	F	F	F	N		
F	F	F	T	C		
F	F	T	F	S	L = CAPS LOCK	
F	F	T	T	SC	B9 = DATA OUTPUT B9	
					N = NORMAL	
F	T	F	F	N	S = SHIFT	
F	T	F	T	C	C = CONTROL	
F	T	T	F	S	SC = SHIFT and CONTROL	
F	T	T	T	SC		
T	F	F	F	N		
T	F	F	T	C		
T	F	T	F	S		
T	F	T	T	SC		
T	T	F	F	S	Force N–>S	allow shift (ie m–>M)
T	T	F	T	SC	Force C–>SC	shift of Control
T	T	T	F	*S/N	Opt Force S–>N	allow reverse (ie M–>m)
T	T	T	T	*SC/C	Opt Force SC–>C	remove shift in Shift-Control

*The mask programmable option for the removal of the shift is coded as either ON for all keys or OFF. Note that the B9 DATA output (and all the others) is the code of the second decode. Note that shift only occurs when both the lock is true and the unmodified code gives a B9 ROM output as true.

Repeat: ARD AR0 AR1

When the Auto-repeat option is selected and a key is pressed, either of two delays can be selected. Typically a long initial delay after the key is pressed, and short delays afterwards if the key is still pressed. These delays consist of a programmable number of scan frequency time clocks varying from 2 to 131071 clock times.

This option is masked programmable and dependent on the programming of the data bit 10 of the ten data outputs to be true for the resultant key code (after lock logic) and upon whether any repeat action should occur at all.

There are three optional pins associated with the auto repeat logic: AR0, AR1, and ARD. Each of these can individually optionally have a pulldown resistor to ground. ARD controls the selection of the initial repeat delay count code, while the combination of AR0 and AR1 controls the selection of the short delays as shown below. If no external pins are desired then those functions can be mask programmed.

TYPICAL INITIAL REPEAT DELAY COUNTS

ARD = hi 80000 clock times
ARD = low 40000 clock times

The repeat delays are selected by a two bit code where one decode is used to disable the repeat operation completely.

TYPICAL SECONDARY REPEAT COUNTS

AR0	AR1	Count
0	0	All Auto-Repeat Disabled
0	1	6250
1	0	3125
1	1	1250

Typical Example:

One typical approach would be to mask program ARD for only one long delay value and mask AR0 to ground. This way one can save two option pins for ARD and AR0 and still be able to select or disable auto-repeat via AR1 and have the option of having one fixed short delay value.

ROM Data:

The actual programming data is in 10 bit wide characters with four function codes for each key position. There are 90 key positions organized as 9 "X" outputs with 10 "Y" inputs. The four functions as previously defined are Control, Shift, Normal, and Shift-Control.

The use of the optional Lock requires the programming of the B9 data bit. The use of the optional Auto-Repeat requires the programming of the B10 data bit. If the B9 or B10 outputs are used then these will show the result of the contents of the "corrected" key function data bits. The "corrected" function is the possibly changed Normal to Shift etc. etc. so that the output is that of the 'Shifted key code' NOT that of the initial key code.

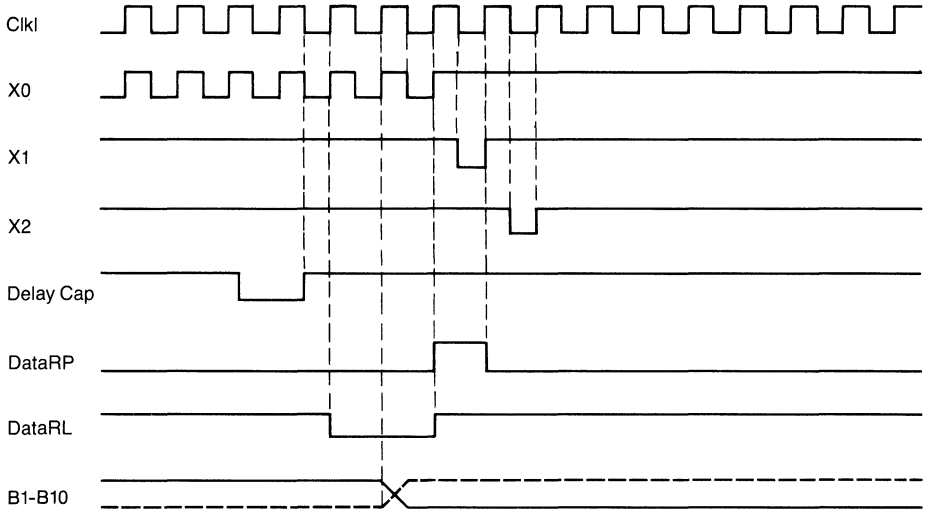
Minimum Switch Closure:

T = Switch bounce + (90 x 1/f) + Strobe delay + Strobe width

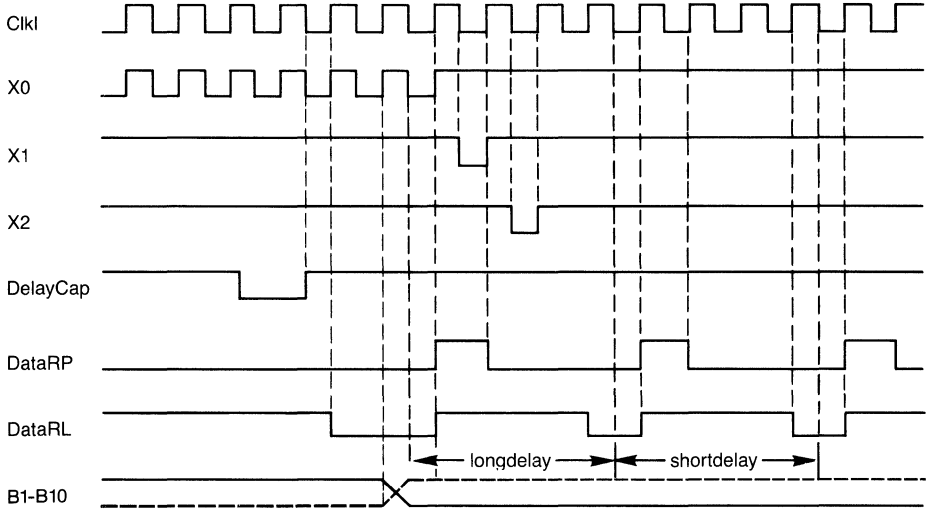
maximum expected	determined by frequency of operation	determined by external capacitance	minimum time required by external circuitry

CONDITIONS:

The clock divider is 1 so that Clkl is "same as clock IN".
A key is pressed down at X0Y0 but the delay cap has not timed out.
Data Ready is high true and we have already had another key.
DataRP = Data Ready as a Pulse DataRL = Data Ready as a Level



Condition: Test mode autorepeat at divide by 4 and keep key down



ELECTRICAL CHARACTERISTICS: KR9600, KR9601, KR9602

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range** ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level	V_{IL}			0.8	V	All inputs
High Level	V_{IH}	2.0			V	Except Y + 16X CLK
		2.2			V	16X CLK only
Y INPUTS						
High Level	V_{YIH}	2.8			V	Y input
Low Level	V_{YIL}			0.8	V	Y input
INPUT CURRENT						
Leakage	I_L			10.0	μA	All inputs except Y V_{IN} = 5V
Input with Pull-down resistor selected as option		75		220	μA	V_{IN} = 5V
Y inputs	I_{YIL}	−100	−400	−500	μA	V_{YIL} = 1 volt Y inputs only
OUTPUT VOLTAGE LEVELS						
Low Level	V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level	V_{OH}	2.4			V	I_{OH} = 100 μA Except X outputs
X output voltage	V_{OL}		0.4		V	600 μA
	V_{OH}	3.4	4.0		V	clock high I_{OH} = 10 μA
TRI-STATE LEAKAGE				10	μA	B1-B10
INPUT CAPACITANCE						
All inputs	C_{IN}			10	pF	Except Y inputs
POWER SUPPLY CURRENT	I_{CC}		20	40	mA	KR9600/01
	I_{CC}		15	35	mA	KR9602
A.C. CHARACTERISTICS						
CLOCK FREQUENCY*	F_{IN}	0.01		4	MHz	KR9601/02
		0.01		0.1	MHz	KR9600
16X CLOCK FREQUENCY		DC		640	KHz	KR9602
Chip enable access time	T_{CE}			250	ns	
SWITCH CHARACTERISTICS						
Min switch closure						see timing diagram
Contact closure resistance	Z_{CC}			300	ohms	
	Z_{CC}	1×10^7				

NOTE: The KR9600 is a direct replacement for the KR3600. Please note that due to the logic level of the KR9600, when replacing the KR3600 in a N-Key rollover system where diodes are utilized, the polarity of the diodes must be reversed.

* Divisor on KR9601/02 must be selected such that the resulting internal scan frequency is 10 KHz min to 100 KHz max.

** Parts optionally available in extended temperature ranges in hermetic packages. Inquire at factory.

KR9600-PRO DESCRIPTION

The KR9600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR9600 parts, the KR9600 PRO contains all of the logic to de-bounce and encode keyswitch closures, while providing either a 2-key or N-key rollover.

The output of the KR9600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR9600 is shown in Table I. The format is simple: output bits, 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256 x 8 PROM, and Figure 2 a full 90 key, 4 mode application utilizing a 512 x 8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

FIGURE 1
KR9600 PRO TYPICAL APPLICATION
64 KEY, 4 MODE

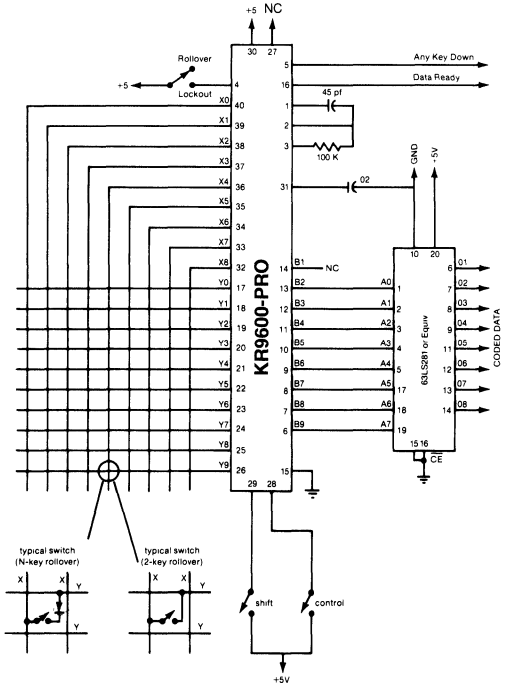
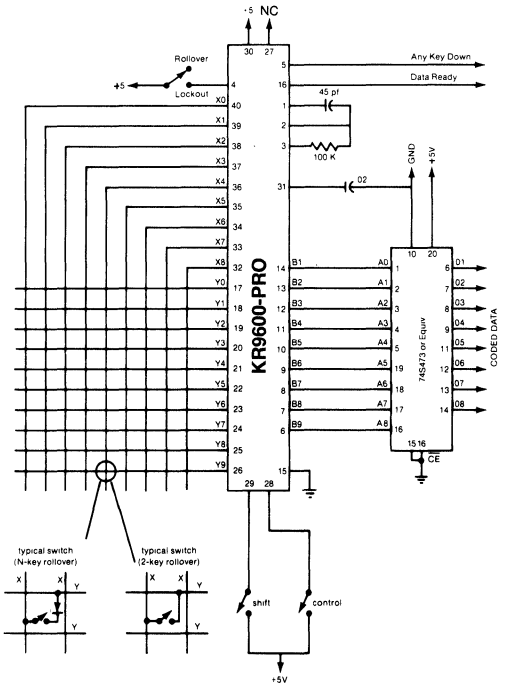


FIGURE 2
KR9600 PRO TYPICAL APPLICATION
90 KEY, 4 MODE



SECTION VIII

TABLE 1
KR9600-PRO CODING SHEET AND OPTIONS

XY	Normal B-12345678 910	Shift B-12345678 910	Control B-12345678 910	Shift/Control B-12345678 910
00	000000000	001000000	010000000	011000000
01	000000001	001000001	010000001	011000001
02	000000010	001000010	010000010	011000010
03	000000011	001000011	010000011	011000011
04	000000100	001000100	010000100	011000100
05	000000101	001000101	010000101	011000101
06	000000110	001000110	010000110	011000110
07	000000111	001000111	010000111	011000111
08	000001000	001001000	010001000	011001000
09	000001001	001001001	010001001	011001001
10	000001010	001001010	010001010	011001010
11	000001011	001001011	010001011	011001011
12	000001100	001001100	010001100	011001100
13	000001101	001001101	010001101	011001101
14	000001110	001001110	010001110	011001110
15	000001111	001001111	010001111	011001111
16	000010000	001010000	010010000	011010000
17	000010001	001010001	010010001	011010001
18	000010010	001010010	010010010	011010010
19	000010011	001010011	010010011	011010011
20	000010100	001010100	010010100	011010100
21	000010101	001010101	010010101	011010101
22	000010110	001010110	010010110	011010110
23	000010111	001010111	010010111	011010111
24	000011000	001011000	010011000	011011000
25	000011001	001011001	010011001	011011001
26	000011010	001011010	010011010	011011010
27	000011011	001011011	010011011	011011011
28	000011100	001011100	010011100	011011100
29	000011101	001011101	010011101	011011101
30	000011110	001011110	010011110	011011110
31	000011111	001011111	010011111	011011111
32	000100000	001100000	010100000	011100000
33	000100001	001100001	010100001	011100001
34	000100010	001100010	010100010	011100010
35	000100011	001100011	010100011	011100011
36	000100100	001100100	010100100	011100100
37	000100101	001100101	010100101	011100101
38	000100110	001100110	010100110	011100110
39	000100111	001100111	010100111	011100111
40	000101000	001101000	010101000	011101000
41	000101001	001101001	010101001	011101001
42	000101010	001101010	010101010	011101010
43	000101011	001101011	010101011	011101011
44	000101100	001101100	010101100	011101100
45	000101101	001101101	010101101	011101101
46	000101110	001101110	010101110	011101110
47	000101111	001101111	010101111	011101111
48	000110000	001110000	010110000	011110000
49	000110001	001110001	010110001	011110001
50	000110010	001110010	010110010	011110010
51	000110011	001110011	010110011	011110011
52	000110100	001110100	010110100	011110100
53	000110101	001110101	010110101	011110101
54	000110110	001110110	010110110	011110110
55	000110111	001110111	010110111	011110111
56	000111000	001111000	010111000	011111000
57	000111001	001111001	010111001	011111001
58	000111010	001111010	010111010	011111010
59	000111011	001111011	010111011	011111011
60	000111100	001111100	010111100	011111100
61	000111101	001111101	010111101	011111101
62	000111110	001111110	010111110	011111110
63	000111111	001111111	010111111	011111111
64	100000000	101000000	110000000	111000000
65	100000001	101000001	110000001	111000001
66	100000010	101000010	110000010	111000010
67	100000011	101000011	110000011	111000011
68	100000100	101000100	110000100	111000100
69	100000101	101000101	110000101	111000101
70	100000110	101000110	110000110	111000110
71	100000111	101000111	110000111	111000111
72	100001000	101001000	110001000	111001000
73	100001001	101001001	110001001	111001001
74	100001010	101001010	110001010	111001010
75	100001011	101001011	110001011	111001011
76	100001100	101001100	110001100	111001100
77	100001101	101001101	110001101	111001101
78	100001110	101001110	110001110	111001110
79	100001111	101001111	110001111	111001111
80	100010000	101010000	110010000	111010000
81	100010001	101010001	110010001	111010001
82	100010010	101010010	110010010	111010010
83	100010011	101010011	110010011	111010011
84	100010100	101010100	110010100	111010100
85	100010101	101010101	110010101	111010101
86	100010110	101010110	110010110	111010110
87	100010111	101010111	110010111	111010111
88	100011000	101011000	110011000	111011000
89	100011001	101011001	110011001	111011001

OPTIONS:

Internal Oscillator (Pins 1, 2, 3)
Lockout/Rollover (Pin 4)
  Internal Resistor to GND
Lockout is Logic 1
Pulse Data Ready
Any Key Down (Pin 5) Positive Output
  Internal Resistor to GND on Shift
  and Control Pins

CODING FOR KR9600–STD

XY	Normal	B-12345678910	Shift	B-12345678910	Control	B-12345678910	Shift Control	B-12345678910
00	1	1000111001	<	0011111001	1	1000111011	SUB	0101100001
01	q	1000110101	Q	1000100101	q	1000111111	DLE	0000100001
02	a	1000010101	A	1000000101	a	1000011111	@	0000000101
03	z	0101110101	Z	0101100101	z	0101111111	P	0000100101
04	HT	1001000001	HT	1001000001	HT	1001000001	I	1001000101
05	H	0001000101	H	0001000101	H	0001000101	H	0001000111
06	+	1101011001	+	1101011001	+	1101011001	+	1101011011
07	SO	0111001001	>	0111111001	SO	0111000001	SO	0111000011
08	p	0000110101	@	0000000101	NUL	0000000001	NUL	0000000001
09	1	1000111001	!	1000011001	SOH	1000000001	SOH	1000000001
10	2	0100111001	@	0000000101	2	0100111011	ETB	1110100001
11	w	1110110101	W	1110100101	w	1110111111		0011100101
12	s	1100110101	S	1100100101	s	1100111111	A	1000000101
13	x	0001110101	X	0001100101	x	0001111111	Q	1000100101
14	RS	0111100001	RS	0111100001	RS	0111100001	FS	0011100001
15	%	1010011001	%	1010011001	%	1010011001	%	1010011011
16	m	1011010101	]	1011100101	CR	1011000001	CR	1011000001
17	SI	1111000001	SI	1111000001	SI	1111000001	SI	1111000011
18	n	0111010101		0111100101	SO	0111000001	SO	0111000001
19	2	0100111001	"	0100011001	STX	0100000001	STX	0100000001
20	3	1100111001	#	1100011001	3	1100111011	NAK	1010100001
21	e	1010010101	E	1010000101	e	1010011111	DC3	1100100001
22	d	0010010101	D	0010000101	d	0010011111	B	0100000101
23	c	1100010101	C	1100000101	c	1100011111	R	0100100101
24	—	1111100100	—	1111100100	—	1111100100		0111100100
25	$	0010011001	$	0010011001	$	0010011001	$	0010011011
26	L	0011000101	L	0011000101	L	0011000101	L	0011000111
27	US	1111100001	US	1111100001	US	1111100001	US	1111100011
28	6	0110111001	&	0110011001	ACK	0110000001	ACK	0110000001
29	k	1101010101	[	1101100101	DEL	1111111101	DEL	1111111101
30	4	0010111001	$	0010011001	4	0010111011	DC4	0010100001
31	r	0100110101	R	0100100101	r	0100111111	ENQ	1010000001
32	f	0110010101	F	0110000101	f	0110011111	C	1100000101
33	SP	0000011000	SP	0000011000	SP	0000011000	SP	0000011000
34	CAN	0001101000	(	0001011000	CAN	0001100000	BS	0001000000
35	CR	1011000001	CR	1011000001	CR	1011000001	M	1011000101
36	[	1101111101	[	1101111101	[	1101111111	K	1101000101
37	VT	1101000000	VT	1101000000	VT	1101000000	VT	1101000010
38	7	1110111001	'	1110011001	BEL	1110000001	BEL	1110000001
39	"	0100011001	"	0100011001	"	0100011001	"	0100011011
40	5	1011111001	%	1010011001	5	1010111011	STX	0100000001
41	t	0010110101	T	0010100101	t	0010111111	EOT	0010000001
42	g	1110010101	g	1110000101	G	1110011111	D	0010000101
43	v	0110110101	V	0110100101	v	0110111111	S	1100100101
44	ETX	1100000001	ETX	1100000001	ETX	1100000001	ETX	1100000001
45	)	1011111101	)	1011111101	)	1011111111	N	0111000101
46	?	1111110001	?	1111110001	?	1111110011	[	1101100101
47	—	1011011001	—	1011111001	—	1011011001	—	1011011011
48	)	1001011001	)	1001011001	)	1001011001	)	1001011011
49	SP	0000011001	SP	0000011001	SP	0000011001	SP	0000011011
50	6	0110111001	>	0111111001	6	0110111011	SOH	1000000001
51	y	1001110101	Y	1001100101	y	1001111111	DC1	1000100001
52	h	0001010101	H	0001000101	h	0001011111	E	1010000101
53	b	0100010101	B	0100000101	b	0100011111	T	0010100101
54	:	0101111001	*	0101011001	:	0101111011	SYN	0110100001
55	>	0111111001	>	0111111001	>	0111111011	Z	0101100101
56	;	1101111001	+	1101011001	;	1101111011	Y	1001100101
57	NUL	0000000001	NUL	0000000001	NUL	0000000001	NUL	0000000001
58	*	0101011001	*	0101011001	*	0101011001	*	0101011011
59	!	1000011001	!	1000011001	!	1000011001	!	1000011011
60	7	1110111001	&	0110011001	7	1110111011	ETX	1100000001
61	u	1010110101	U	1010100101	u	1010111111	BEL	1110000001
62	j	0101010101	J	0101000101	j	0101011111	F	0110000101
63	n	0111010101	N	0111000101	n	0111011111	U	1010100101
64	=	1011110000	=	1011110000	=	1011110010	=	1011111100
65	<	0011111001	<	0011111001	<	0011111011	W	1110100101
66	p	0000110101	P	0000100101	p	0000111111	J	0101000101
67	0	0000111001	)	1001011001	0	0000111011	DC2	0100100001
68	&	0110011001	&	0110011001	&	0110011001	&	0110011011
69	#	1100011001	#	1100011001	#	1100011001	#	1100011011
70	8	0001111001	*	0101011001	8	0001111011	ESC	1101100001
71	i	1001010101	I	1001000101	i	1001011111	ACK	0110000001
72	k	1101010101	K	1101000101	k	1101011111	G	1110000101
73	m	1011010101	M	1011000101	m	1011011111	V	0110100101
74	/	1111011001	?	1111111001	/	1111011001	'	1110011001
75	'	1110011001	"	0100011001	'	1110011001	"	0100011001
76	LF	0101000000	LF	0101000000	LF	0101000000	GS	1011100000
77	'=	1011111001	+	1101011001	=	1011111001	+	1101011001
78	FF	0011001001	<	0011111001	FF	0011000001	FF	0011000011
79	(	0001011001	(	0001011001	(	0001011001	(	0001011011
80	9	1001111001	(	0001011001	9	1001111011	EM	1001100001
81	o	1111010101	O	1111000101	o	1111011111	]	1011100101
82	l	0011010101	L	0011000101	l	0011011111	X	0001100101
83	,	0011011001	,	0011011001	,	0011011001	,	0011011011
84	.	0111011001	.	0111011001	.	0111011001	.	0111011011
85	;	1101111001	;	0101111001	;	1101111001	;	0101111001
86	]	1011100101	[	1101100101	]	1011100101	[	1101100101
87	-	1011011001	—	1111100101	-	1011011001	—	1111100101
88	0	0000111001	0	0000111001	0	0000111001	0	0000111001
89	9	1001111001	)	1001011001	HT	1001000001	HT	1001000001

OPTIONS:

Internal Oscillator (Pins 1, 2, 3)
Any Key Down (Pin 4) Positive Output
N-Key Rollover only
Pulse Data Ready signal

Internal Resistor to GND on Shift and Control Pins
KR9600-STD outputs provides ASCII bits 1-6 on B1-B6, and bit 7 on B8

CODING FOR KR9601 AND KR9602 STD

XY	Normal B-12345678 910	Shift B-12345678 910	Control B-12345678 910	Shift/Control B-12345678 910
00	00000001 00	01010101 00	10101001 00	10101001 00
01	00000010 01	01010110 01	10101010 01	10101010 01
02	00000011 01	01010111 01	10101011 01	10101011 01
03	00000100 01	01011000 01	10101100 01	10101100 01
04	00000101 01	01011001 01	10101101 01	10101101 01
05	00000110 01	01011010 01	10101110 01	10101110 01
06	00000111 01	01011011 01	10101111 01	10101111 01
07	00001000 01	01011100 01	10110000 01	10110000 01
08	00001000 01	01011100 01	10110000 01	10110000 01
09	00001001 01	01011101 01	10110001 01	10110001 01
10	00001010 01	01011110 01	10110010 01	10110010 01
11	00001011 01	01011111 01	10110011 01	10110011 01
12	00001100 01	01100000 01	10110100 01	10110100 01
13	00001100 01	01100000 01	10110100 01	10110100 01
14	00001101 01	01100001 01	10110101 01	10110101 01
15	00001110 01	01100010 01	10110110 01	10110110 01
16	00001111 01	01100011 01	10110111 01	10110111 01
17	00010000 01	01100100 01	10111000 01	10111000 01
18	00010001 01	01100101 01	10111001 01	10111001 01
19	00010010 01	01100110 01	10111010 01	10111010 01
20	00010011 11	01100111 11	10111011 11	10111011 11
21	00010100 11	01101000 11	10111100 11	10111100 11
22	00010101 11	01101001 11	10111101 11	10111101 11
23	00010110 11	01101010 11	10111110 11	10111110 11
24	00010111 11	01101011 11	10111111 11	10111111 11
25	00011000 11	01101100 11	11000000 11	11000000 11
26	00011001 11	01101101 11	11000001 11	11000001 11
27	00011010 11	01101110 11	11000010 11	11000010 11
28	00011011 11	01101111 11	11000011 11	11000011 11
29	00011100 11	01110000 11	11000100 11	11000100 11
30	00011101 01	01110001 01	11000101 01	11000101 01
31	00011110 01	01110010 01	11000110 01	11000110 01
32	00011111 01	01110011 01	11000111 01	11000111 01
33	00011111 01	01110011 01	11000111 01	11000111 01
34	00100000 01	01110100 01	11001000 01	11001000 01
35	00100001 01	01110101 01	11001001 01	11001001 01
36	00100010 01	01110110 01	11001010 01	11001010 01
37	00100011 01	01110111 01	11001011 01	11001011 01
38	00100100 01	01111000 01	11001100 01	11001100 01
39	00100101 01	01111001 01	11001101 01	11001101 01
40	00100110 11	01111010 11	11001110 11	11001110 11
41	00100111 11	01111011 11	11001111 11	11001111 11
42	00101000 11	01111100 11	11010000 11	11010000 11
43	00101001 11	01111101 11	11010001 11	11010001 11
44	00101010 11	01111110 11	11010010 11	11010010 11
45	00101011 11	01111111 11	11010011 11	11010011 11
46	00101100 11	10000000 11	11010100 11	11010100 11
47	00101101 11	10000001 11	11010101 11	11010101 11
48	00101110 11	10000010 11	11010110 11	11010110 11
49	00101110 11	10000010 11	11010110 11	11010110 11
50	00101111 01	10000011 01	11010111 01	11010111 01
51	00110000 01	10000100 01	11011000 01	11011000 01
52	00110001 01	10000101 01	11011001 01	11011001 01
53	00110001 01	10000101 01	11011001 01	11011001 01
54	00110010 01	10000110 01	11011010 01	11011010 01
55	00110011 01	10000111 01	11011011 01	11011011 01
56	00110100 01	10001000 01	11011100 01	11011100 01
57	00110101 00	10001001 00	11011101 00	11011101 00
58	00110110 01	10001010 01	11011110 01	11011110 01
59	00110111 01	10001011 01	11011111 01	11011111 01
60	00111000 11	10001100 11	11100000 11	11100000 11
61	00111001 11	10001101 11	11100001 11	11100001 11
62	00111010 11	10001110 11	11100010 11	11100010 11
63	00111011 11	10001111 11	11100011 11	11100011 11
64	00111100 11	10010000 11	11100100 11	11100100 11
65	00111101 11	10010001 11	11100101 11	11100101 11
66	00111110 11	10010010 11	11100110 11	11100110 11
67	00111111 11	10010011 11	11100111 11	11100111 11
68	00111111 11	10010011 11	11100111 11	11100111 11
69	00111111 11	10010011 11	11100111 11	11100111 11
70	01000000 01	10010100 01	11101000 01	11101000 01
71	01000001 01	10010101 01	11101001 01	11101001 01
72	01000010 01	10010110 01	11101010 01	11101010 01
73	01000011 01	10010111 01	11101011 01	11101011 01
74	01000100 01	10011000 01	11101100 01	11101100 01
75	01000101 01	10011001 01	11101101 01	11101101 01
76	01000110 01	10011010 01	11101110 01	11101110 01
77	01000111 01	10011011 01	11101111 01	11101111 01
78	01001000 01	10011100 01	11110000 01	11110000 01
79	01001001 01	10011101 01	11110001 01	11110001 01
80	01001010 01	10011110 01	11110010 01	11110010 01
81	01001011 01	10011111 01	11110011 01	11110011 01
82	01001100 01	10100000 01	11110100 01	11110100 01
83	01001101 01	10100001 01	11110101 01	11110101 01
84	01001110 01	10100010 01	11110110 01	11110110 01
85	01001111 01	10100011 01	11110111 01	11110111 01
86	01010000 01	10100100 01	11110000 01	11111000 01
87	01010001 01	10100101 01	11110001 01	11111001 01
88	01010010 01	10100110 01	11111010 01	11111010 01
89	01010011 01	10100111 01	11111011 01	11111011 01

OPTIONS FOR THE KR9601-STD:

PINS 1, 2, 3 INTERNAL OSCILLATOR [Input clock divisor = 1]
PIN 4 CE [Active Low]
PIN 5 AR1 [AR0 fixed at Lo = 0]
[FIXED LONG DELAY OF 40000 CLOCK TIMES]
[FIXED SHORT DELAY OF 6250 CLOCK TIMES]
PIN 6 AKO [positive true]
Pulsed DATA READY signal
N-KEY ROLLOVER
Pull-down resistor to ground at the following pins:
_ SHIFT
_ CONTROL
_ CAPS-LOCK
_ ARO

OPTIONS FOR THE KR9602-STD:

N-KEY ROLLOVER
AUTO-REPEAT
(FIXED LONG DELAY OF 40000 CLOCK TIMES)
(FIXED SHORT DELAY OF 6250 CLOCK TIMES)
1 STOP bit.
No PARITY bit.
Input clock divisor of 63
Pull-down resistor to ground at the following pins:
—SHIFT
—CONTROL
—CAPS-LOCK

CODING FOR KR9602-012 (ASCII)

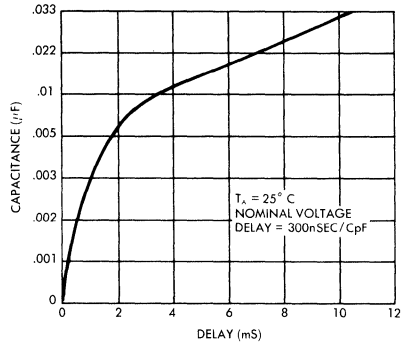
XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	0000110001	1001010001	0000110001	1001010001
01	1001110001	0001010001	1001110001	0001010001
02	0001110001	0101010001	0001110001	0101010001
03	1110110001	0110010001	1110110001	0110010001
04	0110110001	0111101001	0110110001	0111101001
05	1010110001	1010010001	1010110001	1010010001
06	0010110001	0010010001	0010110001	0010010001
07	1100110001	1100010001	1100110001	1100010001
08	0100110001	0000001001	0100110001	0000001001
09	1000110001	1000010001	1000110001	1000010001
10	0001000001	0001000001	0001000001	0001000001
11	1010110001	1101010001	1011110001	1101010001
12	1011010001	1111101001	1111100001	1111100101
13	1010101001	1010111001	1011100001	1010100101
14	1101101001	1101111001	1101100000	1101100100
15	1111011011	0000101011	0000100011	0000100111
16	1111011011	1111001011	1111000011	1111000111
17	1001011011	1001001011	1001000011	1001000111
18	1010111011	1010101011	1010100011	1010100111
19	1001111011	1001101011	1001100011	1001100111
20	0010111011	0010101011	0010100011	0010100111
21	0100111011	0100101011	0100100011	0100100111
22	1010011011	1010001011	1010000011	1010000111
23	1110111011	0101001011	1110100011	1110100111
24	1000111011	1000101011	1000100011	1000100111
25	1101100000	1101100000	1101100000	1101100000
26	1001000001	1001000101	1001000001	1001000101
27	1011000001	1011000001	1011000001	1011000001
28	0000011001	0111111001	0000011001	0111111001
29	1110010001	0100010001	1110010001	0100010001
30	1101110001	0101110001	1101110001	0101110001
31	0011011011	0011001011	0011000011	0011000111
32	1101011011	1101001011	1101000011	1101000111
33	0101011011	0101001011	0101000011	0101000111
34	0001011011	0001001011	0001000011	0001000111
35	1110011011	1110001011	1110000011	1110000111
36	0110011011	0110001011	0110000011	0110000111
37	0010011011	0010001011	0010000011	0010000111
38	1100111011	1100101011	1100100011	1100100111
39	1000011011	1000001011	1000000011	1000000111
40	1111010001	1111110001	1111010001	1111110001
41	0111010001	0111110001	0111010001	0111110001
42	0011010001	0011110001	0011010001	0011110001
43	1011011011	1011001011	1011000011	1011100111
44	0111011011	0111001011	0111000011	0111000111
45	0100011011	0100001011	0100000011	0100000111
46	0110111011	0110101011	0110100101	0110100111
47	1100011011	1100001011	1110100101	1100000111
48	0001100011	0001100011	0001100101	0001100111
49	0101111011	0101101011	0101100011	0101100111
50	0011101001	0011111001	0011100001	0011100101
51	0000010001	0000010001	0000010001	0000010001
52	1010000001	1010000001	1010000101	1010000101
53	0110000001	0110000001	0110000101	0110000101
54	1110000001	1110000001	1110000101	1110000101
55	1001000001	1001000001	1001000101	1001000101
56	0101000001	0101000001	0101000101	0101000101
57	1101000001	1101000001	1101000101	1101000101
58	0111000001	0111000001	0111000101	0111000101
59	1111000001	1111000001	1111000101	1111000101
60	0000100001	0000100001	0000100101	0000100101
61	1000100001	1000100001	1000100101	1000100101
62	0100100001	0100100001	0100100101	0100100101
63	1100100001	1100100001	1100100101	1100100101
64	0010000001	0010000001	0010000101	0010000101
65	1010100001	1010100001	1010100101	1010100101
66	0110100001	0110100001	0110100101	0110100101
67	1110100001	1110100001	1110100101	1110100101
68	0001100001	0001100001	0001100101	0001100101
69	1001100001	1001100001	1001100101	0001100101
70	0101100001	0101100001	0101100101	0101100101
71	0011100001	0011100001	0011100101	0011100101
72	1011100001	1011100001	1011100101	1011100101
73	0111100001	0111100001	0111100101	0111100101
74	1111100001	1111100001	1111100101	1111100101
75	0000000001	0000000001	0000000101	0000000101
76	1000000001	1000000001	1000000101	1000000101
77	0100000001	0100000001	0100000101	0100000101
78	1100000001	1100000001	1100000101	1100000101
79	0010000001	0010000001	0010000101	0010000101
80	0000110111	0000110011	0000110111	0000110011
81	1001110111	1001110011	1001110111	1001110011
82	1000100011	0001110011	1000100011	0001110011
83	1110110111	1110110011	1110110111	1110110011
84	1100100011	0110110011	1100100011	0110110011
85	1010110111	1010110011	1010110111	1010110011
86	0100100011	0010110011	0100100011	0010110011
87	1100110111	1100110011	1100110111	1100110011
88	0010100011	0100110011	0010100011	0100110011
89	1000110011	1000110011	1000110111	1000110011

OPTIONS FOR THE KR9602-012 ASCII:

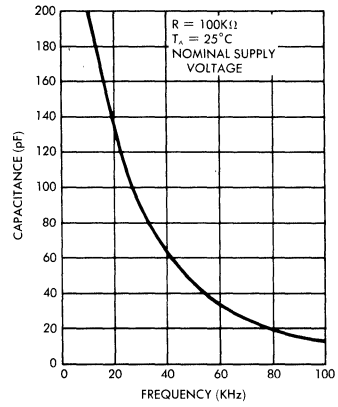
Lockout
Auto Repeat
(Fixed Long Delay of 60,000 Clock Times)
(Fixed Short Delay of 2000 Clock Times)
One Stop Bit
Input Clock Divisor of 32

No Parity
Eight Data Bits
Pull down Resistor to Ground is at the following pins:
— SHIFT
— CONTROL
— CAPS LOCK

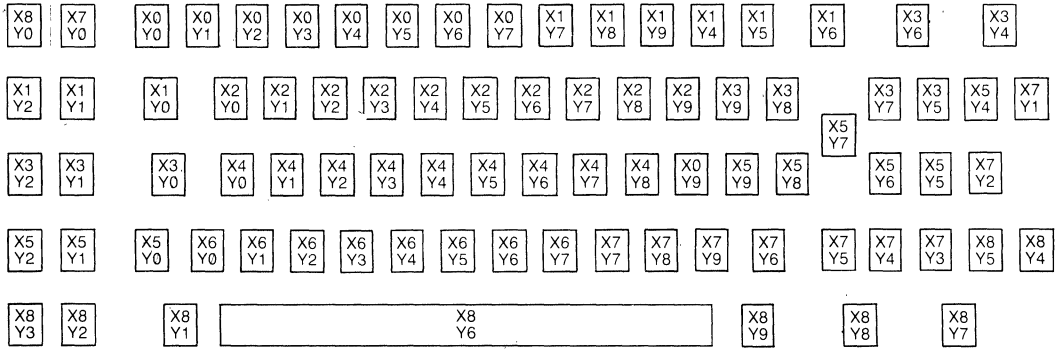
STROBE DELAY vs C2 FOR KR9600/1/2



OSCILLATOR FREQUENCY vs C1 FOR KR9600/KR9601



KEYBOARD LAYOUT FOR KR9601/9602-STD



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Microprocessor Products

Part Number	Description	Size	Process	Speed	Power Supplies	Package	Page
MPU800	Microprocessor	8 Bit	CMOS	2.5 MHz	5V	40 DIP	755-756
MPU800-1	Microprocessor	8 Bit	CMOS	1.0 MHz	5V	40 DIP	755-756
MPU800-4	Microprocessor	8 Bit	CMOS	4.0 MHz	5V	40 DIP	755-756
MPU810A	RAM-I/O-Timer	8 Bit	CMOS	2.5 MHz	5V	40 DIP	757-758
MPU810A-1	RAM-I/O-Timer	8 Bit	CMOS	1.0 MHz	5V	40 DIP	757-758
MPU810A-4	RAM-I/O-Timer	8 Bit	CMOS	4.0 MHz	5V	40 DIP	757-758
MPU830	ROM-I/O	8 Bit	CMOS	2.5 MHz	5V	40 DIP	759-760
MPU830-1	ROM-I/O	8 Bit	CMOS	1.0 MHz	5V	40 DIP	759-760
MPU830-4	ROM-I/O	8 Bit	CMOS	4.0 MHz	5V	40 DIP	759-760
MPU831	I/O	8 Bit	CMOS	2.5 MHz	5V	40 DIP	759-760
MPU831	I/O	8 Bit	CMOS	1.0 MHz	5V	40 DIP	759-760
MPU831-4	I/O	8 Bit	CMOS	4.0 MHz	5V	40 DIP	759-760

STANDARD MICROSYSTEMS CORPORATION

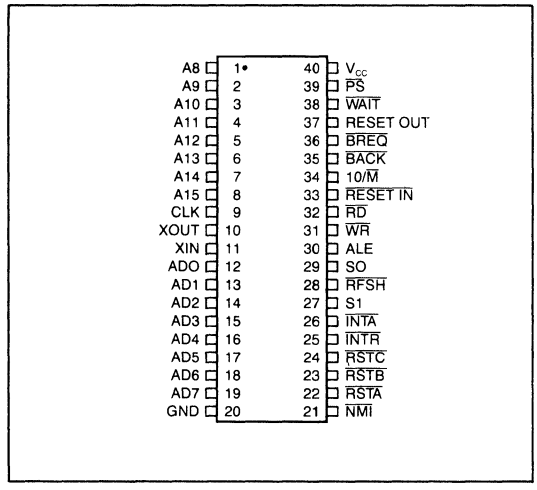
MPU 800
MPU 800-1
MPU 800-4
PRELIMINARY

High-Performance Low-Power Microprocessor

FEATURES

- ☐ Variable Power Supply: 2.4V - 6.0V
- ☐ Fully Compatible Wth Z80® Instruction Set
- ☐ Pin-Compatible With NSC800
- ☐ Powerful Set of 158 Instructions
- ☐ 10 Addressing Modes
- ☐ 22 Internal Registers
- ☐ Low Power: 50 mW at 5 V Vcc
- ☐ Multiplexed Bus Structure
- ☐ On Chip Bus Controller and Clock Generator
- ☐ On-Chip 8 bit Dynamic RAM Refresh Circuitry
- ☐ Three Speed Versions:
  - MPU800-4 4 MHz
  - MPU800 2.5 MHz
  - MPU800-1 1 MHz
- ☐ Capable of addressing 64 k bytes of memory, and 256 I/O devices
- ☐ Five interrupt request lines on-chip
- ☐ Schmitt trigger input on reset
- ☐ Power-Save Feature

PIN CONFIGURATION



SECTION IX

GENERAL DESCRIPTION

The MPU800 is an 8 bit microprocessor that functions as the central processing unit (CPU) in Standard Microsystems MPU800 microcomputer family. The device is fabricated in double-poly CMOS to combine high performance with the low-power of CMOS.

Many system functions are incorporated on the device including: vectored priority interrupts, refresh control, power save, and interrupt acknowledge.

Dedicated peripherals (MPU810 Ram I/O Timer, MPU830 ROM I/O Timer, and (MPU831 I/O Timer) have on-chip logic for direct interface to the MPU800.

Z80 is a registered trademark of Zilog Corporation.

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

MPU 810A
MPU 810A-1
MPU 810A-4

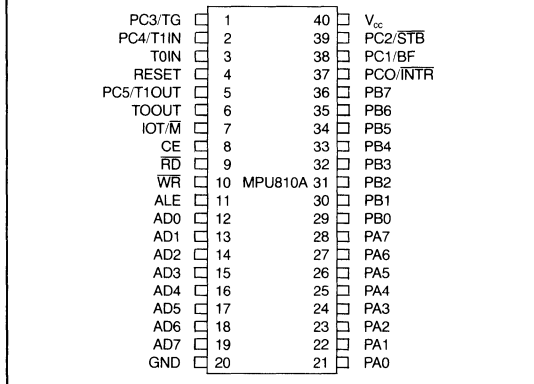
PRELIMINARY

RAM-I/O-Timer

FEATURES

- ☐ Variable Power Supply: 2.4V–6.0V
- ☐ Pin-Compatible With NSC810
- ☐ Three Programmable I/O Ports
- ☐ Two 16 Bit Programmable Counter Timers
- ☐ Very Low Power Consumption
- ☐ Fully Static Operation
- ☐ Single Instruction I/O Bit Operations
- ☐ Timer Operation: DC to 5 MHz
- ☐ Bus Compatible with MPU800 Family
- ☐ Three Speed Versions For Full Compatibility with the MPU800:
  MPU810-4–4 MHz
  MPU810 –2.5 MHz
  MPU810-1–1 MHz

PIN CONFIGURATION



BLOCK DIAGRAM

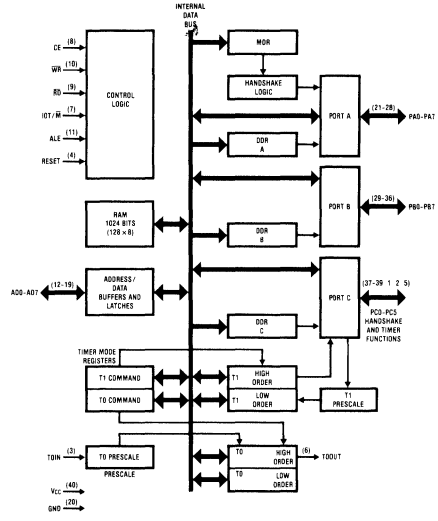


FIGURE 1

GENERAL DESCRIPTION

The MPU810A functions as a memory, input/output peripheral interface, and a timing device. The memory is comprised of 1024 bits of static RAM organized 128 by 8.

The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A.

The timer portion of the device consists of two programmable 16 bit binary down-counters each capable of operation in any one of 6 modes. Timer counts are extendable by one of the available pre-scale values. The MPU810A comes in three speed versions to match the MPU800.

SECTION IX

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 • TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

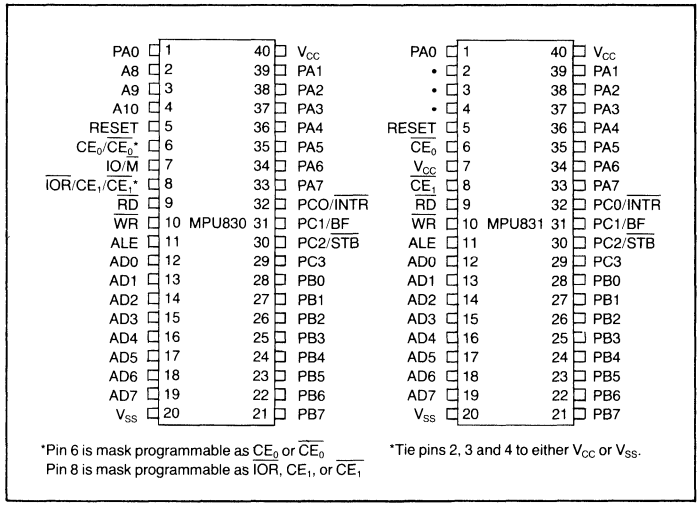
MPU 830
MPU 831
PRELIMINARY

MPU 830 ROM I/O Device
MPU 831 I/O Device

FEATURES

- ☐ Variable Power Supply: 2.4V–6.0V
- ☐ Pin-Compatible With NSC830/NSC831
- ☐ Three Programmable I/O Ports
- ☐ 2K x 8 Read Only Memory (MPU830)
- ☐ Very Low Power Consumption
- ☐ Fully Static Operation
- ☐ Single Instruction I/O Bit Operations
- ☐ Bus Compatible With MPU800 Family
- ☐ Strobed Mode Available on Port A

PIN CONFIGURATION



*Pin 6 is mask programmable as $\overline{CE_0}$ or CE_0
Pin 8 is mask programmable as $\overline{IOR}$, CE_1, or $\overline{CE_1}$

*Tie pins 2, 3 and 4 to either V_{CC} or V_{SS}.

GENERAL DESCRIPTION

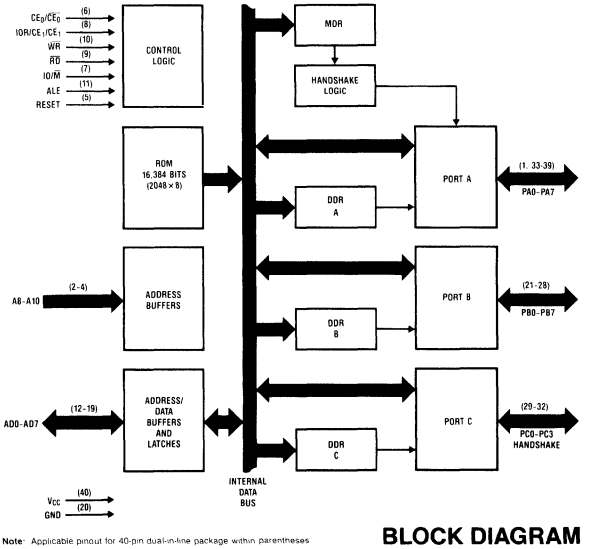
The MPU830 is a combination ROM and I/O peripheral device contained in a standard 40 pin package.

The ROM is comprised of 16,384 bits of Read Only Memory organized as 2048 by 8.

The I/O portion consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A.

The MPU831 is similar to the MPU830 except that is contains no ROM. The MPU831 is useful for prototyping work prior to ordering the MPU830, and when on chip ROM is not required.

Figure 1



Note: Applicable pinout for 40-pin dual-in-line package within parentheses

BLOCK DIAGRAM

SECTION IX

For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 • TWX 510 227 8898

Shift Register

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-80, 81, 133	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls	1 MHz	+5	16 DIP	763-764
SR 5017	Quad 133 Bit	Shift Left/Shift Right, Recirculate Controls	1 MHz	+5	16 DIP	765-766
SR 5018	Quad 81 Bit					

STANDARD MICROSYSTEMS CORPORATION

SR 5015-XXX

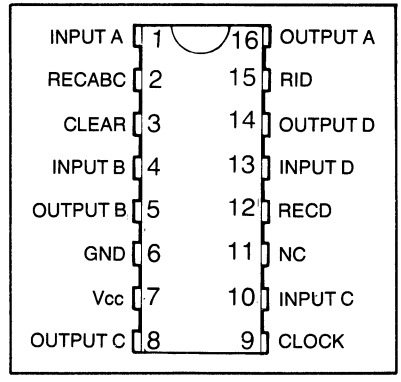
SR 5015-80
SR 5015-81
SR 5015-133

Quad Static Shift Register

FEATURES

- ☐ COPLAMOS® N Channel Silicon Gate Technology
- ☐ Variable Length—Single Mask Programmable—1 to 134 bits
- ☐ Directly TTL-compatible on all inputs, outputs, and clock
- ☐ Clear function
- ☐ Operation guaranteed from DC to 1.0 MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ 16 pin ceramic DIP Package
- ☐ Pin for Pin replacement for AMI S2182, 83, 85

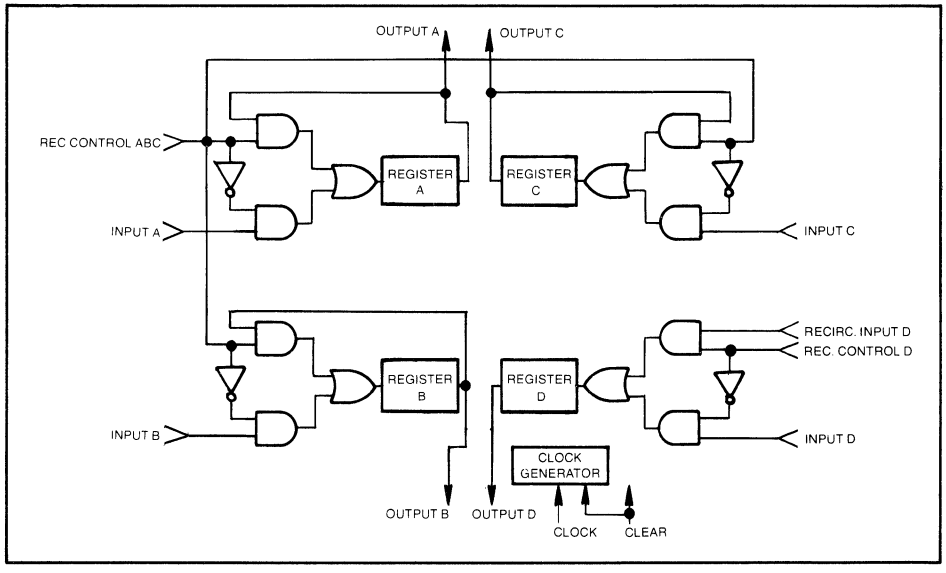
PIN CONFIGURATION



APPLICATIONS

- ☐ Memory Buffering
- ☐ Unique Buffering Lengths
- ☐ Terminals

BLOCK DIAGRAM



SECTION X

For additional information, consult your 1986 catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • TWX: 510-227-8898

STANDARD MICROSYSTEMS CORPORATION

SR 5017
SR 5018

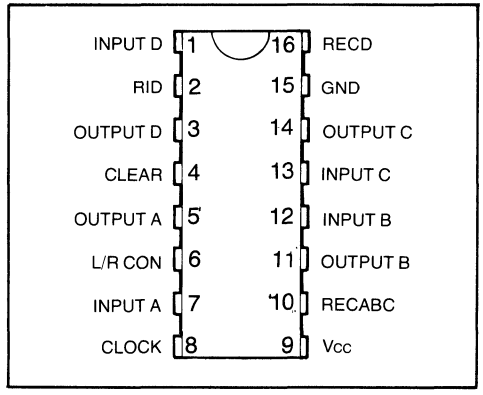
Quad Static Shift Right/Shift Left Shift Register

Last In First Out Buffer
LIFO

FEATURES

- ☐ COMPLAMOS® N-Channel Silicon Gate Technology.
- ☐ Quad 81 bit or Quad 133 bit
- ☐ Directly Compatible with T²L, MOS
- ☐ Operation Guaranteed from DC to 1.0MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ Single phase clock at T²L levels
- ☐ Clear function
- ☐ 16-pin Ceramic DIP Package

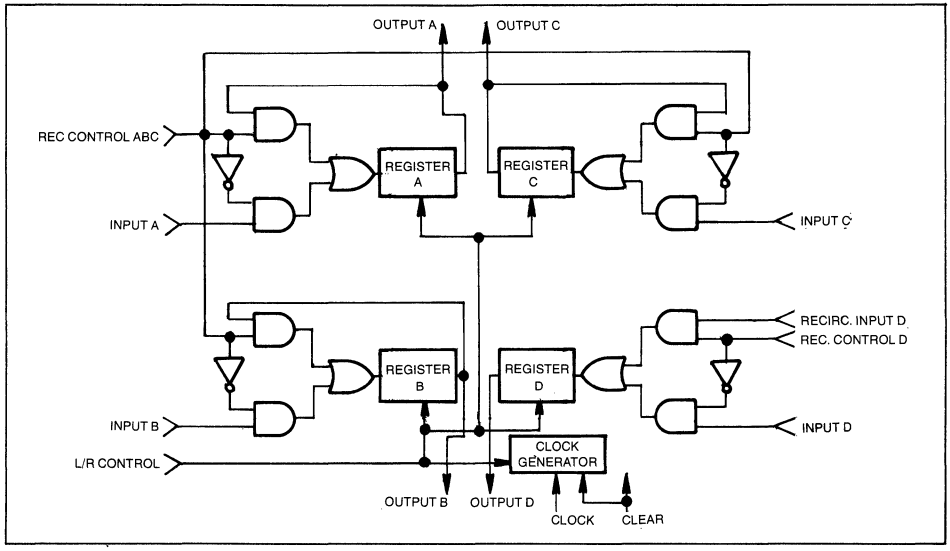
PIN CONFIGURATION



APPLICATIONS

- ☐ Bi-Directional Printer
- ☐ Computers—Push Down Stack—LIFO
- ☐ Buffer data storage—memory buffer
- ☐ Delay lines—delay line processing
- ☐ Digital filtering
- ☐ Telemetry Systems
- ☐ Terminals
- ☐ Peripheral Equipment

BLOCK DIAGRAM



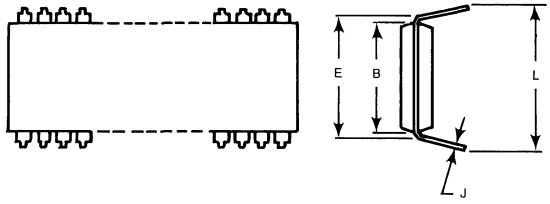
SECTION X

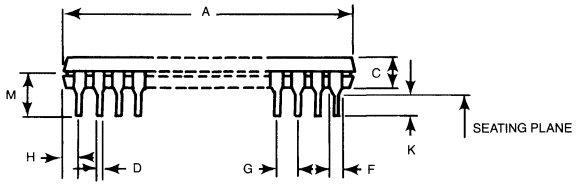
For additional information, consult your 1986 SMC catalog or contact our product marketing department at (516) 273-3100.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 • TWX 510 227 8898

STANDARD MICROSYSTEMS CORPORATION

Plastic Package Outlines





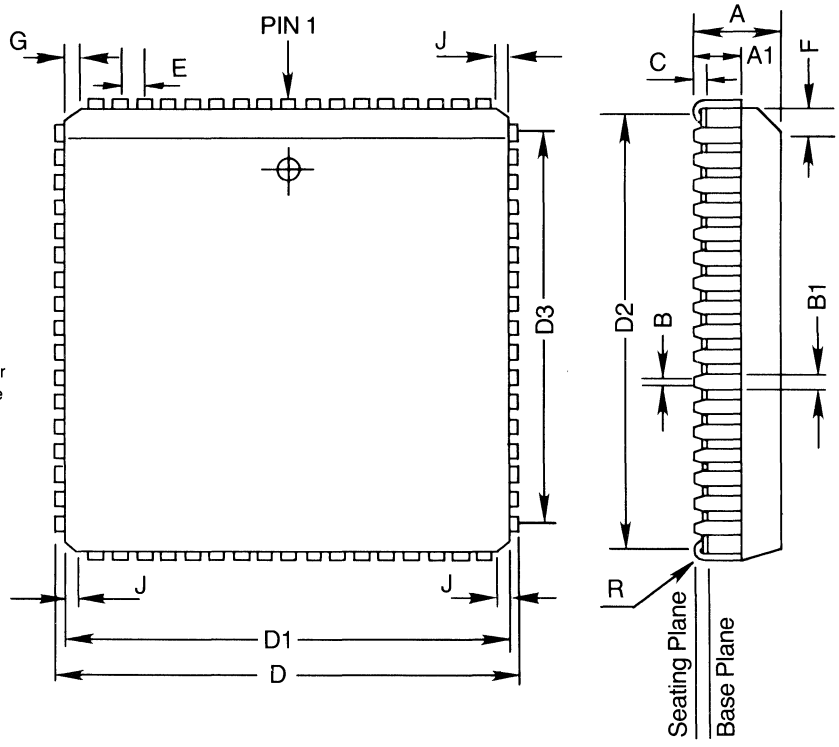
DIM	8 LEAD	14 LEAD	16 LEAD	18 LEAD	20 LEAD	24 LEAD	28 LEAD	40 LEAD	48 LEAD
A	.380-.400	.750-.770	.750-.770	.900-.920	1.025-1.050	1.245-1.265	1.450-1.470	2.050-2.070	2.430-2.460
B	.240-.250	.240-.250	.240-.250	.240-.250	.240-.260	.530-.545	.535-.550	.535-.550	.530-.550
C	.125-.135	.125-.135	.130-.140	.125-.140	.125-.140	.145-.155	.145-.155	.145-.155	.140-.200
D	.016-.021	.016-.021	.016-.021	.016-.021	.016-.021	.016-.021	.016-.021	.016-.021	.015-.021
E	.290-.330	.290-.330	.290-.330	.290-.330	.290-.330	.590-.630	.590-.630	.590-.630	.580-.630
F	.055-.065	.060-.070	.060-.070*	.060-.070	.060-.070	.060-.070	.060-.070	.050-.060	.040-.065
G	.090-.110	.090-.110	.090-.110	.090-.110	.090-.110	.090-.110	.090-.110	.090-.110	.090-.110
H	.040-.050	.075-.085	.025-.035	.040-.060	.065-.075	.065-.085	.070-.090	.070-.090	.065-.090
J	.010-.014	.010-.014	.010-.014	.010-.014	.010-.014	.010-.014	.010-.014	.010-.014	.007-.014
K	.120-.140	.120-.140	.120-.140	.120-.140	.120-.140	.120-.140	.120-.140	.120-.140	.120-.160
L	.315-.370	.315-.365	.315-.365	.315-.365	.315-.365	.610-.670	.610-.670	.610-.670	.610-.675
M	.210-.250	.210-.250	.210-.250	.210-.250	.210-.250	.210-.250	.210-.250	.210-.250	.210-.250

*.045 TYP FOR END LEADS

Plastic Surface Mount Package Outlines
20, 28, 44, 68, 84 J-Lead Carrier

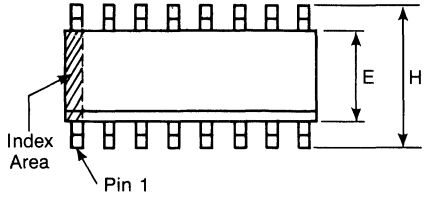
NOTE:

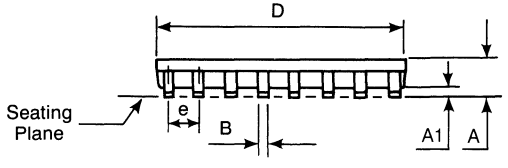
1. All dimensions are in inches.
2. Circle indicating pin 1 can appear on a top surface as shown on the drawing or right above it on a beveled edge.

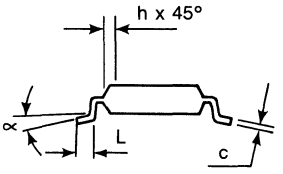


DIM	20L	28L	44L	68L	84L
A	.165-.180	.160-.188	.160-.188	.160-.190	.165-.179
A1	.090-.120	.090-.120	.090-.120	.090-.130	.095-.109
D	.385-.395	.482-.495	.682-.695	.982-.995	1.185-1.195
D1	.350-.356	.450-.456	.650-.656	.950-.956	1.150-1.156
D2	.290-.330	.390-.430	.590-.630	.890-.930	1.090-1.130
D3	.200	.300	.500	.800	1.000
F	.050 TYP	.042-.056	.042-.060	.042-.062	.050 TYP
G	.045 TYP	.042-.048	.042-.048	.042-.048	.045 TYP
J	.000-.020	.000-.020	.000-.028	.00-.028	.010
E	.047-.053	.047-.053	.047-.053	.047-.053	.047-.053
R	.025-.045	.025-.045	.025-.045	.025-.045	.025-.045
B	.013-.021	.013-.021	.013-.021	.013-.021	.013-.021
B1	.026-.032	.026-.032	.026-.032	.026-.032	.027
C	.020-.045	.020-.045	.020-.045	.020-.045	.020-.045

Small Outline Package (SOIC), 16 Lead Plastic



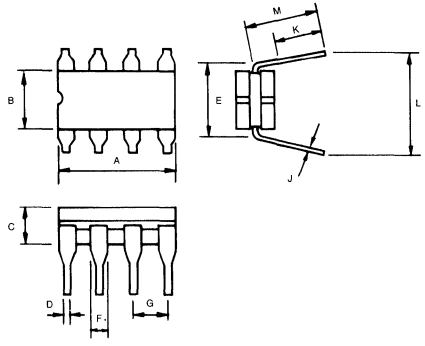




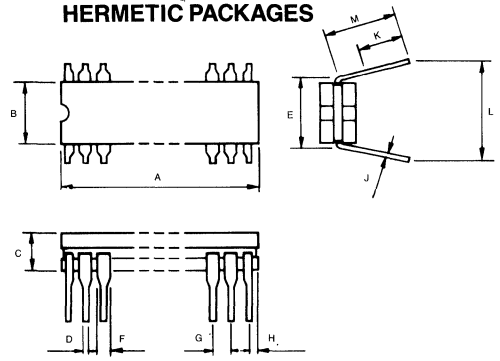
DIM	MIN	MAX
A	.053	.069
A1	.004	.010
B	.014	.019
C	.0075	.010
D	.386	.394
E	.150	.158
e	.050 BSC	
H	.228	.244
h	.010	.020
L	.016	.050
∝	0°	8°

Cerdip Hermetic Package Outlines

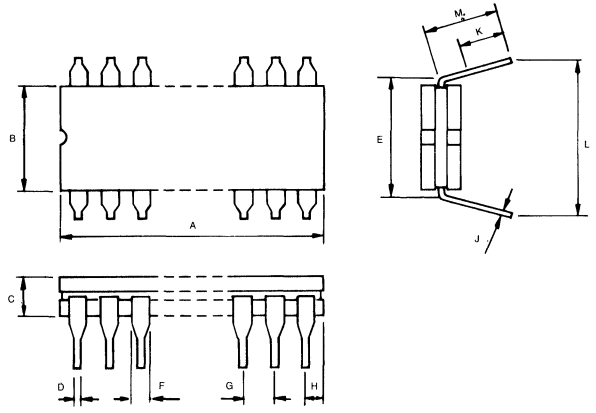
8 PIN CERDIP HERMETIC PACKAGES



14, 16, 18, 20 PIN CERDIP HERMETIC PACKAGES



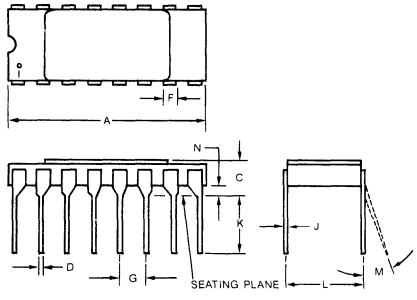
24, 28, 40 PIN CERDIP HERMETIC PACKAGES



DIM	8 LEAD	14 LEAD	16 LEAD	18 LEAD	20 LEAD	24 LEAD	28 LEAD	40 LEAD
A	.400 MAX	.785 MAX	.810 MAX	.915 MAX	.970 MAX	1.280 MAX	1.460 MAX	2.070 MAX
B	.245-.295	.244-.295	.244-.295	.265-.295	.265-.295	.510-.595	.510-.595	.510-.595
C	.160 MAX	.160 MAX	.180 MAX	.180 MAX	.180 MAX	.180 MAX	.180 MAX	.180 MAX
D	.016-.020	.016-.020	.016-.020	.016-.020	.016-.020	.016-.020	.016-.020	.016-.020
E	.290-.320	.290-.320	.290-.320	.310-.330	.310-.330	.590-.620	.590-.620	.590-.620
F	.050-.070	.050-.070	.050-.070	.050-.070	.050-.070	.050-.070	.050- .070	.050-.070
G	.100 ± .010	.100 ± .010	.100 ± .010	.100 ± .010	.100 ± .010	.100 ± .010	.100 ± .010	.100-.010
H	—	.065 TYP	.020 TYP	.040 TYP	.020 TYP	.045 TYP	.045 TYP	.045 TYP
J	.008-.012	.008-.012	.008-.012	.008-.012	.008-.012	.008-.012	.008-.012	.008-.012
L	.400 MAX	.400 MAX	.400 MAX	.400 MAX	.400 MAX	.700 MAX	.700 MAX	.700 MAX
M	.240-.300	.240-.300	.240-.300	.240-.300	.240-.300	.240-.300	.240-.300	.240-.300
K	.125 MIN	.125 MIN	.125 MIN	.125 MIN	.125 MIN	.125 MIN	.125 MIN	.125 MIN

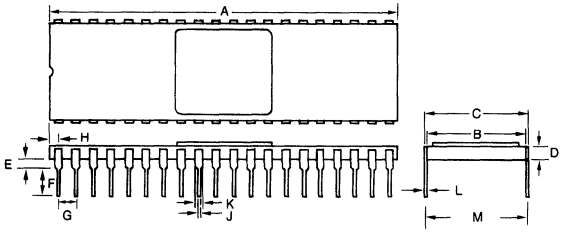
Ceramic Package Outlines

14, 16, 18, 20 PIN HERMETIC PACKAGE



	14 LEAD		16 LEAD		18 LEAD		20 LEAD	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.670	.760	.790	.810	.885	.915	.965	.995
C		.175		.175		.175		.175
D	.015	.021	.015	.021	.015	.021	.015	.021
F	.048	.060	.048	.060	.048	.060	.048	.060
G	.090	.110	.090	.110	.090	.110	.090	.110
J	.008	.012	.008	.012	.008	.012	.008	.012
K	.130	.170	.130	.170	.130	.170	.130	.170
L	.295	.325	.295	.325	.295	.325	.295	.325
M		10°		10°		10°		10°
N	.025	.060	.025	.060	.025	.060	.025	.060

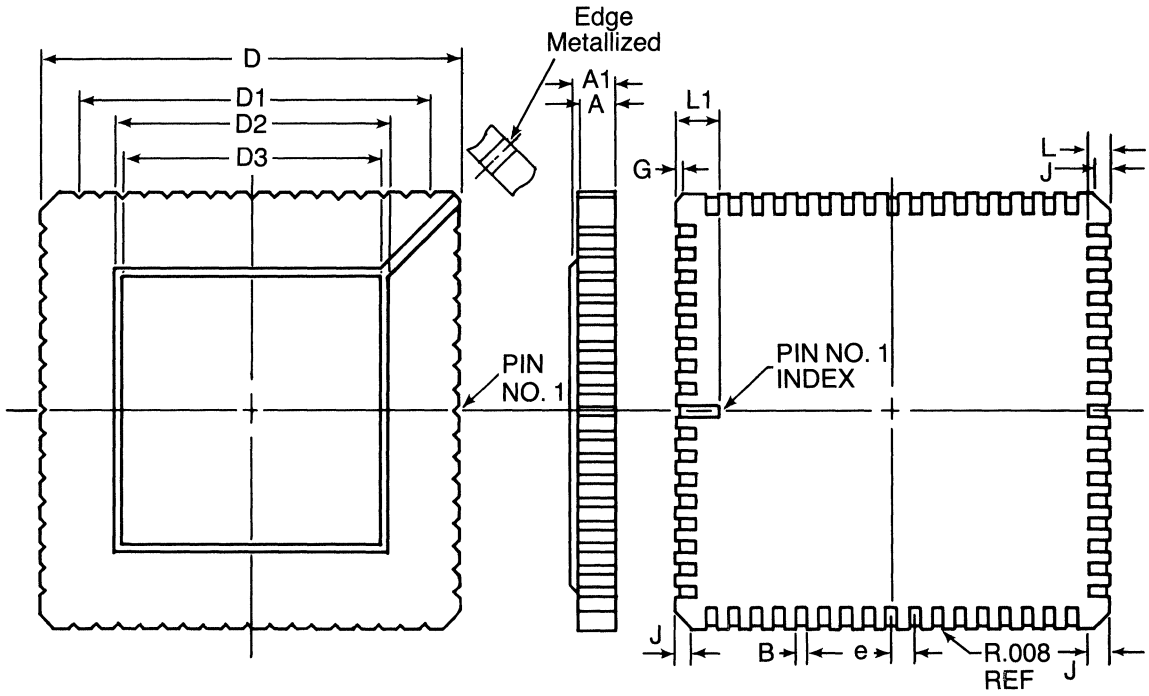
24, 28, 40, 48 PIN HERMETIC DIP



	24 LEAD		28 LEAD		40 LEAD		48 LEAD	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	1.180	1.220	1.380	1.430	1.980	2.030	2.376	2.424
B	.575	.610	.580	.610	.580	.610	.567	.600
C	.595	.625	.595	.625	.595	.625	.590	.620
D	.065	.120	.065	.120	.065	.120	.077	.093
E	.020	.070	.020	.070	.020	.070	.025	.060
F	.125	.175	.125	.175	.125	.175	.130	.170
G	0.100 TP		0.100 TP		0.100 TP		0.100 TP	
H	0.05 TP		0.05 TP		0.05 TP		0.500 TP	
J	0.018 TP		0.018 TP		0.018 TP		0. 018 TP	
K	0.040 TP		0.040 TP		0.040 TP		0.040 TP	
L	0.010 NOM		0.010 NOM		0.010 NOM		0.010 NOM	
M	0.600 TP		0.600 TP		0.600 TP		0.600 TP	

ALL UNITS INCHES UNLESS OTHERWISE SPECIFIED

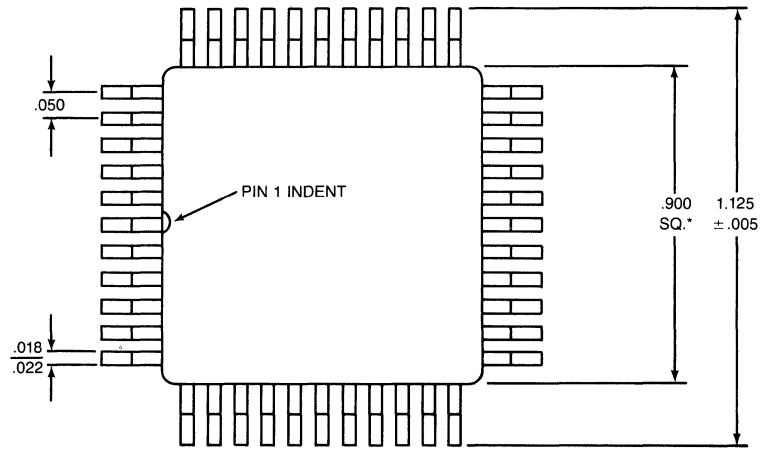
Ceramic Leadless Chip Carrier Outlines



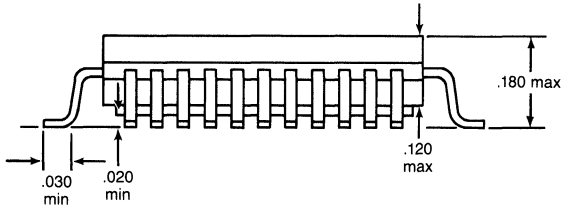
DIM	68 LEAD	44 LEAD	84 LEAD
A	.072-.088	.062-.078	.072-.088
A1	.081-.099	.071-.089	.081-.099
B	.025 TYP	.025 TYP	.025 TYP
D	.940-.965	.640-.660	1.135-1.165
D1	.800	.500	1.000
D2	.455-.820	.355-.598	.530-1.020
D3	.450-.820	.350-.590	.500-.990
e	.050 BSC	.050 BSC	.050 BSC
G	.020 x 45°	.020 x 45°	.020 x 45°
J	.040 x 45°	.040 x 45°	.040 x 45°
L	.045-.055	.045-.055	.042 x .048
L1	.075-.095	.075-.095	.075-.095

Cerquad Package Outline

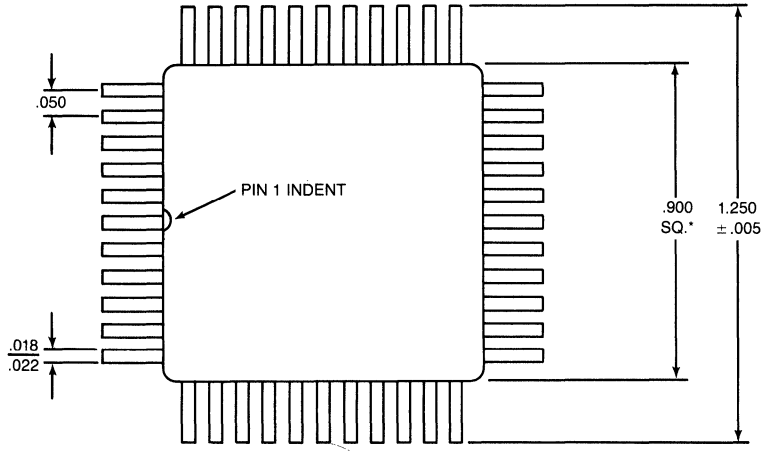
68 LEADED CERQUAD GULLWING (GA)



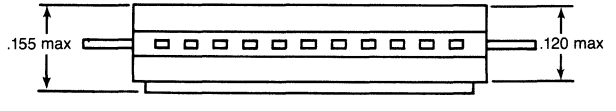
*DEFINES MINIMUM CLEAR LEADFRAME ZONE –zone consists of package body, including ceramic and glass.



68 LEADED CERQUAD FLAT LEAD (FA)



*DEFINES MINIMUM CLEAR LEADFRAME ZONE –zone consists of package body, including ceramic and glass.



**PC Board Socket available from Cannon ITT
- p/n CA111484
10550 Talbert Ave., Fountain Valley, CA 92728-8048

STANDARD MICROSYSTEMS CORPORATION

SALES REPRESENTATIVES

REGIONAL OFFICES

NORTHEAST SALES/ APPLICATIONS OFFICE
Standard Microsystems Corporation
1 Tara Blvd. Suite 202
Nashua, New Hampshire 03062
PHONE: 603-891-0040
FAX: 603-891-2120

NORTH CENTRAL SALES OFFICE
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive, Ste. 106
Kettering, Ohio 45429
PHONE: 513-293-5393
TELEX: 82882274
FAX: 513-293-7557

SOUTH CENTRAL APPLICATIONS OFFICE
Standard Microsystems Corporation
250 South Stemmons, Ste. 334
Lewisville, Texas 75067
PHONE: 214-436-4009
TWX: 62906119 (Easylink)
FAX: 214-221-9364

WESTERN SALES OFFICE
Standard Microsystems
4010 Moorpark, Ste. 105
San Jose, California 95117
PHONE: 408-249-5000
FAX: 408-247-5122

WESTERN APPLICATIONS OFFICE
4900 Eclipse Avenue
Mira Loma, California 91752
PHONE: 714-681-4461
FAX: 714-681-5297

ALABAMA
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, Alabama 35805-0306
PHONE: 205-536-3044
FAX: 205-533-5097

ALASKA
Quest Marketing, Inc.
15921 N.E. 8th Street, Ste. 207
Bellevue, Washington 98008
PHONE: 206-747-9424
FAX: 206-643-3488

ARIZONA
Southwest Technical Sales
4314 E. Tonto St.
Phoenix, Arizona 85044
PHONE: 602-893-1209
TELEX: 910-950-0195
FAX: 602-893-1312

ARKANSAS
Southern States Marketing
1143 Rockingham, Suite 106
Richardson, Texas 75080
PHONE: 214-238-7500
TWX: 910-867-4754
FAX: 214-231-7662

CALIFORNIA/North
Costar, Inc.
19220 Stevens Creek Blvd.
Cupertino, California 95014
PHONE: 408-446-9339
TELEX: 910-338-0206
FAX: 408-446-4885

CALIFORNIA/South
Varigon, Inc.
137 Eucalyptus Drive
El Segundo, California 90245
PHONE: 213-634-2116

Varigon, Inc.
23441 S. Pointe Dr.
Suite 90
Laguna Hills, CA 92653
PHONE: 714-855-0233
TELEX: 910-997-0225
FAX: 714-458-0854

Cerco
5230 Carroll Canyon Road
Suite 214
San Diego, California 92121
PHONE: 619-450-1755
TELEX: 910-335-1220
FAX: 619-450-3681

COLORADO
Elcom, Inc.
2015 South Dayton Street
Denver, Colorado 80231
PHONE: 303-337-2300
TELEX: 62927893 (Easylink)
FAX: 303-745-0462

CONNECTICUT
Orion Group
27 Meriden Avenue
Southington, Connecticut 06489
PHONE: 203-621-8371
TWX: 510-601-1381
FAX: 203-628-0494

DELAWARE
Tritek Sales, Inc.
21 E. Euclid Avenue
Haddonfield, New Jersey 08033
PHONE: 609-429-1551
TELEX: 710-896-0881
FAX: 609-429-4915

FLORIDA
MEC
600 W. Hillsboro Blvd., Ste. 300
Deerfield Beach, FL 33441
PHONE: 305-426-8944
TELEX: 510-100-4470
FAX: 305-427-9911

MEC
989 Woodgate Drive
Palm Harbor, FL 33563
PHONE: 813-784-8561
FAX: 305-427-9911

MEC
375 S. North Lake Blvd.
Altamonte Springs, FL 32701
PHONE: 305-332-7158

GEORGIA
Electronic Marketing Associates
6695 Peachtree Industrial Blvd.
Suite 109
Atlanta, Georgia 30360
PHONE: 404-448-1215
FAX: 404-446-9363

IDAHO
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, Washington 98008
PHONE: 206-747-9424
FAX: 206-643-3488

ILLINOIS/North
Sumer, Inc.
1675 Hicks Road
Rolling Meadows, Illinois 60008
PHONE: 312-991-8500
TELEX: 62958372 (Easylink)
FAX: 312-991-0474

ILLINOIS/South
S.W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, Kansas 66072
PHONE: 913-898-6552
FAX: 913-898-6081

INDIANA
Wilson Technical Sales, Inc.
P.O Box 688510
Indianapolis, Indiana 46268
PHONE: 317-872-2513
TELEX: 910-997-8120
FAX: 317-872-0664

IOWA
S.W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, Kansas 66072
PHONE: 913-898-6552
FAX: 913-898-6081

KANSAS
S.W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, Kansas 66072
PHONE: 913-898-6552
FAX: 913-898-6081

KENTUCKY
Wilson Technical Sales, Inc.
P.O. Box 688510
Indianapolis, Indiana 46268
PHONE: 317-872-2513
TELEX: 910-997-8120
FAX: 317-872-0664

LOUISIANA
Southern States Marketing
1143 Rockingham, Suite 106
Richardson, Texas 75080
PHONE: 214-238-7500
TWX: 910-867-4754
FAX: 214-231-7662

MAINE
The Orion Group
607 North Ave.
Wakefield, Massachusetts 01880
PHONE: 617-245-5220
TWX: 510-601-0667

MARYLAND
Robert Electronic Sales
5525 Twin Knolls Rd., Ste. 325
Columbia, Maryland 21045
PHONE: 301-995-1900
FAX: 301-964-3364

MASSACHUSETTS
The Orion Group
607 North Ave.
Wakefield, Massachusetts 01880
PHONE: 617-245-5220
TWX: 510-601-0667

Digital Equipment Corp. Only
Mill-Bern Associates, Inc.
2 Mack Road
Woburn, Massachusetts 01801
PHONE: 617-932-3311
FAX: 617-932-0511

MICHIGAN
A.P. Associates
PO. Box 777
Brighton, Michigan 48116
PHONE: 313-229-6550
TELEX: 287310
FAX: 313-229-9356

MINNESOTA
Comstrand, Inc.
2852 Anthony Lane South
Minneapolis, Minnesota 55418
PHONE: 612-788-9234
TELEX: 910-576-0924
FAX: 612-788-7218

MISSISSIPPI
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, Alabama 35805-0306
PHONE: 205-536-3044
FAX: 205-533-5097

MISSOURI
S.W. Wollard
Rural Route 1
Post Office Box 66A
Parker, Kansas 66072
PHONE: 913-898-6552
FAX: 913-898-6081

MONTANA
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, Washington 98008
PHONE: 206-747-9424
FAX: 206-643-3488

NEBRASKA
S.W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, Kansas 66072
PHONE: 913-898-6552
FAX: 913-898-6081

NEVADA/North
Costar, Inc.
19220 Stevens Creek Blvd.
Cupertino, California 95014
PHONE: 408-448-9339
TELEX: 910-338-0206
FAX: 408-446-4885

NEVADA/South
Southwest Technical Sales
4314 E. Tonto St.
Phoenix, Arizona 85044
PHONE: 602-893-1209
TELEX: 910-950-0195
FAX: 602-893-1312

NEW HAMPSHIRE
The Orion Group
607 North Ave.
Wakefield, Massachusetts 01880
PHONE: 617-245-5220
TWX: 510-601-0667

NEW JERSEY/Northern
Technical Marketing Group
705 Cedar Lane
Teaneck, N.J. 07666
PHONE: 201-692-0200
TWX: 710-990-5086
FAX: 201-692-8367

NEW JERSEY/Southern
Tritek Sales, Inc.
21 E. Euclid Avenue
Haddonfield, New Jersey 08033
PHONE: 609-429-1551
TELEX: 710-896-0881
FAX: 609-429-4915

NEW MEXICO
Southwest Technical Sales
4314 E. Tonto St.
Phoenix, Arizona 85044
PHONE: 602-893-1209
TELEX: 910-950-0195
FAX: 602-893-1312

NEW YORK
Technical Marketing Group
20 Broad Hollow Road
Melville, N.Y. 11747
PHONE: 516-351-8833
TWX: 910-997-3030
FAX: 516-351-8667

T-Squared Elec. Co., Inc.
7353 Victor Pittsford Rd.
Victor, New York 14564
PHONE: 716-924-9101
FAX: 716-924-4946

T-Squared Elec. Co., Inc.
6443 Ridings Road
Syracuse, New York 13206
PHONE: 315-463-8592

NORTH CAROLINA
Electronic Marketing Associates
9225 Honeycutt Creek Road
Raleigh, North Carolina 27609
PHONE: 919-847-8800
TELEX: 510-928-0594
FAX: 919-848-1787

NORTH DAKOTA
Comstrand, Inc.
2852 Anthony Lane South
Minneapolis, Minnesota 55418
PHONE: 612-788-9234
TELEX: 910-576-0924
FAX: 612-788-7218

OHIO
Thompson & Associates
23215 Commerce Dr., Suite 202
Beachwood, Ohio 44122
PHONE: 216-831-6277
TELEX: 333804
FAX: 216-831-2553

Thompson & Associates
309 Regency Ridge
Dayton, Ohio 45459
PHONE: 513-435-7733
TELEX: 810-459-1767
FAX: 513-435-1898

OKLAHOMA
Southern States Marketing
1143 Rockingham, Suite 106
Richardson, Texas 75080
PHONE: 214-238-7500
TELEX: 910-867-4754
FAX: 214-231-7662

OREGON
Quest Marketing, Inc.
6700 S.W. 105th, Ste. 311D
Beaverton, Oregon 97005
PHONE: 503-641-7377
FAX: 503-646-9536

PENNSYLVANIA/Eastern
Tritek Sales, Inc.
21 E. Euclid Avenue
Haddonfield, New Jersey 08033
PHONE: 609-429-1551
TELEX: 710-896-0881
FAX: 609-429-4915

PENNSYLVANIA/Western
Thompson & Associates
309 Regency Ridge
Dayton, Ohio 45459
PHONE: 513-435-7733
TELEX: 810-459-1767

RHODE ISLAND
The Orion Group
607 North Ave.
Wakefield, Massachusetts 01880
PHONE: 617-245-5220
TWX: 510-601-0667

SOUTH CAROLINA
Electronic Marketing Associates
210 West Stone Avenue
Greenville, South
Carolina 29609-5499
PHONE: 803-233-4637/4638
TELEX: 810-281-2225
FAX: 803-242-3089

SOUTH DAKOTA
Comstrand, Inc.
2852 Anthony Lane South
Minneapolis, Minnesota 55418
PHONE: 612-788-9234
TELEX: 910-576-0924
FAX: 612-788-7218

TENNESSEE
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, Alabama 35805-0306
PHONE: 205-536-3044
FAX: 205-533-5097

TEXAS
Southern States Marketing
1143 Rockingham, Suite 106
Richardson, Texas 75080
PHONE: 214-238-7500
TWX: 910-867-4754
FAX: 214-231-7662

Southern States Marketing
400 E. Anderson Lane, Suite 111
Austin, Texas 78752
PHONE: 512-452-9459
TWX: 910-874-2006

UTAH
Elcom, Inc.
2520 South State Street
Suite 116
Salt Lake City, Utah 84115
PHONE: 801-486-4233
TELEX: 62893625 (Easylink)

VERMONT
The Orion Group
607 North Ave.
Wakefield, Massachusetts 01880
PHONE: 617-245-5220
TWX: 510-601-0667

VIRGINIA
Robert Electronic Sales
1901 West Huguenot Road,
Suite 201
Richmond, Virginia 23235
PHONE: 804-276-3979
FAX: 804-794-6090

WASHINGTON
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, Washington 98008
PHONE: 206-747-9424
FAX: 206-643-3488

WASHINGTON D.C.
Robert Electronic Sales
5525 Twin Knolls Rd. Suite 331
Columbia, Maryland 21045
PHONE: 301-995-1900

WEST VIRGINIA
Thompson Associates
23715 Merchantile Road
Beachwood, Ohio 44122
PHONE: 216-831-6277
TELEX: 810-427-9453

WISCONSIN/West
Comstrand, Inc.
2852 Anthony Lane South
Minneapolis, Minnesota 55418
PHONE: 612-788-9234
TELEX: 910-576-0924
FAX: 612-788-7218

WISCONSIN/East
Sumer, Inc.
350 Bishops Way
Brookfield, Wisconsin 53005
PHONE: 414-784-6641
FAX: 414-785-9628

WYOMING
Elcom, Inc.
2015 South Dayton Street
Denver, Colorado 80231
PHONE: 303-337-2300
TELEX: 62927893 (Easylink)
FAX: 303-745-0462

DISTRIBUTORS

ALABAMA
Hall-Mark Electronics Corp.
4900 Bradford Drive
Huntsville, Alabama 35807
PHONE: 205-837-8700

ARIZONA
Cetec Electronics
3617 N. 35th Avenue
Phoenix, Arizona 85017
PHONE: 602-272-7951

Hall-Mark Electronics Corp.
4040 East Raymond
Phoenix, Arizona 85040
PHONE: 602-437-1200

CALIFORNIA
Cetec Electronics
1692 Browning
Irvine, California 92714
PHONE: 714-250-4141

Cetec Electronics
3940 Ruffin Road
San Diego, California 92123
PHONE: 619-278-5020

Cetec Electronics
2300 Owen Street
Santa Clara, California 95051
PHONE: 408-434-1114
FAX: 408-433-0822

Diplomat Electronics, Inc.
6921 San Fernando Road
Glendale, California 91201
PHONE: 818-845-8700
FAX: 818-848-6420

Hall-Mark Electronics Corp.
6341 Auburn Blvd.
Suite D
Citrus Heights, California 95610
PHONE: 916-722-8600

Hall-Mark Electronics Corp.
8130 Remmet Avenue
Canoga Park, California 93104
PHONE: 818-716-7300
FAX: 818-704-4860

Hall-Mark Electronics Corp.
3878 Ruffin Road, Ste. 108
San Diego, California 92123
PHONE: 619-268-1201

Hall-Mark Electronics Corp.
1110 Ringwood Court
San Jose, California 95131
PHONE: 408-432-0900
FAX: 403-433-0745

Hall-Mark Electronics Corp.
19220 S. Normandie Avenue
Torrance, California 90502
PHONE: 213-217-8450

DISTRIBUTORS (con't)

Hall-Mark Electronics Corp.
14831 Franklin Avenue
Tustin, California 92680
PHONE: 714-869-4700

Western Microtechnology, Inc.
10040 Bubb Road
Cupertino, California 95014
PHONE: 408-725-1660
FAX: 408-255-6491

COLORADO
Hall-Mark Electronics Corp.
6950 Tucson Way So.
Suite 206
Englewood, Colorado 80112
PHONE: 303-790-1662
FAX: 303-790-4991

CONNECTICUT
Hall-Mark Electronics Corp.
Barnes Industrial Park W.
33 Village Lane, P.O. Box 5024
Wallingford, Connecticut 06492
PHONE: 203-269-0100

Milgray Electronics, Inc.
378 Boston Post Road
Orange, Connecticut 06477
PHONE: 203-785-0711

FLORIDA
Hall-Mark Electronics Corp.
15301 Roosevelt Blvd.
Suite 303
Clearwater, Florida 33520
PHONE: 813-530-4543
FAX: 813-535-3865

Hall-Mark Electronics Corp.
7648 Southland Blvd.
Suite 100
Orlando, Florida 32809
PHONE: 305-855-4020

Hall-Mark Electronics Corp.
3161 S.W. 15th St.
Pompano Beach, Florida 33069
PHONE: 305-971-9280

Milgray Electronics, Inc.
1850 Lee Road, Suite 104
Winter Park, Florida 32789
PHONE: 305-647-5747
800-327-5262

GEORGIA
Hall-Mark Electronics Corp.
6410 Atlantic Blvd.
Suite 115
Norcross, Georgia 30071
PHONE: 404-447-8000

Milgray Electronics, Inc.
17 Dunwoody Park, Suite 102
Atlanta, Georgia 30338
PHONE: 404-393-9666
800-241-5523

IDAHO
Radar Electric Co., Inc.
5821 Franklin Road
Boise, Idaho 83709
PHONE: 208-336-2227
FAX: 208-336-2322

IOWA
Advent Electronics
682 58th Avenue S.W.
Cedar Rapids, Iowa 52404
PHONE: 319-363-0221

ILLINOIS
Hall-Mark Electronics Corp.
210 Mittel Drive
Wood Dale, Illinois 60191
PHONE: 312-860-3800

Mar-Con
4836 Main Street
Skokie, Illinois 60078
PHONE: 312-675-6450

Milgray Electronics, Inc.
765 Route 83, Ste. 123
Bensenville, Illinois 60106
PHONE: 312-350-0490

INDIANA
Advent Electronics
8446 Moller Road
Indianapolis, Indiana 46268
PHONE: 317-872-4910

Hall-Mark Electronics Corp.
4275 W. 96th Street
Indianapolis, Indiana 46268
PHONE: 317-872-8875

KANSAS
Hall-Mark Electronics Corp.
10815 Lakeview Drive
Lenexe, Kansas 66215
PHONE: 913-888-4747

Milgray Electronics, Inc.
8901 West 63rd Street
Overland Park, Kansas 66202
PHONE: 913-236-8800

MARYLAND
Hall-Mark Electronics Corp.
10240 Old Columbia Road
Columbia, Maryland 21046
PHONE: 301-988-9800

Milgray Electronics, Inc.
9801 Broken Land Parkway
Columbia, Maryland 21046
PHONE: 301-621-6169
800-638-6656

MASSACHUSETTS
Nu Horizons
151 Andover St.
Danvers, MA 01930
PHONE: 617-777-8800

Hall-Mark Electronics Corp.
6 Cook Street
Pinehurst Park
Billerica, Massachusetts 01801
PHONE: 617-935-9777

Milgray Electronics, Inc.
Ballardvale Street
Wilmington, MA 01887
PHONE: 617-657-5900

Jaco
222 Andover Street
Wilmington, Massachusetts 01887
PHONE: 617-273-1860
FAX: 617-273-1942

MICHIGAN
Advent Electronics
24713 Crestview Court
Farmington Hills, Michigan 48018
PHONE: 313-477-1650

MINNESOTA
Hall-Mark Electronics Corp.
10300 Valley View Rd.
Suite 101
Eden Prairie, Minnesota 55344
PHONE: 612-941-2600

MISSOURI
Hall-Mark Electronics Corp.
13750 Shoreline Drive
Earth City, Missouri 63045
PHONE: 314-291-5350

NEW JERSEY
Hall-Mark Electronics Corp.
107 Fairfield Road
Suite 1B
Fairfield, New Jersey 07006
PHONE: 201-575-4415

Hall-Mark Electronics Corp.
11000 Midlantic Drive
Mt. Laurel, New Jersey 08054
PHONE: 609-235-1900
FAX: 609-235-3381

Milgray Electronics, Inc.
3002 Greentree
Executive Campus
Marlton, New Jersey 08053
PHONE: 609-983-5010
800-257-7808/7111

Nu Horizons
258 Route 46
Fairfield, N.J. 07006
PHONE: 201-882-8300

NEW YORK
ADD Electronics
7 Adler Drive
East Syracuse, New York 13057
PHONE: 315-437-0300

Current Components
215 Marcus Boulevard
Hauppauge, New York 11788
PHONE: 516-273-2600
FAX: 516-273-2801

Hall-Mark Electronics Corp.
101 Comac Street
Ronkonkoma, New York 11779
PHONE: 516-737-0600

Milgray Electronics, Inc.
77 Schmitt Blvd.
Farmingdale, New York 11735
PHONE: 516-420-9800
FAX: 516-752-9870

Milgray Electronics, Inc.
57 Monroe Avenue
Pittsford, New York 14534
PHONE: 716-385-9330

Nu Horizons
6000 New Horizons Blvd.
Amityville, N.Y. 11701
PHONE: 516-226-6000

NORTH CAROLINA
Hall-Mark Electronics Corp.
5237 North Blvd. Suite D
Raleigh, North Carolina 27604
PHONE: 919-872-0712

OHIO
Applied Data Management
435 Dayton Street
Cincinnati, Ohio 45214
PHONE: 513-579-8108

Hall-Mark Electronics Corp.
400 E. Wilson Bridge Road
Suite S
Worthington, Ohio 43085
PHONE: 614-888-3313

Hall-Mark Electronics Corp.
5821 Harper Road
Solon, Ohio 44139
PHONE: 216-349-4632

Milgray Electronics, Inc.
6155 Rockside Road
Cleveland, Ohio 44131
PHONE: 216-477-1520
800-321-0006

OKLAHOMA
Quality Components, Inc.
3158 S. 108th East Ave.
Tulsa, Oklahoma 74146
PHONE: 918-664-8812

OREGON
Western Micro
1800 N.W. 169th Place #3300
Beaverton, Oregon 97006
PHONE: 503-629-2082

Radar Electric Co., Inc.
704 S.E. Washington
Portland, Oregon 97214
PHONE: 503-232-3404
FAX: 503-235-0428

PENNSYLVANIA
QED Electronics, Inc.
805 N. Bethlehem Pike
Box 847
Spring House, PA 19477
PHONE: 215-643-9200

TEXAS
Hall-Mark Electronics Corp.
12211 Technology Blvd.
Austin, Texas 78727
PHONE: 512-258-8848

Hall-Mark Electronics Corp.
10375 Brockwood Road
Dallas, Texas 75238
PHONE: 214-553-4300

Hall-Mark Electronics Corp.
8000 Westglen
Houston, Texas 77063
PHONE: 713-781-6100
FAX: 713-953-8420

Quality Components, Inc.
4257 Kellway Circle
P.O. Box 819
Addison, Texas 75001
PHONE: 214-733-4300

Quality Components, Inc.
2120-M Breaker Lane
Austin, Texas 78758
PHONE: 512-835-0220

Quality Components, Inc.
1005 Industrial Blvd.
Sugarland, Texas 77478
PHONE: 713-491-2255
FAX: 713-240-6988

UTAH
Hall-Mark Electronics Corp.
2265 So. 1300 West
West Valley City, Utah 84119
PHONE: 801-972-1008
FAX: 801-972-3446

Milgray Electronics
4190 S. Highland Dr.
Suite 102
Salt Lake City, Utah 84124
PHONE: 801-272-4999

WASHINGTON
Western Microtechnology, Inc.
14636 N.E. 95th Street
Redmond, Washington 98052
PHONE: 206-881-6737
FAX: 206-882-2996

Radar Electric Co., Inc.
East 303 Pacific
Spokane, Washington 99202
PHONE: 509-747-3053
FAX: 509-456-8069

Radar Electric Co., Inc.
292 Torbett Street
Richland, Washington 99352
PHONE: 509-943-8336
FAX: 509-943-6790

Radar Electric Co., Inc.
168 Western Ave. West
Seattle, Washington 98119
PHONE: 206-282-2511
FAX: 206-282-1598

WISCONSIN
Hall-Mark Electronics Corp.
16255 W. Lincoln Avenue
New Berlin, Wisconsin 52153
PHONE: 414-797-7844

INTERNATIONAL SALES REPRESENTATIVES AND DISTRIBUTORS

SUBSIDIARIES
Standard Microsystems Corporation (Asia)
9F-4, 169 Sec. 4 Chung Hsaid, E. Road
Taipei, Taiwan, R.O.C.
PHONE: 02-711-2840
TELEX: 21664 SMCTW
FAX: 886-2-7112845

Standard Microsystems GmbH
Arabella Strasse 5-Buero 131
D-8000 Muenchen 81
West Germany
PHONE: 49-89-919594
TELEX: 5214433 SMCG

Toyo Microsystems Corporation
Akasaka Dai-Ichi, Building 12 F
4-9-17 Akasaka
Minato-ku, Tokyo 107, Japan
PHONE: 03-423-6651
FAX: 03-423-6654

ARGENTINA
Electroquimica Delta Ind. Comp.
Timoteo Gordillo 72
COD Postal 1408
Buenos Aires-R
PHONE: 641-3193
TELEX: 21212 AR EDELTA

AUSTRIA
Othmar Lackner
Elektron Bauelement und Gerate
Landstr Haupstr 37
A-1031 Vienna
PHONE: 43-222-75-26-18

AUSTRALIA
Total Electronics
9 Harker Street
Burwood, Victoria 3125
PHONE: 03-288-4044
TELEX: AA31261

BELGIUM
Auriema Belgium S.A./N.V.
Rue Brogneztraat 172-A
B-1070 Brussels
PHONE: 32-2-523-6295
TELEX: 84621646

BRAZIL
Filcres
Rua Aurora, 165
CEP .01209, Caixa Postal 18767
San Paulo
PHONE: 011-223-7388
TELEX: 1131298

CANADA
Carsten Electronics Ltd.
3791 Victoria Park Avenue #1
Scarborough, Ontario M1W 3K6
PHONE: 416-495-9999
TELEX: 065-26264

Carsten Electronics Ltd.
215 Stafford Road, Unit 106
Nepean, Ontario K2H 9C1
PHONE: 613-726-9250

Carsten Electronics Ltd.
9480 Trans Canada Highway
St. Laurent, Quebec H4S 1R7
PHONE: 514-334-8321

Future Electronics, Inc.
5809 MacLeod Trail S.
Unit 109
Calgary, Alberta T2H 0J
PHONE: 403-259-6408

Future Electronics, Inc.
82 St. Regis Crescent No.
Downsview, Ontario M3J 123
PHONE: 416-638-4771
TELEX: 610-491-1470

Future Electronics, Inc.
237 Hymus Blvd.
(Pointe Claire)
Montreal, Quebec H9R 5C7
PHONE: 514-694-7710

Future Electronics, Inc.
Baxter Center
1050 Baxter Road
Ottawa, Ontario K2C 3P2
PHONE: 613-820-8313

Future Electronics, Inc.
1695 Boundry Road
Vancouver, B.C. V5R 4X7
PHONE: 604-294-1166

Haltronics, Ltd.
1085 North Service Rd. E.
Oakville, Ontario L6H 1A6
PHONE: 416-844-2121
TELEX: 610-495-2664
FAX: 416-844-0129
Eastern & Western Canada
1-800-387-7949
Central Canada
1-800-387-7955

DENMARK
Tage Olsen A/S
Ballerup Byvej 222
DK2750 Ballerup
PHONE: 45-2-658111
TELEX: 85535293

FINLAND
Instrumentarium Elek.
P.O. Box 64
SF-02631 Espoo 63
PHONE: 35805284320
TELEX: 57124426
FAX: 35805021073

FRANCE
Tekelec Airtronic
Cite Des Bruyeres
Rue Carle Vernet
BP2 92310 Sevres
PHONE: 33-14-5347535
TELEX: 204552F

HONG KONG
Protech Components Ltd.
Flat 3, 10/F Wing Shing Ind Bldg.
26 Ng Fong St.
San Po Kong Kowloon
PHONE: 3-255106
TELEX: 38396 PTLD HX

INDIA
Shivam Computers PVT Ltd.
9 National Chambers,
near Dipali Cinema Ashram Road
Ahmedabad
PHONE: 40916(0) 443488(R)
TELEX: 121539 TRCE-IN

ISRAEL
RDT Electronics Engr. Ltd.
ATIDIM Advanced Technologies Pk.
Neve Sharat
Tel Aviv
PHONE: 972-3492187, 188, 191
TELEX: 371452 or 92233551

ITALY
Dott. Ing. Giuseppe De Mico SPA
Viale Vittorio Veneto 8
20060 Cassina De Pecchi
Milano
PHONE: 02-95-20-551
TELEX: 330869

NEDERLAND
Auriema Nederland BV
Doornakkersweg 26
5642MP Eindhoven
PHONE: 31-40-816565
TELEX: 84451992

NORWAY
Henaco A/S
Box 126, Kaldbakken
Trondheimsveien 436
Oslo 9
PHONE: 47-2-16210
TELEX: 76716 Hanac N

SINGAPORE
Logic Devices Ltd.
No. 3, Lorong Bakar Batu
08-04, Brightway Bldg.
Singapore 1334
PHONE: 7438737/74387
TELEX: RS 39142
FAX: 65-7488694

SOUTH AFRICA
Eagle Electric
31-41 Hout Street
Capetown 8000
Republic of South Africa
PHONE: 451421
TELEX: 5-21713

SOUTH KOREA
Kortronics Enterprises
Room 307, B-9
#604-01, Guro-Dong, Guro-gu
Seoul
PHONE: 634-5497
TELEX: MICROS K28484

SPAIN
Amitron S.A.
Avenida de Valladolid, 47A
28008 Madrid
PHONE: 247-93-13/248-58-63
TELEX: 45550 AMIT-E

SWEDEN
NAXAB
Box 4115
17104 Solna
PHONE: 08-98-51-40
TELEX: 17912

SWITZERLAND
Datacomp AG
Silbernstrasse 10
CH-8593 Dietikon
Zurich, Switzerland
PHONE: 41-1-7405140
TELEX: 827750 DACO
FAX: 1-7413423

TAIWAN
Sertek International
3 Fl. No. 135
Chien Kuo N. Road, Sec. 2
Taipei
PHONE: 02-501-0055
TELEX: 23756 SERTEK

UNITED KINGDOM
Golden Gate
Winchester House
Gardner Road
Maidenhead
Berks SL6 7RL
PHONE: 44-628-783631
TELEX: 846263 Golden G
FAX: 44-628-71120

Manhattan Skyline
Manhattan House
Bridge Road
Maidenhead, Berkshire SL6 808
PHONE: 44-628-75851
TELEX: 851-847898

WEST GERMANY
Atlantik Elektronik Gmbh
Fraunhoferstr, 11A
D-8033 Martinsried
PHONE: 49-89-8570000
TELEX: 5215111 ALEC D

Beka Electronics Gmbh
Industriestrasse 39-43
D-2000 Wedel
PHONE: 49-4103840061
TELEX: 2789582

Tekelec Aitronic Gmbh
Kapauzinerstrasse 9
8000 Munich 2
PHONE: 49-89-51640
TELEX: 522241

STANDARD MICROSYSTEMS CORPORATION

APPLICATION AND TECHNICAL NOTE DIRECTORY

DATA COMMUNICATIONS

NUMBER:	TITLE:	USE WITH PART NUMBERS:
TN5-1	Using the COM8004 for High Data Integrity in Bit Oriented Protocols	COM8004 COM5025
TN5-2	Using the COM9026 Local Area Controller and the COM9032 Local Area Network Transceiver	COM9026 COM9032
TN5-3	MIL-STD-1533A and MIL-STD-1553B Overview	COM1553A COM1553B
TN5-5	VLSI Circuit Provides Complete Controller for Token-Pass Systems	COM9026 COM9032
TN5-6	Low Cost High Performance Token Pass LAN	COM9026 COM9032
TN5-7	COM7210 GPIB-488 Talker/ Listener Controller	COM7210

DISPLAY PRODUCTS

AN1-7	Horizontal Scrolling with the CRT5037 VTAC®	CRT5037
AN4-1	CRT9006 Single Row Buffer Enhances Processor Through-put	CRT9006
AN4-3	Programming and Interfacing to the CRT9007	CRT9006 CRT9007 CRT9021 CRT9212
AN4-4	Next Generation CRT Systems	CRT9006 CRT9007 CRT9021 CRT9212
AN4-5	Using the CRT97C11 in an Alphanumeric Terminal	CRT97C11
TN4-2	CRT9007 VPAC® A Next Generation CRT Controller	CRT8002 CRT9006 CRT9007 CRT9021 CRT9212
TN4-5	CRT9028 VTLC™ A New Video Terminal Logic Controller	CRT9028
TN4-6	A Flexible Approach to Video Graphic Systems using the CRT9007 VPAC®	CRT9007
TN4-7	Variable Character Size with the CRT9041	CRT9007 CRT9041

FLOPPY DISK/HARD DISK

NUMBER:	TITLE:	USE WITH PART NUMBERS:
TN6-1	Principles of Digital Floppy Disk Data Separation Using FDC9216, FDC9229 or FDC9266	FDC9216 FDC9229 FDC9266
TN6-2	Improved Functionally Simplifies Disk Controller Design	HDC9224
TN6-3	FDC765A Circuit Recommendation	FDC765A FDC9229
TN6-5	Programming the HDC9224 Universal Disk Controller	HDC9224
TN6-6	Programming the FDC765A, FDC9266 and FDC9267	FDC765A FDC9266 FDC9267
TN6-7	HDC9224 Programmers Reference Card	HDC9224 HDC9225 HDC9226

MAGAZINE REPRINTS

EDN MAGAZINE
- Networking Design Series (1984)

PC MAGAZINE
- LANs Under Netware (12/86)
- LANs in Perspective (4/87)

ELECTRONIC ENGINEERING TIMES
- ARCNET...A Piece of the factory automation puzzle (4/87)

ELECTRONIC DESIGN
- Control System/3x peripheral communication with one chip (6/87)

35 Marcus Boulevard, Hauppauge, NY 11788

2/88-80M