Microprocessors & Memories

PowerPC

Flash Memories

68040

Hi-Rel

Flash Memories

PowerPC™

68020

Hi-Rel

BroadBand
Technical Sales

408-376-0500
FAX 408-376-0505

THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

MICROPROCESSORS
&
MEMORIES

1996-1997

THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

CONTENTS

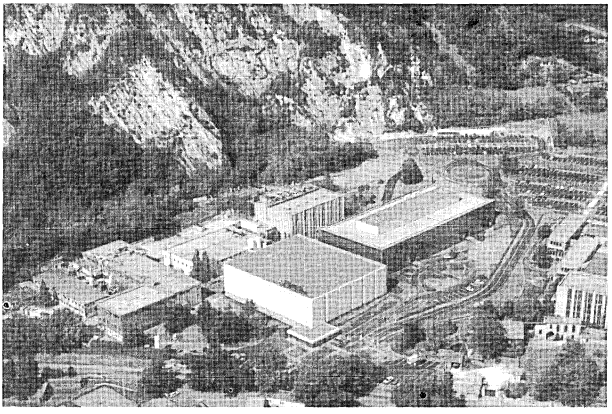
TCS, A LONG TERM PARTNERSHIP FOR HIGH RELIABILITY SEMICONDUCTORS

Over the last 20 years, Thomson has progressively built-up a worldwide expertise in providing silicon semiconductors dedicated to military, aerospace and professionnal electronics applications.

TCS, subsidiary of Thomson-CSF is mainly dedicated to serving these markets and is now organized in three product lines :

- Image Sensors : CCDs, IR sensors,
- ASICs : Analog to Digital and Mixed.
- Standard Products : Microprocessors, Memories and fast A/D Converters.

Thanks to a long term partnership and licences policy with major semiconductors suppliers such as Motorola and SGS-Thomson Microelectronics, TCS is always able to offer the state-of-the art technologies and latest products from commercial world, selected, manufactured and tested to meet the exact requirements of Hi-Rel equipments.



The company's human and material ressources are mainly dedicated to serving high-end professionnal electronics customers. Its highly skilled and motivated personnel offers customers comprehensive technical support and service.

Industrial capabilities

The TCS manufacturing center in Saint-Égrève, near Grenoble, France, covers a 15,000 square meters site.

It includes a wafer foundry of 2,600 square meters clean rooms (class 10 to 1) and a fully automated assembly line of 1000 square meters for hermetic packages.

High performance automatic test equipments (Teradyne J971, Genrad 180 etc.) running the original test programs from our partners give a total garanty that the products can operate under even the most severe temperature conditions.

Numerous Quality Controle equipment is also available to verify hermeticity, for complete usual climato-mechanical tests for military operations and for component analysis.

A wide range of Hi-Rel silicon semiconductors

- Global ASICs design and production capabilities : from high complexity CMOS digital products to high-performance analog arrays and mixed analog/digital products.
- Linear and area array CCDs for high-end applications (including space, military, scientific, astronomy, medical and industrial) covering the full wavelength spectrum from X-rays and UV to Infrared.
- Microprocessors range supporting Motorola architecture 68000 family from 8 to 32-Bit, Power PC, MCUs from 8 to 32-Bit.
- Non-volatile memories from UV-EPROMs 16 KBit to 1 MBit, to flash EPROMs.
- A range of high speed, low power dissipation A/D converters from 8 bits 60 MHz to 12 bits 40 MHz and 8 bits 1 GHz for Hi-end applications from Military and Space to Industrial, scientific and medical).

A core focus on quality

A core component of TCS strategy is to continuously invest in quality for its customers satisfaction, implementing Total Quality Management concepts.

Thanks to this policy, TCS is ISO9001 and RAQ1 (equivalent to NATO AQUAP1) certified.

Every components of TCS are offered in conformity to the most exacting internationnal standards, from MIL-STD-883 to ESA/SCC 9000. On top of this, a number of TCS microprocessors are DESC certified for Military applications.

Long term availability

Concerned with the long life time of Hi-Rel systems, TCS has implemented a specific strategy to insure that the devices are available for periods in excess of 25 years. This strategy is based on long term process availability and wafer storage, secured by the use of severe validation and periodic controle procedures.

ALPHANUMERICAL INDEX

CROSS REFERENCE INDEX

MOTOROLA AND TCS CROSS REFERENCE

	MIL 883 MOTOROLA P/N	MIL 883 TCS P/N	PACKAGE	DESC SMD P/N	COMMENTS
32-bit	68020-16/BZAJC 68020-16/BYCJC	TS68020MR1B/C16 TS68020MFB/C16	PGA 114 CLCC 132	5962-8603202XA 5962-8603202YC	Other available speeds : 20 MHz & 25 MHz
	68040-25/BZAJC 68040-25/BYCJC	TS68040MR1B/C25 TS68040MFB/C25	PGA 179 CLCC 196	5962-9314301MXA 5962-9314301MYC	Other available speeds : 33 MHz
	68882-16/BZAJC 68882-16/BYCJC	TS68882MR1B/C16 TS68882MFB/C16	PGA 68 CLCC 68	5962-8946301XA 5962-8946301YC	Other available speeds : 20 MHz, 25 MHz & 33 MHz
16-bit	68000-8/BXAJC 68000-8/BZAJC	TS68000MC1B/C8 TS68000MR1B/C8	DIL 64 PGA 68	8202102YA 8202102TA	Other available speeds : 10 MHz
	68000-8/BYCJC	TS68000ME1B/C8	LCC 68 CLCC 68	8202102ZA 8202102UC	12 MHz (TCS only)
		TS68008M/C8	DIL 48		Limited supply
		TS68230MCB/C8 TS68230ME1B/C8	DIL 48 LCC 52	5962-9317001MXC 5962-9317001MYA	Other available speeds : 10 MHz
		TS68901MCB/C4 TS68901ME1B/C4	DIL 48 LCC 52	5962-8850601XC 5962-8850601YA	Other available speeds : 5 MHz
	68HC000-8BXAJC 68HC000-8BUAJC 68HC000-8BZAJC 68HC000-8BYCJC	TS68C000MC1B/C8 TS68C000ME1B/C8 TS68C000MR1B/C8 TS68C000MFB/C8	DIL 64 LCC 68 PGA 68 CLCC 68	5962-8946201MYA 5962-8946201MXA 5962-8946201MUA 5962-8946201MZC	Other available speeds : 10 MHz & 12 MHz
		TS68C901BMCB/C4 TS68C901BME1B/C4	DIL 48 LCC 52	5962-9086401MXC 5962-9086401MYA	Other available speeds : 5 MHz & 8 MHz
		TS68C901BMRB/C4 TS68C901BMFB/C4	PGA 68 CLCC 52	5962-9086401MZC 5962-9086401MUC	
8-bit	6800/BQAJC	EF6800CMB/B	DIL 40		Limited supply
	6802/BQAJC	EF6802CMB/C	DIL 40		Limited supply
		EF6803CMB/C	DIL 40		Limited supply
	6809/BQAJC	EF6809CMB/C EF6809ECMB/B	DIL 40 DIL 40		
		EF6810CMB/B	DIL 24		Limited supply
	6821/BQAJC	EF6821CMB/C	DIL 40		
	6840/BXAJC	EF6840CMB/C	DIL 28		
	6850/BJAJC	EF6850CNB/C	DIL 24		
	6852/BJAJC	EF6852CMB/B	DIL 24		Limited supply
	6854/BXAJC	EF6854CMB/B	DIL 28		Limited supply
MCU	68HC11A1/BXAJC 68HC11A1/BYCJC	TS68HC11A1MC1B/C TS68HC11A1MFB/C	DIL 48 CLCC 52	5962-9051002XA 5962-9051002YC	
	68HC811E2/BXAJC 68HC811E2/BYCJC	TS68HC811E2MC1B/C TS68HC811E2MFB/C	DIL 48 CLCC 52	5962-8952701XA 5962-8952701YC	
	68302-16/BZAJC 68302-16/BYCJC	TS68302MR1B/C16 TS68302MFB/C16	PGA 132 CLCC 132	5962-9315901MXA 5962-9315901MYC	
	68332-16/BZAJC 68332-16/BYCJC	TS68332MR1B/C16 TS68332MFB/C16	PGA 132 CLCC 132	5962-9150101MZA 5962-9150101MYC	
		TS68EN360MFB/C	CLCC 240		To be introduced
		PC603EMAB/C100	CLCC 240		To be introduced

DESC QUALIFIED PRODUCT LIST

DESC qualified products - ARINC

TCS GENERIC P/N	TCS-DESC P/N	SMD #	PACKAGE	LEAD FINISH	AVAILABILITY STATUS
EF4442JMB/C	EF4442DESC01MA	5962-9071901MA	CERDIP	Tin	Yes

DESC qualified products - 16-bit family

TCS GENERIC P/N	TCS-DESC P/N	SMD #	PACKAGE	LEAD FINISH	AVAILABILITY STATUS
TS68000MR1B/C8	TS68000DESC02TA	8202102TA	PGA	Tin	Yes
TS68000MRB/C8	TS68000DESC02TC	8202102TC	PGA	Gold	Yes
TS68000MR1B/C10	TS68000DESC03TA	8202103TA	PGA	Tin	Yes
TS68000MRB/C10	TS68000DESC03TC	8202103TC	PGA	Gold	Yes
TS68000MR1B/C12	TS68000DESC04TA	8202104TA	PGA	Tin	Yes
TS68000MRB/C12	TS68000DESC04TC	8202104TC	PGA	Gold	Yes
TS68000MC1B/C8	TS68000DESC02YA	8202102YA	DIL S/B	Tin	Yes
TS68000MC1B/C10	TS68000DESC03YA	8202103YA	DIL S/B	Tin	Yes
TS68000MC1B/C12	TS68000DESC04YA	8202104YA	DIL S/B	Tin	Yes
TS68000ME1B/C8	TS68000DESC02ZA	8202102ZA	LCC	Tin	Yes
TS68000ME1B/C10	TS68000DESC03ZA	8202103ZA	LCC	Tin	Yes
TS68000ME1B/C12	TS68000DESC04ZA	8202104ZA	LCC	Tin	Yes
TS68230MCB/C8	TS68230DESC01XC	5962-9317001MXC	DIL S/B	Gold	Yes
TS68230MCB/C10	TS68230DESC02XC	5962-9317002MXC	DIL S/B	Gold	Yes
TS68230ME1B/C8	TS68230DESC01YA	5962-9317001MYA	LCCC	Tin	Yes
TS68230ME1B/C10	TS68230DESC02YA	5962-9317002MYA	LCCC	Tin	Yes
TS68901MC1B/C4	TS68901DESC01XA	5962-8850601XA	DIL S/B	Tin	Yes
TS68901MC1B/C5	TS68901DESC02XA	5962-8850602XA	DIL S/B	Tin	Yes
TS68901ME1B/C4	TS68901DESC01YA	5962-8850601YA	LCC	Tin	Yes
TS68901ME1B/C5	TS68901DESC02YA	5962-8850602YA	LCC	Tin	Yes
TS68C901BMC1B/C4	TS68C901BDESC01XA	5962-9086401XA	DIL S/B	Tin	Yes
TS68C901BMC1B/C5	TS68C901BDESC02XA	5962-9086402XA	DIL S/B	Tin	Yes
TS68C901BMC1B/C8	TS68C901BDESC03XA	5962-9086403XA	DIL S/B	Tin	Yes
TS68C901BME1B/C4	TS68C901BDESC01YA	5962-9086401YA	LCC	Tin	Yes
TS68C901BME1B/C5	TS68C901BDESC02YA	5962-9086402YA	LCC	Tin	Yes
TS68C901BME1B/C8	TS68C901BDESC03YA	5962-9086403YA	LCC	Tin	Yes
TS68C000MR1B/C8	TS68C000BDESC01TA	5962-8946201TA	PGA	Tin	Yes
TS68C000MRB/C8	TS68C000BDESC01TC	5962-8946201TC	PGA	Gold	Yes
TS68C000MR1B/C10	TS68C000BDESC02TA	5962-8946202TA	PGA	Tin	Yes
TS68C000MRB/C10	TS68C000BDESC02TC	5962-8946202TC	PGA	Gold	Yes
TS68C000MR1B/C12	TS68C000BDESC03TA	5962-8946203TA	PGA	Tin	Yes
TS68C000MRB/C12	TS68C000BDESC03TC	5962-8946203TC	PGA	Gold	Yes
TS68C000MF1B/C8	TS68C000DESC01UA	5962-8946201UA	CQFP	Tin	Yes
TS68C000MF1B/C10	TS68C000DESC02UA	5962-8946202UA	CQFP	Tin	Yes
TS68C000MF1B/C12	TS68C000DESC03UA	5962-8946203UA	CQFP	Tin	Yes
TS68C000ME1B/C8	TS68C000DESC01XA	5962-8946201XA	LCC	Tin	Yes
TS68C000ME1B/C10	TS68C000DESC02XA	5962-8946202XA	LCC	Tin	Yes
TS68C000ME1B/C12	TS68C000DESC03XA	5962-8946203XA	LCC	Tin	Yes
TS68C000MC1B/C8	TS68C000DESC01YA	5962-8946201YA	DIL S/B	Tin	Yes
TS68C000MC1B/C10	TS68C000DESC02YA	5962-8946202YA	DIL S/B	Tin	Yes
TS68C000MC1B/C12	TS68C000DESC03YA	5962-8946203YA	DIL S/B	Tin	Yes

DESC QUALIFIED PRODUCT LIST

DESC qualified products - 32-bit family

TCS GENERIC P/N	TCS-DESC P/N	SMD #	PACKAGE	LEAD FINISH	AVAILABILITY STATUS
TS68020MR1B/C16	TS68020DESC02XA	5962-8603202XA	PGA	Tin	Yes
TS68020MRB/C16	TS68020DESC02XC	5962-8603202XC	PGA	Gold	Yes
TS68020MR1B/C20	TS68020DESC03XA	5962-8603203XA	PGA	Tin	Yes
TS68020MRB/C20	TS68020DESC03XC	5962-8603203XC	PGA	Gold	Yes
TS68020MR1B/C25	TS68020DESC04XA	5962-8603204XA	PGA	Tin	Yes
TS68020MRB/C25	TS68020DESC04XC	5962-8603204XC	PGA	Gold	Yes
TS68020MF1B/C16	TS68020DESC02YA	5962-8603202YA	CQFP	Tin	Yes
TS68020MF1B/C20	TS68020DESC03YA	5962-8603203YA	CQFP	Tin	Yes
TS68020MFB/C25	TS68020DESC04YC	5962-8603204YC	CQFP	Gold	Yes
TS68020MF1B/C25	TS68020DESC04YA	5962-8603204YA	CQFP	Tin	Yes
TS68040MRB/C25	TS68040DESC01XC	5962-9314301MXC	PGA	Gold	Yes
TS68040MF1B/C25	TS68040DESC01XA	5962-9314301MXA	PGA	Tin	Yes
TS68040MFB/C25	TS68040DESC01YC	5962-9314301MYC	CQFP	Gold	Yes
TS68040MF1B/C25	TS68040DESC01YA	5962-9314301MYA	CQFP	Tin	Yes
TS68882MR1B/C16	TS68882DESC01XA	5962-8946301XA	PGA	Tin	Yes
TS68882MRB/C16	TS68882DESC01XC	5962-8946301XC	PGA	Gold	Yes
TS68882MR1B/C20	TS68882DESC02XA	5962-8946302XA	PGA	Tin	Yes
TS68882MRB/C20	TS68882DESC02XC	5962-8946302XC	PGA	Gold	Yes
TS68882MR1B/C25	TS68882DESC03XA	5962-8946303XA	PGA	Tin	Yes
TS68882MRB/C25	TS68882DESC03XC	5962-8946303XC	PGA	Gold	Yes
TS68882MR1B/C33	TS68882DESC04XA	5962-8946304XA	PGA	Tin	Yes
TS68882MRB/C33	TS68882DESC04XC	5962-8946304XC	PGA	Gold	Yes
TS68882MF1B/C16	TS6882DESC01YA	5962-8946301YA	CQFP	Tin	Yes
TS68882MFB/C16	TS6882DESC01YC	5962-8946301YC	CQFP	Gold	Yes
TS68882MF1B/C20	TS6882DESC02YA	5962-8946302YA	CQFP	Tin	Yes
TS68882MFB/C20	TS6882DESC02YC	5962-8946302YC	CQFP	Gold	Yes
TS68882MF1B/C25	TS6882DESC03YA	5962-8946303YA	CQFP	Tin	Yes
TS68882MFB/C25	TS6882DESC03YC	5962-8946303YC	CQFP	Gold	Yes
TS68882MF1B/C33	TS6882DESC04YA	5962-8946304YA	CQFP	Tin	Yes
TS68882MFB/C33	TS6882DESC04YC	5962-8946304YC	CQFP	Gold	Yes

DESC qualified products - MCU's

TCS GENERIC P/N	TCS-DESC P/N	SMD #	PACKAGE	LEAD FINISH	AVAILABILITY STATUS
TS68HC811E2MFB/C	TS68HC811E2DESC01YC	5962-8952701YC	CQFP	Gold	Q396
TS68HC811E2MF1B/C	TS68HC811E2DESC01YA	5962-8952701YA	CQFP	Tin	Q396
TS68HC811E2MCB/C	TS68HC811E2DESC01XC	5962-8952701XC	DIL S/B	Gold	Yes
TS68HC811E2C1MB/C	TS68HC811E2DESC01XA	5962-8952701XA	DIL S/B	Tin	Yes
TS68HC11A1MC1B/C	TS68HC11A1DESC01XA	5962-9051002XA	DIL S/B	Tin	Yes
TS68HC11A1MCB/C	TS68HC11A1DESC01XC	5962-9051002XC	DIL S/B	Gold	Yes

ARINC 429 INTERFACE

5

EF 4442

ARINC 429 MULTI-CHANNEL BUFFER RECEIVER (RTA) (N CHANNEL, SILICON GATE)

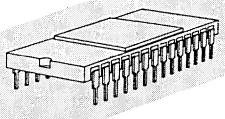
ONGOING REDESIGN

DESCRIPTION

The EF 4442 is a reception interface for 4 ARINC 429 channels.

Two models of operation are provided :

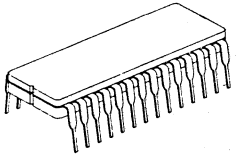
- When in A mode, the circuit can be considered as a peripheral of an EF 6800 or EF 6802 microprocessor and is totally software programmable (for example for test purposes).
- When in B mode, the parameters are hardware programmed. Reading the registers which contain messages is only possible (max. scan frequency : 2 MHz).



C Suffix
DIL 28
Ceramic Side Brazed package
(obsolete package)

MAIN FEATURES

- 4 independant receivers.
- 1 transmitter in A mode.
- Direct 6800 microprocessor interface.
- 8 bit data bus.
- ARINC interface : «1» & «0» lines, RZ code.
- Software label control in A mode.
- Parity control : odd or no parity.
- Interrupt capability in A mode.
- Test mode capability.

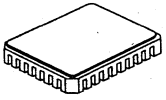


J Suffix
DIL 28
Ceramic package (preferred)

SCREENING QUALITY

This product is manufactured in full compliance with either :

- NFC 96883 class G.
- MIL-STD-883 class B.
- DESC : 5962-90719.
- According to TCS standards.



E Suffix
LCCC 32
Leadless Ceramic Chip Carrier package
(on request only)

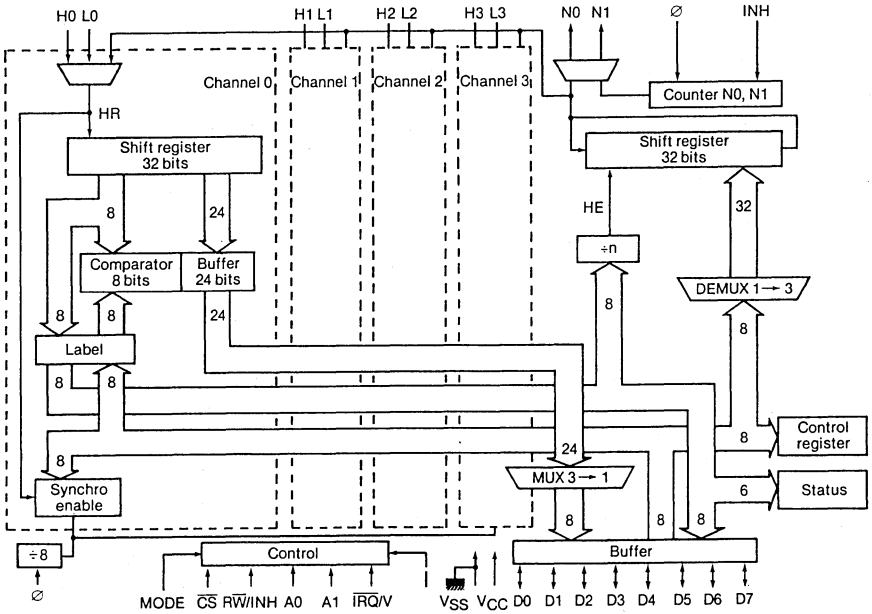
APPLICATION NOTE

Ask for application note : «General application principles EF 4442 (RTA)».

SUMMARY

A - GENERAL DESCRIPTION

1 - BLOCK DIAGRAM



2 - PIN DESCRIPTION

Name number	Description
V_{SS}	This pin is connected to the negative side of the power supply (ground).
$\overline{RW}$/INH	This input selects the direction of transfer (write or read) of data between the circuit and the microprocessor when the circuit is programmed in mode A (cf. pin 28). In B mode, this input is used to disable the channel scanning divide by 4 counter.
N0	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the complemented output signal of the transmit shift register (logic «0» clock output) is available on this pin. In B mode, the value of the least significant bit of the address of the scanned channel is available on this pin.
N1	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the output signal of the transmit shift register (logic «1» clock output) is available on this pin. In B mode, the value of the most significant bit of the address of the scanned channel is available on this pin.
$\overline{CS}$	In A mode, this input (active when low) selects the chip for a microprocessor access.
A0	In A mode, this input corresponds to the least significant bit of the circuit function address. In B mode, this input corresponds to the least significant bit of the address of the data byte in the message.
A1	In A mode, this input corresponds to the most significant bit of the circuit function address. In B mode, this input corresponds to the most significant bit of the address of the data byte in the message.

2 - PIN DESCRIPTION (Continued)

Name number	Description
$\overline{RESET}$	This input (active when low) initializes the circuit by resetting some registers.
∅	This input receives the clock signal from the circuit which corresponds to phase ∅2 of the microprocessor clock.
D7	This tristate input/output is connected to the eighth line of the data bus.
D6	This tristate input/output is connected to the seventh line of the data bus.
D5	This tristate input/output is connected to the sixth line of the data bus.
D4	This tristate input/output is connected to the fifth line of the data bus.
V_{CC}	This pin is connected to the positive side of the power supply (+5 V)
D3	This tristate input/output is connected to the fourth line of the data bus.
D2	This tristate input/output is connected to the third line of the data bus.
D1	This tristate input/output is connected to the second line of the data bus.
D0	This tristate input/output is connected to the first line of the data bus.
L0	This input receives the logic «0» clock from the signal shaping separation subsystem of the first ARINC channel.
H0	This input receives the logic «1» clock from the signal shaping/separation subsystem of the first ARINC channel.
L1	This input receives the logic «0» clock from the signal shaping/separation subsystem of the second ARINC channel.
H1	This input receives the logic «1» clock from the signal shaping/separation subsystem of the second ARINC channel.
L2	This input receives the logic «0» clock from the signal shaping/separation subsystem of the third ARINC channel.
H2	This input receives the logic «1» clock from the signal shaping/separation subsystem of the third ARINC channel.
L3	This input receives the logic «0» clock from the signal shaping/separation subsystem of the fourth ARINC channel.
H3	This input receives the logic «1» clock from the signal shaping/separation subsystem of the fourth ARINC channel.
$\overline{IRQ}$ V	In A mode, this pin (active when low) constitutes an open drain output delivering the signal for interrupting the microprocessor. In B mode, this pin is an input used to program the number of high speed channels.
Mode	This input is used to program the operating mode (A or B) of the circuit and also to enable or disable the parity check.

3 - DESCRIPTION OF REGISTERS

The EF 4442 circuit features three types of internal register :

- Registers concerned with general circuit operation,
- Registers specific to the transmit channel,
- Registers specific to each receive channel.

3.1 - General registers

3.1.1 - Status register

This register is used only when the circuit is programmed in A mode. Its contents inform the microprocessor about the status of the circuit functions. Bits S0 to S4 activate output IRQ when at 1 (except S4 which is maskable - cf. description of control register).

Bits S0 to S3 at 1 indicate that the channel with the address which corresponds to the rank of the bit has received a correct message (label recognised and correct parity in the case of a circuit programmed to check the parity of messages).

Each bit is reset to 0 on reading the registers of the corresponding channel.

In transmit mode, bit S4 of the status register is set to 1 when transmission of the message is terminated.

Bit S4 is reset to 0 when control bit C4 (see below) is at 1.

Bits S5 and S6 are not used.

Bit S7 is at 1 throughout transmission.

3.1.2 · Control register

This eight-bit register (C0-C7) monitors operation of the circuit in A mode.

In receive mode, bits C0-C3 select the corresponding channels for writing or reading when set to 1 by the microprocessor.

Bit C4 at 1 enables programming of the transmit channel (data to send and transmission speed). The setting of bit C4 to 1 resets to 0 the index of the four-byte stack constituting the message to send.

Bit C5 at 1 is used to initiate transmission of the message. It is set to 0 when transmission is terminated.

Bit C6 at 1 simultaneously with bit C5 at 1 loops back the transmitted data to the input of the receive channel selected by bits C0-C3, for test purposes. It is set to 0 by any control register access.

Bit C7 at 1 masks status bit S4 and thus prevents activation of output $\overline{IRQ}$.

3.2 · Transmit channel registers (A mode only)

3.2.1 · Programmable divider register

This eight-bit register is programmed by the microprocessor and contains the value n of the division ratio (the least significant bit is always considered to be at 0).

The programmable divider generates a clock signal at a frequency equal to clock ∅ divided by n.

3.2.2 · Transmit register

This 32-bit shift register may be programmed in four phases by the microprocessor. This writing must be effected immediately after the setting to 1 of control bit C4 (cf. description of control register). This resets to zero the index of the four-byte stack.

The transmit register shifts the data present in it to the outputs in accordance with the states of the bits in the control register.

3.3 · Receive channel registers

Each receive channel comprises the following registers :

3.3.1 · Synchronization / enable register

This eight-bit register is programmable by the microprocessor.

The most significant bit (bit 7) is used, in A mode only, to disable the transfer of data received at the input into the buffer register (cf. description of these two registers).The channel affected is then seen as being out of service.

The other seven bits (bits 0 - 6) select the value of the time-delay used to detect the presence of a «gap». This is the space between two consecutive messages, the minimum duration of which is four periods of the transmit clock. This value is loaded into the register by the microprocessor, in A mode, at the same time as the enable bit.

In B mode, this value is selected from two hardwired values, according to the state on pin $\overline{IRQ}$/V.

If n is the programmed value, the gap detection time-delay will be (8 n − 4) ± 4 period of clock ∅.

3.3.2 · Input register

This 32-bit shift register receives the data corresponding to the messages. The message received is transferred into the registers on its output side if :

- a gap detection signal has previously occurred,
- the registers which will receive the transferred data are not being read,
- the parity of the received message is correct if the circuit is programmed with the parity check enabled,
- the enable bit of the synchronization/enable register is set to 1 (A mode only),
- in A mode, the first eight bits received correspond to the programmed label (cf. description of label register).

3.3.3 · Label register

In A mode, this eight-bit register is programmed by the microprocessor. It contains the label to be recognised.

In B mode, this register receives the first eight bits of the received message transferred from the input register.

In this case, this register may be read by the external automatic scanning device.

3.3.4 · Buffer register

This 24-bit register receives data transferred from the input regiester.

It may be read by the microprocessor in A mode or by the external automatic scanning device in B mode.

4 · CIRCUIT OPERATION

4.1 · Logic convention

«1» (high state) = most positive level

«0» (low state) = most negative level

4.2 · Operation of a receive channel

4.2.1 · Data acquisition

Serial data is received on the «low» and the «high» lines (Hi and Li inputs). Clock is reconstructed by OR-ing these inputs. Data is then directed towards a 32-bit shift register. Parity is computed. The reconstructed clock fall edge resets the message synchronization counter. This counter is incremented on each ∅ : 8 clock period and delivers a word synchronization signal (gap) as described below (figure 1) when reading a programmed value.

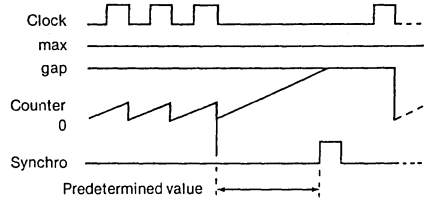


Figure 1 : Gap detection.

The predetermined value together with an enable bit is loaded in the internal synchro/validation register when in A mode ; it is choosen between two hardware programmed values when in B mode, according to the $\overline{IRQ}$/V pin.

Then :

• **When in A mode** – the first 8-bit (M0-M7) which are received, are compared to a programmed word (label), this for each channel. If identical, the 24 other bit of the shift register are transferred in a 24-bit buffer register. The corresponding status bit is switched to 1 and the $\overline{IRQ}$ line is activated ($\overline{IRQ}$ = 0).

If the channel enable bit is in the low state, transfer is not executed and the $\overline{IRQ}$ line is not activated.

• **When in B mode** – All the shift register bit are transferred in the label and the 24-bit buffer register.

Transfers are inhibited if the message parity is wrong in either mode (even number of bits in the high state) and if the circuit is programmed for parity check (Mode pin).

This last one generates a ∅ + n frequency square wave, n being the programmed value (the least significant bit being always set to 0).

then successively addresses the 8-bit bytes of the 24-bit buffer which are then available on the bus (D0-D7).

Reading the last byte resets the corresponding status byte to the low state.

The transfer from the receive register to the buffer register is inhibited from the «read» addressing of the channel (first or second byte) to the end of the last byte reading.

• **When in B mode** – A divide by 4 counter is incremented on each ∅ clock period and successively addresses the 4 channels. When the circuit is selected ($\overline{CS}$ = 0) and when A0-A1 = 11, the label of the addressed channel is available on the bus (D0-D7), as well as the channel number on the N0-N1 outputs.

Counting is inhibited when $\overline{RW}$/INH is in the high state. If the circuit is selected, the three bytes of the buffer register are then available on the bus when addressed through A0-A1 in the same way as for A mode register of the addressed channel is reset on the next A0-A1 = 11 configuration.

The transfert from the receive register to the buffer register is done in the same way as in A mode.

In order to read the message corresponding to label received, $\overline{CS}$ has to stay activated to 0 during the reading of label and message RT1-RT3 (minimum $\overline{CS}$ = 0 during the reading of the label and RT1).

However $\overline{CS}$ has to stay activated to 0 during less than 30 clock periods of PHI (∅).

4.3 · Operation of the transmit channel (only in A mode)

The transmit channel is composed of a 32-bit shift register and a programmable divider. The operation of this channel is controlled by the control register (C0-C7).

C4 selects the programmation of the transmit channel (see paragraph Programmation A mode). The 4 bytes of the shift register are loaded (including the microprocessor computed parity bit). So is the divider by n register byte.

This last one generates a ∅ divided by n frequency square wave, n being the programmed value (the least significant bit being always set to 0).

Transmission starts when C5 is set to 1. The data of the shift register is then available on the 0 and 1 lines of the channel and is clocked out at the choosen frequency.

The shift register is also feed forwarded so that data should not be lost. After the transmission of the 32nd bit, C5 is reset. The S4 bit is set to 1. It will be reset when C4 will be positionned to 1.

The S7 bit of the status register is set to 1 during all the transmission time.

If C5 is set to 1 after transmission of the 32nd bit, the message is retransmitted after 4 transmit clock periods. Status bit S4 will also be reset when control bit C4 is set to 1.

C6 is used for starting the receive channel testing. This test cannot be done during the reception of a message. If C6 = 1 the transmission channel signals are switched to the inputs of the control register selected receive channel. C6 is reset by any access to the control register.

C7 is a mask bit of the S4 bit of the status register. If C7 = 0 and S4 = 1, the $\overline{IRQ}$ line will be activated. If C7 = 1, the IRQ line will not be activated by S4.

Nota : C5 and C6 should be programmed at the same time in order to avoid transmission or test errors.

4.4 · Programmation in A mode (MODE = 0)

When seen from the microprocessor, the circuit looks like 4 addresses («read» or «write»).

Addressing any register of a channel is done in two steps :

- channel addressing by the control register
- byte of the selected channel addressing.

Thus, programmation of the synchro registers or the labels and reading of the 24-bit buffers or the status register are possible.

Loading of the transmit channel shift register is done through successive writing of the 4 bytes, the first being the label and then RT1, RT2, RT3. The addresses of the 4 bytes are generated by an internal modulo-4 counter which is reset by any addressing of the control register (see table 1 – Addressing with $\overline{CS}$ = 0 and table 2 – Addressing of the channels by the control register).

Table 1 · Addressing with $\overline{CS}$ = 0

RW/INH	A1	A0	Direct addressing	Channel addressing with the control register
Read	0	0	–	RT1
1	0	1	–	RT2
	1	0	–	RT3
	1	1	Status	–
Write	0	0	–	Synchro and divider by n
0	0	1	Control	–
	1	0	Not used	–
	1	1	–	Label

Table 2 · Channel addressing by the control register

C0	C1	C2	C3	Channel number
1	x	x	x	channel 0
0	1	x	x	channel 1
0	0	1	x	channel 2
0	0	0	1	channel 3

The gap detection counters are incremented on each ∅ divided by 8 clock period, if n is the synchro register value, the minimum detected gap length is (8n – 4) ± 4 ∅ clock periods.

C4 to C7 bits are independently interpreted.

C4 Pile loading if A0-A1 = 11 and divider by n if A0-A1 = 00.

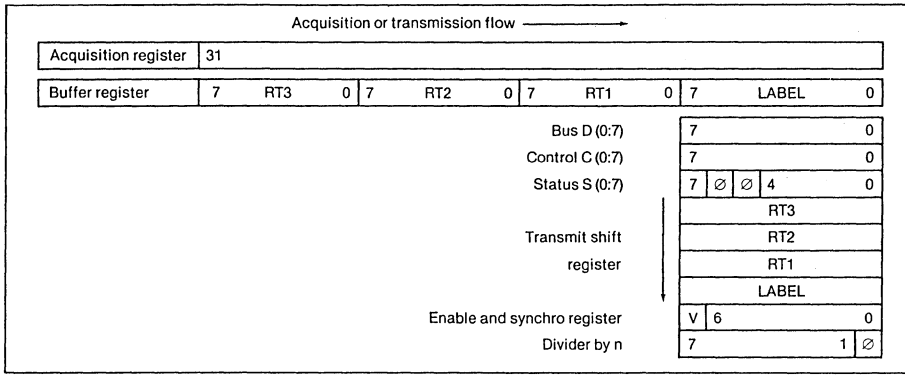
The loading of the 4 bytes to be transmitted should be done immediately after positionning C4 to 1, this operation resetting the pile index at the level of the label byte.

C5 Transmission start.

C6 Test mode.

C7 Transmit channel interrupt mask.

Table 3 · Bit correspondance



4.5 · Programmation in B mode (MODE = 1)

When in B mode, programmation is done by hardware. The number of high speed channels is programmed on IRQ/V pin (see table 4).

The synchro register is set to 5 for high speed channels and to 32 for low speed channels. This corresponds to a nominal ∅ clock frequency of 2 MHz and transmission frequencies of 12 to 14.5 KHz for low speed and of 99 to 101 KHz for high speed.

Table 4 · Programmation of the $\overline{IRQ}$/V pin

$\overline{IRQ}$/V	High speed channel numbers
0 : Low impedance	–
0 : High impedance	0
1 : Low impedance	0,1
1 : High impedance	0, 1, 2

4.6 · Parity check

If the MODE pin senses a high impedance (typ. > 10 kΩ) the circuit checks the parity of the messages for each receive channel. If the number of received 1's in an message is even, the transfer is not done and the message is discarded (odd parity).

When transmitting, the parity bit value is computed and loaded by the microprocessor or is the value of the received test message.

If the MODE pin is directly strapped to V_{CC} or V_{SS}, parity check is not done.

4.7 · Initialization

On power-on or when the $\overline{RESET}$ pin is set to 0, the following registers are reset to 0 :

- control register
- status register
- the 4 label registers of the receive channels
- the 4 synchro registers.

The first gap after initialization is also ignored for each channel because acquired data could not be error-free.

B - DETAILED DESCRIPTION

1 - ELECTRICAL CHARACTERISTICS

1.1 - Maximum ratings

Symbol	Rating		Value	Unit
V_{CC}	Supply voltage		−0.3 to +7	V_{dc}
V_{in}	Input voltage		−0.3 to +7	V_{dc}
T_C	Operating temperature range		TL to TH −55 to +125	°C
T_{stg}	Storage temperature range		−55 to +150	°C
Pd	Power dissipation	T_C = 125°C T_C = 25°C T_C = −55°C	300 350 550	mW mW mW

This device contains circuitry to protect the inputs against damage due to higt static voltages or electric fields : however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1.2 - Thermal characteristics (at 25°C)

Package	Symbol	Parameter	Value	Unit
DIL 28	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	50	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	10	°C/W
LCCC 32	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	45	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	9	°C/W

5

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

1.3 · Recommanded static operating conditions

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	2.0	5.25	V
V_{IL}	Input low voltage	−0.3	0.8	V
V_{CC}	Supply voltage	4.75	5.25	V

1.4 - Static characteristics

(V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 V ; −55°C < TC < +125°C)

Symbol	Characteristics	Min	Typ	Max	Unit
V_{IH}	Input high voltage (except MODE, $\overline{IRQ}$/V)	2.2		V_{CC}	V
V_{IL}	Input low voltage (except MODE, $\overline{IRQ}$/V)	−0.3		0.8	V
I_{in}	Input state leakage current (except MODE, $\overline{IRQ}$/V) (V_{in} = 0.4 to 5.25 V)	−10			µA
ITSI	Three state leakage current N0-N1, D0-D7 (V_{in} = 0.4 to 2.4 V)	−10		10	µA
V_{OH}	Output high voltage (I_{Load} = −250 µA) N0-N1, D0-D7 (I_{Load} = + 10 µA) $\overline{IRQ}$/V	2.4 2.4		V_{CC} V_{CC}	V
V_{OL}	Output low voltage (I_{Load} = 1.6 mA) N0-N1, D0-D7 (I_{Load} = 3.2 mA) $\overline{IRQ}$/V			0.4	V
C_{in}	Capacitance (Vin = 0, TC = 25°C, f = 1 MHz) (except MODE, $\overline{IRQ}$/V)			10	pF
R_H	External high programmation impedance MODE, $\overline{IRQ}$/V, (C_{load} ⩽ 20 pF) Scan frequency = f clock : 8)	10 K			Ω
R_L	External low programmation impedance MODE, $\overline{IRQ}$/V (C_{load} ⩽ 20 pF) Scan frequency = f clock : 8)			10	Ω
P_D	Power dissipation		310	550	mW
f	Maximum operating frequency in A mode	500		2000	kHz
F	Maximum operating frequency in B mode	1000		2000	kHz

5

1.5 · Dynamic characteristics

1.5.1 · Bus timing characteristics (load conditions, see Figure 7)

(V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 V ; −55°C < TC < +125°C)

Symbol	Characteristic		Min	Max	Unit
READ A MODE (Figure 2)					
t_{AH}	Address input hold time	A0-A1, R/$\overline{W}$/INH, $\overline{CS}$	10		ns
t_{ACC}	Data access time	D0-D7		300	ns
t_{DH}	Data output hold time	D0-D7	10		ns
WRITE - A MODE (Figure 3)					
t_{AS}	Address input setup time	A0-A1, R/$\overline{W}$/INH, $\overline{CS}$	50		ns
t_{AH}	Address input hold time	A0-A1, R/$\overline{W}$/INH, $\overline{CS}$	10		ns
t_{DS}	Data set up time	D0-D7	100		ns
t_{DH}	Data input hold time	D0-D7	50		ns
READ - B MODE (Figure 4)					
t_{AS}	Address setup time	A0-A1, $\overline{CS}$	50		ns
t_{AH}	Address input hold time	A0-A1, R/$\overline{W}$/INH, $\overline{CS}$	10		ns
t_{DH}	Data output hold time	N0-N1, D0-D7	10		ns
t_{ACC}	Data access time	N0-N1, D0-D7		300	ns
t_{SI}	R/$\overline{W}$/INH setup time		50		ns

1.5.2 · Clock timing characteristics (Figure 6)

Symbol	Characteristic	Min	Max	Unit
t_{CA}	A mode cycle time	500	2000	ns
t_{CB}	B mode cycle time	500	1000	ns
t_{WH}	Pulse width - high	180	2000	ns
t_{WL}	Pulse width - low	180	2000	ns
t_r, t_f	Rise time, fall time		15	ns

1.5.3 · $\overline{IRQ}$/V output timing characteristics (Figure 5)

Symbol	Characteristic	Max	Unit
t_{PLH}	Delay time - Low to high state	1600	ns
t_{PHL}	Delay time - high to low state	1000	ns

1.5.4 · Timing diagrams

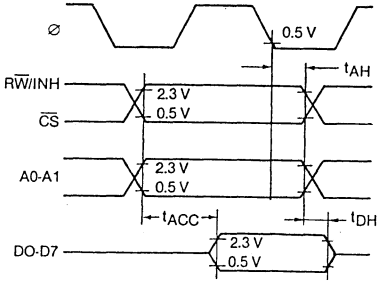


Figure 2 : Read A mode.

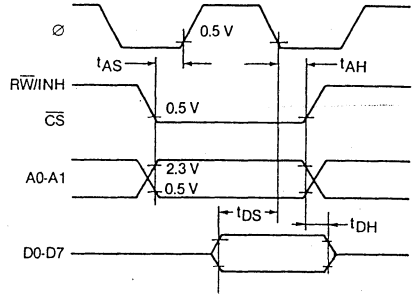


Figure 3 : Write A mode.

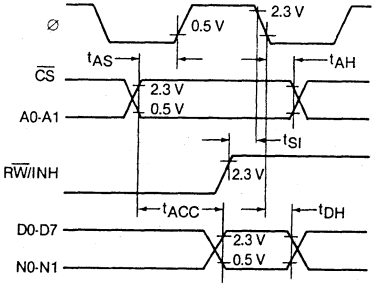


Figure 4 : Read B mode.

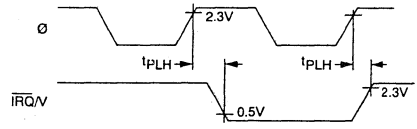


Figure 5 : IRQ/V output.

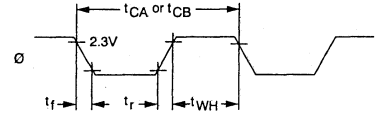


Figure 6 : Clock.

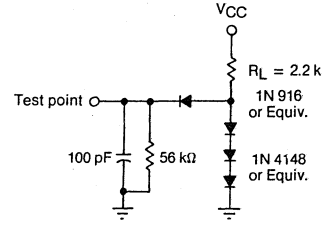


Figure 7 : Test load.

2 · PREPARATION FOR DELIVERY

2.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510.

2.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or TCS standard and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

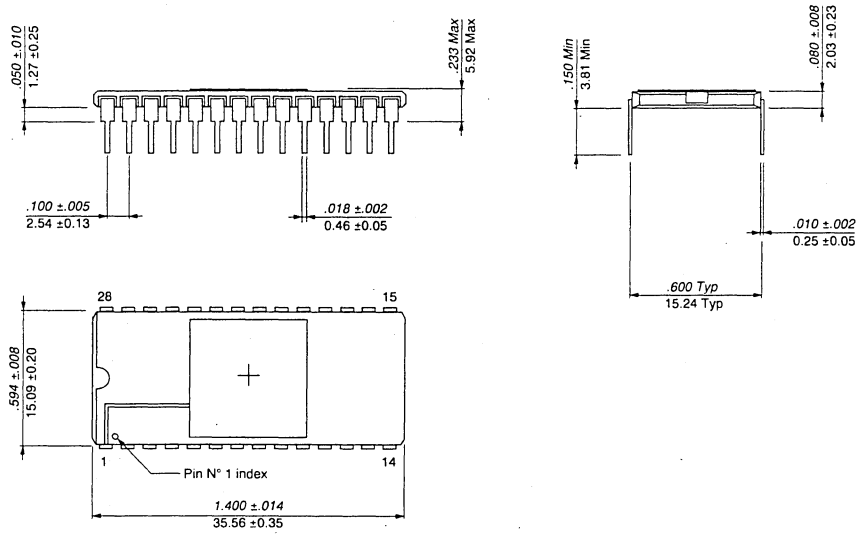
3 · HANDLING

Devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

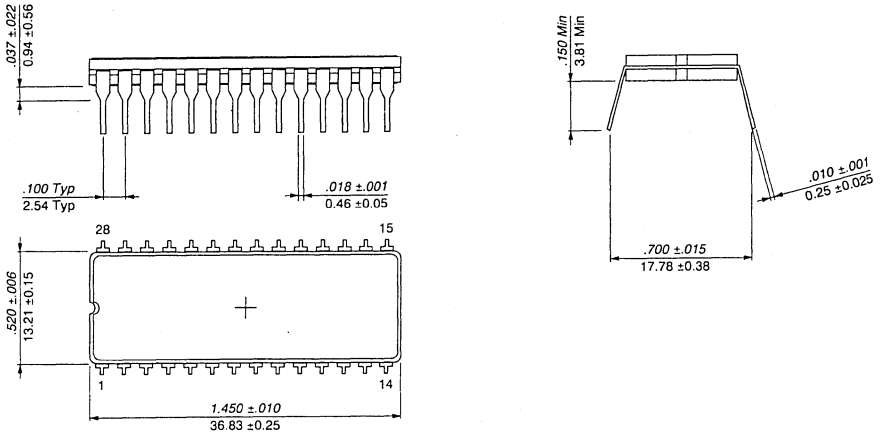
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk.
f) Maintain relative humidity above 50 %, if practical.

4 · PACKAGE MECHANICAL DATA

4.1 · DIL 28 - Ceramic Side Brazed package (obsolete package)

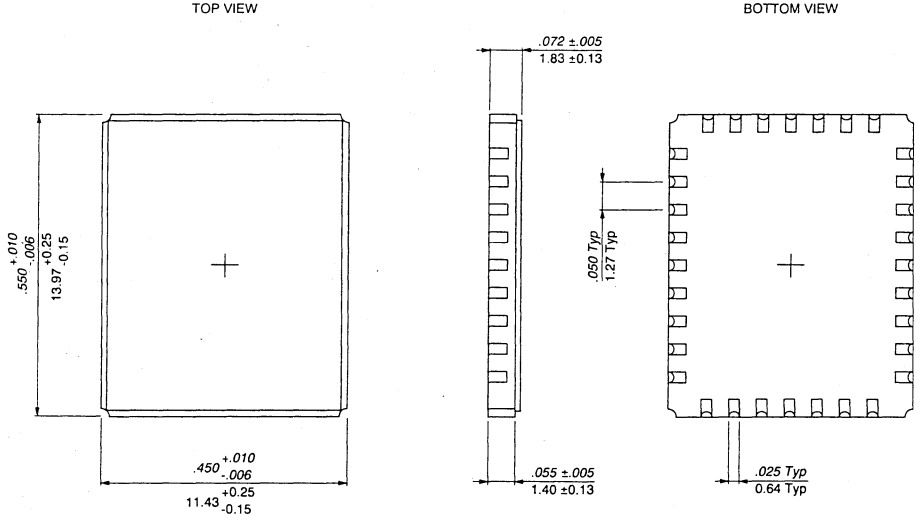


4.2 - DIL 28 - Cerdip package



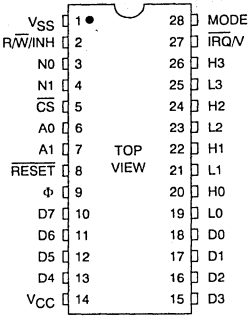
4.3 - LCCC 32 - Leadless Ceramic Chip Carrier package (Possible on request)

To be confirmed.

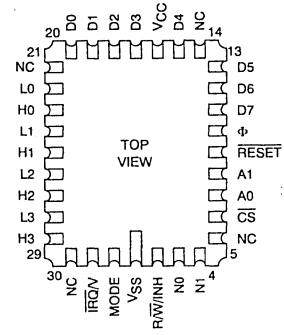


5 - TERMINAL DESIGNATION

5.1 - DIL 28



5.2 - LCCC 32



6 - ORDERING INFORMATION

6.1 - Hi-REL product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Class	Drawing number
EF4442JMG/B*	NFC 96883	Cerdip 28	−55 / +125	G	Data sheet
EF4442CMB/G (obsolete)	NFC 96883	DIL 28 Side Brazed	−55 / +125	G	Data sheet
EF4442C1MB/C (obsolete)	MIL-STD-883	DIL 28	−55 / +125	B	Data sheet
EF4442JMB/C*	MIL-STD-883	Cerdip 28	−55 / +125	B	Data sheet
EF4442DESC01XA	DESC	Cerdip 28	−55 / +125	B	5962-90719

* Preferred package.
LCC package available on request.

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

APPLICATION NOTE

GENERAL APPLICATION PRINCIPLES
EF 4442 (RTA)

SUMMARY

1 · PROCEDURE FOR EXCHANGE OF DATA BETWEEN A MICROPROCESSOR AND EF 4442 ARINC 429 CIRCUIT (RTA) WHEN OPERATING IN A MODE.

In A mode, the EF 4442 operates in receiver and transmit per modes. Thus there are two possible transfer directions :

– the microprocessor can receive data from the EF 4442 on one of four receiver lines of an ARINC 429 line. In this case, the microprocessor reads the buffers register of the channel in question,

– the microprocessor can send data to the EF 4442, which will transmit it over its transmit line on an ARINC 429 line. In this case, the microprocessor writes into the transmit channel shift register.

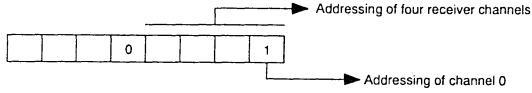
1.1 · Receiver mode

Data is received by the circuit on one of four receiver channels and is accessible to the microprocessor in the buffer register of this channel.

Let us assume that the EF 4442 occupies the four addresses from $F800 to $F803. In this case, the chip select signal CS is obtained by decoding the 14 most significant bits on the address bus.

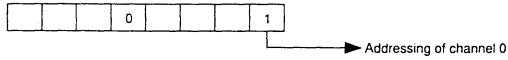
The microprocessor executes the following sequence :

(1) It programs the label.
It writes the control register at $F801 :

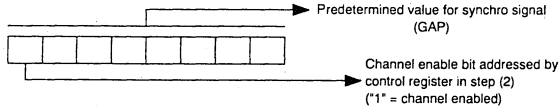


It writes the 8-bit label of the data to be received on the channel addressed by the control register at address $F803.

(2) It writes the control register at $F801 :



(3) It writes the synchro enable register at $F800 :



The EF 4442 then compares the first 8-bits received on the addressed channel with the label which has been programmed. It also checks the parity if the parity check is enabled.

If there is coincidence, the other 24 data bits are transferred into the 24 bit buffer register for the considered channel.

The status bit corresponding to this channel is then set to «1».

If the channel is enabled, interrupts are also enabled and the interrupt sequence is as follows :

– the control register is written at $F801 to address the considered channel,

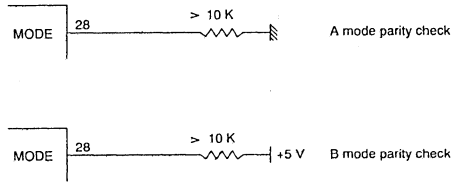
– the first byte of the channel buffer register is read at $F800,

– the second byte of the channel buffer register is read at $F801,

– the third and last byte of the channel buffer register is read at $F802 and the status bit corresponding to the channel is then reset to 0.

Parity check

To enable the parity check, the MODE pin of the EF 4442 must see a high impedance (typically not less than 10 kΩ) :



When the parity check is enabled, if the number of «1»'s received in a message is even, transfer does not take place and the message is ignored.

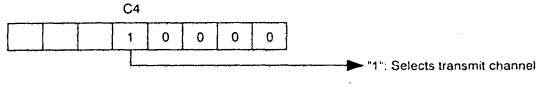
If the MODE pin is connected directly to the +5 V supply in B mode (or to ground in A mode), the parity check is disabled.

1.2 - Transmit mode

In the transmit mode, the microprocessor loads four data bytes into the shift register of the EF 4442 transmit channel.

The microprocessor executes the following sequence :

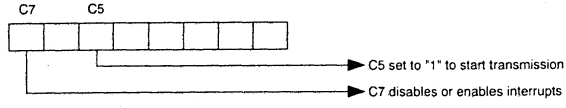
- the value selected for the «divide by n» circuit (the transmit frequency will be ϕ / n) is written at $F801,
- the control register is written at $F801 :



- the first byte (label) is written at $F803,
- the second byte is written at $F803,
- the third byte is written at $F803,
- the fourth byte is written at $F803.

The four bytes are then loaded into the shift register and the microprocessor can begin the corresponding transmission.

- the control register is written at $F801 :



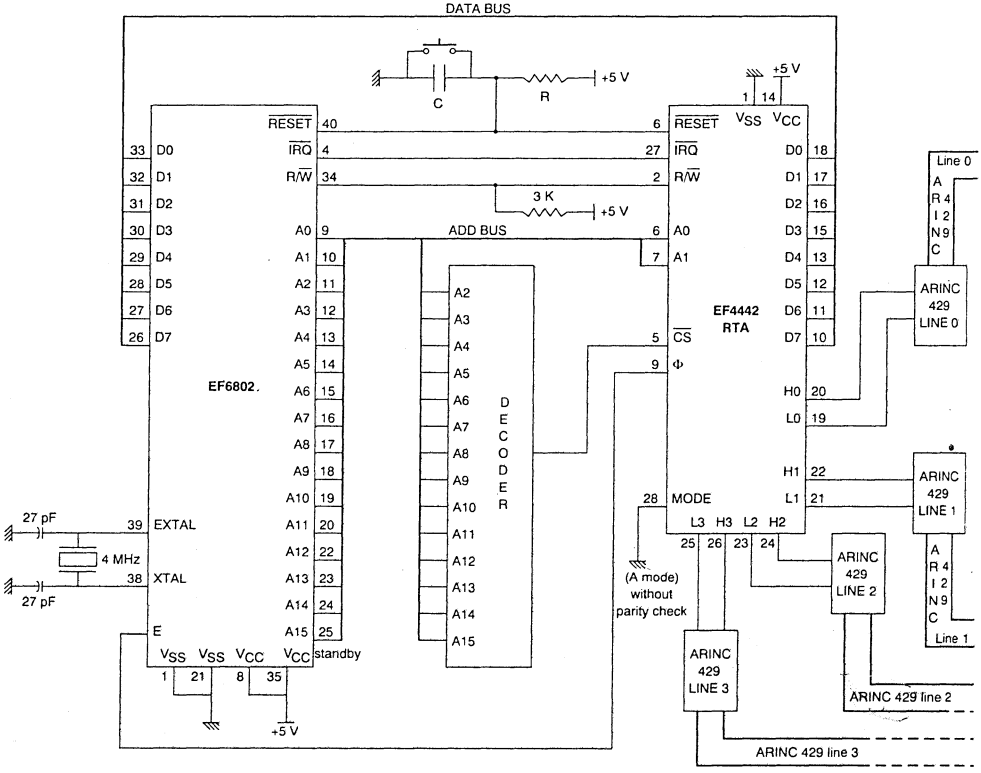
When the 32nd bit has been sent, C5 is reset to «0» and status register bit S4 is set to «1». Status register bit S7 is set to «1» throughout transmission of the 32 bits of the message.

If C7 : «0», IRQ is activated.
If C7 : «1», IRQ is disabled.

If bit C5 is set to «1» again after transmission of the 32nd bit, the message is retransmitted after four periods of the transmit clock.

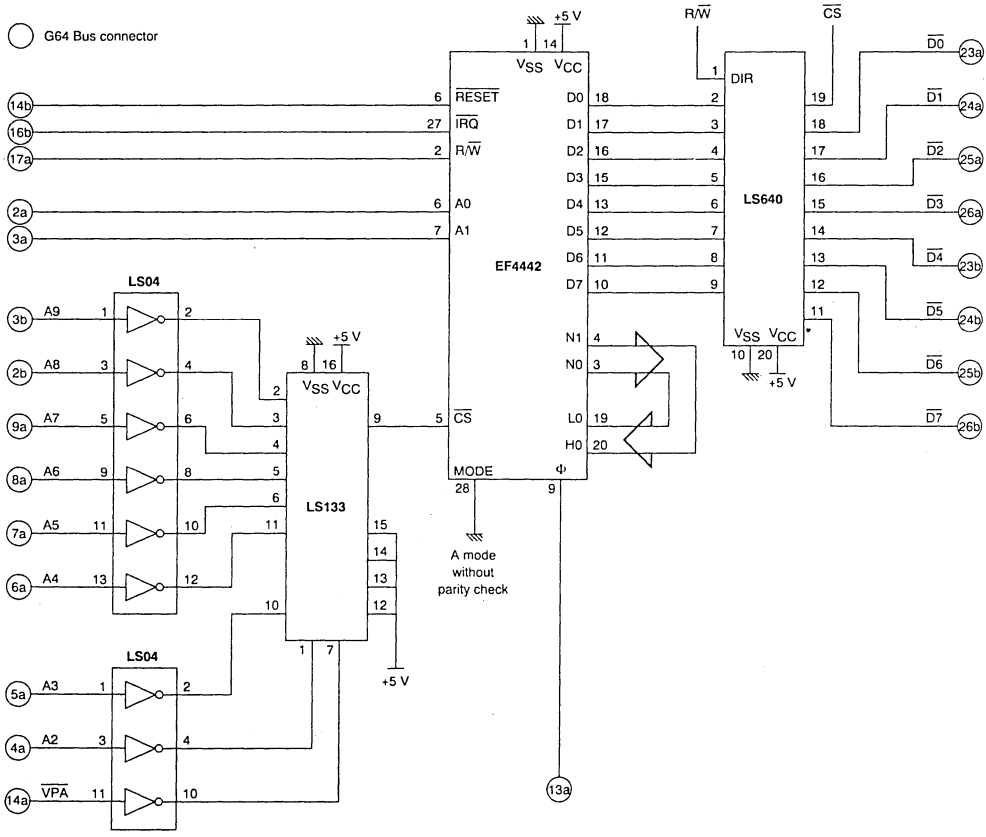
Note : Bit S4 of the status register is reset to «0» on any write mode access to the internal register of transmit channel.

1.3 - Connecting the EF 4442 circuit to the microprocessor



5

1.4 - EF 4442 circuit connection to the G64 bus



2 - EXAMPLE OF USE OF EF 4442 IN A MODE

2.1 - Introduction

Program RTAPROG shows how to program the EF 4442 in transmitter and receiver modes (see annexe 1).

Schematic shows the hardware configuration required to run this program. The «0» and «1» lines N0, N1 of the transmitter channel of the EF 4442 are connected to the «0» and «1» lines L0, H0 of receive channel 0.

The program requests the microprocessor to send a 32 bit data word to the EF 4442 for transmission.

This data will therefore be present on the receive channel of the circuit. The microprocessor will then read what the circuit receives. Thus, it remains to verify whether the data received corresponds to what was sent.

Important note

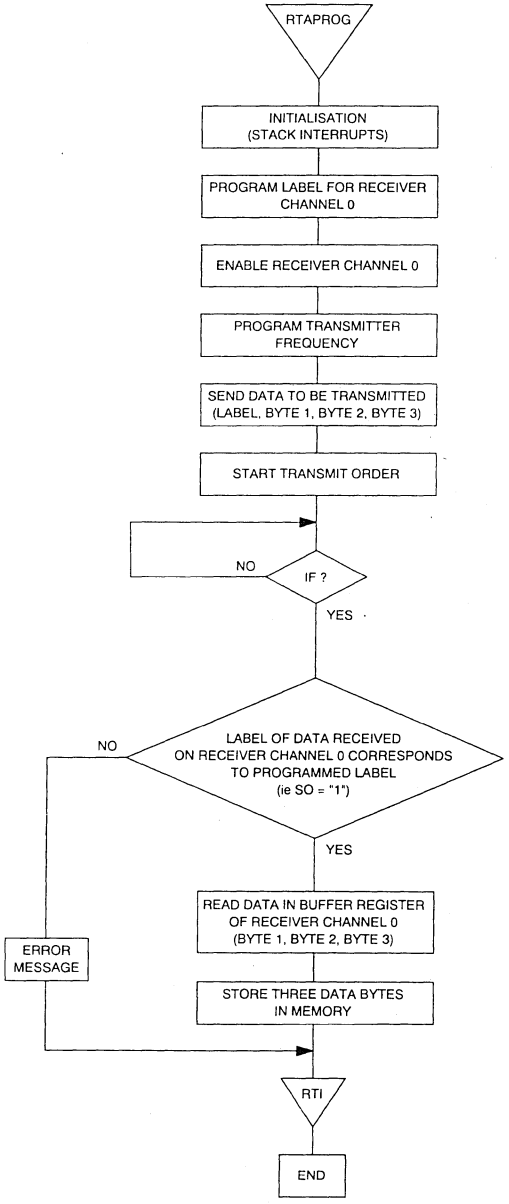
The EF 4442 can transmit data it has just received without connecting the transmit channel to a receiver channel, by using test mode.

In test mode bit C6 of the control register is associated with bit C5. They must be programmed at the same time.

During the seventh stage of the transmitter sequence C6 and C5 are therefore set to «1» and the signal generated by the transmitter channel is switched in the circuit at the input to the receiver channel selected by the control register.

Bit C6 is involved only in the internal loopback of the transmission to one receive channel. C6 is reset to «0» on any write operation in the control register.

ANNEXE 1 : RTAPROG FLOW CHART - A MODE



3 - OPERATION OF EF 4442 IN B MODE

In B mode, parameters are hardwired. It is possible to read only registers containing messages. Thus the EF 4442 operates in receiver mode only.

In this mode, there is no label ckeck. All bits in the receiver register are transferred into the label register and the 24-bit buffer register.

The EF 4442 can operate with parity check enabled, in the same way as in A mode.

In this case, outputs NO and N1 are the outputs of a counter which divides by four and is incremented by signal ∅. This addresses the four chanels consecutively when the circuit is selected.

If (A1 A0) = (11), the label of the channel addressed by the counter is then available on the data bus and the number of the channel is available on outputs N1, N0.

The forcing of input (R / $\overline{W}$) / INH to «1» disables the counter dividing by 4. If the circuit is selected the 3 bytes contained in the buffer of the channel may be set on the bus by addressing them by means of A1, A0.

A1	A0	
0	0	RT1
0	1	RT2
1	0	RT3
1	1	LABEL

(A1 A0) at (11) forces the label register of the channel to «0». Transfer from the receiver register to the buffer register is disabled, as in A mode.

TS 68C429A

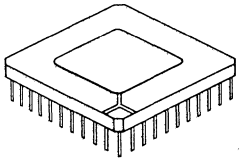
CMOS ARINC 429 MULTICHANNEL RECEIVER/TRANSMITTER (MRT)

DESCRIPTION

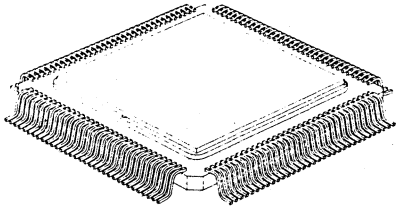
The TS 68C429A is an ARINC 429 controller. It is an enhanced version of the EF 4442 and it is designed to be connected to the new 16 or 32 bit microprocessors, especially these of the TCS TS 68xxx family.

MAIN FEATURES

- 8 independent receivers (Rx).
- 3 independent transmitters (Tx).
- Full 68xxx microprocessor interface compatibility.
- 16 bit data-bus.
- ARINC 429 interface : «1» & «0» lines, RZ code.
- Support all ARINC 429 data rate transfer and up to 2.5 Mbit/s.
- Multi label capability.
- Parity control : odd, even, no parity, interrupt capability.
- Independent programmable frequency for Rx and Tx channels.
- 8 messages FIFO per Tx channel.
- Independant interrupt request line for Rx and Tx functions.
- Vectored interrupts.
- Daisy chain capability.
- Direct addressing of all registers.
- Test modes capability.
- 20 MHz operating frequency.
- Self-test capability for receiver label memories and Transmit FIFO.
- Low power : 400 mW.



R suffix
PGA 84
Ceramic Pin Grid Array



F suffix
CQFP 132
Ceramic Quad Flat Pack

SCREENING

- MIL-STD-883, class B.
- DESC.
- TCS Standard.

APPLICATION NOTE

- See chapter 7.
- A detailled application note is available «AN 68C429A» on request.

SUMMARY

A - GENERAL DESCRIPTION

1 - HARDWARE OVERVIEW

The TS 68C429A is a high performance ARINC 429 controller designed to interface primary to the TCS TS 68xxx family microprocessor in a straight forward fashion (see application note chapter 7). It can be connected to any 68xxx processor family with asynchronous bus with some additionnal logic in some cases.

As shown in Figure 1, the TS 68C429A is divided in 5 mains bocks, the microprocessor interface unit (MIU), the logical control unit (LCU), the interrupt control unit (ICU), the receiver channel unit (RCU) and the transmitter channel unit (TCU).

- The MIU handles the interface protocol of the host processor. Through this unit, the host sees the TS 68C429A as a set of registers.
- The LCU controls the internal data flow and initializes the TS 68C429A.
- The ICU manages one interrupt line for the RCU and one for the TCU. Each of these 2 parts has a daisy chain capability. All channels have a dedicated vectored interrupt answer. Receiver channels prority is programmable.
- The RCU is composed of 8 ARINC receiver channels made of :
  - a serial to parallel converter to translate the 2 serial signals (the «1» and «0» in RZ code) into 2 16 bit words,
  - a memory to store the valid labels,
  - a control logic to check the validity of the received message,
  - a buffer to keep the last valid received message.
- The TCU is composed of 3 ARINC transmitter channels made of :
  - a parallel to serial converter to translate the messages into 2 serial signals (the «1» and «0» in RZ code),
  - a FIFO memory to store eight 32 bit ARINC messages,
  - a control logic to synchronize the message transmitter (parity, gap, speed,...).
- Test facility : Rx inputs can be internally connected to TX3 output.
- Self-test facility : The receiver control label matrix and transmitter FIFO can be tested. This self-test can be used to verify the integrity of the TS 68C429A memories.

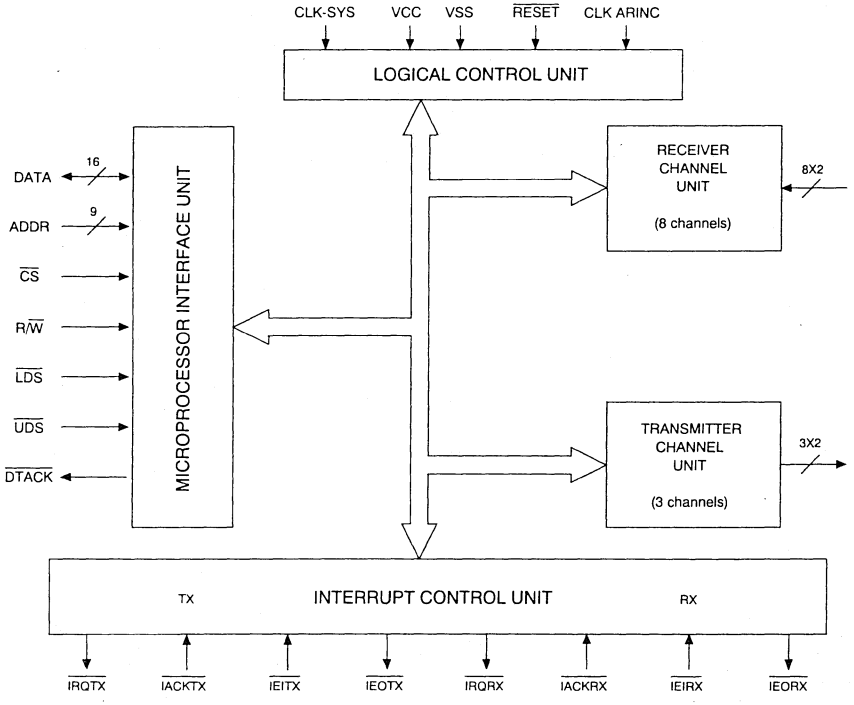


Figure 1 : Simplified block diagram.

2 - PACKAGE

See § B.10 and B.11.

3 - SIGNAL DESCRIPTION

Figure 2 illustrates the functional signal groups.

Pin Name	Type	Function
A0-8	I	Address bus. The address bus is used to select one of the internal registers during a processor read or write cycle.
D0-15	I/O	This bidirectional bus is used to receive data from or transmit data to an internal register during a processor read or write cycle. During an interrupt acknowledge cycle, the vector number is given on the lower data bus (D0-D7).
$\overline{CS}$	I	Chip select (active low). This input is used to select the chip for internal register access.
$\overline{LDS}$	I	Lower data strobe. This input (active low) validates lower data during R/$\overline{W}$ access (D0-D7).
$\overline{UDS}$	I	Upper data strobe. This input (active low) validate upper data during R/$\overline{W}$ access (D8-D15).
R/$\overline{W}$	I	Read / write. This input defines a data transfer as a read (high) or a write (low) cycle.
$\overline{DTACK}$	O	Data transfert acknowledge. If the bus cycle is a processor read, the chip asserts $\overline{DTACK}$ to indicate that the information on the data bus is valid. If the bus cycle is a processor write, $\overline{DTACK}$ acknowledges the acceptance of the data by the MRT. $\overline{DTACK}$ will be asserted during chip select access ($\overline{CS}$ asserted) or interrupt acknowledge cycle ($\overline{IACKTX}$ or $\overline{IACKRX}$ asserted).
$\overline{IRQTX}$	O	Interrupt transmit request. This open drain output signals to the processor that an interrupt is pending from the transmission part of the MRT. There are 6 causes that can generate an interrupt request (2 per channel : FIFO empty and end of transmission).
$\overline{IACKTX}$	I	Interrupt transmit acknowledge. If $\overline{IRQTX}$ is active, the MRT will begin an interrupt acknowledge cycle. The MRT will generate a vector number to the processor which is the highest priority channel requesting interrupt service.
$\overline{IEITX}$	I	Interrupt transmit enable in. This input, together with $\overline{IEOTX}$ signal, provides a daisy chained interrupt structure for a vectored interrupt scheme. $\overline{IEITX}$ (active low) indicates that no higher priority device is requesting interrupt service.
$\overline{IEOTX}$	O	Interrupt transmit enable out. This output, together with $\overline{IEITX}$ signal, provides a daisy chained interrupt structure for a vectored interrupt scheme. $\overline{IEOTX}$ (active low) indicates to lower priority devices that neither the TS 68C429A not any highest priority peripheral is requesting an interrupt.
$\overline{IRQRX}$	O	Interrupt transmit request. This open drain output signals to the procesor that an interrupt is pending from the receiving part of the chip. There are 9 causes that can generate an interrupt request (1 per channel : valid message received, and 1 for bad parity on a received message).
$\overline{IACKRX}$	I	Interrupt receive acknowledge. Same function as $\overline{IACKTX}$ but for receiver part.
$\overline{IEIRX}$	I	Interrupt receive enable in. Same function as $\overline{IEITX}$ but for receiver part.
$\overline{IEORX}$	I	Interrupt receive enable out. Same function as $\overline{IEOTX}$ but for receiver part.

TX1H	O	Transmission «1» line of the channel 1.
TX1L	O	Transmission «0» line of the channel 1.
TX2H	O	Transmission «1» line of the channel 2.
TX2L	O	Transmission «0» line of the channel 2.
TX3H	O	Transmission «1» line of the channel 3.
TX3L	O	Transmission «0» line of the channel 3.
RX1H	I	Receiving «1» line of the channel 1.
RX1L	I	Receiving «0» line of the channel 1.
RX2H	I	Receiving «1» line of the channel 2.
RX2L	I	Receiving «0» line of the channel 2.
RX3H	I	Receiving «1» line of the channel 3.
RX3L	I	Receiving «0» line of the channel 3.
RX4H	I	Receiving «1» line of the channel 4.
RX4L	I	Receiving «0» line of the channel 4.
RX5H	I	Receiving «1» line of the channel 5.
RX5L	I	Receiving «0» line of the channel 5.
RX6H	I	Receiving «1» line of the channel 6.
RX6L	I	Receiving «0» line of the channel 6.
RX7H	I	Receiving «1» line of the channel 7.
RX7L	I	Receiving «0» line of the channel 7.
RX8H	I	Receiving «1» line of the channel 8.
RX8L	I	Receiving «0» line of the channel 8.
$\overline{\text{RESET}}$	I	This input (active low) will initialize the TS 68C429A registers.
V_{CC}/GND	I	These inputs supply power to the chip. The V_{CC} is powered at +5 volts and GND is the ground connection.
CLK-SYS	I	The clock input is a single-phase signal used for internal timing of processor interface.
CLK-ARINC	I	This input provides the timing clock to synchronize received/transmitted messages.

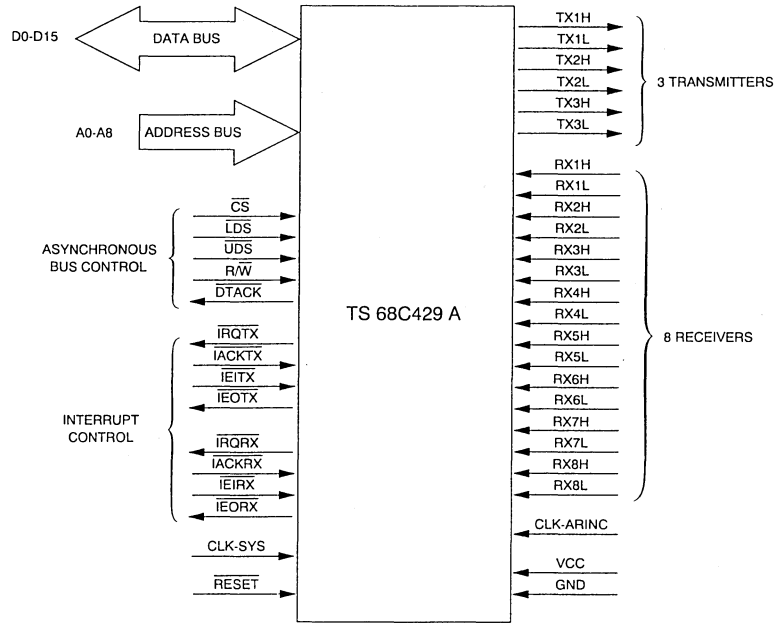


Figure 2 : Functional signal groups.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the ARINC multi channel receiver / transmitter, in compliance either with MIL-STD-883 class B or SMD drawing.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38535 : general specifications for microcircuits.
3) MIL-STD-1835 microcircuit case outlines.
4) DESC / SMD : T.B.D.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections is detailled in § B.11.

3.2.2 · Package

The circuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 (when defined) :

- PGA 84,
- CQFP 132.

The precise case outlines are described at the end of the specification (chapter 10) and into MIL-STD-1835.

3.2.3 · Special recommanded conditions for C.MOS devices

a) CMOS latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a parasitic semiconductor controlled rectifier (SCR) formed and may be triggered when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become «latched» in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients ; others may require no additional circuitery.

b) CMOS / TTL levels

The TS 68C429A doesn't satisfy totaly the input / output drive requirements of TTL logic devices, see Table 4.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_{dmax}	Max Power dissipation			400	mW
T_{case}	Operating temperature	M suffix	−55	+125	°C
		V suffix	−40	+85	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

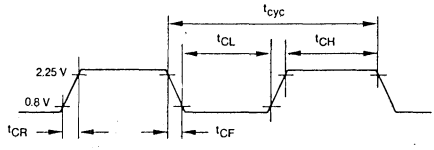
3.3.2 · Recommended condition of use

Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 2

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_{IL}	Low level input voltage		−0.5	0.8	V
V_{IH}	High level input voltage		2.25	5.8	V
T_{case}	Operating temperature	M suffix	−55	+125	°C
		V suffix	−40	+85	°C
C_L	Output loading capacitance			130	pF
$t_{r(c)}$	Clock rise time (see Figure 3)			5	ns
$t_{f(c)}$	Clock fall time (see Figure 3)			5	ns
f_c	Clock system frequency (see Figure 3)		0.5	20	MHz

This device contains protective circuitry against damage due to high static voltages or electrical fields : however, it is advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).



Note : Timing measurements are referenced to and from a low of 0.8 volt and a high voltage of 2.25 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be lineat between 0.8 volt and 2.25 volts.

Figure 3 : Clock input timing diagram.

3.4 · Thermal characteristics

Table 1

Package	Symbol	Parameter	Value	Unit
PGA 68	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	28	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	2	°C/W
CQFP 132	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	27	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	3	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environnement

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or DESC devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo,
- Manufacturer's part number,
- Class B identification,
- Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Tables 4, 5 : Static electrical characteristics for the electrical variants.
- Table 6, 7, 8 : Dynamic electrical characteristics.

For static characteristics (Tables 4, 5), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Tables 6, 7, 8), test methods refer to clause 5.5 of this specification.

5.2 - DC electrical characteristics

Table 4

With $-55°C \leqslant T_{case} \leqslant +125°C$ or $-40°C \leqslant T_{case} \leqslant +85°C$; $V_{CC} = 5\ V \pm 10\ \%$.

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	2.25	$V_{CC}+0.3$	V
V_{IL}	Input low voltage	−0.5	0.8	V
V_{OH}	Output high voltage (except $\overline{IRQRX}$, $\overline{IRQTX}$: open drain outputs)	2.7		V
V_{OL}	Output low voltage		0.5	V
I_{OH}	Output source current (except $\overline{IRQRX}$, $\overline{IRQTX}$: open drain outputs) (V_{out} = 2.7 V)		−8	mA
I_{OL}	Output sink current (V_{out} = 0.5 V)		8	mA
I_{LI}	Input leakage current (V_{in} = 0 to V_{CC})		±20	µA
IDD	Dynamic current (see Note) ($T_{case} = T_{min}$ - $V_{DD} = V_{max}$)		65	mA

Note : IDD is measured with all I/O pins at 0 V, all input pins at 0 V except signals $\overline{CS}$, $\overline{IACKxx}$, $\overline{LDS}$, $\overline{UDS}$ at 5 V and CLK-SYS and CLK-ARINC which run at t_{cyc} mini.

5.3 - Capacitance (T_A = 25°C)

Table 5

Symbol	Parameter	Max	Unit
C_{in}	Input capacitance	10	pF
C_{out}	Hi-Z output capacitance	20	pF

5.4 - Clock timing

5.4.1 - Clock system (CLK SYS)

Table 6

Symbol	Parameter	Min	Max	Unit
t_{cyc} S	Clock period	50	2000	ns
t_{CLS}, t_{CHS}	Clock pulse width	20		ns
t_{crS}, t_{cfS}	Rise and fall times		5	ns

5.4.2 - Clock ARINC (CLK ARINC)

Table 7

Symbol	Parameter	Min	Max	Unit
t_{cyc} A	Cycle time - see Note	200	8000	ns
t_{CLA}, t_{CHA}	Clock pulse width	240		ns
t_{crA}, t_{cfA}	Rise and fall times		5	ns
Note : t_{cyc} A $\geq 4 \times t_{cyc}$ S.				

5.5. - AC electrical characteristics

With V_{CC} = 5 V_{DC} ±10 % V_{SS} = 0 V_{DC}.

$\overline{IEIxx}$, $\overline{IEOxx}$, $\overline{IACKxx}$, must be understood as generic signals (xx = RX and TX).

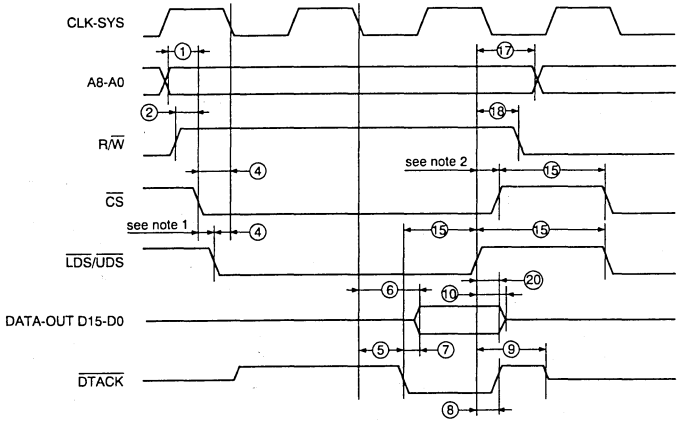


Figure 4a : Read cycle.

Note 1 : $\overline{LDS}/\overline{UDS}$ can be asserted on the next or previous CLK-SYS period after $\overline{CS}$ goes low but ④ must be met for the next period.

Note 2 : The cycle ends when the first of $\overline{CS}$, $\overline{LDS}/\overline{UDS}$ goes high.

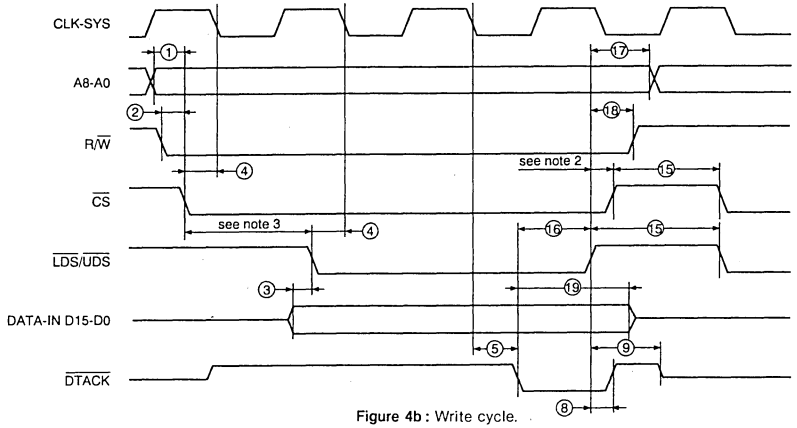


Figure 4b : Write cycle.

Note 3 : $\overline{LDS}/\overline{UDS}$ can be asserted on the same or previous CLK-SYS period as $\overline{CS}$ but ③ and ④ must be met.

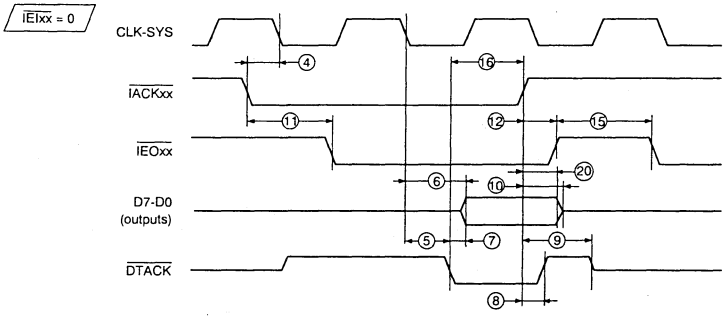
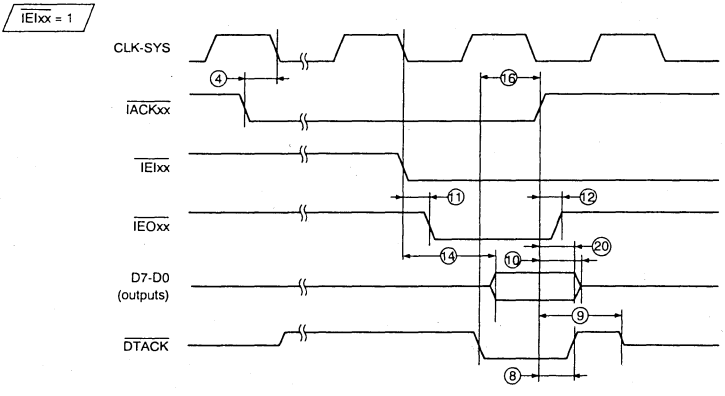


Figure 5 : Interrupt cycle (IEIxx = 0).

Note :

- If $\overline{UDS}$ = 1, D15-D8 stay hi-z else D15-D8 drive the bus with a stable unknown value.
- If $\overline{IEOxx}$ goes low, neither vector nor $\overline{DTACK}$ are generated, else $\overline{IEOxx}$ stays inactive and a vector is generated (D7-D0 and $\overline{DTACK}$).



See note on Figure 5.

Figure 6 : Interrupt cycle (IEIxx = 1).

Table 6

N°	Symbol	Parameter	Min	Max	T/G see Note	Unit
1	t_{AVCSL}	Address valid to $\overline{CS}$ low	0	–	T	ns
2	t_{RWVCSL}	R/W valid to $\overline{CS}$ low	0	–	T	ns
3	t_{DIVDSL}	Data in valid to $\overline{LDS}/\overline{UDS}$ low	0	–	T	ns
4	t_{SVCL}	CS, $\overline{LDS}/\overline{UDS}$, $\overline{IACKxx}$ valid to CLK-SYS low	5	–	T	ns
5	t_{CLDKL}	CLK-SYS low to $\overline{DTACK}$ low	–	45	T	ns
6	t_{CLDOV}	CLK-SYS low to data out valid	–	50	T	ns
7	t_{DKLDOV}	$\overline{DTACK}$ low to data out valid	–	10	G	ns
8	t_{SHDKH}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to $\overline{DTACK}$ high	–	35	G	ns
9	t_{SHDXZ}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to $\overline{DTACK}$ hi-z	–	50	G	ns
10	t_{SHDOZ}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to data out hi-z	–	25	G	ns
11	t_{ILIOL}	$\overline{IEIxx}$ or $\overline{IACKxx}$ low to $\overline{IEOxx}$ low	–	35	T	ns
12	t_{IKHIOH}	$\overline{IACKxx}$ high to IEOxx high	–	40	T	ns
13	t_{IILDKL}	$\overline{IEIxx}$ low to $\overline{DTACK}$ low	–	40	T	ns
14	t_{IILDOV}	$\overline{IEIxx}$ low to data out valid	–	45	T	ns
15	t_{SH}	$\overline{CS}$, $\overline{IACKxx}$, $\overline{LDS}/\overline{UDS}$ inactive time	15	–	T	ns
16	t_{DKLSH}	$\overline{DTACK}$ low to $\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high	0	–	G	ns
17	t_{SHAH}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ high to adress hold time	0	–	G	ns
18	t_{SHRWI}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ high to $\overline{R/W}$ invalid	0	–	G	ns
19	t_{DKLDIH}	$\overline{DTACK}$ low to data in hold time	0	–	G	ns
20	t_{SHDOH}	$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high data out hold time	0	–	G	ns

Note : T/G = Tested / Guaranteed.

6 - FUNCTIONAL DESCRIPTION

6.1 - Receiver Channel Unit (RCU)

6.1.1 - Overview

The RCU is composed of 8 ARINC receiver channels and has per channel :

- a serial to parallel converter to translate the 2 serial signals in 2 16 bit words,
- a memory to store the authorized labels,
- a control logic to check the validity of the received message,
- a buffer to keep the last valid received message.

6.1.2 - Inputs

Each receiver channel has 2 input lines, receiving line high (RxiH) and receiving line low (RXiL) which are not directly compatible with the bipolar modulated ARINC line. This Arinc three-level state signals («HIGH», «NULL», «LOW») should be demultiplexed to generate the two RZ lines according to Figure 7.

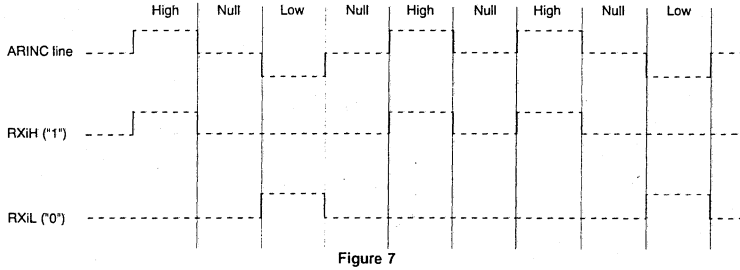


Figure 7

6.1.3 · Description

Each channel has a test mode in which the input signals (RXiH, RXiL) are internaly connected to the 3rd Transmit Channel Lines. This selection is done by programming the Test bit in the receiver control register (see register description) except this difference, the TS 68C429A behaves exactly the same manner in the 2 modes. The receiver channel block diagram is given in Figure 8.

ARINC signals beeing asynchronous, the RCU first rebuilds the received clock in order to transfer the data within the shift-register and when the Gap-controller has detected the end of the message, tests the message validity according to the criterra listed hereafter.

To detect the end of the message, the Gap-Controller waits for a Gap after the last received bit. To do so, at each CLK ARINC cycle, a counter is incremented and compared to the content of the Gap-Register which has the user programmed value. If both values are equal, the counter is stopped and an internal end of message signal is generated. This counter is reseted on the falling edge of the rebuilt clock. Figure 9 shows the gap detection principle.

When the end of message is detected, the TS 68C429A verifies the following points :

- the number of received bits must be 32,
- if requested the message parity (see register description) is compared to the parity bit of the message,
- the message label must be equal to one of the label stored in the Label Control Matrix,
- the Buffer is empty (that is : the last message has been read). The corresponding bit in the Status-register (see logical interface unit), has been cleared,
- when all these 4 conditions are met, the message is transfered from the Shift-register to the Buffer and the corresponding bit is set in the Status-register. If the interrupt mode is enabled (see general circuit control) the IRQRX line is activated.

If not, reception of a new message is enabled, see Note.

If only the message parity is incorrect, an interrupt can be generated (see register description § 6.1.4).

The Buffer is seen as a 2 sixteen bit word registers, the Most Significant Word of the message (MSW) is contained in the lower address, the Less Significant Word of the message (LSW) is contained in the upper address. The MSW should be read first because reading the LSW will release the buffer and allow transfert of a new message from the Shift-register.

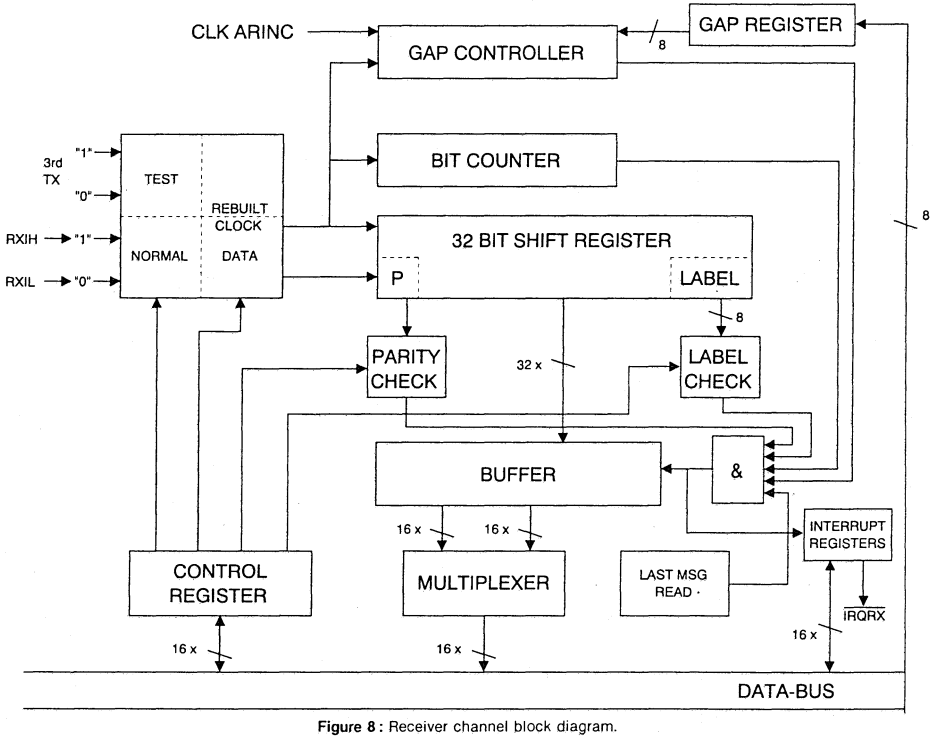


Figure 8 : Receiver channel block diagram.

Note : A valid message is stored in the Shift-Reg. until a new message arrives and so may be transfered to the message buffer as soon as the buffer is «freed».

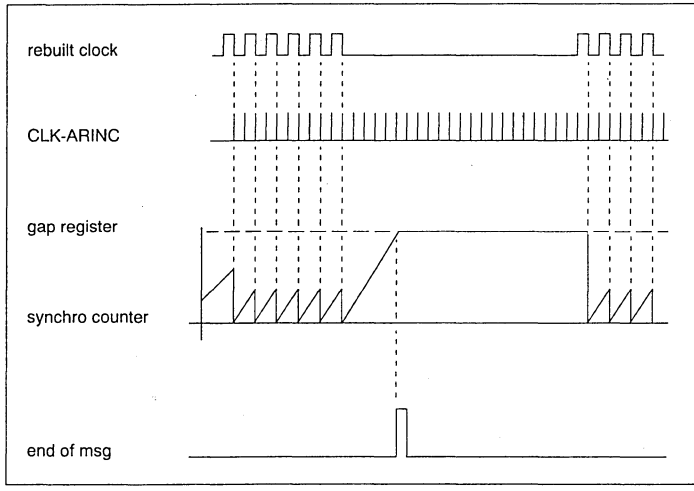


Figure 9

6.1.4 · Register description

Four registers are associated to each receiver channel. These four registers are :

a) receiver control.
b) gap register.
c) message buffer.
d) label control matrix.

6.1.4.1 · Receiver control register

This read / write register controls the function of the related receiver channel :

The lowest value will give the highest prioriy. If two channels have the same priority, one of them will never be able to send its interrupt vector to the microprocessor. Each channel must have a unique channel priority order.

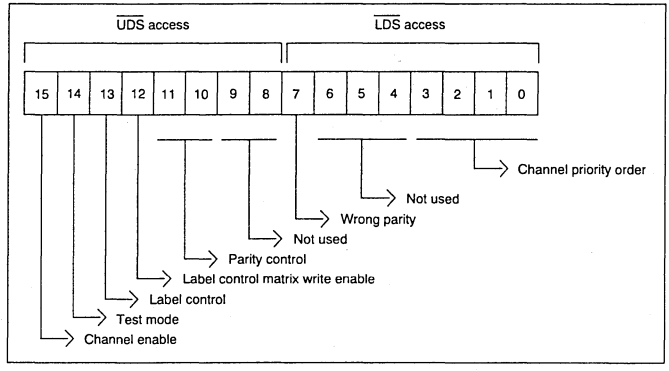


Figure 10

Table 9 - Receiver control register description

Bit	Function	Comments
Bit 15	Channel enable	0 : channel is out of service 1 : channel is in service
Bit 14	Test mode	0 : external ARINC lines as input (normal operation) 1 : third transmitter lines as input (test mode)
Bit 13	Label control	0 : no control, all the labels are accepted 1 : automatic check of the label according to the label control matrix
Bit 12	LCMWE label control matrix write enable	0 : receiving mode (write to the matrix are disabled) 1 : programmation mode for labels control matrix
Bit 11	Parity control	0 : even parity check 1 : odd parity check
Bit 10	Parity control	0 : parity check is disable 1 : parity check is enable
Bit 9 Bit 8	Not used Not used	
Bit 7	Wrong parity : this feature is enable only if self-test register bit 0 is set to 1	0 : received message parity is correct if read, reset wrong wrong parity flag if written. 1 : an incorrect received message parity has been detected (the corresponding message is lost) (set by hardware).
Bit 6 Bit 5 Bit 4	Not used Not used Not used	
Bit 0 to 3	Channel priority : order	The lowest value will give the highest priority. Each channel must have a unique channel priority order. If several messages are pending, the interrupt vector will account for highest priority channel.

5

6.1.4.2 - Gap register (Figure 11)

The gap register is accessible for writing operations only. It contains the value on which the gap counter will be stopped and will generate the end of the message signal (see § 6.1.2). The value is interpreted as a multiple of the CLK ARINC period.

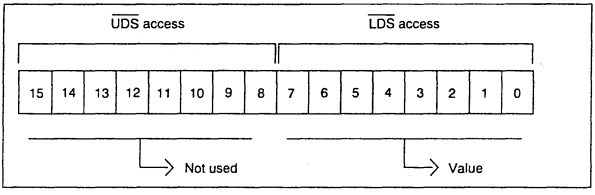


Figure 11 : Gap register description.

The value of the gap register must be chosen so as to generate the end of the message before the minimal gap as defined in the ARINC-429 norm.

6.1.4.3 - Message buffer

The Buffer is made of 2 16-bit registers, the Most Significant Word of the message (MSW) is contained in the lower address register, the Least Significant Word of the message (LSW) is contained in the upper address register. For a correct behaviour, the MSW must be read before the LSW. They are accessible in read mode only and 16 bit access is mandatory.

6.1.4.4 - Label control matrix

The label control matrix is a 256 x 1 bit memory. There is one memory per channel.

The address is driven by the incoming label, the output data is used to validate this incoming message label (see Figure 12). To program this matrix, the LCMWE (label control matrix write enable) bit of the receiver-control-register should be set to «1» to allow the access. At this time, the address is driven by the external address bus and the data are written from the data bus D7 to D0 (one per channel according to Figure 13). Any write to a matrix on which the LCMWE is not set won't have any effect. The label control matrix can be written or read in byte and word mode. In word mode, the state of D15-D8 is unknown. After complete programming of the matrix, the LCMWE bit should be reset to «0» to allow normal receiving mode. A «1» in the memory means that this label is allowed and a «0» means that this label must be ignored.

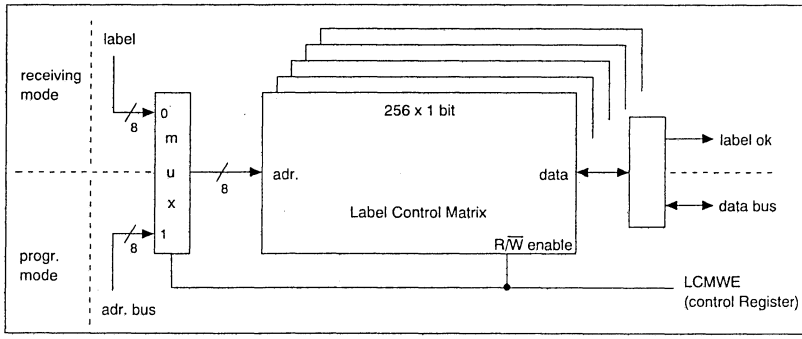


Figure 12

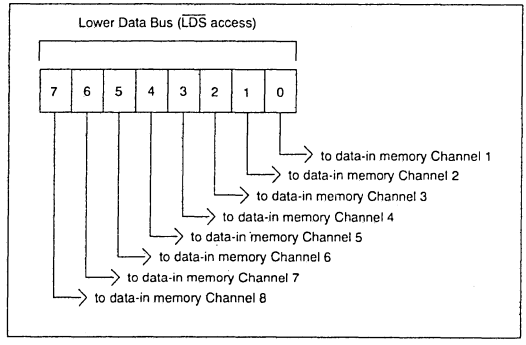


Figure 13

6.2 - Transmitter Channel Unit (TCU)

6.2.1 - Overview

The TCU is composed of 3 ARINC transmit channels and has per channel :

- a parallel to serial converter to translate the messages into 2 serial signals,
- a FIFO memory to store eight 32 bit ARINC messages,
- a control logic to synchronize the message transmitter (parity, gap, speed...).

6.2.2 - Outputs

Each transmitter channel has 2 output lines, Transmit line High (TXiH) and Transmit line Low (TXiL) which are not directly compatible with the bipolar modulated ARINC line. These two RZ format lines should be translated by an outside device into ARINC three-level state signal according to Figure 14.

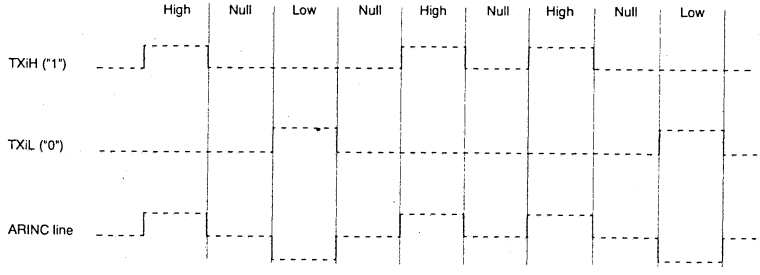


Figure 14

6.2.3 · Description

The block diagram of a transmit channel is given in Figure 15. Only the 3rd channel can be switched to internal lines for test mode, otherwise the channels are identical. The selection of this test mode is done by programming the test bit in the transmitter-control-register (see register description). In this test mode the lines TX3H and TX3L are not driven, they are both kept at «0».

The transmit frequency is generated by dividing the ARINC clock signal (CLK ARINC) by the value contained in the frequency register. This divided clock synchronizes the shift register which sends the 32 bit word on the lines TXiH and TXiL.

The parity is computed and if requested (see register description) the parity bit (32th bit of the message) is modified to have an odd number of «1» in the 32 bit message for odd parity or an even number of «1» in the 32 bit message for even parity.

A gap control block generates a gap between the sent messages. The value of this gap is defined by the 5 bits «transmission gap» of the transmitter-control-register, it is given in number of ARINC bit (see register description).

A FIFO control block manages the messages to be sent. Up to 8 messages can be written into the FIFO. The FIFO is seen as a 2 sixteen bit memory words, the Most Significant Word of the message (MSW) is written in the lower address, the Least Significant Word of the message (LSW) is written in the upper address. The MSW should be written first. The access to the FIFO is 16 bits mandatory. The number of messages within the FIFO is indicated by a counter that can be read through the transmitter-control-register. This counter is incremented when the LSW is written and decremented when the message is transfered to the shift-register. The «Reset FIFO» bit is used to cancel messages within the FIFO. If a transmission is on going, the entire message will be sent. The «reset FIFO» bit remains active until written at 1 by the microprocessor. When the transmitter is disable during a transmission, the out going message is lost.

When the FIFO is empty, a bit is set in the status-register (see general circuit control). If the interrupt mode is enabled (see general circuit control) the $\overline{\text{IRQTX}}$ line is activated.

When the transmitter FIFO is empty and when no transmission is on going, the first write access to the FIFO has to be preceded by the following sequence : disable and enable transmission (see figure 35 : First FIFO access).

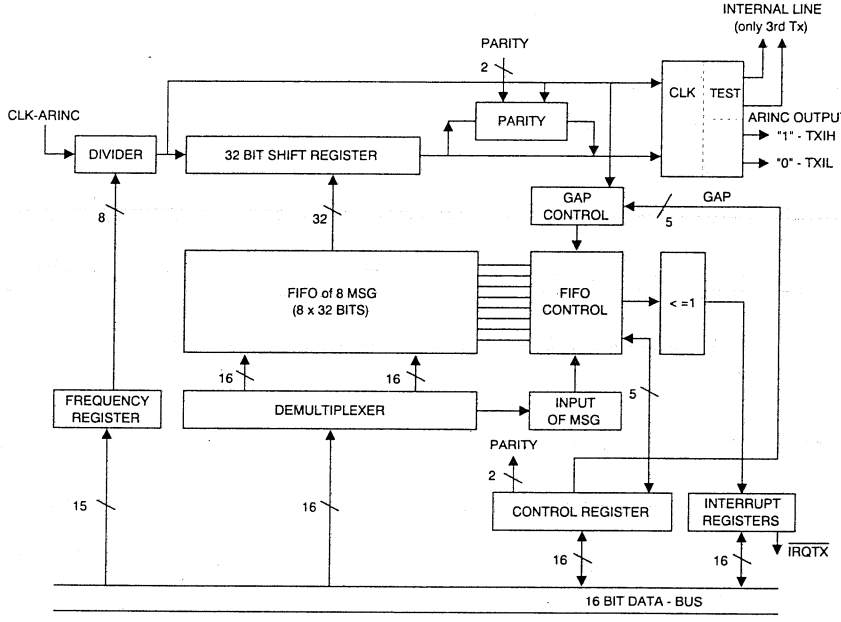


Figure 15 : Transmitter channel block diagram.

6.2.4 · Register description

Three registers are associated to each transmitter channel :

- the frequency register,
- the transmitter control register,
- the FIFO.

6.2.4.1 · The frequency register

The frequency register is only accessible for writing operations by the user and contains the frequency divider.

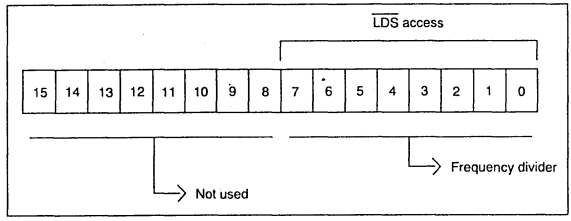


Figure 16 : Frequency register.

The transmission frequency can be computed by dividing the CLK ARINC frequency by the frequency register value. The frequency register must be loaded with a value greater or equal to 2.

6.2.4.2 · The transmitter control register

The transmitter control register is accessible for reading and writing operations.

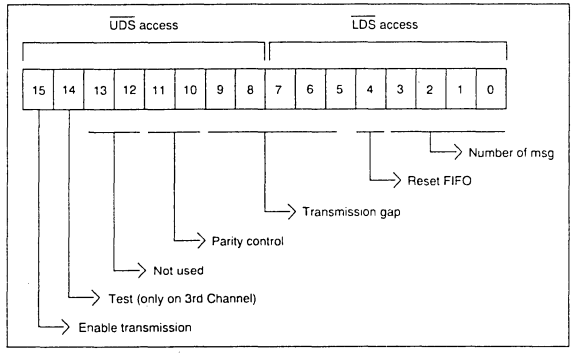


Figure 17 : Transmitter control register.

Table 10 · Transmission control register description

Bit	Function	Comments
Bit 15	Enable transmission	– 0 : channel out of service (stops on going transmission) – 1 : channel in service – 1 to 0 : transition is not allowed at the same time as an 1 to 0 transition of the bit 4 – when the transmitter FIFO is empty and when no transmission is on going, the first write access to the FIFO has to be preceded by the following sequence : reset to 0 and then set to 1
Bit 14	Test (only 3rd channel)	0 : normal operating 1 : test, output are only driven on internal lines for input testing
Bit 13 to 12	Not used	
Bit 11	Parity control	0 : even parity calculation 1 : odd parity calculation
Bit 10	Parity control	0 : parity disable. Bit 32 of the message stays unchanged 1 : parity enable. Bit 32 of the message will be forced by parity control
Bit 9 to 5	Transmission gap	«transmission gap» which is the delay between two 32 bit ARINC messages (in ARINC bit)
Bit 4	Reset FIFO	– write a 0 in this bit reset the FIFO counter – this bit must be set to 1 before any write in the transmit buffer. – 1 to 0 : transition is not allowed at the same time as an 1 to 0 transition of the bit 15
Bit 3 to 0	Number of msg	these four bits indicate the available space within the FIFO

6.2.4.3 - FIFO

The FIFO is seen as 2 16 bit words. The Most Significant Word (MSW) must be written first. The Least Significant Word (LSW) write incrementes the FIFO counter.

Before any write, the user should verify that the FIFO is not full. If the FIFO is full, any write to the FIFO will be lost.

6.3 - General circuit control

6.3.1 - Logical Control Unit (LCU)

The LCU mainly distributes the clocks and reset within the MRT. The reset signal, active low is an asynchronous signal. When it occurs, all registers are reset to zero except the Label-Control-Matrix which is not initialized and the Status-Register which is set to FC00 (hex). Reset duration must be greater than 4 clk-sys periods.

The LCU contains the Status-register. This read / write register indicates the state of the internal operations. It is also the image of the pending interrupts if they are not masked. Clearing a bit «RX-Channel-i» will cancel the received message and release the Message-buffer for reception of a new message. The «End of TX on channel-1» is cleared only when the involved channel FIFO is empty. The format of the Status-Register is given below.

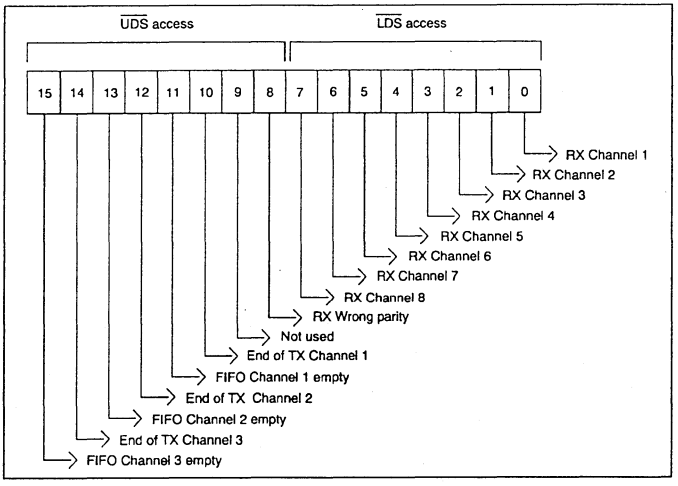


Figure 18 : Status register.

Table 11 - Description of LCU status register

Bit	Function	Comments
Bit 15, 13, 11	FIFO channel 3, 2, 1 empty	0 : FIFO not empty 1 : FIFO empty
Bit 14, 12, 10	End of transmission on channel 3, 2, 1	0 : Transmission occurs 1 : No transmission actually
Bit 8	RX wrong parity. This feature is available only if self-test register bit 0 is set to 1. This bit must be reset to 0 by user when needed.	0 : No wrong parity received. 1 : At least one receiver has received a message with wrong parity (set by hardware).
Bit 7, 6, 5, 4, 3, 2, 1, 0	Receiving channel 8, 7, 6, 5, 4, 3, 2, 1	0 : Waiting for message 1 : Received correct message

6.3.2 - Microprocessor Interface Unit (MIU)

This interface which is directly compatible with the TCS TS 68xxx family is based on an asynchronous data transfert.

The data exchange is mandotory on 16 bits for access to the FIFO messages (transmitter) and to the message buffer (receiver). For other access it can be on byte on D0-D7 with LDS assertion or on D8-D15 with UDS assertion.

Figures 19 and 20 show the read and write flow chart.

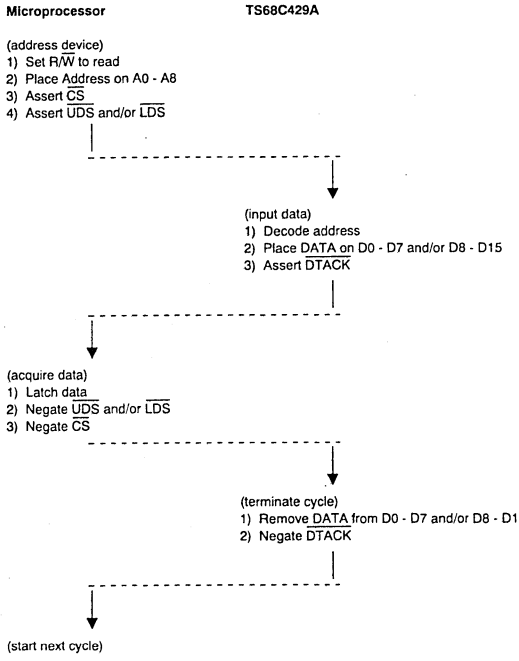


Figure 19 : Read cycle flow chart.

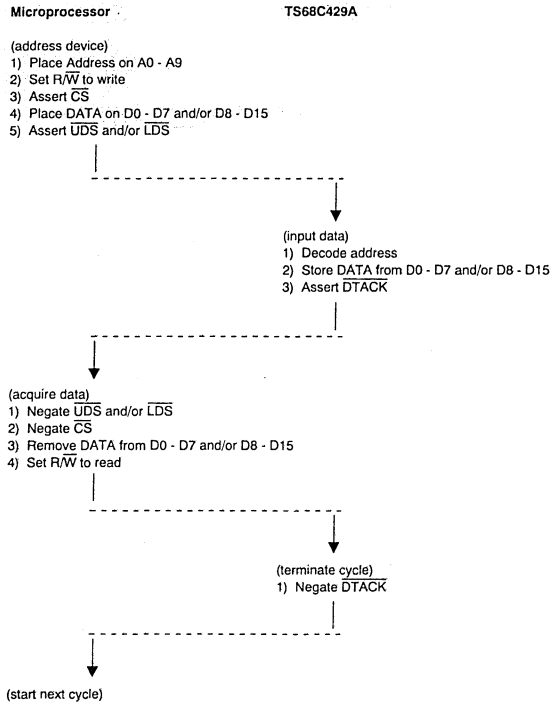


Figure 20 : Write cycle flow chart.

6.3.3 · Interrupt Control Unit (ICU)

6.3.3.1 · Daisy chain

The ICU is composed of 2 interrupt blocks with a daisy chain capability (transmitter and receiver blocks). The daisy chain allows more than one circuit to be connected on the same interrupt line. Figure 21 shows the use of a daisy chain. IRQxx, IACKxx, IEIxx, IEOxx must be understood as generic signals. They are IRQTX, IACKTX, IEITX, IEOTX for the transmitter block and IRQRX, IACKRX, IEIRX IEORX for the receiver block.

If IEIxx = 0, no higher device have an interrupt pending on the same line so the interrupt is requested and the IEOxx is forced high to disable lowest devices to generate interrupt. If IEIxx = 1 it waits for the condition IEIxx = 0. When IEIxx is tied high, IEOxx is forced high.

The daisy chains can be used to program a priority between receivers and transmitters interrupts when only one interrupt level is needed. An example is given in chapter 7.1 (Figure 29).

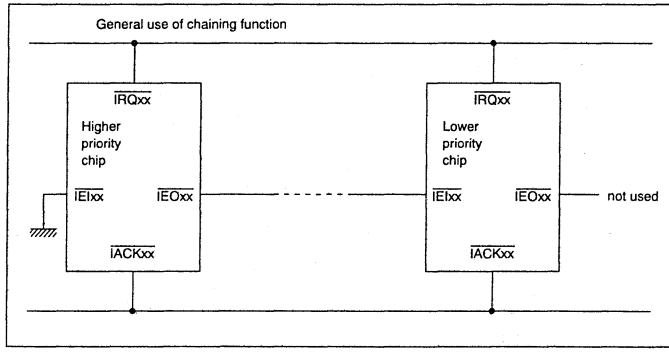


Figure 21

6.3.3.2 · Vectored interrupt

They are 15 possibilities to generate an interrupt and 2 lines to handle them. To be more efficient, a unique vector number for each cause is given to the microprocessor as an answer to an IRQ. Figure 22 shows the interrupt acknowledge sequence flow chart.

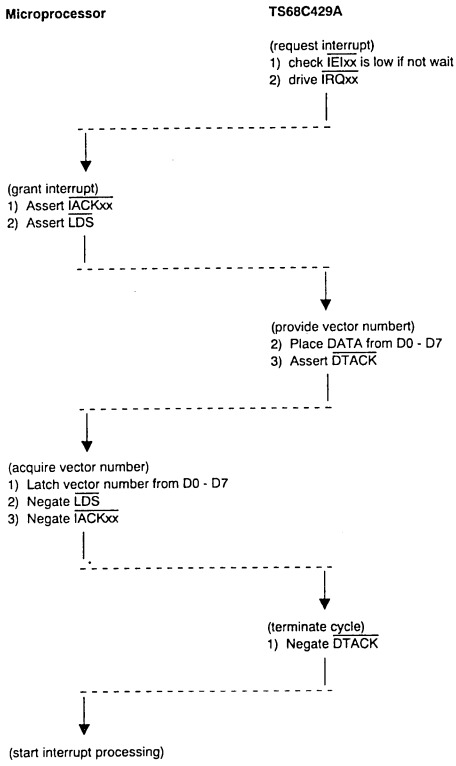


Figure 22 : Interrupt acknowledge sequence flow chart.

6.3.3.3 · Register description

Any internal status change that induces a bit to be set in the status-register will generate an interrupt if this cause is enable by the Mask-register and if no highest priority cause is already activated or pending.
For the receiver blocks, the priority is programmable (see interrupt vector number description). For the transmitter block, the End-of-transmission has higher priority than FIFO-empty and channel 1 has higher priority than channel 2 that has higher priority than channel 3.

The RX wrong parity bit can be set only if self-test register bit 0 is set to 1.
The user has to check which receiver has it receiver control register bit 7 set to 1.
At the end of the interrupt procedure, the user must reset RX wrong parity bit to 0.

RX wrong parity is the higher interrupt priority source for the receiver part of the MRT.

6.3.3.4 - The mask register

The mask register is accessible for reading and writing operations. The mask register is used to disable interrupt source. The bit order is the same as in the status register. A «0» indicates that this source is disable, a «1» enables an interrupt for this source.

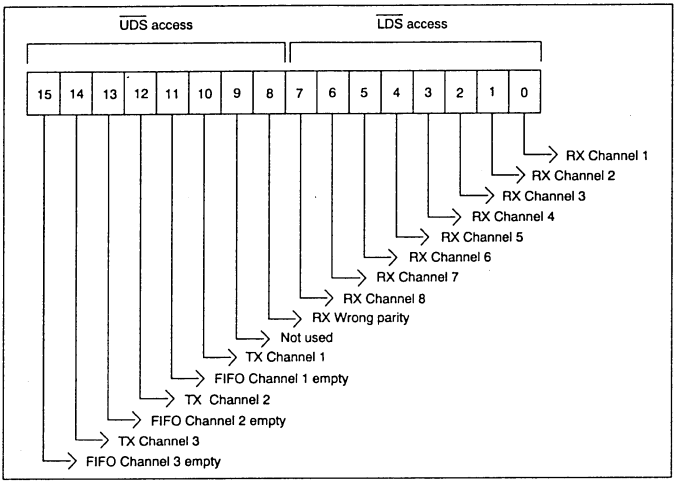


Figure 23 : Mask register.

6.3.3.5 - The base register

The base register is only accessible for writing operations by the user. The base register must be programmed at the initialization phase. It contains the base for the vector generation during an interrupt acknowledge. This allows the use of several peripherals. If not programmed interrupt vector is set to $ 0F.

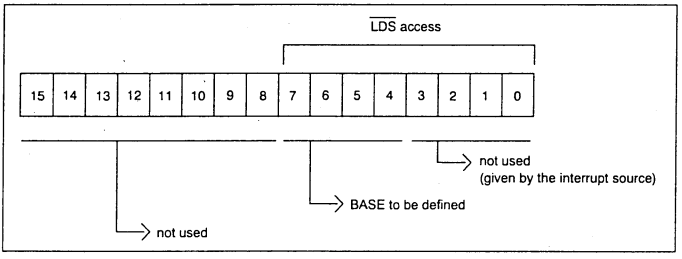
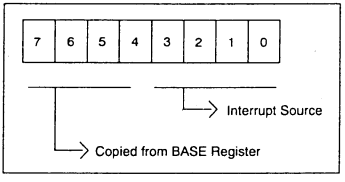


Figure 24 : Base register.

6.3.3.6 - The interrupt vector number

During an interrupt acknowledge cycle, an 8 bit vector number is presented to the microprocessor on D0-D7 lines. This vector number corresponds to the interrupt source requesting service. The format of this number is given below.



Bit 3 to 0 : Interrupt source :

0000 : Msg on receiving channel 1
0001 : Msg on receiving channel 2
0010 : Msg on receiving channel 3
0011 : Msg on receiving channel 4
0100 : Msg on receiving channel 5
0101 : Msg on receiving channel 6
0110 : Msg on receiving channel 7
0111 : Msg on receiving channel 8
1000 : RX wrong parity
1001 : Not used
1010 : End of transmission on channel 1
1011 : FIFO of channel 1 empty
1100 : End of transmission on channel 2
1101 : FIFO of channel 2 empty
1110 : End of transmission on channel 3
1111 : FIFO of channel 3 empty

Figure 25

6.4 - Self-test description

A self-test has been implemented for the receiver control label matrix RAM and the transmitter FIFO. This test can be used to guarantee the good behaviour of the different MRT's memories.

6.4.1 - Register description

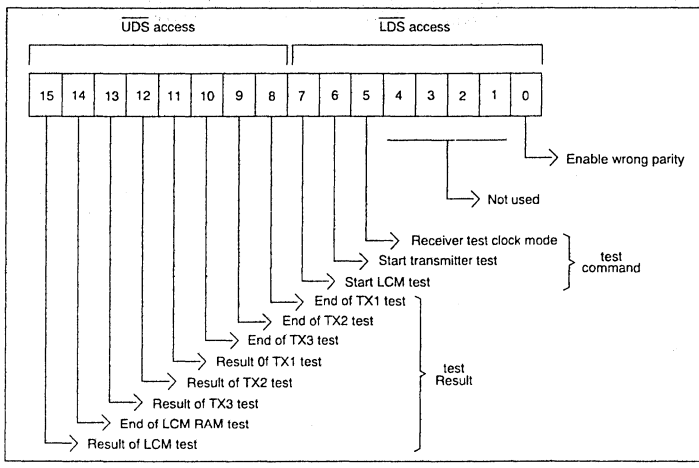


Figure 26 : Self-test register.

The self-test register can be split in 3 parts :

a) bit 0 : Used to enable receiver wrong parity detection. This bit has been implemented to guarantee compatibility with previous designs :
0 : Receiver wrong parity detection disable,
1 : Receiver wrong parity detection enable.

b) Seft-test command :

bit 5 : Receiver test clock mode :
0 : If CLK-SYS is less or egal to 10 MHz,
1 : If CLK-SYS is higher than 10 MHz.

bit 6 : Start transmitter self-test if a 0 to 1 transition is programmed (before a new self-test, the user must reprogram this bit to 0).

bit 7 : Start receiver Label Control Matrix self-test if a 0 to 1 transition is programmed (before a new self-test, the user must reprogram this bit to 0).

c) Self-test result :

bit 8 : 0 : Transmitter 1 self-test is running,
1 : End of Transmitter 1 self-test.

bit 9 : 0 : Transmitter 2 self-test is running,
1 : End of Transmitter 2 self-test.

bit 10 : 0 : Transmitter 3 self-test is running,
1 : End of Transmitter 3 self-test.

bit 11 : Result of Transmitter 1 self-test :
0 : (if bit 8 is set to 1) self-test pass,
1 : Self-test fail.

bit 12 : Result of Transmitter 2 self-test :
0 : (if bit 9 is set to 1) self-test pass,
1 : Self-test fail.

bit 13 : Result of Transmitter 3 self-test :
0 : (if bit 10 is set to 1) self-test pass,
1 : Self-test fail.

bit 14 : 0 : Receiver Label Control Matrix self-test is running,
1 : End of receiver Label Control Matrix self-test.

bit 15 : Result of receiver LCM self-test :
0 : (if bit 14 is set to 1) self-test pass,
1 : Self-test fail.

6.4.2 - Self-test use

The self-test destroys the content of the tested memory. So, it could be used after system reset, during system initialization. Only 1 self-test (transmitters and receivers) can be performed after a reset. If the self-test must be restarted, the reset must be activated (then released) before the new self-test start.

To program the self-test :

1) If receiver self-test will be used :
   set to 1 LCMWE bits (for all receivers).

2) If receiver self-test will be used and CLK-SYS is > 10 MHz :
   set to 1 self-test register bit 5.

3) Start self-test :
   set to 1 self-test register bit 6 for Transmitter test,
   set to 1 self-test register bit 7 for Receiver RAM test.

   At this point, self-test is running. The test duration is :
   710 CLK-SYS periods for Transmitter self-test,
   2820 CLK-SYS periods for Receiver RAM test if self-test register bit 5 is 0,
   5640 CLK-SYS periods for Receiver RAM test if self-test register bit 5 is 1.

To read the self-test result, the user must :

1) poll the self-test register and wait for an end of test set to 1 (bits 8 to 10, bit 14) then.
2) read again the self-test register to have a valid result on bits 11, 12, 13, 15 according to the tests which end at point 1.

5

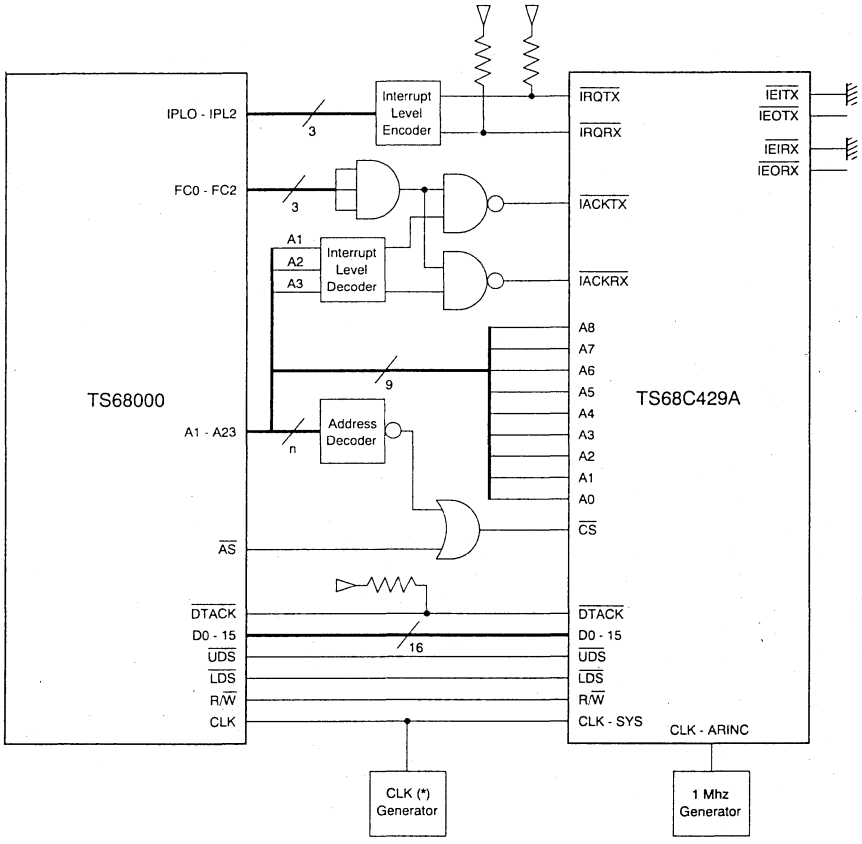
6.5 · Memory MAP

Address	Access	Register	
0H 1H 2H 3H	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 1
4H 5H 6H 7H	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 2
8H 9H AH BH	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 3
CH DH EH FH	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 4
10H 11H 12H 13H	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 5
14H 15H 16H 17H	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 6
18H 19H 1AH 1BH	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 7
1CH 1DH 1EH 1FH	R / W W R R	Receiver-control-register Gap-register Message-buffer MSW Message-buffer LSW	Receiving channel 8
20H 21H 22H 23H	R / W W W W	Transmit-control-register Frequency-register Message-FIFO MSW Message-FIFO LSW	Transmission channel 1
24H 25H 26H 27H	R / W W W W	Transmit-control-register Frequency-register Message-FIFO MSW Message-FIFO LSW	Transmission channel 2
28H 29H 2AH 2BH	R / W W W W	Transmit-control-register Frequency-register Message-FIFO MSW Message-FIFO LSW	Transmission channel 3
40H	R / W	Status-register	
41H 42H 43H	R / W W R / W	Mask-register Base-register Self-test register	
100H to 1FFH	R / W	Label-control-matrix	Receiving channels 1-8

MRT address 2CH to 3FH and 44H to FFH do not generate $\overline{\text{DTACK}}$ signal (illegal address).

7 - APPLICATION NOTES (for additional details order the AN 68C429A)

7.1 - Microprocessor interface



(*) This kind of application can also work with an independant clock

Figure 27 : Typical interface with 68000.

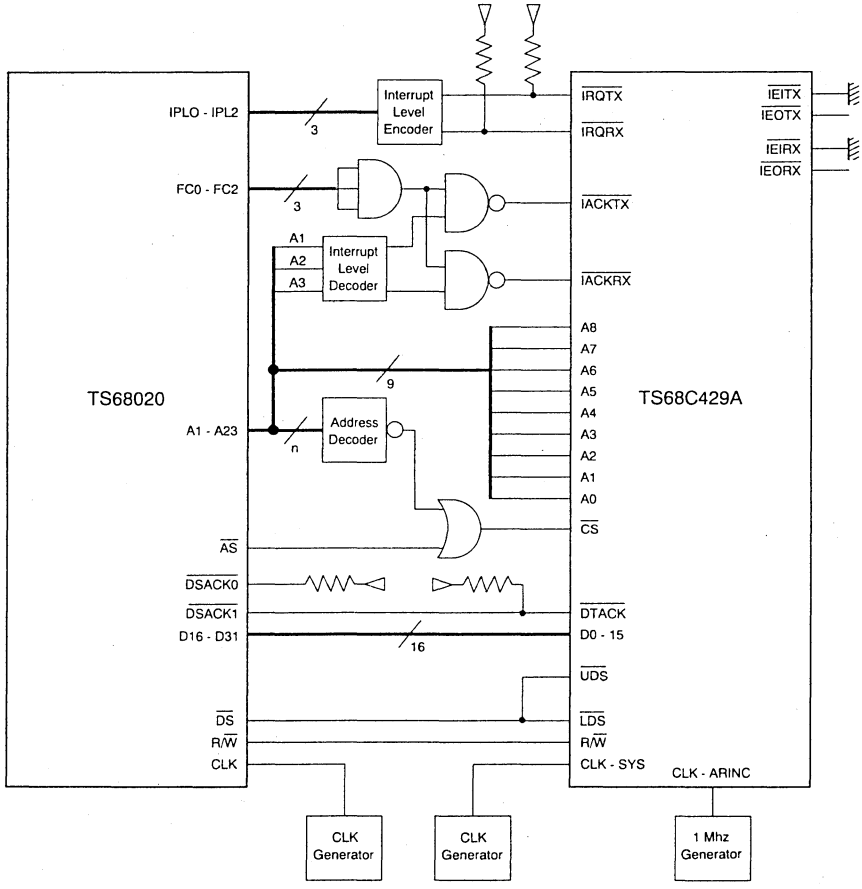


Figure 28 : Typical interface with 68020 / CPU 32 core microcontrollers.

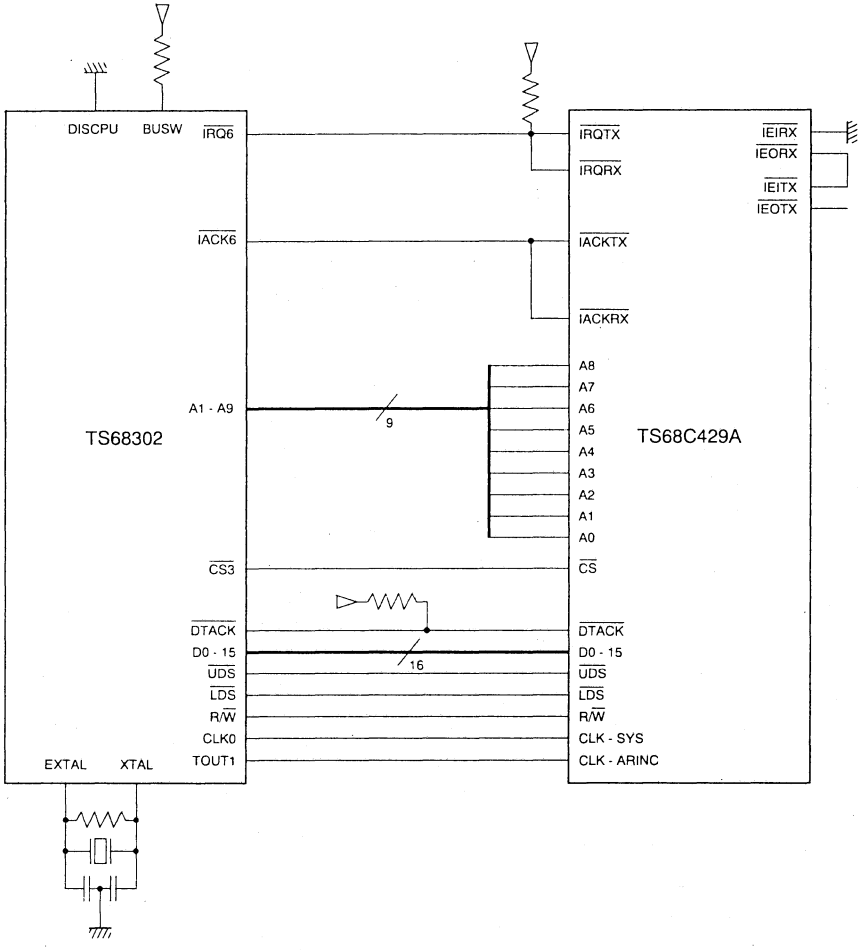


Figure 29 : Typical interface with 68302.

In this example, receiver interrupts have an higher priority than transmitter interrupts.

7.2 - Programms flow-chart

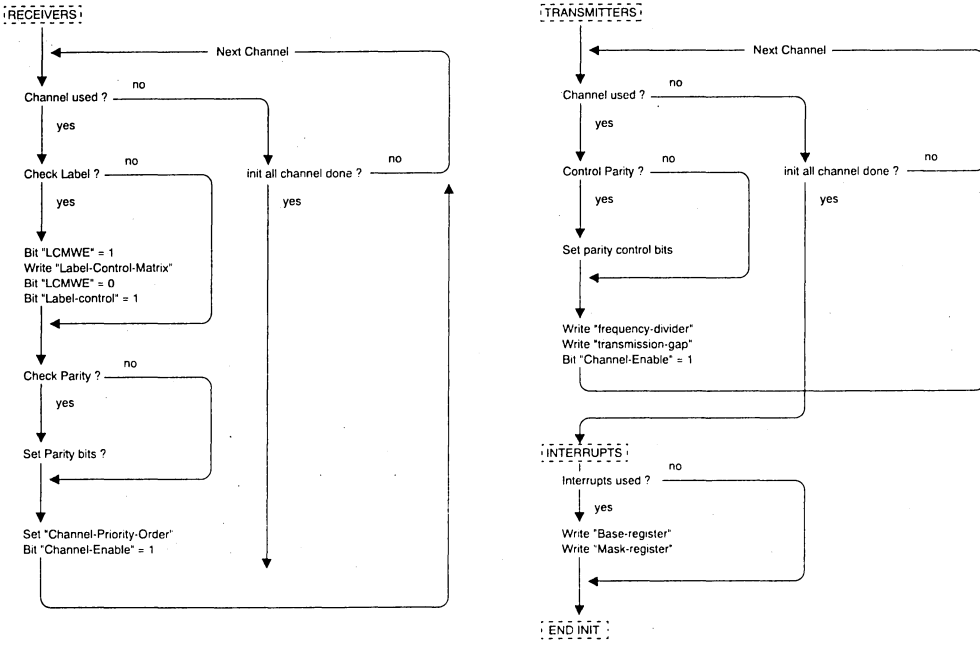


Figure 30 : Initialization after reset flow-chart.

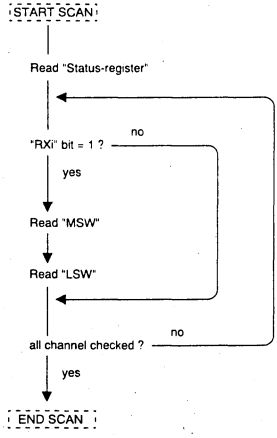


Figure 31 : Receiver without interrupt flow-chart.

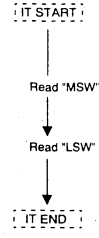


Figure 32 : Receiver with interrupt flow-chart.

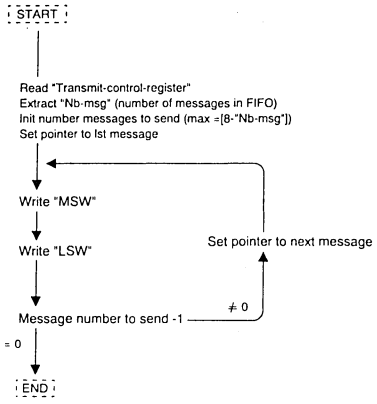


Figure 33 : Transmitter without interrupt flow-chart.

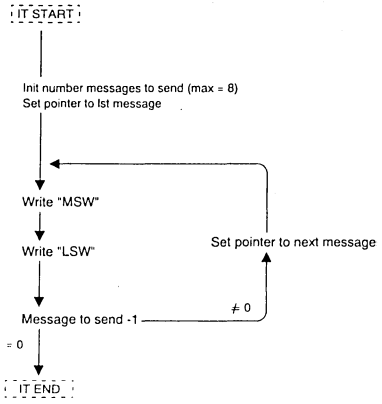


Figure 34 : Transmitter with interrupt flow-chart.

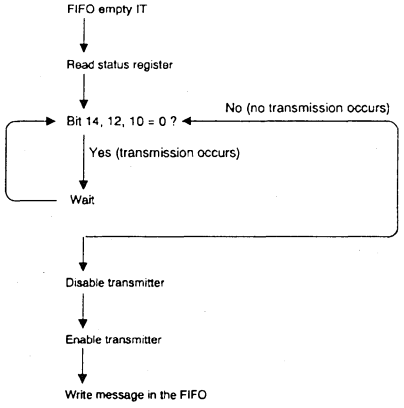


Figure 35 : First FIFO access.

8 - PREPARATION FOR DELIVERY

8.1 - Packaging

Microcircuits are prepared for delivery in accordance with MIL-I-38535 or DESC.

8.2 - Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or DESC and guarantying the parameters not tested at temperature extremes for the entire temperature range.

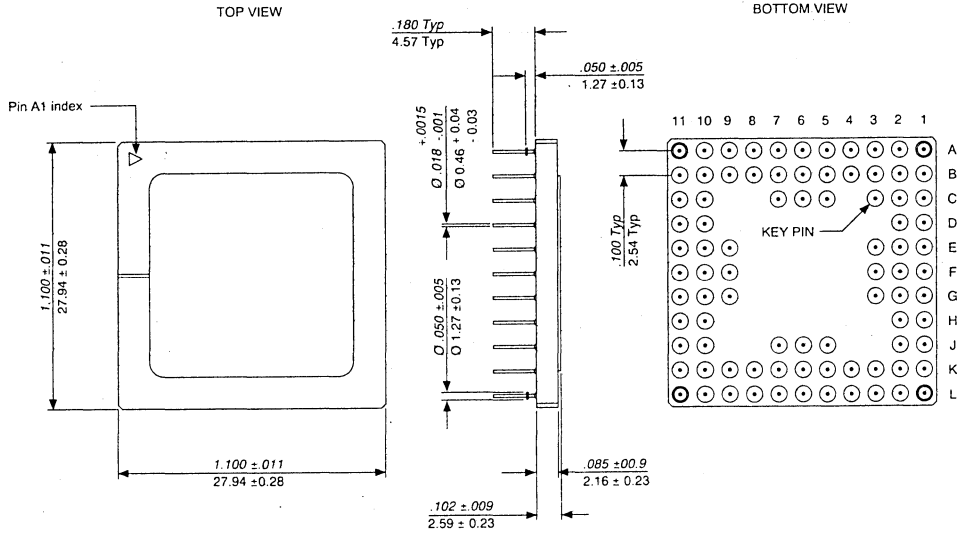
9 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

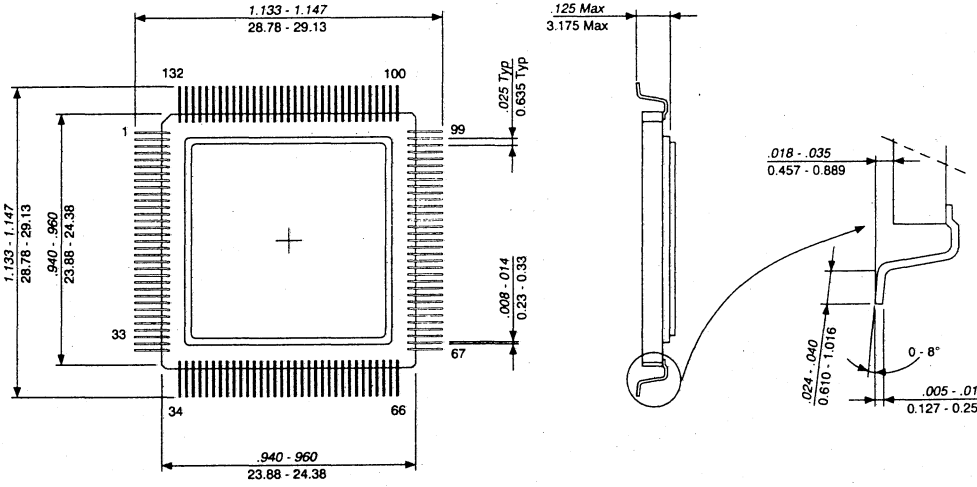
a) Devices should be handled on benches with conductive and grounded surfaces.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent if practical.

10 - PACKAGE MECHANICAL DATA

10.1 - PGA 84

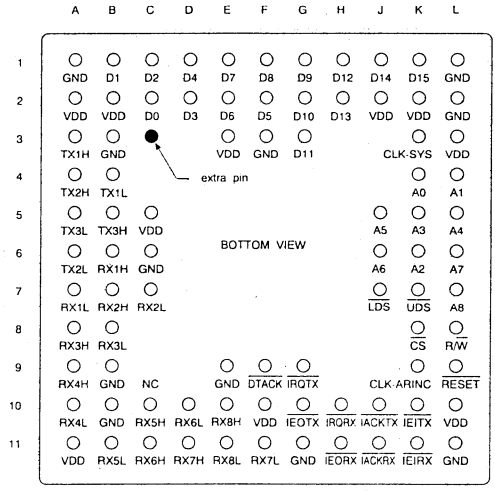


10.2 - CQFP 132

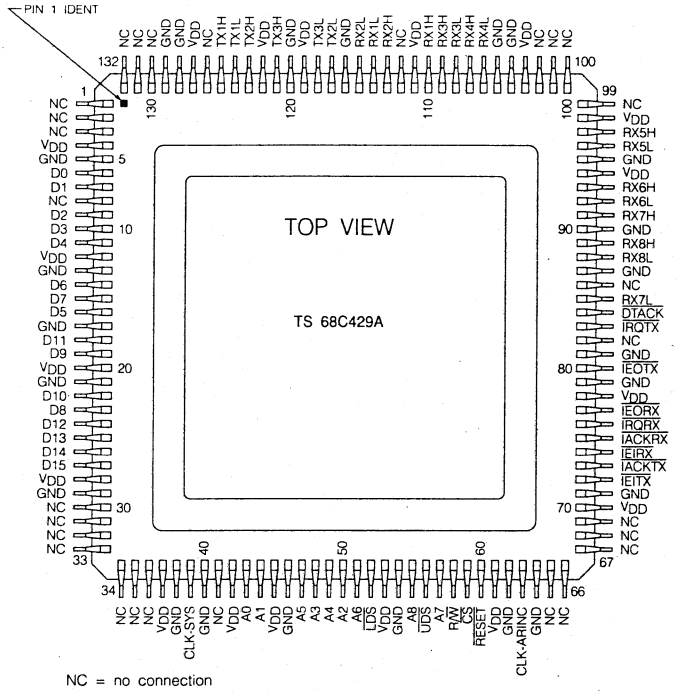


11 - TERMINAL CONNECTIONS

11.1 - PGA 84 pin assignment



11.2 - CQFP 132 pin assignement



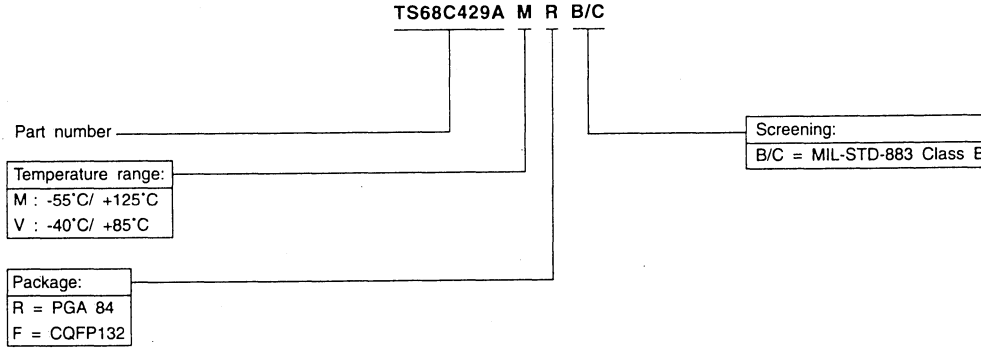
12 · ORDERING INFORMATION

12.1 · Standard product

TCS part number	Norms	Package	Temperature range T_C (°C)	Detailed qualification
TS68C429AMR	TCS Standard	PGA 84	−55 / +125	TCS internal
TS68C429AMF	TCS Standard	CQFP 132	−55 / +125	TCS internal
TS68C429AVR	TCS Standard	PGA 84	−40 / +85	TCS internal
TS68C429AVF	TCS Standard	CQFP 132	−40 / +85	TCS internal

12.2 · Hi-REL products

TCS part number	Norms	Package	Temperature range T_C (°C)	Detailed qualification
TS68C429AMRB/C	MIL-STD-883	PGA 84	−55 / +125	TCS internal
TS68C429AMFB/C	MIL-STD-883	CQFP 132	−55 / +125	TCS internal
TS68C429ADESCxx	DESC	PGA 84	−55 / +125	T.B.D.
TS68C429ADESCxx	DESC	CQFP 132	−55 / +125	T.B.D.



DRAFT

AN68C429A

APPLICATION NOTE

FOR TS68C429A : CMOS ARINC 429 MULTICHANNEL RECEIVER/TRANSMITTER CONTROLLER (MRT)

SCOPE

"HOW TO CONNECT THE 68C429A TO HOST SYSTEM"

The ARINC 429 Avionic protocol is widely implemented on a lot of different equipments using a wide variety of microprocessors and microcontrollers. The purpose of this application note is to describe in addition to the elements already mentioned into the TS68C429A datasheet, the connection of the MRT with three different bus worlds.

5

- MOTOROLA ASYNCHRONOUS BUS with 68302 as an example of this generic family including 68000, 68C000, 68020, 68030 and MCU"s : 683xx like 68302, 68332.
- MOTOROLA SYNCHRONOUS BUS with 68040.
- INTEL BUS such as 80C186.

Users will find inside this application note a complete set of hardware and mainly software examples for the different functional units of the MRT.

Table of contents

APPLICATION NOTE
TS68C429A (MRT) : microprocessor connection examples

INTRODUCTION

This document is divided into two main parts. First, you will find support for the TS68C429A hardware, then you will find a set of programs in assembler language.

The first part provides you with information about the way the TS68C429A can be connected up to 3 microprocessors : the TS68302, the TS68040 and the I80C186EB. Indeed, you will find the electrical schematics diagrams and the PLD programmation description to connect the TS68C429A to the MOTOROLA ADS302 and IDP040 boards, and the INTEL EV186EB board.

The second part of these documents provides you with four programs. Whatever your problem can be, we hope you will be able to find the appropriate answer within these programs. You will also find in this document examples of these program outputs.

This application note has been written to answer to the most common problems encountered when using the MRT.

I) HARDWARE

a) General comments :

We tried to designed the connections in order to get a tool as flexible as possible. That is why each receiver and each transmitter line has been connected externally. So, when you don't use the MRT in test mode you must connect the receivers and the transmitters externally through connectors.

We used the same system to connect the daisy chain driving signals. So, you can choose whether you want to use the MRT daisy chain possibilities or not. But if you don't use them, do not forget to connect the IEIRX* and IEITX* signals to the ground.

You can also select the priority level you want to assign to the IRQTX* and IRQRX* signals, thanks to this system. With the ADS302 board and the IDP040 board, you can also select the corresponding IACK* lines. When you use the MRT interrupt possibilities, do not forget to connect the IRQ* lines to the level priority you want, and the IACK* lines to the corresponding ones.

b) Connecting the MRT to the MOTOROLA ADS302 board :

CLK-SYS must be connected externally to 68302 CLKO or to an external oscillator. This is the only example we will provide where the MRT can be used in synchronous or asynchronous mode.

CLK-ARINC is connected to the 68302 timer 1 output (TOUT1). This timer must be software initialised before using the MRT.

Finally, the A1 pin from the 68302 is connected to the MRT A0 pin, so the MRT is addressed through even addresses only (in word mode).

c) Connecting the MRT to the MOTOROLA IDP040 board :

The MRT signals and the 68040 signals are not fully compatible. So, in order to decode them, we use two PLD : a 20R4 PLD and a 16R4 PLD. They are used to decode the MRT control signals -CS*, LDS*, DTACK*, and they are also used to decode the interrupt control signals - IRQxx*, IACKxx*. The 16R4 PLD is used in order to generate CLK-SYS and to be able to work in synchronous mode. The PLD equations can be found within the following documents.

The LDS* signal must be active when the component is selected, in byte or word mode, on the D0-D7 lines (as for UDS* on the D8-D15 lines). But, unlike UDS*, it must also be selected when an IACKxx* access occurs.

IACKTx* is designed to be a level 2 or level 4 IACK*, depending on the external connections made by the user. IACKRx* is designed to be a level 4 or level 6 IACK*. Indeed, if two interrupt levels are used (level 2 and 4),when there are a receiver and a transmitter interrupt request pending together, the 68040 detects a level 6 interrupt request.So, the receivers having a higher priority level than the transmitters, the IACKRx* signal must be activated.

The address decoding is very partial in the example provided : it is because its main purpose is to be a teaching tool and we didn't want to use too many PLD. If you want to use it with a specific application, you should decode this address less partially. We point out that the software provided assumes that the MRT address is $6000000.

CLK-ARINC is connected to an external clock generator. You can refer to the MRT preliminary data to decide how to generate this signal. We point out that the software provided assumes that this clock frequency is 1MHz.

Finally, the A2 pin from the 68040 is connected to the MRT A0 pin, so you must beware of the address translation writting the corresponding software.

d Connecting the MRT to the INTEL EV80C186EB board :

The MRT signals aren't designed to be compatible with the INTEL family components. That is why we must use a 16R4 PLD in order to decode these signals. The PLD equation can be found within the following documents.

CLK-ARINC is connected to the I80C186EB timer output TOUT0. This timer must be software initialized before using the MRT.

This is the only example where no decoding of the IACKxx* signals is performed.

Finally, the A1 pin from the I80C186EB is connected to the MRT pin A0, so the MRT is addressed through even addresses only.

PLD 16R4 FOR THE 68040 : Equations

```
TITLE  MRT16R40
PATTERN MRT16R440
REVISION     C
AUTHOR  THOMSON TCS
COMPANY THOMSON TCS
DATE   05/28/94
;
; ACKNOWLEDGES AND CLOCK SYSTEM FOR THE 68C429A
;
CHIP   U2    PAL16R4
; 1          2     3     4          5     6     7     8          9          10
  BCLK       TS    TIP   SIZ1       SIZ0  TT1   TT0   TM2        TM1        GND
  OE         TM0   NC    CLKSYS     NC    NC    NC    IACKRX     IACKTX     VCC
; 11         12    13    14         15    16    17    18         19         20
;
;
EQUATIONS
/CLKSYS  := CLKSYS + /TS

/IACKRX  = /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * /TM1 * /TM0 * /TIP
         + /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * TM1 * TM0 * /TIP

/IACKTX  = /SIZ1 * SIZ0 * TT1 * TT0 * /TM2 * TM1 * /TM0 * /TIP
```

'/'	Stands for	'not' operator
'+'	Stands for	'or' operator
'*'	Stands for	'and' operator
'='	Stands for	combinatorial equal
':='	Stands for	registered equal

PLD 20R4 FOR THE 68040 : Equations

```
TITLE MRT20R40
PATTERN MRT20R40
REVISION     E
AUTHOR  THOMSON TCS
COMPANY THOMSON TCS
DATE   24/05/94

; CONTROL SIGNALS FOR THE 68C429A
;
;
CHIP   U4    PAL20R4
;1          2     3     4          5     6     7     8     9     10    11    12
 BCLK       A27   A26   TM0        TM1   TT0   TT1   SIZ0  SIZ1  TM2   TS    GND

 OEI        A0    OEO   DTACK      NC    ADR   CS    TA    UDS   LDS   A1    VCC
;13         14    15    16         17    18    19    20    21    22    23    24
;
;
EQUATIONS
/ADR   := /A27 * A26

/OEO   = TS * /TT1 * /TT0 * /ADR
       + TS * /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * /TM1 * /TM0
       + TS * /SIZ1 * SIZ0 * TT1 * TT0 * /TM2 * TM1 * /TM0
       + TS * /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * TM1 * /TM0

/CS    := TS * /TT1 * /TT0 * /ADR * TA

/TA    := /DTACK * TS * TA

/LDS   = /SIZ1 * SIZ0 * A1 * A0* /CS
       + SIZ1 * /SIZ0 * A1* /A0 * /CS
       + /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * /TM1 * /TM0
       + /SIZ1 * SIZ0 * TT1 * TT0 * /TM2 * TM1 * /TM0
       + /SIZ1 * SIZ0 * TT1 * TT0 * TM2 * TM1 * /TM0

/UDS   = /SIZ1 * SIZ0 * A1 * /A0 * /CS
       + SIZ1 * /SIZ0 * A1 * /A0 * /CS

DTACK.TRST = GND
```

'/'	Stands for	'not' operator
'+'	Stands for	'or' operator
'*'	Stands for	'and' operator
'='	Stands for	combinatorial equal
':='	Stands for	registered equal

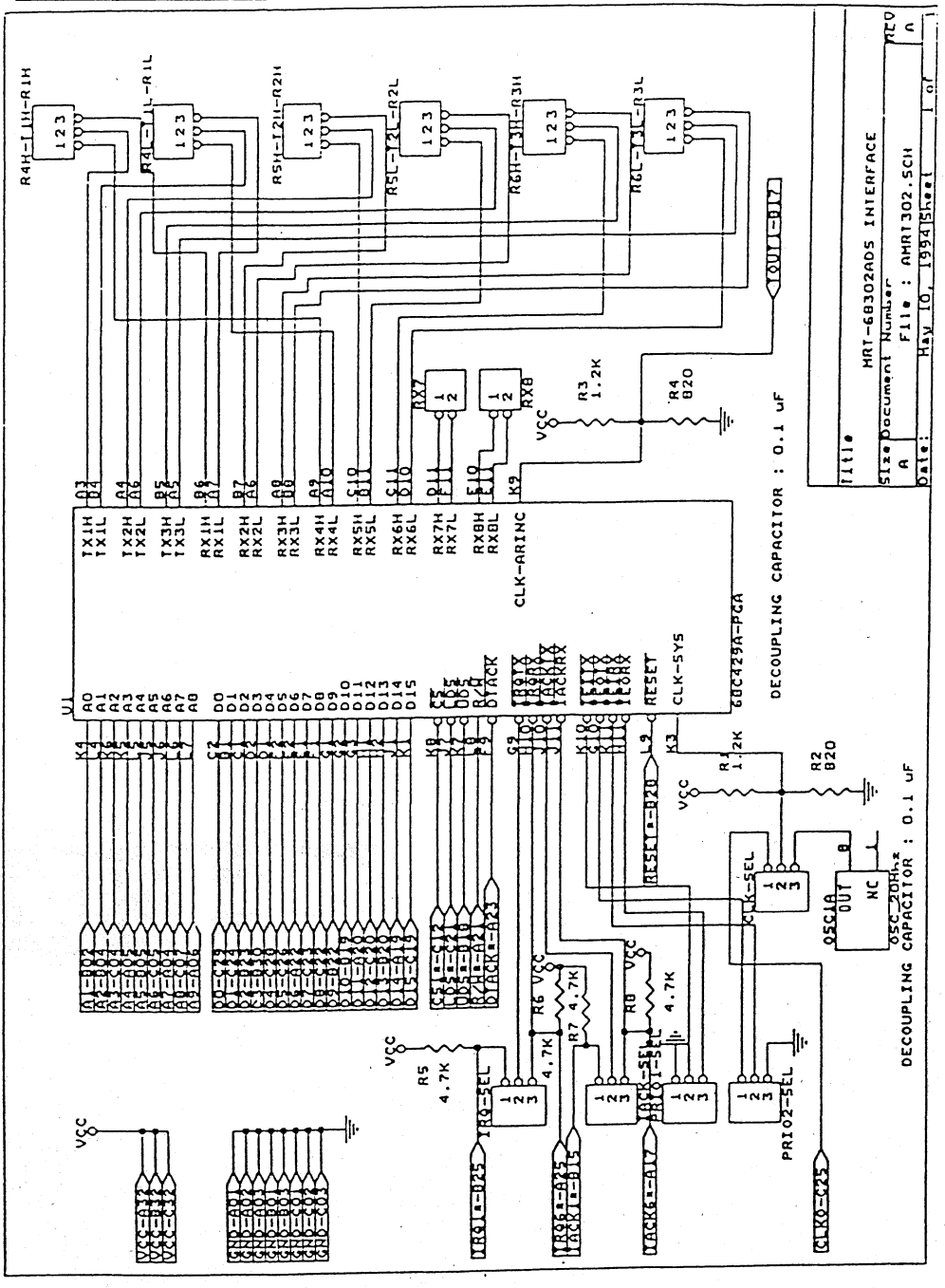
IPLD 16R4 FOR THE I80C186EB : Equations

```
TITLE   AMRT186B
PATTERN AMRT186B
REVISION      B
AUTHOR  THOMSON TCS
COMPANY THOMSON TCS
DATE    24 Oct 94
;
; DECODING SIGNALS FROM THE I80C186EB FOR THE MRT
;

CHIP   U2     PAL16R4
; 1          2          3          4          5          6          7          8          9          10
 CLKOUT     IRQTX      IRQRX      DTR        DEN        BHE        ALE        GCS4       RESOUT     GND
 OE         UDS        LDS        RESET      INT2       INT0       CS1        RW         CS         VCC
;11         12         13         14         15         16         17         18         19         20
;
EQUATIONS
/CS     = /CS1
/RW     = DTR
/CS1    := /GCS4 * /ALE
/RESET  := RESOUT
/INT0   := IRQTX
/INT2   := IRQRX
/LDS    = /CS1 * /DEN
/UDS    = /CS1 * /BHE * /DEN
```

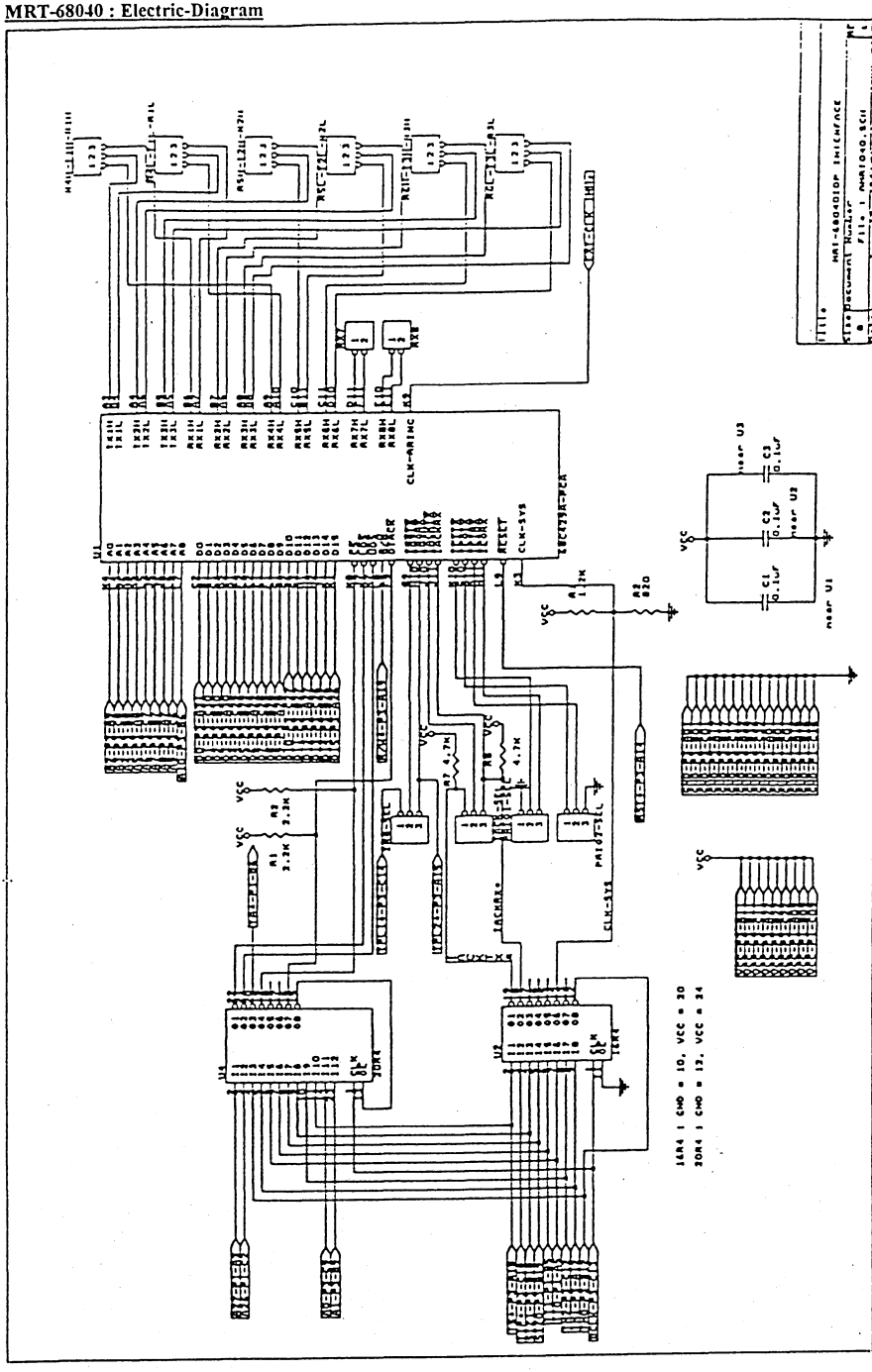
'/ '	Stands for **'not'** operator
'+ '	Stands for **'or'** operator
'* '	Stands for **'and'** operator
'= '	Stands for **combinatorial equal**
':= '	Stands for **registered equal**

MRT-68302 : Electric Diagram

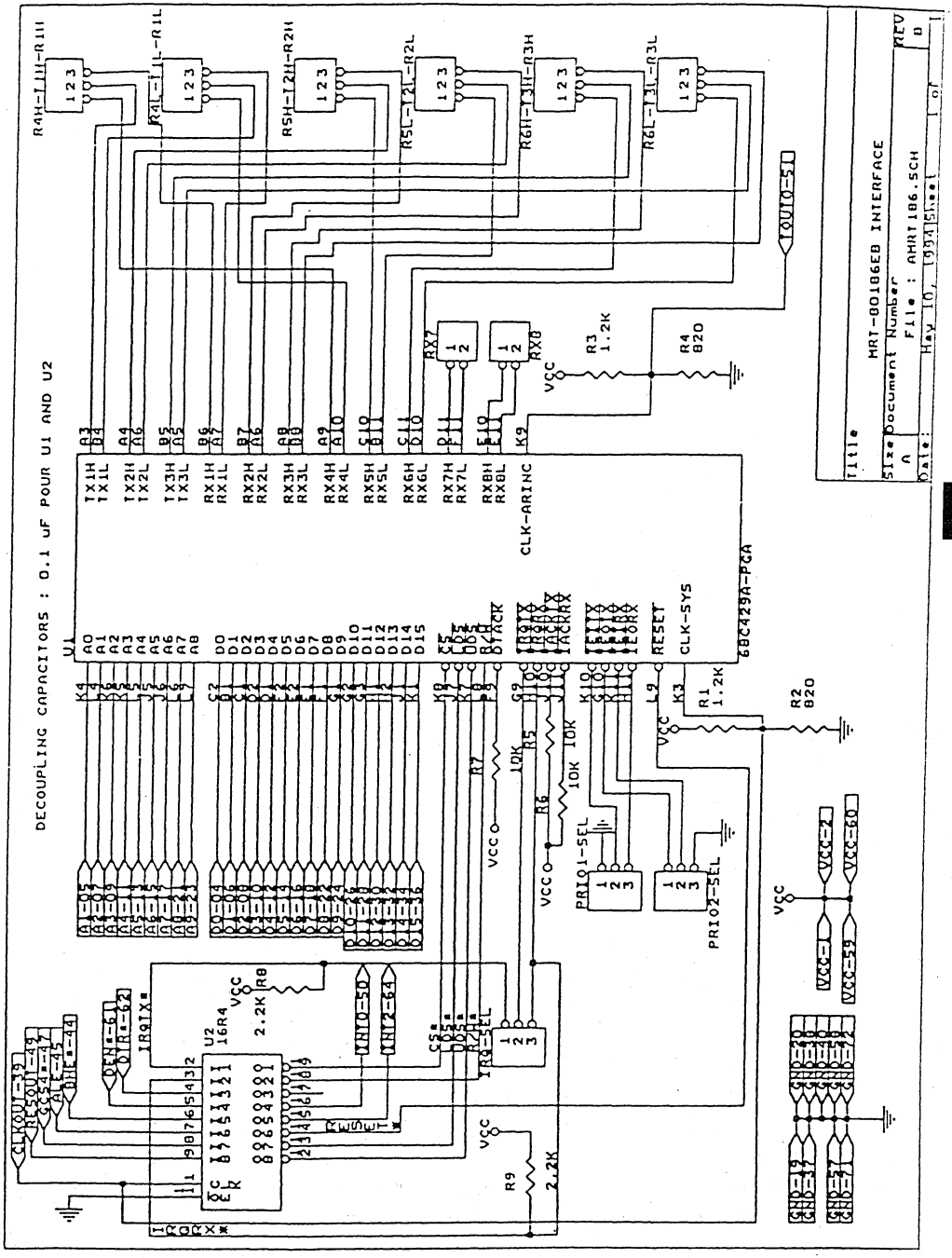


5

MRT-68040 : Electric-Diagram



MRT-I80C186EB : Electric Diagram



II) SOFTWARE

a) Contents :

In this part, you will find four different programs. Each one is divided into its main subroutines. Thanks to them, you will be able to find out how to program the parity control, the selftest, the label control matrix, and how to send and receive messages using the MRT interrupt capabilities.

The two first programs are designed for the MOTOROLA ADS302 board. The first one is the simplest. It will provide you with the bases you will need to program the MRT. Thanks to the second one, you will be able to program and to use all the functions of the MRT: it is the most detailed example you will find there.

The third program is designed for the MOTOROLA IDP040 board. It is also a very detailed program, using all the MRT functions.

The last program is designed for the INTEL EV80C186EB board. This example is very simple and is only designed in order to provide you with the bases you need to use the MRT with an INTEL family microprocessor.

b) A simple example with the MOTOROLA ADS302 board :

This first example is very simple. After the program you will find the output provided by this program. It only sends and receives a number of messages specified by the user, using the MRT interrupt capabilities, in test mode, thanks to transmitter 3 (transmitters 1 and 2 are disabled). The user must also specify the content of the first message to be sent. The content of this message will be increased by one between each sending.

You will find the way the MOTOROLA ADS302 board has been initialized in order to be used with the MRT. Timer1 has been programmed in order to output a 1MHz square wave signal. The MRT address will be $80 0000 and it will be activated through Chip Select 1.

Then, you will find how to initialize the MRT in order to enable it to communicate with the MOTOROLA ADS302 board. There, the 8 receivers are used, but we must point out that the 8 priority levels must be programmed, from 0 to 7, no matter if all the receivers are enabled or not. So, if a receiver is disabled, you must anyway credit it with an interrupt priority level between 0 and 7 (and with an higher value than the receivers that are used)..

At last, you will find the interrupt routines, allowing you to send and receive messages. There, we send and receive messages in two steps, writing first a word at the MSW address, and then an other word at the LSW address. With the latest MRT versions, you can also send and receive messages in a single step, writing a long word at the LSW address.

The generic in-out subroutines that allow you to communicate with the monitor (puts, write, etc...) are provided with the second program dealing with the MOTOROLA ADS302 board, as the general register addressing and interrupt addressing for the MRT.

```
; Part of Send302.s
    ;
    ;THIS PROGRAM INITIALIZES THE ADS 302 BOARD IN ORDER TO
     ENABLE IT TO COMMUNICATE WITH THE MRT
    ;
    ;IT FIRST INITIALIZES THE INTERRUPTION MODE
    ;
    ;THEN IT ENABLES THE ADS 302 TIMER 1 THAT WILL PROVIDE CLK-ARINC
    ;FOR THE MRT
    ;
    ;THEN, IT SETS THE CHIP SELECT FOR THE MRT AT @ 800000
    ;
    ;IN ORDER TO USE THE MRT, YOU WILL THEN NEED TO INITIALIZE IT
    ;
    ;YOU CAN USE A MENU IN ORDER TO SET THE MRT FOR AN APPROPRIATE
    ;TASK
    ;
    ;YOU CAN SEND AND RECEIVE MESSAGES THANKS TO THE
     INTERRUPTIONS THAT CAN BE GENARATED BY THE MRT, OR NOT
    ;
                lea         STKTOP,a7                ; init stack

    ;INITIALIZE THE ADS 302 INTERRUPT CONTROL UNIT
                move.w      #$b0a0,gimr              ; dedicated interruption mode
                clr.w       imr                      ; mask all INR interruptions
                move.w      #$0016,pbcnt             ; IACK1*, IACK6*, T1OUT activation

    ;SET ADS 302 TIMER 1 (CLK-ARINC) :
                move.w      #$0001,tr1               ; toggle when count = 1
                move.w      #$092b,tmr1              ; Pre-scaler = 9, no capture, toggle,
                                                     ;no IT, restart
                                                     ; Master clock, enable
    ; CS1 PROGRAMMATION :
                move.w      #$1001,br1               ; base address = 800000
                move.w      #$FFFC,or1               ; no DTACK, no FC, R/W enabled
                clr.w       mask                     ; mask TS68C429A interruptions

    ; JUMP TO CURRENT APPLICATION SUBROUTINES :
                bsr         initmrt                  ; MRT setup
                bsr         menu                     ; what do you want to do ?
                bsr         initsys                  ; Interruption enable or disable

    ; There, you should insert a test in order to wait for the end of your transmission/reception
    ;sequence if you use the MRT interrupting possibilities. For instance :

    fini        cmp         d5,d3                    ; msg received ?
                beq         fin                      ; No, wait
                move.l      d4,d4                    ; end of transmit ?
                bpl             fini                 ; no : loopfin
        clr.w   mask    ; mask TS68C429A interruptions
                trap        #15
                dc.w        0                        ; Return monitor

        END
```

```
; Part of Send302.s
;
; THANKS TO THIS KIND OF SUBROUTINE, YOU CAN GET
 INFORMATION FROM THE CONSOLE
;
; THERE WE FIRST ASK FOR THE NUMBER OF MESSAGES THE USER
;WANT TO SEND
;
; THEN, WE ASK FOR THE FIRST MESSAGE CONTENT
;

menu        lea         nbmsg,a6
            jsr         puts                ; Ask for nb of msg to be sent
            jsr         getcn               ; Wait for an answer
            jsr         write
            move.l      d0,d5               ; Fill nb of msg buffer
            subq.l      #1,d0
            move.l      d0,d4               ; Initialise transmiter 3  message counter

            lea         msg,a6
            jsr         puts                ; Ask for msg to be sent
            jsr         get8hx              ; Wait for an answer
            move.l      d0,d6

            rts

; THANKS TO THIS SUBROUTINE, YOU ENABLE INTERRUPTIONS FROM
 THE MRT AND THE CPU CAN BE INTERRUPTED
;
initsys     move.w      #$8007,mask         ; enable Rx1,2,3,Tx3 ITs
            move.w      #$2000,sr           ; enable 68000 ITs
      rts

; Part of Send302.s
;
; THANKS TO THIS SUBROUTINE, YOU WILL BE ABLE TO INITIALIZE THE
 MRT.  TEST MODE IS IN USE

; ARINC setup procedure :

initmrt     clr.w       status              ; only for receivers (byte)

            move.w      #$1E,rx1_gap        ; gap lenght = 3 arinc bits
            move.w      #$C007,rx1_ctr      ; priority 1, no parity, No Test
                                            ; gap lenght = 30 clk-arinc periods
            move.w      #$1E,rx2_gap        ; idem than rx1
            move.w      #$C006,rx2_ctr      ; priority 2, no parity, No Test

            move.w      #$1E,rx3_gap        ; idem than rx1
            move.w      #$C005,rx3_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx4_gap        ; idem than rx1
            move.w      #$C004,rx4_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx5_gap        ; idem than rx1
            move.w      #$C003,rx5_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx6_gap        ; idem than rx1
            move.w      #$C002,rx6_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx7_gap        ; idem than rx1
            move.w      #$C001,rx7_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx8_gap        ; idem than rx1
            move.w      #$C000,rx8_ctr      ; priority 3, no parity, No Test

; TRANSMITTERS
; unused channels are : disable and fifo is reseted (reset fifo is not
; mandatory)

            move.w      #$10,tx1_ctr
            move.w      #$10,tx1_ctr
```

```
                move.w      #$0014,tx3_frq          ; TX rate = 100 Kbit/s
                move.w      #$8100,tx3_ctr          ; Reset FIFO
                move.w      #$8090,tx3_ctr          ; Means :
; In service, Test mode, no parity, FIFO in use
; Gap = %100 = 4 Arinc bits, No Test

                move.w      #$80,base               ; interrup vector points at #$200
        rts
; Part of Send302.s
;
; MESSAGE SENDING USING THE MRT INTERRUPT POSSIBILITIES
;
;
;THIS SUBROUTINE SENDS #D4 MESSAGES FROM THE MRT TRANSMITTER 3
;
;EACH MESSAGE IS EQUAL TO THE CONTENT OF THE PREVIOUS ONE PLUS
;ONE
;
;THE ECHO TO THE CONSOLE PRINTS ' Transmission nb # '
;
;WHEN THE LAST MESSAGE HAS BEEN SENT, TRANSMISSION IS DISABLED
;
;

txf3a
                ori.w       #$0700,sr               ; disable CPU ITs

; SEND THE MESSAGE :

send            swap        d6
                move.w      d6,tx3_msw  ; Send message, first step
                swap        d6
                move.w      d6,tx3_lsw              ; Send message, second step
                addq.w      #1,d6                   ; Define new message

; ECHO TO THE CONSOLE:

                lea         envoi,a6    ; print envoi
                jsr         puts
                move.l      d4,d0
                jsr         out2hx                  ; print nb of msg

; DISABLE TRANSMISSION WHEN THE LAST MESSAGE HAS BEEN SENT :

                subi.w      #1,d4
                bpl         txf3a2
                andi.w      #$7fff,tx3_ctr          ; end of transmission

txf3a2
                andi.w      #$f8ff,sr               ; enable CPU ITs

        rte
f Send302.s
;
; MESSAGE RECEIVING USING THE MRT INTERRUPT POSSIBILITIES
;
;
; THIS SUBROUTINE RECEIVES MESSAGES IN THE MRT RECEIVERS 1, 2 AND 3
;
; THE ECHO TO THE CONSOLE PRINTS ' Receiver msg nb # = # '
;
; WHEN THE LAST MESSAGE HAS BEEN RECEIVED, TRANSMISSION IS DISABLED
;
;
; RECEIVER 1 :

rx1a
                move.w      rx1_msw,d7              ; Read 32 bit message
```

```
                swap        d7
                move.w      rx1_lsw,d7          ; mess in D7
                addq.l      #1,d1               ; received mess. counter

                lea         rxmessA,a6
                jsr         puts                ; print rxmess
                move.l      d1,d0               ; copy d1 in d0
                jsr         out2hx              ; print mess #
                lea         rxmess2,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content

                cmpi        #0,d4               ; last msg ?
                bge         ret1                ; no, then, go on
ret2            move.w      #$0007,mask         ; disable transmission ITs
ret1
                rte
;
; RECEIVER 2 :
;
rx2a
                move.w      rx2_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx2_lsw,d7          ; mess in D7

                addq.l      #1,d2
                lea         rxmessB,a6
                jsr         puts                ; print rxmess
                move.l      d2,d0               ; copy d2 in d0
                jsr         out2hx              ; print mess #
                lea         rxmess2,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content

                cmpi        #0,d4               ; last msg ?
                blt         ret2                ; yes, then disable transmission
                rte
;
; RECEIVER 3 :
;
rx3a
                move.w      rx3_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx3_lsw,d7          ; mess in D7

                addq.l      #1,d3               ; received mess. counter
                lea         rxmessC,a6
                jsr         puts                ; print rxmess
                move.l      d3,d0               ; copy d3 in d0
                jsr         out2hx              ; print mess #
                lea         rxmess2,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content

                cmpi        #0,d4               ; last msg ?
                blt         ret2                ; yes, the disable transmission
    rt
```

Part of Send302.s

```
;
; THIS SECTION OF CODE GIVES THE REFERENCES FOR UNUSED ITs
  AND GIVES THE MESSAGES TO BE SENT TO THE CONSOLE.
;
;
;
; Unused ITs :
txe3a
txe2a
txf2a
txe1a
txf1a
wpar            rte

rx4a
rx5a
rx6a
```

```
rx7a
rx8a        rte

rxmessA
            dc.b        cr
            dc.b        lf
            dc.b        '     Receiver 1 # '
            dc.b        0

rxmessB
            dc.b        cr
            dc.b        lf
            dc.b        '     Receiver 2 # '
            dc.b        0

rxmessC
            dc.b        cr
            dc.b        lf
            dc.b        '     Receiver 3 # '
            dc.b        0

rxmess2
            dc.b    ', mess = '
            dc.b        0

nbmsg
            dc.b        cr
            dc.b        lf
            dc.b        ' Enter nb of msg (0 to F) to be sent please # '
            dc.b        0

envoi
            dc.b        cr
            dc.b        lf
            dc.b        cr
            dc.b        lf
            dc.b        ' Transmission nb = '
            dc.b        0

msg
            dc.b        cr
            dc.b        lf
            dc.b        ' Enter msg to be sent please # '
            dc.b        0

    end
```

Output to the console

```
302bug> go 30000
 Enter nb of msg (0 to F) to be sent please # 5
 Enter msg to be sent please # 12345678

 Transmission nb = 04
    Receiver 3 # 01, mess = 12345678
    Receiver 2 # 01, mess = 12345678
    Receiver 1 # 01, mess = 12345678

 Transmission nb = 03
    Receiver 3 # 02, mess = 12345679
    Receiver 2 # 02, mess = 12345679
    Receiver 1 # 02, mess = 12345679

 Transmission nb = 02
    Receiver 3 # 03, mess = 1234567A
    Receiver 2 # 03, mess = 1234567A
    Receiver 1 # 03, mess = 1234567A

 Transmission nb = 01
    Receiver 3 # 04, mess = 1234567B
    Receiver 2 # 04, mess = 1234567B
    Receiver 1 # 04, mess = 1234567B

 Transmission nb = 00
    Receiver 3 # 05, mess = 1234567C
    Receiver 2 # 05, mess = 1234567C
    Receiver 1 # 05, mess = 1234567C
302bug>
```

c) A complete example with the MOTOROLA ADS302 board :

This example is the most complete you will find in this document. There, the 8 receivers are enabled, as are the 3 transmitters. To do so, we have connected them externally, and we have disabled test mode.

-Transmitter 1 is connected to receiver 1, 4 and 7.
-Transmitter 2 is connected to receiver 2,5 and 8.
-Transmitter3 is connected to receiver3 and 6.

First, you will find how to **initialize the exception vectors** you will need. Their base address is $200 and is provided by the MRT (cf the MRT initialization procedure, and the base register initialization).

Then, you will find the **global register addressing** for the MRT and the MOTOROLA ADS302 board. Thanks to this routine, you will be able to access these registers without taking care any more of the address calculation. Note that the MRT addressing can be done only through even addresses in word mode with the hardware we are provided with.

You can also find the **in-out routines** that have been designed in order to communicate with the console.

After these preliminary subroutines, you will find how to program the MRT **selftest**. We remind you that before to begin selftest, all the receivers LCMWE bits must be initialized to one. In this example, we test the transmitters and the label control matrix, but you can test them separately if you wish. After selftest execution, the selftest command must be rseted to 0. If you don't want to run selftest, the program skips to the next subroutine.

If you wish, this program enables you to **compute and check parity**. You can program each receiver (parityRX) and each transmitter (parityTX) separately. We remind you that before doing so the selftest register enable wrong parity bit must be set to one. During the wrong parity exception procedure (wpar) we first pool for the receivers that caused this interrupt pending : receiver 8 will be tested first, and receiver 1 will be tested last.

Then, you will find how you can **program the label control matrix**. If you choose to check labels, the label matrix will be initialized to 1 (set1in), before asking you if you want to disable some sections of the matrix (turnlab) that will be set to zero (set0in).This matrix elements are byte or word access, but only D7 to D0 are relevant : so,beware of the addressing of these elements. You must also enable and then disable the writing bits in the receiver control registers. Thanks to this routine, you can also read back the matrix, if you wish to check your programmation.

The menu routine is the gathering of all the routines used to communicate with the console.

Then, you will find a set of routines similar to the previous programmation example, with a specific **MRT setup procedure**. We remind that transmitter 3 has the lowest priority level, transmitter 1 the highest. We are not in test mode, and the label control and parity check bits are set to 1 for the receivers by the label matrix programmation routine and by the parity programmation routine.

The **interruption routines** are similar to the ones provided with the previous example. Each transmitter is disabled after sending a message to allow the other ones (with a lowest priority level) to send their own message. The last transmitter that send a message enables again the other transmitters if other messages have to be sent (in this example we send only one message for each transmitter, d4 register value is forced to one).

After the program you can find the **output** of this program to the console.

```
NAME    addr.s
```

; GLOBAL REGISTER ADDRESSING FOR THE MRT AND THE ADS302 BOARD

; THIS SUBROUTINE PROVIDES YOU WITH THE CORRECT ADDRESS MAP
FOR THE MRT AND THE ADS302 BOARD REGISTERS

```
            XDEF    bar,base302,dep,cmr,sapr,dapr,bcr,csr,fcr,gimr,ipr,imr,isr
            XDEF    br0,or0,br1,or1,br2,or2,br3,or3,creg,spmode,simask,simode
            XDEF    pacnt,paddr,padat,pbcnt,pbddr,pbdat,tmr1,trr1

            XDEF    rx1_ctr,rx1_gap,rx1_msw,rx1_lsw
            XDEF    rx2_ctr,rx2_gap,rx2_msw,rx2_lsw
            XDEF    rx3_ctr,rx3_gap,rx3_msw,rx3_lsw
            XDEF    rx4_ctr,rx4_gap,rx4_msw,rx4_lsw
            XDEF    rx5_ctr,rx5_gap,rx5_msw,rx5_lsw
            XDEF    rx6_ctr,rx6_gap,rx6_msw,rx6_lsw
            XDEF    rx7_ctr,rx7_gap,rx7_msw,rx7_lsw
            XDEF    rx8_ctr,rx8_gap,rx8_msw,rx8_lsw
            XDEF    tx1_ctr,tx1_frq,tx1_msw,tx1_lsw
            XDEF    tx2_ctr,tx2_frq,tx2_msw,tx2_lsw,tx3_ctr
            XDEF    tx3_frq,tx3_msw,tx3_lsw
            XDEF    status,mask,base,label,selftest
            XDEF    CSMRT,STKTOP
            XDEF    cr,lf,intbase

intbase     equ     #$200
bar         equ     $00f2               ; 68302 register addresses
base302     equ     $0700
dep         equ     $800+(base302*4096)
cmr         equ     dep+2
sapr        equ     dep+4
dapr        equ     dep+8
bcr         equ     dep+$c
csr         equ     dep+$e
fcr         equ     dep+$10
gimr        equ     dep+$12
ipr         equ     dep+$14
imr         equ     dep+$16
isr         equ     dep+$18
pacnt       equ     dep+$1e
paddr       equ     dep+$20
padat       equ     dep+$22
pbcnt       equ     dep+$24
pbddr       equ     dep+$26
pbdat       equ     dep+$28
br0         equ     dep+$30
or0         equ     dep+$32
br1         equ     dep+$34
or1         equ     dep+$36
br2         equ     dep+$38
or2         equ     dep+$3a
br3         equ     dep+$3c
or3         equ     dep+$3e
tmr1        equ     dep+$40
trr1        equ     dep+$42
creg        equ     dep+$60
spmode      equ     dep+$b0
simask      equ     dep+$b2
simode      equ     dep+$b4
cr          equ     $0a
lf          equ     $0d

CSMRT       equ     $800000             ; mrt register addresses
rx1_ctr     equ     CSMRT+($0*2)
rx1_gap     equ     CSMRT+($1*2)
rx1_msw     equ     CSMRT+($2*2)
rx1_lsw     equ     CSMRT+($3*2)
rx2_ctr     equ     CSMRT+($4*2)
rx2_gap     equ     CSMRT+($5*2)
rx2_msw     equ     CSMRT+($6*2)
rx2_lsw     equ     CSMRT+($7*2)
rx3_ctr     equ     CSMRT+($8*2)
rx3_gap     equ     CSMRT+($9*2)
rx3_msw     equ     CSMRT+($A*2)
rx3_lsw     equ     CSMRT+($B*2)
rx4_ctr     equ     CSMRT+($C*2)
rx4_gap     equ     CSMRT+($D*2)
rx4_msw     equ     CSMRT+($E*2)
rx4_lsw     equ     CSMRT+($F*2)
rx5_ctr     equ     CSMRT+($10*2)
rx5_gap     equ     CSMRT+($11*2)
```

```
rx5_msw     equ     CSMRT+($12*2)
rx5_lsw     equ     CSMRT+($13*2)
rx6_ctr     equ     CSMRT+($14*2)
rx6_gap     equ     CSMRT+($15*2)
rx6_msw     equ     CSMRT+($16*2)
rx6_lsw     equ     CSMRT+($17*2)
rx7_ctr     equ     CSMRT+($18*2)
rx7_gap     equ     CSMRT+($19*2)
rx7_msw     equ     CSMRT+($1A*2)
rx7_lsw     equ     CSMRT+($1B*2)
rx8_ctr     equ     CSMRT+($1C*2)
rx8_gap     equ     CSMRT+($1D*2)
rx8_msw     equ     CSMRT+($1E*2)
rx8_lsw     equ     CSMRT+($1F*2)
tx1_ctr     equ     CSMRT+($20*2)
tx1_frq     equ     CSMRT+($21*2)
tx1_msw     equ     CSMRT+($22*2)
tx1_lsw     equ     CSMRT+($23*2)
tx2_ctr     equ     CSMRT+($24*2)
tx2_frq     equ     CSMRT+($25*2)
tx2_msw     equ     CSMRT+($26*2)
tx2_lsw     equ     CSMRT+($27*2)
tx3_ctr     equ     CSMRT+($28*2)
tx3_frq     equ     CSMRT+($29*2)
tx3_msw     equ     CSMRT+($2A*2)
tx3_lsw     equ     CSMRT+($2B*2)
status      equ     CSMRT+($40*2)
mask        equ     CSMRT+($41*2)
base        equ     CSMRT+($42*2)
selftest    equ     CSMRT+($43*2)
label       equ     CSMRT+($100*2)
STKTOP      equ     $30000
            end
```

NAME globint.s

;GLOBAL INTERRUPT ROUTING MANAGEMENT SYSTEM

```
            XREF    txe3a,txf3a,txe2a,txf2a,txe1a,txf1a
            XREF    rx1a,rx2a,rx3a,rx4a,rx5a,rx6a,rx7a,rx8a
            XREF    intbase,mask,wpar
            XDEF    glob_int

glob_int
            lea     intbase,a0
            move.l  #rx1a,(a0)+
            move.l  #rx2a,(a0)+
            move.l  #rx3a,(a0)+
            move.l  #rx4a,(a0)+
            move.l  #rx5a,(a0)+
            move.l  #rx6a,(a0)+
            move.l  #rx7a,(a0)+
            move.l  #rx8a,(a0)+
            move.l  #wpar,(a0)+
            addq    #4,a0
            move.l  #txe1a,(a0)+
            move.l  #txf1a,(a0)+
            move.l  #txe2a,(a0)+
            move.l  #txf2a,(a0)+
            move.l  #txe3a,(a0)+
            move.l  #txf3a,(a0)+

            ori.w   #$FDFF,mask         ; enable Rx,Tx. Parity ITs
            move.w  #$2000,sr           ; enable 68000 ITs

    rts
```

NAME in_out.s

```
; GENERIC IN/OUT SUBROUTINES, DESIGNED FOR THE ADS302 BOARD
;
; out8x, out4x, and out2x are designed in order to allow the user to print respectively
 8,4 or 2 hexa numbers from the d0 data register to the monitor
;
; write is designed in order to print an hexa number -which is in d0, to the monitor
;
; puts is designed in order to allow the user to print a string of caracters to the monitor
 when the string address is given in the a6 address register
;
; getc is designed in order to allow the user to get an ascii caracter from the monitor to
 the effective address given in a6
;
; getcn is designed in order to allow the user to get a numeric value from the monitor to
 the effective address given in a6 and to the d0 data register
;
; get8hx is designed in order to allow the user to get 8 hexa numbers from the monitor
 to the d0 data register

            XDEF    out8hx,out4hx,out2hx,prt,loop1,loop2,loop3,loop4,loop5
            XDEF    write,puts,getc,getcn,get8hx,get2hx,suite,sort1
;
sra         equ     $400001+(2*1)
tba         equ     $400001+(2*3)
rba         equ     tba
;-------------------------------------------------------------------------

out8hx      move.l  d1,-(a7)            ; print a long word, save d1
            moveq   #1,d1               ; nb of loops = 2

loop1       swap    d0                  ; swap long word
            jsr     out4hx              ; print word after word
            dbf     d1,loop1            ; next half of the long word
            move.l  (a7)+,d1            ; get back d1
            rts
;-------------------------------------------------------------------------

out4hx      move.l  d2,-(a7)            ; print a word, save d2
            moveq   #1,d2               ; nb of loops = 2

loop2       rol.w   #8,d0               ; swap word
            jsr     out2hx              ; print byte after byte
            dbf     d2,loop2            ; next half of the word
            move.l  (a7)+,d2            ; get back d2
            rts
;-------------------------------------------------------------------------

out2hx      move.l  d3,-(a7)            ; print a byte, save d3
            moveq   #1,d3               ; ng of loops = 2

loop3       rol.b   #4,d0               ; swap byte
            bsr     write
            dbf     d3,loop3            ; next half of the byte
            move.l  (a7)+,d3            ; get back d3
            rts
;-------------------------------------------------------------------------
write       move.l  d0,-(a7)            ; save element to write
            andi.l  #$F,d0              ; translation into ASCII
            addi.b  #$30,d0
            cmpi.b  #$3A,d0
            blt     write2
            addi.b  #$7,d0
write2      bsr     prt
            move.l  (a7)+,d0            ; get back element to write
            rts

prt         movem.l d0/d1/d2,-(a7)      ; print 1 ASCII char
prtatt      move.b  sra,d1
            btst    #2,d1               ; channel A ready ?
            beq     prtatt              ; br if no
            move.b  d0,tba              ; transmit char
            move.w  #500,d1
del3        muls.w  #$0,d2              ; kill some time
            dbf     d1,del3
            movem.l (a7)+,d0/d1/d2
            rts
;-------------------------------------------------------------------------
```

```
puts
                move.l      d0,-(a7)                ;save registers
puts2           move.b      (a6)+,d0
                beq         putend
                bsr         prt
                bra         puts2
putend          movem.l     (a7)+,d0                ; restore registers
                rts

;_____________________________________________________________________

getc            movem.l     a6/d1/d2/d3/d4/d5/d6/d7,-(a7) ; save registers
                movea.l     getabyte,a0             ; a0 = effective @
                clr.b       (a0)

loop4           trap        #15                     ; get a caracter
                dc.w        3
                tst         (a0)                    ; caracter got ?
                beq         loop4                   ; no, wait
                movem.l     (a7)+,a6/d1/d2/d3/d4/d5/d6/d7 ; yes, restore registers
                rts
                .align      2
getabyte:
                ds.w        1
;_____________________________________________________________________

getcn           jsr         getc                    ; get an ascii code
                move.b      (a0),d0                 ; in d0
                cmpi.b      #$3A,d0                 ; convert in hexa
                blt         suite
                subi.b      #$7,d0
suite           subi.b      #$30,d0
                bclr        #5,d0                   ; lower case to upper case
                rts
;_____________________________________________________________________

get8hx          movem.l     d1/d2,-(a7)
                clr.w       d2
                moveq       #7,d1                   ; 8 bytes to get
loop5           jsr         getcn                   ; get a byte
                jsr         write                   ; echo to the monitor
                or.l        d0,d2                   ; record the byte
                tst         d1                      ; last byte ?
                beq         sort1                   ; yes = stop
                asl.l       #4,d2                   ; no = prepare for the next byte
sort1           dbra        d1,loop5                ; next byte to get
                move.l      d2,d0
;               move.w      #300,d1
;del2           muls.w      #$0,d2                  ; kill some time
;               dbf         d1,del2
                movem.l     (a7)+,d1/d2
                rts

get2hx          movem.l     d1/d2,-(a7)
                clr.w       d2
                moveq       #1,d1                   ; 2 bytes to get
                bra         loop5
    rts
```

autotest.s

; SELFTEST

; THANKS TO THIS SUBROUTINE, YOU WILL BE ABLE TO RUN SELFTEST FOR THE MRT

```
                XDEF        progtest
                XREF        pass,err,report,result1,result2,result3,resultlab
                XREF        askself,selftest,puts
                XREF        rx1_ctr,rx2_ctr,rx3_ctr,rx4_ctr
                XREF        rx5_ctr,rx6_ctr,rx7_ctr,rx8_ctr

progtest        move.l      d0,-(a7)
                jsr         askself
                bne         retourself

;INITIALIZE ALL RECEIVER LCMWE BITS TO 1

                move.w      #$1000,d0
```

```
            move.w      d0,rx1_ctr
            move.w      d0,rx2_ctr
            move.w      d0,rx3_ctr
            move.w      d0,rx4_ctr
            move.w      d0,rx5_ctr
            move.w      d0,rx6_ctr
            move.w      d0,rx7_ctr
            move.w      d0,rx8_ctr

; INITIALIZE TEST CLOCK MODE BIT

            clr.w       selftest            ; there, CLK-SYS is higher than 10MHz
            ori.w       #$20,selftest

; BEGIN SELFTEST

            ori.w       #$40,selftest       ;transmitter test
            ori.w       #$80,selftest       ; matrix of label test

; WAIT FOR THE END OF THE TEST

waitlab     move.w      selftest,d0         ;wait for the end of label control matrix test
            btst.l      #14,d0
            beq         waitlab

; READ THE RESULT OF THE TEST

            lea         report,a6           ; print title
            jsr         puts

            move.w      selftest,d0

            lea         result1,a6          ; print 'transmitter 1 ='
            jsr         puts
            btst.l      #11,d0              ; test result bit
            bne         fail1               ; print 'failed' if result bit = 1
            jsr         passed              ; print 'passed' if result bit = 0

tx2         lea         result2,a6          ; print 'transmitter 2 ='
            jsr         puts
            btst.l      #12,d0              ; test result bit
            bne         fail2               ; print 'failed' if result bit = 1
            jsr         passed              ; print 'passed' if result bit = 0

tx3         lea         result3,a6          ; print 'transmitter 3 ='
            jsr         puts
            btst.l      #13,d0              ; test result bit
            bne         fail3               ; print 'failed' if result bit = 1
            jsr         passed              ; print 'passed' if result bit = 0

lab         lea         resultlab,a6        ; print 'label matrix  ='
            jsr         puts
            btst.l      #15,d0              ; test result bit
            bne         faillab             ; print 'failed' if result bit = 1
            jsr         passed              ; print 'passed' if result bit = 0

retourself  clr.w       selftest
            move.l      (a7)+,d0
            rts

fail1
            jsr         failed              ; print 'failed'
            bra         tx2                 ; next transmitter

fail2
            jsr         failed              ; print 'failed'
            bra         tx3                 ; next transmitter

fail3
            jsr         failed              ; print 'failed'
            bra         lab                 ; next result (label matrix)

faillab
            jsr         failed              ; print 'failed'
            bra         retourself          ; end

failed      lea         err,a6
            jsr         puts
            rts
```

```
passed      lea         pass,a6
            jsr         puts
      rts
```

NAME checkpar.s

; PARITY PROGRAMMATION ROUTINES

```
; THANKS TO THIS SUBROUTINE, YOU WILL BE ABLE TO PROGRAM PARITY
; CALCULATION FOR EACH TRANSMITTER AND PARITY CHECK FOR EACH
; RECEIVER SEPARATELY

            XDEF        wpar,parityRX,parityTX
            XREF        askpar0,askpar1,oddeven,askpar2,parmess,rxmess1
            XREF        selftest,rx1_ctr,tx1_ctr,mask,write,puts

parityRX
            movem.l     d1/d2/d6/a5,-(a7)
            clr.w       d6                      ; set askpar1 flag
            bsr         askpar0                 ; check parity [y/n] ?
            bne         endpar                  ; no, then end
            ori.w       #$1,selftest            ; yes, then enable wrong parity ITs
            ori.w       #$100,mask
            movea.l     #rx1_ctr,a5             ; set up a5 pointer
            moveq       #$7,d1                  ; 8 receivers to program
turnpar     move.l      d1,d2                   ; get right offset for current receiver
            asl.l       #3,d2                   ; control register addressing
            bsr         askpar1                 ; check parity for this receiver ?
            bne         nextpar                 ; no, then next receiver
            bsr         oddeven                 ; odd or even parity ?
            beq         even
            ori.w       #$0C00,(d2,a5)          ; programming odd parity
            bra         nextpar
even        ori.w       #$0400,(d2,a5)          ; programming even parity
nextpar     dbra        d1,turnpar              ; next receiver
endpar      movem.l     (a7)+,d1/d2/d6/a5
            rts

parityTX
            movem.l     d1/d2/d6/a5,-(a7)
            moveq       #1,d6                   ; set askpar1 flag
            bsr         askpar2                 ; compute parity [y/n] ?
            bne         endpar                  ; no, then end
            movea.l     #tx1_ctr,a5             ; set up a5 pointer
            moveq       #$2,d1                  ; 3 transmitters to program
            bra         turnpar                 ; programmation loop = the receiver one



wpar        movem.l     d0/d1/d2/a0/a5,-(a7)    ; wrong parity exception procedure
            movea.l     #rx1_ctr,a5             ; set up a5 pointer
            moveq       #7,d1                   ; 8 receivers to  poll
parit       move.l      d1,d2                   ; get the right address for receiver
            asl.l       #3,d2                   ; control register addressing
            addq        #1,d2                   ; LDS access
            bclr.b      #7,(d2,a5)              ; test wrong parity flag and clear it
            beq         nextparit               ; if 0 test the following one
            lea         rxmess1,a6              ; output wrong parity msg
            jsr         puts
            move.l      d1,d0
            addq        #1,d0
            jsr         write
            lea         parmess,a6
            jsr         puts
            cmpi.l      #0,d1                   ; increase received msg counter
            bne         nextparit               ; for receiver nb 1
            addq        #1,d3
nextparit   dbra        d1,parit                ; test the following one
            movem.l     (a7)+,d0/d1/d2/a0/a5
      rte
```

```
NAME    label.s
;
        XDEF    labelprog
        XREF    asklab0,readlab,space,asklab3,asklab2,asklab1,endrd
        XREF    rx1_ctr,label,out2hx,puts
```

; LABEL MATRIX PROGRAMMATION :

```
labelprog   movem.l  d1/d2/d3/d4/d5/d6/d7/a0/a5,-(a7)

            bsr      asklab0          ; do you want to program the matrix ?
            bne      retourlab        ; no, then return
            movea.l  #rx1_ctr,a5      ; initialise a5 pointer
            moveq    #7,d1            ; initialise d1, 7 vectors to program
turnlab
            move.l   d1,d2
            asl.l    #3,d2            ; get the offset for the receiver control
                                      ; register addressing
default                               ; default programmation is 1
            bsr      initlab
            bsr      set1             ; default is 1
            bsr      asklab1          ; program receiver nb #d1 ?
            bne      nextlab          ; no, then next vector
other       bsr      asklab2          ; what section do you want to disable ?
            movea.l  #label,a0        ; programmation zone pointer
            sub.l    d3,d4
            subq.l   #1,d4            ; get the right references in order to
            add.l    d3,d3            ; disable the good section of the vector
            adda.l   d3,a0            ; d3 = beginning , d4 = end of this section
            bsr      set0in           ; disable the chosen section of the vector
            bsr      asklab3          ; other section of the vector to disable ?
            beq      other            ; yes, then do it
            bra      nextlab          ; next vector to program

nextlab
            bsr      disable
            dbra     d1,turnlab       ; programmation loop
            bsr      verify           ; read the programmed matrix

retourlab
            movem.l  (a7)+,d1/d2/d3/d4/d5/d6/d7/a0/a5
            rts
verify
            bsr      readlab          ; do you want to check the programmation ?
            bne      retourlab        ; no,then exit
            move.w   #7,d7
            clr.l    d0
readon      ori.w    #$3000,(d0,a5)   ; enable reading
            addq     #$8,d0
            dbra     d7,readon
            lea      endrd,a6
            jsr      puts
            move.w   #$FF,d5          ; 256 elements to read
            movea.l  #label,a0        ; points to reading zone
            clr.l    d2               ; line lenght is 10h
look        addq     #1,d2
            addq     #1,a0
            move.b   (a0)+,d0         ; get the element
            jsr      out2hx           ; output
            lea      space,a6
            jsr      puts
            cmpi     #$10,d2          ; next line ?
            bne      looplook         ; no, then go on
            lea      endrd,a6         ; yes, then cr lf
            jsr      puts
            clr.b    d2
looplook    dbra     d5,look
            lea      endrd,a6
            jsr      puts
            move.w   #7,d7            ; disable reading mode
            clr.l    d0
readoff     andi.w   #$EFFF,(d0,a5)
            addq     #$8,d0
            dbra     d7,readoff
            rts
initlab
            move.l   #$FF,d0
            ori.w    #$3000,(d2,a5)   ;programming mode
```

```
                                                ;label control active .
            movea.l     #label,a0               ; programmation zone pointer
            move.l      #$FF,d5                 ; 256 elements to program
            move.l      #$FF,d0
            rts

set1in      move.l      #$FF,d0                 ; set the vector to 1
set1        addq        #1,a0
            move.b      d0,(a0)+
            dbf         d5,set1
            rts

set0in      clr.l       d0                      ; set the disable zone to 0
set0        addq        #1,a0
            move.b      d0,(a0)+
            dbf         d4,set0
            rts

disable
            andi.w      #$EFFF,(d2,a5)          ; disable the programming mode
      rts
```

NAME menu.s

; MENU

; THE ROUTINES PROVIDED WITH THIS PROGRAM CAN GET INFORMATION
; AND INSTRUCTIONS FROM THE USER THANKS TO THE FOLLOWING
; SUBROUTINES

```
            XREF        puts,getcn,write,get8hx,get2hx,getc,prt,par1,par2,rxpar,par3,par4
            XREF        nb,rxlab0,rxlab2,rxlab3,rxlab4,rdlab,self,msg,lab1,rxlab1,txmess
            XDEF        menu2,asklab0,asklab1,asklab2,asklab3,readlab,askself,ask
            XDEF        askpar0,askpar1,askpar2,oddeven

; Menu of sending

menu2
            lea         txmess,a6
            jsr         puts
            move.w      d7,d0
            jsr         write
            lea         msg,a6
            jsr         puts                    ; Ask for msg to be sent
            jsr         get8hx                  ; Wait for an answer
            move.l      d0,d6
            rts

; Menu of labels

asklab0     lea         lab1,a6
            jsr         ask
            rts

asklab1     lea         rxlab0,a6
            jsr         puts
            move.l      d1,d0
            addq        #1,d0
            jsr         write
            lea         rxlab1,a6
            jsr         ask
            rts

asklab2     lea         rxlab2,a6
            jsr         puts
            jsr         get2hx
            move.l      d0,d3                   ; in d3 : beginning of the section
            lea         rxlab3,a6
            jsr         puts
            jsr         get2hx
            move.l      d0,d4                   ; in d4 : end of the section
            rts

asklab3     lea         rxlab4,a6
            jsr         ask
            rts

readlab     lea         rdlab,a6
            jsr         ask
            rts
```

```
; Menu of Selftest

askself     lea       self,a6
            jsr       ask
            rts

; Menu of parity

askpar0
            lea       par1,a6
            jsr       ask
            rts

askpar1
            cmpi.w    #1,d6             ; test d6 flag
            beq       Tpar              ; if 0 then output transmitter msg
            lea       rxlab0,a6         ; if 1 then output receiver msg
            bra       go
Tpar        lea       par3,a6
go          jsr       puts
            move.l    d1,d0
            addq      #1,d0
            jsr       write
            lea       rxpar,a6
            jsr       ask
            rts

askpar2
            lea       par4,a6
            jsr       ask
            rts

oddeven
            lea       par2,a6
            jsr       puts
            jsr       getc
            move.b    (a0),d0
            bclr      #5,d0
            jsr       prt
            cmpi      #$45,d0
            rts


ask         jsr       puts
            jsr       getc
            move.b    (a0),d0           ; in d0
            bclr      #5,d0             ; lower case to upper case
            jsr       prt
            cmpi      #$59,d0
    rts
```

NAME mrtinit.s

;

; MRTINIT

; THANKS TO THIS SUBROUTINE, YOU WILL BE ABLE TO INITIALIZE THE MRT
; IN THIS EXAMPLE, PARITY PROGRAMMING IS ACHIEVED BY A SPECIFIC
; SUBROUTINE

```
            XDEF      initmrt
            XREF      status,base
            XREF      rx1_ctr,rx1_gap
            XREF      rx2_ctr,rx2_gap
            XREF      rx3_ctr,rx3_gap
            XREF      rx4_ctr,rx4_gap
            XREF      rx5_ctr,rx5_gap
            XREF      rx6_ctr,rx6_gap
            XREF      rx7_ctr,rx7_gap
            XREF      rx8_ctr,rx8_gap
            XREF      tx1_ctr,tx1_frq
            XREF      tx2_ctr,tx2_frq
            XREF      tx3_frq,tx3_ctr
```

; ARINC setup procedure :

```
initmrt     clr.w       status              ; only for receivers (byte)

            move.w      #$1E,rx1_gap        ; gap lenght = 3 arinc bits
            move.w      #$8007,rx1_ctr      ; priority 1, no parity, No Test
                                            ; gap lenght = 30 clk-arinc periods
            move.w      #$1E,rx2_gap        ; idem than rx1
            move.w      #$8006,rx2_ctr      ; priority 2, no parity, No Test

            move.w      #$1E,rx3_gap        ; idem than rx1
            move.w      #$8005,rx3_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx4_gap        ; idem than rx1
            move.w      #$8004,rx4_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx5_gap        ; idem than rx1
            move.w      #$8003,rx5_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx6_gap        ; idem than rx1
            move.w      #$8002,rx6_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx7_gap        ; idem than rx1
            move.w      #$8001,rx7_ctr      ; priority 3, no parity, No Test

            move.w      #$1E,rx8_gap        ; idem than rx1
            move.w      #$8000,rx8_ctr      ; priority 3, no parity, No Test

; TRANSMITTERS
; unused channels are : disable and fifo is reseted (reset fifo is not
; mandatory)

            move.w      #$0014,tx1_frq      ; TX rate = 100 Kbit/s
            move.w      #$8100,tx1_ctr      ; Reset FIFO
            move.w      #$8090,tx1_ctr

            move.w      #$0014,tx2_frq      ; TX rate = 100 Kbit/s
            move.w      #$8100,tx2_ctr      ; Reset FIFO
            move.w      #$8090,tx2_ctr

            move.w      #$0014,tx3_frq      ; TX rate = 100 Kbit/s
            move.w      #$8100,tx3_ctr      ; Reset FIFO
            move.w      #$8090,tx3_ctr      ; Means :
; In service, Test mode, no parity, FIFO in use
; Gap = %100 = 4 Arinc bits, No Test

            move.w      #$80,base           ; interrup vector points at #$200
    rts
```

```
NAME    int.s
        XREF    tx3_msw,tx3_lsw,tx2_msw,tx2_lsw,tx1_msw,tx1_lsw
        XREF    envoi,puts,out2hx,mask,write
        XDEF    txf3a,txe3a,txf2a,txe2a,txf1a,txe1a
        XREF    rx1_msw,rx1_lsw,rx2_msw,rx2_lsw
        XREF    rx3_msw,rx3_lsw,rx4_msw,rx4_lsw
        XREF    rx5_msw,rx5_lsw,rx6_msw,rx6_lsw
        XREF    rx7_msw,rx7_lsw,rx8_msw,rx8_lsw
        XREF    mask,out8hx,rxmess,puts,rxmess1
        XDEF    rx1a,rx2a,rx3a,rx4a,rx5a,rx6a,rx7a,rx8a
```

; INT Transmission

; THERE, YOU WILL FIND THE INTERRUPTION SUBROUTINES THAT ALLOW
; TRANSMITTER 1, 2, and 3 TO SEND MESSAGES
; REMEMBER : TRANMITTER 1 HAS THE HIGHEST PRIORITY LEVEL,
TRANSMITTER 3 THE LOWEST .

```
txf3a
txe3a
        ori.w   #$0700,sr       ; disable CPU ITs
        swap    d6
        move.w  d6,tx3_msw      ; Send message, first step
        swap    d6
        move.w  d6,tx3_lsw      ; Send message, second step

        lea     envoi,a6        ; print envoi
        jsr     puts
        move.w  #$3,d0
        jsr     write           ; print transmitter nb
        subi.w  #1,d4
        bpl     txf3a2
        andi.w  #$1FF,mask      ; end of transmission
        andi.w  #$f8ff,sr       ; enable CPU ITs
        rte

txf3a2
        ori.w   #$FDFF,mask
        andi.w  #$F8FF,sr       ; enable CPU ITs
        rte

txf2a
txe2a
        ori.w   #$0700,sr       ; disable CPU ITs
        swap    d2
        move.w  d2,tx2_msw      ; Send message, first step
        swap    d2
        move.w  d2,tx2_lsw      ; Send message, second step

        lea     envoi,a6        ; print envoi
        jsr     puts
        move.w  #$2,d0          ; print transmitter nb
        jsr     write□
        andi.w  #$C1FF,mask     ; disable TX2 ITs
        andi.w  #$f8ff,sr       ; enable CPU ITs
        rte

txf1a
txe1a
        ori.w   #$0700,sr       ; disable CPU ITs
        swap    d1
        move.w  d1,tx1_msw      ; Send message, first step
        swap    d1
        move.w  d1,tx1_lsw      ; Send message, second step

        lea     envoi,a6        ; print envoi
        jsr     puts
        move.w  #$1,d0          ; print transmitter nb
        jsr     write
        move.l  d4,d0
        andi.w  #$F1FF,mask     ; disable TX1 ITs
        andi.w  #$f8ff,sr       ; enable CPU ITs
        rte
```

5

; INT Reception

; THERE, YOU WILL FIND THE INTERRUPTION SUBROUTINES THAT ALLOW
; RECEIVERS 1 TO 8 TO RECEIVE MESSAGES

```
; Interrupt service routines :
;
; Receiver 1 :
; rem : IT IS MANDATORY TO READ MESS. AT LEAST IN WORD MODE.

rx1a
                move.l      d6,-(a7)
                moveq       #1,d6                   ; set receiver nb flag
                move.w      rx1_msw,d7              ; Read 32 bit message
                swap        d7
                move.w      rx1_lsw,d7              ; mess in D7
                addq.l      #1,d3                   ; received mess. counter
                lea         rxmess1,a6
                jsr         puts                    ; print receiver
                move.l      d6,d0
                jsr         write                   ; print receiver nb
                lea         rxmess,a6
                jsr         puts                    ; print rxmess
                move.l      d7,d0
                jsr         out8hx                  ; print mess content
                cmpi        #0,d4
                bge         ret1
ret2            andi.w      #$3fff,mask             ; disable transmission ITs
ret1            move.l      (a7)+,d6
                rte
;
; Receiver 2 :
;
rx2a
                move.l      d6,-(a7)
                moveq       #2,d6                   ; set receiver nb flag
                move.w      rx2_msw,d7              ; Read 32 bit message
                swap        d7
                move.w      rx2_lsw,d7              ; mess in D7
                lea         rxmess1,a6
                jsr         puts                    ; print receiver
                move.l      d6,d0
                jsr         write                   ; print receiver nb
                lea         rxmess,a6
                jsr         puts                    ; print rxmess
                move.l      d7,d0
                jsr         out8hx                  ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1
;
; Receiver 3 :
;
rx3a
                move.l      d6,-(a7)
                moveq       #3,d6                   ; set receiver nb flag
                move.w      rx3_msw,d7              ; Read 32 bit message
                swap        d7
                move.w      rx3_lsw,d7              ; mess in D7
                lea         rxmess1,a6
                jsr         puts                    ; print receiver
                move.l      d6,d0
                jsr         write                   ; print receiver nb
                lea         rxmess,a6
                jsr         puts                    ; print rxmess
                move.l      d7,d0
                jsr         out8hx                  ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1
;
; Receiver 4 :
;
rx4a
                move.l      d6,-(a7)
                moveq       #4,d6                   ; set receiver nb flag
                move.w      rx4_msw,d7              ; Read 32 bit message
                swap        d7
                move.w      rx4_lsw,d7              ; mess in D7

                lea         rxmess1,a6
```

```
                jsr         puts                ; print receiver
                move.l      d6,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess4
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1

; Receiver 5 :
;
rx5a
                move.l      d6,-(a7)
                moveq       #5,d6               ; set receiver nb flag
                move.w      rx5_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx5_lsw,d7          ; mess in D7
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      d6,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1

; Receiver 6 :
;
rx6a
                move.l      d6,-(a7)
                moveq       #6,d6               ; set receiver nb flag
                move.w      rx6_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx6_lsw,d7          ; mess in D7
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      d6,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1

; Receiver 7 :
;
rx7a
                move.l      d6,-(a7)
                moveq       #7,d6               ; set receiver nb flag
                move.w      rx7_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx7_lsw,d7          ; mess in D7
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      d6,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess2
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                cmpi        #0,d4
                blt         ret2
                bra         ret1

; Receiver 8 :
;
rx8a
                move.l      d6,-(a7)
                moveq       #8,d6               ; set receiver nb flag
                move.w      rx8_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx8_lsw,d7          ; mess in D7
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      d6,d0
```

```
                jsr         write                   ; print receiver nb
                lea         rxmess,a6
                jsr         puts                    ; print rxmess
                move.l      d7,d0
                jsr         out8hx                  ; print mess content
                cmpi        #0,d4
                blt         ret2
        bra     ret1
NAME    main302.s
; MAIN

; THIS ROUTINE SET UP THE ADS302 BOARD TO ENABLE IT TO
 COMMUNICATE WITH THE MRT
; THEN IT CALLS THE SPECIFIC SUBROUTINES TO ACHIEVE THE GOALS OF
 THIS PROGRAM
; THERE, YOU WILL ALSO FIND ALL THE MESSAGES USED TO
 COMMUNICATE WITH THE CONSOLE

                XREF        gimr,imr,br1,or1,STKTOP
                XREF        pbcnt,tmr1,trr1,parityTX
                XREF        mask,glob_int,initmrt,labelprog,progtest,parityRX
                XDEF        rxmess1,rxmess,parmess,txmess
                XDEF        rxlab0,rxlab1,rxlab2,rxlab3,rxlab4
                XDEF        result1,result2,result3,resultlab
                XDEF        err,report,space,pass,endrd,self,lab1
                XDEF        msg,envoi,rdlab,par1,par2,par3,par4,rxpar
                XREF        cr,lf,menu2
-------------------------------------------------------------------------------
                ori.w       #$700,sr
                lea         STKTOP,a7               ; init stack□
                move.w      #$b0a0,gimr             ; dedicated interruption mode
                clr.w       imr                     ; mask all INR interruptions
                move.w      #$0016,pbcnt            ; IACK1*, IACK6*, T1OUT activation
    ; CLK-ARINC programmation (T1OUT) :
                move.w      #$0001,trr1             ; toggle when count = 1
                move.w      #$092b,tmr1             ; Pre-scaler = 9, no capture, toggle, no IT, restart

; Master clock, enable
    ; programmation of CS1 :
                move.w      #$1001,br1              ; base address = 800000
                move.w      #$FFFC,or1              ; no DTACK, no FC, R/W enabled
                clr.w       mask                    ; mask TS68C429A interruptions

                clr.l       d1
                clr.l       d2
                clr.l       d3
                clr.l       d4
                clr.l       d5
                clr.l       d6
                clr.l       d7
                bsr         progtest                ; Selftest ?
                bsr         initmrt                 ; ARINC setup
                bsr         labelprog               ; program the label matrix
                bsr         parityTX                ; compute parity ?
                bsr         parityRX                ; check parity ?
                move.w      #$1,d5
                move.w      #$0,d4
                move.w      #$1,d7
                bsr         menu2                   ; sending of the messages
                move.l      d6,d1                   ; transmitter 1
                move.w      #$2,d7
                bsr         menu2
                move.w      #$3,d7
                move.l      d6,d2                   ; transmitter 2
                bsr         menu2                   ; transmitter 3
                bsr         glob_int                ; Interruption init
    fini
                cmp         d5,d3                   ; msg received ?
                beq         fin                     ; No, wait
                move.l      d4,d4                   ; end of transmit ?
                bpl         fini                    ; no : loop
    fin         clr.w       mask                    ; mask TS68C429A interruptions
                trap        #15
                dc.w        0                       ; Return monitor

    rxmess1
                dc.b        cr
                dc.b        lf
```

```
                dc.b        '     Receiver '
                dc.b        0

txmess
                dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Transmitter '
                dc.b        0
rxmess
                dc.b  ', mess = '
                dc.b        0

parmess
                dc.b        ', wrong parity detected !'
                dc.b        0

envoi
                dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Transmitter nb '
                dc.b        0

msg
                dc.b        cr
                dc.b        lf
                dc.b        ' Enter msg to be sent please # '
                dc.b        0

rxlab0          dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Do you want to program receiver '
                dc.b        0

par3            dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Do you want to program transmitter '
                dc.b        0

rxlab1          dc.b        'matrix [y/n] ? '
                dc.b        0

rxlab2          dc.b        cr
                dc.b        lf
                dc.b        ' Beginning of the section to disable [00-FF] ?'
                dc.b        0

rxlab3          dc.b        cr
                dc.b        lf
                dc.b        ' End of the section to disable [Beginning-FF] ?'
                dc.b        0

rxlab4          dc.b        cr
                dc.b        lf
                dc.b        ' Other section to disable [y/n] ? '
                dc.b        0

lab1            dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Do you want to program the Label Control Matrix [y/n] ? '
                dc.b        0

rdlab           dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Read  the programmed matrix [y/n] ? '
                dc.b        0

self            dc.b        cr
                dc.b        lf
                dc.b        ' Do you want to run self test [y/n] ? '
```

5

```
space       dc.b        ' '
            dc.b        0

endrd       dc.b        cr
            dc.b        lf
            dc.b        0

report      dc.b        cr
            dc.b        lf
            dc.b        cr
            dc.b        lf
            dc.b        'SELFTEST REPORT : '
            dc.b        cr
            dc.b        lf
            dc.b        0
pass
            dc.b        ' PASSED'
            dc.b        cr
            dc.b        lf
            dc.b        0

err
            dc.b        ' FAILED'
            dc.b        cr
            dc.b        lf
            dc.b        0

result1
            dc.b        'TRANSMITTER 1 = '
            dc.b        0

result2
            dc.b        'TRANSMITTER 2 = '
            dc.b        0

result3
            dc.b        'TRANSMITTER 3 = '
            dc.b        0

resultlab
            dc.b        'LABEL MATRIX = '
            dc.b        0

par1
            dc.b        cr
            dc.b        lf
            dc.b        cr
            dc.b        lf
            dc.b        ' Check parity [y/n] ? '
            dc.b        0

rxpar       dc.b        'parity [y/n] ? '
            dc.b        0

par2
            dc.b        cr
            dc.b        lf
            dc.b        ' Odd or Even [o/e] ? '
            dc.b        0

par4
            dc.b        cr
            dc.b        lf
            dc.b        cr
            dc.b        lf
            dc.b        ' Compute parity [y/n] ? '
            dc.b        0

    end
```

Output to the console example

```
302bug> go 30000
  Do you want to run self test [y/n] ?  Y

 SELFTEST REPORT :
 TRANSMITTER 1 =     PASSED
 TRANSMITTER 2 =     PASSED
 TRANSMITTER 3 =     PASSED
 LABEL MATRIX =      PASSED

Do you want to program the Label Control Matrix [y/n] ?  Y

Do you want to program receiver 8 matrix [y/n] ?  Y
Beginning of the section to disable [00-FF] ?10
End of the section to disable [Beginning-FF] ?20
Other section to disable [y/n] ?  Y
Beginning of the section to disable [00-FF] ?50
End of the section to disable [Beginning-FF] ?60
Other section to disable [y/n] ?  N

Do you want to program receiver 7 matrix [y/n] ?  N

Do you want to program receiver 6 matrix [y/n] ?  N

Do you want to program receiver 5 matrix [y/n] ?  N

Do you want to program receiver 4 matrix [y/n] ?  Y
Beginning of the section to disable [00-FF] ?A0
End of the section to disable [Beginning-FF] ?C0
Other section to disable [y/n] ?  N

Do you want to program receiver 3 matrix [y/n] ?  N

Do you want to program receiver 2 matrix [y/n] ?  N

Do you want to program receiver 1 matrix [y/n] ?  N

 Read the programmed matrix [y/n] ?  Y
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7
F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF

Compute parity [y/n] ?  Y

Do you want to program transmitter 3 parity [y/n] ?  Y
Odd or Even [o/e] ?  O

Do you want to program transmitter 2 parity [y/n] ?  Y
Odd or Even [o/e] ?  E

Do you want to program transmitter 1 parity [y/n] ?  Y
Odd or Even [o/e] ?  O

Check parity [y/n] ?  Y

Do you want to program receiver 8 parity [y/n] ?  Y
Odd or Even [o/e] ?  O

Do you want to program receiver 7 parity [y/n] ?  Y
Odd or Even [o/e] ?  E

Do you want to program receiver 6 parity [y/n] ?  Y
Odd or Even [o/e] ?  O

Do you want to program receiver 5 parity [y/n] ?  Y
Odd or Even [o/e] ?  E
```

```
Do you want to program receiver 4 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 3 parity [y/n] ? Y
Odd or Even [o/e] ? E

Do you want to program receiver 2 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 1 parity [y/n] ? Y
Odd or Even [o/e] ? E

Transmitter 1
Enter msg to be sent please # 12312312

Transmitter 2
Enter msg to be sent please # 12345678

Transmitter 3
Enter msg to be sent please # 87654321

Transmitter nb 1
    Receiver 7, wrong parity detected !
    Receiver 1, wrong parity detected !
    Receiver 4, mess = 92312312

Transmitter nb 2
    Receiver 8, wrong parity detected !
    Receiver 2, wrong parity detected !
    Receiver 5, mess = 92345678

Transmitter nb 3
    Receiver 3, wrong parity detected !
    Receiver 6, mess = 87654321
302bug>
```

d) A complete example with the MOTOROLA IDP040 board :

There, as for the previous example, the 8 receivers are enabled, but they are initialized in test mode and only transmitter 3 is used. As for the first program, you will be asked how many messages you want to send, and each message sent will be equal to the previous one plus one.

Nevertheless, you will find there the same set of routines than for the second example given for the MOTOROLA ADS302 board. There, we will only point out the differences between these two sets of routines.

The first routine you will find is used in order to remap the MOTOROLA IDP040 board address map and to allocate the address $600 0000 to the MRT. This program must be loaded on the MOTOROLA IDP040 board, for instance at address $8000. Then, you must use the command "mp s 8000" in order to transfer it to the MOTOROLA IDP040 board NVRAM. After a reset, you will have to re-use the "mp g" command in order to remap the MOTOROLA IDP040 memory space, if you want to use it with the MRT.

If you use the register addressing, we remind you that the pin A2 from the 68040 is connected to the MRT address line A0 (all address values must be multiplied by four).

The console being different, the in-out subroutines are slightly different from the ones provided for the MOTOROLA ADS302 board. The differences are situated in the procedures "getc" and "prt".

In the parity check, parity compute and label control matrix programmation subroutines, the only differences lie in the receiver control register address calculation.

There is an important difference in the interrupt service routines. This difference is due to the fact that the TS68040 detects the pending interrupts only on transitions of the IPL* lines. That is why the transitions of these lines are software forced. When we transmit a message, we first clear the mask. At the end of the transmission procedure, we set the mask in order to enable only the receivers and the wrong parity exception procedures. Inside these procedures, we use d2 as a counter. When 8 messages have been received, transmissions is enabled again. If less than 8 messages have been received (because of the label control matrix programmation, or because of a hardware problem) and if there is really no interrupt pending (after a determined amount of time without any interrupt request), then the "main" enables again the transmission interrupt requests, setting the appropriates bits within the mask register.

After the program, you can find the output of this program to the console.

```
NAME        mapsys.s

; MAPPING OF THE IDP040 BOARD IN ORDER TO USE IT WITH THE
  TS68C429A

SYSTEMBYTE  equ     $0          ; set starting logical addr of system
ENABLED     equ     0
DISABLED    equ     1

BUS_ARB     equ     ENABLED
INTERRUPTS  equ     DISABLED
BERR        equ     ENABLED     ; default is enabled

log_0       equ     $6000000    ; starting logical address
phy_0       equ     $0F00000    ; starting     physical address
siz_0       equ     1           ; 1*64=64 kbytes

log_1       equ     $0
phy_1       equ     $0
siz_1       equ     0

log_2       equ     0
phy_2       equ     0
siz_2       equ     0

log_3       equ     0
phy_3       equ     0
siz_3       equ     0

log_4       equ     0
phy_4       equ     0
siz_4       equ     0

log_5       equ     0
phy_5       equ     0
siz_5       equ     0

log_6       equ     0
phy_6       equ     0
siz_6       equ     0

log_7       equ     0
phy_7       equ     0
siz_7       equ     0

log_8       equ     0
phy_8       equ     0
siz_8       equ     0

log_9       equ     0
phy_9       equ     0
siz_9       equ     0

log_10      equ     0
phy_10      equ     0
siz_10      equ     0

log_11      equ     0
phy_11      equ     0
siz_11      equ     0

log_12      equ     0
phy_12      equ     0
siz_12      equ     0

log_13      equ     0
phy_13      equ     0
siz_13      equ     0

log_14      equ     0
phy_14      equ     0
siz_14      equ     0

log_15      equ     0
phy_15      equ     0
siz_15      equ     0

log_16      equ     0
phy_16      equ     0
siz_16      equ     0
```

```
log_17      equ     0
phy_17      equ     0
siz_17      equ     0

log_18      equ     0
phy_18      equ     0
siz_18      equ     0

log_19      equ     0
phy_19      equ     0
siz_19      equ     0

log_20      equ     0
phy_20      equ     0
siz_20      equ     0

            dc.b    BERR<<2+BUS_ARB<<1+INTERRUPTS
                                        ; inter status in bit position 0
                                        ; bus arb status in bit position 1
                                        ; bus err status in bit position 2
            dc.b    SYSTEMBYTE          ; starting logical addr for system
                                        ; hardware resources
            dc.l    log_0,phy_0         ; define logical and physical start
                                        ; addresses
            dc.b    siz_0,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_1,phy_1         ; define logical and physical start
                                        ; addresses
            dc.b    siz_1,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_2,phy_2         ; define logical and physical start
                                        ; addresses
            dc.b    siz_2,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_3,phy_3         ; define logical and physical start
                                        ; addresses
            dc.b    siz_3,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_4,phy_4         ; define logical and physical start
                                        ; addresses
            dc.b    siz_4,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_5,phy_5         ; define logical and physical start
                                        ; addresses
            dc.b    siz_5,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_6,phy_6         ; define logical and physical start
                                        ; addresses
            dc.b    siz_6,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_7,phy_7         ; define logical and physical start
                                        ; addresses
            dc.b    siz_7,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_8,phy_8         ; define logical and physical start
                                        ; addresses
            dc.b    siz_8,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_9,phy_9         ; define logical and physical start
                                        ; addresses
            dc.b    siz_9,0             ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_10,phy_10       ; define logical and physical start
                                        ; addresses
            dc.b    siz_10,0            ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_11,phy_11       ; define logical and physical start
                                        ; addresses
            dc.b    siz_11,0            ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_12,phy_12       ; define logical and physical start
                                        ; addresses
            dc.b    siz_12,0            ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_13,phy_13       ; define logical and physical start
                                        ; addresses
            dc.b    siz_13,0            ; define nb of 64k byte blocks
                                        ; to be translated
            dc.l    log_14,phy_14       ; define logical and physical start
                                        ; addresses
```

5

```
        dc.b    siz_14,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_15,phy_15       ; define logical and physical start
                                    ; addresses
        dc.b    siz_15,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_16,phy_16       ; define logical and physical start
                                    ; addresses
        dc.b    siz_16,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_17,phy_17       ; define logical and physical start
                                    ; addresses
        dc.b    siz_17,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_18,phy_18       ; define logical and physical start
                                    ; addresses
        dc.b    siz_18,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_19,phy_19       ; define logical and physical start
                                    ; addresses
        dc.b    siz_19,0            ; define nb of 64k byte blocks
                                    ; to be translated
        dc.l    log_20,phy_20       ; define logical and physical start
                                    ; addresses
        dc.b    siz_20,0            ; define nb of 64k byte blocks
                                    ; to be translated

NAME    addr.s
```

; GLOBAL REGISTER ADDRESSING FOR THE MRT AND THE IDP040 BOARD

; THIS SUBROUTINE PROVIDES YOU WITH THE CORRECT ADDRESS MAP FOR THE MRT AND THE IDP040 BOARD REGISTERS

```
        XDEF    cprh,cprl,cprm,tcr,pcddr,pgcr,imr
        XDEF    rx1_ctr,rx1_gap,rx1_msw,rx1_lsw
        XDEF    rx2_ctr,rx2_gap,rx2_msw,rx2_lsw
        XDEF    rx3_ctr,rx3_gap,rx3_msw,rx3_lsw
        XDEF    rx4_ctr,rx4_gap,rx4_msw,rx4_lsw
        XDEF    rx5_ctr,rx5_gap,rx5_msw,rx5_lsw
        XDEF    rx6_ctr,rx6_gap,rx6_msw,rx6_lsw
        XDEF    rx7_ctr,rx7_gap,rx7_msw,rx7_lsw
        XDEF    rx8_ctr,rx8_gap,rx8_msw,rx8_lsw
        XDEF    tx1_ctr,tx1_frq,tx1_msw,tx1_lsw
        XDEF    tx2_ctr,tx2_frq,tx2_msw,tx2_lsw,tx3_ctr
        XDEF    tx3_frq,tx3_msw,tx3_lsw
        XDEF    status,mask,base,label,selftest
        XDEF    CSMRT,STKTOP
        XDEF    cr,lf,intbase

intbase equ     #$200

pit     equ     $00C0003
pgcr    equ     pit+(0)             ; port general control register
pssr    equ     pit+(1*4)           ; port service request register
pcddr   equ     pit+(4*4)           ; port C data direction register
pcdr    equ     pit+(12*4)          ; port C data register
tcr     equ     pit+(16*4)          ; timer control register
cprh    equ     pit+(19*4)          ; counter preload high
cprm    equ     pit+(20*4)          ; counter preload mid
cprl    equ     pit+(21*4)          ; counter preload low
duart   equ     $00B0003
imr     equ     duart+(5*4)
cr      equ     $0a
lf      equ     $0d

CSMRT   equ     $6000002            ; mrt register addresses
rx1_ctr equ     CSMRT+($0*4)
rx1_gap equ     CSMRT+($1*4)
rx1_msw equ     CSMRT+($2*4)
rx1_lsw equ     CSMRT+($3*4)
rx2_ctr equ     CSMRT+($4*4)
rx2_gap equ     CSMRT+($5*4)
rx2_msw equ     CSMRT+($6*4)
rx2_lsw equ     CSMRT+($7*4)
rx3_ctr equ     CSMRT+($8*4)
rx3_gap equ     CSMRT+($9*4)
rx3_msw equ     CSMRT+($A*4)
rx3_lsw equ     CSMRT+($B*4)
```

```
rx4_ctr     equ     CSMRT+($C*4)
rx4_gap     equ     CSMRT+($D*4)
rx4_msw     equ     CSMRT+($E*4)
rx4_lsw     equ     CSMRT+($F*4)
rx5_ctr     equ     CSMRT+($10*4)
rx5_gap     equ     CSMRT+($11*4)
rx5_msw     equ     CSMRT+($12*4)
rx5_lsw     equ     CSMRT+($13*4)
rx6_ctr     equ     CSMRT+($14*4)
rx6_gap     equ     CSMRT+($15*4)
rx6_msw     equ     CSMRT+($16*4)
rx6_lsw     equ     CSMRT+($17*4)
rx7_ctr     equ     CSMRT+($18*4)
rx7_gap     equ     CSMRT+($19*4)
rx7_msw     equ     CSMRT+($1A*4)
rx7_lsw     equ     CSMRT+($1B*4)
rx8_ctr     equ     CSMRT+($1C*4)
rx8_gap     equ     CSMRT+($1D*4)
rx8_msw     equ     CSMRT+($1E*4)
rx8_lsw     equ     CSMRT+($1F*4)
tx1_ctr     equ     CSMRT+($20*4)
tx1_frq     equ     CSMRT+($21*4)
tx1_msw     equ     CSMRT+($22*4)
tx1_lsw     equ     CSMRT+($23*4)
tx2_ctr     equ     CSMRT+($24*4)
tx2_frq     equ     CSMRT+($25*4)
tx2_msw     equ     CSMRT+($26*4)
tx2_lsw     equ     CSMRT+($27*4)
tx3_ctr     equ     CSMRT+($28*4)
tx3_frq     equ     CSMRT+($29*4)
tx3_msw     equ     CSMRT+($2A*4)
tx3_lsw     equ     CSMRT+($2B*4)
status      equ     CSMRT+($40*4)
mask        equ     CSMRT+($41*4)
base        equ     CSMRT+($42*4)
selftest    equ     CSMRT+($43*4)
label       equ     CSMRT+($100*4)
STKTOP      equ     $8000
            end
```

5

```
NAME        globint.s
```

;GLOBAL INTERRUPT ROUTING MANAGEMENT SYSTEM

```
            XREF    txe3a,txf3a,txe2a,txf2a,txe1a,txf1a
            XREF    rx1a,rx2a,rx3a,rx4a,rx5a,rx6a,rx7a,rx8a
            XREF    intbase,mask,wpar.
            XDEF    glob_int

glob_int
            lea     intbase,a0
            move.l  #rx1a,(a0)+
            move.l  #rx2a,(a0)+
            move.l  #rx3a,(a0)+
            move.l  #rx4a,(a0)+
            move.l  #rx5a,(a0)+
            move.l  #rx6a,(a0)+
            move.l  #rx7a,(a0)+
            move.l  #rx8a,(a0)+
            move.l  #wpar,(a0)+
            addq    #4,a0
            move.l  #txe1a,(a0)+
            move.l  #txf1a,(a0)+
            move.l  #txe2a,(a0)+
            move.l  #txf2a,(a0)+
            move.l  #txe3a,(a0)+
            move.l  #txf3a,(a0)+

            ori.w   #$81FF,mask         ; enable Rx,Tx3 ITs
            move.w  #$2000,sr           ; enable 68000 ITs

    rts
```

```
NAME        in_out.s
; GENERIC IN/OUT SUBROUTINES, DESIGNED FOR THE IDP040 BOARD
;
; out8x, out4x, and out2x are designed in order to allow the user to print respectively
 8,4 or 2 hexa numbers from the d0 data register  to the monitor
;
; write is designed in order to print an hexa number -which is in d0, to the monitor
;
; puts is designed in order to allow the user to print a string of caracters to the monitor
 when the string address is given in the a6 address register
;
; getc is designed in order to allow the user to get an ascii caracter from the monitor to
 the effective address given in a6
;
; getcn is designed in order to allow the user to get a numeric value from the monitor to
 the effective address given in a6 and to the d0 data register
;
; get8hx is designed in order to allow the user to get 8 hexa numbers from the monitor
 to the d0 data register

            XDEF    out8hx,out4hx,out2hx,prt,loop1,loop2,loop3,loop4,loop5
            XDEF    write,puts,getc,getcn,get8hx,get2hx,suite,sort1
;-------------------------------------------------------------------------------
out8hx      movem.l a0/d1,-(a7)         ; print a long word, save d1
            moveq   #1,d1               ; nb of loops = 2

loop1       swap    d0                  ; swap long word
            jsr     out4hx              ; print word after word
            dbf     d1,loop1            ; next half of the long word
            movem.l (a7)+,a0/d1         ; get back d1
            rts
;-------------------------------------------------------------------------------
out4hx      movem.l a0/d2,-(a7)         ; print a word, save d2
            moveq   #1,d2               ; nb of loops = 2

loop2       rol.w   #8,d0               ; swap word
            jsr     out2hx              ; print byte after byte
            dbf     d2,loop2            ; next half of the word
            movem.l (a7)+,a0/d2         ; get back d2
            rts
;-------------------------------------------------------------------------------
out2hx      movem.l a0/d3,-(a7)         ; print a byte, save d3
            moveq   #1,d3               ; ng of loops = 2

loop3       rol.b   #4,d0               ; swap byte
            bsr     write
            dbf     d3,loop3            ; next half of the byte
            movem.l (a7)+,a0/d3         ; get back d3
            rts
;-------------------------------------------------------------------------------
write       movem.l a0/d0,-(a7)         ; save element to write
            andi.l  #$F,d0              ; translation into ASCII
            addi.b  #$30,d0
            cmpi.b  #$3A,d0
            blt     write2
            addi.b  #$7,d0
write2      bsr     prt
            movem.l (a7)+,a0/d0         ; get back element to write
            rts

prt         movem.l a0/a6/d0/d1/d2/d3/d4/d5/d6/d7,-(a7)          ; save registers
            move.w  d0,d1
            move.w  #$13,d0
            trap    #15
            movem.l (a7)+,a0/a6/d0/d1/d2/d3/d4/d5/d6/d7         ; yes, restore registers
            rts
;-------------------------------------------------------------------------------
puts
            movem.l a0/d0,-(a7)         ;save registers
puts2       move.b  (a6)+,d0
            beq     putend
            bsr     prt
            bra     puts2
```

```
putend      movem.l   (a7)+,a0/d0          ; restore registers
            rts
;_____________________________________________________________________
getc        movem.l   a0/a6/d1/d2/d3/d4/d5/d6/d7,-(a7);          ; save registers
loop4       move.w    #$10,d0
            trap      #15
            cmpi.w    #1,d0
            beq       loop4
            move.l    d1,d0
            movem.l   (a7)+,a0/a6/d1/d2/d3/d4/d5/d6/d7          ; yes, restore registers
            rts
;_____________________________________________________________________
getcn       jsr       getc              ; get an ascii code
            cmpi.b    #$3A,d0           ; convert in hexa
            blt       suite
            subi.b    #$7,d0
suite       subi.b    #$30,d0
            bclr      #5,d0             ; lower case to upper case
            rts
;_____________________________________________________________________
get8hx      movem.l   a0/d1/d2,-(a7)
            clr.w     d2
            moveq     #7,d1             ; 8 bytes to get
loop5       jsr       getcn             ; get a byte
            jsr       write             ; echo to the monitor
            or.l      d0,d2             ; record the byte
            tst       d1                ; last byte ?
            beq       sort1             ; yes = stop
            asl.l     #4,d2             ; no = prepare for the next byte
sort1       dbra      d1,loop5          ; next byte to get
            move.l    d2,d0
            movem.l   (a7)+,a0/d1/d2
            rts

get2hx      movem.l   a0/d1/d2,-(a7)
            clr.w     d2
            moveq     #1,d1             ; 2 bytes to get
            bra       loop5
    rts
```

NAME menu.s

; MENU

```
            XREF      puts,getcn,write,get8hx,get2hx,getc,prt,par1,par2,rxpar,par3,par4
            XREF      nb,rxlab0,rxlab2,rxlab3,rxlab4,rdlab,self,msg,lab1,rxlab1
            XDEF      menu,asklab0,asklab1,asklab2,asklab3,readlab,askself,ask
            XDEF      askpar0,askpar1,askpar2,oddeven

; Menu of sending

menu        lea       nb,a6
            jsr       puts              ; Ask for nb of msg to be sent
            jsr       getcn             ; Wait for an answer
            jsr       write
            move.l    d0,d5             ; Fill nb of msg buffer
            subq.l    #1,d0
            move.l    d0,d4             ; Initialise transmiter 3  message counter
            lea       msg,a6
            jsr       puts              ; Ask for msg to be sent
            jsr       get8hx            ; Wait for an answer
            move.l    d0,d6
            rts

asklab0     lea       lab1,a6
            jsr       ask
            rts

asklab1     lea       rxlab0,a6
            jsr       puts
            move.l    d1,d0
            addq      #1,d0
```

5

```
                jsr         write
                lea         rxlab1,a6
                jsr         ask
                rts

asklab2         lea         rxlab2,a6
                jsr         puts
                jsr         get2hx
                move.l      d0,d3           ; in d3 : beginning of the section
                lea         rxlab3,a6
                jsr         puts
                jsr         get2hx
                move.l      d0,d4           ; in d4 : end of the section
                rts

asklab3         lea         rxlab4,a6
                jsr         ask
                rts

readlab         lea         rdlab,a6
                jsr         ask
                rts

askself         lea         self,a6
                jsr         ask
                rts

askpar0
                lea         par1,a6
                jsr         ask
                rts

askpar1
                cmpi.w      #1,d6           ; test d6 flag
                beq         Tpar            ; if 0 then output transmitter msg
                lea         rxlab0,a6       ; if 1 then output receiver msg
                bra         go
Tpar            lea         par3,a6
go              jsr         puts
                move.l      d1,d0
                addq        #1,d0
                jsr         write
                lea         rxpar,a6
                jsr         ask
                rts

askpar2
                lea         par4,a6
                jsr         ask
                rts

oddeven
                lea         par2,a6
                jsr         puts
                jsr         getc
                bclr        #5,d0
                jsr         prt
                cmpi        #$45,d0
                rts


ask             jsr         puts
                jsr         getc
                bclr        #5,d0           ; lower case to upper case
                jsr         prt
                cmpi.b      #$59,d0
    rts
```

NAME mrtinit.s

```
        XDEF    initmrt
        XREF    status,base
        XREF    rx1_ctr,rx1_gap
        XREF    rx2_ctr,rx2_gap
        XREF    rx3_ctr,rx3_gap
        XREF    rx4_ctr,rx4_gap
        XREF    rx5_ctr,rx5_gap
        XREF    rx6_ctr,rx6_gap
        XREF    rx7_ctr,rx7_gap
        XREF    rx8_ctr,rx8_gap
```

```
                XREF    tx1_ctr,tx1_frq
                XREF    tx2_ctr,tx2_frq
                XREF    tx3_frq,tx3_ctr
```

; ARINC setup procedure

```
initmrt         clr.w   status          ; only for receivers (byte)

                move.w  #$1E,rx1_gap    ; gap lenght = 3 arinc bits
                move.w  #$C007,rx1_ctr  ; priority 1, no parity, Test
                                        ; gap lenght = 30 clk-arinc periods
                move.w  #$1E,rx2_gap    ; idem than rx1
                move.w  #$C006,rx2_ctr  ; priority 2, no parity, Test

                move.w  #$1E,rx3_gap    ; idem than rx1
                move.w  #$C005,rx3_ctr  ; priority 3, no parity, Test

                move.w  #$1E,rx4_gap    ; idem than rx1
                move.w  #$C004,rx4_ctr  ; priority 3, no parity, Test

                move.w  #$1E,rx5_gap    ; idem than rx1
                move.w  #$C003,rx5_ctr  ; priority 3, no parity, Test

                move.w  #$1E,rx6_gap    ; idem than rx1
                move.w  #$C002,rx6_ctr  ; priority 3, no parity, Test

                move.w  #$1E,rx7_gap    ; idem than rx1
                move.w  #$C001,rx7_ctr  ; priority 3, no parity, Test

                move.w  #$1E,rx8_gap    ; idem than rx1
                move.w  #$C000,rx8_ctr  ; priority 3, no parity, Test

; TRANSMITTERS
; unused channels are : disable and fifo is reseted (reset fifo is not
; mandatory)

                move.w  #$10,tx1_ctr
                move.w  #$10,tx2_ctr

                move.w  #$0014,tx3_frq  ; TX rate = 100 Kbit/s
                move.w  #$8100,tx3_ctr  ; Reset FIFO
                move.w  #$8090,tx3_ctr  ; Means :
; In service, Test mode, no parity, FIFO in use
; Gap = %1000 = 8 Arinc bits

                move.w  #$80,base       ; interrup vector points at #$200
                rts
```

NAME autotest.s

; SELFTEST

```
                XDEF    progtest
                XREF    pass,err,report,result1,result2,result3,resultlab
                XREF    askself,selftest,puts
                XREF    rx1_ctr,rx2_ctr,rx3_ctr,rx4_ctr
                XREF    rx5_ctr,rx6_ctr,rx7_ctr,rx8_ctr

progtest        move.l  d0,-(a7)
                jsr     askself
                bne     retourself

;INITIALIZE ALL RECEIVER LCMWE BITS TO 1

                move.w  #$1000,d0
                move.w  d0,rx1_ctr
                move.w  d0,rx2_ctr
                move.w  d0,rx3_ctr
                move.w  d0,rx4_ctr
                move.w  d0,rx5_ctr
                move.w  d0,rx6_ctr
                move.w  d0,rx7_ctr
                move.w  d0,rx8_ctr

; INITIALIZE TEST CLOCK MODE BIT

                clr.w   selftest        ; there, CLK-SYS is higher than 10MHz
```

```
                ori.w       #$20,selftest

; BEGIN SELFTEST

                ori.w       #$40,selftest       ;transmitter test
                ori.w       #$80,selftest       ; matrix of label test

; WAIT FOR THE END OF THE TEST

waitlab         move.w      selftest,d0         ;wait for the end of label control matrix test
                btst.l      #14,d0
                beq         waitlab

; READ THE RESULT OF THE TEST

                lea         report,a6           ; print title
                jsr         puts

                move.w      selftest,d0

                lea         result1,a6          ; print 'transmitter 1 ='
                jsr         puts
                btst.l      #11,d0              ; test result bit
                bne         fail1               ; print 'failed' if result bit = 1
                jsr         passed              ; print 'passed' if result bit = 0

tx2             lea         result2,a6          ; print 'transmitter 2 ='
                jsr         puts
                btst.l      #12,d0              ; test result bit
                bne         fail2               ; print 'failed' if result bit = 1
                jsr         passed              ; print 'passed' if result bit = 0


tx3             lea         result3,a6          ; print 'transmitter 3 ='
                jsr         puts
                btst.l      #13,d0              ; test result bit
                bne         fail3               ; print 'failed' if result bit = 1
                jsr         passed              ; print 'passed' if result bit = 0

lab             lea         resultlab,a6        ; print 'label matrix  ='
                jsr         puts
                btst.l      #15,d0              ; test result bit
                bne         faillab             ; print 'failed' if result bit = 1
                jsr         passed              ; print 'passed' if result bit = 0

retourself      clr.w       selftest
                move.l      (a7)+,d0
                rts

fail1
                jsr         failed              ; print 'failed'
                bra         tx2                 ; next transmitter

fail2
                jsr         failed              ; print 'failed'
                bra         tx3                 ; next transmitter

fail3
                jsr         failed              ; print 'failed'
                bra         lab                 ; next result (label matrix)
faillab
                jsr         failed              ; print 'failed'
                bra         retourself          ; end
failed          lea         err,a6
                jsr         puts
                rts
passed          lea         pass,a6
                jsr         puts
    rts
```

NAME checkpar.s

; PARITY PROGRAMMATION ROUTINES

```
                XDEF        wpar,parityRX,parityTX
                XREF        askpar0,askpar1,oddeven,askpar2,parmess,rxmess1
                XREF        selftest,rx1_ctr,tx1_ctr,mask,write,puts,returnit

parityRX
```

```
                movem.l     d1/d2/d6/a5,-(a7)
                clr.w       d6                      ; set askpar1 flag
                bsr         askpar0                 ; check parity [y/n] ?
                bne         endpar                  ; no, then end
                ori.w       #$1,selftest            ; yes, then enable wrong parity ITs
                ori.w       #$100,mask
                movea.l     #rx1_ctr,a5             ; set up a5 pointer
                moveq       #$7,d1                  ; 8 receivers to program
                move.l      #$70,d2
turnpar         bsr         askpar1                 ; check parity for this receiver ?
                bne         nextpar                 ; no, then next receiver
                bsr         oddeven                 ; odd or even parity ?
                beq         even
                ori.w       #$0C00,(d2,a5)          ; programming odd parity
                bra         nextpar
even            ori.w       #$0400,(d2,a5)          ; programming even parity
nextpar         sub.l       #$10,d2                 ; get right offset for current receiver
                dbra        d1,turnpar              ; next receiver
endpar          movem.l     (a7)+,d1/d2/d6/a5
                rts

parityTX
                movem.l     d1/d2/d6/a5,-(a7)
                moveq       #1,d6                   ; set askpar1 flag
                bsr         askpar2                 ; compute parity [y/n] ?
                bne         endpar                  ; no, then end
                movea.l     #tx1_ctr,a5             ; set up a5 pointer
                moveq       #$2,d1                  ; 3 transmitters to program
                move.l      #$20,d2
                bra         turnpar                 ; programmation loop = the receiver one


wpar
                movem.l     d0/d6/d7/a0/a5,-(a7)    ; wrong parity exception procedure
                movea.l     #rx1_ctr,a5             ; set up a5 pointer
                addq        #$1,a5                  ; LDS access
                moveq       #7,d7                   ; 8 receivers to  poll
                move.l      #$70,d6
parit
                bclr.b      #7,(d6,a5)              ; test wrong parity flag and clear it
                beq         nextparit               ; if 0 test the following one
                addq.l      #1,d2
                lea         rxmess1,a6              ; output wrong parity msg
                jsr         puts
                move.l      d7,d0
                addq        #1,d0
                jsr         write
                lea         parmess,a6
                jsr         puts
                cmpi.l      #0,d7                   ; increase received msg counter
                bne         nextparit               ; for receiver nb 1
                addq        #1,d3
nextparit       sub.l       #$10,d6                 ; get the right address for receiver
                dbra        d7,parit                ; test the following one
                movem.l     (a7)+,d0/d6/d7/a0/a5
        bra         returnit
```

```
NAME    label.s
;
        XDEF    labelprog
        XREF    asklab0,readlab,space,asklab3,asklab2,asklab1,endrd
        XREF    rx1_ctr,label,out2hx,puts

; LABEL MATRIX PROGRAMMATION :

labelprog   movem.l d1/d2/d3/d4/d5/d6/d7/a0/a5,-(a7)
            bsr     asklab0         ; do you want to program the matrix ?
            bne     retourlab       ; no, then return
            movea.l #rx1_ctr,a5     ; initialise a5 pointer
            moveq   #7,d1           ; initialise d1, 7 vectors to program

            move.l  #$70,d2         ; get the offset for the receiver control
                                    ; register addressing
turnlab
default                             ; default programmation is 1
            bsr     initlab
            bsr     set1            ; default is 1
            bsr     asklab1         ; program receiver nb #d1 ?
            bne     nextlab         ; no, then next vector
other       bsr     asklab2         ; what section do you want to disable ?
            movea.l #label,a0       ; programmation zone pointer
            addi.l  #$1,a0          ; LDS access
            sub.l   d3,d4
            subq.l  #1,d4           ; get the right references in order to
            add.l   d3,d3           ; disable the good section of the vector
            add.l   d3,d3
            adda.l  d3,a0           ; d3 = beginning , d4 = end of this section
            bsr     set0in          ; disable the chosen section of the vector
            bsr     asklab3         ; other section of the vector to disable ?
            beq     other           ; yes, then do it
            bra     nextlab         ; next vector to program

nextlab
            bsr     disable
            sub.l   #$10,d2
            dbra    d1,turnlab      ; programmation loop
            bsr     verify          ; read the programmed matrix


retourlab
            movem.l (a7)+,d1/d2/d3/d4/d5/d6/d7/a0/a5
            rts

verify      bsr     readlab         ; do you want to check the programmation ?
            beq     go              ; no,then exit
            rts
go          move.w  #7,d7
            move.w  #$70,d2
readon      ori.w   #$3000,(d2,a5)  ; enable reading
            subi.l  #$10,d2
            dbra    d7,readon
            lea     endrd,a6
            jsr     puts
            move.w  #$FF,d5         ; 256 elements to read
            movea.l #label,a0       ; points to reading zone
            addq    #$1,a0          ; LDS access
            clr.l   d6              ; line lenght is 10h
look        addq    #1,d6
            move.b  (a0)+,d0        ; get the element
            addq    #3,a0
            jsr     out2hx          ; output
            lea     space,a6
            jsr     puts
            cmpi    #$10,d6         ; next line ?
            bne     looplook        ; no, then go on
            lea     endrd,a6        ; yes, then cr lf
            jsr     puts
            clr.b   d6
looplook    dbra    d5,look
            lea     endrd,a6
            jsr     puts
            move.w  #7,d7           ; disable reading mode
            move.w  #$70,d2
readoff     andi.w  #$EFFF,(d2,a5)
            subi.l  #$10,d2
            dbra    d7,readoff
            rts
```

```
initlab
                move.l      #$FF,d0
                ori.w       #$3000,(d2,a5)      ;programming mode
                                                ;label control active
                movea.l     #label,a0           ; programmation zone pointer
                addq.l      #$1,a0
                move.l      #$FF,d5             ; 256 elements to program
                move.l      #$FF,d0
                rts

set1in          move.l      #$FF,d0             ; set the vector to 1
set1            move.b      d0,(a0)+
                addq        #$3,a0
                dbf         d5,set1
                rts

set0in          clr.l       d0                  ; set the disable zone to 0
set0            move.b      d0,(a0)+
                addq        #$3,a0
                dbf         d4,set0
                rts

disable
                andi.w      #$EFFF,(d2,a5)      ; disable the programming mode
    rts

NAME            int.s
; INT Transmission

                XREF        tx3_msw,tx3_lsw,tx2_msw,tx2_lsw,tx1_msw,tx1_lsw
                XREF        envoi,puts,out2hx,mask,write
                XDEF        txf3a,txe3a,txf2a,txe2a,txf1a,txe1a
                XREF        rx1_msw,rx1_lsw,rx2_msw,rx2_lsw
                XREF        rx3_msw,rx3_lsw,rx4_msw,rx4_lsw
                XREF        rx5_msw,rx5_lsw,rx6_msw,rx6_lsw
                XREF        rx7_msw,rx7_lsw,rx8_msw,rx8_lsw
                XREF        mask,out8hx,rxmess,puts,rxmess1
                XDEF        rx1a,rx2a,rx3a,rx4a,rx5a,rx6a,rx7a,rx8a,returnit
```

; THERE, YOU WILL FIND THE INTERRUPTION SUBROUTINE THAT ALLOWS TRANSMITTER 3 TO SEND MESSAGES

```
; sending a message

txf3a
                clr.w       mask                ; clear mask in order to force IPL signals to 1
send            swap        d6□
                move.w      d6,tx3_msw          ; Send message, first step
                swap        d6
                move.w      d6,tx3_lsw          ; Send message, second step
                addq.w      #1,d6               ; Define new message

                lea         envoi,a6            ; print envoi
                jsr         puts
                move.l      d4,d0
                jsr         out2hx              ; print nb of msg
                subi.w      #1,d4
                clr.w       d2
                move.w      #$1FF,mask          ; enable ITs to allow IPL signals low
                rte                             ; for reception only
;_____________________________________________________________________
; INT
; Interrupt service routines :
```

; THERE, YOU WILL FIND THE INTERRUPTION SUBROUTINES THAT ALLOW RECEIVERS 1 TO 8 TO RECEIVE MESSAGES

```
;
; Receiver 1 :
; rem : IT IS MANDATORY TO READ MESS. AT LEAST IN WORD MODE.

rx1a
                move.w      rx1_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx1_lsw,d7          ; mess in D7
                addq.l      #1,d3               ; received mess. counter

                addq.l      #1,d2               ; an other receiver answered
```

```
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$1,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit

;
; Receiver 2 :
;
rx2a
;               ori.w       #$0700,sr           ; disable CPU ITs
                move.w      rx2_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx2_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$2,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit
;
; Receiver 3 :
;
rx3a
                move.w      rx3_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx3_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$3,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit

;
; Receiver 4 :
;
rx4a
                move.w      rx4_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx4_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$4,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit
;
;
; Receiver 5 :
;
rx5a
                move.w      rx5_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx5_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$5,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit
```

```
;
; Receiver 6 :
;
rx6a
                move.w      rx6_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx6_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$6,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit

;
; Receiver 7 :
;
rx7a
                move.w      rx7_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx7_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$7,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit

;
; Receiver 8 :
;
rx8a
                move.w      rx8_msw,d7          ; Read 32 bit message
                swap        d7
                move.w      rx8_lsw,d7          ; mess in D7
                addq.l      #1,d2               ; an other receiver answered□
                lea         rxmess1,a6
                jsr         puts                ; print receiver
                move.l      #$8,d0
                jsr         write               ; print receiver nb
                lea         rxmess,a6
                jsr         puts                ; print rxmess
                move.l      d7,d0
                jsr         out8hx              ; print mess content
                bra         returnit
returnit        cmpi.l      #$8,d2              ; all receivers answered ?
                bne         ret                 ; no, then next receiver
                cmpi        #0,d4               ; all messages sent ?
                blt         ret                 ; no, then send next message
                move.w      #$81FF,mask         ; enable ITs to allow IPL signals low
ret             rte                             ; for all ITs sources□
; Unused ITs :
txe3a
txe2a
txf2a
txe1a
txf1a
```

NAME main040.s

; MAIN

; THIS SUBROUTINE CALLS THE SPECIFIC SUBROUTINES TO ACHIEVE THE
; GOALS OF THIS PROGRAM
; THERE, YOU WILL ALSO FIND ALL THE MESSAGES USED TO
COMMUNICATE WITH THE CONSOLE
; IN THE END, IT LOOPS TILL ALL MESSAGES HAVE BEEN SENT AND
RECEIVED AND IT ENABLES ITs SOURCES IF IT IS USEFULL TO ACHIEVE THIS

```
                XREF    imr,STKTOP
                XREF    parityTX
                XREF    mask,glob_int,menu,initmrt,labelprog,progtest,parityRX
                XDEF    rxmess1,rxmess,parmess
                XDEF    rxlab0,rxlab1,rxlab2,rxlab3,rxlab4
                XDEF    result1,result2,result3,resultlab
                XDEF    err,report,space,pass,endrd,self,lab1
                XDEF    msg,envoi,nb,rdlab,par1,par2,par3,par4,rxpar
                XREF    cr,lf
;_____________________________________________________________________

                ori.w   #$700,sr
                lea     STKTOP,a7           ; init stack
                clr.w   imr                 ; mask all INR interruptions

                clr.w   mask                ; mask TS68C429A interruptions

                clr.l   d1                  ; Clear receiver 1 message counter
                clr.l   d2                                  ; Clear receiver 2 message counter
                clr.l   d3                  ; Clear receiver 3 message counter
                clr.l   d4                  ; Clear transmiter 3 message counter
                clr.l   d5                  ; Clear nb of msg buffer
                clr.l   d6                  ; Clear msg to sent
                clr.l   d7                  ; Clear msg buffer
                bsr     progtest            ; Selftest ?
                bsr     initmrt             ; ARINC setup
                bsr     labelprog           ; program the label matrix
                bsr     parityTX            ; compute parity ?
                bsr     parityRX            ; check parity ?
                bsr     menu                ; sending of the messages
                bsr     glob_int            ; Interruption init
fini
                cmp     d5,d3               ; msg received ?
                beq     fin                 ; No, wait
                move.w  d4,d4               ; end of transmission ?
                blt     fin                 ; no : loop
del             muls.w  #$0,d2
                dbf     d1,del              ;kill some time
                move.w  #$81FF,mask         ; enable all ITs sources□
                bra     fini
fin

endless         bra     endless

rxmess1
                dc.b    cr
                dc.b    lf
                dc.b    '     Receiver '
                dc.b    0

rxmess
                dc.b    ', mess = '
                dc.b    0

parmess
                dc.b    ', wrong parity detected !'
                dc.b    0

nb:
                dc.b    cr
                dc.b    lf
                dc.b    cr□
                dc.b    lf
                dc.b    ' Enter nb of msg (0 to F) to be sent please # '
                dc.b    0

envoi
                dc.b    cr
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    ' Transmission nb = '
                dc.b    0

msg
                dc.b    cr
                dc.b    lf
                dc.b    ' Enter msg to be sent please # '
                dc.b    0

rxlab0          dc.b    cr
```

```
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    ' Do you want to program receiver '
                dc.b    0

par3            dc.b    cr
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    ' Do you want to program transmitter '
                dc.b    0

rxlab1          dc.b    ' matrix [y/n] ? '
                dc.b    0

rxlab2          dc.b    cr
                dc.b    lf
                dc.b    ' Beginning of the section to disable [00-FF] ?'
                dc.b    0

rxlab3          dc.b    cr
                dc.b    lf
                dc.b    ' End of the section to disable [Beginning-FF] ?'
                dc.b    0

rxlab4          dc.b    cr
                dc.b    lf
                dc.b    ' Other section to disable [y/n] ? '
                dc.b    0

lab1            dc.b    cr
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    ' Do you want to program the Label Control Matrix [y/n] ? '
                dc.b    0

rdlab           dc.b    cr
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    ' Read  the programmed matrix [y/n] ? '
                dc.b    0

self            dc.b    cr
                dc.b    lf
                dc.b    ' Do you want to run self test [y/n] ? '

space           dc.b    ' '
                dc.b    0

endrd           dc.b    cr
                dc.b    lf
                dc.b    0

report          dc.b    cr
                dc.b    lf
                dc.b    cr
                dc.b    lf
                dc.b    'SELFTEST REPORT : '
                dc.b    cr
                dc.b    lf
                dc.b    0
pass
                dc.b    '  PASSED'
                dc.b    cr
                dc.b    lf
                dc.b    0

err
                dc.b    '  FAILED'
                dc.b    cr
                dc.b    lf
                dc.b    0

result1
                dc.b    'TRANSMITTER 1 =
                dc.b    0

result2
                dc.b    'TRANSMITTER 2 =
```

```
                dc.b        0

result3
                dc.b        'TRANSMITTER 3 =  '
                dc.b        0

resultlab
                dc.b        'LABEL MATRIX =  '
                dc.b        0

parl
                dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Check parity [y/n] ? '
                dc.b        0

rxpar           dc.b        'parity [y/n] ? '
                dc.b        0

par2
                dc.b        cr
                dc.b        lf
                dc.b        ' Odd or Even [o/e] ? '
                dc.b        0

par4
                dc.b        cr
                dc.b        lf
                dc.b        cr
                dc.b        lf
                dc.b        ' Compute parity [y/n] ? '
                dc.b        0

                end
```

Output to the console example

```
ROM68K>>>go 8000

 Do you want to run self test [y/n] ?  Y

SELFTEST REPORT :
TRANSMITTER 1 =    PASSED
TRANSMITTER 2 =    PASSED
TRANSMITTER 3 =    PASSED
LABEL MATRIX =    PASSED

 Do you want to program the Label Control Matrix [y/n] ?  Y

 Do you want to program receiver 8 matrix [y/n] ?  Y
 Beginning of the section to disable [00-FF] ?10
 End of the section to disable [Beginning-FF] ?20
 Other section to disable [y/n] ?  Y
 Beginning of the section to disable [00-FF] ?50
 End of the section to disable [Beginning-FF] ?60
 Other section to disable [y/n] ?  N

 Do you want to program receiver 7 matrix [y/n] ?  N

 Do you want to program receiver 6 matrix [y/n] ?  N

 Do you want to program receiver 5 matrix [y/n] ?  N

 Do you want to program receiver 4 matrix [y/n] ?  Y
 Beginning of the section to disable [00-FF] ?A0
 End of the section to disable [Beginning-FF] ?D0
 Other section to disable [y/n] ?  N

 Do you want to program receiver 3 matrix [y/n] ?  N

 Do you want to program receiver 2 matrix [y/n] ?  N

 Do you want to program receiver 1 matrix [y/n] ?  N

 Read  the programmed matrix [y/n] ?  Y
```

```
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F 7F
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7
F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7
F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7 F7
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF

Compute parity [y/n] ? Y

Do you want to program transmitter 3 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program transmitter 2 parity [y/n] ? N

Do you want to program transmitter 1 parity [y/n] ? N

Check parity [y/n] ? Y

Do you want to program receiver 8 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 7 parity [y/n] ? Y
Odd or Even [o/e] ? E

Do you want to program receiver 6 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 5 parity [y/n] ? Y
Odd or Even [o/e] ? E

Do you want to program receiver 4 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 3 parity [y/n] ? Y
Odd or Even [o/e] ? E

Do you want to program receiver 2 parity [y/n] ? Y
Odd or Even [o/e] ? O

Do you want to program receiver 1 parity [y/n] ? Y
Odd or Even [o/e] ? E

Enter nb of msg (0 to F) to be sent please # 5
Enter msg to be sent please # 12345678

Transmission nb = 04
    Receiver 7, wrong parity detected !
    Receiver 5, wrong parity detected !
    Receiver 3, wrong parity detected !
    Receiver 1, wrong parity detected !
    Receiver 8, mess = 12345678
    Receiver 6, mess = 12345678
    Receiver 4, mess = 12345678
    Receiver 2, mess = 12345678
Transmission nb = 03
    Receiver 7, wrong parity detected !
    Receiver 5, wrong parity detected !
    Receiver 3, wrong parity detected !
    Receiver 1, wrong parity detected !
    Receiver 8, mess = 92345679
    Receiver 6, mess = 92345679
    Receiver 4, mess = 92345679
    Receiver 2, mess = 92345679
Transmission nb = 02
    Receiver 7, wrong parity detected !
    Receiver 5, wrong parity detected !
    Receiver 3, wrong parity detected !□
    Receiver 1, wrong parity detected !
    Receiver 8, mess = 9234567A
    Receiver 6, mess = 9234567A
```

5

```
    Receiver 4, mess = 9234567A
    Receiver 2, mess = 9234567A

Transmission nb = 01
    Receiver 7, wrong parity detected !
    Receiver 5, wrong parity detected !
    Receiver 3, wrong parity detected !
    Receiver 1, wrong parity detected !
    Receiver 8, mess = 1234567B
    Receiver 6, mess = 1234567B
    Receiver 4, mess = 1234567B
    Receiver 2, mess = 1234567B

Transmission nb = 00
    Receiver 7, wrong parity detected !
    Receiver 5, wrong parity detected !
    Receiver 3, wrong parity detected !
    Receiver 1, wrong parity detected !
    Receiver 8, mess = 9234567C
    Receiver 6, mess = 9234567C
    Receiver 4, mess = 9234567C
    Receiver 2, mess = 9234567C
```

e) A short example with the INTEL EV80C186EB board :

The achievements of this program are similar to the ones of the first example provided with the MOTOROLA ADS302 board.

9 messages are sent by transmitter 3. The only receiver active is receiver 3, in test mode.

We only use the interrupt line INT2. Receivers and transmitters are both connected to this line. The INT2 vector in the I80C186EB memory space is initialized at the beginning of the program.

After the INTEL EV80C186EB board initialization, and the MRT initialization the interrupt service routine must, first of all, identify the interruption source (in this case, the MRT provides no interrupt vector to the microprocessor). The receiver lines are tested first, and that is why they have a higher priority than the transmitter ones (this is the only example we provide where it is software designed). Indeed, you determine their priority level testing first the one that has the highest priority level (and last the one that has the lowest priority level) during the "Identify IT" routine.

The priority level between the transmitter lines is determined in the same way than the priority level between the receivers (we remind you that usually transmitter 3 has the lowest priority level, transmitter 1 the highest).

Indeed, you should first test the wrong parity bit, then the receiver bits (in any order), and at last the transmitter bits (first transmitter 1, last transmitter 3) to identify the interrupt source.

There is no output to the console, but the received messages are written into the memory at address 2000h, and the messages to send are picked up from the memory.

After the program, you can find a copy of the receiving section of the memory before receiving any message, and after having received 9 messages on receiving channel 3.

```
NAME    int.asm

; SEND AND RECEIVE  A MESSAGE THROUGH THE MRT USING ITs
APPLICATION FOR THE EV80C186EB BOARD
;
;
; THIS PROGRAM ENABLES YOU TO SEND 10 MESSAGES FROM THE DATA
;SECTION TO THE MEMORY THROUGH THE MRT USING ITs
;
;THE ONLY INTERRUPT LINE IN USE IS INT2, NO INTERRUPT
 ACKNOWLEDGE IS GENERATED
;
;SO, THE PRIORITY LEVELS ARE SOFTWARE DEFINED WITHIN THE
 INTERRUPT ROUTINE FOR THE RECEIVERS AND THE TRANSMITTERS
;
;THIS PROGRAM FIRST INITIALIZES THE 80C18EB, THEN IT INITIALIZES
 THE MRT BEFORE TO DEVELOP THE INTERRUPT ROUTINE
;


$           include(EBPCBMAP.INC)

eram_base   equ     756             ;expansion RAM base add
(Kbytes)
eram_size   equ     64              ;expansion RAM window (Kbytes)
waitst      equ     4               ;wait states for gcs4
defstate    equ     10              ;gcs4 : disable ready
                                    ;decode memory space

;*************************************************************************
;
; THE 80C186EB PROGRAMMATION :
;
;*************************************************************************

gcs4st_val  equ     (eram_base shl 6) or (waitst)
gcs4sp_val  equ     (((eram_base) + (eram_size)) shl 6) or (defstate)

prog_code   segment
assume      cs:prog_code, es:nothing, ds:data
begin:
            CLI                             ;disable interrupts
            mov     di,4*14                 ;INT2 vector address
            mov     word ptr [di], offset IDENTIFY_IT
            mov     [di+2],seg IDENTIFY_IT  ;program INT2 vector
            push    0bd00h                  ;
            pop     es                      ;es = bd00
            push    data
            pop     ds                      ; init ds

;_____________________________________________________________________

;CHIP SELECT PROGRAMMATION :
; In this example, the MRT is selected BY CS4, at address started at BD000h.
;_____________________________________________________________________
            mov     dx,gcs5sp
            in      ax,dx                   ; disable CS5
            and     ax,0fff7h
            out     dx,ax

            mov     dx,gcs4st               ;set up gcs4 start register
            mov     ax,gcs4st_val
            out     dx,ax

            mov     dx,gcs4sp               ;set up gcs4 stop register
            mov     ax,gcs4sp_val
            out     dx,ax


;Program Port 1 control register to enable gcs4 as chip select rather than port pin
            mov     dx, p1con               ; point to port 1 control register
            in      ax, dx                  ; read register
            mov     ax, 0f0h                ; set p1.4 to 1 (cs function)
            out     dx, ax
```

```
;_____________________________________________________________________
;TIMER 0 PROGRAMMATION
; This programmation has been designed in order to provide a square signal on TOUT0 at
;1MHz.
; This value of 1 MHz allows 12.5Kbit/s and a 100Kbit/s transfer rate
;_____________________________________________________________________

                mov     dx, t0cmpa          ;set up timer 0 compare A value
                mov     ax,02h
                out     dx,ax

                mov     dx, t0cmpb          ;set up timer 0 compare B value
                out     dx,ax

                mov     dx,t0con            ;enable timer 0
                mov     ax,0C003h
                out     dx,ax
;_____________________________________________________________________
;
; INITIALIZE INTERRUPT CONTROL UNIT :
; There, INT2 is the only interrupt line that is used..
; Both receivers and transmitters use this unique interrupt line (IRQRX and IRQTX are
; short-circuited).
;_____________________________________________________________________
;
; Initialize Interrupt 2
;
; Special Fully Nested Mode = 0
; Cascade Mode = 0
; Level Trigger = 1
; Interrupt Mas = 0
; Priority Level = 2
;
                mov     dx,i2con
                mov     ax,012h
                out     dx,al
; Unmask INT2
                mov     dx,imask
                mov     ax,0bdh
                out     dx,ax
;**********************************************************************
;
;MRT PROGRAMMATION :
; In this example, only the MRT lines RX1 and TX3 are enabled, in test mode.
; This program is designed in order to provide the highest priority level to the receivers.
; TX1 has a higher priority level than TX2 that has a higher priority level than TX3.
; RX1 has the highest priority level within the receivers, RX8 the lowest.
;
;**********************************************************************

                mov     dx,0000ah           ;prog transmit frequency register 3
                mov     di,offset tx3_frq   ;tranmission rate = 100Kbit/s
                mov     es:[di],dx

                mov     dx,08090h           ;prog TX3 transmit control register
                mov     di,offset tx3_ctr   ;TX3 enable, FIFO enable
                mov     es:[di],dx          ;no parity, gap length = 4 arinc bits

                mov     dx,01Eh             ;prog RX1 gap register
                mov     di,offset rx1_gap   ;gap lenght = 3 arinc bits
                mov     es:[di],dx          ;gap lenght = 30 clk-arinc periods

NOTE THAT RX GAP LENGTH MUST ALWAYS BE GREATER THAN 1 ARINC BIT

                mov     dx,0C000h           ;prog receiver 1 control register
                mov     di,offset rx1_ctr   ;enable receiver 1, test mode
                mov     es:[di],dx          ; no priority level programmed

                mov     dx,0C001h           ;enable TX3 ITs,RX1 ITs
                mov     di,offset mas
                mov     es:[di],dx

;**********************************************************************
;
;MAIN :
; Just wait for interruptions
```

```
;
;*************************************************************************
boucle2:        STI                             ;ENABLE INTERRUPTS
                jmp         boucle2

;*************************************************************************
;
;INTERRUPT SERVICE ROUTINES :
;There, the first goal is to identify which interrupt is really pending.
;The respective priorities are programmed during this operation.
;Only ten messages are sent : after that, transmission is disabled.

*************************************************************************

IDENTIFY_IT:
                mov         di,offset status    ; Read status register
                mov         ax,es:[di]
                mov         di, offset mas      ; and status with mask register
                and         ax,es:[di]
                test        al,0ffh             ; RX IT ? Receiver lines tested
                                                ; first have a higher priority than
                                                ; transmitter lines
                je          testTX              ; no, then test transmitters

testRX:         test        al,01h              ; RX1 ? RX1 tested first has the
                jne         itrx1               ; highest RX priority level.
                test        al,02h              ; RX2 ?
                jne         itrx2
; etc ...

itrx1:          xor         bx,bx               ; bx = receiver number minus 1
                jmp         RECEIVER

itrx2:          mov         bx,01h
                jmp         RECEIVER
; etc ...
;
testTX:         test        ah,4                ; TX1 empty?
                jne         itx1e               ; tested first : the highest priority

                test        ah,8                ; TX1 fifo empty?
                jne         itx1f
; etc ...
                test        ah,40h              ;TX3 empty?
                jne         itx3e

                test        ah,80h              ;TX3 fifo empty?
                jne         itx3f               ; tested last : the lowest priority

                jmp         retour

itx1e:
itx1f:
                xor         bx,bx
                jmp         TRANSMITTER
; etc ...
itx3e:
itx3f:
                mov         bx,02h
                jmp         TRANSMITTER

;_____________________________________________________________________
;
RECEIVER:
;_____________________________________________________________________

                add         bx,bx               ; *2 (table of words)
                mov         si,[bx + offset mrtrxaddr]  ;points to mrt rx buffer
                mov         di,[bx + offset addrrx1]    ; points to rx buffer pointer
                push        es
                push        ds
                pop         es
                pop         ds                  ; exchange pointer values
                mov         cx,2
                rep         movsw               ; read mess
                push        es
                push        ds
                pop         es
```

```
                pop     ds                      ; restore segments
                mov     [bx + offset addrrx1],di  ;points to next place in rx buffer
                jmp     retour
;_____________________________________________________________________
TRANSMITTER:
;_____________________________________________________________________

                add     bx,bx                   ;*2 (word table)
                mov     di,[bx + offset mrttxaddr]  ; points to mrt tx buffer
                mov     si,[bx + offset addrtx1]  ;points to first msg to send
                mov     cx,2
                rep     movsw                                   ; send mess
                mov     [bx + offset addrtx1],si  ; points to next msg to send
                xor     bx,bx
                mov     ax,[bx + offset cmpt]   ; adjust message counter
                inc     ax
                mov     word ptr [bx + offset cmpt],ax
                cmp     ax,0ah                  ; 10 message sent ?
                jne     retour                  ; no, then go on
                mov     ax,0ffh                 ; yes, then disable transmission
                mov     di,[bx + offset mas]
                and     es:[di],ax
                jmp     retour


retour:         mov     dx,eoi
                mov     ax,0eh                  ; end of interrupt
                out     dx,ax
                iret


prog_code       ends

data            SEGMENT at 200h
cmpt            dw      0
;
addrrx1         dw      offset mesrx1           ; pointer to first free location
addrrx2         dw      offset mesrx2
addrrx3         dw      offset mesrx3
addrrx4         dw      offset mesrx4
addrrx5         dw      offset mesrx5
addrrx6         dw      offset mesrx6
addrrx7         dw      offset mesrx7
addrrx8         dw      offset mesrx8
;
mesrx1          dd      10 dup (0)              ; allocate memory for 10 mess
mesrx2          dd      10 dup (0)
mesrx3          dd      10 dup (0)
mesrx4          dd      10 dup (0)
mesrx5          dd      10 dup (0)
mesrx6          dd      10 dup (0)
mesrx7          dd      10 dup (0)
mesrx8          dd      10 dup (0)
;
addrtx1         dw      offset mestx1
addrtx2         dw      offset mestx2
addrtx3         dw      offset mestx3
;
mestx1          dd      (11110001h)
                dd      (11110002h)
                dd      (11110003h)
                dd      (11110004h)
                dd      (11110005h)
                dd      (11110006h)
                dd      (11110007h)
                dd      (11110008h)
                dd      (11110009h)
                dd      (1111000ah)
;
mestx2          dd      (22220001h)
                dd      (22220002h)
                dd      (22220003h)
                dd      (22220004h)
                dd      (22220005h)
                dd      (22220006h)
                dd      (22220007h)
                dd      (22220008h)
                dd      (22220009h)
                dd      (2222000ah)
```

```
mestx3      dd      (33330001h)
            dd      (33330002h)
            dd      (33330003h)
            dd      (33330004h)
            dd      (33330005h)
            dd      (33330006h)
            dd      (33330007h)
            dd      (33330008h)
            dd      (33330009h)
            dd      (3333000ah)
;
mrtrxaddr   dw      4           ;offset for rx1 MSW
            dw      12          ;offset for rx2 MSW
            dw      20          ;offset for rx3 MSW
            dw      28          ;offset for rx4 MSW
            dw      36          ;offset for rx5 MSW
            dw      44          ;offset for rx6 MSW
            dw      52          ;offset for rx7 MSW
            dw      60          ;offset for rx8 MSW
;
mrttxaddr   dw      68          ;offset for tx1 MSW
            dw      76          ;offset for tx2 MSW
            dw      84          ;offset for tx3 MSW
;
rx1_ctr     dw      0
rx1_gap     dw      2
rx2_ctr     dw      8
rx2_gap     dw      10
rx3_ctr     dw      16
rx3_gap     dw      18
rx4_ctr     dw      24
rx4_gap     dw      26
rx5_ctr     dw      32
rx5_gap     dw      34
rx6_ctr     dw      40
rx6_gap     dw      42
rx7_ctr     dw      48
rx7_gap     dw      50
rx8_ctr     dw      56
rx8_gap     dw      58
tx1_ctr     dw      64
tx1_frq     dw      66
tx2_ctr     dw      72
tx2_frq     dw      74
tx3_ctr     dw      80
tx3_frq     dw      82
status      dw      128
mas         dw      130
data        ends
end         begin
```

Output to the memory at 200h :

```
;===List file opened on 05/31/1994 at 09:26:56
*word 2000 to 21F0
;  THE DEFAULT BASE IS HEXADECIMAL
;
; 00002000H: 0000     0012    003A    0062    008A    00B2    00DA    0102
; 00002010H: 012A     0000    0000    0000    0000    0000    0000    0000
; 00002020H: 0000     0000    0000    0000    0000    0000    0000    0000
; 00002030H: 0000     0000    0000    0000    0000    0000    0000    0000
; 00002040H: 0000     0000    0000    0000    0000    0000    0000    0000
; 00002050H: 0000     0000    0000    0000    0000    0000    0000    0000

*go from 1000
>word 2000 to 21F0
;  THE DEFAULT BASE IS HEXADECIMAL
;
; 00002000H: 0009     0036    003A    0062    008A    00B2    00DA    0102
; 00002010H: 012A     0001    3333    0002    3333    0003    3333    0004
; 00002020H: 3333     0005    3333    0006    3333    0007    3333    0008
; 00002030H: 3333     0009    3333    0000    0000    0000    0000    0000
; 00002040H: 0000     0000    0000    0000    0000    0000    0000    0000
; 00002050H: 0000     0000    0000    0000    0000    0000    0000    0000
>hal
```

5

THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

EF 6809

HMOS 8-BIT MICROPROCESSOR UNIT (MPU)*

DESCRIPTION

The EF 6809 is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.
This third-generation addition to the EF 6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.
The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The EF 6809 has the most complete set of addressing modes availables on any 8-bit microprocessor today.
The EF 6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

MAIN FEATURES

EF 6800 compatible

- Hardware - interfaces with all EF 6800 peripherals.
- Software - upward source code compatible instruction set and addressing modes.

Architectural features

- Two 16-bit index registers.
- Two 16-bit indexable stack pointers.
- Two 8-bit accumulators can be concatenated to form one 16-bit accu mulator.
- Direct page register allows direct addressing throughout memory.

Hardware features

- On-chip oscillator (crystal frequency = 4 x E).
- DMA/BREQ allows DMA operation on memory refresh.
- Fast interrupt request input stacks only condition code register and program counter.
- MRDY input extends data access times for use with slow memory.
- Interrupt acknowledge output allows vectoring by devices.
- Sync acknowledge output allows for syncronization to external event.
- Single bus-cycle RESET.
- Single 5-volt supply operation.
- NMI inhibited after RESET until after first load of stack pointer.
- Early address valid allows use with slower memories.
- Early write data for dynamic memories.

Software features

- 10 addressing modes :
  - EF 6800 upward compatible addressing modes,
  - direct addressing anywhere in memory map,
  - long relative branches,
  - program counter relative,
  - expended indexed addressing :
    - 0-, 5-, 8- or 16-bit constant offsets,
    - 8- or 16-bit accumulator offsets,
    - auto increment/decrement by 1 or 2.
- Improved stack manipulation.
- 1464 instructions with unique addressing modes.
- 8 x 8 unsigned multiply.
- 16-bit arithmetic.
- Transfer/exchange all registers.
- Push/pull any registers or any set of registers.
- Load effective address.
- Frequency of operation over full military temperature range : 1 & 1.5 MHz.
- EF68B09J (2 MHz in 0 – 70°C).

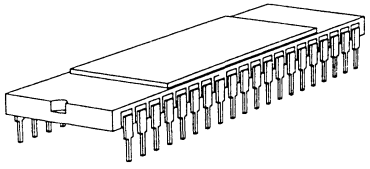
SCREENING / QUALITY

This product could be manufactured in full compliances with either :

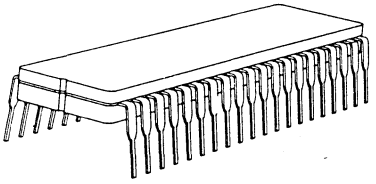
- CECC 90000 (class B, assessment level Y) 90110-008.
- MIL-STD-883 (class B).
- or according to TMS standards.

* High density, N channel silicon gate.

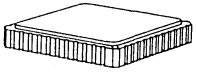
NOT FOR NEW DESIGN
Data sheet available on request



C suffix
DIL 40
Ceramic Side Brazed package



J suffix
DIL 40
Ceramic Cerdip package



E suffix
LCCC 44
Ceramic Leadless Chip Carrier

See the ordering information page 50.

Pin connection : see page 49.

5

EF 6809E

HMOS* 8-BIT MICROPROCESSOR UNIT (MPU)

DESCRIPTION

The EF 6809E is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.
This third-generation addition to the EF 6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.
The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The EF 6809E has the most complete set of addressing modes availables on any 8-bit microprocessor today.
The EF 6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems, or other MPUs.

MAIN FEATURES

EF 6800 compatible
- Hardware - interfaces with all EF 6800 peripherals.
- Software - upward source code compatible instruction set and addressing modes.

Architectural features
- Two 16-bit index registers.
- Two 16-bit indexable stack pointers.
- Two 8-bit accumulators can be concatenated to form one 16-bit accu mulator.
- Direct page register allows direct addressing throughout memory.

Hardware features
- External clock inputs, E and Q, allows synchronization.
- TSC input controls internal bus buffers.
- LIC indicates opcode fetch.
- ACMA allows efficient use of common ressources in a multiprocessor ststem.
- BUSY is a status line for multiprocessing.
- Fast interrupt request input stacks only condition code register and program counter.
- Interrupt acknowledge output allows vectoring by devices.
- Sync acknowledge output allows for syncronization to external event.
- Single bus-cycle RESET.
- Single 5-volt supply operation.
- NMI inhibited after RESET until after first load of stack pointer.
- Early address valid allows use with slower memories.
- Early write data for dynamic memories.

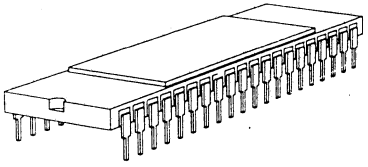
Software features
- 10 addressing modes :
  - EF 6800 upward compatible addressing modes,
  - direct addressing anywhere in memory map,
  - long relative branches,
  - program counter relative,
  - true indirect addressing,
  - expended indexed addressing :
    - 0-, 5-, 8- or 16-bit constant offsets,
    - 8- or 16-bit accumulator offsets,
    - auto increment/decrement by 1 or 2.
- Improved stack manipulation.
- 1464 instructions with unique addressing modes.
- 8 x 8 unsigned multiply.
- 16-bit arithmetic.
- Transfer/exchange all registers.
- Push/pull any registers or any set of registers.
- Load effective address.
- Processor speed 1 and 1.5 MHz over military temperature range.

SCREENING / QUALITY

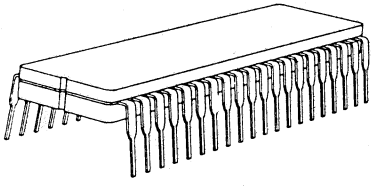
This product could be manufactured in full compliances with either :
- CECC 90000 (class B, assessment level Y).
- MIL-STD-883 (class B).
- or according to TMS standards.

* High density, N channel silicon gate.

NOT FOR NEW DESIGN
Data sheet available on request



C suffix
DIL 40
Ceramic Side Brazed package



J suffix
DIL 40
Ceramic Cerdip package

See the ordering information page 49.

Pin connection : see page 48.

NMOS PERIPHERAL INTERFACE ADAPTER (PIA)

DESCRIPTION

The EF 6821 peripheral interface adapter provides the universal means of interfacting peripheral equipment to the 6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

MAIN FEATURES

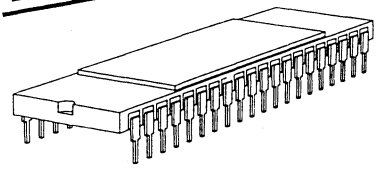
- 8-bit bidirectional data bus for communication with the MPU.
- Two bidirectional 8-bit buses for interface to peripherals.
- Two programmable control registers.
- Two programmable data direction registers.
- Four individually-controlled interrupt input lines ; two usable as peripheral control outputs.
- Handshake control logic for input and output peripheral operation.
- High-impedance three-state and direct transistor drive peripheral lines.
- Program controlled interrupt and interrupt disable capability.
- CMOS drive capability on side A peripheral lines.
- Two TTL drive capability an all A and B side buffers.
- TTL-compatible.
- Static operation.
- Three available versions : EF 6821 (1 MHz),
  EF 68A21 (1.5 MHz),
  EF 68B21 (2 MHz).

SCREENING / QUALITY

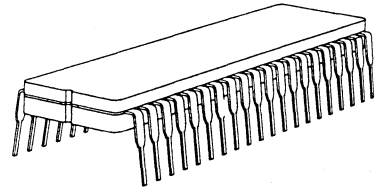
This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- NFC 96883 (class G).
- or according to TMS standards.

NOT FOR NEW DESIGN
Data sheet available on request



C suffix
DIL 40
Ceramic Side Brazed package



J suffix
DIL 40
Ceramic Cerdip package

E suffix
LCCC 44
Leadless Ceramic Chip Carrier

See the ordering information page 18.

Pin connection : see page 17.

5

EF 6840

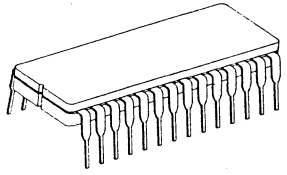
NMOS PROGRAMMABLE TIMER MODULE (PTM)

DESCRIPTION

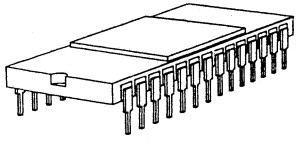
The EF 6840 is a programmable subsystem component of the 6800 family designed to provide variable system time intervals.

The EF 6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The EF 6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for squatre wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

NOT FOR NEW DESIGN
Data sheet available on request



J suffix
DIL 28
Cerdip package



C suffix
DIL 28
Ceramic Side Brazed package

E suffix
LCCC 28
Leadless Ceramic Chip Carrier package

See the ordering information page 21.

Pin connection : see page 20.

MAIN FEATURES

- Operates from a single 5 V power supply.
- Fully TTL compatible.
- Single system clock required (enable).
- Selectable prescaler on timer 3 capable of 4 MHz for the EF 6840, 6 MHz for the EF 68A40 and 8 MHz for the EF 68B40.
- Programmable interrupts ($\overline{IRQ}$) output to MPU.
- Readable down counter indicates counts to go to time-out.
- Selectable gating for frequency or pulse-width comparison.
- RESET input.
- Three asynchronous external clock and gate/trigger inputs internally synchronized.
- Three maskable outputs.
- Three available versions :
  EF 6840 (1.0 MHz),
  EF 68A40 (1.5 MHz),
  EF 68B40 (2 MHz) - (0°C to +70°C only).

SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- NFC 96863 class G.
- or according to TMS standards.

EF 6850

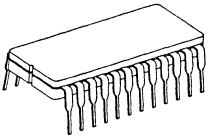
NMOS ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

NOT FOR NEW DESIGN
Data sheet available on request

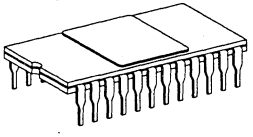
DESCRIPTION

The EF 6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the EF 6800 Microprocessing Unit.

The bus interface of the EF 6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional and data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided.



J suffix
DIL 24
Ceramic Cerdip package



C suffix
DIL 24
Ceramic Side Brazed package

E suffix
LCCC 28
Leadless Ceramic Chip Carrier package

See the ordering information § 11.

Pin connection : see § 10.

MAIN FEATURES

- 8- and 9-bit transmission.
- Optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional +1, +16 and +64 clock modes.
- Up to 1.0 Mbps transmission.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered.
- One- or two-stop bit operation.
- Three available versions :
  - EF 6850 (1.0 MHz),
  - EF 68A50 (1.5 MHz),
  - EF 68B50 (2 MHz) - 0°C to 70°C only.

SCREENING / QUALITY

This product is manufactured in full compliance with either :

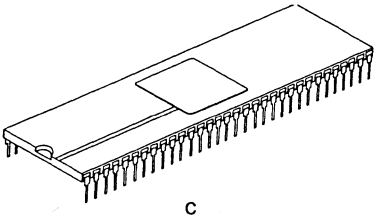
- MIL-STD-883 class B.
- NFC 96863 class G.
- or according to TMS standards.

TS 68000

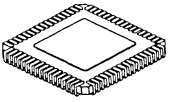
HMOS HIGH DENSITY N-CHANNEL SILICON-GATE DEPLETION LOAD 16/32 BIT MICROPROCESSOR

DESCRIPTION

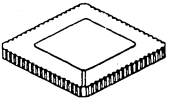
The TS 68000 is the first implementation of the 68000 16/32 microprocessor architecture. The TS 68000 has a 16-bit data bus and 24-bit address bus. It is completely cod e-compatible with the TS 68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the TS 68020 32-bit implementation of the architecture. Any user-mode programs written using the TS 68000 instruction set will run unchanged on the TS 68008 and TS 68020. This is possible because the user programming model is identical for all three processors and the instruction sets are proper sub-sets of the complete architecture.



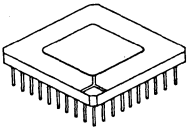
C
DIL 64
Ceramic package



W
LDCC 68
Leaded Ceramic Chip Carrier
(On request only)



E
LCCC 68
Leadless Ceramic Chip Carrier



R
PGA 68
Pin Grid Array

PIN CONNECTIONS (See chapter 10)
See the Ordering Information at the end of the data sheet.

MAIN FEATURES

- 16/32-bit data and address register.
- 16 megabytes direct addressing range.
- 56 powerful instruction types.
- Operations on five main data types.
- Memory mapped I/O.
- 14 addressing modes.
- 3 available versions : 8 / 10 and 12.5 MHz.
- Military temperature range :
  − 55°C / + 125°C (8 / 10 and 12.5 MHz).
- Power supply : 5.0 V_{DC} ±5 %.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 class B.
- DESC 82021.
- TCS standard.

SUMMARY

1 - SCOPE

This drawing describes the specific requirements for the microprocessor 68000, 8, 10 and 12.5 MHz in compliance either with MIL-STD-883 class B rev C, CECC 90000 class B or TCS STANDARD.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
3) Desc Drawing 8202102 (8 MHz) - 8202103 (10 MHz) - 8202104 (12.5 MHz).

2.2 - CECC 90000

1) CECC 90000.
2) Specification CECC 90110-001 8 / 10 and 12.5 MHz.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be as shown in § 10.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1895.

3.2.3 - Package

The microcircuits are packaged in a hermetically sealed ceramic package which is conformed to case outlines of MIL-STD-1835 (when defined).

- 64 lead DIL / SB - C8 - C7
- 68 lead LDCC - W8 (on request)
- 68 lead LCCC - E8 - E7
- 68 lead PGA - R8 - R7

The precise case outlines are described in § 9 of this document.

3.3 - Electrical requiremetns

3.3.1 - Absolute maximum ratings

Symbol	Characteristics	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7	V
V_I	Input voltage		−0.3	+7	V
T_{stg}	Storage temperature		−65	+150	°C
P_D	Power dissipation	T_{case} = −55°C for 8 - 10 - 12.5 MHz		1.75	W
		T_{case} = +125°C for 8 - 10 MHz for 12.5 MHz		1.5 1.7	W W
T_j	Junction temperature			170	°C
T_{leads}	Lead temperature	max soldering 5 seconds		270	°C
T_{case}	Operating temperature - see Note	T_{case} 8 - 10 - 12.5 MHz	−55	+125	°C

Note : T_{case} could be −40°C / +85°C or 0°C / +70°C as specified in ordering information § 11.4.

3.3.2 · Recommended operating conditions

Symbol	Characteristics and conditions	Operating ranges		
		Min	Max	Unit
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High level input voltage	2		V
V_{IL}	Low level input voltage		0.8	V
f	Frequency of operation – 8 MHz part – 10 MHz part – 12.5 MHz part	 2 2 4	 8 10 12.5	 MHz MHz MHz
T_{case}	Case operating temperature range - see Note T_{case} 8 - 10 - 12.5 MHz part	 – 55	 + 125	 °C
tr	Clock rise time		10	ns
tf	Clock fall time		10	ns
Note : T_{case} could be – 40°C / + 85°C or 0°C / + 70°C as specified in ordering information § 11.4.				

3.3.3 · Electrical performance conditions

The electrical performance characteristics are specified in tables 1 and are applied over full operating temperature range unless otherwise specified (see § 11).

3.4 · Mechanical and environment

The microcircuit shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.5 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following informations as minimum :

3.5.1 · Thomson logo
3.5.2 · Manufacturer's part number
3.5.3 · Class B identification
3.5.4 · Date-code of inspection lot
3.5.5 · ESD identifier if available
3.5.6 · Country of manufacturing

3.6 - Thermal characteristics

Package	Symbol	Parameter	Value	Unit
DIL 64	θ J-A	Thermal resistance Junction to Ambient	25	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
PGA 68	θ J-A	Thermal resistance Junction to Ambient	30	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
LCCC 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	8	°C/W
LDCC 68	θ J-A	Thermal resistance Junction to Ambient	50	°C/W
	θ J-C	Thermal resistance Junction to Case	10	°C/W
CQFP 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	8	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each inspection lot. Group C and D inspection are performed on a periodic basis in accordance with method 5005 of MIL-STD-883.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each inspection lot as specified in CECC 90110-001. Group C inspection is performed on a periodic basis in accordance with CECC 90110-001.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 1A : Static electrical characteristics for all electrical variants.
- Table 1B : Dynamic electrical characteristics for TS 68000-8 (8 MHz).
- Table 1C : Dynamic electrical characteristics for TS 68000-10 (10 MHz).
- Table 1D : Dynamic electrical characteristics for TS 68000-12 (12.5 MHz).

For static characteristics (table 1A), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to § 5.2 of this specification (tables 1B, 1C and 1D).

Indication of «min.» or «max.» in the column «Test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.3 here above.

5.2 - Test conditions specific to the device

5.2.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of tables 1B, 1C and 1D refering to the loading network number as shown in figures 1A and 1B below.

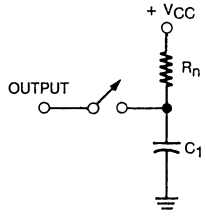


Figure 1A : Passive loads.

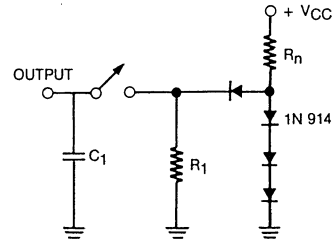


Figure 1B : Active loads.

Load NBR	Figure	R_1	R_n	C_1*	Output application
1	1A	—	910 Ω	130 pF	$\overline{\text{RESET}}$
2	1A	—	2.9 kΩ	70 pF	$\overline{\text{HALT}}$
3	1B	6.0 k	1.22 kΩ	130 pF	A1 to A23 $\overline{\text{BG}}$ and FC0 to FC2
4	1B	6.0 k	740 Ω	130 pF	All other outputs
* C_1 includes all parasitic capacitances of test machines.					

5.2.2 · Time definitions

The times specified in tables 1B and 1C as dynamic characteristics are defined in figures 2 to 5 below by a reference number given in the column «test number» of the tables together with the relevant «figure number».

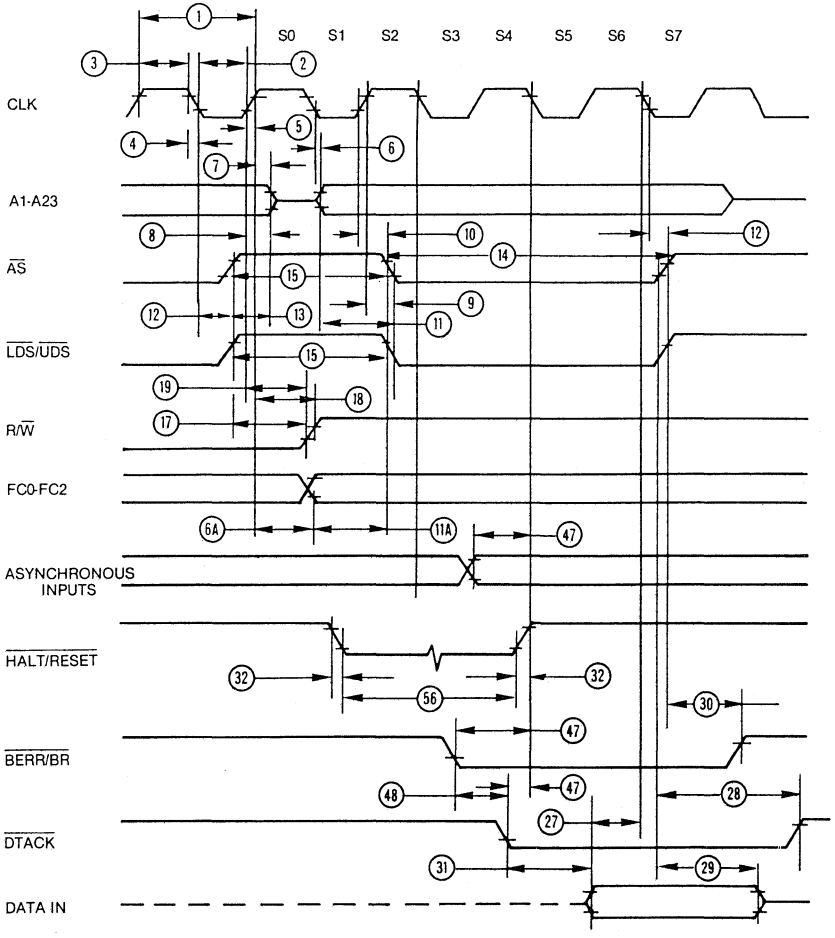


Figure 2 : Read cycle timing.

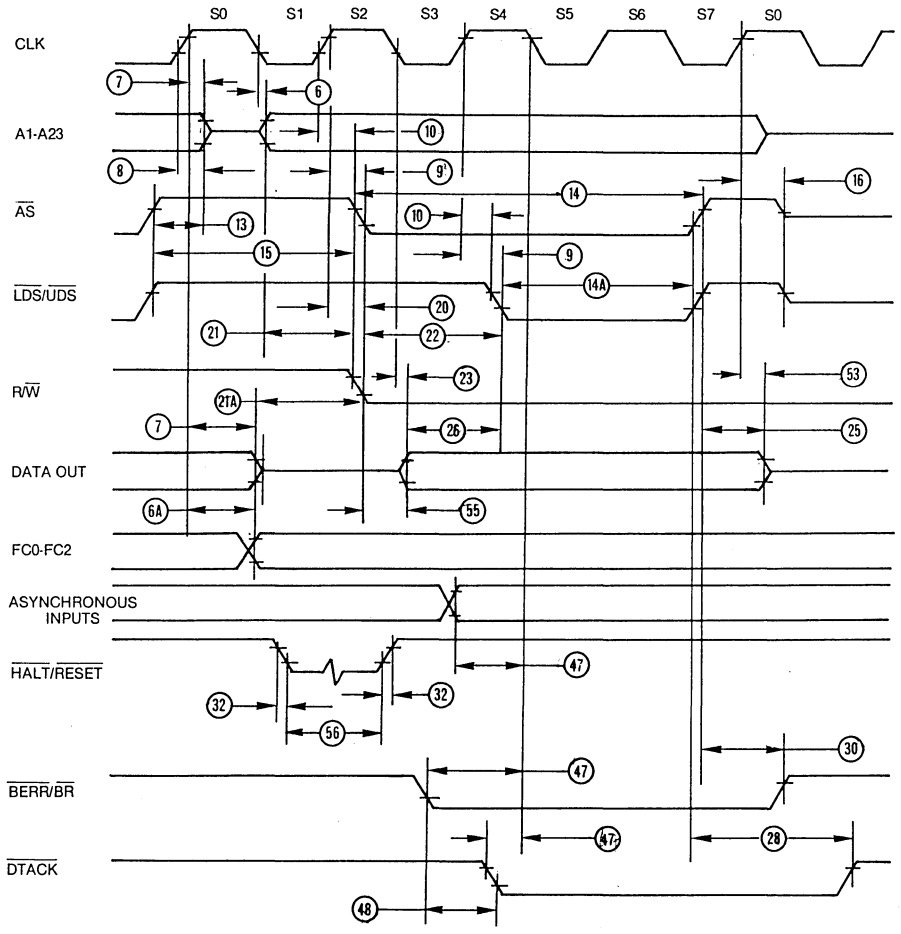


Figure 3 : Write cycle timing.

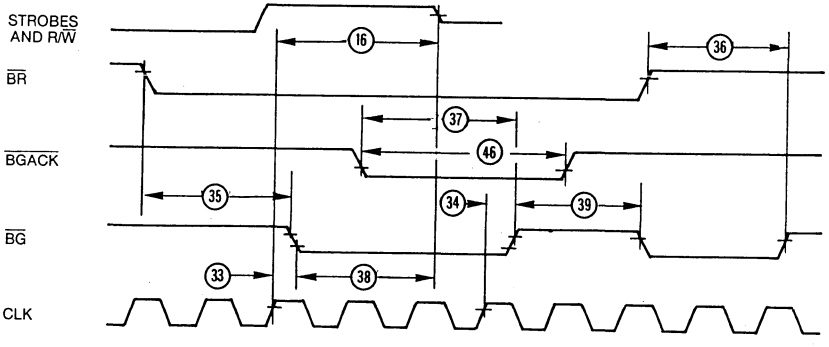


Figure 4 : AC electrical waveforms - bus arbitration.

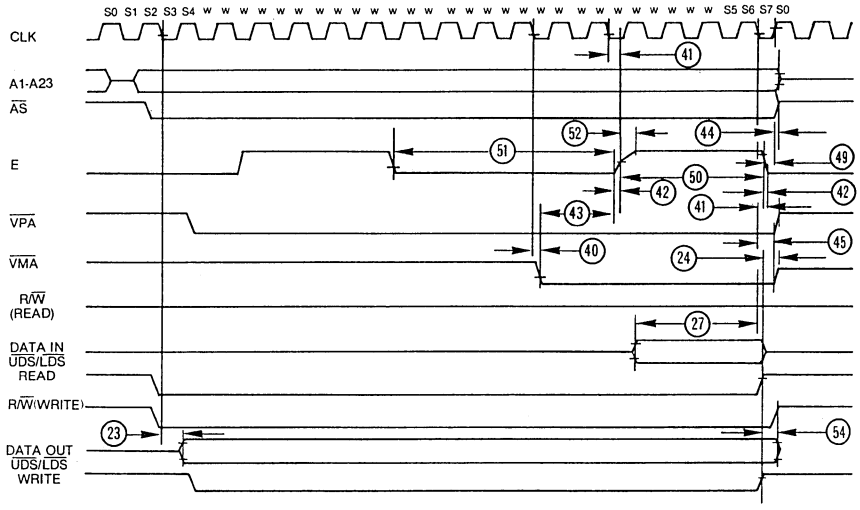


Figure 5 : Enable / interface timing.

5

5.2.3 · Input and output signals for dynamic measurements

a) Input pulse characteristics

Where input pulse generator is loaded by only a 50 Ω resistor, the input pulse characteristics shall be as shown in figure 6.

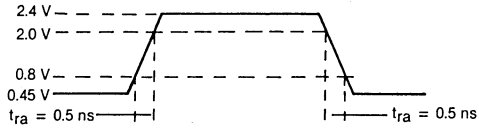


Figure 6 : Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be :

V_{IL} = 0.8 V

V_{IH} = 2.0 V

c) Time measurement output voltage reference for valid state ouput

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in figure 7.

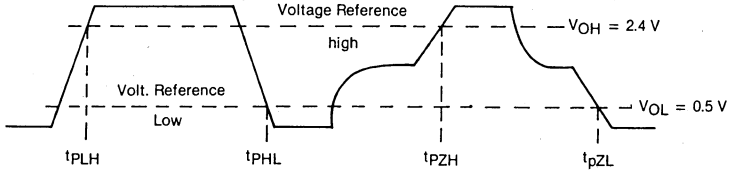


Figure 7 : Output voltage references.

5.2.4 · Refered notes to the tables 1x

The following notes shall apply where refered into the tables 1B, 1C and 1D.

Note 1 : If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.

Note 2 : Where «CLKS» is stated as unit time limit, the reve vant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.

Note 3 : For a loading capacitance of less than or equal to 50 picofarads, substract 5 nanoseconds from the value given in the maximum columns.

Note 4 : Actual value depends on actual period.

Note 5 : If 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, 48 may be ignored. In absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input set up time (47).

Note 6 : The processor will negate BG and begin driving the bus again if external arbitration logic negates BR before asserting $\overline{BGACK}$.

Note 7 : The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$, and $\overline{LDS}$/$\overline{UDS}$) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

Note 8 : When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (± 20 %), substract 10 nanoseconds from the values in these columns.

Note 9 : This value should be treated as a minimum for design purpose. For the conformance testing the value shall be regarded as the maximum time.

Table 1A - Static characteristics

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.25 V	25°C max min	—	335	mA
2	V_{OL} (1)	Low level output voltage for : A_1 to A_{23} FC0 to FC2 ; $\overline{BG}$	37	V_{CC} = 4.75 V I_{OL} = 3.2 mA	25°C max min	—	0.5	V
3	V_{OL} (2)	Low level output voltage for : $\overline{HALT}$	37	V_{CC} = 4.75 V I_{OL} = 1.6 mA	25°C max min	—	0.5	V
4	V_{OL} (3)	Low level output voltage for : AS ; R/$\overline{W}$: D0 to D15 $\overline{UDS}$; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.75 V I_{OL} = 5.3 mA	25°C max min	—	0.5	V
5	V_{OL} (4)	Low level output voltage for : $\overline{RESET}$	37	V_{CC} = 4.75 V I_{OL} = 5.0 mA	25°C max min	—	0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.75 V I_{OH} = −400 µA	25°C max min	2.4	—	V
7	I_{IH} (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.25 V V_{IN} = 5.25 V	25°C max min	—	2.5	µA
8	I_{IL} (1)	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.25 V V_{IN} = 0	25°C max min	− 2.5	—	µA
9	I_{IH} (2)	High level input current for : $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.25 V V_{IN} = 5.25 V	25°C max min	—	20	µA
10	I_{IL} (2)	Low level input current for : $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.25 V V_{IN} = 0 V	25°C max min	− 20	—	µA
11	I_{OHZ}	High level output three-state leakage current for all outputs	—	V_{CC} = 5.25 V V_{OH} = 2.4 V	25°C max min	—	20	µA

(*) Measurement method : see § 5.1.

Table 1A - Static characteristics (continued)

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
12	I_{OLZ}	Low level output three-state leakage current for all outputs	—	V_{CC} = 5.25 V V_{OL} = 0.4 V	25°C max min	— —	20 —	µA —
13	V_{IH}	High level input voltage for all inputs	—	V_{CC} = 4.75 V	25°C max min	2.0 —	— —	V —
14	V_{IL}	Low level input voltage for all inputs	—	V_{CC} = 4.75 V	25°C max min	— —	0.8 —	V —
14A	C_{in}	Input capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min	— — —	25 NA NA	pF — —
14B	C_{out}	Output capacitance (all outputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min	— — —	20 NA NA	pF — —
14C	V_{test}	Internal protection Transient energy rating		See 5.2 of this DS 5 cycles	25°C	- 500	+ 500	V

(*) Measurement method : see § 5.1.

Table 1B - Dynamic characteristics - TS 68000-8

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) f_C = 8 MHz	25°C max min	15 Note 9	— —	ns —
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	15 Note 9	— —	ns —
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	15 Note 9	— —	ns —
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	15 Note 9	— —	ns —
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	15 Note 9	— —	ns —
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	15 Note 9	— —	ns —
2	t_w (CL)	Clock width low	2	Idem test 27	25°C max min	55 Note 9	125 —	ns —
3	t_w (CH)	Clock width high	2	Idem test 27	25°C max min	55 —	125 —	ns —
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	2	Idem test 27 Load : 3	25°C max min	— —	70 —	ns —

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

Table 1B - Dynamic characteristics - TS 68000-8 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	2	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	2	Idem test 27 Load : 4	25°C max min	—	70 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	2	Idem test 27 Load : 4	25°C max min	—	70 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	2	Idem test 27 Load : 4	25°C max min	—	70 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	3	Idem test 27 Load : 4	25°C max min	—	70 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C max min	—	70 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 3	25°C max min	—	70	ns
32	t_{HRRF}	$\overline{RESET}$ / $\overline{HALT}$ input transition time	2 - 3	Idem test 27	25°C max min	—	200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	—	70	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	—	70	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	5	Idem test 27 Load : 4	25°C max min	—	70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	5	Idem test 27 Load : 4	25°C max min	—	70	ns
8	t_h (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C max min	0	—	ns
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	30 Note 4	—	ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 90	CLKS Note 2 ns
37	t_{PLH} (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 90	CLKS Note 2 ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

Table 1B - Dynamic characteristics - TS 68000-8 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
48	t_{su} (BELDAL)	Set-up time BERR low to DTACK low	3	Idem test 27	25°C max min	 20 Note 5	 —	ns
48	t_{su} (BELDAL)	Set-up time BERR low to DTACK low	2	Idem test 27	25°C max min	 20 Note 5	 —	ns
26	t_h (DOSL)	Hold time Data-out valid to LDS, UDS low	3	Idem test 27 Load : 4	25°C max min	 30 Note 4	 —	ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

Table 1C - Dynamic characteristics - TS 68000-10

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) f_C = 10 MHz	25°C max min	 10 Note 9	 —	ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	 10 Note 9	 —	ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	 10 Note 9	 —	ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	 10 Note 9	 —	ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	 10 Note 9	 —	ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	 10 Note 9	 —	ns
2	t_w (CL)	Clock width low	2	Idem test 27	25°C max min	 45	 125	ns
3	t_w (CH)	Clock width high	2	Idem test 27	25°C max min	 45	 125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to $\overline{FC}$ valid	2	Idem test 27 Load : 3	25°C max min	 —	 60	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	2	Idem test 27 Load : 4	25°C max min	 —	 55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	 —	 55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	2	Idem test 27 Load : 4	25°C max min	 —	 55 Note 3	ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

5

Table 1C - Dynamic characteristics - TS 68000-10 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	2	Idem test 27 Load : 4	25°C max min	—	55 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	2	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	3	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C max min	—	55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 4	25°C max min	—	60	ns
32	t_{HRRF} (CHGL)	$\overline{RESET}$ / $\overline{HALT}$ transition time	2 - 3	Idem test 27	25°C max min	—	200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	—	60	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	—	60	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	5	Idem test 27 Load : 4	25°C max min	—	70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to $\overline{E}$ low	5	Idem test 27 Load : 4	25°C max min	—	55	ns
8	t_h (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C max min	0	—	ns
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	20 Note 4	—	ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 80	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 80	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	3	Idem test 27	25°C max min	20 Note 5	—	ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	2	Idem test 27	25°C max min	20 Note 5	—	ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	3	Idem test 27 Load : 4	25°C max min	20 Note 4	—	ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

Table 1D - Dynamic characteristics - TS 68000-12

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	2	See 5.2.3 (a) to (c) f_C = 12 MHz	25°C max min	10 Note 9	—	ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	10 Note 9	—	ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	10 Note 9	—	ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	10 Note 9	—	ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	10 Note 9	—	ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	2	Idem test 27	25°C max min	10 Note 9	—	ns
2	t_w (CL)	Clock width low	2	Idem test 27	25°C max min	35	125	ns
3	t_w (CH)	Clock width high	2	Idem test 27	25°C max min	35	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to $\overline{FC}$ valid	2	Idem test 27 Load : 3	25°C max min	—	55	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	2	Idem test 27 Load : 4	25°C max min	—	55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	—	55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	2	Idem test 27 Load : 4	25°C max min	—	50 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	2	Idem test 27 Load : 4	25°C max min	—	50 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	2	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	3	Idem test 27 Load : 4	25°C max min	—	60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	3	Idem test 27 Load : 4	25°C max min	—	55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	2	Idem test 27 Load : 4	25°C max min	—	55	ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

5

Table 1D - Dynamic characteristics - TS 68000-12 (continued)

Test Nbr	Symbol	Parameter	Figure Number (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
32	t_{HRRF}	$\overline{RESET}$ / $\overline{HALT}$ transition time	2 - 3	Idem test 27	25°C max min	—	150	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	—	50	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	—	50	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	5	Idem test 27 Load : 4	25°C max min	—	70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to $\overline{E}$ low	5	Idem test 27 Load : 4	25°C max min	—	45	ns
8	t_h (SHAZ)	Hold time CLK high to Address	2	Idem test 27 Load : 3	25°C max min	0	—	ns
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	2	Idem test 27 Load : 4	25°C max min	15 Note 4	—	ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 70	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	4	Idem test 27 Load : 3	25°C max min	1.5 —	3.5 + 70	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	3	Idem test 27	25°C max min	20 Note 5	—	ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	2	Idem test 27	25°C max min	20 Note 5	—	ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	3	Idem test 27 Load : 4	25°C max min	15 Note 4	—	ns

(*) Measurement method : see § 5.1.
Refered notes are given in § 5.2.4 (before Table 1A).

Table 2 - AC electrical specification - clock timing (see Figure 8)

Symbol	Parameter	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	12.5 MHz Min	12.5 MHz Max	Unit
f	Frequency of operation	2.0	8.0	2.0	10.0	4.0	12.5	MHz
t_{cyc}	Cycle time	125	250	100	250	80	250	ns
t_{CL} t_{CH}	Clock pulse width	55 55	125 125	45 45	125 125	35 35	125 125	ns
t_{Cr} t_{Cf}	Rise and fall time		10 10		10 10		10 10	ns

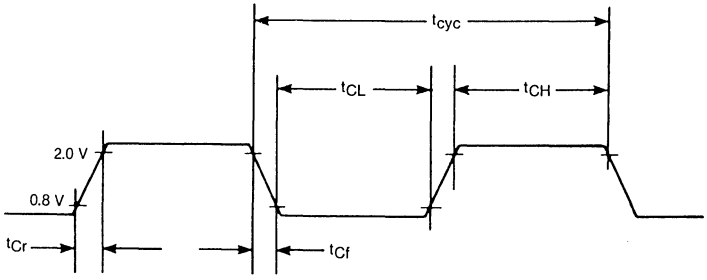


Figure 8 : Clock input timing diagram.

Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

6 · FUNCTIONAL DESCRIPTION

6.1 · General description

The TS 68000 is the first of a family of VLSI microprocessor. It combins state of the art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The TS 68000 is a fully implemented 16-bit microprocessor with 32-bit registers a rich basic instruction set, and versatile addressing modes.

5

The TS 68000 prossesses an asynchronous bus structure with a 24-bit address bus and a 16-bit data bus.

The resources available to the TS 68000 user consist of the following :

- 17 32-bit data and address registers,
- 16 megabyte direct addressing range,
- 56 powerful instruction types,
- operations on five main data types,
- memory mapped I/O,
- 14 addressing modes.

As shown in the programming model (figure 9), the TS 68000 offers seventeen 32-bit registers, a 32-bit program counter, and a 16-bit status register. The first eight registers (D0-D7) are used as data register for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the system stack pointers may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 17 registers may be used as index registers.

The status register (figure 10) contains the interrupt mask (eight levels available) as well as the condition code extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

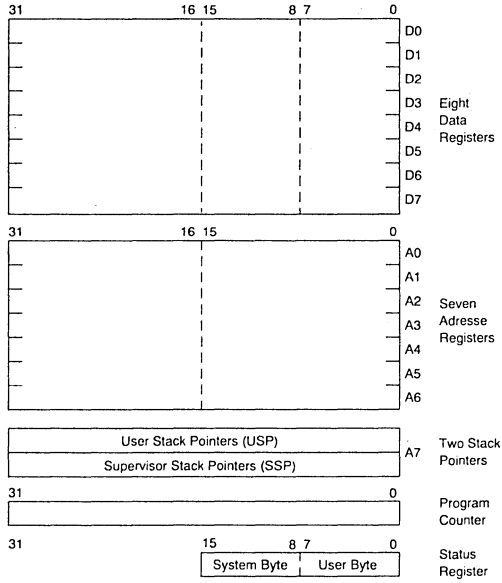


Figure 9 : Programming model.

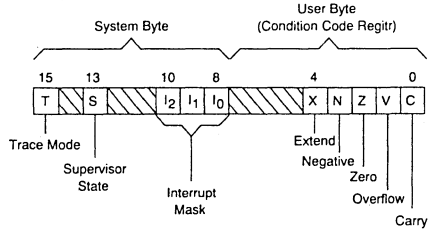


Figure 10 : Status register.

6.2 · Memory organization

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in figure 11. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

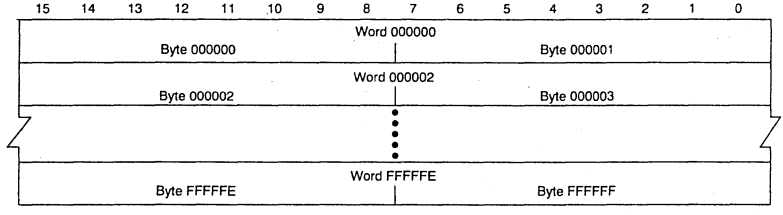


Figure 11 : Word organization in memory.

The data types supportes by TS 68000 are : bit data, integer data of 8, 16 or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in figure 12. The numbers indicate the order in which the data would be accessed from the processor.

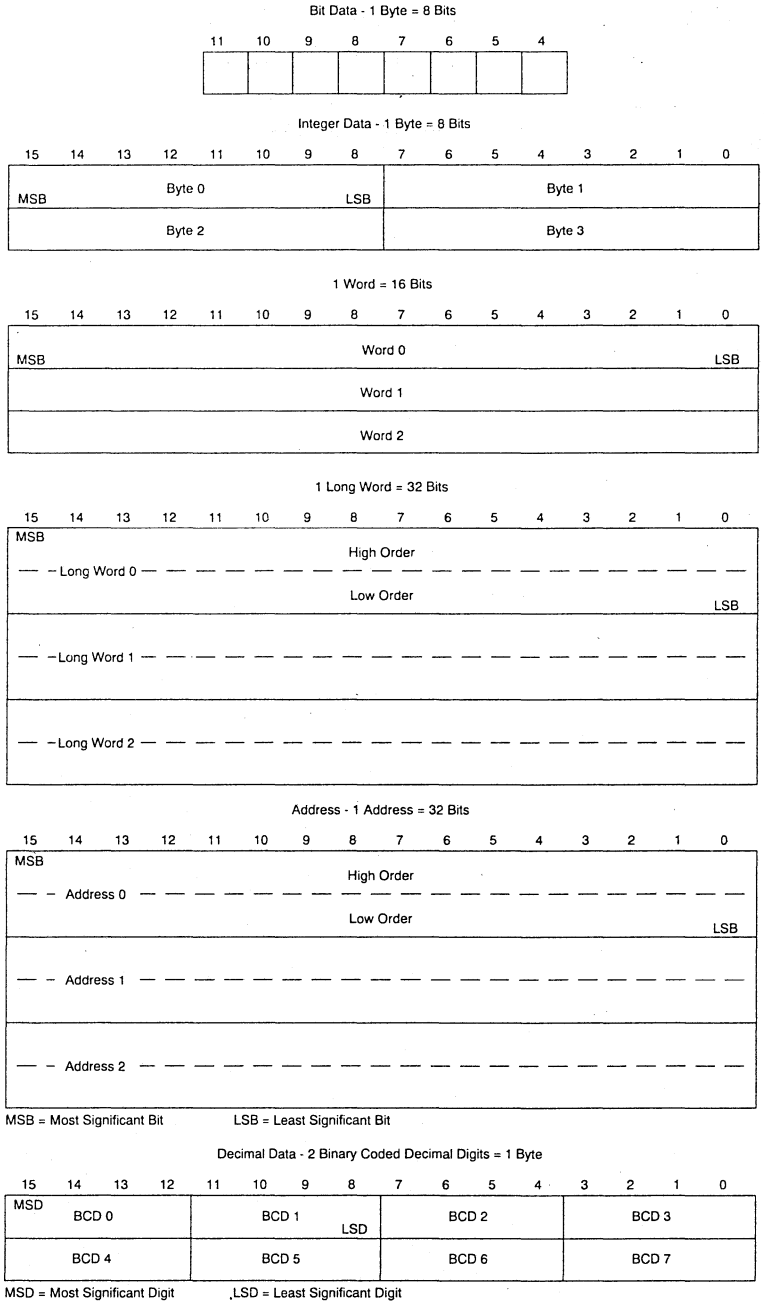


Figure 12 : Memory data organization.

6.3 · Addressing modes and data types

Five basic data are supported. These data types are :

- Bits,
- BCD Digits (4 bits),
- Bytes (8 bits),
- Words (16 bits),
- Long Words (32 bits).

In addition, operations on other data types such as memory addresses, status word data, etc... are provided in the instruction set.

The 14 address modes, shown in table 3, include six basic types :

- Register Direct,
- Register Indirect,
- Absolute,
- Program Counter Relative,
- Immediate,
- Implied.

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

Table 3 · Addressing modes

Mode	Generation
Register direct addressing	
Data register direct	EA = Dn
Address register direct	EA = An
Absolute data addressing	
Absolute short	EA = (Next word)
Absolute long	EA = (Newt two words)
Program counter relative addressing	
Relative with offset	EA = (PC) + d_{16}
Relative with index and offset	EA = (PC) + (Xn) + d_8
Register indirect addressing	
Register indirect	EA = (An)
Postincrement register indirect	EA = (An), An ← An + N
Predecrement register indirect	An ← An − N, EA = (An)
Register indirect with offset	EA = (An) + d_{16}
Indexed register indirect with offset	EA = (An) + (Xn) + d_8
Immediate data addressing	
Immediate	DATA = Next word(s)
Quick immediate	Inherent data
Implied addressing	
Implied register	EA = SR, USP, SP, PC

Notes :

EA : Effective Address.
An : Address Register.
Dn : Data Register.
Xn : Address or Data Register Used as Index Register.
SR : Status Register.
PC : Program Counter.
( ) : Contents of.
d_8 : 8-Bit Offset (Displacement).
d_{16} : 16-Bit Offset (Displacement).
N : 1 for byte, 2 for word, and 4 for long word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundary.
← : Replaces.

6.4 · Instruction set overview

The TS 68000 instruction set is shown in table 4. Some additional instructions are variations, or subsets, of these and they appear in table 5. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can be used any of the 14 addressing modes Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, «quick» arithmetic operations, BCD arithmetic, and expanded operation (through traps).

Table 4 · Instruction set summary

Mnemonic	Description
ABCD	Add Decimal With Extend
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical Or
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Sey Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Table 5 · Variation of instruction types

Instruction type	Variation	Description
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND	Logical And
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition Codes
	ANDI to SR	And Immediate to Status Register
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive Or
	EORI	Exclusive Or Immediate
	EORI to CCR	Exclusive Or Immediate to Condition Codes
	EORI to SR	Exclusive Or Immediate to Status Register
MOVE	MOVE	Move
	MOVEA	Move Address
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVEA to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical Or
	ORI	Or Immediate
	ORI to CCR	Or Immediate to Condition Codes
	ORI to SR	Or Immediate to Status Register
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

5

6.5 - Designation of the terminals

The function, category and relevant symbol of each terminal of the device are given in the following table 6.

Table 6

Symbol	Function	Category
V_{CC}	Power supply (2 terminals)	Supply terminals
V_{GND}	Power supply (2 terminals)	
FC0 to FC2	Processor status	Outputs
$\overline{IPL0}$ to $\overline{IPL2}$	Interrupt control	Inputs
A1 to A23	Address Bus	Outputs
$\overline{AS}$	Asynchronous Bus Control	Outputs
R / $\overline{W}$		
$\overline{UDS}$		
$\overline{LDS}$		
$\overline{DTACK}$		Input
$\overline{BR}$	Bus arbitration Control	Inputs
$\overline{BGACK}$		
$\overline{BG}$		Output
$\overline{BERR}$	System control	Input
$\overline{RESET}$		Input / Output
$\overline{HALT}$		
$\overline{VPA}$	6800 peripheral control	Input
$\overline{VMA}$		Output
E		Output
CLK	Clock	Input
D0 to D15	Data Bus	Input / Output
(*) V_{SS} is the reference terminal for the voltages.		

6.6 - Initialisation of the device

6.6.1 - Power supply sequencing

V_{CC} and V_{GND} have to be connected before power supply V_{CC} increases to the full operational value.

In addition, for power up, the microprocessor TS 68000 shall be held with low level to the $\overline{RESET}$ for at least 100 milliseconds to allow stabiliation of the die circuitry.

6.6.2 - Initialisation procedure after power up

The microprocessor TS 68000 is initialised by only application of low level to the $\overline{RESET}$ input during at least 10 clock periods after V_{CC} has reached its operating value.

6.7 - Detailed block diagram

The functional block diagram is given in figure 13 below.

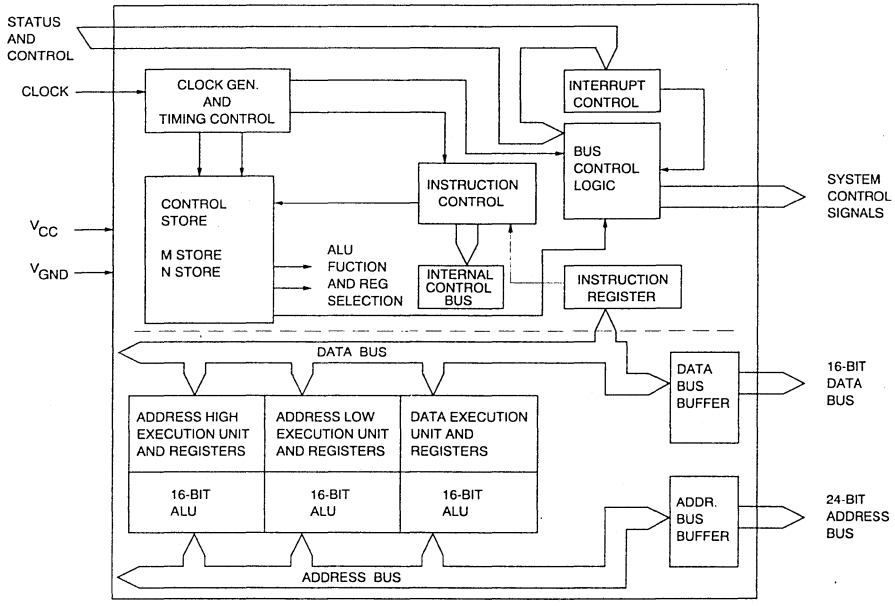


Figure 13 : Block diagram.

6.8 - Signal description

The input and output signals can be functionally organized into the groups shown in figure 14.

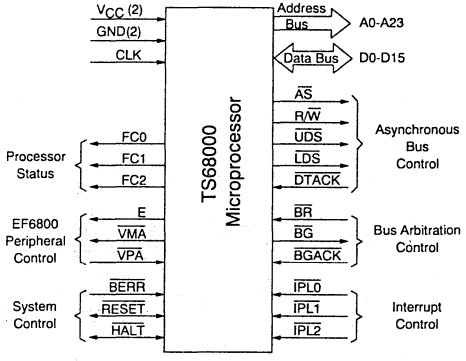


Figure 14 : Input and output signals.

6.9 - Interface with 6800 peripherals

Extensive line of 6800 peripherals are directly compatible with the TS 68000.

Note : It is the own user's responsibility to verify the actual 6800 peripheral performances to be compatible to the actual used TS 68000 microprocessor performances.

Some of 6800 peripherals that are particularly useful are :

- **6821** Peripheral interface adapter,
- **6840** Programmable timer module,
- **6850** Asynchronous communications interface adapter,
- **6852** Synchronous serial data adapter,
- **6854** Advanced data link controller.

To interface the synchronous 6800 peripherals with the asynchronous TS 68000, the processor modifies its bus cycle to meet the 6800 cycle requirements whenever an 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 15 is a flowchart of the interface operation between the processor and 6800 devices.

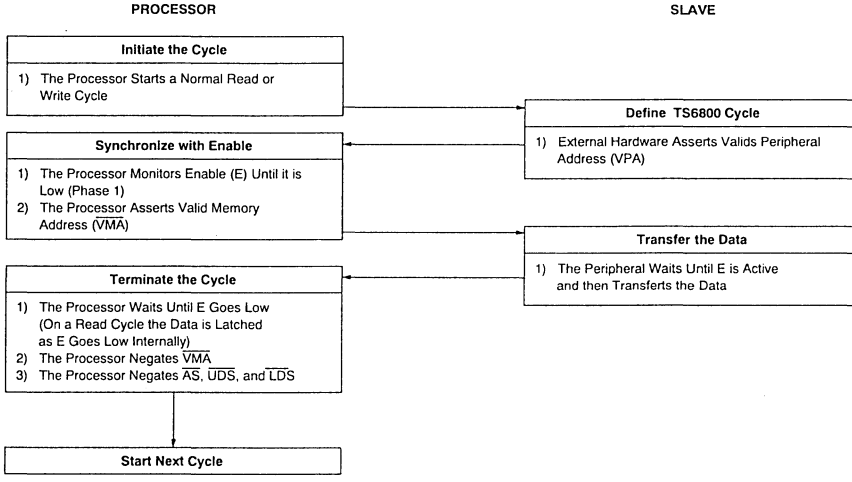


Figure 15 : 6800 interfacing flowchart.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

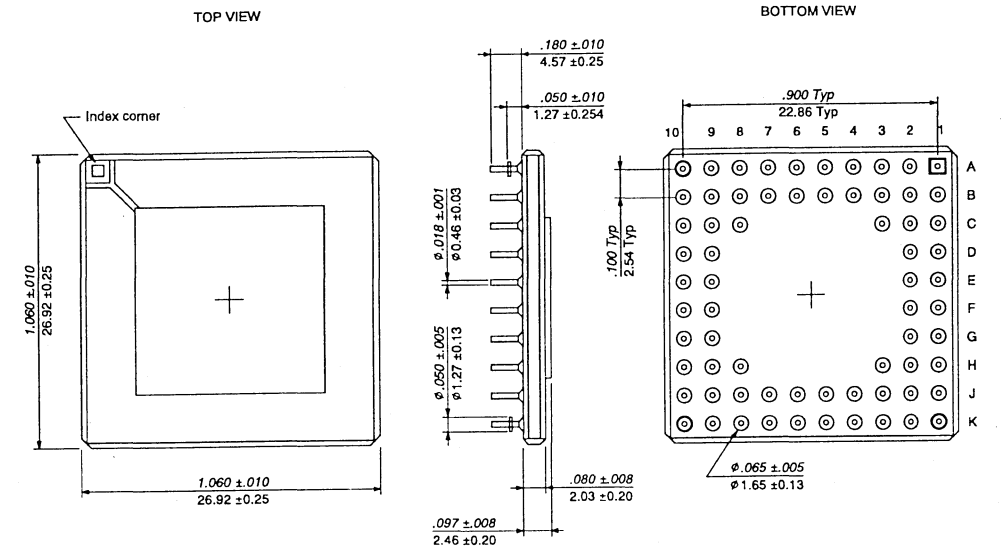
8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

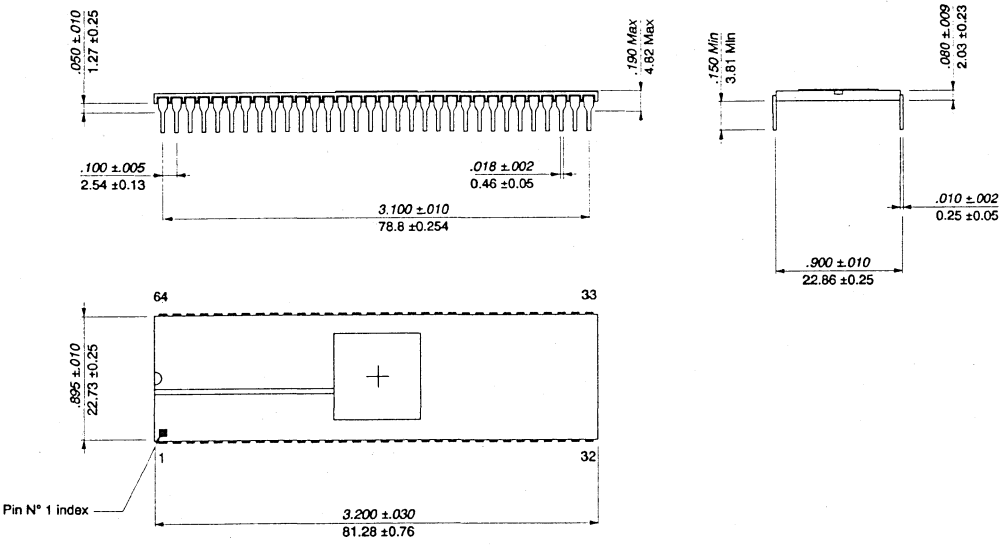
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

9 - PACKAGE MECHANICAL DATA

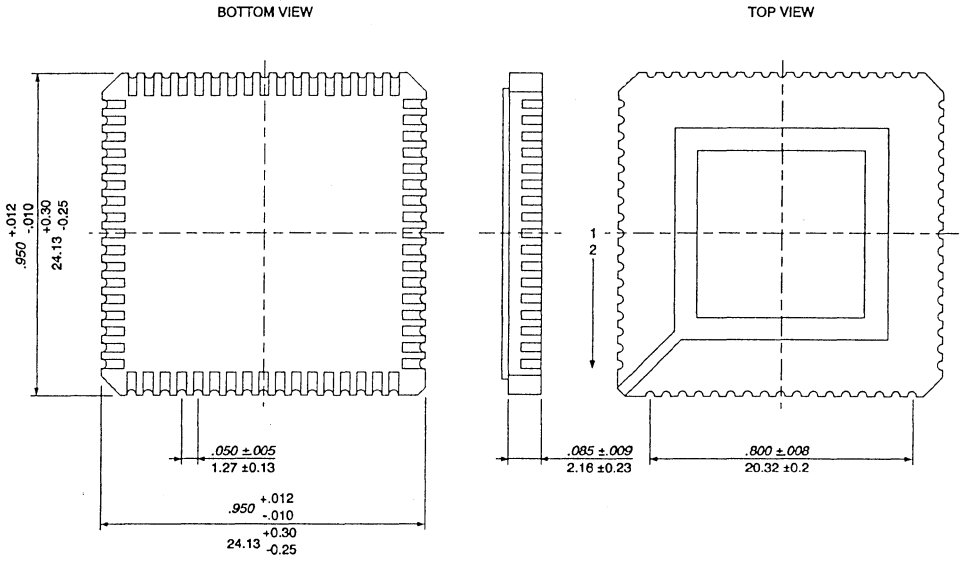
9.1 - 68 pins - Pin Grid Array



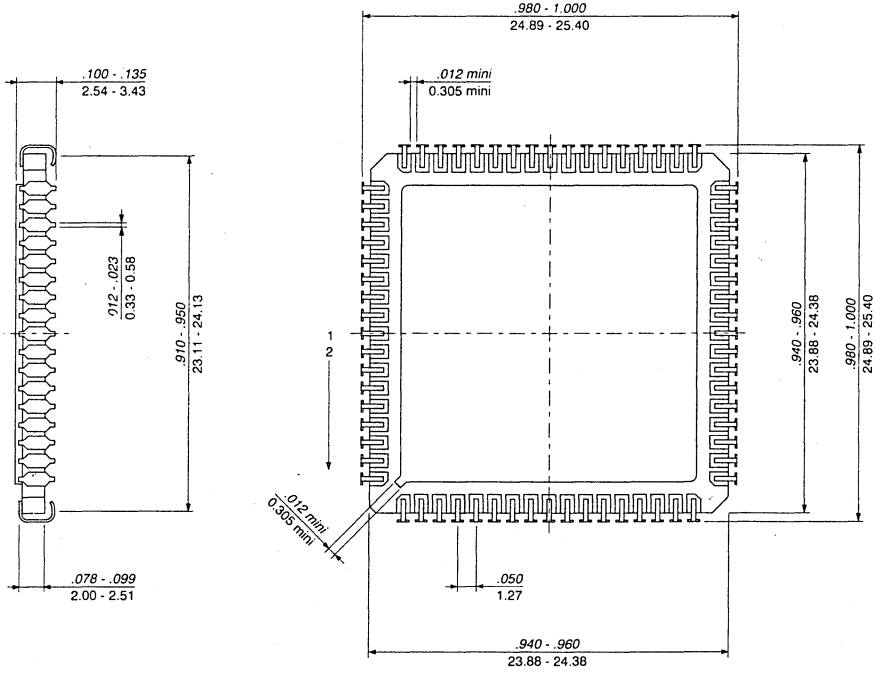
9.2 - 64 pins - Ceramic Side Brazed Package



9.3 - 68 pins - Leadless Ceramic Chip Carrier

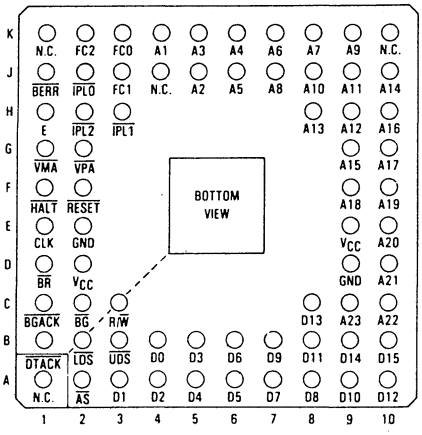


9.4 - 68 pins - Leaded Ceramic Chip Carrier (on request only)

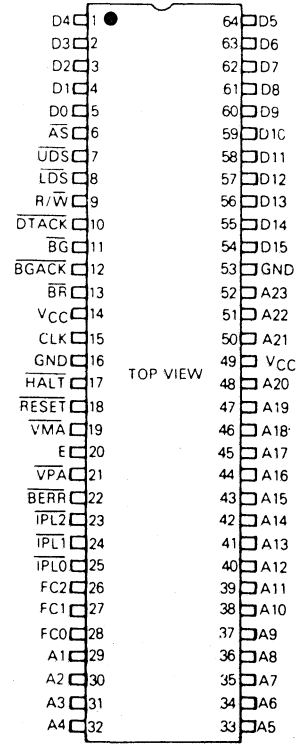


10 - TERMINAL CONNECTIONS

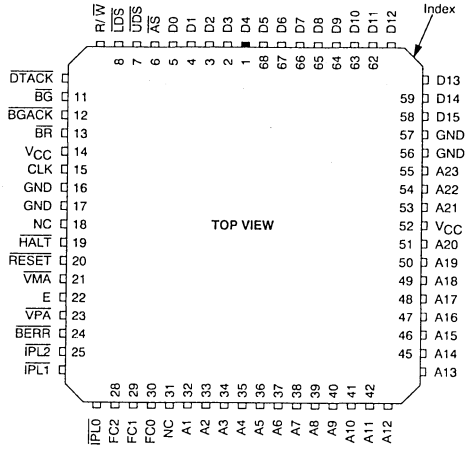
10.1 - 68 pins - Pin Grid Array



10.2 - 64 pins - Ceramic DIL

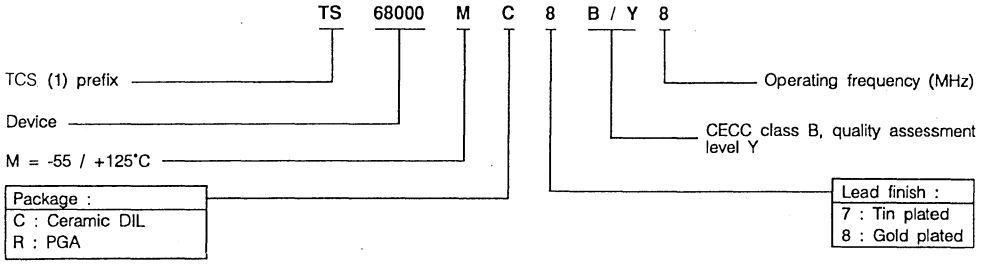


10.3 · 68 pins · Leaded and Leadless Ceramic Chip Carrier

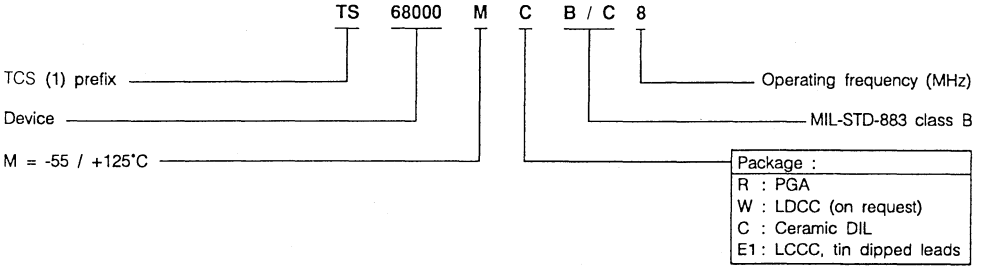


11 · ORDERING INFORMATION

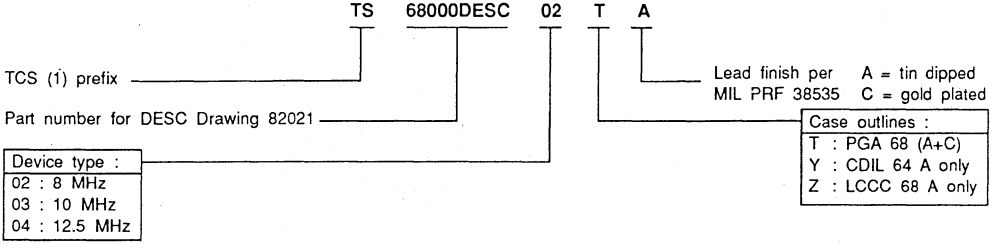
11.1 · CECC (CECC spec number is 90110-001)



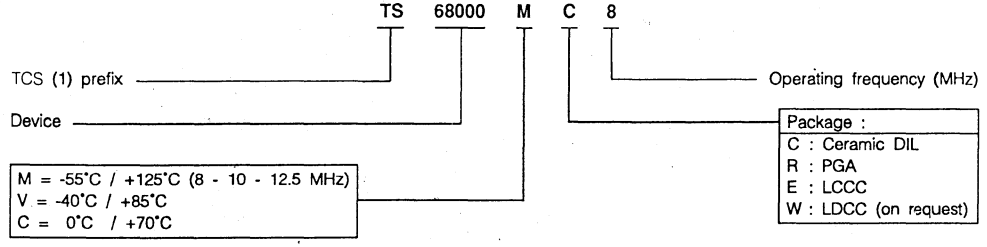
11.2 · MIL-STD-883



11.3 · DESC



11.4 · Standard product



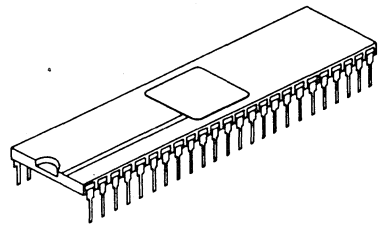
Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

TS 68230

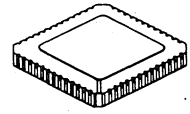
HMOS HIGH DENSITY N-CHANNEL SILICON-GATE PARALLEL INTERFACE / TIMER

DESCRIPTION

The TS 68230 parallel interface/timer (PI/T) provides versatile double buffered parallel interfaces and a system oriented timer for TS 68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is on input or output. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or auto-vectored interrupts, and also provide a DMA request pin for connection to a direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.



C suffix
DIL 48
Ceramic Side Brazed package



E suffix
LCCC 52
Leadless Ceramic Chip Carrier

See the Ordering Information at the end of the data sheet.

MAIN FEATURES

- TS 68000 bus compatible.
- Port modes include :
  - Bit I/O,
  - Unidirectional 8-bit and 16-bit,
  - Bidirectional 8-bit and 16-bit,
- Programmable handshaking options.
- 24-bit programmable timer modes.
- Five separate interrupt modes.
- Separate port and timer interrupt service requests.
- Registers are read/write and directly addressable.
- Registers are addressed for MOVEP (move peripheral) and DMAC compatibility.
- $V_{CC} = 5\ V_{DC} \pm 5\ \%$.

SCREENING / QUALITY

This part is manufactured in full compliance with :

- DESC/SMD 5962-93170.
- MIL-STD-883, class B.
- TCS standard.

SUMMARY

A - GENERAL DESCRIPTION

1 - INTRODUCTION

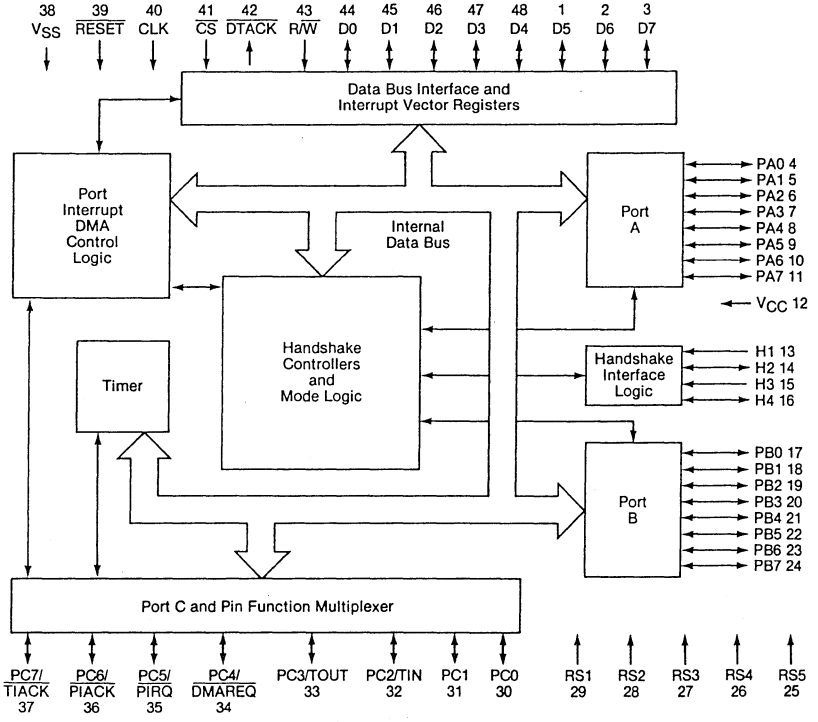
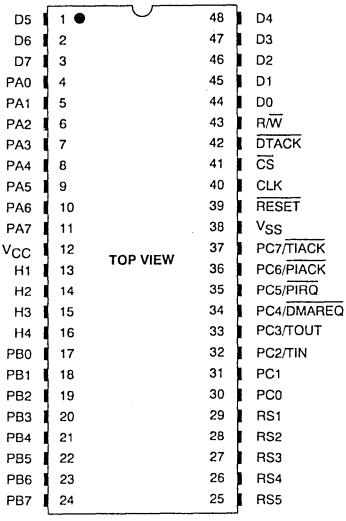
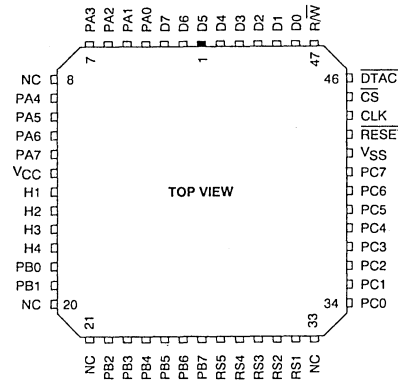


Figure 1 : TS 68230 block diagram.

2 · PIN ASSIGNMENTS



DIL 48



LCCC 52

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the peripheral TS 68230 processes in HMOS technology and class B in compliance with the MIL-STD-883.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535, appendix A : general specification for microcircuits.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be as shown in § A.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 · Package

The microcircuits are packaged in a hermetically sealed ceramic package which is conformed to case outlines of MIL-STD-1835.

- 48-lead DIP case outline : D-14
- 52-Terminal SQ.LCC case outline : C-6

The precise case outlines are described in § 8 of this document.

3.3 · Electrical requirements

3.3.1 · Absolute maximum ratings

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_d	Power dissipation	T_{case} = −55°C		800	mW
		T_{case} = +125°C		500	mW
T_c	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{lead}	Lead temperature	Max. 5 sec. soldering		+270	°C

5

3.3.2 · Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal.

Symbol	Parameter	Model	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_{IL}	Low level input voltage (except input H1, H2, H3, H4)		0	0.8	V
V_{IL}	Low level input H1, H2, H3, H4		0	0.5	V
V_{IH}	High level input voltage		2.0	5.25	V
T_{case}	Operating temperature		−55	+125	°C
R_L	Value of output load resistance		see Note		Ω
C_L	Output loading capacitance			see Note	pF
$t_{r(c)}$	Clock rise time (see Figure 2)			10	ns
$t_{f(c)}$	Clock fall time (see Figure 2)			10	ns
f_c	Clock frequency (see Figure 2)	TS 68230-8	2	8	MHz
		TS 68230-10	2	10	
t_{cyc}	Cycle time (see Figure 2)	TS 68230-8	125	500	ns
		TS 68230-10	100	500	
$t_{w(cL)}$	Clock pulse width low (see Figure 2)	TS 68230-8	55	250	ns
		TS 68230-10	45	250	
$t_{w(cH)}$	Clock pulse width high (see Figure 2)	TS 68230-8	55	250	ns
		TS 68230-10	45	250	

Note : Load network number 1 and 2 as specified in (Figure 5.2.2) gives the maximum loading of the relevant output.

3.3.3 · Electrical performance conditions

The electrical performance characteristics are specified in Tables 1 and 2 and are applied over full operating temperature range unless otherwise specified (see § 10).

3.4 · Mechanical and environmental

The microcircuits shall meet all mechanical and environmental requirements of MIL-STD-883 for class B devices.

3.5 · Marking

The documents where are defined the marking are identified in the reference documents (3) to (8).

Each microcircuit are legible and permanently marked with the following informations as minimum :

3.5.1 · Thomson logo
3.5.2 · Manufacturer's part number
3.5.3 · class B identification
3.5.4 · Date-code of inspection lot
3.5.5 · ESD identifier if available
3.5.6 · Country of manufacturing

3.6 · Thermal characteristics

Symbol	Parameter	Value	Unit
$\theta_{J\text{-}C}$	Thermal resistance junction to case DIL 48	10	°K/W
$\theta_{J\text{-}C}$	Thermal resistance junction to case LCC 52	6	°K/W
$\theta_{J\text{-}A}$	Thermal resistance junction to ambient DIL 48	45	°K/W
$\theta_{J\text{-}A}$	Thermal resistance junction to ambient LCC 52	50	°K/W

4 · QUALITY CONFORMANCE INSPECTION

4.1 · MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883.

Group A & B inspection are performed on each inspection lot or as specified in method 5005 of MIL-STD-883.

Group C & D are performed on a periodic basis in accordance with MIL-M-38510.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 1 : Static electrical characteristics for all electrical variants.
- Table 2A : Dynamic electrical characteristics for 68230-8 (8 MHz).
- Table 2B : Dynamic electrical characteristics for 68230-10 (10 MHz).

For static characteristics (Table 1), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to § 5.2 / 5.3 / 5.6.5 of this specification (Tables 2A and 2B).

Indication of «min» or «max» in the column «Test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.3 here above.

5.2 · Test conditions specific to the device

5.2.1 · Loading network

The applicable loading network shall be as defined in column «Test conditions» of Tables 2A and 2B, refering to the loading network number as shown in figure below.

Load NBR	Figure	R1	R2	C1	Output application
B	5.2.2.1	750	19 k	82 pF	D0-D7
T	5.2.2.2	1.62 k	24.3 k		PC0, PC1, PC2, PC4, PC6, PC7
S	5.2.2.3	1.62 k	16.2 k		PA0-PA7, H2, H4, PB0-PB7
U	5.2.2.4	475			PC5, PC3
E	5.2.2.5	750		82 pF	$\overline{\text{DTACK}}$

5.2.2 · Figures

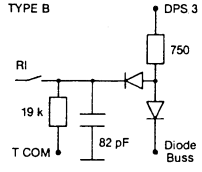


Figure 5.2.2.1

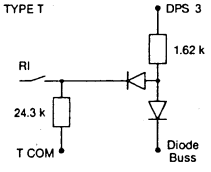


Figure 5.2.2.2

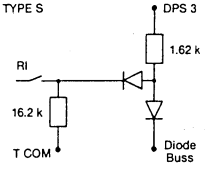


Figure 5.2.2.3

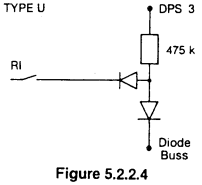


Figure 5.2.2.4

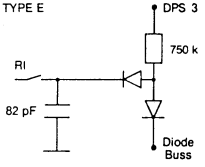


Figure 5.2.2.5

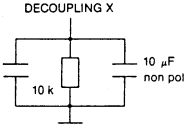


Figure 5.2.2.6

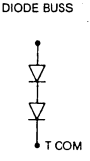


Figure 5.2.2.7

5.3 - Time definition

5.3.1 - Read and write cycle timings

1 - See 1.4 Bus Interface Operation for exception.

2 - This specification only applies if the PI/T had completed all operations initiated by previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted if $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

3 - Assuming the RS1-RS5 to data valid time has also expired.

4 - This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

5 - Synchronized means that the input signal has been by the PI/T on the appropriate adge of the clock (rising edge for H1 (H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

6 - This limit applies to the frequency of the signal at TIN compared to the fraquency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90 % of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100 % of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an "AND" function of the clock and a control signal.

7 - CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

5.3.2 - Peripheral input timings

1 - This specification assures recognition of the asserted edge to H1 (H3).

2 - This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

3 - The maximum value is caused by a peripheral access (H1) (H3) asserted and bus access (CS asserted) occuring at the same time.

4 - Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1 (H3) and falling edge for CS). (Refer to the 1.4 Bus Interface Operation for the exception concerning CS).

5 - If the setup time on the rising edge of the clock is not met, H1 (H3) may not be recognized until the next rising of the clock.

5.3.3 - Peripheral output timings

1 - This specification assures recognition of the asserted edge to H1 (H3).

2 - This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

3 - The maximum value is caused by a peripheral access (H1) (H3) asserted and bus access ($\overline{CS}$ asserted) occuring at the same time.

4 - Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1 (H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

5 - If the setup time on the rising edge of the clock is not met, H1 (H3) may not be recognized until the next rising of the clock.

5.4 · Static characteristics for all covered models

Table 1

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
1	I_{CC}	Supply current	41	V_{CC} = 5.25 V	all		133	mA
2	V_{OL}	Low level output PC3/TOUT, PC5/$\overline{PIRQ}$	37	I_{OL} = 8.8 mA V_{CC} = 4.75 V	all		0.5	V
3	V_{OL}	Low level output voltage D0/D7, $\overline{DTACK}$	37	I_{OL} = 5.3 mA V_{CC} = 4.75 V	all		0.5	V
4	V_{OL}	Low level output voltage PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	37	I_{OL} = 2.4 mA V_{CC} = 4.75 V	all		0.5	V
5	V_{OH}	High level output D0-D7, $\overline{DTACK}$	37	I_{OH} = −400 µA V_{CC} = 4.75 V	all	2.4		V
6	V_{OH}	High level output voltage H2, H4, PB0-PB7, PA0-PA7	37	I_{OH} = −150 µA V_{CC} = 4.75 V	all	2.4		V
7	V_{OH}	High level output voltage PC0-PC7	37	V_{OH} = −100 µA V_{CC} = 4.75 V	all	2.4		V
8	I_{IH}	High level input current H1, H3, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$ 1) Other inputs at 0 2) Other inputs at 1		V_{IN} = 5.25 V	all		10	µA
9	I_{IL}	Low level input current H1, H3, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$ 1) Other inputs at 0 2) Other inputs at 1		V_{IN} = 0 V	all	−10		µA
10	I_{LO}	Power off leakage			all	−10	+10	µA
11	I_{OZH1}	Tristate input high leakage $\overline{DTACK}$, PC0-PC7, D0-D7		V_{IH} = 2.4 V V_{CC} = 5.25 V	all	−20	+20	µA
12	I_{OZH2}	Tristate input high leakage H2, H4, PA0-PA7, PB0-PB7		V_{IH} = 2.4 V V_{CC} = 5.25 V	all	−0.1	+0.1	mA
13	I_{OZL1}	Tristate input low leakage $\overline{DTACK}$, PC0-PC7, D0-D7		V_{IH} = 0.4 V V_{CC} = 5.25 V	all	−20	+20	µA
14	I_{OZL2}	Tristate input low leakage H2, H4, PA0-PA7, PB0-PB7		V_{IH} = 0.4 V V_{CC} = 5.25 V	all	−0.1	+0.1	mA
15	V_{IH}	High level input voltage (all inputs)			all	2.0	V_{CC} +0.3	V
16	V_{IL}	Low level input voltage (all inputs except H1, H2, H3, H4)			all	−0.3	0.8	V
16A	V_{IL}	Low level input voltage (inputs H1, H2, H3, H4)			all	−0.3	0.5	V
97	C_{IN}	Input capacitance (all inputs)	method 11 IEC 748-2	Reverse voltage = 0 V f = 1.0 MHz	25°C		25	pF
					min		NA	
					max		NA	
98	C_{OUT}	Input capacitance (all inputs)	method 11 IEC 748-2	Reverse voltage = 0 V f = 1.0 MHz	25°C		25	pF
					min		NA	
					max		NA	
99	V_{ESD}	Internal protection Transient energy rating	See 5.3	See 5.3 5 cycles	25°C	−500	+500	V
					min	NA	NA	
					max	NA	NA	

* IEC measurement method number unless otherwise stated.

5

5.5 · Dynamic (switching) characteristics · TS 68230-8

5.5.1 · Read and write cycle timings · TS 68230-8

Table 2A

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
17	t_{su} (TRVSL)	R/$\overline{W}$, RS1-RS5 valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 1	See 5.6.5 (a) to (c) f_C = 8 MHz	0		ns
18	t_h (TSRI)	$\overline{CS}$ low to R/$\overline{W}$ and RS1-RS5 invalid (Note 1)	Fig. 3, 4 Ref. 2	See test 17	100		ns
19	t_{su} (TSLCL)	$\overline{CS}$ low to CLK low (Note 2)	Fig. 3, 4 Ref. 2	See test 17	30		ns
20	t_{phl} t_{plh} (TSLDV)	$\overline{CS}$ low to data out valid (Note 3)	Fig. 3, 4 Ref. 4	See test 17 Load B		75	ns
21	t_{phl} t_{plh} (TRLDV)	RS1-RS5 valid to data out valid	Fig. 3, 4 Ref. 5	See test 17 Load B		140	ns
22	t_{phl} (TCLDL)	CLK low to $\overline{DTACK}$ low (read-write cycle time)	Fig. 3, 4 Ref. 6	See test 17 Load E	0	70	ns
23	t_h (TDTLSH)	$\overline{DTACK}$ low to $\overline{CS}$ high (Note 4)	Fig. 3, 4 Ref. 7	See test 17	0		ns
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 3, 4 Ref. 9	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 3, 4 Ref. 9	See test 17 Load B		50	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high	Fig. 3, 4 Ref. 10	See test 17 Load E	0	50	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high (to $\overline{DTACK}$ high Z)	Fig. 3, 4 Ref. 11	See test 17 Load E	0	100	ns
28	t_{su} (TDVSL)	Data in valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 12	See test 17	0		ns
29	t_h (TSLDI)	$\overline{CS}$ low to data in invalid	Fig. 3, 4 Ref. 13	See test 17 Load B	100		ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 3, 4 Ref. 13	See test 17 Load T		3	CLK. per
32	t_{phl} (TSSCLDMA)	Synchronized $\overline{CS}$ to CLK low on which $\overline{DMAREQ}$ is asserted (Note 5)	Fig. 3, 4 Ref. 32	See test 17 Load T	3	3	CLK. per
33	t_{phl} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 35	See test 17 Load T	0	120	ns
34	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 36	See test 17 Load T	0	120	ns
35	t_{phl} (TSHCLPIA)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is asserted	Fig. 3, 4 Ref. 37	See test 17 Load U	3	3	CLK. per
36	t_{phl} (TSHCLPIZ)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is high Z (Note 5)	Fig. 3, 4 Ref. 38	See test 17 Load U	3	3	CLK. per
37	t_{plz} t_{phl} (TCLPLZ)	CLK low to $\overline{PIRQ}$ low or high-Z	Fig. 3, 4 Ref. 39	See test 17 Load U	0	250	ns

5.5.1 · Read and write cycle timings · TS 68230-8 (Continued)

Table 2A

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
38	t_{cy} (TINPN)	TIN frequency (external CLK) prescaler used (Note 6)	Fig. 3, 4 Ref. 40	See test 17	0	1	f clk (HZ) (Note 7)
39	t_{cy} (TINPN)	TIN frequency (external CLK) prescaler not used	Fig. 3, 4 Ref. 41	See test 17	0	1/8	f clk (HZ) (Note 7)
40	t_w (TIWEC)	TIN pulse width high or low (external CLK)	Fig. 3, 4 Ref. 42	See test 17	55		ns
41	t_w (TIWRH)	TIN pulse width low (RUN/ halt control)	Fig. 3, 4 Ref. 43	See test 17	1		CLK. per
42	t_{plh} t_{plz} (TCTHZ)	CLK low to tout high, low or H-Z	Fig. 3, 4 Ref. 44	See test 17 Load U	0	250	ns
43	t_{phl} (SHSL)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ low	Fig. 3, 4 Ref. 45	See test 17 Load T	50		ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.1.

5

5.5.2 · Peripheral input timings · TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
44	t_{su} (TDVHA)	Port input data valid to H1 (H3) asserted	Fig. 5 Ref. 14	See test 17	100		ns
45	t_h (THADI)	H1 (H3) asserted to port data invalid	Fig. 5 Ref. 15	See test 17 Load B	20		ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 5 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 5 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 5 Ref. 18	See test 17 Load S		150	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 5 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Note 3, 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 5 Ref. 23	See test 17 Load T		3	CLK. per
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17	50		ns

5.5.2 · Peripheral input timings · TS 68230-8 (Continued)

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
54	t_{plh} (TSHCLHA)	Synchronized H1 (H3) to CLK low on which H2 (H4) asserted (Note 3, 4)	Fig. 5 Ref. 33	See test 17 Load S		4.5	ns
34	t_{plh} (TCLDML)	CLK low to $\overline{\text{DMAREQ}}$ low	Fig. 5 Ref. 35	See test 17 Load T	0	120	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{\text{DMAREQ}}$ high	Fig. 5 Ref. 36	See test 17 Load T	0	120	ns
* Measurement method see § 5.2 / 5.3 / 5.6.5. Notes : See § 5.3.2.							

5.5.3 · Peripheral output timings · TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 6 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 6 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 6 Ref. 18	See test 17 Load S		150	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 6 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 6 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 6 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{\text{DMAREQ}}$ is asserted (Note 3, 4)	Fig. 6 Ref. 22	See test 17 Load t	2.5	3.5	ns
30	t_{plh} (TCDMA-CDMN)	CLK low on which $\overline{\text{DMAREQ}}$ is asserted to CLK low on which $\overline{\text{DMAREQ}}$ is negated	Fig. 6 Ref. 23	See test 17 Load T	2.5	3	CLK. per
55	t_{plh} t_{phl} (TCLPOD)	CLK low to port output data valid (Modes 0 or 1)	Fig. 6 Ref. 24	See test 17 Load B		150	ns
56	t_{phl} t_{plh} (TSHDI)	Synchronized H1 (H3) to port output data invalid (Note 3, 4) (Mode 0 and 1)	Fig. 6 Ref. 25	See test 17 Load B	1.5	2.5	CLK per.
57	t_{phl} t_{plh} (THNDV)	H1 negated to port output data valid (Mode 2 and 3)	Fig. 6 Ref. 26	See test 17 Load B		70	ns
58	t_{phz} t_{plz} (THADZ)	H1 asserted to port output data high-Z (Mode 2 and 3)	Fig. 6 Ref. 27	See test 17 Load B		70	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 6 Ref. 30	See test 17 Load T	50		ns
34	t_{plh} (TCLDML)	CLK low to $\overline{\text{DMAREQ}}$ low	Fig. 6 Ref. 35	See test 17 Load T	0	120	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{\text{DMAREQ}}$ high	Fig. 6 Ref. 36	See test 17 Load T	0	120	ns
* Measurement method see § 5.2 / 5.3 / 5.6.5. Notes : See § 5.3.3.							

5.5.4 · IACK timings · TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 7 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSDHZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 7 Ref. 9	See test 17 Load B		50	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 10	See test 17 Load E		50	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 11	See test 17 Load E		100	ns
59	t_{plh} t_{phl} (TCLDVIAC)	CLK low to data output valid interrupt acknowledge	Fig. 7 Ref. 29	See test 17 Load B		120	ns
60	t_{su} (TILCL)	$\overline{PIACK}$ to $\overline{TIACK}$ low to CLK low	Fig. 7 Ref. 31	See test 17	50		ns
61	t_{phl} (TCLDLIAC)	CLK low to $\overline{DTACK}$ low interrupt acknowledge	Fig. 7 Ref. 34	See test 17 Load E		100	ns
* Measurement method see § 5.2 / 5.3 / 5.6.5.							

5

5.6 · Dynamic (switching) characteristics · TS 68230-10

5.6.1 · Read and write cycle timings · TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
17	t_{su} (TRVSL)	R/$\overline{W}$, RS1-RS5 valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 1	See 5.6.5 (a) to (c) f_C = 8 MHz	0		ns
18	t_h (TSRI)	$\overline{CS}$ low to R/$\overline{W}$ and RS1-RS5 invalid (Note 1)	Fig. 3, 4 Ref. 2	See test 17	65		ns
19	t_{su} (TSLCL)	$\overline{CS}$ low to CLK low (Note 2)	Fig. 3, 4 Ref. 3	See test 17	20		ns
20	t_{phl} t_{plh} (TSLDV)	$\overline{CS}$ low to data out valid (Note 3)	Fig. 3, 4 Ref. 4	See test 17 Load B		60	ns
21	t_{phl} t_{plh} (TRLDV)	RS1-RS5 valid to data out valid	Fig. 3, 4 Ref. 5	See test 17 Load B		105	ns
22	t_{phl} (TCLDL)	CLK low to $\overline{DTACK}$ low (read-write cycle time)	Fig. 3, 4 Ref. 6	See test 17 Load E	0	60	ns
23	t_h (TDTLSH)	$\overline{DTACK}$ low to $\overline{CS}$ high (Note 4)	Fig. 3, 4 Ref. 7	See test 17	0		ns
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 3, 4 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 3, 4 Ref. 9	See test 17 Load B		45	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high	Fig. 3, 4 Ref. 10	See test 17 Load E		45	ns

5.6.1 · Read and write cycle timings · TS 68230-10 (Continued)

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 3, 4 Ref. 11	See test 17 Load E		55	ns
28	t_{su} (TDVSL)	Data in valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 12	See test 17	0		ns
29	t_h (TSLDI)	$\overline{CS}$ low to data in invalid	Fig. 3, 4 Ref. 13	See test 17 Load B	65		ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 3, 4 Ref. 23	See test 17 Load T	2.5	3	CLK. per
31	t_{su} (TRDDTL)	Read data valid to $\overline{DTACK}$ low	Fig. 3, 4 Ref. 28	See test 17 Load E	0		ns
32	t_{phl} (TSSCLDMA)	Synchronized $\overline{CS}$ to CLK low on which $\overline{DMAREQ}$ is asserted (Note 5)	Fig. 3, 4 Ref. 32	See test 17 Load T	3	3	CLK. per
33	t_{phl} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 35	See test 17 Load T	0	100	ns
34	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 36	See test 17 Load T	0	100	ns
35	t_{phl} (TSHCLPIA)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is asserted	Fig. 3, 4 Ref. 37	See test 17 Load U	3	3	CLK. per
36	t_{phl} (TSHCLPIZ)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is high Z (Note 5)	Fig. 3, 4 Ref. 38	See test 17 Load U	3	3	CLK. per
37	t_{plz} t_{phl} (TCLPLZ)	CLK low to $\overline{PIRQ}$ low or high-Z	Fig. 3, 4 Ref. 39	See test 17 Load U	0	225	ns
38	t_{cy} (TINPU)	TIN frequency (external CLK) prescaler used (Note 6)	Fig. 3, 4 Ref. 40	See test 17	0	1	f clk (HZ) (Note 7)
39	t_{cy} (TINPU)	TIN frequency (external CLK) prescaler not used	Fig. 3, 4 Ref. 41	See test 17	0	1/8	f clk (HZ) (Note 7)
40	t_w (TIWEC)	TIN pulse width high or low (external CLK)	Fig. 3, 4 Ref. 42	See test 17	45		ns
41	t_w (TIWRH)	TIN pulse width low (RUN/ halt control)	Fig. 3, 4 Ref. 43	See test 17	1		CLK. per
42	t_{plh} t_{plz} (TCTHZ)	CLK low to tout high, low or H-Z	Fig. 3, 4 Ref. 44	See test 17 Load U	0	225	ns
43	t_{phl} (SHSL)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ low	Fig. 3, 4 Ref. 45	See test 17 Load T	30		ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.1.

5.6.2 · Peripheral input timings · TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 5 Ref. 23	See test 17 Load T	2.5	3	CLK. per
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 5 Ref. 35	See test 17 Load T	0	100	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 5 Ref. 36	See test 17 Load T	0	100	ns
44	t_{su} (TDVHA)	Port input data valid to H1 (H3) asserted	Fig. 5 Ref. 14	See test 17	60		
45	t_h (THADI)	H1 (H3) asserted to port data invalid	Fig. 5 Ref. 15	See test 17 Load B	20		ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 5 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 5 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 5 Ref. 18	See test 17 Load S		120	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 5 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Notes 3 and 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17	40		ns
54	t_{plh} (TSHCLHA)	Synchronized H1 (H3) to CLK low on which H2 (H4) asserted (Notes 3 and 4)	Fig. 5 Ref. 33	See test 17 Load S	3.5	4.5	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.2.

5

5.6.3 · Peripheral output timings · TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
30	t_{phl} (TCDMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 6 Ref. 23	See test 17 Load T	2.5	3	CLK. per
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 6 Ref. 35	See test 17 Load T	0	100	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 6 Ref. 36	See test 17 Load T	0	100	ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 6 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 6 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 6 Ref. 18	See test 17 Load S		120	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 6 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Notes 3 and 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17 Load T	40		ns
55	t_{plh} t_{phl} (TCLPOD)	CLK low to port output data valid (Modes 0 or 1)	Fig. 5 Ref. 24	See test 17 Load B		120	ns
56	t_{phl} t_{plh} (TSHDI)	Synchronized H1 (H3) to port output data invalid (Notes 3 and 4) (Mode 0 and 1)	Fig. 5 Ref. 25	See test 17 Load B	1.5	2.5	CLK per.
57	t_{phl} t_{plh} (THNDV)	H1 negated to port output data valid (Mode 2 and 3)	Fig. 5 Ref. 26	See test 17 Load B		60	ns
58	t_{phz} t_{plz} (THADZ)	H1 asserted to port output data high-Z (Mode 2 and 3)	Fig. 5 Ref. 27	See test 17 Load B	0	70	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.3.

5.6.4 · IACK timings · TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 7 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 7 Ref. 9	See test 17 Load B		45	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 10	See test 17 Load E		45	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 11	See test 17 Load E		55	ns
59	t_{plh} t_{phl} (TCLDVIAC)	CLK low to data output valid interrupt acknowledge cycle	Fig. 7 Ref. 29	See test 17 Load B		105	ns
60	t_{su} (TILCL)	$\overline{PIACK}$ to $\overline{TIACK}$ low to CLK low	Fig. 7 Ref. 31	See test 17	40		ns
61	t_{phl} (TCLDLIAC)	CLK low to $\overline{DTACK}$ low interrupt acknowledge cycle	Fig. 7 Ref. 34	See test 17 Load E		100	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

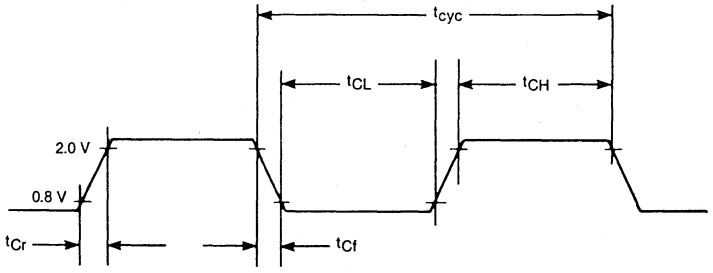


Figure 2 : Clock input timing diagram.

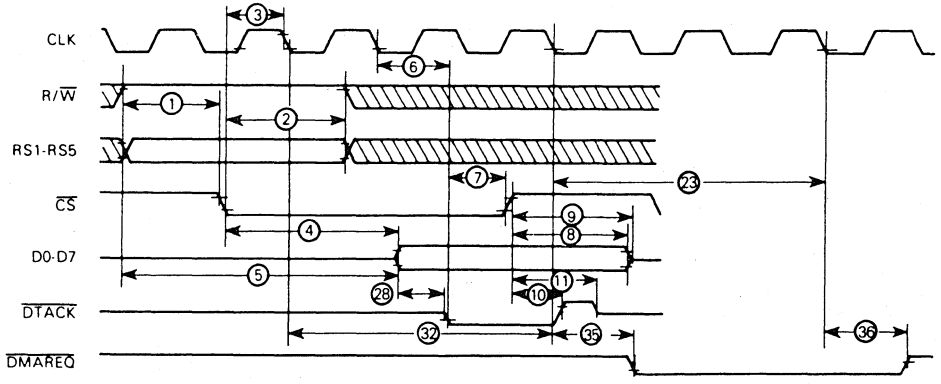


Figure 3 : Read cycle timing diagram.

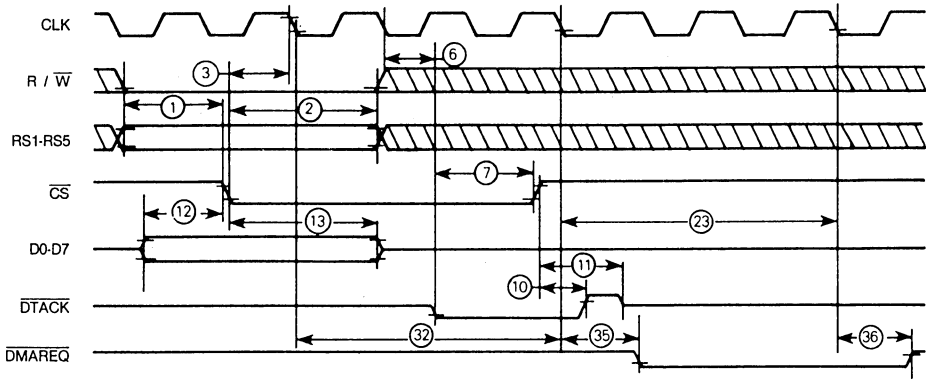


Figure 4 : Write cycle timing diagram.

Note : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

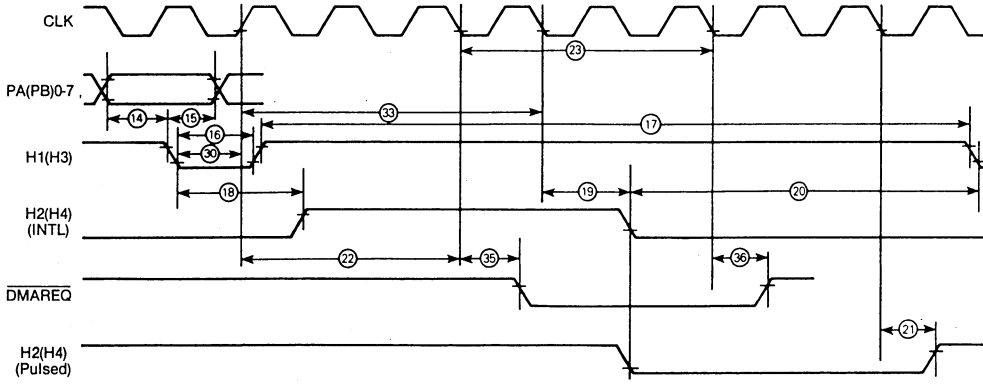


Figure 5 : Peripheral input timing diagram.

Note 1 : Timing diagram shows H1, H2, H3 and H4 asserted low.
Note 2 : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

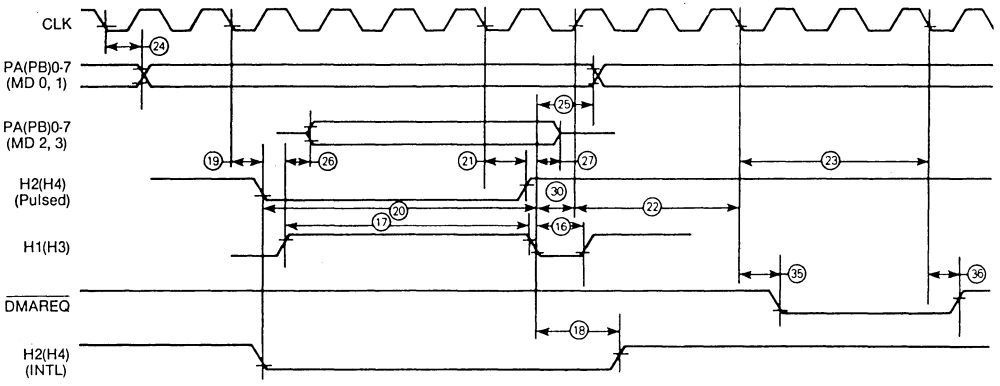


Figure 6 : Peripheral output timing diagram.

Note 1 : Timing diagram shows H1, H2, H3 and H4 asserted low.
Note 2 : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

5

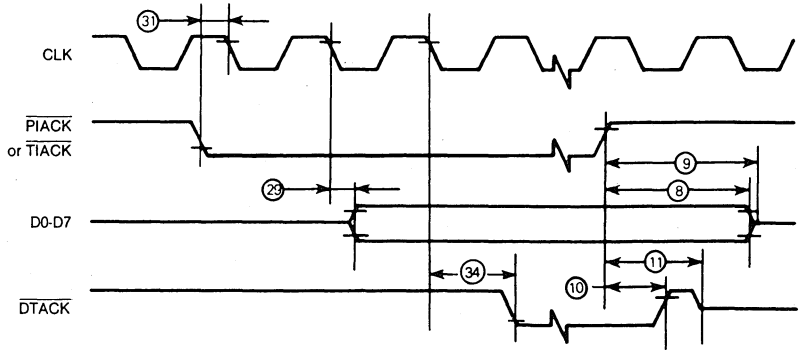


Figure 7 : IACK timing diagram.

Note : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

5.6.5 · Input and output signals for dynamic measurements

a) Input pulse characteristcs

Where input pulse generator is loaded by a 90 Ω resistor, the input pulse characteristics shall be as shown in figure 8.

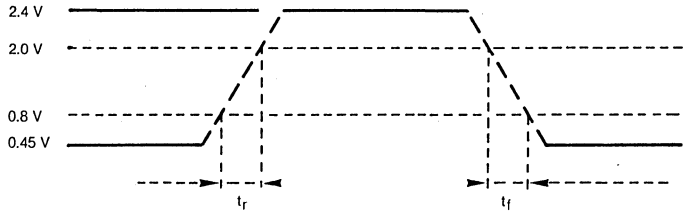


Figure 8 : Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurements shall be :

$$V_{IL} = 0.8\ V$$
$$V_{IH} = 2.0\ V$$

c) Time measurement output voltage reference for time valid state output

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in figure 9.

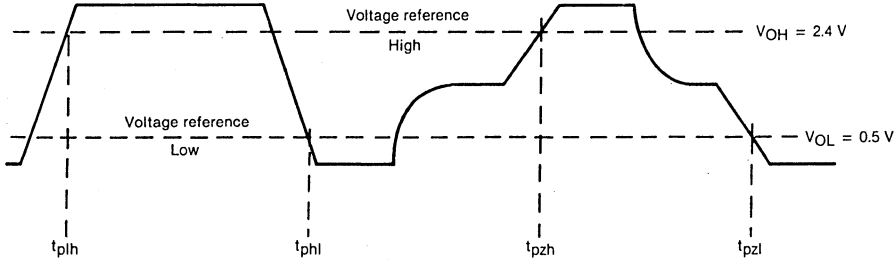


Figure 9 : Ouput voltage references.

6 · PREPARATION FOR DELIVERY

6.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

6.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

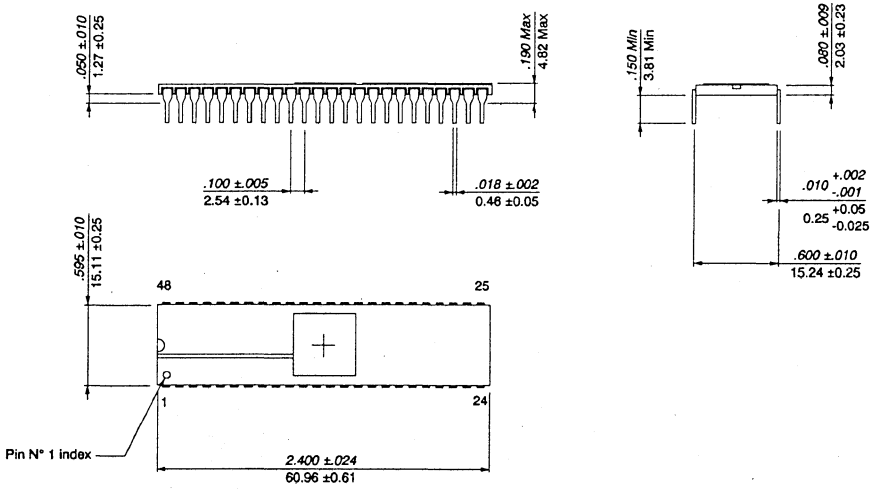
7 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

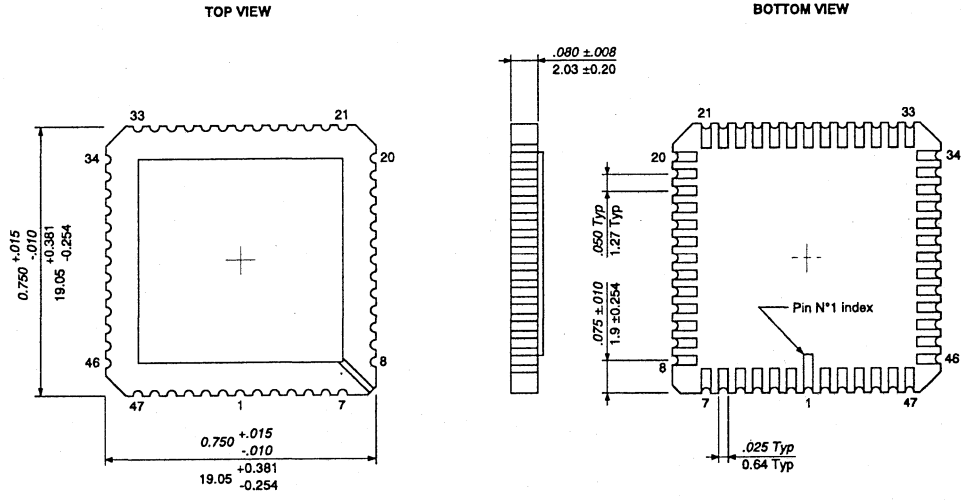
a) Devices should be handled on benches with conductive and grounded surfaces.
b) Ground test equipment, tools, and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent, if practical.

8 · PACKAGE MECHANICAL DATA

8.1 · 48 pins · Ceramic Side Brazed package



8.2 · 52 pins · Leadless Ceramic Chip Carrier



9 · TERMINAL CONNECTIONS

9.1 · Ceramic DIL

See § A.2.

9.2 · LCCC

See § A.2.

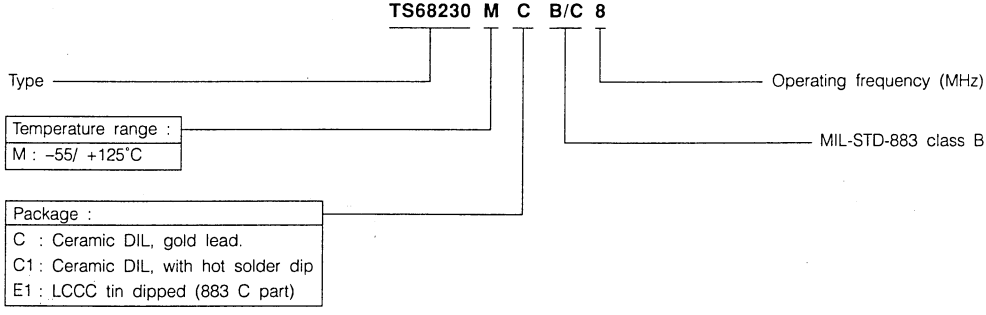
9.3 · Terminal designation of the device

The function, category and relevant symbol of each terminal of the device are given in the following table :

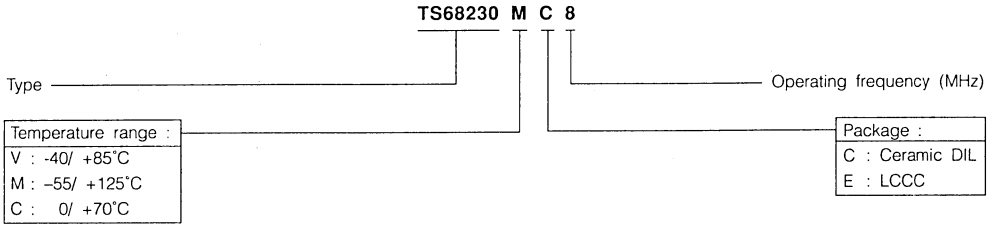
Symbol	Function	Category
V_{CC}	Power supply	Supply Terminals
V_{SS}	Power supply	
D0-D7	Bidirectionnal data bus	Bi-directionnal
RS1-RS5	Register select	Input
$R/\overline{W}$	Read / Write	Input
$\overline{CS}$	Chip select	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
$\overline{RESET}$	Reset	Input
CLK	Clock	Input
PA0-PA7 PB0-PB7	Port A and Port B	Input / Output
H1-H3	Handshake Pins	Input
H2-H4	Handshake Pins	Input or Output
PC0-PC7	Port C	Input or Output

10 · ORDERING INFORMATION

10.1 · MIL-STD-883



10.2 · Standard product



10.3 · DESC

Refer to 5962-93170.

5

SERIAL INPUT / OUTPUT CONTROLLER

DESCRIPTION

The TS 68564 SIO (Serial Input Output) is a dual-channel, multi-function peripheral circuit, designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, however within that role, it is systems software configurable so that its «personality» may be optimized for any given serial data communications application.

The TS 68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The TS 68564 can generate and check CRC codes in any synchronous mode and may be programmed to check date integrity in various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

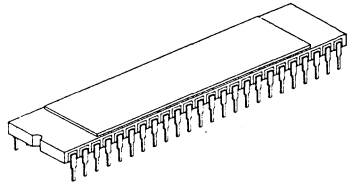
FEATURES

- Compatible with TS 68000 CPU.
- Compatible with TS 68000 Series DMA's.
- Two independent, full-duplex channels.
- Two independent baud rate generators
  - Crystal oscillator input
  - Single-phase TTL clock input.
- Directly addressable registers (all control registers are read/write).
- Data rate in synchronous or asynchronous modes
  - 0-1.25 M bits/second with 5.0 MHz system clock rate.
- Self-test capability.
- Receive data registers are quadruply buffered ; transmit data registers are doubly buffered.
- Daisy-chain priority interrupt logic provides automatic interrupt vectoring without external logic.
- Modem status can be monitored
  - Separate modem controls for each channel.
- Asynchronous features
  - 5, 6, 7 or 8 bits/character
  - 1, 1 1/2 or 2 stop bits
  - Even, odd, or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection.
- Byte synchronous features
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC-16 or CRC-CCITT block check generation and checking.
- Bit synchronous features
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handing
  - Valid receive messages protected from overrun
  - CRC-CCITT block check generation and checking.
- Military temperature range
  – 55/ + 125°C (3, 4 and 5 MHz).

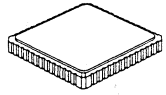
SCREENING / QUALITY

This product is manufactured in full compliance with :

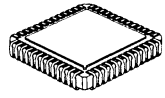
- MIL-STD-883 (class B).
- TCS STANDARDS.



C suffix
DIL 48
Ceramic side brazed package



E suffix
LCCC 52
Leadless ceramic chip carrier



W suffix (on request)
LDCC 52
Leaded ceramic chip carrier

PIN CONNECTIONS (See chapter 9)
See the Ordering Information at the end of the data sheet.

5

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The TS 68564 SIO is a dual-channel, Serial Intput/Output Controller designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to parallel, parallel-to-serial converter/controller ; however, within that role, it is systems software configurable so that it may be optimized for any given serial data communications application.

The TS 68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The TS 68564 can generate and check CRC codes in any synchronous mode and may be programmed to check integrity various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

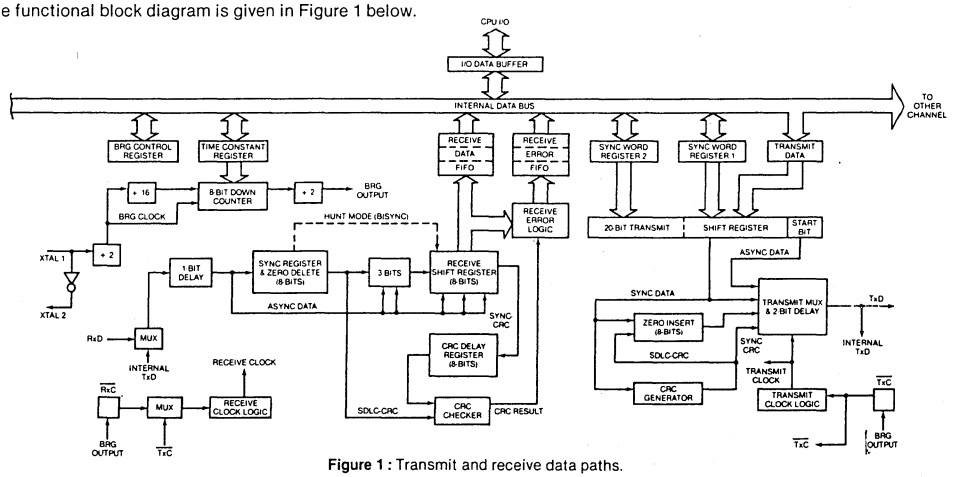


Figure 1 : Transmit and receive data paths.

2 - PIN ASSIGNMENTS

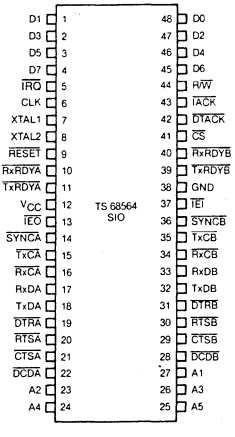


Figure 2.1 : Pin DIL package (top view).

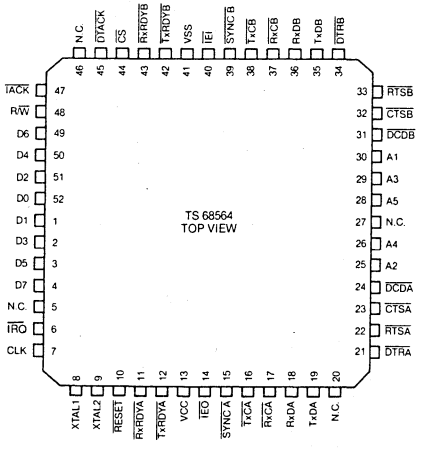


Figure 2.2 : Terminal chip carrier packages (codes : E and W).

3 · TERMINAL DESIGNATIONS OF THE DEVICE

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply	Supply
V_{SS}*	Power supply	Terminals
$\overline{CS}$	Chip select	Input
R/$\overline{W}$	Read/Write	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
A1 to A15	Address bus	Inputs
D0 to D7	Data bus	Bi-directionnal
CLK	Clock	Input
$\overline{RESET}$	Device Reset	Input
$\overline{IRQ}$	Interrupt Request	Output
$\overline{IACK}$	Interrupt Acknowledge	Input
$\overline{IEI}$	Interrupt Enable In	Input
$\overline{IEO}$	Interrupt Enable Out	Output
XTAL1-XTAL2	Baude rate generator inputs	Input
$\overline{RxRDYA}$, $\overline{RxRDYB}$	Receiver ready	Output
$\overline{TxRDYA}$, $\overline{TxRDYB}$	Transmitter ready	Output
$\overline{CTSA}$, $\overline{CTSB}$	Clear to send	Input
$\overline{DCDA}$, $\overline{DCDB}$	Data carrier detect	Input
RxDA, RxDB	Receive data	Input
TxDA, TxDB	Transmit data	Output
$\overline{RxCA}$, $\overline{RxCB}$	Receiver clock	Input/Output
$\overline{TxCA}$, $\overline{TxCB}$	Transmitter clock	Input/Output
$\overline{RTSA}$, $\overline{RTSB}$	Request to send	Output
$\overline{DTRA}$, $\overline{DTRB}$	Data terminal ready	Output
$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronisation	Input/Output

* V_{SS} is the reference terminal for the voltages.

4 - PIN DESCRIPTION

GND : Ground.

V_{CC} : +5 Volts (± 5 %).

$\overline{CS}$: Chip Select (input, active low). $\overline{CS}$ is used to select the TS 68564 SIO for accesses to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

R/$\overline{W}$: Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle.

$\overline{DTACK}$: Data Transfert Acknowledge (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that the data is ready, or that data has been accepted by the TS 68564 SIO.

A1-A5 : Address Bus (inputs). The address bus is used to address one of the internal registers during a read or write cycle.

D0-D7 : Data Bus (bi-directionnal, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.

CLK : Clock (input). This input is used to provide the internal timing for the TS 68564 SIO.

$\overline{RESET}$: Device reset (input, active low). Reset disables both receivers and transmitters, forces TxDA and TxDB to a marking condition, forces the modem controls high, and disables all interrupt. With the exception of the status registers, data registers, and the vector register, all internal registers are cleared. The vector register is reset to «OFH».

$\overline{IRQ}$: Interrupt Request (output, active low, open drain). $\overline{IRQ}$ is asserted when the TS 68564 SIO is requesting an interrupt. $\overline{IRQ}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.

$\overline{IACK}$: Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the TS 68564 SIO that the CPU is acknowledging an interrupt. CS and $\overline{IACK}$ must not be asserted at the same time. If interrupts are not used then $\overline{IACK}$ should be pulled high.

$\overline{IEI}$: Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the TS 68564 SIO that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the TS 68564 SIO nor another higher priority peripheral is requesting interrupt service.

XTAL1
XTAL2 : Baud Rate Generator inputs. A crystal may be connected between XTAL1 and XTAL2, or XTAL1 may be driven with a TTL Level clock. When using a crystal, external capacitors must be connected. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float.

$\overline{RxRDYA}$
$\overline{RxRDYB}$: Receiver Ready. Outputs, active low. Programmable DMA output for the receiver. The $\overline{RxRDY}$ pins pulse low when a character is available in the receive buffer.

$\overline{TxRDYA}$
$\overline{TxRDYB}$: Transmitter Ready. Outputs, active low. Programmable DMA output for the transmitter. The $\overline{TxRDY}$ pins pulse low when the transmit buffer is empty.

$\overline{CTSA}$
$\overline{CTSB}$: Clear to send. Inputs, active low. If Tx Auto Enables is selected, these inputs enable the transmitter of their respective channels. If Tx Auto Enable is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.

DCBA
DCDB : Data carrier detect. Inputs, active low. If Rx Auto Enables is selected, these inputs enable the receiver of their respective channels. If RX Auto Enable is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.

RxDA
RxDB : Receive Data. Inputs, active high. Serial data input to the receiver.

TxDA
TxDB : Transmit Data. Outputs, active high. Serial data output of the transmitter.

$\overline{RxCA}$
$\overline{RxCB}$: Receiver Clocks. Input/output. Programmable pin receive clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.

$\overline{TxCA}$
$\overline{TxCB}$: Transmitter Clocks. Input/output. Programmable pin, transmit clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.

$\overline{RTSA}$
$\overline{RTSB}$: Request to Send. Outputs, active low. These outputs follow the inverted state programmed into the $\overline{RTS}$ bit. When the $\overline{RTS}$ bit is reset in the asynchronous mode, the output will not change until the character in the transmitter is completely shifted out. These pins may also be used as general purpose outputs.

$\overline{DTRA}$
$\overline{DTRB}$: Data Terminal Ready. Outputs, active low. These outputs follow the inverted state programmed into the DTR bit. These pins may also be used as general purpose outputs.

$\overline{SYNCA}$
$\overline{SYNCB}$: Synchronization. Input/output, active low. The $\overline{SYNC}$ pin is an output when Monosync, Bisync, or SDLC mode is programmed. It is asserted when a sync/flag character is detected by the receiver. The $\overline{SYNC}$ pin is a general purpose input in the Asynchronous mode and an input to the receiver in the External Sync mode.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the TS 68564 - 3, 4 and 5 MHz, in compliance either with MIL-STD-883 class B or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535, appendix A : general specifications for microcircuits.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1 and 2.2 (§ A).

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 (when defined) :

- 48 LEAD DIP
- SQ LCC 52 PINS
- 52 TERMINAL JCC.

The precise case outlines are described on chapter 9 at the end of the specification.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 2 · Absolute maximum ratings

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in § A.4 of this specification.

Symbol	Characteristics	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	7.0	V
V_I	Input voltages		−0.3	7.0	V
P_d	Power dissipation	T_{case} = −55°C		1.5	W
		T_{case} = +125°C		1.25	W
T_c	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{lead}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 · Guaranteed characteristics · recommended conditions of use

3.3.2.1 · Guaranteed characteristics

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified in § 3.3.2.2. below.

3.3.2.2 · Recommended conditions of use

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also § 3.3.2.1. above).

These conditions shall not be for inspection purposes.

Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

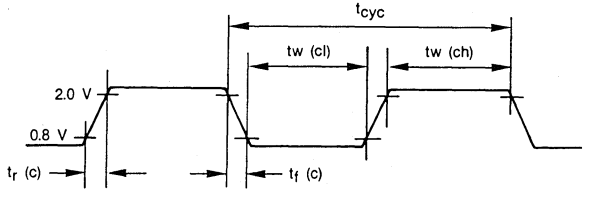


Figure 3 : Clock input timing diagram.

Table 3 - Recommended conditions of use
Unless otherwise stated, all voltages are referenced to the reference terminal (see § A.4).

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	All	4.75	5.25	V
V_{IL}	Low level input voltage	All	0	0.8	V
V_{IH}	High level input voltage	All	2.0	V_{CC}	V
T_{case}	Operating temperature	All	− 55	+ 125	°C
R_L	Value of output load resistance	All	Note		Ω
C_L	Output loading capacitance	All		Note	pF
$t_{r(c)}$	Clock rise time (see Figure 3)	All		30	ns
$t_{f(c)}$	Clock fall time (see Figure 3)	All		30	ns
f_c	Clock frequency (see Figure 3)	68564-3	1	3	MHz
		68564-4	1	4	MHz
		68564-5	1	5	MHz
t_{cyc}	Cycle time (see Figure 3)	68564-3	330	1000	ns
		68564-4	250	1000	ns
		68564-5	200	1000	ns
t_W (cL)	Clock pulse width low (see Figure 3)	68564-3	145		ns
		68564-4	105		ns
		68564-5	80		ns
t_W (cH)	Clock pulse width high (see Figure 3)	68564-3	145		ns
		68564-4	105		ns
		68564-5	80		ns
Note : Figures 4 and 5 gives the maximum loading of the relevant output.					

3.4 - Thermal characteristics

Table 4

Package	Symbol	Parameter	Value	Unit
DIL 48	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	40	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	11	°C/W
LCCC 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	45	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	15	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

5

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 5 : Static electrical characteristics for the electrical variants.
- Table 6 : Dynamic electrical characteristics for TS 68564-3 (3 MHz), TS 68564-4 (4 MHz) and TS 68564-5 (5 MHz).

For static characteristics (Table 5), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause 5.4 of this specification (Table 6).

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.2.2 here above.

5.2 · Static characteristics

Table 5 · Static characteristics for all covered models

$-55°C \leqslant T_C \leqslant +125°C$

Test Nbr	Symbol	Characteristic	IEC 748-2 method	Test Conditions	Test Temp.	Limits		Unit
						Min	Max	
1	I_{CC}	Supply current outputs opens	41	V_{CC} = 5.25 V	all		200	mA
2	V_{OL} (1)	Low level output voltage $\overline{IRQ}$, $\overline{DTACK}$, D0-D7	37	I_{OL} = 5.3 mA V_{CC} = 4.75 V	all		0.6	V
3	V_{OL} (2)	Low level output voltage (all others outputs except XTAL2)*	37	I_{OL} = 2.4 mA V_{CC} = 4.75 V	all		0.5	V
4	V_{OH} (1)	High level output voltage $\overline{DTACK}$, D0-D7	37	I_{OH} = −400 µA V_{CC} = 4.75 V	all	2.4		V
5	V_{OH} (2)	High level output voltage $\overline{DTACK}$, D0-D7	37	I_{OH} = −400 µA V_{CC} = 4.75 V	all	2.4		V
6	I_{IN}	Input leakage current (0 to 5.25 V)			all	−20	+20	µA
7	I_{TSI} (1)	Three-state (off state) input current $\overline{DTACK}$, D0-D7, $\overline{SYNC}$, $\overline{TxC}$, $\overline{RxC}$		0 inf V_{CC} inf V_{IN}	all	−10	+10	µA
8	I_{TSI} (2)	Three-state (off state) input current $\overline{IRQ}$		0 inf V_{CC} inf V_{IN}	all		+20	µA
9	V_{IH}	High level input voltage (all inputs)			all	2.0	V_{CC} +0.3	V
10	V_{IL}	Low level input voltage (all inputs)			all	−0.3	0.8	V
97	C_{IN}	Input capacitance (all inputs)	11	Reverse	25°C		25	pF
				voltage = 0 V	min		NA	pF
				F = 1.0 MHz	max		NA	pF
98	C_{OUT}	Output capacitance (all inputs)	11	Reverse	25°C		25	pF
				voltage = 0 V	min		NA	pF
				F = 1.0 MHz	max		NA	pF
99	V_{ESD}	Internal protection Transient energy rating	See Note 12	See Note 12 5 cycles	25°C	−500	+500	V
					min	NA	NA	V
					max	NA	NA	V

* XTAL = SPECIAL, $\overline{IRQ}$ = (OPEN DRAIN).

Refered note is given after Table 6.

5.3 · Dynamic (switching) characteristics

Table 6 · Dynamic (switching) characteristics TS 68564-3, 4 and 5 MHz

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Method (*)	Test Conditions	Test Temp.	3 MHz Limits		4 MHz Limits		5 MHz Limits		Unit
						Min	Max	Min	Max	Min	Max	
11	t_{su} (T_{SLCH})	$\overline{CS}$ low to CLK high (Note 1)	Fig. 6-7 Ref. 6	See 5.4.3 (a) to (c) f_C = 3, 4, 5 MHz	all	0		0		0		ns
12	t_{su} (T_{AVSL})	A1-A5 valid to $\overline{CS}$ low	Fig. 6-7 Ref. 7	See test 11	all	0		0		0		ns
13	t_{wcy} (T_{DVSL})	Data valid to $\overline{CS}$ low	Fig. 7 Ref. 8	See test 11	all	0		0		0		ns
18	t_{phl} (T_{CHDKL})	CLK high to $\overline{DTACK}$ low	Fig. 8-9 Ref. 13	See test 11 Load : 3	all		325		320		295	ns
20	t_{su} (T_{RVSL})	R/$\overline{W}$ valid to $\overline{CS}$ low	Fig. 6-7 Ref. 14	See test 11	all	0		0		0		ns
22	t_{plh} t_{phl} (T_{CLDO})	CLK low to data out	Fig. 6 Ref. 16	See test 11 Load : 3	all		550		450		450	ns
23	t_h (T_{SHDOI})	CS high to data out valid (Note 11)	Fig. 6 Ref. 17	See test 11 Load : 3	all	0		0		0		ns
28	t_{plh} (T_{IKLCH})	$\overline{IACK}$ low to CLK high (Note 1)	Fig. 8-9 Ref. 22	See test 11	all	0		0		0		ns
29	t_{phl} (T_{CLID})	CLK low to $\overline{IRQ}$ disabled (Note 2)	Fig. 8 Ref. 23	See test 11 Load : 1	all		410		410		410	ns
30	t_{phl} t_{plh} (T_{CLDO})	CLK low to data out (Note 2)	Fig. 8 Ref. 24	See test 11 Load : 3	all		330		330		330	ns
34	t_h (T_{IKHDV})	$\overline{IACK}$ high to data out valid	Fig. 8-9 Ref. 28	See test 11 Load : 3	all	0		0		0		ns
37	t_{phl} (T_{ILIOL})	$\overline{IEI}$ low to $\overline{IEO}$ low (Note 3)	Fig. 9 Ref. 31	See test 11 Load : 2	all		140		140		140	ns
38	t_{plh} (T_{IHIOH})	$\overline{IEI}$ high to $\overline{IEO}$ high (Note 4)	Fig. 9 Ref. 32	See test 11 Load : 2	all		190		190		190	ns
40	t_{phl} (T_{EKHIRL})	$\overline{IACK}$ high to $\overline{IRQ}$ low (Note 5)	Fig. 8 Ref. 34	See test 11 Load : 1	all		200		200		200	ns
41	t_{phl} (T_{ILCL})	$\overline{IEO}$ low to CLK low	Fig. 8-9 Ref. 35	See test 11	all	10		10		10		ns
42	t_{phl} (T_{LIRD})	$\overline{IEI}$ low to $\overline{IRQ}$ disabled (Note 6)	Fig. 9 Ref. 36	See test 11 Load : 1	all		500		500		500	ns
43	t_{plh} t_{phl} (T_{ILDOV})	$\overline{IEI}$ low to data out valid (Note 6)	Fig. 9 Ref. 37	See test 11 Load : 3	all		225		425		425	ns
48	t_{phl} (T_{SIKHCL})	$\overline{CS}$ or $\overline{IACK}$ high to CLK low (Note 7)	Fig. 7-8 9 Ref. 41	See test 11	all	100		100		100		ns
50	t_{phl} (T_{CHXL})	CLK high to TSRDY or RxRDY low	Fig. 10 Ref. 43	See test 11 Load : 2	all		300		300		300	ns
51	t_{plh} (T_{CHXH})	CLK high to $\overline{TxRDY}$ or $\overline{RxRDY}$ high	Fig. 10 Ref. 44	See test 11 Load : 2	all		335		300		300	ns
53	t_w (T_{CDSWH})	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width high	Fig. 11 Ref. 45	See test 11	all	200		200		200		ns
54	t_w (T_{CDSWL})	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width low	Fig. 11 Ref. 46	See test 11	all	200		200		200		ns
55	t_{cy} (T_{TXP})	$\overline{TxC}$ period (Note 9)	Fig. 11 Ref. 47	See test 11	all	1320	DC	1000	DC	800	DC	ns
56	t_w (T_{TXWL})	$\overline{TxC}$ width high	Fig. 11 Ref. 48	See test 11	all	180	DC	180	DC	180	DC	ns
57	t_w (T_{TXWH})	$\overline{TxC}$ width high	Fig. 11 Ref. 49	See test 11	all	180	DC	180	DC	180	DC	ns
58	t_{phl} (T_{TXLXDD})	$\overline{TxC}$ low to TxD delay (x1 mode)	Fig. 11 Ref. 50	See test 11 Load : 2	all		300		300		300	ns

* Measurement method : see § 5.1.

Refered notes are given after Table 6.

Table 6 - Dynamic (switching) characteristics TS 68564-3, 4 and 5 MHz (Continued)
$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Method (*)	Test Conditions	Test Temp.	3 MHz Limits		4 MHz Limits		5 MHz Limits		Unit
						Min	Max	Min	Max	Min	Max	
60	t_p (T_{RXP})	$\overline{RxC}$ period (Note 9)	Fig. 11 Ref. 52	See test 11	all	1320	DC	1000	DC	800	DC	ns
61	t_w (T_{RXWL})	$\overline{RxC}$ width low	Fig. 11 Ref. 53	See test 11	all	180	DC	180	DC	180	DC	ns
62	t_w (T_{RXWH})	$\overline{RxC}$ width high	Fig. 11 Ref. 54	See test 11	all	180	DC	180	DC	180	DC	ns
63	t_{su} (T_{XHSU})	RxD to $\overline{RxC}$ high setup time (x1 mode)	Fig. 11 Ref. 55	See test 11	all	0		0		0		
64	t_h (T_{XHHO})	$\overline{RxC}$ to RxD high hold time (x1 mode)	Fig. 11 Ref. 56	See test 11	all	140		140		140		ns
66	t_{phl} (T_{RXHSYL})	$\overline{RxC}$ high to $\overline{SYNC}$ low delay (outputs mode) (Note 10)	Fig. 11 Ref. 58	See test 11 Load : 2	all	4	7	4	7	4	7	CLK period
67	t_p (T_{RL})	$\overline{RESET}$ low (Note 10)	Fig. 10 Ref. 59	See test 11	all	1		1		1		CLK period
68	t_w (T_{TAWH})	XTAL1 width high (TTL in)	Fig. 10 Ref. 60	See test 11	all	145		100		80		ns
69	t_w (T_{TAWH})	XTAL1 width low (TTL in)	Fig. 10 Ref. 61	See test 11	all	145		100		80		ns
70	t_p (T_{XTP})	XTAL1 period (TTL in)	Fig. 10 Ref. 62	See test 11	all	330	2000	250	2000	200	2000	ns

* Measurement method : see § 5.1.

Refered notes are given after Table 6.

REFERRED NOTES TO THE TABLES 5 AND 6

The following notes shall apply where referred into the tables 5 and 6 and/or additional information given in table 7 of this specification.

Note 1 : This specification only applies if the SIO has completed all operations initiated by the previous bus cycle, when CE or $\overline{IACK}$ was asserted. Following a read, write, or interrupt acknowledge cycle, all operations are complete within two CLK cycles after the rising edge of $\overline{CS}$ or $\overline{IACK}$. If $\overline{CS}$ or $\overline{IACK}$ is asserted prior to the completion of the internal operations, the new bus cycle will be postponed.

Note 2 : If $\overline{IEI}$ meets the setup tome to the falling edge of CLK, 1 1/2 cycles following the clocking in of $\overline{IACK}$.

Note 3 : No internal interrupt request pending at the stard of an interrupt acknowledge cycle.

Note 4 : Time starts when first signal goes invalid (high).

Note 5 : If an internal interrupt is pending at the end of the interrupt acknowledge cycle.

Note 6 : If Note 2 timing is not met.

Note 7 : If this spec is met, the delay listed in Note 1 will be one CLK cycle instead of two.

Note 8 : Ready signals will be negated asynchronous to the CLK, if the condition causing the assertion of the signals is cleared.

Note 9 : If $\overline{RxC}$ and $\overline{TxC}$ are asynchronous to the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ should be no more than one-fifth the System Clock rate. If $\overline{RxC}$ and $\overline{TxC}$ are synchronized to the falling edge of the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ can be one-fouth the System Clock rate.

Note 10 : SIO Clock (CLK) Cycles as defined in Parameter 1.

Note 11 : Due to the dynamic nature of the internal data bus, if $\overline{CS}$ is held low for more than a few hundred milliseconds the read data may go to 00H before the end of the cycle.

Note 12 : Transient energy rating - The test shall be performed as specified in Generic Specification and its associated documents. The test voltages are as given in Table 5 for test 99.
Each terminal of the device under test shall be tested separately against all existing V_{CC} and V_{SS} terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in Table 5 for test 99.

5.4 · Test conditions specific to the device

5.4.1 · Loading network

The applicable loading network shall be as defined in column «Test conditions» of Tables 5 and 6, refering to the loading network number as shown in Figures 4 and 5 below.

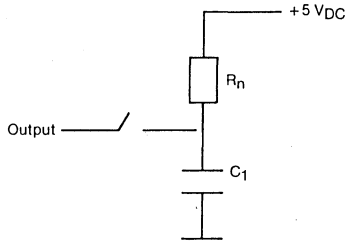


Figure 4 : Passive loads.

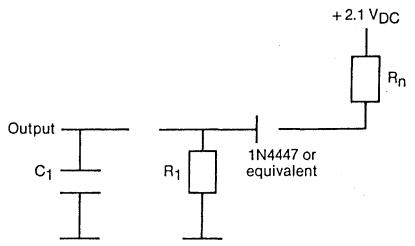


Figure 5 : Active loads.

Load NBR	Figure	R_1 (Ω)	R_n (Ω)	C_1 (pF)	Output application
1	4		740	130	IRQ
2	5	16 k	450	130	All outputs except IRQ, D0-D7, XTAL2, DTACK
3	5	6 k	200	130	DTACK, D0-D7
Note : Equivalent loading may be simulated by the tests.					

5

5.4.2 · Time definitions

The times specified in Tables 5 and 6 as dynamic characteristics are defined in Figures 6 to 13 below by a reference number given in the column «Method» of the tables together with the relevant figure number.

Note : Waveform measurements for all inputs and outputs are specified at logic high = 2.0 V, logic low = 0.8 V.

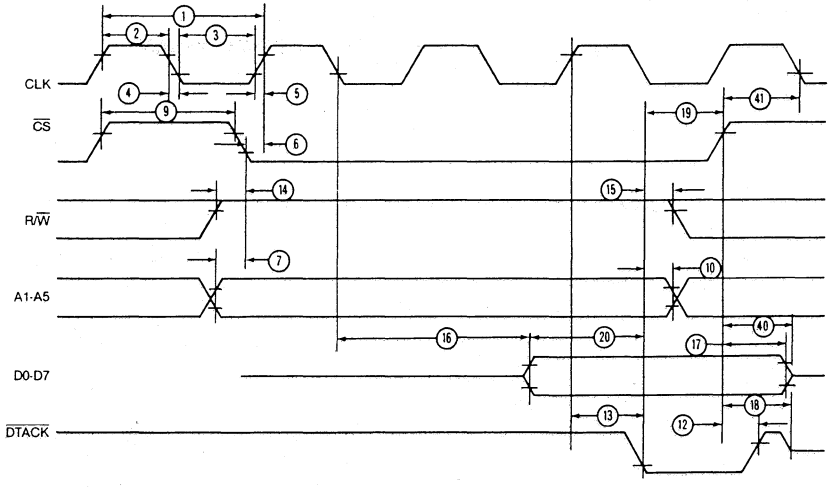


Figure 6 : Read cycle.

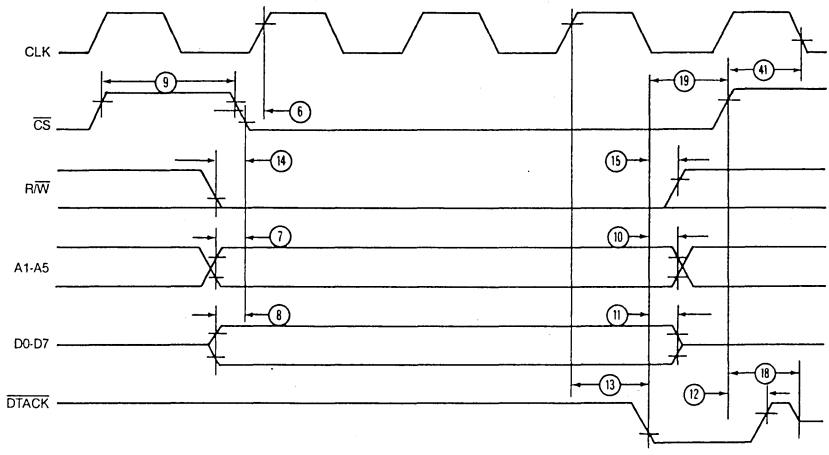


Figure 7 : Write cycle.

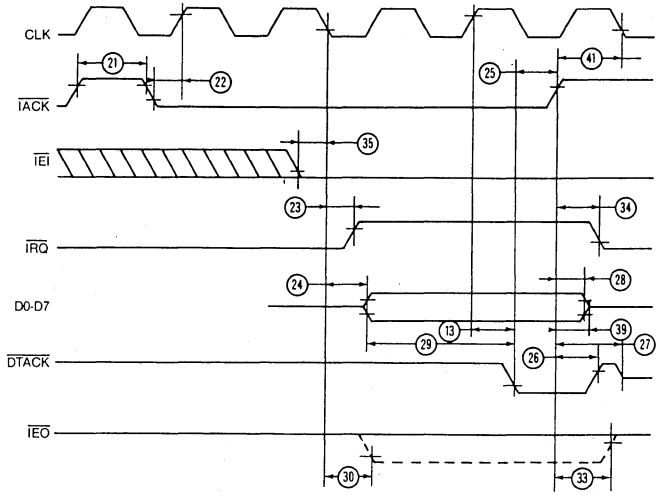


Figure 8 : Interrupt acknowledge cycle ($\overline{IEI}$ low).

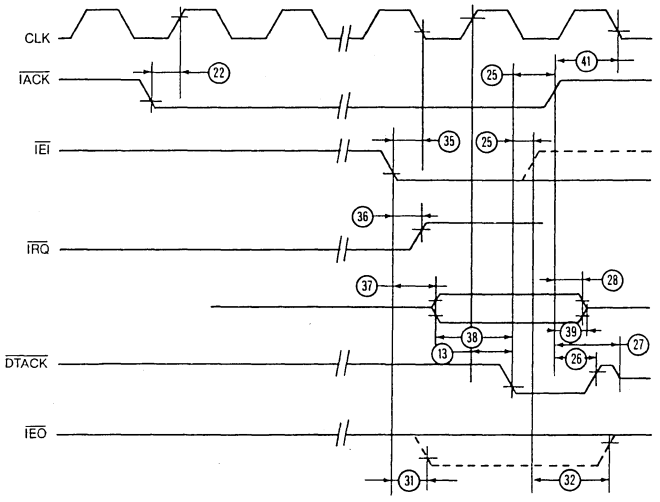


Figure 9 : Interrupt acknowledge cycle ($\overline{IEI}$ high).

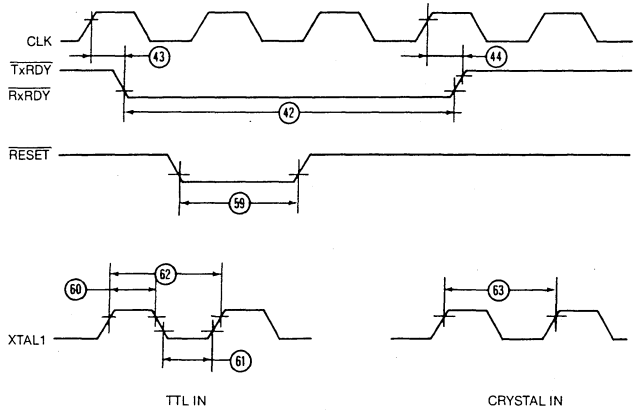


Figure 10 : DMA interface timing.

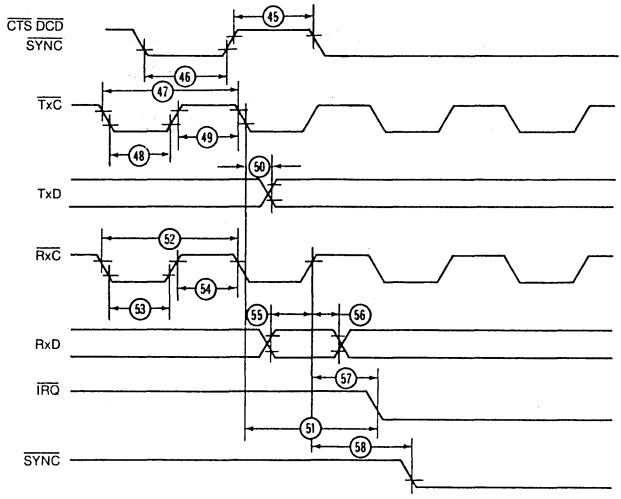


Figure 11 : Serial interface timing.

5.4.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics
Where input pulse generator is loaded by 90 ohms resistor, the input pulse characteristics shall be as shown in Figure 12.

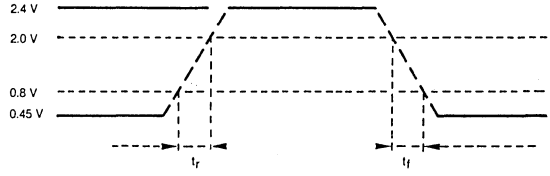


Figure 12 : Input pulse characteristics.

b) Time measurement input voltage references
Input voltages which are taken as reference for time measurement shall be :

V_{IL} = 0.8 V

V_{IH} = 2.0 V

c) Time measurement output voltage reference for time valid state output
Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in Figure 13.

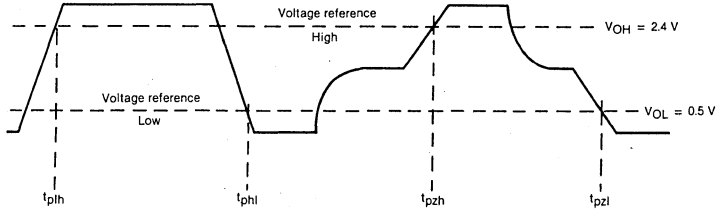


Figure 13 : Output voltage references.

5.5 · Additional information

Additional information shall not be for any inspection purposes.

5.5.1 · Power consideration

See § 3.4.

5.5.2 · Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 6 to 13 and loading number refer to Figures 4 and 5 (see § 5.4.1 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2.2 of this specification.

Table 7 · Additional electrical characteristics TS 68564-3, 4 and 5 MHz

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Method	Test Conditions	Test Temp.	3 MHz Limits Min (*)	3 MHz Limits Max (*)	4 MHz Limits Min (*)	4 MHz Limits Max (*)	5 MHz Limits Min (*)	5 MHz Limits Max (*)	Unit
14	t_{su} (T_{SVCL})	$\overline{CS}$ width high (Note 1)	Fig. 6 - 7 Ref. 9	See test 11	all	50		50		50		ns
15	t_h (T_{DLAI})	$\overline{DTACK}$ low to A1-A5 invalid	Fig. 6 - 7 Ref. 10	See test 11	all	0		0		0		ns
16	t_{wcyh} (T_{DLDI})	$\overline{DTACK}$ low to data invalid	Fig. 7 Ref. 11	See test 11 Load : 3	all	0		0		0		ns
17	t_{plh} (T_{SHDKH})	$\overline{CS}$ high to $\overline{DTACK}$ high	Fig. 6 - 7 Ref. 12	See test 11 Load : 3	all		60		55		50	ns
21	t_h (T_{DKLRI})	$\overline{DTACK}$ low to R/$\overline{W}$ invalid	Fig. 6 - 7 Ref. 15	See test 11	all	0		0		0		ns
24	t_{phz} (T_{SHDKZ})	$\overline{CS}$ high to $\overline{DTACK}$ Hi-Z	Fig. 6 - 7 Ref. 18	See test 11 Load : 3	all		110		105		100	ns
25	t_{plh} (T_{DKLSH})	$\overline{DTACK}$ low to $\overline{CS}$ high	Fig. 6 - 7 Ref. 19	See test 11	all	0		0		0		ns
26	t_{phl} (T_{DVDKL})	Data valid to $\overline{DTACK}$ low	Fig. 6 Ref. 20	See test 11 Load : 3	all	70		70		70		ns
27	t_{plh} (T_{IKWH})	$\overline{IACK}$ width high (Note 1)	Fig. 8 Ref. 21	See test 11	all	50		50		50		ns
31	t_{plh} (T_{DKLIH})	$\overline{DTACK}$ low to $\overline{IACK}$, IEI high	Fig. 8 - 9 Ref. 25	See test 11	all	0		0		0		ns
32	t_{plh} (T_{IHDKH})	$\overline{IACK}$ high to $\overline{DTACK}$ high	Fig. 8 - 9 Ref. 26	See test 11 Load : 3	all		60		55		50	ns
33	t_{plz} (T_{IHDRKZ})	$\overline{IACK}$ high to $\overline{DTACK}$ Hi-Z	Fig. 8 - 9 Ref. 27	See test 11 Load : 3	all		110		105		100	ns
35	t_{phl} (T_{DVDKL})	Data valid to $\overline{DTACK}$ low (Note 2)	Fig. 8 Ref. 29	See test 11 Load : 3	all	195		195		195		ns
36	t_{phl} (T_{CLIL})	CLK low to $\overline{IEO}$ low (Note 3)	Fig. 8 Ref. 30	See test 11	all		220		220		220	ns
39	t_{plh} (T_{IKHIOH})	$\overline{IACK}$ high to $\overline{IEO}$ high (Note 4)	Fig. 8 Ref. 33	See test 11 Load : 2	all		190		190		190	ns
44	t_{phl} (T_{DVDKL})	Data out valid to $\overline{DTACK}$ low (Note 6)	Fig. 9 Ref. 38	See test 11 Load : 3	all	55		55		55		ns
46	t_{plh} t_{phl} (T_{IKHDZ})	$\overline{IACK}$ high to data out Hi-Z	Fig. 8 - 9 Ref. 39	See test 11 Load : 3	all		150		120		90	ns
47	t_{phl} (T_{SHDOV})	$\overline{CS}$ high to data out Hi-Z	Fig. 6 Ref. 40	See test 11 Load : 3	all		150		120		90	ns
49	t_w (T_{XWL})	$\overline{TxRDY}$ or $\overline{RxRDY}$ width low	Fig. 10 Ref. 42	See test 11	all		3		3		3	CLK period
52	t_{phl}	$\overline{IACK}$ high to $\overline{CS}$ high to $\overline{IACK}$ low (Note 1)	not shown			50		50		50		
59	t_{phl} (T_{XLIRL})	TxC low to $\overline{IRQ}$ low delay (Note 10)	Fig. 11 Ref. 51	See test 11 Load : 1	all	5	9	5	9	5	9	CLK period
65	t_{phl} (T_{RXHIRL})	RxC high to $\overline{IRQ}$ low delay (Note 10)	Fig. 11 Ref. 57	See test 11 Load : 1	all	10	13	10	13	10	13	CLK period
71	t_p (T_{XTPC})	XTAL1 period (crystal in)	Fig. 10 Ref. 63	See test 11	all	330	1000	250	1000	200	1000	ns

* Algebraic values.

Refered notes are given after Table 6.

6 · FUNCTIONAL DESCRIPTION

6.1 · System interface

The TS 68564 SIO is designed for simple and efficient interface to a 68000 CPU system. All data transfers between the SIO and the CPU are asynchronous to the system clock. The SIO system timing is derived from the chip select input ($\overline{CS}$) during normal read and write sequences, and from the interrupt acknowledge input ($\overline{IACK}$) during an exception processing sequence. $\overline{CS}$ is a function address decode and (normally) lower data strobe (LDS). $\overline{IACK}$ is a function of the interrupt level on address lines A1, A2, and A3, an interrupt acknowledge function code (FC0-FC2), and LDS.

Note : CS and $\overline{IACK}$ can never be asserted at the same time.

Note : Unused inputs shoud be pulled up or down, but never left floating.

6.1.1 · Read Sequence

The SIO will begin a read cycle if, on the falling edge of $\overline{CS}$, the R/$\overline{W}$ pin is high. The SIO will respond by decoding the address bus (A1-A5) for the register selected, by placing the contents of that register on the data bus pins (D0-D7), and by driving the data transfer acknowledge ($\overline{DTACK}$) pin low. If the register selected is not implemented on the SIO, the data bus pins will be driven high, an then $\overline{DTACK}$ will be asserted.

When the CPU has acquired the data, the $\overline{CS}$ signal is driven high, at which time the SIO will drive $\overline{DTACK}$ high and then three-state $\overline{DTACK}$ and D0-D7.

6.1.2 · Write sequence

The SIO will begin a write cycle if, on the falling edge of $\overline{CS}$, the R/$\overline{W}$ pin is low. The SIO will respond by latching the data bus, by decoding the address bus for the register selected, by loading the register with the contents of the data bus, and by driving $\overline{DTACK}$ low. When the CPU has finished the cycle, the $\overline{CS}$ input is driven high. At this time, the SIO will drive $\overline{DTACK}$ high and will then three-state $\overline{STACK}$. If the register selected is not implemented on the SIO, the normal write sequence will proceed, but the data bus contents will not be stored.

6.1.3 · Interrupt sequence

The SIO is designed to operate as an independent, interrupting peripheral, or, when interconnected with other components, an interrupt priority daisy chain can be formed.

6.1.3.1 · Independent operation

Independent operation requires that the interrupt enable in pin (IEI) be connected to ground. The SIO starts the interrupt sequence by driving the interrupt request pin ($\overline{IRQ}$) low. The CPU responds to the interrupt by starting an interrupt acknowledge cycle, in which the SIO $\overline{IACK}$ pin is driven low. The highest priority interrupt request in the SIO, at the time $\overline{IACK}$ goes low, places its vector on the data bus pins. The SIO releases the $\overline{IRQ}$ pin and drives $\overline{DTACK}$ low. When the CPU has acquired the vector, the $\overline{IACK}$ signal is driven high. The SIO responds by driving $\overline{DTACK}$ to a high level and then three-stating DTACK and D0-D7. If more than one interrupt resquest is pending at the start of an interrupt acknowledge sequence, the SIO will drive the $\overline{IRQ}$ pin low following the completion of the interrupt acknowledge cycle. This sequence will continue untill all pending interrupts are cleared. If the SIO is not requesting a interrupt when $\overline{IACK}$ goes low, the SIO will not respond to the $\overline{IACK}$ signal ; $\overline{DTACK}$ and the data bus will remain three-stated.

6.1.3.2 · Daisy chain operation

The interrupt priority chain is formed by connecting the interrupt enable out pin ($\overline{IEO}$) of a higher priority part to $\overline{IEI}$ of the next lower priority part. The highest prioprity part in the chain should have $\overline{IEI}$ tied to ground. The Daisy chaining capability (Figures 14 and 15) requires that all parts in a chain have a common $\overline{IACK}$ signal. When the common $\overline{IACK}$ goes low, all parts freeze and prioritize interrupts in parallel. Then priority is passed down the chain, via $\overline{IEI}$ and $\overline{IEO}$, until a part which has a pending interrupt, once $\overline{IEI}$ goes low, passes a vector, does not propagate $\overline{IEO}$, and generates $\overline{DTACK}$.

The state of the $\overline{IEI}$ does not affect the SIO can generate an interrupt request any time its interrupts are enabled. The $\overline{IEO}$ pin is normally high ; it will only go low during an $\overline{IACK}$ cycle if $\overline{IEI}$ is low and no interrupt is pending in the SIO. The $\overline{IEO}$ pin will be forced high whenever $\overline{IACK}$ or $\overline{IEI}$ goes high.

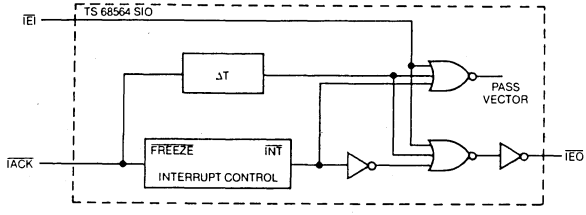


Figure 14 : A conceptual circuit of the TS 68564 SIO chaining logic.

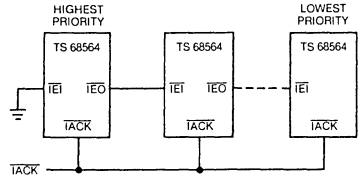


Figure 15 : Daisy chaining.

6.1.4 · DMA interface

The SIO is designed to interface to the TS 68000 family DMA's as a 68000 compatible device, using the cycle steal mode. The SIO provides four outputs (TxRDYA, RxRDYA, TxRDYB, RxRDYB) for requesting service from the DMA. The SIO issues a request for service by pulsing the RDY pin low for three clock (CLK) cycles (see Figure 16) TxRDY (when enabled) will be active when the transmit buffer. If Receive interrupt On First Character Only is enabled during a DMA operation and a special receive condition is detected, the RxRDY pin will not become active. Instead, a special receive condition interrupt will be generated by the channel.

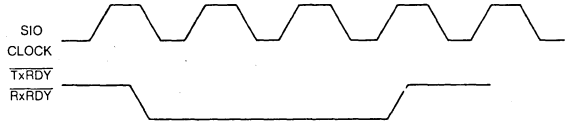


Figure 16 : DMA interface timing.

6.1.5 · Reset

There are two ways of resetting the SIO : an individual programmable channel reset and an external hardware reset.

The individual channel reset is generated by writting «18H» to the Command Register for the channel selected. All outputs associated with the channel are reset high, TxC and RxC are inputs, SYNC is an output, and TxD is forced marking, all R/W registers for the channel are reset to «00H», except the vector register and the data register, which are not affected.

Read only status register 1 is reset to «01H» (All Sent set). Break/Abort, Interrupt Pending, and Rx Character available bits in read only status register 0 are reset ; Underrun/EOM, Hunt/Sync, and Tx Buffer Empty are set ; CTS and DCD bits are set to the inverted state of their respective input pins. Any interrupts pending for the channel are reset (any pending interrupts in the other channel will not be affected).

An external hardware reset occurs when the RESET pin is driven low for at least on clock (CLK) cycle. Both channels are reset as listed above, and the vector register is reset tot «OFH».

6.2 · Architecture

The TS 68564 SIO contains two independent, fullduplex channels. Each channel contains a transmitter, receiver, modem control logic, interrupt control logic, a baud rate generator, ten Read/Write registers, and two read only status registers. Each channel can communicated with the bus master using polling, interrupts, DMA, or any combination of these three techniques. Each channel also has the ability to connect the transmitter output into the receiver without disturbing any external hardware.

6.2.1 · Register set

The register set is the heart of each channel. A channel is configured for different communication protocols and interface options by programming the registers. Table 8 lists all the registers available in the SIO and their adresses. Figure 17 shows the register models.

INTERNAL REGISTERS

The TS 68564 SIO has 25 internal registers. Each channel has ten R/$\overline{W}$ registers and two read only registers associated with it. The vector register may be accessed through either channel.

Table 8 · Register Map

Address					Abbreviation	Channel	Register name	Access	
5	4	3	2	1				Read/ write	Read only
0	0	0	0	0	CMDREG	A	Command Register	x	
0	0	0	0	1	MODECTL	A	Mode Control Register	x	
0	0	0	1	0	INTCTL	A	Interrupt Control Register	x	
0	0	0	1	1	SYNC 1	A	Sync Word Register 1	x	
0	0	1	0	0	SYNC 2	A	Sync Word Register 2	x	
0	0	1	0	1	RCVCTL	A	Receiver Control Register	x	
0	0	1	1	0	XMTCTL	A	Transmitter Control Register	x	
0	0	1	1	1	STAT 0	A	Status Register 0		x
0	1	0	0	0	STAT 1	A	Status Register 1		x
0	1	0	0	1	DATARG	A	Data Register	x	
0	1	0	1	0	TCREG	A	Time Constant Register	x	
0	1	0	1	1	BRGCTL	A	Baud Rate Generator Control Reg	x	
0	1	1	0	0	VECTRG	A/B	Interrupt Vector Register (Note 2)	x	
0	1	1	0	1		A	(Note 1)	x	
0	1	1	1	0		A	(Note 1)	x	
0	1	1	1	1		A	(Note 1)	x	
1	0	0	0	0	CMDREG	B	Command Register	x	
1	0	0	0	1	MODECTL	B	Mode Control Register	x	
1	0	0	1	0	INTCTL	B	Interrupt Control Register	x	
1	0	0	1	1	SYNC 1	B	Sync Word Register 1	x	
1	0	1	0	0	SYNC 2	B	Sync Word Register 2	x	
1	0	1	0	1	RCVCTL	B	Receiver Control Register	x	
1	0	1	1	0	XMTCTL	B	Transmitter Control Register	x	
1	0	1	1	1	STAT 0	B	Status Register 0		x
1	1	0	0	0	STAT 1	B	Status Register 1		x
1	1	0	0	1	DATARG	B	Data Register	x	
1	1	0	1	0	TCREG	B	Time Constant Register	x	
1	1	0	1	1	BRGCTL	B	Baud Rate Generator Control Reg	x	
1	1	1	0	0	VECTRG	A/B	Interrupt Vector Register (Note 2)	x	
1	1	1	0	1		B	(Note 1)	x	
1	1	1	1	0		B	(Note 1)	x	
1	1	1	1	1		B	(Note 1)	x	

Note 1 : Not used, read as «FFH».
Note 2 : Only one Vector Register, accessible through either channel.

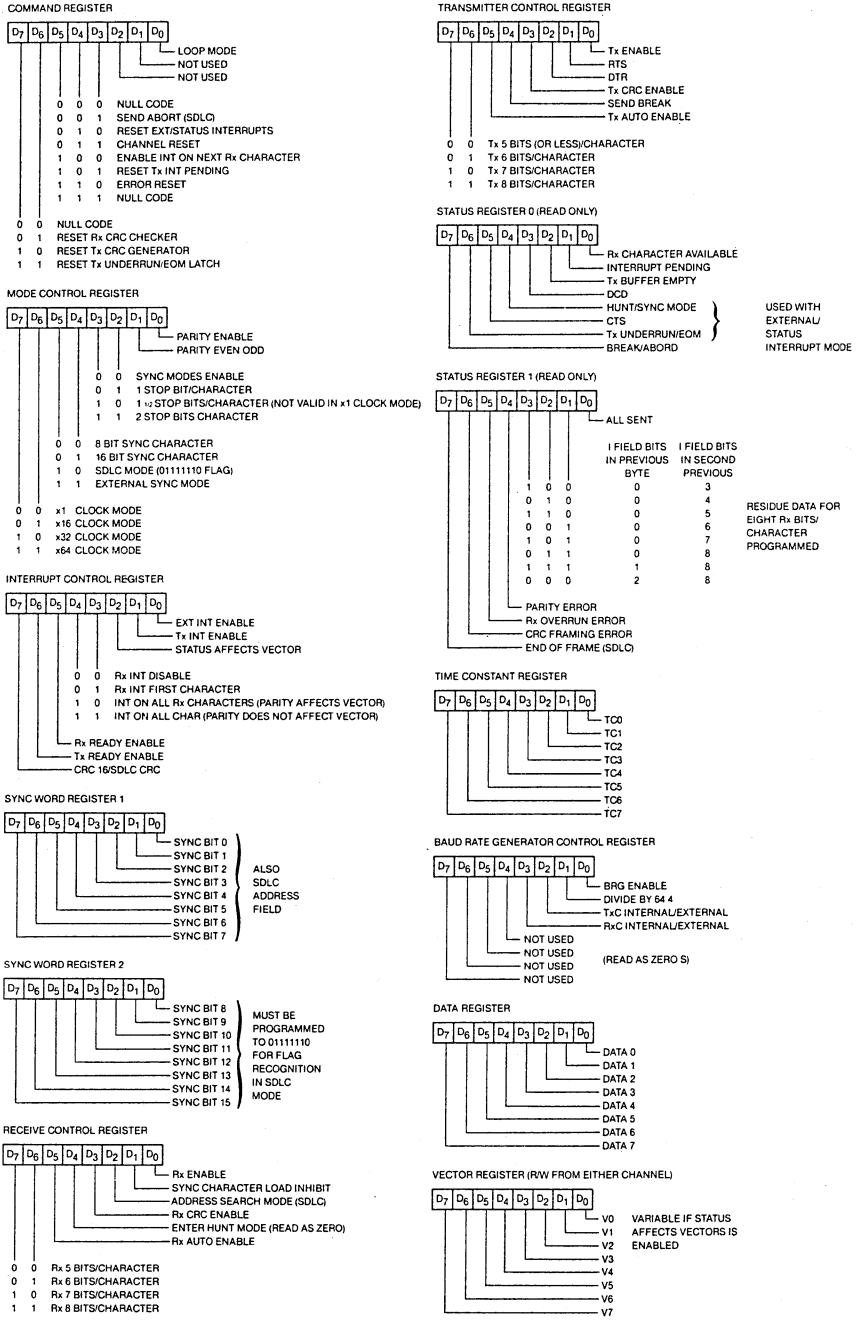


Figure 17 : Register bit function.

6.2.1.1 - Data register

The Data Register is composed of two separate registers : a write only register, which is the Transmit Buffer, and a read only register, which is the Receive Buffer. The Receive Buffer is also the top register of a three register stack called the receive data FIFO.

6.2.1.2 - Vector register

The Vector register is different from the other 24 registers, becausez it may be accessed through either Channel A or Channel B during a R/W cycle. During an Interrupt Acknowledge cycle, the contents of the Vector Register are passed to the CPU to be used as a pointer to an interrupt service routine. If the Status Affects Vector bit is low in the Interrupt Control register, any data written to the Vector Register will be returned unmodified during a Read cycle or an $\overline{IACK}$ cycle. If the Status Affects Vector bit is High, the lower three bits of the vector returned during a Read or $\overline{IACK}$ cycle are modified to reflect the highest priority interrupt pending in the SIO at that time. The upper five bits written to the Vector Register are unaffected. After a hardware reset only, this register contains a «OFH» value, which is the 68000's uninitialized interrupt vector assignment.

6.2.2 - Data path

The transmit and receive data paths for each channel are shown in Figure 18. The receiver has three 8-bit buffer registers in a FIFO arrangement (to provide a 3-byte delay) in addition to the 8-bit receive shift register. This arrangement creates additional time for the CPU to service an interrupt at the beginning of a block of high speed data. The receiver error FIFO stores parity and framing errors and other types of status information for each of the three bytes in the receive data FIFO. The receive error FIFO is loaded at the same time as the receive data FIFO. The contents of the receive error are read through the upper four bits in Status Register 1.

Incoming data is routed through on of several paths, depending on the mode and character length. In the Asynchronous modes, serial data is entered into the 3-bit buffer, if it has a character length of seven or eight bits, or the data is entered into the 8-bit receive shift register, if it has a length of five or six bits.

In the Synchronous mode, the data path is determined by the phase of the receive process currently in operation. A Synchronous Receive operation begins with the receive in the hunt phase, during which time the receiver searches the incoming data stream for a bit pattern that matches the pre-programmed sync characters (or flags in the SDLC mode). If the device is programmed for Monosync Hunt, a match is made with a single sync character stored in Sync Word Register 2. In Bisync Hunt, a match is made with the dual sync character stored in Syn Word Registers 1 and 2. In either case, the incoming data passes through the receive sync register and is compared against the programmed sync characters in Sync Registers 1 and 2.

In the Monosync mode, a match between the sync character programmed into Sync Word Register 2 and the character assembled in the receive sync register establishes synchronization.

In the Bisync mode, incoming data is shifted to the receive shift register, while the next eight bits of the message are assembled in the receive sync register. The match between the assembled character in the sync register and the programmed character in Sync Word Register 2, and between the character in the shift register and the programmed character in Sync Word Register 1 establishes synchronization. Once synchronization is established, incoming data bypasses the receive sync register and directly enters the 3-bit buffer.

In the SDLC mode, all incoming data passes through the receive sync register, which continuously monitors the receive data stream and performs zero deletion when indicated. Upon receiving five contiguous ones, the sixth bit is inspected. If the sixth bit is a 0, it is deleted from the data stream. If the sixth bit is a 1, an Abort sequence has been received.

The reformatted data from the receive sync register enters the 3-bit buffer and is transferred to the receive shift register. Note that the SDLC receive operation also begins in the Hunt Phase, during which time the SIO tries to match the assembled character in the receive sync register with the flag pattern in Sync Word Register 2. Once the first flag character is recognized, all subsequent data is routed through the path described above, regardless of character length.

Although the same CRC checker is used for both SDLC and synchronous data, the path taken for each mode is different In Bisync protocol, the byte-oriented operation requires that the CPU decide whether or not to include the data character in the CRC calculation. To allow the CPU ample time to make this decision, the SIO provides an 8-bit delay before the data enters the CRC checker. In the SDLC mode, no delay is provided, since CRC is calculated on all data between the opening and closing flags.

The transmitter has 8-bit transmit data register, which is loaded from the internal bus, and a 20-bit transmit shift register, which can be loaded from Sync Word register 1, Sync Word register 2, and the transmit data register. Sync Word register 1 and 2 contain sync characters in the Monosync, Bisync, or External Sync modes, or address field (one character long) and flag, respectively, in the SDLC mode.

During Synchronous modes, information contained in Sync Word registers 1 and 2 is loaded into the transmit shift register at the beginning of the message and, as a time filler, in the middle of the message if a transmit Underrun condition occurs. In SDLC mode, the flags are loaded into the transmit shift register at the beginning and end of the message.

Asynchronous data in the transmit shift register is formatted with start and stop bits, and it is shifted out to the transmit multiplexer at the selected clock rate.,

Synchronous (Monosync, Bisync, or External Sync) data is shifted out to the transmit multiplexer and also the CRC generator at the x1 clock rate.

SDLC/HDLC data is shifted out through the zero insertion logic, which is disabled while flags are being sent. For all other fields (address, control, and frame check), a 0 is inserted following five contiguous ones in the data stream. Note that the CRC generator result (frame check) for SDLC data is also routed through the zero insertion logic.

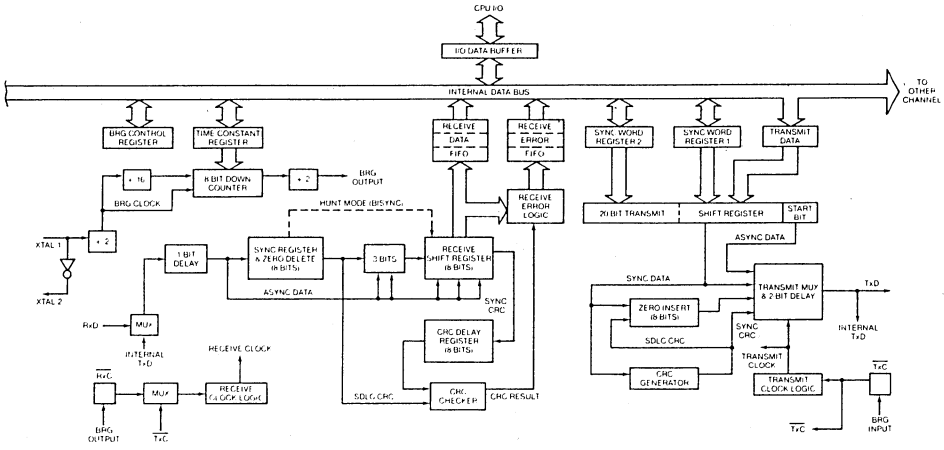


Figure 18 : Transmit and receive data paths.

6.3 · I/O capabilities

The SIO offers the choice of Polling. Interrupt (vectored or non-vectored), and DMA Transfer modes to transfer data, status, and control information to and from the CPU or other bus master.

5

6.3.1 · Polling

The Polled mode avoids interrupts. Status Registers 0 and 1 are updated at appropriate times for each function being performed (for example, CRC Error status valid at the end of the message). All the interrupt modes of the SIO must be disabled to operate the device in a polled environment.

While in its Polling sequence, the CPU examines the Status Register 0 for each channel. The state of the status bits in Status Register 0 serves as an acknowledge to the Poll inquiry. Status bits D0 and D2 indicate that a receive or transmit data transfer is needed. The rest of the Status bits in Status Register 0 indicate special status conditions. The receiver error condition bits in Status Register 1 do not have to be read until the Rx Character Available status bit in Status Register 0 is set to a one.

6.3.2 · Interrupts

The SIO offers an elaborate interrupt scheme to provide fast interrupt response in real-time applications. The interrupt vector points to an interrupt service routine in the memory. To service operations in both channels and to eliminate the necessity of writing a status analysis routine (as required for a polling scheme). The SIO can modify the interrupt vector so it points to one of eight interrupt service routines. This is done under program control by setting the Status Affects Vector bit in the Interrupt Control Register of channel A or channel B, to a one. When this bit is set, the interrupt vector is modified according to the assigned priority of the various interrupting conditions.

Note : If the Status Affects Vector bit is set in either channel, the vector is modified for both channel. This is the only control bit that operates in this manner in the SIO.

Transmit interrupts. Receive interrupts, and External/Status interrupts are the sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmitter, and External/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. This implies that the transmitted must have had a data character written into it to it can become empty. When enabled, the receiver can interrupt the CPU in one of three ways :

- Interrupt On First Character Only
- Interrupt On All Receive Characters
- Interrupt On a Special Receive Condition.

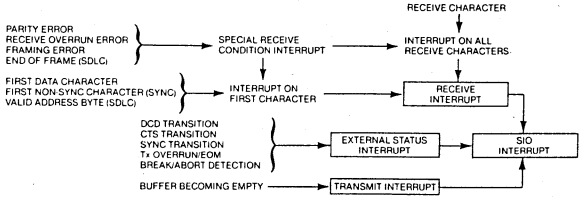


Figure 19 : Interrupt structure.

6.3.2.1 - Interrupt on first character only

This mode is normally used to start a software Polling loop or a DMA transfer routine using the $\overline{\text{RxRDY}}$ pin. In this mode, the SIO generates an interrupt on the first character received after this mode is selected and, thereafter, only generates an interrupt if a Special Receive Condition occurs. The Special Receive Conditions that can cause an interrupt in this mode are : Rx Overrun Error, Framing Error (in Asynchronous modes), and End of Frame (in SDLC mode). This mode is reinitialized by the Enable Interrupt On next Rx Character command. If a Special Receive Condition interrupt occurs in this interrupt mode, the data with the special condition is held in the receive data FIFO until an Error Reset Command is issued.

6.3.2.2 - Interrupt on all receive characters

In this mode, an interrupt is generated whenever the receive data FIFO contains a character or a Special Receive Condition occurs. The special Receive Conditions that can cause an interrupt in this mode are : Rx Overrun Error, Framing Error (in Asynchronous modes), End of Frame (in SDLC mode), and Parity Error (if selected).

6.3.2.3 - Interrupt on a special receive condition

The Special Receive Condition interrupt is not, as such, a separate interrupt mode. Before a Special Receive Condition can cause an interrupt, either the Interrupt On First Character Only or Interrupt On All Receive Characters mode must be selected. The Special Receive condition interrupt will modify the receive interrupt vector if Status Affects Vector is enabled. The Special Receive Condition Status is displayed in the upper four bits a Status Register 1. Two of the conditions causing a special receive interrupt are latched when they occur ; they are : Parity Error an Rx Overrun Error. These status bits may only be reset by an Error Reset command. When either of these conditions occur, a read of Status Register 1 will reflect any errors in the current word in the receive buffer plus any parity or overrun errors since the last Error Reset command was issued.

6.3.2.4 - External/status interrupts

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, and $\overline{\text{SYNC}}$ pins however, an External/Status interrupt is also caused by a Transmit Underrun condition or by the detection of a Break (Asynchronous mode) or Abort (SDLC mode) sequence in the received data stream. When any one of the above conditions occur, the external/status logic latches the current state of all five input conditions, and generates an interrupt. To reinitialize the external/status logic to detect another transition, a Reset External/Status Interrupts command must be issued. The Break/Abort condition allows the SIO to generate an interrupt when the Break/Abort sequence is detected and terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break/Abort condition in external logic.

6.3.3 - DMA transfer

The SIO provides two output signals per channel for connection to a DMA controller ; they are $\overline{\text{TxRDY}}$ and $\overline{\text{RxRDY}}$. The outputs are enabled under software control by writing to the Interrupt Control Register. Both outputs will pulse Low for three system clock cycles when their input conditions are active. $\overline{\text{TxRDY}}$ will be active when the Transmit Buffer becomes empty. $\overline{\text{RxRDY}}$ will be active when a character is available in the Receive Buffer. If a Special Receive Condition occurs when interrupt On First Character Only mode is selected, a receiver interrupt will be generated and $\overline{\text{RxRDY}}$ will not become active. This will automatically inform the CPU of a discrepancy in the data transfer.

6.3.4 - Self test

When the Loop Mode bit is set in the Command Register, the receiver shift clock input pin ($\overline{\text{RxC}}$) and the receiver data input pin (RxD) are electrically disconnected from the internal logic. The transmit data output pin (TxD) is connected to the internal receiver data logic, and the transmit shift clock pin ($\overline{\text{TxC}}$) is connected to the internal receiver shift clock logic. All other features of the SIO are unaffected.

6.3.5 - Baud rate generators

Each channel in the SIO contains a programmable baud rate generator (BRG). Each BRG consists of an 8-bit time constant register, and 8-bit down counter, a control register, and a flip-flop on the output to provide a square wave signal out. In addition to the flip-flop on the output, there is also a flip-flop on the input clock ; therefore, the maximum output frequency of the BRG is one-forth of the input clock frequency. This maximum output frequency occurs when divide by four mode is selected, and the time constant register is loaded with the minimum count of «01H». The equation to determine the output frequency is :

$$\text{Output frequency} = \frac{\text{Input frequency}}{(\text{divide by selected}) \times (\text{time constant value in decimal})}$$

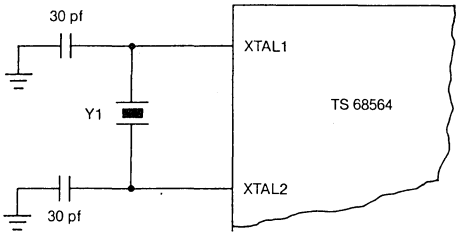
For example, when the constant register is loaded with «01H» and divide by four is selected, one output clock will occur for every four input clocks. If the time constant value loaded is «00H» (256 decimal) instead of «01H» and divide by 64 is selected, one output clock will occur for every 16384 input clocks. Note that the minimum count value is «01H» (1 decimal), and the maximum count value is «00H» (256 decimal).

The output of the baud rate generator may be programmed to drive the transmitter (BRG output on $\overline{\text{TxC}}$), the receiver (BRG output of the baud) rate generator may be programmed to drive the transmitter (BRG output on $\overline{\text{TxC}}$), the receiver (BRG output on $\overline{\text{RxC}}$), both (BRG output on $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$), or neither ($\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ are inputs). After a reset, the baud rate generator is disabled, divide by four is selected, and $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ are inputs.

The baud rate generator should be disabled before the CPU writes to the time constant register. This is necessary because no attempt was made to synchronize the loading of a new time constant with the clock used to drive the BRG.

Figure 20 indicates the external components needed to connect a crystal oscillator to the SIO XTAL inputs. The allowed crystal parameters are also listed.

For a 3.6864 MHz input signal to the baud rate generator, the time constants, listed in Table 9, are loaded to obtain the desired baud rates (in x1 clock mode).



Crystal Parameters :

Parallel resonance, fundamental mode AT cut
R_S = < 150 Ω (Fr = 2.8 – 5.0 MHz) ;
R_S = < 300 Ω (Fr = 2.0 – 2.7 MHz) ;
C_L = 18 pF ; C_M = 0.02 pF ; C_h = 5 pF ; L_M = 96 mH
F_R (type) = 2.4576 MHz

Figure 20 : SIO external oscillator components.

5

6.4 · Asynchronous operation

Many types of Asynchronous operations are performed by the TS 68564 SIO. Figure 21 represents a typical Asynchronous message format and some of the options available on the SIO. The transmit process inserts start, stop, and parity bits to a variable data format and supplies a serial data stream to the Transmit Data output (TxD). The receiver takes the data from the Receive Data input (RxD) and strips away expected start and stop bits at a programmed clock rate. It provides error checking for overrun, parity, and carrier-loss errors, and, if desired, provides interrupts for these conditions.

To set up the SIO for Asynchronous operation, the following registers need to be initialized : Mode Control Register, Interrupt Control Register, and transmitter Control register. The Mode Control Register must be programmed before the other registers to assure proper operation of the SIO. The following registers are used to transfer data or to communicate status between the SIO and the CPU or other bus master when operating in Asynchronous modes : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

The SIO provides five I/O lines that may be used for modem control, for external interrupts, or as general purpose I/O. The Request To Send ($\overline{RTS}$) and Data Terminal Ready ($\overline{DTR}$) pins are outputs that follow the inverted state of their respective bits in the Transmitter Control Register. The $\overline{RTS}$ pin can also be used to signal the end of a message in Asynchronous modes, as explained below in the Transmitter section. The Data Carrier Detect ($\overline{DCD}$), Clear To Send ($\overline{CTS}$), and $\overline{SYNC}$ pins are inputs to the SIO in Asynchronous modes. $\overline{DCD}$ and $\overline{CTS}$ can be used as auto enables to the receiver and transmitter, respectively, or if External/Status Interrupts are enabled all three input pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

Table 9 · Time-constant values

Rate	Time constant	Divide by	Error
19200	48	4	—
9600	96	4	—
7200	128	4	—
4800	192	4	—
3600	256	4	—
2400	24	64	—
2000	29	64	69 %
1800	32	64	—
1200	48	64	—
600	96	64	—
300	192	64	—

6.4.1 · Asynchronous transmit

6.4.1.1 · Start of transmission

The SIO will start transmitting data when the Transmit Enable bit is set to a one, and a character has been loaded into the transmit buffer. If the Tx Auto Enables bit is set, the SIO will wait for a Low on the Clear to Send input ($\overline{CTS}$) before starting data transmission. The Tx Auto Enables features allows the programmer to send the first data character of the message to the SIO without waiting for $\overline{CTS}$ to go low. In all cases, the Transmit Enable bit must be set before transmission can begin. The transitions on the $\overline{CTS}$ pin will generate External/Status interrupt requests and also latch up the external/status logic. The external/Status logic should be rearmed by issuing a Reset external/Status Interrupts command.

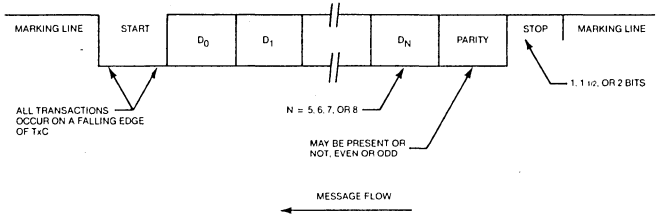


Figure 21 : Asynchronous message format.

6.4.1.2 · Transmit characteristics

The SIO automatically inserts a start bit, the programmed parity bit (odd, even, or no parity), and the programmed number of stop bits to the data character to be transmitted. The transmitter can transmit from one to eight data bits per character. All characters are transmitted least-significant bit first. When the character length programmed is six or seven bits, the unused bits of the transmit buffer are automatically ignored. When a character length of five bits or less is programmed, the data loaded into the transmit buffer must be formatted as described in the Transmitter Control Register part of the Register Description section. Serial data is shifted out of the TxD pin on the falling edge of the Transmit Clock ($\overline{TxC}$) at a rate equal to 1, 1/16th, 1/32nd, or 1/64th of $\overline{TxC}$.

6.4.1.3 · Data transfer

The SIO will signal the CPU or orther bus master with a transmit interrupt request and set the Tx Buffer Empty bit in Status Register 0, every time the contents of the transmit buffer are loaded into the transmit shift register. The interrupt request will be cleared when a new character is loaded into the transmit buffer, or a Reset Tx Interrupt Pending command (Command 5) is issued. If Command 5 is issued, the transmit buffer will have to be loaded before any additional transmit interrupt requests are generated. The Tx Buffer Empty bit is reset when a new character is loaded into the transmit buffer.

The All Sent bit in Status Register 1 is used to indicate when all data in the shift register has been transmitted, and the transmit buffer is empty. This bit is low, while the transmitter is sending characters, and it will go High one bit time after the transmit clock that clocks out the last stop bit of the character ont the TxD pin. No interrupts are generated by the All Sent bit transitions. The Request To Send ($\overline{RTS}$) bit in the Transmitter Control Register may also be used to signal the end of transmission. If this bit is set to a one, its associated output pin ($\overline{RTS}$) will go Low. When this bit is reset to a zero, the $\overline{RTS}$ pin will go High one bit time after the transmit clock that clocks out the last stop bit, only if the transmit buffer is empty.

The Transmit Data output (TxD) is held marking (High) after a reset or when the transmitter has no data to send. Under program control, the Send Break command can be issued to hold TxD spacing (low) until the command is cleared, even if the transmitter is not enabled.

6.4.2 · Asynchronous receive

Asynchronous operation begins when the Receiver Enable bit in the Receiver Control Register is set to a one. If the Rx Auto Enables bit is also set, the Data Carrier Detect ($\overline{DCD}$) input pin must be Low as well. The receiver will start assembling a character as soon as a valid start bit is detected, if a clock mode other than x1 is selected. A valid start bit is a High-to-Low transition on the Receive Data input (RxD) with the Low time lasting at least one-half bit time. The High-to-Low transition starts an internal counter and, at mid-bit time, the counter output is used to sample the input signal to detect if it is still low. When this condition is satisfied, the following data bits are samped at mid-bit time until the entire character is assembled. The start bit detection logic is then rearmed to detect the next High-to-Low transition. If the x1 clock mode is selected, the start bit detection logic is disabled, and bit synchronization must be accomplished externally. Receive data is sampled on the rising edge of the Receiver Clock ($\overline{RxC}$).

The Receiver may be programmed to assemble five to eight data bits, plus a parity bit, into a character. The character is right-justified in the shift register and then transferred to the receive dat FIFO. All data transferts to the FIFO are in eight-bit groups. If the character length assembled is less than eight-bits, the receiver inserts ones in the unused bits. If parity is enabled, the parity bit is transferred with the character, unless eight bits per character is programmed, in which case, the parity bit is stripped from the character before transfer.

A Receiver Interrupt request is generated every time a character is shifted to the top of the receive data FIFO, if Interrupt on All Receive Characters mode is selected. The Rx Character Available bit in Status Register 0 is also set to a one every time a character is shifted to the top of the receive data FIFO. The Rx Character Available bit is reset to a zero when the receive buffer is read.

After a character is received, it is checked for the following error conditions :

6.4.2.1 - Parity error

If parity is enabled, the Parity Error bit in Status Register 1 is set to a one whenever the parity bit of the received character does not match the programmed parity. Once this bit is set, it remains set (latched), until an Error Reset command (command 6) is issued. A Special receive Condition interrupt is generated when this bit is set, if parity is programmed as a Special Receive Condition.

6.4.2.2 - Framing error

The CRC/Framing Error bit in Status Register 1 is set to a one, if the character is assembled without a stop bit (a Low level detected instead of a stop bit). This bit is set only for the character on which the framing error occured ; it is updated at every character time. Detection of a framing erros adds an additional one-half of a bit time to the character time, so the framing error is not interpreted as a new start bit. A Special Receive Condition interrupt is generated when this bit is set.

6.4.2.3 - Overrun error

If four or more characters are received before the CPU (or other bus master) reads the receive buffer, the fourth character assembled will replace the third character in the receive dat FIFO. If more than four characters have been received, the last character assembled will replace the third character in the data FIFO. The character that ha been written over is flagged with an overrun error in the error FIFO.

When this character is shifted to the top of the receive data FIFO, the Receive Overrun Error bit in Status Register 1 is set to a one ; the error bit is latched in the status register, and a Special Receive Condition interrupt is generated. Like Parity Error, this bit can only be reset by an Error Reset command.

6.4.2.4 - Break condition

A Break character is defined as a start bit, an all zero data word, and a zero in place of the stop bit. When a break character is detected in the receive data stream, the Break/Abort bits in Status Register 0 is set to a one, and an External/Status interrupt is requested. This interrupt is then followed by a Framing Error interrupt request when the CRC/Framing Error bit in Status Register 1 is set. A Reset External/Status Interrupts command (Command 2) should be issued to reinitialize the break detection interrupt logic. The receiver will monitor the data stream input for the termination of the break sequence. When this condition is detected, the Break/Abort bit will be interrupt should also be handled by issuing Command 2 to reinitialize the external/status logic. At the end of the break sequence, a single null character will be left in the receive data FIFO. This character should be read and discarded.

Because Parity Error and receive Overrun Error flags are latched, the error status that is read from Status Register 1 reflects an error in the current word in the receive data FIFO, plus any parity or overrun erros received since the last Error Reset Command. To keep correspondence between the state of the error FIFO and the contents of the receive data FIFO. Status Register 1 should be read before the receive buffer. If the status is read after the data and more than one character is stacked in the data FIFO during the read of the receive buffer, the status flags read will be for the next word. Keep in mind that when a character is shifted up to the top of the data FIFO (the receive buffer), its error flags are shifted into Status Register 1.

An exception to the normal flow of data through the receive data FIFO occurs when the Receive Interrupt On First Character Only mode is selected. A special Receive Condition interrupt in this mode holds the error data, and the character itself (even if read from the data FIFO) until the Error Reset command (Command 6) is issued. This prevents further data from becoming available in the receiver, until Command 6 is issued, and allows CPU intervention on the character with the error even if DMA or block transfer techniques are being used.

6.5 · Synchronous operation

6.5.1 · Introduction

Before describing byte-oriented, synchronous transmission and reception, the three types of character synchronization - Monosync, Bisync, and External Sync - require some explanation. These modes uses the x1 clock for both Transmit and Receive operations. Data is sampled on the rising edge of the Receive Clock inout ($\overline{RxC}$). Transmitter data transitions occur on the falling edge of the Transmit Clock input ($\overline{TxC}$).

The difference between Monosync, Bisync, and External Sync are in the manner in which initial receive character synchronization is achieved. The mode of operation must be selected before sync characters are loaded, because the registers are used differently in the various modes. Figure 22 shows the formats for all three synchronous modes.

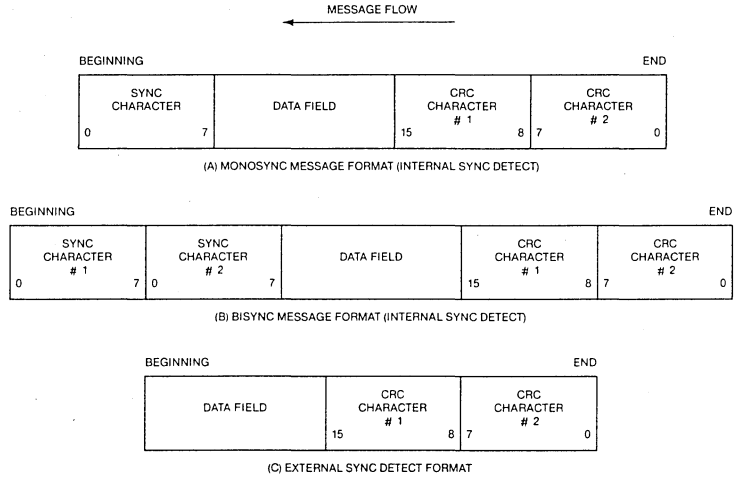


Figure 22 : Syncrhonous formats.

6.5.1.1 · Monosync

In the Monosync mode (8-bit sync mode), the transmitter transmits the sync character in Sync Word Register 1. The receiver compares the single sync character with the programmed sync character stored in Sync Word Register 2. A match implies character synchronization and enables data transfer. The $\overline{SYNC}$ pin is used as an output in this mode and is active for the part of the receive clock that detects the sync character.

6.5.1.2 · Bisync

In the Bisync mode (16-bit sync mode), the transmitter transmits the sync character in Sync Word Register 1 followed by the sync character in Sync Word Register 2. The receiver compares the two contiguous sync characters with the programmed sync characters stored in Sync Word registers 1 and 2. A match implies character synchronization and enables data transfer. The SYNC pin is used as an output in this mode and is active for the part of the receive clock that detects the sync characters.

6.5.1.3 · External sync

In the External Sync mode, the transmitter transmits the sync character in Sync Word Register 1. Character synchronization for the receiver is established externally. The $\overline{SYNC}$ pin as an input that indicates that external character synchronization has been achieved. After the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input pin (see Figures 23 and 24). The $\overline{SYNC}$ input pin must be held Low until character synchronization is lost. Character assembly begins on the rising edge of the Receive Clock that precedes the falling edge of the $\overline{SYNC}$ input pin.

In all cases, after a reset (hardware or software), the receiver is in the Hunt phase, during which time the SIO looks for character synchronization. The Hunt phase can begin only when the receiver is enabled, and data transfer can begin only when character synchronization has been achieved. If character synchronization is lost ; the Hunt phase can be reentered by setting the Enter Hunt Mode bit in the Receiver Control Register. In the transmit mode, the transmitter always sends the programmed number of sync bits (8 or 16), regardless of the bits per character programmed.

In the Monosync, Bisync, and External Sync modes, assembly of received data continues until the SIO is reset, or until the receiver is disabled (by command or the $\overline{DCD}$ pin in the Rx Auto Enables mode), or until the CPU sets the Enter Hunt Mode bit.

After initial synchronization has been achieved, the operation of the Monosync, Bisync, and External Sync modes is quite similar. Any differences are specified in the following text.

To set up the SIO for Synchronous operations, the following registers need to be initialized : Mode control Register, Interrupt Control Register, Receiver Control Register, Transmitter Control Register, Sync Word 1, and Sync Word 2. The Mode Control Register must be programmed before other registers to assure proper operation of the SIO. The following registers are used to transfer data or communicate status between the SIO and the CPU or other bus master : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

The SIO provides four I/O lines in Synchronous modes that may be used for modem control, for external interrupts, or as general purpose I/O. The Request to Send ($\overline{RTS}$) and Data Terminal Ready ($\overline{DTR}$) pins are outputs that follow the inverted state of their respective bits in the Transmit Control register. The Data Carrier Detect ($\overline{DCD}$) and Clear To Send ($\overline{CTS}$) pins are inputs that can be used as auto enables to the receiver and transmitter, respectively. If External/Status Interrupts are enabled, the $\overline{DCD}$ and $\overline{CTS}$ pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

6.5.2 - Synchronous transmit

6.5.2.1 - Initialization

Byte-oriented transmitter programs are usually initialized with the following parameters : odd-even or no parity, x1 clock mode, 8- or 16-bit sync character(s), CRC polynomial, Transmit Enables, interrupt modes, and transmit character length. If Parity is enabled, the transmitter will only add a parity bit to a character that is loaded into the transmit buffer ; it will not add a parity bit to the automatically inserted sync character(s) or the CRC characters.

One of two polynomials may be used with Synchronous modes, CRC-16 ($x^{16} + x^{15} + x^2 + 1$) or SDLC-CRC ($x^{16} + x^{12} + x^5 + 1$). For either polynomial (SDLC mode not selected), the CRC generator and checker are reset to all zeros. Both the receiver and transmitter use the same polynomial.

After reset (hardware or software), or when the transmitter is not enabled, the Transmit Data (TxD) output pin is held High (marking). Under program control, the Send Break bit in the Transmitter Control Register can be set to a one, forcing the TxD output pin to a Low level (spacing), even if the transmitter is not enabled. The spacing condition will persist until the Send Break bit is reset to a zero. A programmed break is effective as soon as it is written into the Transmit Control Register ; any characters in the transmit buffer and transmit shift register are lost.

If the transmit buffer is empty when the Transmit enable bit is set to a one, the transmitter will start sending 8- or 16-bit sync characters. Continuous syncs will be transmitted on the TxD output pin, as long as no data is loaded into the transmit buffer. Note, if a character is loaded into the transmit buffer before enabling the transmitter, that character will be sent in place of the sync character(s).

6.5.2.2 - Start of transmission

Transmission will begin with the loading of the first data character into the transmit buffer, if the transmitter is already enabled. For CRC to be calculated correctly on each message, the CRC generator must be reset to all zeros before the first data character is loaded into the transmit buffer. This is accomplishezd by issuing a Reset TxCRC Generator command in the Command Register.

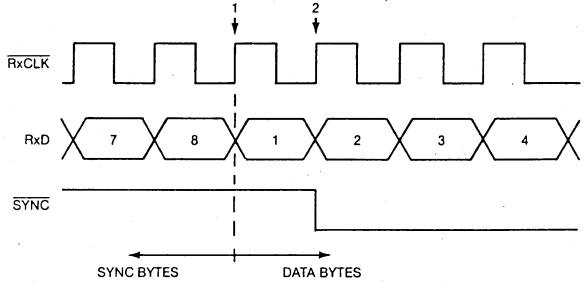


Figure 23 : External SYNC timing.

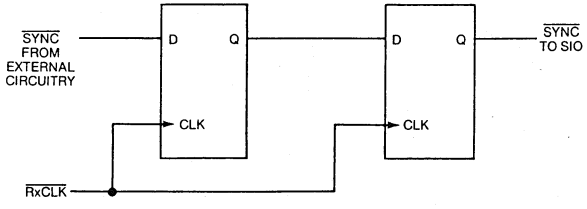


Figure 24 : Simple external SYNC delay.

6.5.2.3 - Synchronous transmit characteristics

In all Synchronous modes, characters are sent with the least-significant bits first. All data is shifted out of the Transmit Data pin (TxD) on the falling edge of the Transmit Clock (TxC). The transmitter can transmit from one to eight data bits per character. This requires right-hand justification of data written to the transmit buffer, if the selected word length is less than eigth bits per character. When the programmed character length is six or seven bits, the unused bits in the transmit buffer are ignored. If a word length of five bits per character or less is selected, the data loaded into the transmit buffer must be formatted as described in the Transmit Control register part of the Register Description section.

The number of bits per character to be transmitted can be changed on the fly. Any data written to the transmit buffer, after the bits per character field is changed, are affected by the change. The same is true of any characters in the buffer at the time the bits per character field is changed. The change in the number of bits per character does not affect the character in the process of being shifted out.

A Transmitted message can be terminated by CRC and sync characters only, or by pad characters (replacing the sync character(s) in the Sync Word Registers with pad characters). How a message is terminated is controlled by the Tx Underrun/EOM latch in Status Register 0.

6.5.2.4 - Data transfer

A Transmit Interrupt is generated each time the transmit buffer becomes empty. The interrupt may be satisfied either by writing another character into the transmit buffer or by resetting the Transmit Interrupt Pending latch with a Reset Tx interrupt Pending command. If the interrupt is satisfied with this command, and nothing more is written into the transmit buffer, there can be no further Transmit interrupts due to a Buffer Empty condition, because it is the process of the buffer becoming empty that causes the interrupts. This situation does cause a Transmit Underrun condition when the data in the shift register is shifted out.

Another way of detecting when the transmitter requires service is to poll the Tx Buffer Empty bit in Status Register 0. This bit is set to a one every time the data in the transmit buffer is downloaded into the transmit shift register. When data is written to the transmit buffer, this bit is reset to zero.

The SIO has all the signals and controls necessary to implement a DMA transfer routine for the transmitter. The routine may be configured to enable the DMA controller, after the first character is written to the transmit buffer, and then using the TxRDY output pin to signal the DMA that the transmitter requires service. If a data character is not loaded into the transmit buffer by the time the transmit shift register is empty, the SIO enters the Transmit Underrun condition.

6.5.2.5 - Transmit underrun/end of message

When the transmitter has no further data to transmit, the SIO inserts filler characters to maintain synchronization. The SIO has two programmable options for handling this situation : sync characters can be inserted, or the CRC characters generated so far can be sent, followed by sync characters. These options are controlled by the state of the Transmit Underrun/EOM Latch in Status Register 0.

Following a hardware or software reset, the Transmit Underrun/EOM Latch is set to a one. This allows sync characters to be inserted when there is no data to send. CRC is not calculated on the automatically inserted sync characters. To allow CRC characters to be sent when the transmitter has no data, the Transmit Underrun/EOM Latch must be reset to zero. This Latch is reset by issuing a Reset TxUnderrun/EOM Latch command in the Command Register. Following the CRC characters, the SIO sends sync characters to terminate the message.

There is no restriction as to when, in the message, the Transmit Underrun/EOM Latch can be reset, but once the reset command is issued, the 16-bit CRC is sent and followed by sync characters the first time the transmitter has no data to send. A Transmit Underrun condition will cause an External/Status Interrupt to be generated whenever the Transmit Underrun/EOM Latch is set.

For sync character insertion only, at the determination of a message, a Transmit Interrupt is generated only after the first automatically inserted sync character is loaded into the transmit shift register. The status bits in Status Register 0 indicate that the Transmit Underrun/EOM Latch and the TxBuffer Empty bit are set.

For CRC insertion, followed by sync characters, at the termination of a message, the Transmit Underrun/EOM Latch is set, and the Tx Buffer Empty bit is reset while the CRC characters are being sent. When the CRC characters are completely transmitted, the Tx Buffer status bit is set, and a Transmit Interrupt is generated, indicating to the CPU that another message can begin.

This Transmit Interrupt occurs when the first sync character following the CRC characters is loaded into the transmit shift register. If no more messages are to be transmitted, the program can terminate transmission by disabling the transmitter.

6.5.2.6 - CRC generation

Setting the Tx CRC Enable bit in the Transmit Control Register initiates CRC accumulation when the program sends the first data character to the SIO. To ensure CRC is calculated correctly on each message, the reset Tx CRC Generator command should be issued before the first data character of the message is sent to the SIO.

The Tx CRC Enable bit can be changed on the fly at any point in the message to include or exclude a particular data character from CRC accumulation. The TxCRC Enable bit should be in the desired state when the data character is loaded from the transmit dat buffer into the transmit shift register. To ensure this bit is in the proper state, the TxCRC Enable bit should be loaded before sending the data character to the SIO.

6.5.2.7 - Transmit termination

The SIO is equipped with a special termination feature that maintains data integrity and validity. If the transmitter is disabled (by resetting the Transmit Enable bit or using the Tx Auto Enable signal) while a data or sync character is being transmitted, the character is transmitted as usual but is followed by a marking line instead of sync or CRC characters.

When the Transmitter is disabled, a character in the transmit buffer remains in the buffer. If the transmitter is disabled. While CRC characters are being transmitted, the 16-bit transmission is completed, but the remaining bits of the CRC characters are replaced by sync characters.

6.5.2.8 - Bisync protocol transmission

In a Bisync Protocol operation, once synchronization is achieved between the transmitter and receiver, fill characters are inserted to maintain that synchronization when the transmitter has no more data to send. The different options available in the SIO are described in the Transmit Underrun/End of Message part of this section. If pad characters are to be sent in place of sync characters following the transmission of the CRC, the program can set the SIO transmitter to eight bits per character and then load «FFH» to the transmit buffer while the CRC characters are being sent. Alternativaly, the sync characters in Sync Word Registers 1 and 2 can be redefined to be pad characters during this time. The following example is included to clarify this point :

The SIO interrupts the CPU with a Transmit Interrupt when the Tx Buffer Empty bit is set.

The CPU recognizes that the last character (ETX) of the message has already been sent to the SIO transmit buffer by examining the internal program status.

To force the SIO to send CRC, the CPU issues the Reset Tx Underrun/EOM Latch command and clears the current Transmit Interrupt with the Reset Tx Interrupt Pending command. Resetting the interrupt with this command prevents the SIO from requesting more data. The SIO then begins to send CRC (because the transmitter is an underrun condition) and sets the Transmit Underrun/EOM Latch, with causes an External/Status interrupt.

The CPU Satisfies the External/Status Interrupt by loading pad characters into the transmit buffer and clears the interrupt by issuing the Reset External/Status Interrupt command.

The pad character will follow the CRC characters in this sequence, instead of the usual sync characters. A Transmit Interrupt is generated when the pad character is loaded into the transmit shift register.

From this point on, the CPU can send more pas characters or sync characters.

The Transparent mode of operation in Bisync Protocol is made possible with the SIO's ability to change the Tx CRC Enable bit at any time during program sequencing and with the additional capability of inserting 16-bit sync characters. Exclusion of DLE (Data Link Escape) characters from CRC calculation can be achieved by disabling CRC calculations immediately preceding the DLE character transfer to the transmit buffer. In the case of a transmit underrun condition in the transparent mode, a pair of DLE-SYN characters is sent. The SIO can be programmed to send the DLE—SYNC sequence by loading a DLE character into Sync Word Register 1 and SYNC character into Sync Word register 2.

5

The SIO always transmits two sync characters (16 bits) in Bisync mode. If additional sync characters are to be transmitted before a message, the CPU can delay loading data to the transmit buffer until the required number of syncs have been sent. No CRC calculations are done on any automatically inserted sync characters. An alternate method of sending additional sync characters is to load the sync characters into the transmit buffer, in which case the transmitter will treat the characters as data. The Tx CRC Enable bit should not be set, until true data is going to be loaded into the buffer, to avoid performing CRC calculations on the additional sync characters.

6.5.3 - Synchronous receive

6.5.3.1 - Initialization

Byte-oriented receive programs are usually initialized with the following parameters : odd-even or no parity, x1 clock mode (necessary because of the start bit detection logic), 8- or 16-bit sync character(s), CRC polynomial, Receiver Enables, interrupt modes, and receive character length. Care must be taken is Parity is enabled. The receiver will usually detect a Parity Error on all sync characters, after synchronization is achieved, and on the CRC characters.

6.5.3.2 - Receiver hunt mode

After the SIO is initialized for a Synchronous receive operation, the receiver is in the Hunt phase. During the Hunt phase, the receiver does a bit-by-bit comparison of the incoming data stream and the sync character(s) stored in the Sync Word register 2 (for Monosync mode) and Sync Word registers 1 and 2 (for Bisync mode). When a match occurs, the Hunt phase is terminated, and the following data bits are assembled into the programmed character length and loaded into the receive data FIFO.

6.5.3.3 - Receive characteristics

The receiver may be programmed to assemble five to eight data bits into a character. The character is right-justified in the shift register and transferred to the receive data FIFO. All data transfers to the FIFO are in 8-bit groups. When the programmed character length is less than eight bits, the most significant bit(s) transferred with a character will be the least significant bit(s) of the next character. The programmed character length may be changed on the fly during a message ; however, care must be taken to assure that the change is effective before the number of bits specified for the character length have been assembled.

When the Sync Character Load Inhibit bit in the receiver Control Register is set, all characters in the receive data stream that match the byte loaded into Sync Word Register 1 will be inhibited from loading into the receive data FIFO. The comparison between Sync Word Register 1 and the incoming data occurs at a character boundary time.

This is an 8-bit comparison, regardless of the bits per character programmed. CRC calculations will be performed on all bytes, even if the characters are not transferred to the receive data FIFO, as long as the RxCRC Enable bit set.

6.5.3.4 - Data transfer and status monitoring

After character synchronization is achieved, the assembled characters are transferred to receive data FIFO, and the status information for each character is transferred to the receive error FIFO. The following four modes are available to transfer the received data and its associated status to the CPU.

6.5.3.5 - No receive interrupts enabled

This mode is used either for polling operations or for off-line conditions. When transferring data, using a polling routine, the Rx Character Available bit in Status register 0 should be checked to determine if a receive character is available for transfer. Only when a character is available should the receive buffer and Status Register 1 be read. The Rx Character Available bit is set when a character is loaded to the top of the receive data FIFO. This bit is reset during a read of the receive buffer.

6.5.3.6 - Interrupt on first character only

This interrupt mode is normally used to start a DMA transfer routine or, in some cases, a polling loop. The SIO will generate an interrupt the first time a character is shifted to the top of the receive data FIFO after his mode is selected or reinitialized. An interrupt will be generated thereafter only if a Special Receive condition is detected. This mode is reinitialized with the Enable Interrupt On Next Receive character command. Parity Errors do not cause interrupts in this mode ; however, a Receive Overrun Error will.

6.5.3.7 - Interrupt on every character

This interrupt mode will generate a receiver Interrupt every time a character is shifted to the top of the receive data FIFO. A Special Receive Condition interrupt on a parity error is optional in this mode.

6.5.3.8 - Special receive condition interrupt

The special condition interrupt mode is not an interrupt mode as such, but works in conjunction with Interrupt On Every Character or interrupt On First Character Only modes. When the Status Affects Vector bit in either channel is set, a Special Receive condition will modify the receive Interrupt vector to signal the CPU of the special condition.

Receive Overrun Error and Parity Error are the only Special Receive conditions in Synchronous receive mode. The overrun and parity error status bits in Status register 1 are latched when they occur ; they will remain latched until and Error Reset command is issued. As long as either one of these bits is set, a Special Receive condition interrupt will be generated at every character available time. Since these two status bits are latched, the error status in Status Register 1, when read, will reflect an error in the current word in the receive buffer, in addition to any Parity or Overrun errors received since the last Error Reset command.

6.5.3.9 - CRC error checking and receiver message termination

A CRC error check on the received mesdsage can be performed on a per character basis under program control. The RxCRC Enable bit must set/reset by the program before the next character is transferred from the receive shift register to the receive data FIFO. This ensures proper inclusion or exclusion of data characters in the CRC check.

There is an 8-bit delay between the time a character is transferred to the receive data FIFO and the time the same character starts to enter the CRC checker. An additional 8-bit times are needed to perform CRC calculations on the character. Due to this serial nature of CRC calculations, the receive Clock ($\overline{RxC}$) must cycle 16 times after the second CRC character has been loaded into the receive data FIFO or 20 times (the previous 16 plus 3-bit buffer delay and 1-bit input delay) after the last bit is at the RxD input, before CRC calculation is complete. The CRC Framing Error bit in Status Register 1 will contain the comparison results of the CRC checker. The comparison results should be zero, indicating error-free transmission. The results in the status bit are valid only at the end of CRC calculation. If the result is examined before this time, it usually indicates an error (the bit is High). The comparison is made at each character available time and is valid until the character is read from the receive data FIFO.

6.6 - SDLC/HDLC operation

The TS 68564 SIO is capable of handling both High-level Synchronous data Link Control (HDLC) and IBM Synchronous Data Link Control (SDLC) protocols. In the following discussion, only SDLC is referenced beacause of the high degree of similarity between SDLC and HDLC.

The SDLC mode is considerably different from Monosync and Bisync protocols, because it is bit oriented rather than character oriented. Bit orientation makes SDLC a flexible protocol in terms of message length and bit patterns. The SIO has several built-in features to handle variable message length. Detailed information concerning SDLC protocol can be found in literature on this subject, such as IMB document GA27-3093.

The SDLC message, called the frame (Figure 25) is opened and closed by flags, which are similar to the sync characters used in other Synchronous protocols. The SIO handles the transmission and recognition of the flag characters that mark the beginning and end of the frame. Note that the SIO can receive shared-zero flags but cannot transmit them. The 8-bit address field of a SDLC frame contains the secondary station address. The SIO receiver has an Address Search mode, which recognizes the secondary station so that it can accept or reject a frame.

The control field of the SDLC frame is Transparent to the SIO ; it is simply transferred to the CPU. The SIO handles the Frame Check sequence in a manner that simplifies the program by incorporating features such as initializing the CRC generator to all ones, resetting the CRC checker when the opening flag is detected in the receive mode, and sending the Frame Check/Flag sequence in the transmit mode. Controller hardware is simplified by automatic zero insertion and delection logic, contained in the SIO.

To set up the SIO for SDLC operation, the following registers need to be initialized : Mode control Register, Interrupt Control Register, Register Control Receiver, Transmitter Control Register, Sync Word Register 1, and Sync Word register 2. The Mode Control Register must be programmed before the other registers to assure proper operation of the SIO. The following registers are used to transfer data or communicate status between the SIO and the CPU or other bus master when operating in SDLC mode : Command Register, Status Register 0, Status Register 1, Data Register, and the Vector Register.

Sync Word Register 1 contains the secondary station address, and Sync Word Register 2 stores the flag character and must be programmed to «01111110».

The SIO provides four I/O lines in SDLC mode that may be used for modem control, for external interrupts, or as general purpose I/O. The Request to Send ($\overline{RTS}$) and Data Terminal Ready ($\overline{DTR}$) pins are output that follow the inverted state of their respective bits in the Transmit Control Register. The Data Carrier Detect ($\overline{DCD}$) and Clear To Send ($\overline{CTS}$) pins are inputs that can be used as auto enables to the receiver and transmitter, respectively. If External/Status Interrupts are enabled, the $\overline{DCD}$ and $\overline{CTS}$ pins will be monitored for a change of status. If these inputs change for a period of time greater than the minimum specified pulse width, an interrupt will be generated.

In the following discussion, all interrupt modes are assumed enabled.

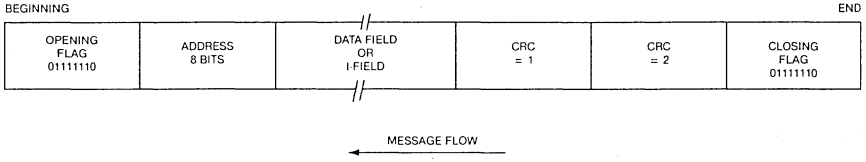


Figure 25 : Transmit/receive SDLC/HDLC message format.

6.6.1 - SDLC transmit

6.6.1.1 - Initialization

The SIO is initialized for SDLC mode by selecting these parameters in the Mode Control Register : x1 Clock Mode, SDLC Mode, and Sync Modes Enabled. Parity is normally not used in SDLC mode, because the transmitter will not add parity to the flag character or the CRC characters, thus causing Parity Errors in the receiver. If CRC is to be calculated on the transmitted data, the SDLC-CRC polynomial must be selected in the Interrupt Control Register (CRC-16 polynomial in SDLC Mode produce unknown results).

After reset (hardware of software), or when the transmitter is not enabled, the Transmit Data (TxD) output is held High (marking). Under program control, the Send Break bit in the Transmit Control Register can be set to a one, forcing the TxD output to a Low level (spacing), even if the transmitter is not enabled. The spacing condition will persist until the Send Break bit is reset to a zero. If the transmit buffer is empty when the Transmit Enable bit is set to a one, the transmitter will start sending flag characters. Continuous flags will be transmitted on the TxD output pin as long as no data is loaded into the transmit buffer.

Note : If a character is loaded into the transmit buffer before enabling the transmitter, that character will be sent in place of a flag.

An abort sequence may be transmitted at any time by issuing the Sent Abort command (Command 1). This causes at least eight, but less than fourteen, ones to be sent before the output revers back to continuous flags. It is possible that the Abort sequence (eight 1's) could follow up to five continuous ones (allowed by the zero insertion logic) and, thus, cause as many as thirteen ones to be sent. Any data being transmitted and any data in the transmit buffer is lost when an abort is issued.

The zero insertion logic in the transmitter will automatically insert a 0 after five continuous ones in the data stream. This does not apply to flags or aborts.

6.6.1.2 - Start of transmission

Transmission will begin with the loading of the first character into the transmit buffer if the transmitter is already enabled. For CRC to be calculated correctly on each frame, the CRC generator must be initialized to all ones before the first character is loaded. This is accomplished by issuing a Reset Tx CRC Generator command in the Command Register. The first non-flag character transmitted is the address field. The SIO does not automatically transmit a station address, this is left to the programmer. The SIO will only transmit flags and CRC characters automatically.

6.6.1.3 - SDLC transmit characteristics

Any length SDLC frame can be transmitted. All characters are transmitted with the least-significant bits first. All data is shifted out of the Transmit Data pin (TxD) on the falling edge of the Transmit Clock ($\overline{TxC}$). The transmitter can transmit from one to eight data bits per character. This requires right-hand justification of data written to the transmit buffer, if the word length selected is less than eight bits per character. When the programmed character length is six or seven bits, the unused bits in the transmit buffer are ignored. If a word length of five bits per character or less is selected, the data loaded into the transmit buffer must be formatted as described in the Transmit Control Register part of the Register Description section.

The number of bits per character to be transmitted can be changed on the fly. Any data, written to the transmit buffer after the bits per charater field is changed, are affected by the change. The same is true of any characters in the buffer at the time the bits per character field is changed, are affected by the change. The same is true of any characters in the buffer at the time the bits per character field is changed. The change in the number of bits per character does not affect the character in the process of being shifted out. Flag characters are always eight bits in length, and CRC is always 16 bits in length, regardless of the programmed bits per character. A transmitted frame can be terminated by CRC and a flag, by a flag only, or by an abort. This is controlled by the Tx Underrun/EOM Latch and the Send Abort command.

6.6.1.4 - Data transfers

A Transmit Interrupt is generated each time the transmit buffer becomes empty. The interrupt may be satisfied either by writing another character into the transmit buffer or by resetting the Transmit Interrupt Pending latch with a Reset Tx Interrupt Pending command. If the interrupt is satisfied with this command, and nothing more is written into the transmit buffer, there

are no further transmitter interrupts, and Transmit Underrun condition will occur when the data in the shift register is shifted out. When another character is written to the buffer and loaded into the shift register, the transmit buffer can again become empty and interrupt the CPU. Following the flags in an SDLC operation, the 8-bit address field, control field, and information field may be sent to the SIO, using the Transmit Interrupt mode. The SIO transmits the frame check sequence using the Transmit Underrun feature.

When the transmitter is first enabled, the transmit buffer is already empty and obviously cannot then become empty. Therefore, no transmit interrupt can occur until after the first data character is written to the transmit buffer.

Another way of detecting when the transmitter requires service is to poll the Tx Buffer Empty bit in Status Register 0. This bit is set to a one every time the data in the transmit buffer is downloaded into the transmit shift register. When data is written to the transmit buffer, this bit is reset to zero.

The SIO has all the signals and controls necessary to implement a DMA transfer routine for the transmitter. The routine may be configured to enable the DMA controller, after the first character is written into the transmit buffer, using the $\overline{\text{TxRDY}}$ output pin to signal the DMA that the transmitter requires service. The DMA transfer can be terminated, when the DMA block count is reached, using the Tx Underrun/EOM interrupt.

6.6.1.5 - Transmit underrun/End of message

SDLC-like protocols do not have provisions for fill characters within a message. The SIO , therefore automatically terminates an SDLC frame when the transmit data buffer is empty, and the output shift register has no more bits to send. It does this by first sending the two bytes of CRC and then following these with one or more flags. This technique allows very high-speed transmission under DMA or CPU control, without requiring the CPU to respond quickly to the end of message situation.

The action that the SIO takes in the underrun situation depends on the state of the Transmit Underrun/EOM status bit in Status Register 0. Following a reset, the Transmit Underrun/EOM bit is set to a one and prevents the insertion of CRC characters during the time there is no data to send. Consequently, flag character are sent. If the Transmit Underrun/EOM status bit is zero when the underrun condition occurs, the 16-bit CRC character is sent, followed by one or more flag characters. The Transmit Underrun/EOM bit is reset to zero by issuing the Reset Tx Underrun/EOM Latch command in the Command Register.

The SIO begins to send a frame when data is written into the transmit buffer. Between the time the first data byte is written and the end of the message, the Reset Tx Underrun/EOM Latch command must be issued. The Transmit Underrun/EOM status bit will then be in the reset state at the end of the message (when underrun occurs), and CRC characters will automatically be sent. The transmission of the first CRC bit set the Transmit Underrun/EOM status bit to a one and generates an External/Status interrupt. Also, while CRC is being sent, the Tx Buffer Empty bit in Status Register 0 is reset to indicate that the transmit shift register is full of CRC data. When CRC has been completely sent, the Tx Buffer Empty status bit is set, and a Transmit Interrupt is generated to indicate that another message may begin. This interrupt occurs because CRC has been sent, and a flag has been loaded into the shift register. If no more messages are to be sent, the program can terminate transmission by disabling the transmitter.

Although there is no restriction as to when the Transmit Underrun/EOM bit can be reset within a message, it is usually reset after the first data character (secondary address field) is sent to the SIO. By resetting the status bit early in the message, the CPU has additional time (16 bits to CRC) to recognize if an unintentional transmit underrun situation has occured and to respond with an Abort command. Issuing the Abort command stops the flags from going on the line prematurely and eliminates the possibility of the receiver accepting the frame as valid data. This situation can happen if, at the receiving end, the data pattern immediately preceding the automatic flag insertion matches the CRC checker, giving a false CRC check result.

6.6.1.6 - CRC generation

The CRC generator must be reset to all ones at the beginning of each frame before CRC accumulation can begin. Actual accumulation begins on the first data character (address field) loaded into the transmit buffer. The Tx CRC Enable bit in the Transmit Control Register should be set to a one before the first character is loaded into the transmit buffer. In SDLC mode, all characters between the opening and the closing flags are included in CRC accumulation. The output of the CRC generator is inverted before it is transmitted.

6.6.1.7 - Transmit termination

The normal sequence at the end of a frame is :

A Transmit Interrupt occurs when the last data character to the transmit buffer is downloaded into the transmit shift register. This interrupt may be cleared by issuing a Reset Tx Interrupt Pending command.

An External/Status Interrupt occurs when the first bit of the CRC character is transmitted. This interrupt condition should first be tested to see if the interrupt was caused by the Tx Underrun/EOM bit going High and then reset by issuing a Reset External/Status Interrupts command.

A Transmit Interrupt occurs when the first bit of the flag is transmitted. This interrupt may be cleared by issuing a Reset Tx Interrupt Pending command, by loading the first character of the next message, or by disabling the transmitter.

If the transmitter is disabled while a character is being sent, that character (data or flag) is sent in the normal fashion but is followed by a marking line rather than CRC or more flag characters. If CRC characters are being sent at the time the transmitter is disabled, all 16 bits will be transmitted, followed by a marking line ; however, flags are sent in place of CRC. A character in the buffer when the transmitter is disabled remains in the buffer.

6.6.2 - SDLC receive

6.6.2.1 - Initialization

The receiver is enabled only after all of the receive parameters are initialized. After the Receiver Enable bit in the Receiver Control Register is set to a one, the receiver will be in the Hunt phase and will remain in this phase until the first flag is

received. While in the SDLC mode, the receiver never re-enters the Hunt phase, unless specifically instructed to do so by the program or when an Abort character is detected in the incomming data stream.

6.6.2.2 - Receiver characteristics

The receiver may be programmed to assemble five to eight data bits into a character. The character is right-justified in the shift register and transferred to the receive data FIFO. All data transfers to the FIFO are in 8-bit groups. When the character length programmed is less than eight bits, the most significant bit(s) transferred with a character, will be the least-significant bit(s) of the next character. The character length programmed may be changed on the fly during the reception of a frame ; however, care must be taken to assure that the change is effective, before the number of bits specified for the character length has been assembled.

The address field in the SDLC frame is defined as an 8-bit field. When the Address Search Mode is selected, the receiver will compare the 8-bit character following the flag (first non-flag character) against the address programmed in Sync Word Register 1 or the hardwired global address (11111111). When the address field of the SDLC frame matches either address, data transfer will begin with the address character being loaded into the receive data FIFO. If the frame address does not match either address, the receiver will remain idle and continue checking every frame received for an address match. The address comparison is always done on the first eight bits following a flag, regardless of the bits per character programmed.

The SIO receiver is capable of matching only one address character. Once a match occurs, all data is transferred to the receive data FIFO at the programmed bits per character rate. If SDLC extended address field recognition is used (two or more address characters), the CPU program must be capable of determining whether or not the frame has a correct address field. If the correct address field is not received, the Hunt bit can be set to suspend reception and start searching for the next frame. The control field of and SDLC frame is transparent to the SIO ; it is transferred to the data FIFO as a data character. All extra zeros, inserted in the data stream by the transmitter, are automatically deleted in the receiver.

6.6.2.3 - Data transfer and status monitoring

After receipt of a valid flag, the assembled characters are transferred to the receive data FIFO, and the status information for each character is transferred to the receive error FIFO. The following four modes are available to transfer the received data and its associated status to the CPU.

6.6.2.4 - No receiver interrupts enabled

This mode is used for polling operations or for off-line conditions. When transfering data, using a polling routine, the Rx Character Available bit in Status Register 0 should be checked to determine whether or not a receive character is available for transfer. Only when a character is available should the receive buffer and Status Register 1 be read. The Rx Character Available bit is set to a one every time a character is shifted to the top of the receive data FIFO. This bit is reset when the receive buffer is read.

6.6.2.5 - Interrupt on first character only

This interrupt mode is normally used to start a DMA transfer routine, or in some cases, a polling loop. The SIO will generate an interrupt the first time a character is shifted to the top of the receive data FIFO after this mode is selected or reinitialized. An interrupt will be generated thereafter only if a Special Receive Condition is detected. This mode is reinitialized with the Enable Interrupt On Next Character command. Parity Errors do not cause interrupts in this mode but a Receive Overun Error or an End Of Frame condition will.

6.6.2.6 - Interrupt on every character

This interrupt mode will generate a Receiver Interrupt every time a character is shifted to the top of the receive data FIFO. A Special Receive Condition interrupt on a Parity error is optional in this mode.

6.6.2.7 - Special receive condition interrupt

The special condition interrupt mode is not an Interrupt mode, as such, but works in conjunction with the interrupt On Every Character or Interrupt On First Character Only modes. When the Status Affects Vector bit in either channel is set, a Special Receive Condition will modify the Receive Interrupt vector to signal the CPU of the special condition. Receive Overrun Error, Parity Error, and End Of Frame are the Special Receive Conditions in SDLC mode. The Overrun and Parity error status bit in Status Register 1 are latched when they occur, the End Of Frame bit is not latched. The two bits that are latched will remain latched and will generate a Special Receive Condition Interrupt at every character available time until an Error Reset command is issued. Since the two status bits are latched, the error status in Status Register 1, when read, will reflect an error in the current word in the receive buffer, in addition to any Parity or Overrun errors received since the last Error Reset command.

6.6.2.8 - SDLC receive CRC checking

Control of the receiver CRC checker is automatic. It is reset by the leading flag, and CRC is calculated up to the final flag. The byte that has the End Of Frame bit set is the byte that contains the result of the CRC check. If the CRC/Framing Error bit is not set (zero), the CRC indicates a valid received message. A special check sequence is used for the SDLC check, because the transmitted CRC character is inverted. The final check must be 0001110100001111. The 2-byte CRC check characters should be read and discarded by the CPU, because the last two bits of the 2-byte SDLC CRC check characters are not transferred to the receive data FIFO due to the internal timing associated with detecting the closing flag.

Unlike Synchronous modes, the logic path in SDLC mode does not have 8-bit delay between the time a character is transferred to the receive data FIFO and the time a character enters the CRC checker. This delayis not needed, because in SDLC, all characters between the opening and closing flags are included in the CRC calculations. When the second CRC character (six bits only) is loaded into the receive buffer CRC calculation is complete.

6.6.2.9 - SDLC receive termination

An SDLC frame is terminated when the closing flag is detected. The detection of the flag sets the End Of Frame bit in Status Register 1 and generates a Special Receive Condition Interrupt. In addition to the End Of Frame bit being set and the results of the CRC check, Status Register 1 have three bits of Residue code valid at this time. The Residue bit indicates the boundary between the CRC check bits and the I-field bits in the frame. A detailed description of the Residue code bits is given in the Register Description section, under Status Register 1.

Any frame can be prematurely aborted by an Abort sequence. Aborts are detected if seven or more continuous ones occur in the received data stream. This condition will cause an External/Status Interrupt to be generated with the Break/Abort bit in Status Register 0 set. After the Reset External/Status Interrupts command have been issued, a second interrupt will occur when the continuous ones condition has been cleared. This second interrupt can be used to distinguish between the Abort and Idle line condition.

6.7 - Register description

The following setions describe the TS 68564 SIO registers. Each register is detailed in terms of bit configuration, the active states of each bit, their definitions, their functions, and their effects upon the internal hardware and external pins.

6.7.1 - Command register (CMDREG)

This register command and reset functions used in the prorgamming of the SIO. This register is reset to «00H» by a channel or hardware reset. All bits, except Loop Mode, will be read as zeros during a read cycle.

D7	D6	D5	D4	D3	D2	D1	D0
CRC 1	CRC 0	CMD 2	CMD 1	CMD 0			LOOP MODE

6.7.1.1 - D7, D6 : CRC reset codes 1 and 0

CRC 1	CRC 0	
0	0	Null Code (no effect)
0	1	Reset Receiver CRC Checker
1	0	Reset Transmit CRC Generator
1	1	Reset Tx Underrun/End of Message Latch

Null Code. The null code has no effect on the TS 68564 SIO. It is used when writing to the Command Register for some reason other than a CRC Reset.

Reset Receiver CRC Checker. It is necessary in Synchronous modes (except SDLC) to reset the receive CRC circuitery between received messages. The CRC circuitery may be reset by one of the following : disabling the receiver, setting the Enter Hunt Mode bit in the Receiver Control Register, or issuing this Reset command. The CRC circuitery is reset automatically in SDLC mode when the End Of Frame flag is detected. This Reset command will initialize the CRC checker circuit to all ones SDLC mode and all zeros in the other Synchronous modes.

Reset Transmit CRC Generator. This command resets the CRC generator to all ones in the SDLC mode and all zeros in the other Synchronous modes. This command should be issued after the transmitter is enabled but before the first character of a message is loaded in the transmit buffer.

Reset Transmit Underrun/EOM Latch. This command resets the Underrun/EOM latch is the Status Register 0 if the transmitter is enabled. The Underrun/EOM latch controls the transmission of CRC at the end of a message in Synchronous modes. When a transmit underrun occurs and this latch is down, CRC will be append to the end of the transmission.

6.7.1.2 - D5, D4, D3 : Command codes

COMMAND	CMD2	CMD1	CMD0	
0	0	0	0	Null Command (no effect)
1	0	0	1	Send Abort (SDLC Mode)
2	0	1	0	Reset External/Status Interrupts
3	0	1	1	Channel Reset
4	1	0	0	Enable Interrupt On Next Rx Character
5	1	0	1	Reset Tx Interrupt Pending
6	1	1	0	Error Reset
7	1	1	1	Null Command (no effect)

Command 0 (Null). The Null command has no effect on the TS 68564 SIO.

Command 1 (Send Abort). This command is used in the SDLC mode to transmit a sequence of eight to thirteen ones. This command always empties the transmit buffer and sets the Tx Underrun/EOM Latch in Status Register 0 to a one.

Command 2 (Reset External/Status Interrupts). After an External/Status interrupt (a change on a modem line or a Break condition, for example), the upper five bits in Status Register 0 are latched. This command re-enables these bits and allows interrupts to occur again as a result of a status change. Latching the status bits captures short pulses, until the CPU has time to read the change, This command should be issued prior to enabling External/Status Interrupts.

Command 3 (Channel Reset). This command disables both the receiver and transmitter, forces TxD to a marking state («1»), forces the modem control signals high, resets any pending interrupts from this channel, and resets all control registers. See the Reset section in the SIO System Interface Description for a more detailed list. All control registers for the channel must be rewritten after a Channel Reset command.

Command 4 (Enable Interrupt On Next Character). This command is used to reactivate the Receive Interrupt On First Character Only interrupt mode. This command is normally issued after the present message is completed but before the next message has started to be assembled. The next character to enter the receive data FIFO after this command will cause a receiver interrupt request.

Note : If the data FIFO has more than one character stored when this command is issued, the first previously stored character will cause the receiver interrupt request.

Command 5 (Reset Tx Interrupt Pending). When the Transmit Interrupt Enable mode is selected, the transmitter requests an interrupt when the transmit buffer becomes empty. In those cases, where there are no more characters to be sent (at the end of message, for example), issuing this commend resets the pending transmit interrupt and prevents any further transmitter interrupt requests until the next character has been loaded into the transmit buffer or until CRC has been completely sent.

Command 6 (Error Reset). This command resets the upper seven bits in Status Register 1. Anytime a Special Receive Condition exists when Receive Interrupt On First Character Only mode is selected, the data with the special condition is held in the receive data FIFO until this command is issued.

Command 7 (Null). The Null command has no effect on the TS 68564 SIO.

6.7.1.3 - D2, D1 : Not used (read as zeros)

6.7.1.4 - D0 : Loop mode

When this bit is set to a 1, the transmitter output is connected to the Receveir input and $\overline{TxC}$ is connected to the receiver clock. $\overline{RxC}$ and RxD pins are used by the receiver ; they are bypassed internally. $\overline{RxC}$ may still be used as the baud rate generator output in Loop Mode.

6.7.2 - Mode control register (MODECTL)

The mode Control Register contains control bits that affect both the receiver and the transmitter. This register must be initialized before loading the Interrupt, Tx, and Rx Control Registers, and the Sync Word Registers. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
CLOCK RATE 1	CLOCK RATE 0	SYNC MODE 1	SYNC MODE 0	STOP BITS 1	STOP BITS 0	PARITY E/O	PARITY ON/OFF

6.7.2.1 - D7, D6 : Clock rate 1 and 0

These bits specify the multiplier between the input shift clock rates ($\overline{TxC}$ and $\overline{RxC}$) and data rate. The same multiplier is used for both the transmitter and receiver, although the input clock rates may be different. In x16, x32, and x64 clock modes, the receiver start bit detection logic is enabled ; therefore, for Synchronous modes, the x1 clock rate must be specified. Any clock rate may be specified for Asynchronous mode ; however, if the x1 clock rate is selected, synchronization between the receive data and the receive clock must be accomplished externally.

CLOCK RATE 1	CLOCK RATE 0	MULTIPLIER	
0	0	x1	Clock Rate = Data Rate
0	1	x16	Clock Rate = 16 x Data Rate
1	0	x32	Clock Rate = 32 x Data Rate
1	1	x64	Clock Rate = 64 x Data Rate

6.7.2.2 - D5, D4 : Sync modes 1 and 0

These bits select the various options for character synchronization. These bits are ignored, unless Sync modes is selected in the Stop Bits field of this register.

SYNC MODE 1	SYNC MODE 0	
0	0	8-bit programmed sync
0	1	16-bit programmed sync
1	0	SDLC mode (01111110 flag pattern)
1	1	External Sync mode

6.7.2.3 - D3, D2 : Stop bits 1 and 0

These bits determinate the number of stop bits added to each asynchronous character that is transmitted. The receiver always checks for one stop bit in Asynchronous mode. A special code (00) signifies that a Synchronous mode is to be selected. 1 1/2 stop bits is not allowed if x1 clock rate is selected, because it will lock up the transmitter.

STOP BIT 1	STOP BIT 0	
0	0	Sync modes
0	1	1 stop bit per character
1	0	1 1/2 stop bits per character
1	1	2 stop bits per character

6.7.2.4 - D1 : Parity even/odd

If the Parity Enable is set, this bit determines whether parity is checked as even or as odd. (1 = even, 0 = odd). This bit is ignored if the Parity Enable is reset.

6.7.2.5 - D0 : Parity enable

If this bit is set to a one, additional bit position beyond those specified in the bits/character control field is added to the transmitted data and is excepted in the receive data. The received parity bit is transferred to the CPU as part of the data character, unless eight bits per character is selected in the Receiver Control Register.

6.7.3 - Interrupt control register (INTCTL)

This register contains the control bits for the various interrupt modes and the DMA handshaking signals. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
CRC 16/ SDLC	Tx RDY ENABLE	Rx RDY ENABLE	Rx INT MODE 1	Rx INT MODE 0	STATUS AFFECTS	Tx INT ENABLE	EXT INT ENABLE

6.7.3.1 - D7 : CRC-16/SDLC-CRC

This bit selects the CRC polynomial used by both the transmitter and receiver. When set to a one, the CRC-16 polynomial ($x^{16} + x^{15} + x^2 + 1$) is used ; when reset to a zero, the SDLC-CRC polynomial ($x^{16} + x^{12} + x^5 + 1$) is used. If the SDLC mode is selected, the CRC generator and checker are preset to all ones and a special check sequence is used. The SDLC-CRC polynomial must be selected in SDLC mode. Failure to do so will result in receiver errors. When a Synchronous mode, other than SDLC, is selected, the CRC generator and checker are preset to all zeros (for both polynomials). This bit must be programmed before CRC is enabled in the receiver and transmitter control registers, to assure valid CRC generation and checking. This bit is ignored in Asynchronous modes.

6.7.3.2 - D6 : Tx ready enable

When this bit is set to a one, the $\overline{\text{TxRDY}}$ output pin will pulse Low for three clock cycles (CLK) when the transmit buffer becomes empty. When this bit is zero, the $\overline{\text{TxRDY}}$ pin is held High.

6.7.3.3 - D5 : Rx Ready Enable

When this bit is set to a one, the $\overline{\text{RxRDY}}$ output pin will pulse Low for three clock cycles (CLK) when a character is available in the receive buffer. If a Special Receive Condition is detected when the Receive Interrupt On First Character Only interrupt mode is selected, the $\overline{\text{RxRDY}}$ pin will not became active ; instead, a Special Receive Condition interrupt will be generated. When this bit is a zero, the $\overline{\text{RxRDY}}$ pin will be held High.

6.7.3.4 - D4,D3 : Receive interrupt modes 1 and 0

Together, these two bits specify the various character available conditions that will cause interrupt requests. When receiver interrupts are enabled, a Special Receive Condition can cause an interrupt request and modify the interrupt vector. Special Receive Conditions are : Rx Overrun Error, Framing Error (in async mode), End Of Frame (in SDLC mode), and Parity Error (when selected). The Rx Overrun Error and the Parity Error conditions are latched in Status Register 1 when they occur ; they are cleared by an Error Reset command (Command 4) or by hardware or channel reset.

Rx INT MODE 1	Rx INT MODE 0	
0	0	Receive Interrupts Disabled
0	1	Receive Interrupt On First Character Only
1	0	Interrupt On All Receive Characters - parity error is a Special Receive Condition
1	1	Interrupt On All Receive Characters - parity error is nos a Special Receive Condition

Receive Interrupts Disabled. This mode prevents the receiver from generating an interrupt request and clears any pending receiver interrupts. If a character is available in the receiver data FIFO, or if a Special Receive Condition exists before or during the time receiver interrupts are disabled, and receiver interrupts are then enabled without clearing these conditions, an interrupt request will immediately be generated.

Receive Interrupt On First Character Only. The receiver requests an interrupt in this mode on the first available character (or stored FIFO character), or on a Special Receive Condition. If a Special Receive Condition occurs, the data with the special condition is held in the receive data FIFO until an Error Reset command (Command 6) is issued.

The Receive Interrupt On First Character Only mode can be enabled by the Enable Interrupt On Next Rx Character command (Command 4). If this interrupt mode was terminated by a Special Receive Condition, the Error Reset command must be issued, before Command 4, for proper operation to resume.

Interrupt On All Receive Characters. This mode allows an interrupt for every character received (or character in the receive data FIFO) and provides a unique vector (if Status Affects Vector is enabled) when a Special Receive Condition exists. When the interrupt request is due to a special condition, the data containing that condition is not held in the receive data FIFO.

6.7.3.5 - D2 : Status affects vector

When this bit is zero, the value programmed into the Vector Register is returned during a read cycle or an interrupt acknowledge cycle. If the Vector Register has not been programmed following a hardware reset, then «0FH» is returned.

Whent this bit is a one, the vector returned during a read cycle or an interrupt acknowledge cycle is variable. The variable field returned depends on the highest-priority pending interrupt at the start of the cycle.

The Status Affects Vector control bits from both channels are logical «or» ed together ; therefore, if either is programmed to a one, its operation affects both channels. This is the only control bit that functions in this manner on the TS 68564.

V2	V1	0	INTERRUPT CONDITION
0	0	0	Ch B Transmit Buffer Empty
0	0	1	Ch B External/Status Change
0	1	0	Ch B Receive Character Available
0	1	1	Ch B Special Receive Condition*
1	0	0	Ch A Transmit Buffer Empty
1	0	1	Ch A External/Status Change
1	1	0	Ch A Receive Character Available
1	1	1	Ch A Special Receive Condition*

* Special Receive Conditions : Parity Error, Rx Overrun, Framing Error (Async), End Of Frame (SDLC).

6.7.3.6 - D1 : Transmit interrupt enable

When this bit is set to a one, the transmitter will request an interrupt whenever the transmit buffer becomes empty. When this bit is zero, no transmitter interrupts will be requested.

6.7.3.7 - D0 : External/status interrupt enable

When this bit is set to a one, an interrupt will be requested by the external/status logic on any of the following occurences : a transition (high-to-low or low-to-high) on the DCD, CTS, or SYNC input pins, a break/abort condition that has been detected and terminated or at the beginning of CRC transmission when the Transmit Underrun/EOM latch in Status Register 0 becomes set. When this bit is zero, no External/Status interrupts will occur.

If this bit is set when an External/Status condition is pending, an interrupt will be requested. If is recommended that a Reset External/Status Interrupts command (Command 2 in the Command Register) be issued prior to enabling External/Status interrupts.

6.7.4 - Sync word register (SYNC 1)

This register is programmed to contain the transmit sync character in the Monosync mode, the first eight bits of the 16-bit sync character in the Bisync mode, or the transmit sync character in the External Sync mode. This register is not used in Asynchronous mode. In the SDLC mode, this register is programmed to contain the secondary address field used to compare against the address field of the SDLC frame. The SIO does not automatically transmit the station address at the beginning of a reponse frame. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
SYNC/ SDLC 7	SYNC/ SDLC 6	SYNC/ SDLC 5	SYNC/ SDLC 4	SYNC/ SDLC 3	SYNC/ SDLC 2	SYNC/ SDLC 1	SYNC/ SDLC 0

6.7.5 - Sync word register 2 (SYNC 2)

This register is programmed to contain the receive sync character in the Monosync mode, the first eight bits of the 16-bit sync character in the Bisync mode, or a flag character (01111110) in the SDLC mode. This register is not used in the External Sync mode and the Asynchronous mode. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
SYNC/ SDLC 15	SYNC/ SDLC 14	SYNC/ SDLC 13	SYNC/ SDLC 12	SYNC/ SDLC 11	SYNC/ SDLC 10	SYNC/ SDLC 9	SYNC/ SDLC 8

6.7.6 - Receiver control register (RCVCTL)

This register contains the controls bits and parameters for the receiver logic. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
Rx BITS CHAR 1	Rx BITS CHAR 0	Rx AUTO ENABLES	HUNT MODE	Rx CRC ENABLE	ADDRESS SEARCH	STRIP SYNC	Rx ENABLE

The state of these two bits determines the number of bits to be assembled as a character in the received serial data stream. If Parity is enabled, one additional bit will be added to each character. The number of bits per character can be changed while a character is being assembled but only before the number of bits currently programmed is reached. All data is right-justified in the shift registers and transferred to the receive data FIFO in 8-bit groups.

In Asynchronous mode, transfers are made at character boundaries, and all unused bits of character are set to a one. In Synchronous modes and SDLC mode, an 8-bit segment of the serial data stream is transferred to the data FIFO when the internal counter reaches the number of bits per character programmed. For less than eight bits per character, no parity, the MSB bit(s) of the first transfer will be the LSB bit(s) of the next transfer.

Rx BITS CHAR 1	Rx BITS CHAR 0	BITS/CHARACTER (NO PARITY)	BITS/CHARACTER (PARITY)
0	0	5	6
0	1	6	7
1	0	7	8
1	1	8	9

6.7.6.2 - D5 : Receiver auto enables

When this bit is set to a one, and the Receiver Enable bit is also set, a Low on the $\overline{DCD}$ input pin becomes the enable for the receiver. When this bit is zero, the $\overline{DCD}$ pin is simply an input to the SIO, and its status is dislayed in status register 0.

6.7.6.3 - D4 : Enter hunt mode

This bit, when written to a one, rearms the receiver synchronization logic and forces the comparison of the received bit stream to the contents of Sync Word Register 1 and/or Sync Word Register 2, depending upon which Synchronous mode is selected, until bit synchronization is achieved. The SIO automatically enters the Hunt mode after a channel or hardware reset, after an Abort condition is detected, or when the receiver is disabled. When the Hunt mode is entered, the Hunt/Sync bit in Status register 0 is set to a one. When synchronization is achieved, the Hunt/Sync bit is reset to a zero. If External/Status interrupts are enabled, an interrupt request will be generated on both transitions of the Hunt/Sync bit. Enter Hunt Mode has no effect in Asynchronous modes. This bit is not latched and will always be read as a zero.

6.7.6.4 - D3 : Receiver CRC enable

This bit, when set to a one in a Synchronous mode other than SDLC, is used to initiate CRC calculation at the beginning of the last byte transferred from the receiver shift register to the receive data FIFO. This operation occurs independently of the number of bytes in the receive dat FIFO. As long as this bit is set, CRC will be calculated on all characters received (data or sync). When a particular byte is to be excluded from CRC calculation, this bit should be reset to a zero before the next byte is transferred to the receive data FIFO. If this feature is used, care must be taken to ensure that eight bits per character are selected in the receiver because of an inherent eight-bit delay from the receiver shift register to the CRC checker.

When this bit is set to a one in SDLC mode, the SIO will calculate CRC on all bits between the opening and closing flags. There is no delay from the receiver shift register to the CRC checker in SDLC mode. This bit is ignored in Asynchronous modes.

6.7.6.5 - D2 : Address search mode

Setting this bit to a one in SDLC mode forces the comparison of the first non-flag character of a frame with the address programmed in Sync Word Register 1 or the global address (11111111). If a match does not occur, the frame is ignored, and the receiver remains idle until the next frame is detected. No receiver interrupts can occur in this mode, unless there is an address match. This bit is ignored in all modes except SDLC.

6.7.6.6 - D1 : Sync character load inhibit

When this bit is set to a one in any Synchronous mode except SDLC, the SIO compares the byte in Sync Word Register 1 with the byte about to be loaded into the receiver data FIFO. If the two bytes are equal, the load is inhibited, and no receiver interrupt will be generated by this character. CRC calculation is performed on all bytes, whether they are loaded into the data FIFO or not, when the receiver CRC is enabled. Note that the register used in the comparison contains the transmit sync character in Monosync and External sync modes. This bit is ignored in SDLC mode because all flag characters are automatically striped in this mode without performing CRC calculations on them.

If this bit is set to a one in Asynchronous modes, any character received matching the contents of Sync Word Register 1 will not be loaded into the receive data FIFO, and no receiver interrupt will be generated for the character.

6.7.6.7 - D0 : Receive enable

When this bit is set to a one, receiver operation begins if Rx Auto Enables mode is not selected. This bit should be set only after all receiver parameters are established, and the receiver is completely initialized. When this bit is zero, the receiver is disabled ; the receiver CRC checker is reset, and the receiver is in the Hunt mode.

6.7.7 - Transmitter control register (XMTCTL)

This register contains the control bits and parameters for the transmitter logic. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
Tx BITS CHAR 1	Tx BITS CHAR 0	Tx AUTO ENABLES	SEND BREAK	Tx CRC ENABLE	DTR	RTS	Tx ENABLE

6.7.7.1 - D7, D6 : Transmit bits/character 1 and 0

The state of these two bits determine the number of bits in each byte transferred from the transmit buffer to the transmit shift register. All data written to the transmit buffer must be right-justified with the least-significant bits first. The Five Or Less mode allows transmission of one to five bits per character ; however, the CPU should format the data characters as shown. If Parity is enabled, one additional bit per character will be transmitted.

Tx BITS/ CHAR 1	Tx BITS/ CHAR 0	BITS/ CHARACTER (NO PARITY)
0	0	Five or Less
0	1	6
1	0	7
1	1	8

D7	D6	D5	D4	D3	D2	D1	D0	FIVE OR LESS
1	1	1	1	0	0	0	D	Sends one data bit
1	1	1	0	0	0	D	D	Sends two data bits
1	1	0	0	0	D	D	D	Sends three data bits
1	0	0	0	D	D	D	D	Sends four data bits
0	0	0	D	D	D	D	D	Sends five data bits

6.7.7.2 - D5 : Transmit auto enables

When this bit is set to a one, and the Transmit Enable bit is also set, a Low on the $\overline{CTS}$ input pin will enable the transmitter. When this bit is zero, the $\overline{CTS}$ pin is simply an input to the SIO, and the status is displayed in Status Register 0.

6.7.7.3 - D4 : Send break

When set to a one, this bit immediately forces the Transmit Data output pin (TxD) to a spacing condition (continuous 0's), regardless of any data being transmitted at the time. This bit functions, whether the transmitter is enabled or not. When this bit is reset to zero, the transmitter is enabled or not. When this bit is reset to zero, the transmitter will continue to send the contents of the transmit shift register. The shift register may contain sync characters, data characters, or all ones.

6.7.7.4 - D3 : Transmitter CRC enable

This bit determines if CRC calculations are performed on a transmitted data character. If this bit is a one at the time a character is loaded from the transmit buffer to the transmit shift register, CRC is calculated on the character. CRC is not calculated on any automatically inserted sync character. CRC is not automatically append to the end of a message unless this bit is set, and the Transmit Underrun/EOM status bit in Status Register 0 is reset when a Transmit Underrun condition occurs. If this bit is a zero when a character is loaded from the transmit buffer to the transmit shift register, CRC is calculated on the character. CRC is not automatically appended to the end of a message unless this bit is set, and the Transmit Underrun/EOM status bit in Status Register 0 is reset when a Transmit Underrun condition occurs. If this bit is a zero when a character is loaded from the transmit buffer into zero when a character is loaded from the transmit buffer into the transmit shift register, no CRC calculations are performed on the character. This bit is ignored in Asynchronous modes.

6.7.7.5 - D2 : Data terminal ready ($\overline{DTR}$)

This is the control bit for the $\overline{DTR}$ output pin. When this bit is set to a one, the $\overline{DTR}$ pin goes Low ; when this bit is reset to a zero, the $\overline{DTR}$ goes High.

6.7.7.6 - D1 : Request to send ($\overline{RTS}$)

This is the control bit for the $\overline{RTS}$ output pin. In Synchronous modes, when this bit is set to a one, the $\overline{RTS}$ pin goes Low ; when this bit is reset to a zero, the $\overline{RTS}$ pin goes High. In Asynchronous modes, when this bit is reset, the $\overline{RTS}$ pin goes Low ; when this bit is reset, the $\overline{RTS}$ pin will go High only after all the bits of the character are transmitted, and the transmit buffer is empty.

6.7.7.7 - D0 : Transmitter enable

Data is not transmitted until this bit is set to a one, until the Send Break bit is reset and, if Tx Auto enables mode is selected, until the $\overline{CTS}$ pin is Low. To transmit sync or flag characters in Synchronous modes, this bit has to be set when the transmit buffer is empty. Data or sync characters in the process of being transmitted are completely sent if this bit is reset to zero after transmission has started. If this bit is reset during the transmission of a CRC character, sync or flag character are sent instead of the CRC character.

6.7.8 - Status register 0 (STAT 0) read only

This register contains the status of the receive and transmit buffers and the status bits for the five sources of External/Status interrupts.

D7	D6	D5	D4	D3	D2	D1	D0
BREAK/ ABORT	UNDERRUN /EOM	CTS	HUNT/ SYNC	DCD	Tx BUFR EMPTY	INTERPT PENDING	Rx CHAR AVAIL

6.7.8.1 - D7 : Break/abort

This bit is reset by a channel or hardware reset. In Asynchronous modes, this bit is set when a Break sequence (null character plus framing error) is detected in the received data stream. An External/Status Interrupt command (Command 2) to the SIO, so the break detection logic can recognize the termination of the Break sequence.

The Break/Abort bit is reset to a zero when the termination of the Break sequence is detected in the incoming data stream. The termination of the Break sequence also causes the generation of an External/Status Interrupt. Command 2 must be issued to enable the break detection logic to look for the next Break sequence. A single extraneous null character is present in the receiver after the termination of a break ; it should be read and discarded.

In SDLC mode, this bit is set by the detection of an Abort sequence (seven or more ones) in the received data stream. The External/Status Interrupt is handled the same way as in the case of a Break sequence. The Break/Abort bit is not used in the other Synchronous modes.

6.7.8.2 - D6 : Transmit underrun/EOM

This bit is set to a one following a hardware or channel reset, when the transmitter is disabled or when a Send Abort command (Command 1) is issued. This bit can only be reset by the Reset Transmit Underrun/EOM Latch command in the Command Register. This bit is used to control the transmission of CRC at the end of a message in Synchronous modes. When a transmit underrun condition occurs and this bit is low, CRC will be appended to the end of the transmission, and this bit will be set. Only the 0-1 transition of this bit causes an External/Status interrupt, when enabled. This bit is not used in Asynchronous modes.

6.7.8.3 - D5 : Clear to send ($\overline{CTS}$)

This bit indicates the inverted state of the $\overline{CTS}$ input pin at the time of the last change of any of the five External/Status bits. Any transition of the $\overline{CTS}$ input causes the $\overline{CTS}$ bit to be latched and generates an External/Status interrupt request, if enabled. To read the current state of the $\overline{SYNC}$ pin, this bit must be read immediately following a Reset External/Status Interrupts command (Command 2).

6.7.8.4 - D4 : Hunt/Sync

In Asynchronous modes, this bit indicates the inverted state of the $\overline{SYNC}$ input pin at the time of the last change of any of the five External/Status bits. Any transition of the $\overline{SYNC}$ input causes the Hunt/Sync bit to be latched and generates an External/Status interrupt request, if enabled. To read the current state if the $\overline{SYNC}$ pin, this bit must be read immediately following a Reset External/Status Interrupt command (Command 2).

In External sync mode, the $\overline{SYNC}$ pin is used by external logic to signal character synchronization. When synchronization is achieved, the $\overline{SYNC}$ pin is driven Low on the second rising edge of the Receive Clock (RxC) on which the last bit of the sync character was received. Once the $\overline{SYNC}$ pin is low, it should be held Low until the end of the message and then driven back High. Both transitions on the $\overline{SYNC}$ pin cause External/Status interrupt requests, if enabled. The inverted state of the $\overline{SYNC}$ pin is indicated by this bit.

In Monosync, Bisync, and SDLC modes, this bit indicates when then receiver is in the Hunt mode. This bit is set to a one following a hardware or channel reset, after the Enter Hunt Mode bit is written High, when the receiver is disavled, or when an Abort sequence (SDLC mode) is detected. This bit will remain in this state until character synchronization is achieved. External/Status interrupt requests will be generated on both transitions of the Hunt/Sync bit.

5

6.7.8.5 - D3 : Data carrier defect ($\overline{DCD}$)

This bit indicates the inverted state of the $\overline{DCD}$ input pin at the time of the last change of any of the five External/Status bits. Any transition of the $\overline{DCD}$ input causes the $\overline{DCD}$ bit to be latched and generates an External/Status interrupt request, if enabled. To read the current state of the $\overline{DCD}$ pin, this bit must be read immediately following a Reset External/Status Interrupts command (Command 2).

6.7.8.6 - D2 : Transmit buffer empty

This bit is set to a one, when the transmit buffer becomes empty, and when the last CRC bit is transmitted in Synchronous or SDLC modes. This bit is reset when the transmit buffer is loaded or while the CRC character is being sent is Synchronous or SDLC modes. This bit is set to a one following a hardware or channel reset.

6.7.8.7 - D1 : Interrupt pending

Any interrupt condition, pending in the interrupt control logic for this channel, will set this bit to a one. This bit is reset to a zero by a hardware channel reset, or when all the interrupt conditions are cleared.

6.7.8.8 - D0 : Receive character available

This bit is set to a one when a character becomes available in the receive data FIFO. This bit is reset to zero when the receive dat FIFO (receive buffer) is read, or by a hardware or channel reset.

6.7.9 - Status register 1 (STAT 1) read only

This register contains the Special Receive Condition status bits and the Residue codes for the I-field in the SDLC receive mode. The All Sent bit is set High, and all other bits are reset to a Low by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
END OF FRAME	CRC/FRAME ERROR	Rx OVER-RUN ERR	PARITY ERROR	RESIDUE CODE 2	RESIDUE CODE 1	RESIDUE CODE 0	ALL SENT

6.7.9.1 - D7 : End of frame (SDLC)

This bit is used only in SDLC mode. When set to a one, this bit indicates that a valid closing flag has been received and that the CRC/Framing Error bit and Residue codes are valid. If receiver interrupts are enabled, a Special Receive Condition interrupt will also be generated. This bit can be reset by issuing an Error Reset command (Command 6). This bit is also updated by the first character of the following frame, this bit is a zero in all modes except for SDLC.

6.7.9.2 - D6 : CRC/framing error

In Asynchronous modes, if a Framing Error occurs, this bit is set to a one for the receive character in which the framing error occured. Whent this bit is set to a one, a Special error occured. When this bit is set to a one, a Special Receive Condition interrupt will be requested, if receiver interrupts are enabled. Detection of a Framing Error adds an additional one-half bit time to the character time, so that the Framing Error is not interpreted as a new start bit.

In Synchronous and SDLC modes, this bit indicates the result of comparing the received CRC value to the appropriate check value. A zero indicates that a match has occured. This bit is usually set since most bit combinations results in a non-zero CRC, except for a correctly completed message. Receiver interrupts are not requested by the CRC Error bit.

6.7.9.3 - D5 : Receive overrun error

This bit indicates that the receive data FIFO has overflowed Only the character that has been written over is flag with this error. When the character is read, the error condition is latched until reset by the Error Reset command (Command 6). If receiver interrupts are enabled, the overrun character and all subsequent characters received, until the Error Reset command is issued, will generate a Special Receive Condition interrupt request.

6.7.9.4 - D4 : Parity error

When parity is enabled, this bit is set to a one for those characters whose parity does not match the programmed sence (even/odd). This bit is latched so that once an error occurs, it remains set until the Error Reset command (Command 6) is issued. If parity is a Special Receive Condition, a Parity Error will cause a Special Receive Condition interrupt request on the character containing the error and on all subsequent characters until the Error Reset command is issued.

6.9.7.5 - D3, D2, D1 : Residue codes 2, 1 and 0

In those cases of the SDLC receive mode, where the I-field is not an integral multiple of the character length, these three bits indicate the length of the residual I-fiels read in the previous bytes. These codes are meaningful only for the transfer in which the End of Frame bit is set. This field is set to 000 by a channel or hardware reset and can leave this state only if SDLC mode is selected, and a character is received.

For Eight Bits Per Character

RESIDUE CODE 2	RESIDUE CODE 1	RESIDUE CODE 0	I-FIELD BITS IN PREVIOUS BYTE	I-FIELD BITS IN SECOND PREVIOUS BYTE
1	0	0	0	3
0	1	0	0	4
1	1	0	0	5
0	0	1	0	6
1	0	1	0	7
0	1	1	0	8
1	1	1	1	8
0	0	0	2	8

I-Field bits are right-justified in all cases

If a receive character length, different from eight bits, is used for the I-field, a table similar to the previous one may be constructed for each different character length. For no residue (that is, the last character boundary coincides with the boundary of the I-field and CRC field), the Residue codes are as follows :

BITS PER CHARACTER	RESIDUE CODE 2	RESIDUE CODE 1	RESIDUE CODE 0
8 bits per Character	0	1	1
7 bits per Character	0	0	0
6 bits per Character	0	1	0
5 bits per Character	0	0	1

6.7.9.6 - D0 : All sent

This bit is only active in Asynchronous modes ; it is always High in Synchronous or SDLC modes. This bit is Low while the transmitter is sending characters ; it will go High only after all the bits of the character are transmitted, and the transmit buffer is empty.

6.7.10 - Data register (DATARG)

The Data Register is actually two separate registers ; a write only register that is the Transmit Buffer, and a read only register that is the Receive Buffer. The Receiver Buffer is also the top register of a three register stack called the receive data FIFO. The Data Register is not affected by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0

6.7.11 - Time constant register (TCREG)

This register contains the time constant used by the down counter in the baud rate generator. The time constant may be changed at any time, but the new value does not take effect until the next time the time constant is loaded into the down counter. It is recommended that the BRG be disabled before writing to this register, as no attempt was made to synchronize the loading of new time constant with the clock used to drive the BRG. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

6.7.12 - Baud rate generator control register (BRGCTL)

This register contains the control bits used to program the baud rate generator and to select the BRG output mode. This register is reset to «00H» by a channel or hardware reset.

D7	D6	D5	D4	D3	D2	D1	D0
				RxC INT/EXT	TxC INT/EXT	DIVIDE BY 64/4	BRG ENABLE

5

6.7.12.1 - D7, D6, D5, D4 : Not used (read as zeros)

6.7.12.2 - D3 : Receiver clock, internal/external

This bit determines the direction of the $\overline{RxC}$ pin. When this bit is set to a one, the $\overline{RxC}$ pin is the output of the baud rate generator. If this bit is a zero, the $\overline{RxC}$ pin is an input, and an external source must supply the receiver clock. The receiver clock is always the signal on the $\overline{RxC}$ pin, except in Loop Mode, when the transmitter clock is connected internally to the receiver clock.

6.7.12.3 - D2 : Transmitter clock, internal/external

This bit determines the direction of the $\overline{TxC}$ pin. When this bit is set to a one, the $\overline{TxC}$ pin is the output of the baud rate generator. If this bit is a zero, the $\overline{TxC}$ pin is an input, and an external source must supply the transmitter clock. The transmit clock is always the signal on the $\overline{TxC}$ pin.

6.7.12.4 - D1 : Divide by 64/4

This bit specified the minimum BRG input clock cycles to output clock cycle. This minimum occurs when the Time Constant Register is loaded with a «01H» value. When this bit is set to a one, 64 input clocks are required for every output clock. When this bit is a zero, four input clocks are required for every output clock.

6.7.12.5 - D0 : Baud rate generator enable

This bit controls the operation of the baud rate generator. When this bit is set to a one, the BRG will start counting down from the value left in the down counter when this bit was last reset to zero. If the Time Constant Register is loaded while this bit is reset, the new time constant value is loaded immediately into the down counter. The baud rate generator is disabled from counting when this bit is reset.

6.7.13 - Interrupt vector register (VECRG)

This register is used to hold a vector that is passed to the CPU during an interrupt acknowledge cycle. This register can also be accessed through a read/write cycle. If the Status Affects Vector bit in the Interrupt Control Register is disabled, the value programmed into the Vector Register will be passed to the CPU during an interrupt acknowledge cycle or read cycle. If the Status Affects Vector bit in either channel is enabled, the lower three bits of this register are modified, according to the table listed in the Interrupt Control Register description. With Status Affects Vector on, and no interrupt pending in the SIO, the lower three bits will be read as 011. Only one Vector Register exists in the SIO, but it can be accessed through either channel. This register is reset to «0FH» by a hardware reset only.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2 ★	V1 ★	V0 ★
★ Variable if Status Affects Vectors is enabled.							

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TMS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

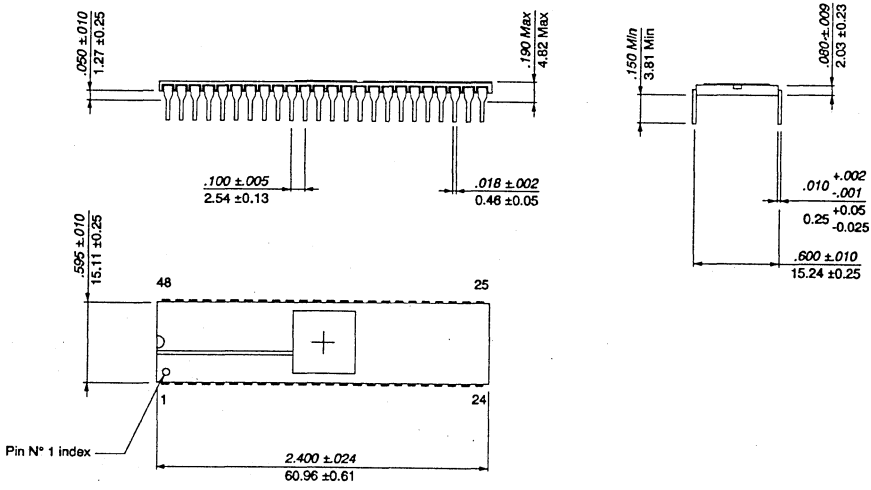
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

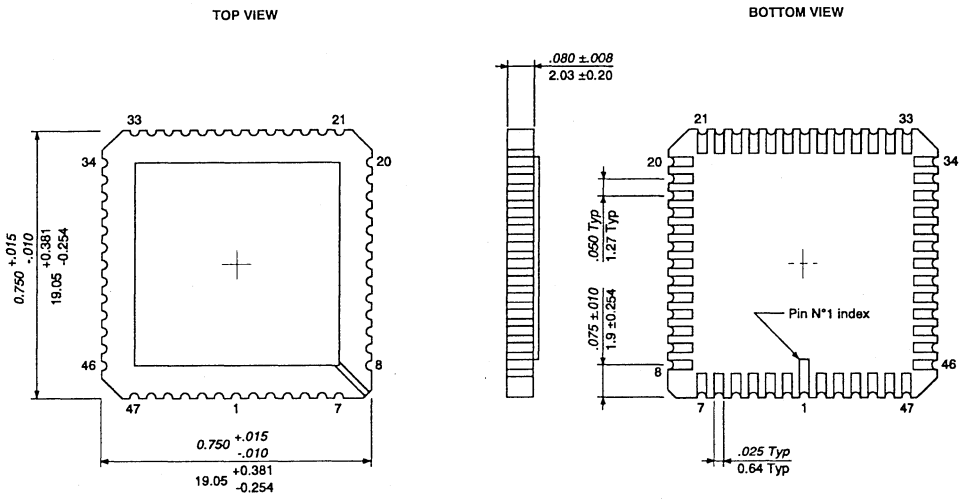
a) Devices should be handled on benches with conductive and grounded surfaces.
b) Ground test equipement, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent if practical.

9 · PACKAGE MECHANICAL DATA

9.1 · 48 Pins - Ceramic side brazed

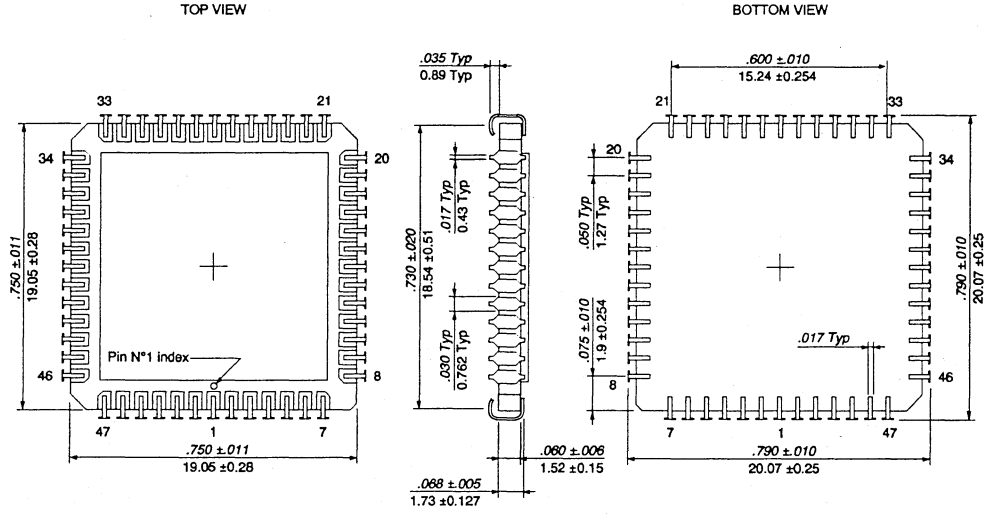


9.2 - 52 Pins - Leadless ceramic chip carrier



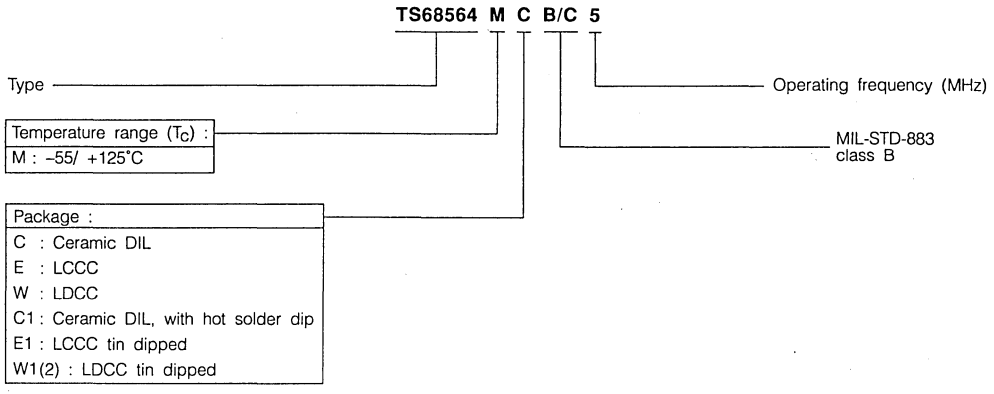
5

9.3 - 52 Pins - Leaded ceramic chip carrier



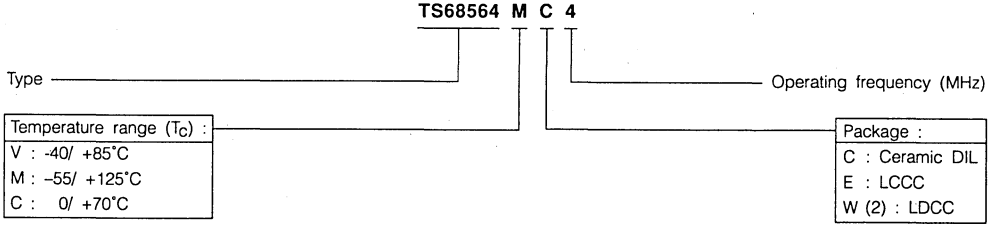
10 - ORDERING INFORMATION

10.1 - MIL-STD-883



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : On request.

10.2 - Standard product



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : On request.

10.3 - Detailed ordering information

10.3.1 - Hi-REL product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68564MCB/C3	MIL-STD-883	DIL 48	– 55 / + 125	3	TCS data sheet
TS 68564MCB/C4	MIL-STD-883	DIL 48	– 55 / + 125	4	TCS data sheet
TS 68564MCB/C5	MIL-STD-883	DIL 48	– 55 / + 125	5	TCS data sheet
TS 68564ME1B/C3	MIL-STD-883	LCC 52	– 55 / + 125	3	TCS data sheet
TS 68564ME1B/C4	MIL-STD-883	LCC 52	– 55 / + 125	4	TCS data sheet
TS 68564ME1B/C5	MIL-STD-883	LCC 52	– 55 / + 125	5	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

10.3.2 · Standard product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68564VC3	TCS standard	DIL 48	−40 / +85	3	TCS data sheet
TS 68564VC4	TCS standard	DIL 48	−40 / +85	4	TCS data sheet
TS 68564VC5	TCS standard	DIL 48	−40 / +85	5	TCS data sheet
TS 68564MC3	TCS standard	DIL 48	−55 / +125	3	TCS data sheet
TS 68564MC4	TCS standard	DIL 48	−55 / +125	4	TCS data sheet
TS 68564MC5	TCS standard	DIL 48	−55 / +125	5	TCS data sheet
TS 68564ME3	TCS standard	LCC 52	−55 / +125	3	TCS data sheet
TS 68564ME4	TCS standard	LCC 52	−55 / +125	4	TCS data sheet
TS 68564ME5	TCS standard	LCC 52	−55 / +125	5	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

5

TS 68901

MULTI-FUNCTION PERIPHERAL

DESCRIPTION

The TS 68901 multi-function peripheral (CMFP) is a member of the TS 68000 Family of peripheral. The CMFP directly interfaces to the TS 68000 processor Family via an asynchronous bus structure. Both vectored, non vectored and polled interrupt schemes are supported, with the CMFP providing unique vector number generation for each of its 16 interrupt sources. Additionally, handshake line are provided to facilitate DMAC interfacing.

The TS 68901 performs many of the functions common to most microprocessor-based systems.

By incorporating multiple functions within the CMFP, the system designer retains flexibility while minimizing device count.

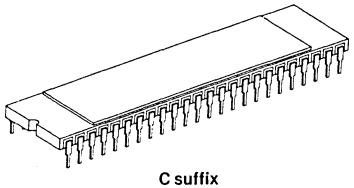
FEATURES

- 8 Input/output pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmables edge selection.
- 16 Source interrupt controller
  - 8 Internal sources
  - 8 external sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
    - Optional In-service status
  - Daisy chaining capability.
- Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
  - Independent clock input
  - Time out output option.
- Single channel USART
  - Full Duplex
  - Asynchronous to 65 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals
  - Modem control
  - Loop back mode.
- 68000 Bus compatible.
- Available in 4 and 5 MHz.
- Military temperature range : 55/ + 125°C.
- See application note.

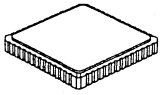
SCREENING / QUALITY

This product is manufactured in full compliance with :

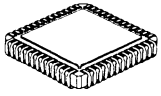
- MIL-STD-883 (class B).
- DESC Drawing 5962-88506.
- TCS STANDARDS.



C suffix
DIL 48
Ceramic Side Brazed package



E suffix
LCCC 52
Leadless Ceramic Chip Carrier



W suffix
LDCC 52 (on request)
Leaded Ceramic Chip Carrier

PIN CONNECTIONS (see § A2)
Ordering information (see chapter 10).

5

SUMMARY

A · GENERAL DESCRIPTION

1 · DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

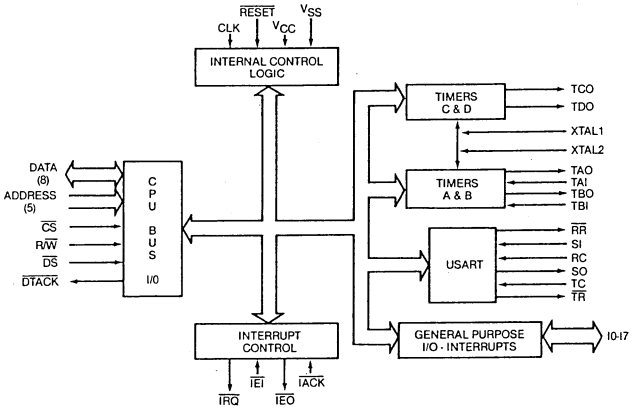


Figure 1 : Functional block diagram.

2 · PIN ASSIGNMENTS

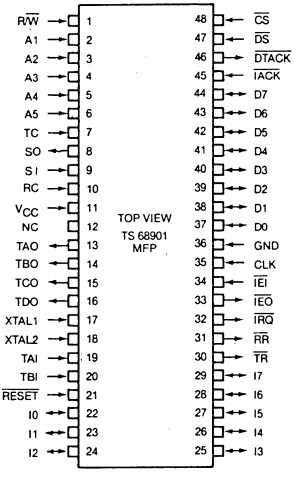


Figure 2.1 : DIL package - C suffix.

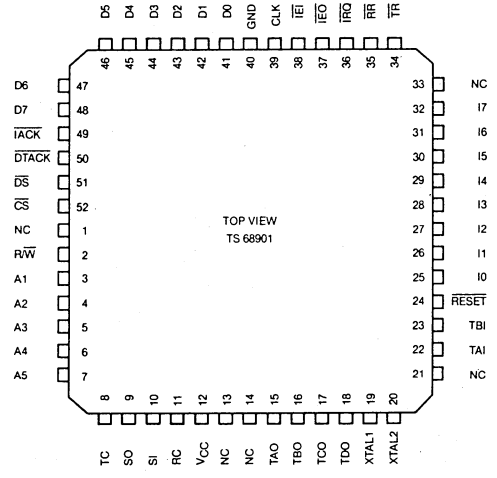


Figure 2.2 : Terminal chip-carrier packages E and W suffix.

3 - TERMINAL DESIGNATIONS OF THE DEVICE

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply	Supply Terminals
V_{SS}*	Power supply	
CS	Chip select	Input
DS	Data strobe	Input
R/W	Read/Write	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
A1 to A15	Address bus	Inputs
D0 to D7	Data bus	Bi-directionnal
CLK	Clock	Input
$\overline{RESET}$	Device Reset	Input
$\overline{IRQ}$	Interrupt Request	Output
$\overline{IACK}$	Interrupt Acknowledge	Input
$\overline{IEI}$	Interrupt Enable In	Input
$\overline{IEO}$	Interrupt Enable Out	Output
I0-I7	General purpose interrupt I/O lines	Bi-directionnal
SO	Serial Output	Output
SI	Serial Input	Input
TC	Transmitter clocks	Input
XTAL1, 2	Timer clock	Input
TAI, TBI	Timer input	Input
TAO, TBO, TCO, TDO	Timer output	Output
RC	Receiver Clock	Input
$\overline{RR}$	Receiver Ready	Output
$\overline{TR}$	Transmitter Ready	Output

* V_{SS} is the reference terminal for the voltage.

4 - PIN DESCRIPTION

GND : Ground.

V_{CC} : +5 Volts (± 5 %).

$\overline{CS}$: Chip Select (input, active low). $\overline{CS}$ is used to select the TS 68901 MFP for accesses to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

$\overline{DS}$: Data Strobe (input, active low). $\overline{DS}$ is used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle.

$\overline{DTACK}$: Data Transfert Acknowledge (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that the data is ready, or that data has been accepted by the TS 68901 MFP.

A1-A5 : Address Bus (inputs). The address bus is used to address one of the internal registers during a read or write cycle.

D0-D7 : Data Bus (bi-directionnal, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.

CLK : Clock (input). This input is used to provide the internal timing for the TS 68901 MFP.

$\overline{RESET}$: Device reset (input, active low). Reset disables the USART receiver and transmitter, stops all timers and forces the timer outputs low, disables all interrupt channels and clears any pending interrupts. The General Purpose Interrupt I/0 lines will be placed in the tri-stated input mode. All internal registers (except the timer, USART data registers, and transmit status register) will be cleared.

$\overline{IRQ}$: Interrupt Request (output, active low, open drain). $\overline{IRQ}$ is asserted when the TS 68901 MFP is requesting an interrupt. $\overline{IRQ}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.

$\overline{IACK}$: Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the TS 68901 MFP that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must no be asserted at the same time.

$\overline{IEI}$: Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the TS 68901 MFP that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the TS 68901 MFP nor another higher priority peripheral is requesting interrupt service.

I0/I7 : General Purpose Interrupt I/0 lines. These lines may be used as interrupt inputs and/or I/0 lines. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

SO : Serial Output. This is the output of the USART transmitter.

SI : Serial Input. This is the input to the USART receiver.

RC : Receiver Clock. This input controls the serial bit rate of the USART receiver.

TC : Transmitter Clock. This input controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready (output, active low). DMA output for receiver, which reflects the same status of Buffer Full in port number 15.

$\overline{TR}$: Transmitter Ready (output, active low). DMA output for transmitter, which reflects the status of Buffer Full in part number 16.

TAO, TBO, TCO, TDO : Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle ; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO be reset (logic «0») by a write to TACR or TBCR respectively.

XTAL1, XTAL2 : Timer Clock inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with a TTL level clock. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float. When using a crystal, external capacitors are required. See figure 6. All chip accesses are independent of the timer clock.

TAI, TBI : Timer A, B inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with I4 and I3 are used for TAI and TBI respectively. Thus, when running a timer in the pulse width measurement mode, I4 or I3 can be used for I/0 only.

5

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the TS 68901 - 4 and 5 MHz, in compliance either with MIL-STD-883 class B rev C or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-PRF-38535 appendix A : general specifications for microcircuits
3) DESC 5962-88506

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1 and 2.2 (§ A).

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 :

- 48 LEAD DIP, style D14
- SQ LCC 52 PINS, style C6
- 52 TERMINAL JCC.

The precise case outlines are described at the end of the specification (chapter 9).

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 2 - Absolute maximum ratings

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in § A.4 of this specification.

Symbol	Characteristics	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	—	−0.3	7.0	V
V_I	Input voltages	—	−0.3	7.0	V
V_O	Output voltage	—	NA	NA	V
V_{OZ}	Off state voltage	—	−0.3	11.0	V
I_o	Output currents	—	NA	NA	mA
I_i	Input currents	—	NA	NA	mA
P_d	Power dissipation	T_{case} = − 55°C	—	1.5	W
		T_{case} = +125°C	—	1.25	W
T_c	Operating temperature	—	−55	+125	°C
T_{stg}	Storage temperature	—	−55	+150	°C
T_j	Junction temperature	—	—	+170	°C
T_{lead}	Lead temperature	Max 5 sec. soldering	—	+270	°C

3.3.2 - Guaranteed characteristics - recommended conditions of use

3.3.2.1 - Guaranteed characteristics

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified in § 3.3.2.2. below.

3.3.2.2 - Recommended conditions of use

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also § 3.3.2.1. above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

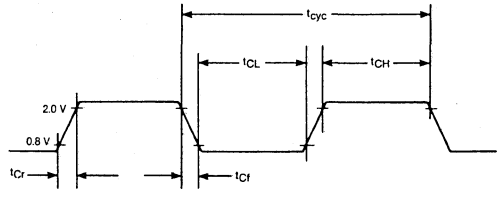


Figure 3 : Clock input timing diagram.

Table 3 - Recommended conditions of use
Unless otherwise stated, all voltages are referenced to the reference terminal (see § A.4).

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	—	4.75	5.25	V
V_{IL}	Low level input voltage	—	−0.3	0.8	V
V_{IH}	High level input voltage	—	2.0	V_{CC}	V
T_{case}	Operating temperature	—	−55	+125	°C
R_L	Value of output load resistance	—	Note	—	Ω
C_L	Output loading capacitance	—	—	Note	pF
$t_{r(c)}$	Clock rise time (see Fig. 3)	—	—	10	ns
t_f	Clock fall time (see Fig. 3)	—	—	10	ns
f_c	Clock frequency (see Fig. 3)	TS 68901-4	—	4	MHz
		TS 68901-5	—	5	MHz
t_{cyc}	Cycle time (see Fig. 3)	TS 68901-4	250	1000	ns
		TS 68901-5	200	1000	ns
$t_{w(CL)}$	Clock pulse width low (see Fig. 3)	TS 68901-4	—	110	ns
		TS 68901-5	—	90	ns
$t_{w(CH)}$	Clock pulse width high (see Fig. 3)	TS 68901-4	—	110	ns
		TS 68901-5	—	90	ns
Note : Load network number 1 and 2 as specified in Fig. 4 and 5 gives the maximum loading of the relevant output.					

5

3.4 - Thermal characteristics

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Table 4

Package	Symbol	Parameter	Value	Unit
DIL 48	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	30	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	11	°C/W
LCCC 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	50	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	11	°C/W
LDCC 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	50	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	11	°C/W

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 5 : Static electrical characteristics for the electrical variants.
- Table 6 : Dynamic electrical characteristics for TS 68901-4 (4 MHz) and TS 68901-5 (5 MHz).

For static characteristics (Table 5), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause 5.4 of this specification (Table 6).

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.2.2 here above.

5.2 · Static characteristics

Table 5 - Static characteristics for all covered models

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 5\,\%$; GND = $0\,V_{DC}$

Test Nbr	Symbol	Characteristic	Method (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
1	I_{CC}	Supply current outputs opens	41	$V_{CC} = 5.25\,V$	all	—	220	mA
2	V_{OL}	Low level output voltage (Except DTACK/)	37	$V_{CC} = 4.75\,V$ $I_{OL} = 2.0\,mA$	all	—	0.5	V
3	V_{OH}	High level output voltage (Except DTACK/)	37	$V_{CC} = 4.75\,V$ $I_{OH} = -120\,\mu A$	all	2.4	—	V
4	I_{OH}	DTACK/ output source current	—	$V_{OUT} = 2.4\,V$	all	—	−400	µA
5	I_{OL}	DTACK/ output sink current	—	$V_{OUT} = 0.5\,V$	all	5.3	—	mA
6	I_{IN}	Input leakage current (0 to 5.25 V)	—	—	all	−10	+10	µA
7	I_{LOH}	Three-state input current in float	—	$V_{OUT} = 2.4$ to V_{CC}	all	—	+10	µA
8	I_{LOL}	Three-state input current in float	—	$V_{OUT} = 0.5$	all	—	−10	µA
9	V_{IH}	High level input voltage for all inputs	—	—	all	2.0	V_{CC} +0.3	V
10	V_{IL}	Low level input voltage for all inputs	—	—	all	−0.3	0.8	V
97	C_{IN}	Input capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C	—	25	pF
					min	—	NA	pF
					max	—	NA	pF
98	C_{OUT}	Output capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C	—	25	pF
					min	—	NA	pF
					max	—	NA	pF
99	V_{ESD}	Internal protection Transient energy rating	See Note 8	See Note 8 5 cycles	25°C	−500	+500	V
					min	NA	NA	V
					max	NA	NA	V

(*) IEC measurement method number unless otherwise stated (see § 5.1).

Refered note is given after Table 6.

5.3 · Dynamic characteristics

Table 6 · Dynamic (switching) characteristics TS 68901-4 and 5 MHz

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 5\,\%$; $GND = 0\,V_{DC}$

Test Nbr	Symbol	Parameter	Method (*)	Test Conditions	Test Temp.	4 MHz Limits		5 MHz Limits		Unit
						Min	Max	Min	Max	
11	t_w (T_{SWH})	$\overline{CS}$/ $\overline{DS}$/ width high (Note 5)	Fig. 7 - 8 Ref. 1	See 5.4.3 (a) to (c) f_C = 4 MHz	all	50	—	35	—	ns
12	t_{su} (T_{RASL})	R/$\overline{W}$/, A1-A5 valid to falling CS/	Fig. 7 - 8 Ref. 2	See test 11	all	0	—	0	—	ns
13	t_{su} (T_{DVCL})	Data valid prior to falling CLK	Fig. 8 Ref. 3	See test 11	all	0	—	0	—	ns
14	t_{su} (T_{SVCL})	$\overline{CS}$/ $\overline{IACK}$/ valid prior to falling CLK (Note 3)	Fig. 7 - 10 Ref. 4	See test 11	all	50	—	45	—	ns
15	t_{phl} (T_{CLDL})	CLK low to $\overline{DTACK}$/ low	Fig. 7 - 8 Ref. 5	See test 11 Load : 3	all	—	220	—	180	ns
16	t_{phl} (T_{SHDH})	$\overline{CS}$/, $\overline{DS}$/ or $\overline{IACK}$/ high to $\overline{DTACK}$/ high	Fig. 7 - 8 Ref. 6	See test 11 Load : 3	all	—	60	—	55	ns
18	t_h (T_{DLDI})	$\overline{DTACK}$/ low to data invalid	Fig. 8 Ref. 8	See test 11	all	20	—	20	—	ns
20	t_h (T_{SHRAI})	$\overline{CS}$/, $\overline{DS}$/ or $\overline{IACK}$/ high to R/$\overline{W}$/ A1-A15 invalid	Fig. 7 - 9 10 Ref. 10	See test 11	all	0	—	0	—	ns
21	t_{phl} t_{plh} (T_{DVSL})	Data valid from $\overline{CS}$/ low (Note 3 and 6)	Fig. 7 - 8 Ref. 10	See test 11	all	—	310	—	260	ns
22	t_{su} (T_{RVDL})	Read data valid to $\overline{DTACK}$/ low valid	Fig. 7 Ref. 12	See test 11 Load : 3	all	50	—	50	—	ns
23	t_h (T_{DLSH})	$\overline{DTACK}$/ low to $\overline{DS}$/ $\overline{CS}$/ or $\overline{IACK}$/ high	Fig. 7 - 9 Ref. 13	See test 11	all	0	—	0	—	ns
24	t_{su} (T_{ILCL})	$\overline{IEI}$/ low to falling CLK/	Fig. 9 - 10 Ref. 14	See test 11	all	50	—	50	—	ns
25	t_{phl} (T_{IVCL})	$\overline{IEO}$/ valid from CLK low (Note 1)	Fig. 9 - 10 Ref. 15	See test 11	all	—	180	—	180	ns
26	t_{phl} t_{plh} (T_{DAVCL})	Data valid from $\overline{CS}$/ low	Fig. 9 Ref. 16	See test 11	all	—	300	—	300	ns
27	t_{plh} (T_{IIIH})	$\overline{IEO}$/ invalid from $\overline{IACK}$/ high	Fig. 9 - 10 Ref. 17	See test 11	all	—	150	—	150	ns
28	t_{plh} (T_{DLCH})	$\overline{DTACK}$/ low from CLK high	Fig. 9 - 10 Ref. 18	See test 11	all	—	180	—	165	ns
29	t_{phl} (T_{IVIL})	$\overline{IEO}$/ valid from $\overline{IEI}$/ low (Note 1)	Fig. 10 Ref. 19	See test 11	all	—	100	—	100	ns
30	t_{phl} t_{plh} (T_{DAVIL})	Data valid from $\overline{IEI}$/ low	Fig. 10 Ref. 20	See test 11	all	—	220	—	220	ns
31	t_{cy} (T_{CT})	CLK cycle time (Note 1)	Fig. 7 Ref. 21	See test 11	all	250	—	200	—	ns
32	t_w (T_{CL})	CLK width low	Fig. 7 Ref. 22	See test 11	all	120	—	90	—	ns
33	t_w (T_{CH})	CLK width high	Fig. 7 Ref. 23	See test 11	all	120	—	110	—	ns
34	t_{su} (T_{SICH})	$\overline{CS}$/ $\overline{IACK}$/ inactive to rising CLK (Note 4 and 5)	Fig. 7 Ref. 24	See test 11	all	100	—	80	—	ns
35	t_w (T_{IOAW})	I/O min active pulse width	Fig. 11 Ref. 25	See test 11	all	100	—	100	—	ns
37	t_{phl} t_{plh} (T_{IDVSL})	I/O valid data valid from rising CS/ or DS/	Fig. 12 Ref. 27	See test 11	all	—	450	—	400	ns

(*) Measurement method : see § 5.1.

Refered notes are given after Table 6.

Table 6 - Dynamic (switching) characteristics TS 68901-4 and 5 MHz (Continued)
$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 5\,\%$; $GND = 0\,V_{DC}$

Test Nbr	Symbol	Parameter	Method (*)	Test Conditions	Test Temp.	4 MHz Limits		5 MHz Limits		Unit
						Min	Max	Min	Max	
38	t_{phI} (T_{RRCL})	Receiver ready delay from rising RC	Fig. 13 Ref. 28	See test 11	all	—	600	—	600	ns
39	t_{phI} (T_{TRCL})	Transmitter ready from rising RC	Fig. 14 Ref. 29	See test 11	all	—	600	—	600	ns
40	t_{phI} (T_{TLSH})	Timer output low from rising edge of $\overline{CS}$/ $\overline{DS}$/ (Note 7)	Fig. 15 Ref. 30	See test 11	all	—	450	—	450	ns
41	t_{plh} (T_{VIT})	T_{OUT} valid from internal time-out (Note 2)	Fig. 15 Ref. 31	See test 11	all	—	$2\,T_{CLK}$ + 300	—	$2\,T_{CLK}$ + 300	ns
42	t_w (T_{TCL})	Timer CLK low time	Fig. 15 Ref. 32	See test 11	all	110	—	90	—	ns
43	t_w (T_{TCH})	Timer CLK high time	Fig. 15 Ref. 33	See test 11	all	110	—	90	—	ns
44	t_w (T_{TCC})	Timer CLK cycle time	Fig. 15 Ref. 34	See test 11	all	250	1000	200	1000	ns
46	t_{phI} (T_{DILI})	Delay to falling $\overline{IRQ}$ from external interrupt active transition	Fig. 11 Ref. 36	See test 11	all	—	380	—	380	ns
47	t_{phI} (T_{TTCL})	Transmitter interrupt delay falling TC	Fig. 14 Ref. 37	See test 11	all	—	550	—	550	ns
48	t_{phI} (T_{RICL})	Receiv buffer full inter trans delay FR rising RC	Fig. 13 Ref. 38	See test 11	all	—	800	—	800	ns
50	t_{plh} (T_{SRCL})	Serial in set-up time of rising edge of RC (divide by one only)	Fig. 13 Ref. 40	See test 11	all	80	—	70	—	ns
51	t_h (T_{DHRL})	Data hold time FR edge of RC (divide by one only)	Fig. 13 Ref. 41	See test 11	all	350	—	325	—	ns
52	t_{plh} t_{phI} (T_{DTCL})	Serial output data valid FR falling edge of TC/(1)	Fig. 14 Ref. 42	See test 11	all	—	440	—	420	ns
53	t_w (T_{TACL})	Transmitter CLK low time	Fig. 14 Ref. 43	See test 11	all	500	—	450	—	ns
54	t_w (T_{TACH})	Transmitter CLK high time	Fig. 14 Ref. 44	See test 11	all	500	—	450	—	ns
55	t_w (T_{TACC})	Transmitter CLK cycle time	Fig. 14 Ref. 45	See test 11	all	1050	—	950	—	ns
56	t_w (T_{RCL})	Receiver CLK low time	Fig. 13 Ref. 46	See test 11	all	500	—	450	—	ns
57	t_w (T_{RCH})	Receiver CLK high time	Fig. 13 Ref. 47	See test 11	all	500	—	450	—	ns
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 13 Ref. 48	See test 11	all	1050	—	950	—	ns
60	t_{plh} t_{phI} (T_{DATCL})	Serial output data valid from falling edge TC (+ 16)	Fig. 14 Ref. 50	See test 11	all	—	490	—	400	ns

(*) Measurement method : see § 5.1.

Refered notes are given after Table 6.

REFERRED NOTES TO THE TABLES

The following notes shall apply where referred into the tables 5 and 6 and/or additional information given in table 7 of this specification.

Note 1 : $\overline{IEO}$ only goes low if no acknwoledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain tri-stated.

Note 2 : T_{CLK} refers to the clock applied to the MFP CLK input pin. tclk refers to the timer clock signal, regardless of whether this signal comes from the XTAL1/XTAL2 crystal clock inputs or the TAI or TBI timer inputs.

Note 3 : If the set-up time is not met, $\overline{CS}$ or $\overline{IACK}$ will not be recognized until the next falling CLK.

Note 4 : If the set-up time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

Note 5 : $\overline{CS}$ is latched internally, therefore if spec's 1 and 24 are met then $\overline{CS}$ may be reasserted before the rising clock and still terminate the current bus cycle. The new bus cycle will be delayed by the TS 68901 until all appropriate internal operations have completed.

Note 6 : Although $\overline{CS}$ and $\overline{DTACK}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, relying only on $\overline{CS}$ for timing.

Note 7 : Spec. 30 applies to timer outputs TAO and TBO only.

Note 8 : Transient energy rating
The test shall be performed as specified in Generic Specification and its asociated documents. The test voltages are as given in table 5 for test 99.
Each terminal of the device under test shall be tested separately against all existing Vcc and Vss terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in table 5 for test 99.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Table 6, refering to the loading network number as shown in Figures 4 and 5 below.

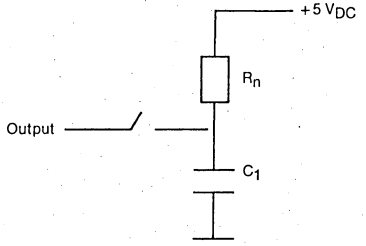


Figure 4 : Passive loads.

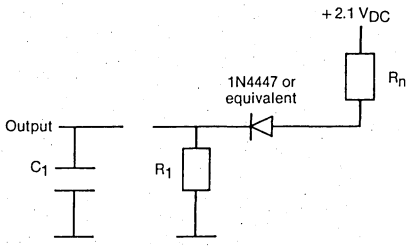
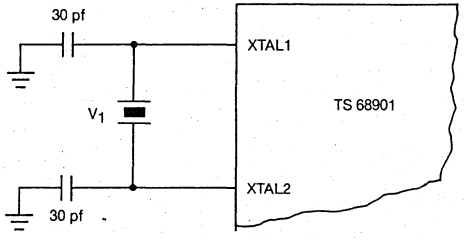


Figure 5 : Active loads.

Load NBR	Figure	R_1	R_n	C_1	Output application
1	4	—	2.25 k	100 pF	$\overline{IRQ}$
2	5	20 k	180	100 pF	All outputs except $\overline{DTACK}$
3	5	6 k	470	130 pF	$\overline{DTACK}$
Note : Equivalent loading may be simulated by the tests.					



Crystal Parameters :
Parallel resonance, fundamental mode AT cut
R_L = < 180 Ω (Fr = 2.8 – 5.0 MHz) ;
R_L = < 300 Ω (Fr = 2.0 – 2.7 MHz) ;
C_L = 10 pF ; C_M = 0.02 pF ; C_h = 5 pF ; L_M = 96 mH
F_R (type) = 2.4676 MHz

Figure 6 : TS 68901 MFP external oscillator components.

5.4.2 - Time definitions

The times specified in Table 6 as dynamic characteristics are defined in Figures 7 to 15 below by a reference number given in the column «Method» of the tables together with the relevant figure number.

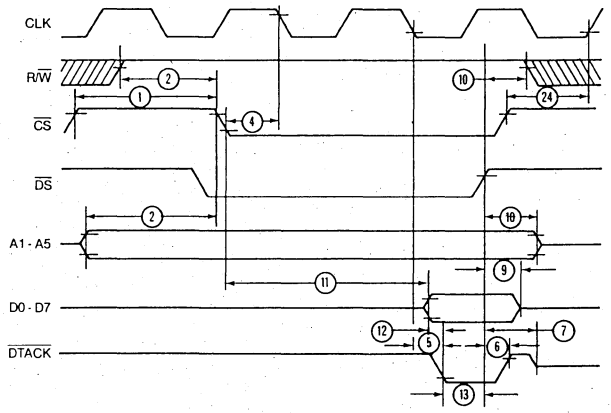
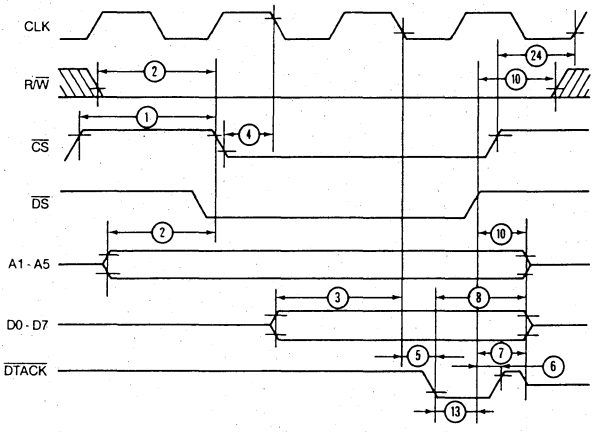
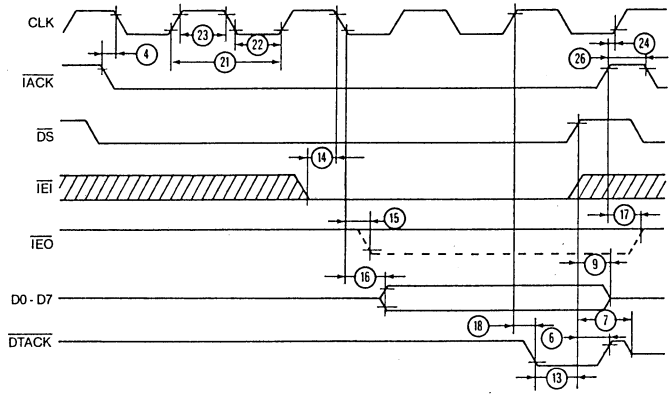


Figure 7 : Read cycle timing.



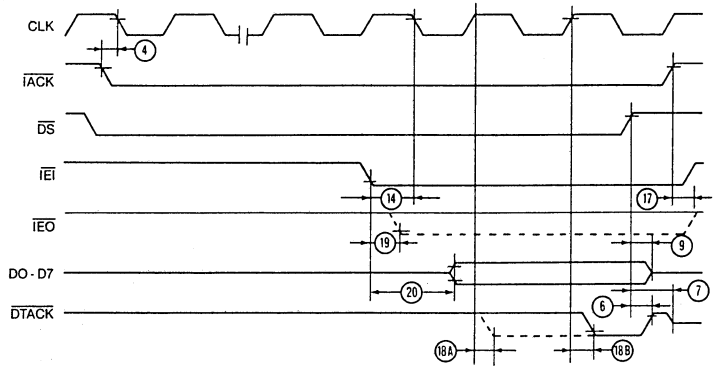
Note : $\overline{CS}$ and $\overline{IACK}$ must be a function of $\overline{DS}$.

Figure 8 : Write cycle timing.



Note : $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain in the high impedance state.

Figure 9 : Interrupt acknowledge cycle ($\overline{IEI}$ low).

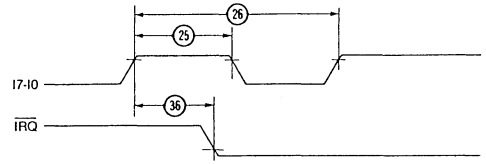


Note : $\overline{CS}$ and $\overline{IACK}$ must be a function of $\overline{DS}$.

Note 1 : $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain in the high impedance state

Note 2 : $\overline{DTACK}$ will go low at A if specification number 14 is met. Otherwise $\overline{DTACK}$ will go low at 8.

Figure 10 : Interrupt acknowledge cycle ($\overline{IEI}$ high).



Note : Active edge is assumed to be the rising edge.

Figure 11 : Interrupt timing.

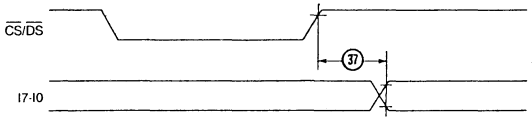


Figure 12 : Port timing.

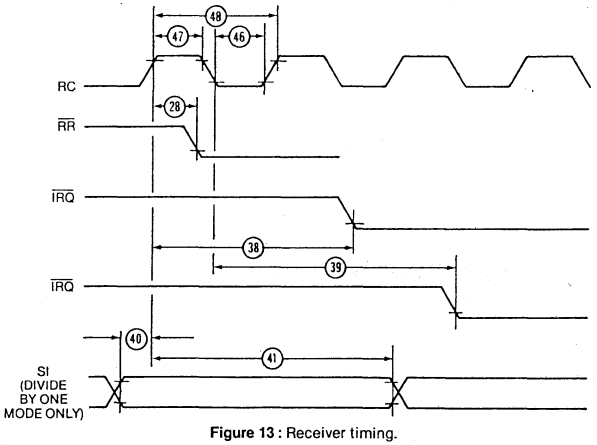


Figure 13 : Receiver timing.

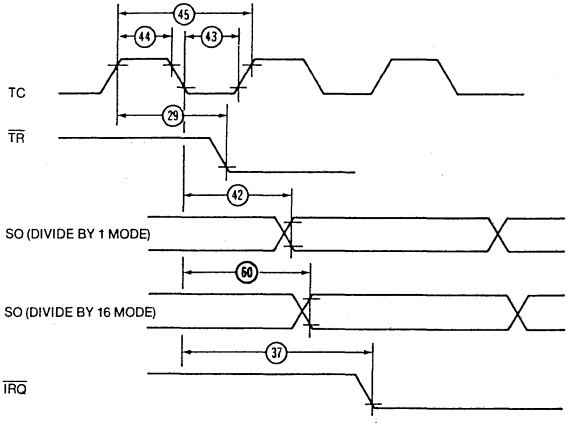


Figure 14 : Transmitter timing.

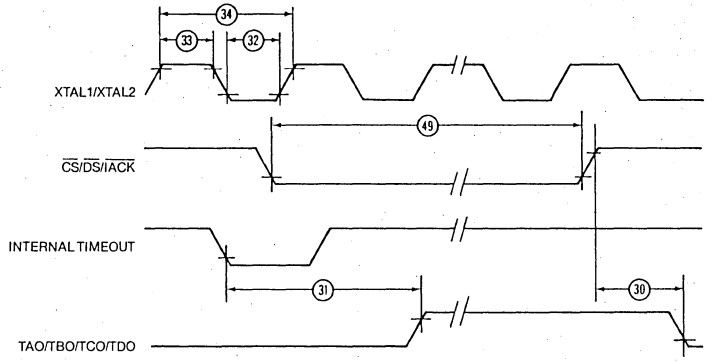


Figure 15 : Timer timing.

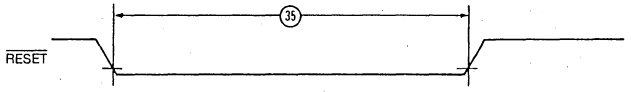


Figure 16 : Reset timing.

5.4.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics
Where input pulse generator is loaded by 90 ohms resistor, the input pulse characteristics shall be as shown in Figure 17.

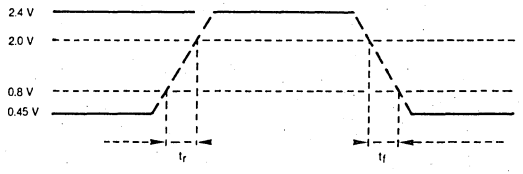


Figure 17 : Input pulse characteristics.

b) Time measurement input voltage references
Input voltages which are taken as reference for time measurement shall be :

$$V_{IL} = 0.8\,V$$
$$V_{IH} = 2.0\,V$$

c) Time measurement output voltage reference for time valid state output
Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in Figure 18.

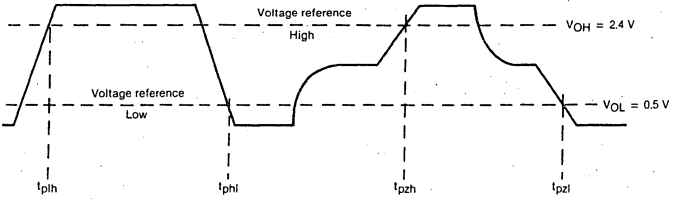


Figure 18 : Output voltage references.

5.4.4 - Timer AC characteristics

Definitions :

Error = Indicated time value - actual time value,
t_{psc} = t_{CLK} * Prescale value.

Internal Timer Mode :

Single Interval Error (Free Running) (See Note 2) ..... ± 100 ns
Cumulative Internal Error 0
Error Between Two Timer Reads ..... ± (t_{psc} − 4 t_{CLK})
Start Timer to Stop Timer Error ..... 2 t_{clk} + 100 ns to − (t_{psc} + 6 t_{CLK} + 100 ns)
Start Timer to Read Timer Error ..... 0 to − (t_{psc} + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (See Note 3) ..... 2 t_{CLK} to − (4 t_{CLK} + 800 ns)

Pulse Width Measurement Mode :

Measurement Accuracy (See Note 1) ..... 2 t_{CLK} to (t_{psc} + 4 t_{CLK})
Minimum Pulse Width ..... 4 t_{CLK}

Event Counter Mode :

Minimun Active Time of TAI and TBI ..... 4 t_{CLK}

Note 1 : Error may be cumulative if repetitively performed.

Note 2 : Error with respect to t_{out} or $\overline{IRQ}$ if Note 3 is true.

Note 3 : Assuming it is possible for the timer to make an interrupt request immediately.

5.5 - Additional information

Additional information shall not be for any inspection purposes.

5

5.5.1 - Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 7 to 16 and loading number refer to Figures 4 and 5 (see § 5.4.1 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2.2 of this specification.

Table 7 - Additional electrical characteristics TS 68901-4 and 5 MHz

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 5\,\%$; GND = 0 V_{DC}

Test Nbr	Symbol	Parameter	Method	Test Conditions	Test Temp.	4 MHz Limits		5 MHz Limits		Unit
						Min	Max	Min	Max	
17	t_{phz} (T_{SHDZ})	CS/, DS/ or IACK/ high to DTACK/ three state	Fig. 8 Ref. 7	—	all	—	100	—	95	ns
19	t_{phz} (T_{SHDAZ})	CS/, DS/ or ICK/ high to data three state	Fig. 7 - 9 10 Ref. 9	—	all	—	50	—	50	ns
31	t_{cy} (T_{CT})	CLK cycle time	Fig. 7 Ref. 21	—	all	—	1000	—	1000	ns
36	t_w (T_{IWH})	IACKL/ width high	Fig. 8 - 9 Ref. 26	—	all	—	2	—	2	T_{CLK}
44	t_{cy} (T_{TCC})	Timer CLK cycle time	Fig. 15 Ref. 34	—	all	—	1000	—	1000	ns
45	t_w (T_{RL})	RESET/ low time	Fig. 16 Ref. 35	—	all	2	—	1.8	—	µs
49	t_{plh} (T_{RIRCL})	Receiv error interrupt trans delay FR falling edge of RC	Fig. 13 Ref. 39	—	all	—	800	—	800	ns
55	t_{cy} (T_{TACC})	Transmitter CLK cycle time	Fig. 14 Ref. 45	See test 11	all	—	0	—	0	ns
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 13 Ref. 48	See test 11	all	—	0	—	0	ns
59	t_w (T_{SWL})	CS/ IACK/ DS/ width low (Note 2)	Fig. 15 Ref. 49	See test 11	all	—	20	—	20	T_{CLK}

Refered note is given after Table 6.

6 · FUNCTIONAL DESCRIPTION

6.1 · Interrupt structure

Address Port N°	Abbreviation	Register name
0	GPIP	General Purpose I/O
1	AER	Active Edge Register
2	DDR	Data Direction Register
3	IERA	Interrupt Enable Register A
4	IERB	Interrupt Enable Register B
5	IPRA	Interrupt Pending Register A
6	IPRB	Interrupt Pending Register B
7	ISRA	Interrupt in Service Register A
8	ISRB	Interrupt in Service Register B
9	IMRA	Interrupt Mask Register A
A	IMRB	Interrupt Mask Register B
B	VR	Vector Register
C	TACR	Timer A Control Register
D	TBCR	Timer B Control Register
E	TCDCR	Timer C and D Control Register
F	TADR	Timer A Data Register
10	TBDR	Timer B Data Register
11	TCDR	Timer C Data Register
12	TDDR	Timer D Data Register
13	SCR	Sync Character Register
14	UCR	Usart Control Register
15	RSR	Receiver Status Register
16	TSR	Transmitter Status Register
17	UDS	Usart Data Register

Figure 19 : Register MAP.

The General Purpose I/O-Interrupt Port (GPIP) provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt in either a positive going edge or a negative going edge of the input signal.

The GPIP has three associated registers. One allows the programmer to specify the Active Edge for each bit that will trigger an interrupt. Another register specifies the Data Direction (input or output) associated with each bit. The third register is the actual data I/0 register used to input or output data to the port. These three registers are illustrated in Figure 20.

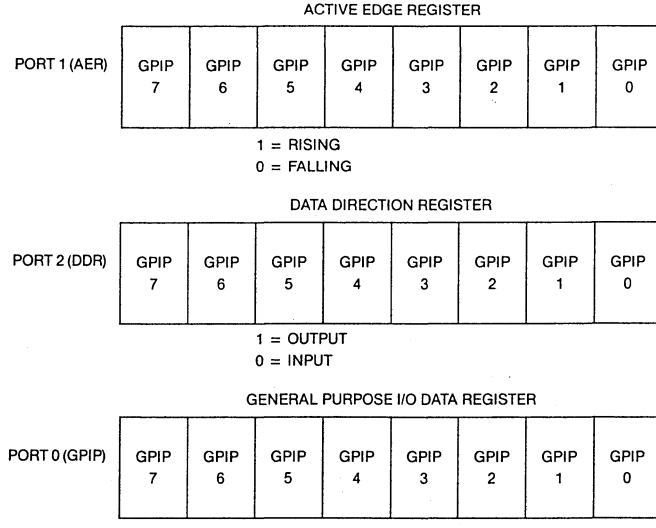


Figure 20 : General purpose I/O registers.

The Active Edge Register (AER) allows each of the General Purpose Interrupts to provide an interrupt on either a 1-0 transition or a 0-1 transition. Writing a zero to the appropriate bit of the AER causes the associated input to produce an interrupt on the 1-0 transition. The edge bit is simply one input to an exclusive or gate, with the other input coming from the input buffer and the output going to a 1-0 transition detector. Thus, depending upon the state of the input, writing the AER can cause an interrupt-producing transtion, which will cause an interrupt on the associated channel, if that channel is enabled. One would then normally configure the AER before enabling interrupts via IERA and IERB.

Note : changing the edge bit, with the interrupt enabled, may cause an interrupt on that channel.

The Data Direction Register (DDR) is used to define I0-I7 as inputs or as outputs on a bit by bit basis. Writing a zero into a bit of the DDR causes the correponding Interrupt-I/O pin to be a Hi-Z input. Writing a one into a bit of the DDR causes the corresponding pin to be configured as a push-pull output. When data is writen into the GPIP, those pins defined as inputs will remain in the Hi-Z state while those pins defined as outputs will assume the state (high or low) or their corresponding bit in the GPIP. When the GPIP is read, the data read will come directly from the corresponding bit of the GPIP register for all pins defined as output, while the data read on all pins defined as inputs will come from the input buffers.

Each individual function in the TS 68901 is provided while a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during the interrupt acknowledge cycle is shown in Figure 21, while register is shown in Figure 22.

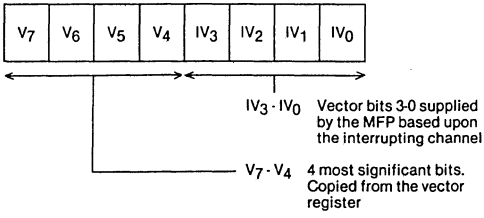


Figure 21 : Interrupt vector.

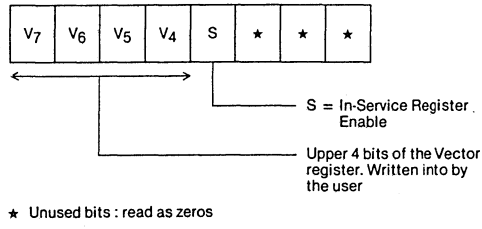


Figure 22 : Vector register.

There are 16 vectors addresses generated internally by the TS 68901, one for each of the interrupt channels.

The Interrupt Control Registers (Figure 23) provide control of interrupt processing for all I/O facilities of the TS 68901. These registers allow the programmer to enable or disable any or all of the 16 interrupts, providing masking for any interrupt, and provide access to the pending and in-service status of the interrupt. Optional end-of-interrupt modes are available under software control. All the interrupts are prioritized as shown in Figure 24.

ADDRESS

INTERRUPT ENABLE REGISTERS

PORT 3	A (IERA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Full	XMIT Error	TIMER B
PORT 4	B (IERB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

INTERRUPT PENDING REGISTERS

PORT 5	A (IPRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Full	XMIT Error	TIMER B
PORT 6	B (IPRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

WRITTING 0 = CLEAR
WRITTING 1 = UNCHANGED

INTERRUPT IN-SERVICE REGISTERS

PORT 7	A (ISRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Full	XMIT Error	TIMER B
PORT 8	B (ISRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

INTERRUPT MASK REGISTERS

PORT 9	A (IMRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Full	XMIT Error	TIMER B
PORT A	B (IMRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

Figure 23 : Interrupt control registers.

Priority	Channel	Description
Highest	1111	General Purpose Interrupt 7 (I7)
	1110	General Purpose Interrupt 6 (I6)
	1101	Timer A
	1100	Receive Buffer Full
	1011	Receive Error
	1010	Transmit Buffer Empty
	1001	Transmit Error
	1000	Timer B
	0111	General Purpose Interrupt 5 (I5)
	0110	General Purpose Interrupt 4 (I4)
	0101	Timer C
	0100	Timer D
	0011	General Purpose Interrupt 3 (I3)
	0010	General Purpose Interrupt 2 (I2)
	0001	General Purpose Interrupt 1 (I1)
Lowest	0000	General Purpose Interrupt 0 (I0)

Figure 24 : Interrupt control register definitions.

Interrupts may be either polled or vectored. Each channel may be individual enabled or disabled by writing a one or a zero in the appropriate bit of Interrupt Enable Registers (IERA, IERB - see Figure 23 for all registers in this section). When disabled, an interrupt channel is completly inactive. Any internal or external action which would normally produce an interrupt on that channel is ignored and any pending interrupt on that channel will be cleared by disabling that channel. Disabling an interrupt channel has no effect on the corresponding bit in Interrupt In-Service Registers (ISRA, ISRB) ; thus, if the In-Service Registers are used and an interrupt is in service on that channel when the channel is disabled, it will remain in service until cleared in the normal manner. IERA and IERB are also readable.

When an interrupt is received on an enabled channel, its corresponding bit in the pending register will be set. When that channel is acknowledged it will passed its vector, and the corresponding bit in the Interrupt Pending Register (IPRA or IPRB) will be cleared. IPRA and IPRB are readable ; thus by polling IPRA and IPRB, it can be determined whether a channel has a pending interrupt. IPRA and IPRB are also writeable and a pending interrupt can be cleared without going through the acknowledge sequence by writing a zero to the appropriate bit. This allows any one bit to be cleared without altering any other bits, simply by writing all ones except for the bit position to be cleared, to IPRA or IPRB. Thus a fully polled interrupt scheme is possible.

Note : writing a one to IPRA, IPRB has no effect on the interrupt register.

The interrupt mask register (IMRA and IMRB) may be used to block a channel from making an interrupt request. Writing a zero into the corresponding bit of the mask register will still allow the channel to receive an interrupt and latch it into its pending bit (if that channel is enabled), but will prevent that channel from making an interrupt request. If that channel is causing an interrupt request at the time the corresponding bit in the mask register is cleared, the request will cease. If no other channel is making a request, $\overline{IRQ}$ will go inactive. If the mask bit is re-enable, any pending interrupt is now free to resume its request unless blocked by a higher priority request for service. IMRA and IMRB are also readable. A conceptual circuit of an interrupt channel is shown in Figure 25.

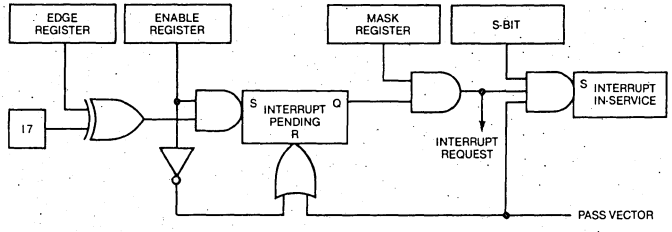


Figure 25 : A conceptual circuit of an interrupt channel.

There are two end-of-interrupt modes : the automatic end-of-interrupt mode and the software end-of-interrupt mode. The mode is selected by writing a one or a zero to the S bit in the Vector Register (VR). If the S bit of the VR is a one, all channels operate in the software end-of-interrupt mode. If the S bit is a zero, all channels operate in the automatic end-of-interrupt mode, and a reset is held on all in-service bits. In the automatic end-of-interrupt mode, the pending bit is cleared when that channel passes its vector. At that point, no further history of that interrupt remains in the TS 68901 MFP. In the software end-of-interrupt mode, the in-service bit is set and the pending bit is cleared when the channel passes its vector. With the in-service bit set, no lower priority channel is allowed to request an interrupt or to pass its vector during an acknowledge sequence ; however, a lower priority channel may still receive an interrupt and latch it into the pending bit. The in-service bit of a particular channel may be cleared by writing a zero to the corresponding bit in ISRA or ISRB.

Typically, this will be done at the conclusion of the interrupt routine just before the return. Thus no lower priority channel will be allowed to request service. While the in-service bit is set, a second interrupt on that channel may be received and latched into the pending bit, through no service request will be made in reponse to the second interrupt until the in-service bit is cleared. ISRA and ISRB may be read at any time. Only a zero may be writen into any bit of ISRA and ISRB ; thus the in-service bits may be cleared in software but cannot be set in software. This allows any one bit to be cleared, without altering any other bits, simply by writing all ones except for the bit position to be cleared to ISRA or ISRB, as with IPRA and IPRB.

Each interrupt channel responds with a discrete 8-bit vector when acknowledged. The upper four bits of the vector are set by writing the upper four bits of the VR. The four low order bits (Bit 3 - Bit 0) are generated by the interrupting channel.

To acknowledge an interrupt, $\overline{IACK}$ goes low, the $\overline{IEI}$ input must go low (or be tied low) and the TS 68901 MFP must have an acknowledgeable interrupt pending. The Daisy Chaining capability (Figure 12) requires that all parts in a chain have a common $\overline{IACK}$. When the $\overline{IACK}$ goes low, all parts freeze and priotize interrupts in parallel. Then priority is passed down the chain, via $\overline{IEI}$ and $\overline{IEO}$, until a part wich has a pending interrupt is reached. The part with the pending interrupt, passes a vector, does not propagate $\overline{IEO}$, and generates $\overline{DTACK}$.

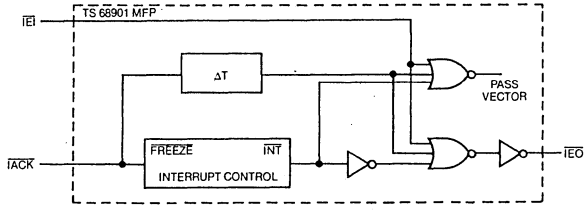


Figure 26 : A conceptual of the TS 68901 MFP daisy chaining.

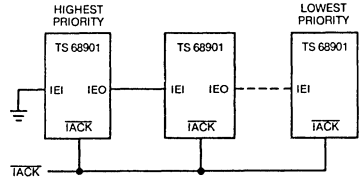


Figure 27 : Daisy chaining.

Figure 24 describes the 16 prioritized interrupt channels. As shown, General Purpose Interrupt 7 has the highest priority, while General Purpose Interrupt 0 is assigned the lowest priority. Each of these channels may be reprioritized, in effect, by selectively masking interrupts under software control. The binary numbers under «channel» correspond to the modified bits IV_3, IV_2, IV_1 and IV_0, respectively, of the interrupt Vector for each channel (see Figure 21).

Each channel has an enable bit contained in IERA or IERB, a pending latch contained in IMRA or IMRB, and an in-service latch contained in ISRA or ISRB. Additionally, the eight General Purpose Interrupts each have an edge bit contained in the Active Edge Register (AER), a bit to define the line as input or output contained in the Data Direction Register (DDR) and an I/O bit in the General Purpose Interrupt-I/O Port (GPIP).

Note : Concerning operation in the software end-of-interrupt mode (S bit sets to 1 in VR) with multiple sources.
In order to have good behaviour of the MFP, at the end of an interrupt routine (after the corresponding in-service bit has been cleared), the ISRA (and ISRB) must be tested. If an higher priority in-service bit is set, the actual interrupt programm must directly execute a jump to the highest priority interrupt routine for which the in-service bit is set instead of executing an return (RTE) instruction. To avoid the test of ISRA and ISRB, the automatic end of interrupt mode can be used (S bit = 0).

6.2 - Timers

There are four timers on the TS 68901 MFP. Two of the timers (Timer A and Timer B) are full function timers which can perform the basic delay function and can also perform event counting, pulse width measurement, and waveform generation. The other two timers (Timer C and Timer D) are delay timers only. One or both of these timers can be used to supply the baud rate clocks for the USART. All timers are prescaler/counter timers with a common independent clock input (XTAL1, XTAL2). In addition, all timers have a time-out ouput function that toggles each time the timer times out.

The four timers are programmed via three Timer Control Registers and four Timer Data Registers. Timer A and B are controlled by the control registers TACR and TBCR, respectively (see Figure 28), and by the data registers TCDR (Figure 29). Timers C and D are controlled by the control register TCDCR (see Figure 30) and two data registers TCDR and TDDR. Bits in the control registers allow the selection of operational mode, prescale, and control while the data registers are used to read the timer or write into the time constant register. Timer A and B input pins, TAI and TBI, are used for the event and pulse width modes for timers A and B.

PORT C (TACR)	★	★	★	TIMER A RESET	AC_3	AC_2	AC_1	AC_0
PORT D (TBCR)	★	★	★	TIMER B RESET	BC_3	BC_2	BC_1	BC_0

C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode : 4 Prescale
0	0	1	0	Delay Mode : 10 Prescale
0	0	1	1	Delay Mode : 16 Prescale
0	1	0	0	Delay Mode : 50 Prescale
0	1	0	1	Delay Mode : 64 Prescale
0	1	1	0	Delay Mode : 100 Prescale
0	1	1	1	Delay Mode : 200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode : 4 Prescale
1	0	1	0	Pulse Width Mode : 10 Prescale
1	0	1	1	Pulse Width Mode : 16 Prescale
1	1	0	0	Pulse Width Mode : 50 Prescale
1	1	0	1	Pulse Width Mode : 64 Prescale
1	1	1	0	Pulse Width Mode : 100 Prescale
1	1	1	1	Pulse Width Mode : 200 Prescale

★ Unused bits : read as zeros

Figure 28 : Timer A and B control register.

PORT F (TADR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PORT 10 (TBDR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PORT 11 (TCDR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PORT 12 (TDDR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Figure 29 : Timer data registers (A, B, C and D).

PORT E (TCDCR)	★	CC_2	CC_1	CC_0	★	DC_2	DC_1	DC_0

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, : 4 Prescale
0	1	0	Delay Mode, : 10 Prescale
0	1	1	Delay Mode, : 16 Prescale
1	0	0	Delay Mode, : 50 Prescale
1	0	1	Delay Mode, : 64 Prescale
1	1	0	Delay Mode, : 100 Prescale
1	1	1	Delay Mode, : 200 Prescale

★ Unused bits : read as zeros.

Figure 30 : Timer C and D register.

With the timer stopped, no counting can occur. The timer contents will remain unaltered while the timer is stopped (unless reloaded by writing the Timer Data Register), but any residual count in the prescaler will be lost.

In the delay mode, the prescaler is always active. A count pulse will be applied to the main timer unit each time the prescribed number of timer clock cycles has elapsed. Thus, if the prescaler is programmed to divide by ten, acount pulse will be applied to the main counter every ten cycles of the timer clock.

Each time a count pulse is applied to the main counter, it will decrement its contents. The main counter is initially loaded by writing to the Timer Data Register. Each count pulse will cause the current count to decrement. When the timer has decremented down to «01», the next count pulse will not cause it to decrement to «00». Instead, the next count pulse will cause the timer to be reloaded from the Timer Data Register. Additionally, a «Time out» pulse will be produced. This Time Out pulse is coupled to the timer output pin and will cause the pin to change states. The output will remain in this new state until the next Time Out pulse occurs. Thus the output will complete one full cycle for each two Time Out pulses.

If, for example, the prescaler were programmed to divide by ten, and the Timer Data Register were loaded with 100 (decimal), the main counter would decrement once for every ten cycles of the timer clock. A Time Out pulse will occur (hence an interrupt if that channel is enabled) every 1000 cycles of the timer clock, and the timer output will complete one full cycle every 2000 cycles of the timer clock.

The main counter is an 8-bit binary down counter. It may be read at any time by reading the Timer Data Register. The information read is the information last clocked into the timer read register when the DS pin had last gone high prior to the current read cycle. When written, data is loaded into the Timer Data Register, and the main counter, if the timer is stopped. If the Timer Data Register is written while the timer is running, the new word is not loaded into the timer until it counts through H «01». However, if the timer is written while it is counting through H «01»,an indeterminate value will be written into the timer constant register. This may be circumvented by ensuring that the data register is not written when the count is H «01».

If the main counter is loaded with «01», a Time Out Pulse will occur every time the prescaler presents a count pulse to the main counter. If loaded with «00», a Time Out Pulse will occur every 256 count pulses.

Changing the prescale value with the timer running can cause the first Time Out pulse to occur at an indeterminate time, (no less than one nor more than 200 timer clock cycles times the number in the time constant register), but subsequent Time Out pulses will then occur at the correct interval.

In addition to the delay mode described above, Timers A and B can also function in the Pulse Width Measurement mode or in the Event Count mode. In either of these two mode, an auxilary control signal is required. The auxilary control input for Timer A is TAI, and for timer B, TBI is used. The interrupt channels associated with 14 and 13 are used for TAI and TBI, respectively, in Pulse Width mode. See Figure 31.

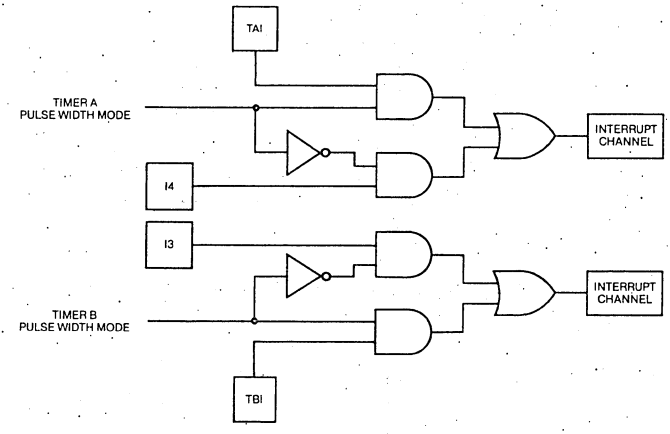


Figure 31 : A conceptual circuit of the MFP timers in the pulse width measurement mode.

The pulse width measurement mode functions much like the delay mode. However, in this mode, the auxilary control signal on TAI or TBI acts as an enable to the timer. When the control signal on TAI or TBI is inactive, the timer will be stopped. When it is active, the prescaler and main counter are allowed to run. Thus the width of the active pulse on TAI or TBI is determined by the number of timer counts which occur while the pulse allows the timer to run. The active state of the signal on TAI or TBI is dependent upon the associted Interrupt Channel's edge bit (GPIP 4 for TAI and GPIG 3 for TBI ; see Active Edge Register in Figure 20). If the edge bit associated with the TAI or TBI input is a one, it will be active high ; thus the timer will be allowed to run when the input is at a high level. If the edge bit is a zero, the TAI or TBI input will be active low. As previously stated, the interrupt channel (13 or 14) associated with the input still functions when the timer is used in the pulse width measurement mode. However, if the timer is programmed for the pulse width measurement mode, the interrupt caused by transitions on the associated TAI or TBI input will occur on the opposite transition.

For example, if the edge bit associated with the TAI input (AER-GPIP 4) is a one, an interrupt would normally be generated on the 0-1 transition of the 14 input signal. If the timer associated with this input (Timer A) is placed in the pulse width measurement mode, the interrupt will occur on the 1-0 transition of the TAI signal instead. Because the edge bit (AER-GPIP 4) is a one, Timer A will stop, and it is at time this point that the interrupt will occur (assuming that the channel is enabled). This allows the interrupt to signal the CPU that the pulse being measured has terminated ; thus Timer A may now be read to determine the pulse width. (Again not that 13 and 14 may still be used for I/O when the timer is in the pulse width measurement mode). If Timer A is reprogrammed for another mode, interrupts will again occur on the transition, as normally defined by the edge bit. Note that, like changing the edge bit, placing the timer into or taking it out of the pulse width mode can produce a transition on the signal to the interrupt channel and may cause an interrupt. If measuring consecutive pulses, it is obvious that one must read this contents of the timer and then reinitialize the main counter by writing to the timer data register. If the timer data register is written after the pulse goes active, the timer counts from the previous content, and when it counts through H «01», the correct value is written into the timer. The pulse width then includes counts from before the timer was reloaded.

In the event count mode, the prescaler is disabled. Each time the control input on TAI or TBI makes an active transition as defined by the associated Interrupt Channel's edge bit, a count pulse will be generated, and the main counter will decrement. In all other respects, the timer functions as previously described. Altering the edge bit while the timer is in the event count mode can produce a count pulse. The interrupt channel associated with the input (I3 or I4 for TAI) is allowed to function normally. To count transition reliably, the input must remain in each state (1/0) for a length of time equal to four periods of the timer clock ; thus signals of a frequency up to one fourth of the timer clock can be counted.

The manner in which the timer output pins toggle states has previously been described. All timer outputs will be forced low by a device RESET. The output associated with Timers A and B will toggle on each Time Out pulse regardless of the mode the timers are programmed to. In addition, the outputs from Timers A and B can be forced low at any time by writing a «1» to the reset location in TACR and TBCR, respectively. The output will be forced to the low state during the WRITE operation, and at the conclusion of the operation, the output will again be free to toggle each time a Time Out pulse occurs. This feature will allow waveform generation.

During reset, the Timer Data registers and the main counters are not reset. Also, if using the reset option on Timers A or B, one must make sure to keep the other bits in the correct state so as no to affect the operation of Timers A and B.

5

6.3 · USART

Serial Communication is provided by a full-duplex double-buffured USART, which is capable of either asynchronous or synchronous operation. Variable word length and start/stop bit configurations are available under software control for asyncrhonous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for transmission. Moreover, the TS 68901 allows stripping of all Sync Words received in synchronous operation. The handshake control lines RR (Receiver Ready) and TR (Transmitter Ready) allow DMA operation. Seperate receive and transmit clocks are available, and seperate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

The USART is provided with the three Control/Status Registers and a Data Register. The USART Data Register form is illustrated in Figure 32. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 33. Status of both the Receiver and Transmitter sections is accessed by means of the two Status Registers, as shown in Figures 34 and 35. Data written to the Data Register is passed to the transmitter, while reading the Data Register will acces data received by the USART.

PORT 17 (UDR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Figure 32 : Usart data register.

	UCR_7							UCR_0
PORT 14 (UCR)	1 = :16 0 = :1	WL_1	WL_0	ST_1	ST_0	PARTY ENABLE ON 1	1 = EVEN 0 = ODD	★

★ Unused bit : read as zero

Figure 33 : Usart control register (UCR).

: 16/: 1 : When this bit is zero, data will be clocked into and out of the receiver and transmitter at the frequency of their respective clocks. When this bit is loaded with a one, data will be clocked into and out the receiver and transmitter at one sixteenth the frequency of their respective clocks. Additionally, when placed in the divide by sixteen mode, the receiver data transition resynchronization logic will be enabled.

$WL_0 - WL_1$: Word Length Control. These two bits set the length of the data word (exclusive of start bits, stop bits, and parity bits) as follows :

WL_1	WL_0	Word Length
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

$ST_0 - ST_1$: Start/Stop bit control (format control). These two bits set the format as follows :

ST_1	ST_0	Start Bits	Stop Bits	Format
0	0	0	0	SYNC
0	1	1	1	ASYNC
+1	0	1	$1^{1/2}$	ASYNC
1	1	1	2	ASYNC

+ NOTE : 16 only

PARITY : Parity Enabled. When set («1»), parity will be checked by the receiver, parity will be calculated, and a parity bit will be inserted by the transmitter. When cleared («0»), no parity check will be made and no parity bit will be inserted for transmission.
For a word length of 8 the MFP calculates the parity and appends it when transmitting a sync character. For shorter lengths, the parity must be stored in the Sync Character Register (SCR) along with the sync character.

E/O : Even-Odd. When set («1»), even parity will be used if parity is enabled. When cleared («0»), odd parity will be used when parity is enabled.

Note : that the synchronous or asynchronous format may be selected independently of a ÷1 or ÷16 clock. Thus it is possible to clock data synchronously into the device but still use start and stop bits. In this mod, all normal asynchronous format features still apply. Data will be shifted in after a start bit is encountered, and a stop bit will be checked to determine proper framing. If a transmit underrun condition occurs, the output will be placed in a marking state, etc. It is conversely possible to clock data in asynchronously using a synchronous format. There is data transition detection logic built into the receive clock circuitry which will re-synchronize the internal shift clock on each data transition so that, with sufficiently frequent data transitions, start bits are not required. In this mode, all other common synchronous features function normally. This re-synchronization logic is only active in ÷16 clock mode.

6.4 - Receiver

The receiver section of the USART is configured by the UCR as previously described. The status of the receiver can be determined by reading and writing to the Receiver Status Register (RSR). The RSR is configured as follows :

PORT 15 (RSR)

RSR_7							RSR_0
BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND / $\overline{\text{SEARCH}}$ OR BREAK DETECT	MATCH / CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

Figure 34 : Receive status register (RSR).

BF : Buffer Full. This bit is set when the incoming word is transferred to the receive buffer. The bit is cleared when the receive buffer is ready by reading the UDR. This bit of the RSR is read only.

OE : Overrun Error. This flag is set if the incoming word is completely received and due to be transfered to the receive buffer, but the last word in the receive buffer has not yet been read. When this condition occurs, the word in the receive buffer is not overwritten by the new word. Note that the status flag always reflect the status of the data word currently in the receive buffer. As such, the OE flag is not actually set until the good word currently in the buffer has been read. The interrupt associated with this error will also no be generated until the old word in the receive buffer has nos been read.

OE flag is cleared by reading the receiver status register, and new data words cannot be shifted to the receive buffer until this is done.

PE : Parity Error. This flag is set if the word received has a parity error. The flag is set when the received word is transferred from the shift register to the receive buffer if the error condition exists. The flag is cleared when the next word which does not have a parity error is transferred to the receive buffer.

FE : Frame Error. This flag only applies to the asynchronous format. A frame error is defined as a non-zero data word which is not followed by a stop bit. Like the PE flag, the FE flag is set or cleared when a word is transferred to the receive buffer.

F/$\overline{S}$ Found/$\overline{\text{Search}}$. This combination control bit and flag bit is only used with the synchronous format. It can be set or cleared by writing to this bit of the RSR. When this bit is cleared, the receiver is placed in the search mode. In this mode, a bit by bit comparison of the incoming data to the character in the Sync Character Register (SCR) is made. The word length counter is disabled. When a match is found, this bit will be set automatically, and the word length counter will start as sync has not been archieved. An interrupt will be generated on the receive error channel when the match occurs. The word just shifted in will, of necessity, be equal to the sync character, and it will not be transferred to the receive buffer.

B : Break. This flag is used only when the asynchronous format is selected. This flag will be set when an all zero data word, followed by no stop bit, is received. The flag will stay set until both a non-zero bit is received and the RSR has been read at least once since the flag was set. Break indication will not occur if the receive buffer is full.

M/CIP : Match/Character in Progress. If the synchronous format is selected, this flag is the Match flag. It will be set each time the word transferred to the receive buffer matches the sync character. It will be reset each time the word transferred to the receive buffer does not match the sync character. If the asyncrhonous format is selected, this flag represents Character in Progress. It will be set upon a start bit detect and cleared at the end of the word.

SS : Sync Stip Enable. If this bit is set to a one, data words, that match the sync character will not be loaded into the receive buffer, and no buffer full signal will be generated.

RE : Receive Enable. This control bit is used to enable or disable the receiver. If a zero is written to this bit of the RSR, the receiver will not turn off immediately. All flags including the F/S bit will be cleared. If a one is written to this bit, normal receiver operation is enabled. The receive clock has to be running before the receiver is enabled.

There are two interrupt channels associated with the receiver. One channel is used for the normal Buffer Full condition, while the other channel is used whenever an error condition occurs. Only one interrupt is generated per word received, but dedicating two channels allows seperate vectors : one for the normal condition, and one for an error condition. If the error channel is disabled, an interrupt will be generated via the Buffer Full Channel, whether the word received is normal or in error. Those conditions which produce an interrupt via the error channel are : Overrun, Parity Error, Frame Error, Sync Found and Break. If a received word has an error associated with it, and the error interrupt channel is enabled, an interrupt will occur on the error channel only.

Each time a word is transferred into the receive buffer, a corresponding set of flags is latched into the RSR. No flags (except CIP) are allowed to change until the data word has been read from the receive buffer. Reading the receive buffer allows a new data word to be transferred to the receive buffer when it is received. This one should first read the RSR then receive buffer (UDR) to ensure that the flags just read match the data word just read. If done in the reverse order, it is possible that subsequent to reading the data word from the receive buffer, but prior to reading the RSR, a new word may be received and transferred to the receive buffer and, with it, its associated flags latched into the RSR. Thus, when the RSR is read, those flags may actually correspond to a different data word. It is good pratice, also to read the RSR prior to a data read as, when an overrun error occurs, the receiver will not assemble new characters until the RSR has been read.

As previously stated, when overrun occurs, the OE flag will not be set and the associated interrupt will not be generated until the receive buffer has nos been read. If a break occurs, and the receive buffer has not yet been read, only the B flag will be set (OE will not been set). Again, this flag will not be set until the last valid word has been read from the receive buffer. If the break condition ends and another whole data word is received before the receive buffer is read, both the B and OE flags will be set once the receive buffer is read.

If a break occurs while the OE flag is set, the B flag will also be set.

A break generates an interrupt when the condition occurs and again when the condition ends. If the break condition ends before it is acknowledged by reading the RSR, the receiver error interrupt indicating end of break will be generated once the RSR is read.

Anytime the asynchronous format is selected, start bit detection is also enabled. New data is not shift into the shift register until a zero bit is detected. If a : 16 clock is selected, along with the asynchronous format, false start bit detection is enabled. Any transition to be stable for 3 positive going edges of the receive clock to be called a valid transition. For a start bit to be good, a valid 0-1 transition must not occur for 8 positive clock transitions after the initial valid 1-0 transition.

After a good start bit has been detected, valid transitions in the data are checked for countinously. When a valid transition is detected, the counter is forced to state zero, and no more transition checking is started until state four. At state eight, the «previous state» of the transition checking logic is clocked into the receiver.

As a result of this synchronization logic, it is possibler to run with asynchronous clocks without start and stop bits if there are sufficient valid transitions in the data stream. This logic also makes the unit more tolerant of clock skew for normal asynchronous communications than the device which employs only start bit synchronization.

6.5 - Transmitter

The transmitter section of the USART is configured as the format, word length, etc. by the UCR, as previously described. The status of the transmitter can be determined by reading or writing the Transmitter Status Register (TSR). The TSR is configured as follows :

	TSR_7							TSR_0
PORT 16 (TSR)	BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	ENDS OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

Figure 35 : Transmitter status register (TSR).

BE : Buffer Empty. This status bit is set when the word in the transmit buffer is transferred to the output shift register and thus the transmit buffer may be reloaded with the next data word. The flag is cleard when the transmit is loaded by writing to the UDR.

UE : This bit is set when the last word has been shifted out of the transmit shift register before a new word has been loaded into the transmit buffer. It is not necessary to clear this bit before loading the UDR.
This bit may be cleared by either reading the TSR or by disabling the transmitter. After the setting of the UE bit, one full transmitter clock cycle is required before this bit can be cleared by a read. The timing in some systems may allow a read of the TSR before the required clock cycle has been completed. This would result in the UE bit not being cleared until the following read. To avoid this problem, a dummy read of the TSR should be performed at the end of the UE service routine.
Only one underrun error may be generated between loads of the UDR regardless of the number of transmitter clock cycles between UDR loads.

AT : This bit causes the receiver to be enabled at the end of the transmission of the last word in the transmitter if the transmitter has been disabled.

END : End of Transmission. When the transmitter is turned off with a character still in the output shift register, transmission will continue until that character is shifted out. Once it has cleared the output register, the END bit will be set. If no character is being transmitted when the transmitter is disabled, the transmitter will stop at the next rising edge of the internal shift clock, and END will immediately be set. The END bit is cleared by re-enabling the transmitter.

B : Break. This control bit will cause a break to be transmitted. When a «1» is written to the B bit of the TSR, a break will be transmitted upon completion of the character (if any) currently being transmitted. A break will continue to be transmitted until the B bit is cleared by writing a «0» to this bit of the TSR. At that time, normal transmission will resume. The B bit has no function in the synchronous format. Setting the «B» bit to a one keeps the «BE» bit from being set to a one. So, if there were a word in the buffer at the start of break, it would remain there until the end of break, at which time it would be transmitted (if the transmitter is still enabled). If the buffer were not full at the start of break, it could be written at any time during the break. If the buffer is empty at the end of break, the underrun flag will be set (unless the transmitter is disabled).
The BREAK bit cannot be set until the transmitter has been enabled and the transmitter has had sufficient time (one clock cycle) to perform the internal reset and initialization functions.

H, L : High and Low. These two control bits are used to configure the transmitter output, when the transmitter is [isabled, as follows :

H	L	Output State
0	0	Hi-Z
0	1	Low («0»)
1	0	High («1»)
1	1	Loop-Connects transmitter output to receiver input, and TC to Receiver Clock (RC and SI are not used ; they are bypassed internally). In loop back mode, transmitter output goes high when disabled.

Altering these two bits after Transmitter Enable (XE) is set will alter the output state until END is false. These bits should be set prior to enabling the transmitter. The state of these bits determine the state of the first transmitted character after the transmitter is enabled. If the high impedance mode was selected prior to the transmitter being enabled, the first bit transmitted is indeterminate.

XE : Transmitter Enable. This control bit is used to enable or disable the transmitter. When set, the transmitter is enabled. When cleared, the transmitter will be disabled. If disabled, any word currently in the output register will continue to be transmitted until finished. If a break is being transmitted until finished. If a break is being transmitted when XE is cleared, the transmitter will turn off at the end of the break character boundary, and no end of break stop bit is transmitted. The transmit clock must be running before the transmitter is enabled. A «one» bit always precede the first word out of the transmitter after the transmitter is enabled. There is a delay between the time the transmitter enable bit is written and when the transmitter reset goes low ; therefore, the H and L bits should be written with the desired state prior to enabling the transmitter.

Like the receiver section, there are two seperate interrupt channels associated with the transmitter. The buffer Empty condition causes an interrupt via one channel, while the Underrun and End conditions will cause an interrupt via the second channel. When underrun occurs in the synchronous format, the character in the SCR will be transmitted until a new word is loaded into the transmit buffer. In the asynchronous format, a «Mark» will be continously transmitted when underrun occurs.

The transmit buffer can be loaded prior to enabling the transmitter. When the transmitter is disabled, any character currently in the process of being transmitted will continue to conclusion, but any charcter in the transmit buffer will not be transmitted and will remain in the buffer. Thus no buffer empty interrupt will occur nor will the BE flag be set. If the buffer were already empty, the BE flag would not be set and would remain set. When the transmitter is disabled with a character in the output register but not with no character in the transmit buffer, an Underrun Error will not occur when the character in progress concludes.

Often it is necessary to send a break for some particular periode. To aid in timing a break transmission, a transmit error interrupt will be generated at every normal character boundary time during a break transmission. The status register information is unaffected by this error condition interrupt. It should be noted that an underrun error, if present, must be cleared from the TSR, and the interrupt pending register must be cleared of pending transmitter errors at the beginning of the break transmission or no interrupts will be generated at the character boundary time.

If the synchronous format is selected, the sync character should be loaded into the Sync Character Register (SCR) as shown in Figure 36. This character is compared to the received serial data during a Search, and will be continuously transmitted during an underrun condition.

PORT 13 (SCR),	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Figure 36 : Sync character register.

All flags in the RSR or TSR will continue to function as described whether their associated interrupt channel is disabled or enabled. All interrupt channels are edge triggered and, in many cases, it is the actual output of a flag bit or flag bits which is coupled to the interrupt channel. Thus, if a normal interrupt producing condition occurs while the interrupt channel is disabled, no interrupt would be produced even if the channel was subsequently enabled, because a transition did not occur whil the interrupt channel was enabled. That particular flag bit would have to occur a second time before another «edge» was produced, causing an interrupt to be generated.

Error conditions in the USART are determined by monitoring the Receive Status Register and the Transmitter Status Register. These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save error conditions during data transfer, the TS 68901 MFP interrupt controller may be used by enabling error interrupts for the desired channel (Receive error or Transmit error) and by masking these bits off. Once the transfer is complete, the Interrupt Pending Register can be polled, to determine the presence of a pending error interrupt, and therefore an error.

Unused bits in the sync character register are zeroed out ; therefore, word length should be set up prior to writing the sync word in some cases. Sync word length is the word length plus one when parity is enabled. The user has to determinate the parity of the sync word when the word length is not 8 bits. the TS 68901 MFP does not add a parity bit to the sync word if the word length is less than 8 bits. The extra bit in the sync word is transmitted as the parity bit. With a word length of eight, and parity selected, the pariry bit for the sync word is computed and added on by the TS 68901 MFP.

$\overline{RR}$ **Receiver ready**
$\overline{RR}$ is asserted when the Buffer Full bit is set in the RSR unless a parity error or frame error is detected by the receiver.

$\overline{TR}$ **Transmitter Ready**
$\overline{TR}$ is asserted when the Buffer Empty bit is set in the TSR unless a break is currently being transmitted.

5

6.6 · Register accesses

All register accesses are dependent on CLK as shown in the timing diagrams. To read a register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The internal read control signal is essentially the combination of $\overline{CS}$, $\overline{DS}$ and R/$\overline{W}$. Thus the read operation will begin when $\overline{CS}$ and $\overline{DS}$ go active and will end when either $\overline{CS}$ or $\overline{DS}$ goes inactive. The address bus must be stable prior to the start of the operation and must remain stable until the end of the operation. Unless a read operation or interrupt acknowledge cycle is inprogress the data bus (D_0 - D_7) will remain in the tri-state condition.

To write a register, $\overline{CS}$ and $\overline{DS}$ must be asserted and R/$\overline{W}$ must be low. The address must be stable prior to the start of the operation and must remain stable until the end of the operation. After the TS 68901 MFP asserts $\overline{DTACK}$ the CPU negates $\overline{DS}$. At this time, the MFP latches the data bus and writes the contents into the appropriate register. Also when $\overline{DS}$ is negated, the MFP rescinds $\overline{DTACK}$.

For an interrupt acknowledge, the operation starts when $\overline{IACK}$ goes low, and ends when $\overline{IACK}$ goes high. The data bus is tri-stated when either $\overline{IACK}$ or $\overline{DS}$ goes high.

When $\overline{CS}$ or $\overline{IACK}$ are asserted the MFP starts an internal cycle. $\overline{DS}$ is needed to enable the address and data buffers. It is recommanded that $\overline{CS}$ and $\overline{IACK}$ be gated by $\overline{DS}$ so that $\overline{DS}$ is always present whenever an MFP bus cycle starts.

6.7 · Reset operation

The reset operation will initialize the CMFP to a known state. The reset operation requires that the RESET input be asserted for a minimun of two microseconds. During a device reset condition, all internal CMFP registers are cleared except fot the timer data registers (TADR, TBDR, TCDR, and TDDR), the USART data register (UDR), the transmitter status register (TSR) and the interrupt vector register. All timers are stopped and the USART receiver and transmitter are disabled. The interrupt channels are also disabled and any pending interrupts are cleared.

In addition, the general purpose interrupt I/O lines are placed in the high-impedance input mode and timer outputs are driven low. External CMFP signals are negated. The interrupt vector register is initialized to a $0F.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipement, tools and operator.

c) Do not handle devices by the leads.

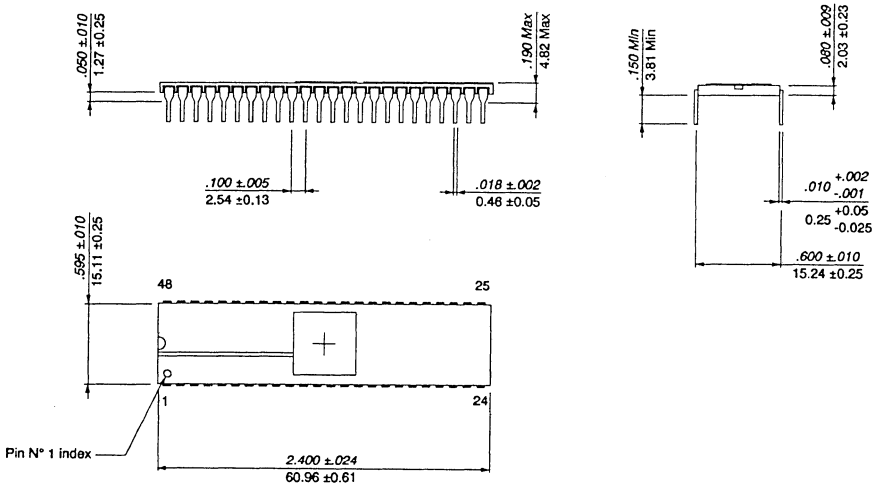
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

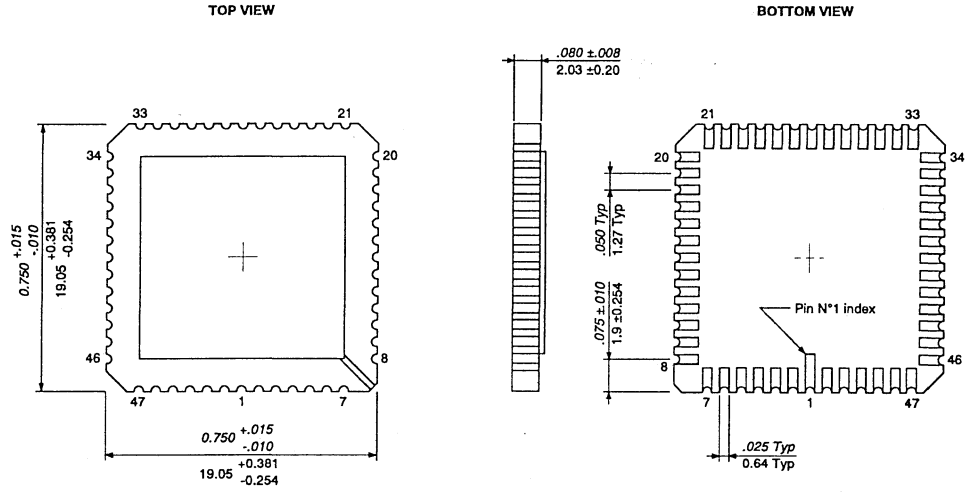
f) Maintain relative humidity above 50 percent, if practicla.

9 · PACKAGE MECHANICAL DATA

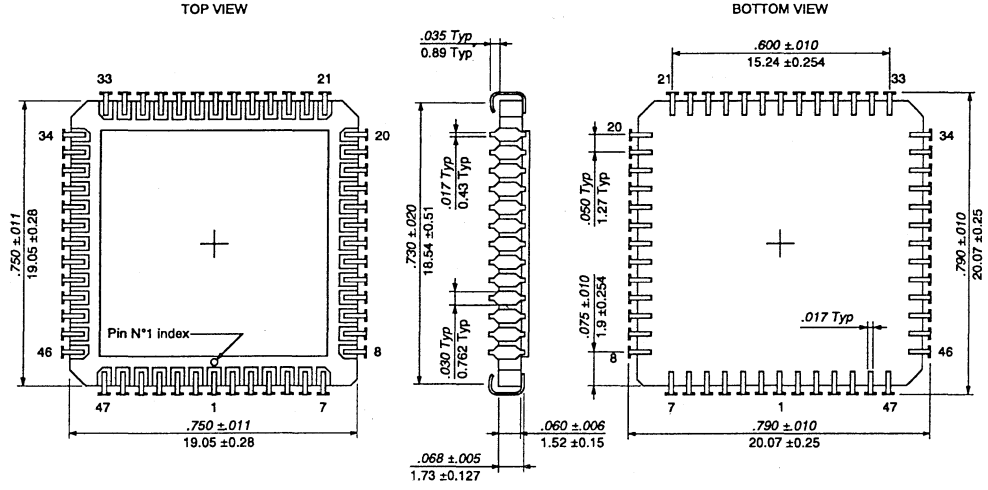
9.1 · 48 Pins · Ceramic side brazed package



9.2 · 52 Pins · Leadless ceramic chip carrier

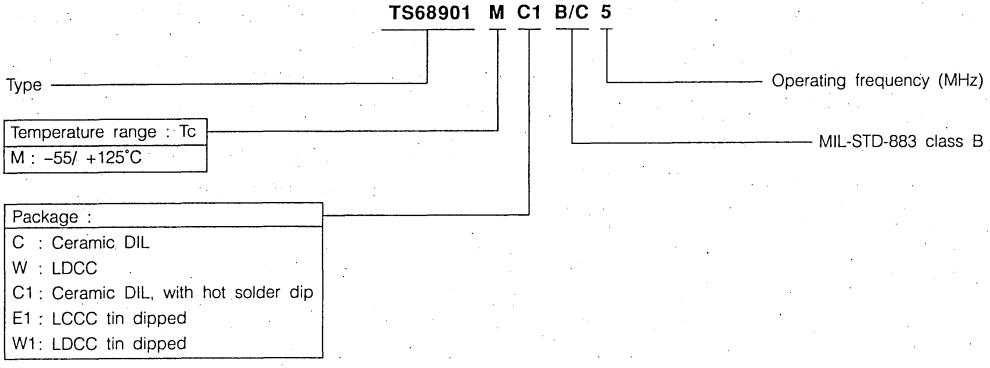


9.3 · 52 Pins · Leaded ceramic chip carrier

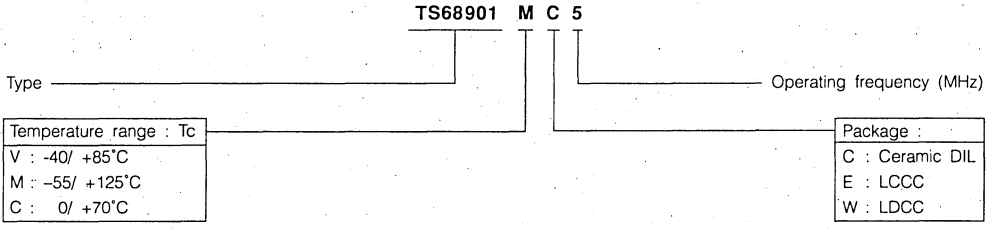


10 - ORDERING INFORMATION

10.1 - MIL-STD-883



10.2 - Standard product



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

10.3 · Detailed ordering information

10.3.1 · Hi-REL product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68901MCB/C4	MIL-STD-883	DIL 48	– 55 / + 125	4	TCS data sheet
TS 68901MCB/C5	MIL-STD-883	DIL 48	– 55 / + 125	5	TCS data sheet
TS 68901ME1B/C4	MIL-STD-883	LCCC 52	– 55 / + 125	4	TCS data sheet
TS 68901ME1B/C5	MIL-STD-883	LCCC 52	– 55 / + 125	5	TCS data sheet
TS 68901MWB/T4	According to MIL-STD-883	LDCC 52*	– 55 / + 125	4	TCS data sheet
TS 68901MWB/T5	According to MIL-STD-883	LDCC 52*	– 55 / + 125	5	TCS data sheet
TS 68901DESC01XA	DESC	DIL 48	– 55 / + 125	4	5962-88506 01XA
TS 68901DESC02XA	DESC	DIL 48	– 55 / + 125	5	5962-88506 02XA
TS 68901DESC01YA	DESC	LCCC 52 + hot solder dip	– 55 / + 125	4	5962-88506 01YA
TS 68901DESC02YA	DESC	LCCC 52 + hot solder dip	– 55 / + 125	5	5962-88506 02YA

* On request.
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

5

10.3.2 · Standard product

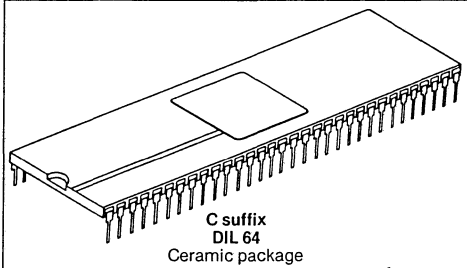
Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68901VC4	TCS standard	DIL 48	– 40 / + 85	4	TCS data sheet
TS 68901VC5	TCS standard	DIL 48	– 40 / + 85	5	TCS data sheet
TS 68901MC4	TCS standard	DIL 48	– 55 / + 125	4	TCS data sheet
TS 68901MC5	TCS standard	DIL 48	– 55 / + 125	5	TCS data sheet
TS 68901ME4	TCS standard	LCCC 52	– 55 / + 125	4	TCS data sheet
TS 68901ME5	TCS standard	LCCC 52	– 55 / + 125	5	TCS data sheet
TS 68901MW4	TCS standard	LDCC 52*	– 55 / + 125	4	TCS data sheet
TS 68901MW5	TCS standard	LDCC 52*	– 55 / + 125	5	TCS data sheet

* On request.
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

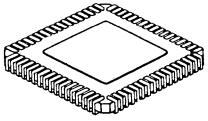
LOW POWER HCMOS 16/32 BIT MICROPROCESSOR

DESCRIPTION

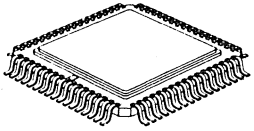
The TS 68C000 reduced power consumption device dissipates an order of magnitude less power than the HMOS TS 68000. The TS 68C000 is an implementation of the TS 68000 16/32 microprocessor architecture. The TS 68C000 has a 16-bit data bus and 24-bit address bus while the full architecture provides for 32-bit address and data-buses. It is completely code-compatible with the HMOS TS 68000, TS 68008 8-bit data bus implementation of the TS 68000 and the TS 68020 32-bit implementation of the architecture. Any user-mode programs written using the TS 68C000 instruction set will run unchanged on the TS 68000, TS 68008 and TS 68020. This is possible because the user programming model is identical for all processors and the instruction sets are proper sub-sets of the complete architecture.



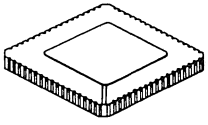
C suffix
DIL 64
Ceramic package



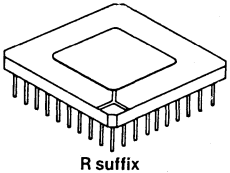
W suffix
LDCC 68
Leaded ceramic chip carrier



F Suffix
CQFP 68
Ceramic quad flat pack (on request)



E suffix
LCCC 68
Leadless ceramic chip carrier



R suffix
PGA 68
Pin grid array

PIN CONNECTIONS (See chapter A2)

See the ordering information at the end of the data sheet.

MAIN FEATURES

- 16/32-bit data and address register.
- 16 megabytes direct addressing range.
- 56 powerful instruction types.
- Operations on five main data types.
- Memory mapped I/O.
- 14 addressing modes.
- 3 available versions : 8 MHz / 10 and 12.5 MHz.
- Military temperature range : − 55 / + 125°C.
- Power supply : 5 V_{DC} ± 10 %.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y) : 90110-007.
- MIL-STD-883 class B.
- DESC drawing 5962-89462.
- TCS standard.

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

This detail specification contains both a summary of the TS 68C000 as well as detailled set of parametrics. The purpose is twofold to provide an instruction to the TS 68C000 and support for the sophisticated user. For detail information on the TS 68C000, refer to «68000 16-Bit Microprocessor User's Manual».

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

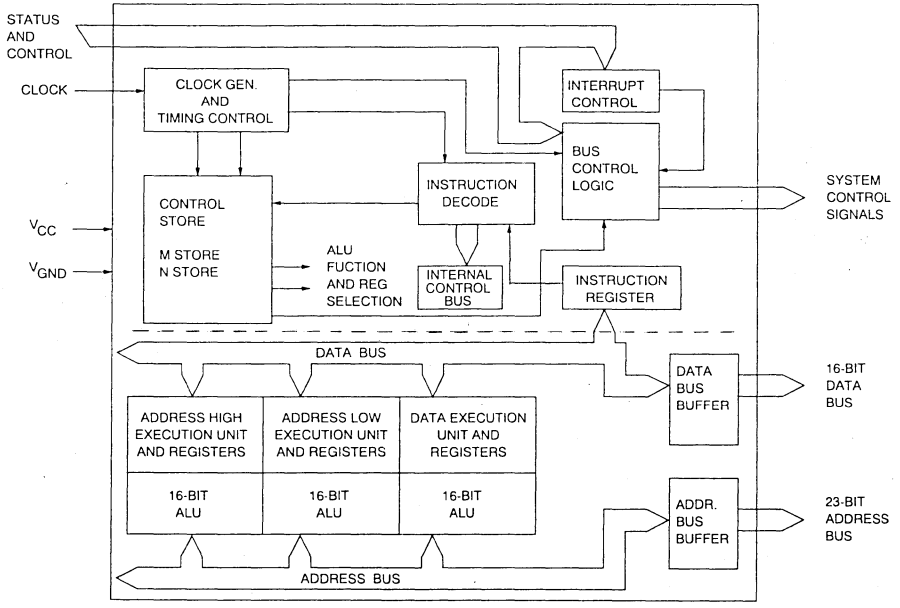


Figure 1 : Block diagram.

5

2 - PIN ASSIGNMENTS

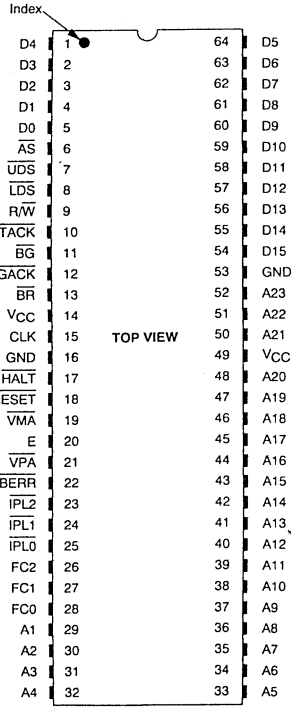


Figure 2.1 : 64-pin dual-in-line package.

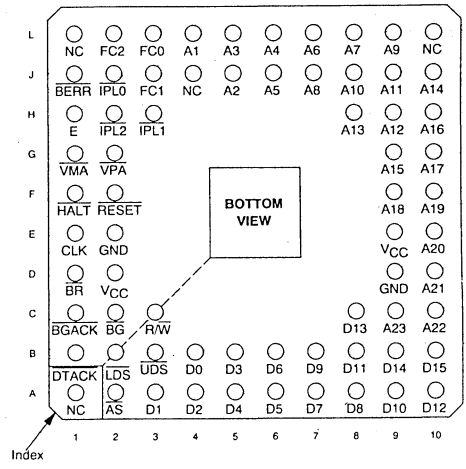


Figure 2.2 : 68-terminal pin grid array.

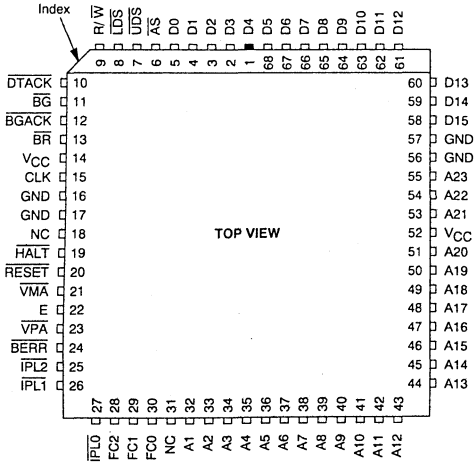


Figure 2.3 : 68-lead quad pack

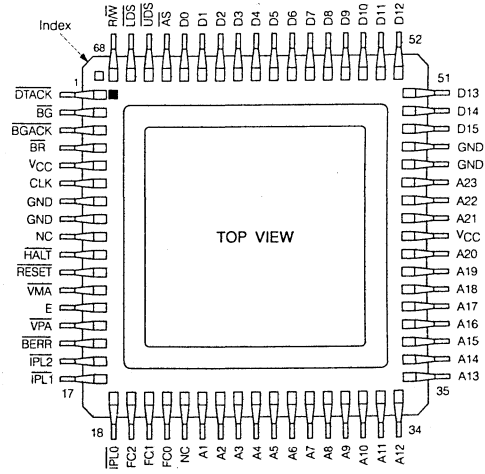


Figure 2.4 : 68-ceramic quad flat pack.

3 - TERMINAL DESIGNATIONS

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply (2 terminals)	Supply
V_{SS}	Power supply (2 terminals)	Terminals
FC0 to FC2	Processor status	Outputs
$\overline{IPL0}$ to $\overline{IPL2}$	Interrupt control	Inputs
A1 to A23	Address Bus	Outputs
AS	Asynchronous Bus Control	Outputs
R / $\overline{W}$		
$\overline{UDS}$		
$\overline{LDS}$		
$\overline{DTACK}$		Input
$\overline{BR}$	Bus arbitration Control	Inputs
$\overline{BGACK}$		
$\overline{BG}$		Output
$\overline{BERR}$	System control	Input
$\overline{RESET}$		Input / Output
$\overline{HALT}$		
$\overline{VPA}$	6800 peripheral control	Input
$\overline{VMA}$		Output
E		Output
CLK	Clock	Input
D0 to D15	Data Bus	Input / Output

* V_{SS} is the reference terminal for the voltages.

4 - SIGNAL DESCRIPTION

The input and output signals are illustrated functionnally in Figure 3 and are described in the following paragraphs.

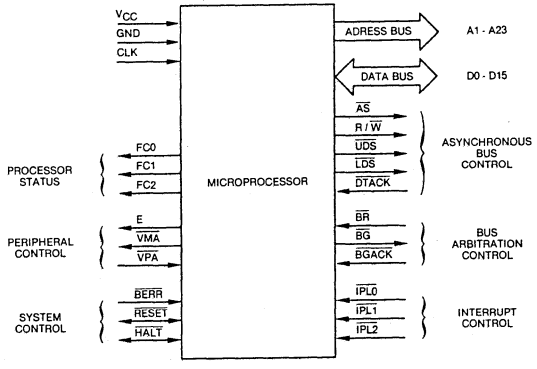


Figure 3 : Input and output signals.

Table 2 - Data strobe control of data bus

$\overline{UDS}$	$\overline{LDS}$	R / $\overline{W}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	Valid data bits 8-15

ADDRESS BUS (A1 THROUGH A23)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 megabytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2 and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are set to a logic high.

DATA BUS (D0 THROUGH D15)

This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL

Asynchronous data transfers are handled using the following control signals : address strobe, read / write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

ADDRESS STROBE ($\overline{AS}$)

This signal indicates that there is a valid address on the address bus.

READ / WRITE (R / $\overline{W}$)

This signal defines the data bus transfer as a read or write cycle. The R / $\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

UPPER AND LOWER DATA STROBE ($\overline{UDS}$, $\overline{LDS}$)

These signals control the flow of data on the data bus, as shown in Table 2. When the R / $\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R / W line is low, the processor will write to the data bus as shown.

DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$)

This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

BUS REQUEST ($\overline{BR}$)

This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

BUS GRANT ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

BUS GRANT ACKNOWLEDGE ($\overline{BGACK}$)

This input indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met :

1 - a bus grant has been received,
2 - address strobe is inactive which indicates that the microprocessor is not using the bus,
3 - data transfer acknowledge is inactive which indicates that neither memory nor peripherals are using the bus, and
4 - bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)

These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in IPL0 and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

SYSTEM CONTROL

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

BUS ERROR ($\overline{BERR}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of :

1 - nonresponding devices,

2 - interrupt vector number acquisition failure,

3 - illegal access request as determined by a memory management unit, or

4 - other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

RESET ($\overline{RESET}$)

This bidirectional signal line acts to reset (start a system initialization sequence) to processor in response to an external reset signal. An internally generated reset (result of a $\overline{RESET}$ instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied at the same time.

HALT ($\overline{HALT}$)

When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped.

EF 6800 PERIPHERAL CONTROL

These control signals are used to allow the interfacing of synchronous EF 6800 peripheral devices with the asynchronous TS 68C000. These signals are explained in the following paragraphs.

ENABLE (E)

This signal is the standard enable signal common to all EF 6800 type peripheral devices. The period for this output is ten TS 68C000 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

VALID PERIPHERAL ADDRESS ($\overline{VPA}$)

This input indicates that the device or region addressed is an TS 68000 Family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt during an IACK cycle.

VALID MEMORY ADDRESS ($\overline{VMA}$)

This output is used to indicate to TS 68000 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is an TS 68000 Family device.

PROCESSOR STATUS (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 3. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

Table 3

Function code output			Cycle time
FC2	FC1	FC0	
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt Acknowledge

CLOCK (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times. The clock is a constant frequency square wave with no stretching or shapping techniques required.

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the microprocessor TS 68C000, 8, 10 and 12.5 MHz, in compliance either with MIL-STD-883 class B or CECC 90000.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38510 : general specifications for microcircuits.

2.2 · CECC 90000

1) CECC 90000.
2) Specification 90110-007.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1, 2.2, 2.3 and 2.4.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- PGA 68 64 LEAD DIP
- 64 DIL SQ. LCC 68 PINS
- 68 LCCC 68 TERMINALS JCC
- 68 LDCC 68 PIN SQ. PGA UP
- 68 CQFP

The precise case outlines are described on figures 9.1, 9.2, 9.3 and 9.4 and into MIL-M-38510.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (Table 4)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 4 - Absolute maximum ratings

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Table 1, § A-3 of this specification.

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+6.5	V
V_I	Input voltage		−0.3	+6.5	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		−0.3	11.0	V
I_o	Output currents		NA	NA	mA
I_i	Input currents		NA	NA	mA
P_{dmax}	Max power dissipation	T_{case} = −55°C		0.27	W
		T_{case} = +125°C		0.27	W
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

5

3.3.2 - Recommended conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 8 and 9)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 5)

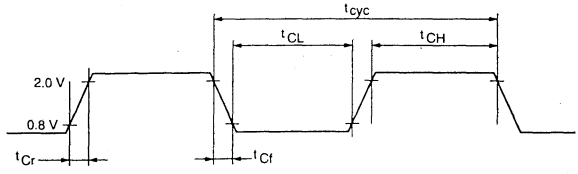
To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 10).

c) Additionnal electrical characteristics (Table 10)

See § 5.5.2.



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 : Clock input timing diagram.

Table 5 · Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Table 1, § A-3 of this specification.

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage	All	4.5	5.5	V
V_{IL}	Low level input voltage	All	0	0.8	V
V_{IH}	High level input voltage (see also § 3.3.3)	All	2.0	V_{CC}	V
T_{case}	Operating temperature	All	− 55	+ 125	°C
R_L	Value of output load resistance	All	Note		Ω
C_L	Output loading capacitance	All		Note	pF
$t_{r(c)}$	Clock rise time (see Figure 4)	All		10	ns
$t_{f(c)}$	Clock fall time (see Figure 4)	All		10	ns
f_c	Clock frequency (see Figure 4)	TS 68C000-8	4.0	8.0	MHz
		TS 68C000-10	4.0	10.0	MHz
		TS 68C000-12	4.0	12.5	MHz
t_{cyc}	Clock time (see Figure 4)	TS 68C000-8	125	250	ns
		TS 68C000-10	100	250	ns
		TS 68C000-12	80	250	ns
$t_{w(CL)}$	Clock pulse width low (see Figure 4)	TS 68C000-8	55	125	ns
		TS 68C000-10	45	125	ns
		TS 68C000-12	35	125	ns
$t_{w(CH)}$	Cycle pulse width high (see Figure 4)	TS 68C000-8	55	125	ns
		TS 68C000-10	45	125	ns
		TS 68C000-12	35	125	ns

Note : Load networks number 1 to 4 as specified in § 5.4 (Figures 5.1 and 5.2) gives the maximum loading for the relevant output.

3.3.3 · Special recommended conditions for C.MOS devices

a) CMOS latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become «latched» in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients ; others may require no additional circuitery.

b) CMOS applications

– The TS 68C000 completely satisfies the input/output drive requirements of CMOS logic devices.

– The HCMOS TS 68C000 provides an order of magnitude power dissipation reduction when compared to the HMOS TS 68000. However, the TS 68C000 does not offer a «power down» or «halt» mode. The minimum operating frequency of the TS 68C000 is 4 MHz.

3.4 · Thermal characteristics

Table 6

Package	Symbol	Parameter	Value	Unit
DIL 64	θ J-A	Thermal resistance Junction to Ambient	25	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
PGA 68	θ J-A	Thermal resistance Junction to Ambient	30	°C/W
	θ J-C	Thermal resistance Junction to Case	6	°C/W
LCCC 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	8	°C/W
LDCC 68	θ J-A	Thermal resistance Junction to Ambient	50	°C/W
	θ J-C	Thermal resistance Junction to Case	10	°C/W
CQFP 68	θ J-A	Thermal resistance Junction to Ambient	40	°C/W
	θ J-C	Thermal resistance Junction to Case	10	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θJ_C. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification

- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 90110-007. Group C inspection is performed on a periodic basis in accordance with CECC 90110-007.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below :

- Table 7 : Static electrical characteristics for all electrical variants.
- Tables 8 and 9 : Dynamic electrical characteristics for 8, 10 and 12.5 MHz.

For static characteristics (Table 7), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Tables 8 and 9).

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause § 3.3.2 here above.

5.2 - Static characteristics

V_{CC} = 5.0 V V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C and T_C = −40°C / +85°C.

Table 7

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.5 V F_C = 8 MHz F_C = 10 MHz F_C = 12 MHz	All		42 45 50	mA
2	V_{OL} (1)	Low level output voltage for : A1 to A23 FC0 to FC2 ; $\overline{BG}$	37	V_{CC} = 4.5 V I_{OL} = 3.2 mA	25°C max min		0.5	V
3	V_{OL} (2)	Low level output voltage for : $\overline{HALT}$	37	V_{CC} = 4.5 V I_{OL} = 1.6 mA	25°C max min		0.5	V
4	V_{OL} (3)	Low level output voltage for : $\overline{AS}$; R/$\overline{W}$: D0 to D15 UDS ; $\overline{LDS}$; $\overline{VMA}$ and E	37	V_{CC} = 4.5 V I_{OL} = 5.3 mA	25°C max min		0.5	V
5	V_{OL} (4)	Low level output voltage for : $\overline{RESET}$	37	V_{CC} = 4.5 V I_{OL} = 5.0 mA	25°C max min		0.5	V
6	V_{OH}	High level output voltage for all outputs	37	V_{CC} = 4.5 V I_{OH} = −400 µA	25°C max min	2.4	V_{CC} −0.75	V
7	I_{IH} (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 5.5 V	25°C max min		2.5	µA
8	I_{IL} (1)	Low level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 0 V	25°C max min	−2.5		µA

Table 7 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
9	I_{IH} (2)	High level input current for : $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 5.5 V	25°C max min		20	µA
10	I_{IL} (2)	Low level input current for $\overline{HALT}$ and $\overline{RESET}$	38	V_{CC} = 5.5 V V_I = 0 V	25°C max min	−20		µA
11	I_{OHZ}	High level output 3-state leakage current		V_{CC} = 5.5 V V_{OH} = 2.4 V	25°C max min		20	µA
12	I_{OLZ}	Low level output 3-state leakage current		V_{CC} = 5.5 V V_{OL} = 0.4 V	25°C max min		20	µA
13	V_{IH}	High level input voltage for all inputs		V_{CC} = 4.5 V V_{CC} = 5.5 V	25°C max min	2.0		V
14	V_{IL}	Low level input voltage for all inputs		V_{CC} = 4.5 V V_{CC} = 5.5 V	25°C max min		0.8 0.8 0.8	V V V
14A	C_{in}	Input capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min		25 NA NA	pF pF pF
14B	C_{out}	Output capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C max min		20 NA NA	pF pF pF
14C	V_{test}	Internal protection Transient energy rating		See Note 9 5 cycles	25°C	−500	+500	V

* Algebraic values.

** Measurement method : see § 5.1. and 5.4.

Refered notes are given in § 5.4.4.

5

5.3 - Dynamic characteristics

V_{CC} = 5.0 V V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C and T_C = −40°C / +85°C.

Table 8A - Dynamic characteristics - TS 68C000-8

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.2.3 (a) to (c) f_C = 8 MHz	25°C max min	20 Note 9		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns

Table 8A - Dynamic characteristics - TS 68C000-8 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
47	t_{su} (SBERCL)	Set-up time BERR low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
2	t_w (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	 55 Note 9	 125	ns
3	t_w (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	 55	 125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		 70	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to AS low	6 - 7	Idem test 27 Load : 4	25°C max min		 60 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to LDS, UDS low	6 - 7	Idem test 27 Load : 4	25°C max min		 60 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to AS high	6 - 7	Idem test 27 Load : 4	25°C max min		 70 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to LDS, UDS high	6 - 7	Idem test 27 Load : 4	25°C max min		 70 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/W high	6 - 7	Idem test 27 Load : 4	25°C max min		 70 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/W low	6 - 7	Idem test 27 Load : 4	25°C max min		 70 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	6 - 7	Idem test 27 Load : 4	25°C max min		 70 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 3	25°C max min		 70	ns
32	t_{HRRF}	RESET / HALT input transition time	6 - 7	Idem test 27	25°C max min		 200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to BG low	8	Idem test 27 Load : 3	25°C max min		 70	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to BG high	8	Idem test 27 Load : 3	25°C max min		 70	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to VMA low	9	Idem test 27 Load : 4	25°C max min		 70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		 70	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	 0		ns

Table 8A - Dynamic characteristics - TS 68C000-8 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min	30 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +90	CLKS Note 2 ns
37	t_{PLH} (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +90	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	7	Idem test 27	25°C max min	20 Note 5	—	ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	20 Note 5	—	ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	30 Note 4	—	ns

* Algebraic values.

** Measurement method : see § 5.4.

Refered notes are given in § 5.4.4.

5

Table 8B - Dynamic characteristics - TS 68C000-10

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.2.3 (a) to (c) f_C = 10 MHz	25°C max min	20 Note 9		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	20 Note 9		ns
2	t_w (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	45	125	ns
3	t_w (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	45	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		60	ns

Table 8B - Dynamic characteristics - TS 68C000-10 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
9	t_{PHL} (CHSLX)	Propagation time clock high to AS low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to LDS, UDS low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to AS high	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to LDS, UDS high	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/W high	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/W low	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 4	25°C max min		60	ns
32	t_{HRRF} (CHGL)	RESET / HALT transition time	6 - 7	Idem test 27	25°C max min		200	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to BG low	8	Idem test 27 Load : 3	25°C max min		60	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to BG high	8	Idem test 27 Load : 3	25°C max min		60	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to VMA low	9	Idem test 27 Load : 4	25°C max min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		55	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	0		ns
11	t_{su} (AVSL)	Set-up time Address valid to AS, LDS, UDS low	6 - 7	Idem test 27 Load : 4	25°C max min	20 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time BR low to BG low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +80	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time BGACK low to BG high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +80	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time BERR low to DTACK low	7	Idem test 27	25°C max min	20 Note 5		ns

Table 8B - Dynamic characteristics - TS 68C000-10 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	 20 Note 5		ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	 20 Note 4		ns

* Algebraic values.
** Measurement method : see § 5.4.
Refered notes are given in § 5.4.4.

Table 8C - Dynamic characteristics - TS 68C000-12

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
27	t_{su} (DICL)	Set-up time Data-in to clock low (Note 1)	6 - 7	See 5.2.3 (a) to (c) f_C = 12 MHz	25°C max min	 10 Note 9		ns
47	t_{su} (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
47	t_{su} (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
47	t_{su} (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
47	t_{su} (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
47	t_{su} (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	6 - 7	Idem test 27	25°C max min	 20 Note 9		ns
2	t_W (CL)	Clock width low	6 - 7	Idem test 27	25°C max min	 35	125	ns
3	t_W (CH)	Clock width high	6 - 7	Idem test 27	25°C max min	 35	125	ns
6A	t_{PLH} t_{PHL} (CHFCV)	Propagation time clock high to FC valid	6 - 7	Idem test 27 Load : 3	25°C max min		55	ns
9	t_{PHL} (CHSLX)	Propagation time clock high to $\overline{AS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
9	t_{PHL} (CHSL)	Propagation time CLK high to $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{AS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		50 Note 3	ns
12	t_{PLH} (CLSH)	Propagation time CLK low to $\overline{LDS}$, $\overline{UDS}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		50 Note 3	ns

5

Table 8C - Dynamic characteristics - TS 68C000-12 (Continued)

Test Nbr	Symbol	Parameter	Figure Number (**)	Test Conditions	Test Temp.	Limits Min (*)	Limits Max (*)	Unit
18	t_{PLH} (CHRHX)	Propagation time CLK high to R/$\overline{W}$ high	6 - 7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
20	t_{PHL} (CHRL)	Propagation time CLK high to R/$\overline{W}$ low	7	Idem test 27 Load : 4	25°C max min		60 Note 3	ns
23	t_{PZL} t_{PZH} (CLDO)	Propagation time CLK low to Data-out valid	7	Idem test 27 Load : 4	25°C max min		55 Note 3	ns
6	t_{PZL} t_{PZH} (CLAV)	Propagation time CLK low to Address valid	6 - 7	Idem test 27 Load : 4	25°C max min		55	ns
32	t_{HRRF}	$\overline{RESET}$ / $\overline{HALT}$ transition time	6 - 7	Idem test 27	25°C max min		150	ns
33	t_{PHL} (CHGL)	Propagation time CLK high to $\overline{BG}$ low	5	Idem test 27 Load : 3	25°C max min		50	ns
34	t_{PLH} (CHGH)	Propagation time CLK high to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min		50	ns
40	t_{PHL} (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	9	Idem test 27 Load : 4	25°C max min		70	ns
41	t_{PHL} (CLE)	Propagation time CLK low to E low	9	Idem test 27 Load : 4	25°C max min		45	ns
8	t_h (SHAZ)	Hold time CLK high to Address	6 - 7	Idem test 27 Load : 3	25°C max min	0		ns
11	t_{su} (AVSL)	Set-up time Address valid to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ low	6 - 7	Idem test 27 Load : 4	25°C max min	15 Note 4		ns
35	t_{PHL} (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +70	CLKS Note 2 ns
37	t_{PLH} (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	8	Idem test 27 Load : 3	25°C max min	1.5	3.5 +70	CLKS Note 2 ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	7	Idem test 27	25°C max min	20 Note 5		ns
48	t_{su} (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	6 - 7	Idem test 27	25°C max min	20 Note 5		ns
26	t_h (DOSL)	Hold time Data-out valid to $\overline{LDS}$, $\overline{UDS}$ low	7	Idem test 27 Load : 4	25°C max min	15 Note 4		ns

* Algebraic values.

** Measurement method : see § 5.4.

Refered notes are given in § 5.4.4.

Table 9 - AC electrical specification - clock timing

Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f	Frequency of operation	4.0	8.0	4.0	10.0	4.0	12.5	MHz
t_{cyc}	Cycle time	125	250	100	250	80	250	ns
t_{CL} t_{CH}	Clock pulse width	55 55	125 125	45 45	125 125	35 35	125 125	ns
t_{Cr} t_{Cf}	Rise and fall time		10 10		10 10		10 10	ns

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Tables 8, refering to the loading network number as shown in Figures 5.1 and 5.2 below.

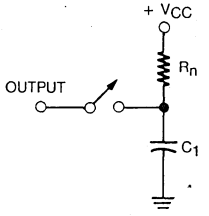


Figure 5.1 : Passive loads.

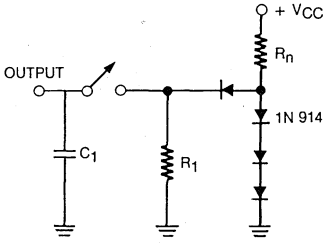


Figure 5.2 : Active loads.

Load NBR	Figure	R_1	R_n	C_1*	Output application
1	5.1	—	910 Ω	130 pF	$\overline{\text{RESET}}$
2	5.1	—	2.9 kΩ	70 pF	$\overline{\text{HALT}}$
3	5.2	6.0 k	1.22 kΩ	130 pF	A1 to A23, $\overline{\text{BG}}$ and FC0 to FC2
4	5.2	6.0 k	740 Ω	130 pF	All other outputs
* C_1 includes all parasitic capacitances of test machines.					

5.4.2 - Time definitions

The times specified in Table 8 as dynamic characteristics are defined in Figures 6 to 9 below by a reference number given column «Method» of the tables together with the relevant figure number.

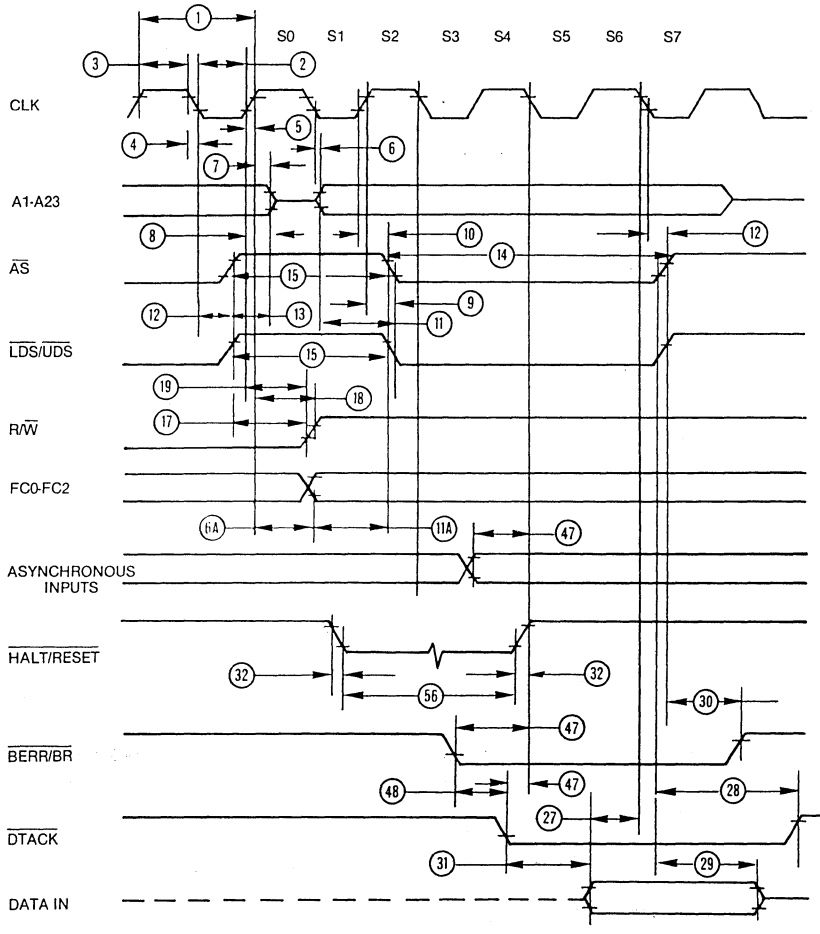


Figure 6 : Read cycle timing.

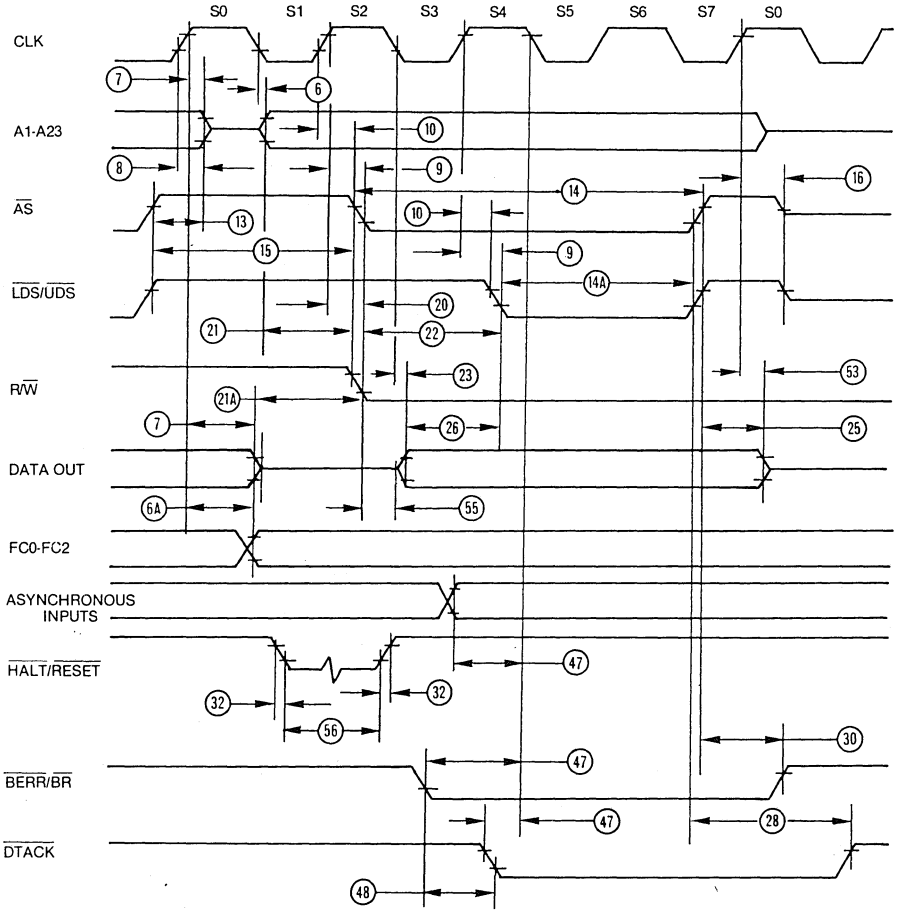


Figure 7 : Write cycle timing.

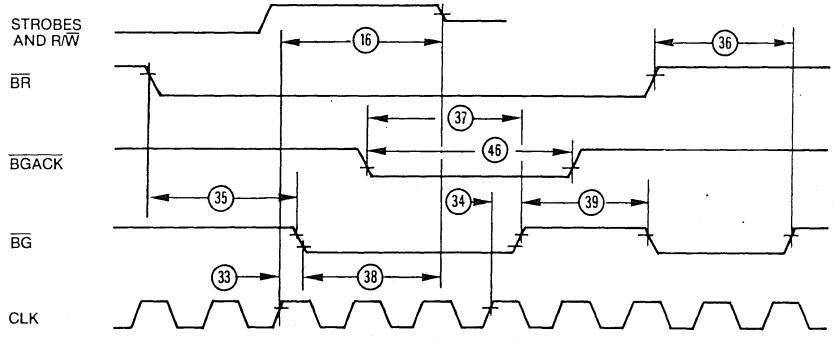


Figure 8 : AC electrical waveforms - bus arbitration.

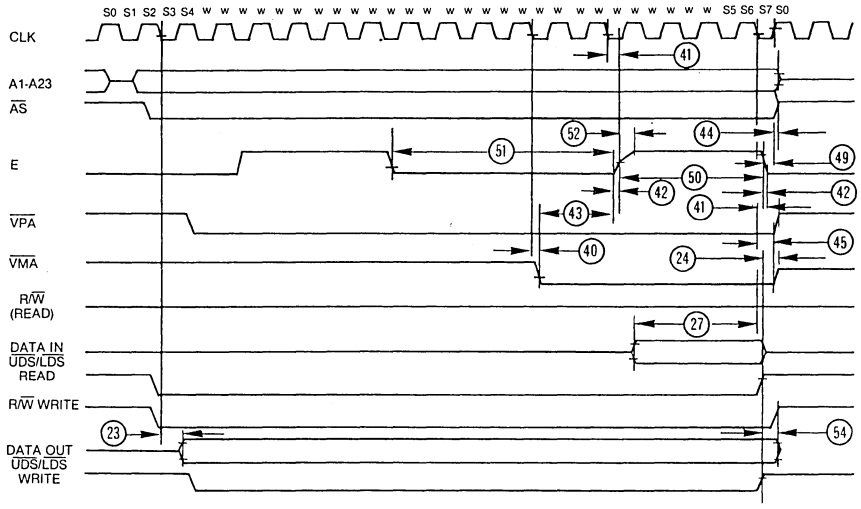


Figure 9 : Enable / interface timing.

5.4.3 · Input and output signals for dynamic measurements

a) Input pulse characteristics

Where input pulse generator is loaded by only a 50 Ω resistor, the input pulse characteristics shall be as shown in Figure 10.

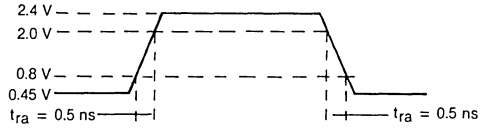


Figure 10 : Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be :

V_{IL} = 0.8 V

V_{IH} = 2.0 V

c) Time measurement output voltage reference for valid state output

Where output ios (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in Figure 11.

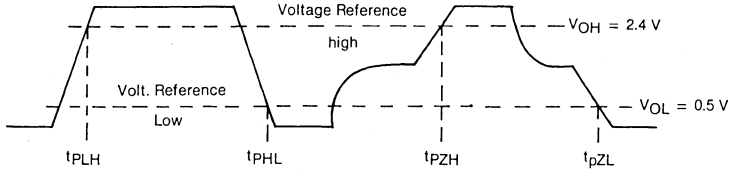


Figure 11 : Output voltage references.

5.4.4 · Refered notes to the Tables 7 and 8

The following notes shall apply where refered into the Tables 8 and 9 and/or additional information given in § 5.5.2 of this specification.

Note 1 : If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.

Note 2 : Where «CLKS» is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.

Note 3 : For a loading capacitance of less than or equal to 50 picofarads, substract 5 nanoseconds from the value given in the maximum columns.

Note 4 : Actual value depends on actual period.

Note 5 : If 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.

Note 6 : The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

Note 7 : The falling edge of 56 triggers both the negation of the strobes ($\overline{AS}$, and X $\overline{DS}$) and the falling edge of E. either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

Note 8 : When $\overline{AS}$ and R / $\overline{W}$ are equally loaded (± 20 %), substract 10 nanoseconds from the values in these columns.

Note 9 : Each terminal of the device under test shall be tested separately against all existing V_{CC} and V_{SS} terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in Table 8.

5.5 · Additional information

Additional information shall not be for any inspection purposes.

5.5.1 · Power considerations

See § 3.4.

5.5.2 · Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 6 to 9 and loading number refer to Figures 5.1 and 5.2 (see § 5.4 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2 of this specification.

Table 10

Item Nbr	Symbol	Parameter	Ref Nbr	Load Nbr	TS 68C000-8 Limits Min	TS 68C000-8 Limits Max	TS 68C000-10 Limits Min	TS 68C000-10 Limits Max	TS 68C000-12 Limits Min	TS 68C000-12 Limits Max	Unit
6A	V_{OH}	High level output voltage for E with pullup R = 1.1 K to V_{CC}			min	V_{CC} - 0.75	min	V_{CC} - 0.75	min	V_{CC} - 0.75	V
37	t_{PLZ} t_{PHZ} (CLAZX)	Propagation time CLK low to Address 3-state	Fig. 6 Ref. 7	3		80		70		60	ns
39	t_{PHZ} (CHSZX)	Propagation time CLK high to $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ 3-state	Fig. 7 Ref. 16	4		80		70		60	ns
40	t_{PLZ} t_{PHZ} (CHRZ)	Propagation time CLK high to R / $\overline{W}$ 3-state	Fig. 8 Ref. 16	4		80		70		60	ns
41	t_{PHZ} t_{PLZ} (CHAZX)	Propagation time CLK high to Data 3-state	Fig. 7 Ref. 7	4		80		70		60	ns
43	t_h (SHAZ)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Address	Fig. 6 Ref. 13	3	30		20		10		ns
44	t_w (SL)	$\overline{AS}$/DS width low	Fig. 6 Ref. 14		240 Note 4		195 Note 4		160 Note 4		ns
45	t_w (SL)	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ width high	Fig. 6 Ref. 15		150 Note 4		105 Note 4		65 Note 4		ns
46	t_{su} (SHRH)	Set-up time $\overline{LDS}$, $\overline{UDS}$ high to R / $\overline{W}$ high	Fig. 6 Ref. 17	4	40 Note 4		20 Note 4		10 Note 4		ns
47	t_{su} (AVRL)	Set-up time Address valid to R / $\overline{W}$ low	Fig. 6 Ref. 21	4	20 Note 4		0 Note 4		0 Note 4		ns

Table 10 (Continued)

Item Nbr	Symbol	Parameter	Ref Nbr	Load Nbr	TS 68C000-8 Limits		TS 68C000-10 Limits		TS 68C000-12 Limits		Unit
					Min	Max	Min	Max	Min	Max	
48	t_{PHL} (RLSL)	Propagation time R / $\overline{W}$ low to lds, uds low	Fig. 7 Ref. 22	4	80 Note 4		50 Note 4		30 Note 4		ns
49	t_h (SHDO)	Hold time $\overline{LDS}$, $\overline{UDS}$ high to Data-out	Fig. 7 Ref. 25	4	30 Note 4		20 Note 4		15 Note 4		ns
50	t_h (SHDI)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to Data-in	Fig. 6 Ref. 29		0		0		0		ns
52	t_h (BRHGH)	Propagation time $\overline{BR}$ high to $\overline{BG}$ high (Note 6)	Fig. 8 Ref. 36	3	1.5	3.5 + 90	1.5	3.5 + 80	1.5	3.5 + 70	CLKS Note 2 ns
54	t_{PHZ} t_{PLZ} (GLZ)	Propagation time $\overline{BG}$ low to Data and Address 3-state	Fig. 8 Ref. 36	BG, address 3 Data 4		80		70		60	ns
55	t_w (GH)	$\overline{BG}$ width high	Fig. 8 Ref. 39		1.5		1.5		1.5		CLKS ns
56	t_{PLH} (VMLEH)	Propagation time $\overline{VMA}$ low to E high	Fig. 9 Ref. 43	4	200		150		90		ns
57	t_h (SHVPH)	Hold time $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ high to VPA high	Fig. 20 Ref. 44 (see § 6.6.3)	4	0	120	0	90	0	70	ns
58	t_h (ELAI)	Hold time E low to address	Fig. 9 Ref. 45	3	30		10		10		ns
59	t_w (BGL)	$\overline{BGACK}$ width low	Fig. 8 Ref. 46		1.5		1.5		1.5		CLKS Note 2
61	t_w (EH)	E width high	Fig. 9 Ref. 50		450		350		280		ns
62	t_w (EL)	E width low	Fig. 9 Ref. 51		700		550		440		ns
63	t_{PHL} (FCVSL)	Propagation time FC valid to $\overline{AS}$, $\overline{DS}$ low	Fig. 6 Ref. 1A or 11A	4	60 Note 4		50 Note 4		40 Note 4		ns
64	t_{PHL} (SHDAH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	Fig. 6 Ref. 28	4	0	245 Note 4	0	190 Note 4	0	150 Note 4	ns
65	t_{PLH} (SHBEH)	Propagation time $\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high	Fig. 8 Ref. 30	4	0		0		0		ns
66	t_{su} (DALDI)	Set-up time $\overline{DTACK}$ low to Data-in (Note 1)	Fig. 6 Ref. 31			90 Note 4		65 Note 4		50 Note 4	ns
67	t_{THL} t_{TLH} (RH)	Transition time $\overline{HALT}$, $\overline{RESET}$ input	Fig. 6 Ref. 32			200		200		200	ns
69	t_w (HRPW)	$\overline{HALT}$ and $\overline{RESET}$ pulse width after power up	Fig. 6 Ref. 56		10		10		10		CLKS Note 2
70	t_{PHL} (ASRV)	Propagation time $\overline{AS}$ low to R / $\overline{W}$ valid	Fig. 7 Ref. 20A	4		20 Note 8		20 Note 8		20 Note 8	ns
71	t_{PHL} (FCVRL)	Propagation time FC valid to R / $\overline{W}$ low	Fig. 7 Ref. 21A	4	60 Note 4		50 Note 4		30 Note 4		ns
73	t_h (CHDOI)	Hold time CLK high to Data-out	Fig. 7 Ref. 53	4	0		0		0		ns
74	t_{PLH} t_{PHL} (RLDBO)	Propagation time R / $\overline{W}$ low to Data-bus impedance change	Fig. 7 Ref. 55	4	30		20		10		ns
75	t_{PHL} (SHEL)	Propagation time $\overline{AS}$, $\overline{DS}$ low to E low	Fig. 9 Ref. 49	4 Note 7	− 70	+ 70	− 55	+ 55	− 45	+ 45	ns
76	t_h (ELDOI)	Hold time E low to Data-out	Fig. 9 Ref. 54	4	30		20		15		ns

Refered notes are given in § 5.4.4.

6 · FUNCTIONAL DESCRIPTION

6.1 · Description of registers

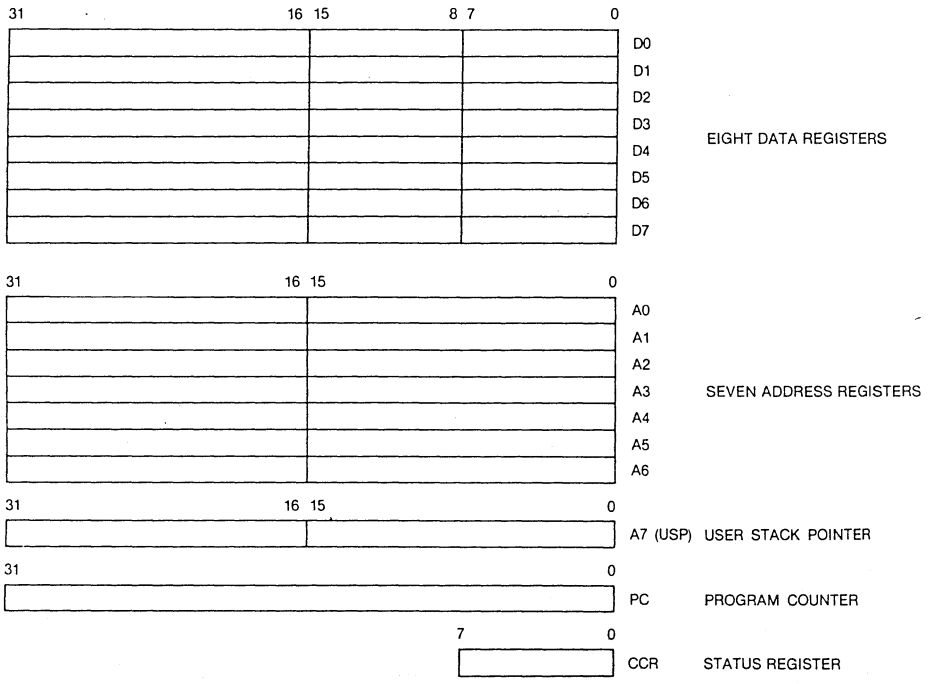


Figure 12 : User programming model.

As shown in the user programming model (Figure 12), the TS 68C000 offers 16/32-bit registers and a 32-bit program counter. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 16 registers may be used as index registers.

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in Figure 13.

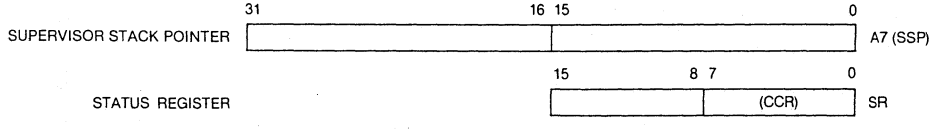


Figure 13 : Supervisor programming model supplement.

The status register (Figure 14) contains the interrupt mask (eight levels available) as well as the condition codes : extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

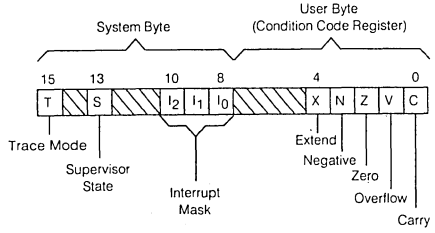


Figure 14 : Status register.

6.2 · Data types and addressing modes

Five basic data types are supported. These data types are :

- Bits
- BCD Digits (4 Bits)
- Bytes (8 Bits)
- Words (16 Bits)
- Long Words (32 Bits)

In addition, operations on other data types such as memory addresses, status word data, etc. are provided in the instruction set.

The 14 addressing modes, shown in Table 11, include six basic types :

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Immediate
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

6.3 · Data transfer operations

Transfer of data between devices involves the following leads :

1 - address bus A1 through A23,

2 - data bus D0 through D15, and

3 - control signals.

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the TS 68C000 for interlocked multiprocessor communications.

READ CYCLE

During a read cycle, the processor receives data from the memory of a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobes is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions is internally.

WRITE CYCLE

During a write cycle, the processor sends data to either the memory of a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued.

Table 11 · Addressing modes

Addressing Modes	Syntax
Register Direct Addressing	
Data Register Direct	Dn
Address Register Direct	An
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Program Counter Relative Addressing	
Relative with Offset	d_{16}(PC)
Relative with Index Offset	d_8(PC,Xn)
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An) +
Predecrement Register Indirect	− (An)
Register Indirect with Offset	d_{16}(An)
Indexed Register Indirect with Offset	d_8(An,Xn)
Immediate Data Addressing	
Immediate	= XXX
uick Immediate	= 1- = 8
Implied Addressing	
Implied Register	SR / USP / SP / PC

Notes :

Dn = Data Register.
An = Address Register.
Xn = Address of Data Register used as Index Register.
SR = Status Register.
PC = Program Counter.
SP = Stack Pointer.
USP = User Stack Pointer.
( ) = Effective Address.
d_8 = 8-Bit Offset (Displacement).
d_{16} = 16-Bit Offset (Displacement).
= xxx = Immediate Data.

5

Table 12 - Instruction set summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Lead Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the datra back to the same address. In the TS 68C000, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write are byte operations.

6.4 - Instruction set overview

The TS 68C000 instruction set is shown in Table 12. Some additional instructions are variations, or sub-sets, of these and they appear in Table 13. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, «quick» arithmetic operations, BCD arithmetic, and expanded operations (through traps).

Table 13 - Variations of instruction types

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical AND And Immediate And Immediate to Condition Codes And Immediate to Status Register
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Move Address Move Multiple Registers Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract Extend

5

6.5 - Processing states

The TS 68C000 is always in one of three processing states : normal, exception, or halted.

NORMAL PROCESSING

The normal processing state is that associated with instruction execution ; the memory references are to fetch instructions and operands, and to store results. A special case of normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

EXCEPTION PROCESSING

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

HALTED PROCESSING

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus errors occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

Asserting the reset and halt line for ten cycles will cause a processor reset, except when V_{CC} is initially applied to the processor. In this case, an external reset must be applied for least 100 milliseconds.

6.6 - Interface with EF 6800 peripherals

Extensive line of EF 6800 peripherals are directly compatible with the TS 68C000.

Note : It is the own user's responsibility to verify the actual EF 6800 peripheral performances to be compatible to the actual used TS 68C000 microprocessor performances.

Some of the EF 6800 peripheral that are particulary useful are :

EF 6821 : Peripheral Interface Adapter

EF 6840 : Programmable Timer Module

EF 6850 : Asynchronous Communications Interface Adapter

EF 6852 : Synchronous Serial Data Adapter

EF 6854 : Advanced Data Link Controller

To interface the synchronous EF 6800 peripherals with the asynchronous TS 68C000, the processor modifies its bus cycle to meet the EF 6800 cycle requirements whenever an EF 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 15 is a flowchart of the interface operation between the processor and EF 6800 devices.

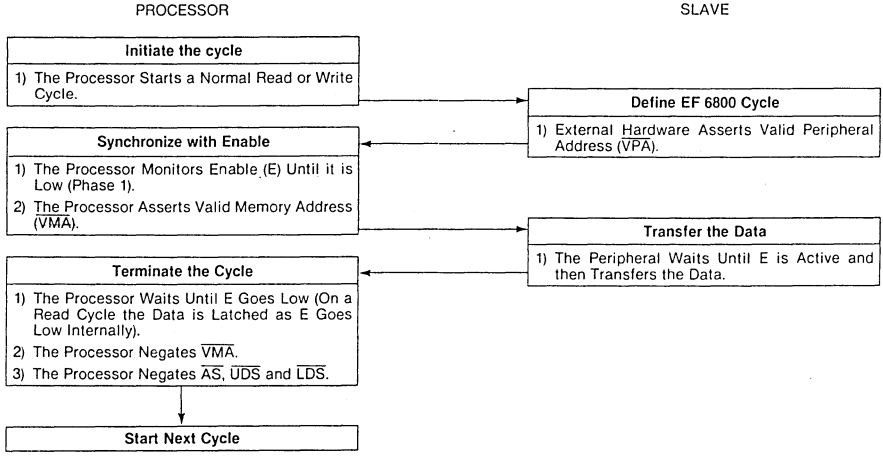


Figure 15 : EF 6800 interfacing flowchart.

6.6.1 · Data Transfer Operation

Three signals on the processor provide the EF 6800 interface. They are : enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or phase 2 signal in existing EF 6800 systems. The bus frequency is one tenth of the incoming TS 68C000 clock frequency. The timing of E allows 1 MHz peripherals to be used 8 MHz TS 68C000. Enable has a 60/40 duty cycle, that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

EF 6800 cycle timing is given in Figures 16, 17, 19 and 20. At state zero (SO) in the cycle, the address bus is in the high-impedance state. A function code is asserted on the function code output lines. One-half clock later, in state 1, the address bus is released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R / $\overline{W}$) signal is switched to low (write) during state 2. One-half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$.

The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an EF 6800 device (or an area reserved for EF 6800 devices) and that the bus should conform to the phase 2 transfer characteristics of the EF 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the EF 6800 peripherals should be derived by decoding the address bus conditioned by $\overline{VMA}$.

After recognition of $\overline{VPA}$, the processor assures that the enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the EF 6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 16 and 17 depict the best and worst case EF 6800 cycle timing. This cycle length is dependent strictly upon when $\overline{VPA}$ is asserted in relationship to the E clock.

If we assume that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of S4. In this case, no «extra» wait cycles will be inserted prior to the recognition of $\overline{VPA}$ asserted and only the wait cycles inserted to synchronize with the E clcok will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes :

1 - Best Case - $\overline{VPA}$ is recognized as being asserted on the falling edge three clock cycles before E rizes (or three clock cycles after E falls).

2 - Worst Case - $\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one-half clock cycle later in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after the address strobe is negated.

$\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted. Notice that the TS 68C000 $\overline{VMA}$ is active low, constrasted with the active high EF 6800 $\overline{VMA}$. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting the peripherals.

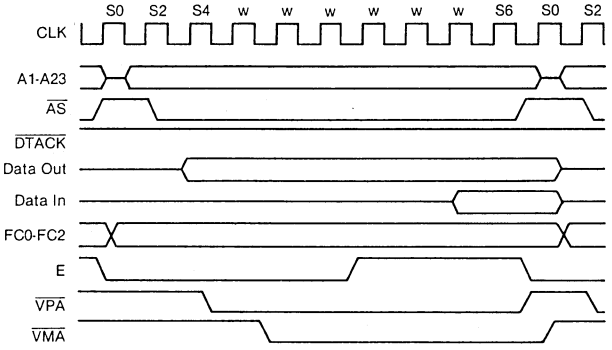


Figure 16 : TS 68C000 to EF 6800 peripheral timing - best case.

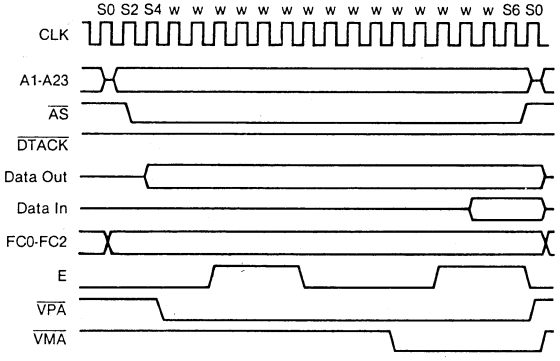


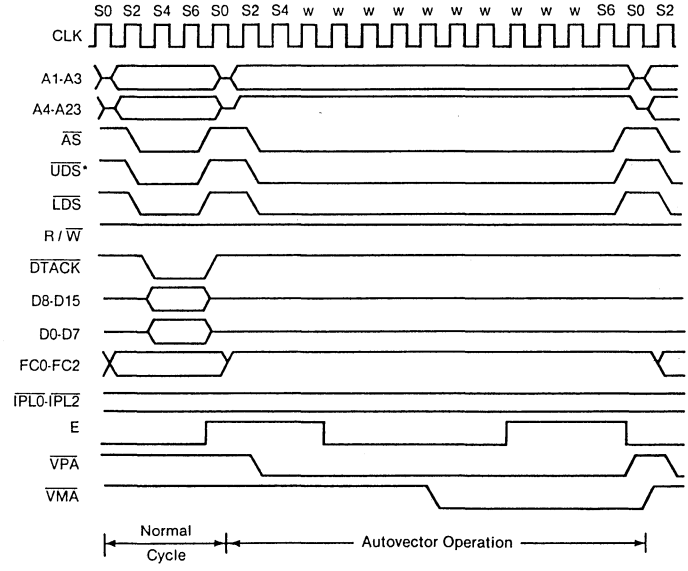
Figure 17 : TS 68C000 to EF 6800 peripheral timing - worst case.

6.6.2 · Interrupt Interface Operation

During an interrupt acknowledge cycle while the processor is fetching the vector, the $\overline{VPA}$ is asserted, the TS 68C000 will assert $\overline{VMA}$ and complete a normal EF 6800 read cycle as shown in Figure 18. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is know as autovectoring. The seven autovectors are vector number 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the EF 6800 interrupt sequence. The basic difference is that there are six normalinterrupt vectors and one NMI type vector. As with both the EF 6800 and the TS 68C000's normal vectored interrupt, the interrupt service routine can be located any-where in the address space. This is due to the fact that while the vector numbers are fixed the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring. The EF 6800 peripheral address decoding should prevent unintended accesses.



Allthrough $\overline{UDS}$ and $\overline{LDS}$ are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally).

Figure 18 : Autovector operation timing diagram.

6.6.3 · Dynamic electrical characteristics TS 68C000 to EF 6800 peripheral

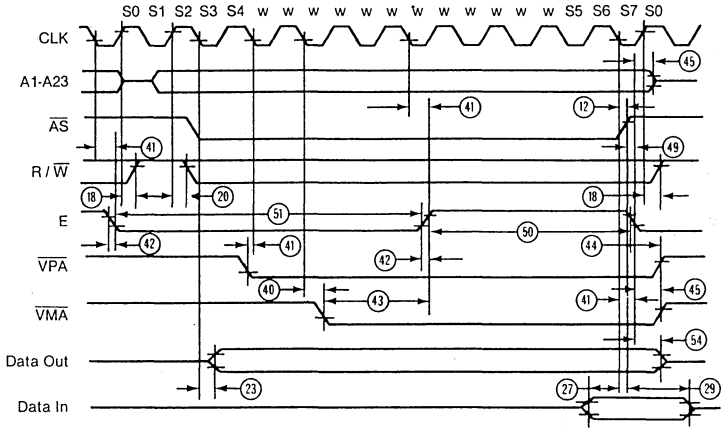
Num.	Symbol	Parameter	8 MHz Limits		10 MHz Limits		12.5 MHz Limits		Unit
			Min	Max	Min	Max	Min	Max	
12	CLSH	Clock low to $\overline{AS}$, $\overline{DS}$ high (see Note 1)		70		55		50	ns
18	CHRH	Clock high to R / $\overline{W}$ high (see Note 1)	0	70	0	60	0	60	ns
20	CHRL	Clock high to R / $\overline{W}$ low (write) (see Note 1)		70		60		60	ns
23	CLDO	Clock low to data out valid (write)		70		55		55	ns
27	CLDO	Data in to clock low (setup time on read) (see Note 2)	15		10		10		ns
29	SHDII	$\overline{AS}$, $\overline{DS}$ high to Data in invalid (hold time on read)	0		0		0		ns
40	CLVML	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high		70		70		70	ns
41	CLET	Clock low to E transition		70		55		45	ns
42	Erf	E output rise and fall time		25		25		25	ns
43	VMLEH	$\overline{VMA}$ low to E high	200		150		90		ns
44	SHVPH	$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	0	120	0	90	0	70	ns
45	ELCAI	E low to control, address bus invalid (address hold time)	30		10		10		ns
47	ASI	Asynchronous input setup time (see Note 2)	20		20		20		ns
49	SHEL	$\overline{AS}$, $\overline{DS}$ high to E low (see Note 3)	−70	70	−55	55	−80		ns
50	EH	E width high	450		350		280		ns
51	EL	E width low	700		550		440		ns
54	ELDOI	E low to data out invalid	30		20		15		ns

Note 1 : For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

Note 2 : If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) required can be ignored. The data must only satisfy the date in clock-low setup time (27) for the following cycle.

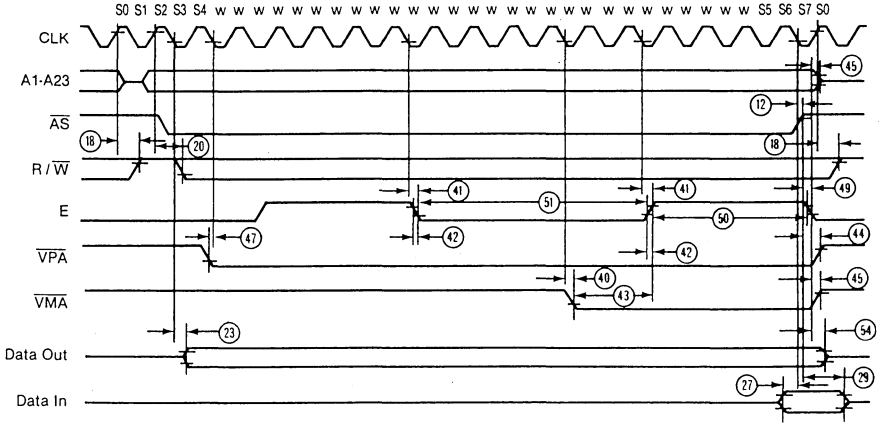
Note 3 : The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and × $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

5



Note : This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly atteinable.

Figure 19 : TS 68C000 to EF 6800 peripheral timing diagram - best case.



Note : This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly atteinable.

Figure 20 : TS 68C000 to EF 6800 peripheral timing diagram - worst case.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

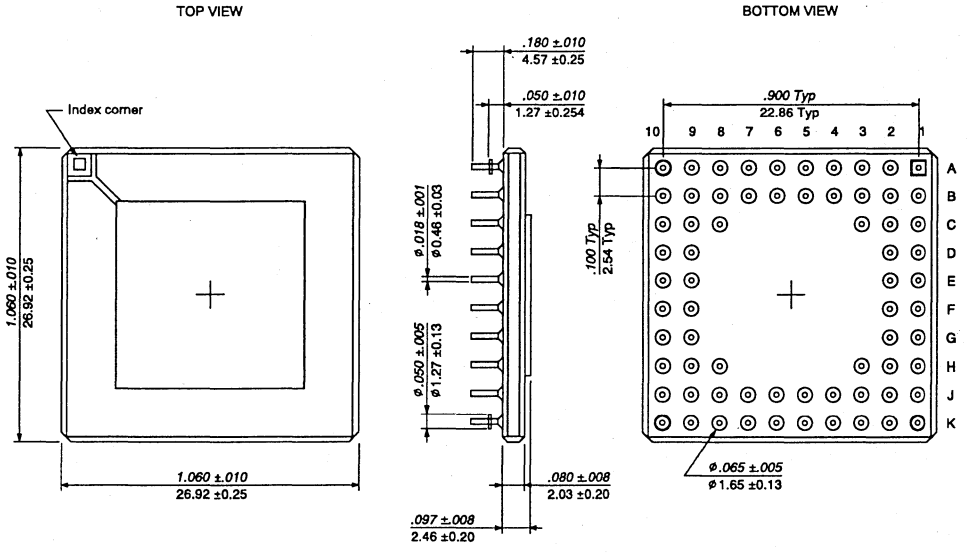
8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

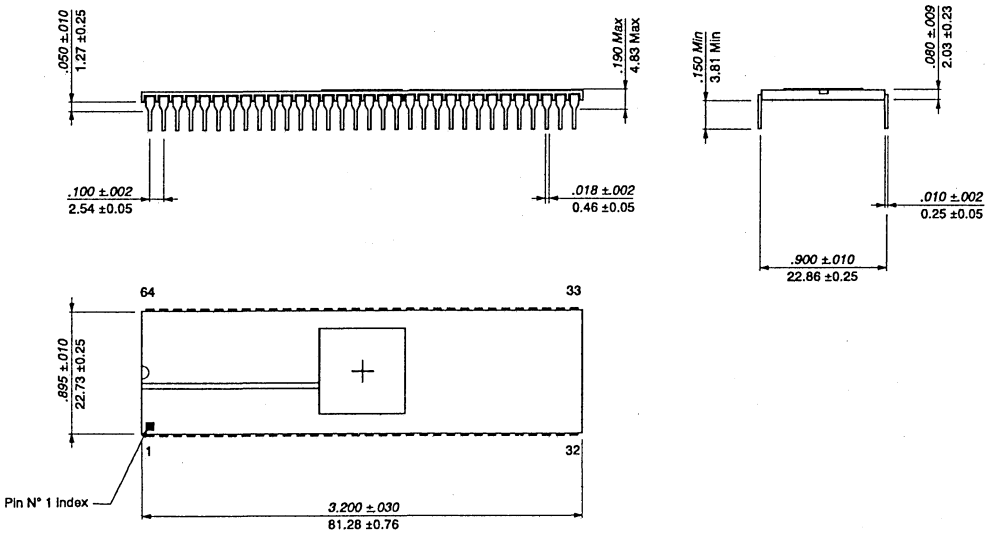
9 - PACKAGE MECHANICAL DATA

9.1 - 68 pins - Pin grid array

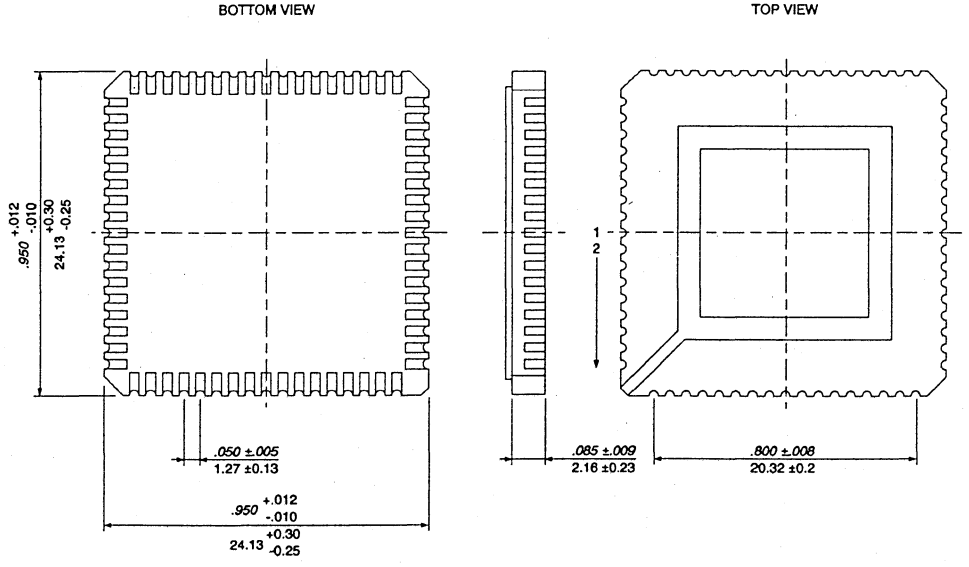


5

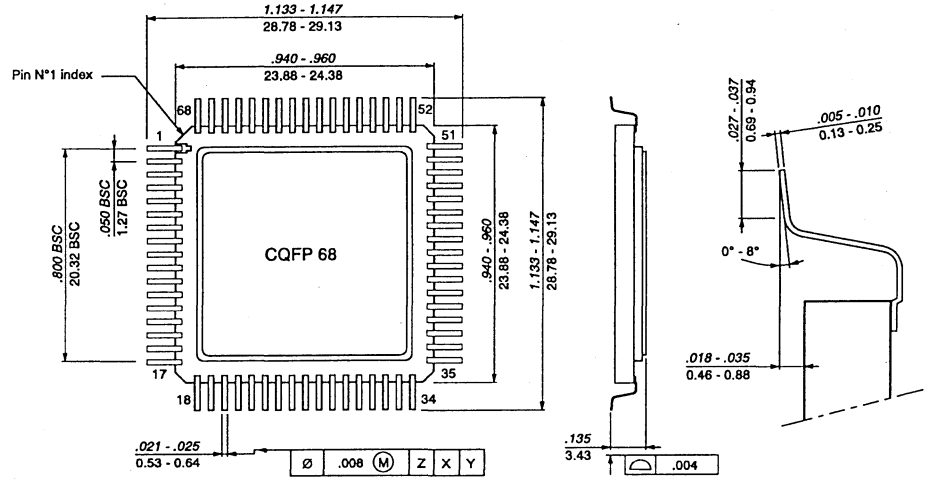
9.2 · 64 pins · Ceramic side brazed package



9.3 · 68 pins · Leadless ceramic chip carrier

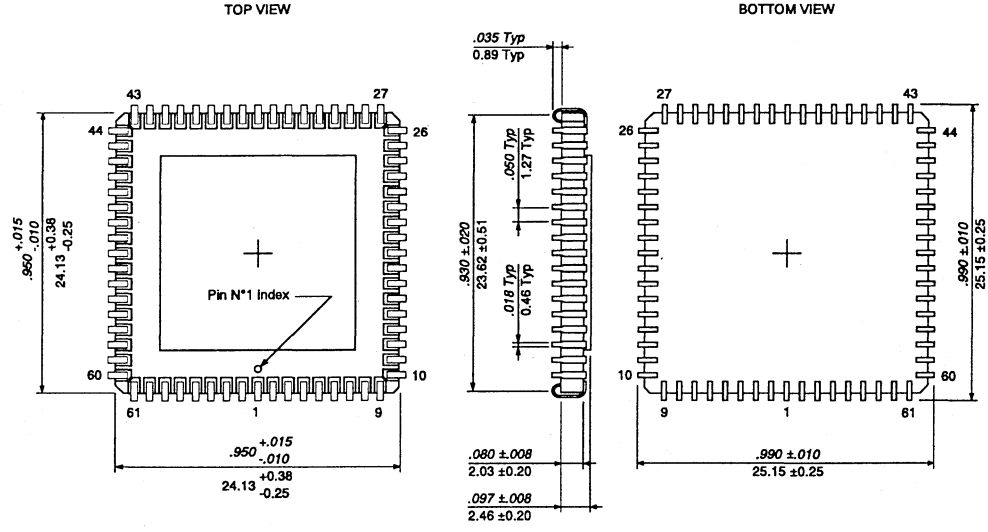


9.4 - 68 pins - Ceramic quad flat pack



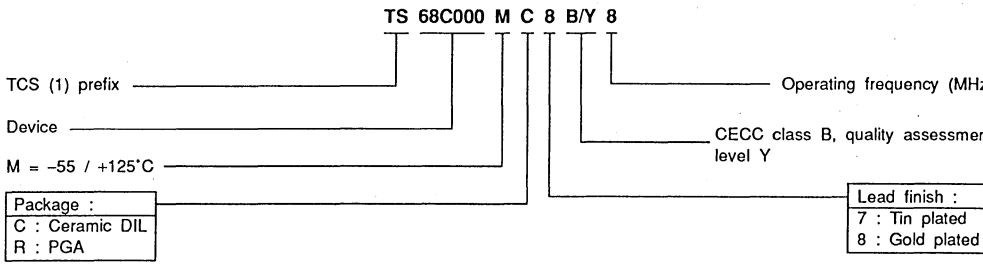
5

9.5 - 68 pins - Leaded ceramic chip carrier

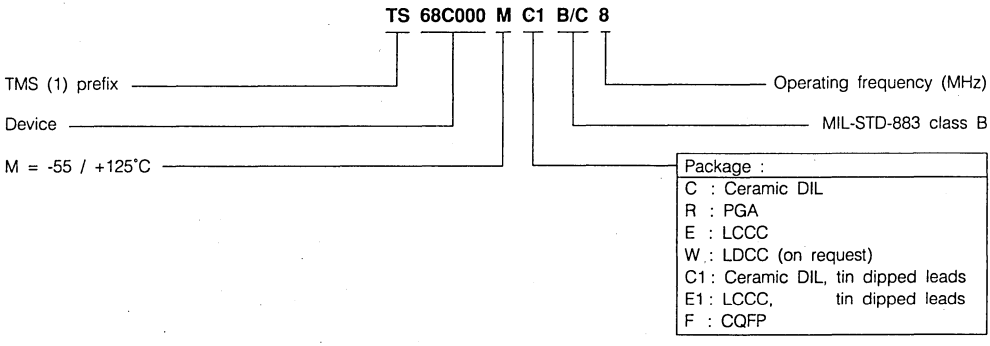


10 · ORDERING INFORMATION

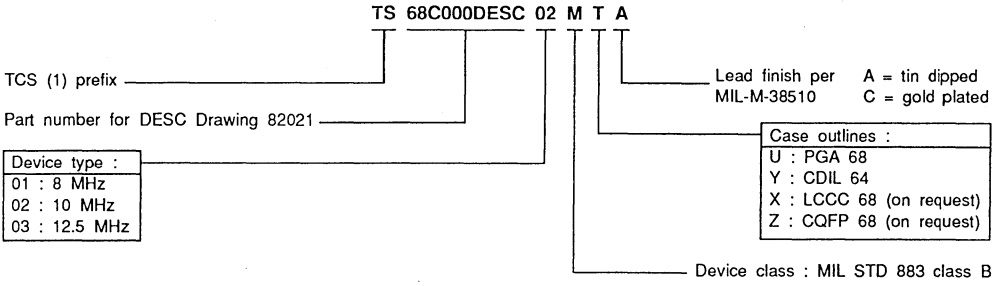
10.1 · CECC (CECC spec number is 90110-007)



10.2 · MIL-STD-883

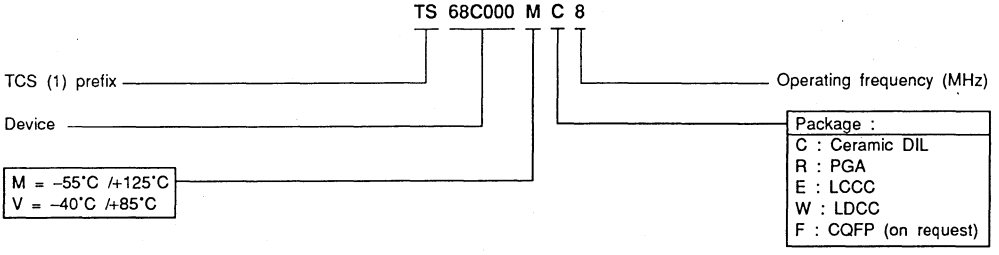


10.3 - DESC



Note : Temperature range is $-55°C \leqslant T_C \leqslant +125°C$ for DESC product.

10.4 - Standard product



Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

TS 68C901B

HCMOS MULTI FUNCTION PERIPHERAL

DESCRIPTION

The TS 68C901B multi-function peripheral (CMFP) is a member of the TS 68000 Family of peripheral and the CMOS version of the TS 68901. The CMFP directly interfaces to the TS 68000 processor family via an asynchronous bus structure and can also support both multiplexed and non multiplexed buses. Both vectored, non vectored and polled interrupt schemes are supported, with the CMFP providing unique vector number generation for each of its 16 interrupt sources. Additionally, handshake line are provided to facilitate DMAC interfacing.

The TS 68C901B performs many of the functions common to most microprocessor-based systems.

By incorporating multiple functions within the CMFP, the system designer retains flexibility while minimizing device' count.

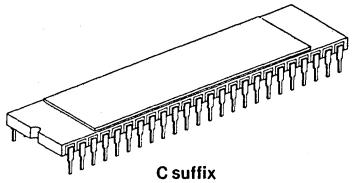
MAIN FEATURES

- 8 input/output pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmable edge selection.
- 16 source interrupt controller
  - 8 internal sources
  - 8 external sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
      - Optimal in-service status
  - Daisy chaining capability.
- Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
  - Independent clock input
  - Time out output option.
- Single channel USART
  - Full duplex
  - Asynchronous to 65 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals
  - Modem control
  - Loop back mode.
- 68000 Bus compatible.
- CMOS technology
  low power dissipation P_D = 55 mW max.
- Available in 4, 5 and 8 MHz.
- See application note.

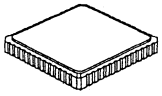
SCREENING / QUALITY

This product is manufactured in full compliance with :

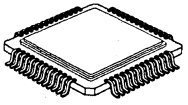
- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 (class B).
- DESC Drawing : 5962-90864.
- TCS STANDARDS.



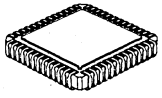
C suffix
DIL 48
Ceramic Side Brazed package



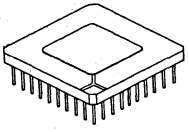
E suffix
LCCC 52
Leadless Ceramic Chip Carrier



F suffix
CQFP 52
Ceramic Quad Flat Pack



W suffix
LDCC 52
Leaded Ceramic Chip Carrier
(on request only)



F suffix
PGA 68
Ceramic Pin Grid Array

PIN CONNECTIONS (see A2)

Ordering information (see chapter 10).

5

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The TS 68C901B CMFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are :

- Eight parallel I/O lines,
- Interrupt controller for 16 sources,
- Four timers,
- Single channel full duplex USART.

The use of the CMFP in a system can significantly reduce chip count, thereby reducing system cost. The CMFP is completely 68000 bus compatible, and 24 directly addressable internal registers provide the necessary control and status interface to the programmer.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

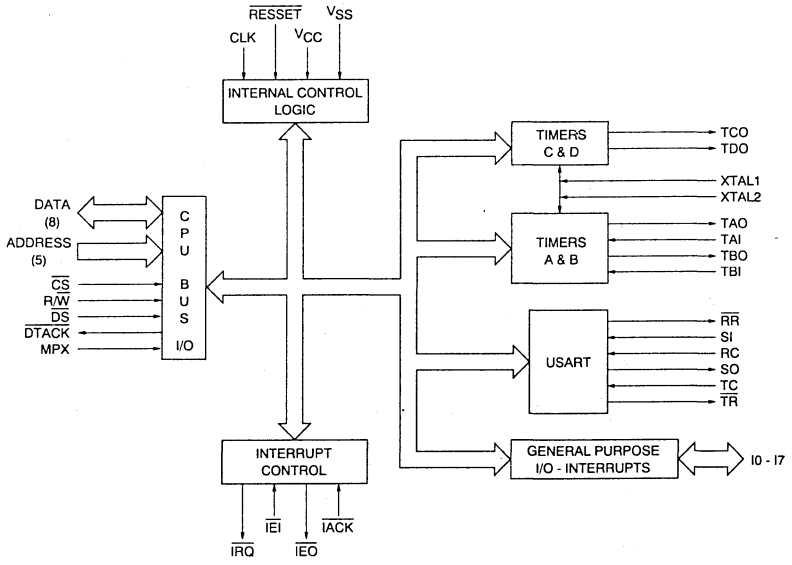


Figure 1 : Functional block diagram.

2 - PIN ASSIGNMENTS

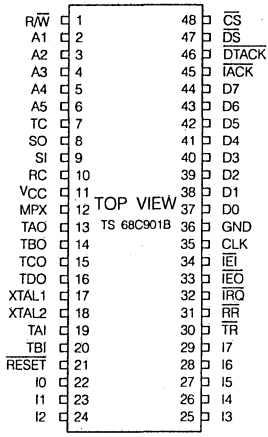


Figure 2.1 : Pin DIL package.

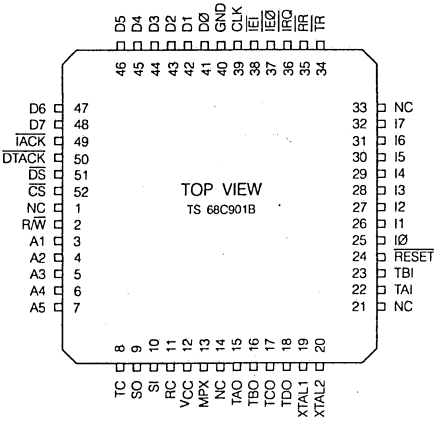


Figure 2.2 : Terminal Chip Carrier package.
(codes : E and W).

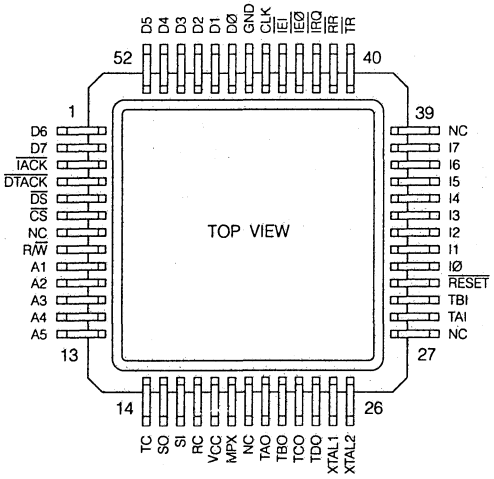


Figure 2.3 : CQFP terminal designation.

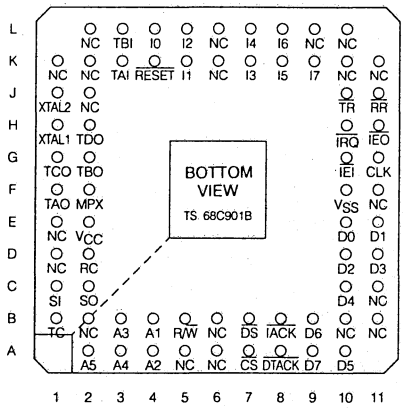


Figure 2.4 : PGA terminal Pin Grid Array.

3 - TERMINAL DESIGNATIONS

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply	Supply Terminals
V_{SS}*	Power supply	
$\overline{CS}$	Chip select	Input
$\overline{DS}$	Data strobe	Input
R/$\overline{W}$	Read/Write	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
A1 to A15	Address bus	Inputs
D0 to D7	Data bus	Bi-directionnal
CLK	Clock	Input
$\overline{RESET}$	Device Reset	Input
$\overline{IRQ}$	Interrupt Request	Output
$\overline{IACK}$	Interrupt Acknowledge	Input
$\overline{IEI}$	Interrupt Enable In	Input
$\overline{IEO}$	Interrupt Enable Out	Output
I0-I7	General purpose interrupt I/O lines	Bi-directionnal
SO	Serial Output	Output
SI	Serial Input	Input
TC	Transmitter Clock	Input
MPX	Multiplex Mode Select	Input
XTAL 1, 2	Timer clock	Input
TAI, TBI	Timer input	Input
TAO, TBO, TCO, TDO	Timer output	Output
RC	Receiver clock	Input
$\overline{RR}$	Receiver ready	Output
$\overline{TR}$	Transmitter ready	Output

* V_{SS} is the reference terminal for the voltage.

4 - SIGNAL DESCRIPTION

The input and output signals can be functionnaly organized into the groups shown in Figure 3.

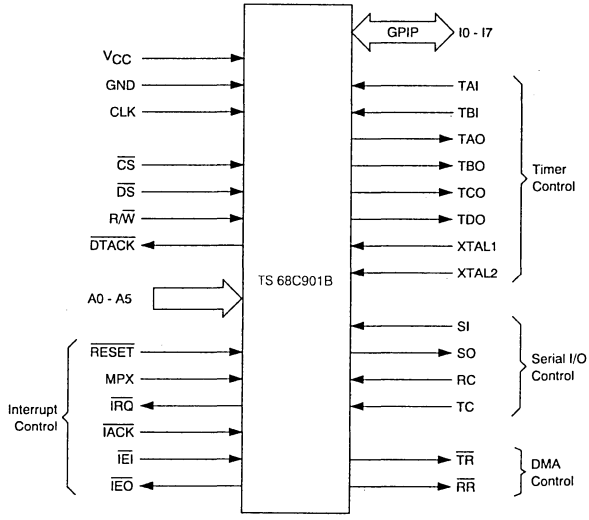


Figure 3 : Input and output signals.

4.1 - Pin description

GND : Ground.

V_{CC} : +5 Volts (± 10 %).

$\overline{CS}$: Chip Select (input, active low). $\overline{CS}$ is used to select the TS 68C901B for accesses to the internal registers. $\overline{CS}$ and IACK must not be asserted at the same time.

$\overline{DS}$: Data Strobe (input, active low). $\overline{DS}$ is used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle.

$\overline{DTACK}$: Data Transfert Acknowledge (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that the data is ready, or that data has been accepted by the TS 68C901B.

A1-A5 : Address Bus (inputs). The address bus is used to address one of the internal registers during a read or write cycle.

D0-D7 : Data Bus (bi-directionnal, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.

CLK : Clock (input). This input is used to provide the internal timing for the TS 68C901B.

$\overline{RESET}$: Device reset (input, active low). Reset disables the USART receiver and transmitter, stops all timers and forces the timer outputs low, disables all interrupt channels and clears any pending interrupts. The General Purpose Interrupt I/O lines will be placed in the tri-stated input mode. All internal registers (except the timer, USART data registers, and transmit status register) will be cleared.

$\overline{IRQ}$: Interrupt Request (output, active low, open drain). $\overline{IRQ}$ is asserted when the TS 68C901B is requesting an interrupt. $\overline{IRQ}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.

$\overline{IACK}$: Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the TS 68C901B that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

$\overline{IEI}$: Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the TS 68C901B that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the TS 68C901B nor another higher priority peripheral is requesting interrupt service.

I0-I7 : General Purpose Interrupt I/O lines. These lines may be used as interrupt inputs and/or I/O lines. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

SO : Serial Output. This is the output of the USART transmitter. This output is configured by the TSR register.

SI : Serial Input. This is the input to the USART receiver.

RC : Receiver Clock. This input controls the serial bit rate of the USART receiver.

TC : Transmitter Clock. This input controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready (output, active low). DMA output for receiver, which reflects the same status of Buffer Full in port number 15.

$\overline{TR}$: Transmitter Ready (output, active low). DMA output for transmitter, which reflects the status of Buffer Full in port number 16.

TAO, TBO
TCO, TDO : Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle ; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO can be reset (logic «0») by a write to TACR or TBCR respectively.

XTAL 1
XTAL 2 : Timer Clock Inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with EXTERNAL clock. When driving XTAL1 with EXTERNAL clock. XTAL2 must be allowed to float. When using a crystal, external capacitors are required. See Figure 19. All chip accesses are independent of the timer clock.

TAI, TBI : Timer A, B Inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with 14 and 13 are used for TAI and TBI respectively. Thus, when running a timer in the pulse width measurement mode, 14 or 13 can be used for I/O only.

MPX : This signal select the data bus mode :
MPX = 0 : non multiplex mode
MPX = 1 : multiplex mode. The register select lines RS1-RS5 and the data bus D0-D7 are multiplexed.
An address strobe must be connected to the CLK pin.

5

4.2 - Signal Summary

Table 2 is a summary of all the signals discussed in the previous paragraph.

Table 2 - Signal summary

Symbol	Signal name	I/O	Active
V_{CC}	Power input	Input	High
GND	Ground	Input	Low
CLK	Clock	Input	N/A
$\overline{CS}$	Chip Select	Input	Low
$\overline{DS}$	Data Strobe	Input	Low
R/$\overline{W}$	Read/Write	Input	Read - High, Write - Low
$\overline{DTACK}$	Data Transfer Acknowledge	Output	Low
A1-A5	Register Select Bus	Input	N/A
D0-D7	Data Bus	I/O	N/A
$\overline{RESET}$	Reset	Input	Low
$\overline{IRQ}$	Interrupt Request	Output	Low
$\overline{IACK}$	Interrupt Acknowledge	Input	Low
$\overline{IEI}$	Interrupt Enable In	Input	Low
$\overline{IEO}$	Interrupt Enable Out	Output	Low
I0-I7	General Purpose I/O - Interrupt Lines	I/O	N/A
XTAL1, XTAL2	Timer Clock	Input	High
TAI, TBI	Timer Inputs	Input	N/A
TAO, TBO, TCO, TDO	Timer Outputs	Output	N/A
SI	Serial Input	Input	N/A
SO	Serial Output	Output	N/A
RC	Receiver Clock	Input	N/A
TC	Transmitter Clock	Input	N/A
$\overline{RR}$	Receiver Ready	Output	Low
$\overline{TR}$	Transmitter Ready	Output	Low
MPX	MPX	Input	N/A

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the multi function peripheral TS 68C901B-4, 5 and 8 MHz, in compliance either with MIL-STD-883 class B or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits
3) DESC 5962-90864

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1 and 2.2 (§ A).

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38535 except finish C (as described in § 3.5.6.1 of 38535).

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 48 LEAD DIP Style D14
- SQ LCC 52 PINS Style C6
- 52 TERMINAL JCC
- CQFP 52
- PGA 68.

The precise case outlines are described at the end of the specification (chapter 9) and into MIL-M-38510.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 3 · Absolute maximum ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	7.0	V
V_I	Input voltage		−0.3	7.0	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		NA	NA	V
I_O	Output currents		NA	NA	mA
I_I	Input currents		NA	NA	mA
P_d	Power dissipation	T_{case} = −55°C		55	mW
		T_{case} = +125°C		55	mW
T_c	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{lead}	Lead temperature	Max. 5 sec soldering		+270	°C

3.3.2 · Guaranteed characteristics · recommended conditions of use

3.3.2.1 · Guaranteed characteristics

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified in § 3.3.2.2. below.

3.3.2.2 - Recommended conditions of use

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also § 3.3.2.1. above).

These conditions shall not be for inspection purposes.

Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

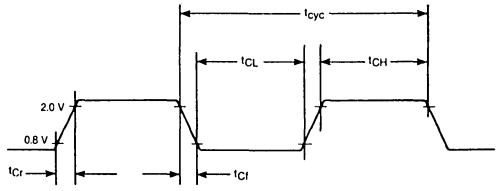


Figure 4 : Clock input timing diagram.

Table 4 - Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal (see § A.3).

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_{IL}	Low level input voltage (except XTAL1, XTAL2 and CLK : $V_{IL\ max}$ = 0.5 V)		− 0.3	0.8	V
V_{IH}	High level input voltage		2.0	V_{CC}	V
T_{case}	Operating temperature		− 55	+ 125	°C
R_L	Value of output load resistance		Note		Ω
C_L	Output loading capacitance			Note	pF
t_{cr}	Clock rise time (see Figure 4)			10	ns
t_{cf}	Clock fall time (see Figure 4)			10	ns
f_c	Clock frequency (see Figure 4)	TS 68C901B-4	1	4	MHz
		TS 68C901B-5	1	5	MHz
		TS 68C901B-8	1	8	MHz
t_{cyc}	Cycle time (see Figure 4)	TS 68C901B-4	250	1000	ns
		TS 68C901B-5	200	1000	ns
		TS 68C901B-8	125	1000	ns
t_w (cL)	Clock pulse width low (see Figure 4)	TS 68C901B-4	110		ns
		TS 68C901B-5	90		ns
		TS 68C901B-8	55		ns
t_w (cH)	Clock pulse width high (see Figure 4)	TS 68C901B-4	110		ns
		TS 68C901B-5	90		ns
		TS 68C901B-8	55		ns
V_{IL}	Low level input voltage for clock		− 0.3	0.5	V

Note : Load network number 1 and 2 as specified in (Figures 5 and 6) gives the maximum loading of the relevant output.

3.3.3 - Special recommanded conditions for C.MOS devices

a) CMOS latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become «latched» in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients ; others may require no additional circuitery.

b) CMOS applications

– The TS 68C901B completely satisfies the input/output drive requirements of CMOS logic devices.

– The HCMOS TS 68C901B, provides an order of magnitude power dissipation reduction when compared to the HMOS TS 68901. However the TS 68C901B does not offer a «power down» or «halt» mode. The minimum operating frequency of the TS 68C901B is 1 MHz.

3.4 - Thermal characteristics

Table 5

Package	Symbol	Parameter	Value	Unit
DIL 48	θ_{J-A}	Thermal resistance Junction-to-Ambient	30	°C/W
	θ_{J-C}	Thermal resistance Junction-to-Case	10	°C/W
LCCC 52	θ_{J-A}	Thermal resistance Junction-to-Ambient	40	°C/W
	θ_{J-C}	Thermal resistance Junction-to-Case	10	°C/W
LDCC 52	θ_{J-A}	Thermal resistance Junction-to-Ambient	40	°C/W
	θ_{J-C}	Thermal resistance Junction-to-Case	10	°C/W
CQFP 52	θ_{J-A}	Thermal resistance Junction-to-Ambient	40	°C/W
	θ_{J-C}	Thermal resistance Junction-to-Case	10	°C/W
PGA 68	θ_{J-A}	Thermal resistance Junction-to-Ambient	5	°C/W
	θ_{J-C}	Thermal resistance Junction-to-Case	33	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 6 : Static electrical characteristics for the electrical variants.
- Table 7 : Dynamic electrical characteristics for TS 68C901B-4 (4 MHz), TS 68C901B-5 (5 MHz) and TS 68C901B-8 (8 MHz).

For static characteristics (Table 6), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 7), test methods refer to clause 5.4 of this specification.

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.2.2 here above.

Table 6 - Static characteristics for all covered models

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Characteristic	Method (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
1	I_{CC}	Supply current outputs opens	41	$V_{CC} = 5.5\ V$	all		10	mA
2	V_{OL}	Low level output voltage (Except $\overline{DTACK}$)	37	$V_{CC} = 4.5\ V$ $I_{OL} = 2.0\ mA$	all		0.5	V
3	V_{OH}	High level output voltage (Except $\overline{DTACK}$)	37	$V_{CC} = 4.5\ V$ $I_{OH} = -120\ \mu A$	all	2.4		V
4	I_{OH}	$\overline{DTACK}$ output source current		$V_{OUT} = 2.4\ V$	all		−400	µA
5	I_{OL}	$\overline{DTACK}$ output sink current		$V_{OUT} = 0.5\ V$	all	5.3		mA
6	I_{IN}	Input leakage current (0 to 5.5 V)			all	−10	+10	µA
7	I_{LOH}	Three-state input current in float		$V_{OUT} = 2.4$ to V_{CC}	all		+10	µA
8	I_{LOL}	Three-state input current in float		$V_{OUT} = 0.5$	all		−10	µA
9	V_{IH1}	High level input voltage for all inputs (except : XTAL1, XTAL2, CLK)			all	2.0	V_{CC} +0.3	V
9A	V_{IH2}	High level input voltage for XTAL1, XTAL2, CLK			all	V_{CC} −1.5	V_{CC} +0.3	V
10	V_{IL1}	Low level input voltage for all inputs (except : XTAL1, XTAL2, CLK)			all	−0.3	0.8	V
10A	V_{IL2}	Low level input voltage for CLK, XTAL1, XTAL2			all	−0.3	0.5	V
97	C_{IN}	Input capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C		10	pF
					min		NA	pF
					max		NA	pF
98	C_{OUT}	Output capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C		10	pF
					min		NA	pF
					max		NA	pF
99	V_{ESD}	Internal protection Transient energy rating	See Note 7	See Note 7 5 cycles	25°C	−500	+500	V
					min	NA	NA	V
					max	NA	NA	V

* IEC measurement method number unless otherwise stated (see § 5.1).
Refered note is given after Table 7.

5

5.3 - Dynamic characteristics

Table 7 - Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (see Figures 5 and 6)
$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
11	t_W (T_{SWH})	$\overline{CS}$ $\overline{DS}$ width high (Note 5)	Fig. 8 - 9 Ref. 1	See 5.4 (a) to (c) f_C = 4 MHz	50		35		25		ns
12	t_{su} (T_{RASL})	R/$\overline{W}$, A1-A5 valid to falling $\overline{CS}$	Fig. 8 - 9 Ref. 2	See test 11	30		25		20		ns
13	t_{su} (T_{DVCL})	Data valid prior to $\overline{DS}$ high	Fig. 9 Ref. 3	See test 11	250		200		120		ns
14	t_{su} (T_{SVCL})	$\overline{CS}$, $\overline{IACK}$ valid prior to falling CLK (Note 3)	Fig. 8 - 10 - 11 Ref. 4	See test 11	50		50		50		ns
15	t_{phl} (T_{CLDL})	CLK low to $\overline{DTACK}$ low	Fig. 8 - 9 Ref. 5	See test 11 Load : 3		220		180		90	ns
16	t_{phl} (T_{SHDH})	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ high to $\overline{DTACK}$ high	Fig. 8 - 9 Ref. 6	See test 11 Load : 3		60		55		50	ns
18	t_h (T_{SLDIW})	$\overline{CS}$$\overline{DS}$ or $\overline{IACK}$ high to data invalid (WRITE)	Fig. 9 Ref. 8	See test 11	0		0		0		ns
18A	t_h (T_{SLDIR})	$\overline{CS}$$\overline{DS}$ or $\overline{IACK}$ high to data invalid (READ)	Fig. 8 Ref. 8A	See test 11	0		0		0		ns
20	t_h (T_{SHRAI})	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ high to R/$\overline{W}$ A1-A5 invalid	Fig. 8 - 10 - 11 Ref. 10	See test 11	0		0		0		ns
21	t_{phl} t_{plh} (T_{DVSL})	Data valid from $\overline{CS}$ low (Notes 3 and 5)	Fig. 8 - 9 Ref. 11	See test 11		310		260		180	ns
22	t_{su} (T_{RVDL})	Read data valid to $\overline{DTACK}$ low valid	Fig. 8 Ref. 12	See test 11 Load : 3	10		10		10		ns
23	t_h (T_{DLSH})	$\overline{DTACK}$ low to $\overline{DS}$, $\overline{CS}$ or $\overline{IACK}$ high	Fig. 8 - 10 Ref. 13	See test 11	10		10		10		ns
24	t_{su} (T_{ILCL})	$\overline{IEI}$ low to falling CLK	Fig. 10 - 11 Ref. 14	See test 11	50		50		50		ns
25	t_{phl} (T_{IVCL})	$\overline{IEO}$ valid from CLK low (Note 1)	Fig. 10 - 11 Ref. 15	See test 11		180		180		120	ns
26	t_{phl} t_{plh} (T_{DAVCL})	Data valid from CLK low	Fig. 10 Ref. 16	See test 11		300		300		180	ns
27	t_{plh} (T_{IIIH})	$\overline{IEO}$ invalid from $\overline{IACK}$ high	Fig. 10 - 11 Ref. 17	See test 11		150		150		100	ns
28	t_{plh} (T_{DLCH})	$\overline{DTACK}$ low from CLK high	Fig. 10 - 11 Ref. 18	See test 11		180		165		100	ns
29	t_{phl} (T_{IVIL})	$\overline{IEO}$ valid from $\overline{IEI}$ low (Note 1)	Fig. 11 Ref. 19	See test 11		100		100		100	ns
30	t_{phl} t_{plh} (T_{DAVIL})	Data valid from $\overline{IEI}$ low	Fig. 10 Ref. 20	See test 11		220		220		140	ns
31	t_{cy} (T_{CT})	CLK cycle time	Fig. 8 Ref. 21	See test 11	250		200		125		ns
32	t_w (T_{CL})	CLK width low	Fig. 8 Ref. 22	See test 11	110		90		55		ns
33	t_w (T_{CH})	CLK width high	Fig. 8 Ref. 23	See test 11	110		90		55		ns
34	t_{su} (T_{SICH})	$\overline{CS}$ $\overline{IACK}$ inactive to rising CLK (Note 4)	Fig. 8 - 11 Ref. 24	See test 11	100		80		50		ns
35	t_w (T_{IOAW})	I/O min active pulse width	Fig. 15 Ref. 25	See test 11	100		100		100		ns
36	t_w (T_{IWH})	$\overline{IACK}$ width high	Fig. 9 - 10 Ref. 26			2		2		2	TCLK
37	t_{phl} t_{plh} (T_{IDVSL})	I/O data valid from the first $\overline{CLK}$ ↓ following $\overline{CS}$ ↓ or $\overline{DS}$ ↓	Fig. 16 Ref. 27	See test 11		220		210		190	ns

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

Table 7 - Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (continued) (see Figures 5 and 6)
$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
38	t_{phl} (T_{RRCL})	Receiver ready delay from rising RC	Fig. 17 Ref. 28	See test 11		600		600		200	ns
39	t_{phl} (T_{TRCL})	Transmitter ready delay from rising RC	Fig. 18 Ref. 29	See test 11		600		600		200	ns
40	t_{phl} (T_{TLSH})	Timer output low from rising edge of CS/ DS/ (Note 7)	Fig. 19 Ref. 30	See test 11		450		450		200	ns
42	t_w (T_{TCL})	Timer CLK low time	Fig. 19 Ref. 32	See test 11	110		90		55		ns
43	t_w (T_{TCH})	Timer CLK high time	Fig. 19 Ref. 33	See test 11	110		90		55		ns
44	t_w (T_{TCC})	Timer CLK cycle time	Fig. 19 Ref. 34	See test 11	250	1000	200	1000	125	1000	ns
45	t_w (T_{RL})	RESET/ low time	Fig. 20 Ref. 35	See test 11	2.0		1.6		1.0		µs
46	t_{phl} (T_{DILI})	Delay to falling IRQ from external interrupt active transition	Fig. 15 Ref. 36	See test 11		380		380		250	ns
47	t_{phl} (T_{TTCL})	Transmitter interrupt delay falling TC	Fig. 18 Ref. 37	See test 11		550		550		300	ns
47a	t_{phl} (T_{TTCH})	Transmitter underrun error or end of break interrupt delay from rising edge of TC	Fig. 18 Ref. 37a	See test 11		550		550		300	ns
48	t_{phl} (T_{RICL})	Receiver buffer full inter trans delay FR rising RC	Fig. 17 Ref. 38	See test 11		800		800		400	ns
49	t_{plh} (T_{RIRCL})	Receive error interrupt trans delay FR falling edge of RC	Fig. 17 Ref. 39	See test 11		800		800		800	ns
50	t_{plh} (T_{SRCL})	Serial in set-up time of rising edge of RC (divide by one only	Fig. 17 Ref. 40	See test 11	80		70		50		ns
51	t_h (T_{DHRL})	Data hold time FR rising edge of RC (divide by one only)	Fig. 17 Ref. 41	See test 11	350		325		100		ns
52	t_{plh} t_{phl} (T_{DTCL})	Serial output data valid FR falling edge of TC/(1)	Fig. 18 Ref. 42	See test 11		440		420		200	ns
53	t_w (T_{TACL})	Transmitter CLK low time	Fig. 18 Ref. 43	See test 11	500		450		250		ns
54	t_w (T_{TACH})	Transmitter CLK high time	Fig. 18 Ref. 44	See test 11	500		450		250		ns
55	t_w (T_{TACC})	Transmitter CLK cycle time	Fig. 18 Ref. 45	See test 11	1000		900		500		ns
56	t_w (T_{RCL})	Receiver CLK low time	Fig. 17 Ref. 46	See test 11	500		450		250		ns
57	t_w (T_{RCH})	Receiver CLK high time	Fig. 17 Ref. 47	See test 11	500		450		250		ns
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 17 Ref. 48	See test 11	1000		900		500		ns
59	t_w (T_{SWL})	CS/IACK/DS/ width low (Note 2)	Fig. 19 Ref. 49	See test 11		80		80		80	TCLK
60	t_{plh} t_{phl} (T_{DATCL})	Serial output data valid from falling edge TC (+ 16)	Fig. 18 Ref. 50	See test 11		490		370		240	ns
61	t_{cy} (T_{CY})	Cycle time	Fig. 12 Ref. 51	See test 11	1000		1000		1000		ns
62	t_w (T_{WEH})	Pulse width, E high	Fig. 12 Ref. 52	See test 11	430		430		430		ns
63	t_w (T_{WEL})	Pulse width, E low	Fig. 12 Ref. 53	See test 11	450		450		450		ns

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

5

Table 7 · Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (continued) (see Figures 5 and 6)
$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
64	t_{su} (T_{AEH})	Address R/U/Setup time before E	Fig. 12 Ref. 54	See test 11	80		80		80		ns
65	t_{su} (T_{SEH})	$\overline{CS}$/Setup time before E	Fig. 12 Ref. 55	See test 11	80		80		80		ns
66	t_h (T_{HA})	Address hold time	Fig. 12 Ref. 56	See test 11	10		10		10		ns
67	t_h (T_{HS})	$\overline{CS}$/Hold time	Fig. 12 Ref. 57	See test 11	10		10		10		ns
68	t_{plh} (T_{EDV})	Output data delay (READ)	Fig. 12 Ref. 58	See test 11		250		250		250	ns
69	t_h (T_{HD})	Data hold time	Fig. 12 Ref. 59	See test 11	0	100	0	100	0	100	ns
70	t_{su} (T_{DEL})	Input data setup time (WRITE)	Fig. 12 Ref. 60	See test 11	280		280		280		ns
71	t_h (T_{HDW})	Data hold time (WRITE)	Fig. 12 Ref. 61	See test 11	20		20		20		ns
72	t_{cy} (T_{CY})	Cycle time	Fig. 13 - 14 Ref. 62	See test 11	800		800		800		ns
73	t_w (T_{SWH})	Pulse width $\overline{DS}$/ low or RD/WR/High	Fig. 13 - 14 Ref. 63	See test 11	350		350		350		ns
74	t_w (T_{SWL})	Pulse width $\overline{DS}$/ low or RD/WR/low	Fig. 13 - 14 Ref. 64	See test 11	340		340		340		ns
75	t_w (T_{ALEH})	Pulse width AS/ALE high	Fig. 13 - 14 Ref. 65	See test 11	100		100		100		ns
76	t_{phl} (T_{SLSL})	Delay as fall to $\overline{DS}$/ rise or Ale fall to RD/WR/Fall	Fig. 13 - 14 Ref. 66	See test 11	30		30		30		ns
77	t_{plh} (T_{SHSH})	Delay $\overline{DS}$/ or RD/WR/ rise to AS/ALE	Fig. 13 - 14 Ref. 67	See test 11	30		30		30		ns
78	t_{su} (T_{RLSH})	R/$\overline{W}$/Setup time $\overline{DS}$/	Fig. 13 - 14 Ref. 68	See test 11	100		100		100		ns
79	t_h (T_{RHSL})	R/$\overline{W}$/Hold time to $\overline{DS}$/	Fig. 13 - 14 Ref. 69	See test 11	10		10		10		ns
80	t_{su} (T_{ASL})	Address setup time to AS/ALE	Fig. 13 - 14 Ref. 70	See test 11	20		20		20		ns
81	t_h (T_{SLAV})	Address setup to AS/ALE	Fig. 13 - 14 Ref. 71	See test 11	20		20		20		ns
82	t_{su} (T_{DVSL})	Data setup time to $\overline{DS}$/ or or WR (WRITE)	Fig. 13 - 14 Ref. 72	See test 11	280		280		280		ns
83	t_{plh} (T_{SHDV})	Delay data to $\overline{DS}$/ or RD (Read)	Fig. 13 - 14 Ref. 73	See test 11		250		250		250	ns
84	t_h (T_{SLDV})	Data hold time to $\overline{DS}$ or WR (Write)	Fig. 13 - 14 Ref. 74	See test 11	20		20		20		ns
85	t_h (T_{SLDZ})	Data hold time to $\overline{DS}$ or RD (Read)	Fig. 13 - 14 Ref. 75	See test 11	0	100	0	100	0	100	ns
86	t_{su} (T_{RSH})	CE setup time to as/Ale Falll	Fig. 13 - 14 Ref. 76	See test 11	20		20		20		ns
87	t_h (T_{SLCEH})	CE hold time to $\overline{DS}$ RD or WR	Fig. 13 - 14 Ref. 77	See test 11	20		20		20		ns

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

REFERED NOTES TO THE TABLES

The following notes shall apply where referred into the tables and/or additional information given in of this specification.

Note 1 : IEO only goes low if no acknwoledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain tri-stated.

Note 2 : T_{CLK} refers to the clock applied to the MFP CLK input pin. t_{CLK} refers to the timer clock signal, regard less of whether this signal comes from the XTAL1/XTAL2 crystal clock inputs or the TAI or TBI timer inputs.

Note 3 : If the set-up time is not met, $\overline{CS}$ or $\overline{IACK}$ will not be recognized until the next falling CLK.

Note 4 : If the set-up time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

Note 5 : Although $\overline{CS}$ and $\overline{DTACK}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, relying only on CS for timing.

Note 6 : Spec. 30 applies to timer outputs TAO and TBO only.

Note 7 : The test shall be performed as specified in Generic Specification and its associated documents. The test voltages are as given in Table 6 for test 99.
Each terminal of the device under test shall be tested separately against all existing V_{CC} and V_{SS} terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in Table 6 for test 99.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Table 7, refering to the loading network number as shown in Figures 5 and 6 below.

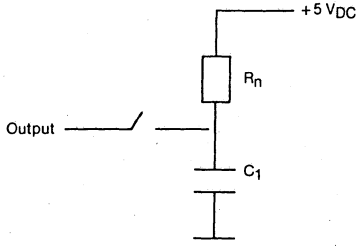


Figure 5 : Passive loads.

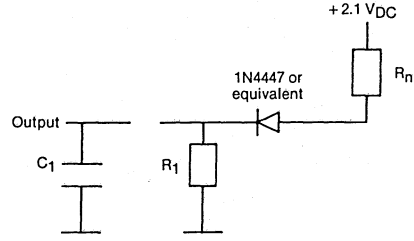
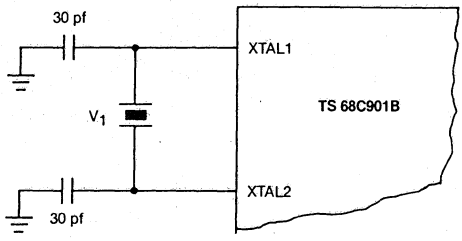


Figure 6 : Active loads.

Load NBR	Figure	R_1	R_n	C_1	Output application
1	5	—	2.25 k	100 pF	$\overline{IRQ}$
2	6	20 k	150	100 pF	All outputs except $\overline{DTACK}$
3	6	6 k	470	130 pF	$\overline{DTACK}$
Note : Equivalent loading may be simulated by the tester.					

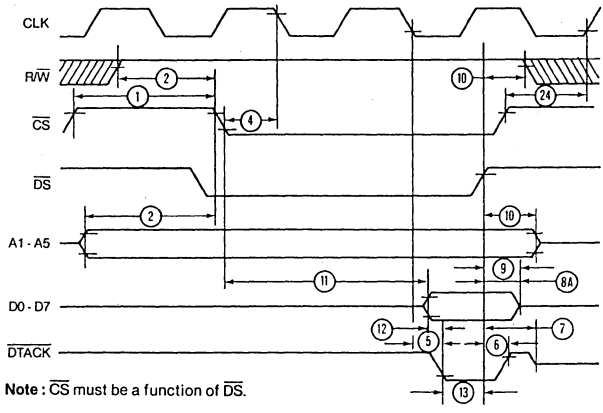


Crystal Parameters :
Parallel resonance, fundamental mode AT cut
R_L = < 150 Ω (Fr = 2.8 – 8.0 MHz) ;
R_L = < 300 Ω (Fr = 2.0 – 2.7 MHz) ;
C_L = 18 pF ; C_M = 0.02 pF ; C_h = 5 pF ; L_M = 96 mH
F_R (type) = 2.4676 MHz

Figure 7 : TS 68C901B MFP external oscillator components.

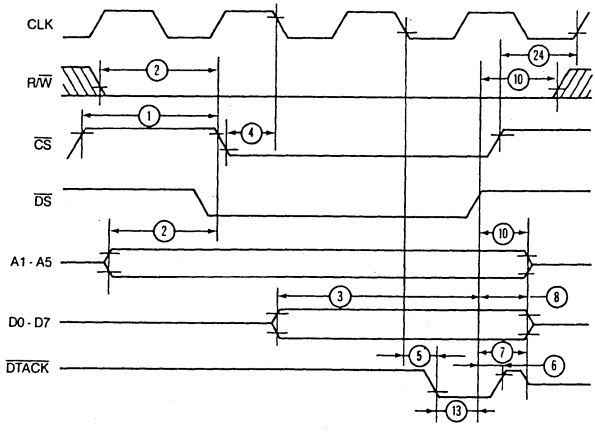
5.4.2 - Time definitions

The times specified in Table 7, as dynamic characteristics are defined in Figures 8 to 20 below by a reference number given in the column «Method» of the tables together with the relevant figure number.



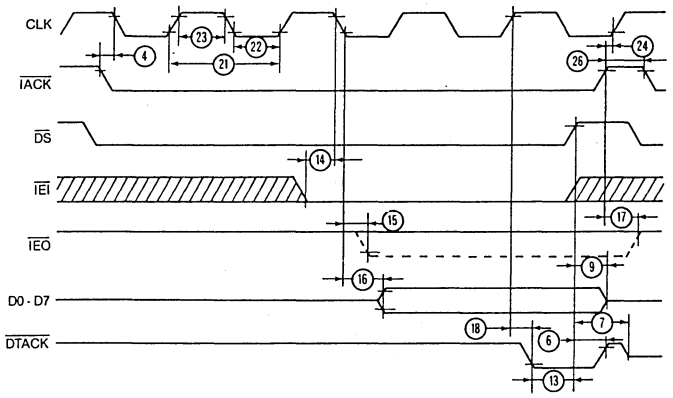
Note : $\overline{CS}$ must be a function of $\overline{DS}$.

Figure 8 : Read cycle timing.



Note : $\overline{CS}$ must be a function of $\overline{DS}$.

Figure 9 : Write cycle timing.

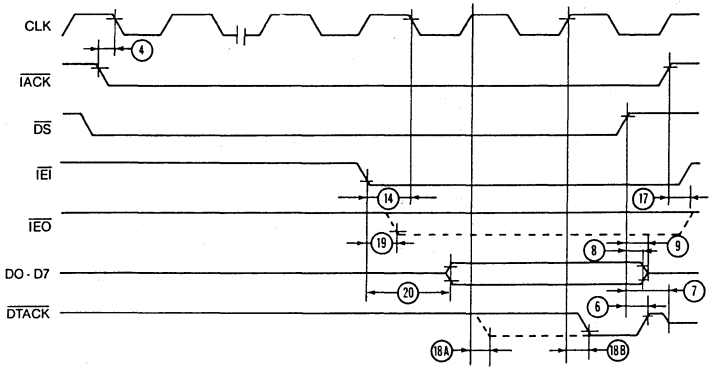


Note 1 : $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If IEO goes low, DTACK and the data bus remain in the high impedance state.

Note 2 : $\overline{IACK}$ must be a function of DS.

Figure 10 : Interrupt acknowledge cycle (IEI low).

5



Note 1 : $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain in the high impedance state.

Note 2 : $\overline{DTACK}$ will go low at A if specification number 14 is met. Otherwise $\overline{DTACK}$ will go low at 8.

Note 3 : $\overline{IACK}$ must be a function of $\overline{DS}$.

Figure 11 : Interrupt acknowledge cycle (IEI high).

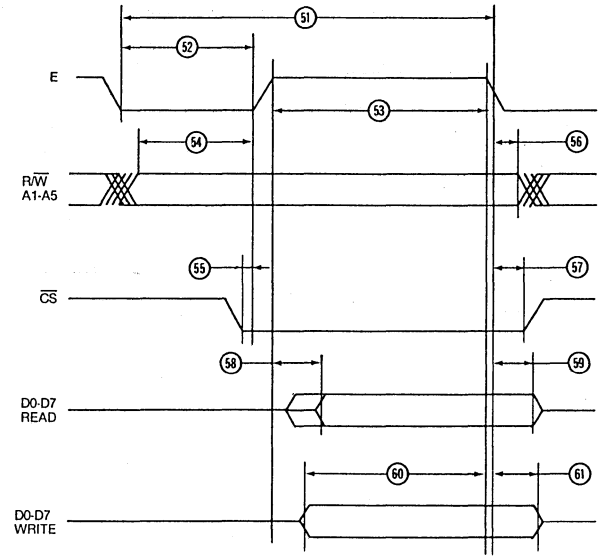


Figure 12 : 6800 interfacing timing.

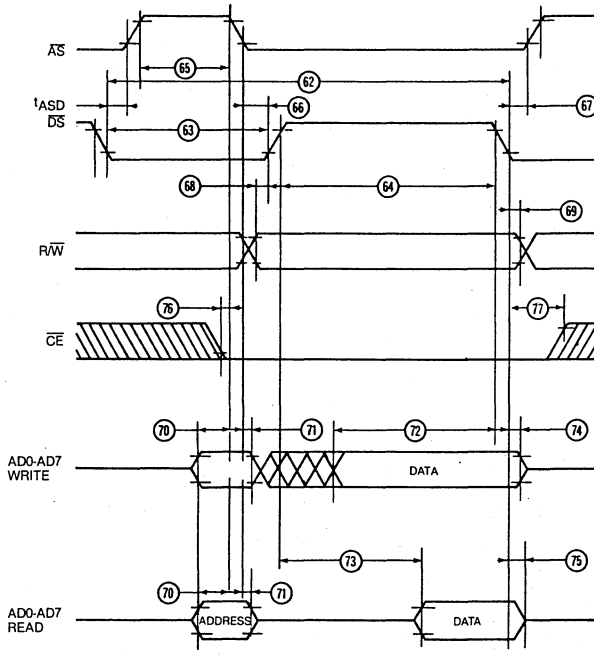


Figure 13 : Multiplexed bus timing Motorola type.

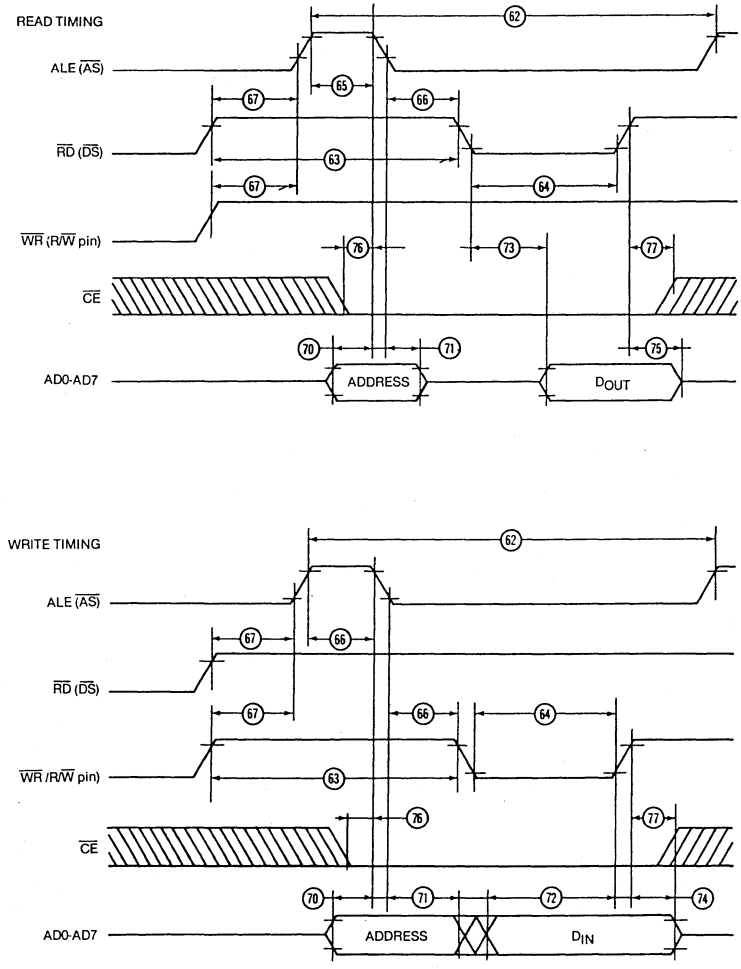
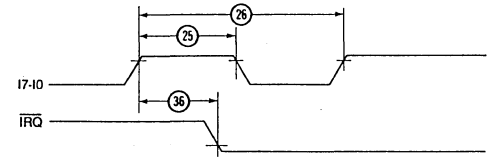


Figure 14 : Multiplexed bus timing - Intel type.



Note : Active edge is assumed to be the rising edge.

Figure 15 : Interrupt timing.

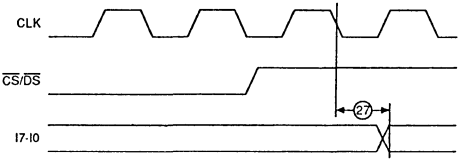


Figure 16 : Port timing.

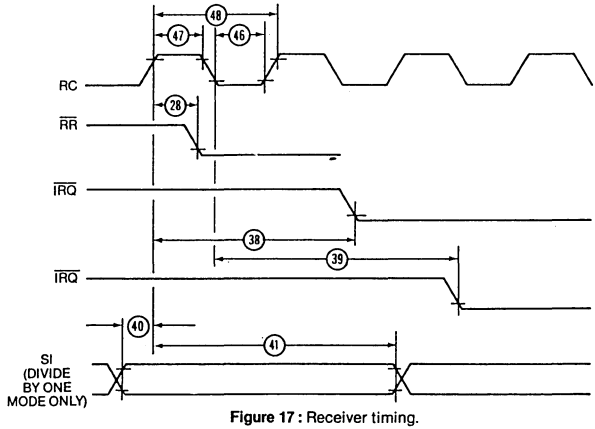


Figure 17 : Receiver timing.

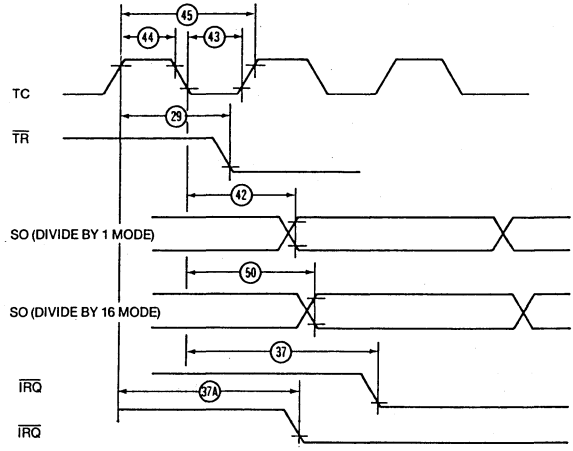


Figure 18 : Transmitter timing.

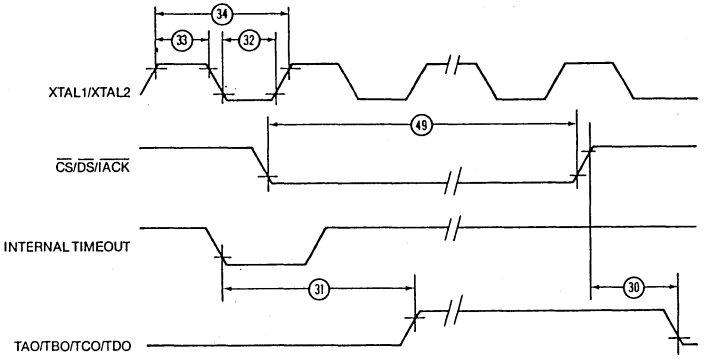


Figure 19 : Timer timing.

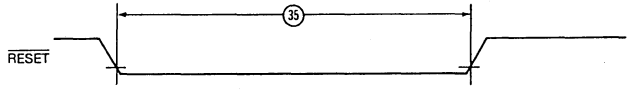


Figure 20 : Reset timing.

5.4.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics
Where input pulse generator is loaded by 90 ohms resistor, the input pulse characteristics shall be as shown in Figure 21.

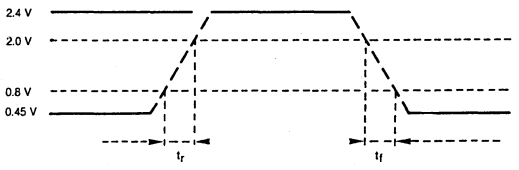


Figure 21 : Input pulse characteristics.

b) Time measurement input voltage references
Input voltages which are taken as reference for time measurement shall be :
V_{IL} = 0.8 V
V_{IH} = 2.0 V

c) Time measurement output voltage reference for time valid state output
Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in Figure 22.

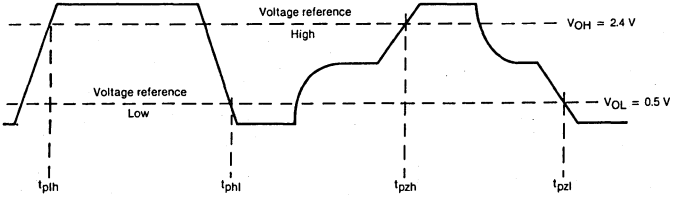


Figure 22 : Output voltage references for timing measurement.

5.4.4 · Timer AC characteristics

Definitions :

Error = Indicated time value - actual time value,
$t_{psc} = t_{CLK}$* Prescale value.

Internal Timer Mode :

Single Interval Error (Free Running) (See Note 2) ..... ± 100 ns
Cumulative Internal Error 0
Error Between Two Timer Reads ..... ± (t_{psc} − 4 t_{CLK})
Start Timer to Stop Timer Error ..... 2 t_{clk} + 100 ns to − (t_{psc} + 6 t_{CLK} + 100 ns)
Start Timer to Read Timer Error ..... 0 to − (t_{psc} + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (See Note 3) ..... 2 t_{CLK} to −(4 t_{CLK} + 800 ns)

Pulse Width Measurement Mode :

Measurement Accuracy (See Note 1) ..... 2 t_{CLK} to (t_{psc} + 4 t_{CLK})
Minimum Pulse Width ..... 4 t_{CLK}

Event Counter Mode :

Minimun Active Time of TAI and TBI ..... 4 t_{CLK}

Note 1 : Error may be cumulative if repetitively performed.
Note 2 : Error with respect to t_{out} or IRQ if Note 3 is true.
Note 3 : Assuming it is possible for the timer to make an interrupt request immediately.

5.5 · Additional information

Additional information shall not be for any inspection purposes.

5.5.1 · Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 8 to 20 and loading number refer to Figures 5 and 7 (see § 5.4 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2.2 of this specification.

Table 8 · Additional electrical characteristics TS 68C901B-4, 5 and 8 MHz (see Figures 5 and 6)
$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
17	t_{plz} (T_{SHDZ})	$\overline{CS}/\overline{DS}$/ or $\overline{IACK}$ high to $\overline{DTACK}$/ three state	Fig. 9 Ref. 7			100		100		100	ns
19	t_{phz} (T_{SHDAZ})	$\overline{CS}/\overline{DS}$/ or $\overline{IACK}$/ high to data three state	Fig. 8 - 10 - 11 Ref. 9			50		50		50	ns
31	t_{cy} (T_{CT})	CLK cycle time	Fig. 8 Ref. 21			1000		1000		1000	ns
41	t_{plh} (T_{VIT})	T_{out} valid from internal time-out (Note 2)	Fig. 19 Ref. 31			2TCLK + 300		2TCLK + 300		2TCLK + 300	ns
44	t_{cy}	Timer CLK cycle time	Fig. 19 Ref. 34	See test 11		1000		1000		1000	ns
55	t_{cy} (T_{TACC})	Transmitter CLK cycle time	Fig. 18 Ref. 45			DC		DC		DC	
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 17 Ref. 48			DC		DC		DC	

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

6 - FUNCTIONAL DESCRIPTION

6.1 - Bus operation

The following paragraphs explain the control signals and bus operation during data transfer operations and reset.

6.1.1 - Data transfer operations

Transfer of data between devices involves the following pins :

Register Select Bus – RS1 through RS5

Data Bus – D0 through D7

Control Signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. Additionally, the bus master is responsible for deskewing the acknowledge and data signals from the peripheral devices.

READ CYCLE. To read a CMFP register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The CMFP will place the contents of the register which is selected by the register select bus (RS1 through RS5) on the data bus (D0 through D7) and then assert $\overline{DTACK}$. The register addresses are shown in Figure 27.

After the processor has latched the data, $\overline{DS}$ is negated. The negation of either $\overline{CS}$ or $\overline{DS}$ will terminate the read operation. The CMFP will drive $\overline{DTACK}$ high and place it in the high-impedance state. Also, the data bus will be in the high-impedance state. The timing for a read cycle is shown in Figure 23. Refer to for actual numbers.

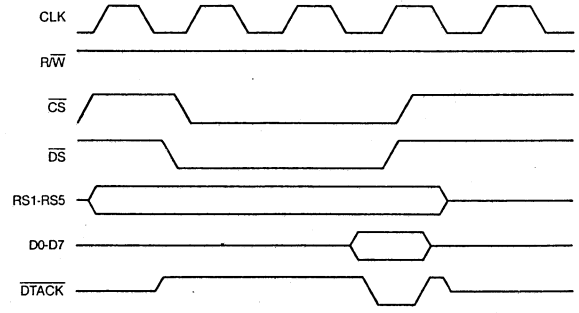


Figure 23 : Read cycle timing.

WRITE CYCLE. To write a register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be low. The CMPF will decode the address bus to determine which register is selected (the register map is shown in Figure 27). Then the register will be loaded with the contents of the data bus and $\overline{DTACK}$ will be asserted.

When the processor recognizes $\overline{DTACK}$, $\overline{DS}$ will be negated. The write cycle is terminated when either $\overline{CS}$ or $\overline{DS}$ is negated. The CMFP will drive $\overline{DTACK}$ high and place it in the high-impedance state. The timing for a write cycle is shown in Figure 24 Refer to for actual numbers.

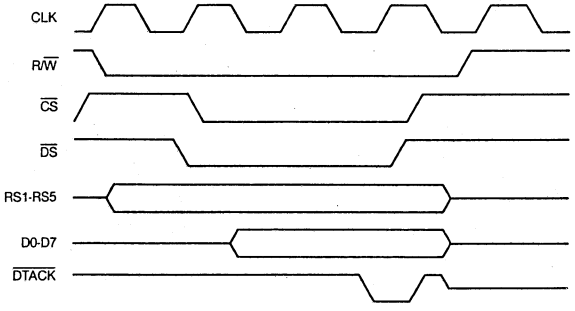


Figure 24 : Write cycle timing.

Interrupt acknowledge operation

The CMFP has 16 interrupt sources, eight internal sources, and eight external sources. When an interrupt request is pending, the CMFP will assert $\overline{IRQ}$. In a vectored interrupt sheme, the processor will acknowledge the interrupt request by performing an interrupt acknowledge cycle. $\overline{IACK}$ and $\overline{DS}$ will be asserted. The CMFP responds to the $\overline{IACK}$ signal by placing a vector number on the lower eight bits of the data bus. This vector number corresponds to the $\overline{IRQ}$ handler for the particular interrupt requesting service. The format of this vector number is given in Figure 28.

When the CMFP asserts $\overline{DTACK}$ to indicate that valid data is on the bus, the processor will latch the data and terminate the bus cycle by negating $\overline{DS}$. When either $\overline{DS}$ or $\overline{IACK}$ are negated, the CMFP will terminate the interrupt acknowledge operation by driving $\overline{DTACK}$ high and placing it in the high-impedance state. Also, the data bus will be placed in the high-impedance state. $\overline{IRQ}$ will be negated as a result of the $\overline{IACK}$ cycle unless additional interrupts are pending.

The CMFP can be part of a daisy-chain interrupt structure which allows multiple CMFPs to be placed at the same interrupt level by sharing a common $\overline{IACK}$ signal. A daisy-chain priority scheme is implemented with signals $\overline{IEI}$ and $\overline{IEO}$. IEI indicates that no higher priority device is requesting interrupt service. $\overline{IEO}$ signals lower priority devices that neither this device nor any higher priority device is requesting service.

To daisy-chain CMFPs, the highest priority CMFP has its IEI tied low and successive CMFPs have their $\overline{IEI}$ connected to the next higher priority device's $\overline{IEO}$. Note that when the daisy-chain interrupt structure is not implemented, the IEI of all CMFPs must be tied low. Refer to § 6.2.3 for additional information.

When the processor initiates an interrupt acknowledge cycle by driving $\overline{IACK}$ and $\overline{DS}$, the CMFP whose $\overline{IEI}$ is low may respond with a vector number if an interrupt is pending. If this device does not have a pending interrupt, $\overline{IEO}$ is asserted which allows the next lower priority device to respond to the interrupt acknowledge. When an CMFP propagates $\overline{IEO}$, it will not drive the data bus nor $\overline{DTACK}$ during the interrupt acknowledge cycle. The timing for an $\overline{IACK}$ cycle is shown in Figure 25. Refer to for further information.

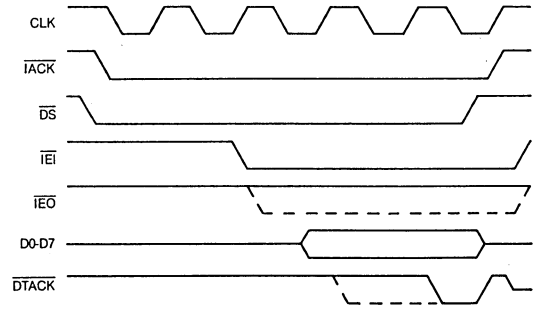


Figure 25 : IACK cycle timing.

Reset operation

The reset operation will initialize the CMFP to a known state. The reset operation requires that the $\overline{RESET}$ input be asserted for a minimum of two microseconds. During a device reset condition, all internal CMFP registers are cleared except fot the timer data registers (TADR, TBDR, TCDR, and TDDR), the USART data register (UDR), the transmitter status register (TSR) and the interrupt vector register. All timers are stopped and the USART receiver and transmitter are disabled. The interrupt channels are also disabled and any pending interrupts are cleared.

In addition, the general purpose interrupt I/O lines are placed in the high-impedance input mode and the timer outputs are driven low. External CMFP signals are negated. The interrupt vector register is initialized to a $0F.

Non multiplexed mode

In this mode the MPX input must be set to zero, and the TS 68C901B can be used with a 68000 processor type or a 6800 processor type. Refer to figure for the electrical characteristics.

With a 6800 processor type the $\overline{DS}$ pin is connected to the E signal of the processor, the $\overline{DTACK}$ signal is not used and the CLK must be zeroed.

Multiplexed mode

The CMFP can be used either on a MOTOROLA or INTEL bus type. In this case the MPX pin is connected to Vcc. The following table gives the signification of the different signals used. A dummy access to the TS 68C901B has to be done before any valid access in order to set up the internal logic of sampling.

LCCC pin out	DIL pin out	MOTOROLA 68000 type	MOTOROLA Multiplexed	INTEL
52	48	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
51	47	$\overline{DS}$	$\overline{DS}$	RD
2	1	R/$\overline{W}$	R/$\overline{W}$	WR
40	36	V_{SS}	AS	ALE

6.1.2 - DMA operation

USART error conditions are only valid for each character boundary. When the USART performs block data transfers by using the DMA handshake lines $\overline{RR}$ (Receiver Ready) and $\overline{TR}$ (Transmitter Ready), errors must be saved and-checked at the end of a block. This is accomplished by enabling the error channel for channel for the receiver or transmitter and by masking interrupts for this channel. Once the transfer is complete, interrupt pending register A is read. Any pending receiver or transmitter error indicates an error in the data transfer.

6.2 - Interrupt structure

In a 68000 system, the CMFP will be assigned to one fo the seven possible interrupt levels. All interrupt service requests from the CMFP's 16 interrupt channels will be presented at this level. Although, as an interrupt controller, the CMFP will internally prioritize its 16 interrupt sources. Additional interrupt sources may be placed at the same interrupt level by daisy-chaining multiple CMFPs. The CMFPs will be prioritized by their position in the chain.

6.2.1 - Interrupt processing

Each CMFP provides individual interrupt capability for its various functions. When an interrupt is received on one of the external interrupt channels or from one of the eight internal sources, the CMFP will request interrupt service. The 16 interrupt channels are assigned a fixed priority so that multiple pending interrupts are serviced according to their relative importance. Since the CMFP can internally generate 16 vector numbers, the unique vector number which corresponds to the highest priority channel that has a pending interrupt is presented to the processor during an interrupt acknowledge cycle. This unique vector number allows the processor to immediately begin execution of the interrupt handler for the interrupting source, decreasing interrupt latency time.

5

Address						Abbreviation	Register name
Hex	Binary						
	RS5	RS4	RS3	RS2	RS1		
01	0	0	0	0	0	GPIP	General purpose I/O register
03	0	0	0	0	1	AER	Active edge register
05	0	0	0	1	0	DDR	Data direction register
07	0	0	0	1	1	IERA	Interrupt enable register A
09	0	0	1	0	0	IERB	Interrupt enable register B
0B	0	0	1	0	1	IPRA	Interrupt pending register A
0D	0	0	1	1	0	IPRB	Interrupt pending register B
0F	0	0	1	1	1	ISRA	Interrupt in-service register A
11	0	1	0	0	0	ISRB	Interrupt in-service register B
13	0	1	0	0	1	IMRA	Interrupt mask register A
15	0	1	0	1	0	IMRB	Interrupt mask register B
17	0	1	0	1	1	VR	Vector register
19	0	1	1	0	0	TACR	Timer A control register
1B	0	1	1	0	1	TBCR	Timer B control register
1D	0	1	1	1	0	TCDCR	Timers C and D control register
1F	0	1	1	1	1	TADR	Timer A data register
21	1	0	0	0	0	TBDR	Timer B data register
23	1	0	0	0	1	TCDR	Timer C data register
25	1	0	0	1	0	TDDR	Timer D data register
27	1	0	0	1	1	SCR	Synchronous character register
29	1	0	1	0	0	UCR	USART control register
2B	1	0	1	0	1	RSR	Receiver status register
2D	1	0	1	1	0	TSR	Transmitter status register
2F	1	0	1	1	1	UDR	USART data register

Note : Hex addresses assume that RS1 connects with A1. RS2 connects with A2, etc... and that DS is connected to LDS on the 68000 or DS is connected to DS on the 68008.

Figure 26 : Register MAP.

6.2.1.1 - Interrupt channel prioritization

The 16 interrupt channels are prioritized as shown in Figure 27 general purpose interrupt 7 (17) is the highest priority interrupt channel and 10 is the lowest priority channel. Pending interrupts are presented to the CPU in order of priority unless they have been masked off. By selectively masking interrupts, the channels are in effect re-prioritized.

Priority	Channel	Description
Highest	1111	General purpose interrupt 7 (I7)
	1110	General purpose interrupt 6 (I6)
	1101	Timer A
	1100	Receiver buffer full
	1011	Receive error
	1010	Transmit buffer empty
	1001	Transmit error
	1000	Timer B
	0111	General purpose interrupt 5 (I5)
	0110	General purpose interrupt 4 (I4)
	0101	Timer C
	0100	Timer D
	0011	General purpose interrupt 3 (I3)
	0010	General purpose interrupt 2 (I2)
	0001	General purpose interrupt 1 (I1)
Lowest	0000	General purpose interrupt 0 (I0)

Figure 27 : Interrupt prioritization.

6.2.1.2 - Interrupt vector number format

During an interrupt acknowledge cycle, a unique 8-bit vector number is presented to the system which corresponds to the specific interrupt source which is requesting service. The format of the vector is shown in Figure 28. The most significant four bits of the interrupt vector number are user programmable. These bits are set by writing the upper four bits of the vector register which is shown in Figure 29. The low order bits are generated internally by the TS 68C901B. Note that the binary channel number shown in Figure 27 corresponds to the low order bits of the vector number associated with each channel.

7	6	5	4	3	2	1	0
V7	V6	V5	V4	IV3	IV2	IV1	IV0

V7-V4 : The four most significant bits are copied from the vector register.

IV3-IV0 : These bits are supplied by the CMFP. They are the binary channel number of the highest priority channel that is requesting interrupt service.

Figure 28 : Interrupt vector format.

	7	6	5	4	3	2	1	0
Address 17 (Hex)	V7	V6	V5	V4	S	★	★	★

★ Unused are read as zero.

V7-V4 : The upper four bits of the vector register are written by the user. These bits become the most significant four bits of the interrupt vector number.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset (VR must be written at least once by MPU, if not, low order bits remain 1111).

S : In-Service Register Enable. When the S bit is zero, the CMFP is in the automatic end-of-interrupt mode and the in-service register bits are forced low. When the S bit is a one, the CMFP is in the software end-of-interrupt mode and the in-service register bits are enabled. Refer to § 6.2.4.2 and § 6.2.4.3 for additionnal information.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 29 : Vector register format (VR).

6.2.2 - Daisy-chaining CMFPs

As an interrupt controller, the TS 68C901B CMFP will support eight external interrupt sources in addition to its eight internal interrupt sources. When a system requires more than eight external interrupt sources to be placed at the same interrupt level, sources may be added to the prioritized structure by daisy-chaining CMFPs. Interrupt sources are prioritized internally within each CMFP and the CMFPs are prioritized by their position in the chain. Unique vector numbers are provided for each interrupt source.

The $\overline{IEI}$ and $\overline{IEO}$ signals implement the daisy-chained interrupt structure. The $\overline{IEI}$ of the highest priority CMFP is tied low and the $\overline{IEO}$ output of this device is tied to the next highest priority CMFP's $\overline{IEI}$. The $\overline{IEI}$ and $\overline{IEO}$ signals are daisy-chained in this manner for all CMFPs in the chain, with the lowest priority CMFP's $\overline{IEO}$ left unconnected. A diagram of an interrupt daisy-chain is shown in Figure 30.

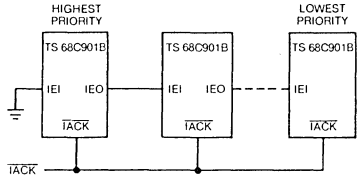


Figure 30 : Daisy-chained interrupt structure.

Daisy-chaining requires that all parts in the chain have a common $\overline{IACK}$. When the common $\overline{IACK}$ is asserted during an interrupt acknowledge cycle, all parts will prioritize interrupts in parallel. When the $\overline{IEI}$ signal to a CMFP is asserted, the part may respond to the $\overline{IACK}$ cycle if it requires interrupt service. Otherwise, the part will assert $\overline{IEO}$ to the next lower priority device. Thus, priority is passed down the chain via $\overline{IEI}$ and $\overline{IEO}$ until a part which has a pending interrupt is reached. The part with the pending interrupt passes a vector number to the processor and does not propagate $\overline{IEO}$.

6.2.3 - Interrupt control registers

CMFP interrupt processing is managed by the interrupt enable registers A and B, interrupt pending registers A and B, and interrupt mask registers A and B. These registers allow the programmer to enable or disable individual interrupt channels, mask individual interrupt channels, and access pending interrupt status information. In-service registers A and B allow interrupts to be nested as described in. The interrupt control registers are shown in figure.

6.2.3.1 - Interrupt enable registers

The interrupt channels are individually enabled or disabled by writing a one or zero, respectively, to the appropriate bit of interrupt enable register A (IERA) or interrupt enable register B (IERB). The processor may read theses registers at any time.

When a channel is enabled, interrupts received on the channel will be recognized by the CMFP and $\overline{IRQ}$ will be asserted to the processor, indicating that interrupt service is required. On the other hand, a disabled channel is completely inactive ; interrupts received on the channel are ignored by the CMFP.

Writing a zero to a bit of interrupt enable register A or B will cause the corresponding bit of interrupt pending register A or B to cleared. This will terminate all interrupt service request for the channel and also negate $\overline{IRQ}$, unless interrupts are pending from other sources. Disabling a channel, however, does not affect the corresponding bit in interrupt in-service registers A or B. So, if the CMFP is in the software end-of-interrupt mode (see) and an interrupt is in service when a channel is disabled, the in-service status bit for that channel will remain set until cleared by software.

(a) Interrupt Enable Registers (IERA and IERB)

	7	6	5	4	3	2	1	0
Address 07 (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 09 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is zero the associated interrupt channel is disabled. When a bit is a one the associated interrupt channel is enabled.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(b) Interrupt Pending Registers (IPRA and IPRB)

	7	6	5	4	3	2	1	0
Address 0B (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 0D (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, no interrupt is pending on the associated interrupt channel. When a bit is a one, an interrupt is pending on the associated interrupt channel.
SET a) Interrupt is received on an enabled interrupt channel.
CLEARED a) Interrupt vector for the associated interrupt channel is passed during an $\overline{IACK}$ cycle.
b) Associated interrupt channel is disabled.
c) MPU writes a zero.
d) Reset.

(c) Interrupt In-Service Registers (ISRA and ISRB)

	7	6	5	4	3	2	1	0
Address 0F (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 11 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, no interrupt processing is in progress for the associated interrupt channel. When a bit is a one, interrupt processing is in progress for the associated interrupt channel.
SET a) Interrupt vector number for the associated, interrupt channel is passed during an $\overline{IACK}$ cycle and the S bit of the vector register is set.
CLEARED a) Interrupt service is completed for the associated interrupt channel.
b) The S bit of the vector register is a zero.
c) MPU writes a zero.
d) Reset.

(d) Interrupt Mask Registers (IMRA and IMRB)

	7	6	5	4	3	2	1	0
Address 13 (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 15 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, interrupts are masked for the associated interrupt channel. When a bit a one, interrupts are not masked for the associated interrupt channel.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 31 : Interrupt control registers.

6.2.3.2 - Interrupt pending registers

When an interrupt is received on an enabled, the corresponding interrupt pending bit is set in interrupt pending register A or B (IPRA or IPRB). In a vectored interrupt scheme, this bit will be cleared when the processor acknowledges the interrupting channel and the CMFP responds with a vector number. In a polled interrupt system, the interrupt pending registers must be read to determine the interrupting channel and then the interrupt pending bit is cleared by the interrupt handling routine without performing an interrupt acknowledge sequence.

A single bit of the interrupt pending registers is cleared in software by writing ones to all bit positions except the bit to be cleared. This allows any one bit to be cleared, without altering any other bits, simply by writing all ones except for the bit position to be cleared to IPRA or IPRB. Thus a fully polled interrupt scheme is possible. Note that writing ones to IPRA and IPRB has no effect on the contents of the register. A single bit of the interrupt pending registers is also cleared when the corresponding channel is disabled by writing a zero to the appropriate bit of IERA or IERB.

6.2.3.3 - Interrupt mask registers

Interrupts are masked for a channel by clearing the appropriate bit in interrupt mask register A or B (IMRA or IMRB). Even though an enabled channel is masked, the channel will recognize subsequent interrupts and set its interrupt pending bit. Howevern, the channel is prevented from requesting interrupt service (IRQ to the processor) as long as the mask bit for that channel is cleared.

If a channel is requesting interrupt service at the time that its corresponding bit in IMRA or IMRB is cleared, the request will cease and IRQ will be negated, unless another channel is requesting interrupt service. Later, when the mask bit is set, any pending interrupt on the channel will be processed according to the channel's assigned priority. IMRA and IMRB may be read at any time.

6.2.4 - Nesting CMFP interrupts

In a 68000 vectored interrupt system, the CMFP is assigned to one of seven possible interrupt levels. When an interrupt is received from the CMFP, an interrupt acknowledge for that level is initiated. Once an interrupt is recognized at a particular level, interrupts at that same level or below are masked by 68000. As long as the processor's interrupt mask is unchanged, the 68000 interrupt structure will prohibit the nesting of interrupts at the same interrupt level. However, additional interrupt requests from the CMFP can be recognized before a previous channel's interrupt level within the interrupt handler.

When nesting CMFP interrupts it may be desirable to permit interrupts on any CMFP channel, regardless of its priority, to preempt or delay interrupt processing of an earlier channel's interrupt service request. Or, it may be desirable to only allow subsequent higher priority interrupt requests. The CMFP interrupt structure provides this flexibility by offerinG two end-of-interrupt options for vectored interrupt schemes. Note that the end-of-interrupt modes are not active in a polled interrupt schema.

6.2.4.1 - Selecting the end-of-interrupt mode

In a vectored interrupt scheme, the CMFP may be programmed to operate in either the automatic end-of-interrupt mode of the software end-of-interrupt mode. The mode is selected by writing the S bit of the vector register (see Figure 29).

When the S bit is programmed to a one, the CMFP is placed in the software end-of-structure mode and when the S bit is a zero, all channels operate in the automatic end-of-interrupt mode.

6.2.4.2 - Automatic end-of-interrupt

When an interrupt vector number is passed to the processor during an interrupt acknowledge cycle, the corresponding channel's interrupt pending bit is cleared. In the automatic end-of-interrupt mode, no further history of the interrupt remains in the CMPF. The in-service bits of the interrupt in-service registers (ISRA and ISRB) are force low. Subsequent interrupts which are received on any CMFP channel will generate an interrupt request to the processor, even if the current interrupt's service routine has not been completed.

6.2.4.3 - Software end-of-interrupt

In the software end-of-interrupt mode, the channel's associated interrupt pending bit is cleared and in addition, the channel's in-service bit of in-service register A or B is set when its vector number is passed to the processor during an IACK cycle. A higher priority channel may subsequently request interrupt service and be acknowledged, but as long as the channel's in-service bit is set, no lower priority channel may request interrupt service nor pass its vector during an interrupt acknowledge sequence.

While only higher priority channels may request interrupt service, any channel can receive an interrupt and set its interrupt pending bit. Even the channel whose in-service bit is set can receive a second interrupt. However, no interrupt service request is made until its in-service bit is cleared.

The in-service bit for a particular channel can be cleared by writing a zero to its corresponding bit in ISRA or ISRB and ones to all other bit positions. Since bits in the in-service registers can only be cleared in software and not set, writing ones to the registers does not alter their contents. ISRA and ISRB may be read at any time.

6.3 - General purpose input/output interrupt port

The general purpose interrupt input/output (I/O) port (GPIP) provides eight I/O lines (10 through 17) that may be oprerated as either inputs or outputs under software control. In addition, these lines may optionally generate an interrupt on either a positive transition or a negative transition of the input signal. The flexibility of the GPIP allows it to be configured as an 8-bit I/O port or for bit I/O. Since interrupts are enabled on an bit-by-bit basis, a subset of the GPIP could be programmed as handshake lines or the port could be connected to as many as eight external interrupt sources, which would be prioritized by the CMFP interrupt controller for interrupt service.

6.3.1 · 6800 interrupt controller

The CMFP interrupt controller is particularly useful in a system which has many 6800-type devices. Typically, in a vectored 68000 system, 6800-type peripherals use the autovector which corresponds to their assigned interrupt level since they do not provide a vector number in response to an IACK cycle. The autovector interrupt handler must then poll all 6800-type devices at that interrupt level to determine which device is requesting service. However, by tying the IRQ output from a 6800-type device to the general purpose I/O interrupt port (GPIP) of a CMFP, a unique vector number will be provided to the processor during an interrupt acknowledge cycle. This interrupt structure will significantly reduce interrupt latency for 6800-type devices and other peripheral devices which do not support vector-by-device.

6.3.2 · GPIP control registers

The GPIP is programmed via three control registers shown in Figure 32. These registers control the data direction, provide user access to the port and specify the active edge for each bit of the GPIP which will produce an interrupt. These registers are described in detail in the following paragraphs.

6.3.2.1 · GPIP data register

The general purpose I/O data register is used to input or output data to the port. When data is written to the GPIP data register, those pins which are defined as inputs will remain in the high-impedance state. Pins which are defined as outputs will assume the state (high or low) of their corresponding bit in the data register. When the GPIP is read, data will be passed directly from the bits of the data register for pins which are defined as outputs. Data from pins defined as inputs will come from the input buffers.

6.3.2.2 · Active edge register

The active edge register (AER) allows each of the GPIP lines to produce an interrupt on either a one-to-zero or a zero-to-one transition. Writing a zero to the appropriate edge bit of the active edge register causes the associated input to generate an interrupt on the one-to-zero transition of the corresponding GPIP line.

(a) GPIP Data Register (GPIP)

	7	6	5	4	3	2	1	0
Address 01 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(b) Active Edge Register (AER)

	7	6	5	4	3	2	1	0
Address 03 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, interrupts will be generated on the falling edge of the associated input signal. When a bit is a one, interrupts will be generated on the rising edge of the associated input signal.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(c) Data Direction Register (DDR)

	7	6	5	4	3	2	1	0
Address 05 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, the associated I/O line is defined to be an input. When a bit is a one, the associated I/O line is defined to be an output.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 32 : GPIP control registers.

Note : The transition detector is an exclusive-OR gate whose inputs are the edge bit and the input buffer. As a result, writing the AER may cause an interrupt-producing transition, depending upon the state of the input. So, the AER should be configured before enabling interrupts via the interrupt enable registers (IERA and IERB). Also, changing the edge bit while interrupts are enabled may cause an interrupt on the corresponding channel.

6.3.2.3 · Data direction register

The data direction register (DDR) allows the programmer to define 10 through 17 as inputs or outputs by writing the corresponding bit. When a bit of the data direction register is written as a zero, the corresponding interrupt I/O pin will be a high-impedance input. Writing a one to any bit of the data direction register will cause the corresponding pin to be configured as a push-pull output.

6.4 · Timers

The CMFP contains four 8-bit timers which provide many functions typically required in microprecessor systems. The timers can supply the baud rate clocks for the on-chip serial I/O channel, generate periodic interrupts, measure elapsed time, and count signal transitions. In addition, two timers have waveform generation capability.

All timers are prescaler/counter timers with a common independent clock input (XTAL1 or XTAL2) and are not required to be operated from the system clock. Each timer's output signal toggles when the timer's main counter times out. Additionally, timers A and B have auxiliary control signals which are used in two of the operation modes. An interrupt channel is assigned to each timer and when the auxiliary control signals are used, a separate interrupt channel will respond to transitions on these inputs.

6.4.1 · Operation modes

Timers A and B are full function timers which, in addition to the delay mode, operate in the pulse width measurement mode and the event count mode. Timers C and D are delay timers only. A brief discussion of each of the timer modes follows.

6.4.1.1 · Delay mode operation

All timers may operate in the delay mode. In this mode the prescaler is always active. The prescaler specifies the number of timer clock cycles which must elpase before a count pulse is applied to the main counter. A count pulse causes the main counter to decrement by one. When the timer has decremented down to 01 (hexadecimal), the next count pulse will cause the main counter to be reloated from the timer's interrupt channel time out pulse also causes the timer output pin to toggle. The output will remain in this new state until the next time out pulse occurs.

For example, if delay mode with a divide-by-10 prescaler is selected and the timer data register is loaded with 100 (decimal), the main counter will decrement once every 10 timer clock cycles. After 1,000 timer clocks, a time out pulse will be produced. This time out pulse will generate an interrupt if the channel is enabled (IERA, IERB) and in addition the timer's output line will toggle. The output line will complete one full periode every 2,000 cycles of the timer clock.

The main counter is an 8-bit binary down counter. It may be read at any time by reading the Timer Data Register. The information read is the information last clocked into the timer read register when the $\overline{DS}$ pin had last gone high prior to the current read cycle. When written, data is loaded into the Timer Data Register, and the main counter, if the timer is stopped. If the Timer Data Register is written while the timer is running, the new word is not loaded into the timer until it counyer through H«01». However, if the timer is written while it is counting through H«01», an indeterminate value will be written into the timer constant register. This may be circumvented by ensuring that the data register is not written when the count is H«01».

If the prescaler value is changed while the timer is enabled, the first time out pulse will occur at an indeterminate time no less than one nor more than 200 timer clock cycles. Subsequent time out pulses will then occur at the correct interval.

If the main counter is loaded with 01 (hexadecimal), a time out pulse will occur every time the prescaler presents a count pulse to the main counter. If the main counter is loaded with 00, a time out pulse will occur every 256 count pulses.

6.4.1.2 · Pulse width measurement operation

Besides the delay mode, timers A and B may be programmed to operate in the pulse width measurement mode. In this mode an auxiliary control input is required ; timers A and B auxiliary input are TAI and TBI. Also, in the pulse width measurement mode, interrupt channels normally associated with 14 and 13 will respond to transitions on TAI and TBI, respectively. General purpose lines 13 and 14 may still be used for I/O. A conceptual circuit of the timers in the pulse width measurement mode is shown in Figure 33.

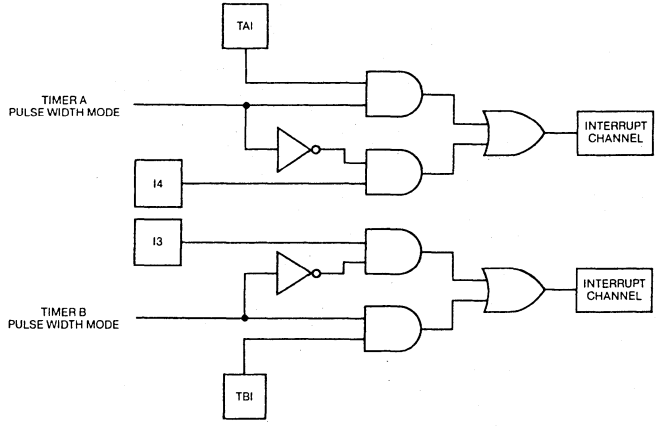


Figure 33 : Conceptual circuit of timers A and B in pulse width measurement mode.

The pulse width measurement mode functions similarly to the delay mode, with the auxiliary control signal acting as an enable to the timer. When the control signal is active, the prescaler and main counter are allowed to operate. When the control signal is negated, the timer is stopped. So, the width of the active pulse on TAI or TBI is measured by the number of timer counts which occur wile the timer is allowed to operate.

The active state of the auxiliary input line is defined by the associated interrupt channel's edge bit in the active edge register (AER). GPIP4 of the AER is the edge bit associated with TAI and GPIP3 is associated with TBI. When the edge bit is a one, the auxiliary input will be active high, enabling the timer while the input signal is at a high level. If the edge bit is low, the auxiliary input will be active low and the timer will operate while the input signal is at a low level.

The state of the active edge bit also specifies whether a zero to-one transition or a one-to-zero transition of the auxiliary input pin will produce an interrupt when the interrupt channel is enabled. In normal operation, programming the active edge bit to a zero will produce an interrupt on the one-to-zero transition of the input signal. However, in the pulse width measurement mode, the interrupt generated by a transition on TAI or TBI will occur on the opposite transition as that normally defined by the edge bit.

For example, in the pulse width measurement mode, if the edge bit is a one, the timer will be allowed to run while the auxiliary input TAI is high. When TAI transitions from high to low, the timer will stop and, if the interrupt channel is enabled, an interrupt will occur. By having the interrupt occur on the one-to-zero transition instead of the zero-to-one transition, the processor will be interrupted when the pulse being measured has terminated and the width of the pulse is available from the timer. Therefore, the timers act like a divide-by-prescaler that can be programmed by the timer data register and the timer's A and B control register.

After reading the contents of the timer, the main counter must be reinitialized by writing to the timer data register to allow consecutive pulses to be measured. If the timer is written after the auxiliary input signal is active, the timer will count from the previous contents of the timer data register until it counts through 01 (hexadecimal). At that time, the main counter is loaded with the new value from the timer data register, a time out pulse is generated which will toggle the timer output, and an interrupt may be optionally generated on the timer interrupt channel. Note that the pulse width measured will include counts from before the main counter was reloaded. If the timer data register is written while the pulse is transtioning to the active state, an indeterminate value may be written into the main counter.

Once the timer is reprogrammed for another mode, interrupts will again occur as normally defined by the edge bit. Note that an interrupt may be generated as the result of placing the timer into the pulse width measurement mode or by reprogramming the timer for another mode. Also, an interrupt may be generated by changing the stae of the edge bit while in the pulse width measurement mode.

6.4.1.3 - Event count mode operation

In addition to the delay mode and the pulse width measurement mode, timers A and B may be programmed to operate in the event count mode. Like the pulse width measurement mode, the event count mode also requires an auxiliary input signal, TAI or TBI, and the interrupt channels normally associated with 14 and 13 will respond to transitions on TAI and TBI, respectively. General purpose lines 13 and 14 still function normally.

In the event count mode the prescaler is disabled, allowing each active transition on TAI and TBI to produce a count pulse. The count pulse causes the main counter to decrement by one. When the timer counts through 01 (hexadecimal), a time out pulse is generated which will cause the output signal to toggle and may optionally produce an interrupt via the associated timer interrupt channel. The timer's main counter is also reloated from the timer clock periods. For this reason, the input signal must have a maximum frequency equal to one-fourth that of the timer clock.

The active edge of the auxiliary input signal is defined by the associated interrupt channel's edge bit. GPIP4 of the AER specifies the active edge for TAI and GPIP3 defines the active edge for TBI. When the edge bit is programmed to a one, a count pulse will be generated on the zero-to-one transition of the auxiliary input signal. When the edge bit is programmed to a zero, a count pulse will be generated on the one-to-zero transition. Also, note that changing the state of the edge bit while the timer is in the event count mode may produce a count pulse.

Besides generating a count pulse, the active transition of the auxiliary input signal will also produce an interrupt on the 13 or 14 interrupt channel, if the interrupt channel is enabled. Typically, in the event count mode, these channels are not enabled since the timer is automatically counting transitions on the input signal. If the interrupt channel were enabled, the number of transitions could be counted in the interrupt routine without requiring the use of the timer.

6.4.2 - Timer registers

The four timers are programmed via three control registers and four timer data registers. Control registers TACR and TBCR and timer data registers TADR and TBDR (refer to figure are associated with timers A and B respectively. Timers C and D are controlled by the control register TCDCR and the data registers TCDR and TDDR (refer to Figure 34).

(a) Timer A Data Register (TADR)

	7	6	5	4	3	2	1	0
Address 1F (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(b) Timer B Data Register (TBDR)

	7	6	5	4	3	2	1	0
Address 21 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(c) Timer C Data Register (TCDR)

	7	6	5	4	3	2	1	0
Address 23 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(d) Timer D Data Register (TDDR)

	7	6	5	4	3	2	1	0
Address 25 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

Figure 34 : Timer data registers.

6.4.2.1 - Timer data registers

Each timer's main counter is an 8-bit binary down counter. The value of the main counter may be read at any time by reading the timer's data register. The information read is the value of the counter which was captured on the last low-to-high transition of the DS pin.

The main counter is initialized by writing to the timer's data register. If the timer is stopped, data is loaded simultaneously into both the timer data register and the main counter. If the timer data register is written while the timer is enabled, the value is not loaded into the timer until the timer counts through 01 (hexadecimal). Writing the timer data register while the timer is counting through 01 (hexadecimal) will cause an indeterminate value to be loaded into the timer's main counter. The four data registers are shown in Figure 34.

6.4.2.2 - Timer control registers

Bits in the timer control registers select the operation mode, select the prescale value, and disable the timers. Timer control registers TACR and TBCR also have bits which allow the programmer to reset output lines TAO and TBO. These control registers are shown in Figure 35.

(a) Timer A Control Register (TACR)

	7	6	5	4	3	2	1	0
Address 19 (Hex)	★	★	★	Reset TA0	AC3	AC2	AC1	AC0

★ Unused bits read as zero.

(b) Timer B Control Register (TBCR)

	7	6	5	4	3	2	1	0
Address 1B (Hex)	★	★	★	Reset TB0	BC3	BC2	BC1	BC0

★ Unused bits read as zero.

Reset TAO/TBO : Timer's A and B output lines (TAO and TBO) may be forced low at any time by writing a one the reset location in TACR and TBCR respectively. The output will be held low only during the write operation at the conclusion of the operation the output will be allowed to toggle in response to a time-out pulse. When resetting TAO and TBO, the remaining bits in the control register must be written with their previous value to avoid altering the operating mode.
SET a) End of write cycle which clears the bit.
CLEARED a) MPU writes a zero.
b) Reset.

AC3-AC0, BC3-BC0 : These bits are decoded to determine the timer operation mode.

AC3 BC3	AC2 BC2	AC1 BC1	AC0 BC0	Operation Mode
0	0	0	0	Timer Stopped*
0	0	0	1	Delay Mode, + 4 Prescaler
0	0	1	0	Delay Mode, + 10 Prescaler
0	0	1	1	Delay Mode, + 16 Prescaler
0	1	0	0	Delay Mode, + 50 Prescaler
0	1	0	1	Delay Mode, + 64 Prescaler
0	1	1	0	Delay Mode, + 100 Prescaler
0	1	1	1	Delay Mode, + 200 Prescaler
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, + 4 Prescaler
1	0	1	0	Pulse Width Mode, + 10 Prescaler
1	0	1	1	Pulse Width Mode, + 16 Prescaler
1	1	0	0	Pulse Width Mode, + 50 Prescaler
1	1	0	1	Pulse Width Mode, + 64 Prescaler
1	1	1	0	Pulse Width Mode, + 100 Prescaler
1	1	1	1	Pulse Width Mode, + 200 Prescaler

* Regardless of the operation mode, counting is inhibited when the timer is stopped. The contents of the timer's main counter is not affected, althought any residual count in the prescaler is lost.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(c) Timers C and D Control Register (TCDCR)

	7	6	5	4	3	2	1	0
Address 1D (Hex)	★	CC2	CC1	CC0	★	DC2	DC1	DC0

★ Unused bits read as zero.

CC2 - CC0 DC2 - DC0 : The bits are decoded to determine the timer operation mode.

CC2 DC2	CC1 DC1	CC0 DC0	Operation Mode
0	0	0	Timer Stopped*
0	0	1	Delay Mode, + 4 Prescaler
0	1	0	Delay Mode, + 10 Prescaler
0	1	1	Delay Mode, + 16 Prescaler
1	0	0	Delay Mode, + 50 Prescaler
1	0	1	Delay Mode, + 64 Prescaler
1	1	0	Delay Mode, + 100 Prescaler
1	1	1	Delay Mode, + 200 Prescaler

* When the timer is stopped, counting is inhibited. The contents of the timer's main counter is not affected, although any residual count in the prescaler is lost.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 35 : Timer control registers.

6.5 · Universal synchronous/asynchronous receiver-transmitter

The universal synchronous/asynchronous receiver-transmitter (USART) is a single full-duplex serial channel with a double-buffered receiver and transmitter. There are separate receive and transmit clocks and separate receive and transmit status and data bytes. The receive and transmit sections are also assigned separate interrupt channels. Each section has both a normal condition interrupt channel and an error condition interrupt channel. These channels can be optionally disabled from interrupting the processor and instead, DMA transfers can be performed using the receiver ready and transmitter ready external CMFP signals.

6.5.1 · Character protocols

The CMPFP USART supports asynchronous and with the aid of a polynomial generator checker (PGC) supports byte synchronous character formats. These formats are selected independently of the divide-by-one and divide-by-16 clock modes.

When the divide-by-one clock mode is selected, synchronization must be accomplished externally. The receiver will sample the serial data on the rising edge of the receiver clock. In the divide-by-16 clock mode, the data is sampled at mid-bit time to increase transient noise rejection.

Also, when the divide-by-16 clock is selected, the USART resynchronization logic is enabled. This logic increases the channel's clock skew tolerance. When a valid transition is detected, an internal counter is reset to state zero. Transition checking is then inhibited until state four. Then at state eight, the previous state of the transition checking logic is clocked into the receive shift register.

6.5.1.1 · Asynchronous format

Variable word length and start/stop bit configurations are available under software control for asynchronous operation. The word length can be five to eight bits and one, one and one-half, or two stop bits can be selected. The user can also slect odd, even, or no parity. For character lengths of less than eight bits, the assembled character will consist of the required number of data bits followed by zeros in the unused bit positions and a parity bit, if parity is enabled.

In the asynchronous format, start bit detection is always enabled. New data is not shifted into the receive shift register until a zero bit is received. When the divide-by-16 clock mode is selected, the false start bit logic is also active. Any transition must be stable for three positive receive clock edges to be considered valid. Then a valid zero-to-one transition must not occur for at least eight additional positive clock edges.

5

6.5.1.1.1 · Wake-up feature

In a typical serial loop multiprocessor configuration, the software protocol will usually identify the addresse(s) at the beginning of the message. In order to permit uninterested MPUs to ignore the remainder of the message, wade-up feature is included whereby all further USART receiver flag (and interrupt) processing can be inhibited until its data line goes idle. An USART receiver is re-enabled by an idle string of ten consecutive ones of during reset. Software must provide for the required idle string between consecutive messages and prevent it within messages.

6.5.1.2 · Synchronous format

When the synchronus character format is selected, the 8-bit synchronous character loaded into the synchronous character register is compared to received serial data until a match is found. Once synchronization is established, incoming data is clocked into the receiver. The synchronous word will be continuously transmitted during an underrun condition. All synchronous characters can be optionally stripped from the receive buffer. Figure 36 shows the synchronous character register.

	7	6	5	4	3	2	1	0
Address 27 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

Figure 36 : Synchronous character register (SCR).

The synchronous character is typically written after the data word length is selected, since unused bits in the synchronous character register are zeroed out. When parity is enabled, synchronous word length is the data word length plus one. The CMFP will compute and append the parity bit for the synchronous word when a word length of eight is selected. However, if the word length is less than eigth, the user must determine the synchronous word parity and write it into the synchronous character register along with the synchronous character. The CMFP will then transmit the extra bit in the synchronous word as a parity bit.

6.5.1.3 · USART control register

The USART control register (UCR) selects the clock mode and the character format for the receive and transmit sections. This register is shown in Figure 37.

6.5.2 · Receiver

As data is received on the serial input line (S1), it is clocked into an internal 8-bit shift register until the specified number of data bits have been assembled. This character will then be transferred to the receive buffer, assuming that the last word in the receiver buffer has been read. This transfert produces a buffer full interrupt to the processor.

Reading the receive buffer satisfies the buffer full condition and allows a new data word to be transferred to the receive buffer when it is assembled. The receive buffer is accessed by reading the USART data register (UDR). The UDR is simply an 8-bit data register used when transferring data from the CMFP and the CPU.

Each time a word is transferred to the receive buffer, its status information is latched into the receiver status register (RSR). The RSR is not updated again until the data word in the receive buffer has been read. When a buffer full condition exists, the RSR should always be read before the receive buffer (UDR) to maintain the correct correspondance between data and flags. Otherwise, it is possible that after reading the UDR and prior to reading the RSR, a new word could be received and transferred to the receive buffer. Its associated flags would ba latched into the RSR overwriting the flags for the previous data word. Then when the RSR were read to access the status information for the first data word, the flags for the new word would be retrieved.

	7	6	5	4	3	2	1	0
Address 29 (Hex)	CLK	WL1	WL0	ST1	ST0	PE	E/O	WU

CLK : Clock Mode. When this bit is zero, data will be clocked into and out of the receiver and transmitter at the frequency of their respective clocks. When this bit is a one, data will be clocked into and out of the receiver and transmittor at one sixteenth the frequency of their respective clocks. Also, the receiver data transition resynchronization logic will be enabled.
SET + 16 a) MPU writes a one.
CLEARED + 1 a) MPU writes a zero.
b) Reset.

WL0, WL1 : Word Length. These two bits specify the length of the data word exclusive of start bits, stop bits, and parity.

WL1	WL0	Word Length
0	0	8 Bits
0	1	7 Bits
1	0	6 Bits
1	1	5 Bits

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

ST0, ST1 : Start/Stop Bit and format control. These two bits select the number of start and stop bits and also specify the character format.

ST1	ST0	Start Bits	Stop Bits	Format
0	0	0	0	Synchronous
0	1	1	1	Asynchronous
1	0	1	1 1/2	Asynchronous*
1	1	1	2	Asynchronous

* Only used with divide-by-16 clock mode.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

PE : Parity Enable. When this bit is zero, no parity check will be made and no parity bit will be computed for transmission. When this bit is a one, parity will be checked by the receiver and parity will be calculated and inserted during data transmission. Note that parity is not automatically appended to the synchronous character for word lengths of less than eight bits in this case, the parity should be written into the synchronous character register along with the synchronous word.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

E/O : Even/Odd Parity. When this bit is zero, odd parity is selected. When this bit is a one, even parity is selected.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

WU : Bit 0 «Wake-up» in idle line. When set, WU enables the wake-up function ; it is cleared by ten consecutive ones or during reset. WU will not be set if the line is idle. Refer to § 6.5.1.1.1.

Figure 37 : Usart control register (UCR).

6.5.2.1 - Receiver interrupt channels

The USART receive section, is assigned two interrupt channels. One indicates the buffer full condition, while the other channel indicates an error condition. Error conditions include overrun, parity error, synchronous found, and break. These interrupting conditions correspond to the BF, OE, PE, and F/S or B bits of the receiver status register. These flags will function as described in § 6.5.2.2 whether the receiver interrupt channels are enabled or disabled.

While only one interrupt is generated per character received, two dedicated interrupt channels allow separate vector numbers to be assigned for normal and abnormal receiver conditions. When a received word has an error associated with it and the error interrupt channel is enabled, an interrupt will be generated on the error channel only. However, if the error channel is disabled, an interrupt for an error condition will be generated on the buffer full interrupt channel along with interrupts produced by the buffer full condition. The receiver status register must always be read to determine which error condition produced the interrupt.

6.5.2.2 - Receiver status register

The receiver status contains the receive buffer full flag, the synchronous strip enable, the receiver enable, and various status information associated with the data word in the receive buffer. The RSR is latched each time a data word is transferred to the receive buffer. RSR flags cannot change again until the data word has been read. The exception is the character in progress flag which monitors when a new word is being assembled in the asynchronous character format. The receiver status register is shown on Figure 38.

Address 2B	BF	OE	PE	FE	F/S or B	M/CIP	SS	RE

BF : Buffer Full. This bit is set when a received word is transferred ot the receive buffer. This bit is cleared when the receive buffer is read by accessing the USART data register (UDR) this bit is read only.
SET a) Received word transferred to buffer.
CLEARED a) Receive buffer read.
b) Reset.

OE : Overrun Error. An overrun error occurs when a received word is due to be transferred to the receive buffer, but the receive buffer is full. Neither the receive buffer not the RSR is overwritten. The OE bit is set after the receive buffer full condition is satisfied by reading the UDR. This error condition will generate an interrupt to the processor. The OE bit is cleared by reading the RSR. New data words will not be assembled until the RSR is read.
SET a) Incoming word received and receive buffer full.
CLEARED a) Receiver status register read.
b) Reset.

PE : Parity Error. This bit is set when the word transferred to the receive buffer has a parity error. This bit is cleared when the word transferred to the receive buffer does not have a parity error.
SET a) Word in receive buffer has a parity error.
CLEARED a) Word in receive buffer does not have a parity error.
b) Reset.

FE : Frame Error. A frame error exists when a non-zero data word is not followed by a stop bit in the asynchronous character format. The FE bit is set when the word transferred to the receive buffer has a frame erro. The FE bit is cleared when the word transferred to the receive buffer does not have a frame error.
SET a) Word in receive buffer has a frame error.
CLEARED a) Word in receive buffer does not have a frame error.
b) Reset.

F/S or B : Found/Search or Break Detect. In the synchronous character format this bit can be set or cleared in software. When the bit is a zero, the USART receiver is placed in the search mode. The incoming data is compared to the synchronous character register (SCR) and the word length counter is disabled. The F/S bit will automatically be set when a match is found and the word length counter will be enabled. An interrupt will also be produced on the receive error channel.
SET a) Incoming word matches synchronous character.
CLEARED a) MPU writes a zero.
b) Incoming word does not match synchronous character.
c) Reset.

In the asynchronous character format, this flag indicates a break condition. A break is detected when an all zero data word with no stop bit is received. The break condition continues until a non-zero data bit is received. The B bit is set when the word transferred to the receive buffer is a break indication. A break condition generates an interrupt to the processor. This bit is cleared when a non-zero data bit is received and the break condition has been acknowledged by reading the RSR at least once. An end of break interrupt will be generated when the bit is cleared.
SET a) Word in receive buffer is a break.
CLEARED a) Break terminates and receiver status register read since beginning of break condition.
b) Reset.

M or CIP : Match/Character in Progress. In the synchronous character format, this flag indicates that a synchronous character has been received. The M bit is set when the word transferred to the receive buffer matches the synchronous character register. The M bit is cleared when the word transferred to the receive buffer does not match the synchronous character register.
SET a) Word transferred to receive buffer matches the synchronous character.
CLEARED a) Word transferred to receive buffer does match synchronous character.
b) Reset.

In the asynchronous character format, this flag indicates that a word is being assembled. The CIP bit is set when a start bit is detected. The CIP bit is cleared when the final stop bit has been received.
SET a) Start bit is detected.
CLEARED a) End of word detected.
b) Reset.

SS : Synchronous Strip Enable. When this bit is a one, data words that match the synchronous character register will not be loaded into the receive buffer and no buffer full condition will be produced. When this bit is a zero, data words that match the synchronous character register will be transferred to the receive buffer and a buffer full condition will be produced.
SET a) MPU writes a one.
CLEARED a) MPU writtes a zero.
b) Reset.

RE : Receiver Enable. When this bit is a zero, the receiver will be immediately disabled. All flags will be cleared. When this bit is a one, normal receiver operation is enabled. This bit should not be set to a one until the receiver clock is active.
SET a) MPU writes a one.
b) Transmitter is disabled in auto-turnaround mode.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 38 : Receiver status register (RSR).

6.5.2.3 - Special receive considerations

Certain receive conditions relating to the overrun error flag and the break detect flag require further explanation. Consider the following examples :

1) A break is received while the receive buffer is full. This does not produce an overrun condition. Only the B flag will be set after the receiver buffer is read.

2) A new word is received and the receive buffer is full. A break is received before the receive buffer is read. Both the B and OE flags wil be set when the buffer full condition is satisfied.

6.5.3 - Transmitter

The transmit buffer is loaded by writing to the USART data register (UDR). The data word will be transferred to an internal 8-bit shift register when the last word in the shift register has been transmitted. This will produce a buffer empty condition. If the transmitter completes the transmission of the word in the shift register before a new word is written to the transmit buffer, an underrun error will occur. In the asynchronous character format, the transmitter will send a mark until the transmit buffer is written. In the synchronous character format, the transmitter will continuously send the synchronous character.

The transmit buffer can be loaded prior to enabling the transmitter. After the transmitter is enabled, there is a delay before the first bit is output. The serial output line (SO) should be programmed to be high, low, or high impedance when the transmitter is enabled to force the output line to the desired state until the transmitted prior to the word in the transmit shitf register when the transmitter is first enabled.

When the transmitter is disabled, any word currently being transmitted will continue to completion. Howerver, any word in the transmit buffer will not be transmitted and will remain in the buffer. So, no buffer empty condition will occur. If the buffer is empty when the transmitter is disabled, the buffer empty condition will remain, but no underrun condition will be generated when the word in transmission is completed. If no word is being transmitted when the transmitter is disabled, the transmitter will stop at the next rising edge of the internal shift clock.

In the asynchronous character format, the transmitter can be programmed to send a break. The break will be transmitted once the word currently in the shift register has been sent. If the shift register is empty, the break command will be effective immediately. An END interrupt will be generated at every normal character boundary to aid in timing the break transmission. The break will continue until the break command is cleared.

Any character in the transmit buffer at the start of a break will be transmitted when the break is terminated. If the transmit buffer is empty at the start of a break, it may be written at any time during the break. If the buffer is still empty at the end of the break, an underrun condition will exist.

Disabling the transmitter during a break condition causes the transmitter to cease transmission of the break character at the end of the current character. No end of break stop bit will be transmitted. Even if the transmit buffer is empty, no buffer empty condition will occur nor will an underrun condition occur. Also, any word in the transmit buffer will remain.

6.5.3.1 - Transmitter interrupt channels

The USART transmit sectin is assigned two interrupt channels. One channel indicates a buffer empty condition and the other channel indicates an underrun or end condition. These interrupting conditions correspond to the BE, UE, and END flag bits of the transmitter status register (TCR). The flag bits will function as described in § 6.5.3.2 whether their associated interrupt channel is enabled or disabled.

6.5.3.2 - Transmitter status register

The transmitter status register contains various transmitter error flags and transmitter control bits for selecting autoturnaround and loopback mode. The TSR is shown in Figure 39.

	7	6	5	4	3	2	1	0
Address 2D (Hex)	BE	UE	AT	END	B	H	L	TE

BE : Buffer Empty. This bit is set when the word in the transmit buffer is transferred to the transmit shift register. This bit is cleared when the transmit buffer is reloaded by writing to the USART data register (UDR).
SET a) Transmit buffer contents transferred to transmit shift register.
CLEARED a) Transmit buffer written.

UE : Underrun Error. This bit is set when the would in the transmit shift register has been transmitted before a new word is loaded into the transmit buffer. This bit is cleared by reading the TSR or by disabling the transmitter. This bit does not need to be cleared before writing to the UDR.
SET a) Transmit shift register contents transmitted before transmit buffer written.
CLEARED a) Transmitter status register read.
b) Transmitter disabled.

AT : Auto Turnaround. When this bit is set, the receiver will be enabled automatically after the transmitter has been disabled and the last character being transmitted is completed.
SET a) MPU writes a one.
CLEARED a) Transmitter disabled.

END : End of Transmission. When the transmitter is disabled while a character is being transmitted, the END with be set after the character transmission is complete. If no word is being transmitted when the transmitter is disabled, the END bit will be set immediately. The END bit is cleared by reenabling the transmitter.
SET a) Transmitter disabled.
CLEARED a) Transmitter enabled.

B : Break. This bit has no function in the synchronous character format. In the asynchronous character format, when this bit is set to a one, a break will be transmitted upon the completion of the transmission of any word in the transmit shift register. A break consists of an all zero data word with no stop bit. When this bit is cleared by software, the break indication will cease and normal transmission will resume. Note that when B is set, BE cannot be set.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

H, L : High and Low. These control bits configure the transmitter output (SO) when the transmitter is disabled. These bits also force the transmitter output after the transmitter is enabled until END is cleared.

H	L	Output State
0	0	High Impedance
0	1	Low
1	0	High
1	1	Loopback Mode

Loopback mode internally connects the transmitter output to the receiver input and the transmitter clock to the receiver clock internally. The receiver clock (RC) and the serial input (SI) are not used. When the transmitter is disabled. SO is forced high.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

TE : Transmitter Enable. When this bit is cleared, the transmitter is disabled. The UE will be cleared and the END bit will be set. When this bit is set, the transmitter is enabled. The transmitter output will be driven according to the H and L bits until transmission begins. A one bit will be transmitted before the transmission of the word in the transmit shift register is begun.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 39 : Transmitter status register (TSR).

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

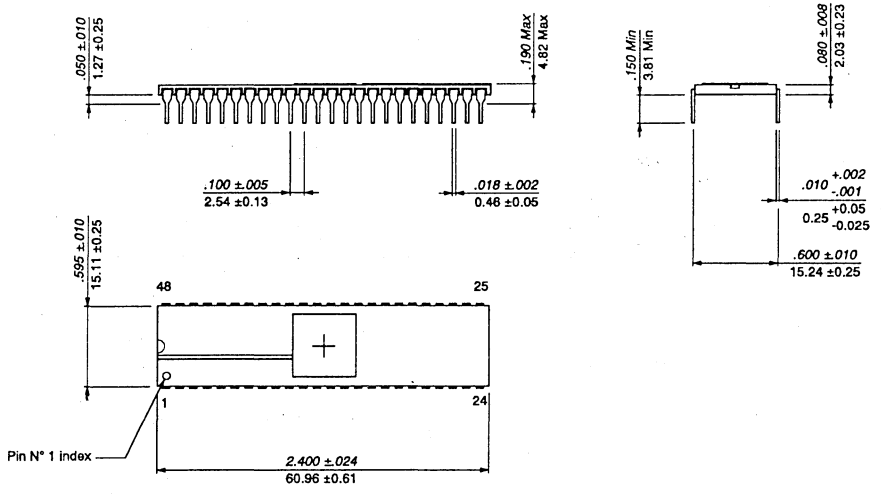
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

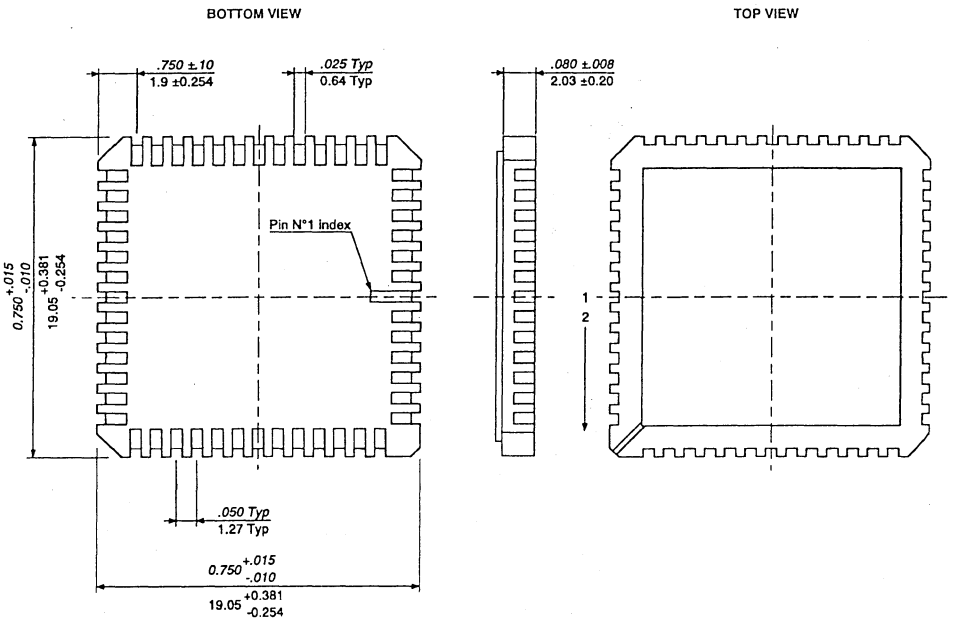
a) Devices should be handled on benches with conductive and grounded surfaces.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent if practical.

9 · PACKAGE MECHANICAL DATA

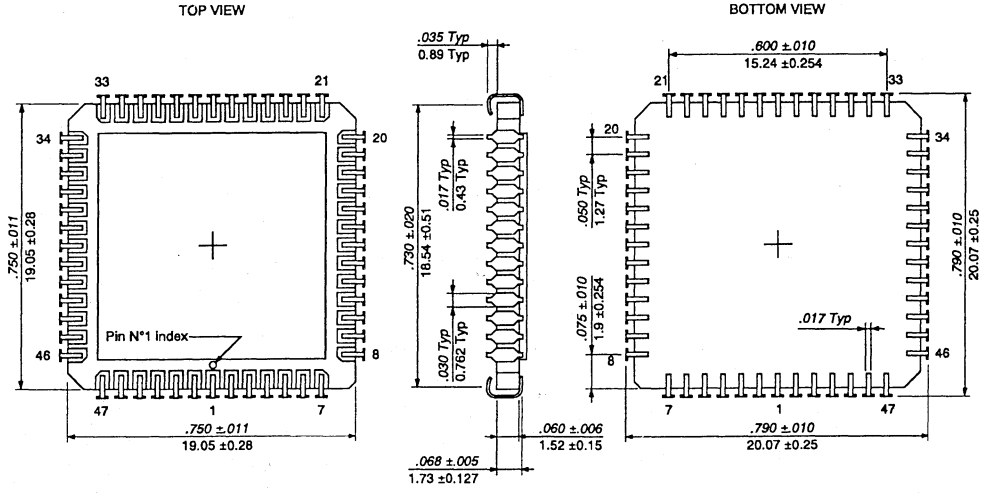
9.1 · 48 Pins · Ceramic DIL



9.2 · 52 Pins - Leadless ceramic chip carrier

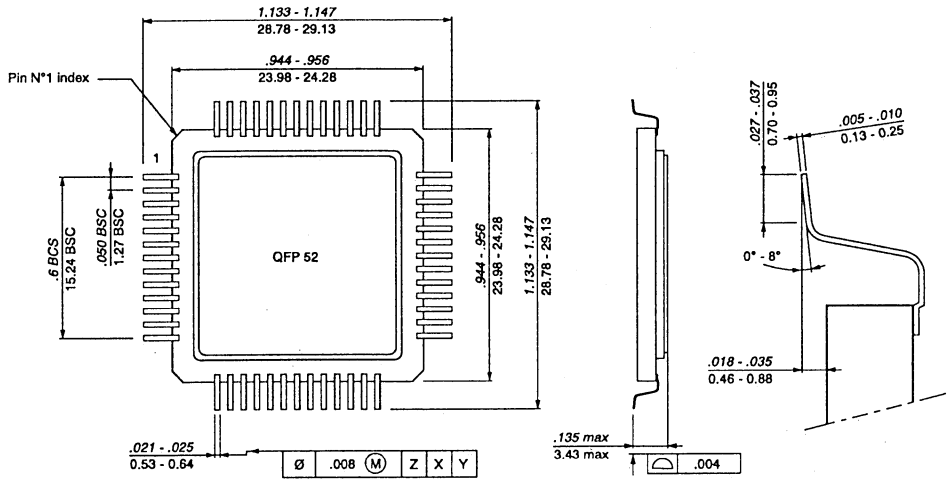


9.3 · 52 Pins - Leaded ceramic chip carrier (on request only)

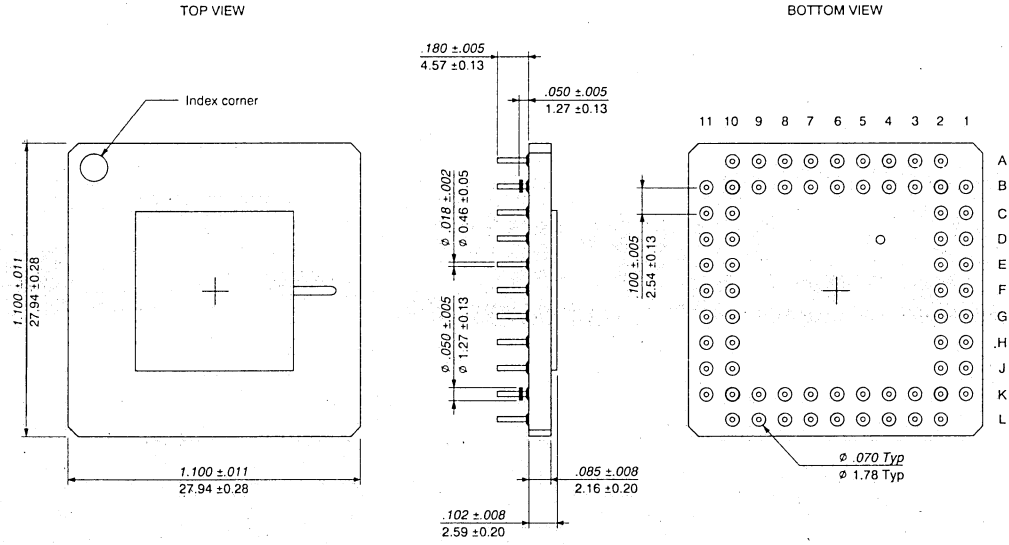


5

9.4 - 52 Pins - Ceramic quad flat pack

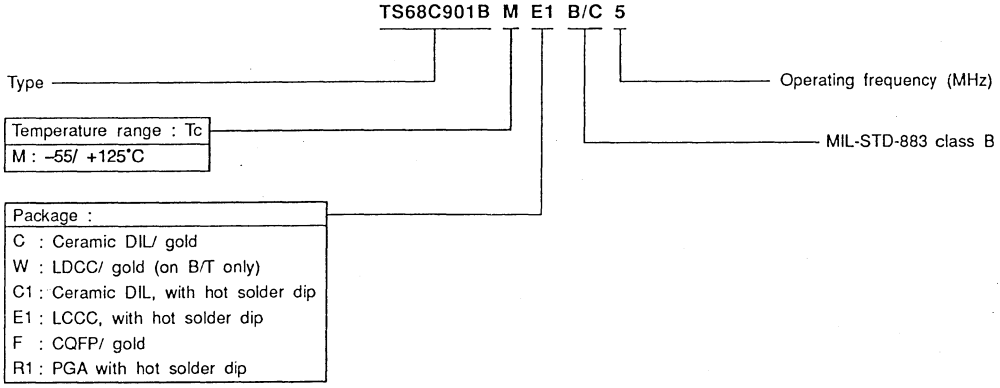


9.5 - 68 Pins - Pin Grid Array



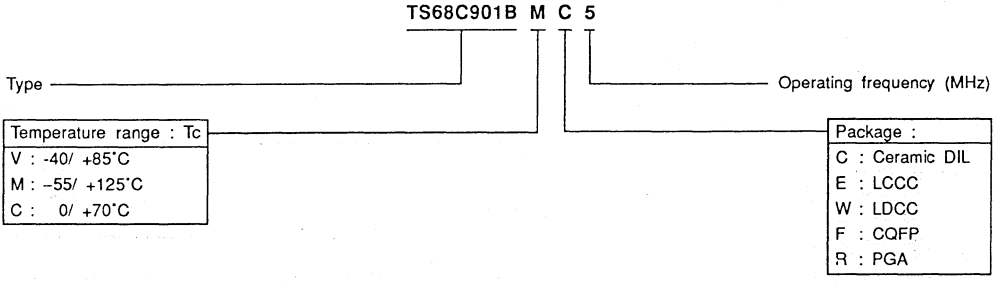
10 · ORDERING INFORMATION

10.1 · MIL-STD-883 C



5

10.2 · Standard product



10.3 · Detailed TS 68C901B part list

10.3.1 · Hi-REL product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_{case} (°C)	Frequency (MHz)	Drawing number
TS68C901BMCB/C4	MIL-STD-883	DIL 48	−55 / +125	4	TCS data sheet
TS68C901BMCB/C5	MIL-STD-883	DIL 48	−55 / +125	5	TCS data sheet
TS68C901BMCB/C8	MIL-STD-883	DIL 48	−55 / +125	8	TCS data sheet
TS68C901BME1B/C4	MIL-STD-883	LCCC 52	−55 / +125	4	TCS data sheet
TS68C901BME1B/C5	MIL-STD-883	LCCC 52	−55 / +125	5	TCS data sheet
TS68C901BME1B/C8	MIL-STD-883	LCCC 52	−55 / +125	8	TCS data sheet
TS68C901BMWB/T4	MIL-STD-883	LDCC 52	−55 / +125	4	on request only
TS68C901BMWB/T5	MIL-STD-883	LDCC 52	−55 / +125	5	on request only
TS68C901BMWB/T8	MIL-STD-883	LDCC 52	−55 / +125	8	on request only
TS68C901BMFB/C8	MIL-STD-883	CQFP 52	−55 / +125	8	TCS data sheet
TS68C901BDESC01XA	DESC	DIL 48	−55 / +125	4	5962-9086401XA
TS68C901BDESC02XA	DESC	DIL 48	−55 / +125	5	5962-9086402XA
TS68C901BDESC03XA	DESC	DIL 48	−55 / +125	8	5962-9086403XA
TS68C901BDESC01YA	DESC	LCCC 52 + hot solder dip	−55 / +125	4	5962-9086401YA
TS68C901BDESC02YA	DESC	LCCC 52 + hot solder dip	−55 / +125	5	5962-9086402YA
TS68C901BDESC03YA	DESC	LCCC 52 + hot solder dip	−55 / +125	8	5962-9086403YA
TS68C901BMFB/C4	MIL-STD-883	CQFP 52	−55 / +125	4	TCS data sheet
TS68C901BMFB/C5	MIL-STD-883	CQFP 52	−55 / +125	5	TCS data sheet
TS68C901BMFB/C8	MIL-STD-883	CQFP 52	−55 / +125	8	TCS data sheet

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

10.3.2 - Standard product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_{case} (°C)	Frequency (MHz)	Drawing number
TS68C901BVC4	TCS standard	DIL 48	−40 / +85	4	TCS data sheet
TS68C901BVC5	TCS standard	DIL 48	−40 / +85	5	TCS data sheet
TS68C901BVC8	TCS standard	DIL 48	−40 / +85	8	TCS data sheet
TS68C901BMC4	TCS standard	DIL 48	−55 / +125	4	TCS data sheet
TS68C901BMC5	TCS standard	DIL 48	−55 / +125	5	TCS data sheet
TS68C901BMC8	TCS standard	DIL 48	−55 / +125	8	TCS data sheet
TS68C901BME4	TCS standard	LCCC 52	−55 / +125	4	TCS data sheet
TS68C901BME5	TCS standard	LCCC 52	−55 / +125	5	TCS data sheet
TS68C901BME8	TCS standard	LCCC 52	−55 / +125	8	TCS data sheet
TS68C901BMW4	TCS standard	LDCC 52	−55 / +125	4	on request only
TS68C901BMW5	TCS standard	LDCC 52	−55 / +125	5	on request only
TS68C901BMW8	TCS standard	LDCC 52	−55 / +125	8	on request only
TS68C901BMF4	TCS standard	CQFP 52	−55 / +125	4	TCS data sheet
TS68C901BMF5	TCS standard	CQFP 52	−55 / +125	5	TCS data sheet
TS68C901BMF8	TCS standard	CQFP 52	−55 / +125	8	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

5

APPLICATION NOTE (July 1992)

TIMERS USE FOR TS 68C901B IN POLLING MODE

Due to the use of high speed processors, the user can have some trouble with the timers of the TS 68C901B (CMFP).

The problem occurs when polling is made on the timer data registers (TxDR) for the 4 timers of the CMFP if different clock sources are used for CLK input and timer clock (XTAL1/XTAL2).

Due to the fact that there is no phase relation between the 2 clock sources, the content of the TADR, TBDR, TCDR and TDDR (TxDR) can be modified when $\overline{\text{DTACK}}$ signal is asserted at low state.

This problem occurs because high speed CPU can perform lots of accesses to the CMFP during a short period of time. The TxDR are updated after a rising edge of DS signal plus a particular timer clock phase which is activated by a particular rising edge of XTAL1 signal. This TxDR update can occurs during a CPU access if there is no phase relation between XTAL1 and CLK.

Rem : If timers are only used to generate baud rate or are used as delay interrupt sources, there is no problem with the CMFP.

That means that if the TxDR are not read back when timer is running, the CMFP can be used as usualy.

Work around

To avoid this problem, 2 hardware solutions can be implemented. These solutions can be used only if XTAL1 signal is a logical signal (no crystal used for XTAL1/XTAL2). This means that it is possible to externally synchronize the 2 CMFP clocks (CLK and XTAL1).

This solution is usefull for XTAL1 at «high frequency» (min spec. is 1 MHz). The goal is to delay the $\overline{DTACK}$ signal as far as possible from a rising edge of the XTAL1 signal.

In that case, the worst access time is about one XTAL1 period (1/2 XTAL1 period plus CMFP access time) so it is about 1 μs worst case. This value must be considerated if a bus error detection is used in the application.

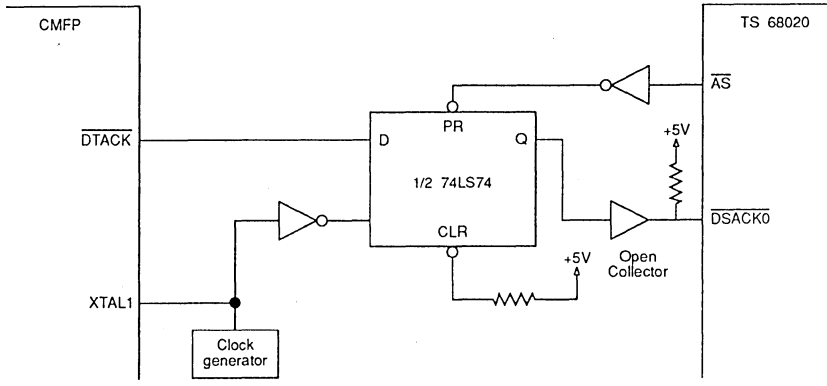


Figure 1 : Work around for «high frequency» clock.

This second solution must be considerate when the TAI or TBI inputs are used as «low frequency» timer clock. In that case, the event count input (TAI or TBI) can not toggles when the CMFP is selected ($\overline{CS}$ = 0) so no TxDR modification can occurs and the data bus is stable during the CMFP access from the CPU.

Do not forget that any toggle of TAI can not be detected during an CMFP access. The CMFP keeps a normal behaviour only if the time during $\overline{CS}$ = 0 is less than a TAI (TBI) period plus min. timer pulse width.

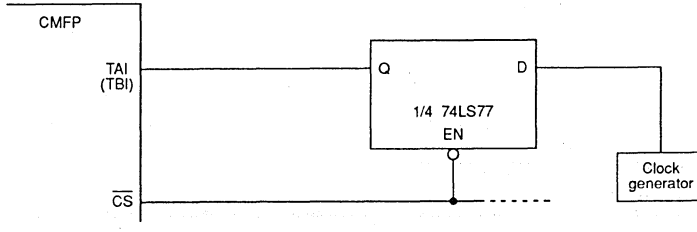


Figure 2 : Work around for «low frequency» clock.

32-BIT FAMILY

5

HCMOS 32-BIT VIRTUAL MEMORY MICROPROCESSOR

DESCRIPTION

The TS 68020 is the first full 32-bit implementation of the TS 68000 family of microprocessors. Using HCMOS technology, the TS 68020 is implemented with 32-bit registers and data paths, 32-bit addresses, a rich instruction set, and versatile addressing modes.

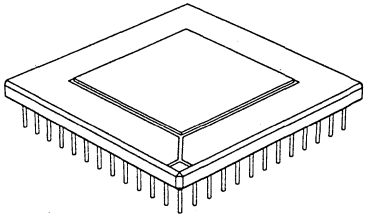
MAIN FEATURES

- Object code compatible with earlier TS 68000 microprocessors.
- Addressing mode extensions for enhanced support of high level languages.
- New bit field data type accelerates bit-oriented application, i.e. video graphics.
- Fast on-chip instruction cache speeds instructions and improves bus bandwidth.
- Coprocessor interface to companion 32-bit peripherals : TS 68881 and TS 68882 floating point coprocessors.
- Pipelined architecture with high degree of internal parallelism allowing multiple instructions to be executed concurrently.
- High performance asynchronous bus in non-multiplexed and full 32 bits.
- Dynamic bus sizing efficiently supports 8-/ 16-/ 32-bit memories and peripherals.
- Full support of virtual memory and virtual machine.
- Sixteen 32-bit general-purpose data and address registers.
- Two 32-bit supervisor stack pointers and 5 special purpose control registers.
- 18 addressing modes and 7 data types.
- 4-Gigabyte direct addressing range.
- Processor speed : 16.67 MHz - 20 MHz - 25 MHz.
- Power supply : 5.0 V_{DC} ± 5 %.

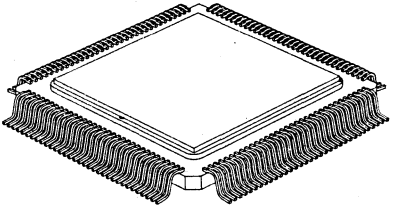
SCREENING / QUALITY

This product is manufactured in full compliance with either :

- CECC 90000 (class B, assessment level Y) / CECC 90110-004
- MIL-STD-883 (class B)
- DESC 5962 - 860320
- or according to TCS standards.



R Suffix
PGA 114
Ceramic Pin Grid Array



F Suffix
CQFP 132
Ceramic Quad Flat Pack

See the ordering information page 31.

Pin connection : see page 4.

SUMMARY

A · GENERAL DESCRIPTION

INTRODUCTION

The TS 68020 is a high-performance 32-bit microprocessor. It is the first microprocessor to have evolved from a 16-bit machine to a full 32-bit machine that provides 32-bit address and data buses as well as 32-bit internal structures. Many techniques were utilized to improve performance and at the same time maintain compatibility with other processors of the TS 68000 Family. Among the improvements are new addressing modes which better support high-level language structures, an expanded instruction set which provides 32-bit operations for the limited cases not supported by the TS 68000 and sereval new instructions which support new data types. For special-purpose applications when a general-purpose processor alone is not adequate, a coprocessor interface is provided.

The TS 68020 is a high-performance microprocessor implemented in HCMOS, low power, small geometry process. This process allows CMOS and HMOS (high density NMOS) gates to be combined on the same device. CMOS structures are used where speed and low power is required, and HMOS structures are used where minimum silicon area is desired. This technology enables the TS 68020 to be very fast while consuming less power (less than 1.5 watts) and still have a reasonably small die size. It utilizes about 190.000 transistors, 103.000 of which are actually implemented. The package is a pin-grid array (PGA) with 114 pins, arranged 13 pins on a side with a depopulated center and 132 pins ceramic quad flat pack.

Figure 1 is a block diagram of the TS 68020. The processor can be divided into two main sections : the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

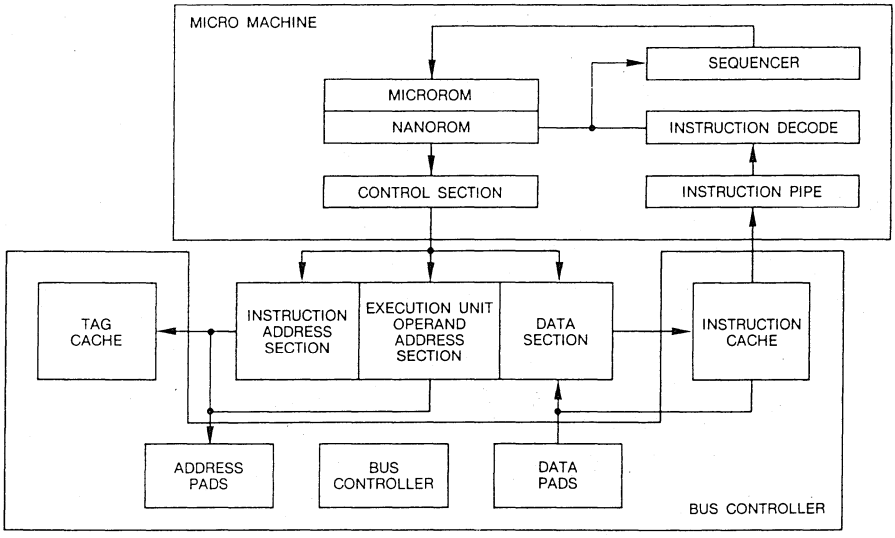


Figure 1 : TS 68020 block diagram.

The bus controller consists of the address and data pads and multiplexers required to support dynamic bus sizing, a macro bus controller which schedules the bus cycles on the basis of priority with two state machines (one to control the bus cycles for operated accesses and the other to control the bus cycles for instruction accesses), and the instruction cache with its associated control.

The micromachine consists of an execution unit, nanorom and microrom storage, an instruction decoder, an instruction pipe, and associated control sections. The execution unit consists of an address section, an operand address section, and a data section. Microcode control is provided by a modified two-level store of microrom and nanorom. Programmed logical arrays (PLAs) are used to provide instruction decode and sequencing information. The instruction pipe and other individual control sections provide the secondary decode of instructions and generated the actual control signals that result in the decoding and interpretation of nanorom and microrom information.

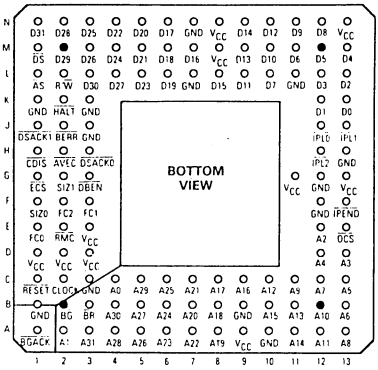


Figure 2.1 : PGA terminal designation.

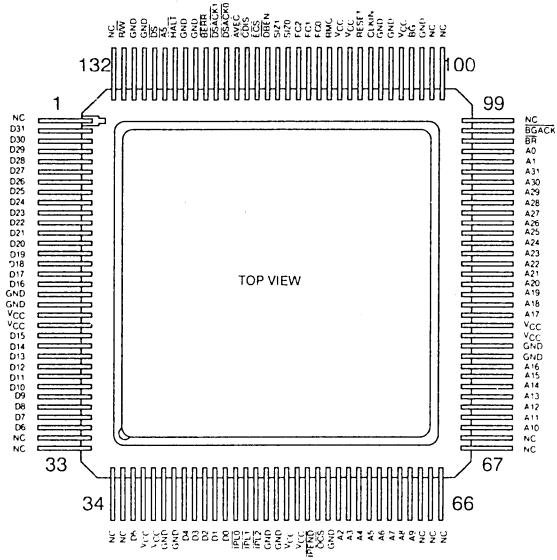


Figure 2.2 : CQFP terminal designation.

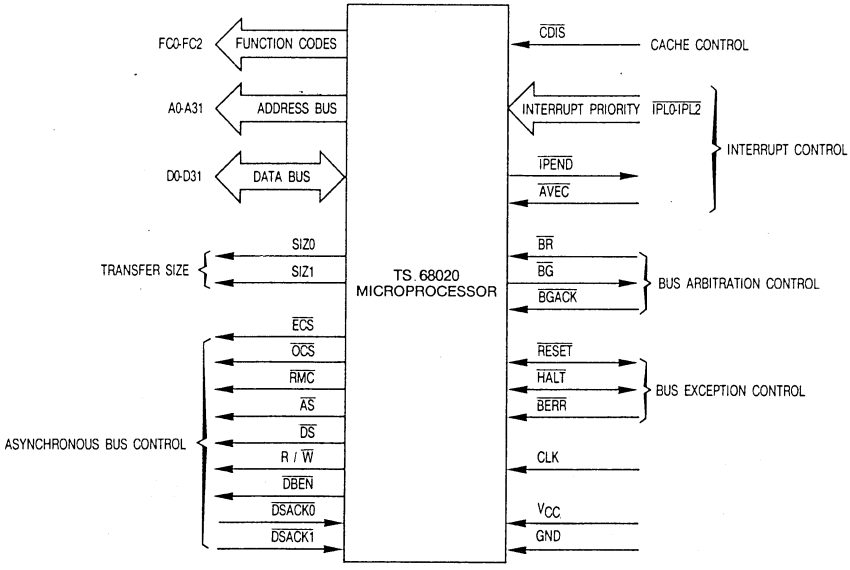


Figure 3 : Functional signal groups.

SIGNAL DESCRIPTION

Figure 3 illustrates the functional signal groups and Table 1 lists the signals and their function.

The V_{CC} and GND pins are separated into four groups to provide individual power supply connections for the address bus buffers, data bus buffers, and all other output buffers and internal logic.

Group	V_{CC}	GND
Address Bus	A9, D3	A10, B9, C3, F12
Data Bus	M8, N8, N13	L7, L11, J7, K3
Logic	D1, D2, E3, G11, G13	G12, H13, J3, K1
Clock	—	B1

Table 1 · Signal index

Signal Name	Mnemonic	Function
Address Bus	A0-A31	32-bit address bus used to address any of 4,294,967,296 bytes.
Data Bus	D0-D31	32-bit data bus used to transfer 8, 16, 24 or 32 bits of data per bus cycle.
Function Codes	FC0-FC2	3-bit function case used to identify the adress space of each bus cycle.
Size	SIZ0 / SIZ1	Indicates the number of bytes remaining to be transferred for this cycle. These signals, together with A0 and A1, define the active sections of the data bus.
Read-Modify-Write Cycle	$\overline{RMC}$	Provides an indicator that the current bus cycle is part of an indivisible read-modify-write operation.
External Cycle Start	$\overline{ECS}$	Provides an indication that a bus cycle is beginning.
Operand Cycle Start	$\overline{OCS}$	Identical operation to that of ECS except that OCS is asserted only during the first bus cycle of an operand transfer.
Address Strobe	$\overline{AS}$	Indicates that a valid address is on the bus.
Data Strobe	$\overline{DS}$	Indicates that valid data is to be placed on the data bus by an external device or has been placed on the data bus by the TS 68020.
Read / Write	R / $\overline{W}$	Defines the bus transfer as an MPU read or write.
Data Buffer Enable	$\overline{DBEN}$	Provides an enable signal for external data buffers.
Data Transfert and Size Acknowledge	$\overline{DSACK0}$ / $\overline{DSACK1}$	Bus response signals that indicate the requested data transfer operation is completed. In addition, these two lines indicate the size of the external bus port on a cycle-by-cycle basis.
Cache Disable	$\overline{CDIS}$	Dynamically disables the on-chip cache to assist emulator support.
Interrupt Priority Level	$\overline{IPL0}$-$\overline{IPL2}$	Provides an encoded interrupt level to the processor.
Autovector	$\overline{AVEC}$	Requests an autovector during an interrupt acknowledge cycle.
Interrupt Pending	$\overline{IPEND}$	Indicates that an interrupt is pending.
Bus Request	$\overline{BR}$	Indicates that an external device requires bus mastership.
Bus Grant	$\overline{BG}$	Indicates that an external device may assume bus mastership.
Bus Grant Acknowledge	$\overline{BGACK}$	Indicates that an external device has assumed bus mastership.
Reset	$\overline{RESET}$	System reset.
Halt	$\overline{HALT}$	Indicates that the processor should suspend bus activity.
Bus Error	$\overline{BERR}$	Indicates an invalid or illegal bus operation is being attempted.
Clock	$\overline{CLK}$	Clock input to the processor.
Power Supply	V_{CC}	+5 volt ±5 % power supply.
Ground	GND	Ground connection.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microprocessor 68020, 16.67 MHz and 20 MHz, in compliance either with MIL-STD-883 class B or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
3) Desc Drawing 5962 - 860320xxx.

2.2 - CECC 90000

1) CECC 90000.
2) Specification CECC 90110-004 for 16 and 20 MHz (TBD for 25 MHz).

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 (when defined) :

- 114-PIN SQ.PGA UP PAE outline,
- 132-PIN Ceramic Quad Flat Pack CQFP,
- OVCC (on request).

The precise case outlines are described on Figures 9.1 and 9.2.

3.3 - Electrical characteristics

*3.3.1 - **Absolute maximum ratings*** (see Table 2)

Table 2

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+7.0	V
V_I	Input voltage		-0.3	+7.0	V
P_{dmax}	Max Power dissipation	T_{case} = -55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating temperature	M suffix	-55	+125	°C
		V suffix	-40	+85	°C
T_{stg}	Storage temperature		-55	+150	°C
T_j	Junction temperature			+160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 - Recommended condition of use

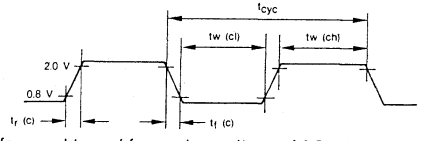
Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Table 3

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_{IL}	Low level input voltage		−0.3	0.5	V
V_{IH}	High level input voltage		2.4	5.25	V
T_{case}	Operating temperature		−55	+125	°C
R_L	Value of output load resistance		see Note		Ω
C_L	Output loading capacitance			see Note	pF
$t_r(c)$	Clock rise time (see Figure 4)			5	ns
$t_f(c)$	Clock fall time (see Figure 4) resistance			5	ns
f_c	Clock frequency (see Figure 4)	68020-16	8	16.67	MHz
		68020-20	12.5	20	
		68020-25	12.5	25	
t_{cyc}	Cycle time (see Figure 4)	68020-16	60	125	ns
		68020-20	50	80	
		68020-25	40	80	
$t_{W(CL)}$	Clock pulse width low (see Figure 4)	68020-16	24	95	ns
		68020-20	20	54	
		68020-25	19	61	
$t_{W(CH)}$	Clock pulse width high (see Figure 4)	68020-16	24	95	ns
		68020-20	20	50	
		68020-25	19	61	

Note : Load network number 1 to 4 as specified (Table 7) gives the maximum loading of the relevant output.

This device contains protective circuitry against damage due to high static voltages or electrical fields ; however, it is advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 : Clock input timing diagram.

3.4 - Thermal characteristics (at 25°C)

Table 4

Package	Symbol	Parameter	Value	Unit
PGA 114	θ JA	Thermal resistance - Ceramic Junction to Ambient	26	°C/W
	θ JC	Thermal resistance - Ceramic Junction to Case	5	°C/W
CQFP 132	θ JA	Thermal resistance - Ceramic Junction to Ambient	34	°C/W
	θ JC	Thermal resistance - Ceramic Junction to Case	2	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 · Thomson logo

3.6.2 · Manufacturer's part number

3.6.3 · Class B identification

3.6.4 · Date-code of inspection lot

3.6.5 · ESD identifier if available

3.6.6 · Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 · CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 9011 0-004. Group C inspection is performed on a periodic basis in accordance with CECC 90110-004.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below. For inspection purpose, refer to relevant specification :

- DESC see § 4.1
- CECC see § 4.2

(last issue on request to our marketing services).

Table 5 : Static electrical characteristics for all electrical variants. See § 5.2.
Table 6 : Dynamic electrical characteristics for 68020-16 (16.67 MHz), 68020-20 (20 MHz) and 68020-25 (25 MHz). See § 5.3.

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 7).

For dynamic characteristics (Table 6), test methods refer to IEC 748-2 method number, where existing.

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature.

5.2 · Static characteristics

Table 5

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C or −40 / +85°C (See Figure 3 to Figure 7)

Symbol	Parameter	Condition	Min	Max	Units
I_{CC}	Maximum supply current	V_{CC} = 5.25 V T_{case} −55°C to +25°C		333	mA
I_{CC}	Maximum supply current	V_{CC} = 5.25 V T_{case} = 125°C		207	mA
V_{IH}	High level input voltage	V_O = 0.5 V or 2.4 V V_{CC} = 4.75 V to 5.25 V	2.0	V_{CC}	V
V_{IL}	Low level input voltage	V_O = 0.5 V or 2.4 V V_{CC} = 4.75 V to 5.25 V	−0.3	0.8	V
V_{OH}	High level output voltage All outputs	I_{OH} = 400 µA	2.4		V
V_{OL}	Low level output voltage Outputs A0-A31, FC0-FC2, D0-D31, SIZ0-SIZ1, $\overline{BG}$	I_{OL} = 3.2 mA Load circuit as Figure 7 R = 1.22 kΩ		0.5	V
V_{OL}	Low level output voltage Outputs $\overline{AS}$, $\overline{DS}$, $\overline{RMC}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{IPEND}$	I_{OL} = 5.3 mA Load circuit as Figure 7 R = 740 Ω		0.5	V
V_{OL}	Low level output voltage Outputs $\overline{ECS}$, $\overline{OCS}$	I_{OL} = 2.0 mA Load circuit as Figure 7 R = 2 kΩ		0.5	V
V_{OL}	Low level output voltage Outputs $\overline{HALT}$, $\overline{RESET}$	I_{OL} = 10.7 mA Load circuit as Figure 5 and Figure 6		0.5	V
I_{IN}	Input leakage current (high and low state)	−0.5 V ≤ V_{IN} ≤ V_{CC} (max)		2.5	µA
I_{OHZ}	High level leakage current at three-state outputs Outputs A0-A31, AS, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OH} = 2.4 V		2.5	µA
I_{OLZ}	Low level leakage current at three-state outputs Outputs A0-A31, $\overline{AS}$, $\overline{DBEN}$, $\overline{DS}$, D0-D31, R/$\overline{W}$, FC0-FC2, $\overline{RMC}$, SIZ0-SIZ1	V_{OL} = 0.5 V		2.5	µA
I_{OS}	Output short-circuit current (Any output)	V_{CC} = 5.25 V V_O = 0 V (Pulsed. Duration 1 ms Duty Cycle 10:1)		200	mA

5.3 · Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.75 V to 5.25 V V_{IL} = 0.5 V and V_{IH} = 2.4 V (See also note 12 and 13).

The INTERVAL numbers refer to the timing diagrams. See Figures 4, 8, and 9.

Table 6

Symbol	Parameter	Interval N°	68020-16 Min	68020-16 Max	68020-20 Min	68020-20 Max	68020-25 Min	68020-25 Max	Unit	Notes
t_{CPW}	Clock pulse width	2,3	24	95	20	54	19	61	ns	
t_{CHAV}	Clock high to Address/FC/Size/$\overline{RMC}$ valid	6	0	30	0	25	0	25	ns	
t_{CHEV}	Clock high to $\overline{ECS}$, $\overline{OCS}$ asserted	6A	0	20	0	15	0	12	ns	
t_{CHAZX}	Clock high to Address/Data/FC/$\overline{RMC}$/ Size high impedance	7	0	60	0	50	0	40	ns	11
t_{CHAZn}	Clock high to Address/FC/Size/$\overline{RMC}$ invalid	8	0		0		0		ns	
t_{CLSA}	Clock low to $\overline{AS}$, $\overline{DS}$ asserted	9	3	30	3	25	3	18	ns	
t_{STSA}	$\overline{AS}$ to $\overline{DS}$ assertion (Read) (Skew)	9A	– 15	15	– 10	10	– 10	10	ns	1
t_{ECSA}	$\overline{ECS}$ width asserted	10	20		15		15		ns	
t_{OCSA}	$\overline{OCS}$ width asserted	10A	20		15		15		ns	
t_{EOCSN}	$\overline{ECS}$, $\overline{OCS}$ width asserted	10B	15		10		5		ns	11
t_{AVSA}	Address/FC/Size/$\overline{RMC}$ valid to $\overline{AS}$ asserted (and $\overline{DS}$ asserted, read)	11	15		10		6		ns	6
t_{CLSN}	Clock low to $\overline{AS}$, $\overline{DS}$ negated	12	0	30	0	25	0	15	ns	
t_{CLEN}	Clock low to $\overline{ECS}$/$\overline{OCS}$ negated	12A	0	30	0	25	0	15	ns	
t_{SNAI}	$\overline{AS}$, $\overline{DS}$ negated to Address/FC/Size/ $\overline{RMC}$ invalid	13	15		10		10		ns	
t_{SWA}	$\overline{AS}$ (and $\overline{DS}$, read) width asserted	14	100		85		70		ns	
t_{SWAW}	$\overline{DS}$ width asserted, write	14A	40		38		30		ns	
t_{SN}	$\overline{AS}$, $\overline{DS}$ width negated	15	40		38		30		ns	11
t_{SNSA}	$\overline{DS}$ negated to $\overline{AS}$ asserted	15A	35		30		25		ns	8
t_{CSZ}	Clock high to $\overline{AS}$/$\overline{DS}$/R/$\overline{W}$/$\overline{DBEN}$ high impedance	16		60		50		40	ns	11
t_{SNRN}	$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ high	17	15		10		10		ns	6
t_{CHRH}	Clock high to R/$\overline{W}$ high	18	0	30	0	25	0	20	ns	
t_{CHRL}	Clock high to R/$\overline{W}$ low	20	0	30	0	25	0	20	ns	
t_{RAAA}	R/$\overline{W}$ high to $\overline{AS}$ asserted	21	15		10		5		ns	6
t_{RASA}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write)	22	75		60		50		ns	6
t_{CHDO}	Clock high to data out valid	23		30		25		25	ns	
t_{SNDI}	AS, DS negated to data out invalid	25	15		10		5		ns	6
t_{DNDBN}	$\overline{DS}$ negated to $\overline{DBEN}$ negated (write)	25A	15		10		5		ns	9
t_{DVSA}	Data out valid to $\overline{DS}$ asserted (write)	26	15		10		5		ns	6
t_{DICL}	Data in valid to clock low (data setup)	27	5		5		5		ns	
t_{BELCL}	Late $\overline{BERR}$/$\overline{HALT}$ asserted to clock low setup time	27A	20		15		10		ns	
t_{SNDN}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{DSACK}$x/$\overline{BERR}$/ $\overline{HALT}$/$\overline{AVEC}$ negated	28	0	80	0	65	0	50	ns	

Table 6 (continued)

Symbol	Parameter	Interval N°	68020-16 Min	68020-16 Max	68020-20 Min	68020-20 Max	68020-25 Min	68020-25 Max	Unit	Notes
t_{SNDI}	$\overline{DS}$ negated to data in invalid (data in hold time)	29	0		0		0		ns	6
t_{SNDIZ}	$\overline{DS}$ negated to data in high impedance	29A		60		50		40	ns	
t_{DADI}	$\overline{DSACKx}$ asserted to data in valid	31		50		43		32	ns	2, 11
t_{DADV}	$\overline{DSACKx}$ asserted to $\overline{DSACKx}$ valid ($\overline{DSACK}$ asserted skew)	31A		15		10		10	ns	3, 11
t_{HRrf}	$\overline{RESET}$ input transition time	32		1.5		1.5		1.5	Clks	
t_{CLBA}	Clock low to $\overline{BG}$ asserted	33	0	30	0	25	0	20	ns	
t_{CLBN}	Clock low to $\overline{BG}$ negated	34	0	30	0	25	0	20	ns	
t_{BRAGA}	$\overline{BR}$ asserted to $\overline{BG}$ asserted (RMC not asserted)	35	1.5	3.5	1.5	3.5	1.5	3.5	Clks	11
t_{GAGN}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated	37	1.5	3.5	1.5	3.5	1.5	3.5	Clks	11
t_{GABRN}	$\overline{BGACK}$ asserted to $\overline{BR}$ negated	37A	0	1.5	0	1.5	0	1.5	Clks	11
t_{GN}	$\overline{BG}$ width negated	39	90		75		60		ns	11
t_{GA}	$\overline{BG}$ width asserted	39A	90		75		60		ns	
t_{CHDAR}	Clock high to $\overline{DBEN}$ asserted (read)	40	0	30	0	25	0	20	ns	
t_{CLDNR}	Clock low to $\overline{DBEN}$ negated (read)	41	0	30	0	25	0	20	ns	
t_{CLDAW}	Clock low to $\overline{DBEN}$ asserted (write)	42	0	30	0	25	0	20	ns	
t_{CHDNW}	Clock high to $\overline{DBEN}$ negated (write)	43	0	30	0	25	0	20	ns	
t_{RADA}	R/W low to $\overline{DBEN}$ asserted (write)	44	15		10		10		ns	6
t_{DA}	$\overline{DBEN}$ width asserted Read Write	45	60 120		50 100		40 80		ns ns	5 5
t_{RWA}	R/$\overline{W}$ width asserted (write or read)	46	150		125		100		ns	
t_{AIST}	Asynchronous input setup time	47A	5		5		5		ns	11
t_{AIHT}	Asynchronous input hold time	47B	15		15		10		ns	11
t_{DABA}	$\overline{DSACKx}$ asserted to BERR/HALT asserted	48		30		20		18	ns	4, 11
t_{DOCH}	Data out hold from clock high	53	0		0		0		ns	
t_{BNHN}	$\overline{BERR}$ negated to $\overline{HALT}$ negated (rerun)		0		0		0		ns	
f	Frequency of operation		8.0	16.67	12.5	20.0	12.5	25	MHz	
t_{RADC}	R/W asserted to data bus impedance change	55	30		25		20		ns	11
t_{HRPW}	$\overline{RESET}$ pulse width (reset instruction)	56	512		512		512		Clks	11
t_{GANBD}	$\overline{BGACK}$ negated to bus driven	58	1		1		1		Clks	10, 11
t_{GNBD}	$\overline{BG}$ negated to bus driven	59	1		1		1		Clks	10, 11

5

NOTES (= = INTERVAL Number)

1 - This number can be reduced to 5 nanoseconds if the strobes have equal loads.

2 - If the asynchronous setup time (= 47) requirements are satisfied, the $\overline{DSACKx}$ low to data setup time (= 31) and $\overline{DSACKx}$ low the $\overline{BERR}$ low setup time (= 48) can be ignored. The data must only satisfy the data in to clock low setup time (= 27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock setup time (= 27) for the following clock cycle.

3 - This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted pattern = 47 must be met by $\overline{DSACK0}$ and $\overline{DSACK1}$.

4 - In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (= 47).

5 - $\overline{DBEN}$ may stay asserted on consecutive write cycles.

6 - Actual value depends on the clock input waveform.

7 - This pattern indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by a cache miss or operand cycle.

8 - This specification guarantees operations with the 68881 coprocessor, and defines a minimum time for DS negated to AS asserted (= 13A). Without this parameter, incorrect interpretation of = 9A and = 15 would indicate that the 68020 does not meet 68881 requirements.

9 - This pattern allows the systems designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$.

10 - Guarantees that an alternate bus master has stopped driving the bus when the 68020 regains control of the bus after an arbitration sequence.

11 - Cannot be tested. Provided for system design purposes only.

12 - T_{case} = −55°C and +130°C in a Power off condition under Thermal soak for 4 minutes or until thermal equilibrium. Electrical parameters are tested «instant on» 100 m sec after power is applied.

13 - All outputs unload except for load capacitance. Clock = fmax,
LOW : $\overline{HALT}$, $\overline{RESET}$
HIGH : $\overline{DSACK0}$, $\overline{DSACK1}$, $\overline{CDIS}$, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{DBEN}$, $\overline{AVEC}$, $\overline{BERR}$.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Table 6, refering to the loading network number as shown in Figures 5, 6 and 7 below.

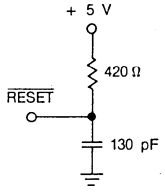


Figure 5 : RESET test load.

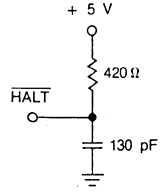


Figure 6 : HALT test load.

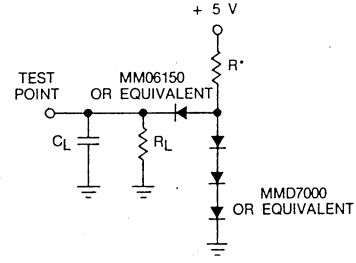


Figure 7 : Test load.

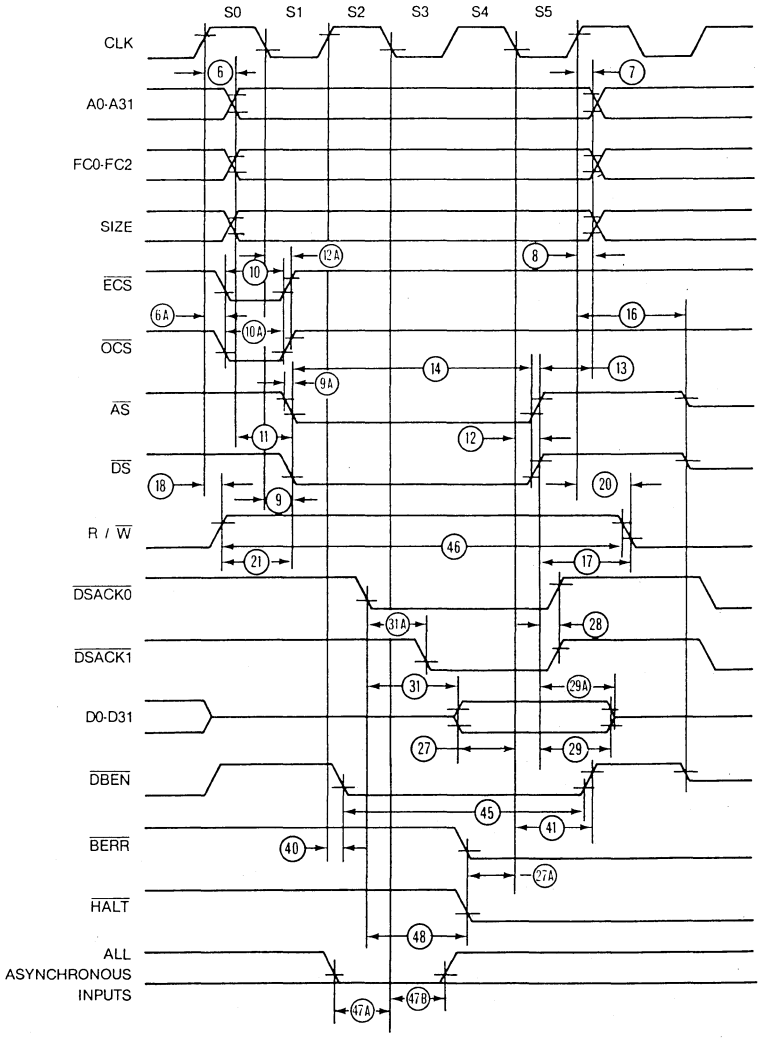
Table 7

Load NBR	Figure	R	R_L	C_L	Output Application
1	7	2 k	6.0 k	50 pF	$\overline{OCS}$, $\overline{ECS}$
2	7	1.22 k	6.0 k	130 pF	A0-A31, D0-D31, $\overline{BG}$, FC0-FC2, SIZ0-SIZ1
3	7	0.74 k	6.0 k	130 pF	$\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{RMC}$, $\overline{DBEN}$, $\overline{IPEND}$

Note : Equivalent loading may be simulated by the tester.

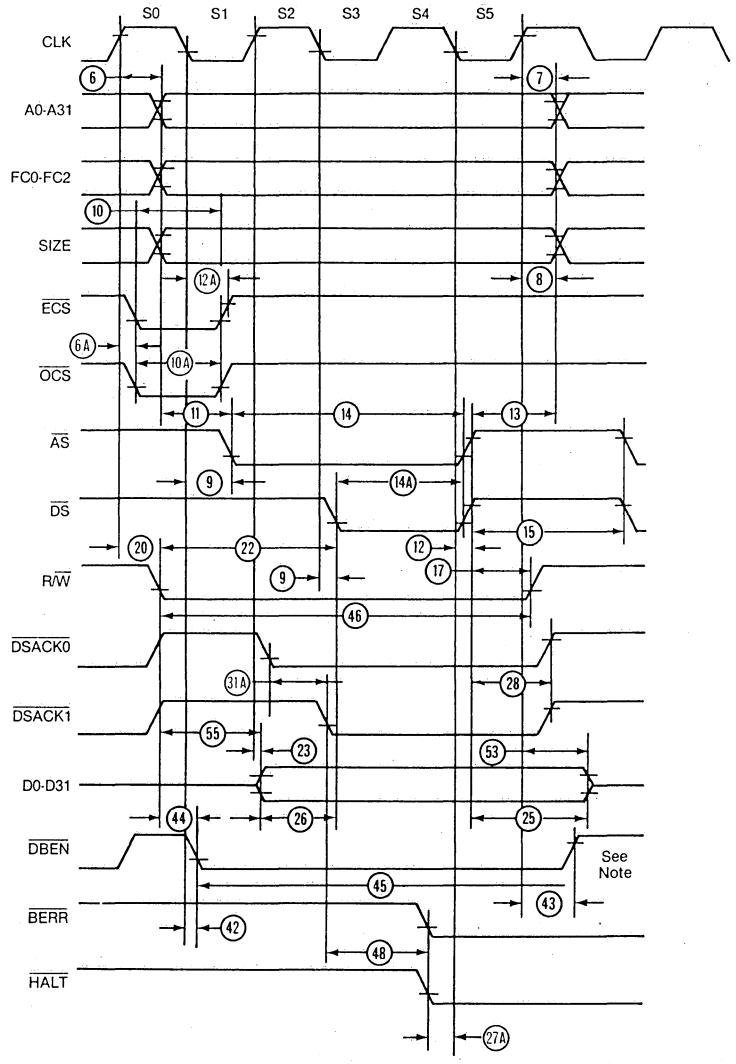
5.4.2 · Time definitions

The times specified in Table 6 as dynamic characteristics are defined in Figure 8 below, by a reference number given the column «interval N°» of the tables together with the relevant figure number.



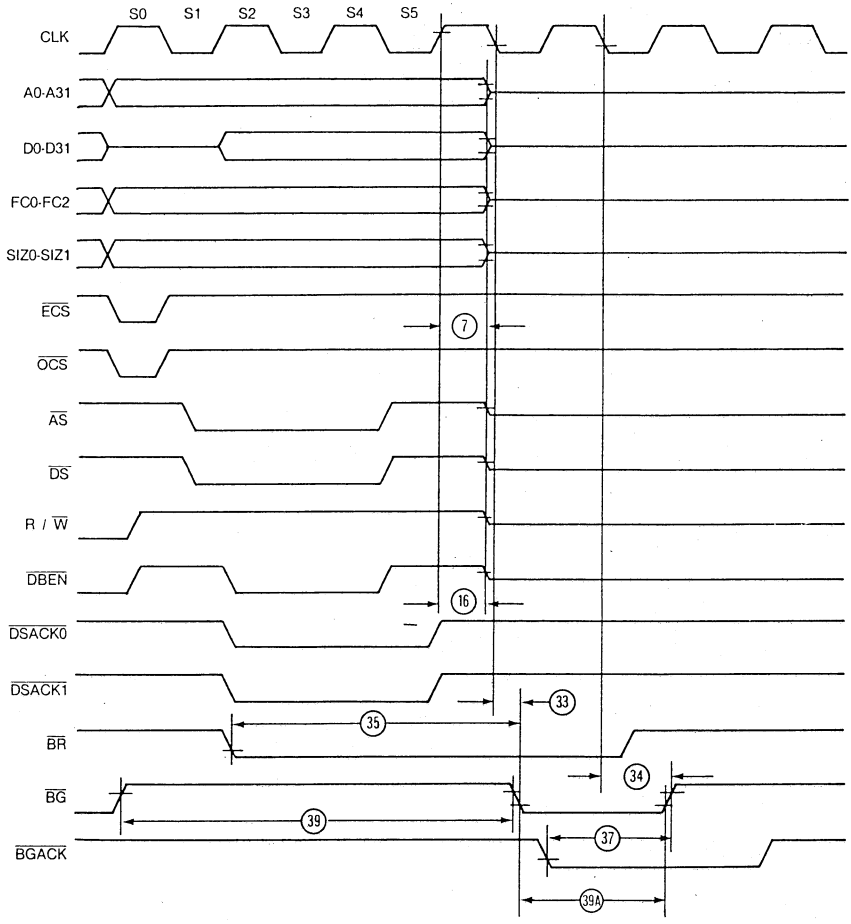
Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8 : Read cycle timing diagram.



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8 : Read cycle timing diagram (continued).



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8 : Read cycle timing diagram (continued).

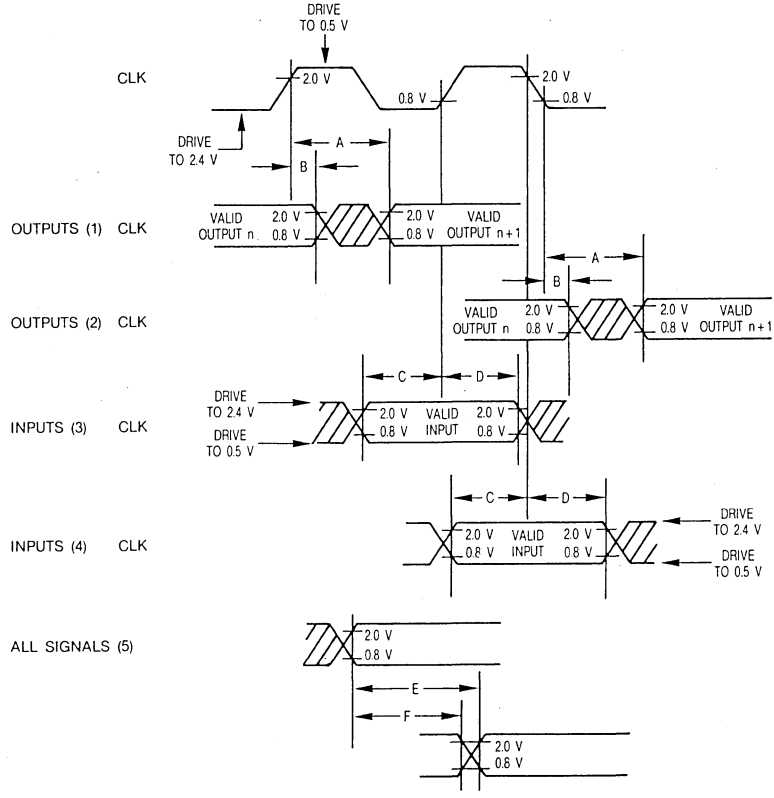
5.4.3 · Input and output signals for dynamic measurements

AC electrical specifications definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the TS 68020 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 9. In order to test the parameters guaranteed by TCS, inputs must be driven to the voltage levels specified in Figure 9. Outputs of the TS 68020 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the TS 68020 are specified with minimum and, as appropriate, maximum setup and hold times, and are measurement as shown. Finally, the measurements for signal-to-signal specifications are also shown.

Note that the testing levels used to verify conformance of the TS 68020 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



Legend : A - Maximum output delay specification.
B - Minimum output hold time.
C - Minimum input setup time specification.
D - Minimum input hold time specification.
E - Signal valid to signal valid specification (maximum or minimum.
F - Signal valid to signal invalid specification (maximum or minimum).

Notes : 1 - This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2 - This output timing is applicable to all parameters specified relative to the failing edge of the clock.
3 - This input timing is applicable to all parameters specified relative to the failing edge of the clock.
4 - This input timing is applicable to all parameters specified relative to the failing edge of the clock.
5 - This timing is applicable to all parameters specified relative to the assertion / negation of another signal.

Figure 9 : Drive levels and test points for AC specifications.

5.5 - Additional information

Additional information shall not be for any inspection purposes.

5.5.1 - Power considerations (see § 3.4)

5.5.2 - Capacitance (Not for inspection purposes)

Symbol	Parameter	Test conditions	Typ	Unit
C_{in}	Input capacitance	V_{in} = 0 V T_{amb} = 25°C f = 1 MHz	20	pF

Capacitance derating curves

Figures 10 to 15 inclusive show the typical derating conditions which apply. The capacitance includes any stray capacitance. The graphs may not be linear outside the range shown.

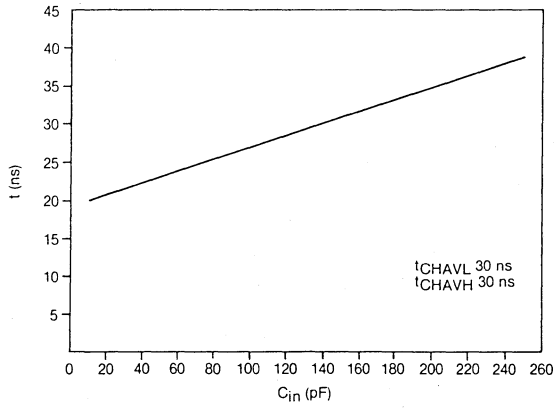


Figure 10 : Address capacitance derating curve.

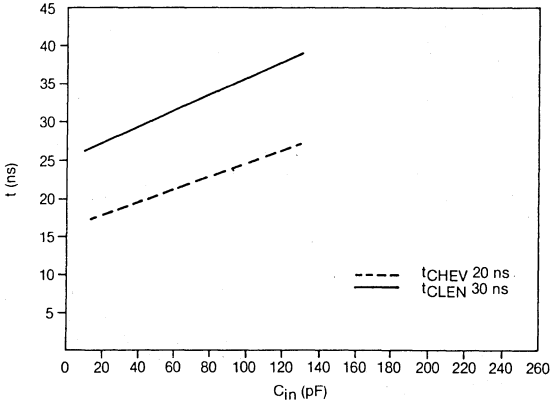


Figure 11 : ECS and OCS capacitance derating curve.

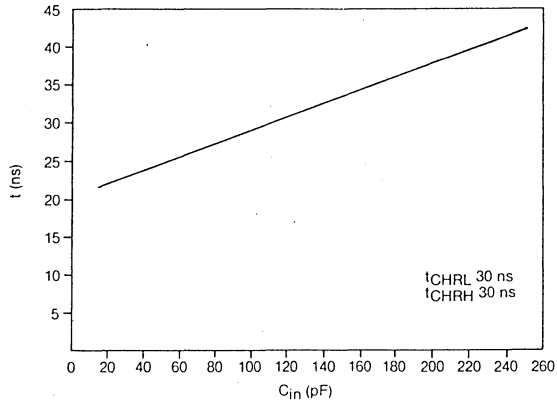


Figure 12 : R/W, FC, SIZ0-SIZ1, and RMC capacitance derating curve.

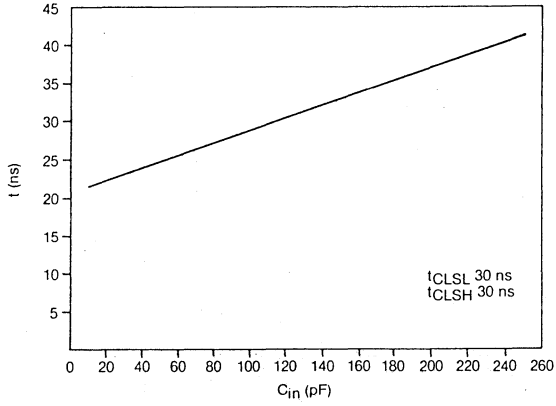


Figure 13 : DS, AS, IPEND, and BG capacitance derating curve.

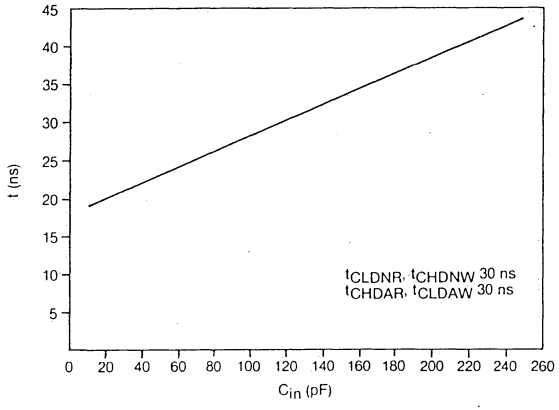


Figure 14 : DBEN capacitance derating curve.

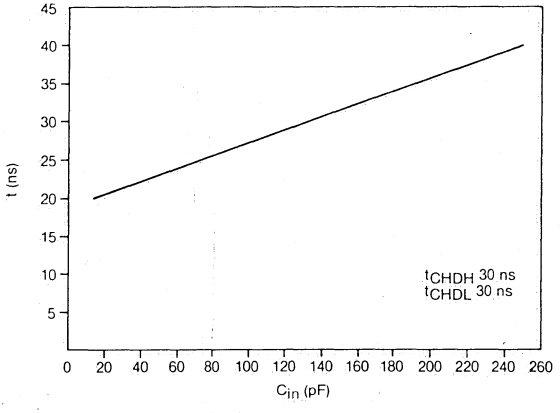


Figure 15 : Data capacitance derating curve.

6 - FUNCTIONNAL DESCRIPTION

Description of registers

As shown in the programming models (Figures 16 and 17) the TS 68020 has sixteen 32-bit general-purpose registers, a 32-bit program counter, two 32-bit supervisor stack pointers, a 16-bit status register, a 32-bit vector base register, two 3-bit alternate function code registers, and two 32-bit cache handling (address and control) registers. Registers D0-D7 are used as data registers for bit and bit field (1 to 32 bit), byte (8 bit), long word (32 bit), and quad word (64 bit) operations. Registers A0-A6 and the user, interrupt, and master stack pointers are address registers that may be used as software stack pointers or base address registers. In addition, the address registers may be used for word and long word operations. All of the 16 (D0-D7, A0-A7) registers may be used as index registers.

The status register (Figure 18) contains the interrupt priority mask (three bits) as well as the condition codes : extend (X), negated (N), zero (Z), overflow (V), and carry (C). Additional control bits indicate that the processor is in the trace mode (T1 or T0), supervisor / user state (S), and master / interrupt state (M).

All microprocessors of the TS 68000 Family support instruction tracing (via the T0 status bit in the TS 68020) where each instruction executed is followed by a trap to a user-defined trace routine. The TS 68020 adds the capability to trace only the change of flow instructions (branch, jump, subroutine call and return, etc.) using the T1 status bit. These features are important for software program development and debug.

The vector base register is used to determine the runtime location of the exception vector table in memory, hence it supports multiple vector tables so each process or task can propertly manage exceptions independent of each other.

The TS 68000 Family processors distinguish address spaces as supervisor / user and program / data. These four combinations are specified by the function code pins (FC0 / FC1 / FC2) during bus cycles, indicating the particular address space. Using the function codes, the memory sub-system can distinguish between authorized access (supervisor mode is privileged access) and unauthorized access (user mode may not have access to supervisor program or data areas). To support the full privileges of the supervisor, the alternate function code registers allow the supervisor to specify an access to user program or data areas by preloading the SFC / DFC registers appropriately.

The cache registers (control — CACR, address — CAAR) allow software manipulation of the on-chip instruction cache. Control and status accesses to the instruction cache are provided by the cache control register (CACR), while the cache address register (CAAR) holds the address for those cache control functions that require an address.

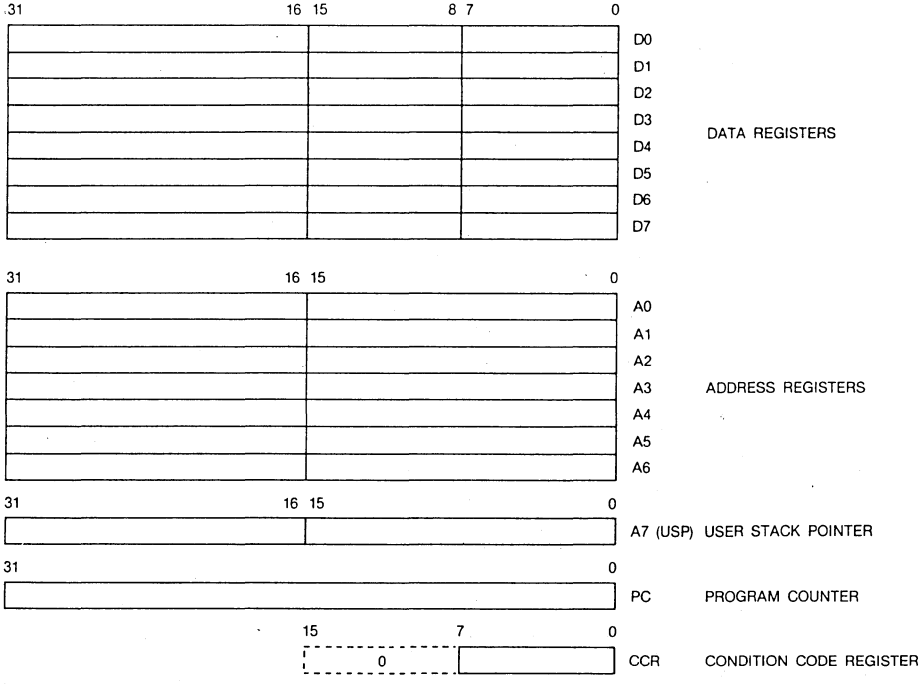


Figure 16 : User programming model.

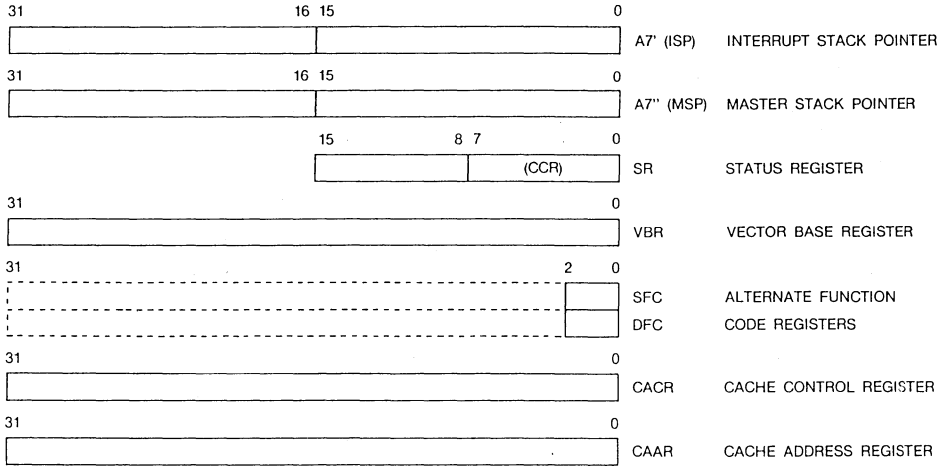


Figure 17 : Supervisor programming model supplement.

5

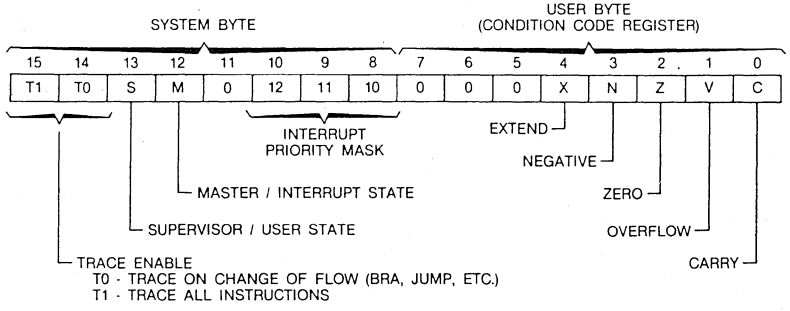


Figure 18 : Status register.

Data types and addressing modes

Seven basic types are supported. These data types are :

- Bits,
- Bits Flieds (String of consecutive bits, 1-32 bits long),
- BCD Digits (Packed : 2 digits/byte, Unpacked : 1 digit/byte),
- Byte Integers (8 bits),
- Word Integers (16 bits),
- Long Word Integers (32 bits),
- Quad Word Integers (64 bits).

In additions, operations on other data types, such as memory addresses, status word data, etc..., are provided in the instruction set. The coprocessor mechanism allows direct support of floating-point data types with the TS 68881 and TS 68882 floating-point coprocessors, as well as specialized user-defined data types and functions.

The 18 addressing modes, shown in Table 8, include nine basic types :

- Register Direct,
- Register Indirect,
- Register Indirect with Index,
- Memory Indirect,
- Program Counter Indirect with Displacement,
- Program Counter Indirect with Index,
- Program Counter Memory Indirect,
- Absolute,
- Immediate.

The register indirect addressing modes support postincrement, predecrement, offset, and indexing. Programmers find these capabilities particularly useful for handling advanced data structures common to sophisticated applications and high level languages. The program counter relative mode also has index and offset capabilities ; programmers find that this addressing mode is required to support position-independent software. In addition to these addressing modes, the TS 68020 provides data operand sizing and scaling ; these features provide performance enhancements to the programmer.

Table 8 - TS 68020 addressing modes

Addressing Modes	Syntax
Register Direct	
Data Register Direct	Dn
Address Register Direct	An
Register Indirect	
Address Register Indirect	(An)
Address Register Indirect with Post Increment	(An) +
Address Register Indirect with Predecrement	− (An)
Address Register Indirect with Displacement	(d_{16} An)
Register Indirect with Index	
Address Register Indirect with Index (8-Bit Displacement)	(d_8, An, Xn)
Address Register Indirect with Index (Base Displacement)	(bd, An, Xn)
Memory Indirect	
Memory Indirect Post-Indexed	([bd, An], Xn, od)
Memory Indirect Pre-Indexed	([bd, An, Xn], od)
Program Counter Indirect with Displacement	(d_{16}, PC)
Program Counter Indirect with Index	
PC Indirect with Index (8-Bit Displacement)	d_8, PC, Xn)
PC Indirect with Index (Base Displacement)	(bd, PC, Xn)
Program Counter Memory Indirect	
PC Memory Indirect Post-Indexed	([bd, PC], Xn, od)
PC Memory Indirect Pre-Indexed	([bd, PC, Xn]), od)
Absolute	
Absolute Short	xxx.W
Absolute Long	xxx.L
Immediate	= (data)

Notes :

Dn = Data Register, D0-D7.

An = Address Register, A0-A7.

d_8, d_{16} = A twos-complement, or sign—extended displacement ; added as part of the effective calculation ; size is 8 (d_8) or 16 (d_{16}) bits ; when omitted assemblers use a value of zero.

Xn = Address or data register used as an index register ; form is Xn, SIZE*SCALE, where SIZE is .W or .L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register is multiplied by SCALE) ; use of SIZE and / or SCALE is optionnal.

bd = A two-complement base displacement ; when present, size can be 16 or 32 bits.

od = Outer displacement, added as part of effective address calculation after any memory indirection ; use is optional with a size of 16 or 32 bits.

PC = Program Counter.

(data) = Immediate value of 8, 16 or 32-bits.

( ) = Effective Address.

[ ] = Use as indirect address to long word address.

Instruction set overview

The TS 68020 instruction set is shown in Table 9. Special emphasis has been given to the instruction set's support of structured high-level languages and sophisticated operating systems. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 18 addressing modes. Many instruction extensions have been made on the TS 68020 to take advantage of the full 32-bit operation where, on the earlier 68000 Family members, only 8- and 16-bit values were used. The TS 68020 is upward source- and object-level code compatible with the family because it supports all of the instructions that previous family members offer. Additional instructions are now provided by the TS 68020 in support of its advanced features.

Table 9 · Instruction Set

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BFCHG	Test Bit Field and Change
BFCLR	Test Bit Field and Clear
BFEXTS	Signed Bit Field Extract
BFEXTU	Unsigned Bit Field Extract
BFFFO	Bit Field Find First One
BFINS	Bit Field Insert
BFSET	Test Bit Field and Set
BFTST	Test Bit Field
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit
CALLM	Call Module
CAS	Compare and Swap Operands
CAS2	Compare and Swap Dual Operands
CHK	Check Register Against Bound
CHK2	Check Register Against Upper and Lower Bounds
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Tape
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LSL, LSR	Logical Shift Left and Right
MOVE	Move
MOVEA	Move Address
MOVE CCR	Move Condition Code Register
MOVE SR	Move Status Register
MOVE USP	Move User Stack Pointer
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral
MOVEQ	Move Quck
MOVES	Move Alternate Address Sapce
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
NOT	Logical Complement
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PACK	Pack BCD
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return from Exception
RTM	Return from Module
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words
TAS	Test Operand and Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink
UNPK	Unpack BCD

5

Coprocessor Instructions.

Mnemonic	Description
cpBCC	Branch Conditionally
cpDBcc	Test Coprocessor Condition, Decrement and Branch
cpGEN	Coprocessor General Instruction

Mnemonic	Description
cpRESTORE	Restore Internal State of Coprocessor
cpSAVE	Save Internal State of Coprocessor
cpTRAPcc	Set Conditionally
cpTRAPcc	Trap Conditionally

Bit field operations

The TS 68020 supports variable length bit field operations up to 32 bits. A bit field may start in any bit position and span any address boundary for the full length of the bit field, up to the 32 bit maximum. The bit field insert (BFINS) inserts a value into a field. Bit field extract unsigned (BFEXTU) and bit field extract signed (BFEXTS) extract a unsigned or signed value from the field. BFFFO finds the first bit in a bit field that is set. To complement the TS 68000 bit manipulation instruction, there are bit field change, clear, set, and test instructions (BFCHG, BFCLR, BFSET, BFTST). Using the on-chip barrel shifter, the bit and bit field instructions are very fast and particularly useful in applications using packed bits and bit fields, such as graphics and communications.

Binary coded decimal (BCD) support

The TS 68000 Family supports BCD operations including add, subtract, and negation. The TS 68020 adds the PACK and UNPACK operations for BCD conversions to and from binary form as well as other conversions, e.g., ASCII and EBCDIC. The PACK instruction reduces two bytes of data into a single byte while UNPACK reverses the operation.

Bounds checking

Previous 68000 Family members offer variable bounds checking only on the upper limit of the bound. The underlying assumption is that the lower bound is zero. This is expanded on the TS 68020 by providing two new instructions, CHK2 and CMP2. These instructions allow checking and comparing of both the upper and lower bounds. These instructions may be either signed or unsigned. The CMP2 instructions sets the condition codes upon completion while the CHK2 instruction, in addition to setting the condition codes, will take a system trap if either boundary condition is exceeded.

System traps

Three additions have been made to the system trap capabilities of the TS 68020. The current TRAPV (trap on overflow) instruction has been expanded to a TRAPcc format where any condition code is allowed to be the trapping condition. And, the TRAPcc instruction is expanded to optionally provide one or two additionnal words following the trap instruction so user-specified information may be presented to the trap handler. These additional words can be used when needed to provide simple error codes or debug information for interactive runtime debugging or post-mortem program dumps. Compilers may provide direction to run-time execution routines towards handling of specific conditions.

The breakpoint instruction, BKPT, is used to support the program breakpoint function for debug monitors and real-time in-circuit or hardware emulators, and the operation will be dependent on the actual system implementation. Execution of this instruction causes the TS 68020 to run a breakpoint acknowledge bus cycle, with a 3-bit breakpoint identifier placed on address lines A2, A3, and A4. This 3-bit identifier permits up to eight breakpoints to be easily differentiated. The normal response to the TS 68020 is an operation word (typically an instruction, originally replaced by the debugger with the breakpoint instruction) placed on the data lines by external debugger hardware and the breakpoint acknowledge cycle properly terminated. The TS 68020 then executes this operation word in place of the breakpoint instruction. The debugger hardware can count the number of executions of each breakpoint and halt execution after a pre-determined number of cycles.

Multi-processing

To further support multi-processing with the TS 68020, a compare and swap instruction, CAS, has been added. This instruction makes use of the read-modify-write cycle to compare two operands and swap a third operand pending the results of the compare. A varient of this instruction, CAS2, performs similarly comparing dual operand pairs, and updating two operands.

These multi-processing operations are useful when using common memory to share or pass data between multiple processing elements. The read-modify-write cycle is an indivisible operand that allows reading and updating a «lock» operand used to control access to the common memory elements. The CAS2 instruction is more powerful since dual operands allow the «lock» to the checked and two values (i.e., both pointers in a doubly-linked list) to be updated according to the lock's status, all in a single operation.

Module support

The TS 68020 includes support for modules with the call module (CALLM) and return from module (RTM) instructions. The CALLM instruction references a module descriptor. This descriptor contains control information for entry into the associated module. The CALLM instruction creates a module stack frame and stores the module state in that frame. The RTM instruction recovers the previous module state from the stack frame and returns to the calling module.

The module interface also provides a mechanism for finer resolution of access control by external hardware. Although the TS 68020 does not interpret the access control information, it does communicate with external hardware when the access control is to be changed, and relies on the external hardware to verify that the changes are legal.

CALLM and RTM, when used as subroutine calls and returns with proper descriptor formats, cause the TS 68020 to perform the necessary actions to verify legitimate access to modules.

Virtual memory / machine concepts

The full addressing range of the TS 68020 is 4 gigabytes (4, 294, 967, 296). However, most TS 68020 systems implement a smaller physical memory. Nonetheless, by using virtual memory techniques, the system can be made to appear to have a full 4 gigabytes of physical memory available to each user program. These techniques have been used for many years in large mainframe computers and minicomputers. With the TS 68020 (as with the TS 68010 and TS 68012), virtual memory can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available to it when actually only a smaller amount of memory is physically present in the system. In a similar fashion, a system provides user programs access to other devices that are not physically present in the system such as tape drives, disk drives, printers, or terminals. With proper software emulation, a physical system can be made to appear to a user program as any other 68000 computer system and the program may be given full access to all of the resources of that emulated system. Such an emulated system is called a virtual machine.

Virtual memory

The basic mechanism for supporting virtual memory is to provide a limited amount of high-speed physical memory that can be accessed directly by the processor while maintaining an image of a much larger «virtual» memory on secondary storage devices such as large capacity disk drives. When the processor attempts to access a location in the virtual memory map that is not resident in physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from secondary storage and placed in physical memory ; the suspended access is then either restarted or continued.

The TS 68020 uses instruction continuation to support virtual memory. In order for the TS 68020 to use instruction continuation, it stores its internal state on the supervisor stack when a bus cycle is terminated with a bus error signal. It then loads the program counter with the address of the virtual memory bus error handler from the exception vector table (entry number two) and resumes program execution at that new address. When the bus error exception handler routine has completed execution, an RTE instruction is executed which reloads the TS 68020 with the internal state stored on the stack, reruns the faulted bus cycle (when required), and continues the suspended instruction.

Instruction continuation is crucial to the support of virtual I/O devices in memory-mapped input / output systems. Since the registers of a virtual device may be simulatated in the memory map, an access to such a register will cause a fault and the function of the register can be emulated by software.

5

Virtual machine

A typical use for a virtual machine system is the development of software, such as an operating system, for a new machine also under development and not yet available for programming use. In such a system, a governing operating system emulates the hardware of the prototype system and allows the new operating system to be executed and debugged as though it were running on the new hardware. Since the new operating system is controlled by the governing operating system, it is executed at a lower privilege level than the governing operating system. Thus, any attempts by the new operating system to use virtual resources that are not physically present (and should be emulated) are trapped to the governing operating system and handled by its software. In the TS 68020, a virtual machine is fully supported by running the new operating system in the user mode. The governing operating system executes in the supervisor mode and any attempt by the new operating system to access supervisor resources or execute privileged instructions will cause a trap to the governing operating system.

Operand transfer mechanism

Though the TS 68020 has a full 32-bit data bus, it offers the ability to automatically and dynamically downsize its bus to 8 or 16 bits if peripheral devices are unable to accomodate the entire 32 bits. This feature allows the programmer the ability to write code that is not bus-width specific. For example, long word (32 bit) accesses to peripherals may be used in the code, yet the TS 68020 will transfer only the amount of data that the peripheral can manage. This feature allows the peripheral to define its port size as 8, 16, or 32 bits wide and the TS 68020 will dynamically size the data transfer accordingly, using multiple bus cycles when necessary. Hence, programmers are not required to program for each device port size or know the specific port size before coding ; hardware designers have flexibility to choose implementations independent of software prejudices.

This is accomplished through the use of the $\overline{\text{DSACK}}$ pins and occurs on a cycle-by-cycle basis. For example, if the processor is executing an instruction that requires the reading of a long word operand, it will attempt to read 32 bits during the first bus cycle to a long word address boundary. If the port responds that it is 32 bits wide, the TS 68020 latches all 32 bits of data and continues. If the port responds that it is 16 bits wide, the TS 68020 latches 16 valid bits of data an runs another cycle to obtain the other 16 bits of data. An 8-bit port is handled similarly but with four bus read cycles. Each port is fixed in assignment to particular sections of the data bus.

Justification of data on the bus is handled automatically by dynamic bus sizing. When reading 16-bit data from a 32 -bit port, the data may appear on the top or bottom half of the bus, depending on the address of the data. The TS 68020 determines which portion of the bus is needed to support the transfer and dynamically adjusts to read or write the data on those data lines.

The TS 68020 will always transfer the maximum amount of data on all bus cycles ; i.e., it always assumes the port is 32 bits wide when beginning the bus cycle. In addition, the TS 68020 has no restrictions concerning alignment of operands in memory ; long word operands need not be aligned on long word address boundaries. When misaligned data requires multiple bus cycles, the TS 68020 aligned data requires multiple bus cycles, the TS 68020 automatically runs the minimum number of bus cycles.

The coprocessor concept

The coprocessor interface is a mechanism for extending the instruction set of the TS 68000 Family. Examples of these extensions are the addition of specialized data operands for the existing data types or, for the case of floating point, the inclusion of new data types and operations for them as implemented by the TS 68881 and TS 68882 floating-point coprocessors.

The programmer's model for the TS 68000 Family of microprocessors is based on sequential, non-concurrent instruction execution. This means each instruction is completely executed prior to the beginning of the next instruction. Hence, instructions do not operate concurrently in the programmer's model. Most microprocessors implement the sequential model which greatly simplifies the programmer responsabilities since sequencing control is automatic and discrete.

The TS 68000 coprocessor interface is designed to extend the programmers model and it provides full support for the sequential, non-concurrent instruction execution model. Hence, instruction execution by the coprocessor is assumed to not overlap with instruction execution with the main microprocessor. Yet, the TS 68000 coprocessor interface does allow concurrent operation when concurrency can be properly accomodated. For example, the TS 68881 or TS 68882 floating-point coprocessor will allow the TS 68020 to proceed executing instructions while the coprocessor continues a floating-point operation, up to the point that the TS 68020 sends another request to the coprocessor. Adhering to the sequential execution model, the request to the coprocessor continues a floating-point operation, up to the coprocessor completes each TS 68881 and TS 68882 instruction before is starts the next, and the TS 68020 is allowed to proceed as it can in a concurrent fashion.

Coprocessors are divided into two types by their bus utilization characteristics. A coprocessor is a DMA coprocessor if it can control the bus independent of the main processor. A coprocessor is a non-DMA coprocessor if it does not have the capability of controlling the bus. Both coprocessor types utilize the same protocol and main processor resources. Impementation of a coprocessor as a DMA or non-DMA type is based primarily on bus bandwidth requirements of the coprocessor, performance, and cost issues.

The communication protocol between the main processor and the coprocessor necessary to execute a coprocessor instruction is based on a group of coprocessor interface registers (Table 10) which are defined for the TS 68000 Family coprocessor interface. The TS 68020 hardware uses standard TS 68000 asynchronous bus cycles to access the registers. Thus, the coprocessor doesn't require a special bus hardware ; the bus interface implemented by a coprocessor for its interface register set must only satisfy the TS 68020 address, data, and control signal timing to guarantee proper communication with the main processor. The TS 68020 implements the communication protocol with all coprocessors in hardware (and microcode) and handles all operations automatically so the programmer is only concerned with the instructions and data types provided by the coprocessor as extensions to the TS 68020 instruction set and data types.

Other microprocessors in the TS 68000 Family can operate any TS 68000 coprocessor even though they may not have the hardware implementation of the coprocessor interface as does the TS 68020. Since the coprocessor is operated through the coprocessor interface registers which are accessed via normal asynchronous bus cycles, the coprocessor may be used as a peripheral device. Software easily emulates the communication protocol by addressing the coprocessor interface registers appropriately and passing the necessary commands and operands required by the coprocessor.

The coprocessor interface registers are implemented by the coprocessor in addition to those registers implemented as extensions to the TS 68020 programmer's model. For example, the TS 68881 implements the coprocessor interface registers shown in Table 10 and the registers in the programming model, including eight 80-bit floating-point data registers and three 32-bit control / status registers used by the TS 68881 programmer.

Up to eight coprocessors are supported in a single system with a system-unique coprocessor identifier encoded in the coprocessor instruction. When accessing a coprocessor, the TS 68020 executes standard read and write bus cycle in CPU address

Table 10 - Coprocessor interface registers

Register	Function	R / W
Response	Requests Action from CPU	R
Control	CPU Direct Control	W
Save	Initiate Save of Internal State	R
Restore	Initiate Restore of Internal State	R / W
Operation Word	Current Coprocessor Instruction	W
Command Word	Coprocessor Specific Command	W
Condition Word	Condition to be Evaluated	W
Operand	32-Bit Operand	R / W
Register Select	Specifies CPU Register or Mask	R
Instruction Address	Pointer to Coprocessor Instruction	R / W
Operand Address	Pointer to Coprocessor Operand	R /W

Table 11 - Coprocessor primitives

Processor Synchronization Busy with Current Instruction Proceed with Next Instruction, If No Trace Service Interrupts and Re-query, If Trace Enable Proceed with Execution, Condition True / False
Instruction Manipulation Transfer Operation Word Transfer Words from Instruction Stream
Exception Handling Take Privilege Violation if S Bit Not Set Take Pre-Instruction Exception Take Mid-Instruction Exception Take Post-Instruction Exception
General Operand Transfer Evaluate and Pass (ea) Evaluate (ea) and Transfer Data Write to Previously Evaluated (ea) Take Address and Transfer Data Transfer to / from Top of Stack
Register Transfer Transfer CPU Register Transfer CPU Control Register Transfer Multiple CPU Registers Transfer Multiple Coprocessor Registers Transfer CPU SR and / or ScanPC

space, as encoded by the function codes, and places the coprocessor identifier on the address bus to be used by chip-select logic to select the particular coprocessor. Since standard bus cycle are used to access the coprocessor, the coprocessor may be located according to system design requirements, whether it be located on the microprocessor local bus, on another board on the system bus, or any other place where the chip-select and coprocessor protocol using standard TS 68000 bus cycles can be supported.

Coprocessor protocol

Interprocessor transfers are all initiated by the main processor during coprocessor instruction execution. During the processing of a coprocessor instruction, the main processor transfers instruction information and data to the associated coprocessor, and receives data, requests, and status information from the coprocessor. These transfers are all based on the TS 68000 bus cycles.

The typical coprocessor protocol which the main processor follows is :

a) The main processor initiates the communications by writing command information to a location in the coprocessor interface.

b) The main processor reads the coprocessor response to that information.

1) The response may indicate that the coprocessor is busy, and the main processor should again query the coprocessor. This allows the main processor and coprocessor to synchronize their concurrent operations.

2) The response may indicate some exception condition ; the main processor acknowledges the exception and begins exception processing.

3) The response may indicate that the coprocessor needs the main processor to perform some service such as transferring data to or from the coprocessor. The coprocessor may also request that the main processor query the coprocessor again after the service is complete.

4) The response may indicate that the main processor is not needed for further processing of the instruction. The communication is terminated, and the main processor is free to begin execution of the next instruction. At this point in the coprocessor protocol, as the main processor continues to execute the instruction stream, the main processor may operate concurrently with the coprocessor.

When the main processor encounters the next coprocessor instruction, the main processor queries the coprocessor until the coprocessor is ready ; meanwhile, the main processor can go on to service interrupts and do a context switch to execute other tasks, for example.

5

Each coprocessor instruction type has specific requirements based on this simplified protocol. The coprocessor interface may use as many extension words as required to implement a coprocessor instruction.

Primitives / response

The response register is the means by which the coprocessor communicates service requests to the main processor. The content of the coprocessor response register is a primitive instruction to the main processor which is read during coprocessor communication by the main processor. The main processor «executes» this primitive, thereby providing the services required by the coprocessor. Table 11 summarizes the coprocessor primitives that the TS 68020 accepts.

Exceptions

Kinds of exceptions

Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts, the bus error, and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset pins are used for access control and processor restart. The internally generated exceptions come from instructions, address errors, tracing, or breakpoints. The TRAP, TRAPcc, TRAPV, cpTRAPcc, CHK, CHK2, and DIV instructions can all generate exceptions as part of their instruction execution. Tracing behaves like a very high priority, internally generated interrupt whenever it is processed. The other internally generated exceptions are caused by illegal instructions, instruction fetches from odd addresses, and privilege violations.

Exception processing sequence

Exception proccesing occurs in four steps. During the first step, an internal copy is made of the status register. After the copy is made, the special processor state bits in the status register are changed. The S bit is set, putting the processor into supervisor privilege state. Also, the T1 and T0 bits are negated, allowing the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor read that is classified as an interrupt acknowledge cycle. For coprocessor detected exceptions, the vector number is included in the coprocessor exception primitive response. For all other exceptions, internal logic provides the vector number. This vector number is then used to generated the address of the exception vector.

The third step is to save the current processor status. The exception stack frame is created and filled on the supervisor stack. In order to minimize the amount of machine state that is saved, various stack frame sizes are used to contain the processor state depending on the type of exception and where it occurred during instruction execution. If the exeption is an interrupt and the M bit is on, the M bit is forced off, and a short four word exception stack frame is saved on the master stack which indicates that the exception is saved on the interrupt stack. If the exception is a reset, the M bit is simply forced off, and the reset vector is accessed.

The TS 68020 provides an extension to the exception stacking process. If the M bit in the status register is set, the master stack pointer (MSP) is used for all task related exceptions. When a non-task related exception occurs (i.e., an interrupt), the M bit is cleared and the interrupt stack pointer (ISP) is used. This feature allows all the task's stack area to be carried within a single processor control block and new tasks may be initiated by simply reloading the master stack pointer and setting the M bit.

The fourth and last step of exception processing is the same for all exceptions. The exception vector offset is determined by multiplying the vector number by four. This offset is then added to the contents of the vector base register (VBR) to determine the memory address of the exception vector. The new program counter value is fetched from the exception vector. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

On-chip instruction cache

Studies have shown that typical programs spend most of their execution time in a few main routines or tight loops. This phenomenon is known as locality of reference, and has an impact on performance of the program. The TS 68020 takes limited advantage of this phenomenon in the form of its loop mode operation which allows certain instructions, when coupled with the DBcc instruction, to execute without the overhead of instruction fetches. In effect this is a three word cache. Although the cache hardware has been supplied in a full range of computer systems for many years, technology now allows this feature to be integrated into the microprocessor.

TS 68020 cache goals

There where two primary goals for the TS 68020 microprocessor cache. The first design goal was to reduce the processor external bus activity. In a given TS 68000 system, the TS 68000 processor will use approximately 80 to 90 percent (for greater) of the available bus bandwidth. This is due to its extremely efficient prefetching algorithm and the overall speed of its internal architecture design. Thus, in an TS 68000 system with more than one bus master (such as a processor and DMA device) or in a multiprocessor system, performance degradation can occur due to lack of available bus bandwidth. Therefore, an important goal for an TS 68020 on-chip cache was to provide a substantial increase in the total available bus bandwidth.

The second primary design goal was to increase effective CPU throughput as larger memory sizes or slower memories increased average access time. By placing a high speed cache between the processor and the rest of the memory system, the effective access time now becomes :

$$t_{acc} = h^{*}t_{cache} + (1 - h)^{*}t_{ext}$$

where t_{acc} is the effective system access time, t_{cache} is the cache access time, t_{ext} is the access time of the rest of the system, and h is the hit ratio or the percentage of time that the data is found in the cache. Thus, for a given system design, an TS 68020 on-chip cache provides a substantial CPU performance increase, or allows much slower and less expensive memories to be used for the same processor performance.

The throughput increase in the TS 68020 is gained in two ways. First, the TS 68020 cache is accessed in two clock cycles versus the three cycles (minimum) required for an external access. Any instruction fetch that is currently resident in the cache will provide a 33 % improvement over the corresponding external access.

Second, and probably the most important benefit of the cache, is that it allows instruction stream fetches and operand accesses to proceed in parallel. For example, if the TS 68020 requires both an instruction stream access and an operand access, and the instruction is resident in the cache, the operand access will proceed unimpeded rather than being queued behind the instruction fetch. Similarly, the TS 68020 is fully capable of executing several internal instructions (instructions that do not require the bus) while completing an operand access for another instruction.

The TS 68020 instruction cache is a 256-byte direct mapped cache organized as 64 long word entries. Each cache entry consists of a tag field made up of the upper 24 address bits, the FC2 (user / supervisor) value, one valid bit, and 32 bits of instruction data (Figure 19).

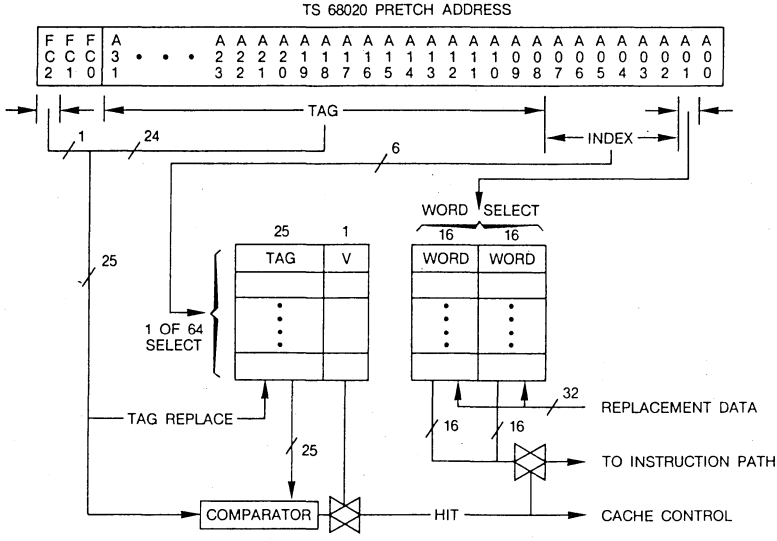


Figure 19 : TS 68020 on-chip cache organization.

The TS 68020 employs a 32 bit data bus and fetches instructions on long word address boundaries. Hence, each 32-bit instruction fetch brings in two 16-bit instruction words which are then written into the on-chip cache. When the cache is enabled, the subsequent prefetch will find the next 16-bit instruction word is already present in the cache and the related bus cycle is saved. If the cache were not enabled, the subsequent prefetch will find the bus controller still holds the full 32 bits and can satisfy the prefetch and again save the related bus cycle. So, even when the on-chip instruction cache is not enabled, the bus controller provides an instruction «cache hit» rate up to 50 %.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

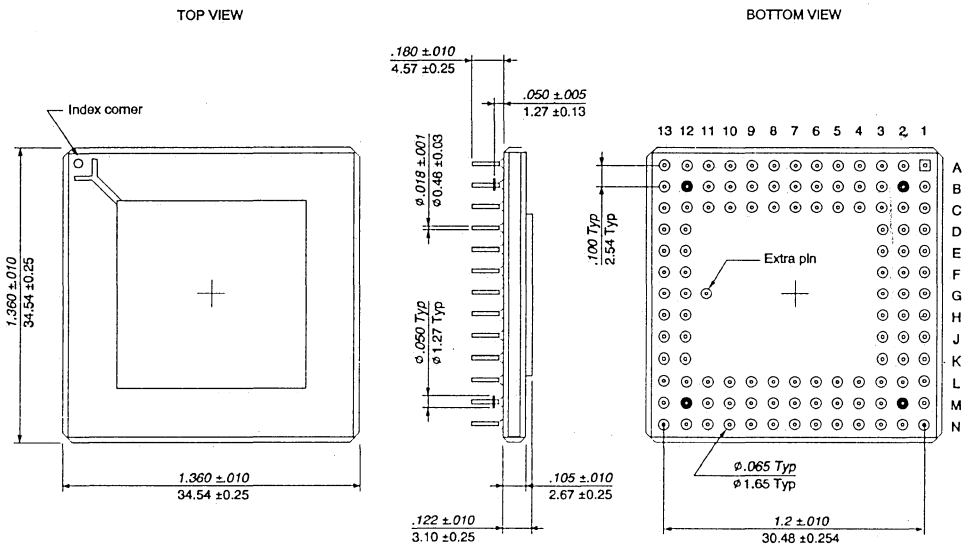
e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 %, if practical.

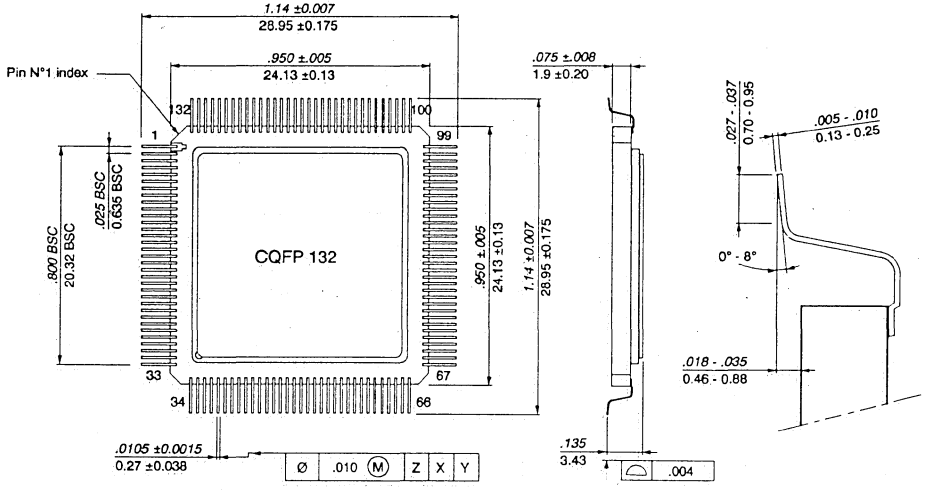
9 · PACKAGE MECHANICAL DATA

9.1 · 114 pins · Ceramic Pin Grid Array

Conform to MIL-M-38510, appendix C, P-AE outline.



9.2 · 132 pins · Ceramic Quad Flat Pack



10 · TERMINAL CONNECTIONS

10.1 · 114 pins · Ceramic Pin Grid Array

See Figure 2.1 page 4.

10.2 · 132 pins · Ceramic Quad Flat Pack

See Figure 2.2 page 4.

11 - ORDERING INFORMATION

11.1 - Hi-REL product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68020MR8B/Y16	CECC	PGA 114	−55 / +125	16.67	90110-004
TS68020MR8B/Y20	CECC	PGA 114	−55 / +125	20	90110-004
TS68020MR8B/Y25	CECC	PGA 114	−55 / +125	25	90110-004
TS68020MF8B/Y16	CECC	CQFP 132	−55 / +125	16.67	90110-004
TS68020MF8B/Y20	CECC	CQFP 132	−55 / +125	20	90110-004
TS68020MF8B/Y25	CECC	CQFP 132	−55 / +125	25	90110-004
TS68020MRB/C16	MIL-STD-883	PGA 114	−55 / +125	16.67	—
TS68020MR1B/C16	MIL-STD-883	PGA 114 / tin	−55 / +125	16.67	—
TS68020MRB/C20	MIL-STD-883	PGA 114	−55 / +125	20	—
TS68020MR1B/C20	MIL-STD-883	PGA 114 / tin	−55 / +125	20	—
TS68020MRB/C25	MIL-STD-883	PGA 114	−55 / +125	25	—
TS68020MR1B/C25	MIL-STD-883	PGA 114 / tin	−55 / +125	25	—
TS68020MFB/C16	MIL-STD-883	CQFP 132	−55 / +125	16.67	—
TS68020MF1B/C16	MIL-STD-883	CQFP 132 / tin	−55 / +125	16.67	—
TS68020MFB/C20	MIL-STD-883	CQFP 132	−55 / +125	20	—
TS68020MF1B/C20	MIL-STD-883	CQFP 132 / tin	−55 / +125	20	—
TS68020MFB/C25	MIL-STD-883	CQFP 132	−55 / +125	25	—
TS68020MF1B/C25	MIL-STD-883	CQFP 132 / tin	−55 / +125	25	—
TS68020DESC02XA	DESC	PGA 114 / tin	−55 / +125	16.67	5962-86032XA
TS68020DESC03XA	DESC	PGA 114 / tin	−55 / +125	20	5962-86033XA
TS68020DESC04XA	DESC	PGA 114 / tin	−55 / +125	25	5962-86034XA
TS68020DESC02YA	DESC	CQFP 132 / tin	−55 / +125	16.67	5962-86032YA
TS68020DESC03YA	DESC	CQFP 132 / tin	−55 / +125	20	5962-86033YA
TS60020DESC04YA	DESC	CQFP 132 / tin	−55 / +125	25	5962-86034YA

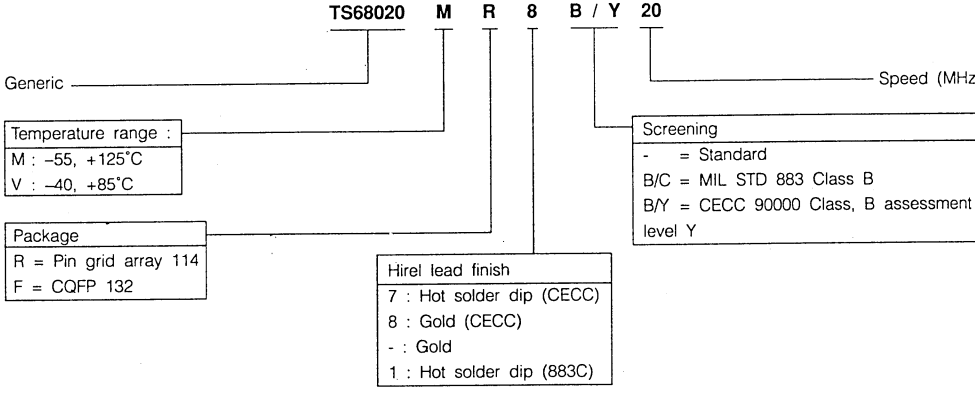
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

5

11.2 · Standard product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68020VR16	TCS Standard	PGA 114	−40 / +85	16.67	Internal
TS68020VR20	TCS Standard	PGA 114	−40 / +85	20	Internal
TS68020VR25	TCS Standard	PGA 114	−40 / +85	25	Internal
TS68020MR16	TCS Standard	PGA 114	−55 / +125	16.67	Internal
TS68020MR20	TCS Standard	PGA 114	−55 / +125	20	Internal
TS68020MR25	TCS Standard	PGA 114	−55 / +125	25	Internal
TS68020VF16	TCS Standard	CQFP 132	−40 / +85	16.67	Internal
TS68020VF20	TCS Standard	CQFP 132	−40 / +85	20	Internal
TS68020VF25	TCS Standard	CQFP 132	−40 / +85	25	Internal
TS68020MF16	TCS Standard	CQFP 132	−55 / +125	16.67	Internal
TS68020MF20	TCS Standard	CQFP 132	−55 / +125	20	Internal
TS68020MF25	TCS Standard	CQFP 132	−55 / +125	25	Internal

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.



TS 68040

THIRD-GENERATION 32-BIT MICROPROCESSOR

DESCRIPTION

The TS 68040 is Thomson's third generation of 68000-compatible, high-performance, 32-bit microprocessors. The TS 68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. On a single chip, the TS 68040 integrates an 68030-compatible integer unit, an IEEE 754-compatible floating-point unit (FPU), and fully independent instruction and data demand-paged memory management units (MMUs), including independent 4K-byte instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses. The TS 68040 also directly supports cache coherency in multimaster applications with dedicated on-chip bus snooping logic.

The TS 68040 is user-object-code compatible with previous members of the TS 68000 Family and is specifically optimized to reduce the execution time of compiler-generated code. The 68040 HCMOS technology, provides an ideal balance between speed, power, and physical device size.

Figure 1 is a simplified block diagram of the TS 68040. Instruction execution is pipelined in both the integer unit and FPU. Independent data and instruction MMUs control the main caches and the address translation caches (ATCs). The ATCs speed up logical-to-physical address translations by storing recently used translations. The bus snooper circuit ensures cache coherency in multimaster and multiprocessing applications.

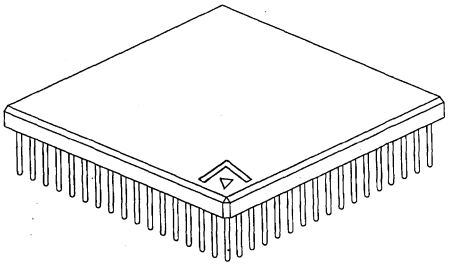
MAIN FEATURES

- 26-42 MIPS integer performance.
- 3.5-5.6 MFLOPS floating-point-performance.
- IEEE 754-Compatible FPU.
- Independant instruction and data MMUs.
- 4K-byte physical instruction cache and 4K-byte physical data cache accessed simultaneously.
- 32-bit, nonmultiplexed external address and data buses with synchronous interface.
- User-object-code compatibility with all earlier TS 68000 microprocessors.
- Multimaster / multiprocessor support via bus snooping.
- Concurrent integer unit, FPU, MMU, bus controller, and bus snooper maximize throughput.
- 4-Gbyte direct addressing range.
- Software support including optimizing C compiler and unix* system V port.
- IEEE P 1149-1 test mode (J tag).
- f = 25 MHz, 33 MHz ; V_{CC} = 5 V ± 5 % ; P_D = 7 W.

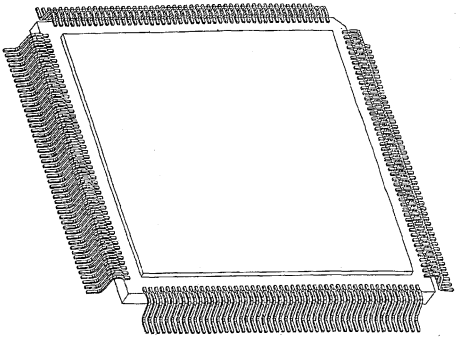
SCREENING

- MIL-STD-883.
- DESC. Drawing 5962-93143.
- TCS standards.

* UNIX is a registered trademark of AT&T Bell Laboratories.



R suffix
PGA 179
Ceramic Pin Grid Array
Cavity down



F suffix
CQFP 196
Gullwing shape lead Ceramic Quad Flat Pack

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

SUMMARY

A - GENERAL DESCRIPTION

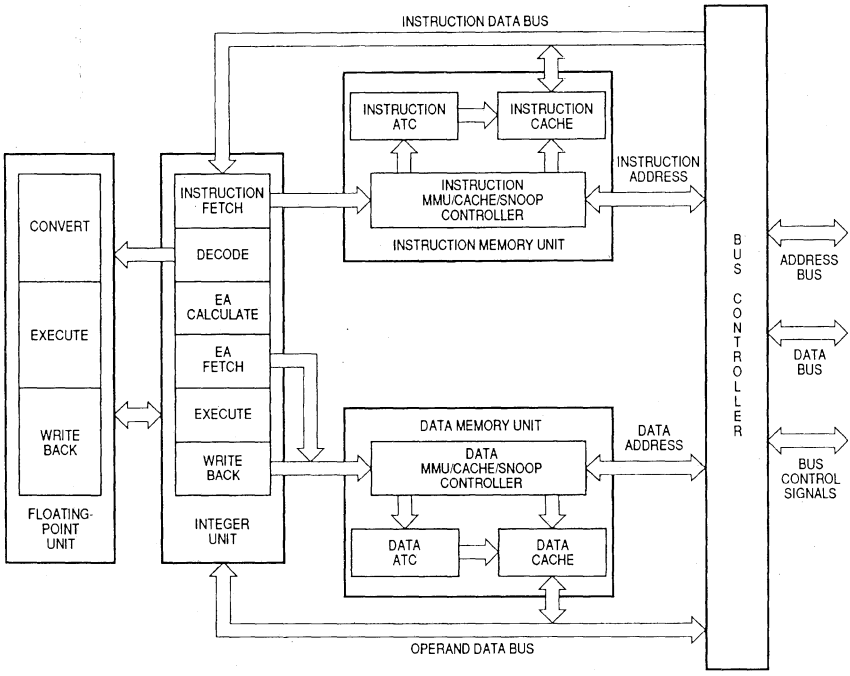


Figure 1 : Block diagram.

1 - INTRODUCTION

The TS 68040 is an enhanced, 32-bit, HCMOS microprocessor that combines the integer unit processing capabilities of the TS 68030 microprocessor with independent 4K-byte data and instruction caches and an on-chip FPU. The TS 68040 maintains the 32-bit registers available with the entire TS 68000 Family as well as the 32-bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high-level language environments.

The TS 68040 FPU is user-object-code compatible with the TS 68882 floating-point coprocessor and conforms to the ANSI / IEEE Standard 754 for binary floating-point arithmetic. The FPU has been optimized to execute the most commonly used subset of the TS 68882 instruction set, and includes additional instruction formats for single and double-precision rounding of results. Floating-point instructions in the FPU execute concurrently with integer instructions in the integer unit.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. The MMUs store recently used address mappings in two separate ATCs-on-chip. When an ATC contains the physical address for a bus cycle requested by the processor, a translation table search is avoided and the physical address is supplied immediately, incurring no delay for adress translation. Each MMU has two transparent translation registers available that define a one-to-one mapping for adress space segments ranging in size from 16 Mbytes to 4 Gbytes each.

Each MMU provides read-only and supervisor-only protections on a page basis. Also, processes can be given isolated address spaces by assigning each a unique table structure and updating the root pointer upon a task swap. Isolated address spaces protect the integrity of independent processes.

The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides writethrough or copyback write modes that can be configured on a page-by-page basis.

The TS 68040 bus controller supports a high-speed, nonmultiplexed, synchronous external bus interface, which allows the following transfer sizes : byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

2 - PIN ASSIGNMENTS

2.1 - PGA 179

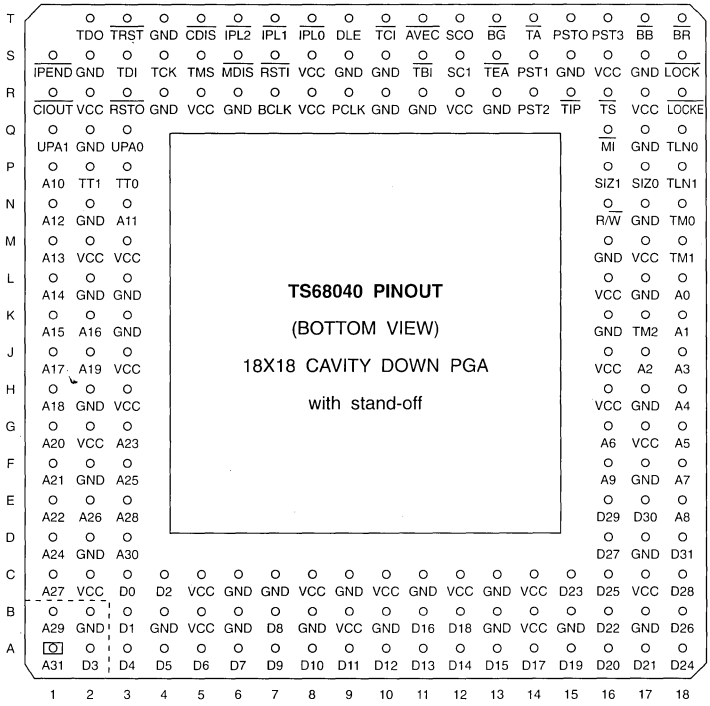


Figure 2 : Bottom view.

Table 1

	GND	V_{CC}
PLL		S8
Internal logic	C6, C7, C9, C11, C13, K3, K16, L3, M16, R4, R11, R13, S10, T4	C5, C8, C10, C12, C14, H3, H16, J3, J16, L16, M3, R5, R12, R8
Output drivers	B2, B4, B6, B8, B10, B13, B15, B17, D2, D17, F2, F17, H2, H17, L2, L17, N2, N17, Q2, Q17, S2, S15, S17	B5, B9, B14, C2, C17, G2, G17, M2, M17, R2, R17, S16

2.2 - CQFP 196

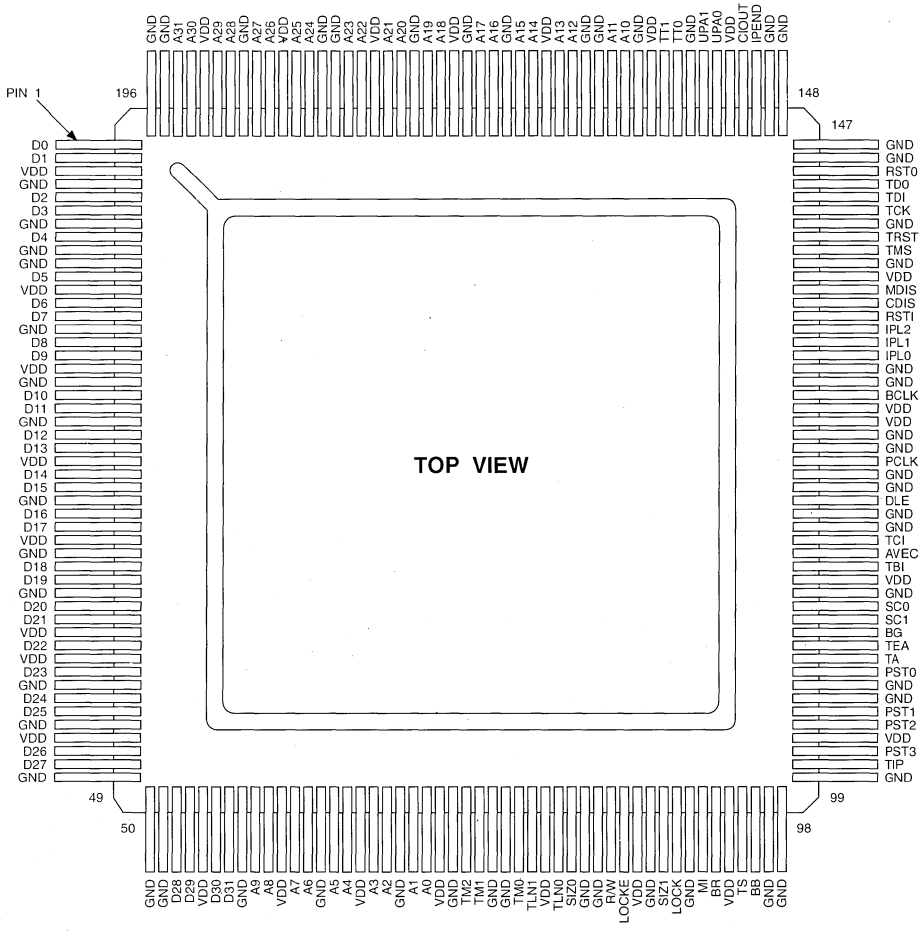


Figure 3 : Pin assignments.

Table 2

	GND	V_{CC}
PLL		127
Internal logic	4, 9, 19, 32, 45, 73, 88, 113, 119, 121, 122, 124, 125, 129, 130, 141, 159, 172	3, 18, 31, 40, 46, 60, 72, 87, 114, 126, 137, 158, 173
Output drivers	7, 15, 22, 28, 35, 42, 49, 50, 51, 57, 63, 69, 76, 77, 83, 84, 91, 97, 98, 99, 105, 106, 146, 147, 148, 149, 155, 162, 163, 169, 176, 182, 183, 189, 195, 196	12, 25, 38, 54, 66, 80, 94, 102, 152, 166, 179, 192

3 - SIGNAL DESCRIPTION

Figure 4 and Table 3 describe the signals on the TS 68040 and indicate signal functions. The test signals, $\overline{TRST}$, TMS, TCK, TDI, and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

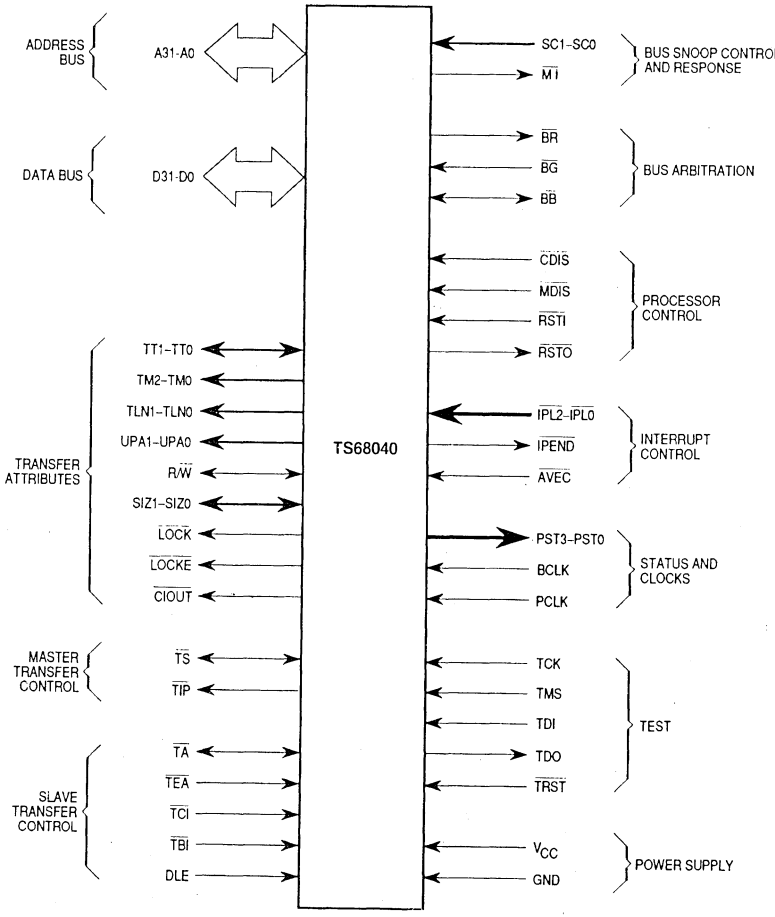


Figure 4 : Functional signal groups.

Table 3 - Signal index

Signal Name	Mnemonic	Function
Address bus	A31-A0	32-bit address bus used to address any of 4 Gbytes
Data bus	D31-D0	32-bit data bus used to transfer up to 32 bits of data per bus transfer
Transfer type	TT1, TT0	Indicates the general transfer type : normal, MOVE 16, alternate logical function code, and acknowledge
Transfer modifier	TM2, TM0	Indicates supplemental information about the access
Transfer line number	TLN1, TLN0	Indicates which cache line in a set is being pushed or loaded by the current line transfer
User programmable attributes	UPA1, UPA0	User-defined signals, controlled by the corresponding user attribute bits from the address translation entry
Read write	R/$\overline{W}$	Identifies the transfer as a read or write
Transfer size	SIZ1, SIZ0	Indicates the data transfer size. These signals, together with A0 and A1, define the active sections of the data bus
Bus lock	$\overline{LOCK}$	Indicates a bus transfer is part of a read-modify-write operation, and that the sequence of transfers should not be interrupted
Bus lock end	$\overline{LOCKE}$	Indicates the current transfer is the last in a locked sequence of transfer
Cache inhibit out	$\overline{CIOUT}$	Indicates the processor will not cache the current bus transfer
Transfer start	$\overline{TS}$	Indicates the beginning of a bus transfer
Transfer in progress	$\overline{TIP}$	Asserted for the duration of a bus transfer
Transfer acknowledge	$\overline{TA}$	Asserted to acknowledge a bus transfer
Transfer error acknowledge	$\overline{TEA}$	Indicates an error condition exists for a bus transfer
Transfer cache inhibit	$\overline{TCI}$	Indicates the current bus transfer should not be cached
Transfer burst inhibit	$\overline{TBI}$	Indicates the slave cannot handle a line burst acces
Data latch enable	DLE	Alternate clock input used to latch input data when the processor is operating in DLE mode
Snoop control	SC1, SC0	Indicates the snooping operation required during an alternate master access
Memory inhibit	$\overline{MI}$	Inhibits memory devices from responding to an alternate master access during snooping operations
Bus request	$\overline{BR}$	Asserted by the processor to request bus mastership
Bus grant	$\overline{BG}$	Asserted by an arbiter to grant bus mastership to the processor
Bus busy	$\overline{BB}$	Asserted by the current bus master to indicate it has assumed ownership of the bus
Cache disable	$\overline{CDIS}$	Dynamically disables the internal caches to assist emulator support
MMU disable	$\overline{MDIS}$	Disables the translation mechanism of the MMUs
Reset in	$\overline{RSTI}$	Processor reset
Reset out	$\overline{RSTO}$	Asserted during execution of the RESET instruction to reset external devices
Interrupt priority level	$\overline{IPL2}$-$\overline{IPL0}$	Provides an encoded interrupt level to the processor
Interrupt pending	$\overline{IPEND}$	Indicates an interrupt is pending
Autovector	$\overline{AVEC}$	Used during an interrupt acknowledge transfer to request internal generation of the vector number
Processor status	PST3-PST0	Indicates internal processor status
Bus clock	BCLK	Clock input used to derive all bus signal timing

Table 3 - Signal index (Continued)

Signal Name	Mnemonic	Function
Processor clock	PCLK	Clock input used for internal logic timing. The PCLK frequency is exactly 2X the BCLK frequency
Test clock	TCK	Clock signal for the IEEE P1149.1 test access port (TAP)
Test mode select	TMS	Selects the principle operations of the test-support circuitry
Test data input	TDI	Serial data input for the TAP
Test data output	TDO	Serial data output for the TAP
Test reset	$\overline{TRST}$	Provides an asynchronous reset of the TAP controller
Power supply	V_{CC}	Power supply
Ground	GND	Ground connection

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microprocessor TS 68040 - 25 MHz and 33 MHz, in compliance with MIL-STD-883 class B or TCS standard screening.

2 - APPLICABLE DOCUMENTS

MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.

2) MIL-I-38535 : general specifications for microcircuits.

3) DESC 5962-93143.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2 and 3 (§ A).

3.2.2 - Lead material and finish

Lead material and finish shall be as specified in MIL-STD-853 (see enclosed § 10).

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835-or as follow :

– CMGA 10-179-PAK pin grid array, but see § 9.1.

– similar to CQCC1-F196C-U6 ceramic uniform lead chip carrier package with ceramic non conductiv tie-bar but use our internal drawing see § 9.2,

– gullwing shape CQFP see § 9.3.

The precise case outlines are described at the end of the specification (§ 9) and into MIL-STD-1835.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 4 - **Absolute maximum ratings**

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Supply voltage range		- 0.3	7.0	V
V_I	Input voltage range		- 0.3	7.0	V
P_D	Power dissipation	Large buffers enabled		7.7	W
		Small buffers enabled		6.3	W
T_C	Operating temperature		- 55	T_J	°C
T_{stg}	Storage temperature range		- 65	+ 150	°C
T_J	Junction temperature (see Note)			+ 125	°C
T_{lead}	Lead temperature	Max.10 sec soldering		+ 300	°C

Note : This device is not tested at T_C = + 125°C. Testing is performed by setting the junction temperature T_j = + 125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

3.3.2 - Recommended conditions of use

Table 5

Unless otherwise stated, all voltages are referenced to the reference terminal (see § A.3).

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range		+ 4.75		+ 5.25	V
V_{IL}	Logic low level input voltage range		GND - 0.3		0.8	V
V_{IH}	Logic high level input voltage range		+ 2.0		VCC + 0.3	V
V_{OH}	High level output voltage		2.4			V
V_{OL}	Low level output voltage				0.5	V
f_c	Clock frequency	- 25 MHz version		25		MHz
		- 33 MHz version		33		MHz
T_C	Case operating temperature range (see Note)		- 55		T_{Jmax}	°C
T_J	Maximum operating junction temperature				+ 125	°C

Note : This device is not tested at T_C = + 125°C. Testing is performed by setting the junction temperature T_J = + 125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

3.4 - Thermal considerations

3.4.1 - General thermal considerations

This section is given for information only of user.

As microprocessors are becoming more complex and requiring more power, the need to efficiently cool the device becomes increasingly more important. In the past, the TS 68000 Family, has been able to provide a 0-70°C ambient temperature part for speeds less than 40 MHz. However, the TS 68040, which has a 50 MHz arithmetic logic unit (ALU) speed, is specified with a maximum power dissipation for a particular mode, a maximum junction temperature, and a thermal resistance from the die junction to the case. This provides a more accurate method of evaluating the environment, taking into consideration both the air-flow and ambient temperature available. This also allows a user the information to design a cooling method which meets both thermal performance requirements and constraints of the board environment.

This section discusses the device charateristics for thermal management, several methods of thermal management, and an example of one method of cooling the TS 68040.

Thermal device characteristics

The TS 68040 presents some inherent characteristics which should be considered when evaluating a method of cooling the device. The following paragraphs discuss these die / package and power considerations.

Die and package

The TS 68040 is being placed in a cavity-down alumina-ceramic 179-pin PGA that has a specified thermal resistance from junction to case of 1°C/W. This package differs from previous TS 68000 Family PGA packages which were cavity up. This cavity-down design allows the die to be attached to the top surface of the package, which increases the ability of the part to dissipate heat through the package surface or an attached heat sink. The maximum perimeter that the TS 68040 allows for a heat sink on its surface without interfering with the capacitor pads is 1.48" × 1.48". The specific dimensions and design of the particular heat sink will need to be determined by the system designer considering both thermal performance requirements and size requirements.

Power considerations

The TS 68040 has a maximum power rating, which varies depending on the operating frequency and the output buffer mode combination being used. The large buffer output mode dissipates more power than the small, and the higher frequencies of operation dissipate more power than the lower frequencies. The following paragraphs discuss tradeoffs in using the different output buffer modes, calculation of specific maximum power dissipation for different modes, and the relationship of thermal resistances and temperatures.

Output buffer mode

The 68040 is capable of resetting to enable for a combination of either large buffers or small buffers on the outputs of the miscellaneous control signals, data bus, and address bus / transfer attribute pins. The large buffers offer quicker output times, which allow for an easier logic design. However, they do so by driving about 11 times as much current as the small buffers (refer to TS 68040 Electrical specifications for current output). The designer should consider whether the quicker timings present enough advantage to justify the additional consideration to the individual signal terminations, the die power consumption, and the required cooling for the device. Since the TS 68040 can be powered-up in one of eight output buffer modes upon reset, the actual maximum power consumption for TS 68040 rated at a particular maximum operating frequency is dependent upon the power up mode. Therefore, the TS 68040 is rated at a maximum power dissipation for either the large buffers or small buffers at a particular frequency (refer to TS 68040 Electrical specifications). This allows the possibility of some of the thermal management to be controlled upon reset. The following equation provides a rough method to calculate the maximum power consumption for a chosen output buffer mode :

$$P_D = P_{DSB} + (P_{DLB} - P_{DSB}) * (PINS_{LB}/PINS_{CLB}) \qquad \text{(Equation 4.1)}$$

where :

P_D = Max. power dissipation for output buffer mode selected

P_{DSB} = Max. power dissipation for small buffer mode (all outputs)

P_{DLB} = Max. power dissipation for large buffer mode (all outputs)

$PINS_{LB}$ = Number of pins large buffer mode

$PINS_{CLB}$ = Number of pins capable of the large buffer mode

Table 6 shows the simplified relationship on the maximum power dissipation for eight possible configurations of output buffer modes.

Table 6 - Maximum power dissipation for output buffer mode configurations

Output configuration			Maximum power dissipation
Data bus	**Address bus and transfer attrib.**	**Misc. control signals**	**P_D**
Small buffer	Small buffer	Small buffer	P_{DSB}
Small buffer	Small buffer	Large buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 13\,\%$
Small buffer	Large buffer	Small buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 52\,\%$
Small buffer	Large buffer	Large buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 65\,\%$
Large buffer	Small buffer	Small buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 35\,\%$
Large buffer	Small buffer	Large buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 48\,\%$
Large buffer	Large buffer	Small buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 87\,\%$
Large buffer	Large buffer	Large buffer	$P_{DSB} + (P_{DLB} - P_{DSB}) * 100\,\%$

To calculate the specific power dissipation of a specific design, the termination method of each signal must be considered. For example, a signal output that is not connected would not dissipate any additional power if it were configured in the large buffer rather than the small buffer mode.

Relationships between thermal resistances and temperatures

Since the maximum operating junction temperature has been specified to be 125°C. The maximum case temperature, T_C, in °C can be obtained from :

$$T_C = T_J - P_D * \Phi_{JC} \quad \text{(Equation 4.2)}$$

where :

T_C = Maximum case temperature
T_J = Maximum junction temperature
P_D = Maximum power dissipation of the device
Φ_{JC} = Thermal resistance between the junction of the die and the case

In general, the ambient temperature, T_A, in °C is a function of the following formula :

$$T_A = T_J - P_D * \Phi_{JC} - P_D * \Phi_{CA} \quad \text{(Equation 4.3)}$$

Where the thermal resistance from case to ambient, Φ_{CA}, is the only user-dependent parameter once a buffer output configuration has been determined. As seen from equation (4.3), reducing the case to ambient thermal resistance increases the maximum operating ambient temperature. Therefore, by utilizing such methods as heat sinks and ambient air cooling to minimize the Φ_{CA}, a higher ambient operating temperature and / or a lower junction temperature can be achieved.

However, an easier approach to thermal evaluation uses the following formulas :

$$T_A = T_J - P_D * \Phi_{JA} \quad \text{(Equation 4.4)}$$

or alternatively,

$$T_J = T_A + P_D * \Phi_{JA} \quad \text{(Equation 4.5)}$$

where :

Φ_{JA} = thermal resistance from the junction to the ambient ($\Phi_{JC} + \Phi_{CA}$).

This total thermal resistance of a package, Φ_{JA}, is a combination of its two components, Φ_{JC} and Φ_{CA}. These components represent the barrier to heat flow from the semiconductor junction to the package (case) surface (Φ_{JC}) and from the case to the outside ambient (Φ_{JC}). Although Φ_{JC} is device related and cannot be influenced by the user, Φ_{CA} is user dependent. Thus, good thermal management by the user can significantly reduce Φ_{CA} achieving either a lower semiconductor junction temperature or a higher ambient operating temperature.

Thermal management techniques

To attain a reasonable maximum ambient operating temperature, a user must reduce the barrier to heat flow from the semiconductor junction to the outside ambient (Φ_{JA}). The only way to accomplish this is to significantly reduce Φ_{CA} by applying such thermal management techniques as heat sinks and ambient air cooling.

The following paragraphs discuss some results of a thermal study of the TS 68040 device without using any thermal management techniques ; using only air-flow cooling, using only a heat sink, and using heat sink combined with air-flow cooling.

Thermal characteristics in still air

A sample size of three TS 68040 packages was tested in free-air cooling with no heat sink. Measurements showed that the average Φ_{JA} was 22.8°C/W with a standard deviation of 0.44°C/W. The test was performed with 3 W of power being dissipated from within the package. The test determined that Φ_{JA} will decrease slightly for the increasing power dissipation range possible. Therefore, since the variance in Φ_{JA} within the possible power dissipation range is negligible, it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Using the formulas introduced previously, Table 7 shows the results of a maximum power dissipation of 3 and 5 W with no heat sink or air-flow (refer to Table 6 to calculate other power dissipation values).

Table 7 - Thermal parameters with no heat sink or air-flow

Defined paramaters			Measured	Calculated		
P_D	T_J	Φ_{JC}	Φ_{JA}	$\Phi_{CA} = \Phi_{JA} - \Phi_{JC}$	$T_C = T_J - P_D * \Phi_{JC}$	$T_A = T_J - P_D * \Phi_{JA}$
3 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	122°C	59.6°C
5 Watts	125°C	1°C/W	21.8°C/W	20.8°C/W	120°C	16°C

As seen by looking at the ambient temperature results, most users will want to implement some type of thermal management to obtain a more reasonable maximum ambient temperature.

Thermal characteristics in forced air

A sample size of three TS 68040 packages was tested in forced air cooling in a wind tunnel with no heat sink. This test was performed with 3 W of power being dissipated from within the package. As previously mentioned, since the variance in Φ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Using the previous formulas, Table 8 shows the results of the maximum power dissipation at 3 and 5 W with air-flow and no heat sink (refer to Table 6 to calculate other power dissipation values).

Table 8 - Thermal parameters with forced air flow and no heat sink

Thermal Mgmt. Technique	Defined parameters			Measured	Calculated		
Air-flow velocity	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	3 W	125°C	1°C/W	11.7°C/W	10.7°C/W	122°C	89.9°C
250 LFM	3 W	125°C	1°C/W	10°C/W	9°C/W	122°C	95°C
500 LFM	3 W	125°C	1°C/W	8.9°C/W	7.9°C/W	122°C	98.3°C
750 LFM	3 W	125°C	1°C/W	8.5°C/W	7.5°C/W	122°C	99.5°C
1 000 LFM	3 W	125°C	1°C/W	8.3°C/W	7.3°C/W	122°C	100.1°C
100 LFM	5 W	125°C	1°C/W	11.7°C/W	10.7°C/W	120°C	66.5°C
250 LFM	5 W	125°C	1°C/W	10°C/W	9°C/W	120°C	75°C
500 LFM	5 W	125°C	1°C/W	8.9°C/W	7.9°C/W	120°C	80.5°C
750 LFM	5 W	125°C	1°C/W	8.5°C/W	7.5°C/W	120°C	82.5°C
1 000 LFM	5 W	125°C	1°C/W	8.3°C/W	7.3°C/W	120°C	83.5°C

By reviewing the maximum ambient operating temperatures, it can be seen that by using the all-small-buffer configuration of the TS 68040 with a relatively small amount of air flow (100 LFM), a 0-70°C ambient operating temperature can be achieved. However, depending on the output buffer configuration and available forced-air cooling, additional thermal management techniques may be required.

Thermal characteristics with a heat sink

In choosing a heat sink the designer must consider many factors : heat sink size and composition, method of attachment, and choice of a wet or dry connection. The following paragraphs discuss the relationship of these decisions to the thermal performance of the design noticed during experimentation.

The heat sink size is one of the most significant parameters to consider in the selection of a heat sink. Obviously a larger heat sink will provide better cooling. However, it is less obvious that the most benefit of the larger heat sink of the pin fin type used in the experimentation would be at still air conditions. Under forced-air conditions as low as 100 LFM, the difference between the Φ_{CA} becoms very small (0.4°C/W or less). This difference continues to decrease as the forced air flow increases. The particular heat sink used in our testing fit the perimeter package surface area available within the capacitor pads on the TS 68040 (1.48" × 1.48") and showed a nice compromise between height and thermal performance needs. The heat sink base perimeter area was 1.24" × 1.30" and its heigh was 0.49". It was a pin-fin-type (i.e. bed of nails) design composed of Al alloy. The heat sink is shown in Figure 5 can be obtained through Thermalloy Inc. by referencing part number 2338B.

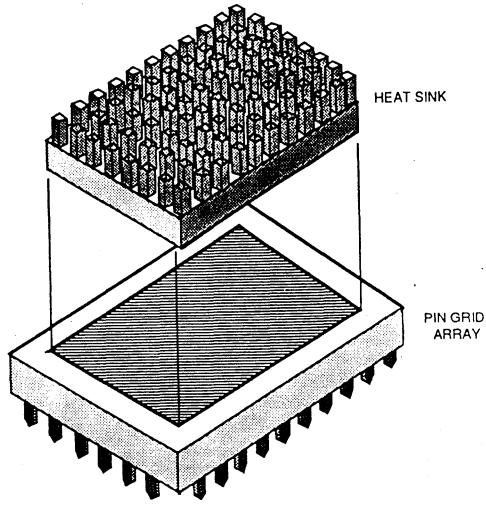


Figure 5 : Heat sink example.

All pin fin heat sinks tested were made from extrusion Al products. The planar face of the heat sink mating to the package should have a good degree of planarity ; if it has any curvature, the curvature should be convex at the central region of the heat sink surface to provide intimate physical contact to the PGA surface. All heat sinks tested met this criteria. Nonplanar, concave curvature the central regions of the heat sink will result in poor thermal contact to the package. A specification needs to be determined for the planarity of the surface as part of any heat sink design.

Although there are several ways to attach a heat sink to the package, it was easiest to use a demountable heat sink attach called «E-Z attach for PGA packages» developed by Thermalloy (see Figure 6). The heat sink is clamped to the package with the help of a steel spring to a plastic frame (or plastic shoes Besides the height of the heat sink and plastic frame, no additional height added to the package. The interface between the ceramic package and the heat sink was evaluated for both dry and wet (e.i., thermal grease) interfaces in still air. The thermal grease reduced the Φ_{CA} quite significantly (about 2.5 °C/W) in still air. Therefore, it was used in all other testing done with the heat sink. According to other testing, attachment with thermal grease provided about the same thermal performance as if a thermal epoxy were used.

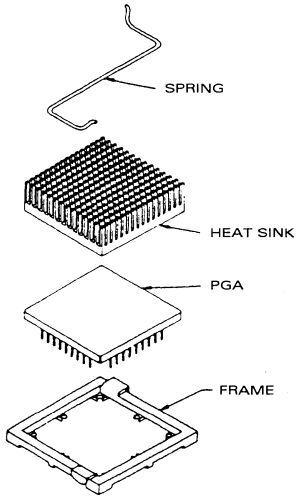


Figure 6 : Heat sink with attachment.

A sample size of one TS 68040 package was tested in still air with the heat sink and attachment method previously described. This test was performed with 3 W of power being dissipated from within the package. Since the variance in Φ_{JA} within the possible power range is negligible, it can be assumed for calculation purposes that Φ_{JA} is constant at all power levels. Table 9 shows the result assuming a maximum power dissipation of the part at 3 and 5 W (refer to Table 6 to calculate other power dissipation values).

Table 9 - Thermal parameters with heat sink and no air-flow

Thermal Mgmt. Technique	Defined parameters			Measured	Calculated		
Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
2338B	3 W	125°C	1°C/W	14°C/W	13°C/W	122°C	83°C
2338B	5 W	125°C	1°C/W	14°C/W	13°C/W	120°C	55°C

Thermal characteristics with a heat sink and forced air

A sample size of three TS 68040 packages was tested in forced-air cooling in a wind tunnel with a heat sink. This test was performed with 3 W of power being dissipated from within the package. As mentioned previously, the variance in Φ_{JA} within the possible power range is negligible ; it can be assumed for calculation purposes that Φ_{JA} is valid at all power levels. Table 10 shows the results, assuming a maximum power dissipation at 3 and 5 W with air flow and heat sink thermal management (refer to Table 6 to calculate other power dissipation values).

Table 10 - Thermal parameters with heat sink and air-flow

Thermal Mgmt. Technique		Defined parameters			Measured	Calculated		
Air-flow	Heat sink	P_D	T_J	Φ_{JC}	Φ_{JA}	Φ_{CA}	T_C	T_A
100 LFM	2338B	3 W	125°C	1°C/W	3.1°C/W	2.1°C/W	122°C	115.7°C
250 LFM	2338B	3 W	125°C	1°C/W	2.2°C/W	1.2°C/W	122°C	118.4°C
500 LFM	2338B	3 W	125°C	1°C/W	1.7°C/W	0.7°C/W	122°C	119.9°C
750 LFM	2338B	3 W	125°C	1°C/W	1.5°C/W	0.5°C/W	122°C	120.5°C
1 000 LFM	2338B	3 W	125°C	1°C/W	1.4°C/W	0.4°C/W	122°C	120.8°C
100 LFM	2338B	5 W	125°C	1°C/W	3.1°C/W	2.1°C/W	120°C	109.5°C
250 LFM	2338B	5 W	125°C	1°C/W	2.2°C/W	1.2°C/W	120°C	114°C
500 LFM	2338B	5 W	125°C	1°C/W	1.7°C/W	0.7°C/W	120°C	116.5°C
750 LFM	2338B	5 W	125°C	1°C/W	1.5°C/W	0.5°C/W	120°C	117.5°C
1 000 LFM	2338B	5 W	125°C	1°C/W	1.4°C/W	0.4°C/W	120°C	118°C

Thermal testing summary

Testing proved that a heat sink in combination with a relatively small amount of air-flow (100 LFM or less) will easily realize a 0-70°C ambient operating temperature for the TS 68040 with almost any configuration of the output buffers. A heat sink alone may be capable of providing all necessary cooling, depending on the particular heat sink height / size restraints, the maximum ambient operating temperature required, and the output buffer configuration chosen. Also forced air cooling alone may attain a 0-70°C ambient operating temperature. However this factor is highly dependent on the output buffer configuration chosen and the available forced air for cooling. Figure 7 is a summary of the test results of the relationship between Φ_{JA} and air-flow for the TS 68040.

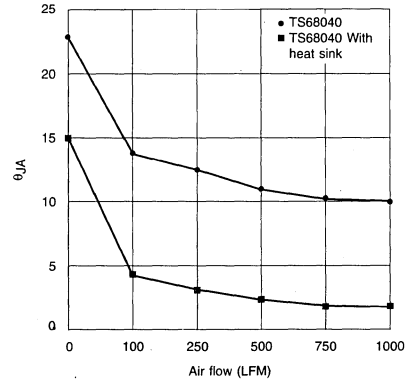


Figure 7 : Relationship of Φ_{JA} air-flow.

3.4.2 - Characteristics guaranted

Table 11

Package	Symbol	Parameter	Value	Unit
PGA 179	θ_{J-A}	Thermal resistance junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal resistance junction-to-case	1	°C/W
CQFP 196	θ_{J-A}	Thermal resistance junction-to-ambient	TBD	°C/W
	θ_{J-C}	Thermal resistance junction-to-case	1	°C/W

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or for TCS standard screening.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo,
- Manufacturer's part number,
- Class B identification,
- Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 12 : Static electrical characteristics for the electrical variants,
- Table 13 : Dynamic electrical characteristics for TS 68040 (25 MHz, 33 MHz).

5

For static characteristics (Table 12), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 13), test methods refer to clause 5.2 of this specification.

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.2. here above.

5.2 - Static characteristics

Table 12 - Electrical characteristics

$-55°C \leq T_C \leq T_{Jmax}$; $4.75\,V \leq V_{CC} \leq 5.25\,V$ unless otherwise specified - Notes 1, 2, 3 and 4

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input high voltage	2	VCC	V
V_{IL}	Input low voltage	GND	0.8	V
V_U	Undershoot		– 0.8	V
I_{in}	Input leakage current @ 0.5 / 2.4 V — $\overline{AVEC}$, BCLK, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$, PCLK, $\overline{RSTI}$, SCn, $\overline{TBI}$, $\overline{TCI}$, TCK, $\overline{TEA}$	– 20	20	µA
I_{TSI}	Hi-Z (off-state) leakage current @ 0.5 / 2.4 V — An, $\overline{BB}$, $\overline{CIOUT}$, Dn, $\overline{LOCK}$, $\overline{LOCKE}$, R/$\overline{W}$, SIZn, $\overline{TA}$, TDO, $\overline{TIP}$, TLNn, TMn, $\overline{TS}$, TTn, UPAn	– 20	20	µA
I_{IL}	Signal low input current V_{IL} = 0.8 V — TMS, TDI, $\overline{TRST}$	– 1.1	– 0.18	mA
I_{IH}	Signal high input current V_{IH} = 2.0 V — TMS, TDI, $\overline{TRST}$	– 0.94	– 0.16	mA
V_{OH}	Output high voltage Larger buffers - I_{OH} = 35 mA Small buffers - I_{OH} = 5 mA	2.4		V

Table 12 - Electrical characteristics (Continued)

Symbol	Characteristic	Min.	Max.	Unit
V_{OL}	Output low voltage Larger buffers - I_{OL} 35 mA Small buffers - I_{OL} 5 mA		0.5	V
P_D	Power dissipation (T_J 125 °C) Larger buffers enabled Small buffers enabled		7.7 6.3	W
C_{in}	Capacitance - Note 4 V_{in} = 0 V, f = 1 MHz		25	pF

Note 1 : All testing to be performed using worst-case test conditions unless otherwise specified.

Note 2 : Maximum operating junction temperature (T_J) + 125 °C. Minimum case operating temperature (T_C) – 55 °C. This device is not tested at T_C + 125 °C. Testing is performed by setting the junction temperature T_J + 125 °C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Note 3 : Capacitance is periodically sampled rather than 100 % tested.

Note 4 : Power dissipation may vary in between limits depending on the application.

5.3 - Dynamic characteristics

Table 13 - Clock AC timing specifications (see Figure 8)

– 55 °C ≤ T_C ≤ T_{Jmax} ; 4.75 V ≤ V_{CC} ≤ 5.25 V unless otherwise specified - Notes 1, 2, 3 and 4

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
	Frequency of operation	20	25	20	33	MHz
1	PCLK cycle time	20	25	15	25	ns
2	PCLK rise time - Note 4		1.7		1.7	ns
3	PCLK fall time - Note 4		1.6		1.6	ns
4	PCLK duty cycle measured at 1.5 V - Note 4	47.5	52.5	46.67	53.33	%
4a	PCLK pulse width high measured at 1.5 V - Notes 3 and 4	9.5	10.5	7	8	ns
4b	PCLK pulse width low measured at 1.5 V - Notes 3 and 4	9.5	10.5	7	8	ns
5	BCLK cycle time	40	50	30	60	ns
6, 7	BCLK rise and fall time		4		3	ns
8	BCLK duty cycle measured at 1.5 V - Note 4	40	60	40	60	%
8a	BCLK pulse width high measured at 1.5 V - Note 4	16	24	12	18	ns
8b	BCLK pulse width low measured at 1.5 V - Note 4	16	24	12	18	ns
9	PCLK, BCLK frequency stability - Note 4		1000		1000	ppm
10	PCLK to BCLK skew		9		n/a	ns

Note 1 : All testing to be performed using worst-case test conditions unless otherwise specified.

Note 2 : Maximum operating junction temperature (T_J) = + 125 °C. Minimum case operating temperature (T_C) = – 55 °C. This device is not tested at T_C = + 125 °C. Testing is performed by setting the junction temperature T_J = + 125 °C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Note 3 : Specification value at maximum frequency of operation.

Note 4 : If not tested, shall be guaranteed to the limits specified.

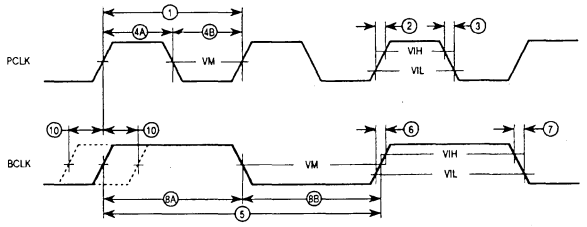


Figure 8 : Clock input timing

Table 14 - Output AC timing specifications (Note 1) (Figures 9 - 15)

These output specifications are for only 25 MHz they must be scaled for lower operating frequencies. Refer to TS 3804DH/AD for further information.

$-55°C < T_C < T_{Jmax}$; $4.75\,V < V_{CC} < 5.25\,V$ unless otherwise specified - Notes 2, 3 and 4

Num	Characteristic	25 MHz				33 MHz				Unit
		Large buffer Note 1		Small buffer Note 1		Large buffer Note 1		Small buffer Note 1		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
11	BCLK to adress CIOUT, LOCK, LOCKE, R/W, SIZn, TLN, TMn, TTn, UPAn valid - Note 5	9	21	9	30	6.50	18	6.50	25	ns
12	BCLK to output invalid (output hold)	9		9		6.50		6.50		ns
13	BCLK to TS valid	9	21	9	30	6.50	18	6.50	25	ns
14	BCLK to TIP valid	9	21	9	30	6.50	18	6.50	25	ns
18	BCLK to data-out valid - Note 6	9	23	9	32	6.50	20	6.50	27	ns
19	BCLK to data-out invalid (output hold) - Note 6	9		9		6.50		6.50		ns
20	BCLK to output low impedance - Notes 5 and 6	9		9		6.50		6.50		ns
21	BCLK to data-out high impedance	9	20	9	20	6.50	17	6.50	17	ns
26	BCLK to multiplexed address valid - Note 5	19	31	19	40	14	26	14	33	ns
27	BCLK to multiplexed address driven - Note 5	19		19		14		14		ns
28	BCLK to multiplexed address high impedance Notes 5 and 6	9	18	9	18	6.50	15	6.50	15	ns
29	BCLK to multiplexed data driven - Note 6	19		19		14	20	14	20	ns
30	BCLK to multiplexed data valid - Note 6	19	33	19	42	14	28	14	35	ns
38	BCLK to address, CIOUT, LOCK, LOCKE, R/W, SIZn, TS, TLNn, TMn, TTn, UPAn high impedance Note 5	9	18	9	18	6.50	15	6.50	15	ns
39	BCLK to BB, TA, TIP high impedance	19	28	19	28	14	23	14	23	ns
40	BCLK to BR, BB valid	9	21	9	30	6.50	18	6.50	25	ns

5

Table 14 - Output AC timing specifications (Continued)

Num	Characteristic	25 MHz				33 MHz				Unit
		Large buffer Note 1		Small buffer Note 1		Large buffer Note 1		Small buffer Note 1		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
43	BCLK to $\overline{MI}$ valid	9	21	9	30	6.50	18	6.50	25	ns
48	BCLK to $\overline{TA}$ valid	9	21	9	30	6.50	18	6.50	25	ns
50	BCLK to $\overline{IPEND}$, PSTn, $\overline{RSTO}$ valid	9	21	9	30	6.50	18	6.50	25	ns

Note 1 : Output timing is specified for a valid signal measured at the pin. Large buffer timing is specified driving a 50 Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay, terminated through 50 Ω to 2.5 V. Large buffer output impedance is typically 3 Ω, resulting in incident wave switching for this environnement. Small buffer timing is specified driving an unterminated 30 Ω transmission line with a length characterized by a 2.5 ns one-way propagation delay. Small buffer output impedance is typically 30 Ω ; the small buffer specifications include approximately 5 ns for the signal to propagate the lenght of the transmission line and back.

Note 2 : All testing to be performed using worst-case test conditions unless otherwise specified.

Note 3 : The following pins are active low : AVEC, BG, BS, BR, CDIS, CIOUT, IPEND, IPLO, IPL1, IPL2, LOCK, LOCKE, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, TA, TBI, TCI, TEA, TIP, TRST, TS and W of R/W.

Note 4 : Maximum operating junction temperature (T_J) = + 125°C. Minimum case operating temperature (T_C) = – 55°C. This device is not tested at T_C = + 125°C. Testing is performed by setting the junction temperature T_J = + 125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Note 5 : Timing specifications 11, 20 and 38 for address bus output timing apply when normal bus operation is selected. Specifications 26, 27 and 28 should be used when the multiplexed bus mode of operation is enabled.

Note 6 : Timing specifications 18 and 19 for data bus output timing apply when normal bus operation is selected. Specifications 28 and 29 should be used when the multiplexed bus mode of operation is enabled.

Table 15 - Input AC timing specifications (Figures 9 - 15)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75\,V \leq V_{CC} \leq 5.25\,V$ unless otherwise specified - Notes 1, 2, 3 and 4

Num	Characteristic	25 MHz		33 MHz		Unit
		Min.	Max.	Min.	Max.	
15	Data-in valid to BCLK (setup)	5		4		ns
16	BCLK to data-in invalid (hold)	4		4		ns
17	BCLK to data-in high impedance (read followed by write)		49		36.5	ns
22a	$\overline{TA}$ valid to BCLK (setup)	10		10		ns
22b	$\overline{TEA}$ valid to BCLK (setup)	10		10		ns
22c	$\overline{TCI}$ valid to BCLK (setup)	10		10		ns
22d	$\overline{TBI}$ valid to BCLK (setup)	11		10		ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ invalid (hold)	2		2		ns
24	$\overline{AVEC}$ valid to BCLK (setup)	5		5		ns
25	BCLK to $\overline{AVEC}$ invalid (hold)	2		2		ns
31	DLE width high	8		8		ns
32	Data-in valid to DLE (setup)	2		2		ns
33	DLE to data-in invalid (hold)	8		8		ns
34	BCLK to DLE hold	3		3		ns
35	DLE high to BCLK	16		12		ns
36	Data-in valid to BCLK (DLE mode setup)	5		5		ns
37	BCLK Data-in invalid (DLE mode hold)	4		4		ns
41a	$\overline{BB}$ valid to BCLK (setup)	7		7		ns
41b	$\overline{BG}$ valid to BCLK (setup)	8		7		ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ valid to BCLK (setup)	10		8		ns
41d	$\overline{IPLn}$ valid to BCLK (setup)	4		3		ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, $\overline{IPLn}$, $\overline{MDIS}$ invalid (hold)	2		2		ns
44a	Address valid to BCLK (setup)	8		7		ns
44b	SIZn valid BCLK (setup)	12		8		ns
44c	TTn valid to BCLK (setup)	6		8.5		ns
44d	R/$\overline{W}$ valid to BCLK (setup)	6		5		ns
44e	SCn valid to BCLK (setup)	10		11		ns
45	BCLK to address SIZn, TTn, R/$\overline{W}$, SCn invalid (hold)	2		2		ns
46	$\overline{TS}$ valid to BCLK (setup)	5		9		ns
47	BCLK to $\overline{TS}$ invalid (hold)	2		2		ns
49	BCLK to $\overline{BB}$ high impedance (68040 assumes bus mastership)		9		9	ns
51	$\overline{RSTI}$ valid to BCLK	5		4		ns
52	BCLK to $\overline{RSTI}$ invalid	2		2		ns
53	Mode select setup to $\overline{RSTI}$ negated - Note 4	20		20		ns
54	$\overline{RSTI}$ negated to mode selects invalid - Note 4	2		2		ns

Note 1 : All testing to be performed using worst-case test conditions unless otherwise specified.

Note 2 : The following pins are active low : $\overline{AVEC}$, $\overline{BG}$, $\overline{BS}$, $\overline{BR}$, $\overline{CDIS}$, $\overline{CIOUT}$, $\overline{IPEND}$, $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{MDIS}$, $\overline{MI}$, $\overline{RST0}$, $\overline{RSTI}$, $\overline{TA}$, $\overline{TBI}$, $\overline{TCI}$, $\overline{TEA}$, $\overline{TIP}$, $\overline{TRST}$, $\overline{TS}$ and $\overline{W}$ of R/$\overline{W}$.

Note 3 : Maximum operating junction temperature (T_J) = + 125°C. Minimum case operating temperature (T_C) = – 55°C. This device is not tested at T_C = + 125°C. Testing is performed by setting the junction temperature T_J = + 125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Note 4 : The levels on $\overline{CDIS}$, $\overline{MDIS}$, and the $\overline{IPL2}$-$\overline{IPL0}$ signals enable or disable the multiplexed bus mode, data latch enable mode, and driver impedance selection respectively.

5

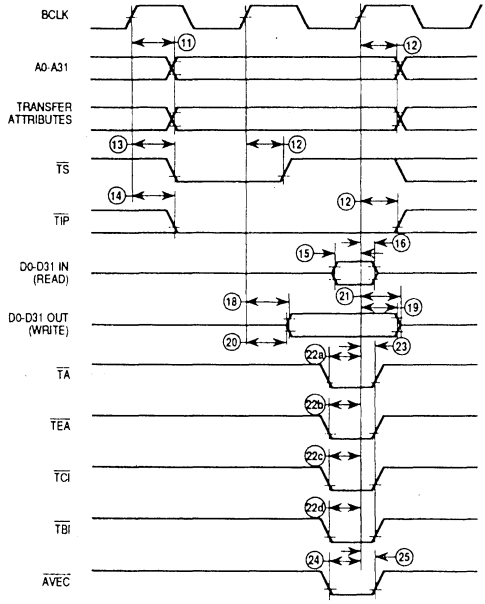


Figure 9 : Read / write timing.

Note : Transfer attribute signals UPAN, SIZN, TTN, TMN, TLNN, R/$\overline{W}$, $\overline{LOCK}$, $\overline{LOCKE}$, $\overline{CIOUT}$

Table 16 - JTAG timing application (Figures 16 - 19)
$-55°C \leq T_C \leq T_{Jmax}$; $4.75\ V \leq V_{CC} \leq 5.25\ V$ unless otherwise specified - Notes 1 and 2

Num	Characteristic	Min.	Max.	Unit
	TCK frequency	0	10	MHz
1	TCK cycle time	100		ns
2	TCK clock pulse width measured at 1.5 V	40		ns
3	TCK rise and fall times	0	10	ns
4	$\overline{TRST}$ setup time to TCK falling edge	40		ns
5	$\overline{TRST}$ assert time	100		ns
6	Boundary scan input data setup time	50		ns
7	Boundary scan input data hold time	50		ns
8	TCK to output data valid	0	50	ns
9	TCK to output high impedance	0	50	ns
10	TMS, TDI data setup time	20		ns
11	TMS, TDI data hold time	5		ns
12	TCK to TDO data valid	0	20	ns
13	TCK to TDO high impedance	0	20	ns

Note 1 : All testing to be performed using worst-case test conditions unless otherwise specified.

Note 2 : Maximum operating junction temperature (T_J) = + 125°C. Minimum case operating temperature (T_C) = – 55°C. This device is not tested at T_C = + 125°C. Testing is performed by setting the junction temperature T_J = + 125°C and allowing the case and ambient temperatures to rise and fall as necessary so as not to exceed the maximum junction temperature.

Table 17 - Boundry scan instruction codes

Bit 2	Bit 1	Bit 0	Instruction selected	Test data register accessed
0	0	0	Extest	Boundry scan
0	0	1	Highz	Bypass
0	1	0	Sample / preload	Boundry scan
0	1	1	DRVCTLT	Boundry scan
1	0	0	Shutdown	Bypass
1	0	1	Private	Bypass
1	1	0	DRVCTLS	Boundry scan
1	1	1	Bypass	Bypass

5.4 - Switching test circuit and waveforms

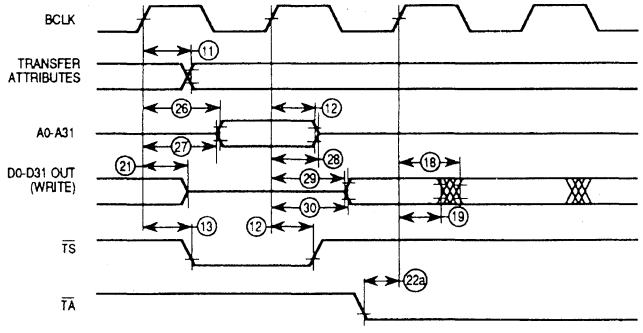


Figure 10 : Address and data bus timing. Multiplexed bus mode.

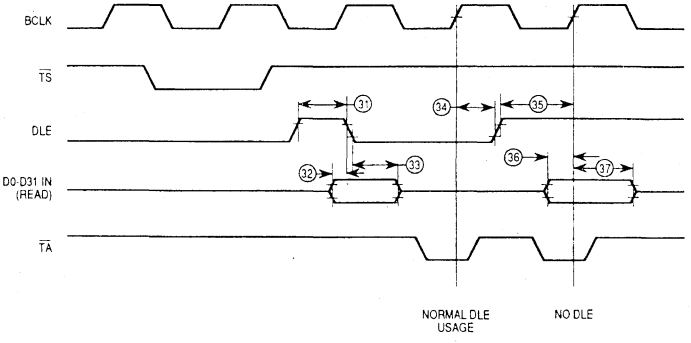


Figure 11 : DLE timing burst access.

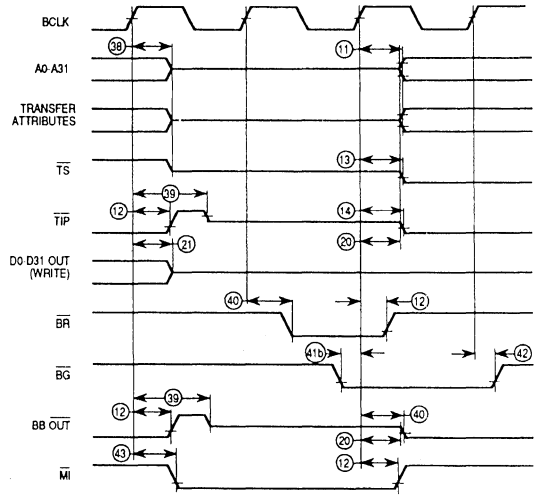


Figure 12 : Bus arbitation timing.

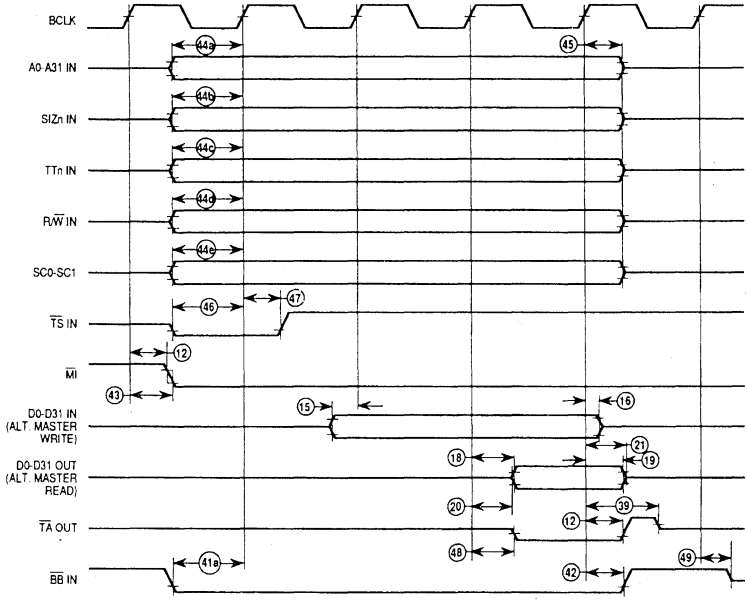


Figure 13 : Snoop hit timing.

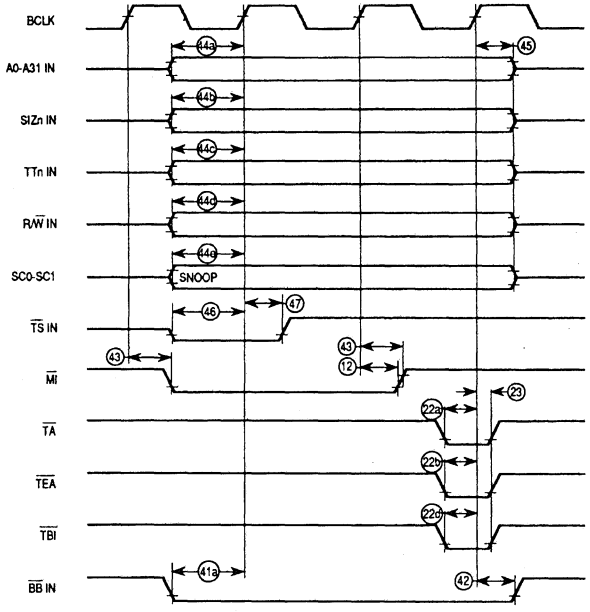


Figure 14 : Snoop miss timing.

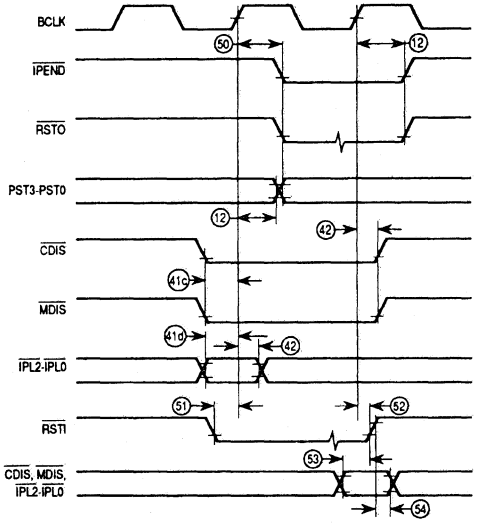


Figure 15 : Other signal timing.

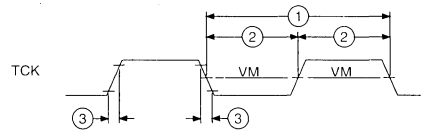


Figure 16 : Clock input timing diagram.

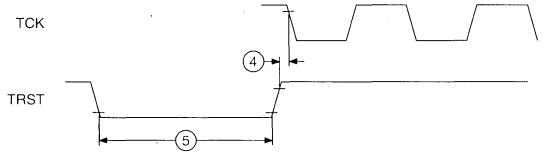


Figure 17 : $\overline{\text{TRST}}$ timing diagram.

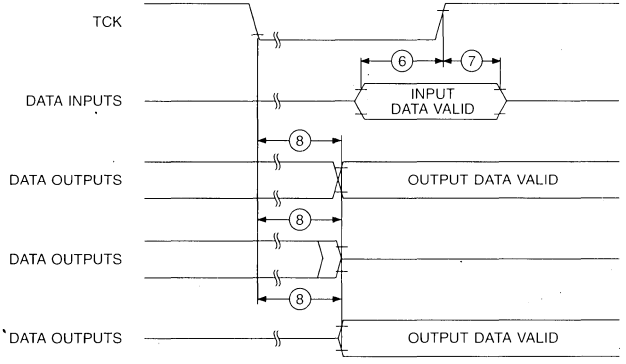


Figure 18 : Boundry scan timing diagram.

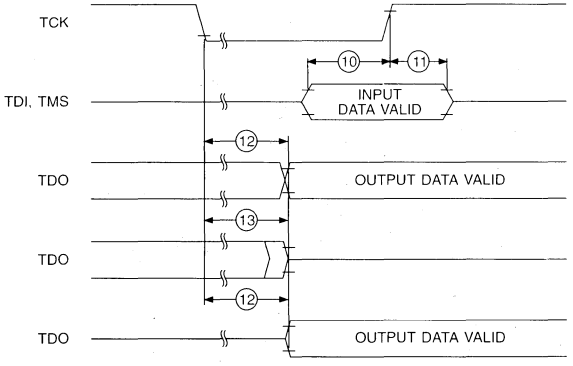


Figure 19 : Test access port timing diagram.

6 - FUNCTIONAL DESCRIPTION

6.1 - Programming model

The TS 68040 integrates the functions of the integer unit, MMU, and FPU. As shown in Figure 20, the registers depicted in the programming model provide access and control for the three units. The registers are partitioned into two levels of privilege : user and supervisor. User programs, executing in the user mode, can only use the resources of the user model. System software, executing in the supervisor mode, has unrestricted access to all processor resources.

The integer portion of the user programming model, consisting of 16, general-purpose, 32-bit registers and two control registers, is the same as the user programming model of the TS 68030. The TS 68040 user programming model also incorporates the TS 68882 programming model consisting of eight, floating-point, 80-bit data registers, a floating-point control register, a floating-point status register, and a floating-point instruction address register.

The supervisor programming model is used exclusively by TS 68040 system programmers to implement operating system functions, I/O control, and memory management subsystems. This supervisor / user distinction in the TS 68000 architecture was carefully planned so that all application software can be written to execute in the nonprivileged user mode and migrate to the TS 68040 from any TS 68000 platform without modification. Since system software is usually modified by system designers when porting to a new design, the control features are properly placed in the supervisor programming model. For example, the transparent translation registers of the TS 68040 can only be read or written by the supervisor software ; the programming resources of user application programs are unaffected by the existence of the transparent translation registers

Registers D0-D7 are data registers containing operands for bit and bit field (1 to 32 bits), byte (8 bit), word (16 bit), long-word (32 bit), and quad-word (64 bit) operations. Registers A0-A6 and the stack pointer registers (user, interrupt, and master) are address registers that may be used as software stack pointers or base address registers. Register A7 is the user stack pointer in user mode, and is either the interrupt or master stack pointer (A7' or A7") in supervisor mode. In supervisor mode, the active stack pointer (interrupt or master) is selected based on a bit in the status register (SR). The address registers may be used for word and long-word operations, and all of the 16 general-purpose registers (D0-D7, A0-A7 in Figure 20) may be used as index registers.

The eight, 80-bit, floating-point data registers (FP0-FP7) are analogous to the integer data registers (D0-D7) of all TS 68000 Family processors. Floating-point data registers always containt extended-precision numbers. All external operands, regardless of the data format, are converted to extended-precision values before being used in any floating-point calculation or stored in a floating-point data register.

The program counter (PC) usually contains the address of the instruction being executed by the TS 68040. During instruction execution and exception processing, the processor automatically increments the contents of the PC or places a new value in the PC, as appropriate. The status register (SR in the supervisor programming model) contains the condition codes that reflect the results of a previous operation and can be used for conditional instruction execution in a program. The lower byte of the SR is accessible in user mode as the condition code register (CCR). Access to the upper byte of the SR is restricted to the supervisor mode.

As part of exception processing, the vector number of the exception provides an index into the exception vector table. The base address of the exception vector table is stored in the vector base register (VBR). The displacement of an exception vector is added to the value in the VBR when the TS 68040 accesses the vector table during exception processing.

Alternate function code registers, SFC and DFC (source and destination), contain 3-bit function codes. Function codes can be considered extensions of the 32-bit linear address. Function codes are automatically generated by the processor to select address spaces for data and program accesses at the user and supervisor modes. The alternate function code registers are used by certain instructions to explicitly specify the function codes for various operations. The cache control register (CACR) controls enabling of the on-chip instruction and data caches of the TS 68040.

The supervisor root pointer (SRP) and user root pointer (URP) registers point to the root of the address translation table tree to be used for supervisor mode and user mode accesses. The URP is used if FC2 of the logical address is zero, and the SRP is used if FC2 is one.

The translation control register (TC) enables logical-to-physical address translation and selects either 4K or 8K page sizes. As shown in Figure 20, there are four transparent translation registers - ITT0 and ITT1 for instruction accesses and DTT0 and DTT1 for data accesses. These registers allow portions of the logical address space to be transparently mapped and accessed without the use of resident descriptors in an ATC. The MMU status register (MMUSR) contains status information from the execution of a PTEST instruction. The PTEST instruction searches the translation tables for the logical address as specified by this instruction's effective address field and the DFC.

The 32-bit floating-point control register (FPCR) contains an exception enable byte that enables disables traps for each class of floating-point exceptions and a mode byte that sets the user-selectable modes. The FPCR can be read or written to by the user and is cleared by a hardware reset or a restore operation of the null state. When cleared, the FPCR provides the IEEE 754 standard defaults. The floating-point status register (FPSR) contains a condition code byte, quotient bits, an exception status byte, and an accrued exception byte. All bits in the FPSR can be read or written by the user. Execution of most floating-point instructions modifies this register.

For the subset of the FPU instructions that generate exception traps, the 32-bit floating-point instruction address register (FPIAR) is loaded with the logical address of an instruction before the instruction is executed. This address can then be used by a floating-point exception handler to locate a floating-point instruction that has caused an exception. The move floating-point data register (FMOVE) instruction (to from the FPCR, FPSR, or FPIAR) and the move multiple data registers (FMOVEN) instruction cannot generate floating-point exceptions ; therefore, these instructions do not modify the FPIAR. Thus, the FMOVE and FMOVEM instructions can be used to read the FPIAR in the trap handler without changing the previous value.

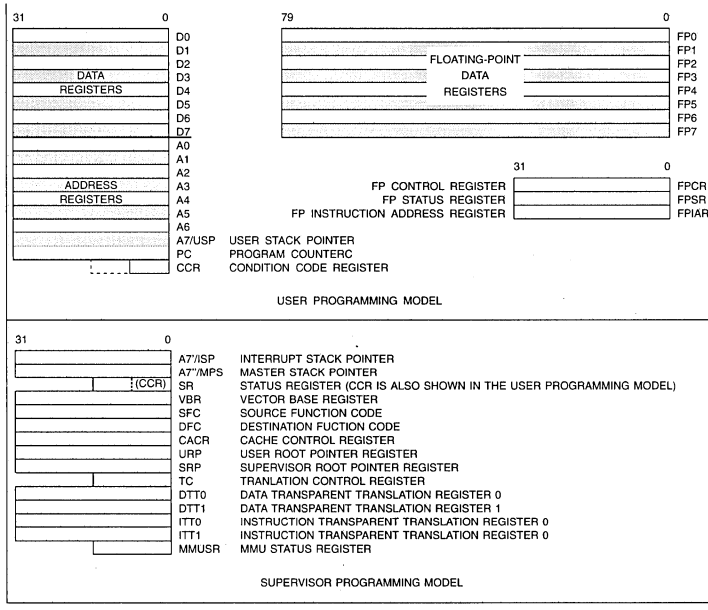


Figure 20 : Programming model.

6.2 - Data types and addressing modes

The TS 68040 supports the basic data types shown in Table 18. Some data types apply only to the integer unit, some only to the FPU, and some to both the integer unit and the FPU. In addition, the instruction set supports operations on other data types such as memory addresses.

Table 18 - Data types

Operand data type	Size	Execution unit (IU*, FPU)	Notes
Bit	1 bit	IU	
Bit field	1-32 bits	IU	Field of consecutive bits
BCD	32 bits	IU	Packaged : 2 digits byte Unpacked : 1 digit byte
Byte integer	8 bits	IU, FPU	
Word integer	16 bits	IU, FPU	
Long-word integer	32 bits	IU, FPU	
Quad-word integer	64 bits	IU	Any two data registers
16 byte	128 bits	IU	Memory-only, aligned 16-byte boundary
Single-precision real	32 bits	FPU	1-bit sign, 8-bit exponent, 23-bit mantissa
Double-precision real	64 bits	FPU	1-bit sign, 11-bit exponent, 52-bit mantissa
Extended-precision real	80 bits	FPU	1-bit sign, 15-bit exponent, 64-bit mantissa
* IU = Integer unit.			

The three integer data formats that are common to both the integer unit and the FPU (byte, word, and long word) are the standard twos-complement data formats defined in the TS 68000 Family architecture. Whenever an integer is used in a floating-point operation, the integer is automatically converted by the FPU to an extended-precision floating-point number before being used. The ability to effectively use integers in floating-point operations saves user memory because an integer representation of a number usually requires fewer bits than the equivalent floating-point representation.

Single- and double-precision floating-point data formats are implemented in the FPU as defined by the IEEE standard. These data formats are the main floating-point formats and should be used for most calculations involving real numbers.

The extended-precision data format is also in conformance with the IEEE standard, but the standard does not specify this format to the bit level as it does for single- and double-precision. The memory format for the FPU consists of 96 bits (three long words). Only 80 bits are actually used ; the other 16 bits are reserved for future use and for long-word alignment of the floating-point data structures in memory. The extended-precision format has a 15-bit exponent, a 64-bit mantissa, and a 1-bit mantissa sign. Extended-precision numbers are intended for use as temporary variables, intermediate values, or where extra precision is needed.

The TS 68040 addressing modes are shown in Table 19. The register indirect addressing modes support post-increment, predecrement, offset, and indexing, which are particularly useful for handling data structures common to sophisticated applications and high-level languages. The program counter indirect mode also has indexing and offset capabilities ; this addressing mode is typically required to support position-independent software. In addition to these addressing modes, the TS 68040 provides index sizing and scaling features that enhance software performance. Data formats are supported orthogonally by all arithmetic operations and by all appropriate addressing modes.

Table 19 - Addressing modes

Addressing modes	Syntax
Register direct	
Date register direct	Dn
Address register direct	An
Register indirect	
Address register indirect	(An)
Address register indirect with postincrement	(An)
Address register indirect with predecrement	(An)
Address register indirect with displacement	(d_{16}, An)
Register indirect with index	
Address register indirect with index (8-bit displacement)	(d_8, An, Xn)
Address register indirect with index (base displacement)	(bd, An, Xn)
Memory indirect	
Memory indirect postincrement	([bd, An], Xn, od)
Memory indirect preindexed	([bd, An, Xn], od)
Program counter indirect with displacement	(d_{16}, PC)
Program counter indirect with index	
PC indirect with index (8-bit displacement)	(d_8, PC, Xn)
PC indirect with index (base displacement	(bd, PC, Xn)
Program counter memory indirect	
PC memory indirect postindexed	([bd, PC], Xn, od)
PC memory indirect preindexed	([bd, PC, Xn], od)
Absolute	
Absolute short	xxx.W
Absolute long	xxx.L
Immediate	# (data)

Notes :

DN = Data register, D0-D7
AN = Address register, A0-A7
d_8, d_{16} = A twos-complement or sign-extended displacement ; added as part of the effective address calculation ; size is 8 (d_8) or 16 (d_{16}) bits ; when omitted, assemblers use a value of zero.
Xn = Address or data register used as an index register ; form is Xn, SIZE*SCALE, where SIZE is W or L (indicates index register size) and SCALE is 1, 2, 4 or 8 (index register os multiplied by SCALE) ; use of SIZE and or SCALE is optional.
bd = A twos-complement base displacement ; when present, size can be 16 or 32 bits.
od = Outer displacement added as part of effective address calculation after any memory indirection ; use is optional with a size of 16 or 32 bits.
PC = Program counter.
(data) = Immediate value of 8, 16 or 32 bits.
( ) = Effective address.
[ ] = Used as indirect address to long-word address.

6.3 - Instruction set overview

The instruction provided by the TS 68040 are listed in Table 20. The instruction set has been tailored to support high-level languages and is optimized for those instructions most commonly executed (however, all instructions listed are fully supported). Many instructions operate on bytes, words, and long words, and most instructions can use any of the addressing modes of Table 19.

Table 20 - Instruction set summary

Mnemonic	Description
ABCD	Add decimal with extend
ADD	Add
ADDA	Add address
ADDI	Add immediate
ADDQ	Add quick
ADDX	Add with extend
AND	Logical AND
ANDI	Logical AND immediate
ASL, ASR	Arithmetic shift left and right
Bcc	Branch conditionally
BCHG	Test bit and change
BCLR	Test bit and clear
BFCHG	Test bit field and change
BFCLR	Test bit field and clear
BFEXTS	Signed bit field extract
BFEXTU	Unsigned bit field extract
BFFFO	Bit field find first one
BFINS	Bit field insert
BFSET	Test bit field and set
BFTST	Test bit field
BKPT	Breakpoint
BRA	Branch
BSET	Test bit and set
BSR	Branch to subroutine
BTST	Test bit
CAS	Compare and swap operands
CAS2	Compare and swap dual operands
CHK	Check register against bounds
CHK2	Check register against upper and lower bounds
*CINV	Invalidate cache entries
CLR	Clear
CMP	Compare
CMPA	Compare address
CMPI	Compare immediate
CMPM	Compare memory to memory
CMP2	Compare register against upper and lower bounds
*CPUSH	Push then invalidate cache entries
DBcc	Test condition, decrement and branch
DIVS, DIVSL	Signed divide
DIVU, DIVUL	Unsigned divide
EOR	Logical exclusive OR
EORI	Logical exclusive OR immediate
EXG	Exchange registers
EXT, EXTB	Sign extend
ILLEGAL	Take illegal instruction trap
JMP	Jump
JSR	Jump to subroutine
LEA	Load effective address
LINK	Link and allocate
LSL, LSR	Logical Shift left and right
MOVE	Move
*MOVE16	16-byte block move
MOVEA	Move address
MOVE CCR	Move condition code register
MOVE SR	Move status register
MOVE USP	Move user stack pointer
*MOVEC	Move control register
MOVEM	Move multiple registers
MOVEP	Move peripheral
MOVEQ	Move quick
*MOVES	Move alternate address space
MULS	Signed multiply
MULU	Unsigned multiply
NBCD	Negate decimal with extend
NEG	Negate
NEGX	Negate with extend
NOP	No operation
NOT	Logical complement
OR	Logical inclusive OR
ORI	Logical inclusive OR immediate
PACK	Pack BCD
PEA	Push effective address
*PFLUSH	Flush entry(ies) in the ATCs
*PTEST	Test a logical address
RESET	Reset external devices
ROL, ROR	Rotate left and right
ROXL, ROXR	Rotate with extend left and right
RTD	Return and deallocate
RTE	Return from exception
RTR	Return and restore codes
RTS	Return from subroutine
SBCD	Substract decimal with extend
Scc	Set conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract address
SUBI	Subtract immediate
SUBQ	Subtract quick
SUBX	Subtract with extend
SWAP	Swap register words
TAS	Test operand and set
TRAP	Trap
TRAPcc	Trap conditionally
TRAPV	Trap on overflow
TST	Trap operand
UNLK	Unlink
UNPK	Unpack BCD

* TS 68040 additions or alterations to the TS 68030 and TS 68881 / TS 68882 instruction sets.

Table 21 - Floating-point instructions

Mnemonic	Description
*FABS	Floating-point absolute value
*FADD	Floating-point add
FBcc	Branch on floating-point condition
FCMP	Floating-point compare *
FDBcc	Floating-point decrement and branch
*FDIV	Floating-point divide
*FMOVE	Move floating-point register
FMOVEM	Move multiple floating-point registers
*FMUL	Floating-point multiply
*FNEG	Floating-point negate
FRESTORE	Restore floating-point internal state
FSAVE	Save floating-point internal state
FScc	Set according to floating-point condition
*FSQRT	Floating-point Square Root
*FSUB	Floating-point substract
FTRAPcc	Trap on floating-point condition
FTST	Floating-point test

* TS 68040 additions or alterations to the TS 68030 and TS 68881 / TS 68882 instruction sets.

The TS 68040 floating-point instructions, a commonly used subset of the TS 68882 instruction set, are implemented in hardware. The remaining unimplemented instructions are less frequently used and are efficiently emulated in software, maintaining compatibility with the TS 68881 / TS 68882 floating-point coprocessors.

The TS 68040 instruction set includes MOVE16, a new user instruction that allows high-speed transfers of 16-byte blocks between external devices such as memory to memory or coprocessor to memory.

6.4 - Instruction and data caches

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the TS 68000 Family took advantage of this locality of reference phenomenon to varying degrees. The TS 68040 takes further advantage of cache technology with its two, independent, on-chip, physical address space caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the TS 68040 yield a very high hit rate, providing a substantial increase in system performance. Additionally, the caches are automatically burstfilled from the external bus whenever a cache miss occurs.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and a third external access to occur simultaneously with instruction execution. For example, if the TS 68040 requires both an instruction-stream access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and if it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The parallelism inherent in the TS 68040 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

6.4.1 - Cache organization

The instruction and data caches are four-way set-associative with 64 sets of four, 16-byte lines for a total cache storage of 4K bytes each. As shown in Figure 21, each 16-byte line contains an address tag and state information. State information for each entry consists of a valid flag for the entire line in both instruction and data caches and write status for each long word in the data cache. The write status in the data cache signifies whether or not the long-word data is dirty (meaning that the data in the cache has been modified but has not been written back to external memory) for data in copyback pages.

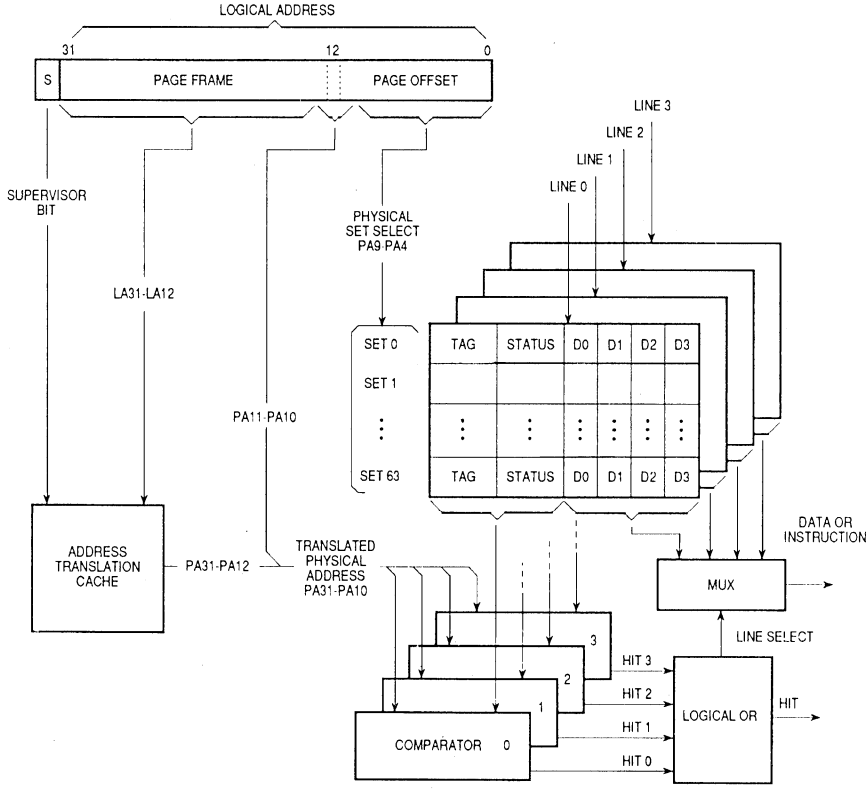


Figure 21 : Cache organization overview.

The caches are accessed by physical addresses from the on-chip MMUs. The translation of the upper bits of the logical address occurs concurrently with the accesses into the set array in the cache by the lower address bits. The output of the ATC is compared with the tag field in the cache to determine if one of the lines in the selected set matches the translated physical address. If the tag matches and the entry is valid, then the cache has a hit.

If the cache hits and the access is a read, the appropriate long word from the cache line is multiplexed onto the appropriate internal bus. If the cache hits and the access is a write, the data, regardless of size, is written to the appropriate portion of the corresponding longword entry in the cache.

When a data cache miss occurs and a previously valid cache line is needed to cache the new line, any dirty data in the old line will be internally buffered and copied back to memory after the new cache line has been loaded.

Pushing of dirty data can be forced by the CPUSH instruction.

Cachability of data in each memory page is controlled by two bits in the page descriptor for each page. Cachable pages may be either writethrough or copyback, with no write-allocate for misses to writethrough pages. Non-cachable pages may also be specified as noncachable I O, forcing accesses to these pages to occur in order of instruction execution.

6.4.2 - Cache coherency

The TS 68040 has the ability to snoop the external bus during accesses by other bus masters to maintain coherency between the TS 68040's caches and external memory systems. External write cycles are snooped by both the instruction cache and data cache ; whereas, external read cycles are snooped only by the data cache. In addition, external cycles can be flagged on the bus as snoopable or nonsnoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches for a coherency conflict based on the state of the corresponding cache line and the type of external cycle.

Although the internal execution units and the bus snooper circuit all have access to the on-chip caches, the snooper has priority over the execution units to allow the snooper to resolve coherency discrepancies immediately.

6.4.3 - Cache instructions

The TS 68040 supports the following instructions for cache maintenance. Both instructions may selectively operate on the data or instruction cache.

CINV : Invalidates a single line, all lines in a physical page, or the entire cache.

CPUSH : Pushes selected dirty data cache lines to memory, then invalidates all selected lines.

6.5 - Operand transfer mechanisms

The TS 68040 external synchronous bus supports multiple masters and overlaps arbitration with data transfers. The bus is optimized to perform high-speed transfers to and from an external cache or memory. The data and address buses are each 32 bits wide.

6.5.1 - Transfer types

The TS 68040 provides two signals (TT1-TT0) that define four types of bus transfers : normal access, MOVE16 access, alternate access, and interrupt acknowledge access. Normal accesses identify normal memory references : MOVE16 accesses are memory accesses by a MOVE16 instruction ; and alternate accesses identify accesses to the undefined address spaces (function code values of 0, 3, 4, 7). The interrupt acknowledge access is used to fetch an interrupt vector during interrupt exception processing.

6.5.2 - Burst transfer operation

During burst read write to cache transfers, the values on the address and transfer type signals do not change ; they are the address of the first requested item of the cache line. When the TS 68040 request a burst read transfer of a cache line, the address bus indicates the address of the long word in the line needed first, but the memory system is expected to provide data in the following order (modulo 4) : 0, 1, 2, 3 (long-word offsets). The first address needed may not be from offset 0 ; nevertheless, all four long words must be transferred. Burst writes occur in a similar manner.

6.5.3 - Bus snooping

Bus snooping ensures that data in main memory is consistent with data in the on-chip caches. If an alternate bus master is performing a read transfer on the bus and snooping is enabled, and if the snoop logic determines that the on-chip data cache has dirty data (data valid but not consistent with memory) for this transfer, ther memory is prevented from responding to the read request, and the TS 68040 supplies the data directly to the master. If the alternate master is performing a write transfer on the bus and snooping is enabled, and if the snooper determines that one of the on-chip caches has a valid line for this request, then the snooper may either invalidate or update the line as selected by the snoop control signals.

6.6 - Exception processing

The TS 68040 provides the same extensions to the exception stacking process as the TS 68030. If the M bit in the status register is set, the master stack pointer is used for all task-related exceptions. When a nontask-related exception occurs (i.e., an interrupt), the M bit is cleared, and the interrupt stack pointer is used. This feature allows a task's stack area to be carried within a single processor control block, and new tasks may be initiated by simply reloading the master stack pointer and setting the M bit.

The externally generated exceptions are interrupts, bus errors, and reset conditions. The interrupts are requests from external devices for processor action ; whereas, the bus error and reset signals are used for access control and processor initialization. The internally generated exceptions come from instructions, address errors, tracing, or breakpoints. The TRAP, TRAPcc, TRAPVcc, FTRAPcc, CHK, CHK2, and DIV instructions can all generate exceptions as part of their instruction execution. Tracing behaves like a very high-priority, internally generated interrupt whenever it is processed. The other internally generated exceptions are caused by unimplemented floating-point instructions, illegal instructions, instruction fetches from odd addresses, and privilege violations. Finally, the MMU can generate exceptions, for access violations and for when invalid descriptors are encountered during table searches.

Exception processing for the TS 68040 occurs on the following sequence :

1 - an internal copy is made of the status register,

2 - the vector number of the exception is determined,

3 - current processor status is saved,

4 - the exception vector offset is determined by multiplying the vector number by four.

This offset is then added to the contents of the VBR to determine the memory address of the exception vector. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execition is started.

6.7 - Memory management units

The full addressing range of the TS 68040 is 4 Gbytes (4,294,967,296 bytes). However, most TS 68040 systems implement a much smaller physical memory. Nonethless, by using virtual memory techniques, the system can be made to appear to have a full 4 Gbytes of physical memory available to each user program. The independent instruction and data MMUs fully support demandpaged virtual-memory operating systems with either 4K or 8K page sizes. In addition to its main function of memory management, each MMU protects supervisor areas from accesses by user programs and also provides write protection on a page-by-page basis. For maximum efficiency, each MMU operates in parallel with other processor activities.

6.7.1 - Translation mechanism

Because logical-to-physical address translation is one of the most frequently executed operations of the TS 68040 MMUs, this task has been optimized. Each MMU initiates address translation by searching for a descriptor containing the address translation information in the ATC. If the descriptor does not reside in the ATC, then the MMU performs external bus cycles via the bus controller to search the translation tables in physical memory. After being located, the page descriptor is loaded into the ATC, and the address is correctly translated for the access, provided no exception conditions are encountered.

6.7.2 - Address translation cache

An integral part of the translation function previously described is the dual cache memory that stores recently used logical-to-physical address translation information (page descriptors) for instruction and date accesses. These caches are 64-entry, four-way, set associative. Each ATC compare the logical address of the incoming access against its entries. If one of the entries matches, there is a hit, and the ATC sends the physical address to the bus controller, which then starts the external bus cycle (provided there was no hit in the corresponding cache for the access).

6.7.3 - Translation tables

The translation tables of the TS 68040 have a threelevel tree structure and reside in main memory. Since only a portion of the complete tree needs to exist at any one time, the tree structure minimizes the amount of memory necessary to set up the tables for most programs. As shown in Figure 20, either the user root pointer or the supervisor root pointer points to the first level table, depending on the values of the function code for an access. Table entries at the second level of the tree (pointer tables) contain pointers to the third level (page tables). Entries in the page tables contain either page descriptors or indirect pointers to page descriptors. The mechanism for performing table search operations uses portions of the logical address (as indices) at each level of the search. All addresses in the translation table entries are physical addresses.

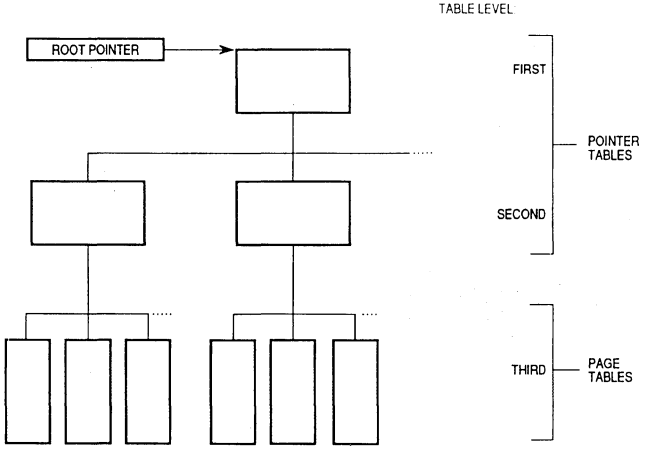


Figure 22 : Translation table structure.

There are two variations of table searches for both 4K and 8K page sizes : normal searches and indirect searches. An indirect search differs in that the entry in the third level page table contains a pointer to a page descriptor rather than the page descriptor itself.

Entries in the translation tables contain control and status information on addition to the physical address information. Control bits specify write protection, limit access to supervisor only, and determine cachability of data in each memory page. Each page descriptor also has two user-programmable bits that appear on the UPA0 and UPA1 signals during an external access for use as address modifier bits.

A global bit can be set in each page descriptor to prevent flushing of the ATC entry for that page by some PFLUSH instruction variants, allowing system ATC entries to remain resident during task swaps. If these special PFLUSH instructions are not used, this bit can be user defined. The MMUs automatically maintain access history information for the pages by updating the used (U) and modified (M) status bits.

6.7.4 - MMU instructions

The MMU instructions supported by the TS 68040 are as follows :

PFLUSH : Allows flushing of either selected ATC entries by function code and logical address or the entire ATCs.

PTEST : Takes an address and function code and searches the translation tables for the corresponding entry, which is then loaded into the ATC. The results of the search are available in the MMU status register and are often useful in determining the cause of a fault.

All of the TS 68040 MMU instructions are privileged and can only be executed from the supervisor mode.

6.7.5 - Transparent translation

Four transparent translation registers, two each for instruction and data accesses, have been provided on the TS 68040 MMU to allow portions of the logical address space to be transparently mapped and accessed without the need for corresponding entries resident in the ATC. Each register can be used to define a range of logical addresses from 16 Mbytes to 4 Gbytes with a base address and a mask. All addresses within these ranges are not mapped, and are optionally protected against user or supervisor accesses and write accesses. Logical addresses in these areas become the physical addresses for memory access. The transparent translation feature allows rapid movement of large blocks of data in memory or I/O space without disturbing the context of the on-chip ATCs or incurring delays associated with translation table searches.

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or TCS standard.

7.2 - Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or TCS standard and guarantying the parameters not tested at temperature extremes for the entire temperature range.

8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

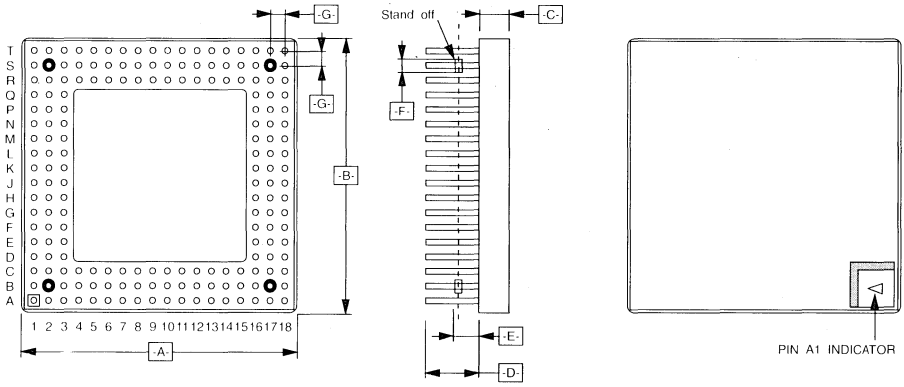
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 percent if practical.

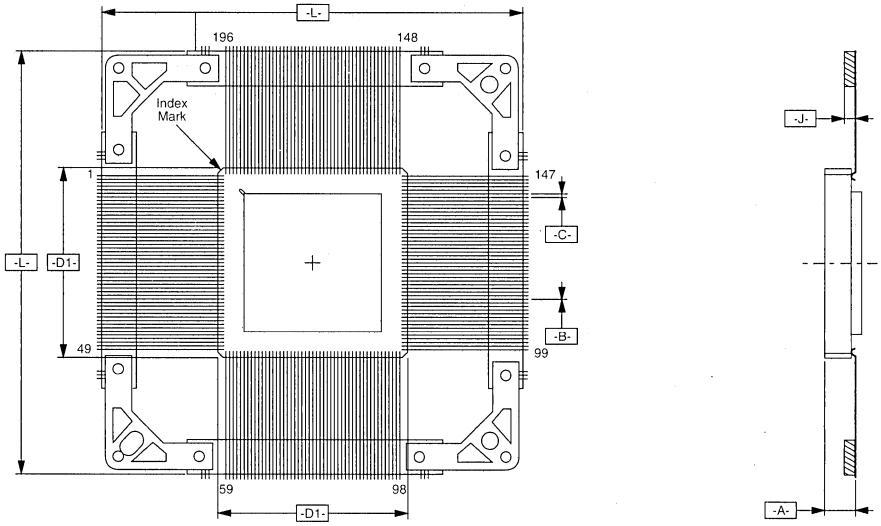
9 - PACKAGE MECHANICAL DATA

9.1 - 179 pins - PGA



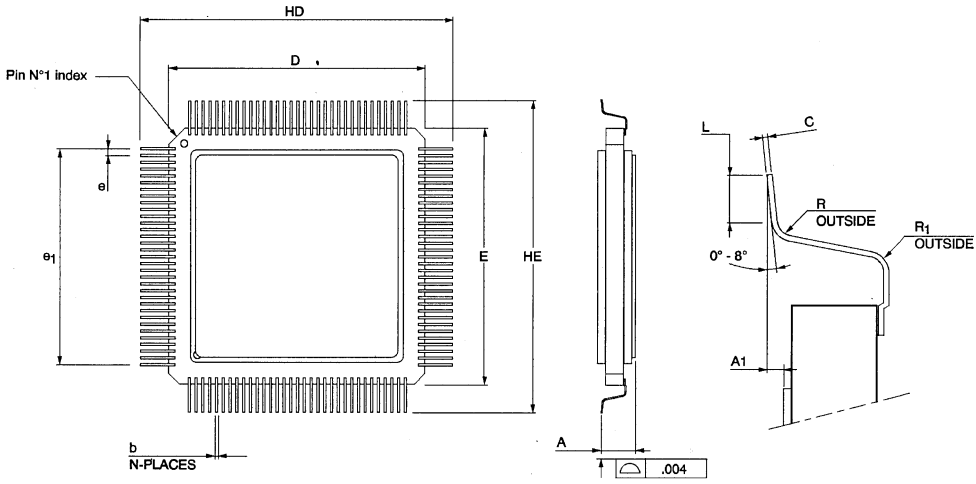
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	46.863	47.625	1.845	1.875
B	46.863	47.625	1.845	1.875
C	2.3876	1.875	0.094	0.116
D	4.318	4.826	0.170	0.190
E	1.143	1.4	0.045	0.055
F	1.143	1.4	0.045	0.055
G	2.54 BSC		0.100 BSC	

9.2 - 196 pins - Tie bar CQFP cavity up (on request)



Dim	Millimeters	Inches
A	3.30 max	0.130 max
B	$0.23^{+0.05}_{-0.038}$	$.009^{+.002}_{-.015}$
C	0.635 typ.	.025 typ.
D1	33.91 ± 0.25	$1.335 \pm .01$
J	0.89 ± 0.13	$.035 \pm .005$
L	63.5 ± 0.51	$2.5 \pm .02$

9.3 - 196 pins - Gullwing CQFP cavity up

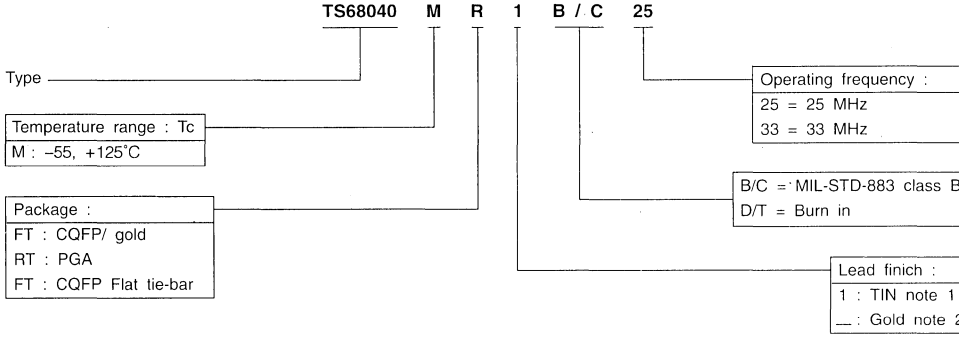


* Reduced pin count shown for clarity, 49 pins per side

Symbol	Millimeters	Inches
A	4.19 max	1.65 max
A1	$.673 \pm 0.2$	$.0265 \pm .008$
b	$.23 \begin{matrix}+0.5 \\ -.038\end{matrix}$	$.009 \begin{matrix}+.002 \\ -.0015\end{matrix}$
c	$.127 \begin{matrix}+.05 \\ -.025\end{matrix}$	$.005 \begin{matrix}+.002 \\ -.001\end{matrix}$
D/E	33.91 ± 0.25	1.335 ± 0.1
e	.635 BSC	.025 BSC
e1	30.48 ± 0.13	$1.2 \pm .005$
HD/HE	38.8 ± 0.18	$1.528 \pm .007$
L	0.813 ± 0.2	$.032 \pm .008$
N	196	196
R	0.55 ± 0.25	$.022 \pm .01$
R1	0.23 min	.009 min

10 - ORDERING INFORMATION

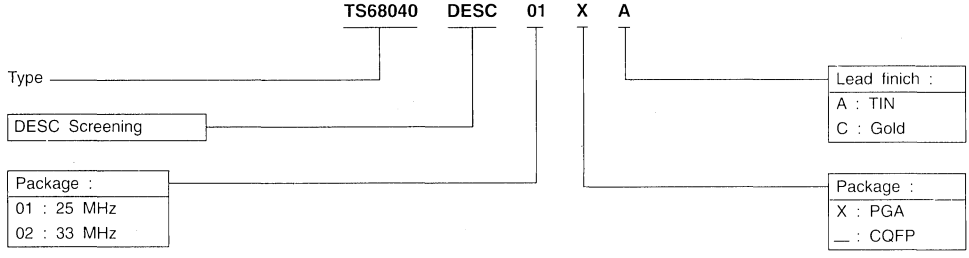
10.1 - MIL-STD-883 C



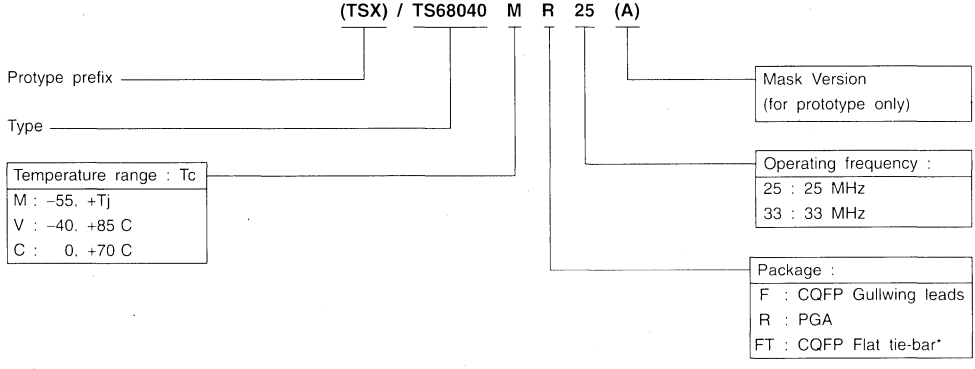
Note 1 : On request.

Note 2 : Standard process.

10.2 - DESC Drawing 5962-93143



10.3 - Standard product



* On request/ small quantity.

10.4 - Detailed TS 68040 part list

10.4.1 - Hi-REL product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68040MRB/C25	MIL-STD-883	PGA 179	– 55 / + T_J	25	TCS data sheet
TS68040MRB/C33	MIL-STD-883	PGA 179	– 55 / + T_J	33	TCS data sheet
TS68040MFB/C25	MIL-STD-883	CQFP 196	– 55 / + T_J	25	TCS data sheet
TS68040MFB/C33	MIL-STD-883	CQFP 196	– 55 / + T_J	33	TCS data sheet
TS68040DESC01XA	DESC	PGA 179	– 55 / + T_J	25	5962-9314301MXA
TS68040DESC02XA	DESC	PGA 179	– 55 / + T_J	33	5962-9314302MXA
TS68040DESC01XC	DESC	PGA 179	– 55 / + T_J	25	5962-9314301MXC
TS68040DESC02XC	DESC	PGA 179	– 55 / + T_J	33	5962-9314302MXC
TS68040DESC01YC	DESC	CQFP 196	– 55 / + T_J	25	5962-9314301MYC
TS68040DESC02YC	DESC	CQFP 196	– 55 / + T_J	33	5962-9314302MYC
TS68040MFB/C25	MIL-STD-883	CQFP 196	– 55 / + T_J	25	TCS data sheet
TS68040MFB/C33	MIL-STD-883	CQFP 196	– 55 / + T_J	33	TCS data sheet
TS68040MRD/T25	BURN IN	PGA 179	– 55 / + T_J	25	TCS data sheet
TS68040MRD/T33	BURN IN	PGA 179	– 55 / + T_J	33	TCS data sheet
TS68040MFD/T25	BURN IN	CQFP 196	– 55 / + T_J	25	TCS data sheet
TS68040MFD/T33	BURN IN	CQFP 196	– 55 / + T_J	33	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

10.4.2 - Standard product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TSX68040VR25	TCS standard	PGA 179	– 40 / + T_J	25	TCS data sheet
TSX68040VR33	TCS standard	PGA 179	– 40 / + T_J	33	TCS data sheet
TSX68040MR25	TCS standard	PGA 179	– 55 / + T_J	25	TCS data sheet
TSX68040MR33	TCS standard	PGA 179	– 55 / + T_J	33	TCS data sheet
TSX68040VF25	TCS standard	CQFP 196	– 40 / + T_J	25	TCS data sheet
TSX68040VF33	TCS standard	CQFP 196	– 40 / + T_J	33	TCS data sheet
TSX68040MF25	TCS standard	CQFP 196	– 55 / + T_J	25	TCS data sheet
TSX68040MF33	TCS standard	CQFP 196	– 55 / + T_J	33	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

CMOS ENHANCED FLOATING-POINT COPROCESSOR

DESCRIPTION

The TS 68882 enhanced floating-point coprocessor is a full implementation of the IEEE Standard for Binary Floating-Point Arithmetic (754) for use with the THOMSON TS 68000 Family of microprocessors. It is a pin and software compatible upgrade of the TS 68881 with an optimized MPU interface that provides over 1.5 times the performance of the TS 68881. It is implemented using VLSI technology to give systems designers the highest possible functionality in a physically small device.

Intended primarily for use as a coprocessor to the TS 68020/68030 32-bit microprocessor units (MPUs), the TS 68882 provides a logical extension to the main MPU integer data processing capabilities. It does this by providing a very high performance floating-point arithmetic unit and a set of floating-point data registers that are utilized in a manner that is analogous to the use of the integer data registers. The TS 68882 instruction set is a natural extension of all earlier members of the TS 68000 Family, and supports all of the addressing modes of the host MPU. Due to the flexible bus interface of the TS 68000 Family, the TS 68882 can be used with any of the MPU devices of the TS 68000 Family, and it may also be used as a peripheral to non-TS 68000 processors.

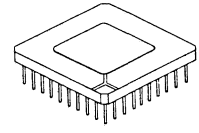
MAIN FEATURES

- Eight general purpose floating-point data registers, each supporting a full 80-bit extended precision real data format (a 64-bit mantissa plus a sign bit, and a 15-bit signed exponent).
- A 67-bit arithmetic unit to allow very fast calculations, with intermediate are precision greater than the extended precision format.
- A 67-bit barrel shifter for high-speed shifting operations (for normalizing etc.).
- Special purpose hardware for high-speed conversion between single, double, and extended formats and the internal extended format.
- An independent state machine to control main processor communication for pipelined instruction processing.
- Forty-six instructions, including 35 arithmetic operations.
- Full conformation to the IEEE 754 standard, including all requirements and suggestions.
- Support of functions not defined by the IEEE standard, including a full set of trigonometric and transcendental functions.
- Seven data types : byte, word and long integers ; single, double, and extended precision real numbers ; and packed binary coded decimal string real numbers.
- Twenty-two constants available in the on-chip ROM, including π, e, and powers of 10.
- Virtual memory / machine operations.
- Efficient mechanisms for procedure calls, context switches, and interrupt handling.
- Fully concurrent instruction execution with the main processor.
- Fully concurrent instruction execution of multiple floating-point instructions.
- Use with any host processor, on an 8-, 16- or 32-bit data bus.
- Available in 16.67, 20, 25 and 33 MHz for T_C from $-55°C$ to $+125°C$.
- $V_{CC} = 5\ V \pm 10\ \%$.

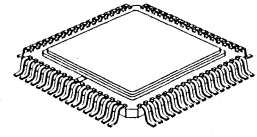
SCREENING / QUALITY

This product could be manufactured in full compliance with either :

- CECC 90110-024 (class B, assessment level Y).
- MIL-STD-883 class B.
- DESC 5962-89436.
- or according to TCS standards.



R suffix
PGA 68
Ceramic Pin Grid Array



F suffix
CQFP 68
Ceramic Quad Flat Pack

5

SUMMARY

A · GENERAL DESCRIPTION

1 · INTRODUCTION

The TS 68882 is a high performance floating-point device designed to interface with the TS 68020 or TS 68030 as a coprocessor. This device fully supports the TS 68000 virtual machine architecture, and is implemented in HCMOS, THOMSON's low power, small geometry process. This process allows CMOS and HMOS (high-density NMOS) gates to be combined on the same device. CMOS structures are used where speed and low power is required, and HMOS structures are used where minimum silicon area is desired. The HCMOS technology enables the TS 68882 to be very fast while consuming less power than comparable HMOS, and still have a reasonably small die size.

With some performance degradation, the TS 68882 can also be used as a peripheral processor in systems where the TS 68020 or TS 68030 is not the main processor (e.g., TS 68000, TS 68008, TS 68010). The configuration of the TS 68882 as a peripheral processor or coprocessor may be completely transparent to user software (i.e., the same object code may be executed in either configuration).

The architecture of the TS 68882 appears to the user as a logical extension of the TS 68000 Family architecture. Coupling of the coprocessor interface, allows the TS 68020 / TS 68030 programmer to view the TS 68882 registers as though the registers are resident in the TS 68020 / TS 68030. Thus, a TS 68020 or TS 68030 / TS 68882 device pair appears to be one processor that supports seven floating-point and integer data types, and has eight integer data registers, eight address registers, and eight floating-point data registers.

As shown in Figure 1, the TS 68882 is internally divided into four processing elements ; the bus interface unit (BIU), the conversion control unit (CCU), the execution control unit (ECU), and the microcode control unit (MCU). The BIU communicates with the main processor, the CCU controls the main processor communications dialog and performs some data conversions, and the ECU and MCU execute most floating-point calculations.

The BIU contains the coprocessor interface registers, and the 32-bit control, status, and instruction address registers. In addition to these registers, the register select and DSACK timing control logic is contained in the BIU. Finally, the status flags used to monitor the status of communications with the main processor are contained in the BIU.

The CCU contains special purpose hardware that performs conversions between the single, double, and extended precision memory data formats and the internal data format used by the ECU. It also contains a state machine that controls communications with the main processor during coprocessor interface dialogs.

The eight 80-bit floating-point data registers (FP0-FP7) are located in the ECU. In addition to these registers, the ECU contains a high-speed 67-bit arithmetic unit used for both mantissa and exponent calculations, a barrel shifter that can shift from 1 bit to 67 bits in one machine cycle, and ROM constants (for use by the internal algorithms or user programs).

The MCU contains the clock generator, a two-level microcoded sequencer that controls the ECU, the microcode ROM, and self-test circuitry. The built-in self-test capabilities of the TS 68882 enhance reliability and ease manufacturing requirements ; however, these diagnostic functions are not available to the user.

5

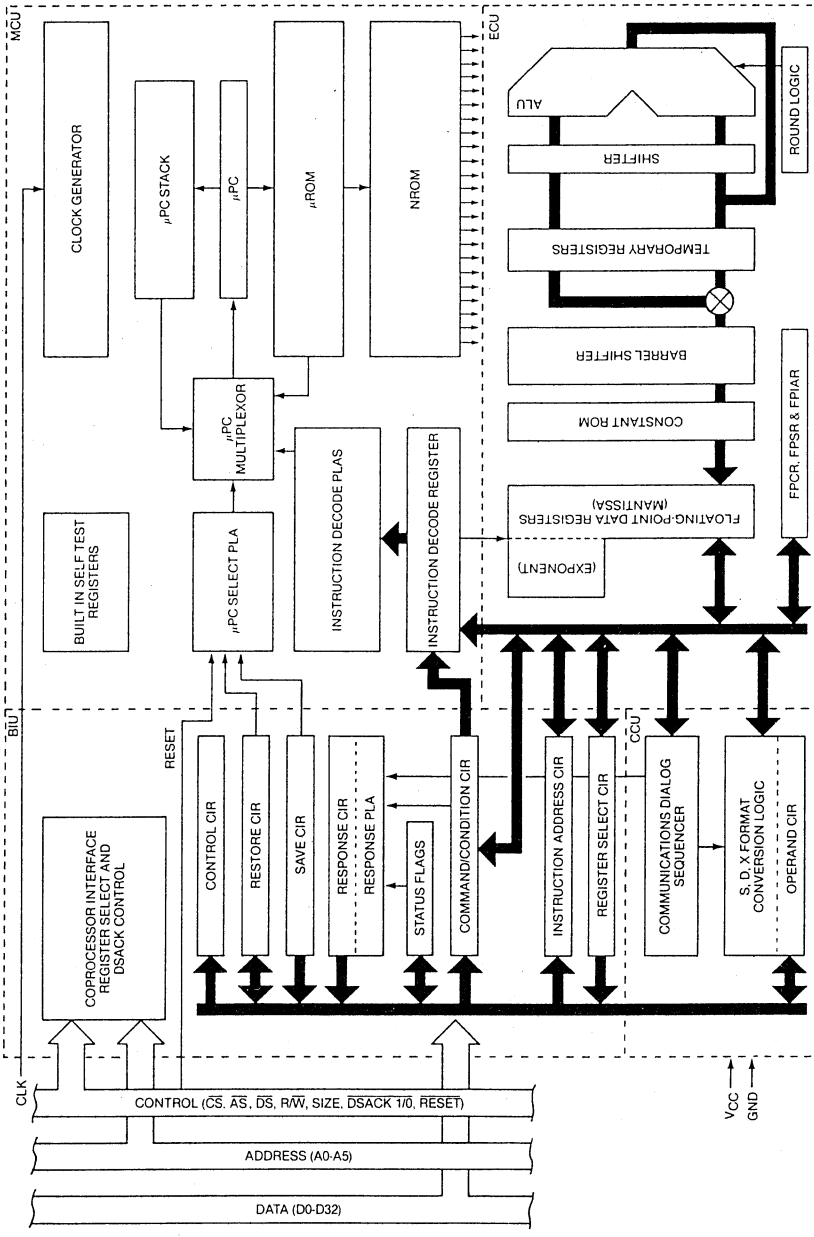
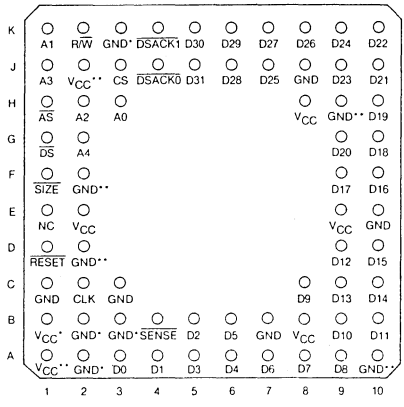


Figure 1 : TS 68882 simplified block diagram.

2 - PIN ASSIGNMENTS



Pin group	V_{CC}	GND
D31-D16	H8	J8
D15-D00	B8	B7
Internal logic DSACK1, DSACK0	E2, E9	A2, B2, B3, B4 (note), C3, E10, K3
Separate	—	C1
Extra	A1, B1, J2	A10, D2, F2, H9
Note : SENSE pin, may be used as an additional GND pin.		

* Reserved for future THOMSON use.

Figure 2.1. : PGA terminal designation.

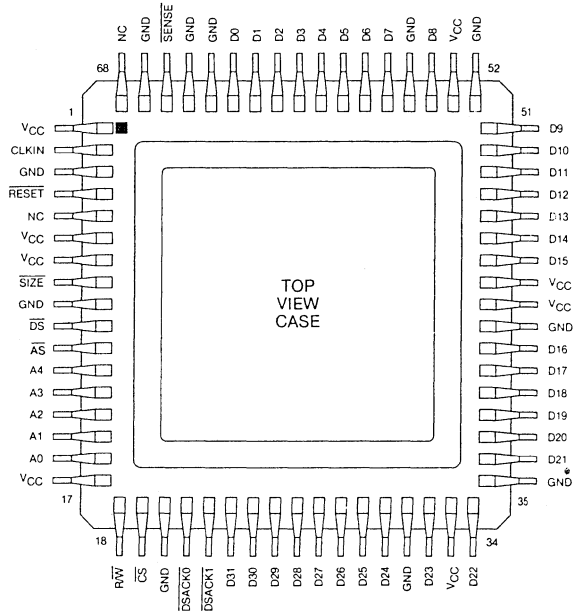
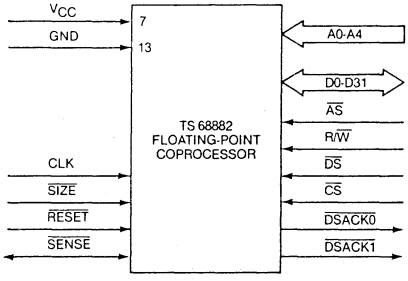


Figure 2.2. : CQFP terminal designation.

3 - FUNCTIONAL SIGNAL DESCRIPTIONS

This section contains a brief description of the input and output signals for the TS 68882 floating-point coprocessor. The signals are functionally organized into groups as shown in Figure 3.



Note : The terms assertion and negation are used extensively. This is done to avoid confusion when describing «active-low» and «active-high» signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or faise.

Figure 3 : TS 68882 input/output signals.

4 · SIGNAL SUMMARY

Table 1 provides a summary of all the TS 68882 signals described in this section.

Table 1 · Signal summary

Signal name	Mnemonic	Input / Output	Active state	Three state
Address bus	A0-A4	Input	High	
Data bus	D0-D13	Input / Output	High	Yes
Size	$\overline{SIZE}$	Input	Low	
Address strobe	$\overline{AS}$	Input	Low	
Chip select	$\overline{CS}$	Input	Low	
Read/Write	R/$\overline{W}$	Input	High / Low	
Data strobe	$\overline{DS}$	Input	Low	
Data transfer and size acknowledge	$\overline{DSACK0}$, $\overline{DSACK1}$	Output	Low	Yes
Reset	$\overline{RESET}$	Input	Low	
Clock	CLK	Input		
Sense device	$\overline{SENSE}$	Input / Output	Low	No
Power input	V_{CC}	Input		
Ground	GND	Input		

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the microprocessor 68882, 16.67, 20 MHz and 25 MHz, in compliance with MIL-STD-883 class B or CECC 90000.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
3) Desc Drawing 5962 - 89436xxx.

2.2 · CECC 90000

1) CECC 90000.
2) Specification CECC 90110-024 for 16, 20 and 25 MHz.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 · Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 (when defined) :

- 68-PIN SQ.PGA UP PAE outline,
- 68-PIN Ceramic Quad Flat Pack CQFP.

The precise case outlines are described on Figures § 9.1 and 9.2.

3.3 · Electrical characteristics

*3.3.1 · **Absolute maximum ratings** (see Table 2)*

Table 2

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_{dmax}	Max Power dissipation	T_{case} = −55°C		2.0	W
		T_{case} = +125°C		1.9	W
T_{case}	Operating temperature	M suffix	−55	+125	°C
		V suffix	−40	+85	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

*3.3.2 · **Recommended condition of use***

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

5

Table 3 · DC electrical characteristics

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C to +125°C

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
T_{case}	Operating temperature		−55	+125	°C
V_{IH}	Input high voltage		2.0	V_{CC}	V
V_{IL}	Input low voltage		GND −0.3	0.8	V
I_{IN}	Input leakage current @ 5.5 V	$\overline{CLK}$, $\overline{RESET}$, R/$\overline{W}$, A0-A4, $\overline{CS}$, $\overline{DS}$, $\overline{AS}$, $\overline{SIZE}$		10	µA
I_{TSI}	HI-Z (Off state) input current @ 2.4 V / 0.4 V	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		20	µA
V_{OH}	Output high voltage (I_{OH} = −400 µA) - Note 1	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	2.4		V
V_{OL}	Output low voltage (I_{OL} = 5.3 mA) - Note 1	$\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		0.5	V
I_{OL}	Output low current (V_{OL} = GND)	SENSE		500	µA
P_D	Power dissipation			0.75	W
C_{in}	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz) - Note 2			20	pF
C_L	Output load capacitance			130	pF

Note 1 : Test load, see Figure 5.
Note 2 : Capacitance is periodically sampled rather than 100 % tested.

3.4 - Thermal characteristics

Table 4

Package	Symbol	Parameter	Value	Rating
PGA 68	θ_{JA}	Thermal resistance - Ceramic junction to ambient	33	°C/W
	θ_{JC}	Thermal resistance - Ceramic junction to case	4	°C/W
CQFP 68	θ_{JA}	Thermal resistance - Ceramic junction to ambient	33	°C/W
	θ_{JC}	Thermal resistance - Ceramic junction to case	3	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 90110-024. Group C inspection is performed on a periodic basis in accordance with CECC 90110-024.

5 - ELECTRICAL CHARACTERISTICS

5

5.1 - General requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below. For inspection purpose, refer to relevant specification :

- DESC see § 4.1
- CECC see § 4.2

Table 5 : Static electrical characteristics for all electrical variants. See § 5.2.

Table 6 : Dynamic electrical characteristics for 68882-16 (16.67 MHz), 68882-20 (20 MHz), 68882-25 (25 MHz) and 68882-33 (33 MHz). See § 5.3.

For static characteristics, test methods refer to clause 5.4.1 hereafter of this specification (Table 5).

For dynamic characteristics (Tables 6 and 7), test methods refer to IEC 748-2 method number, where existing, see § 5.4.2.

5.2 · Static characteristics

Table 5

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / +125°C or −40 / +85°C (see Figure 5)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	2.0	V_{CC}	V
V_{IL}	Input low voltage	GND −0.3	0.8	V
I_{IN}	Input leakage current @ 5.5 V CLK, $\overline{RESET}$, R/$\overline{W}$, A0-A4, $\overline{CS}$, $\overline{DS}$, $\overline{AS}$, $\overline{SIZE}$		10	μA
I_{TSI}	HI-Z (Off state) input current @ 2.4 V / 0.4 V $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		20	μA
V_{OH}	Output high voltage (I_{OH} = −400 μA) - Note 1 $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	2.4		V
V_{OL}	Output low voltage (I_{OL} = 5.3 mA) - Note 1 $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31		0.5	V
I_{OL}	Output low current (V_{OL} = GND) $\overline{SENSE}$		500	μA
P_D	Power dissipation		0.75	W
C_{in}	Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz) - Note 2		20	pF
C_L	Output load capacitance		130	pF

Note 1 : Test load, see Figure 5.
Note 2 : Capacitance is periodically sampled rather than 100 % tested.

5.3 · Dynamic (switching) characteristics

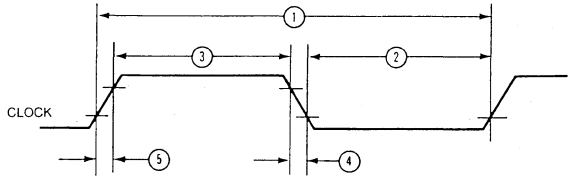
The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.5 V to 5.5 V, see § 5.4.2.

The numbers (N°) refer to the timing diagrams. See Figures 4, 6, 7, 8, and 9.

Table 6 · AC electrical characteristics · Clock input

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C to +125°C (see Figure 4)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of operation	8	16.67	12.5	20	12.5	25	16.7	33.33	MHz
1	Clock time	60	125	50	80	40	80	30	60	ns
2, 3	Clock pulse width	24	95	20	54	15	59	14	66	ns
4, 5	Rise and fall times		5		5		4		3	ns



Note : Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.

Figure 4 : Clock input timing diagram.

Table 7 - AC electrical characteristics - Read and write cycles
V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or T_C = −40°C / +85°C (see Figures 7, 8, 9)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
6	Address valid to $\overline{AS}$ asserted (see Note 5)	15		10		5		5		ns
6a	Address valid to $\overline{DS}$ asserted (read) (see Note 5)	15		10		5		5		ns
6b	Address valid to $\overline{DS}$ asserted (write) (see Note 5)	50		50		35		26		ns
7	$\overline{AS}$ negated to address invalid (see Note 6)	10		10		5		5		ns
7a	$\overline{DS}$ negated to address invalid (see Note 6)	10		10		5		5		ns
8	$\overline{CS}$ asserted to $\overline{AS}$ asserted or $\overline{AS}$ asserted to $\overline{CS}$ asserted (see Note 9)	0		0		0		0		ns
8a	$\overline{CS}$ asserted to $\overline{DS}$ asserted or $\overline{DS}$ asserted to $\overline{CS}$ asserted (read) (see Note 9)	0		0		0		0		ns
8b	$\overline{CS}$ asserted to $\overline{DS}$ asserted (write) (see Note 9)	30		25		20		15		ns
9	$\overline{AS}$ negated to $\overline{CS}$ negated	10		10		5		5		ns
9a	$\overline{DS}$ negated to $\overline{CS}$ negated	10		10		5		5		ns
10	R/$\overline{W}$ high to $\overline{AS}$ asserted (read)	15		10		5		5		ns
10a	R/$\overline{W}$ high to $\overline{DS}$ asserted (read)	15		10		5		5		ns
10b	R/$\overline{W}$ low to $\overline{DS}$ asserted (write)	35		30		25		25		ns
11	$\overline{AS}$ negated to R/$\overline{W}$ low (read) or $\overline{AS}$ negated to R/$\overline{W}$ high (write)	10		10		5		5		ns
11a	$\overline{DS}$ negated to R/$\overline{W}$ low (read) or $\overline{DS}$ negated to R/$\overline{W}$ high (write)	10		10		5		5		ns
12	$\overline{DS}$ width asserted (write)	40		38		30		23		ns
13	$\overline{DS}$ width negated	40		38		30		23		ns
13a	$\overline{DS}$ negated to $\overline{AS}$ asserted (see Note 4)	30		30		25		18		ns
14	$\overline{CS}$, $\overline{DS}$ asserted to data-out valid (read) (see Note 2)		80		45		45		30	ns
15	$\overline{DS}$ negated to data-out invalid (read)	0		0		0		0		ns
16	$\overline{DS}$ negated to data-out high impedance (read)		50		35		35		30	ns
17	Data-in valid to $\overline{DS}$ asserted (write)	15		10		5		5		ns
18	$\overline{DS}$ negated to data-in invalid (write)	15		10		5		5		ns
19	$\overline{START}$ true to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (see Note 2)		50		35		25		20	ns
19a	$\overline{DSACK0}$ asserted to $\overline{DSACK1}$ asserted (skew) (see Note 7)	−15	15	−10	10	−10	10		5	ns
20	$\overline{DSACK0}$ or $\overline{DSACK1}$ asserted to data-out valid		50		43		32		17	ns
21	$\overline{START}$ false to $\overline{DSACK0}$ and $\overline{DSACK1}$ negated (see Note 8)		50		30		40		30	ns

Table 7 - AC electrical characteristics - Read and write cycles (continued)
V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or T_C = −40°C / +85°C (see Figures 7, 8, 9)

N°	Parameter	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
22	$\overline{START}$ false to $\overline{DSACK0}$ and $\overline{DSACK1}$ high impedance (see Note 8)		70		55		55		40	ns
23	$\overline{START}$ true to clock high (synchronous read) (see Notes 3 and 8)	0		0		0		0		ns
24	Clock low to data-out valid (synchronous read) (see Note 3)		105		80		60		45	ns
25	$\overline{START}$ true to data-out valid (synchronous read) (see Notes 3 and 8)	0 1.5	105 + 2.5	1.5	80 + 2.5	1.5	60 + 2.5	1.5	45 − 2.5	ns Clks
26	Clock low to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (synchronous read) (see Note 3)		75		55		45		30	ns
27	$\overline{START}$ true to $\overline{DSACK0}$ and $\overline{DSACK1}$ asserted (synchronous read) (see Notes 3 and 8)	1.5	75 + 2.5	1.5	55 + 2.5	1.5	45 + 2.5	1.5	30 − 2.5	ns Clks

NOTES

Note 1 : Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.

Note 2 : These specifications only apply if the TS 68882 has completed all internal operations initiated by the termination of the previous bus cycle when $\overline{DS}$ was negated.

Note 3 : Synchronous read cycles occur *only* when the save or response CIR locations are read.

Note 4 : This specification only applies to systems in which back-to-back accesses (read-write or write-write) of the operand CIR can occur. When the TS 68882 is used as a coprocessor to the TS 68020 / 68030, this can occur when the addressing mode is immediate.

Note 5 : If the $\overline{SIZE}$ pin is *not* strapped to either V_{CC} or GND, it must have the same setup times as do addresses.

Note 6 : If the $\overline{SIZE}$ pin is *not* strapped to either V_{CC} or GND, it must have the same hold times as do addresses.

Note 7 : This number is reduced to 5 nanoseconds if $\overline{DSACK0}$ and $\overline{DSACK1}$ have equal loads.

Note 8 : $\overline{START}$ is not an external signal ; rather, it is the logical condition that indicates the start of an access. The logical equation for this condition is $\overline{START}$, $\overline{CS}$, $\overline{AS}$, R/$\overline{W}$-$\overline{DS}$.

Note 9 : If a subsequent access is not a FPCP access, $\overline{CS}$ must be negated before the assertion of $\overline{AS}$ and or $\overline{DS}$ on the non-FPCP access. These specifications replace the old specifications 8 and 8A (the old specifications implied that in all cases, transitions in $\overline{CS}$ must not occur simultaneously with transitions of $\overline{AS}$ or $\overline{DS}$. This is not a requirement of the TS 68882).

5

5.4 - Test conditions specific to the device

5.4.1 - Test load

The applicable loading network shall be as defined in column «Test conditions» of Table 6, refering to the loading network number as shown in Figure 5.

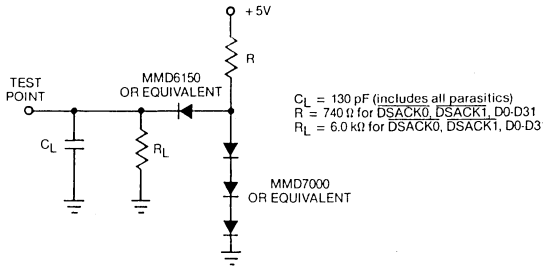


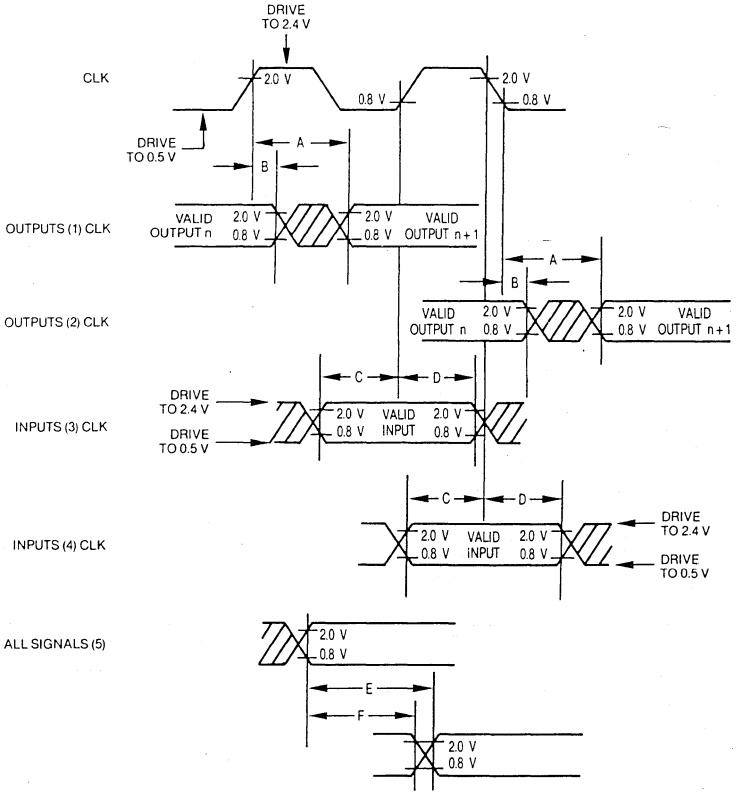
Figure 5 : Test loads.

5.4.2 · AC electrical specification definitions

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock input and, possibly, relative to one or more other signals.

The measurement of the AC specfifications is defined by the waveforms shown in Figure 6. In order to test the parameters guaranteed by THOMSON inputs must be driven to the voltage levels specified in Figure 6. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum and, ans appropriate maximum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications are also shown.

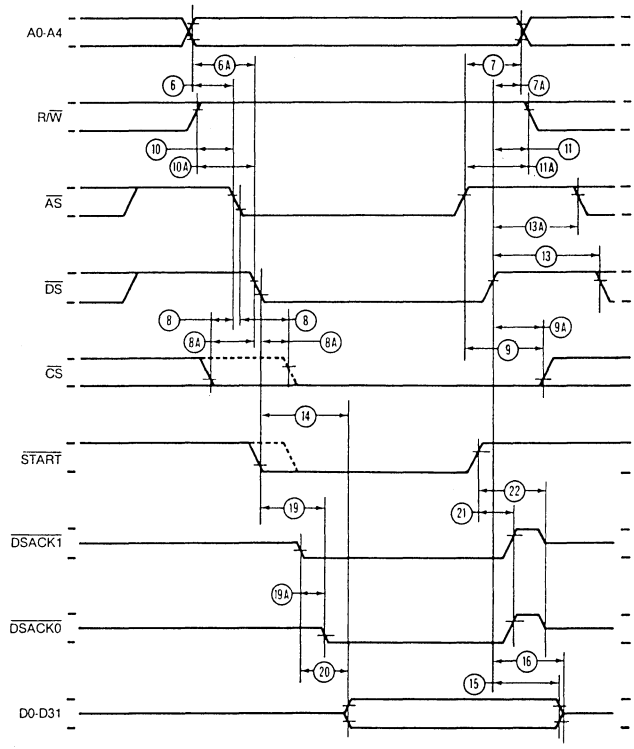
Note that the testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



Legend : A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

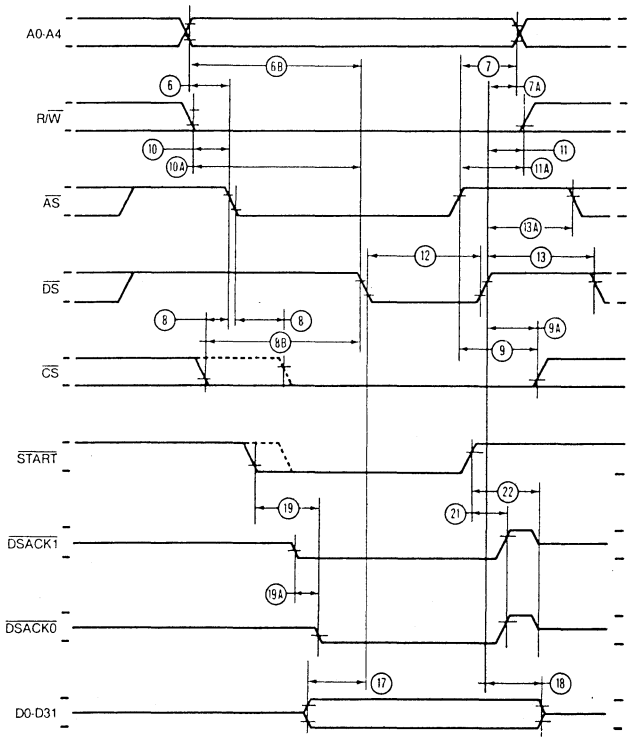
Notes : 1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the failing edge of the clock.
3. This input timing is applicable to all parameters specified relative to the raising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the failing edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

Figure 6 : Drive levels and test points for AC specifications.



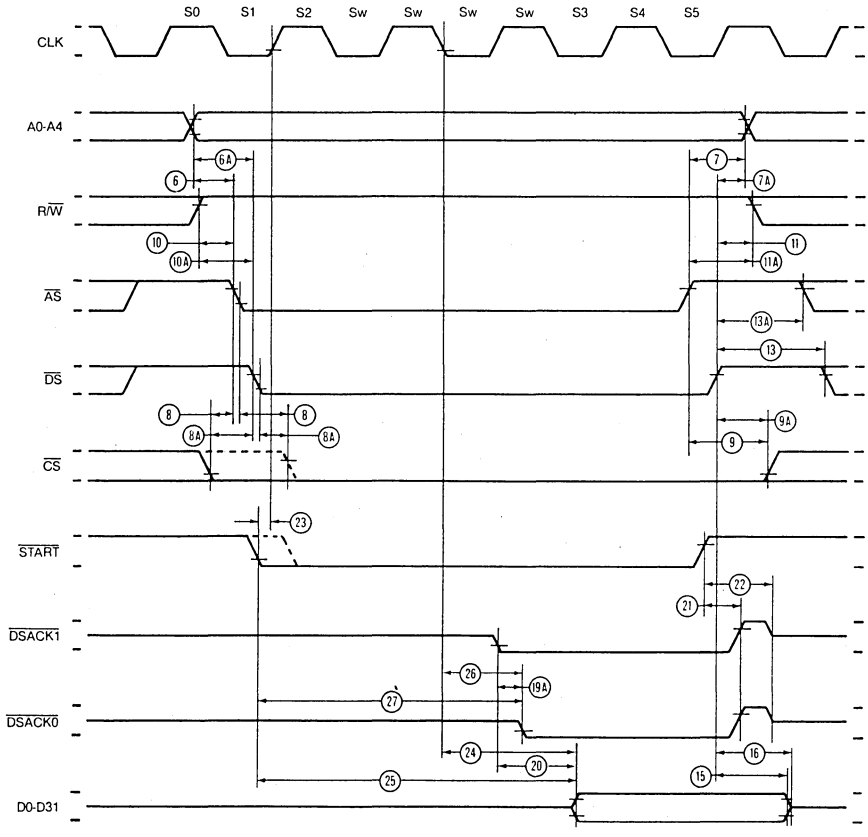
Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 7 : Asynchronous read cycle timing diagram.



Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 8 : Asynchronous write cycle timing diagram.



Note : $\overline{START}$ is actually a logical condition, but is shown as an active signal for clarity. The logical equation for this signal is :
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} \bullet \overline{DS})$.

Figure 9 : Synchronous read cycle timing diagram.

5.5 · Additional information

Additional information shall not be for any inspection purposes.

5.5.1 · Power considerations (see § 3.4)

5.5.2 · Capacitance (Not for inspection purposes)

Symbol	Parameter	Test conditions	Min	Max	Unit
C_{in}	Input capacitance	V_{in} = 0 T_{amb} = 25°C f = 1 MHz		20	pF

6 · FUNCTIONNAL DESCRIPTION

The coprocessor concept

The TS 68882 functions as a coprocessor in systems where the TS 68020 or TS 68030 is the main processor via the TS 68000 coprocessor interface. It functions as a peripheral processor in systems where the main processor is the TS 68000, TS 68010

The TS 68882 utilizes the TS 68000 Family coprocessor interface to provide a logical extension of the TS 68020 / TS 68030 registers and instruction set in a manner which is transparent to the programmer. The programmer perceives the MPU / FPCP execution model as if both devices are implemented on one chip.

A fundamental goal of the TS 68000 Family coprocessor interface is to provide the programmer with an execution model based upon sequential instruction execution by the TS 68020 / TS 68030 and the TS 68882. For optimum performance, however, the coprocessor interface allows concurrent operations in the TS 68882 with respect to the TS 68020 / TS 68030 whenever possible. In order to simplify the programmer's model, the coprocessor interface is designed to emulate, as closely as possible, non-concurrent operation between the TS 68020 / TS 68030 and the TS 68882.

The TS 68882 is a non-DMA type coprocessor which uses a subset of the general purpose coprocessor interface supported by the TS 68020 / TS 68030. Features of the interface implemented in the TS 68882 are as follows :

- The main processor(s) and TS 68882 communicate via standard TS 68000 bus cycles.
- The main processor(s) and TS 68882 communications are not dependent upon the instruction sets or internal details of the individual devices (e.g., instruction pipes or caches, addressing modes).
- The main processor(s) and TS 68882 may operate at different clock speeds.
- TS 68882 instructions utilize all addressing modes provided by the main processor ; all effective addresses are calculated by the main processor at the request of the coprocessor.
- All data transfers are performed by the main processor at the request of the TS 68882 ; thus memory management, bus errors, address errors, and bus arbitration function as if the TS 68882 instructions are executed by the main processor.
- Overlapped (concurrent) instruction execution enhances throughput while maintaining the programmer's model of sequential instruction execution.
- Coprocessor detection of exceptions which require a trap to be taken are serviced by the main processor at the request of the TS 68882 thus exception processing functions as if the TS 68882 instructions were executed by the main processor.
- Support of virtual memory / virtual machine systems is provided via the FSAVE and FRESTORE instructions.
- Up to eight coprocessors may reside in a system simultaneously ; multiple coprocessors of the same type are also allowed.
- Systems may use software emulation of the TS 68882 without reassembling or relinking user software.

The TS 68882 programming model is shown in Figures 10 through 15, and consists of the following :

- Eight 80-bit floating-point data registers (FP0-FP7). These registers are analogous to the integer data registers (D0-D7) and are completely general purpose (i.e., any instruction may use any register).
- A 32-bit control register that contains enable bits for each class of exceptions trap, and mode bits to set the user-selectable rounding and precision modes.
- A 32-bit status register that contains floating-point condition codes, quotient bits, and exception status information.
- A 32-bit instruction address register that contains the main processor memory address of the last floating-point instruction that was executed. This address is used in exception handling to locate the instruction that caused the exception.

The connection between the TS 68020 / TS 68030 and the TS 68882 is a simple extension of the TS 68000 bus interface. The TS 68882 is connected as a coprocessor to the TS 68020 / TS 68030, and the selection of the TS 68882 is based upon a chip select (CS), which is decoded from the TS 68020 / TS 68030 function codes and address bus. Figure 16 illustrates the TS 68882 / TS 68020 or TS 68030 configuration.

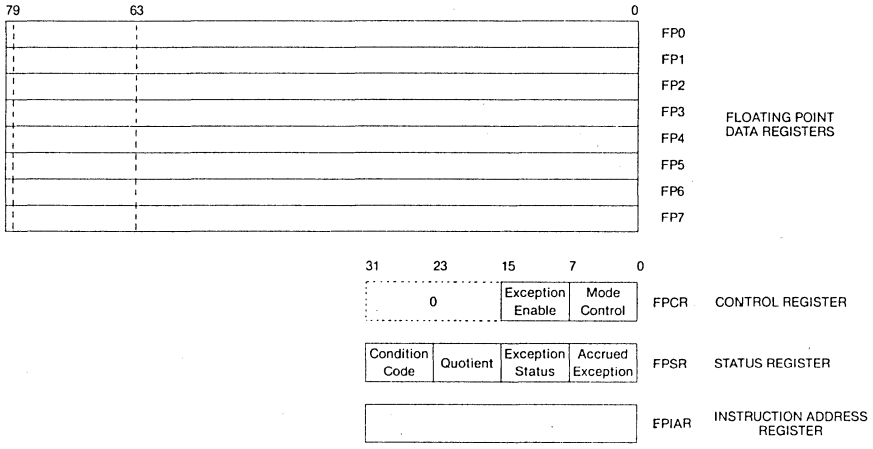


Figure 10 : TS 68882 programming model.

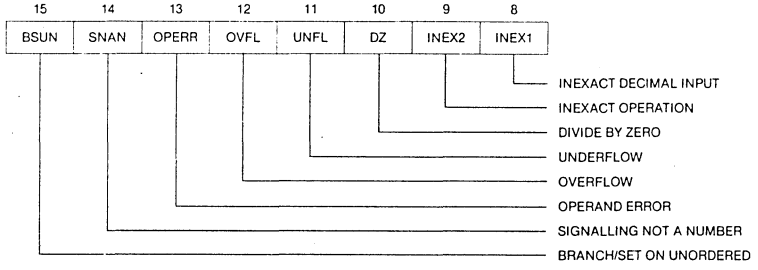


Figure 11 : Exception status/enable byte.

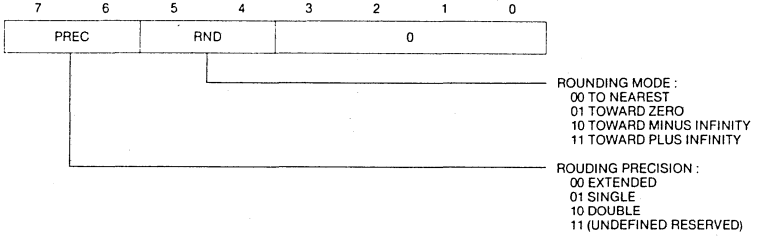


Figure 12 : Mode control byte.

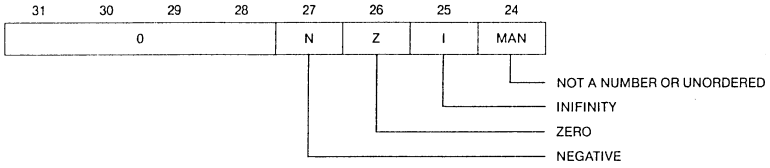


Figure 13 : Condition code byte.

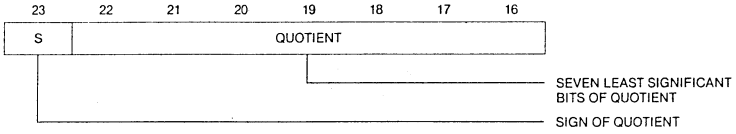


Figure 14 : Quotient byte.

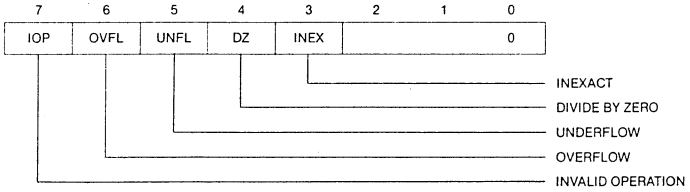


Figure 15 : Accrued exception byte.

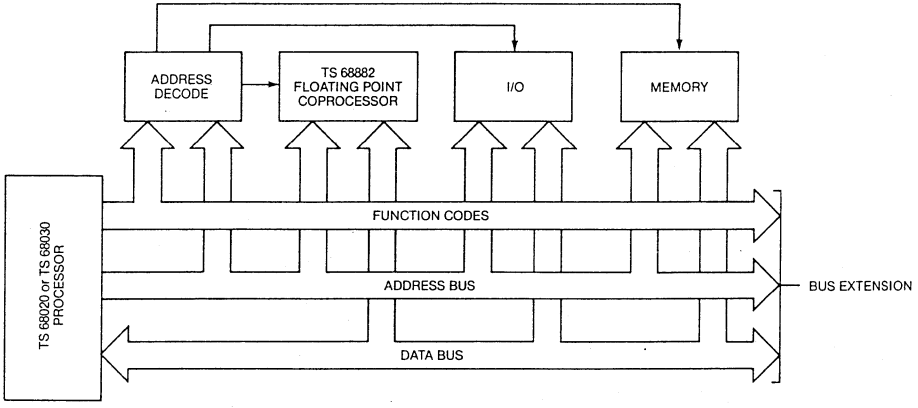


Figure 16 : Typical coprocessor configuration.

Bus interface unit

All communications between the TS 68020 / TS 68030 and the TS 68882 occur via standard TS 68000 Family bus transfers. The TS 68882 is designed to operate on 8-, 16-, or 32-bit data buses.

The TS 68882 contains a number of coprocessor interface registers (CIRs) which are addressed in the same manner as memory by the main processor. The TS 68000 Family coprocessor interface is implemented via a protocol of reading and writing to these registers by the main processor. The TS 68020 and TS 68030 implements this general purpose coprocessor interface protocol in hardware and microcode.

When the TS 68020 / TS 68030 detects a typical TS 68882 instruction, the MPU writes the instruction to the memorymapped command CIR, and reads the response CIR. In this response, the BIU encodes requests for any additional action required of the MPU on behalf of the TS 68882. For example, the response may request that the MPU fetch an operand from the evaluated effective address and transfer the operand to the operand CIR. Once the MPU fulfills the coprocessor request(s), it is free to fetch and execute subsequent instructions.

A key concern in a coprocessor interface that allows concurrent instruction execution is synchronization during main processor and coprocessor communication. If a subsequent instruction is written to the TS 68882 before the CCU has passed the operands for the previous instructions to the ECU, the response instructs the TS 68020 / TS 68030 to wait. Thus, the choice of concurrent or nonconcurrent instruction execution is determined on an instruction-by-instruction basis by the coprocessor.

The only difference between a coprocessor bus transfer and any other bus transfer is that the TS 68020 / TS 68030 issues a function code to indicate the CPU address space during the cycle (the function codes are generated by the TS 68000 Family processors to identify eight separate address spaces). Thus, the memory-mapped coprocessor interface registers do not infringe upon instruction or data address spaces. The TS 68020 / TS 68030 places a coprocessor ID field from the coprocessor instruction onto three of the upper address lines during coprocessor accesses. This ID, along with the CPU address space function code, is decoded to select one of eight coprocessors in the system.

Since the coprocessor interface protocol is based solely on bus transfers, the protocol is easily emulated by software when the TS 68882 is used as a peripheral with any processor capable of memory-mapped I/O over on TS 68000 style bus. When used as a peripheral processor with the 8-bit TS 68008 or the 16-bit TS 68000, or TS 68010, all TS 68882 instructions are trapped by the main processor to an exception handler at execution time. Thus, the software emulation of the processor interface protocol can be totally transparent to the user. The system can be quickly upgraded by replacing the main processor with an TS 68020 TS 68030 without changes to the user software.

Since the bus is asynchronous, the TS 68882 need not run at the same clock speed as the main processor. Total system performance may therefore be customized. For example, a system requiring very fast floating-point arithmetic with relatively slow integer arthmetic can be designed with an inexpensive main processor and a fast TS 68882.

Coprocessor interface

The TS 68000 Family coprocessor interface is an integral part of the TS 68882 and TS 68020 TS 68030 designs, with the interface tasks shared between the two. The interface is fully compatible with all present and future TS 68000 Family products. Tasks are partitioned such that the TS 68020 TS 68030 does not have to decode coprocessor instructions and, the TS 68882 does not have to duplicate main processor functions such as effective address evaluation.

This partitioning provides an orthogonal extension of the instruction set by permitting TS 68882 instructions to utilize all TS 68020 / TS 68030 addressing modes and to generate execution time exception traps. Thus, from the programmer's view, the CPU and coprocessor appear to be integrated onto a single chip. While the execution of the majority of TS 68882 instructions may be overlapped with the execution of TS 68020 / TS 68030 instructions, concurrency is completely transparent to the programmer. The TS 68020 / TS 68030 single-step and program flow (trace) modes are fully supported by the TS 68882 and the TS 68000 Family coprocessor interface.

While the TS 68000 Family coprocessor interface permits coprocessors to be bus masters, the TS 68882 is never a bus master. The TS 68882 requests that the TS 68020 / TS 68030 fetch all operands and store all results. In this manner, the TS 68020 / TS 68030 32-bit data bus provides high speed transfer of floating-point operands and results while simplifying the design of the TS 68882.

Since the coprocessor interface is based solely upon bus cycles and the TS 68882 is never a bus master, the TS 68882 can be placed on either the locical or physical side of the system memory management unit. This provides a great deal of flexibility in the system design.

The virtual machine architecture of the TS 68000 Family is supported by the coprocessor interface and the TS 68882 through the FSAVE and FRESTORE instructions. If the TS 68020 / TS 68030 detects a page fault and/or task time out, it can force the TS 68882 to stop whatever operation is in process at any time (even in the middle of the execution of an instruction) and save the TS 68882 internal state in memory.

The size of the saved internal state of the TS 68882 is dependent upon what the CCU and ECU are doing at the time that the FSAVE is executed. If the TS 68882 is in the reset state when the FSAVE instruction is received, only one word of state is transferred to memory, which may be examined by the operating system to determine that the coprocessor programmer's model is empty. If the coprocessor is idle when the save instruction is received, only a few words of internal state are transferred to memory. If the TS 68882 is in the middle of performing a calculation, it may be necessary to save the entire internal state of the machine. Instructions that can complete execution in less time than it would take to save the larger state in mid-instruction are allowed to complete execution and then save the idle state. Thus the size of the saved internal state is kept to a minimum. The ability to utilize several internal state sizes greatly reduces the average context switching time.

The FRESTORE instruction permits reloading of an internal state that was saved earlier, and continues any operation that was previously suspended. Restoring of the reset internal state functions just like a hardware reset to the TS 68882 in that defaults are re-established.

Note : Though the TS 68882 is instruction set compatible with the TS 68881, the idle and busy state frames are both 32 bytes larger on the TS 68882 than on the TS 68881. A unique format word is generated by the TS 68882 so that system software can detect this difference.

Operand data formats

The TS 68882 supports the following data formats :

Byte Integer (B)

Word Integer (W)

Long Word Integer (L)

Single Precision Real (S)

Double Precision Real (D)

Extended Precision Real (X)

Packed Decimal String Real (P)

The capital letters contained in parenthesis denote suffixes added to instructions in the assembly language source to specify the data format to be used.

Integer data formats

The three integer data formats (byte, word, and long word) are the standard data formats supported in the TS 68000 Family architecture. Whenever an integer is used in a floating-point operation, the integer is automatically converted by the TS 68882 to an extended precision floating-point number before being used. For example, to add an integer constant of five to the number contained in floating-point data register 3 (FP3), the following instruction can be used :

FADD.W #5.FP3

The ability to effectively use integers in floating-point operations saves user memory since an integer representation of a number, if respresentable, is usually smaller than the equivalent floating-point representation.

5

Floating-point data formats

The floating-point data formats single precision (32-bits) and double precision (64-bits) are as defined by the IEEE standard. These are the main floating-point formats and should be used for most calculations involving real numbers. Table 8 lists the exponent and mantissa size for single, double, and extended precision. The exponent is biased, and the mantissa is in sign and magnitude form. Since single and double precision require normalized numbers, the most significant bit of the mantissa is implied as one and is not included, thus giving one extra bit of precision.

Table 8 - Exponent and Mantissa sizes

Data Format	Exponent bits	Mantissa bits	Bias
Single	8	23 (+ 1)	127
Double	11	52 (+ 1)	1023
Extended	15	64	16383

The extended precision data format is also in conformance with the IEEE standard, but the standard does not specify this format to the bit level as it does for single and double precision. The memory format on the TS 68882 consists of 96 bits (three long words). Only 80 bits are actually used, the other 16 bits are for future expandability and for long-word alignment of floating-point data structures. Extended format has a 15-bit exponent, a 64-bit mantissa, and a 1-bit mantissa sign.

Extended precision numbers are intended for use as temporary variables, intermediate values, or in places where extra precision is needed. For example, a compiler might select extended precision arithmetic for evaluation of the right side of an equation with mixed sized data and then convert the answer to the data type on the left side of the equation. It is anticipated that extended precision data will not be stored in large arrays, due to the amount of memory required by each number.

Packed decimal string real data format

The packed decimal data format allows packed BCD strings to be input to and output from the TS 68882. The strings consist of a 3-digit base 10 exponent and 17-digit base 10 mantissa. Both the exponent and mantissa have a separate sign bit. All digits are packed BCD, such that an entire string fits in 96 bits (three long words). As is the case with all data formats, when packed BCD strings are input to the TS 68882, the strings are automatically converted to extended precision real values. This allows packed BCD numbers to be used as inputs to any operation. For example :

FADD.P # – 6.023E + 24, FP5

BCD numbers can be output from the TS 68882 in a format readily used for printing by a program generated by a high-level language compiler. For example :

FMOVE.P FP3.BUFFER (# – 5)

instructs the TS 68882 to convert the floating-point data register 3 (FP3) contents into a packed BCD string with five digits to the right of the decimal point (FORTRAN F format).

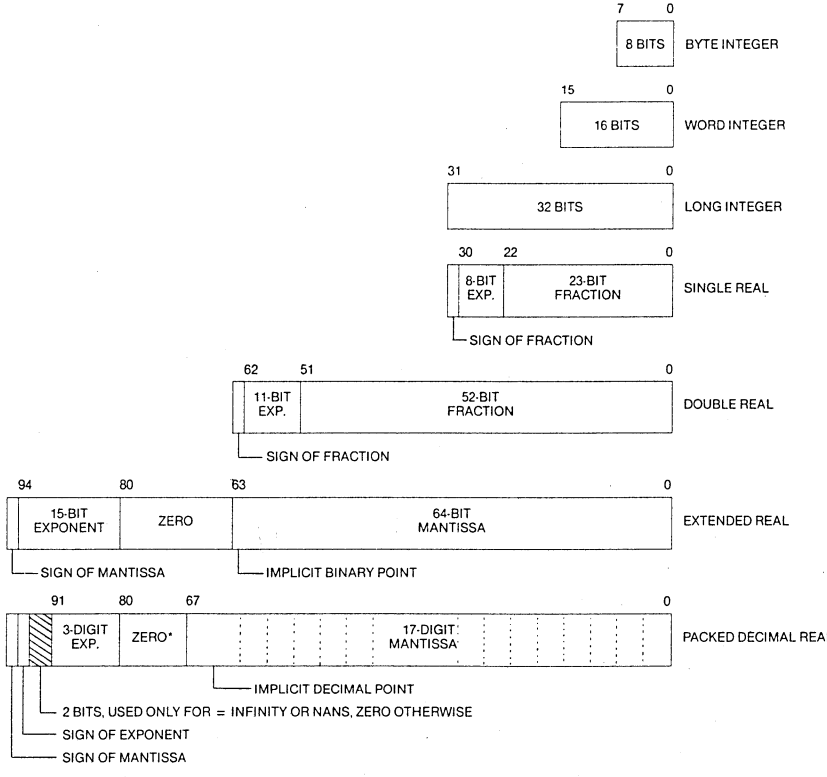
Data format summary

All data formats described above are supported ortrhogonally by all arithmetic and transcendental operations, and by all appropriate TS 68000 Family addressing modes. For example, all of the following are legal instructions :

```
FADD.B    #3.FP0
FADD.W    D2.FP3
FADD.L    BIGINT.FP7
FADD.S    #3.14159.FP5
FADD.D    (SP)+.FP6
FADD.X    [(TEMP – PTR.A7)].FP3
FADD.P    #1.23E25.FP0
```

On-chip calculations are performed to extended precision format, and the eight floating point data registers always contain extended precision values. All data used in an operation is converted to extended precision by the TS 68882 before the specific operation is performed, and all results are in extended precision. This ensures maximum accuracy without sacrificing performance.

Refer to Figure 17 for a summary of the memory formats for the seven data formats supported by the TS 68882.



* Unless a binary-to-decimal conversion overflow occurs.

Figure 17 : TS 68882 data format summary.

Instruction set

The TS 68882 instruction set is organized into six major classes :

1. Moves between the TS 68882 and memory or the MPU (in and out).
2. Move multiple registers (in and out).
3. Monadic operations.
4. Dyadic operations.
5. Branch, set, or trap conditionally, and
6. Miscellaneous.

Moves

All moves from memory (or from an MPU data register) to the TS 68882, cause data conversion from the source data format to the internal extended precision format.

All moves from the TS 68882 to memory (or to an MPU data register), cause data conversion from the internal extended precision format to the destination data format.

Note that data movement instructions perform arithmetic operations, since the result is always rounded to the precision selected in the FPCR mode control byte. The result is rounded using the selected rounding mode, and is checked for overflow and underflow.

The syntax for the move is :

FMOVE.(fmt)	(ea).FPn	Move to TS 68882
FMOVE.(fmt)	FPm.(ea)	Move from TS 68882
FMOVE.X	FPm.FPn	Move within TS 68882

where :

(ea) is an TS 68000 Family effective address operand and (fmt) is the data format size. FPm and FPn are floating-point data registers.

5

Move multiples

The floating-point move multiple instructions on the TS 68882 are much like the integer counterparts on the TS 68000 Family processors. Any set of the floating-point registers FP0 through FP7 can be moved to or from memory with one instruction. These registers are always moved as 96-bit extended data with no conversion (hence no possibility of conversion errors). Some move multiple examples are as follows :

FMOVEM	(ea),FP0-FP3/FP7
FMOVEM	FP2/FP4/FP6,(ea)

Move multiples are useful during context switches and interrupts to save or restore the state of a program. These moves are also useful at the start and end of a procedure to save and restore the calling routine's register set. In order to reduce procedure call overhead, the list of registers to be saved or restored can be contained in a data register. This allows run-time iptimization by allowing a called routine to save as few registers as possible. Note that no rounding or overflow/underflow checking is performed by these operations.

Monadic operations

Monadic operations have one operand. This operand may be in a floating-point data register, memory, or in an MPU data register. The result is always stored in a floating-point data register. For example, the synthax for square root is :

FSQRT.(fmt)	(ea),FPN or,
FSQRT.X	FPm,FPn or,
FSQRT.X	FPn

The TS 68882 monadic operations available are as follows :

FABS	Absolue Value
FACOS	Arc Cosine
FASIN	Arc Sine
FATAN	Arc Tangent
FATANH	Hyperbolic Arc Tangent
FCOS	Cosine
FCOSH	Hyperbolic Cosine
FETOX	e to the x Power
FETOXM1	e to the x Power – 1
FGETEXP	Get Exponent
FGETMAN	Get Mantissa
FINT	Integer Part
FINTRZ	Integer Part (Truncated)
FLOG10	Log Base 10
FLOG2	Log Base 2
FLOGN	Log Base e
FLOGNP1	Log Base e of(x + 1)
FNEG	Negate
FSIN	Sine
FSINCOS	Simultaneous Sine and Cosine
FSINH	Hyperbolic Sine
FSQRT	Square Root
FTAN	Tangent
FTANH	Hyperbolic Tangent
FTENTOX	10 to the x Power
FTST	test
FTWOTOX	2 to the x Power

Dyadic operations

Dyadic operations have two input operands. The first input operand comes from a floating-point data register, memory, or MPU data register. The second input operand comes from a floating-point data register. The destination is the same floating-point data register used for the second input. For example, the syntax for add is :

FADD.(fmt)	(ea).FPn or,
FADD.X	FPm.FPn

The TS 68882 dyadic operations available are as follows :

FADD	Add
FCMP	Compare
FDIV	Divide
FMOD	Modulo Remainder
FMUL	Multiply
FREM	IEEE Remainder
FSCALE	Scale Exponent
FSGLDIV	Single Precision Divide
FSGLMUL	Single Precision Multiply
FSUB	Subtract

Branch, set, and trap-on condition

The floating-point branch, set, and trap-on condition instructions implemented by the TS 68882 are similar to the equivalent integer instructions of the TS 68000 Family processors, except that more conditions exist due to the special values in IEEE floating-point arithmetic. When a conditional instruction is executed, the TS 68882 performs the necessary condition checking and tells the MPU whether the condition is true or faise ; the MPU then takes the appropriate action. Since the TS 68882 and TS 68020 / TS 68030 are closely coupled, the floating-point branch operations executed by the pair are very fast.

The TS 68882 conditional operations are :

FBcc	Branch
FDBcc	Decrement and Branch
FScc	Set Byte According to Condition
FTRAPcc	Trap-on Condition (with an Optional Parameter)

where :

cc is one of the 32 floating-point conditional test specifiers as shown in Table 9.

Table 9 · Floating-point conditional test specifiers

Mnemonic	Definition
Note : The following conditional tests do not set the BSUN bit in the status register exception byte under any circumstances.	
F	False
EQ	Equal
OGT	Ordered Greater Than
OGE	Ordered Greater Than or Equal
OLT	Ordered Less Than
OLE	Ordered Less Than or Equal
OGL	Ordered Greater or Less Than
OR	Ordered
UN	Unordered
UEQ	Unordered or Equal
UGT	Unordered or Greater Than
UGE	Unordered or Greater or Equal
ULT	Unordered or Less Than
ULE	Unordered or Less or Equal
NE	Not Equal
T	True
Note : The following conditional tests set the BSUN bit in the status register exception byte if the NAN condition code bit is set when a conditional instruction is executed.	
SF	Signaling False
SEQ	Signaling Equal
GT	Greater Than
GE	Greater Than or Equal
LT	Less Than
LE	Less Than or Equal
GL	Greater or Less Than
GLE	Greater Less or Equal
NGLE	Not (Greater, Less or Equal)
NGL	Not (Greater or Less)
NLE	Not (Less or Equal)
NLT	Not (Less Than)
NGE	Not (Greater or Equal)
NGT	Not (Greater Than)
SNE	Signaling Not Equal
ST	Signaling True

5

Miscellaneous instructions

Miscellaneous instructions include moves to and from the status, control, and instruction address registers and a no operation function that can be used to «flush» exceptions. Also included are the virtual memory/machine FSAVE and FRESTORE instructions that save and restore the internal state of the TS 68882.

FMOVE	(ea), FPcr	Move to Control Register(s)
FMOVE	FPcr, (ea)	Move from Control Register(s)
FNOP		No Operation
FSAVE	(ea)	Virtual Machine State Save
FRESTORE	(ea)	Virtual Machine State Restore

Addressing modes

The TS 68882 does not perform address calculations. This satifies the criterion that an TS 68000 Family coprocessor must not depend on certain features or capabilities that may or may not be implemented by a given main processor. Thus, when the. TS 68882 instructs the TS 68020 / TS 68030 to transfer an operand via the coprocessor interface, the MPU performs the addressing mode calculations requested in the instruction. In this case, the instruction is encoded specifically for the TS 68020 / TS 68030, and the execution of the TS 68882 is not dependent on that encoding, but only on the value of the command word written to the TS 68882 by the main processor.

This interface is quite flexible and allows any addressing mode to be used with floating-point instructions. For the TS 68000 Family, these addressing modes includ immediate, postincrement, predecrement, data or address register direct, and the indexed/indirect addressing modes of the TS 68020 / TS 68030. Some addressing modes are restricted for some instructions in keeping with the TS 68000 Family architectural definitions (e.g. PC relative addressing is not allowed for a destination operand).

The orthogonal instruction set of the TS 68882, along with the flexible branches and addressing modes, allows a programmer writing assembly language code, or a compiler writer generating object or source code for the MPU / TS 68882 device pair, to think of the TS 68882 as though it is part of the MPU. There are no special restrictions imposed by the coprocessor interface, and floating-point arithmetic is coded exactly like integer arithmetic.

Address bus (A0 through A4)

These active-high address line inputs are used by the main processor to select the coprocessor interface register locations located in the CPU address space. These lines control the register selection as listed in Table 10.

When the TS 68882 is configured to operate over an 8-bit data bus, the A0 pin is used as an address signal for byte acceses of the coprocessor interface registers. When the TS 68882 is configured to operate over a 16- or 32-bit system data bus, both the A0 and SIZE pins are stapped high and/or low as listed in Table 11.

Table 10 - Coprocessor interface register selection

A4-A0	Offset	Width	Type	Register
0000x	S00	16	Read	Response
0001x	S02	16	Write	Control
0010x	S04	16	Read	Save
0011x	S06	16	R/W	Restore
0100x	S08	16	—	(Reserved)
0101x	S0A	16	Write	Command
0110x	S0C	16	—	(Reserved)
0111x	S0E	16	Write	Condition
100xx	S10	32	R/W	Operand
1010x	S14	16	Read	Register select
1011x	S16	16	—	(Reserved)
110xx	S18	32	Read	Instruction Address
111xx	S1C	32	R/W	Operand Address

Table 11 - System data bus size configuration

A0	Size	Data bus
	Low	8-Bit
Low	High	16-Bit
High	High	32-Bit

Data bus (D0 through D31)

This 32-bit, bidirectional, three-state bus serves as the general purpose data path between the TS 68020 / TS 68030 and the TS 68882. Regardless of whether the TS 68882 is operated as a coprocessor or a peripheral processor, all inter-processor transfers of instruction information, operand data, status information, and requests for service occur as standard TS 68000 bus cycles.

The TS 68882 will operate over an 8-, 16-, or 32-bit system data bus. Depending upon the system data bus configuration, both the A0 and $\overline{SIZE}$ pins are configured specifically for the applicable bus configuration. (Refer to ADDRESS BUS (A0 through A4) and SIZE ($\overline{SIZE}$) for futher details).

Size ($\overline{SIZE}$)

This active-low input signal is used in conjunction with the A0 pin to configure the TS 68882 for operation over an 8-, 16-, or 32-bit system data bus. When the TS 68882 is configured to operate over a 16- or 32-bit system data bus, both the $\overline{SIZE}$ and A0 pins are strapped high and/or low as listed in Table 11.

Address Strobe ($\overline{AS}$)

This active-low input signal indicates that there is a valid address on the address bus, and both the chip select ($\overline{CS}$) and read/write (R/$\overline{W}$) signal lines are valid.

Chip Select ($\overline{CS}$)

This active-low input signal enables the main processor access to the TS 68882 coprocessor interface registers. When operating the TS 68882 as a peripheral processor, the chip select decode is system dependent (i.e., like the chip select on any peripheral). The $\overline{CS}$ signal must be valid (either asserted or negated) when $\overline{AS}$ is asserted. Refer to CHIP SELECT TIMING for further discussion of timing restrictions for this signal.

Read/Write (R/$\overline{W}$)

This input signal indicates the direction of a bus transaction (read/write) by the main processor. A logic high (1) indicates a read from the TS 68882, and a logic low (0) indicates a write to the TS 68882. The R/$\overline{W}$ signal must be valid when $\overline{AS}$ is asserted.

Data Strobe ($\overline{DS}$)

This active-low input signal indicates that there is valid data on the data bus during a write bus cycle.

Data transfer and size acknowledge ($\overline{DSACK0}$, $\overline{DSACK1}$)

These active-low, three-state output signals indicate the completion of a bus cycle to the main processor. The TS 68882 asserts both the $\overline{DSACK0}$ and $\overline{DSACK1}$ signals upon assertion of $\overline{CS}$.

If the bus cycle is a main processor read, the TS 68882 asserts $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to indicate that the information on the data bus is valid. (Both DSACK signals may be asserted in advance of the valid data being placed on the bus). If the bus cycle is a main processor write to the TS 68882, $\overline{DSACK0}$ and $\overline{DSACK1}$ are used to acknowledge acceptance of the data by the TS 68882.

The TS 68882 also uses $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to dynamically indicate to the TS 68020 / TS 68030 the «port» size (system data bus width) on a cycle-by-cycle basis. Depending upon which of the two DSACK pins are asserted in a given bus cycle, the TS 68020 / TS 68030 assumes data has been transferred to/from an 8-, 16-, or 32-bit wide data port. Table 12 lists the DSACK assertions that are used by the TS 68882 for the various bus cycles over the various bus cycles over the various system data bus configurations.

Table 12 indicates that all accesses over a 32-bit bus where A4 equals zero are to 16-bit registers. The TS 68882 implements all 16-bit coprocessor interface registers on data lines D16-D13 (to eliminate the need for on-chip multiplexers) ; howerver, the TS 68020 / TS 68030 expects 16-bit registers that are located in a 32-bit port at odd word addresses (A1 = 1) to be implemented on data lines D0-D15. For accesses to these registers when configured for 32-bit bus operation, the TS 68882 generates DSACK signals as listed in Table 12 to inform the TS 68020 / TS 68030 of valid data on D16-D31 instead of D0-D15.

An external holding resistor is required to maintain both $\overline{DSACK0}$ and $\overline{DSACK1}$ high between bus cycles. In order to reduce the signal rise time, the $\overline{DSACK0}$ and $\overline{DSACK1}$ lines are actively pulled up (negated) by the TS 68882 following the rising edge of $\overline{AS}$ or $\overline{DS}$, and both DSACK lines are then three-stated (placed in the high-impedance state) to avoid interference with the next bus cycle.

Table 12 · DSACK assertions

Data Bus	A4	$\overline{DSACK1}$	$\overline{DSACK2}$	Comments
32-Bit	1	L	L	Valid data on D31-D0
32-Bit	0	L	H	Valid data on D31-D16
16-Bit	x	L	H	Valid data on D31-D16 or D15-D0
8-Bit	x	H	L	Valid data on D31-D24, D23-D16, D15-D8 or D7-D0
All	x	H	H	Insert wait states in current bus cycle

Reset ($\overline{RESET}$)

This active-low input signal causes the TS 68882 to initialize the floating-point data registers to non-signaling not-a-numbers (NANs) and clears the floating-point control, status, and instruction address registers.

When performing a power-up reset, external circuity should keep the $\overline{RESET}$ line asserted for a minimum of four clock cycles after V_{CC} is within tolerance. This assures correct initialization of the TS 68882 when power is applied. For compatibility with all TS 68000 Family devices, 100 milliseconds should be used as the minimum.

When performing a reset of the TS 68882 after V_{CC} has been within tolerance for more than the initial power-up time, the $\overline{RESET}$ line must have an asserted pulse width which is greater than two clock cycles. For compatibility with all TS 68000 Family devices, 10 clock cycles should be used as the minimum.

Clock (CLK)

The TS 68882 clock input is a TTL-compatible signal that is internally buffered for development of the internal clock signals. The clock input should be a constant frequency square wave with no stretching or shaping techniques required. The clock should not be gated off at any time and must conform to minimum and maximum period and pulse width times.

Sense device ($\overline{SENSE}$)

This pin may be used optionally as an additional GND pin, or as an indicator to external hardware that the TS 68882 is present in the system. This signal is internally connected to the GND of the die, but it is not necessary to connect it to the external ground for correct device operation. If a pullup resistor (which should be larger than 10 kΩ) is connected to this pin location, external hardware may sense the presence of the TS 68882 in a system.

Power (V_{CC} and GND)

These pins provide the supply voltage and system reference level for the internal circuitry of the TS 68882. Care should be taken to reduce the noise level on these pins with appropriate capacitive decoupling.

No Connect (NC)

One pin of the TS 68882 package is designated as a no connect (NC). This pin position is reserved for future use by THOMSON, and should not be used for signal routing or connected to V_{CC} or GND.

Interfacing methods

TS 68882 / TS 68020 or TS 68030 Interfacing

The following paragraphs describe how to connect the TS 68882 to an TS 68020 or TS 68030 for coprocessor operation via an 8-, 16-, or 32-bit data bus.

32-Bit Data Bus Coprocessor Connection

Figure 18 illustrates the coprocessor interface connection of an TS 68882 to an TS 68020 / TS 68030 via a 32-bit data bus. The TS 68882 is configured to operate over a 32-bit data bus when both the A0 and $\overline{SIZE}$ pins are connected to V_{CC}.

16-Bit Data Bus Coprocessor Connection

Figure 19 illustrates the coprocessor interface connection of an TS 68882 to an TS 68020 / TS 68030 via a 16-bit data bus. The TS 68882 is configured to operate over a 16-bit data bus when the $\overline{SIZE}$ pin is connected to V_{CC}, and the A0 pin is connected to GND. The sixteen least significant data pins (D0-D15) must be connected to the sixteen most siginificant data pins (D16-D31) when the TS 68882 is configured to operate over a 16-bit data bus (i.e., connect D0 to D16, D1 to D17, ... and D15 to D31). The DSACK pins of the two devices are directly connected, although it is not necessary to connect the $\overline{DSACK0}$ pin since the TS 68882 never aserts it in this configuration.

8-Bit Data Bus Coprocessor Connection

Figure 20 illustrates the connection of an TS 68882 to an TS 68020 / TS 68230 as a coprocessor over an 8-bit data bus. The TS 68882 is configured to operate over a 8-bit data bus when the $\overline{SIZE}$ pin is connected to GND. The twenty four least significant data pins (D0-D23) must be connected to the eight most siginificant data pins (D24-D31) when the TS 68882 is configured to operate over a 8-bit data bus (i.e., connect D0 to D8, D16 to D24 ; D1 to D9, D17, and D15 ; ... and D7 to D15, D23 and D31). The DSACK pins of the two devices are directly connected, although it is not necessary to connect the $\overline{DSACK1}$ pin since the TS 68882 never asserts it in this configuration.

TS 68882 / TS 68000 / TS 68008 / TS 68010 Interfacing

The following paragraphs describe how to connect the TS 68882 to an TS 6800, TS 68008, or TS 68010 processor for operation as a peripheral via an 8- or 16-bit data bus.

16-Bit Data Peripheral Processor Connection

Figure 21 illustrates the connection of an TS 68882 to an TS 68000 or TS 68010 as a peripheral processor over an 16-bit data bus. The TS 68882 is configured to operate over an 16-bit data bus when the $\overline{SIZE}$ pin is connected to V_{CC}, and the A0 pin is connected to GND. The sixteen least significant data pins (D0-D15) must be connected to the sixteen most significant data pins (D16-D31) when the TS 68882 is configured to operate over an 16-bit data bus (i.e., connect D0 to D16, D1 to D17,... and D15 to D31). The $\overline{DSACK1}$ pin of the TS 68882, is connected to the $\overline{DTACK}$ pin of the main processor, and the $\overline{DSACK0}$ pin is not used.

When connected as a peripheral processor, the TS 68882 chip select ($\overline{CS}$) decode is system dependent. If the TS 68000 is used as the main processor, the TS 68882 $\overline{CS}$ must be decoded in the supervisor or user data spaces. Howerver, if the TS 68010 is used for the main processor, the MOVES instruction may be used to emulate any CPU space access that the TS 68020 / TS 68030 generates for coprocessor communications. Thus, the $\overline{CS}$ decode logic for such systems may be the same as in an TS 68020 / TS 68030 systems, such that the TS 68882 will not use anly part of the data address spaces.

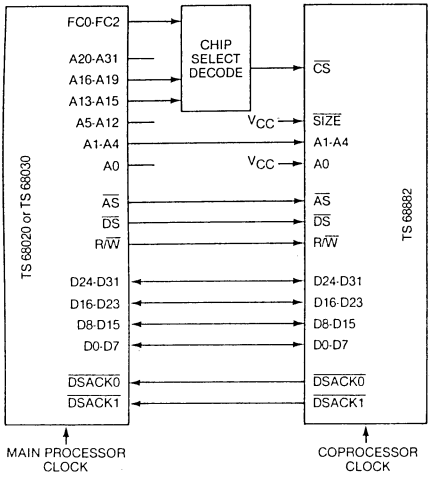


Figure 18 : 32-bit data bus coprocessor connection.

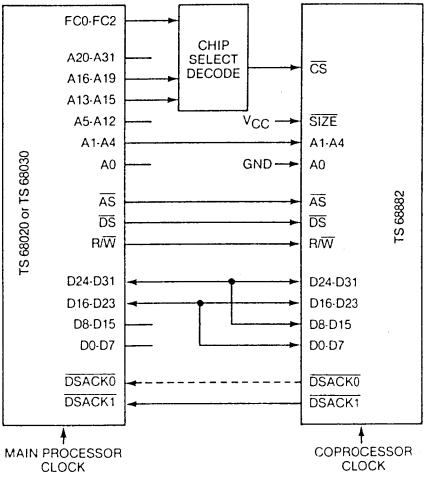


Figure 19 : 16-bit data bus coprocessor connection.

5

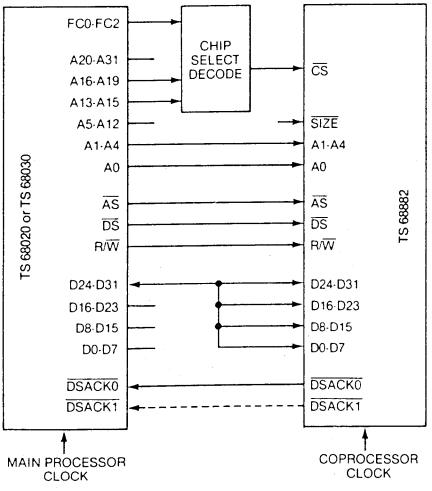


Figure 20 : 8-bit data bus coprocessor connection.

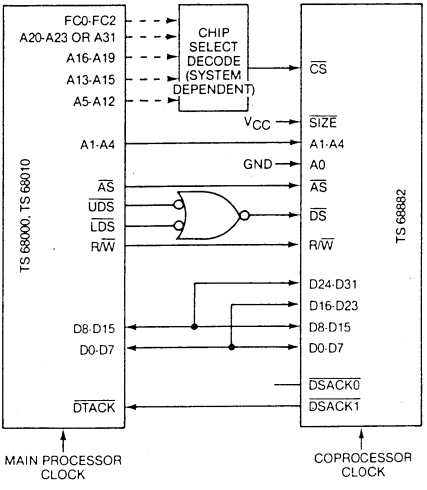


Figure 21 : 16-bit data bus peripheral processor connection.

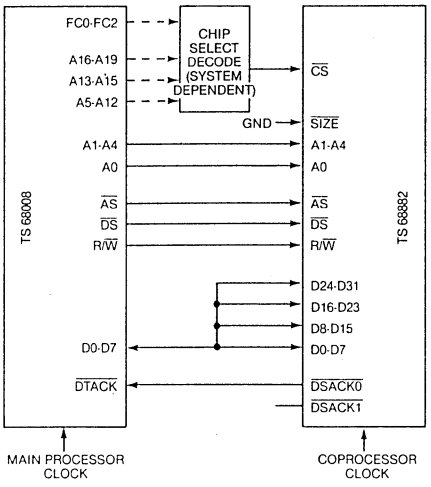


Figure 22 : 8-bit data bus peripheral processor connection.

8-Bit Data Bus Peripheral Processor Connection

Figure 22 illustrates the connection of an TS 68882 to an TS 68008 as a peripheral processor over an 8-bit data bus. The TS 68882 is configured to operate over an 8-bit data bus when the $\overline{SIZE}$ pin is connected to GND. The eight least significant data pins (D0-D7) must be connected to the twenty four most significant data pins (D8-D31) when the TS 68882 is configured to operate over an 8-bit data bus (i.e., connect D0 to D8, D16, and D24 ; D1 to D9, D17, and D25 ; ... and D7 to D15, D23, and D31). The $\overline{DSACK0}$ pin of the TS 68882 is connected to the $\overline{DTACK}$ pin of the TS 68008, and the $\overline{DSACK1}$ pin is not used.

When connected as a peripheral processor, the TS 68882 chip select ($\overline{CS}$) decode is system dependent, and the $\overline{CS}$ must be decoded in the supervisor or user data spaces.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

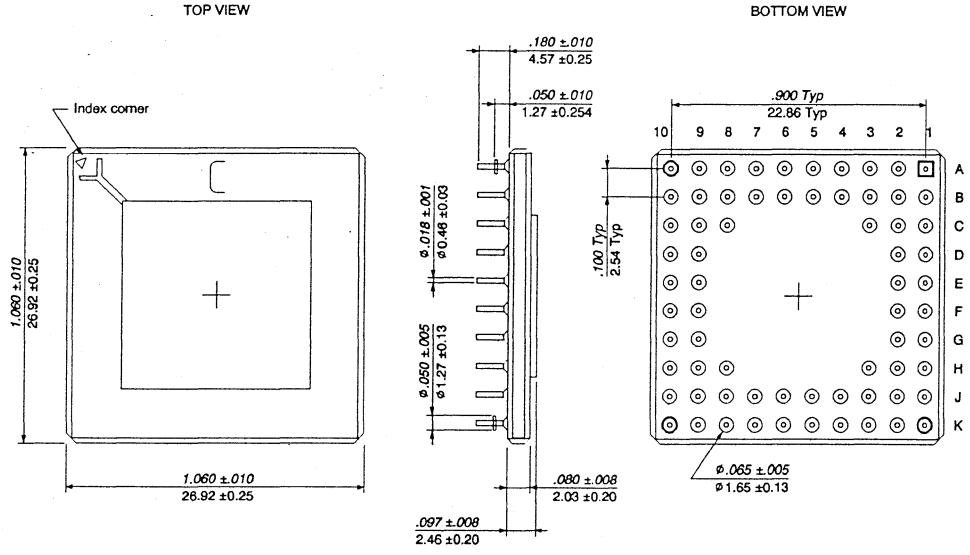
8 · HANDLING

Devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. Howerver, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid us of plastic, rubber, or silk.
f) Maintain relative humidity above 50 %, if practical.

9 · PACKAGE MECHANICAL DATA

9.1 · 68 pins - Ceramic Pin Grid Array



Note 1 : Dimensions A and B are datums and T S datum surface.

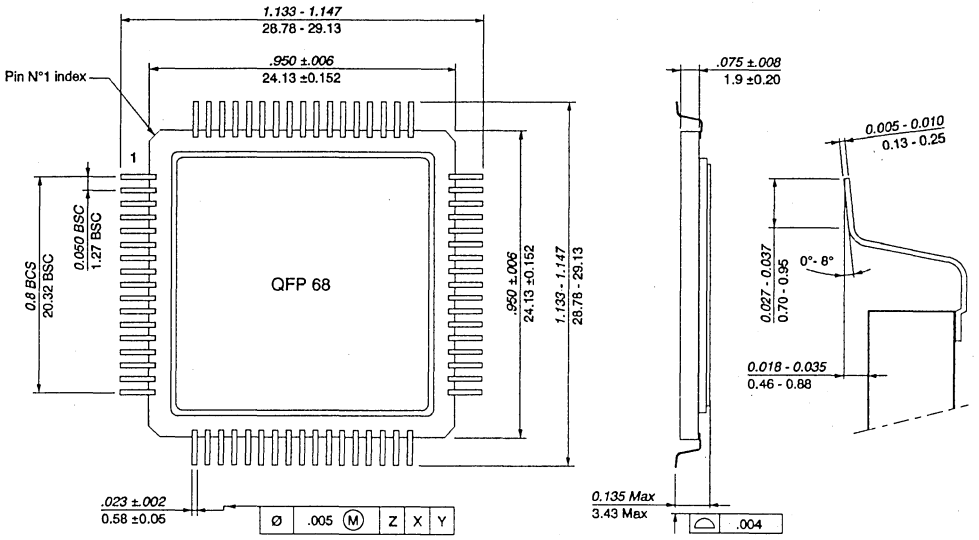
Note 2 : Positional tolerance for leads 168 places :

⌖ ø0.13 (.005) T A S1 B S1

Note 3 : Dimensioning and tolerancing per ANSI Y14 5M 1982.

Note 4 : Controlling dimension : INCH.

9.2 · 68 pins · Ceramic Quad Flat Pack



10 · TERMINAL CONNECTIONS

10.1 · 68 pins · Ceramic Ping Grid Array

See Figure 2.1.

10.2 · 68 pins · Ceramic Quad Flat Pack

See Figure 2.2.

11 - ORDERING INFORMATION

11.1 - Hi-REL product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68882MR8B/Y16	CECC	PGA 68	−55 / +125	16.67	90110-024
TS 68882MR8B/Y20	CECC	PGA 68	−55 / +125	20	90110-024
TS 68882MR8B/Y25	CECC	PGA 68	−55 / +125	25	90110-024
TS 68882MF8B/Y16	CECC	CQFP 68	−55 / +125	16.67	90110-024
TS 68882MF8B/Y20	CECC	CQFP 68	−55 / +125	20	90110-024
TS 68882MF8B/Y25	CECC	CQFP 68	−55 / +125	25	90110-024
TS 68882MRB/C16	MIL-STD-883	PGA 68	−55 / +125	16.67	—
TS 68882MRB/C20	MIL-STD-883	PGA 68	−55 / +125	20	—
TS 68882MRB/C25	MIL-STD-883	PGA 68	−55 / +125	25	—
TS 68882MRB/C33	MIL-STD-883	PGA 68	−55 / +125	33	—
TS 68882MFB/C16	MIL-STD-883	CQFP 68	−55 / +125	16.67	—
TS 68882MFB/C20	MIL-STD-883	CQFP 68	−55 / +125	20	—
TS 68882MFB/C25	MIL-STD-883	CQFP 68	−55 / +125	25	—
TS 68882DESC02XA	DESC	PGA 68	−55 / +125	16.67	5962 8946302XA
TS 68882DESC03XA	DESC	PGA 68	−55 / +125	20	5962 8946303XA
TS 68882DESC04XA	DESC	PGA 68	−55 / +125	25	5962 8946304XA
TS 68882DESC05XA	DESC	PGA 68	−55 / +125	33	5962 8946305XA
TS 68882DESC02YA	DESC	CQFP 68	−55 / +125	16.67	5962 8946302YA
TS 68882DESC03YA	DESC	CQFP 68	−55 / +125	20	5962 8946303YA
TS 68882DESC04YA	DESC	CQFP 68	−55 / +125	25	5962 8946304YA
TS 68882DESC05YA	DESC	CQFP 68	−55 / +125	33	5962 8946305YA

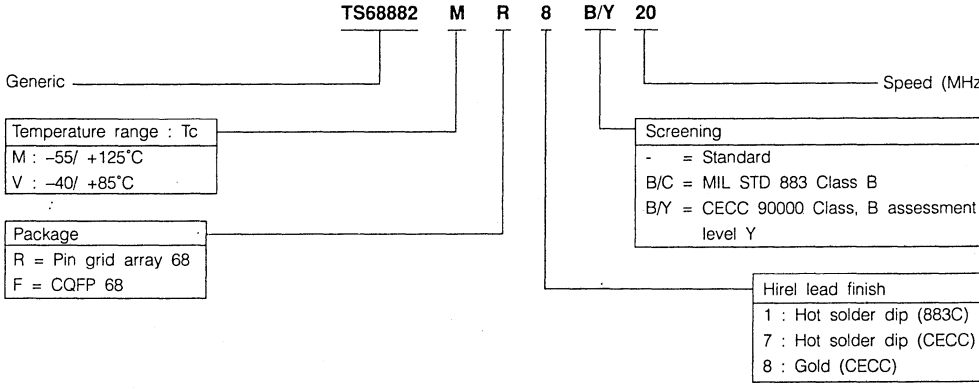
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

5

11.2 · Standard product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS 68882VR16	TCS Standard	PGA 68	−40 / +85	16.67	Internal
TS 68882VR20	TCS Standard	PGA 68	−40 / +85	20	Internal
TS 68882VR25	TCS Standard	PGA 68	−40 / +85	25	Internal
TS 68882VR33	TCS Standard	PGA 68	−40 / +85	33	Internal
TS 68882MR16	TCS Standard	PGA 68	−55 / +125	16.67	Internal
TS 68882MR20	TCS Standard	PGA 68	−55 / +125	20	Internal
TS 68882MR25	TCS Standard	PGA 68	−55 / +125	25	Internal
TS 68882MR33	TCS Standard	PGA 68	−55 / +125	33	Internal
TS 68882VF16	TCS Standard	CQFP 68	−40 / +85	16.67	Internal
TS 68882VF20	TCS Standard	CQFP 68	−40 / +85	20	Internal
TS 68882VF25	TCS Standard	CQFP 68	−40 / +85	25	Internal
TS 68882VF33	TCS Standard	CQFP 68	−40 / +85	33	Internal
TS 68882MF16	TCS Standard	CQFP 68	−55 / +125	16.67	Internal
TS 68882MF20	TCS Standard	CQFP 68	−55 / +125	20	Internal
TS 68882MF25	TCS Standard	CQFP 68	−55 / +125	25	Internal
TS 68882MF33	TCS Standard	CQFP 68	−55 / +125	33	Internal

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.



TS88100

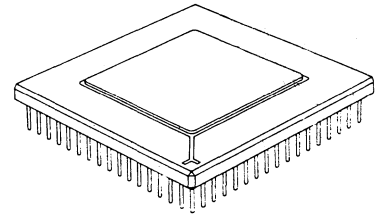
32-BIT RISC MICROPROCESSOR

DESCRIPTION

The TS88100 is the first processor in the TS88000 Family of RISC (reduced instruction set computer) microprocessors. The TS88100 incorporates 32-bit registers, data paths, and addresses. A high degree of fine-grain parallelism has been incorporated in the TS88100 ; four, independent execution units maintain separate, fully concurrent excution pipelines. Most instructions operate in one machine cycle or effective concurrent execution can be accomplished through internal pipelines in one machine cycle. A common register file provides data sharing and synchronization control among the execution units through register scoreboarding.

The TS88100 addresses a variety of applications requiring high operational speeds and efficient, fast execution architectures. All data manipulation instructions are non-destructive register to register or register with immediate operations, allowing both fast operand access and operand reuse. IEEE 754 floating-point arithmetic is supported in the processor. Instruction and data memory space are accessed through separate memory ports, allowing simultaneous access to dedicated memory areas. The TS88000 Family includes the TS88200CMMU (cache/memory management unit), which adds high-speed memory caching, two-level, demand-paged memory management, and support for shared-memory multiprocessing. The TS88100 Family also includes a full line of highly optimizing compilers, operating systems, development boards,and development tools.

NOT FOR NEW DESIGN
Data sheet available on request



R Suffix
PGA 181
(Ceramic Pin Grid Array)

5

MAIN FEATURES

- Single-Clock Integer, Logical, Bit Field, Branch and Store Operations
- Fifty-One Instructions and Seven Data Types
- Fine-Grain Parallelism :
  - Four Fully Independent Execution Units with Concurrent Pipelines
  - Execution Synchronized in Hardware by a Scoreboard Register
- Nondestructive Register and Condition Code Model Allowing Fast Operand Access and Operand Reuse
- Thirty-Two General-Purpose Registers
- Single-and Double-Precision IEEE 754 FloatingPoint Compatibility (Up to One Operation perClock Cycle)
- Full 32-Bit Multiplier
- Separate Data and Instruction Memory Ports (Hardward Bus Stucture) Allowing Simultaneous Accesses :
  - 30-Bit Data Address Bus
  - 32-Bit Data Bus (32-Bit Word)
  - 30-Bit Instruction Address Bus (32-Bit Boun dary Addressing)
  - 32-Bit Instruction Bus (Fixed Instruction Length of 32 Bits)
- Pipelined Load and Store Operations (Up to 80 Mbytes/sec at 20 MHz)
- High-Speed Interrupt Processing with Minimal Interrupt Latency
- Functional Redundancy Fault Detection
- Selectable Big-Endian or Little-Endian Byte Ordering
- Interfaces Directly to Memory or to TS88200 CMMU
- Complex Instruction Sequences Easily Built from Simple Instuctions by High-Level Language Compiler
- Extensible Architecture Facility through Special Function Units.

SCREENING/QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 class B, or according to MIL-STD-883 class B,
- according to TCS standard,
- full military temperature range (– 55°C, + 125°C),
- V_{CC} = 5.0 V ±5 %.
- PGA 181.

TS88200

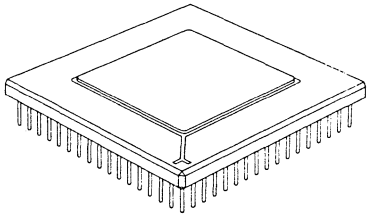
16-KILOBYTE CACHE/MEMORY MANAGEMENT UNIT (CMMU)

DESCRIPTION

The TS88200 CMMU is a high-performance, HCMOS VLSI device providing zero-wait-state memory management and data caching. The MMU (memory management unit) efficiently supports a demand-paged virtual memory environment with two logical address ranges (user/supervisor) of 4 gigabytes each. Translated addresses are provided by one of two ATCs (address translation caches), providing address translation in one clock cycle for most memory accesses. The PATC (page address translation cache) is a 56-entry, fully associative cache containing recently used translations for 4-kilobyte memory pages and is maintained by TS88200 hardware. The BATC (block address translation cache) is a 10-entry cache, loaded by software, containing translations for 512-kilobyte memory blocks. The BATC translations are used for operating system software or for other memory-resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 16-kilobyte, four-way, set-associative cache for instruction or data storage. The cache incorporates memory-update policies and cache-coherency mechanisms that support multiprocessor applications. The TS88200 CMMU also includes an TS88100 compatible P bus (processor bus) interface and an M bus (memory bus) interface.

A processor may use two or more CMMUs for increased data cache and ATC sizes.

NOT FOR NEW DESIGN
Data sheet available on request



R Suffix
PGA 181
(Ceramic Pin Grid Array)

5

MAIN FEATURES

Features of the MMU portion of the TS88200 include :

- Two Logical Address Spaces of 4 Gigabytes Each (User/Supervisor)
- Automatically Maintained PATC and Software-Maintained BATC
- Write Protection for User and Supervisor Accesses
- Used and Modified Flags Maintained in Page Translation Tables
- Probe Capability for Testing the Status of a Memory Location.

Features of the cache portion or the TS88200 include :

- 16-Kilobyte, Four-Way, Set-Associative Physical Cache
- Zero-Wait-State Physical Cache Accesses - Address Translation in Parallel with Cache Access
- LRU (Leat Recently Used) Replacement Algorithm for Each Cache Set
- Cache Entries Allocated with Copyback or Write-through Policies

Multiprocessor support features include :

- Bus Snoop Protocol Keeps the Cache Consistent with Other Caches and with Main Memory
- Cache Flush and Invalidate Initiated Selectively by Software and Automatically by Hardware
- Cache Inhibit Flags on Area, Segment, Page, and Block Basis
- Cache Writethrough or Copyback Selectable on Area, Segment, Page, and Block Basis
- Semaphores for Efficient Multiprocessor Synchronization (In Memory and Cached)
- Data Cache and ATCs Can Be Flushed by Any Processor or I/O Device

Fault-Tolerance application support features include :

- Checker Mode Fault Detection (Functional Redundancy)
- Parity-Protected Memory Bus
- Cache Line Disable Flags

ADVANCE INFORMATION

TS88915T

LOW SKEW CMOS PLL CLOCK DRIVER
3-State 55, 70 and 100 MHz Versions

DESCRIPTION

The TS 88915T Clock Driver utilizes a phazed–locked loop (PLL) technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance microprocessors such as TS68040 and TSPC603e.

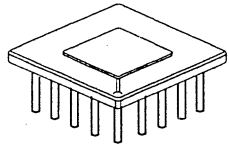
MAIN FEATURES

- **TS68040 & TSPC603e FULL COMPATIBLE**
- **FIVE LOW SKEW OUTPUTS**
  Five Outputs (Q0-Q4) with Output–to–Output skew < 500 ps each being phase end frequency locked to the SYNC input.
- **ADDITIONAL OUTPUTS**
  Three additional outputs are available :
  - The 2X_Q output runs twice the system "Q" frequency
  - The Q/2 output runs at 1/2 the system "Q" frequency
  - The $\overline{Q5}$ output is inverted (180° phase shift)
- **TWO SELECTABLE CLOCK INPUTS**
  - Two selectable CLOCK inputs are available for test or redundancy purposes.
  - Test Mode pin (PLL_EN) provided for low frequency testing.
  - All outputs can go into high impedance (3-state) for board test purpose
- **INPUT FREQUENCY RANGE FROM 5MHz to 2X_Q FMAX**
- **THREE INPUT/OUTPUT RATIOS**
  Input/Output phase–locked frequency ratios of 1:2, 1:1 and 2:1 are available
- **LOW PART-TO-PART SKEW**
  The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew).
- **CMOS AND TTL COMPATIBLE**
  - All outputs can drive either CMOS or TTL inputs
  - All inputs are TTL-level compatible
- **LOCK Indicator (LOCK) Indicated a phase–locked state.**

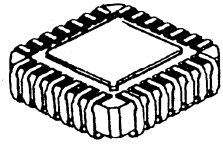
SCREENING/QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 (class B)
- DESC (planned)
- or according to TCS standard



R Suffix
PGA 29
Ceramic Pin grid array



W suffix
LDCC 28
Leaded Ceramic Chip Carrier
(To be confirmed)

5

ADVANCE INFORMATION

TSPC603e

RISC MICROPROCESSOR

DESCRIPTION

The 603e is a low-power implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. The 603e implements 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits.

The 603e is a low-power 3.3-volt design and provides four software controllable power-saving modes.

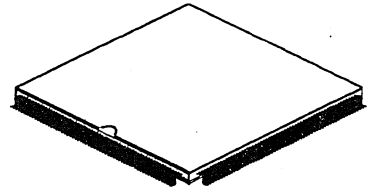
The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance ; however, the 603e makes completion appear sequential. The 603e integrates five execution units and is able to execute five instructions in parallel.

The 603e provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers that provide support for demand-paged virtual memory address translation and variable-sized block translation.

The 603e has a selectable 32 or 64-bit data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to complete for system resources through a central external arbiter. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

The 603e integrates in system testability and debugging features through JTAG boundary-scan capability.



A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier

5

MAIN FEATURES

- 120 SPECint92, 105 SPECfp92 @ 100 MHz.
- Superscalar (3 instructions per clock peak).
- Dual 16KB caches.
- Selectable bus clock.
- 32-bit compatibility PowerPC implementation.
- On chip debug support.
- P_D max = 3 watts, full operating speed and conditions.
- Nap, doze and sleep modes for power savings.
- Branch folding.
- 64-bit data bus (32-bit data bus option).
- 4-Gbyte direct addressing range.
- Pipelined single/double precision float unit. IEEE 754 compatible FPU.
- IEEE P 1149-1 test mode (JTAG/COP).
- f_{int} max = 100 MHz.
- f_{bus} max = 66 MHz.
- Compatible CMOS input
  TTL Output.

SCREENING / QUALITY / PACKAGING

This product is manufactured in full compliance with :

- MIL-STD-883 class B.
- According to TCS standards.
- Full military temperature range (Tj = -55°,+125°C).
- V_{CC} = 3.3 V ± 5 %.
- 240 pin Cerquad.

SUMMARY

A. GENERAL DESCRIPTION

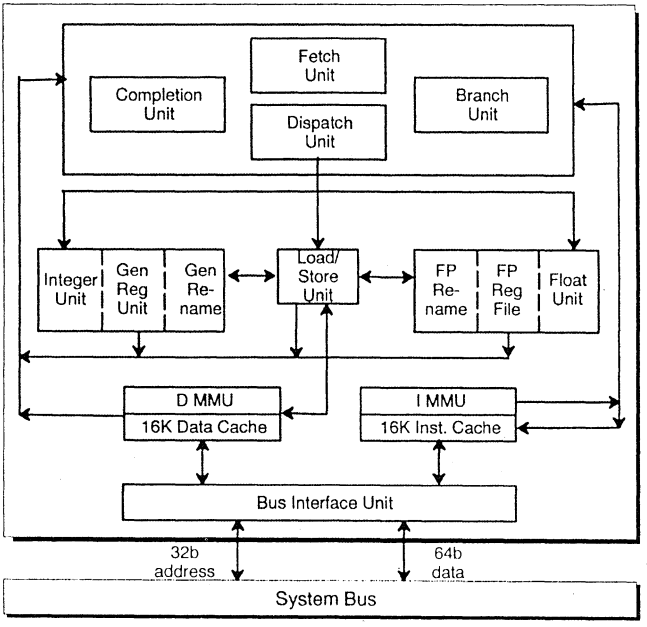


Figure 1 : Block diagram

1. INTRODUCTION

The 603e is a low-power implementation of the PowerPC microprocessor family of reduced instruction set commuter (RISC) microprocessors. The 603e implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603e provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603e to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance ; however, the 603e makes completion appear sequential.

The 603 e integrates five execution units - an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU) and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603e-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603e provides independent on-chip, 16 Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least recently used (LRU) replacement algorithm. The 603e also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The 603e has a selectable 32 - or 64-bit - data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603e provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol as a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 3.3 V CMOS process technology and maintains full interface compatibility with TTL devices.

2. PIN ASSIGNMENTS

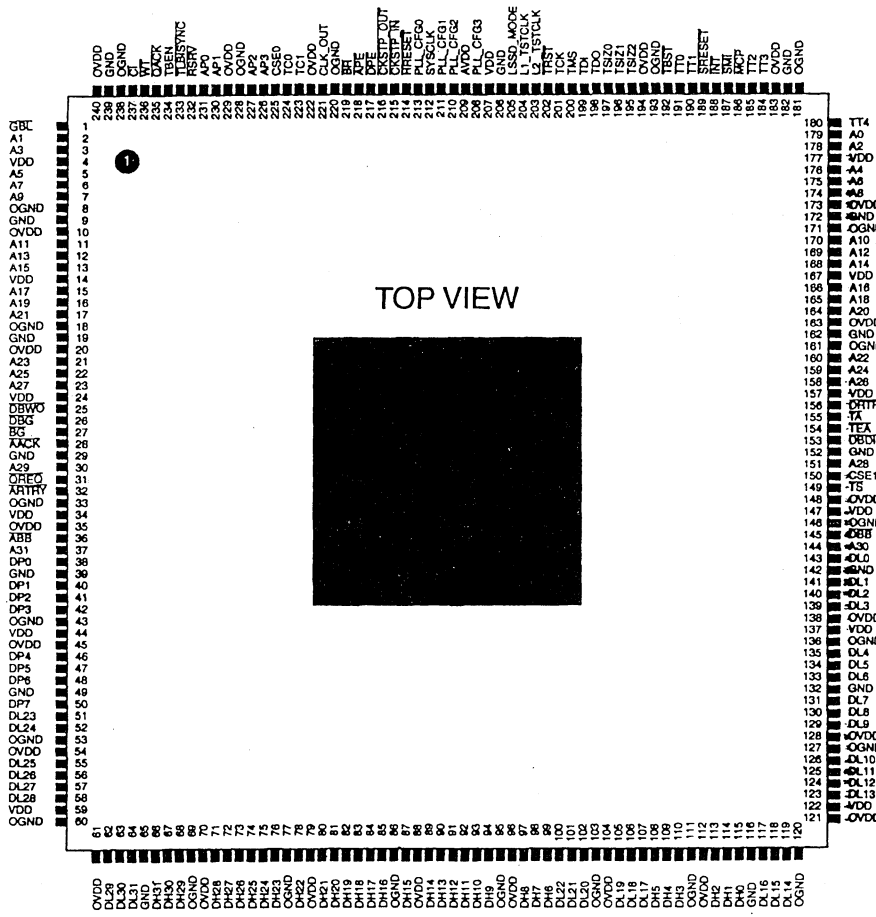


Figure 2 : CQFP 240 : Top view

Table 1 : Power and ground pins

	GND	VCC
PLL		209
Internal logic	9, 19,29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207
Output drivers	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240

3. SIGNAL DESCRIPTION

Figure 3, Table 2 and Table 3 describe the signal on the TSPC603e and indicate signal functions. The test signals, TRST, TMS, TCK, TDI and TDO, comply with subset P-1149.1 of the IEEE testability bus standard.

The 3 signals LSSD_MODE, LI_TSTCLK and L2_TSTCLK are test signals for factory use only and must be pulled up to VDD for normal machine operations.

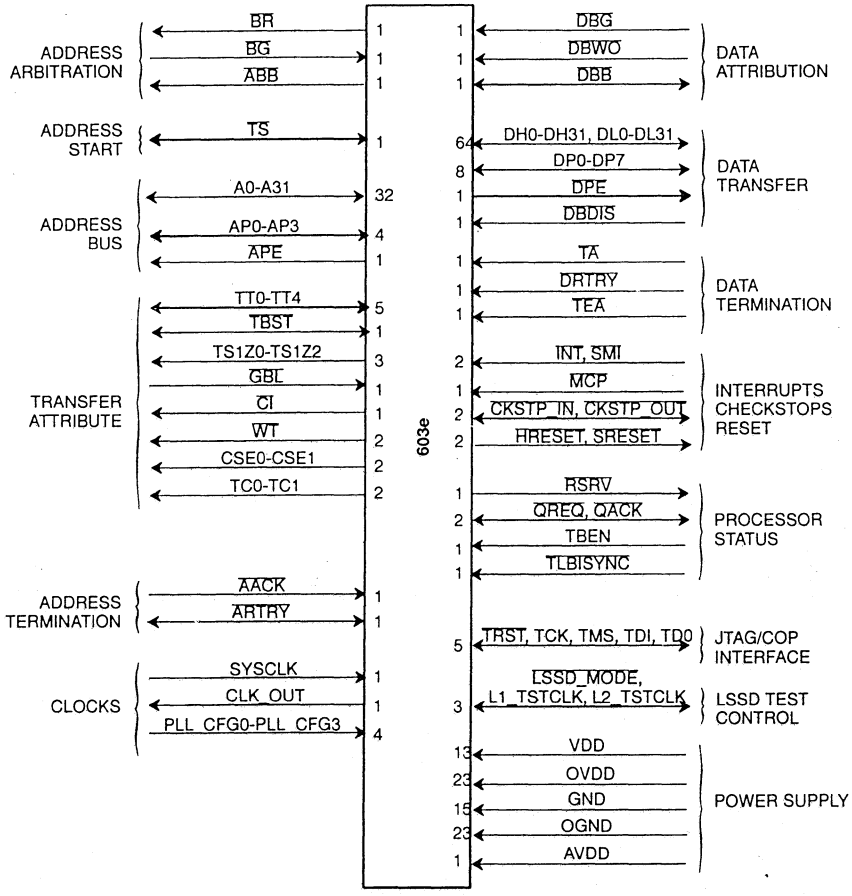


Figure 3 : Functional signal groups

Table 2 : Address and data bus signal index

Signal name	Mnemonic	Pin Number
Address bus	A0-A31	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37
Data bus	DH0-DH31	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75,74, 73, 72, 71, 68, 67, 66
Data bus	DL0-DL31	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64

Table 3 : Signal index

Signal name	Mnemonic	Pinout	Signal function
Address Acknowledge	$\overline{AACK}$	28	The address phase of a transaction is complete
Address Bus Busy	$\overline{ABB}$	36	If output, the 603e is the address bus master If input, the address bus is in use
Address Bus Parity	AP0-AP3	231, 230, 227, 226	If output, represents odd parity for each of 4 bytes of the physical address for a transaction If input, represents odd parity for each of 4 bytes of the physical address for snooping operations
Address Parity Error	$\overline{APE}$	218	Incorrect address bus parity detected on a snoop
Address retry	$\overline{ARTRY}$	32	If output, detects a condition in which a snooped address tenure must be retried If input, must retry the preceding address tenure
Bus grant	$\overline{BG}$	27	May, with the proper qualification, assume mastership of the address bus
Bus request	$\overline{BR}$	219	Request mastership of the address bus
Cache Inhibit	$\overline{CI}$	237	A single-beat transfer will not be cached
Test Clock	CLK_OUT	221	Provides PLL clock output for PLL testing and monitoring
Checkstop Input	$\overline{CKSTP\_IN}$	215	Must terminate operation by internally gating off all clocks, and release all outputs
Checkstop Output	$\overline{CKSTP\_OUT}$	216	Has detected a checkstop condition and has ceased operation
Cache Set Entry	CSE0-CSE1	225, 150	Cache replacement set element for the current transaction reloading into or writing out of the cache
Data Bus Busy	$\overline{DBB}$	145	If output, the 603e is the data bus master If input, another device is bus master
Data Bus Disable	$\overline{DBDIS}$	153	(For a write transaction) must release data bus and the data bus parity to high impedance during the following cycle
Data Bus Grant	$\overline{DBG}$	26	May, with the proper qualification, assume mastership of the data bus
Data Bus Write Only	$\overline{DBW0}$	25	May run the data bus tenure
Data Bus Parity	DP0-DP7	38, 40, 41, 42, 46, 47, 48, 50	If output, odd parity for each of 8 bytes of data write transactions If input, odd parity for each byte of read data
Data Parity Error	$\overline{DPE}$	217	Incorrect data bus parity
Data Retry	$\overline{DRTRY}$	156	Must invalidate the data from the previous read operation
Global	$\overline{GBL}$	1	If output, a transaction is global If input, a transaction must be snooped by the 603e
Hard Reset	$\overline{HRESET}$	214	Initiates a complete hard reset operation
Interrupt	$\overline{INT}$	188	Initiates an interrupt if bit EE of MSR register is set
	$\overline{LSSD\_MODE}$	205	LSSD test control signal for factory use only
	L1_TSTCLK	204	LSSD test control signal for factory use only

	L2_TSTCLK	203	LSSD test control signal for factory use only
Machine Check Interrupt	$\overline{MCP}$	186	Initiates a machine check interrupt operation if the bit ME of MSR register and bit EMCP of HID0 register are set
PLL Configuration	PLL_CFG0-PLL_CFG3	213, 211, 210, 208	Configures the operation of the PLL and the internal processor clock frequency
Quiescent Acknowledge	$\overline{QACK}$	235	All bus activity has terminated and the 603e may enter a quiescent (or low power) state
Quiescent Request	$\overline{QREQ}$	31	Is requesting all bus activity normally to enter a quiescent (low power) state
Reservation	$\overline{RSRV}$	232	Represents the state of the reservation coherency bit in the reservation address register
System Management Interrupt	$\overline{SMI}$	187	Initiates a system management interrupt operation if the bit EE of MSR register is set
Soft Reset	$\overline{SRESET}$	189	Initiates processing for a reset exception
System Clock	SYSCLK	212	Represents the primary clock input for the 603e, and the bus clock frequency for 603e bus operation
Transfer Acknowledge	$\overline{TA}$	155	A single-beat data transfer completed successfully or a data beat in a burst transfer completed successfully
Timebase Enable	TBEN	234	The timebase should continue clocking
Transfer Burst	$\overline{TBST}$	192	If output, a burst transfer is in progress If input, when snooping for single-beat reads
Transfer Code	TC0-TC1	224, 223	Special encoding for the transfer in progress
Test clock	TCK	201	Clock signal for the IEEE P1149.1 test access port (TAP)
Test data input	TDI	199	Serial data input for the TAP
Test data output	TDO	198	Serial data output for the TAP
Transfer Error Acknowledge	$\overline{TEA}$	154	A bus error occurred
TLBI Sync	$\overline{TLBISYNC}$	233	Instruction execution should stop after execution of a **tlbsync** instruction
Test mode select	TMS	200	Selects the principal operations of the test-support circuitry
Test reset	$\overline{TRST}$	202	Provides an asynchronous reset of the TAP controller
Transfer Size	TSIZ0-TSIZ2	197, 196, 195	For memory accesses, these signals along with $\overline{TBST}$ indicate the data transfer size for the current bus operation
Transfer start	$\overline{TS}$	149	If output, begun a memory bus transaction and the address bus and transfer attribute signals are valid If input, another master has begun a bus transaction and the address bus and transfer attribute signals are valid for snooping (see $\overline{GBL}$)
Transfer Type	TT0-TT4	191, 190, 185, 184, 180	Type of transfer in progress
Write-Through	$\overline{WT}$	236	A single-beat transaction is write-through

5

B. DETAILED SPECIFICATIONS

1. SCOPE

This drawing describes the specific requirements for the microprocessor TSPC603e, in compliance with MIL-STD-883 class B or TCS standard screening.

2. APPLICABLE DOCUMENTS

1) MIL-STD-883 : Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A : General specifications for microcircuits.

3. REQUIREMENTS

3.1. General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2. Design and construction

3.2.1. Terminal connections

Depending on the package, the terminal connections shall be is shown in Figure 2 and Figure 3 (§ A. GENERAL DESCRIPTION).

3.2.2. Lead material and finish

Lead material and finish shall be as specified in MIL-STD-1835 (see enclosed § 10.).

3.2.3. Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-STD-1835 or to CQFP 240, but see § 8.

The precise case outlines are described at the end of the specification (§ 8.) and into MIL-STD-1835.

3.3. Electrical characteristics

3.3.1. Absolute maximum ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 4 : Absolute maximum rating for the 603e

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	-0.3	4.0	V
Input voltage	V_{in}	-0.3	5.5	V
Storage temperature range	T_{stg}	-55	+150	°C
Power dissipation	P_D		3.5	W
Operating temperature (junction)	T_j	-55	+125	°C

Note 1 : Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the absolute maximums listed may affect device reliability or cause permanent damage to the device.

Note 2 : **Caution** : input voltage must not be greater than the supply voltage by more than 2.5 V at all times including during power-on reset.

3.4. Power consideration

The PowerPC603e microprocessor is the first microprocessor specifically designed for low-power operation. The 603e provides both automatic and program-controllable power reduction modes for progressive reduction of power consumption. This chapter describes the hardware support provided by the 603e for power management.

3.4.1. Dynamic Power Management

Dynamic power management automatically powers up and down the individual execution units of the 603e, based upon the contents of the instruction stream. For example, if no floating-point instructions are being executed, the floating-point unit is automatically powered down. Power is not actually removed from the execution unit ; instead, each execution unit has an independent clock input, which is automatically controlled on a clock-by- clock basis. Since CMOS circuits consume negligible power when they are not switching, stopping the

clock to an execution unit effectively eliminates its power consumption. The operation of DPM is completely transparent to software or any external hardware. Dynamic power management is enabled by setting bit 11 in HID0 on power-up, of following $\overline{\text{HRESET}}$.

3.4.2. Programmable Power Modes

The 603e provides four programmable power states - full power, doze, nap and sleep. Software selects these modes by setting one (and only one) of the three power saving mode bits. Hardware can enable a power management state through external asynchronous interrupts The hardware interrupt causes the transfer of program flow to interrupt handler code. The appropriate mode is then set by the software. The 603e provides a separate interrupt and interrupt vector for power management - the system management interrupt (SMI). The 603e also contains a decrement timer which allows it to enter the nap or doze mode for a predetermined amount of time and then return to full power operation through the decrementer interrupt (DI). Note that the 603e cannot switch from on power management mode to another without first returning to full on mode. The nap and sleep modes disable bus snooping ; therefore, a hardware handshake is provided to ensure coherency before the 603e enters these power management modes. Table 5 summarizes the four power states.

Table 5 : Power PC 603e Microprocessor Programmable Power Modes

PM Mode	Functioning Units	Activation Method	Full-Power Wake Up Method
Full power	All units active	–	–
Full power (with DPM)	Requested logic by demand	By instruction dispatch	–
Doze	- Bus snooping - Data cache as needed - Decrementer timer	Controlled by SW	External asynchronous exceptions* Decrementer interrupt Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous exceptions Decrementer interrupt Reset
Sleep	None	Controlled by hardware and software	External asynchronous exceptions Reset

* Exceptions are referred to as interrupts in the architecture specification

3.4.3. Power Management Modes

The following sections describe the characteristics of the 603e"s power management modes, the requirements for entering and exiting the various modes, and the system capabilities provided by the 603e while the power management modes are active.

3.4.3.1. Full-Power Mode with DPM Disabled

Full-power mode with DPM disabled power mode is selected when the DPM enable bit (bit 11) in HID0 is cleared.

- Default state following power-up and $\overline{\text{HRESET}}$.
- All functional units are operating at full processor speed at all times.

3.4.3.2. Full-Power Mode with DPM Enabled

Full-power mode with DPM enabled (HID0[11] = 1) provides on-chip power management without affecting the functionality or performance of the 603e.

- Required functional units are operating at full processor speed.
- Functional units are clocked only when needed.
- No software or hardware intervention required after mode is set.
- Software/hardware and performance transparent.

3.4.3.3. Doze Mode

Doze ode disables most functional units but maintains cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the 603e to enable the data cache, copy the data back to memory, disable the cache, and fully return to the doze state.

- Most functional units disabled.
- Bus snooping and time base/decrementer still enabled.
- Dose mode sequence :
  - Set doze bit (HID0[8] = 1).
  - 603e enters doze mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$ or decrementer interrupts.
  - Assert hard reset or soft reset.

- Transition to full-power state takes no more than a few processor cycles.
- PLL running and locked to SYSCLK.

3.4.3.4. Nap Mode

The nap mode disables the 603e but still maintains the phase locked loop (PLL) and the time base/decrementer. The time base can be used to restore the 603e to full-on state after a programmed amount of time. Because bus snooping is disabled for nap and sleep mode, a hardware handshake using the quiesce request ($\overline{QREQ}$) and quiesce acknowledge ($\overline{QACK}$) signals are requires to maintain data coherency. The 603e will assert the $\overline{QREQ}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{QACK}$ and the 603e will enter the sleep or nap mode.

- Time base/decrementer still enabled.
- Most functional units disabled (including bus snooping).
- All nonessential input receivers disables.
- Nap mode sequence :
  - Set nap bit (HID0[9] = 1).
  - 603e asserts quiesce request ($\overline{QREQ}$) signal.
  - System asserts quiesce acknowledge ($\overline{QACK}$) signal.
  - 603e enters sleep mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{INT}$, $\overline{SPI}$, $\overline{MCP}$ or decrementer interrupts.
  - Assert hard reset or soft reset.
- Transition to full-power takes no more than a few processor cycles.
- PLL running and locked to SYSCLK.

3.4.3.5. Sleep Mode

Sleep mode consumes the least amount of power of the four modes since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Due to the fully static design of the 603e, internal processor state is preserved when no internal clock is present. Because the time base and decrementer are disabled while the 603e is in sleep mode, the 603e's time base contents will have to be updated from an external time base following sleep mode if accurate time-of-day maintenance is required. Before the 603e enters the sleep mode, the 603e will assert the $\overline{QREQ}$ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert $\overline{QACK}$ and the 603e will enter the sleep mode.

- All functional units disabled (including bus snooping and time base).
- All nonessential input receivers disabled :
  - Internal clock regenerators disabled.
  - PLL still running (see below).
- Sleep mode sequence :
  - Set sleep bit (HID0[10] = 1).
  - 603e asserts quiesce request ($\overline{QREQ}$).
  - System asserts quiesce acknowledge ($\overline{QACK}$).
  - 603e enters sleep mode after several processor clocks.
- Several methods of returning to full-power mode :
  - Assert $\overline{INT}$, $\overline{SMI}$, or $\overline{MCP}$ interrupts.
  - Assert hard reset or soft reset.
- PLL may be disabled and SYSCLK may be removed while in sleep mode.
- Return to full-power mode after PLL and SYSCLK disabled in sleep mode :
  - Enable SYSCLK.
  - Reconfigure PLL into desired processor clock mode.
  - System logic waits for PLL startup and relock time (100 µsec).
  - System logic asserts one of the sleep recovery signals (for example, INT or SMI).

3.4.4. Power Management Software Considerations

Since the 603e is a dual issue processor with out-of-order execution capability, care must be taken in how the power management mode is entered. Furthermore, nap and sleep modes require all outstanding bus operations to be completed before the power management mode is entered. Normally during system configuration time, one of the power management modes would be selected by setting the appropriate HID0 mode bit. Later on, the power management mode is invoked by setting the MSR[POW] bit. To provide a clean transition into and out of the power management mode, the **stmsr**[POW] should be preceded by a **sync** instruction and followed by an **isync** instruction.

3.4.5. Power dissipation

Table 6 : Power dissipation

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_J ≤ 125°C

CPU clock:SYSCLK		Processor (CPU) frequency		Unit
		80 MHz	100 MHz	
Full-On Mode (DPM Enabled)				
1.5:1	Typical	TBD	TBD	W
	Max	TBD	TBD	W
2:1	Typical	2.1	TBD	W
	Max	3.0	TBD	W
2.5:1	Typical	TBD	2.4	W
	Max	TBD	3.5	W
3:1	Typical	TBD	TBD	W
	Max	TBD	TBD	W
3.5:1	Typical	TBD	TBD	W
	Max	TBD	TBD	W
4:1	Typical	TBD	TBD	W
	Max	TBD	TBD	W
Doze Mode[1]				
1.5:1	Typical	TBD	TBD	mW
2:1	Typical	1.5	TBD	mW
2.5:1	Typical	TBD	1.9	mW
3:1	Typical	TBD	TBD	mW
3.5:1	Typical	TBD	TBD	mW
4:1	Typical	TBD	TBD	mW
Nap Mode[1]				
1.5:1	Typical	TBD	TBD	mW
2:1	Typical	60	TBD	mW
2.5:1	Typical	TBD	116	mW
3:1	Typical	TBD	TBD	mW
3.5:1	Typical	TBD	TBD	mW
4:1	Typical	TBD	TBD	mW
Sleep Mode[1]				
1.5:1	Typical	TBD	TBD	mW
2:1	Typical	41	TBD	mW
2.5:1	Typical	TBD	103	mW
3:1	Typical	TBD	TBD	mW
3.5:1	Typical	TBD	TBD	mW
4:1	Typical	TBD	TBD	mW
Sleep Mode-PLL Disabled[1]				
1.5:1	Typical	TBD	TBD	mW
2:1	Typical	18	TBD	mW
2.5:1	Typical	TBD	26	mW
3:1	Typical	TBD	TBD	mW
3.5:1	Typical	TBD	TBD	mW
4:1	Typical	TBD	TBD	mW
Sleep Mode-PLL and SYSCLK Disabled[1]				
1.5:1	Typical	TBD	TBD	mW
2:1	Typical	TBD	TBD	mW
2.5:1	Typical	TBD	TBD	mW
3:1	Typical	TBD	TBD	mW
3.5:1	Typical	TBD	TBD	mW
4:1	Typical	TBD	TBD	mW

Note 1 : The values provided for this mode do not include pad driver power (OVDD) or analog supply power (AVDD). Worst-case AVDD = 15 mW

5

4. ELECTRICAL CHARACTERISTICS

4.1. General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 7 : Static electrical characteristics for the electrical variants.
- Table 8 : Dynamic electrical characteristics for the 603e.

These specifications are for 80 MHz and 100 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0_PLL_CFG3 signals. All timings are specified respective to the rise edge of SYSCLK.

4.2. Static characteristics

Table 7 : Electrical characteristics

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, $-55°C \leq T_J \leq 125°C$

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current, V_{in} = 3.465 V[1]	I_{in}	—	10	µA
V_{in} = 5.5 V[1]	I_{in}	—	245	µA
Hi-Z (off-state) leakage current, V_{in} = 3.465 V[1]	I_{TSI}	—	10	µA
V_{in} = 5.5 V[1]	I_{TSI}	—	245	µA
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 14 mA	V_{OL}	—	0.4	V
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10.0	pF
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15.0	pF

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals).

2. Capacitance is periodically sampled rather than 100% tested.

4.3. Dynamic characteristics

4.3.1. Clock AC specifications

Table 8 provides the clock AC timing specifications as defined in Figure 4.

Table 8 : Clock AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, −55°C ≤ T_J ≤ 125°C

Num	Characteristic	80 MHz		100 MHz		Unit	Notes
		Min	Max	Min	Max		
	Processor frequency	40	80	50	100	MHz	5
	VCO frequency	100	200	100	200	MHz	5
	SYSCLK (bus) frequency	16.67	66.67	16.67	66.67	MHz	
1	SYSCLK cycle time	15.0	60.0	15.0	60.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	ns	1
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	%	3
8	SYSCLK jitter	—	±150	—	±150	ps	2
9	603e internal PLL relock time	—	100	—	100	µs	3, 4

Notes:

1. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
2. Cycle-to-cycle jitter, and is guaranteed by design.
3. Timing is guaranteed by design and characterization, and is not tested.
4. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution:** The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG0–PLL_CFG3 signal description in Section 1.8, "System Design Information," for valid PLL_CFG0–PLL_CFG3 settings, and to Section 1.9, "Ordering Information," for available frequencies and part numbers.

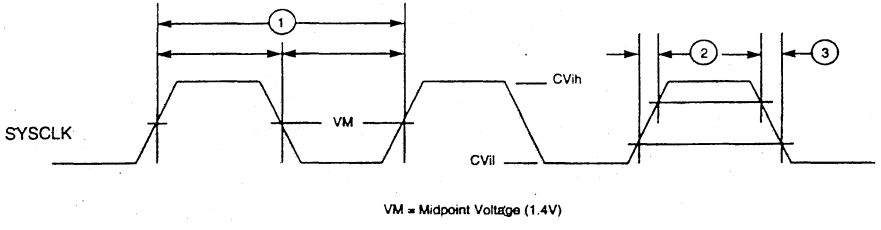


Figure 4 : SYSCLK input timing diagram

4.3.2. Input AC specifications

Table 9 provides the input AC timing specifications for the 603e as defined in Figure 5 and Figure 6. These specifications are for 80 and 100 MHz processor core frequencies.

Table 9 : Input AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_J ≤ 125°C

Num	Characteristic	80 MHz		100 MHz		Unit	Notes
		Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	3.0	—	2.5	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	5.0	—	4.5	—	ns	3
10c	Mode select inputs valid to HRESET (input setup) (for DRTRY, QACK and TLBISYNC)	8 * t_{sys}	—	8 * t_{sys}	—	ns	4, 5, 6, 7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	—	1.0	—	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	—	1.0	—	ns	3
11c	HRESET to mode select inputs invalid (input hold) (for DRTRY, QACK, and TLBISYNC)	0	—	0	—	ns	4, 6, 7

Notes: 1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 2.

2. Address/data/transfer attribute input signals are composed of the following: A0–A31, AP0–AP3, TT0–TT4, TC0-TC1, TBST, TSIZ0–TSIZ2, GBL, DH0–DH31, DL0–DL31, DP0–DP7.

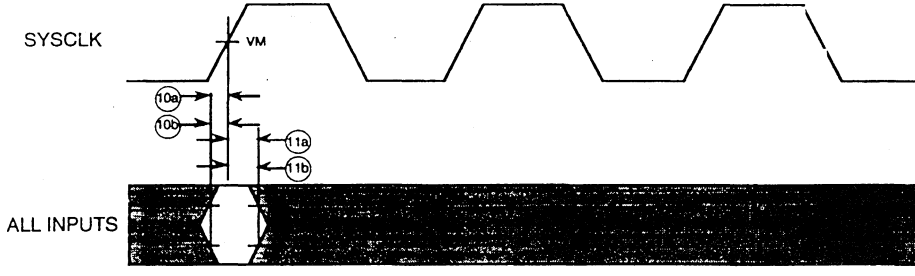
3. All other input signals are composed of the following: TS, ABB, DBB, ARTRY, BG, AACK, DBG. DBWO, TA, DRTRY, TEA, DBDIS,HRESET, SRESET, INT, SMI, MCP, TBEN, QACK, TLBISYNC.

4. The setup and hold time is with respect to the rising edge of HRESET. See Figure 3.

5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.

6. These values are guaranteed by design, and are not tested.

7. This specification is for configuration mode only. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.



VM = Midpoint Voltage (1.4V)

Figure 5 : Input timing diagram

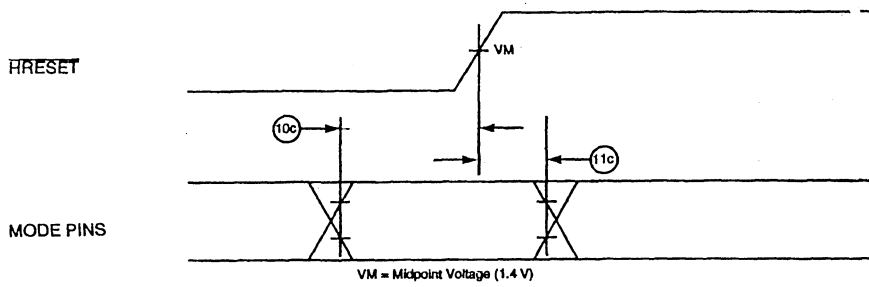


Figure 6 : Mode select input timing diagram

4.3.3. Output AC specifications

Table 10 provides the output AC timing specifications for the 603e (shown in Figure 7). These specifications are for 80 and 100 MHz processor core frequencies.

Table 10 : Output AC timing specifications

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, C_L = 50 pF, –55°C ≤ T_J ≤ 125°C

Num	Characteristic	80 MHz		100 MHz		Unit	Notes
		Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	–	1.0	–	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	10.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	10.0	–	9.0	ns	6
14a	SYSCLK to output valid (5.5 V to 0.8 V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	13.0	–	12.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	10.0	ns	6
15	SYSCLK to output invalid (output hold)	1.5	–	1.5	–	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	9.5	–	8.5	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1.2	–	1.2	t_{sys}	5, 7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	9.0	–	8.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * tsys + 1.0	–	0.2 * tsys + 1.0	–	ns	3, 5, 8
20	Maximum dalay to $\overline{ARTRY}$ precharge	–	1.2	–	1.2	t_{sys}	5, 8
21	SYSCLK to $\overline{ARTRY}$ high impedance after pre-charge	–	2.25	–	2.25	t_{sys}	5, 8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin. See.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).
5. t_{sys} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.

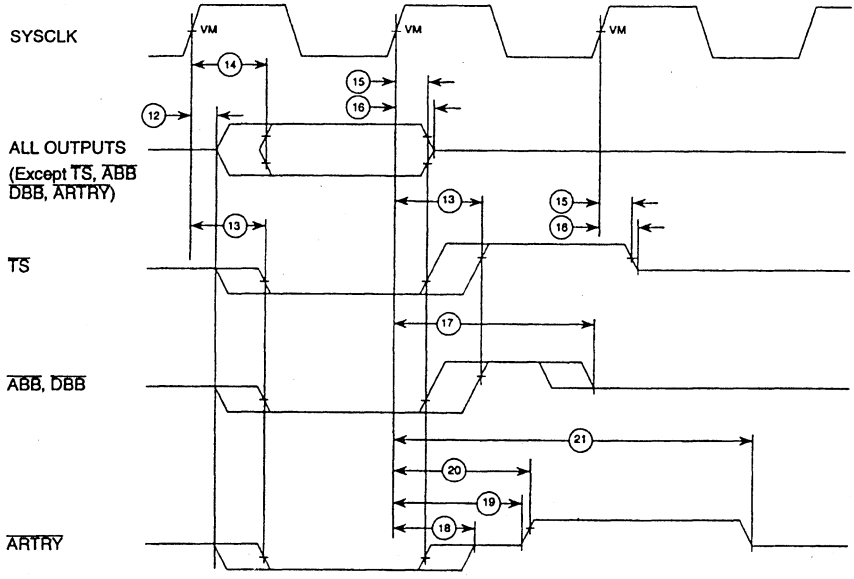


Figure 7 : Output timing diagram

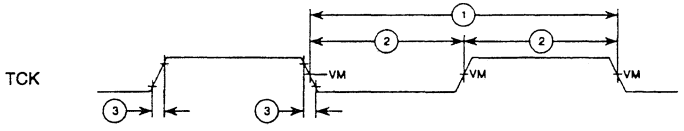
4.4. JTAG AC timing specifications

Table 11 : JTAG AC timing specifications (independent of SYSCLK)

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, C_L = 50 pF, −55°C ≤ T_J ≤ 125°C

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary scan input data setup time	6	—	ns	2
7	Boundary scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes: 1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.



VM = Midpoint Voltage (1.4 V)

Figure 8 : Clock input timing diagram

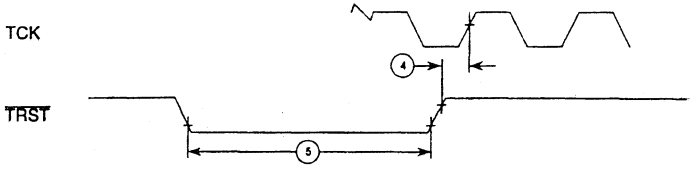


Figure 9 : $\overline{\text{TRST}}$ timing diagram

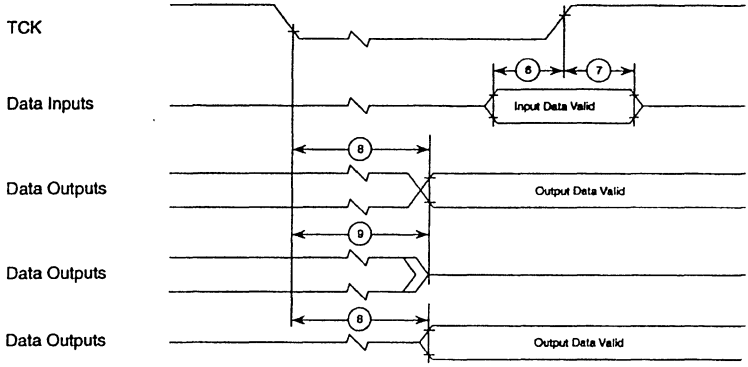


Figure 10 : Boundary-scan timing diagram

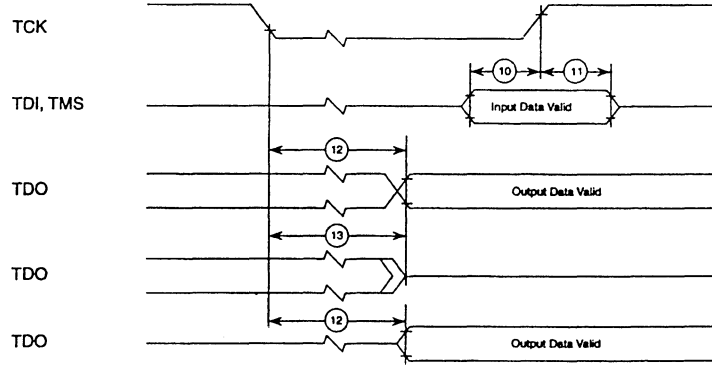


Figure 11 : Test access port timing diagram

5. FUNCTIONAL DESCRIPTION

5.1. PowerPC registers and programming model

The PowerPC architecture defines register-to-register operations for most computational instructions. Source operands for these instructions are accessed from the registers or are provided as immediate values embedded in the instruction opcode. The three-register instruction format allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory.

PowerPC processors have two levels of privilege - supervisor mode of operation (typically used by the operating system) and user mode of operation (used by the application software). The programming models incorporate 32 GPRs, 32 FPRs, special-purpose registers (SPRs) and several miscellaneous registers. Each PowerPC microprocessor also has its own unique set of hardware implementation (HID) registers.

Having access to privilege instructions, registers, and other resources allows the operating system to control the application environment (providing virtual memory and protecting operating-system and critical machine resources). Instructions that control the state of the processor, the address translation mechanism, and supervisor registers can be executed only when the processor is operating in supervisor mode.

The following sections summarize the PowerPC registers that are implemented in the 603e.

5.1.1. General-Purpose Registers (GPRs)

The PowerPC architecture defines 32 user-level, general-purpose registers (GPRs). These registers are either 32 bits wide in 32-bit PowerPC microprocessors and 64 bits wide in 64-bit PowerPC microprocessors. The GPRs serve as the data source or destination for all integer instructions.

5.1.2. Floating-Point Registers (FPRs)

The PowerPC architecture also defines 32 user-level, 64-bit floating-point registers (FPRs). The FPRs serve as the data source or destination for floating-point instructions. These registers can contain data objects of either single - or double - precision floating-point formats.

5.1.3. Condition Register (CR)

The CR is a 32-bit user-level register that consists of eight four-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

5.1.4. Floating-Point Status and Control Register (FPSCR)

The floating-point status and control register (FPSCR) is a user-level register that contains all exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.

5.1.5. Machine State Register (MSR)

The machine state register (MSR) is a supervisor-level register that defines the state of the processor. The contents of this register are saved when an exception is taken and restored when the exception handling completes. The 603e implements the MSR as a 32-bit register, 64-bit PowerPC processors implement a 64-bit MSR.

5.1.6. Segment Registers (SRs)

For memory management, 32-bit PowerPC microprocessors implement sixteen 32-bit segment registers (SRs). To speed access, the 603e implements the segment registers as two arrays ; a main array (for data memory accesses) and a shadow array (for instruction memory accesses). Loading a segment entry with the Move to Segment Register (stsr) instruction loads both arrays.

5.1.7. Special-Purpose Registers (SPRs)

The powerPC operating environment architecture defines numerous special-purpose registers that serve a variety of functions, such as providing controls, indicating status, configuring the processor, and performing special operations. During normal execution, a program can access the registers, shown in Figure 12, depending on the program's access privilege (supervisor or user, determined by the privilege-level (PR) bit in the MSR). Note that register such as the GPRs and FPRs are accessed through operands that are part of the instructions. Access to registers can be explicit (that is, through the use of specific instructions for that purpose such as Move to Special-Purpose Register (mtspr) and Move from Special-Purpose Register (mfspr) instructions) or implicit, as the part of the execution of an instruction. Some registers are accessed both explicitly and implicitly.

Il the 603e, all SPRs are 32 bits wide.

5.1.7.1. User-Level SPRs

The following 603e SPRs are accessible by user-level software :

- Link register (LR) - The link register can be used to provide the branch target address and to hold the return address after branch and link instructions. The LR is 32 bits wide in 32-bit implementations.
- Count register (CTR) - The CRT is decremented and tested automatically as a result of branch-and-count instructions. The CTR is 32 bits wide in 32-bit implementations.
- Integer exception register (XER) - The 32-bit XER contains the summary overflow bit, integer carry bit, overflow bit, and a field specifying the number of bytes to be transferred by a Load String Word Indexed (lswx) or Store String Word Indexed (stswx) instruction.

5.1.7.2. Supervisor-Level SPRs

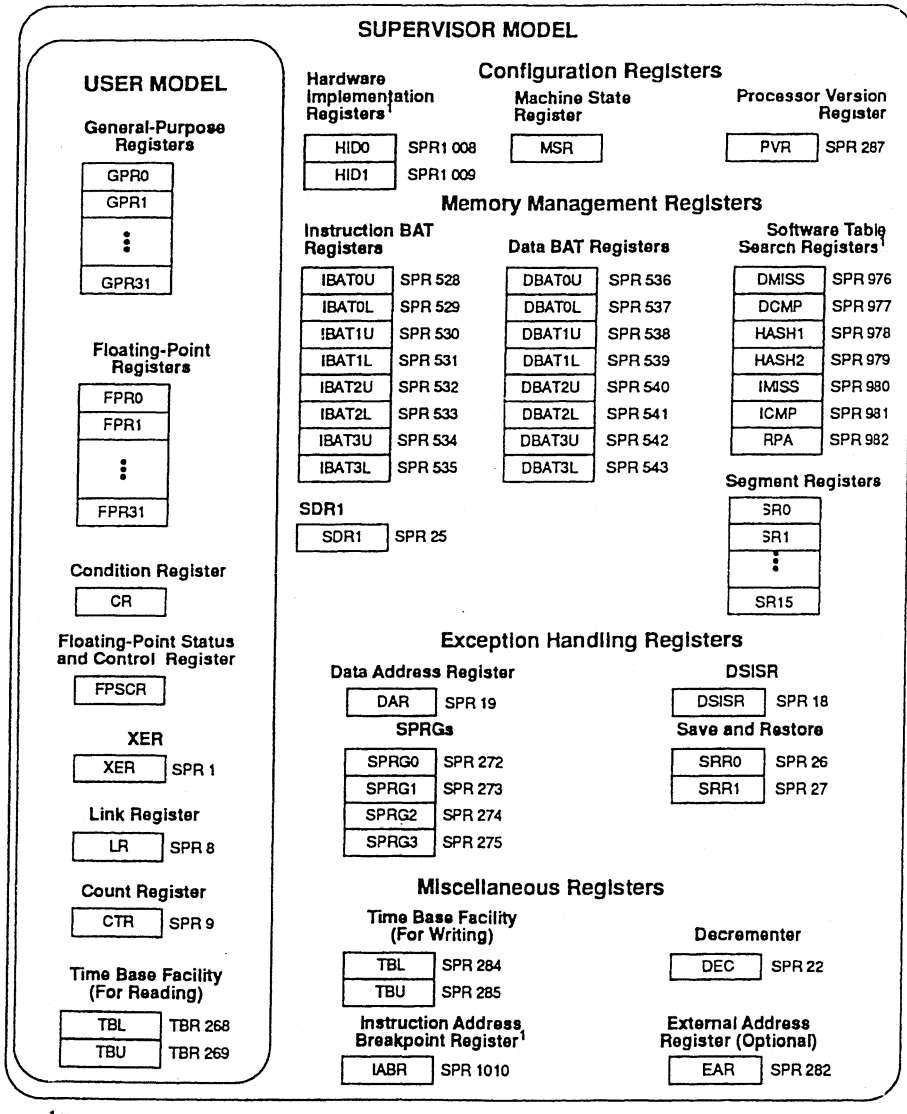
The 603e also contains SPRs that can be accessed only by supervisor-level software. These registers consist of the following :

- The 32-bit DSISR defines the cause of data access and alignment exceptions.
- The data address register (DAR) is a 32-bit register that holds the address of an access after an alignment or DSI exception.
- Decrementer register (DEC) is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.
- The 32-bit SDR1 specifies the page table format used in virtual-to-physical address translation for pages. (Note that physical address is referred to as real address in the architecture specification).
- The machine status save/restore register 0 (SRR0) is a 32-bit register that is used by the 603e for saving the address of the instruction that caused the exception, and the address to return to when a Return from Interrupt (**rfi**) instruction is executed.
- The machine status save/restore register 1 (SRR1) is a 32-bit register used to save machine status on exceptions and to restore machine status when an **rfi** instruction is executed.
- The 32-bit SPRG0-SPRG3 registers are provided for operating system use.
- The external access register (EAR) is a 32-bit register that controls access to the external control facility through the External Control In Word Indexed (**eciwx**) and External Control Out Word Indexed (**ecowx**) instructions.
- The time base register (TB) is a 64-bit register that maintains the time of day and operates interval timers. The TB consists of two 32-bit fields - time base upper (TBU) and time base lower (TBL).
- The processor version register (PVR) is a 32-bit, read-only register that identifies the version (model) and revision level of the PowerPC processor.
- Block address translation (BAT) arrays - The PowerPC architecture defines 16 BAT registers, divided into four pairs of data BATs (DBATs) and four pairs of instruction BATs (IBATs). See Figure 12 for a list of the SPR numbers for the BAT arrays.

The following supervisor-level SPRs are implementation-specific to the 603e :

- The DMISS and IMISS registers are read-only registers that are loaded automatically upon an instruction or data TLB miss.
- The HASH1 and HASH2 registers contain the physical addresses of the primary and secondary page table entry groups (PTEGs).
- The ICMP and DCMP registers contain a duplicate of the first word in the page table entry (PTE) for which the table search is looking.
- The required physical address (RPA) register is loaded by the processor with the second word of the correct PTE during a page table search.
- The hardware implementation (HID0 and HID1) registers provide the means for enabling the 603e"s checkstops and features, and allows software to read the configuration of the PLL configuration signals.
- The instruction address breakpoint register (IABR) is loaded with an instruction address that is compared to instruction addresses in the dispatch queue. When an address match occurs, an instruction address breakpoint exception is generated.

Figure 12 shows all the 603e registers available at the user and supervisor level. The number to the right of the SPRs indicate the number that is used in the syntax of the instruction operands to access the register.



[1] These registers are 603e–specific registers. They may not be supported by other PowerPC processors.

Figure 12 : PowerPC microprocessor programming model - Register

5.2. Instruction set and addressing modes

The following subsections describe the PowerPC instruction set and addressing modes in general.

5.2.1. PowerPC instruction set and addressing modes

All PowerPC instructions are encoded as single-word (32-bit) opcodes. Instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses. This fixed instruction length and consistent format greatly simplifies instruction pipelining.

5.2.1.1. PowerPC instruction set

The PowerPC instructions are divided into the following categories :

- **Integer instructions** - These include computational and logical instructions.
  - Integer arithmetic instructions.
  - Integer compare instructions.
  - Integer logical instructions.
  - Integer rotate and shift instructions.
- **Floating-point instructions** -These include floating-point computational instructions, as well as instructions that affect the FPSCR.
  - Floating-point arithmetic instructions.
  - Floating-point multiply/add instructions.
  - Floating-point rounding and conversion instructions.
  - Floating-point compare instructions.
  - Floating-point status and control instructions.
- **Load/store instructions** - These include integer and floating-point load and store instructions.
  - Integer load and store instruction.
  - Integer load and store multiple instructions.
  - Floating-point load and store.
  - Primitives used to construct atomic memory operations (**lwarx** and **stwcx.** instructions).
- **Flow control instructions** - These include branching instructions, condition register logical instructions, trap instructions, and other instructions that affect the instruction flow.
  - Branch and trap instructions.
  - Condition register logical instructions.
- **Processor control instructions** - These instructions are used for synchronizing memory accesses and management of caches, TLBs, and the segment registers.
  - Move to/from SPR instructions.
  - Move to/from MSR.
  - Synchronize.
  - Instruction synchronize.
- **Memory control instruction** - These instructions provide control of caches, TLBs, and segment registers.
  - Supervisor-level cache management instructions.
  - User-level cache instructions.
  - Segment register manipulation instructions.
  - Translation lookaside buffer management instructions.

Note that this grouping of the instructions does not indicate which execution unit executes a particular instruction or group of instructions.

Integer instructions operate on byte, half-word, and word operands. Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands. The PowerPC architecture uses instructions that are four bytes long and word-aligned. It provides for byte, half-word, and word operand loads and stores between memory and a set of 32 GPRs. It also provides for word and double-word operand loads and stores between memory and a set of 32 floating-point registers (FPRs).

Computational instructions do not modify memory. To use a memory operand in a computation and then modify the same or another memory location, the memory contents must be loaded into a register, modified, and then written back to the target location with distinct instructions.

PowerPC processors follow the program flow when they are in the normal execution state. However, the flow of instructions can be interrupted directly by the execution of an instruction or by an asynchronous event. Either kind of exception may cause one of several components of the system software to be invoked.

5.2.1.2. Calculating effective addresses

The effective address (EA) is the 32-bit address computed by the processor when executing a memory access or branch instruction or when fetching the next sequential instruction.

The PowerPC architecture supports two simple memory addressing modes :

- EA = (RA|0) + offset (including offset = 0) (register indirect with immediate index).
- EA = (RA|0) + rB (register indirect with index).

These simple addressing modes allow efficient address generation for memory accesses. Calculation of the effective address for aligned transfers occurs in a single clock cycle.

For a memory access instruction, if the sum of the effective address and the operand length exceeds the maximum effective address, the memory operand is considered to wrap around from the maximum effective address to effective address 0.

Effective address computations for both data and instruction accesses use 32-bit unsigned binary arithmetic. A carry from bit 0 is ignored in 32-bit implementations.

5.2.2. PowerPC 603e microprocessor instruction set

The 603e instruction set is defined as follows :

- The 603e provides hardware support for all 32-bit PowerPC instructions.
- The 603e provides two implementation-specific instructions used for software table search operations following TLB misses :
  - Load Data TLB Entry (**tlbld**).
  - Load Instruction TLB Entry (**tlbli**).
- The 603e implements the following instructions which are defined as optional by the PowerPC architecture :
  - External Control In Word Indexed (**eciwx**).
  - External Control Out Word Indexed (**ecowx**).
  - Floating Select (**fsed**).
  - Floating Reciprocal Estimate Single-Precision (**fres**).
  - Floating Reciprocal Square Root Estimate (**frsqrte**).
  - Store Floating-Point as Integer Word (**stfiwx**).

5.3. Cache Implementation

The following subsections describe the PowerPC architecture's treatment of cache in general, and the 603e specific implementation, respectively.

5.3.1. PowerPC cache characteristics

The PowerPC architecture does not define hardware aspects of cache implementations. For example, some PowerPC processors, including the 603e, have separate instruction and data caches (harvare architecture), while others, such as the PowerPC 601™ microprocessor, implement a unified cache.

PowerPC microprocessor control the following memory access modes on a page or block basis :

- Write-back/write-through mode.
- Cache-inhibited mode.
- Memory coherency.

Note that in the 603e, a cache line is defined as eight words. The VEA defines cache management instructions that provide a means by which the application programmer can affect the cache contents.

5.3.2. PowerPC 603e microprocessor cache implementation

The 603e has two 16-Kbyte, four-way set-associative (instruction and data) caches. The caches are physically addressed, and the data cache can operate in either write-back or write-through mode as specified by the PowerPC architecture.

The data cache is configured as 128 sets of 4 lines each. Each line consists of 32 bytes, two state bits, and an address tag. The two state bits implement the three-state MEI (modified/exclusive/invalid) protocol. Each line contains eight 32-bit words. Note that the PowerPC architecture defines the term block as the cacheable unit. For the 603e, the block size is equivalent to a cache line. A block diagram of the data cache organization is shown in Figure 13.

The instruction cache also consists of 128 sets of 4 lines, and each line consists of 32 bytes, an address tag, and a valid bit. The instruction cache may not be written to except through a line fill operation. The instruction cache is not snooped, and cache coherency must be maintained by software. A fast hardware invalidation capability is provided to support cache maintenance. The organization of the instruction cache is very similar to the data cache shown in Figure 13.

Each cache line contains eight contiguous words from memory that are loaded from an 8-word boundary (that is, bits A27-A32 of the effective addresses are zero) ; thus, a cache line never crosses a page boundary. Misaligned accesses across a page boundary can incur a performance penalty.

The 603's cache lines are loaded in four beats of 64 bits each. The burst load is performed as "critical double word first". The cache that is being loaded is blocked to internal accesses until the load completes. The critical double word is simultaneously written to the cache and forwarded to the requesting unit, thus minimizing stalls due to load delays.

To ensure coherency among caches in a multiprocessor (or multiple caching-device) implementation, the 603e implemements the MEI protocol. These three states, modified, exclusive, and invalid, indicate the state of the cache block as follows :

- **Modified** - The cache line is modified with respect to system memory ; that is, data for this address is valid only in the cache and not in system memory.
- **Exclusive** - This cache line holds valid data that is identical to the data at this address in system memory. No other cache has this data.
- **Invalid** - This cache line does not hold valid data.

Cache coherency is enforced by on-chip bus snooping logic. Since the 603e's data cache tags are single ported, a simultaneous load or store and snoop access represent a resource contention. The snoop access is given first access to the tags. The load or store then occurs on the clock following snoop.

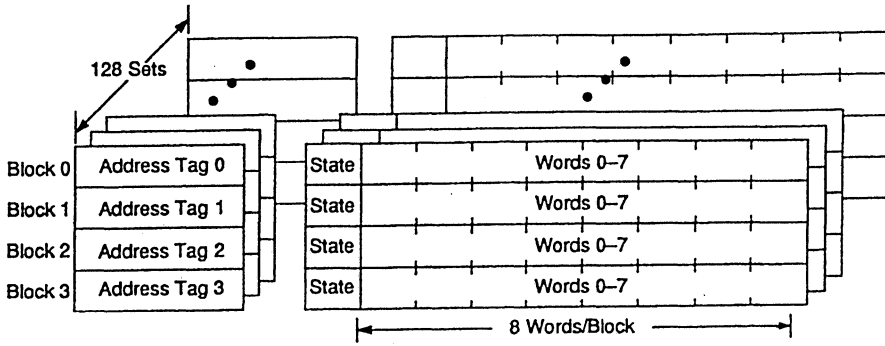


Figure 13 : Data cache organization

5.4. Exception model

The following subsections describe the PowerPC exception model and the 603e implementation, respectively.

5.4.1. PowerPC exception model

The PowerPC exception mechanism allows the processor to change to supervisor state as a result of external singles, errors, or unusual conditions arising in the execution of instructions, and differ from the arithmetic exceptions defined by the IEEE for floating-point operations. When exceptions occur, information about the state of the processor is saved to certain registers and the processor begins execution at an address (exception vector) predetermined for each exception. Processing of exceptions occurs in supervisor mode.

Although multiple exception conditions can map to a single exception vector, a more specific condition may be determined by examining a register associated with the exception - for example, the DSISR and the FPSCR. Additionally, some exception conditions can be explicitly enable or disabled by software.

The PowerPC architecture requires that exceptions be handled in program order ; therefore, although a particular implementation may recognize exception conditions out of order, they are presented strictly in order. When an instruction-caused exception is recognized, any unexecuted instructions that appear earlier in the instruction stream, including any that have not yet entered the execute state, are required to complete before the exception is taken. Any exceptions caused by those instructions are handled first. Likewise, exceptions that are asynchronous and precise are recognized when they occur, but are not handled until the instruction currently in the completion state successfully completes execution or generates an exception, and the completed store queue is emptied.

Unless a catastrophic causes a system reset or machine check exception, only one exception is handled at a time. If, for example, a single instruction encounters multiple exception conditions, those conditions are encountered sequentially. After the exception handler handles an exception, the instruction execution continues until the next exception condition is encountered. However, in many cases there is no attempt to re-execute the instruction. This method of recognizing and handling exception conditions sequentially guarantees that exceptions are recoverable.

Exception handlers should save the information stored in SRR0 and SRR1 early to prevent the program state from being lost due to a system reset and machine check exception or to an instruction-caused exception in the exception handler, and before enabling external interrupts.

The PowerPC architecture support four types of exceptions :

- **Synchronous, precise** - These are causes by instructions. All instruction-caused exceptions are handled precisely ; that is, the machine state at the time the exception occurs is known and can be completely restored. This means that (excluding the trap and system call exceptions) the address of the faulting instruction is provided to the exception handler and that neither the faulting instruction nor subsequent instructions in the code stream will complete execution before the exception is taken. Once the exception is processed, execution resumes at the address of the faulting instruction (or at an alternate address provided by the exception handler). When an exception is taken due to an trap or system call instruction, execution resumes at an address provided by the handler.
- **Synchronous, Imprecise** - The PowerPC architecture defines two imprecise floating-point exception modes, recoverable and nonrecoverable. Even though the 603e provides a means to enable he imprecise modes, it implements these modes identically to the precise mode (-hat is, all enabled floating-point enabled exceptions are always precise on the 603e).
- **Asynchronous, maskable** - The external, SMI, and decrementer interrupts are maskable asynchronous exceptions. When these exceptions occur, their handling is postponed until the next instruction, and any exceptions associated with that instruction, completes execution. If there are no instructions in the execution units, the exception is taken immediately upon determination of the correct restart address (for loading SRR0).

- **Asynchronous, non maskable** - There are two non maskable asynchronous exceptions : system reset and the machine check exception. These exceptions may not be recoverable, or may provide a limited degree of recoverability. All exceptions report recoverability through the SMR[RI] bit.

5.4.2. PowerPC 603e microprocessor exception model

A specified by the PowerPC architecture, all 603e exceptions can be described as either precise or imprecise and either synchronous or asynchronous. Asynchronous exceptions (some or which are maskable) are caused by events external to the processor's execution ; synchronous exceptions, which are all handled precisely by the 603e, are caused by instructions. The 603e exception classes are shown in Table 12.

Synchronous/Asynchronous	precise/Imprecise	Exception type
Asynchronous, non maskable	Imprecise	Machine check System reset
Asynchronous, maskable	Precise	External interrupt Decrementer System management interrupt
Synchronous	Precise	Instruction-caused exceptions

Table 13 : PowerPC 603e microprocessor exception classifications

Although exceptions have other characteristics as well, such as whether they are maskable or non maskable, the distinctions shown in Table 13 define categories of exceptions that the 603e handles uniquely. Note that Table 13 includes no synchronous imprecise instructions. While the PowerPC architecture supports imprecise handling of floating-point exceptions, the 603e implements these exception modes as precise exceptions.

The 603e's exceptions, and conditions that cause them, are listed in Table 14. Exceptions that are specific to the 603e are indicated.

5

Table 14 : Exceptions and conditions

Exception Type	Vector Offset (hex)	Causing Conditions
Reserved	00000	—
System reset	00100	A system reset is caused by the assertion of either $\overline{\text{SRESET}}$ or $\overline{\text{HRESET}}$.
Machine check	00200	A machine check is caused by the assertion of the $\overline{\text{TEA}}$ signal during a data bus transaction, assertion of $\overline{\text{MCP}}$, or an address or data parity error.
DSI	00300	The cause of a DSI exception can be determined by the bit settings in the DSISR, listed as follows: 1 Set if the translation of an attempted access is not found in the primary hash table entry group (HTEG), or in the rehashed secondary HTEG, or in the range of a DBAT register; otherwise cleared. 4 Set if a memory access is not permitted by the page or DBAT protection mechanism; otherwise cleared. 5 Set by an **eciwx** or **ecowx** instruction if the access is to an address that is marked as write-through, or execution of a load/store instruction that accesses a direct-store segment. 6 Set for a store operation and cleared for a load operation. 11 Set if **eciwx** or **ecowx** is used and EAR[E] is cleared.
ISI	00400	An ISI exception is caused when an instruction fetch cannot be performed for any of the following reasons: • The effective (logical) address cannot be translated. That is, there is a page fault for this portion of the translation, so an ISI exception must be taken to load the PTE (and possibly the page) into memory. • The fetch access violates memory protection. If the key bits (Ks and Kp) in the segment register and the PP bits in the PTE are set to prohibit read access, instructions cannot be fetched from this location.
External interrupt	00500	An external interrupt is caused when MSR[EE] = 1 and the $\overline{\text{INT}}$ signal is asserted.
Alignment	00600	An alignment exception is caused when the 603e cannot perform a memory access for any of reasons described below: • The operand of a floating-point load or store instruction is not word-aligned. • The operand of **lmw, stmw, lwarx,** and **stwcx.** instructions are not aligned. • The operand of a single-register load or store operation is not aligned, and the 603e is in little-endian mode. • The instruction is **lmw, stmw, lswi, lswx, stswi, stswx** and the 603e is in little-endian mode. • The operand of **dcbz** is in storage that is write-through-required, or cacning inhibited.

Exception Type	Vector Offset (hex)	Causing Conditions
Program	00700	A program exception is caused by one of the following exception conditions, which correspond to bit settings in SRR1 and arise during execution of an instruction: • Floating-point enabled exception—A floating-point enabled exception condition is generated when the following condition is met: (MSR[FE0] | MSR[FE1]) & FPSCR[FEX] is 1. FPSCR[FEX] is set by the execution of a floating-point instruction that causes an enabled exception or by the execution of one of the "move to FPSCR" instructions that results in both an exception condition bit and its corresponding enable bit being set in the FPSCR. • Illegal instruction—An illegal instruction program exception is generated when execution of an instruction is attempted with an illegal opcode or illegal combination of opcode and extended opcode fields (including PowerPC instructions not implemented in the 603e), or when execution of an optional instruction not provided in the 603e is attempted (these do not include those optional instructions that are treated as no-ops). • Privileged instruction—A privileged instruction type program exception is generated when the execution of a privileged instruction is attempted and the MSR register user privilege bit, MSR[PR], is set. In the 603e, this exception is generated for **mtspr** or **mfspr** with an invalid SPR field if SPR[0] = 1 and MSR[PR] = 1. This may not be true for all PowerPC processors. • Trap—A trap type program exception is generated when any of the conditions specified in a trap instruction is met.
Floating-point unavailable	00800	A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and move instructions) when the floating-point available bit is disabled, (MSR[FP] = 0).
Decrementer	00900	The decrementer exception occurs when the most significant bit of the decrementer (DEC) register transitions from 0 to 1. Must also be enabled with the MSR[EE] bit.
Reserved	00A00–00BFF	—
System call	00C00	A system call exception occurs when a System Call (**sc**) instruction is executed.
Trace	00D00	A trace exception is taken when MSR[SE] =1 or when the currently completing instruction is a branch and MSR[BE] =1.
Reserved	00E00	The 603e does not generate an exception to this vector. Other PowerPC processors may use this vector for floating-point assist exceptions.
Reserved	00E10–00FFF	—
Instruction translation miss	01000	An instruction translation miss exception is caused when an effective address for an instruction fetch cannot be translated by the ITLB.
Data load translation miss	01100	A data load translation miss exception is caused when an effective address for a data load operation cannot be translated by the DTLB.
Data store translation miss	01200	A data store translation miss exception is caused when an effective address for a data store operation cannot be translated by the DTLB; or where a DTLB hit occurs, and the change bit in the PTE must be set due to a data store operation.

Exception Type	Vector Offset (hex)	Causing Conditions
Instruction address breakpoint	01300	An instruction address breakpoint exception occurs when the address (bits 0– 29) in the IABR matches the next instruction to complete in the completion unit, and the IABR enable bit (bit 30) is set to 1.
System management interrupt	01400	A system management interrupt is caused when MSR[EE] =1 and the $\overline{SMI}$ input signal is asserted.
Reserved	01500–02FFF	—

5.5. Memory management

The following subsections describe the memory management features of the PowerPC architecture, and the 603e implementation, respectively.

5.5.1. PowerPC memory management

The primary functions of the MMU are to translate logical (effective) addresses to physical addresses for memory accesses, and to provide access protection on blocks and pages of memory.

There are two types of accesses generated by the 603e that require address translation - instruction accesses, and data accesses to memory generated by load and store instructions.

The PowerPC MMU and exception model support demand-paged virtual memory. Virtual memory management permits execution of programs larger than the size of physical memory ; demand-paged implies that individual pages are loaded into physical memory from system memory only when they are first accessed by an executing program.

The hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

The page table contains a number of page table entry groups (PTEGs). A PTEG contains eight page table entries (PTEs) of eight bytes each ; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

Address translations are enabled by setting bits in the MSR-MSR[IR] enables instruction address translations and MSR[DR] enables data address translations.

5.5.2. PowerPC 603e microprocessor memory management

The instruction and data memory management units in the 603e provide 4 Gbyte of logical address space accessible to supervisor and user programs with a 4-Kbyte page size and 256-Mbyte segment size. Block sizes range from 128 Kbyte to 256Mbyte and are software selectable. In addition, the 603e uses an interim 52-bit virtual address and hashed page tables for generating 32-bit physical addresses. The MMUs in the 603e rely on the exception processing mechanism for the implementation of the paged virtual memory environment and for enforcing protection of designated memory areas.

Instruction and data TLBs provide address translation in parallel with the on-chip cache access, incurring no additional time penalty in the event of a TLB hit. A TLB is a cache of the most recently used page table entries. Software is responsible for maintaining the consistency of the TLB with memory. The 603e's TLBs are 64-entry, two-way set-associative caches that contain instruction and data address translations. The 603e provides hardware assist for software table search operations through the ashed page table on TLB misses. Supervisor software can invalidate TLB entries selectively.

The 603e also provides independent four-entry BAT arrays for instructions and data that maintain address translations for blocks of memory. These entries define blocks that can vary from 128 Kbyte to 256 Mbyte. The BAT arrays are maintained by system software.

As specified by the PowerPC architecture, the hashed page table is a variable-sized data structure that defines the mapping between virtual page numbers and physical page numbers. The page table size is a power of 2, and its starting address is a multiple of its size.

Also as specified by the PowerPC architecture, the page table contains a number of page table entry groups (PTEGs). A PTEG contains eight page table entries (PTEs) of eight bytes each ; therefore, each PTEG is 64 bytes long. PTEG addresses are entry points for table search operations.

5.6. Instruction timing

The 603e is a pipelined superscalar processor. A pipelined processor is one in which the processing of an instruction is reduced into discrete stages. Because the processing of an instruction is broken into a series of stages, an instruction does not require the entire resources of an execution unit. For example, after an instruction completes the decode stage, it can pass on to the next stage, while the subsequent instruction can advance into the decode stage. This improves the throughput of the instruction flow. For example, it may take three cycles for a floating-point instruction to complete, but if there are no stalls in the floating-point pipeline, a series of floating-point instructions can have a throughput of one instruction per cycle.

The instruction pipeline in the 603e has four major pipeline stages, described a follows :

- The fetch pipeline stage primarily involves retrieving instructions from the memory system and determining the location of the next instruction fetch. Additionally, the BPU decodes branches during the fetch stage and folds out branch instructions before the dispatch stage if possible.
- The dispatch pipeline stage is responsible for decoding the instructions supplied by the instruction fetch stage, and determining which of the instructions are eligible to be dispatched in the current cycle. in addition, the source operands of the instructions are read from the appropriate register file and dispatched with the instruction to the execute pipeline stage. At the end of the dispatch pipeline stage, the dispatched instructions and their operands are latched by the appropriate execution unit.
- During the execute pipeline stage each execution unit that has an executable instruction executes the selected instruction (perhaps over multiple cycles), writes the instruction's result into the appropriate rename register, and notifies the completion stage that the instruction has finished execution. In the case of an internal exception, the execution unit reports the exception to the completion/write-back pipeline stage and discontinues instruction execution until the exception is handled. The exception is not signaled until that instruction is the next to be completed. Execution of most floating-point instructions is pipelined within the FPU allowing up to three instructions to be executing in the FPU concurrently. The pipeline stages for the floating-point unit are multiply, add, and round-convert. Execution of most load/store instructions is also pipelined. The load/store units has two pipeline stages. The first stage is for effective address calculation and MMU translation and the second stage is for accessing the data in the cache.
- The complete/writeback pipeline stage maintains the correct architectural machine state and transfers the contents of the rename registers to the GPRs and FPRs as instructions are retired. If the completion logic detects an instruction causing an exception, all following instructions are cancelled, their execution results in rename registers are discarded, and instructions are fetched from the correct instruction stream.

A superscalar processor is one that issues multiple independent instructions into multiple pipelines allowing instructions to execute in parallel. The 603e has five independent execution units, one each for integer instructions, floating-point instructions, branch instructions, load/store instructions, and system register instructions. The IU and the FPU each have dedicated register files for maintaining operands (GPRs and FPRs, respectively), allowing integer calculations and floating-point calculations to occur simultaneously without interference.

Because the PowerPC architecture can be applied to such a wide variety of implementations, instruction timing among various PowerPC processors varies accordingly.

5

6. PREPARATION FOR DELIVERY

6.1. Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

6.2. Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

7. HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

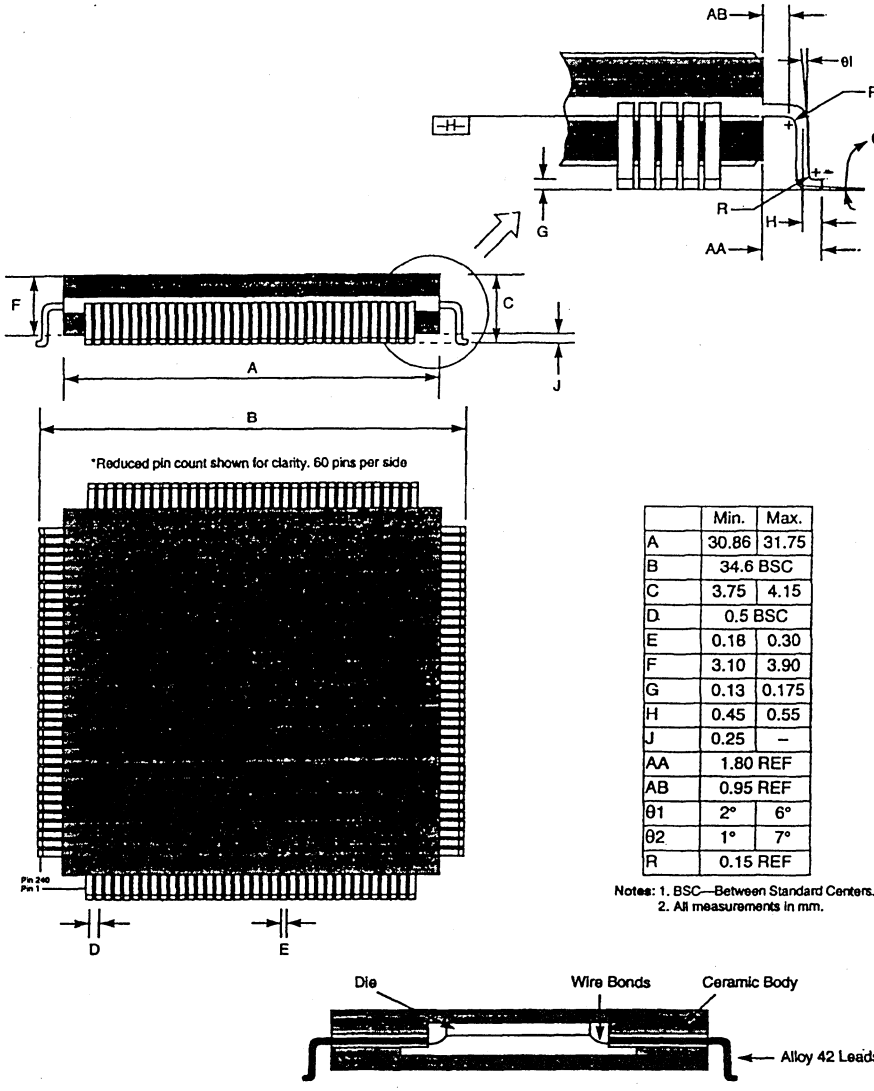
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 percent if practical.

8. PACKAGE MECHANICAL DATA

240 pins - CQFP



	Min.	Max.
A	30.86	31.75
B	34.6 BSC	
C	3.75	4.15
D	0.5 BSC	
E	0.18	0.30
F	3.10	3.90
G	0.13	0.175
H	0.45	0.55
J	0.25	–
AA	1.80 REF	
AB	0.95 REF	
θ1	2°	6°
θ2	1°	7°
R	0.15 REF	

Notes: 1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 14 : Mechanical dimensions of the Wire-bond CQFP package

9. CLOCK RELATIONSHIPS CHOICE

The 603e microprocessors offer customers numerous clocking options. An internal phase-lock loop synchronizes the processor (CPU) clock to the bus or system clock (SYSCLK) at various rations. These ratios allow the designer to utilize the following options :

- Low-speed, low-cost memory systems with economical, low-cost processors.
- Low-speed, economical memory systems isolated from very high-speed processor cores and internal cache.
- High-speed, performance oriented memory systems with maximum achievable processor core and internal cache frequencies.
- Embedded systems with unusual bus speeds dictated by system equirements other than the processor.

Inside each PowerPC microprocessor is a phase-lock loop circuit. A voltage controlled oscillator (VCO) is precisely controlled in f,e-quency and phase by a frequency/phase detector which compares the input bus frequency (SYSCLK frequency) to a submultiple of the VCO.

The ratio of CPU to SYSCLK frequencies is often referred to as the bus mode (for example, 1:1 bus mode and 2:1 bus mode).

In the graph (Figure 15), the horizontal scale represents the CPU or processor core frequency. SYSCLK, or bus frequency, is represented on the left vertical scale in the top half of the graph. The relationship between SYSCLK and CPU frequency, bus mode, is ploted on the heavy solid lines in the top half of the graph.

The VCO frequency is represented on the right vertical scale in the bottom half of the graph. The relationship between VCO frequency and CPU frequency is plotted on the heavy solid lines in the bottom half of the graph.

Note that the vertical scales are different between the top and bottom halves of the graph in order to provide more detail in the critical top half. The bottom half of the graph is used to check that the PLL_CFG signals have been properly chosed to keep the VCO frequency within its specified range of operation.

The graph is used in the following manner :

- Enter the top half with SYSCLK frequency from the left axis and move horizontally to the bus mode line selected by the PLL_CFG input signals.
- Descend vertically to the CPU frequency.
- Continue descending to the line selected by the PLL_CFG signals.
- Move horizontally to the right to read the VCO frequency determined by this SYSCLK input and PLL-CFG signals.

The VCO output divided by M sets the CPU frequency but other circuitry in the processor probably limits the upper maximum of the CPU frequency of operation range. Therefore, both the VCO frequency and the CPU frequency determined from the graph must be checked against the appropriate hardware specification to see that they are within the range specified for the device in question.

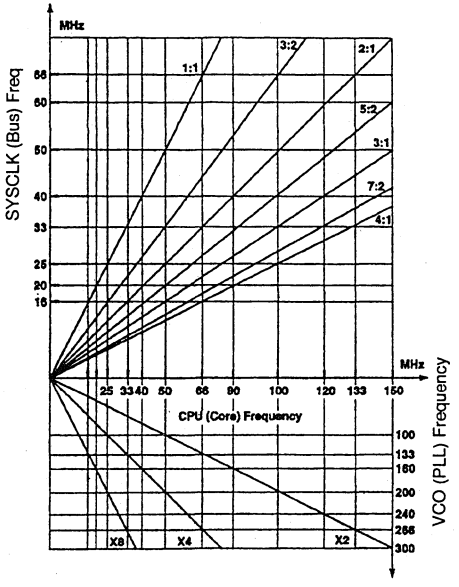
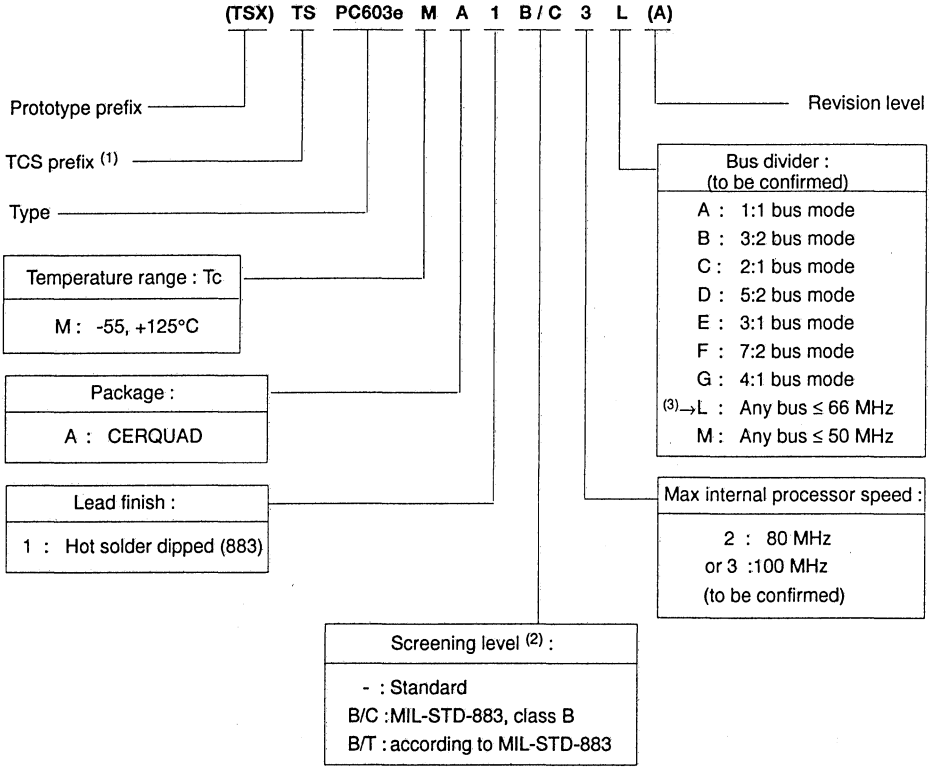


Figure 15 : MPC 603e clock relationships

10.ORDERING INFORMATION



(1) THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES
(2) For availability of the different versions, contact your TCS sale office
(3) Preferred option (to be confirmed)

ADVANCE INFORMATION

TS88915T

LOW SKEW CMOS PLL CLOCK DRIVER
3-State 55, 70 and 100 MHz Versions

DESCRIPTION

The TS 88915T Clock Driver utilizes a phazed–locked loop (PLL) technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance microprocessors such as TS68040 and TSPC603e.

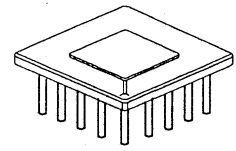
MAIN FEATURES

- **TS68040 & TSPC603e FULL COMPATIBLE**
- **FIVE LOW SKEW OUTPUTS**
  Five Outputs (Q0-Q4) with Output–to–Output skew < 500 ps each being phase end frequency locked to the SYNC input.
- **ADDITIONAL OUTPUTS**
  Three additional outputs are available :
  - The 2X_Q output runs twice the system "Q" frequency
  - The Q/2 output runs at 1/2 the system "Q" frequency
  - The $\overline{Q5}$ output is inverted (180° phase shift)
- **TWO SELECTABLE CLOCK INPUTS**
  - Two selectable CLOCK inputs are available for test or redundancy purposes.
  - Test Mode pin (PLL_EN) provided for low frequency testing.
  - All outputs can go into high impedance (3-state) for board test purpose
- **INPUT FREQUENCY RANGE FROM 5MHz to 2X_Q FMAX**
- **THREE INPUT/OUTPUT RATIOS**
  Input/Output phase–locked frequency ratios of 1:2, 1:1 and 2:1 are available
- **LOW PART-TO-PART SKEW**
  The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew).
- **CMOS AND TTL COMPATIBLE**
  - All outputs can drive either CMOS or TTL inputs
  - All inputs are TTL-level compatible
- **LOCK Indicator (LOCK) indicated a phase–locked state.**

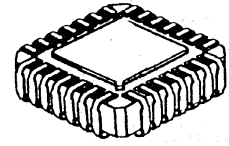
SCREENING/QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 (class B)
- DESC (planned)
- or according to TCS standard



R Suffix
PGA 29
Ceramic Pin grid array



W suffix
LDCC 28
Leaded Ceramic Chip Carrier
(To be confirmed)

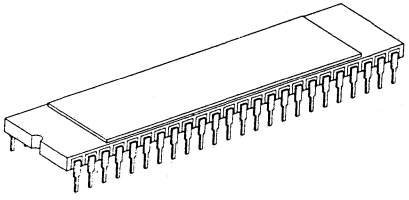
5

TS 68HC11A1

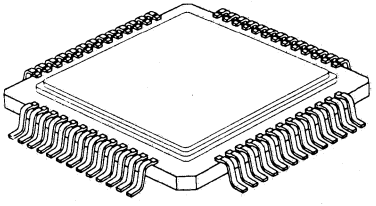
HCMOS 8-BIT MICROCONTROLLER UNIT

DESCRIPTION

The TS 68HC11A1 high density CMOS (HCMOS) microcontroller unit (MCU) contains highly sophisticated on-chip peripheral capabilities. This high-speed and low-power MCU has a nominal bus speed of two megahertz, and the fully static design allows operations at frequencies down to dc. This publication contains condensed information on the MCU.



C Suffix
DIL 48
Ceramic side brazed dual in line



F Suffix
CQFP 52
Ceramic quad flat pack

See the ordering information page 54.

Pin connection : see page 4.

MAIN FEATURES

- Enhanced 16-bit timer system with four-stage programmable prescaler.
- Power saving STOP and WAIT modes.
- Serial Peripheral Interface (SPI).
- Enhanced NRZ serial communications interface (SCI).
- 8-bit pulse accumulator circuit.
- Bit test and branch instructions.
- Real time interrupt circuit.
- 512 bytes of EEPROM.
- 256 bytes of static RAM.
- Eight-channel 8-bit A/D converter (for CQFP only).
- Power supply : 5.0 V_{DC} ± 10 %.
- Military temperature range : − 55°C to + 125°C (T_C).

SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- DESC 5962 90510 on request.
- or according to TCS standards.

SUMMARY

A - GENERAL DESCRIPTION

1 - INTRODUCTION

Figure 1 is a block diagram of the TS 68HC11A1.

BLOCK DIAGRAM

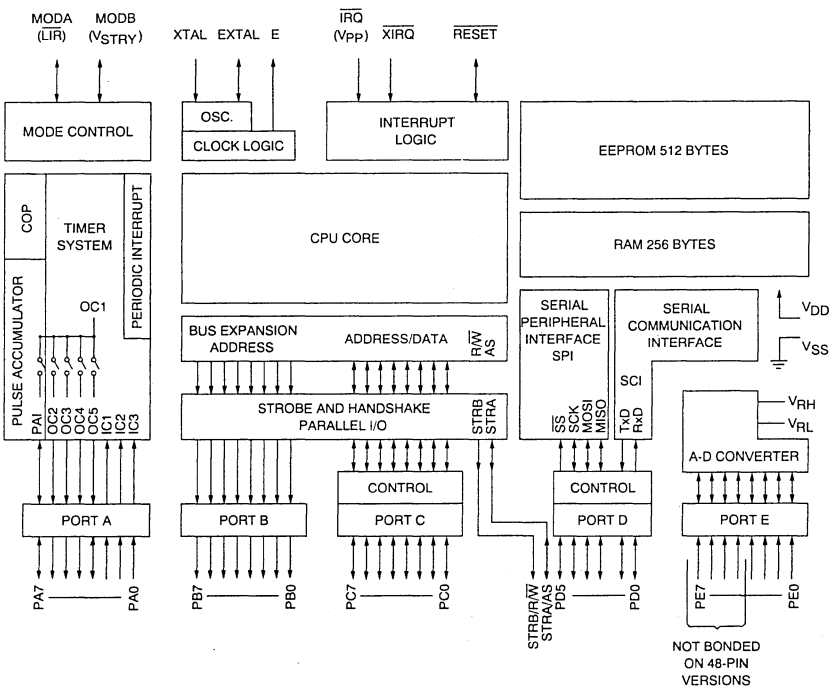


Figure 1 : TS 68HC11A1 block diagram.

More details about description are mentionned in § 6 and also inside Advance Information Manual, HCMOS Single Chip Microcontroller, HCMOS Single Chip Microcontroller Programmer's reference manual.

2 · SIGNAL DESCRIPTION

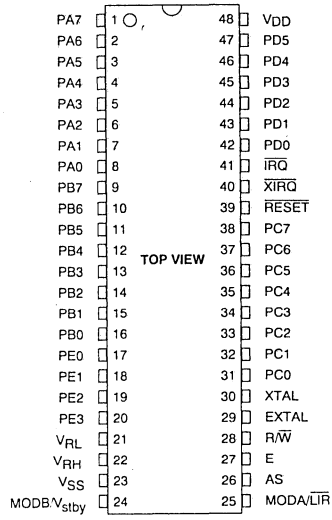


Figure 2 : 48-Pin dual-in-line package.

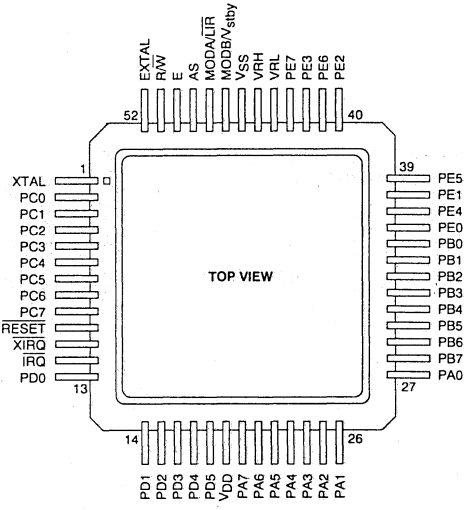


Figure 3 : 52-Lead quad flat package.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microcontroller TS 68HC11A1, in compliance with MIL-STD-883 class B with TCS standards.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 appendix A : general specifications for microcircuits.
3) DESC Drawing 5962-90510.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2 and 3.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-PRF-1835.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic package which is conform to case outlines of MIL-PRF-1835 :

- DIL 48,
- 52-pin ceramic quad flat pack CQFP,

The precise case outlines are described in § 9.1 and 9.2.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
P_{dmax}	Max power dissipation			210	mW
T_{case}	Operating temperature	TS 68HC11A1 CM	−55	+125	°C
		TS 68HC11A1 CV	−40	+85	°C
T_{stg}	Storage temperature		−65	+150	°C
T_j	Junction temperature			+150	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 · Recommended condition of use

Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 2

Symbol	Parameter		Min	Max	Unit
V_{DD}	Supply voltage		4.5	5.5	V
V_{IL}	Low level input voltage		V_{SS}	$0.2 \times V_{DD}$	V
V_{IH}	High level input voltage		$0.8 \times V_{DD}$	V_{DD}	V
T_{case}	Operating temperature	TS 68HC11A1CM	−55	+125	°C
		TS 68HC11A1CV	−40	+85	°C
V_{OH}	Maximum high level output voltage		V_{DD} −0.1		V
V_{OL}	Maximum low level output voltage		V_{SS}	0.4	V
f_C	Clock frequency (crystal frequency)		4	8.4	MHz

This device contains protective circuitry to protect the inputs against damage due to high static voltages or electrical fields ; however, it is advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

3.4 · Thermal characteristics (at 25°C)

Table 3

Package	Symbol	Parameter	Value	Unit
DIL 48	θ JA	Thermal resistance - Ceramic junction to Ambient	38	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/
CQFP 52	θ JA	Thermal resistance - Ceramic junction to Ambient	31	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/W

Power considerations.

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined.

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or TCS standards.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum.

3.6.1 · Thomson logo

3.6.2 · Manufacturer's part number

3.6.3 · Class B identification

3.6.4 · Date-code of inspection lot

3.6.5 · ESD identifier if available

3.6.6 · Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

6

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics are specified for inspection purpose, refer to relevant specification :

– DESC see § 4.1.

Table 4 : Static electrical characteristics for all electrical variants. See § 5.2.

Tables 5 to 10 : Dynamic electrical characteristics. See § 5.3.

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 4).

For dynamic characteristics (Tables 5 to 10), test methods refer to IEC 748-2 method number, where existing.

5.2 · Static characteristics

Table 4 · DC electrical characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = −55°C / +125°C or −40°C / +85°C

Symbol	Parameter		Min	Max	Unit
V_{OH}	Output high voltage I_{Load} = −0.8 mA, V_{DD} = 4.5 V (Note 1)	All outputs except $\overline{RESET}$ XTAL, and MODA	V_{DD} −0.8		V
V_{OL}	Output low voltage I_{Load} = 1.6 mA	All outputs except XTAL		0.4	V
V_{IH}	Input high voltage	All inputs except $\overline{RESET}$ $\overline{RESET}$	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} V_{DD}	V V
V_{IL}	Input low voltage	All inputs	V_{SS}	0.2 x V_{DD}	V
I_{OZ}	I/O ports, three-state leakage V_{in} = V_{IH} or V_{IL}	PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		±10	µA
I_{in}	Input current (Note 2) V_{in} = V_{DD} or V_{SS} V_{in} = V_{DD} or V_{SS}	PA0-PA2, $\overline{IRQ}$, $\overline{XIRQ}$ MODB/V_{STBY}		±1 ±10	µA µA
V_{SB}	RAM standby voltage	Powerdown	4.0	V_{DD}	V
I_{SB}	RAM standby current	Powerdown		20	µA
	Total supply current (Note 3)				
I_{DD}	RUN : Single chip Expanded multiplexed			 20 30	 mA mA
W_{IDD}	WAIT : All peripheral functions shut down Single-chip mode Expanded multiplexed mode			 10 15	 mA mA
S_{IDD}	STOP : No clocks, single-chip mode			 100	 µA
C_{in}	Input capacitance	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, EXTAL PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		8 14	pF pF
P_D	Power dissipation	Single-chip mode Expanded-multiplexed mode		110 165	mW mW

Note 1 : V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.

Note 2 : See A/D specification for leakage current for port E.

Note 3 : All ports configured as inputs, $V_{IL} \leqslant 0.2$ V, $V_{IH} \geqslant V_{DD} - 0.2$ V, no dc loads, EXTAL is driven with a square wave, and t_{cyc} = 476.5 ns.

5.3 · Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V (See also note 1 and 2).

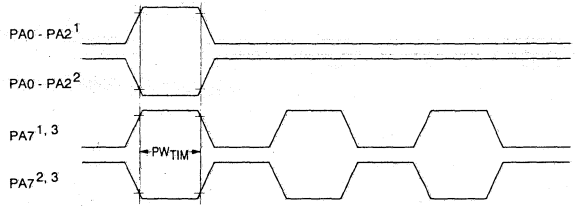
Table 5 - Control timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$

Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_O	Frequency of operation	dc	1.0	dc	2.0	dc	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
f_{XTAL}	Crystal frequency		4.0		8.0		8.4	MHz
4 f_O	External oscillator frequency	dc	4.0	dc	8.0	dc	8.4	MHz
t_{PCS}	Processor control setup Time (see Figures 5 and 7) t_{PCS} = 1/4 t_{cyc} − 50 ns	200		75		69		ns
PW_{RSTL}	Reset input pulse width (Note 1 and Figure 5) (To guarantee external reset vector) (Minimum input time ; may be preempted by internal reset)	8 1		8 1		8 1		t_{cyc}
t_{MPS}	Mode programming setup time (see Figure 5)	2		2		2		t_{cyc}
t_{MPH}	Mode programming hold time (see Figure 5)	0		0		0		ns
PW_{IRQ}	Interrupt pulse width $\overline{IRQ}$ edge sentive mode (see Figures 6 and 8) PW_{IRQ} = t_{cyc} 20 ns	2		2		2		ns
t_{WRS}	Wait recovery startup time (see Figure 7)		4		4		4	t_{cyc}
PW_{TIM}	Timer pulse width Input capture, pulse accumulator input (see Figure 4) PW_{TIM} = t_{cyc} + 20 ns	1020		520		496		ns

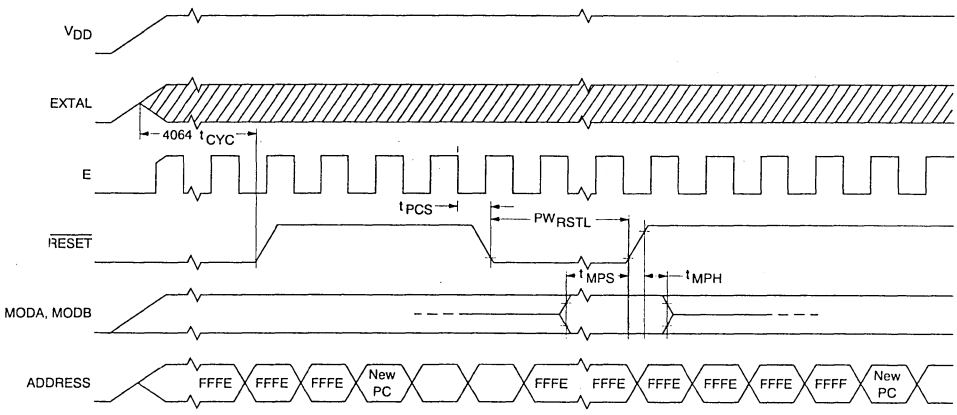
Note 1 : $\overline{RESET}$ will be recognized during the first clock it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. See $\overline{RESET}$, INTERRUPT, AND LOW-POWER MODES for details.

Note 2 : All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.



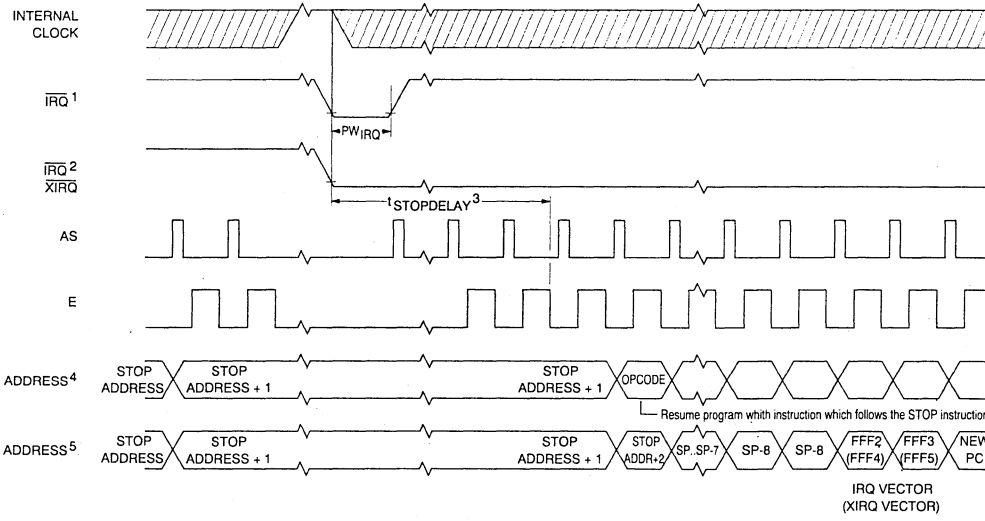
Note 1 : Rising sensitive input.
Note 2 : Falling edge sensitive input.
Note 3 : Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 4 : Timer inputs timing diagram.



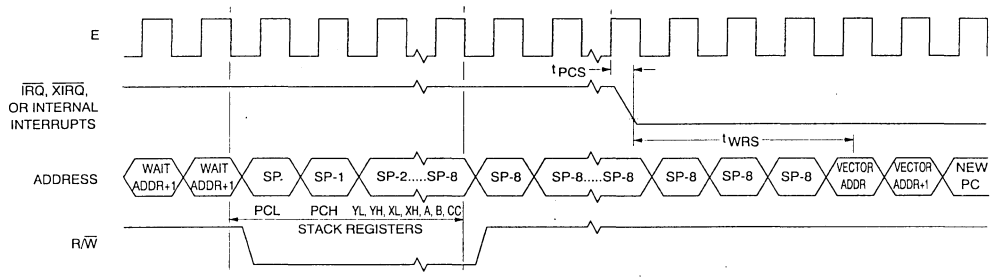
Note : Refer to table - for pin states during RESET

Figure 5 : POR external reset timing diagram.



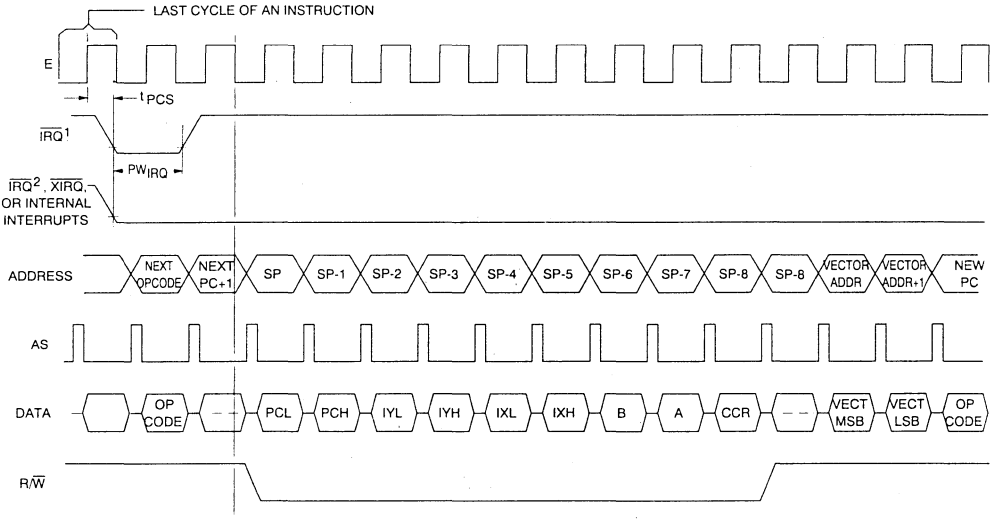
Note 1 : Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
Note 2 : Level sensitive $\overline{IRQ}$ pin (IRQ bit = 0).
Note 3 : $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
Note 4 : $\overline{XIRQ}$ with X bit in CCR = 1.
Note 5 : $\overline{IRQ}$ or ($\overline{XIRQ}$ with X bit in CCR = 0).

Figure 6 : Stop recovery timing diagram.



Note 1 : Refer to table - for pin states during WAIT.
Note 2 : RESET will also cause recovery from WAIT.

Figure 7 : WAIT recovery from interrupt timing diagram.



Note 1 : Edge sensitive IRQ pin (IRQ bit = 1).
Note 2 : Level sensitive IRQ pin (IRQE bit = 0).

Figure 8 : Interrupt timing diagram.

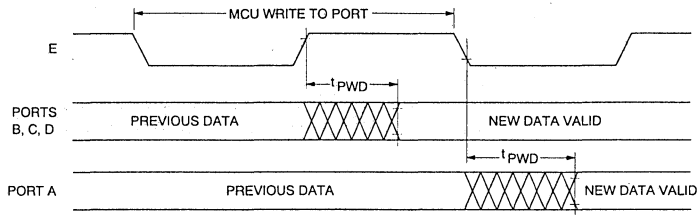
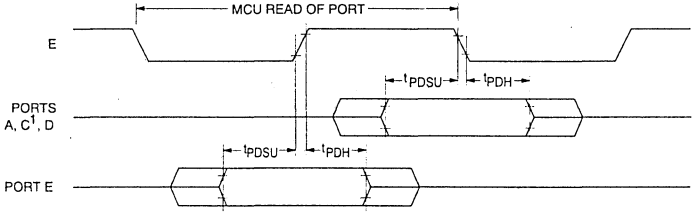


Figure 9 : Port write timing diagram.



Note : For non-latched operation of Port C.

Figure 10 : Port read timing diagram.

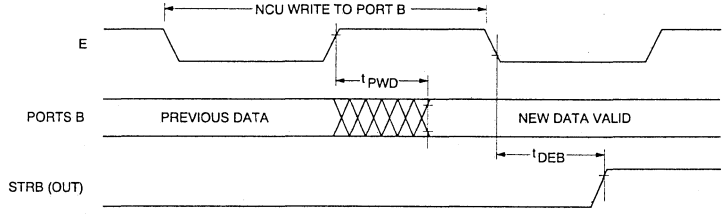


Figure 11 : Simple output strobe timing diagram.

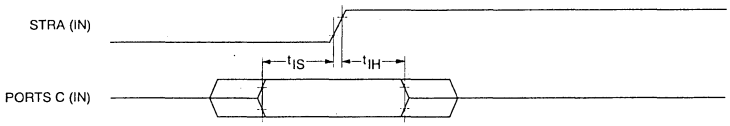
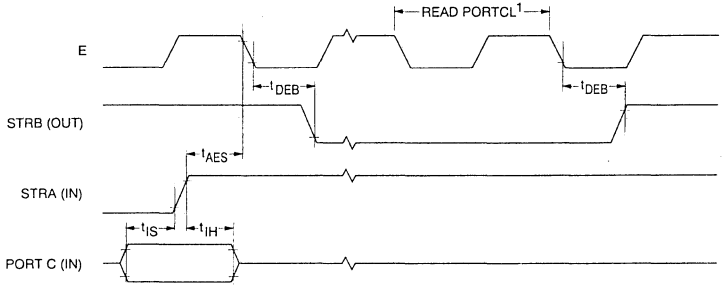
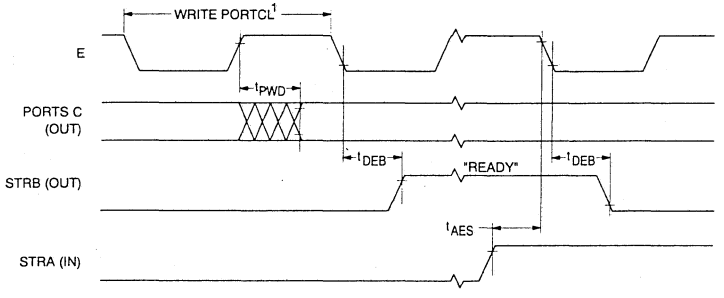


Figure 12 : Simple intput strobe timing diagram.



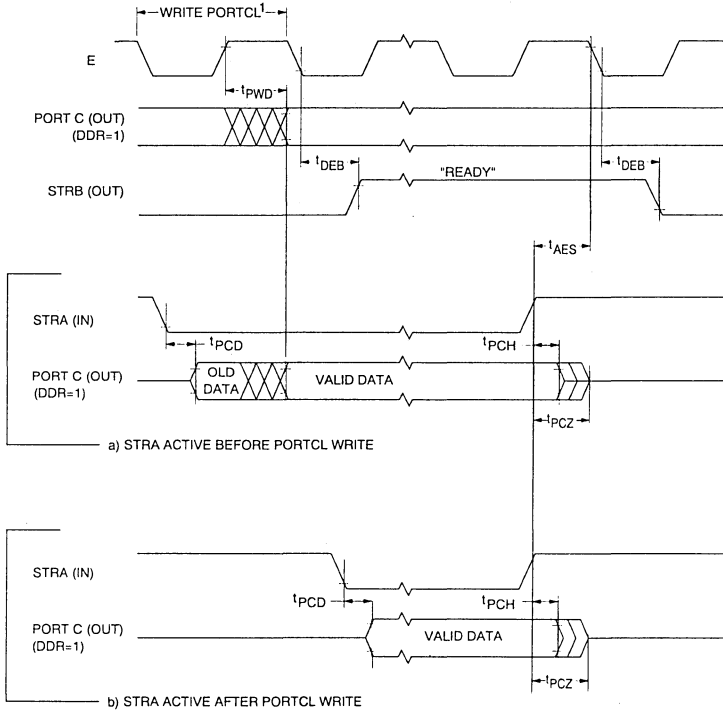
Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 13 : Port C input handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 14 : Port C output handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 15 : Three-state variation of output handshake timing diagram (STRA enables output buffer).

Table 6 - Peripheral port timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$

Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_0	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
t_{PDSU}	Peripheral data setup time (MCU read of ports A, C, D and E) (see Figure 10)	100		100		100		ns
t_{PDH}	Peripheral data hold time (MCU read of ports A, C, D and E) (see Figure 10)	50		50		50		ns
t_{PWD}	Delay time, peripheral data write (See Figures 9, 11, 14 and 15) MCU write to port A MCU writes to ports, B, C and D t_{PWD} = 1/4 t_{cyc} +90 ns		 150 340		 150 215		 150 209	 ns ns
t_{IS}	Input data setup time (port C) (see Figures 12 and 13)	60		60		60		ns
t_{IH}	Input data hold time (port C) (see Figures 12 and 13)	100		100		100		ns
t_{DEB}	Delay time, E fall to STRB t_{DEB} = 1/4 t_{cyc} +130 ns (see Figures 11, 13, 14 and 15)		380		255		249	ns
t_{AES}	Setup time, STRA asserted to E fall (see Note) (see Figures 13 and 15)	0		0		0		ns
t_{PCD}	Delay time, STRA asserted to port C data output valid (see Figure 15)		100		100		100	ns
t_{PCH}	Hold time, STRA negated to port C data (see Figure 15)	10		10		10		ns
t_{PCZ}	Three-state hold time (see Figure 15)		150		150		150	ns

Note : If this setup time is met, STRB will acknoweldge in the next cycle. If it is not met, the respons may be delayed one more cycle.

6

Table 7 - A/D converter characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$; 750 kHz ⩽ E ⩽ 2.1 MHz (unless otherwise noted)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8		Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics		±1/2	LSB
Zero error	Difference between the output of an ideal and an actual A/D for zero input voltage		±1/2	LSB
Full-scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage		±1/2	LSB
Total unadjusted error	Maximum sum of non-linearity, zero, error, and full-state error (Note 1)		±1/2	LSB
Quantization error	Uncertainty due to converter resolution		±1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error source included		±1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage (Note 2)	V_{RL}	V_{DD} +0.1	V
V_{RL}	Minimum analog reference voltage (Note 2)	V_{SS} −0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL} (Note 2)	3		V
Conversion time	Total time to perform a single analog-to-digital conversion: a. E clock b. Internal RC oscillator		32 t_{cyc} +40	t_{cyc} µs
Monotonicity	Conversion result never decreases with an incrase in input voltage and has no missing codes			
Zero-input reading	Conversion result when $V_{in} = V_{RL}$	00		Hex
Full-scale reading	Conversion result when $V_{in} = V_{RH}$		FF	Hex
Sample acquisition time	Analog input acquisition sampling time: a. E clock b. Internal RC oscillator	12	 12	 t_{cyc} µs
Input leakage	Input leakage on A/D pins PE0-PE7 V_{RL}, V_{RH}		400 1.0	nA µA

Note 1: Source impedance greater than 10 kΩ will adversaly affect accurancy, due mainly to input leakage.
Note 2: Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ±10 %.

Table 8 - Expansion bus timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	f_O	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
1	t_{cyc}	Cycle time	1000		500		476		ns
2	PW_{EL}	Pulse width, E low $PW_{EL} = 1/2\ t_{cyc} - 23$ ns	477		227		215		ns
3	PW_{EH}	Pulse width, E high $PW_{EH} = 1/2\ t_{cyc} - 28$ ns	472		222		210		ns
4	t_r, t_f	E and AS rise and fall time		20		20		20	ns
9	t_{AH}	Address hold time $t_{AH} = 1/8\ t_{yc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
12	t_{AV}	Non-muxed address valid time to E rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1b)	281.5		94		85		ns
17	t_{DSR}	Read data setup time	30		30		30		ns
18	t_{DHR}	Read data hold time (maxe = t_{MAD})	10	145.5	10	83	10	80	ns
19	t_{DDW}	Write data delay time $t_{DDW} = 1/8\ t_{cyc} + 65.5$ ns (Note 1a)		190.5		128		125	ns
21	t_{DHW}	Write data hold time $t_{DHW} = 1/8\ t_{cyc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
22	t_{AVM}	Muxed address valid time to E rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1b)	271.5		84		75		ns
24	t_{ASL}	Muxed address valid time to AS fall $t_{ASL} = PW_{ASH} - 90$ ns	151		26		20		ns
25	t_{AHL}	Muxed address hold time $t_{AHL} = 1/8\ t_{cyc} - 29.5$ ns (Note 1b)	95.5		33		30		ns
26	t_{ASD}	Delay time, E to AS rise $t_{ASD} = 1/8\ t_{cyc} - 9.5$ ns (Note 1a)	115.5		53		50		ns
27	PW_{ASH}	Pulse width, AS high $PW_{ASH} = 1/4\ t_{cyc} - 29$ ns	221		96		90		ns
28	t_{ASED}	Delay time, AS to E rise $t_{ASED} = 1/8\ t_{cyc} - 9.5$ ns (Note 1b)	115.5		53		50		ns
29	t_{ACCA}	MPU address access time $t_{ACCA} = t_{AVM} + t_r + PW_{EH} - t_{DSR}$ (Note 1b)	733.5		296		275		ns
35	t_{ACCE}	MPU access time $t_{ACCE} = PW_{EH} - t_{DSR}$		442		192		180	ns

6

Table 8 - Expansion bus timing (continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
36	t_{MAD}	Muxed address delay (previous cycle MPU read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1a)	145.5		83		80		ns

Note 1 : Input clocks with duty cycles other than 50 % will affect bus performance. Timing parameters affected by input clock duty cycle are identified by a and b. To recalculate the approximate bus timing values, substitute the following expression in place of 1/8 t_{cyc} in the above formulas where applicable :

a. (1 – DC) × 1/4 t_{cyc} for : (t_{DDW}, t_{DHW}, t_{MAD})
b. DC × 1/4 t_{cyc} for : (t_{AVM}, t_{AHL}, t_{ASD}, t_{ASED}, t_{ACCA})
where : DC is the decimal value of duty cycle percentage (high time).

Table 9 - Serial peripheral interface (SPI) timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$or $-55 \leqslant T_C \leqslant +125°C$ - See Figures 17 and 18

Num.	Symbol	Characteristic	Min	Max	Unit
		Operating frequency			
	$f_{op}(m)$	Master	dc	0.5	f_{op}
	$f_{op}(s)$	Slave	dc	2.1	MHz
1		Cycle time			
	$t_{cyc}(m)$	Master	2.0		t_{cyc}
	$t_{cyc}(s)$	Slave	480		ns
2		Enable lead time			
	$t_{lead}(m)$	Master	Note 1		ns
	$t_{lead}(s)$	Slave	240		ns
3		Enable lag time			
	$t_{lag}(m)$	Master	Note 1		ns
	$t_{lag}(s)$	Slave	240		ns
4		Clock (SCK) high time			
	$t_{w}(SCKH)m$	Master	340		ns
	$t_{w}(SCKH)s$	Slave	190		ns
5		Clock (SCK) low time			
	$t_{w}(SCKL)m$	Master	340		ns
	$t_{w}(SCKL)s$	Slave	190		ns
6		Data setup time (inputs)			
	$t_{su}(m)$	Master	100		ns
	$t_{su}(s)$	Slave	100		ns
7		Data hold time (inputs)			
	$t_{h}(m)$	Master	100		ns
	$t_{h}(s)$	Slave	100		ns
8		Access time (time to data active from high-impedance state)			
	t_a	Slave	0	120	ns
9		Disable time (hold time to high-impedance state)			
	t_{dis}	Slave		240	ns
10	tv(s)	Data hold (after enable edge) Note 2		240	ns
11	tho	Data valid time (outputs) (after enable edge)	0		ns
12		Rise time (20 % V_{DD} to 70 % V_{DD}, C_L = 200 pF)			
	trm	SPI outputs (SCK, MOSI, and MISO)		100	ns
	trs	SPI inputs (SCK, MISO, MOSI, and SS)		2.0	µs

Table 9 - Serial peripheral interface (SPI) timing (continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C + 85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figures 17 and 18

Num.	Symbol	Characteristic	Min	Max	Unit
13	t_{fm} tfs	Fall time (70 % V_{DD} to 20 % V_{DD}, C_L = 200 pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MISO, MOSI, and SS)		 100 2.0	 ns µs

Note 1 : Signal production depends on software.
Note 2 : Assumes 200 pF load on all SPI pins.

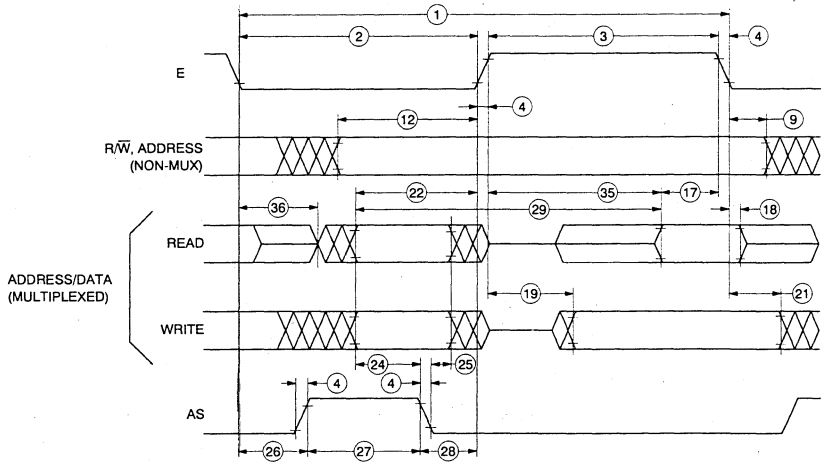
Table 10 - EEPROM characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = 25°C

Characteristics		Min	Max	Unit
Programming time (Note 1)	Under 1.0 MHz with RC oscillator enabled 1.0 to 2.0 MHz with RC oscillator disabled 2.0 MHz (or anytime RC oscillator enabled)		25 must use RC 25	ms ms ms
Erase time (Note 1)	Byte, row, and bulk		10	ms
Write/erase endurance (Note 2)			10.000	cycles
Data retention (Note 2)			10	years

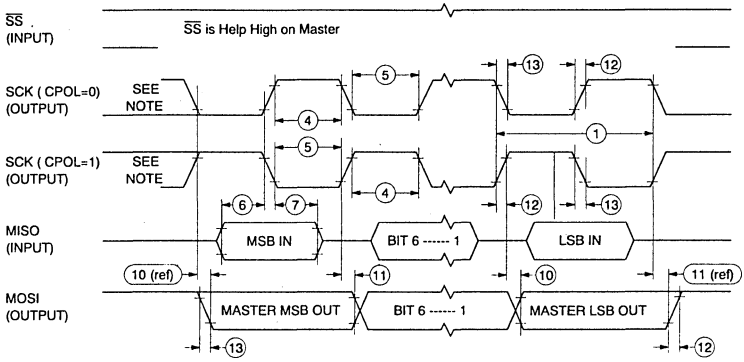
Note 1 : The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
Note 2 : See current quarterly reliability monitor report for current failure rate information.

6



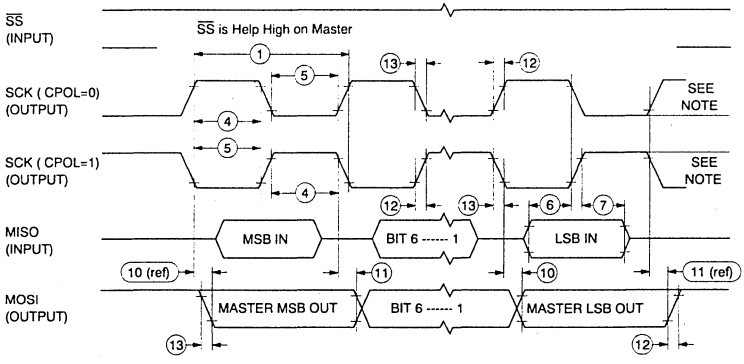
Note : Measurement points shown are 20 % and 70 % V_{DD}.

Figure 16 : Expansion bus timing diagram.



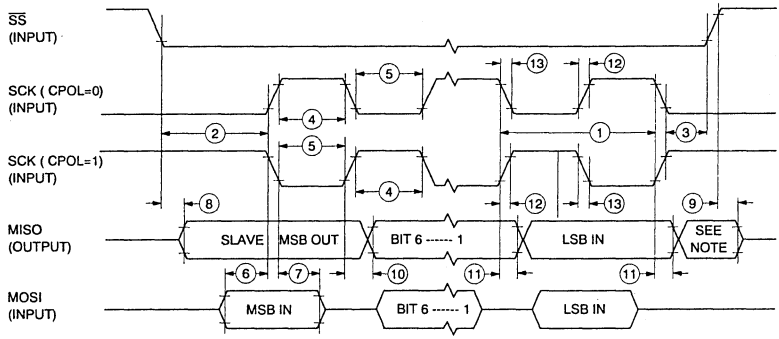
Note : This first clock edge is generated internally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17a : SPI timing diagrams
SPI master timing (CPHA = 0).



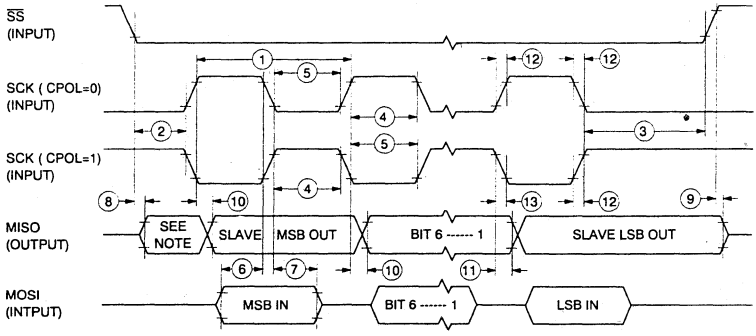
Note : This first clock edge is generated internally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17b : SPI timing diagrams
SPI master timing (CPHA = 1).



Note : Not defined but normally MSB of character just received.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 18a : SPI timing diagrams
SPI slave timing (CPHA = 0).



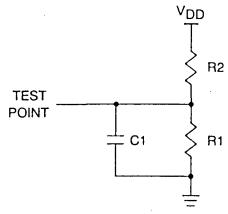
Note : Not defined but normally LSB of character previously transmitted.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 18b : SPI timing diagrams
SPI slave timing (CPHA = 1).

5.4 - Test conditions specific to the device

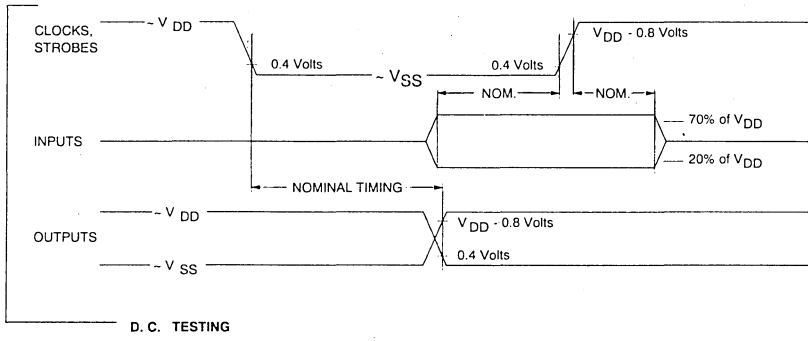
5.4.1 - Loading network

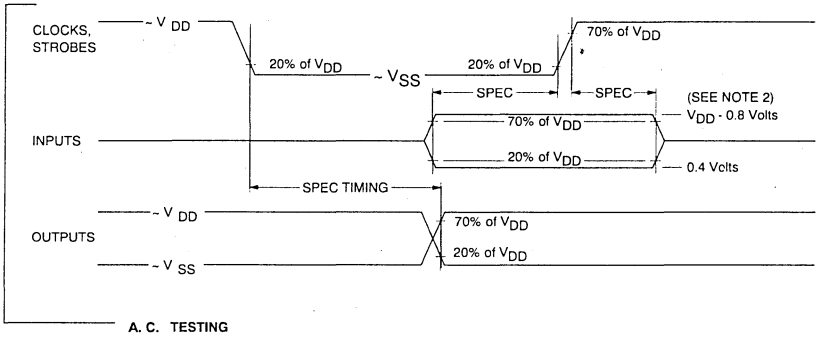
The applicable loading network of the Tables 5, 6, 8, 9 refer to the loading network number as shown in Figure 19 below.



Equivalent test load (Note 1)

Pins	R1	R2	C1
PA3-PA7 PB0-PB7 PC0-PC7 PD0-PD5 E, AS, R/$\overline{W}$	3.26 K	2.38 K	30 pF
PD1-PD4	3.26 K	2.38 K	200 pF





Note 1 : Full test loads are applied during all ac electrical test and ac timing measurements.

Note 2 : During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} – 0.8 volts while timing measurements are taken at the 20 % and 70 % of V_{DD} points.

Figure 19 : Test methods.

5.4.2 - Time definitions

The times specified in Tables 5, 6, 8 and 9 as dynamic characteristics are defined in Figures 4 to 18.

6 · FUNCTIONAL DESCRIPTION

6.1 · Operating modes

The MCU uses two dedicated pins (MODA and MODB) to select one of two basic operating modes or one of two special operating modes. The basic operating modes are single-chip and expanded-multiplexed ; the special operating modes are boostrap and special test. The following paragraphs describe the different modes.

SINGLE-CHIP MODE

In this mode, the MCU functions as a self-contained microcontroller and has no external address or data bus. This mode provides maximum use of the pins for on-chip peripheral functions, and all address and data activity occur within the MCU. This mode would not normally be used on the TS 68HC11A1, because of no internal ROM.

EXPANDED MULTIPLEXED MODE

In this mode, the MCU can address up to 64 K bytes of address space. Higher-order address bits are output on the port B pins, and lower-order address bits and the data bus are multipliexed on the port C pins. The AS pin provides the control output used in demultiplexing the loworder address at port C. The R/W pin is used to control the direction of data transfer on port C bus.

BOOTSTRAP MODE

In this mode, all vectors are fetched from the 192-byte on-chip bootloader ROM. This modes is very versatile and can be used for such functions as test and diagnostics on completed modules and for programming the EEPROM. The serial receive logic is initialized by software in the bootloader ROM, which provides program control for the serial communications interface (SCI) baud and word format. In this mode, a special control bit is configured that allows for self-testing of the MCU. This mode can be changed to other modes under program control.

TEST MODE

This modes is primarily intended for main production at time of manufacture ; howerver, it may be used to program calibration or personality data into the internal EEPROM. In this mode, a special control bit is configured to permit access to a number of special test control bits. This mode can be changed to other modes under program control.

6.2 · Signal description

V_{DD} AND V_{SS}

Power is supplied to the microcontroller using these two pins. V_{DD} is +5 volts (± 0.25 V) power, and V_{SS} is ground.

$\overline{RESET}$

This active low bidirectional control pin is used as an input to initialize the MCU to a known startup state and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the computer operating properly (COP) circuit.

XTAL, EXTAL

These pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied shall be four times higher than the desired clock rate. Refer to Figure 1 for crystal and clock connections.

E

This pin provides an output for the internally generated E clock, which can be used for timing reference. The frequency of the E output is one-fourth that of the input frequency at the XTAL and EXTAL pins.

$\overline{IRQ}$

This pin provides the capability for asynchronously applying interrupts to the MCU. Either negative edge-sensitive or level-sensitive triggering is program selectable. This pin is configured to level sensitive during reset. An external resistor connected to V_{DD} is required on IRQ.

$\overline{XIRQ}$

This pin provides the capability for asynchronously applying non-maskable interrupts to the MCU after a power on reset (POR). During reset, the X bit in the condition code register is set, and anay interrupt is masked until enabled by software. This input is level-sensitive and requires an external pullup resistor to V_{DD}.

MODA/$\overline{LIR}$ AND MODB/V_{stby}

During reset, these pins are used to control the two basic operating modes and the two special operating modes. The $\overline{LIR}$ output can be used as an aid in debugging once reset is completed. The open-drain $\overline{LIR}$ pin goes to an active low during the first E-clock cycle of each instruction and remains low for the duration of that cycle. The mode selections are shown below.

MODB	MODA	Mode selected
1	0	Single chip
1	1	Expanded multiplexed
0	0	Special bootstrap
0	1	Special test

V_{RL} AND V_{RH}

These pins provide the reference voltage for the A/D converter.

R/$\overline{W}$/STRB

This pin provides two different functions, depending on the operating mode. In single-chip mode, the pin provides STRB (output strobe) function ; in the expanded multiplexed mode, it provides R/$\overline{W}$ (read-write) function. The R/$\overline{W}$ is used to control the direction of transfers on the external data bus.

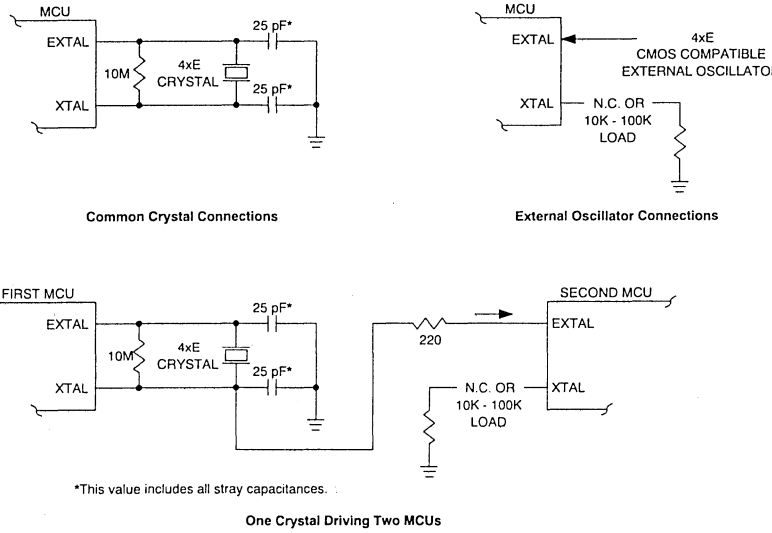


Figure 20 : Oscillator connections.

AS/STRA

This pin provides two different functions depending on the operating mode. In single-chip mode, the pin provides STRA (input strobe) function, and in the expanded-multiplexed mode, it provides AS (address strobe) function. The AS may be used to demultiplex the address and data signals at port C.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PE0-PE7)

These I/O lines are arranged into four 8-bit ports (A, B, C, and E) and one 6-bit port (D). All ports serve more than one purpose depending on the operating mode. Table 11 lists a summary of the pin functions to operating modes. Refer to INPUT/OUTPUT PORTS for additionnal information.

6.3 · Input/output ports

Port functions are controlled by the particular mode selected. In the single-chip mode and bootstrap mode, four ports are configured as parallel I/O data ports and port E can be used for general-purpose static inputs and/or analog-to-digital converter channel inputs. In the expanded-multiplexed mode and test mode, ports B, C, AS, and R/W are configured as a memory expansion bus. Table 11 lists the different port signals available. The following paragraphs describe each port.

PORT A

In all operating modes, port A may be configured for three input capture functions ; four output compare functions ; and pulse accumulator input (PAI) or a fifth output compare function. Each input capture pin provides for a transitional input, which is used to latch a timer value into the 16-bit input capture register. External devices provide the transitional input, and internal decoders determine which input transition edge is sensed. The output compare pins provide an output whenever a match is made between the value in the free-running counter (in the timer system) and a value loaded into the particular 16-bit output compare register. When port A bit 7 is configured as a PAI, the external input pulses are applied to the pulse accumulator system. The remaining port A lines may be used as general-purpose input or output lines.

PORT B

In the single-chip mode, all port B pins are general purpose output pins. Port B may also be used in a simple strobed output mode where the STRB pulses each time port B is written. In the expanded-multiplexed mode, all of the port B pins act as high-order (bits 8-15) address output pins.

Table 11 - Port signal functions

Port-bit	Single-chip and bootstrap mode	Expanded multiplexed and special test mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA0/IC2
A-2	PA2/IC1	PA0/IC1
A-3	PA3/OC5/ and-or OC1	PA3/OC5/ and-or OC1
A-4	PA4/OC4/ and-or OC1	PA4/OC4/ and-or OC1
A-5	PA5/OC3/ and-or OC1	PA5/OC3/ and-or OC1
A-6	PA6/OC2/ and-or OC1	PA6/OC2/ and-or OC1
A-7	PA7/PAI/ and-or OC1	PA7/PAI/ and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/R x D	PD0/R x D
D-1	PD1/T x D	PD1/T x D
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/SS	PD5/SS
	STRA	AS
	STRB	R/W
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4 (see Note)	PE4/AN4 (see Note)
E-5	PE5/AN5 (see Note)	PE5/AN5 (see Note)
E-6	PE6/AN6 (see Note)	PE6/AN6 (see Note)
E-7	PE7/AN7 (see Note)	PE7/AN7 (see Note)

Note : Non bonded in 48-pin versions.

PORT C

In the single-chip mode, port C pins are general-purpose input/output pins. Port C inputs can be latched by the STRA or may be used in full handshake modes of parallel I/O where the STRA input and STRB output acts as handshake control lines. In the expanded-multiplexed mode, port C pins are configured as multiplexed address/data pins. During the address cycle, bits 0 through 7 of the address are output on PC0-PC7 ; during the data cycle, bits 0 through 7 (PC0-PC7) are bidirectionnel data pins controlled by the R/W signal.

PORT D

In all modes, port D bits 0-5 may be used for general-purpose I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Bit 0 is the receive data input, and bit 1 is the transmit data output for the SCI. Bits 2 through 5 are used by the SPI subsystem.

PORT E

Port E is used for general-purpose static inputs and/or analog-to-digital channel inputs in all operating modes. Port E should not be read as static inputs while an A/D conversion is actually taking place.

6.4 · Memory

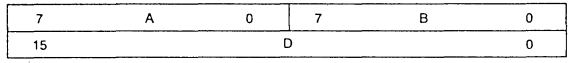
The memory maps for each mode of operation, a single-chip, expanded-multiplexed, special boot, and special test is shown in Figure 21. In the single-chip mode, the MCU does not generate external addresses. The internal memory locations are shown in the shaded areas, and the contents of the shaded areas are shown on the right side of the diagram. In the expanded-multiplexed mode, the memory locations are basically the same as the single-chip, except the memory locations between the shaded areas (EXT) are for externally addressed memory and I/O. The special bootstrap mode is similar to the single-chip mode, except the bootstrap program ROM is located at memory locations $BF40 through $BFFF. The special test mode is similar to the expanded-multiplexed mode, except the interrupt vectors are at external memory locations.

6.5 · Registers

The MCU contains the registers described in the following paragraphs.

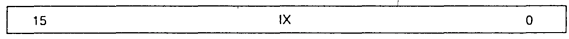
ACCUMULATOR A AND B

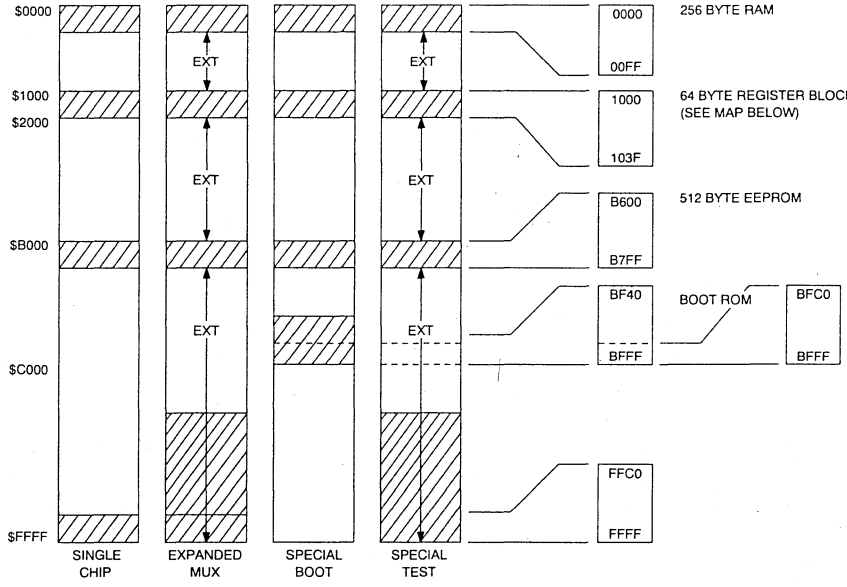
These accumulators are general-purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. These two accumulators are treated as a single, double-byte accumulator called the D accumulator fo some instructions.



INDEX REGISTER X (IX)

This index register is a 16-bit register used for the indexed addressing mode. It provides a 16-bit value that may be added to an 8-bit offset provided in an instruction to create an effective address. The index register may also be used either as a counter or a temporary storage area.





Note 1 : Either or both the internal RAM and registers can be remapped to any 4K boundary by software.

Note 2 : The EEPROM can be disabled using a control register (CONFIG), which is implemented with EEPROM celle.

Figure 21 : Memory map.

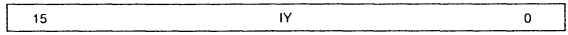
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	—	—	—	—	—	—	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
$1003	Bit 7	—	—	—	—	—	—	Bit 0	PORTC	I/O Port C
$1004	Bit 7	—	—	—	—	—	—	Bit 0	PORTB	Output Port B
$1005	Bit 7	—	—	—	—	—	—	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	—	—	—	—	—	—	Bit 0	DDRC	Data Direction for Port C
$1008	0	0	Bit 5	—	—	—	—	Bit 0	PORTD	I/O Port D
$1009	0	0	Bit 5	—	—	—	—	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	—	—	—	—	—	—	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC	Compare Force Register
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M	OC1 Action Mask Register
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D	OC1 Action Data Register
$100E	Bit 15	—	—	—	—	—	—	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	—	—	—	—	—	—	Bit 0		
$1010	Bit 15	—	—	—	—	—	—	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	—	—	—	—	—	—	Bit 0		
$1012	Bit 15	—	—	—	—	—	—	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	—	—	—	—	—	—	Bit 0		
$1014	Bit 15	—	—	—	—	—	—	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	—	—	—	—	—	—	Bit 0		
$1016	Bit 15	—	—	—	—	—	—	Bit 8	TOC1	Output Capture 1 Register
$1017	Bit 7	—	—	—	—	—	—	Bit 0		
$1018	Bit 15	—	—	—	—	—	—	Bit 8	TOC2	Output Capture 2 Register
$1019	Bit 7	—	—	—	—	—	—	Bit 0		
$101A	Bit 15	—	—	—	—	—	—	Bit 8	TOC3	Output Capture 3 Register
$101B	Bit 7	—	—	—	—	—	—	Bit 0		
$101C	Bit 15	—	—	—	—	—	—	Bit 8	TOC4	Output Capture 4 Register
$101D	Bit 7	—	—	—	—	—	—	Bit 0		
$101E	Bit 15	—	—	—	—	—	—	Bit 8	TI4O5	Output Capture 5 Register
$101F	Bit 7	—	—	—	—	—	—	Bit 0		Input Capture 4 Register
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2

6

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1022	OC1I	OC2I	OC3I	OC4I	I405I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Reg. 1
$1023	OC1F	OC2F	OC3F	OC4F	I405F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Reg. 1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2	Timer Interrupt Mask Reg. 2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2	Timer Interrupt Flag Reg. 1
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL	Pulse Accum. Control Reg.
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accum. Count Reg.
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCCR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	ADR1	EEPROM Block Protect Reg.
$1036 Thru $1038									Reserved	
$1039	ADPU	CSEL	IRGE	DLY	CME	0	CR1	CR0	OPTION	System Configuration Options
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circuitry
$103B	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Prog. Control Reg.
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int and Misc
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Reg.
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
$103F						NOCOP	ROMON	EEON	CONFIG	COP, ROM, and EEPROM Enables.

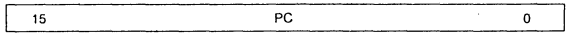
INDEX REGISTER (IY)

This index register is an 16-bit register used for the indexed addressing mode similar to the IX register ; however, most instructions using the IY register are two-byte opcodes and require an extra byte of machine code and an extra cycle of execution time. Time index register may also be used as a counter or a temporary storage area.



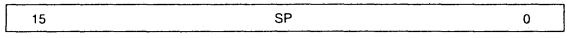
PROGRAM COUNTER (PC)

The program counter is a 16-bit register that contains the address of the next byte to be fetched.



STACK POINTER (SP)

The stack pointer is a 16-bit register that contains the address of the next free location on the stack. The stack is configured as a sequence of last-in-first-out read/write registers, which allow important data to be stored during interrupts and subroutine calls. Each time a new byte is added to the stack, the SP is incremented ; each time a byte is removed, the SP is incremented. The address contained in the SP also indicates the location at which the accumulators A and B registers IX and IY can be stored during certain instructions.



CONDITION CODE REGISTER (CCR)

The condition code register is an 8-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

7	6	5	4	3	2	1	0
S	X	H	I	N	Z	V	C

6

Carry/Borrow (C)
When set, this bit indicates that a carry of borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate instructions.

Overflow (V)
The overflow bit is set if an arithmetic overflow occured as a result of the operation ; otherwise the V bit is cleared.

Zero (Z)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Negative (N)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (the MSB of the result is a logic one).

Interrupt (I)
This bit is set either by hardware or program instruction to disable (mask) all maskable interrupt sources (both external and internal).

Half carry (H)
This bit is set during ADD, ABA, and ADC operations to indicate that a carry occured between bits 3 and 4. This bit is mainly useful in BCD calculations.

X interrupt mask (X)
This mask bit is set only by hardware (reset or $\overline{\text{XIRQ}}$) and is cleared only by program instruction (TAP or RTI).

Stop disable (S)
This bit, under program control, is set to disable the STOP instruction, and is cleared to enable the STOP instruction. The STOP instructions is treated as no operation (NOP) if the S bit is set.

6.6 · Resets

The MCU can be reset four ways :

- an active low input to the $\overline{\text{RESET}}$ pin,
- a power-on reset function,
- a computer operating properly (COP) watchdog-timer timeout and,
- a clock monitor failure.

The $\overline{\text{RESET}}$ input consists mainly of a Schmitt trigger that senses the $\overline{\text{RESET}}$ line logic level.

RESET PIN

To request an external reset, the $\overline{\text{RESET}}$ pin must be held low for eigh E_{cyc} (two E_{cyc} if no distinction is needed between internal and external resets). To prevent the EEPROM contents from being corrupted during power transitions, the reset line should be held low while V_{DD} is below its minimum operating level. A low voltage inhibit (LVI) circuit is required to protect EEPROM from corruption as shown in Figure 22.

POWER-ON RESET (POR)

Power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drop in the power supply voltage. If the external $\overline{\text{RESET}}$ pin is low at the end of the power-on delay time, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

COMPUTER OPERATING PROPERLY (COP) RESET

The MCU contains a watchdog timer that automatically times out if not reset within a specific time by a program reset sequence. If the COP watchdog timer is allowed to timeout, a reset is generated, which drives the $\overline{\text{RESET}}$ pin low to reset the MCU and the external system.

The COP reset function can be enabled or disabled by setting the control bit in an EEPROM cell of the system configuration register. Once programmed, this control bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. Protected control bits (CR1 and CR0),in the configuration options register, allow the user to select one of four COP timeout rates. Table 12 shows the relationship between CR1 and CR0 and the COP timeout period for various system clock frequencies.

CLOCK MONITOR RESET

The MCU contains a clock monitor circuit which measures the E clock input frequency. If the E clock input rate is above 200 kHz, then the clock monitor does not generate a MCU reset. If the E clock signal is lost or its frequency falls below 10 kHz, then a MCU reset is generated, and the $\overline{\text{RESET}}$ pin is driven low to reset the external system.

The clock monitor reset can be enabled or disabled by a read-write control bit (CME) in the system configuration options regter.

6.7 · Interrupts

There are seventeen hardware and one software interrupts (excluding reset type interrupts) that can be generated from all the possible sources. These interrupts can be divided into two categories, maskable and non-maskable. Fifteen of the interrupts can be masked with the condition code register I bit. All the on-chip interrupts are individually maskable by local control bits. The software interrupt is non-maskable. The external input to the $\overline{\text{XIRQ}}$ pin is considered a non-maskable interrupt because, once enabled, it cannot be masked by software ; however, it is masked during reset and upon receipt of an interrupt at the $\overline{\text{XIRQ}}$ pin. The last interrupt, illegal opcode, is alos a non-maskable interrupt. Table 13 provides a list of each interrupt, its vector location in ROM, and the actual condition code and control bits that mask it. Figure 23 shows the interrupt stacking order.

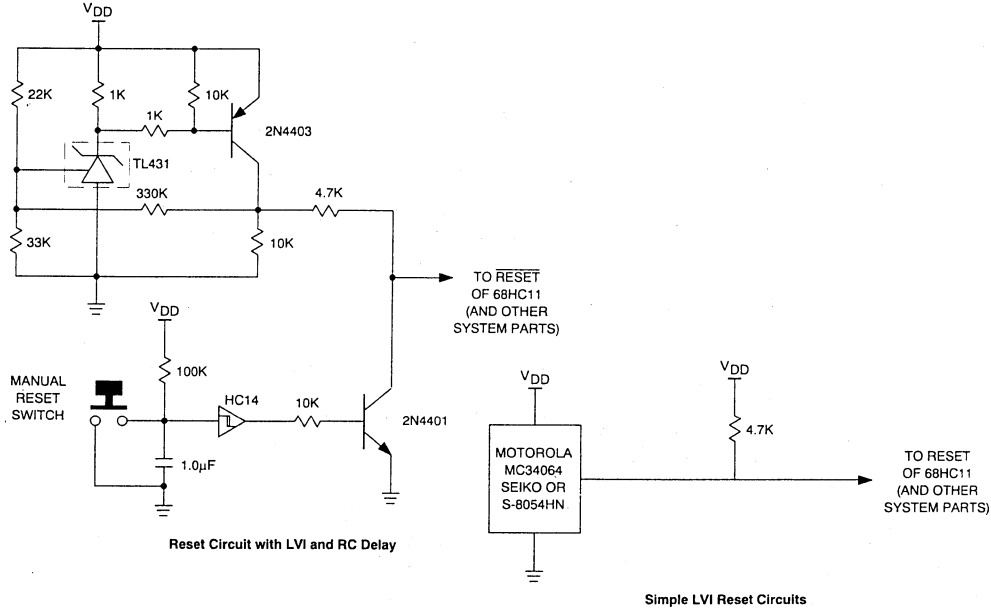


Figure 22 : Typical LVI reset circuits.

Table 12 - COP timeout periods

CR1	CR0	E/2^{15} divided by	XTAL = 2^{23} timeout −1/+15.6 ms	XTAL = 8.0 MHz timeout −0/+16.4 ms	XTAL = 4.9152 MHz timeout −0/+26.7 ms	XTAL = 4.0 MHz timeout −0/+32.8 ms	XTAL = 3.6864 MHz timeout −0/+35.6 ms
0	0	1	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	4	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	16	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	64	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

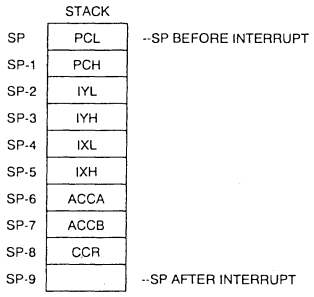


Figure 23 : Stacking order.

6

SOFTWARE INTERRUPT (SWI)

The SWI is executed the same as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the CCR set). The SWI execution is similar to the maskable interrupts such as setting the I bit, CPU registers are stacked, etc.

Note : The SWI instruction cannot be fetched as long as another interrupt is pending execution. However, once fetched, no other interrupt can be honored until the first instruction in the SWI service routine is completed.

ILLEGAL OPCODE TRAP

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included in the MCU. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector.

REAL-TIME INTERRUPT

The real-time interrupt provides a programmable periodic interrupt. This interrupt is maskable by either the 1 bit in the CCR or the RTII control bit. The rate is based on the MCU E clock and is software selectable to be E/2^{13}, E/2^{14}, E/2^{15}, or E/2^{16}.

Table 13 - Interrupt vector assignments

Vector address	Interrupt source	CC register mask	Local mask
FFC0, C1	Reserved		
*	*		
*	*		
FFD4, D5,	Reserved		
FFD6, D7	SCI serial system	I bit	
	Receive data register full		RIE
	Receive overrun		RIE
	Idle line detect		ILIE
	Transmit data register empty		TIE
	Transmit complet		TCIE
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflowd	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer output compare 5	I bit	OC5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	OC3I
FFEC, ED	Timer input capture 2	I bit	OC2I
FFEE, EF	Timer input capture 1	I bit	OC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	IRQ (external pin or parallel I/O)	I bit	
	External pin		None
	Parallel I/O handshake		STAI
FFF4, F5	XIRQ pin (pseudo non-maskable interrupt)	X bit	None
FFF6, F7	SWI	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure (reset)	None	NOCOP
FFFC, FD	COP clock monitor fail (reset)	None	CME
FFFE, FF	RESET	None	None

6.8 - Low-power modes

The MCU contains two programmable low-power operating modes : stop and wait. In the wait mode, the on-chip oscillator remains active ; in the stop mode, the oscillator is stopped. The following paragraphs describe the tow low-power modes.

STOP

The STOP instruciton places the MCU in its lowest power consumption mode, provided the S bit in the CCR is clear. In this mode, all clocks are stopped, thereby halting all internal processing.

To exit the stop mode, a low level must be applied to either $\overline{IRQ}$, $\overline{XIRQ}$ or $\overline{RESET}$. An external interrupt used at $\overline{IRQ}$ is only effective if the I bit in the CCR is clear. An external interrupt applied at the $\overline{XIRQ}$ input would be effective regardless of the X-bit setting in the CCR ; however, the actual recovery sequence differs, depending on the X-bit setting. If the X bit is clear, the MCU starts with the stacking sequence leading to the normal service of the $\overline{XIRQ}$ request. If the X bit is set, the processing will continue (if no $\overline{XIRQ}$ interrupt service routine is requested) with the instruction immediately following the STOP instruction. A low input to the $\overline{RESET}$ pin will always result in an exit from the stop mode, and the start of MCU operations is determined by the reset vector.

If the internal oscillator is being used, a restart delay is required to allow the oscillator to stabilize when exiting the stop mode. If a stable external oscillator is being used, a control bit in the OPTION register may be used (cleared) to bypass the delay. If the control bit is clear, then the $\overline{RESET}$ pin would not normally be used for exiting the stop mode. In this case, the reset sequence sets the delay control bit, and the restart delay will be imposed.

WAIT

The WAIT instruction places the MCU in a low-power consumption mode, but the WAIT mode consumes slightly more power than the STOP mode. In the WAIT mode, the oscillator is kept running. Upon execution of the WAIT instruction, the machine state is stacked and program execution stops. The WAIT state can only be exited by an unmasked interrupt or $\overline{RESET}$. If the I bit is set and the COP is disabled, the timer system will be turned off to further reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins and upon subsystems (i.e., timer, SPI SCI) that are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT-mode current.

6.9 - Programmable timer

The timer system uses a «time-of-day» approach in that all timing functions are related to a single 16-bit free-running counter. The free-running counter is clocked by the output of a programmable prescaler (divide by 1, 4, 8, or 16), which is, in turn, clocked by the MCU E clock. The free-running counter can be read by software at any time without affecting its value because it is clocked and read on opposite half cycles of the E clock. The counter is cleared on reset and is a read-only register. The counter repeats every 65,536 counts, and when the count changes from $FFFF to $0000, a timer overflow flag bit is set. The overflow flag also generates an internal interrupt if the overflow interrupt enable bit is set. The timer has three input capture and five output compare functions. The functions and registers of the timer are explainded in the following paragraphs.

INPUT CAPTURE FUNCTION

There are three 16-bit read-only input capture registers that are not affected by reset. Each register is used to latch the value of the free-running courter when a selected transition at an external pin is detected. External devices provide the inputs on the PA0-PA2 pins, and an interrupt can be generated when an input capture edge is detected. The time of detection can be read from the appropriate register as part of the interrupt routine.

TIMER CONTROL REGISTER 2 (TCTL2)

7	6	5	4	3	2	1	0
0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3A	EDG3A
RESET							
0	0	0	0	0	0	0	0

Bits 7-6 — not implemented

These bits always read zero.

EDGxB and EDGxA — input capture x edge control.

These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x.

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or faling) edge

6

OUTPUT COMPARE FUNCTION

There are five 16-bit read/write output compare registers, which are set to $FFFF on reset. A value writtne into the SE registers is compared to the free-running counter value during each E-clock cycle. If a match is found, the particular output compare flag is set, and an interrupt is generated, provided that particular interrupt is enabled.

In addition to the interrupt, a specified action may be intitiated at a timer output pin(s). For output compare one (OC1), the output action to be taken when a match is found is controlled by a 5-bit mask register and a 5-bit data regiser. The mask register specifies which timer port outputs are to be used, and the data register specifies what data is placed on the SE timer ports. For OC2 through OC5, one specific timer output is affected as controlled by the two-bit fields in a timer control register. These action include :

- timer disconnect from output pin logic,
- toggle output compare line,
- clear output compare line to zero, or
- set output compare line to one.

TIMER COMPARE FORCE REGISTER (CFORC)

This 8-bit write-only register is used to force early output compare actions. This compare force functions is not recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undersirable operation.

7	6	5	4	3	2	1	0
FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET							
0	0	0	0	0	0	0	0

F0C1-C0C5 — Force outpt compare x action
1 = causes action programmed for output compare x, except the OCxF flag bit is not set.
0 = has no meaning
Bits 2-0 — not implemented. These bits always read zero.

OUTPUT COMPARE 1 MASK REGISTER (0C1M)

This register is used with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET							
0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

OUTPUT COMPARE 1 DATA REGISTER (OC1D)

This register is used with output compare 1 to specify the data which is to be stored to the affected bit of port A as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET							
0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output ot port A bit-x on successful OC1 compares.

TIMER CONTROL REGISTER (TCTL1)

7	6	5	4	3	2	1	0
OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET							
0	0	0	0	0	0	0	0

OM2-OM5 — output mode
OL2-OL5 — output level.
These control bit pairs (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

OMx	OLx	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TIMER INTERRUPT MASK REGISTER 1 (TMSK1)

7	6	5	4	3	2	1	0
OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I
RESET							
0	0	0	0	0	0	0	0

OCxI — output compare x interrupt
- 1 = interrupt sequence requested if OCxF-1 in TFLG1
- 0 = interrupt inhibited

Cx | — input capture x interrupt
- 1 = interrupt sequence requested if ICxF-1 in TFLG1
- 0 = interrupt inhibited.

TIMER INTERRUPT FLAG REGISTER 1 (TFLG1)

This register is used to indicate the occurence of timer system events and, with the TMSK1 register, allows the timer sybsystem to operate in a polled or interrupt driven system. Each bit in the TFLG1 has a corresponding bit in the TMSK1 in the same bit position.

7	6	5	4	3	2	1	0
OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F
RESET							
0	0	0	0	0	0	0	0

OCxF — output compare x flag

Set each time the timer counter matches the output compare register x value. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
- 1 = bit cleared
- 0 = not affected.

ICxF — input capture x flag

Set each time a selected active edge is detected on the ICx input line. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
- 1 = bit cleared
- 0 = not affected.

TIMER INTERRUPT MASK REGISTER 2 (TMSK2)

This register is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in TFLG1. Two timer prescaler bits are also included in this register.

7	6	5	4	3	2	1	0
TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET							
0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt enable
- 1 = interrupt request when TOF = 1
- 0 = TOF interrupt disabled.

RTII — RTI Interrupt enable
- 1 = interrupt requested when RTIF = 1
- 0 = RTIF interrupt disabled

PAOVI — Pulse Accumulator OVerflow Interrupt enable
- 1 = interrupt requested when PAOVF = 1
- 0 = PAOVF disabled.

PAII — Pulse Accumulator Input Interrupt enable
1 = interrupt requested when PAIF = 1
0 = PAIF disabeld.

Bits 3-2 — not implemented
These bits always read zero.

PR1 and PR0 — timer prescaler selects.
Can only be written to during intitialization. Writes are disabled after the first write or after 64 E cycles our of reset.

PR1	PR0	Divide-by-factor
0	0	1
0	1	4
1	0	8
1	1	16

TIMER INTERRUPT FLAG RESTIER 2 (TFLG2)

This register is used to indicate the occurrence of timer system events and, with the TMSK2 register, allows the timer subsystem to operate in a polled or interrupt driven system. Each bit in the TFLG2 has a corresponding bit in the TMSK2 in the same bit position.

7	6	5	4	3	2	1	0
TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

TOF — Timer Overflow
Set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. Cleared by a write to TFLG2 with bit 7 set.

RTIF — Real-Time Interrupt Flag
Set at each rising edge of the seleted tap point. Cleared by a write to TFLG2 with bit 6 set.

PAOVF — Pulse-Accumulator OVerflow interrupt Flag
Set when the count in the pulse accumulator rolls over from $FF to $00. Cleared by a write to the TFLG2 with bit 5 set.

PAIF — Pulse-Accumulator Input-edge interrupt Flag
Set when an active edge is detected on the PAI input pin. Cleared by a write to TFLG2 with bit 4 set.

Bits 3-0 — not implemented
These bits always read zero.

RTR1	RTR0	Divide E by	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	2^{13}	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	2^{14}	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	2^{15}	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	2^{16}	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

6.10 - Pulse accumulator

The pulse accumulator is an 8-bit counter that can operate in either of two modes, depending on the state of a control bit in the PACTL register. These are the event counting mode and the gated time accumulation mode. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is activated.

PULSE ACCUMULATOR CONTROL REGISTER (PACTL) $1026

Four bits in this register are used to control an 8-bit pulse accumulator system, and tow other bits are used to select the rate for the real-time interrupt system.

7	6	5	4	3	2	1	0
DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0
RESET							
0	0	0	0	0	0	0	0

DDRA7 — Data Direction for port A bit 7

1 = output

0 = input only

PAEN — Pulse-Accumulator system ENable

1 = pulse accumulator on

0 = pulse accumulator off

PAMOD — Pulse Accumulator Mode

1 = gated time accumultor

0 = exernal even counting

PEDGE — Pulse accumulator EDGE control

This bit provides clock action along with PAMOD.

1 = sensitive to rising edges at PAI pin inf PAMOD = 0. In gated accumulation mode counting is enabled by a low on PAI pin if PAMOD = 1.

0 = sensitive to falling edges at PAI pin if PAMOD = 0. In gated accumulation mode counting is enabled by a high on PAI pin if PAMOD = 1

Bits 3-2 — not implemented

These bits always read zero.

RTR1 and RTR0 — RTI interrupt rate selects.

These two bits select one of four rates for the real-time periodic interrupt circuits. Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

6.11 - EEPROM programming

The 512 bytes of EEPROM are located at $B600 through $B7FF and have the same read cycle time as the internal ROM. Programming of the EEPROM is controled by the EEPROM programming control register (PPROG). The EEPROM is disabled when the EEON bit in the system configuration register (CONFIG) is zero. Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz, the efficiency of this charge pump decreases, which increases the time required to program or erase a location. Recommended program and erase time is 10 milliseconds when the E clock is between 2 MHz and should be increased to as much as 20 milliseconds when E clock is between 1 MHz and 2 MHz. When E clock below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. The following paragraphs describe how to program or erase the EEPROM using the PPROG control register.

ERASING THE EEPROM

Erasure for the EEPROM is controled by bit settings in PPROG. Programs can be written to perform bulk, row, or byte erase. In bulk erase, all 512 bytes of the EEPROM are erased. In row erase, 16 bytes ($B600-$B60F-$B610-$B61F), etc are erased. Other MCU operations can continue to be performed during erasing provided the operations do not include reads of data from EEPROM.

PROGRAMMING EEPROM

During programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Zeros must be erased by a separate erase operation before programming. Other MCU operations can continue to be performed during programming provided the operations do not include reads of data frome EEPROM.

EEPROM PROGRAMMING CONTROL REGISTER (PPROG) $103B

This 8-bit register is used to control programming and erasure of the EEPROM. This register is cleared on reset so the EEPROM is configured for normal reads.

7	6	5	4	3	2	1	0
ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET							
0	0	0	0	0	0	0	0

ODD — program odd rows (TEST)

EVEN — program even rows (TEST)

Bit 5 — not implemented.

This bit always reads zero.

BYTE — byte erase select.

This bit overrides the ROW bit.

1 = erase only one byte

0 = row or bulk erase.

ROW — row erase select.

If BYTE bit = 1, ROW has no meaning.

1 = row erase

0 = bulk or byte erase.

ERASE — erase mode select.

1 = erase mode

0 = normal read or program.

EELAT — EEPROM latch control.

1 = EEPROM address and data configured for programming/erasing

0 = EEPROM address and data configured for read mode.

EEPGM — EEPROM programming voltage enable

1 = programming voltage turned on

0 = programming voltage turned off.

Note : If an attempt is made to set both the EELAT and EEPGM bit in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit si set, the write is ignored, and the programming operation currently in progress is not disturbed. If no EEPROM address is written between when EELAT is set and EEPGM is set, then no program or erase operation will take place. These safeguards were included to prevent accidental EEPROM changes in cases of program runaway.

ERASING THE CONFIG REGISTER

Erasing the CONFIG register follows the same procedures as that used for the EEPROM except that only bulk erase can be used on the CONFIG register. When the CONFIG register is erased, the EEPROM array is also erased.

PROGRAMMING THE CONFIG REGISTER

Programming the CONFIG register follows the same procedures as that used for the EEPROM except the CONFIG register address is used.

SYSTEM CONFIGURATION REGISTER (CONFIG)

The CONFIG is implemented in EEPROM cells and controls the presense of ROM and EEPROM in the memory map and enables the COP watchdog system.

7	6	5	4	3	2	1	0
					NOCOP	ROMON	EEOM

Bits 7-4 — not implemented
These bits are always read as zero.

Bit 3 — not implemented
This bit always reads one.

NOCOP — COP system disable
1 = COP watchdog system disabled
0 = COP watchdog system enabled

ROMON — enable on-chip ROM
This bit is programmed to «zero», disabling the 8K ROM. The 8K ROM memory space becomes externally accessed space. Changing this bit leads to accessing an undefined ROM.

EEON — enable on-chip EEPROM
When this bit is programmed to «zero», the 512-byte EEPROM is disabled, and that memory space becomes externally accessed space.

6.12 · Serial communications interface

The serial communications interface (SCI) allows the MCU to be efficiently interfaced with peripheral devices that require an asynchronous serial data format. The SCI uses a standard NRZ format with a variety of baud rates derived from the crystal clock circuit. Interfacing is accomplished using port D pins : PD0 for receive data (RxD) and PD1 for the transmit data (TxD). The baud-rate generation circuit contains a programmable prescaler and divider clocked by the MCU E clock. Figure 24 shows a block diagram of the SCI.

DATA FORMAT

Receive data in or transmit data out is the serial data presented between the PD0 and the internal data bus and between the internal data bus and PD1. The data format requires :

- an idle line in the high state prior to transmission/reception of a message,
- a start bit that is transmitted/received, indicating the start of each character,
- data that is transmitted and received least-significant bit (LSB) first,
- a stop bit (tenth or eleventh bit set to logic one), which indicates the frame is complet ; and
- a break defined as the transmission or reception of a logic zero for some multiple of frames.

Selection of the word length is controlled by the M bit in serial communications control register 1 (SCCR1).

TRANSMIT OPERATION

The SCI transmitter includes a parallel data register and a serial shift register. This double-buffered system allows a character to be shifted out serially while another character is waiting in the transmit data register to be transferred into the serial shift register. The output of the serial shift register is applied to PD1 as long as transmission is in progress or the transmit enable bit is set.

RECEIVE OPERATION

Data is received in a serial shift register and is transferred to a parallel receive data register as a complete word. This double-buffered system allows a character to be shifted in serially while another character is already in the receive data register. An advanced data recovery scheme is used to distinguish valid data from noise in the serial data stream. The data input is selectively sampled to detect receive data, and a majority voting circuit determines the value and intergrity of each bit.

WAKE-UP FEATURE

The wake-up feature reduces SCI service overhead in multiple receiver systems. Software for each receiver evaluates the first character(s) of each message. If the message is intended for a different receiver, the SCI can be placed in a sleep mode, disabling the rest of the message from generating requests for service. Whenever a new message begins, logic causes the sleeping receivers to awaken and evaluate the initial character(s) of the new message. Two methods of wake up are available : idle-line wake up or address mark wake up. In idle-line wake up, a sleeping receiver wakes up as soon as the RxD line becomes idel. In the address mark wake up, a «one» in the most-significant bit (MSB) of a character is used to indicate that the message is an address that wakes up a sleeping receiver.

SCI REGISTERS

The following paragraphs describe the operations of the five registers used in the SCI.

Serial communications data registers (SCDR)
The SCDR performs two functions : as the receive data register when it is read and as the transmit data register when it is written. Figure 24 shows the SCDR as two separate registers.

Serial communications control register 1 (SCCR1)
The SCCR1 provides the control bits to determine word length and select the method used for the wake-up feature.

7	6	5	4	3	2	1	0
R8	T8	0	M	WAKE	0	0	0
RESET							
U	U	0	0	0	0	0	0

R8 — receive data bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

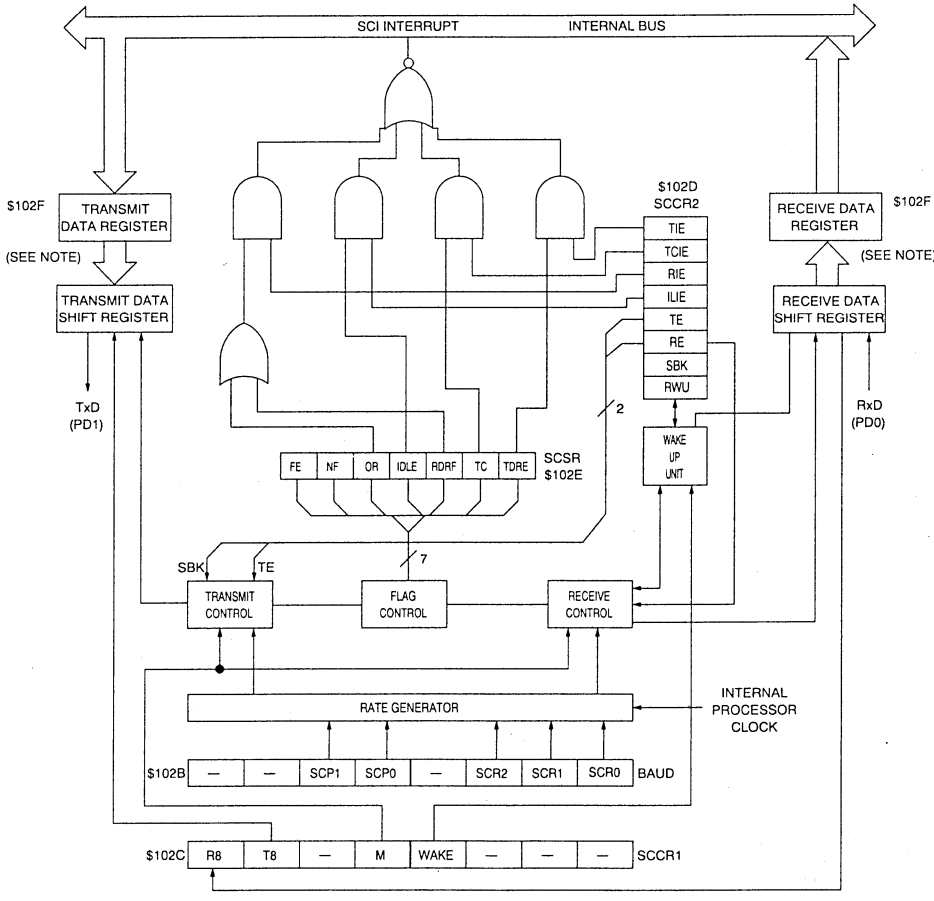
T8 — transmit data bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character.

Bit 5 — not implemented
This bit always reads zero.

M — SCI character length
1 = 1 start bit, 9 data bits, 1 stop bit
0 = 1 start bit, 8 data bits, 1 stop bit.

WAKE — wake-up method select
1 = address mark
0 = idle line.

Bits 2-0 — not implemented
These bits always read zero.



Note : The serial communications data register (SCDR) is controlled by the internal R/W signal. It is the transmit data register when written and received data register when read.

Figure 24 : SCI block diagram.

Serial conmmunications control register 2 (SCCR2)
The SSCR2 provides the control bits that enable/disable individual SCI functions.

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET							
0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
1 = SCI interrupt if TDRE = 1
0 = TDR interrupts disabled.

TCIE — Transmit-Complete Interrupt Enable
1 = SCI interrupt if TC = 1
0 = TC interrupts disabled.

RIE — Receive Interrupt Enabled
1 = SCI interrupt if RDRF or OR = 1
0 = RDRF or OR interrupt disabled.

IE — Idle-line interupt Enable
1 = SCI interrupt if IDLE = 1
0 = IDLE interrupt disabled.

E — transmit Enable
1 = transmit shift register output is applied to the TxD line
0 = PD1 pin reverts to general-purpose I/O as soon as current transmitter activity finishes.

RE — Receive Enable
1 = receiver enabled
0 = receiver disabled and RDRF, IDLE, OR, NF, and FE interrupts are inhibited.

RWU — Receiver Wake Up
When set by user's software, this bit puts the receiver to sleep and enables the «wake-up» function. If the WAKE bit is zero, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If WAKE is one, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send BreaK
If this bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or to sending data. If SBK remains sets, the transmitter will continually send whole frames of zeros (sets of 10 or 11) until cleared.

Serial communications status register (SCSR)
The SCSR provides inputs to the interrupt logic circuits for generation of the SCI system interrupts.

7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET							
1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty
1 = automatically set when contents of the serial communications data register was transferred to the transmit serial shift register
0 = cleared by a read of SCSR (with TDRE = 1) followed by a write to SCDR.

TC — Transmit Complete
1 = automatically set when all data frame, preambel, or break condition transmissions are complete
0 = cleared by a read of SCSR (with TC = 1) followed by a write to SCDR.

RDRF — Receive Data Register Full
1 = automatically set when a character is transferred from the receiver shift register to the SCDR
0 = cleared by a read of SCDR (with RDRF = 1) followed by a read of SCDR.

IDLE — IDLE-line detect
This bit is inhibited while RWU = 1.
1 = automatically set when the receiver serial input becomes idle after having been active
0 = cleared by a read of SCSR (with IDLE = 1) followed by a read of SCDR.

OR — Overrun error

1 = automatically set when a new character cannot transfer from the receive shift register because the character in SCDR has not been read

0 = cleared by a read of SCSR (with OR = 1) followed by a read of SCDR.

NF — Noise Flag

1 = automatically set when majority voting logic does not bind unanimous agreement of all samples in any bit in the recieved frame

0 = cleared by a read of SCSR (with NF = 1) followed by a write to SCDR.

FE — Framing Error

1 = automatically set when a logic 0 is detected where a stop bit was expected

0 = cleared by a read of SCSR (with FE = 1) followed by a read of SCDR.

Bit 0 — not implemented

This bit always reads zero.

Baud-rate register (BAUD)

This register is used to select different baud rates that may be used as the rate control for the receiver and transmitter.

7	6	5	4	3	2	1	0
TDLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET							
1	1	0	0	0	U	U	U

TCLR — clear baud-rate counters (test)

This bit is used to clear the baud-rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

Bit 6 — not implemented

This bit always reads zero.

SCPI and SCP0 — SCI baud-rates prescaler selects

These bits control a prescaler whose output provides the input to a second divider which is controlled by the SCR2-SCR0 bits. Refer to Table 14.

RCKB — SCI baud-rate clock check (test)

This bit is used during factory testing to enable the exlcusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

SCR2-SCR0 — SCI baud-rate selects

These bits select the baud rate for both the transmitter and the receiver. The precaler output selected by SCP1 and SCP0 is further divided by the setting of these bits. Refer to Table 15.

Table 14 - Prescaler highest baud-rate frequency output

SCP bit		Clock * divided by	Crystal frequency (MHz)				
1	0		8.3886	8.0	4.9152	4.0	3.6864
0	0	1	131.072 K Baud	125.000 K Baud	76.80 K Baud	62.50 K Baud	57.60 K Baud
0	1	3	43.690 K Baud	41.666 K Baud	25.60 K Baud	20.833 K Baud	19.20 K Baud
1	0	4	32.768 K Baud	31.250 K Baud	19.20 K Baud	15.625 K Baud	14.40 K Baud
1	1	13	10.082 K Baud	9600 K Baud	5.907 K Baud	48000 K Baud	4430 K Baud

* The clock in the «clock divide by» column is the internal processor clock.

Table 15 - Transmit baud-rate output for a given prescaler output

SCR bit			Divided by	Representative highest output for baud-rate output				
2	1	0		131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 bau	600 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud

6.13 - Serial peripheral interface

The serial peripheral interface (SPI) is a high-speed synchronous serial I/O system. The transfer rate is software selectable up to one-half of the MCU E clock rate. The SPI may be used for simple I/O expansion or to allow several MCUs to be interconnected in a multimaster configuration. Clock phase and polarity are software programmable to allow direct compatibility with a large number of peripheral devices.

Four basic signal lines are associated with the SPI system. These are the master-out-slave-in (MOSI), the master-in-slave-out (MISO), the serial clock (SCK), and the slate select (SS). When data is writtent to the SPI data register of a master device, a transfer is automatically initiated. A series of eight SCK clock cycles are generated to synchronize data transfer.

When a master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. The byte transmitted is replaced by the byte received, thereby eliminating the need for separate transmit-empty and receiver-full status bits. Figure 25 shows a block diagram of the SPI.

6

SPI REGISTERS

There are three registers in the SPI that provide control, status, and data-storage functions. These registers are described in the following paragraphs.

Serial peripheral control register (SPCR)

7	6	5	4	3	2	1	0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET							
0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
- 1 = SPI interrupt if SPIF = 1
- 0 = SPIF interrupts disabled

SPE — Serial Peripheral system Enable
- 1 = SPI system on
- 0 = SPI system off

DWOM — port D Wire-OR Mode option
This bit affects all six port D together.
- 1 = port D outputs act as open-drain outputs
- 0 = port D outputs are normal CMOS outputs

MSTR — master mode select
- 1 = master mode
- 0 = slave mode

CPOL — Clock Polarity
This bit selects the polarity of the SCK clock.
- 1 = SCK line idles high
- 0 = SCK line idles low

CPHA — Clock PHAse

This bit selects one of two fundamentally different clock protocols. Refer to Figure 26.

SPR1 and SPR0 — SPI clock rate select

These two bits select on of four baud rates to be used as SCK if the SPI is set as the master. They have no effect in the slave mode.

SPR1	SPR0	Internal processor clock divide by
0	0	5
0	1	4
1	0	16
1	1	32

Serial Peripheral Status Register (SPSR)

7	6	5	4	3	2	1	0
SPIF	WCOL	0	MODF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

SPIF — SPI transfer complete flag

1 = automatically set when data transfer is complete between processor and external device

0 = cleared by a read of SPSR (with SPIF = 1), followed by a access (read or write) of the SPDR.

WCOL — Write COLlision

If CPHA = 0, transfer begins when SS goes low and ends when SS goes high after eight clock cycles on SCK. If CPHA = 1, transfer begins the first time SCK becomes active while SS is low and ends when the SPIF flag gets set.

1 = automatically set when an attempt is made to write to the SPI data register while data is being transferred

0 = cleared by a read of SPSR (with WCOL = 1), followed by an access (read or write) of the SPDR.

Bit 5 — not implemented

This bit always reads zero.

MODF — mode fault

This bit indicates the possibility of a multi-master conflict for system control and therefore allows a proper exit from system operation to a reset or default system state.

1 = automatically set when a master device has its SS pin pulled low

0 = cleared by a read of SPSR (with MODF = 1), followed by a write to the SPCR.

Bits 3-0 — not implemented

These bits always read zero.

Serial peripheral data I/O (SPDR)

This register is used to transmit and receive data on the serial bus. A write to this register in a master will initiate transmission/reception of another byte. A slave writes data to this register for later transmission to a master. When transmission is complete, the SPIF status bit is set in both the master and slave device. When a read is performed on the SPDR, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated, or an overrun condition will exist. In case of an overrrun, the byte causing the overrrun is lost.

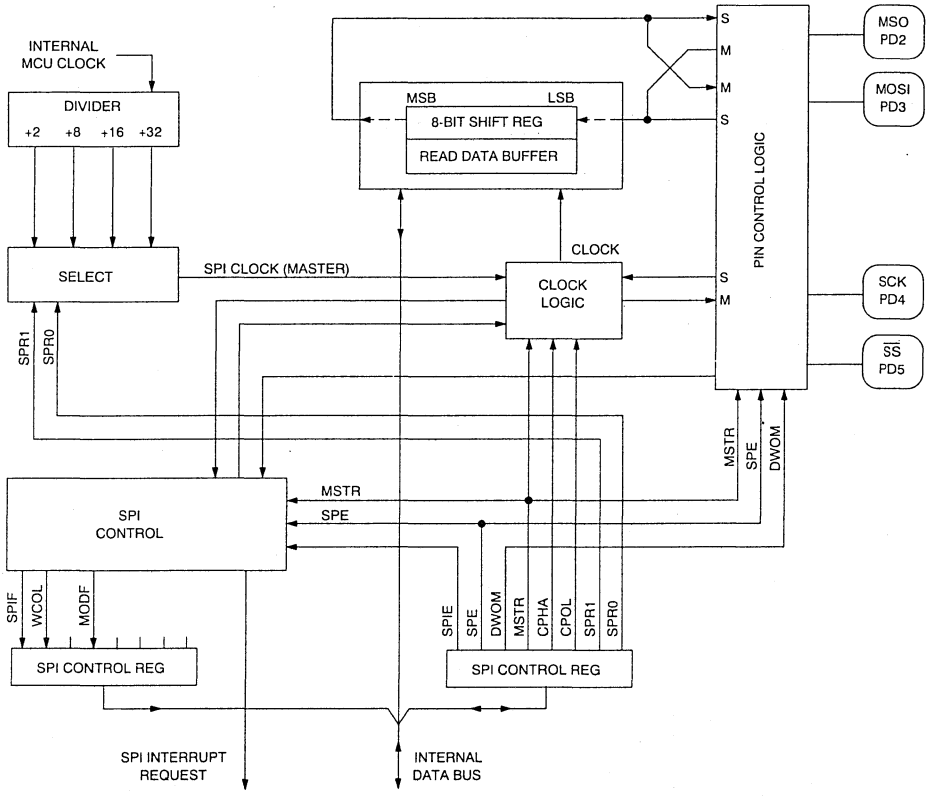


Figure 25 : SPI block diagram.

6.14 · Analog-to-digital converter

The MCU contains an 8-channel, multiplexed-intput, successive approximation, analog-to-digital (A/D) converter with sample and hold. Two dedicated lines (V_{RL}, and V_{RH}) are provided for the reference supply voltage input. These pins are used instead of the device power pins to increase the accuracy of the A/D converions.

The 8-bit A/D conversion of the MCU are accurate to within ± 1 LSB (± 1/2 LSB quantizing errors and ± 1/2 LSB all other errors combined). Each conversion is accomplished in 32 MCU E-clock cycles. An internal control bit allows selection of an internal conversion clock oscillator that allows the A/D to be used with very low MCU clock rates. A typical conversion cycle requires 16 microseconds to complete at a 2-MHz bus frequency.

Four result registers are included to further enhance the A/D subsystem along with control longic to control conversion activity automatically. A single write instruction selects one of four conversion sequences, resulting in a conversion complete flag after the first four conversions. The sequences are as follows :

- Convert one channel four times and stop, sequential results placed in the result registers.
- Convert one group of four channels and stop each result register is dedicated to one channel.
- Convert one channel continuously, updating the result registers in a roud-robin fashion.
- Convert one group of four channels (roud-robin fashion) continuously, each result register is dedicated to one channel.

Note : in the 48-pin dual-in-line package, four conversion channels are not implemented. These include channels four through seven.

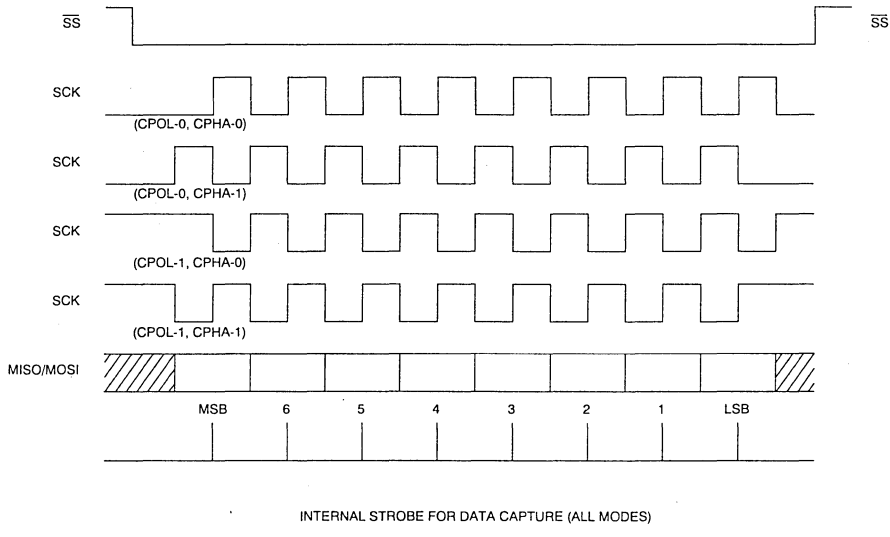


Figure 26 : Data clock timing diagram.

6.15 - Instruction set

The MCU can execute all of the M6800 and M6801 instructions. In addition to these instructions, 91 new opcodes are provided by the paged opcode map. These instructions can be divided into five different types :

- accumulator and memory,
- index register and stack pointer,
- jump, branch, and program control,
- bit manipulation, and
- condiţon code register instructions.

The following paragraphs briefly explain each type.

ACCUMULATOR/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The accumulator/memory instructions can be divided into four subgroups :

- load/store/transfer,
- arithmetic/math,
- logical, and
- shift/rotate.

The following paragraphs describe the different groups of accumulator/memory instructions.

Load/Store/Transfer
Refer to the following table for load/store/transfer instructions.

Function	Mnemonic
Clear memory byte	CLR
Clear accumulator A	CLRA
Clear accumulator B	CLRB
Load accumulator A	LDAA
Load accumulator B	LDAB
Load double accumulator D	LDD
Push A onto stack	PSHA
Push B onto stack	PSHB
Pull A from stack	PULA
Pull B from stack	PULB

Function	Mnemonic
Store accumulator A	STAA
Store accumulator B	STAB
Store accumulator D	STD
Transfer A to B	TAB
Transfer A to CC register	TAP
Transfer B to A	TBA
Transfer CC register to A	TPA
Exchange D with X	XGDX
Exchange D with Y	XGDY

Arithmetic/Math
Refer to the following table for the arithmetic/math instructions.

Function	Mnemonic
Add accumulators	ABA
Add B to X	ABX
Add B to Y	ABY
Add with carry to A	ADCA
Add with carry to B	ADCB
Add memory to A	ADDA
Add memory to B	ADDB
Add 16-bit to D	ADDD
Compare A to B	CBA
Compare A to memory	CMPA
Compare B to memory	CMPB
Compare D to memory (16 bit)	CPD
Decimal adjust A	DAA
Decrement memory byte	DEC
Decrement accumulator A	DECA
Decrement accumulator B	DECB
Fractional divide 16 × 16	FDIV

Function	Mnemonic
Integer divide 16 × 16	IDIV
Increment memory byte	INC
Increment accumulator A	INCA
Increment accumulator B	INCB
Multiply 8 × 8	MUL
2's complement memory byte	NEG
2's complement A	NEGA
2's complement B	NEGB
Subtract B from A	SBA
Subtract with carry from A	SBCA
Subtract with carry from B	SBCB
Subtract memory from A	SUBA
Subtract memory from B	SUBB
Subtract memory from D	SUBD
Test for zero or minus	TST
Test for zero or minus A	SBA
Test for zero or minus B	TSTB

Logical
This group is used to make comparisions, decisions, and extractions of data. Refer to the following list for the logical instructions.

Function	Mnemonic
AND A with memory	ANDA
AND B with memory	ANDB
Bit(s) test A with memory	BITA
Bit(s) test B with memory	BITB
1's complement memory byte	COM
1's complement A	COMA

Function	Mnemonic
1's complement B	COMB
Exclusive OR A with memory	EORA
Exclusive OR B with memory	EORB
OR accumulator A (inclusive)	ORAA
OR accumulator B (inclusive)	ORAB

Shift/Rotate
The shift and rotate instructions automatically operate through the carry bit, which allows easy extension to multiple bytes. Refer to the following list for the shift/rotate instructions.

Function	Mnemonic
Arithmetic shift left	ASL
(Logical shift left)	(LSL)
Arithmetic shift left A	ASLA
(Logical shift left accumulator A)	(LSLA)
Arithmetic shift left B	ASLB
(Logical shift left accumulator B)	(LSLB)
Arithmetic shift left double	ASLD
(Logical shift left double)	(LSLD)
Arithmetic shift right	ASR
Arithmetic shift right A	ASRA
Arithmetic shift right B	ASRB

Function	Mnemonic
Logical shift right	LSR
Logical shift right accumulator A	LSRA
Logical shift right accumulator B	LSRB
Logical shift right double	LSRD
Rotate left	ROL
Rotate left accumulator A	ROLA
Rotate left accumulator B	ROLB
Rotate right	ROR
Rotate right accumulator A	RORA
Rotate right accumulator B	RORB

INDEX-REGISTER AND STACK-POINTER INSTRUCTIONS

These instructions provide a method for storing data and for manipulation of index register, stack pointer, and individual segments of data within the register and stack pointer. Refer to the following list for the index-register and stack-pointer instuctions.

Function	Mnemonic
Add B to X	ABX
Add B to Y	ABY
Compare X to memory (16 bit)	CPX
Compare Y to memory (16 bit)	CPY
Decrement stack pointer	DES
Decrement index register X	DEX
Decrement index register Y	DEY
Increment stack pointer	INS
Increment index register X	INX
Increment index register Y	INY
Load index register X	LDX
Load index register Y	LDY
Load stack pointer	LDS

Function	Mnemonic
Push X onto stack (low first)	PSHX
Push Y onto stack (low first)	PSHY
Pull X from stack (high first)	PULX
Pull Y from stack (high first)	PULY
Store stack pointer	STS
Store index register X	STX
Store index register Y	STY
Transfer stack pointer to X	TSX
Transfer stack pointer to Y	TSY
Transfer X to stack pointer	TXS
Transfer Y to stack pointer	TYS
Exchange D with X	XGDX
Exchange D with Y	XGDY

6

JUMPS/BRANCHES/PROGRAM-CONTROL INSTRUCTIONS

These instructions provide techniques for modifying the normal sequence of the program for conditional and unconditional branching. Refer to the following list for the jump/branch/program-control instructions.

Function	Mnemonic
Branch if carry clear	BCC
(Branch if higher or same)	(BHS)
Branch if carry set	BCS
(Branch if lower)	(BLO)
Branch if = zero	BEQ
Branch if $\geq$ zero	BGE
Branch if > zero	BGT
Branch if higher	BHI
Branch if $\leq$ zero	BLE
Branch if lower or same	BLS
Branch if < zero	BLT
Branch if minus	BMI
Branch if not = zero	BNE
Branch if plus	BPL
Branch always	BRA

Function	Mnemonic
Branch if bit(s) clear	BRCLR
Branch never	BRN
Branch if bit(s) set	BRSET
Branch to subroutine	BSR
Branch if overflow clear	BVC
Branch if overflow set	BVS
Jump	JMP
Jump to subroutine	JSR
No operation	NOP
Return from interrupt	RTI
Return from subroutine	RTS
Stop internal clocks	STOP
Software interrupt	SWI
Test operation (test mode only)	TEST
Wait for interrupt	WAI

BIT-MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit residing in the first 256 bytes of the memory space in direct address mode. The MCU can use any bit in the 64K memory map, and all bit-manipulation instructions can be used with direct or index (x or y) addressing modes. Software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses. The bit-manipulation instructions use an 8-bit mask, which allows simultaneous operations on any combination of bits in a location. Refer to the following list for the bit-manipulation instructions.

Function	Mnemonic
Clear bit(s)	BCRL
Branch if bit(s) clear	BRCRL

Function	Mnemonic
Branch if bit(s) set	BRSET
Set bit(s)	BSET

CONDITION-CODE-REGISTER INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operating during program execution. Refer to the following list for the condition-code-register instructions.

Function	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
Clear overflow flag	CLV
Set carry	SEC

Function	Mnemonic
Set interrupt mask	SEI
Set overflow flag	SEV
Transfer A to CC register	TAP
Transfer CC register to A	TPA

OPCODE MAP SUMMARY

Table 10 is an opcode map for the instructions used on the MCU.

6.16 · Addressing modes

The MCU uses six different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. Some instructions require an additional byte before the opcode to accomodate a multipage opcode map ; this byte is called a prebyte.

The term «effective address» (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored. The following paragraphs describe the different addressing modes.

IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. These are two, three, or four (if prebyte is required) byte instructions.

DIRECT

In the direct addressing mode, the least-significant byte of the operand address is contained in a single byte following the opcode and the most-significant byte of an address is assumed to be $00. Direct addressing allows the user to directly address $0000 through $00FF using two-byte instructions, and execution time is reduced by eliminating the additional memory access. In most applications, this 256-byte area is reserved for frequently referenced data. In the MCU, software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses.

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. These are three or four (if prebyte is required) byte instructions : one or two for the opcode and two for the effective address.

INDEXED

In the indexed addressing mode, one of the index registers (X or Y) is used in calculating the effective address. In this case, the effective address is variable and depends on two factors :

- the current contents of the index register (X or Y) being used, and
- the 8-bit unsigned offset contained in the instruction.

This addressing mode allows referencing any memory location in the 64K byte address space. These are usually two or three (if prebyte is required) byte instructions, the opcode plus the 8-bit offset.

RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instructions. These are usually two-byte instructions.

HI / LOW	INH 0 0000	INH 1 0001	REL 2 0010	INH 3 0011	ACCA 4 0100	ACCB 5 0101	INDX(Y) 6 0110	EXT 7 0111	IMM 8 1000	DIR 9 1001	INDX(Y) A 1010	EXT B 1011	IMM C 1100	DIR D 1101	INDX(Y) E 1110	EXT F 1111	HI / LOW
0 0000	TEST	SBA	BRA	TSX(Y)	NEGA	NEGB	NEG	NEG	SUBA	SUBA	SUBA	SUBA	SUBA	SUBA	SUBA	SUBB	0
1 0001	NOP	CBA	BRN	INS					CMPA	CMPA	CMPA	CMPA	CMPB	CMPB	CMPB	CMPA	1
2 0010	IDIV	BRSET	BHI	PULA					SBCA	SBCA	SBCA	SBCA	SBCB	SBCB	SBCB	SBCB	2
3 0011	FDIV	BRCLR	BLS	PULB	COMA	COMB	COM	COM	★ SUBD	★ SUBD	★ SUBD	★ SUBD	ADDD	ADDD	ADDD	ADDD	3
4 0100	LSRD	BSET	(BHS) BCC	DES	LSRA	LSRB	LSR	LSR	ANDA	ANDA	ANDA	ANDA	ANDB	ANDB	ANDB	ANDB	4
5 0101	(LSLD) ASLD	BCLR	(BLO) BCS	TX(Y)S					BITA	BITA	BITA	BITA	BITB	BITB	BITB	BITB	5
6 0110	TAP	TAB	BNE	PSHA	RORA	RORB	ROR	ROR	LDAA	LDAA	LDAA	LDAA	LDBB	LDBB	LDBB	LDBB	6
7 0111	TPA	TBA	BEQ	PSHB	ASRA	ASRB	ASR	ASR		STAA	STAA	STAA		STBB	STBB	STBB	7
8 1000	INX(Y)	PAGE 2	BVC	PULX(Y)	ASLA	ASLB	ASL	ASL	EORA	EORA	EORA	EORA	EORB	EORB	EORB	EORB	8
9 1001	DEX(Y)	DAA	BVS	RTS	ROLA	ROLB	ROL	ROL	ADCA	ADCA	ADCA	ADCA	ADCB	ADCB	ADCB	ADCB	9
A 1010	CLV	PAGE 3	BPL	ABX(Y)	DECA	DECB	DEC	DEC	DRAA	DRAA	ORAA	ORAA	ORAB	ORAB	ORAB	ORAB	A
B 1011	SEV	ABA	BMI	RTI					ADDA	ADDA	ADDA	ADDA	ADDB	ADDB	ADDB	ADDB	B
C 1100	CLC	BSET	BGE	PSHX(Y)	INCA	INCB	INC	INC	CPX(Y)	CPX(Y)	CPX(Y)	CPX(Y)	LDD	LDD	LDD	LDD	C
D 1101	SEC	BCLR	BLT	MUL	TSTA	TSTB	TST	TST	BSR	JSR	JSR	JSR	PAGE 4	STD	STD	STD	D
E 1110	CLI	BRSET	BGT	WAI			JMP	JMP	LDS	LDS	LDS	LDS	LDX(Y)	LDX(Y)	LDX(Y)	★ LDX(Y)	E
F 1111	SEI	BRCLR	BLE	SWI	CLRA	CLRB	CLR	CLR	XGDX(Y)	STS	STS	STS	STOP	STX(Y)	STX(Y)	★ LDD	F

INH : Inherent REL : Relative IMM : Immediate EXT : Extended DIR : Direct INDX(Y) : Index X(Y).

Mnemonic	Page	Opcode	Bytes	Cycles
CPD	3	83	4	5
	3	93	3	6
	3	B3	4	7
	3	A3	3	7
	4	A3	3	7
CPY	3	AC	3	7
CPX	4	AC	3	7
LDY	3	EE	3	6
LDX	4	EE	3	6
STY	3	EF	3	6
STX	4	EF	3	6

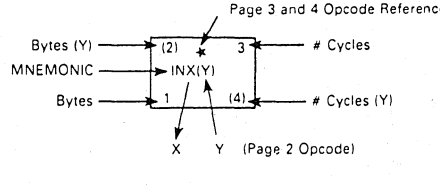


Table 16 - Opcode map

INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructons are one-or two-byte instructions.

PREBYTE

To expand the number of instructions used in the MCU, a prebyte instruction has been added to certain instructions. The instructions affected are usually associated with index register Y. Accessing opcodes from pages 2, 3, or 4 would require a prebyte instruction.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38535 or TCS standards.

7.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

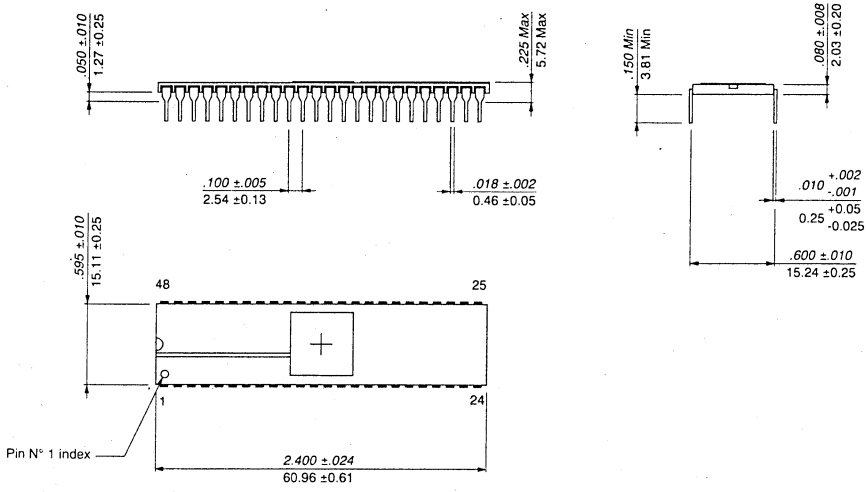
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

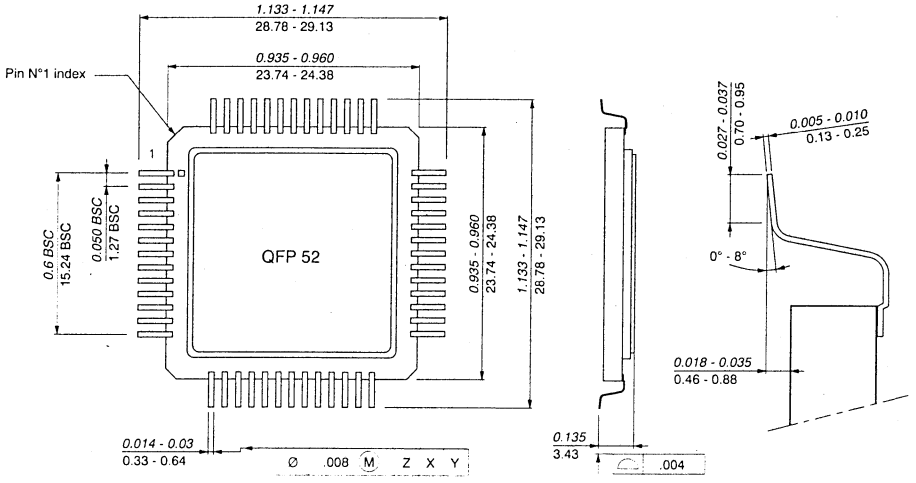
a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if practical.

9 · PACKAGE MECHANICAL DATA

9.1 · 48 pins · Ceramic Dual in Line



9.2 - 52 pins - Ceramic Quad Flat Pack



6

10 · TERMINAL CONNECTIONS

10.1 · 48 pins · Ceramic Dual in Line

See Figure 2 page 4.

10.2 · 52 pins · Ceramic Quad Flat Pack

See Figure 3 page 4.

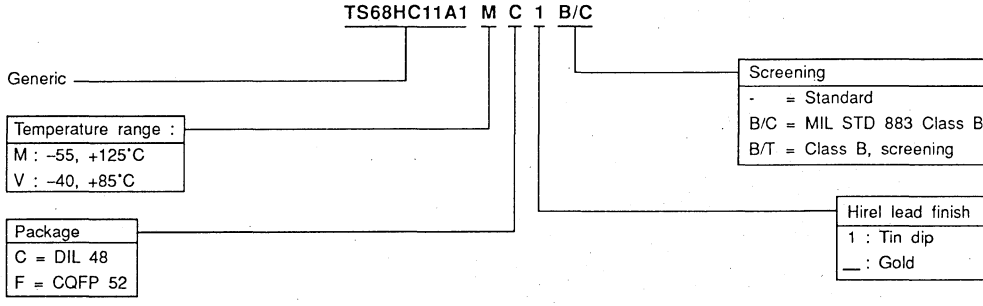
11 · ORDERING INFORMATION

11.1 · Hi-REL product

Commercial TCS part-number (Note 1)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC11A1MCB/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11A1MFB/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11A1MC1B/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11A1MF1B/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11A1DES02XC · Note 2	DESC	DIL 48	−55 / +125	5962-90510
TS68HC11A1DES02XC · Note 2	DESC	CQFP 52	−55 / +125	5962-90510
Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES. **Note 2 :** On request.				

11.2 · Standard product

Commercial TCS part-number (see Note)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC11A1VC	TCS standard	DIL 48	−40 / +85	Internal
TS68HC11A1MC	TCS standard	DIL 48	−55 / +125	Internal
TS68HC11A1VF	TCS standard	CQFP 52	−40 / +85	Internal
TS68HC11A1MF	TCS standard	CQFP 52	−55 / +125	Internal
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.				



TS 68HC811E2

8-BIT MICROCONTROLLER

DESCRIPTION

The TS 68HC811E2 high-density CMOS (HCMOS) microcontroller unit (MCU) contains highly sophisticated on-chip peripheral capabilities. This high-speed and low-power MCU has a multiplexed bus, a nominal bus speed of two megahertz, and the fully static design allows operations at frequencies down to dc. This publication contains condensed information on the MCU.

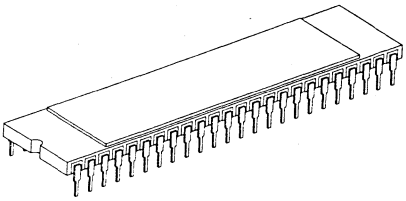
MAIN FEATURES

- 16-bit timer system with four-stage programmable prescaler :
  - 4 output compare channels,
  - 3 input compare channels,
  - 1 input capture or output capture (software selectable).
- Power saving STOP and WAIT modes.
- Synchronous Serial Peripheral Interface (SPI).
- Asynchronous NRZ serial communications interface (SCI).
- 8-bit pulse accumulator circuit.
- Bit test and branch instructions.
- Real time interrupt circuit.
- Computer Operating System (COP) watchdog system.
- TS 68HC11 CPU.
- 2K bytes of on-chip EEPROM with block protect for extra security.
- 256 bytes of on-chip static RAM, all saved during standby.
- Eight-channel 8-bit A/D converter (for CQFP only).
- 38 general purpose I/O pins :
  - 16 bidirectional input/output (I/O) pins,
  - 11 input only pins,
  - 11 output only pins.
- Power supply : 5.0 V_{DC} ± 10 %.
- Military temperature range : − 55 to + 125°C (T_C).

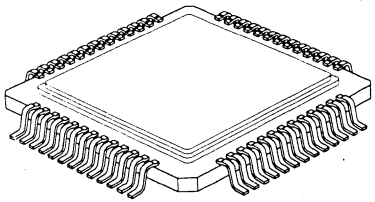
SCREENING / QUALITY

This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- DESC 5962-89527.
- or according to TCS standards.



C Suffix
DIL 48
Ceramic side brazed dual in line



F Suffix
CQFP 52
Ceramic quad flat pack

See the ordering information page 54.

Pin connection : see pages 3 and 32.

SUMMARY

A · GENERAL DESCRIPTION

1 · INTRODUCTION

Figure 1 is a block diagram of the TS 68HC811E2.

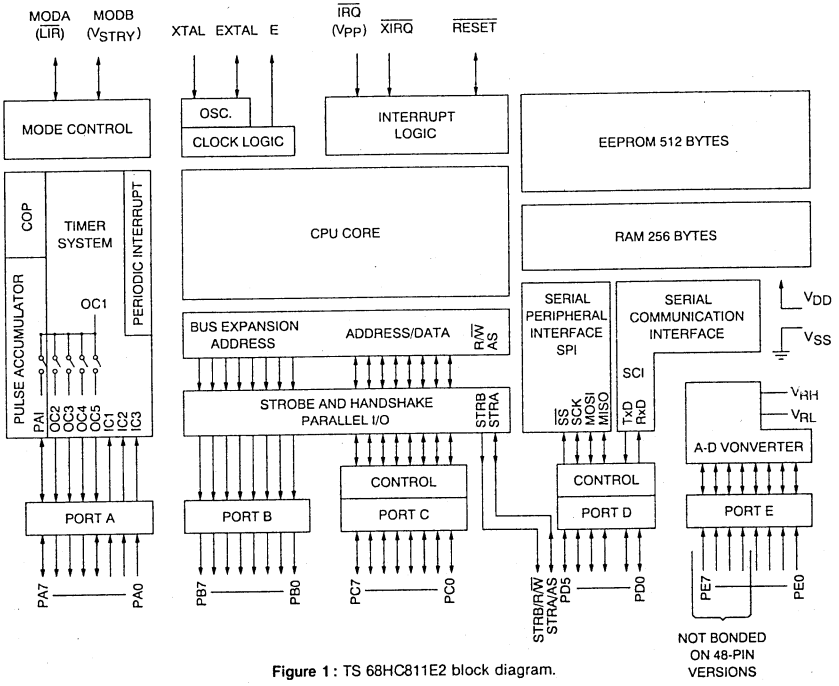


Figure 1 : TS 68HC811E2 block diagram.

2 · SIGNAL DESCRIPTION

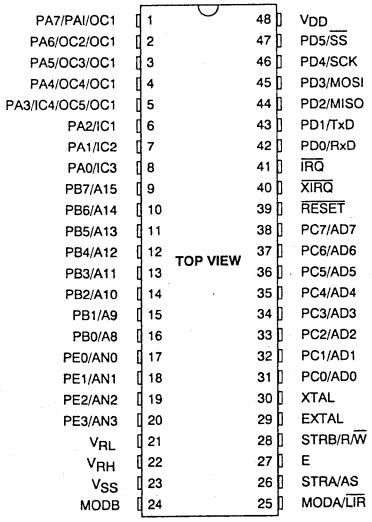


Figure 2.1 : Dil 48 terminal designation.

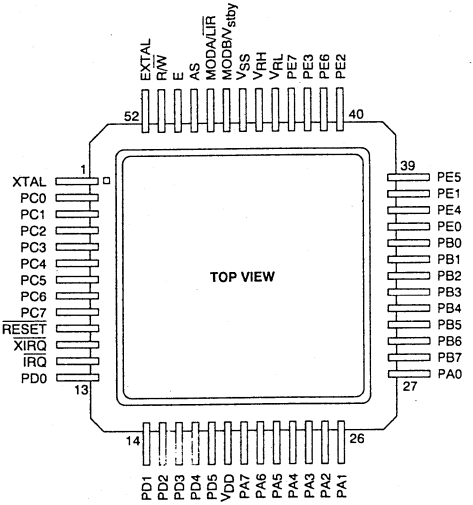


Figure 2.2 : CQFP terminal designation.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microcontroller TS 68HC811E2, in compliance with MIL-STD-883 class B or TCS standards.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535 : general specifications for microcircuits.
3) DESC Drawing 5962-89527.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 (when defined) :

- DIL 48,
- 52 ceramic quad flat pack CQFP.

The precise case outlines are described in § 9.1 and 9.2.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (see Table 1)

Table 1

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+7.0	V
P_{dmax}	Max power dissipation			150	mW
T_{case}	Operating temperature	TS 68HC811E2 CM	-55	+125	°C
		TS 68HC811E2 CV	-40	+85	°C
T_{stg}	Storage temperature		-55	+150	°C
T_j	Junction temperature			+160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.3.2 · Recommended condition of use

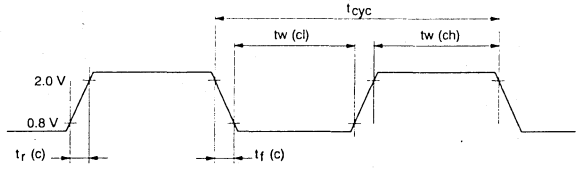
Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 2

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	4.50	5.50	V
V_{IL}	Low level input voltage	V_{SS}	$0.2 \times V_{DD}$	V
V_{IH}	High level input voltage	$0.8 \times V_{DD}$	V_{DD}	V
T_{case}	Operating temperature TS 68HC811E2CM TS 68HC811E2CV	−55 −40	+125 +85	°C °C
V_{OH}	Maximum high level output voltage	V_{DD} −0.1	V_{DD}	V
V_{OL}	Maximum low level output voltage	V_{SS}	0.4	V
f_C	Clock frequency (crystal frequency)		8.4	MHz

This device contains protective circuitry to protect the input against damage due to high static voltages or electrical fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltage to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Load network specified in § 5.4.1.



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise of fall will be linear between 0.8 volt and 2.0 volts.

Figure 3 : Clock input timing diagram.

3.4 · Thermal characteristics (at 25°C)

Table 3

Package	Symbol	Parameter	Value	Unit
DIL 48	θ JA	Thermal resistance - Ceramic junction to Ambient	38	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/
CQFP 52	θ JA	Thermal resistance - Ceramic junction to Ambient	31	°C/W
	θ JC	Thermal resistance - Ceramic junction to Case	5	°C/W

Power considerations.

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 - Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or TCS standards.

3.6 - Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum.

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

– DESC see § 4.1.

Table 4 : Static electrical characteristics for all electrical variants. See § 5.2.

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 5)

For static characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 4).

For dynamic characteristics (Tables 5 to 10), test methods refer to IEC 748-2 method number, where existing.

5.2 - Static characteristics

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_C = −55 / + 125° C or −40 / + 85° C.

Table 4 - DC electrical characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; A = T_L to T_H (unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
V_{OH}	Output high voltage I_{Load} = −0.8 mA, V_{DD} = 4.5 V (Note 1)	All outputs except $\overline{RESET}$ XTAL, and MODA	V_{DD} − 0.8		V
V_{OL}	Output low voltage I_{Load} = 1.6 mA	All outputs except XTAL		0.4	V
V_{IH}	Input high voltage	All inputs except $\overline{RESET}$ $\overline{RESET}$	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} V_{DD}	V V
V_{IL}	Input low voltage	All inputs	V_{SS}	0.2 x V_{DD}	V
I_{OZ}	I/O ports, three-state leakage V_{in} = V_{IH} or V_{IL}	PA3/PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		±10	µA
I_{in}	Input current (Note 2) V_{in} = V_{DD} or V_{SS} V_{in} = V_{DD} or V_{SS}	PA0-PA2, $\overline{IRQ}$, $\overline{XIRQ}$ MODB/V_{STBY}		±1 ±10	µA µA
V_{SB}	RAM standby voltage powerdown		4.0	V_{DD}	V
I_{SB}	RAM standby current powerdown			20	µA
	Total supply current (Note 3)				
I_{DD}	RUN : Single chip Expanded multiplexed			20 30	mA mA
W_{IDD}	WAIT : All peripheral functions shut down Single-chip mode Expanded multiplexed mode			10 15	mA mA
S_{IDD}	STOP : No clocks, single-chip mode			300	µA
C_{in}	Input capacitance	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, $\overline{EXTAL}$ PA3, PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$		8 14	pF pF
P_D	Power dissipation	Single-chip mode Expanded-multiplexed mode		110 165	mW mW

Note 1 : V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.

Note 2 : See A/D specification for leakage current for port E.

Note 3 : All ports configured as inputs, $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{DD} - 0.2$ V, no dc loads, EXTAL is driven with a square wave, and t_{cyc} = 476.5 ns.

5.3 - Dynamic (switching) characteristics

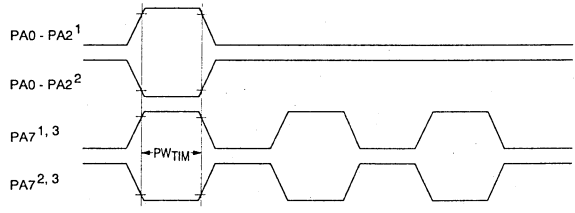
The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V (See also notes 1 and 2).

Table 5 - Control timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$

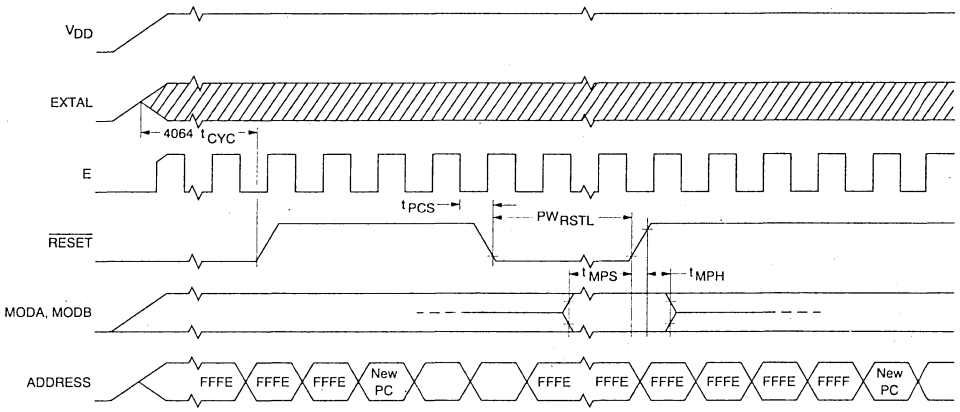
Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_O	Frequency of operation	dc	1.0	dc	2.0	dc	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
f_{XTAL}	Crystal frequency		4.0		8.0		8.4	MHz
4 f_O	External oscillator frequency	dc	4.0	dc	8.0	dc	8.4	MHz
t_{PCS}	Processor control setup Time (see Figures 5, 7 and 8) t_{PCS} = 1/4 t_{cyc} – 50 ns	200		75		69		ns
PW_{RSTL}	Reset input pulse width (Note 1 and Figure 5) (To guarantee external reset vector) (Minimum input time ; may be preempted by internal reset)	8 1		8 1		8 1		t_{cyc}
t_{MPS}	Mode programming setup time (see Figure 5)	2		2		2		t_{cyc}
t_{MPH}	Mode programming hold time (see Figure 5)	0		0		0		ns
PW_{IRQ}	Interrupt pulse width $\overline{IRQ}$ edge sentive mode (see Figures 6 and 8) PW_{IRQ} = t_{cyc} 20 ns	2		2		2		ns
t_{WRS}	Wait recovery startup time (see Figure 7)		4		4		4	t_{cyc}
PW_{TIM}	Timer pulse width Input capture, pulse accumulator input (see Figure 4) PW_{TIM} = t_{cyc} + 20 ns	1020		520		496		ns

Note : $\overline{RESET}$ will be recognized during the first clock it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. See RESET, INTERRUPT, AND LOW-POWER MODES for details.



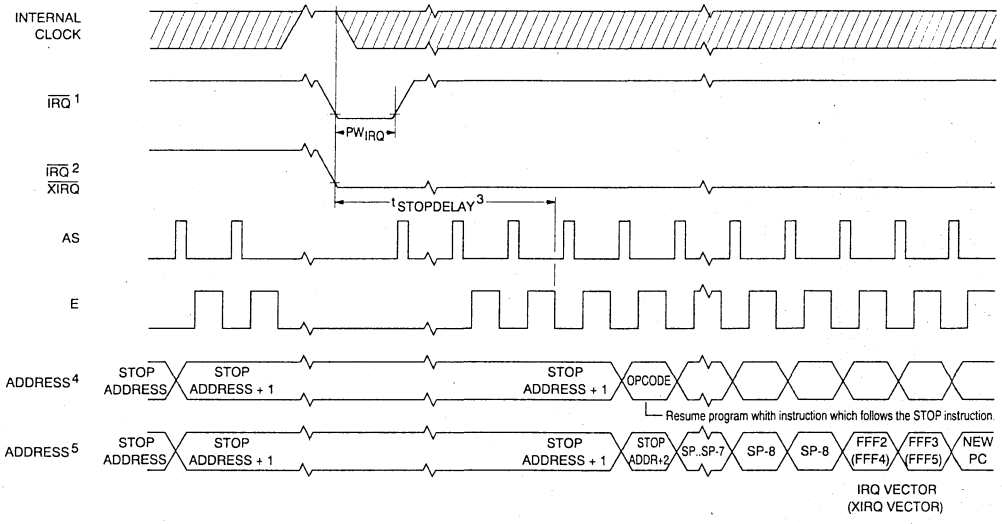
Note 1 : Rising sensitive input.
Note 2 : Falling edge sensitive input.
Note 3 : Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 4 : Timer inputs timing diagram.



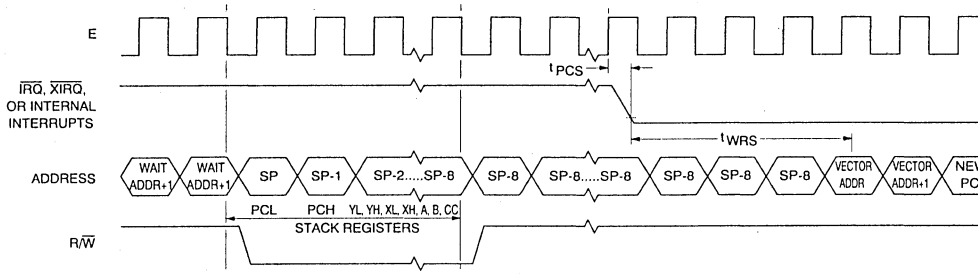
Note : Refer to table 5 for pin states during $\overline{RESET}$

Figure 5 : POR external reset timing diagram.



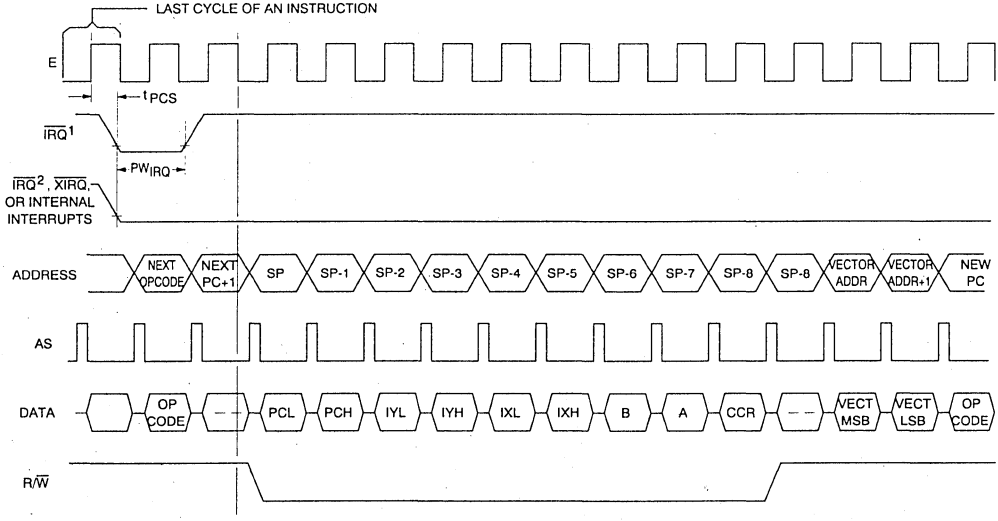
Note 1 : Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
Note 2 : Level sensitive $\overline{IRQ}$ pin (IRQ bit = 0).
Note 3 : $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0.
Note 4 : $\overline{XIRQ}$ with X bit in CCR = 1.
Note 5 : $\overline{IRQ}$ or ($\overline{XIRQ}$ with X bit in CCR = 0).

Figure 6 : Stop recovery timing diagram.



Note 1 : Refer to table 5 for pin states during WAIT.
Note 2 : RESET will also cause recovery from WAIT.

Figure 7 : WAIT recovery from interrupt timing diagram.



Note 1 : Edge sensitive IRQ pin (IRQ bit = 1).
Note 2 : Level sensitive IRQ pin (IRQE bit = 0).

Figure 8 : Interrupt timing diagram.

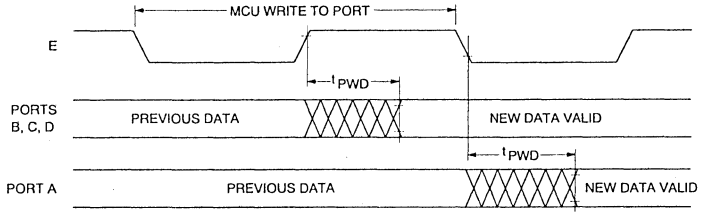
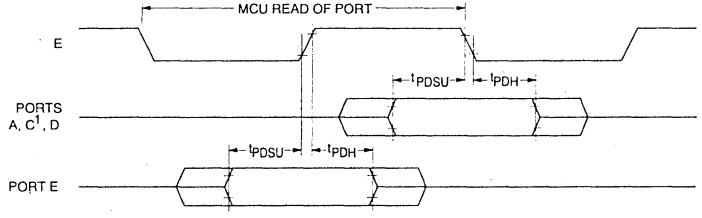


Figure 9 : Port write timing diagram.



Note : For non-latched operation of Port C.

Figure 10 : Port read timing diagram.

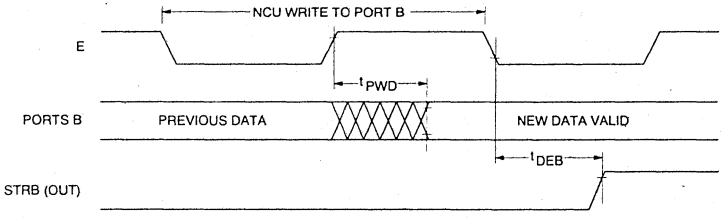


Figure 11 : Simple output strobe timing diagram.

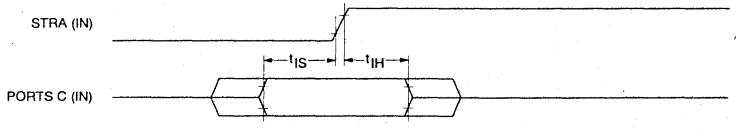
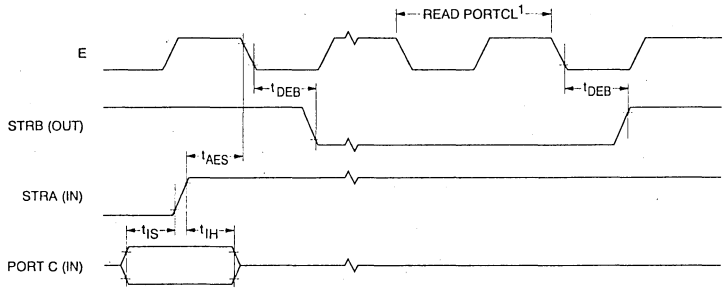
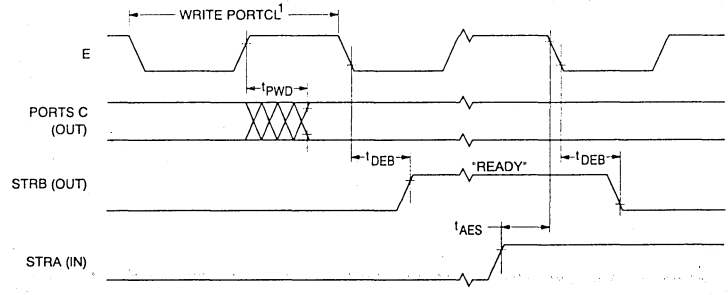


Figure 12 : Simple intput strobe timing diagram.



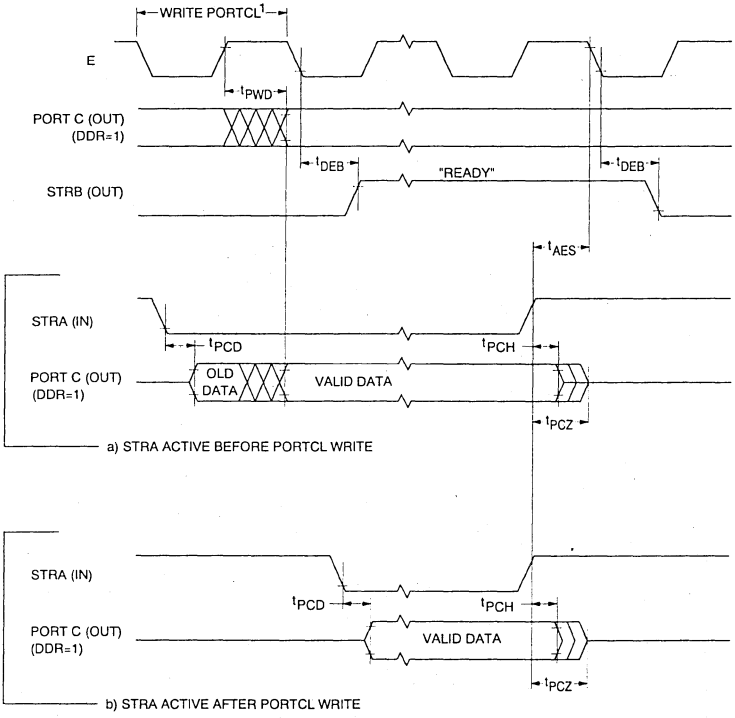
Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 13 : Port C input handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 14 : Port C output handshake timing diagram.



Note 1 : After reading PIOC with STAF set.
Note 2 : Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1).

Figure 15 : Three-state variation of output handshake timing diagram (STRA enables output buffer).

6

Table 6 - Peripheral port timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C +85°C$ or $-55 \leqslant T_C \leqslant +125°C$

Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f_O	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
t_{cyc}	E clock period	1000		500		476		ns
t_{PDSU}	Peripheral data setup time (MCU read of ports A, C, D and E) (see Figure 10)	100		100		100		ns
t_{PDH}	Peripheral data hold time (MCU read of ports A, C, D and E) (see Figure 10)	50		50		50		ns
t_{PWD}	Delay time, peripheral data write (See Figures 9, 11, 13 and 14) MCU write to port A MCU writes to ports, B, C and D t_{PWD} = 1/4 t_{cyc} + 90 ns		 175 340		 175 215		 175 209	 ns ns
t_{IS}	Input data setup time (port C) (see Figures 12 and 13)	60		60		60		ns
t_{IH}	Input data hold time (port C) (see Figures 12 and 13)	100		100		100		ns
t_{DEB}	Delay time, E fall to STRB t_{DEB} = 1/4 t_{cyc} + 130 ns (see Figures 11, 13, 14 and 15)		380		255		249	ns
t_{AES}	Setup time, STRA asserted to E fall (see Note) (see Figures 13, 14 and 15)	0		0		0		ns
t_{PCD}	Delay time, STRA asserted to port C data output valid (see Figure 15)		100		100		100	ns
t_{PCH}	Hold time, STRA negated to port C data (see Figure 15)	10		10		10		ns
t_{PCZ}	Three-state hold time (see Figure 15)		150		150		150	ns

Note : If this setup time is met, STRB will acknoweldge in the next cycle. If it is not met, the respons may be delayed one more cycle.

Table 7 - A/D converter characteristics

V_{DD} = 5.0 Vdc ± 10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C + 85°C$ or $-55 \leqslant T_C \leqslant +125°C$; 750 kHz ⩽ E ⩽ 2.1 MHz (unless otherwise noted)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8		Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics		± 1/2	LSB
Zero error	Difference between the output of an ideal and an actual A/D for zero input voltage		± 1/2	LSB
Full-scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage		± 1/2	LSB
Total unadjusted error	Maximum sum of non-linearity, zero, error, and full-state error (Note 1)		± 1/2	LSB
Quantization error	Uncertainty due to converter resolution		± 1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error source included		± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage (Note 2)	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage (Note 2)	V_{SS} − 0.1	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL} (Note 2)	3		V
Conversion time	Total time to perform a single analog-to-digital conversion : a. E clock b. Internal RC oscillator		32 t_{cyc} + 40	t_{cyc} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Guaranteed		
Zero-input reading	Conversion result when $V_{in} = V_{RL}$	00		Hex
Full-scale reading	Conversion result when $V_{in} = V_{RH}$		FF	Hex
Sample acquisition time	Analog input acquisition sampling time : a. E clock b. Internal RC oscillator	12	 12	t_{cyc} µs
Input leakage	Input leakage on A/D pins PE0-PE7 V_{RL}, V_{RH}		400 1.0	nA µA

Note 1 : Source impedances greater than 10 kΩ will adversaly affect accuracy due mainly to input leakage.
Note 2 : Performance verified down to 2.5 V ΔV_R, but accuracy is tested and guaranteed at ΔV_R = 5 V ± 10 %.

6

Table 8 - Expansion bus timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	f_O	Frequency of operation (E clock frequency)	1.0	1.0	2.0	2.0	2.1	2.1	MHz
1	t_{cyc}	Cycle time	1000		500		476		ns
2	PW_{EL}	Pulse width, E low $PW_{EL} = 1/2\ t_{cyc} - 23$ ns	477		227		215		ns
3	PW_{EH}	Pulse width, E high $PW_{EH} = 1/2\ t_{cyc} - 28$ ns	472		222		210		ns
4	t_r, t_f	E and AS rise and fall time		20		20		20	ns
9	t_{AH}	Address hold time $t_{AH} = 1/8\ t_{yc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
12	t_{AV}	Non-muxed address valid time to E rise $t_{AV} = PW_{EL} - (t_{ASD} + 80$ ns) (Note 1b)	281.5		94		85		ns
17	t_{DSR}	Read data setup time	30		30		30		ns
18	t_{DHR}	Read data hold time (maxe = t_{MAD})	10	145.5	10	83	10	80	ns
19	t_{DDW}	Write data delay time $t_{DDW} = 1/8\ t_{cyc} + 65.5$ ns (Note 1a)		190.5		128		125	ns
21	t_{DHW}	Write data hold time $t_{DHW} = 1/8\ t_{cyc} - 29.5$ ns (Note 1a)	95.5		33		30		ns
22	t_{AVM}	Muxed address valid time to E rise $t_{AVM} = PW_{EL} - (t_{ASD} + 90$ ns) (Note 1b)	271.5		84		75		ns
24	t_{ASL}	Muxed address valid time to AS fall $t_{ASL} = PW_{ASH} - 90$ ns	151		26		20		ns
25	t_{AHL}	Muxed address hold time $t_{AHL} = 1/8\ t_{cyc} - 29.5$ ns (Note 1b)	95.5		33		30		ns
26	t_{ASD}	Delay time, E to AS rise $t_{ASD} = 1/8\ t_{cyc} - 9.5$ ns (Note 1a)	115.5		53		50		ns
27	PW_{ASH}	Pulse width, AS high $PW_{ASH} = 1/4\ t_{cyc} - 29$ ns	221		96		90		ns
28	t_{ASED}	Delay time, AS to E rise $t_{ASED} = 1/8\ t_{cyc} - 9.5$ ns (Note 1b)	115.5		53		50		ns
29	t_{ACCA}	MPU address access time $t_{ACCA} = t_{AVM} + t_r + PW_{EH} - t_{DSR}$ (Note 1b)	733.5		296		275		ns
35	t_{ACCE}	MPU access time $t_{ACCE} = PW_{EH} - t_{DSR}$		442		192		180	ns

Table 8 - Expansion bus timing (Continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 16

Num.	Symbol	Characteristic	1.0 MHz		2.0 MHz		2.1 MHz		Unit
			Min	Max	Min	Max	Min	Max	
36	t_{MAD}	Muxed address delay (previous cycle MPU read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1a)	145.5		83		80		ns

Note 1 : Input clocks with duty cycles other than 50 % will affect bus performance. Timing parameters affected by input clock duty cycle are identified by a and b. To recalculate the approximate bus timing values, substitute the following expression in place of 1/8 t_{cyc} in the above formulas where applicable :
a. (1 – DC) × 1/4 t_{cyc} for : (t_{DDW}, t_{DHW}, t_{MAD})
b. DC × 1/4 t_{cyc} for : (t_{AVM}, t_{AHL}, t_{ASED}, t_{ACCA})
where : DC is the decimal value of duty cycle percentage (high time).

Table 9 - Serial peripheral interface (SPI) timing

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 17

Num.	Symbol	Characteristic	Min	Max	Unit
		Operating frequency			
	$f_{op}(m)$	Master	dc	0.5	f_{op}
	$f_{op}(s)$	Slave	dc	2.1	MHz
1		Cycle time			
	$t_{cyc}(m)$	Master	2.0		t_{cyc}
	$t_{cyc}(s)$	Slave	480		ns
2		Enable lead time			
	$t_{lead}(m)$	Master	Note 1		ns
	$t_{lead}(s)$	Slave	240		ns
3		Enable lag time			
	$t_{lag}(m)$	Master	Note 1		ns
	$t_{lag}(s)$	Slave	240		ns
4		Clock (SCK) high time			
	$t_{w(SCKH)m}$	Master	340		ns
	$t_{w(SCKH)s}$	Slave	190		ns
5		Clock (SCK) low time			
	$t_{w(SCKL)m}$	Master	340		ns
	$t_{w(SCKL)s}$	Slave	190		ns
6		Data setup time (inputs)			
	$t_{su}(m)$	Master	100		ns
	$t_{su}(s)$	Slave	100		ns
7		Data hold time (inputs)			
	$t_h(m)$	Master	100		ns
	$t_h(s)$	Slave	100		ns
8		Access time (time to data active from high-impedance state)			
	t_a	Slave	0	120	ns
9		Disable time (hold time to high-impedance state)			
	t_{dis}	Slave		240	ns
10	tv(s)	Data valid (after enable edge) Note 2		240	ns
11	tho	Data hold time (outputs) (after enable edge)	0		ns
12		Rise time (20 % V_{DD} to 70 % V_{DD}, C_L = 200 pF)			
	t_{rm}	SPI outputs (SCK, MOSI, and MISO)		100	ns
	trs	SPI inputs (SCK, MISO, MOSI, and SS)		2.0	µs

6

Table 9 - Serial peripheral interface (SPI) timing (Continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; $-40 \leqslant T_C \leqslant +85°C$ or $-55 \leqslant T_C \leqslant +125°C$ - See Figure 17

Num.	Symbol	Characteristic	Min	Max	Unit
13		Fall time (70 % V_{DD} to 20 % V_{DD}, C_L = 200 pF)			
	t_{fm}	SPI outputs (SCK, MOSI, and MISO)		100	ns
	tfs	SPI inputs (SCK, MISO, MOSI, and SS)		2.0	µs

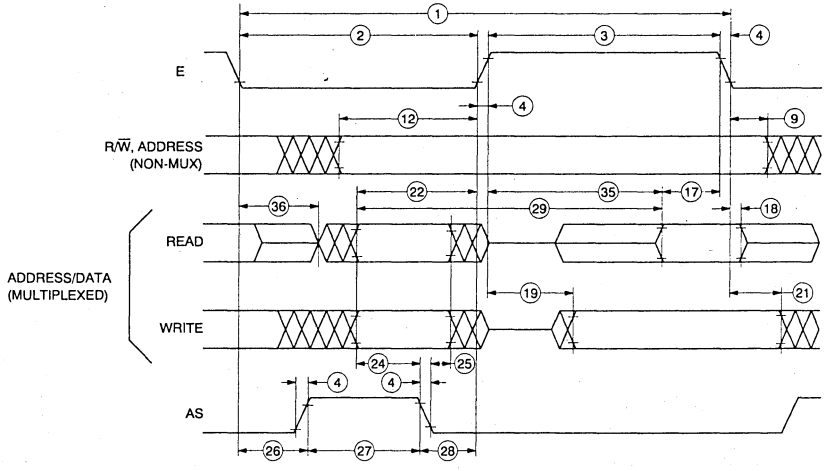
Note 1 : Signal production depends on software.
Note 2 : Assumes 200 pF load on all SPI pins.

Table 10 - EEPROM characteristics

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = 25°C

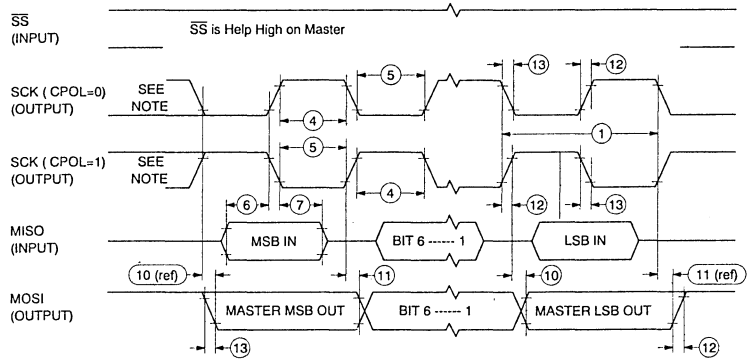
Characteristics		Min	Max	Unit
Programming time (Note 1)	Under 1.0 MHz with RC oscillator enabled		25	ms
	1.0 to 2.0 MHz with RC oscillator disabled		must use RC	ms
	2.0 MHz (or anytime RC oscillator enabled)		25	ms
Erase time (Note 1)	Byte, row, and bulk		10	ms
Write/erase endurance (Note 2)			5.000	cycles
Data retention (Note 2)			10	years

Note 1 : The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.
Note 2 : See current quarterly reliability monitor report for current failure rate information.



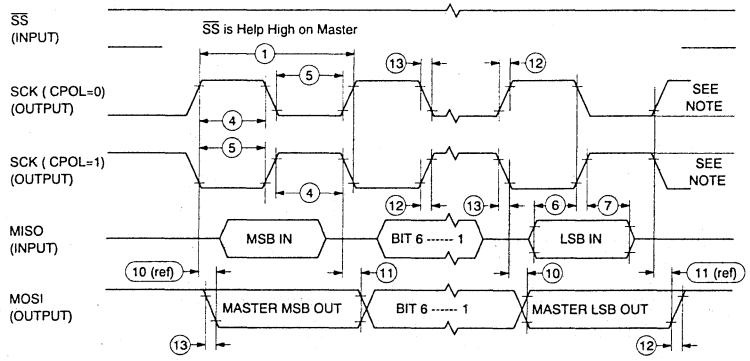
Note : Measurement points shown are 20 % and 70 % V_{DD}.

Figure 16 : Expansion bus timing diagram.



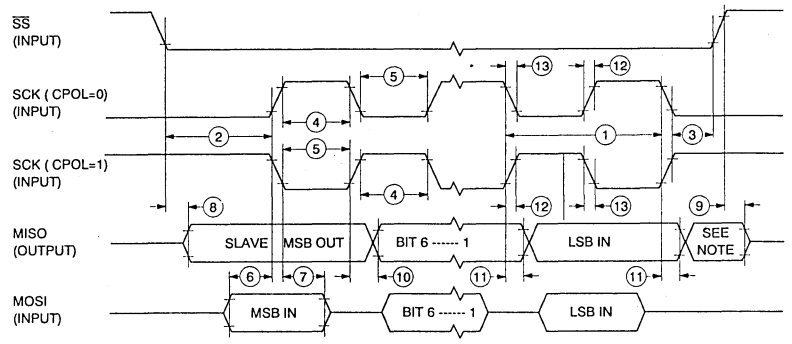
Note : This last clock edge is generated internnally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17a : SPI timing diagrams
SPI master timing (CPHA = 0).



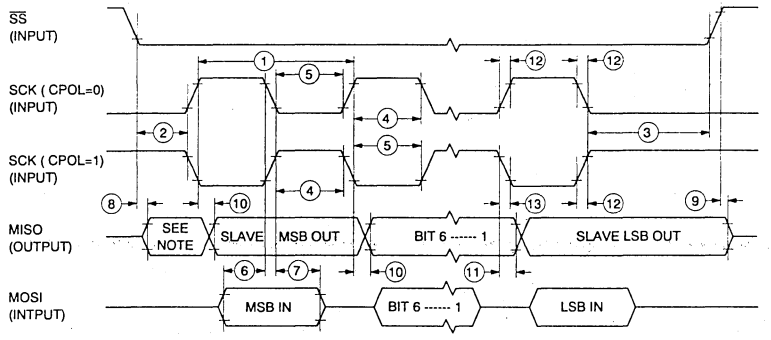
Note : This last clock edge is generated internnally but is not seen at the SCK pin.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17b : SPI timing diagrams
SPI master timing (CPHA = 1).



Note : Not defined but normally LSB of character previously transmitted.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17c : SPI timing diagrams
SPI slave timing (CPHA = 0).



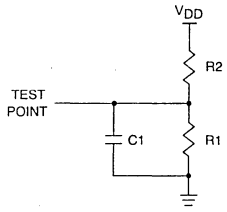
Note : Not defined but normally LSB of character previously transmitted.
All timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} unless otherwise noted.

Figure 17d : SPI timing diagrams
SPI slave timing (CPHA = 1).

5.4 · Test conditions specific to the device

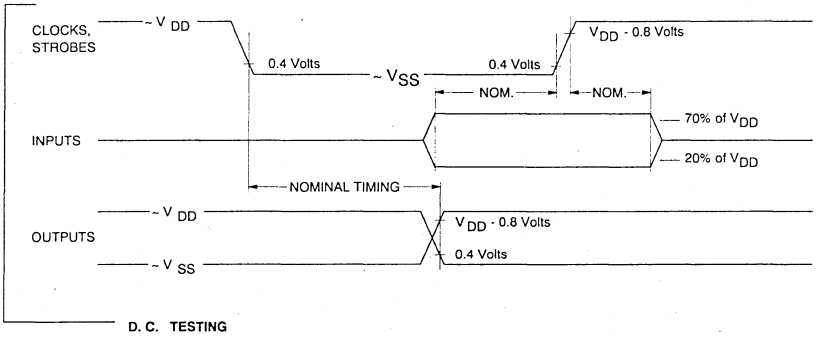
5.4.1 · Loading network

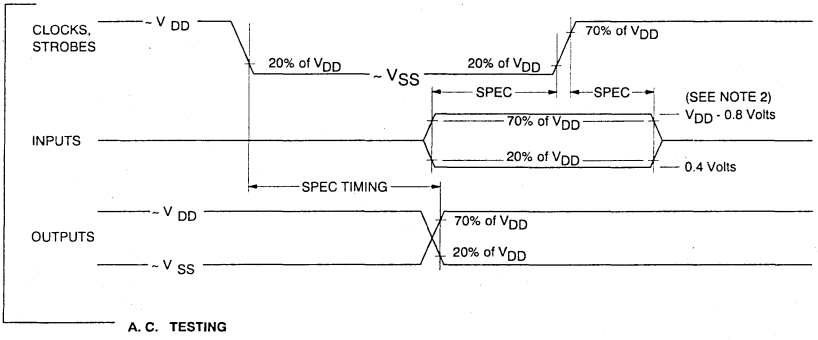
The applicable loading network of Tables 5, 6, 8, 9, refer to the loading network number as shown in Figure 18 below.



Equivalent test load (Note 1)

Pins	R1	R2	C1
PA3-PA7 PB0-PB7 PC0-PC7 PD0-PD5 E, AS, R/$\overline{W}$	3.26 K	2.38 K	30 pF
PD1-PD4	3.26 K	2.38 K	200 pF





Note 1 : Full test loads are applied during all ac electrical test and ac timing measurements.

Note 2 : During ac timing measurements, inputs are driven to 0.4 volts and V_{DD} −0.8 volts while timing measurements are taken at the 20 % and 70 % of V_{DD} points.

Figure 18 : Test methods.

5.4.2 · Time definitions

The times specified in Tables 5, 6, 8, 9 as dynamic characteristics are defined in Figure 18 above.

6 · FUNCTIONAL DESCRIPTION

6.1 · Operating modes

The MCU uses two dedicated pins (MODA and MODB) to select one of two basic operating modes or one of two special operating modes. The basic operating modes are single-chip and expanded-multiplexed ; the special operating modes are bootstrap and special test. The following paragraphs describe the different modes.

SINGLE-CHIP MODE (MODE0)

In this mode, the MCU functions as a self-contained microcontroller and has no external address or data bus. This mode provides maximum use of the pins for on-chip peripheral functions, and all address and data activity occur within the MCU.

EXPANDED MULTIPLEXED MODE (MODE 1)

In this mode, the MCU can address up to 64 K bytes of address space. Higher-order address bits are output on the port B pins, and lower-order address bits and the data bus are multipliexed on the port C pins. The AS pin provides the control output used in demultiplexing the loworder address at port C. The R/$\overline{W}$ pin is used to control the direction of data transfer on port C bus.

BOOTSTRAP MODE

In this mode, all vectors are fetched from the 192-byte on-chip bootloader ROM. This mode is very versatile and can be used for such functions as test and diagnostics on completed modules and for programming the EEPROM. The serial receive logic is initialized by software in the bootloader ROM, which provides program control for the serial communications interface (SCI) baud and word format. In this mode, a special control bit is configured that allows for self-testing of the MCU. This mode can be changed to other modes under program control.

TEST MODE

This modes is primarily intended for main production at time of manufacture ; however, it may be used to program calibration or personality data into the internal EEPROM. In this mode, a special control bit is configured to permit access to a number of special test control bits. This mode can be changed to other modes under program control.

6.2 · Signal description

V_{DD} AND V_{SS}

Power is supplied to the microcontroller using these two pins. V_{DD} is +5 volts (± 0.5 V) power, and V_{SS} is ground.

$\overline{\text{RESET}}$

This active low bidirectional control pin is used as an input to initialize the MCU to a known startup state and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or the computer operating properly (COP) circuit.

XTAL, EXTAL

These pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied shall be four times higher than the desired clock rate. Refer to Figure 19 for crystal and clock connections.

E

This pin provides an output for the internally generated E clock, which can be used for timing reference. The frequency of the E output is one-fourth that of the input frequency at the XTAL and EXTAL pins.

$\overline{\text{IRQ}}$

This pin provides the capability for asynchronously applying interrupts to the MCU. Either negative edge-sensitive or level-sensitive triggering is program selectable. This pin is configured to level-sensitive during reset. An external resistor connected to V_{DD} is required on $\overline{\text{IRQ}}$.

$\overline{\text{XIRQ}}$

This pin provides the capability for asynchronously applying non-maskable interrupts to the MCU after a power on reset (POR). During reset, the X bit in the condition code register is set, and anay interrupt is masked until enabled by software. This input is level-sensitive and requires an external pullup resistor to V_{DD}.

MODA/$\overline{\text{LIR}}$ AND MODB/V_{stby}

During reset, these pins are used to control the two basic operating modes and the two special operating modes. The $\overline{\text{LIR}}$ output can be used as an aid in debugging once reset is completed. The open-drain $\overline{\text{LIR}}$ pin goes to an active low during the first E-clock cycle of each instruction and remains low for the duration of that cycle. The mode selections are shown below.

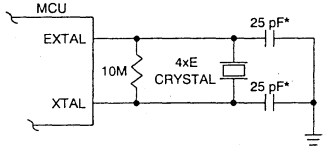
MODB	MODA	Mode selected
1	0	Single chip
1	1	Expanded multiplexed
0	0	Special bootstrap
0	1	Special test

V_{RL} AND V_{RH}

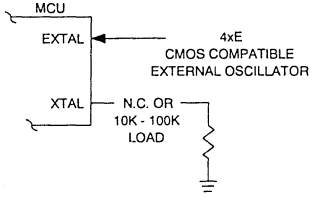
These pins provide the reference voltage for the A/D converter.

R/$\overline{W}$/STRB

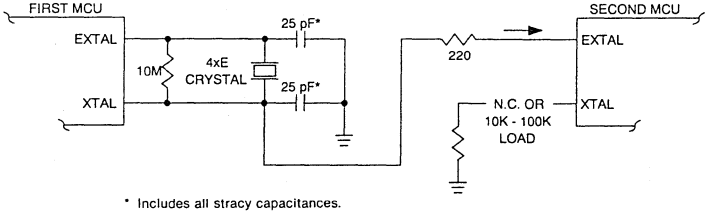
This pin provides two different functions, depending on the operating mode. In single-chip mode, the pin provides STRB (output strobe) function ; in the expanded multiplexed mode, it provides R/$\overline{W}$ (read-write) function. The R/$\overline{W}$ is used to control the direction of transfers on the external data bus.



Common Crystal Connections



External Oscillator Connections



* Includes all stracy capacitances.

One Crystal Driving Two MCUs

Figure 19 : Oscillator connections.

AS/STRA

This pin provides two different functions depending on the operating mode. In single-chip mode, the pin provides STRA (input strobe) function, and in the expanded-multiplexed mode, it provides AS (address strobe) function. The AS may be used to demultiplex the address and data signals at port C.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PE0-PE7)

These I/O lines are arranged into four 8-bit ports (A, B, C, and E) and one 6-bit port (D). All ports serve more than one purpose depending on the operating mode. Table 11 lists a summary of the pin functions to operating modes. Refer to INPUT/OUTPUT PORTS for additionnal information.

6.3 - Input/output ports

Port functions are controlled by the particular mode selected. In the single-chip mode and bootstrap mode, four ports are configured as parallel I/O data ports and port E can be used for general-purpose static inputs and/or analog-to-digital converter channel inputs. In the expanded-multiplexed mode and test mode, ports B, C, AS, and R/$\overline{W}$ are configured as a memory expansion bus. Table 11 lists the different port signals available. The following paragraphs describe each port.

PORT A

In all operating modes, port A may be configured for three input capture funcitons ; four output compare functions ; and pulse accumulator input (PAI) or a fifth output compare function. Each input capture pin provides for a transitional input, which is used to latch a timer value into the 16-bit input capture register. External devices provide the transitional input, and internal decoders determine which input transition edge is sensed. The output compare pins provide an output whenever a match is made between the value in the free-running counter (in the timer system) and a value loaded into the particular 16-bit output compare register. When port A bit 7 is configured as a PAI, the external input pulses are applied to the pulse accumulator system. The remaining port A lines may be used as general-purpose input or output lines.

PORT B

In the single-chip mode, all port B pins are general purpose output pins. Port B may also be used in a simple strobed output mode where the STRB pulses each time port B is written. In the expanded-multiplexed mode, all of the port B pins act as high-order (bits 8-15) address output pins.

Table 11 · Port signal functions

Port-bit	Single-chip and bootstrap mode	Expanded multiplexed and special test mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA0/IC2
A-2	PA2/IC1	PA0/IC1
A-3	PA3/OC5/ and-or OC1	PA3/OC5/ and-or OC1
A-4	PA4/OC4/ and-or OC1	PA4/OC4/ and-or OC1
A-5	PA5/OC3/ and-or OC1	PA5/OC3/ and-or OC1
A-6	PA6/OC2/ and-or OC1	PA6/OC2/ and-or OC1
A-7	PA7/PAI/ and-or OC1	PA7/PAI/ and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/R x D	PDO/R x D
D-1	PD1/T x D	PD1/T x D
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/SS	PD5/SS
	STRA	AS
	STRB	R/W
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4 (see Note)	PE4/AN4 (see Note)
E-5	PE5/AN5 (see Note)	PE5/AN5 (see Note)
E-6	PE6/AN6 (see Note)	PE6/AN6 (see Note)
E-7	PE7/AN7 (see Note)	PE7/AN7 (see Note)

Note : Not bonded in 48-pin versions.

PORT C

In the single-chip mode, port C pins are general-purpose input/output pins. Port C inputs can be latched by the STRA or may be used in full handshake modes of parallel I/O where the STRA input and STRB output acts as handshake control lines. In the expanded-multiplexed mode, port C pins are configured as multiplexed address/data pins. During the address cycle, bits 0 through 7 of the address are output on PC0-PC7 ; during the data cycle, bits 0 through 7 (PC0-PC7) are bidirectionnal data pins controlled by the R/W signal.

PORT D

In all modes, port D bits 0-5 may be used for general-purpose I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Bit 0 is the receive data input, and bit 1 is the transmit data output for the SCI. Bits 2 through 5 are used by the SPI subsystem.

PORT E

Port E is used for general-purpose static inputs and/or analog-to-digital channel inputs in all operating modes. Port E should not be read as static inputs while an A/D conversion is actually taking place.

6.4 · Memory

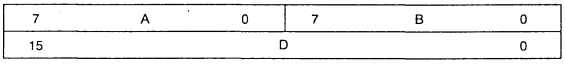
The memory maps for each mode of operation, a single-chip, expanded-multiplexed, special boot, and special test is shown in Figure 20. In the single-chip mode, the MCU does not generate external addresses. The internal memory locations are shown in the shaded areas, and the contents of the shaded areas are shown on the right side of the diagram. In the expanded-multiplexed mode, the memory locations are basically the same as the single-chip, except the memory locations between s shown in Figure 20. In the single-chip mode, the MCU does not (EXT) are for externally addressed memory and I/O. The special bootstrap mode is similar to the single-chip mode, except the bootstrap program ROM is located at memory locations $BF40 through $BFFF. The special test mode is similar to the expanded-multiplexed mode, except the interrupt vectors are at external memory locations.

6.5 · Registers

The MCU contains the registers described in the following paragraphs.

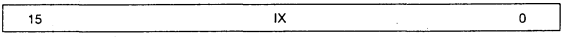
ACCUMULATOR A AND B

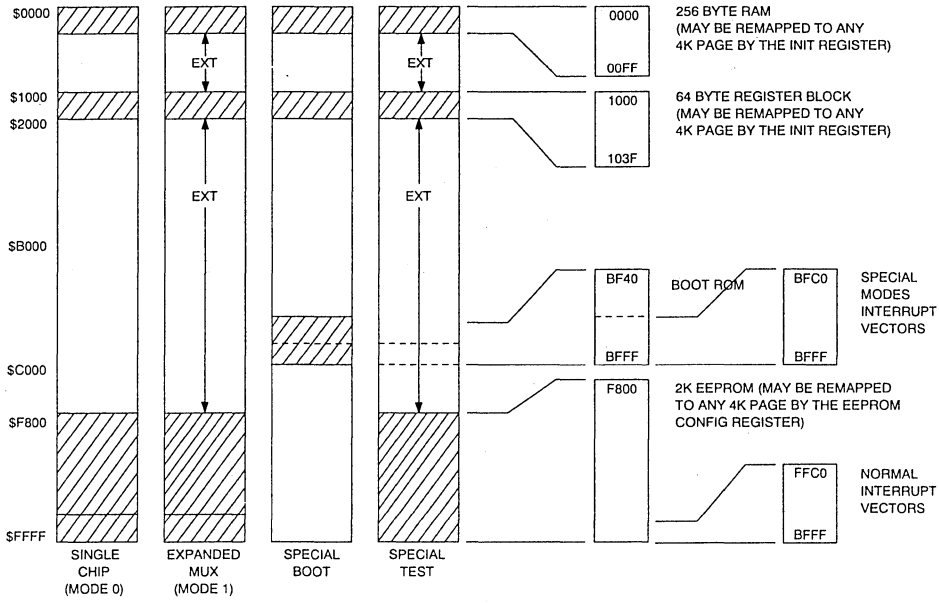
These accumulators are general-purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. These two accumulators are treated as a single, double-byte accumulator called the D accumulator fo some instructions.



INDEX REGISTER X (IX)

This index register is a 16-bit register used for the indexed addressing mode. It provides a 16-bit value that may be added to an 8-bit offset provided in an instruction to create an effective address. The index register may also be used either as a counter or a temporary storage area.





NOTE :

Note : Either or both the internal RAM and registers can be remapped to any 4K boundary by software.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	—	—	—	—	—	—	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF.	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
$1003	Bit 7	—	—	—	—	—	—	Bit 0	PORTC	I/O Port C
$1004	Bit 7	—	—	—	—	—	—	Bit 0	PORTB	Output Port B
$1005	Bit 7	—	—	—	—	—	—	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	—	—	—	—	—	—	Bit 0	DDRC	Data Direction for Port C
$1008			Bit 5	—	—	—	—	Bit 0	PORTD	I/O Port D
$1009			Bit 5	—	—	—	—	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	—	—	—	—	—	—	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Register
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Register

Figure 20 : Memory map.

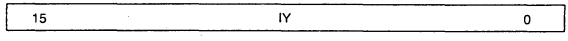
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Register
$100E	Bit 15	—	—	—	—	—	—	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	—	—	—	—	—	—	Bit 0		
$1010	Bit 15	—	—	—	—	—	—	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	—	—	—	—	—	—	Bit 0		
$1012	Bit 15	—	—	—	—	—	—	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	—	—	—	—	—	—	Bit 0		
$1014	Bit 15	—	—	—	—	—	—	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	—	—	—	—	—	—	Bit 0		
$1016	Bit 15	—	—	—	—	—	—	Bit 8	TOC1	Output Capture 1 Register
$1017	Bit 7	—	—	—	—	—	—	Bit 0		
$1018	Bit 15	—	—	—	—	—	—	Bit 8	TOC2	Output Capture 2 Register
$1019	Bit 7	—	—	—	—	—	—	Bit 0		
$101A	Bit 15	—	—	—	—	—	—	Bit 8	TOC3	Output Capture 3 Register
$101B	Bit 7	—	—	—	—	—	—	Bit 0		
$101C	Bit 15	—	—	—	—	—	—	Bit 8	TOC4	Output Capture 4 Register
$101D	Bit 7	—	—	—	—	—	—	Bit 0		
$101E	Bit 15	—	—	—	—	—	—	Bit 8	TOC5	Output Capture 5 Register/
$101F	Bit 7	—	—	—	—	—	—	Bit 0		Input Capture 4 Register
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
$1022	OC1I	OC2I	OC3I	OC4I	I405I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Reg. 1
$1023	OC1F	OC2F	OC3F	OC4F	I405F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Reg. 1
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Reg. 2
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Reg. 1
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL	Pulse Accum. Control Reg.
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accum. Count Reg.
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1

6

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCCR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	ADR1	EEPROM Block Protect Reg.
$1036 Thru $1038									Reserved	
$1039	ADPU	CSEL	IRGE	DLY	CME		CR1	CR0	OPTION	System Configuration Options
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circuitry
$103B	ODD	EVEN	—	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Prog. Control Reg.
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int and Misc
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Reg.
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
$103F	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON	CONFIG	COP, ROM, and EEPROM Enables.

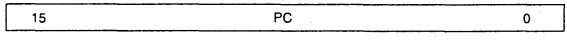
INDEX REGISTER Y (IY)

This index register is an 16-bit register used for the indexed addressing mode similar to the IX register ; however, most instructions using the IY register are two-byte opcodes and require an extra byte of machine code and an extra cycle of execution time. The index register may also be used as a counter or a temporary storage area.



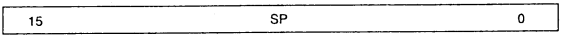
PROGRAM COUNTER (PC)

The program counter is a 16-bit register that contains the address of the next byte to be fetched.



STACK POINTER (SP)

The stack pointer is a 16-bit register that contains the address of the next free location on the stack. The stack is configured as a sequence of last-in-first-out read/write registers, which allow important data to be stored during interrupts and subroutine calls. Each time a new byte is added to the stack, the SP is incremented ; each time a byte is removed, the SP is incremented. The address contained in the SP also indicates the location at which the accumulators A and B registers IX and IY can be stored during certain instructions.



CONDITION CODE REGISTER (CCR)

The condition code register is an 8-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

7	6	5	4	3	2	1	0
S	X	H	I	N	Z	V	C

Carry/Borrow (C)
When set, this bit indicates that a carry of borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate instructions.

Overflow (V)
The overflow bit is set if an arithmetic overflow occured as a result of the operation ; otherwise the V bit is cleared.

Zero (Z)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Negative (N)
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (the MSB of the result is a logic one).

Interrupt (I)
This bit is set either by hardware or program instruction to disable (mask) all maskable interrupt sources (both external and internal).

Half carry (H)
This bit is set during ADD, ABA, and ADC operations to indicate that a carry occured between bits 3 and 4. This bit is mainly useful in BCD calculations.

X interrupt mask (X)
This mask bit is set only by hardware (reset or $\overline{XIRQ}$) and is cleared only by program instruction (TAP or RTI).

Stop disable (S)
This bit, under program control, is set to disable the STOP instruction, and is cleared to enable the STOP instruction. The STOP instructions is treated as no operation (NOP) if the S bit is set.

6.6 · Resets

The MCU can be reset four ways :

- an active low input to the $\overline{RESET}$ pin,
- a power-on reset function,
- a computer operating properly (COP) watchdog-timer timeout and,
- a clock monitor failure.

The $\overline{RESET}$ input consists mainly of a Schmitt trigger that senses the $\overline{RESET}$ line logic level.

RESET PIN

To request an external reset, the $\overline{RESET}$ pin must be held low for eight E_{cyc} (two E_{cyc} if no distinction is needed between internal and external resets). To prevent the EEPROM contents from being corrupted during power transitions, the reset line should be held low while V_{DD} is below its minimum operating level. A low voltage inhibit (LVI) circuit is required to protect EEPROM from corruption as shown in Figure 21.

POWER-ON RESET (POR)

Power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drop in the power supply voltage. If the external $\overline{RESET}$ pin is low at the end of the power-on delay time, the processor remains in the reset condition until $\overline{RESET}$ goes high.

COMPUTER OPERATING PROPERLY (COP) RESET

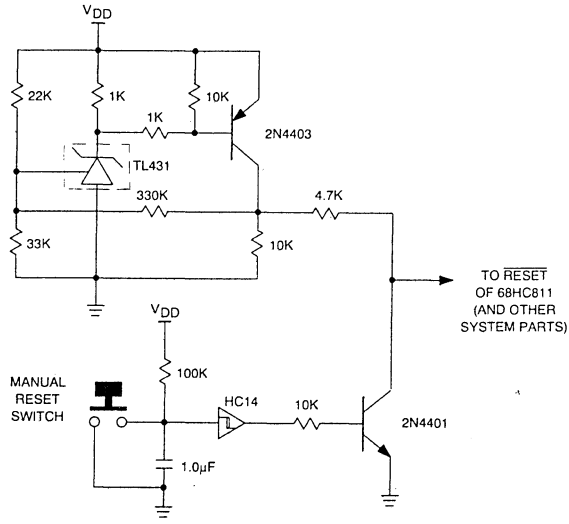
The MCU contains a watchdog timer that automatically times out if not reset within a specific time by a program reset sequence. If the COP watchdog timer is allowed to timeout, a reset is generated, which drives the $\overline{RESET}$ pin low to reset the MCU and the external system.

The COP reset function can be enabled or disabled by setting the control bit in an EEPROM cell of the system configuration register. Once programmed, this control bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. Protected control bits (CR1 and CR0),in the configuration options register, allow the user to select one of four COP timeout rates. Table 12 shows the relationship between CR1 and CR0 and the COP timeout period for various system clock frequencies.

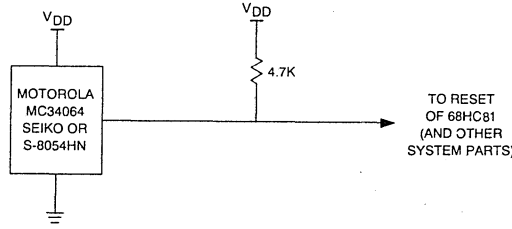
CLOCK MONITOR RESET

The MCU contains a clock monitor circuit which measures the E clock input frequency. If the E clock input rate is above 200 kHz, then the clock monitor does not generate a MCU reset. If the E clock signal is lost or its frequency falls below 10 kHz, then a MCU reset is generated, and the $\overline{\text{RESET}}$ pin is driven low to reset the external system.

The clock monitor reset can be enabled or disabled by a read-write control bit (CME) in the system configuration options register.



Reset Circuit with LVI and RC Delay



Simple LVI Reset Circuits

Figure 21 : Typical LVI reset circuits.

Table 12 - COP timeout periods

CR1	CR0	E/2^{15} divided by	XTAL = 2^{23} timeout −1/+15.6 ms	XTAL = 8.0 MHz timeout −0/+16.4 ms	XTAL = 4.9152 MHz timeout −0/+26.7 ms	XTAL = 4.0 MHz timeout −0/+32.8 ms	XTAL = 3.6864 MHz timeout −0/+35.6 ms
0	0	1	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	4	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	16	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	64	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

6.7 - Interrupts

There are seventeen hardware and one software interrupts (excluding reset type interrupts) that can be generated from all the possible sources. These interrupts can be divided into two categories, maskable and non-maskable. Fifteen of the interrupts can be masked with the condition code register I bit. All the on-chip interrupts are individually maskable by local control bits. The software interrupt is non-maskable. The external input to the $\overline{\text{XIRQ}}$ pin is considered a non-maskable interrupt because, once enabled, it cannot be masked by software ; however, it is masked during reset and upon receipt of an interrupt at the $\overline{\text{XIRQ}}$ pin. The last interrupt, illegal opcode, is also a non-maskable interrupt. Table 13 provides a list of each interrupt, its vector location in ROM, and the actual condition code and control bits that mask it. Figure 22 shows the interrupt stacking order.

SOFTWARE INTERRUPT (SWI)

The SWI is executed the same as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the CCR set). The SWI execution is similar to the maskable interrupts such as setting the I bit, CPU registers are stacked, etc.

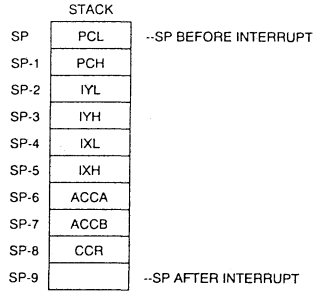


Figure 22 : Stacking order.

Note : The SWI instruction cannot be fetched as long as another interrupt is pending execution. However, once fetched, no other interrupt can be honored until the first instruction in the SWI service routine is completed.

Table 13 - Interrupt vector assignments

Vector address	Interrupt source	CC register mask	Local mask
FFC0, C1	Reserved		
*	*		
*	*		
FFD4, D5,	Reserved		
FFD6, D7	SCI serial system	I bit	
	Receive data register full		RIE
	Receive overrun		RIE
	Idle line detect		ILIE
	Transmit data register empty		TIE
	Transmit complet		TCIE

Table 13 - Interrupt vector assignments (continued)

Vector address	Interrupt source	CC register mask	Local mask
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflowd	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer output compare 5	I bit	OC5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	OC3I
FFEC, ED	Timer input capture 2	I bit	OC2I
FFEE, EF	Timer input capture 1	I bit	OC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	IRQ (external pin or parallel I/O)	I bit	
	External pin		None
	Parallel I/O handshake		STAI
FFF4, F5	XIRQ pin (pseudo non-maskable interrupt)	X bit	None
FFF6, F7	SWI	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure (reset)	None	NOCOP
FFFC, FD	COP clock monitor fail (reset)	None	CME
FFFE, FF	RESET	None	None

ILLEGAL OPCODE TRAP

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included in the MCU. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector.

REAL-TIME INTERRUPT

The real-time interrupt provides a programmable periodic interrupt. This interrupt is maskable by either the I bit in the CCR or the RTII control bit. The rate is based on the MCU E clock and is software selectable to be $E/2^{13}$, $E/2^{14}$, $E/2^{15}$, or $E/2^{16}$.

6.8 - Low-power modes

The MCU contains two programmable low-power operating modes : stop and wait. In the wait mode, the on-chip oscillator remains active ; in the stop mode, the oscillator is stopped. The following paragraphs describe the tow low-power modes.

STOP

The STOP instruction places the MCU in its lowest power consumption mode, provided the S bit in the CCR is clear. In this mode, all clocks are stopped, thereby halting all internal processing.

To exit the stop mode, a low level must be applied to either $\overline{IRQ}$, $\overline{XIRQ}$ or $\overline{RESET}$. An external interrupt used at $\overline{IRQ}$ is only effective if the I bit in the CCR is clear. An external interrupt applied at the $\overline{XIRQ}$ input would be effective regardless of the X-bit setting in the CCR ; however, the actual recovery sequence differs, depending on the X-bit setting. If the X bit is clear, the MCU starts with the stacking sequence leading to the normal service of the $\overline{XIRQ}$ request. If the X bit is set, the processing will always continue with the instruction immediately following the STOP instruction. A low input to the $\overline{RESET}$ pin will always result in an exit from the stop mode, and the start of MCU operations is determined by the reset vector.

A restart delay is required if the internal oscillator is being used, to allow the oscillator to stabilize when exiting the stop mode. If a stable external oscillator is being used, a control bit in the OPTION register may be used (cleared) to bypass the delay. If the control bit is clear, then the $\overline{RESET}$ pin would not normally be used for exiting the stop mode. In this case, the reset sequence sets the delay control bit, and the restart delay will be imposed.

WAIT

The WAIT instruction places the MCU in a low-power consumption mode, but the WAIT mode consumes slightly more power than the STOP mode. In the WAIT mode, the oscillator is kept running. Upon execution of the WAIT instruction, the machine state is stacked and program execution stops. The WAIT state can only be exited by an unmasked interrupt or $\overline{RESET}$. If the I bit is set and the COP is disabled, the timer system will be turned off to further reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins and upon subsystems (i.e., timer, SPI SCI) that are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT-mode current.

6.9 - Programmable timer

The timer system uses a «time-of-day» approach in that all timing functions are related to a single 16-bit free-running counter. The free-running counter is clocked by the output of a programmable prescaler (divide by 1, 4, 8, or 16), which is, in turn, clocked by the MCU E clock. The free-running counter can be read by software at any time without affecting its value because it is clocked and read on opposite half cycles of the E clock. The counter is cleared on reset and is a read-only register. The counter repeats every 65,536 counts, and when the count changes from $FFFF to $0000, a timer overflow flag bit is set. The overflow flag also generates an internal interrupt if the overflow interrupt enable bit is set. The timer has three input capture and five output compare functions. The functions and registers of the timer are explainded in the following paragraphs.

INPUT CAPTURE FUNCTION

There are four 16-bit read-only input capture registers that are not affected by reset. Each register is used to latch the value of the free-running counter when a selected transition at an external pin is detected. External devices provide the inputs on the PA0-PA3 pins, and an interrupt can be generated when an input capture edge is detected. The time of detection can be read from the appropriate register as part of the interrupt routine.

Port A pin 3 serves multiples functions. After reset, data direction bit 3 (DDRA3) in the PACTL register is cleared to zero configuring port A pin 3 as an input. Port A pin 3 can then be used as a input capture 4 (IC4), by setting 14/05 to «one» in the PACTL register. The 14/05 bit is configured to OC5 (cleared to zero) on reset. If DDRA3 is configured as an output and IC4 is enabled, writes to port A bit 3 causes edges on the PA3 to result in input captures. When the TI1405 register is acting as the IC4 capture register it cannot be written to. When PA3 is being used as IC4, writes to TI405 register have no meaning.

TIMER CONTROL REGISTER 2 (TCTL2) $1021

7	6	5	4	3	2	1	0
EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET							
0	0	0	0	0	0	0	0

EDGxB and EDGxA — input capture x edge control.

These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x.

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or faling) edge

6

OUTPUT COMPARE FUNCTION

There are five 16-bit read/write output compare registers, which are set to $FFFF on reset. A value written into the SE registers is compared to the free-running counter value during each E-clock cycle. If a match is found, the particular output compare flag is set, and an interrupt is generated, provided that particular interrupt is enabled.

In addition to the interrupt, a specified action may be intitiated at a timer output pin(s). For output compare one (OC1), the output action to be taken when a match is found is controlled by a 5-bit mask register and a 5-bit data regiser. The mask register specifies which timer port outputs are to be used, and the data register specifies what data is placed on the SE timer ports. For OC2 through OC5, one specific timer output is affected as controlled by the two-bit fields in a timer control register. These action include :

- timer disconnect from output pin logic,
- toggle output compare line,
- clear output compare line to zero, or
- set output compare line to one.

Upon reset, 14/05 is configured as OC5. The OC5 function overides DDRA3 to force the Port A pin 3 to be an output whenever OM5 : OL5 bits are not 0 : 0. In all other aspects, OC5 works the same as the other output compare.

TIMER COMPARE FORCE REGISTER (CFORC) $100B

This 8-bit write-only register is used to force early output compare actions. This compare force function is not recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undersirable operation.

7	6	5	4	3	2	1	0
FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET							
0	0	0	0	0	0	0	0

F0C1-F0C5 — Force output compare x action

1 = causes action programmed for output compare x, except the OCxF flag bit is not set.

0 = has no meaning

Bits 2-0 — not implemented. These bits always read zero.

These bits always read zero.

OUTPUT COMPARE 1 MASK REGISTER (0C1M) $100C

This register is used with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET							
0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

OUTPUT COMPARE 1 DATA REGISTER (OC1D) $100D

This register is used with output compare 1 to specify the data which is to be stored to the affected bit of port A as a result of a successful OC1 compare.

7	6	5	4	3	2	1	0
OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET							
0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit-x on successful OC1 compares.

TIMER CONTROL REGISTER (TCTL1) $1020

7	6	5	4	3	2	1	0
OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET							
0	0	0	0	0	0	0	0

OM2-OM5 — output mode

OL2-OL5 — output level.

These control bit pairs (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx comppare.

OMx	OLx	Action taken upon successful compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TIMER INTERRUPT MASK REGISTER 1 (TMSK1)

7	6	5	4	3	2	1	0
OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I
RESET							
0	0	0	0	0	0	0	0

OCxI — output compare x interrupt
1 = interrupt sequence requested if OCxF = 1 in TFLG1
0 = interrupt inhibited

| Cx | — input capture x interrupt
1 = interrupt sequence requested if ICxF = 1 in TFLG1
0 = interrupt inhibited.

Note : when the 14/05 bit in the PACTL register is one, the | 405 | bit behaves as the input capture 4 interrupt bit. When 14/05 is zero, the | 405 | bit acts as the output compare 5 interrupt control bit.

TIMER INTERRUPT FLAG REGISTER 1 (TFLG1)

This register is used to indicate the occurence of timer system events and, with the TMSK1 register, allows the timer sybsystem to operate in a polled or interrupt driven system. Each bit in the TFLG1 has a corresponding bit in the TMSK1 in the same bit position.

7	6	5	4	3	2	1	0
OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F
RESET							
0	0	0	0	0	0	0	0

OCxF — output compare x flag

Set each time the timer counter matches the output compare register x value. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
1 = bit cleared
0 = not affected.

ICxF — input capture x flag

Set each time a selected active edge is detected on the ICx input line. To clear a flag bit in TFLG1, you must write a «one» to the corresponding bit position(s).
1 = bit cleared
0 = not affected.

Note : When the 14/05 bit in the PACTL register is one, the I405F bit behaves as the input capture 4 flag bit. When 14/05 is zero, the | 405 | bit acts as the output compare 5 flag.

TIMER INTERRUPT MASK REGISTER 2 (TMSK2) $1024

This register is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in TFLG1. Two timer prescaler bits are also included in this register.

7	6	5	4	3	2	1	0
TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET							
0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt enable
1 = interrupt request when TOF = 1
0 = TOF interrupt disabled.

RTII — RTI Interrupt enable
1 = interrupt requested when RTIF = 1
0 = RTIF interrupt disabled

PAOVI — Pulse Accumulator OVerflow Interrupt enable
1 = interrupt requested when PAOVF = 1
0 = PAOVF disabled.

PAII — Pulse Accumulator Input Interrupt enable
1 = interrupt requested when PAIF = 1
0 = PAIF disabeld.

Bits 3-2 — not implemented
These bits always read zero.

PR1 and PR0 — timer prescaler selects.
Can only be written to during intitialization. Writes are disabled after the first write or after 64 E cycles our of reset.

PR1	PR0	Divide-by-factor
0	0	1
0	1	4
1	0	8
1	1	16

TIMER INTERRUPT FLAG REGISTER 2 (TFLG2)

This register is used to indicate the occurrence of timer system events and, with the TMSK2 register, allows the timer subsystem to operate in a polled or interrupt driven system. Each bit in the TFLG2 has a corresponding bit in the TMSK2 in the same bit position.

7	6	5	4	3	2	1	0
TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

TOF — Timer Overflow

Set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. Cleared by a write to TFLG2 with bit 7 set.

RTIF — Real-Time Interrupt Flag

Set at each rising edge of the seleted tap point. Cleared by a write to TFLG2 with bit 6 set.

PAOVF — Pulse-Accumulator OVerflow interrupt Flag

Set when the count in the pulse accumulator rolls over from $FF to $00. Cleared by a write to the TFLG2 with bit 5 set.

PAIF — Pulse-Accumulator Input-edge interrupt Flag

Set when an active edge is detected on the PAI input pin. Cleared by a write to TFLG2 with bit 4 set.

Bits 3-0 — not implemented

These bits always read zero.

6.10 · Pulse accumulator

The pulse accumulator is an 8-bit counter that can operate in either of two modes, depending on the state of a control bit in the PACTL register. These are the event counting mode and the gated time accumulation mode. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is activated.

PULSE ACCUMULATOR CONTROL REGISTER (PACTL) $1026

Four bits in this register are used to control an 8-bit pulse accumulator system, and tow other bits are used to select the rate for the real-time interrupt system.

7	6	5	4	3	2	1	0
DDRA7	PAEN	PAMOD	PEDGE	DDRA3	14/05	RTR1	RTR0
RESET							
0	0	0	0	0	0	0	0

DDRA7 — Data Direction for port A bit 7

1 = output

0 = input only

PAEN — Pulse-Accumulator system ENable

1 = pulse accumulator on

0 = pulse accumulator off

PAMOD — Pulse Accumulator Mode

1 = gated time accumultor

0 = exernal even counting

RTR1	RTR0	Divide E by	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	2^{13}	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	2^{14}	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	2^{15}	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	2^{16}	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

PEDGE — Pulse accumulator EDGE control

This bit provides clock action along with PAMOD.

1 = sensitive to rising edges at PAI pin if PAMOD = 0. In gated accumulation mode counting is enabled by a low on PAI pin if PAMOD = 1.

0 = sensitive to falling edges at PAI pin if PAMOD = 0. In gated accumulation mode counting is enabled by a high on PAI pin if PAMOD = 1

DDRA3 — Data Directional for port A bit 3

1 = output

0 = input only.

14/05 — Input 4/output 5

1 = input capture 4 function enabled (No OC5)

0 = output compare 5 function enabled (No IC4).

RTR1 and RTR0 — RTI interrupt rate selects.

These two bits slect one of four rates for the real-time peirodic interrupt circuits. Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

6.11 · EEPROM programming

The 2K bytes of EEPROM are located at $F800 through $FFFF. Programming of the EEPROM is controled by the EEPROM programming control register (PPROG). The EEPROM is disabled when the EEON bit in the system configuration register (CONFIG) is zero. Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz, the efficiency of this charge pump decreases, which increases the time required to program or erase a location. Recommended program and erase time is 10 milliseconds when the E clock is between 2 MHz and should be increased to as much as 20 milliseconds when E clock is between 1 MHz and 2 MHz. When E clock below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. The following paragraphs describe how to program or erase the EEPROM using the PPROG control register.

EEPROM BLOCK PROTECT REGISTER (BPROT) $1035

This 5-bit register protects against inadvertent writes to the CONFIG register and to the EEPROM. To permit the user to separate EEPROM into categories like «temporary» or «permanent», EEPROM is divided inot four individually protected blocks. The CONFIG register is also protected.

In normal operating modes, EEPROM and CONFIG are protected out of reset, and the user has 64 E clock cycles to unprotect any of the blocks that will require programming or erasing. The BPROT register bits can only be cleared, written to zero, during the first 64 E clock cycles after reset. Once the bits are cleared, the associated EEPROM section and/or the CONFIG register can be programmed or erased in the normal manner. The EEPROM is visible only if the EEON bit in the CONFIG register is set. In the test or bootstrap modes, bits of the BPROT register can be set or cleared at any time. In either single-chip or expanded mode, BPROT register bits can be writtent back to one anytime after the first 64 E clock cycles in order to protect the EEPROM and/or the CONFIG register. However, these bits can only be cleared again in the test or bootstrap modes.

7	6	5	4	3	2	1	0
0	0	0	ITCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET							
0	0	0	1	1	1	1	1

Bits 7-5 — Not implemented

These bits always read zero.

PTCON — Protect CONFIG register bit.

1 = programming / erasure of the CONFIG register disabled

0 = programming / erasure of the CONFIG register allowed.

BPRT3-BPRT0 — block protect bits

1 = a set bit protects a block of EEPROM against programming or erasure

0 = a cleared bit permits programming or erasure of the associated block.

Bit	Block protected	Block size
BPRT0	$1800-19FF	512 bytes
BPRT1	$1A00-1BFF	512 bytes
BPRT2	$1C00-1DFF	512 bytes
BPRT3	$1E00-1FFF	512 bytes

ERASING THE EEPROM

Erasure of the EEPROM is controled by bit settings in PPROG, and the appropriate bits int eh BPROT register must also be cleared before the EEPROM can be changed. Programs can be written to perform bulk, row, or byte erase. In bulk erase, all 2048 bytes of the EEPROM are erased. In row erase, 16 bytes ($F800-$F80F-$F810-$F81F, etc) are erased. Other MCU operations can continue to be performed during erasing provided the operations do not include reads of data from EEPROM.

PROGRAMMING EEPROM

During programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Zeros must be erased by a separate erase operation before programming. Other MCU operations can continue to be performed during programming provided the operations do not include reads of data from EEPROM.

EEPROM PROGRAMMING CONTROL REGISTER (PPROG) $103B

This 8-bit register is used to control programming and erasure of the EEPROM. This register is cleared on reset so the EEPROM is configured for normal reads.

7	6	5	4	3	2	1	0
ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET							
0	0	0	0	0	0	0	0

ODD — program odd rows (TEST)

EVEN — program even rows (TEST)

Bit 5 — not implemented.

This bit always reads zero.

BYTE — byte erase select.

This bit overrides the ROW bit.

1 = erase only one byte

0 = row or bulk erase.

ROW — row erase select.

If BYTE bit = 1, ROW has no meaning.

1 = row erase

0 = bulk or byte erase.

ERASE — erase mode select.

1 = erase mode

0 = normal read or program.

EELAT — EEPROM latch control.

1 = EEPROM address and data configured for programming/erasing

0 = EEPROM address and data configured for read mode.

EEPGM — EEPROM programming voltage enable

1 = programming voltage turned on

0 = programming voltage turned off.

Note : A strict register access seaquence must be followed to allow successfult programming and erase operations. The following procedures for modifying the EEPROM and CONFIG register detail the sequence. If an attempt is made to set bothe the EELAT and EEPGM bits in the same write cycle and if this attempt occurs before the required write cycle with the EELAT bit set, then neither is set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored, and the programming operation in progress is not disturbed. If no EEPROM address is written between when EELAT is set and EEPGM is set, then no program or erase operation takes place. These safeguards were included to preven accidental EEPROM changes in cases of program runaway.

ERASING THE CONFIG REGISTER

Erasing the CONFIG register follows the same procedures as that used for the EEPROM including bulk, byte, and row erase. The CONFIG register may be programmed or erased while the MCU is operating in any mode depending on the setting of bit 4 in BPROT.

PROGRAMMING THE CONFIG REGISTER

Programming the CONFIG register follows the same procedures as that used for the EEPROM except the CONFIG register address is used.

SYSTEM CONFIGURATION REGISTER (CONFIG) $103F

The CONFIG is implemented in EEPROM cells and controls the presense of ROM and EEPROM in the memory map and enables the COP watchdog system.

7	6	5	4	3	2	1	0
EE3	EE2	EE1	EE0	0	NOCOP	0	EEON

EE0-EE3 — EEPROM map position

These four bits specify the upper four bits of the EEPROM address. These bit have no meaning in the single-chip mode, because the 2K EEPROM is forced on a locations $F800 through $FFFF.

EE3	EE2	EE1	EE0	Location
0	0	0	0	$0800-$0FFF
0	0	0	1	$1800-$1FFF
0	0	1	0	$2800-$2FFF
0	0	1	1	$3800-$3FFF
0	1	0	0	$4800-$4FFF
1	0	1	0	$5800-$5FFF
0	1	1	0	$6800-$6FFF
0	1	1	1	$7800-$7FFF
1	0	0	0	$8800-$8FFF
1	0	0	1	$9800-$9FFF
1	0	1	0	$A800-$AFFF
1	0	1	1	$B800-$BFFF
1	1	0	0	$C800-$CFFF
1	1	0	1	$D800-$DFFF
1	1	1	0	$E800-$EFFF
1	1	1	1	$F800-$FFFF

Bit 3 — not implemented

This bit always reads one.

NOCOP — COP system disable

1 = COP watchdog system disabled

0 = COP watchdog system enabled

Bit 1 — not implemented

This bit always reads zero.

EEON — enable on-chip EEPROM

When this bit is programmed to «zero», the 2048-byte EEPROM is disabled, and that memory space becomes externally accessed space.

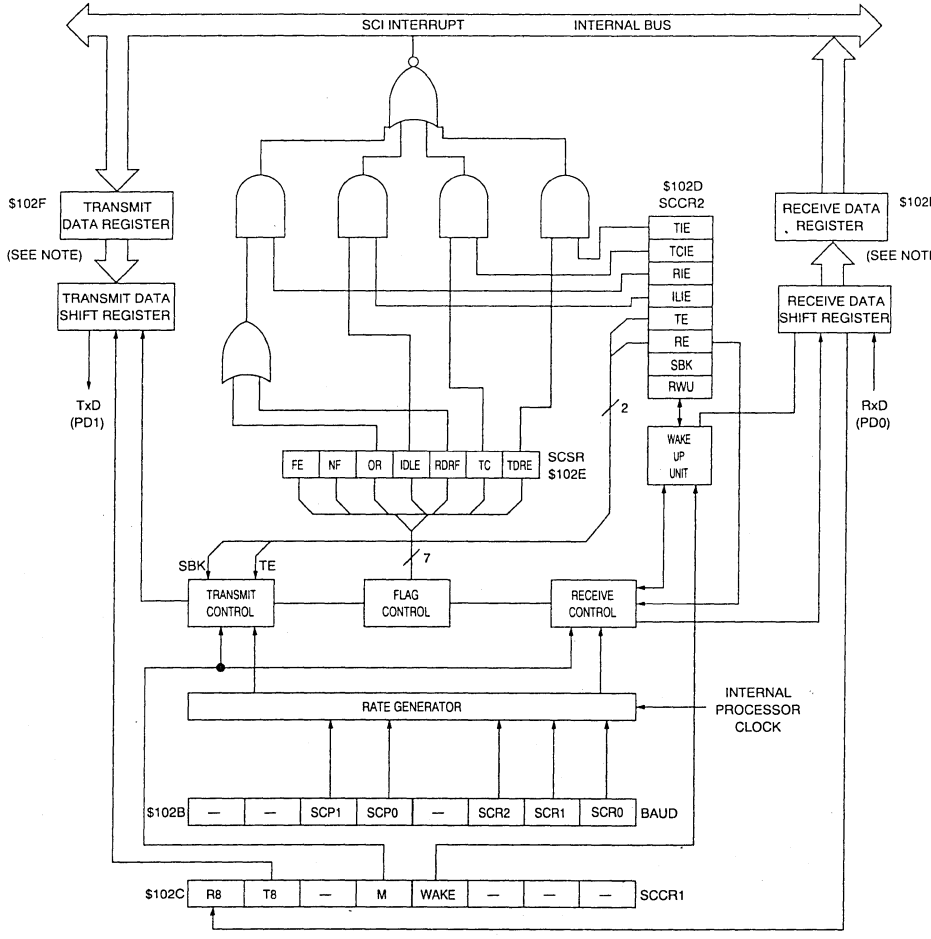
6.12 - Serial communications interface

The serial communications interface (SCI) allows the MCU to be interfaced efficiently with peripheral devices that require an asynchronous serial data format. The SCI uses a standard NRZ format with a variety of baud rates derived from the crystal clock circuit. Interfacing is accomplished using port D pins : PD0 for receive data (RxD) and PD1 for the transmit data (TxD). The baud-rate generation circuit contains a programmable prescaler and divider clocked by the MCU E clock. Figure 23 shows a block diagram of the SCI.

DATA FORMAT

Receive data in or transmit data out is the serial data presented between the PD0 and the internal data bus and between the internal data bus and PD1. The data format requires :

– an idle line in the high state prior to transmission/reception of a message,



Note : The serial communications data register (SCDR) is controlled by the internal R/W signal. It is the transmit data register when written and received data register when read.

Figure 23 : SCI block diagram.

- a start bit that is transmitted/received, indicating the start of each character,
- data that is transmitted and received least-significant bit (LSB) first,
- a stop bit (tenth or eleventh bit set to logic one), which indicates the frame is complet ; and
- a break defined as the transmission or reception of a logic zero for some multiple of frames.

Selection of the word length is controlled by the M bit in serial communications control register 1 (SCCR1).

TRANSMIT OPERATION

The SCI transmitter includes a parallel data register and a serial shift register. This double-buffered system allows a character to be shifted out serially while another character is waiting in the transmit data register to be transferred into the serial shift register. The output of the serial shift register is applied to PD1 as long as transmission is in progress or the transmit enable bit is set.

RECEIVE OPERATION

Data is received in a serial shift register and is transferred to a parallel receive data register as a complete word. This double-buffered system allows a character to be shifted in serially while another character is already in the receive data register. An advanced data recovery scheme is used to distinguish valid data from noise in the serial data stream. The data input is selectively sampled to detect receive data, and a majority voting circuit determines the value and intergrity of each bit.

WAKE-UP FEATURE

The wake-up feature reduces SCI service overhead in multiple receiver systems. Software for each receiver evaluates the first character(s) of each message. If the message is intended for a different receiver, the SCI can be placed in a sleep mode, disabling the rest of the message from generating requests for service. Whenever a new message begins, logic causes the sleeping receivers to awaken and evaluate the initial character(s) of the new message. Two methods of wake up are available : idle-line wake up or address mark wake up. In idle-line wake up, a sleeping receiver wakes up as soon as the RxD line becomes idel. In the address mark wake up, a «one» in the most-significant bit (MSB) of a character is used to indicate that the message is an address that wakes up a sleeping receiver.

SCI REGISTERS

The following paragraphs describe the operations of the five registers used in the SCI.

Serial communications data registers (SCDR)
The SCDR performs two functions : as the receive data register when it is read and as the transmit data register when it is written. Figure 23 shows the SCDR as two separate registers.

Serial communications control register 1 (SCCR1)
The SCCR1 provides the control bits to determine word length and select the method used for the wake-up feature.

7	6	5	4	3	2	1	0
R8	T8	0	M	WAKE	0	0	0
RESET							
U	U	0	0	0	0	0	0

R8 — receive data bit 8

If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

T8 — transmit data bit 8

If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character.

Bit 5 — not implemented

This bit always reads zero.

M — SCI character length

1 = 1 start bit, 9 data bits, 1 stop bit

0 = 1 start bit, 8 data bits, 1 stop bit.

WAKE — wake-up method select

1 = address mark

0 = idle line.

Bits 2-0 — not implemented

These bits always read zero.

Serial conmmunications control register 2 (SCCR2)
The SSCR2 provides the control bits that enable/disable individual SCI functions.

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET							
0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
1 = SCI interrupt if TDRE = 1
0 = TDR interrupts disabled.

TCIE — Transmit-Complete Interrupt Enable
1 = SCI interrupt if TC = 1
0 = TC interrupts disabled.

RIE — Receive Interrupt Enable
1 = SCI interrupt if RDRF or OR = 1
0 = RDRF or OR interrupt disabled.

ILIE — Idle-Line Interupt Enable
1 = SCI interrupt if IDLE = 1
0 = IDLE interrupt disabled.

TE — Transmit Enable
1 = transmit shift register output is applied to the TxD line
0 = PD1 pin reverts to general-purpose I/O as soon as current transmitter activity finishes.

RE — Receive Enable
1 = receiver enabled
0 = receiver disabled and RDRF, IDLE, OR, NF, and FE interrupts are inhibited.

RWU — Receiver Wake Up
When set by user's software, this bit puts the receiver to sleep and enables the «wake-up» function. If the WAKE bit is zero, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If WAKE is one, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send BreaK
If this bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or to sending data. If SBK remains set, the transmitter will continually send whole frames of zeros (sets of 10 or 11) until cleared.

Serial communications status register (SCSR)
The SCSR provides inputs to the interrupt logic circuits for generation of the SCI system interrupts.

7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET							
1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty
1 = automatically set when contents of the serial communications data register was transferred to the transmit serial shift register
0 = cleared by a read of SCSR (with TDRE = 1) followed by a write to SCDR.

TC — Transmit Complete
1 = automatically set when all data frame, preambel, or break condition transmissions are complete
0 = cleared by a read of SCSR (with TC = 1) followed by a write to SCDR.

RDRF — Receive Data Register Full
1 = automatically set when a character is transferred from the receiver shift register to the SCDR
0 = cleared by a read of SCSR (with RDRF = 1) followed by a read of SCDR.

IDLE — IDLE-line detect
This bit is inhibited while RWU = 1.
1 = automatically set when the receiver serial input becomes idle after having been active
0 = cleared by a read of SCSR (with IDLE = 1) followed by a read of SCDR.

OR — Overrun error
1 = automatically set when a new character cannot transfer from the receive shift register because the character in SCDR has not been read
0 = cleared by a read of SCSR (with OR = 1) followed by a read of SCDR.

NF — Noise Flag
1 = automatically set when majority voting logic does not bind unanimous agreement of all samples in any bit in the recieved frame
0 = cleared by a read of SCSR (with NF = 1) followed by a write to SCDR.

FE — Framing Error

1 = automatically set when a logic 0 is detected where a stop bit was expected

0 = cleared by a read of SCSR (with FE = 1) followed by a read of SCDR.

Bit 0 — not implemented

This bit always reads zero.

Baud-rate register (BAUD)

This register is used to select different baud rates that may be used as the rate control for the receiver and transmitter.

7	6	5	4	3	2	1	0
TDLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET							
1	1	0	0	0	U	U	U

TCLR — clear baud-rate counters (test)

This bit is used to clear the baud-rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

Bit 6 — not implemented

This bit always reads zero.

SCP1 and SCP0 — SCI baud-rates prescaler selects

These bits control a prescaler whose output provides the input to a second divider which is controlled by the SCR2-SCR0 bits. Refer to Table 14.

RCKB — SCI baud-rate clock check (test)

This bit is used during factory testing to enable the exlcusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

SCR2-SCR0 — SCI baud-rate selects

These bits select the baud rate for both the transmitter and the receiver. The prescaler output selected by SCP1 and SCP0 is further divided by the setting of these bits. Refer to Table 15.

6

Table 14 - Prescaler highest baud-rate frequency output

SCP bit		Clock * divided by	Crystal frequency (MHz)				
1	0		8.3886	8.0	4.9152	4.0	3.6864
0	0	1	131.072 K Baud	125.000 K Baud	76.80 K Baud	62.50 K Baud	57.60 K Baud
0	1	3	43.690 K Baud	41.666 K Baud	25.60 K Baud	20.833 K Baud	19.20 K Baud
1	0	4	32.768 K Baud	31.250 K Baud	19.20 K Baud	15.625 K Baud	14.40 K Baud
1	1	13	10.082 K Baud	9600 K Baud	5.907 K Baud	48000 K Baud	4430 K Baud

* The clock in the «clock divide by» column is the internal processor clock.

Table 15 - Transmit baud-rate output for a given prescaler output

SCR bit			Divided by	Representative highest output for baud-rate output				
2	1	0		131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 bau	600 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud

6.13 · Serial peripheral interface

The serial peripheral interface (SPI) is a high-speed synchronous serial I/O system. The transfer rate is software selectable up to one-half of the MCU E clock rate. The SPI may be used for simple I/O expansion or to allow several MCUs to be interconnected in a multimaster configuration. Clock phase and polarity are software programmable to allow direct compatibility with a large number of peripheral devices.

Four basic signal lines are associated with the SPI system. These are the master-out-slave-in (MOSI), the master-in-slave-out (MISO), the serial clock (SCK), and the slate select (SS). When data is written to the SPI data register of a master device, a transfer is automatically initiated. A series of eight SCK clock cycles are generated to synchronize data transfer.

When a master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. The byte transmitted is replaced by the byte received, thereby eliminating the need for separate transmit-empty and receiver-full status bits. Figure 24 shows a block diagram of the SPI.

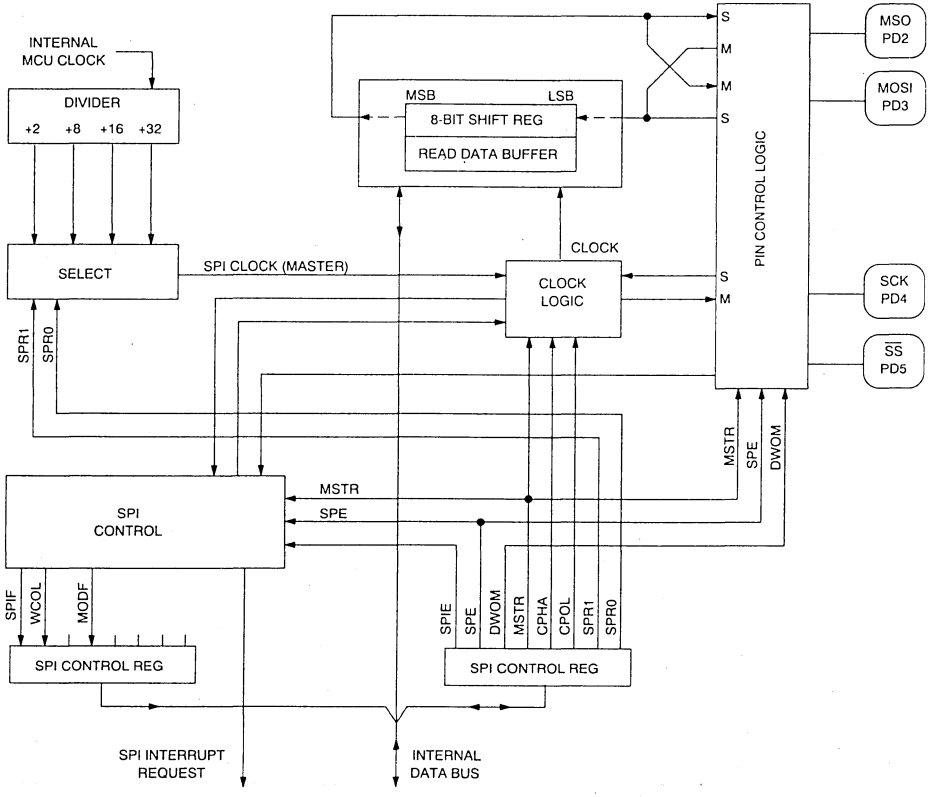


Figure 26 : Opcode map.

SPI REGISTERS

There are three registers in the SPI that provide control, status, and data-storage functions. These registers are described in the following paragraphs.

Serial peripheral control register (SPCR)

7	6	5	4	3	2	1	0
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET							
0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
- 1 = SPI interrupt if SPIF = 1
- 0 = SPIF interrupts disabled

SPE — Serial Peripheral system Enable
- 1 = SPI system on
- 0 = SPI system off

DWOM — port D Wire-OR Mode option

This bit affects all six port D together.
- 1 = port D outputs act as open-drain outputs
- 0 = port D outputs are normal CMOS outputs

MSTR — master mode select
- 1 = master mode
- 0 = slave mode

CPOL — Clock Polarity

This bit selects the polarity of the SCK clock.
- 1 = SCK line idles high
- 0 = SCK line idles low

CPHA — Clock PHAse

This bit selects one of two fundamentally different clock protocols. Refer to Figure 25.

If CPHA = 0, transfer begins when SS goes low and ends when SS goes high after eight clock cycles on SCK. If CPHA = 1, transfer begins the first time SCK becomes active while SS is low and ends when the SPIF flag gests set.

SPR1 and SPR0 — SPI clock rate select

These two bits select on of four baud rates to be used as SCK if the SPI is set as the master. They have no effect in the slave mode.

SPR1	SPR0	Internal processor clock divide by
0	0	5
0	1	4
1	0	16
1	1	32

Serial Peripheral Status Register (SPSR) $1029

7	6	5	4	3	2	1	0
SPIF	WCOL	0	MODF	0	0	0	0
RESET							
0	0	0	0	0	0	0	0

SPIF — SPI transfer complete flag

1 = automatically set when data transfer is complete between processor and external device

0 = cleared by a read of SPSR (with SPIF = 1), followed by a access (read or write) of the SPDR.

WCOL — Write COLlision

1 = automatically set when an attempt is made to write to the SPI data register while data is being transferred

0 = cleared by a read of SPSR (with WCOL = 1), followed by an access (read or write) of the SPDR.

Bit 5 — not implemented

This bit always reads zero.

MODF — mode fault

This bit indicates the possibility of a multi-master conflict for system control and therefore allows a proper exit from system operation to a reset or default system state.

1 = automatically set when a master device has its SS pin pulled low

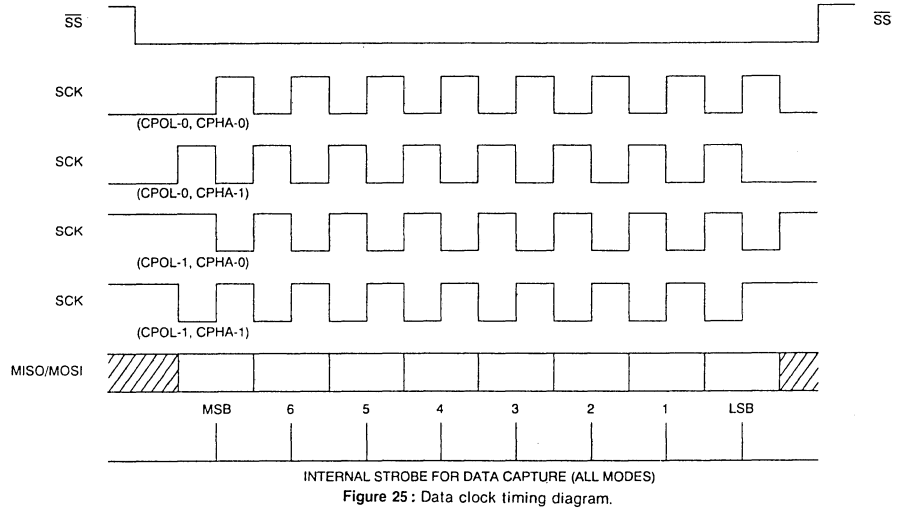


Figure 25 : Data clock timing diagram.

0 = cleared by a read of SPSR (with MODF = 1), followed by a write to the SPCR.

Bits 3-0 — not implemented

These bits always read zero.

Serial peripheral data I/O (SPDR)

This register is used to transmit and receive data on the serial bus. A write to this register in a master will initiate transmission/reception of another byte. A slave writes data to this register for later transmission to a master. When transmission is complete, the SPIF status bit is set in both the master and slave device. When a read is performed on the SPDR, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated, or an overrun condition will exist. In case of an overrrun, the byte causing the overrrun is lost.

6.14 · Analog-to-digital converter

The MCU contains an 8-channel, multiplexed-intput, successive approximation, analog-to-digital (A/D) converter with sample and hold. Two dedicated lines (V_{RL}, and V_{RH}) are provided for the reference supply voltage input. These pins are used instead of the device power pins to increase the accuracy of the A/D converions.

The 8-bit A/D conversions of the MCU are accurate to within ± 1 LSB (± 1/2 LSB quantizing errors and ± 1/2 LSB all other errors combined). Each conversion is accomplished in 32 MCU E-clock cycles. An internal control bit allows selection of an internal conversion clock oscillator that allows the A/D to be used with very low MCU clock rates. A typical conversion cycle requires 16 microseconds to complete at a 2-MHz bus frequency.

Four result registers are included to further enhance the A/D subsystem along with control logic to control conversion activity automatically. A single write instruction selects one of four conversion sequences, resulting in a conversion complete flag after the first four conversions. The sequences are as follows :

- Convert one channel four times and stop, sequential results placed in the result registers.
- Convert one group of four channels and stop, each result register is dedicated to one channel.
- Convert one channel continuously, updating the result registers in a roud-robin fashion.
- Convert one group of four channels (roud-robin fashion) continuously, each result register is dedicated to one channel.

6.15 · Instruction set

The MCU can execute all of the M6800 and M6801 instructions. In addition to these instructions, 91 new opcodes are provided by the paged opcode map. These instructions can be divided into five different types :

- accumulator and memory,
- index register and stack pointer,
- jump, branch, and program control,
- bit manipulation, and
- conditon code register instructions.

The following paragraphs briefly explain each type.

ACCUMULATOR/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The accumulator/memory instructions can be divided into four subgroups :

- load/store/transfer,
- arithmetic/math,
- logical, and
- shift/rotate.

The following paragraphs describe the different groups of accumulator/memory instructions.

Load/Store/Transfer

Refer to the following table for load/store/transfer instructions.

Function	Mnemonic
Clear memory byte	CLR
Clear accumulator A	CLRA
Clear accumulator B	CLRB
Load accumulator A	LDAA
Load accumulator B	LDAB
Load double accumulator D	LDD
Push A onto stack	PSHA
Push B onto stack	PSHB
Pull A from stack	PULA
Pull B from stack	PULB

Function	Mnemonic
Store accumulator A	STAA
Store accumulator B	STAB
Store accumulator D	STD
Transfer A to B	TAB
Transfer A to CC register	TAP
Transfer B to A	TBA
Transfer CC register to A	TPA
Exchange D with X	XGDX
Exchange D with Y	XGDY

Logical

This group is used to make comparisions, decisions, and extractions of data. Refer to the following list for the logical instructions.

Function	Mnemonic
AND A with memory	ANDA
AND B with memory	ANDB
Bit(s) test A with memory	BITA
Bit(s) test B with memory	BITB
1's complement memory byte	COM
1's complement A	COMA

Function	Mnemonic
1's complement B	COMB
Exclusive OR A with memory	EORA
Exclusive OR B with memory	EORB
OR accumulator A (inclusive)	ORAA
OR accumulator B (inclusive)	ORAB

Shift/Rotate
The shift and rotate instructions automatically operate through the carry bit, which allows easy extension to multiple bytes. Refer to the following list for the shift/rotate instructions.

Function	Mnemonic
Arithmetic shift left	ASL
(Logical shift left)	(LSL)
Arithmetic shift left A	ASLA
(Logical shift left accumulator A)	(LSLA)
Arithmetic shift left B	ASLB
(Logical shift left accumulator B)	(LSLB)
Arithmetic shift left double	ASLD
(Logical shift left double)	(LSLD)
Arithmetic shift right	ASR
Arithmetic shift right A	ASRA
Arithmetic shift right B	ASRB

Function	Mnemonic
Logical shift right	LSR
Logical shift right accumulator A	LSRA
Logical shift right accumulator B	LSRB
Logical shift right double	LSRD
Rotate left	ROL
Rotate left accumulator A	ROLA
Rotate left accumulator B	ROLB
Rotate right	ROR
Rotate right accumulator A	RORA
Rotate right accumulator B	RORB

Arithmetic/Math
Refer to the following table for the arithmetic/math instructions.

Function	Mnemonic
Add accumulators	ABA
Add B to X	ABX
Add B to Y	ABY
Add with carry to A	ADCA
Add with carry to B	ADCB
Add memory to A	ADDA
Add memory to B	ADDB
Add 16-bit to D	ADDD
Compare A to B	CBA
Compare A to memory	CMPA
Compare B to memory	CMPB
Compare D to memory (16 bit)	CPD
Decimal adjust A	DAA
Decrement memory byte	DEC
Decrement accumulator A	DECA
Decrement accumulator B	DECB
Fractional divide 16 × 16	FDIV

Function	Mnemonic
Integer divide 16 × 16	IDIV
Increment memory byte	INC
Increment accumulator A	INCA
Increment accumulator B	INCB
Multiply 8 × 8	MUL
2's complement memory byte	NEG
2's complement A	NEGA
2's complement B	NEGB
Subtract B from A	SBA
Subtract with carry from A	SBCA
Subtract with carry from B	SBCB
Subtract memory from A	SUBA
Subtract memory from B	SUBB
Subtract memory from D	SUBD
Test for zero or minus	TST
Test for zero or minus A	SBA
Test for zero or minus B	TSTB

INDEX-REGISTER AND STACK-POINTER INSTRUCTIONS
These instructions provide a method for storing data and for manipulation of index register, stack pointer, and individual segments of data within the register and stack pointer. Refer to the following list for the index-register and stack-pointer instuctions.

Function	Mnemonic
Add B to X	ABX
Add B to Y	ABY
Compare X to memory (16 bit)	CPX
Compare Y to memory (16 bit)	CPY
Decrement stack pointer	DES
Decrement index register X	DEX
Decrement index register Y	DEY
Increment stack pointer	INS
Increment index register X	INX
Increment index register Y	INY
Load index register X	LDX
Load index register Y	LDY
Load stack pointer	LDS

Function	Mnemonic
Push X onto stack (low first)	PSHX
Push Y onto stack (low first)	PSHY
Pull X from stack (high first)	PULX
Pull Y from stack (high first)	PULY
Store stack pointer	STS
Store index register X	STX
Store index register Y	STY
Transfer stack pointer to X	TSX
Transfer stack pointer to Y	TSY
Transfer X to stack pointer	TXS
Transfer Y to stack pointer	TYS
Exchange D with X	XGDX
Exchange D with Y	XGDY

BIT-MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit residing in the first 256 bytes of the memory space in direct address mode. The MCU can use any bit in the 64K memory map, and all bit-manipulation instructions can be used with direct or index (x or y) addressing modes. Software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses. The bit-manipulation instructions use an 8-bit mask, which allows simultaneous operations on any combination of bits in a location. Refer to the following list for the bit-manipulation instructions.

Function	Mnemonic
Clear bit(s)	BCRL
Branch if bit(s) clear	BRCRL

Function	Mnemonic
Branch if bit(s) set	BRSET
Set bit(s)	BSET

JUMPS/BRANCHES/PROGRAM-CONTROL INSTRUCTIONS

These instructions provide techniques for modifying the normal sequence of the program for conditional and unconditional branching. Refer to the following list for the jump/branch/program-control instructions.

Function	Mnemonic
Branch if carry clear	BCC
(Branch if higher or same)	(BHS)
Branch if carry set	BCS
(Branch if lower)	(BLO)
Branch if = zero	BEQ
Branch if ⩾ zero	BGE
Branch if > zero	BGT
Branch if higher	BHI
Branch if ⩽ zero	BLE
Branch if lower or same	BLS
Branch if < zero	BLT
Branch if minus	BMI
Branch if not = zero	BNE
Branch if plus	BPL
Branch always	BRA

Function	Mnemonic
Branch if bit(s) clear	BRCLR
Branch never	BRN
Branch if bit(s) set	BRSET
Branch to subroutine	BSR
Branch if overflow clear	BVC
Branch if overflow set	BVS
Jump	JMP
Jump to subroutine	JSR
No operation	NOP
Return from interrupt	RTI
Return from subroutine	RTS
Stop internal clocks	STOP
Software interrupt	SWI
Test operation (test mode only)	TEST
Wait for interrupt	WAI

CONDITION-CODE-REGISTER INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for the condition-code-register instructions.

Function	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
Clear overflow flag	CLV
Set carry	SEC

Function	Mnemonic
Set interrupt mask	SEI
Set overflow flag	SEV
Transfer A to CC register	TAP
Transfer CC register to A	TPA

OPCODE MAP SUMMARY

Table 26 is an opcode map for the instructions used on the MCU.

6.16 · Addressing modes

The MCU uses six different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. Some instructions require an additional byte before the opcode to accomodate a multipage opcode map ; this byte is called a prebyte.

The term «effective address» (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored. The following paragraphs describe the different addressing modes.

IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. These are two, three, or four (if prebyte is required) byte instructions.

DIRECT

In the direct addressing mode, the least-significant byte of the operand address is contained in a single byte following the opcode and the most-significant byte of an address is assumed to be $00. Direct addressing allows the user to directly address $0000 through $00FF using two-byte instructions, and execution time is reduced by eliminating the additional memory access. In most applications, this 256-byte area is reserved for frequently referenced data. In the MCU, software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses.

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. These are three or four (if prebyte is required) byte instructions : one or two for the opcode and two for the effective address.

INDEXED

In the indexed addressing mode, one of the index registers (X or Y) is used in calculating the effective address. In this case, the effective address is variable and depends on two factors :

- the current contents of the index register (X or Y) being used, and
- the 8-bit unsigned offset contained in the instruction.

This addressing mode allows referencing any memory location in the 64K byte address space. These are usually two or three (if prebyte is required) byte instructions, the opcode plus the 8-bit offset.

RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instructions. These are usually two-byte instructions.

INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructons are one-or two-byte instructions.

PREBYTE

To expand the number of instructions used in the MCU, a prebyte instruction has been added to certain instructions. The instructions affected are usually associated with index register Y. Accessing opcodes from pages 2, 3, or 4 would require a prebyte instruction.

HI / LOW	INH 0	INH 1	REL 2	INH 3	ACCA 4	ACCB 5	INDX(Y) 6	EXT 7	IMM 8	DIR 9	INDX(Y) A	EXT B	IMM C	DIR D	INDX(Y) E	EXT F	HI / LOW
0	TEST	SBA	BRA	TSX(Y)	NEGA	NEGB	NEG	NEG	SUBA	SUBA	SUBA	SUBA	SUBB	SUBB	SUBB	SUBB	0
1	NOP	CBA	BRN	INS					CMPA	CMPA	CMPA	CMPA	CMPB	CMPB	CMPB	CMPB	1
2	IDIV	BRSET	BHI	PULA					SBCA	SBCA	SBCA	SBCA	SBCB	SBCB	SBCB	SBCB	2
3	FDIV	BRCLR	BLS	PULB	COMA	COMB	COM	COM	* SUBD	* SUBD	* SUBD	* SUBD	ADDD	ADDD	ADDD	ADDD	3
4	LSRD	BSET	(BHS) BCC	DES	LSRA	LSRB	LSR	LSR	ANDA	ANDA	ANDA	ANDA	ANDB	ANDB	ANDB	ANDB	4
5	(LSLD) ASLD	BCLR	(BLO) BCS	TX(Y)S					BITA	BITA	BITA	BITA	BITB	BITB	BITB	BITB	5
6	TAP	TAB	BNE	PSHA	RORA	RORB	ROR	ROR	LDAA	LDAA	LDAA	LDAA	LDBB	LDBB	LDBB	LDBB	6
7	TPA	TBA	BEQ	PSHB	ASRA	ASRB	ASR	ASR		STAA	STAA	STAA		STBB	STBB	STBB	7
8	INX(Y)	PAGE 2	BVC	PULX(Y)	ASLA	ASLB	ASL	ASL	EORA	EORA	EORA	EORA	EORB	EORB	EORB	EORB	8
9	DEX(Y)	DAA	BVS	RTS	ROLA	ROLB	ROL	ROL	ADCA	ADCA	ADCA	ADCA	ADCB	ADCB	ADCB	ADCB	9
A	CLV	PAGE 3	BPL	ABX(Y)	DECA	DECB	DEC	DEC	DRAA	DRAA	ORAA	ORAA	ORAB	ORAB	ORAB	ORAB	A
B	SEV	ABA	BMI	RTI					ADDA	ADDA	ADDA	ADDA	ADDB	ADDB	ADDB	ADDB	B
C	CLC	BSET	BGE	PSHX(Y)	INCA	INCB	INC	INC	CPX(Y)	CPX(Y)	* CPX(Y)	CPX(Y)	LDD	LDD	LDD	LDD	C
D	SEC	BCLR	BLT	MUL	TSTA	TSTB	TST	TST	BSR	JSR	JSR	JSR	PAGE 4	STD	STD	STD	D
E	CLI	BRSET	BGT	WAI			JMP	JMP	LDS	LDS	LDS	LDS	LDX(Y)	LDX(Y)	LDX(Y)	* LDX(Y)	E
F	SEI	BRCLR	BLE	SWI	CLRA	CLRB	CLR	CLR	XGDX(Y)	STS	STS	STS	STOP	STX(Y)	STX(Y)	LDD	F

INH : Inherent REL : Relative IMM : Immediate EXT : Extended DIR : Direct INDX(Y) : Index X(Y).

Mnemonic	Page	Opcode	Bytes	Cycles
CPD	3	83	4	5
	3	93	3	6
	3	B3	4	7
	3	A3	3	7
	4	A3	3	7
CPY	3	AC	3	7
CPX	4	AC	3	7
LDY	3	EE	3	6
LDX	4	EE	3	6
STY	3	EF	3	6
STX	4	EF	3	6

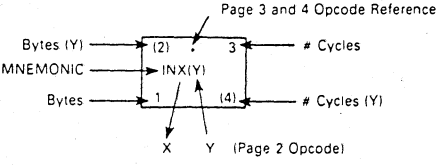


Table 16 - Opcode map

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38535 or TCS standards.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance with MIL-STD-883 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

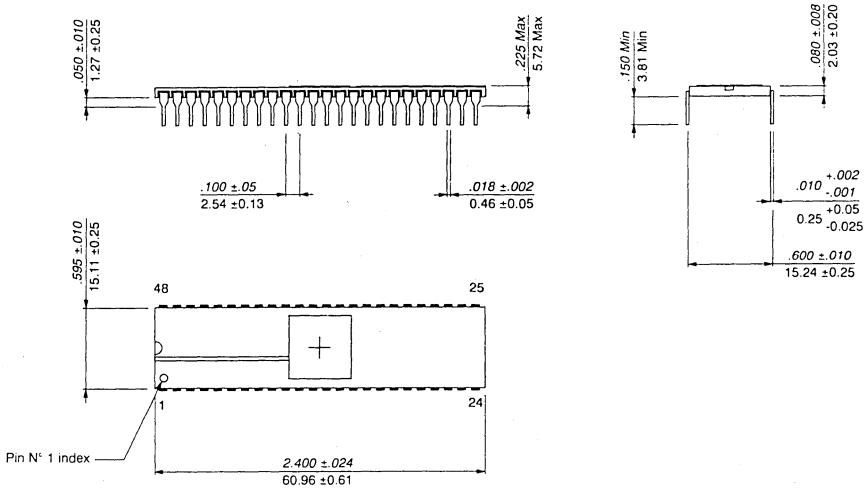
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

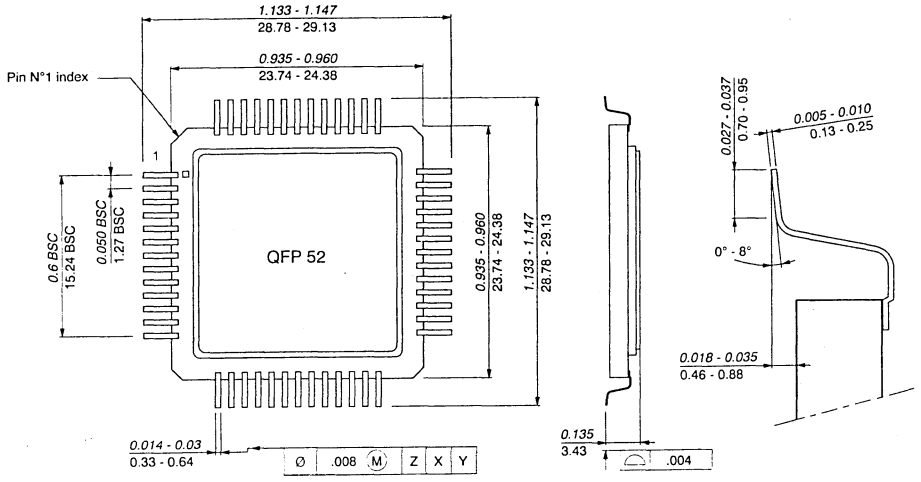
f) Maintain relative humidity above 50 %, if practical.

9 - PACKAGE MECHANICAL DATA

9.1 - 48 pins - Ceramic Side Brazed Dual in Line



9.2 - 52 pins - Ceramic Quad Flat Pack



10 - TERMINAL CONNECTIONS

10.1 - 48 pins - Ceramic Dil

See Figure 2.1 page 3.

10.2 - 52 pins - Ceramic Quad Flat Pack

See Figure 2.2 page 3.

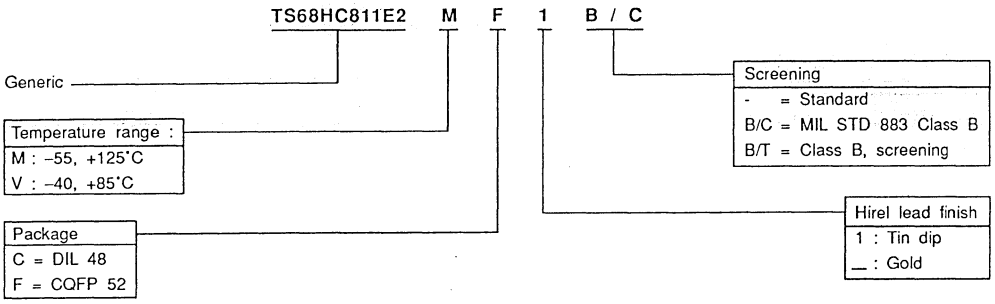
11 - ORDERING INFORMATION

11.1 - Hi-REL product

Commercial TCS part-number (see Note)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC11E2MCB/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11E2MFB/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11E2MC1B/C	MIL-STD-883	DIL 48	−55 / +125	TCS data-sheet
TS68HC11E2MF1B/C	MIL-STD-883	CQFP 52	−55 / +125	TCS data-sheet
TS68HC11E2DES01XC	DESC	DIL 48	−55 / +125	5962-89527
TS68HC11E2DES01YC	DESC	CQFP 52	−55 / +125	5962-89527
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.				

11.2 - Standard product

Commercial TCS part-number (see Note)	Norms	Package	Temperature range T_C (°C)	Drawing number
TS68HC811E2VC	TCS standard	DIL 48	−40 / +85	Internal
TS68HC811E2MC	TCS standard	DIL 48	−55 / +125	Internal
TS68HC811E2VF	TCS standard	CQFP 52	−40 / +85	Internal
TS68HC811E2MF	TCS standard	CQFP 52	−55 / +125	Internal
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.				


TS68HC811E2 M F 1 B / C
Generic
Temperature range :
M : -55, +125°C
V : -40, +85°C
Package
C = DIL 48
F = CQFP 52
Screening
- = Standard
B/C = MIL STD 883 Class B
B/T = Class B, screening
Hirel lead finish
1 : Tin dip
_ : Gold

INTEGRATED MULTIPROTOCOL PROCESSOR (IMP)

DESCRIPTION

The IMP is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard, TS 68000/TS 68008 microprocessor core and a flexible communications architecture. This multichannel communications device may be configured to support a number of popular industry interfaces, including those for the integrated services digital network (ISDN) basic rate and terminal adaptor applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the IMP. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this versatile device.
The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an TS 68000/TS 68008 microprocessor core, a system integration block (SIB), and a communications processor (CP). The TS 68302 block diagram is shown in Figure 1.

MAIN FEATURES

The features of the IMP are as follows :

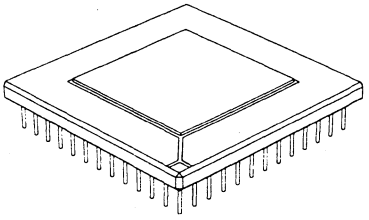
- TS 68000/TS 68008 microprocessor core supporting a 16- or 8-Bit TS 68000 family.
- SIB including :
  - independent direct memory access (IDMA) controller,
  - interrupt controller with two modes of operation,
  - parallel input/output (I/O) ports, some with interrupt capability,
  - on-chip usable 1152 bytes of dual-port random-access memory (RAM),
  - three timers, including a watchdog timer,
  - four programmable chip-select lines with wait-state logic,
  - programmable address mapping of dual-port RAM and IMP registers,
  - on-chip clock generator with an output clock signal,
  - system control : system control register ; bus arbitration logic with low interrupt latency support ; hardware watchdog for monitoring bus activity ; low power (standby) modes ; disable CPU logic (TS 68000) ; freeze control for debugging selected on-chip peripherals ; DRAM refresh controller.
- CP including :
  - main controller (RISC processor),
  - three full-duplex serial communication controllers (SCCs),
  - six serial direct memory access (SDMA) channels dedicated to the three SCCs,
  - flexible physical interface accessible by SCCs for interchip digital link (IDL), general circuit interface (GCI, see note), pulse code modulation (PCM), and nonmultiplexed serial interface (NMSI) operation,
  - serial communication port (SCP) for synchronous communication, clock rate up to 4.096 MHz
  - serial management controllers (SMCs) for IDL and GCI channels.
- Frequency of operation : 16.67 MHz.
- Power supply : 5 V_{DC} ± 10 %.

SCREENING / QUALITY

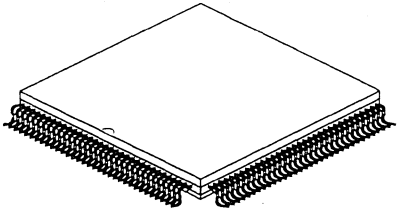
This product is manufactured in full compliance with either :

- MIL-STD-883 (class B).
- DESC. Drawing 5962-93159.
- or according to TCS standards.

Note : GCI is sometimes referred to as IOM2.



R suffix
PGA 132
(Ceramic Pin Grid Array)



A suffix
CERQUAD 132
(Ceramic Quad Flat Pack)

See the ordering information page 37.

Pin connection : see page 4.

SUMMARY

A - GENERAL DESCRIPTION

1 - INTRODUCTION

The TS 68302 integrated multiprotocol processor (IMP) is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard TS 68000 microprocessor core and a flexible communications architecture. The IMP may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Concurrent operation of different protocols is easily achieved through a combination of architectural and programmable features. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an TS 68000 microprocessor core, a system integration block (SIB), and a communications processor (CP).

Figure 1 is a block diagram of the TS 68302. The processor can be divided into two main sections : the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

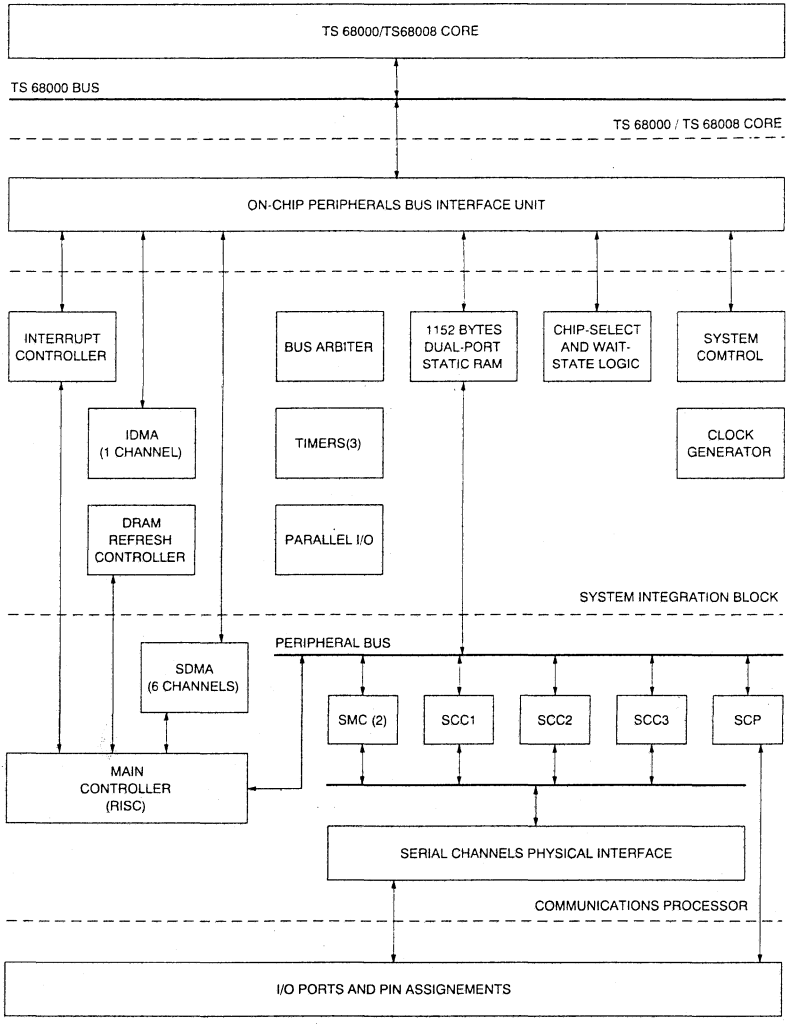


Figure 1 : TS 68302 block diagram.

2 · PIN ASSIGNMENTS

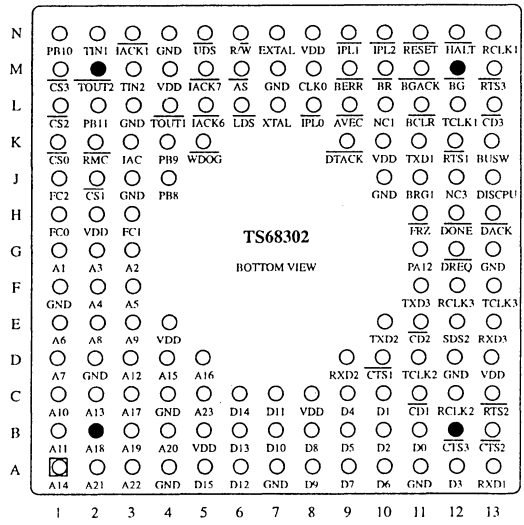


Figure 2.1 : PGA terminal designation.

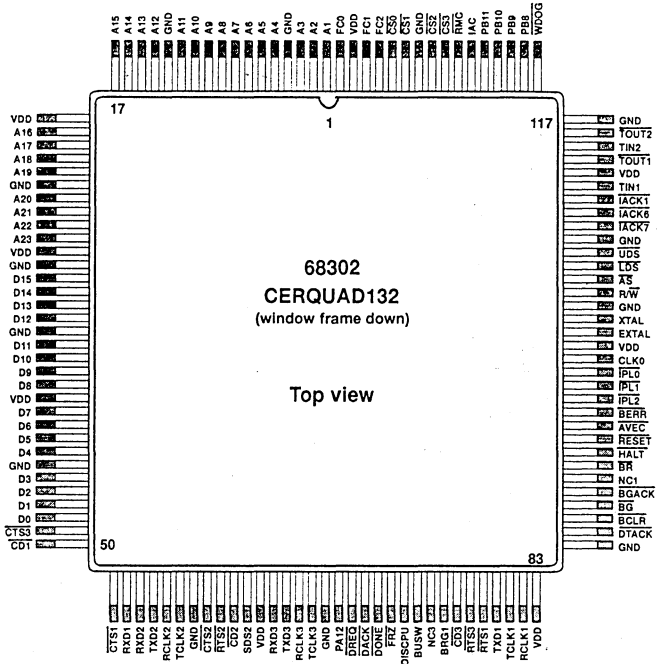


Figure 2.2 : CERQUAD terminal designation.

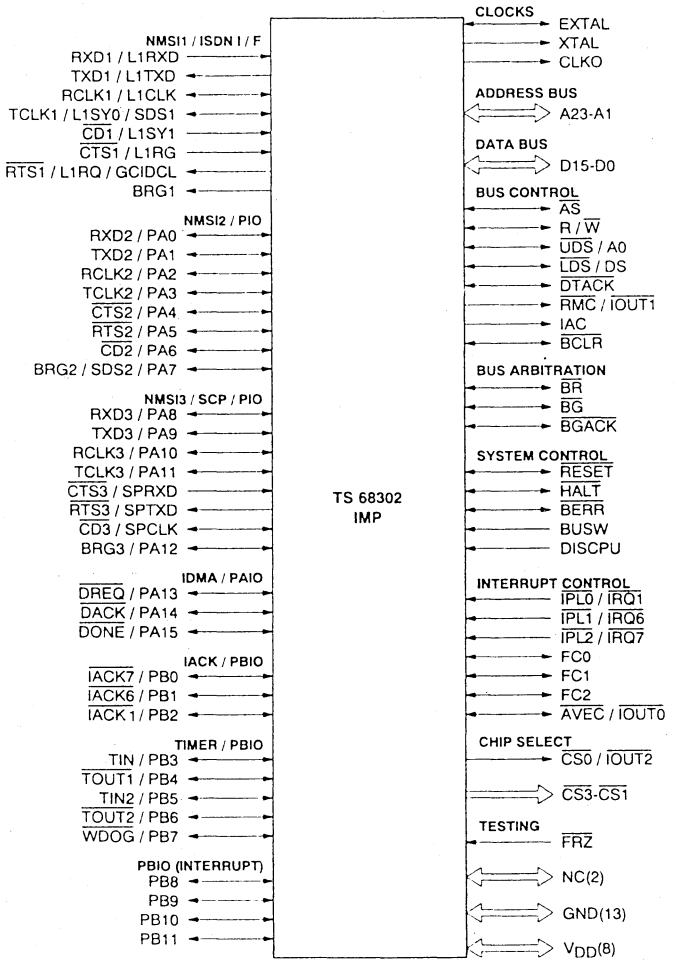


Figure 3 : Functional signal groups.

3 · SIGNAL DESCRIPTIONS

The input and output signals of the TS 68302 are organized into functional groups as shown in Table 1. Refer to TS 68302 Integrated Multiprotocol Processor User's Manual, for detailed information on the TS 68302 signals.

Table 1 · Signal definitions

Functional group	Signals	Num.
Clocks	XTAL, EXTAL, CLKO	3
System Control	$\overline{\text{RESET}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, BUSW, DISCPU	5
Address Bus	A23-A1	23
Data Bus	D15-D0	16
Bus Control	$\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$/A0, $\overline{\text{LDS}}$/$\overline{\text{DS}}$, $\overline{\text{DTACK}}$	5
Bus Control	$\overline{\text{RMC}}$, IAC, $\overline{\text{BCLR}}$	3
Bus Arbitration	$\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BGACK}}$	3
Interrupt Control	$\overline{\text{IPL2}}$-$\overline{\text{IPL0}}$, FC2-FC0, $\overline{\text{AVEC}}$	7
NMSI1/ISDN I/F	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, BRG1	8
NMSI2/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, SDS2	8
NMSI3/SCP/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, PA12	8
IDMA/PAIO	$\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, $\overline{\text{DONE}}$	3
IACK/PBIO	$\overline{\text{IACK7}}$, $\overline{\text{IACK6}}$, $\overline{\text{IACK1}}$	3
Timer/PBIO	TIN2, TIN1, $\overline{\text{TOUT2}}$, $\overline{\text{TOUT1}}$, $\overline{\text{WDOG}}$	5
PBIO	PB11-PB8	4
Chip Select	$\overline{\text{CS3}}$-$\overline{\text{CS0}}$	4
Testing	$\overline{\text{FRZ}}$ (2 Spare)	3
V_{DD}		8
GND		13

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the processor TS 68302, 16.67 MHz, in compliance either with MIL-STD-883 class B or with TCS standards.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38535 : general specifications for microcircuits.
3) Desc Drawing : 5962-93159 (planned).

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38535.

3.2.3 · Package

The macrocircuits are packaged in hermetically sealed ceramic packages which is conform to case outlines of MIL-M-38535 appendix A (when defined) :

- 132-pin Ceramic Pin Grid Array (PGA),
- 132-pin Ceramic Quad Flat Pack (CERQUAD).

The precise case outlines are described on Figures 2.1 and 2.2.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (see Table 2)

Table 2

Symbol	Parameter	Min	Max	Unit
P_D	Power dissipation (typical at 16.67 MHz) - Note 1	53	64	mA
P_D	Power dissipation (typical at 8 MHz) - Note 1	26	31	mA
LP_D	Low power mode dissipation (typical at 16.67 MHz) - Note 2		36	mA
LP_D	Lowest power mode dissipation (typical at 16.67 MHz) - Note 3		32	mA
LP_D	Lowest power mode dissipation (typical at 50 kHz) - Note 4		1	mA

Note 1 : The values shown are typical. The typical value varies as shown, based on how many IMP on-chip peripherals are enabled and the rate at which they are clocked.

Note 2 : LPREC = 0. Divider = 2.

Note 3 : LPREC = 1. Divider = 1024.

Note 4 : The stated frequency must be externally applied to EXTAL only after the IMP has been placed in the lowest power mode with LPREC = 1. The 68000 core is not specified to operate at this frequency, but the rest of the IMP is. In this configuration, the user does not divide the clock internally using the LPCD4-LPCD0 bits in the system control register.

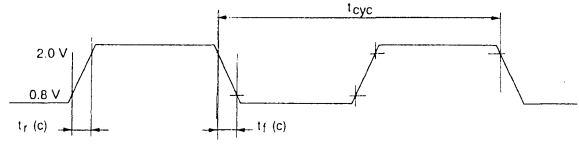
3.3.2 · Recommended condition of use

Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Table 3

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.3	+0.5	V
V_{IH}	High level input voltage	2.4	5.5	V
T_{case}	Operating temperature	−55	+125	°C
$t_r(c)$	Clock rise time - see Figure 4		5	ns
$t_f(c)$	Clock fall time resistance - see Figure 4		5	ns
f_c	Clock frequency - see Figure 4	8	16.67	MHz
t_{cyc}	Cycle time - see Figure 4	60	125	ns

This device contains protective circuitry to protect the inputs against damage due to high static voltages or electrical fields ; however, it is advises that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).



Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 4 : Clock input timing diagram.

3.4 · Thermal characteristics (at 25°C)

Table 4

Package	Symbol	Parameter	Value	Unit
PGA 132	θ_{JA}	Thermal resistance - ceramic junction to ambient	33	°C/W
	θ_{JC}	Thermal resistance - ceramic junction to case	5	°C/W
CERQUAD 132	θ_{JA}	Thermal resistance - ceramic junction to ambient	46	°C/W
	θ_{JC}	Thermal resistance - ceramic junction to case	2	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output pins — user determined

Note : For T_A = 70°C and P_D = 0.5 W @ 12.5 MHz T_j = 88°C.

For most applications $P_{I/O} < 0{,}30\ P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D{}^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or TCS standards.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 · Thomson logo

3.6.2 · Manufacturer's part number

3.6.3 · Class B identification

3.6.4 · Date-code of inspection lot

3.6.5 · ESD identifier if available

3.6.6 · Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each p:oduction lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified. For inspection purpose, refer to relevant specification :

– DESC see § 4.1

Tables 5-6 : Static electrical characteristics for all electrical variants. Test methods refer to IEC 748-2 method number, where existing. See § 5.2.

Tables 7-8 : Dynamic electrical characteristics. Test methods refer to § 5.3 of this specification.

Table 5 · DC electrical characteristics

V_{CC} = 5.0 V_{dc} ± 10 % ; GND = 0 V_{dc} ; T_c = −55°C / +125°C or −40°C / +85°C

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage (except EXTAL)	2.0	V_{DD}	V
V_{IL}	Input low voltage (except EXTAL)	V_{SS} −0.3	0.8	V
V_{CIH}	Input high voltage (EXTAL)	4.0	V_{DD}	V
V_{CIL}	Input low voltage (EXTAL)	V_{SS} −0.3	0.6	V
I_{IN}	Input leakage current		20	µA
C_{IN}	Input capacitance all pins		15	pF
I_{TSI}	Three-state leakage current (2.4 V / 0.5 V)		20	µA
I_{OD}	Open drain leakage current (2.4 V)		20	µA
V_{OH}	Output high voltage (I_{OH} = 400 µA)	V_{DD} −1.0		V

Table 5 · DC electrical characteristics (continued)

V_{CC} = 5.0 V_{dc} ±10 % ; GND = 0 V_{dc} ; T_C = −55°C / +125°C or −40°C / +85°C

Symbol	Parameter	Min	Max	Unit
V_{OL}	Output low voltage			
	(I_{OL} = 3.2 mA) A1-A23, PB0-PB11, FC0-FC3, $\overline{CS0}$-$\overline{CS3}$ IAC, $\overline{AVEC}$, BG, RCLK1, RCLK2, RCLK3, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, $\overline{SDS2}$, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$, $\overline{DREQ}$		0.5	V
	(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, $\overline{RMC}$, DO-D15, $\overline{RESET}$		0.5	V
	(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		0.5	V
	(I_{OL} = 8.9 mA) $\overline{BR}$, $\overline{DONE}$, $\overline{HALT}$, ($\overline{BR}$ as output)		0.5	V
	(I_{OL} = 3.2 mA) CLKO		0.4	V
O_{CLK}	Output drive CLKO		50	pF
O_{GCI}	Output drive ISDN I/F (GCI mode)		150	pF
O_{ALL}	Output drive All other pins		130	pF

Table 6 · DC electrical characteristics · NMSI1 in IDL mode

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	Power		4.5	5.0	5.5	V
V_{SS}	Common		0	0	0	V
T	Temperature	Operating range	−55	25	+125	°C
Input pin characteristics : L1CLK, L1SY1, L1RXD, L1GR						
V_{IL}	Input low level voltage	(% of V_{DD})	−10 %		+20 %	V
V_{IH}	Input high level voltage		V_{DD} −20 %		V_{DD} +10 %	V
I_{IH}	Input low level current	V_{in} = V_{SS}			±10	µA
I_{IH}	Input high level current	V_{in} = V_{DD}			±10	µA
Output pin characteristics : L1TXD, SDS1-SDS2, L1RQ						
V_{OL}	Output low level voltage	I_{OL} = 2.0 mA	0		0.50	V
V_{OH}	Output high level voltage	I_{OH} = 2.0 mA	V_{DD} −0.5		V_{DD}	V

5.3 · Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C or −40°C to +85°C depending on selection see § 11 and V_{CC} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V.

The INTERVAL numbers (NUM) refer to the timing diagrams. See Figures 5 to 25.

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

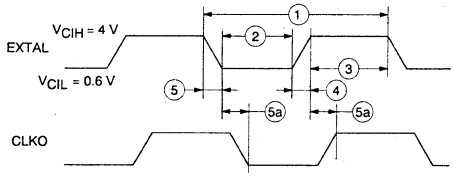


Figure 5 : Clock timing diagram.

Table 7 - AC electrical specifications - Clock timing (see Figure 6)

Num.	Symbol	Parameter	Min	Max	Unit
	f	Frequency of operation	8	16.67	MHz
1	t_{cyc}	Clock period (EXTAL)	60	125	ns
2, 3	t_{CL}, t_{CH}	Clock pulse width (EXTAL)	25	62.5	ns
4, 5	t_{Cr}, t_{Cf}	Clock rise and fall times (EXTAL)		5	ns
5a	t_{CD}	EXTAL to CKLO delay - Notes 1 and 2	2	11	ns

Note 1 : CLKO loading is 50 pF max.

Note 2 : CLKO skew from the rising and falling edges of EXTAL will not differ from each other more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.

Table 8 - AC electrical specifications - IMP bus master cycles (see Figures 6, 7 and 8) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
6	$t_{CHFCADV}$	Clock high to FC, address valid		45	ns
7	t_{CHADZ}	Clock high to address, data bus high impedance (maximum)		50	ns
8	t_{CHAFI}	Clock high to address, FC invalid (minimum)	0		ns
9	t_{CHSL}	Clock high to $\overline{AS}$, $\overline{DS}$ asserted - Note 1	3	30	ns
11	t_{AFCVSL}	Address, FC valid to $\overline{AS}$, $\overline{DS}$ asserted (read) / $\overline{AS}$ asserted (write) Note 2	15		ns
12	t_{CLSH}	Clock low to $\overline{AS}$, $\overline{DS}$ negated - Note 1		30	ns
13	t_{SHAFI}	$\overline{AS}$, $\overline{DS}$ negated to address, FC invalid - Note 2	15		ns
14	t_{SL}	$\overline{AS}$ (and $\overline{DS}$ read) width asserted - Note 2	120		ns
14A	t_{DSL}	$\overline{DS}$ width asserted, write - Note 2	60		ns
15	t_{SH}	$\overline{AS}$, $\overline{DS}$ width negated - Note 2	60		ns
16	t_{CHCZ}	Clock high to control bus high impedance		50	ns
17	t_{SHRH}	$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ invalid - Note 2	15		ns
18	t_{CHRH}	Clock high to R/$\overline{W}$ high - Note 1		30	ns
20	t_{CHRL}	Clock high to R/$\overline{W}$ low - Note 1		30	ns
20A	t_{ASRV}	$\overline{AS}$ asserted to R/$\overline{W}$ low (write) - Notes 2 and 3		10	ns
21	t_{AFCVRL}	Address FC valid to R/$\overline{W}$ low (write) - Note 2	15		ns
22	t_{RLSL}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write) - Note 2	30		ns
23	t_{CLDO}	Clock low to data-out valid		30	ns
25	t_{SHDOI}	$\overline{AS}$, $\overline{DS}$, negated to data-out invalid (write) - Note 2	15		ns
26	t_{DOSL}	Data-out valid to $\overline{DS}$ asserted (write) - Note 2	15		ns
27	t_{DICL}	Data-in valid to clock low (Setup time on read) - Note 4	7		ns
28	t_{SHDAH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{DTACK}$ negated (asynchronous hold) - Note 2	0	110	ns
29	t_{SHDII}	$\overline{AS}$, $\overline{DS}$ negated to data-in invalid (hold time on read)	0		ns
30	t_{SHBEH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{BEER}$ negated	0		ns

6

Table 8 - **AC electrical specifications - IMP bus master cycles (continued)** (see Figures 6, 7 and 8) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
31	t_{DALDI}	$\overline{DTACK}$ asserted to data-in valid (setup time) - Notes 2 and 4		50	ns
32	t_{RHr}, t_{RHf}	$\overline{HALT}$ and $\overline{RESET}$ input transition time		150	ns
33	t_{CHGL}	Clock high to $\overline{BG}$ asserted		30	ns
34	t_{CHGH}	Clock high to $\overline{BG}$ negated		30	ns
35	t_{BRLGL}	$\overline{BR}$ asserted to $\overline{BG}$ asserted	2.5	4.5	clks
36	t_{BRHGH}	$\overline{BR}$ negated to $\overline{BG}$ negated - Note 5	1.5	2.5	clks
37	t_{GALGH}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated	2.5	4.5	clks
37A	t_{GALBRH}	$\overline{BGACK}$ asserted to $\overline{BR}$ negated - Note 6	10	1.5	ns/clks
38	t_{GLZ}	$\overline{BG}$ asserted to control, address, data bus high impedance ($\overline{AS}$ negated)		50	ns
39	t_{GH}	$\overline{BG}$ width negated	1.5		clks
44	t_{SHVPH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{AVEC}$ negated	0	50	ns
46	t_{GAL}	$\overline{BGACK}$ width low	1.5		clks
47	t_{ASI}	Asynchronous input setup time - Note 4	10		ns
48	t_{BELDAL}	$\overline{BERR}$ asserted to $\overline{DTACK}$ asserted - Notes 2 and 7	10		ns
53	t_{CHDOI}	Data-out hold from clock high	0		ns
55	t_{RLDBD}	R/$\overline{W}$ asserted to data bus impedance change	0		ns
56	t_{HRPW}	$\overline{HALT}$/$\overline{RESET}$ pulse width - Note 8	10		clks
57	t_{GASD}	$\overline{BGACK}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven	1.5		clks
57A	t_{GAFD}	$\overline{BGACK}$ negated to FC	1		clks
58	t_{RHSD}	$\overline{BR}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven - Note 5	1		clks
58A	t_{RHFD}	$\overline{BR}$ negated to FC - Note 5	15		clks
60	t_{CHBCL}	Clock high to $\overline{BCLR}$ asserted		30	ns
61	t_{CHBCH}	Clock high to $\overline{BCLR}$ negated - Note 9		30	ns
62	t_{CLRML}	Clock low (S0 falling edge during read) to $\overline{RMC}$ asserted		30	ns
63	t_{CHRMH}	Clock high (S7 rising edge during write) to $\overline{RMC}$ negated		30	ns
64	t_{RMHGL}	$\overline{RMC}$ negated to $\overline{BG}$ asserted - Note 10		30	ns

Note 1 : For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum columns.

Note 2 : Actual value depends on clock period.

Note 3 : When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (± 20 %), subtract 5 ns from the values given in these columns.

Note 4 : If the asynchronous input setup (# 47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (# 31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (# 27) for the following clock cycle.

Note 5 : The TS 68302 will negate $\overline{BG}$ and begin driving the bus if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.

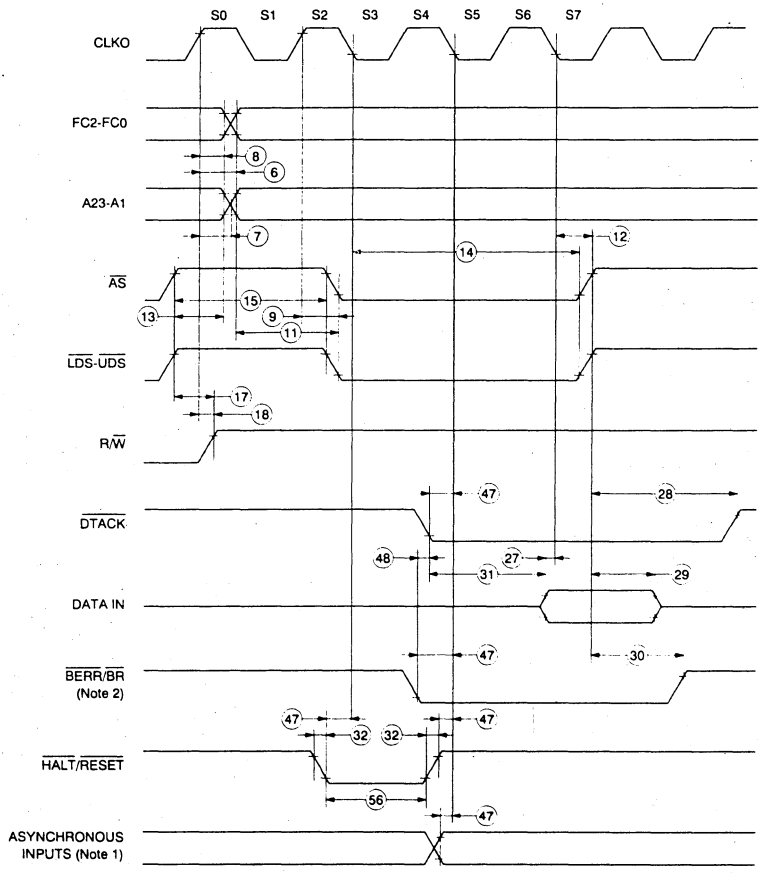
Note 6 : The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.

Note 7 : If # 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, # 48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a synchronous input using the asynchronous input setup time (# 47).

Note 8 : For power-up, the TS 68302 must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up # 56 refers to the minimum pulse width required to reset the processor.

Note 9 : Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.

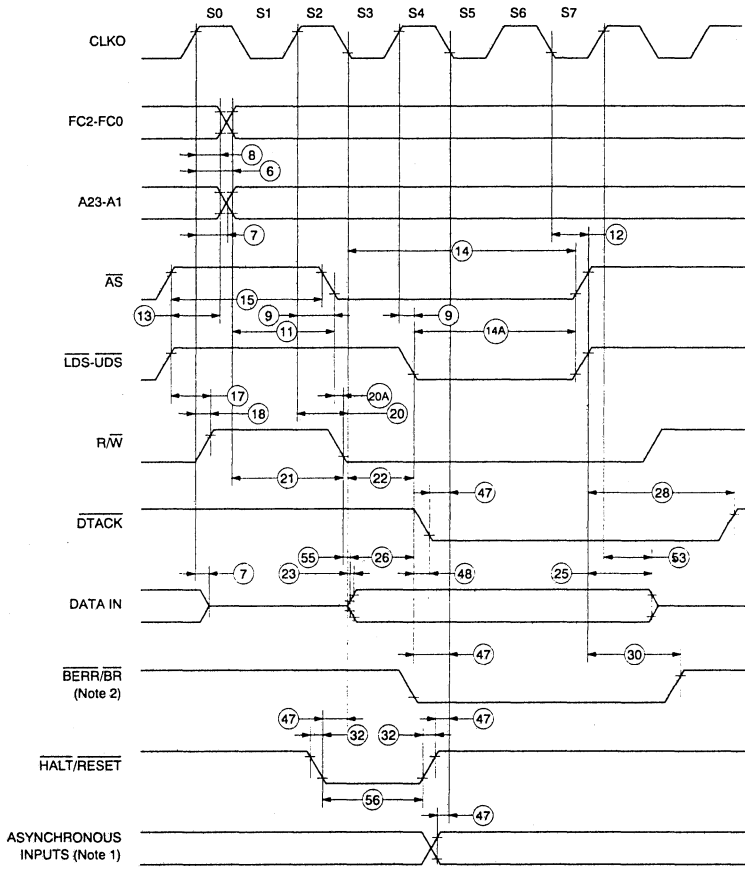
Note 10 : This specification is valid only when the RMCST bit is set in the SCR register.



Notes :

1. Setup time for asymchronous inputs IPL2-IPL0 guarantees their recognition at the next falling edge of the clock
2. BR need fall at this time only to ensure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

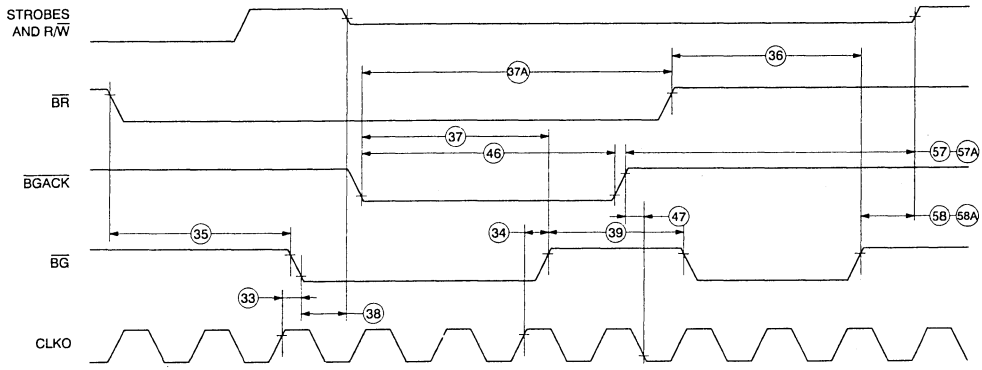
Figure 6 : Read cycle timing diagram.



Notes :

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A)

Figure 7 : Write cycle timing diagram.



Notes : Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, and IPL2-IPL0 guarantees their recognition at the next falling edge of the clock.

Figure 8 : Bus arbitration timing diagram.

Table 9 · AC electrical specifications · DMA (see Figure 9) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
80	t_{REQASI}	DREQ asynchronous setup time - Note 1	15		ns
81	t_{REQL}	DREQ width low - Note 2	2		clk
82	$t_{REQLBRL}$	DREQ low to BR low - Notes 3 and 4		2	clk
83	t_{CHBRL}	Clock high to BR low - Notes 3 and 4		30	ns
84	t_{CHBRZ}	Clock high to BR high impedance - Notes 3 and 4		30	ns
85	t_{BKLBRZ}	BGACK low to BR high impedance - Notes 3 and 4	30		ns
86	t_{CHBKL}	Clock high to BGACK low		30	ns
87	t_{ABHBKL}	AS and BGACK high (the latest one) to BGACK low (when BG is asserted)	1.5	2.5 +30	clk ns
88	t_{BGLBKL}	BG low to BGACK low (no other bus master) Notes 3 and 4	1.5	2.5 +30	clk ns
89	t_{BRHBGH}	BR high impedance to BG high - Notes 3 and 4	0		ns
90	$t_{CLBKLAL}$	Clock on which BGACK low to clock on which AS low	2	2	clk
91	t_{CHBKH}	Clock high to BGACK high		30	ns
92	t_{CLBKZ}	Clock low to BGACK high impedance		15	ns
93	t_{CHACKL}	Clock high to DACK low		30	ns
94	t_{CLACKH}	Clock high to DACK high		30	ns
95	t_{CHDNL}	Clock high to DONE low (output)		30	ns
96	t_{CLDNZ}	Clock low to DONE high impedance		30	ns
97	t_{DNLTCH}	DONE input low to clock high (asynchronous setup)	15		ns

Note 1 : DREQ is sampled on the falling edge of CLK in cycle steal and burst modes.
Note 2 : If # 80 is satified for DREQ, # 81 may be ignored.
Note 3 : BR will not be asserted while AS, HALT, or BERR is asserted.
Note 4 : Specifications are for DISABLE CPU mode only.

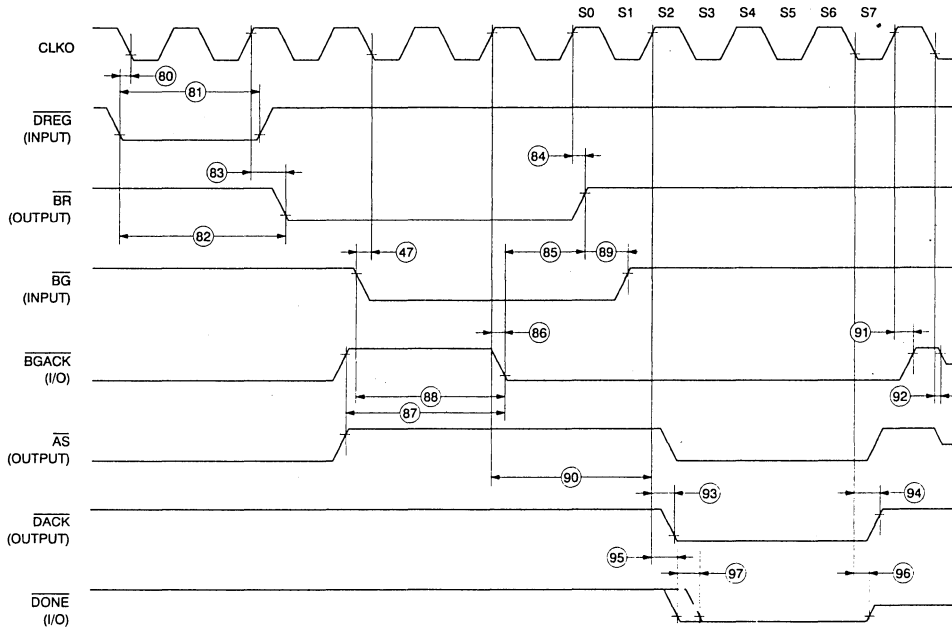


Figure 9 : DMA timing diagram.

Table 10 - AC electrical specifications - External master internal asynchronous read/write cycles (see Figures 10 and 11)
f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
100	t_{RWVDSL}	R/$\overline{W}$ valid to $\overline{DS}$ low	0		ns
101	t_{DSLDIV}	$\overline{DS}$ low to data in valid		30	ns
102	t_{DKLDH}	$\overline{DTACK}$ low to data in hold time	0		ns
103	t_{ASVDSL}	$\overline{AS}$ valid to $\overline{DS}$ low	0		ns
104	t_{DKLDSH}	$\overline{DTACK}$ low to $\overline{DS}$ high	0		ns
105	t_{DSHDKH}	$\overline{DS}$ high to $\overline{DTACK}$ high		45	ns
106	t_{DSIASI}	$\overline{DS}$ inactive to $\overline{AS}$ inactive	0		ns
107	t_{DSHRWH}	$\overline{DS}$ high to R/$\overline{W}$ high	0		ns
108	t_{DSHDZ}	$\overline{DS}$ high to data high impedance		45	ns
108A	t_{DSHDH}	$\overline{DS}$ high to data out hold time	0		ns
109	t_{DSHDOH}	$\overline{DS}$ high to data in hold time - see Note	0		ns
109A	t_{DOVDKL}	Data out valid to $\overline{DTACK}$ low	15		ns

Note : If $\overline{AS}$ is negated before $\overline{DS}$, the data bus could be three-stated (spec 126) before $\overline{DS}$ is negated.

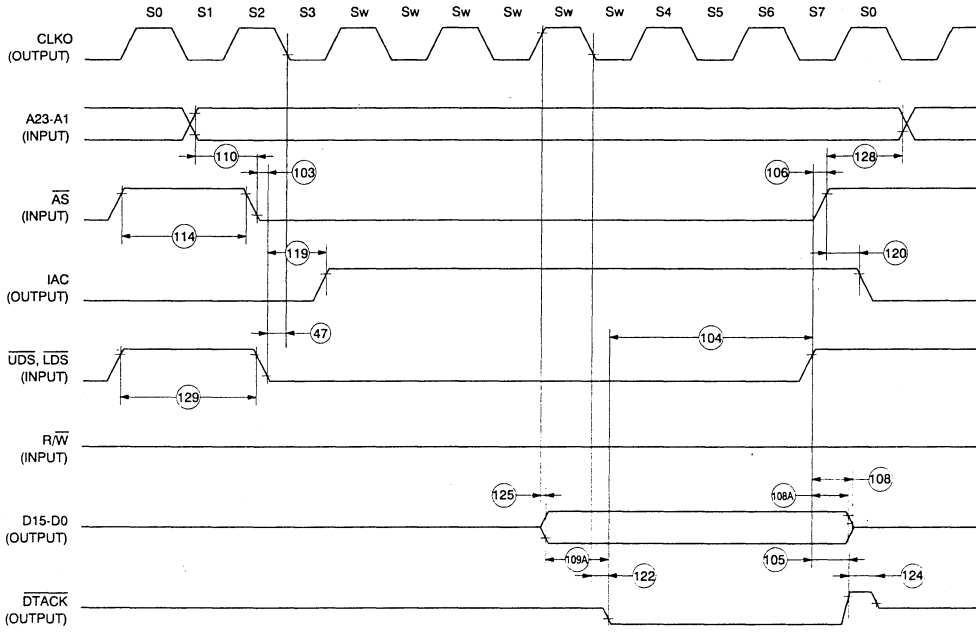


Figure 10 : External master internal asynchronous read cycle timing diagram.

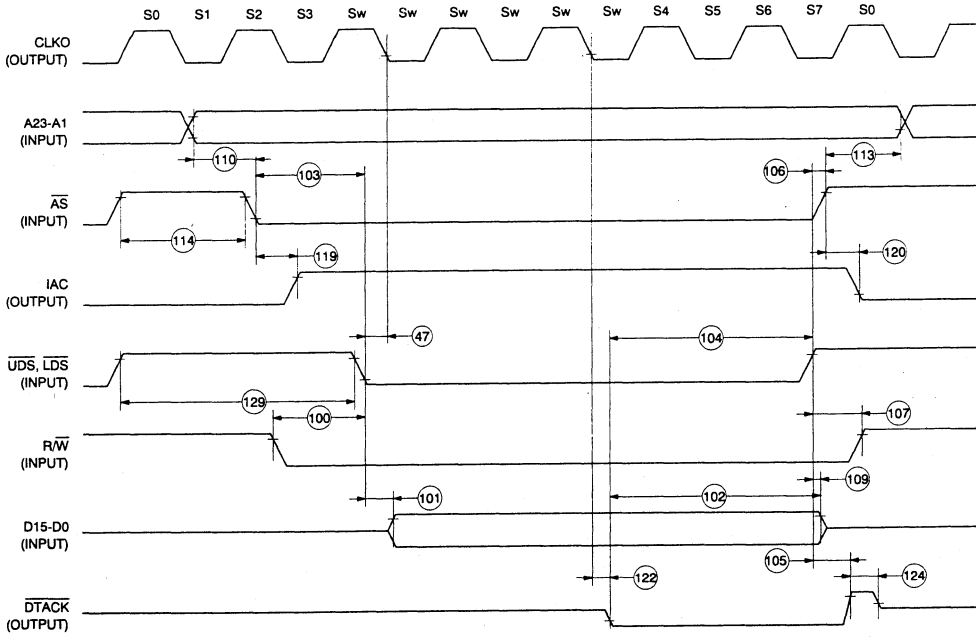


Figure 11 : External master internal asynchronous write cycle timing diagram.

Table 11 - AC electrical specifications - External master internal synchronous read/write cycles
(see Figures 12, 13 and 14) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
110	t_{AVASL}	Address valid to $\overline{AS}$ low	15		ns
111	t_{ASLCH}	$\overline{AS}$ low to clock high	30		ns
112	t_{CLASH}	Clock low to $\overline{AS}$ high		45	ns
113	t_{ASHAH}	$\overline{AS}$ high to adress hold time on write	0		ns
114	t_{ASH}	$\overline{AS}$ inactive time	1		clk
115	t_{SLCH}	$\overline{UDS}/\overline{LDS}$ low to clock high	40		ns
116	t_{CLSH}	Clock low to $\overline{UDS}/\overline{LDS}$ high		45	ns
117	t_{RWVCH}	R/$\overline{W}$ valid to clock high	30		ns
118	t_{CHRWH}	Clock high to R/$\overline{W}$ high		45	ns
119	t_{ASLIAH}	$\overline{AS}$ low to IAC high		40	ns
120	t_{ASHIAL}	$\overline{AS}$ high to IAC low		40	ns
121	t_{ASLDTL}	$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)		45	ns
122	t_{CLDTL}	Clock low to $\overline{DTACK}$ low (1 wait state)		30	ns
123	t_{ASHDTH}	$\overline{AS}$ high to $\overline{DTACK}$ high		45	ns
124	t_{DTHDTZ}	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
125	t_{CHDOV}	Clock high to data out valid		30	ns
126	t_{ASHDZ}	$\overline{AS}$ high to data high impedance		45	ns
127	t_{ASHDOI}	$\overline{AS}$ high to data out hold time	0		ns
128	t_{ASHAI}	$\overline{AS}$ high to address hold time on read	0		ns
129	t_{SH}	$\overline{UDS}/\overline{LDS}$ inactive time	1		clk
130	t_{CLDIV}	Data in valid to clock low	30		ns
131	t_{CLDIH}	Clock low to data in hold time	15		ns

Note : Specifications are valid only when SAM = 1 in the SCR.

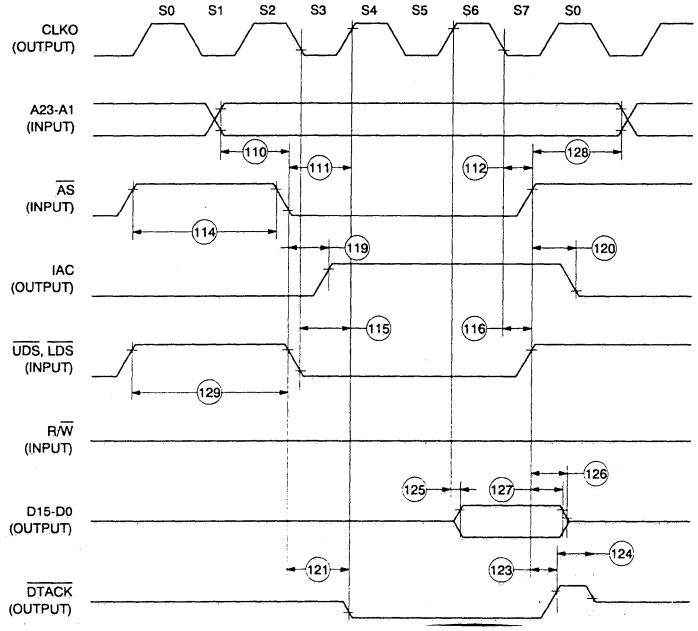


Figure 12 : External master internal synchronous read cycle timing diagram.

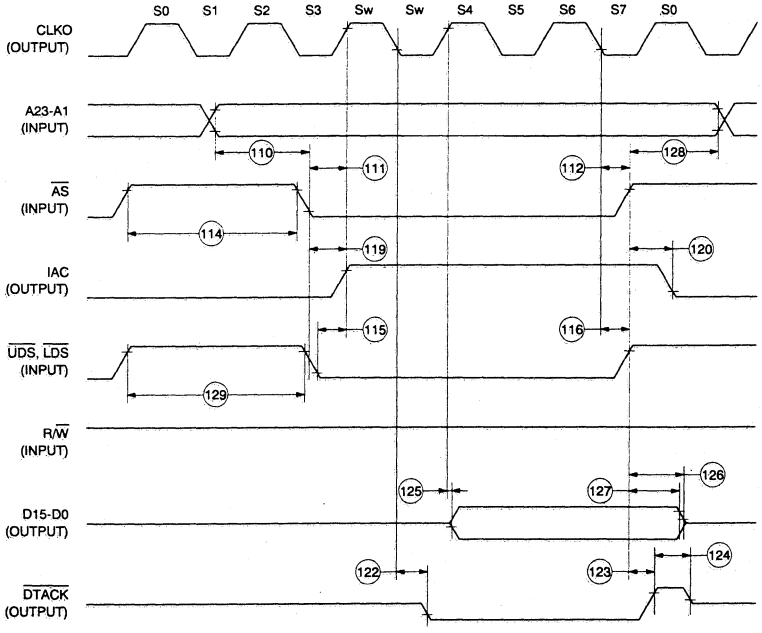


Figure 13 : External master internal synchronous read cycle timing diagram (one wait state).

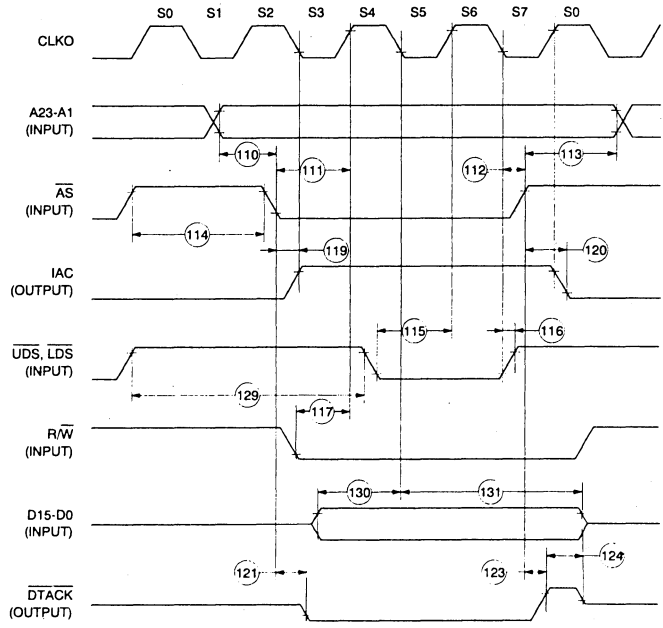


Figure 14 : External master internal synchronous write cycle timing diagram.

Table 12 - AC electrical specifications - Internal master read/write cycles (see Figure 15) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
140	t_{CHIAH}	Clock high to IAC high		40	ns
141	t_{CLIAL}	Clock low to IAC low		40	ns
142	t_{CHDTL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
143	t_{CLDTH}	Clock low to $\overline{DTACK}$ high		40	ns
144	t_{CHDOV}	Clock high to data out valid		30	ns
145	t_{ASHDOH}	$\overline{AS}$ high to data out hold time	0		ns

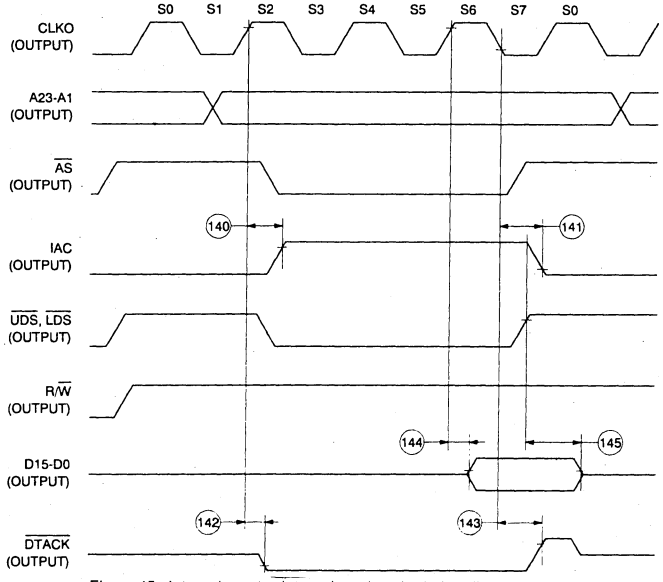


Figure 15 : Internal master internal read cycle timing diagram.

Table 13 - AC electrical specifications - Chip-select timing internal master (see Figure 16) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
150	$t_{CHCSIAKL}$	Clock high to $\overline{CS}$, $\overline{IACK}$ low - Note 1		40	ns
151	$t_{CLCSIAKH}$	Clock low to $\overline{CS}$, $\overline{IACK}$ high - Note 1		40	ns
152	t_{CSH}	$\overline{CS}$ width negated	60		ns
153	t_{CHDTKL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
154	t_{CLDTKL}	Clock low to $\overline{DTACK}$ low (1-6 wait states)		30	ns
155	t_{CLDTKH}	Clock low to $\overline{DTACK}$ high		40	ns
156	t_{CHBERL}	Clock high to $\overline{BERR}$ low - Note 2		40	ns
157	t_{CLBERH}	Clock low to $\overline{BERR}$ high impedance - Note 2		40	ns
158	$t_{DTKHDTKZ}$	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
171	t_{IDHCL}	Input data hold time from S6 low	5		ns
172	t_{CSNDOI}	$\overline{CS}$ negated to data out invalid (write) - Note 3	10		ns
173	t_{AFVCSA}	Address, FC valid to $\overline{CS}$ asserted - Note 3	15		ns
174	t_{CSNAFI}	$\overline{CS}$ negated to address, FC invalid - Note 3	15		ns
175	t_{CSLT}	$\overline{CS}$ low time (0 wait states) - Note 3	120		ns
176	t_{CSNRWI}	$\overline{CS}$ negated to R/$\overline{W}$ invalid - Note 3	10		ns
177	t_{CSARWL}	$\overline{CS}$ asserted to R/$\overline{W}$ low (write) - Note 3		10	ns
178	t_{CSNDII}	$\overline{CS}$ Negated to data in invalid (hold time on read) - Note 3	0		ns

Note 1 : For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
Note 2 : This specification is valid only when the ADCE or WPVE bits in the SCR are set.
Note 3 : Specs 172-178 do not have diagrams. However, similar diagrams for AS are shown as 25-11-13-14-17-20A and 29.

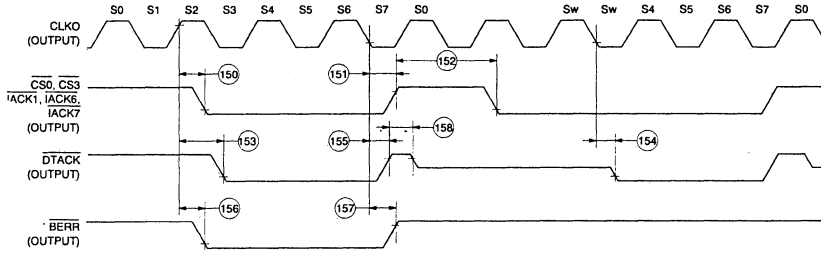


Figure 16 : Internal master chip-select timing diagram.

Table 14 - AC electrical specifications - Chip-select timing external master (see Figure 17) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
154	t_{CLDTKL}	Clock low to $\overline{DTACK}$ low (1-6 wait states)		30	ns
160	t_{ASLCSL}	$\overline{AS}$ low to $\overline{CS}$ low		30	ns
161	t_{ASHCSH}	$\overline{AS}$ high to $\overline{CS}$ high		30	ns
162	t_{AVASL}	Address valid to $\overline{AS}$ low	15		ns
163	t_{RWVASL}	R/$\overline{W}$ valid to $\overline{AS}$ low - Note 1	15		ns
164	t_{ASHAI}	$\overline{AS}$ negated to Address hold time	0		ns
165	$t_{ASLDTKL}$	$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)		45	ns
167	$t_{ASHDTKH}$	$\overline{AS}$ high to $\overline{DTACK}$ high		30	ns
168	$t_{ASLBERL}$	$\overline{AS}$ low to $\overline{BERR}$ low - Note 2		30	ns
169	$t_{ASHBERH}$	$\overline{AS}$ high to $\overline{BERR}$ high - Notes 2 and 3		30	ns

Note 1 : The minimum value must be met to guarantee write protection operation.
Note 2 : This specification is valid when the DCE or WPVE bits in the SCR are set.
Note 3 : Also applies after a timeout of the hardware watchdog.

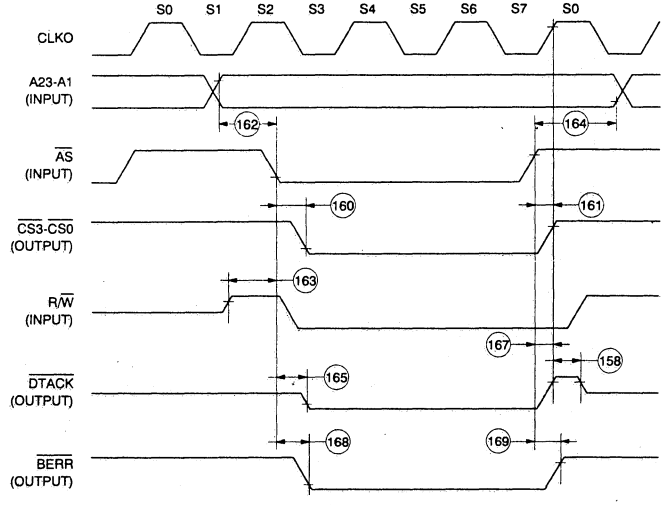


Figure 17 : External master chip-select timing diagram.

Table 15 - AC electrical specifications - Parallel I/O (see Figure 18) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
180	t_{DSU}	Input data setup time (to clock low)	20		ns
181	t_{DH}	Input data hold time (from clock low)	10		ns
182	t_{CHDOV}	Clock high to data out valid (CPU writes data, control, or direction)		35	ns

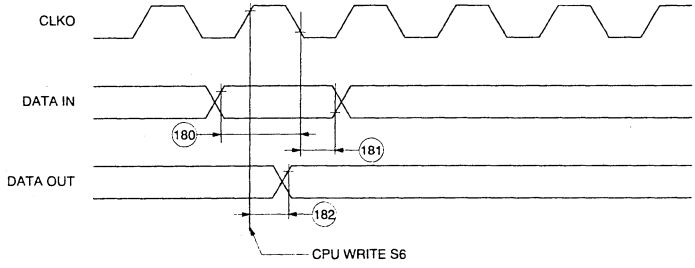


Figure 18 : Parallel I/O data in/data out timing diagram.

Table 16 - AC electrical specifications - Interrupts (see Figure 19) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Unit
190	t_{IPW}	Interrupt pulse width low $\overline{IRQ}$ (edge triggered mode)	50	ns
191	t_{AEMT}	Minimum time between active edges	3	clk
Note : Set up time for the asynchronous inputs IPL2-IPL0 and $\overline{AVEC}$ guarantees their recognition at the next falling edge of the clock.				

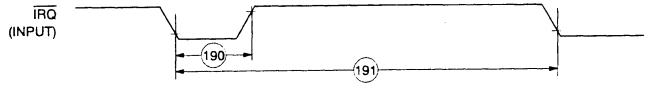


Figure 19 : Interrupts timing diagram.

Table 17 - AC electrical specifications - Timers (see Figure 20) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
200	t_{TPW}	Timer input capture pulse width	50		ns
201	t_{TICLT}	TIN clock low pulse width	50		ns
202	t_{TICHT}	TIN clock high pulse width	1.5		clk
203	t_{cyc}	TIN clock cycle time	3		clk
204	t_{CHTOV}	Clock high to TOUT valid		35	ns
205	t_{FRZSU}	$\overline{FRZ}$ input setup time (to clock high) - see Note	20		ns
206	t_{FRZHT}	$\overline{FRZ}$ input hold time (from clock high)	10		ns
Note : FRZ should be negated during total system reset.					

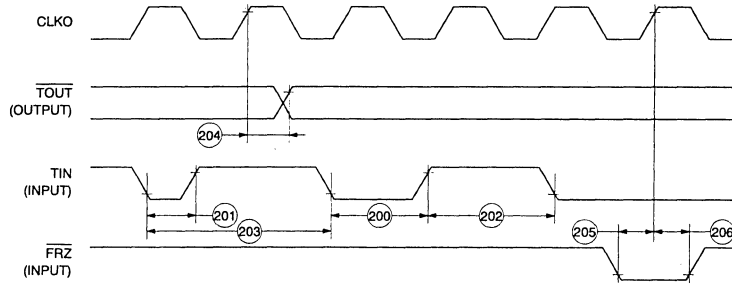


Figure 20 : Timers timing diagram.

Table 18 - AC electrical specifications - Serial communication port (see Figure 21) f = 16.67 MHz

Num.	Parameter	Min	Max	Unit
250	SPCLK clock output period	4	64	clks
251	SPCLK clock output rise/fall time		15	ns
252	Delay from SPCLK to transmit - see Note	0	40	ns
253	SCP receive setup time - see Note	40		ns
254	SPC receive hold time - see Note	10		ns

Note : This also applies when SPCLK is inverted by CI in the SPMODE register.
The enable signals for the slaves may be implemented by the parallel I/O pins.

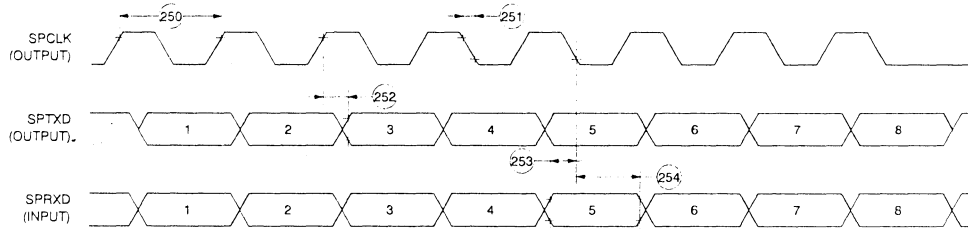


Figure 21 : Serial communication port timing diagram.

Table 19 - AC electrical specifications - IDL timing (see Figure 22) f = 16.67 MHz
All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50 % point of V_{DD}

Num.	Parameter	Min	Max	Unit
260	L1CLK (IDL clock) frequency - Note 1		6.66	MHz
261	L1CLK width low	55		ns
262	L1CLK width high	55		ns
263	L1TXD, L1RQ, SDS1-SDS2 rising/falling time		20	ns
264	L1SY1 (sync) setup time (to L1CLK falling edge)	30		ns
265	L1SY1 (sync) hold time (to L1CLK falling edge)	50		ns
266	L1SY1 (sync) inactive before 4th L1CLK	0		ns
267	L1T x D active delay (from L1CLK rising edge)	0	90	ns

Table 19 - AC electrical specifications - IDL timing (continued) (see Figure 22) f = 16.67 MHz
All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50 % point of V_{DD}

Num.	Parameter	Min	Max	Unit
268	L1T x D to high impedance (from L1CLK rising edge) - Note 2	0	50	ns
269	L1R x D setup time (to L1CLK falling edge)	50		ns
270	L1R x D hold time (from L1CLK falling edge)	50		ns
271	Time between successive IDL syncs	20		L1CLK
272	L1RQ valid before falling edge of L1SY1	1		L1CLK
273	L1GR setup time (to L1SY1 falling edge)	50		ns
274	L1GR hold time (from L1SY1) falling edge)	50		ns
275	SDS1-SDS2 active delay from L1CLK rising edge	10	90	ns
276	SDS1-SDS2 inactive delay from L1CLK falling edge	10	90	ns

Note 1 : The ratio CLK/L1CLK must be greater than 2.5/1.
Note 2 : High impedance is measured at the 30 % and 70 % of V_{DD} points, with the line at $V_{DD}/2$ through 10 K in parallel with 130 pF.

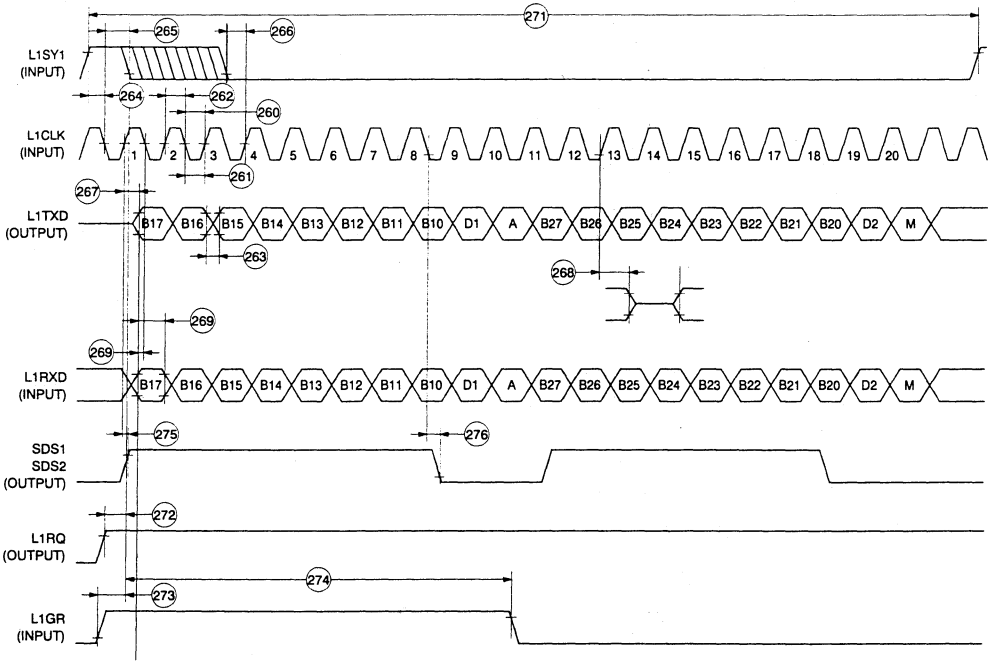


Figure 22 : IDL timing diagram.

Table 20 - AC electrical specifications - GCI timing (see Figure 23) f = 16.67 MHz

GCI supports the NORMAL mode and the GCI channel 0 (GCN0) in MUX mode.
Normal mode uses 512 kHz clock rate (256 K bit rate).
MUX mode uses 256 x n - 3088 Kbits/sec (clock rate is data rate x 2).
The ratio CLK/L1CLK must be greater than 2.5/1.

Num.	Parameter	Min	Max	Unit
	L1CLK GCI clock frequency (normal mode) - Note 1		512	kHz
280	L1CLK clock period normal mode - Note 1	1800	2100	ns
281	L1CLK width low/high normal mode	840	1450	ns
282	L1CLK rise/fall time mormal mode - Note 2	—	—	ns
	L1CLK (GCI clock) period (MUX mode) - Note 1		6.668	MHz
280	L1CLK clock period MUX mode - Note 1	150		ns
281	L1CLK width low/high MUX mode	55		ns
282	L1CLK rise/fall time MUX mode - Note 2	—	—	ns
283	L1SY1 sync setup time to L1CLK falling edge	30		ns
284	L1SY1 sync hold time from L1CLK falling edge	50		ns
285	L1T x D active delay (from L1CLK rising edge) - Note 3	0	100	ns
286	L1T x D active delay (from L1SY1 rising edge) - Note 3	0	100	ns
287	L1R x D setup time to L1CLK rising edge	20		ns
288	L1R x D hold time from L1CLK rising edge	50		ns
289	Time between successive L1SY1 in normal mode SCIT mode	64 192		L1CLK L1CLK
290	SDS1-SDS2 active delay from L1CLK rising edge - Note 4	10	90	ns
291	SDS1-SDS2 active delay from L1SY1 rising edge - Note 4	10	90	ns
292	SDS1-SDS2 inactive delay from L1CLK falling edge	10	90	ns
293	GCIDCL (GCI Data clock) active delay	0	50	ns

Note 1 : The ratio CLK/L1CLK must be greater than 2.5/1.
Note 2 : Schmitt trigger used on input buffer.
Note 3 : Condition C_L = 150 pF. L1T x D becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
Note 4 : SDS1-SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.

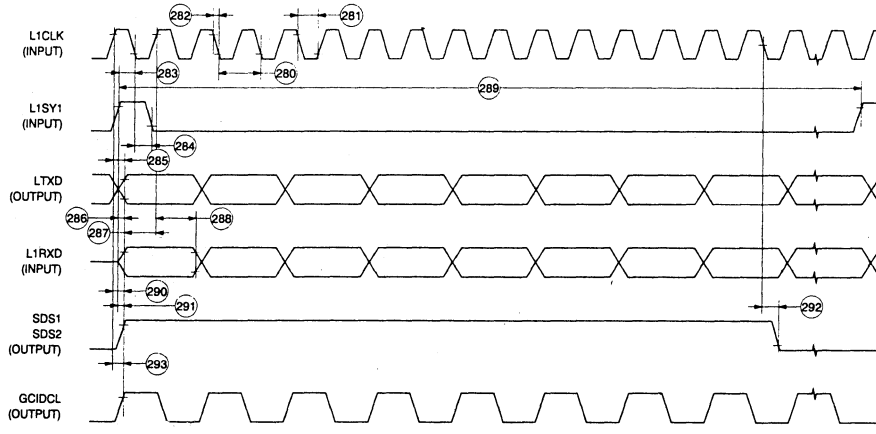


Figure 23 : GSI timing diagram.

Table 21 - AC electrical specifications - PCM timing (see Figure 24) f = 16.67 MHz

There are two syncs types :
Short frame - Sync signals are one clock cycle prior to the data.
Long frame - Sync signals are N-bits that envelope the data, N > 0.

Num.	Parameter	Min	Max	Unit
300	L1CLK (PCM clock) frequency - Note 1		6.66	MHz
301	L1CLK width low/high	55		ns
302	L1SY0-L1SY1 setup time to L1CLK falling edge	20		ns
303	L1SY0-L1SY1 hold time from L1CLK falling edge	40		ns
304	L1SY0-L1SY1 width low	1		L1CLK
305	Time between successive sync signals (short frame)	8		L1CLK
306	L1T x D data valid after L1CLK rising edge - Note 2	0	100	ns
307	L1T x D to high impedance (from L1CLK rising edge)	0	70	ns
308	L1R x D setup time (to L1CLK falling edge) - Note 3	20		ns
309	L1R x D hold time (from L1CLK falling edge) - Note 3	50		ns
310	L1T x D data valid after syncs rising edge (long) - Note 2	0	100	ns
311	L1T x D to high impedance (from L1SY0-L1SY1 falling edge) (long)	0	70	ns

Note 1 : The ratio CLK/TCLK1 must be greater than 2.5/1.
Note 2 : L1T x D becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used.
Note 3 : Specification valid for both sync methods.

6

Table 22 - AC electrical specifications - NMSI timing (see Figure 25)

The NMSI mode uses two clockss, one for receive and one for transmit. Both clocks can be internal or external. When the clock is internal, it is generated by the internal baud rate generator and it is output on L1RXD or L1TXD. All the timing is related to the external clock pin. The timing is specified for NMSI1. It is also valid for NMS12 and NMS13.

Num.	Parameter	Internal clock		External clock		Unit
		Min	Max	Min	Max	
315	RCLK1 and TCLK1 frequency - Note 1		5.12		6.668	MHz
316	RCLK1 and TCLK1 low/high	70		55		ns
317	RCLK1 and TCLK1 rise/fall time - Note 2	—	—	—	—	ns
318	T x D1 active delay from TCLK1 falling edge	0	40	0	70	ns
319	RTS1 active/inactive delay from TCLK1 falling edge	0	40	0	100	ns
320	CTS1 setup time to TCLK1 rising edge	50		10		ns
321	RXD1 setup time to RCLK1 rising edge	50		10		ns
322	RXD1 hold time from RCLK1 rising edge - Note 3	10		50		ns
323	CD1 setup time to RCLK1 rising edge	50		10		ns

Note 1 : The ratio CLK/TCLK1 and CLK/RCLK1 must be greater than 2.5/1 for external clock.
For internal clock the ratio must be greater than 3/1 (the input clock to the baud rate generator may be either CLK or TIM1), in both cases the maximum frequency is limited to 16.67 MHz.
In asynchronous mode (UART), the bit rate is 1/16 of the clock rate.
Note 2 : Schmitt triggers used on input buffers.
Note 3 : Also applies to $\overline{CD}$ hold time when $\overline{CD}$ is used as an external sync in BISYNC or totally transparent mode.

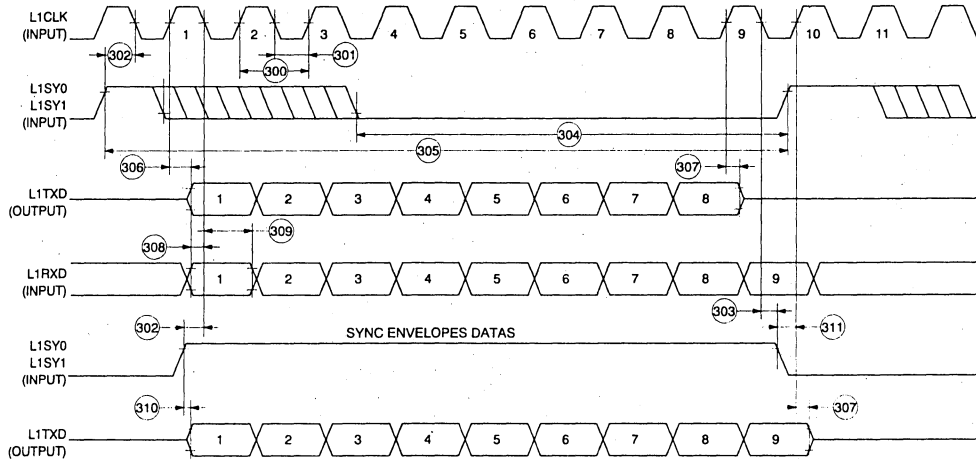


Figure 24 : PCM timing diagram.

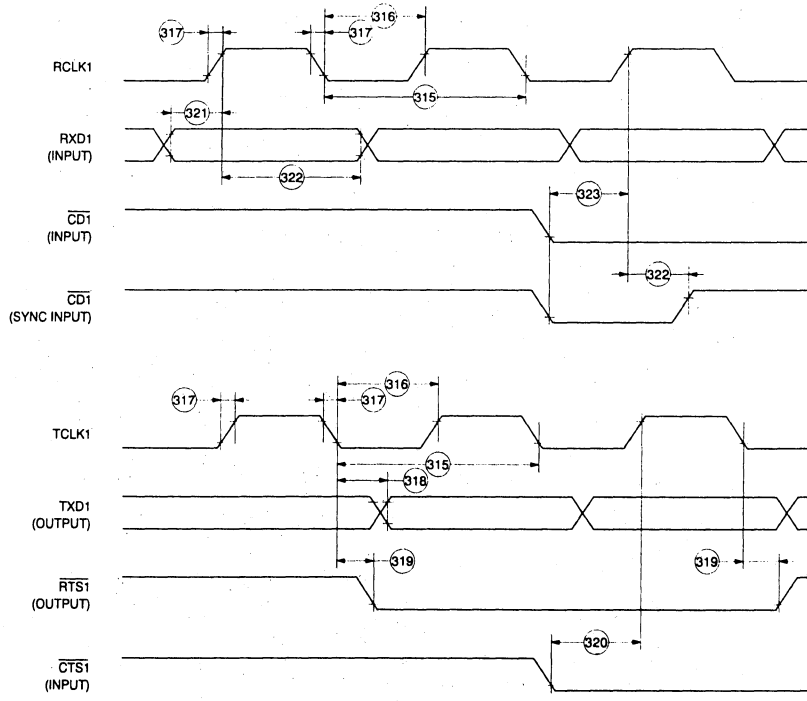


Figure 25 : NMSI timing diagram.

6 · FUNCTIONAL DESCRIPTION

The TS 68302 uses a microprocessor architecture which has peripheral devices connected to the system bus through a dual-port memory. Various parameters, counters, and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffers may be located in this on-chip RAM or in the off-chip system RAM (see Figure 26). Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If an SCC channel's data is programmed to be located in the external RAM, the CP main controller (RISC processor) will program the corresponding DMA channel to perform the required accesses. If the data resides in the on-chip dual-port RAM, then the CP main controller accesses the RAM with one clock cycle access and no arbitration delays.

The buffer memory structure of the TS 68302 can be configured by software to closely match I/O channel requirements. The interrupt structure is also programmable to relieve the on-chip 68000/68008 core from bit manipulation functions for peripherals, allowing the processor to perform application software or protocol processing.

In some cases, the interface to equipment or proprietary networks may require the use of standard control and data signals. For these signals, the TS 68302 can be programmed to use the NMSI mode. This mode is available for one, two, or all three SCC ports; remaining ports may then use one of the multiplexed interface modes : IDL, GCI, or PCM.

6.1 · 68000/68008 core overview

The TS 68302 allows operation either in the full 68000 mode with a 16-bit data bus or in the 68008 mode with an 8-bit data bus.

6.2 · System integration block (SIB)

The TS 68302 has an SIB which simplifies the task of hardware and software design. The IDMA controller eliminates the need for an external DMA controller on the system board. In addition, there is an interrupt controller that can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Similarly, the chip-select signals and wait-state logic eliminate the need to generate these signals externally.

The SIB includes the IDMA controller, interrupt controller, parallel I/O ports, dual-port RAM, three timers, chip-select logic, clock generator, and system control.

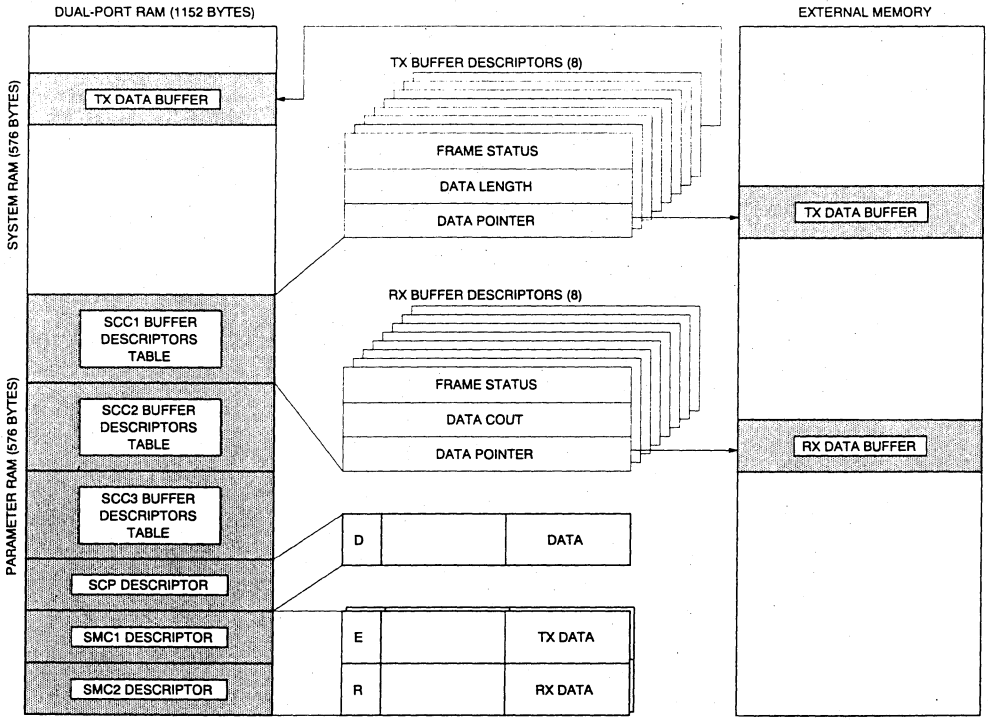


Figure 26 : Buffer memory structure.

6.2.1 · IDMA controller

The TS 68302 has one IDMA channel and six serial DMA channels which operate concurrently with other CPU operations. The IDMA can operate in different modes of data transfer as programmed by the user. The six serial DMA channels for the three full-duplex SCC channels are transparent to the user, implementing bus-cycle-stealing data transfers controlled by the TS 68302's internal RISC controller. These six channels have priority over the separate IDMA channel.

The IDMA controller can transfer data between any combination of memory and I/O devices. In addition, data may be transferred in either byte or word quantities, and the source and destination addresses may be either odd or even. Every IDMA cycle requires between two and four bus cycles, depending on the address boundary and transfer size. If both the source and destination addresses are even, the IDMA fetches one word of data and then immediately deposits it. If either the source or destination block begins on an odd boundary, the transfer takes more bus cycles.

The IDMA features are as follows :

- memory-memory, memory-peripheral, or peripheral-memory data transfers,
- operation with data blocks located at even or odd addresses,
- packing and unpacking of operands,
- fast transfer rates : up to 4 MBps at 16 MHz with no wait states,
- full support of all bus exceptions : halt, bus error, and retry,
- flexible request generation
- two address pointer registers and one counter register,
- three I/O lines for externally requested data transfers,
- asynchronous bus structure with 24-bit address and 8-/16 bit data bus.

6.2.2 · Interrupt controller

The interrupt controller, which manages the priority of internal and external interrupt requests, generates a vector number during the CPU interrupt acknowledge cycle. Nested interrupts are fully supported.

The interrupt controller receives requests from internal sources (INRQ interrupts) such as the timers, the IDMA, the serial controllers, and the parallel I/O pins (port B). The interrupt controller allows the masking of each INRQ interrupt source. When multiple events within a peripheral can cause the interrupt, each of these events is also maskable.

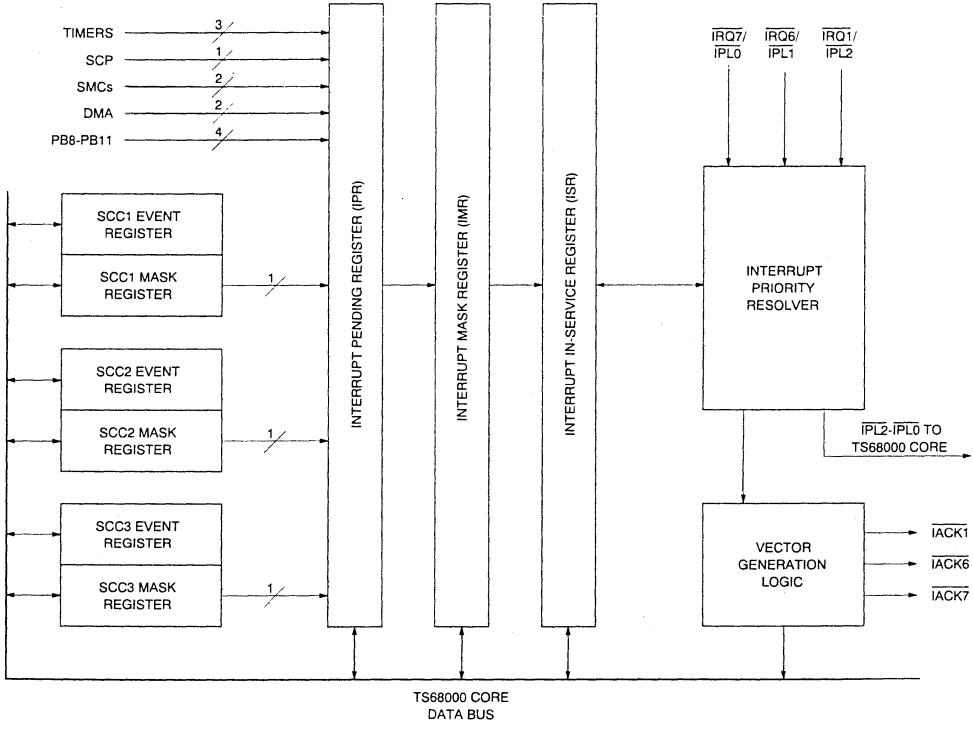


Figure 27 : Interrupt controller block diagram.

The interrupt controller also receives external (EXRQ) requests. EXRQ interrupts are received by the IMP according to the operational mode selected. In the normal operational mode, EXRQ interrupts are encoded onto the IPL lines. In the dedicated operational mode, EXRQ interrupts are presented directly as IRQ7, IRQ6, and IRQ1.

The interrupt controller block diagram is shown in Figure 27. The interrupt controller features are as follows :

- two operational modes : normal and dedicated,
- eighteen priority-organized interrupt sources (internal and external),
- fully nested interrupt environment,
- unique vector number for each internal/external source,
- three selectable interrupt request/interrupt acknowledge pairs.

6.2.3 · Parallel I/O ports

Port A and port B are two general-purpose I/O ports. Each pin in the 16-bit port A may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. Port B has 12 pins. Eight pins may be configured as general-purpose pins or as dedicated peripheral interface pins, and four are general-purpose pins, each with interrupt capability.

6.2.4 · Dual-port RAM

The IMP has 1152 bytes of RAM configured as a dual-port memory. The RAM can be accessed by the internal RISC controller or one of three bus masters : the 68000 core, an external bus master, or the IDMA. All internal bus masters synchronously access the RAM with no wait states. External bus masters can access the RAM and registers synchronously or asynchronously.

The RAM is divided into two parts. There are 576 bytes used as a parameter RAM, which includes pointers, counters, and registers for the serial ports. The other 576 bytes may be used for system RAM, which may include data buffers, or may be used for other purposes such as a no-wait-state cache.

6.3 · Timers

There are three timer units. Two units are identical, general-purpose timers; the third unit can be used to implement a watchdog timer function.

The two general-purpose timers are implemented with a timer mode register (TMR), a timer capture register (TCR), a timer counter (TCN), a timer reference register (TRR), and a timer event register (TER). The TMR contains the prescaler value programmed by the user. The watchdog timer, which has a TRR and TCN, uses a fixed prescaler value.

The timer features are as follows :

- Two general-purpose timer units :
  - maximum period of 16 seconds (at 16.67 MHz),
  - 60-nanosecond resolution (at 16.67 MHz),
  - programmable sources for the clock input,
  - input capture capability,
  - output compare with programmable mode for the output pin,
  - free run and restart modes.
- One watchdog timer with a 16-bit counter and a reference register :
  - maximum period of 16 seconds (at 16.67 MHz),
  - 0.5-millisecond resolution (at 16 MHz),
  - output signal (WDOG),
  - interrupt capability.

6.4 · External chip-select signals and wait-state logic

The TS 68302 has a set of four programmable chip-select signals. Each chip select has an identical structure. For each memory area, an internally generated cycle-termination signal (DTACK) may be defined with up to six wait states to avoid using board space for cycle-termination logic. The four signals may each support four different classes of memory, such as high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. The chip-select and wait-state generation logic is active for all potential bus masters.

6.5 · Clock generator

The TS 68302 has an on-chip clock generator which supplies internal and external high-speed clocks (up to 16.67 MHz). The clock circuitry uses three dedicated pins : EXTAL, XTAL, and CLKO.

6.6 · System control

The IMP system control consists of a system control register (SCR) containing bits for the following system control functions :

- system status and control logic,
- bus arbitration logic with low interrupt latency,
- hardware watchdog,
- low power (standby) modes,
- disable CPU logic (68000),
- freeze control for debugging on-chip peripherals,
- AS control during read-modify-write cycles.

6.6.1 · System control register

The SCR is a 32-bit register that consists of system status and control bits, a bus arbiter control bit, hardware watchdog control bits, low power control bits, and freeze select bits. The eight most significant bits of the SCR report events recognized by the system control logic and set the corresponding bit in the SCR.

The low power modes are used, when no processing is required from the 68000/68008 core, to reduce the system power consumption to its minimum value. The low power modes may be exited by an interrupt from an on-chip peripheral.

6.6.2 · Disable CPU logic (68000)

This control allows an external processor direct connection to the bus and to the IMP's peripherals while the on-chip 68000 core is disabled. Entered during a system reset ($\overline{RESET}$ and $\overline{HALT}$ asserted together), this mode configures the IMP on-chip peripherals for use with other TS 68032 units or other processors and is an effective configuration for systems needing more than three SCCs.

6.6.3 · Freeze control

This control is used to freeze the activity of selected peripherals and to debug systems. The IMP freezes its activity with no new interrupt requests, no memory accesses (internal or external), and no access of the serial channels. The IDMA controller completes any bus cycle in progress and releases bus ownership. No further bus cycles will be started as long as $\overline{FRZ}$ remains asserted.

6.7 · DRAM refresh controller

The CP main (RISC) controller can optionally handle the dynamic RAM (DRAM) refresh task without any intervention from the 68000 core. The refresh request can be generated from an TS 68302 timer, baud rate generator, or externally. The DRAM refresh controller performs a standard 68000-type read cycle at programmable address sequences, with user-provided RAS and CAS generation.

6.8 · Communications processor

The CP in the TS 68302 includes the main controller, six serial DMA channels, three SCCs. an SCP, and two SMCs.

Host software configures each communications channel. as required by the application, to include parameters, baud rates, physical channel interfaces desired, and interrupting conditions. Buffer structures are set up for receive and transmit channels. Up to eight frames may be received or transmitted without host software involvement. Selection of the interrupt interface is also set by register bits in register space of the device.

Data is transmitted and received using the appropriate buffer descriptors and buffer data space for a given channel. The CP operates is a modified polling mode on each channel and buffer descriptor to identify buffers awaiting transmission and channels requiring servicing. The user sets a bit in the buffer descriptor of a transmit frame ; when the CP polls and detects this bit, it will begin transmission. Generally, no other action is required to accomplish transmission.

6.8.1 · Main controller

The main controller is a microcode RISC processor that services all the serial channels. The main controller transfers data between the serial channels and internal/external RAM, executes host commands, and generates interrupts to the interrupt controller.

Data is transferred from the serial channel to the dual-port RAM or to the external memory through the peripheral bus. If data is transferred between the SCC channels and external memory, the main controller uses up to six serial DMA channels for the transfer. The main controller also controls all character and address comparison and cyclic redundancy check (CRC) generation and checking.

The execution unit includes the arithmectic logic unit (ALU), which performs arithmetic and logic operations on the registers.

6.8.2 · Serial Communication Controllers

The TS 68302 has three independent SCCs. Each SCC can be configured to implement different protocols – for example, to perform a gateway function or to interface to an ISDN basic rate channel. To simplify programming, each protocol implementation uses identical data structures.

Five protocols are supported : high-level data link control (HDLC), binary synchronous communication (BISYNC), synchronous/asynchronous digital data communications message protocol (DDCMP), V.110, universal asynchronous receiver transmitter (UART), and a fully transparent mode. To aid system diagnostics, each SCC may be configured to operate in either an echo or loopback mode. In echo mode, the IMP retransmits any signals received; in loopback mode, the IMP locally receives signals originating from itself.

The clock pins (RCLK, TCLK) for each SCC can be programmed for either an external or internal source, with user-programmable baud rates available for each SCC channel.

Each SCC also supports the standard modem control signals : request to send ($\overline{RTS}$), clear to send ($\overline{CTS}$), and carrier detect ($\overline{CD}$). Other modem signals may be provided through the parallel I/O pins.

The SCC features are as follows :

- programmable baud rate generator driven by the internal or external clock,
- data may be clocked by the programmable baud rate generator or directly by an external clock,
- provides modem signals $\overline{RTS}$, $\overline{CTS}$, and $\overline{CD}$,
- Full-duplex operation,
- Automatic echo mode,

- Local loopback mode,
- Baud rate generator outputs available externally.

The SCC HDLC mode key features are as follows :
- flexible data buffers with multiple buffers per frame allowed,
- separate interrupts for frames and buffers (receive and transmit),
- four address comparison registers with mask,
- maintenance of five 16-bit error counters,
- flag/abort/idle generation/detection,
- zero insertion/deletion,
- NRZ/NRZI data encoding,
- 16-bit or 32-bit CRC-CCITT generation/checking,
- detection of non-octet aligned frames,
- detection of frames that are too long,
- programmable 0-15 FLAGS between successive frames,
- automatic retransmission in case of collision.

The SCC BISYNC mode key features are as follows :
- flexible data buffers,
- eight control character recognition registers,
- automatic SYNC1 and SYNC2 detection,
- SYNC/DLE stripping and insertion,
- CRC-16 and LRC generation/checking.
- parity (VRC) generation/checking.
- supports BISYNC transparent operation (use of DLE characters),
- supports promiscuous (totally transparent) reception and transmission,
- maintains parity error counter,
- external SYNC support.
- reverse data mode.

The SCC DDCMP mode key features are as follows :
- synchronous or asynchronous DDCMP links supported,
- flexible data buffers,
- four address comparison registers with mask,
- automatic frame synchronization,
- automatic message synchronization by searching for SOH, ENQ, or DLE,
- CRC-16 generation/checking,
- NRZ/NRZI data encoding,
- maintenance of four 16-bit error counters.

The SCC V.110 mode key features are as follows :
- provides synchronization and reception of 80-bit frames,
- automatic detection of framing errors,
- allows transmission of the 80-bit frame.

The SCC UART mode key features are as follows :
- flexible message-oriented data buffers,
- multidrop operation,
- receiver wakeup on idle line or address mode,
- eight control character comparison registers,
- two address comparison registers,
- four 16-bit error counters,

- programmable data length (7-8 bits),
- programmable 1 or 2 stop bits with fractional stop bits,
- even/odd/force/no parity generation,
- even/odd/no parity check,
- frame error, noise error, break, and idle detection,
- transmits idle and break sequences,
- freeze transmission option,
- maintenance of four 16-bit error counters,
- provides asynchronous link over which DDCMP may be used,
- Flow control character transmission supported.

6.8.3 · Serial communication port

The SCP is a full-duplex, synchronous, character-oriented channel which provides a three-wire interface (TXD, RXD, and clock). The SCP consists of independent transmitter and receiver sections and a common SCP clock generator. The transmitter and receiver section use the same clock, which is derived from the main clock by an on-chip baud rate generator. The TS 68302 is an SCP master, generating both the enable and the clock signals. The enable signals may be generated by the general-purpose I/O pins.

The SCP allows the TS 68302 to communicate with a variety of serial devices for the exchange of status and control information using a subset of the Motorola serial peripheral interface (SPI). Such devices may include industry-standard CODECs and other microcontrollers and peripherals.

The SCP can be configured to operate in a local loopback mode, which is useful for diagnostic functions. The receiver and the transmitter operate normally in these modes.

The SCP features are as follows :

- three-wire interface (SPTXD, SPRXD, and SPCLK),
- full-duplex operation,
- clock rate up to 4.096 MHz,
- programmable baud rate generator,
- local loopback capacibility for testing purposes.

6.8.4 · Serial management controllers

The SMCs are two synchronous, full-duplex ports that may be configured to operate in either IDL or GCI mode to handle the maintenance and control portions of these interfaces. The SMC ports are not used in PCM or NMSI modes. The SMC features are as follows :

- two modes of operation - IDL and GCI,
- local loopback capability for testing purposes,
- full-duplex operation,
- SMC1 in GCI mode detects collisions on the D channel.

6.8.5 · Serial channels physical interface

The serial channels physical interface connects the physical layer serial lines and the serial controllers (three SCCs and two SMCs). The interface implements both the routing and the time-division multiplexing for the full ISDN bandwidth. It supports four buses : IDL, GCI, PCM, and NMSI (a nonmultiplexed modem interface). The multiplexed modes (IDL, GCI, and PCM) also allow multiplie channels (e.g., ISDN B channels) or user-defined subchannels to be assigned to a given SCC. The serial interface also supports two testing modes : echo and loopback.

For the IDL and GCI buses, support of management functions in the frame structure is provided by the SCP or SMCs, respectively. Refer to Figure 28 for the serial channels physical interface block diagram.

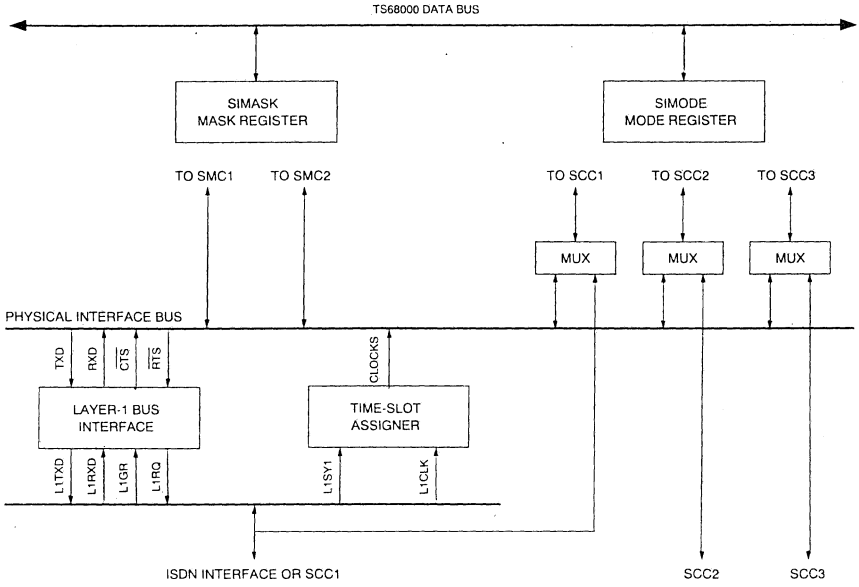


Figure 28 : Serial channels physical interface block diagram.

6

7 - PREPARATION FOR DELIVERY

7.1 - Packaging

Microcircuit are prepared for delivery in accordance with MIL-STD-1835.

7.2 - Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or TCS standards and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

8 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

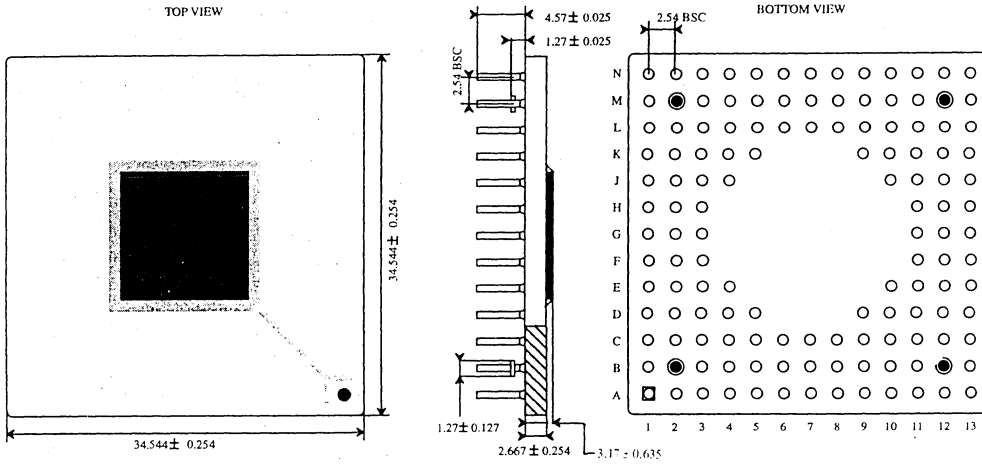
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

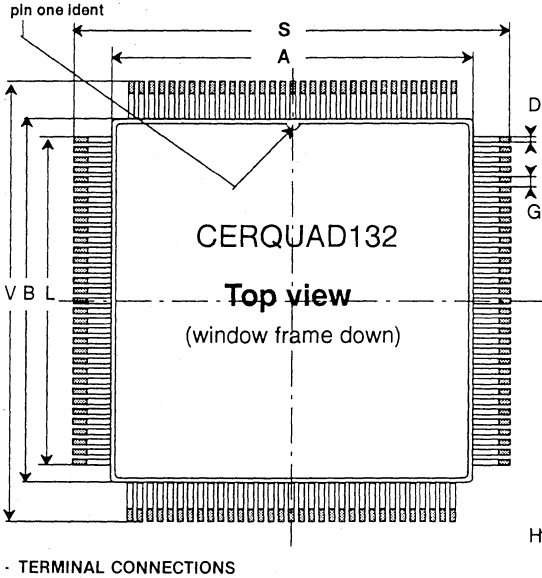
f) Maintain relative humidity above 50 %, if practical.

9 - PACKAGE MECHANICAL DATA

9.1 - 132 pins - Ceramic Pin Grid Array (in millimeter)



9.2 - 132 pins - Ceramic Quad Flat Pack / CERQUAD



DIM	Milimeters MIN	MAX	Inches MIN	MAX
A	21.85	22.86	0.86	0.90
B	21.85	22.86	0.86	0.90
C	3.94	4.52	0.155	0.178
D	0.204	0.292	0.008	0.0115
G	0 64	BSC	0.025	BSC
H	0.5	1.0	0.019	0.039
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
L	20.32	REF	0.800	REF
R	0.64	–	0.025	–
S	27.26	27.6	1.073	1.087
V	27.26	27.6	1.073	1.087

10 - TERMINAL CONNECTIONS

10.1 - 132 pins - Ceramic Pin Grid Array

See Figure 2.1 page 4.

10.2 - 132 pins - Ceramic Quad Flat Pack / CERQUAD

See Figure 2.2 page 4.

11 · ORDERING INFORMATION

11.1 · Hi-REL product

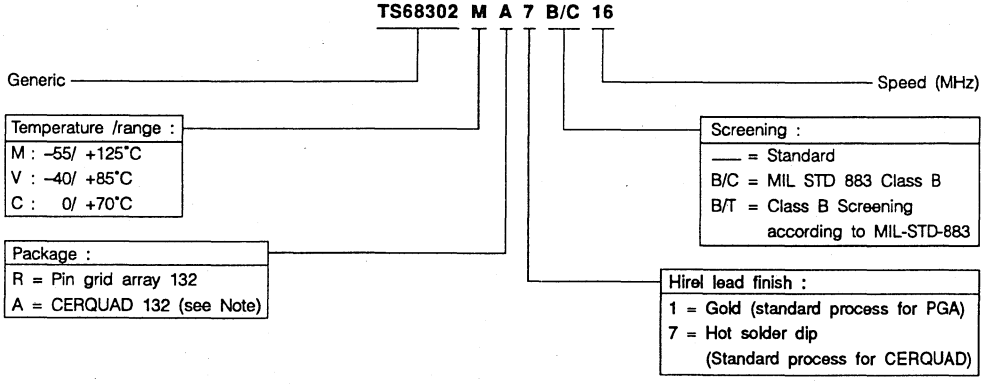
Commercial TCS Part-Number Note 1	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68302MRB/C16	MIL-STD-883	PGA 132	−55 / +125	16.67	–
TS68302MA7B/C16	MIL-STD-883	CERQUAD 132 Note 2	−55 / +125	16.67	–
TS68302DESC01XC	DESC	PGA 132	−55 / +125	16.67	5962-93159
TS68302DESC01YA	DESC	CERQUAD 132 Note 2	−55 / +125	16.67	5962-93159

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : Gullwing leads.

11.2 · Standard product

Commercial TCS Part-Number Note 1	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68302VR16	TCS Standard	PGA 132	−40 / +85	16.67	Internal
TS68302MR16	TCS Standard	PGA 132	−55 / +125	16.67	Internal
TS68302VA16	TCS Standard	CERQUAD 132 Note 2	−40 / +85	16.67	Internal
TS68302MA16	TCS Standard	CERQUAD 132 Note 2	−55 / +125	16.67	Internal

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : Gullwing leads.



TS 68332

ADVANCED INFORMATION

HIGH-PERFORMANCE 32-BIT INTEGRATED MICROCONTROLLER

DESCRIPTION

The TS 68332 is a 32-bit microcontroller, combining high-performance data manipulation capabilities with powerful peripheral subsystems. The TS 68332 is the first member of the 68300 family of modular embedded controllers featuring fully static, high-speed complementary metal-oxyde semiconductor technology. Based on the powerful TS 68020, the CPU32 instruction processing module provides enhanced system performance and utilizes the extensive software base of the 68000 family.

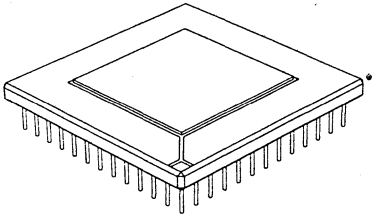
MAIN FEATURES

- Low-power operation including special STOP mode.
- Frequency : 16.78 MHz at 5 V supply, software programmable.
- Technology : 1 μ high-density complementary metal-oxide semiconductor (HCMOS), static design.
- Package : 132-pin Ceramic Leaded Chip Carrier (CERQUAD) and 132-pin Ceramic Pin Grid Array (PGA).
- Modular architecture in a single chip.
- CPU : 32-bit 68000 family (upward object-code compatible with the 68010).
- New instructions for controller applications.
- Intelligent 16-bit timer :
  - 16 independent, programmable channels,
  - Any channel can perform any time function (for example input capture, output compare, pulse width modulation, etc.),
  - Two timer count registers with 2-bit programmable prescalers,
  - Selectable channel priority levels,
  - Reduced CPU intervention,
  - RISC like CPU within the TPU.
- Two serial I/O subsystems :
  - Enhanced 68HC11-type serial communications interface (SCI) universal asynchronous receiver transmitter (UART) with parity,
  - Enhanced 68HC11-type serial peripheral interface with I/O RAM Queue (QSPI).
- On-chip memory : 2 K bytes standby RAM.
- On-chip, programmable, chip-select logic
  - Up to 12 signals for memory and peripheral interface with I/O select.
- System failure protection :
  - 68HC11-type Computer Operating Properly (COP) watchdog timer,
  - 68HC11-type periodic interrupt timer,
  - 68000 family spurious interrupt, HALT, and bus time-out monitors.
- Up to 48 discrete I/O pins.

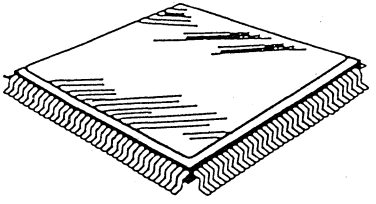
SCREENING / QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 (class B).
- DESC 5962-91501 (planned).
- or according to TCS standard.



R Suffix
PGA 132
Ceramic Pin Grid Array



A Suffix
CERQUAD 132
Ceramic Leaded Chip Carrier

See the ordering information page 36.
Pin connection : see page 4.

6

SUMMARY

A · GENERAL DESCRIPTION

1 · INTRODUCTION

Figure 1 is a block diagram of the TS 68332 showing the major components. The pin descriptions are provided in Table 1. The TS 68332 contains intelligent peripheral modules such as the time processor unit (TPU), which provides 16 microcoded channels for performing time-related activities from simple input capture or output compare to complicated motor control or pulse width modulation. High-speed serial communications are provided by the queued serial module (QSM) with synchronous and asynchronous protocols available. Two kilobytes of fully static standby RAM allow fast two-cycle access for system and data stacks and variable storage with provision for battery back-up. There is a System Integration Module (SIM) which includes twelve chip selects to enhance system integration for fast external memory or peripheral access. The powerful 32-bit CPU (CPU 32) is based on the industry-standard TS 68020. These modules are connected on chip via the intermodule bus (IMB) and provide reduced system part count, size, cost of implementation and increased reliability.

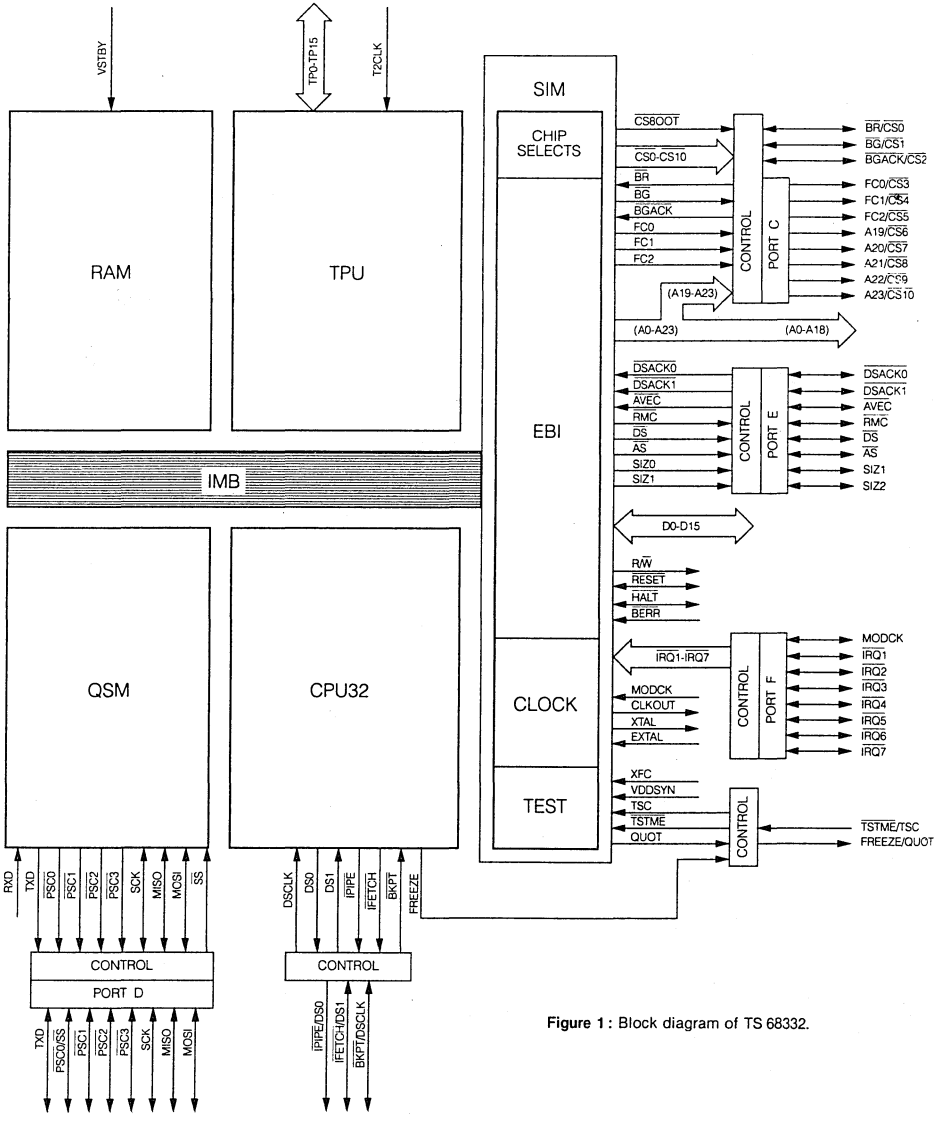


Figure 1 : Block diagram of TS 68332.

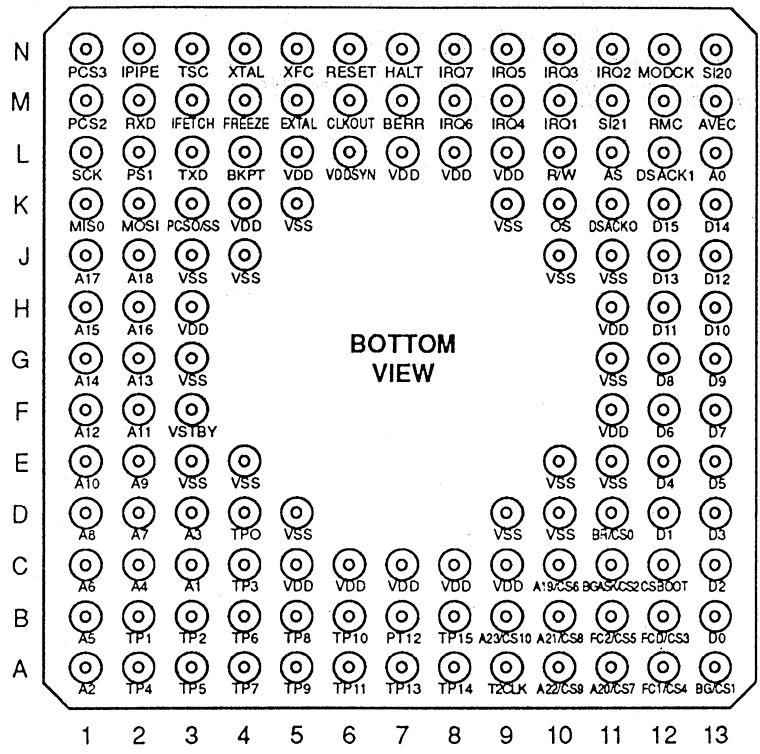


Figure 2.1 : PGA terminal designation.

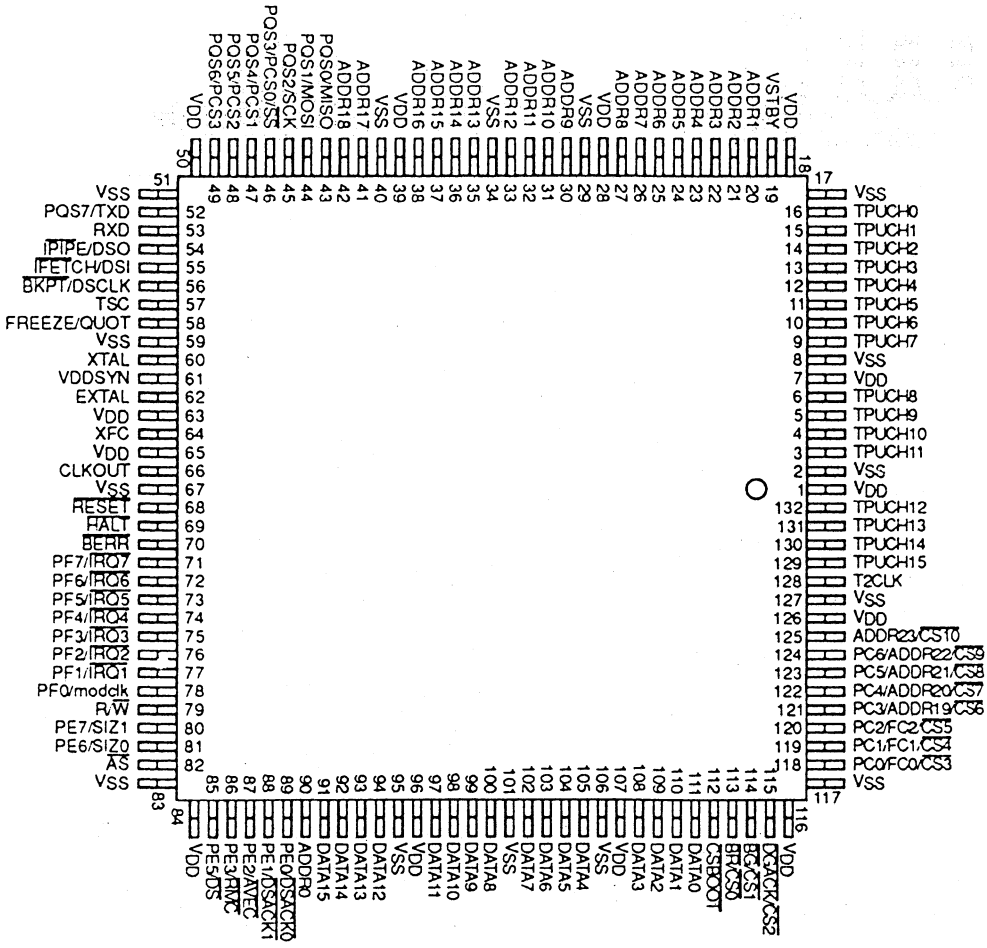


Figure 2.2: CERQUAD terminal designation.

2 · SIGNAL DESCRIPTION

Figure 1 illustrates the functional signal groups and Table 1 lists the signals and their function.

Table 1 · Signal index

Signal name	Mnemonic	Function
Address Bus	A23-A0	24-bit address bus
Data Bus	D15-D0	16-bit data bus used to transfer byte or word data per bus cycle
Data Bus Function Codes	FC2-FC0	Identify the processor state and the address space of the current bus cycle
Boot Chip Select	$\overline{\text{CSBOOT}}$	Chip-select boot statup ROM containing user's reset vector and initialisation program
Chip selects	$\overline{\text{CS10}}$-$\overline{\text{CS0}}$	Enables peripherals at programmed addresses
Bus Request	$\overline{\text{BR}}$	Indicates that an external device requires bus mastership
Bus Grant	$\overline{\text{BG}}$	Indicates that current bus cycle is complete and the TS 68332 has relinquished the bus
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	Indicates that an external device has assumed bus mastership
Data and Size Acknowledgement	$\overline{\text{DSACK1}}$, $\overline{\text{DSACK0}}$	Provides asynchronous data transfers and dynamic bus sizing
Autovector	$\overline{\text{AVEC}}$	Requests an automatic vector during an interrupt acknowledge cycle
Read-Modify-Write Cycle	$\overline{\text{RMC}}$	Identifies the bus cycle as part of an indivisible read-modify-write cycle
Address Strobe	$\overline{\text{AS}}$	Indicates that a valid address is on the address bus
Data Strobe	$\overline{\text{DS}}$	During a read cycle, DS indicates that an external device should place valid data on the data bus. During a write cycle, DS indicates that valid data is on the data bus
Size	SIZ1 - SIZ0	Indicates the number of bytes remaining to be transferred for this cycle
Read/Write	R/$\overline{\text{W}}$	Indicates the direction of data transfer on the bus
Interrupt Request Level	$\overline{\text{IRQ7}}$ - $\overline{\text{IRQ0}}$	Provides an interrupt priority level to the CPU
Reset	$\overline{\text{RESET}}$	System reset
Halt	$\overline{\text{HALT}}$	Suspend external bus activity
Bus Error	$\overline{\text{BERR}}$	Indicates that an erroneous bus operation is being attempted
System Clockout	CLKOUT	Internal system clock
Crystal Oscillator	EXTAL, XTAL	Connection for an external crystal to the internal oscillator circuit
External Filter Capacitor	XFC	Connection pin for an external capacitor to filter the circuit of the phase-locked loop
Clock Mode Select	MODCK	Selects the source of the internal system clock
Instruction Fetch	$\overline{\text{IFETCH}}$	Indicates when the CPU is performing an instruction word prefetch and when the instruction pipeline has been flushed
Instruction Pipe	$\overline{\text{IPIPE}}$	Used to track movement of words through the instruction pipeline
Breakpoint	$\overline{\text{BKPT}}$	Signals a hardware breakpoint to the CPU

Table 1 - Signal index (continued)

Signal name	Mnemonic	Function
Freeze	FREEZE	Indicates that the CPU has acknowledged a breakpoint
Quotient Out	QUOT	Serial I/O and clock for background debug mode
Test Mode Enable	$\overline{\text{TSTME}}$	Hardware enable for test mode
Three-State Control	TSC	Places all output drivers in a high-impedance state
Development Serial In, Out, Clock	DSI, DSO, DSCLK	Serial I/O and clock for background debug mode
TPU Channels	TP15-TP0	TPU channel input/output Serial I/O and clock for background debug mode
TPU Clock In	T2CLK	External clock source to the TPU
SCI Receive Data	RXD	Serial input to the SCI
SCI Transmit Data	TXD	Serial output from the SCI
Peripheral Chip Select	$\overline{\text{PCS3}}$ - $\overline{\text{PCS0}}$	QSPI peripheral chip selects
Slave Select	$\overline{\text{SS}}$	Places the QSPI in slave mode
QSPI Serial Clock	SCK	Furnishes the clock from the QSPI in master mode or to the QSPI in slave mode
Master-In Slave-Out	MISO	Furnishes serial input to the QSPI in master mode, and serial output from the QSPI in slave mode
Master-Out Slave-In	MOSI	Furnishes serial output from the QSPI in master mode, and serial input to the QSPI in slave mode
Standby RAM	V_{STBY}	Power supply for RAM
Synchronizer Power	V_{DDSYN}	Power supply to VCO
System Power Supply and Return	V_{DD}, V_{SS}	Power supply and return to the MCU

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the microcontroller 68332 at 16.78 MHz, in compliance either with MIL-STD-883 class B or TCS standard.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-I-38535 : general specifications for microcircuits.
3) Desc Drawing : 5962-91501.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in Figures 2.1 and 2.2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-853.

3.2.3 - Package

The macrocircuits are packaged in hermetically sealed ceramic packages which are conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 132-PIN SQ.PGA UP PAE outline
- 132-PIN Ceramic CERQUAD

The precise case outlines are described in § 9.1 and § 9.2.

3.3 - Electrical characteristics

Absolute maximum ratings (see Table 2)

The following ratings define the conditions under which the device operates without damage. Sections of the device may not operate normally while being exposed to the electrical extremes and contains circuitry to protect against damage from high static voltages or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either V_{SS} or V_{DD}).

Table 2

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{DD}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_{dmax}	Max Power dissipation	Low power operation		600	mW
		Stand by mode		500	mW
T_{case}	Operating temperature	M suffix	−55	+125	°C
		V suffix	−40	+85	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+160	°C
T_{leads}	Lead temperature	Max 5 sec. soldering		+270	°C

3.4 · Thermal characteristics (at 25°C)

Table 3

Package	Symbol	Parameter	Value	Unit
PGA 132	θ_{J-A}	Thermal resistance ceramic Junction-to-Ambient	TBD	°C/W
	θ_{J-C}	Thermal resistance ceramic Junction-to-Case	10	°C/W
CERQUAD 132	θ_{J-A}	Thermal resistance ceramic Junction-to-Ambient	TBD	°C/W
	θ_{J-C}	Thermal resistance ceramic Junction-to-Case	10	°C/W

Power considerations

The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or screened according to TCS standards devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

3.6.1 - Thomson logo

3.6.2 - Manufacturer's part number

3.6.3 - Class B identification

3.6.4 - Date-code of inspection lot

3.6.5 - ESD identifier if available

3.6.6 - Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified and the relevant measurement conditions are given below. For inspection purpose, refer to relevant specification :

– DESC see § 4.1

(last issue on request to our marketing services).

Table 4 : Static electrical characteristics for all electrical variants. See § 5.2.

Table 6 : Dynamic electrical characteristics for 68332-16 (16.78 MHz). See § 5.3.

For static characteristics, test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause 5.4 hereafter of this specification (Table 7).

5.2 · Static characteristics

Table 4

V_{DD} = 5.0 V_{dc} ±10 % ; GND = 0 V_{dc} ; T_C = −55°C to +125°C or −40°C to +85°C

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	0.7 x V_{DD}	V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{SS} −0.3	0.2 x V_{DD}	V
I_{in}	Input leakage current V_{in} = V_{DD} or V_{SS} $\overline{TSTME}$/TSC, $\overline{BKPT}$, T2CLK, RXD	−2.5	2.5	µA
I_{OZ}	Hi-Z (off-state) leakage current (Note 1) V_{in} = V_{DD} or V_{SS} Group 1 and 2 I/O pins V_{in} = V_{DD} or V_{SS} $\overline{HALT}$, $\overline{RESET}$	−2.5 20	2.5 20	µA µA
V_{OH}	Output high voltage (Notes 1 and 2) I_{OH} = −0.8 mA, V_{DD} = 4.5 V All outputs except $\overline{HALT}$, $\overline{RESET}$	V_{DD} −0.8		V
V_{OL}	Output low voltage (Note 1) I_{OL} = 1.6 mA CLKOUT, $\overline{FREEZE}$/QUOT, $\overline{IPIPE}$, Group 1 I/O pins I_{OL} = 5.3 mA $\overline{CSBOOT}$, $\overline{BG}$/$\overline{CS}$ and Group 2 I/O pins I_{OL} = 15.3 mA $\overline{HALT}$, $\overline{RESET}$		0.4 0.4 0.4	V V V
V_{SB}	RAM standby voltage	3.0	V_{DD}	V
I_{SB}	RAM standby current		50	µA
I_{DD} S_{IDD}	Total supply current RUN (Note 3) STOP (VCO Off)		125 500	mA µA
P_D	Power dissipation		690	mW
C_{in}	Input capacitance (Notes 1 and 4) All input-only pins All I/O pins		10 20	pF pF
C_L	Load capacitance (Note 1) CLKOUT, FREEZE/QUOT, $\overline{IPIPE}$ and Group 1 I/O pins $\overline{BSBOOT}$, $\overline{BG}$/$\overline{CS}$ and Group 2 I/O pins $\overline{HALT}$, $\overline{RESET}$		90 100 130	pF pF pF

Note 1 : Input-only pins : $\overline{TSTME}$/TSC, $\overline{BKPT}$, T2CLK, RXD.
Output-only pins : $\overline{CSBOOT}$, $\overline{BG}$/$\overline{CS}$, CLKOUT, FREEZE/QUOT, $\overline{IPIPE}$.
Input/output pins :
Group 1 : D15-D0, $\overline{IFETCH}$, Port A (TP15-TP8), Port B (TP7-TP0).
Group 2 : Port C (A23-A19/$\overline{CS}$, FC2-FC0/$\overline{CS}$), Port D (MISO, MOSI/SDA, SCK, $\overline{PCS0}$/$\overline{SS}$, $\overline{PCS3}$-$\overline{PCS1}$, TXD), Port E $\overline{DSACK0}$, $\overline{DSACK1}$, AVEC, $\overline{RMC}$, $\overline{DS}$, $\overline{AS}$, SIZ0, SIZ1), Port F (MODCK, $\overline{IRQ7}$-$\overline{IRQ1}$), A18-A0, R/$\overline{W}$, $\overline{BERR}$, $\overline{BR}$/$\overline{CS}$, $\overline{BGACK}$/$\overline{CS}$.
Group 3 : $\overline{HALT}$, $\overline{RESET}$.

Note 2 : V_{OH} specification for $\overline{HALT}$ and $\overline{RESET}$ is not applicable beacause they are open-drain pins. V_{OH} specification is not applicable to Port D (MISO, MOSI/SDA, SCK, PCS0/$\overline{SS}$, $\overline{PCS3}$-$\overline{PCS1}$, TXD) in wire-OR mode.

Note 3 : Supply current measured with system clock frequency of 16.78 MHz.

Note 4 : Input capacitance is periodically sampled rather than 100 % tested.

5.3 - Dynamic (Switching) characteristics

The limits and values given in this section apply over the full case temperature range $-55°C$ to $+125°C$ and V_{DD} in the range 4.5 V to 5.5 V V_{IL} = 0.5 V and V_{IH} = 2.4 V.

The INTERVAL numbers refer to the timing diagrams..

Table 5 - Control timing

V_{DD} = 5.0 V_{dc} ±10 % ; V_{SS} = 0 V_{dc} ; T_C = $-55°C$ to $+125°C$ or $-40°C$ to $+85°C$

Symbol	Parameter	Min	Max	Unit
f_{sys}	System frequency (see Note)	dc	16.78	MHz
f_{XTAL}	Crystal frequency	25	50	kHz
f_{sys}	On-chip VCO system frequency	0.13	16.78	MHz
f_{VCO}	On-chip VCO frequency range	0.1	35	MHz
f_{sys}	External clock operation	dc	16.78	MHz
t_{rc}	PLL startup time (C = 0.1 µF, stable V_{DD} and crystal)		10	ms
Note : All internal registers retain data at 0 Hz.				

Table 6

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = $-55°C$ to $+125°C$ or $-40°C$ to $+85°C$ - (Note 1)

Num.	Symbol	Parameter	Min	Max	Unit	Note
	f	Frequency of operation	0.13	16.78	MHz	
1	t_{cyc}	Clock period	59.6		ns	
1A	t_{Ecyc}	E clock period	476		ns	
2, 3	t_{CW}	Clock pulse width	28		ns	
2A, 3A	t_{ECW}	E clock pulse width	236		ns	
4, 5	t_{Crf}	Clock rise and fall time		5.	ns	
4A, 5A	t_{rf}	Rise and fall time - All outputs except CLKOUT		8	ns	
6	t_{CHAV}	Clock high to address, FC, SIZE, $\overline{RMC}$ valid	0	30	ns	
7	t_{CHAZx}	Clock high to address, Data, FC, SIZE, $\overline{RMC}$ high impedance	0	60	ns	
8	t_{CHAZn}	Clock high to address, FC, SIZE, $\overline{RMC}$ invalid	0		ns	
9	t_{CLSA}	Clock low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{IFETCH}$ asserted	3	30	ns	
9A	t_{STSA}	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ asserted (read)	−15	15	ns	2
11	t_{AVSA}	Address, FC, SIZE, $\overline{RMC}$ valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) asserted	15		ns	
12	t_{CLSN}	Clock low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{IFETCH}$ negated	3	30	ns	
13	t_{SNAI}	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ negated to address, FC, SIZE invalid (address hold)	15		ns	
14	t_{SWA}	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) width asserted	100		ns	
14A	t_{SWAW}	$\overline{DS}$, $\overline{CS}$ width asserted write	45		ns	
14B	t_{SWDW}	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) width asserted (asynchronous cycle)	40		ns	
15	t_{SN}	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ width negated	40		ns	3
16	t_{CHSZ}	Clock high to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ high impedance		60	ns	
17	t_{SNRN}	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ negated to R/$\overline{W}$ high	15		ns	
18	t_{CHRH}	Clock high to R/$\overline{W}$ high	0	30	ns	
20	t_{CHRL}	Clock high to R/$\overline{W}$ low	0	30	ns	

Table 6 (continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = −55°C to +125°C or −40°C to +85°C - (Note 1)

Num.	Symbol	Parameter	Min	Max	Unit	Note
21	t_{RAAA}	R/$\overline{W}$ high to $\overline{AS}$ asserted	15		ns	
22	t_{RASA}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write)	70		ns	
23	t_{CHDO}	Clock high to data out valid		30	ns	
24	t_{DVASN}	Data out valid to negating edge of $\overline{AS}$ (synchronous write)	15		ns	
25	t_{SNDOI}	$\overline{DS}$, $\overline{CS}$ negated to data out invalid (data out hold)	15		ns	
26	t_{DVSA}	Data out valid to $\overline{DS}$ asserted (write)	15		ns	
27	t_{DICL}	Data in valid to clock low (data setup)	5		ns	9
27A	t_{BELCL}	Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ asserted to clock low (setup time)	20		ns	
28	t_{SNDN}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ negated	0	80	ns	
29	t_{SNDI}	$\overline{DS}$ negated to data in invalid (data in hold)	0		ns	4
29A	t_{SHDI}	$\overline{DS}$ negated to data in high impedance		60	ns	4
30	t_{CLDI}	CLKOUT low to data in invalid (synchronous hold)	15		ns	4
30A	t_{CLDH}	CLKOUT low to data in high impedance		90	ns	4
31	t_{DADI}	$\overline{DSACKx}$ asserted to dat in valid		50	ns	5
32	t_{HRrf}	$\overline{HALT}$ and $\overline{RESET}$ input transition time		200	ns	
33	t_{CLBA}	Clock low to $\overline{BG}$ asserted		30	ns	
34	t_{CLBN}	Clock low to $\overline{BG}$ negated		30	ns	
35	t_{BRAGA}	$\overline{BR}$ asserted to $\overline{BG}$ asserted ($\overline{RMC}$ not asserted)	1		Clks	6
37	t_{GAGN}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated	1	2	Clks	
39	t_{GH}	$\overline{BG}$ width negated	2		Clks	
39A	t_{GA}	$\overline{BG}$ width asserted	1		Clks	
46	t_{RWA}	R/$\overline{W}$ width asserted (write or read)	150		ns	
46A	t_{RWAS}	R/$\overline{W}$ width asserted (synchronous write or read)	90		ns	
47A	t_{AIST}	Asynchronous input setup time $\overline{BR}$, $\overline{BG}$, $\overline{DSACKx}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	5		ns	9
47B	t_{AIHT}	Asynchronous input hold time	15		ns	
48	t_{DABA}	$\overline{DSACKx}$ asserted to $\overline{BERR}$, $\overline{HALT}$ asserted		30	ns	7
53	t_{DOCH}	Data out hold from clock high	0		ns	
54	t_{CHDH}	Clock high to data out high impedance		28	ns	
55	t_{RADC}	R/$\overline{W}$ asserted to data bus impedance change	40		ns	
56	t_{HRPW}	$\overline{RESET}$ pulse width (reset instruction)	512		Clks	
57	t_{BNHN}	$\overline{BERR}$ negated to $\overline{HALT}$ negated (rerun)	0		ns	
70	t_{SCLDD}	Clock low to data bus driven (show)	0	30	ns	
71	t_{SCLDS}	Data setup time to clock low (show)	15		ns	
72	t_{SCLDH}	Data hold from clock low (show)	10		ns	
80	t_{EAV}	Address, R/$\overline{W}$ valid to E rise	75		ns	
81	t_{EAH}	Address, R/$\overline{W}$ hold time	30		ns	

Table 6 (continued)

V_{DD} = 5.0 Vdc ±10 % ; V_{SS} = 0 Vdc ; T_C = −55°C to +125°C or −40°C to +85°C - (Note 1)

Num.	Symbol	Parameter	Min	Max	Unit	Note
82	t_{EACCA}	Address access time	289		ns	8
83	t_{EACCE}	MPU access time	206		ns	8
84	t_{EDSR}	Read data setup time	30		ns	
85	t_{EDHR}	Read data hold time	5		ns	
85A	t_{ELDI}	E low to data in high impedance		60	ns	
86	t_{EPWDD}	E fall to write data driven	0	60	ns	
87	t_{EDDW}	Write data delay time		0	ns	
88	t_{EDHW}	Write data hold time	30		ns	
89	t_{EASL}	Address, R/$\overline{W}$ valid to $\overline{AS}$, $\overline{CS}$ fall	15		ns	
90	t_{EASED}	Delay time, $\overline{AS}$ to E rise	150		ns	
91	t_{ELASN}	Delay time, E low to $\overline{AS}$ negated	0		ns	
91A	t_{ELCSN}	Delay time, E low to $\overline{CS}$ negated	20		ns	
92	t_{EPWASH}	Pulse width $\overline{AS}$ negated (E cycle)	30		ns	
S1	t_{SASCH}	Slave mode $\overline{AS}$, $\overline{DS}$ valid to clock high	10		ns	
S2	t_{SAVCL}	Slave mode address, R/$\overline{W}$, FC, SIZ valid to clock low	15		ns	
S3	t_{SAHCL}	Slave mode address, R/$\overline{W}$, FC, SIZ hold time from clock low	15		ns	
S4	t_{SDSKA}	Slave mode clock high to $\overline{DSACK}$ asserted		30	ns	
S5	t_{SDSCKH}	Slave mode $\overline{DSACK}$ hold time from clock low	0	30	ns	
S6	t_{SCLDV}	Slave mode clock low to read data valid		30	ns	
S7	t_{SSRDH}	Slave mode read data hold time from clock low	0	30	ns	
S8	t_{SDSCL}	Slave mode write data input setup time to clock low	20		ns	
S9	t_{SDHCL}	Slave mode write data hold time from clock low	20		ns	
S10	t_{SDLAH}	Slave mode $\overline{DSACK}$ asserted to $\overline{AS}$, $\overline{DS}$ negated	0		ns	

Note 1 : All AC timing is shown with respect to 20 % V_{DD} and 70 % V_{DD} levels unless otherwise noted.

Note 2 : This number can be reduced to 5 ns if strobes have equal loads.

Note 3 : If multiple chip selects are used, the $\overline{CS}$ width negated (= 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous E cycles.

Note 4 : These hold times are specified with respect to $\overline{DS}$ on asynchronous reads and with respect to CLKOUT on synchronous reads. The user is free to use either hold time.

Note 5 : If the asynchronous setup time (= 47A) requirements are satisfied, the $\overline{DSACK}$x low to data setup time (= 31) and $\overline{DSACK}$x low to $\overline{BERR}$ low setup time (= 48) can be ignored. The date must only satisfy the data-in to clock low setup time (= 27) for the following clock cycle ; $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time (= 27A) for the following clock cycle.

Note 6 : To ensure coherency during every operand transfer, $\overline{BG}$ will not be asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete and $\overline{RMC}$ is negated.

Note 7 : In the absence of $\overline{DSACK}$x, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (= 47A).

Note 8 : Synchronous E cycle address access time = $t_{EAV} + t_{rf} + t_{ECW} - t_{EDSR}$ = 289 ns (16.78 MHz clock).
Synchronous E cycle MPU access time = $t_{ECW} - t_{EDSR}$ = 206 ns (16.78 MHz clock).

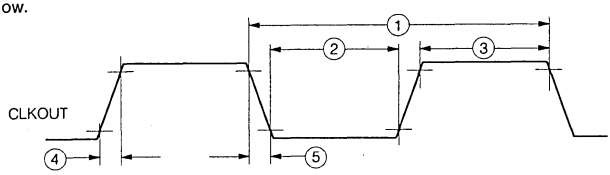
Note 9 : Initial masks of TS 68332 devices require increased input setup times. TMS will be testing the input data setup time (t_{DICL}) and the asynchronous input setup time (t_{AIST}) at 15 ns maximum until circuit improvements are completed. The interim data setup time value will decrease each access time defined in Note 10 by 10 ns.

Note 10 : Address access time = $2\,t_{cyc} + t_{CW} - t_{CHAV} - t_{DICL}$ = 112.2 ns (16.78 MHz clock).
Chip-select access time = $2\,t_{cyc} - t_{CLSA} - t_{DICL}$ = 84.2 ns (16.78 MHz clock).
Synchronous address access time = $t_{cyc} + t_{CW} - t_{CHAV} - t_{DICL}$ = 52.6 ns (16.78 MHz clock).
Synchronous chip-select access time = $t_{cyc} - t_{CLSA} - t_{DICL}$ = 24.6 ns (16.78 MHz clock).

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «NUM» of Table 6, refering to the loading network number as shown in Figure 3 below.

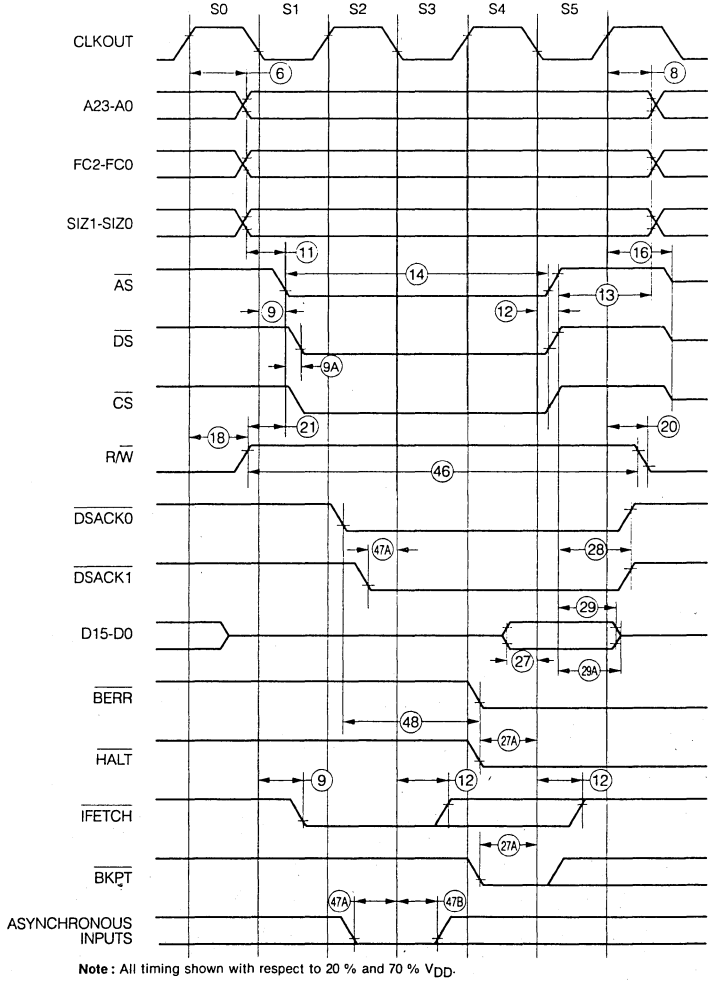


Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 3 : Clock output timing.

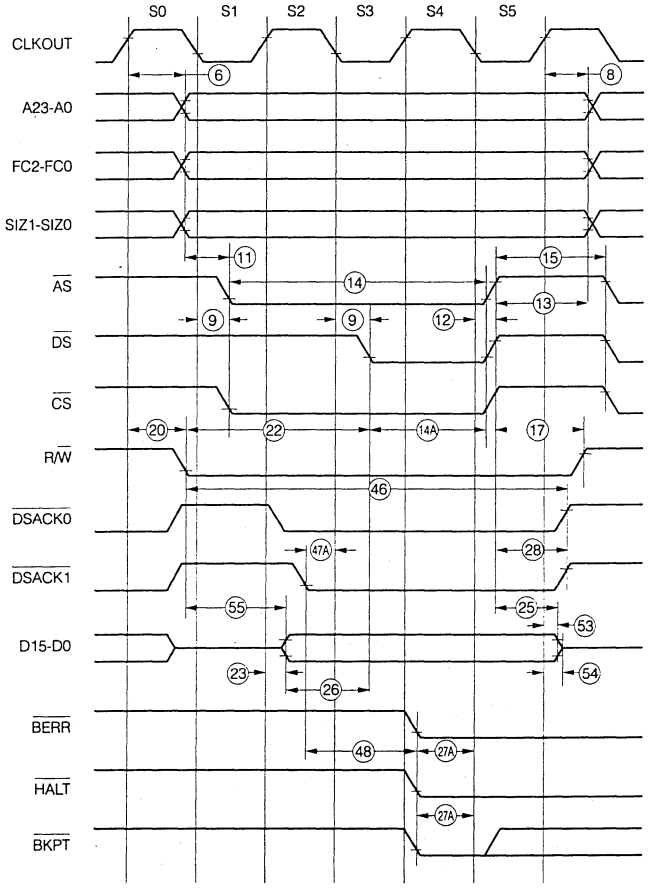
5.4.2 - Time definitions

The times specified in Table 6 as dynamic characteristics are defined in Figures 4 to 11 below, by a reference number given the column «NUM» of the tables together with the relevant figure number.



Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 4 : Read cycle timing diagram.

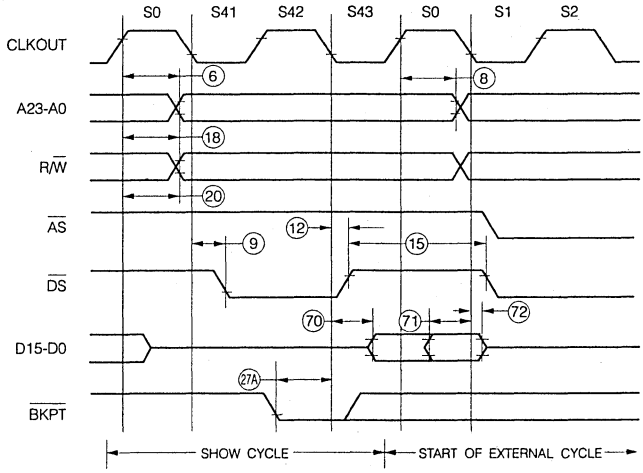


Note : All timing shown with respect to 20 % and 70 % V_{DD}.

* Timing dependent on programed options (i.e., tined with respect to DS or AS assertion).

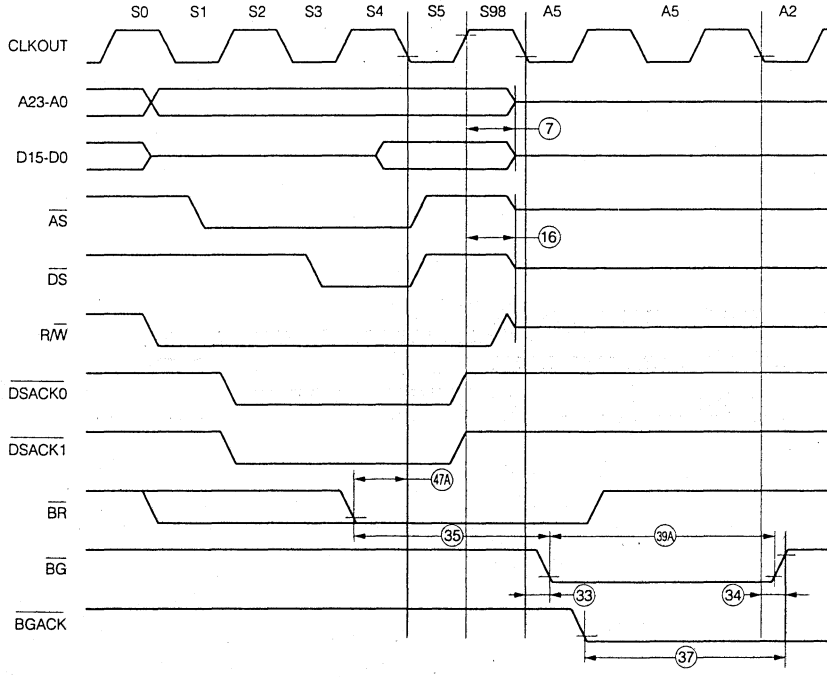
Figure 5 : Write cycle timing diagram.

6



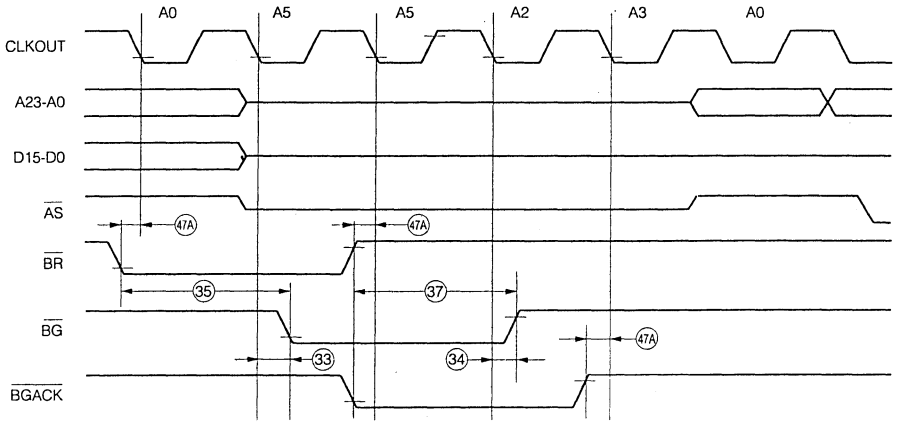
Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 6 : Show cycle timing diagram.



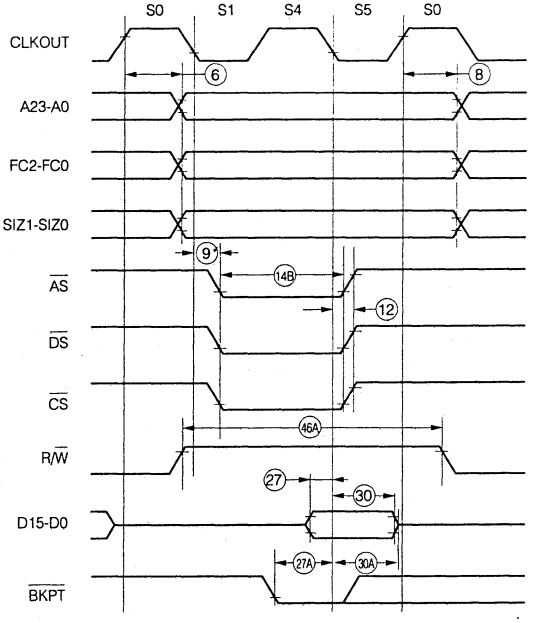
Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 7 : Bus arbitration timing diagram - active bus case.



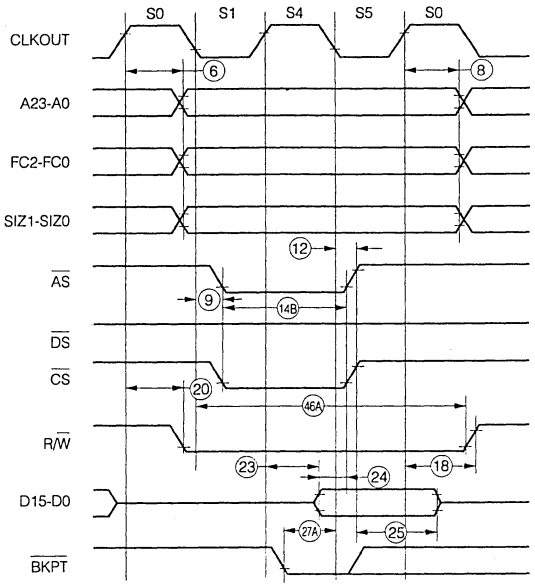
Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 8 : Bus arbitration timing diagram - idle bus case.



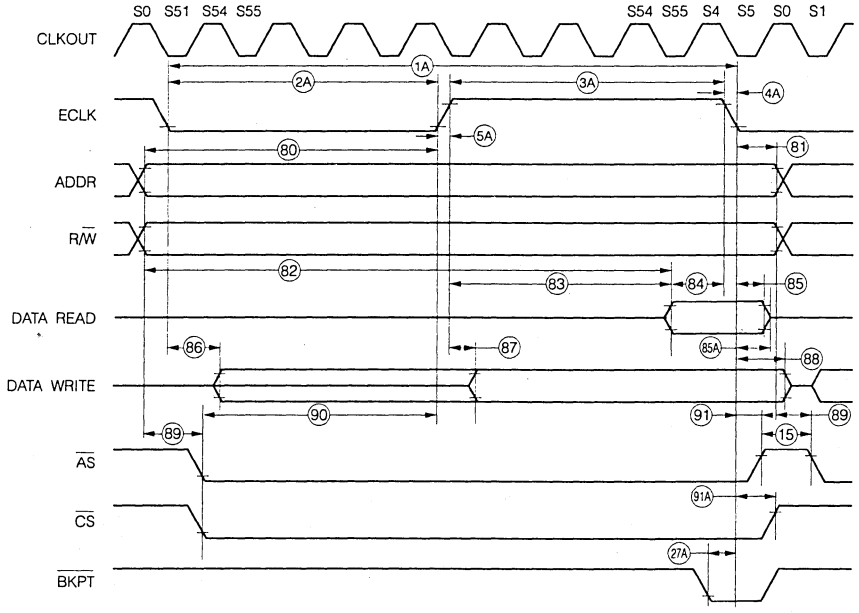
Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 9 : Synchronous read cycle timing diagram.



Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 10 : Synchronous write cycle timing diagram.



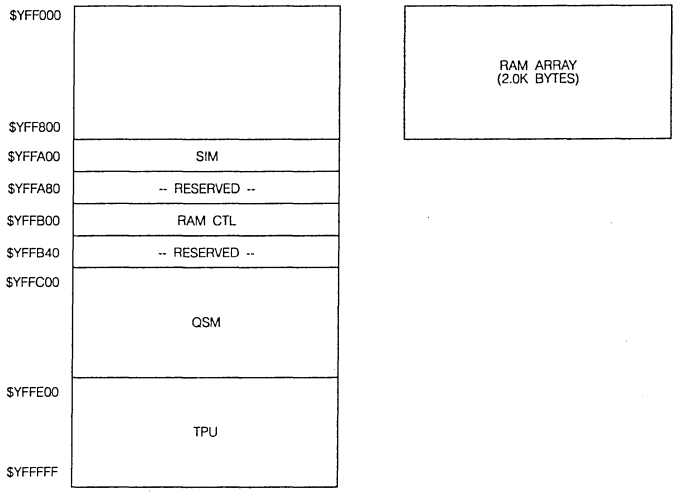
Note : All timing shown with respect to 20 % and 70 % V_{DD}.

Figure 11 : Synchrnous E-cycle timing diagram.

6 · FUNCTIONAL DESCRIPTION

6.1 · Module memory map

Figure 12 illustrates the memory map of the TS 68332. The RAM array is positioned by the base address register in the RAM CTRL block. Reset forces the RAM array to be disabled. Unimplemented blocks are mapped externally.



Y - M111,where M is the modmap signal state on the IMB, which reflects the state of the modmap bit in the module configuration register of the system integration module (Y=$7 or $F).

Figure 12 : Module memory map.

6.2 · CPU32 overview

This section is an overview of the CPU32. All capabilities and functions of this module are detailed fully in the CPU32 reference manuel.

The CPU32, the instruction processing module of the 68300 family, is based on the industry-standard TS 68000 core processor with many features of the 68010 and TS 68020 as well as unique features suited for high-performance controller applications. The CPU32 is designed to provide a significant increase in performance over existing microcontroller CPUs to meet the demand for higher performance requirements for the 1990s, while maintaining source code and binary code compatibility with the 68000 family.

Ease of programming is an important consideration in using a microcontroller. An instruction format implementing a register-memory interaction philosophy predominates in the design, and all data resources are available to all operations requiring those resources.

6.2.1 · Block diagram

Figure 13 shows a block diagram of the CPU32. The major clocks depicted operate in a highly independent fashion that maximizes concurrency of operation while managing the essential synchronization of instruction execution and bus operation. The bus controller loads instructions from the data bus into the decode unit.

The sequencer and control unit provide overall chip control, managing the internal buses, registers, and functions of the execution unit.

6.2.2 · Architecture summary

The CPU32 architecture includes several important features that provide both power and versatility to the user. The CPU32 is source and object code compatible with the TS 68000 and 68010. All user-state programs can be executed unchanged. The major CPU32 features are as follows :

- 32-bit internal data path and arithmetic hardware,
- 32-bit internal address bus, 24-bit external address bus,
- eight 32-bit general-purpose data registers,
- seven 32-bit general-purpose address registers,
- separate user and supervisor stack pointers and address spaces,

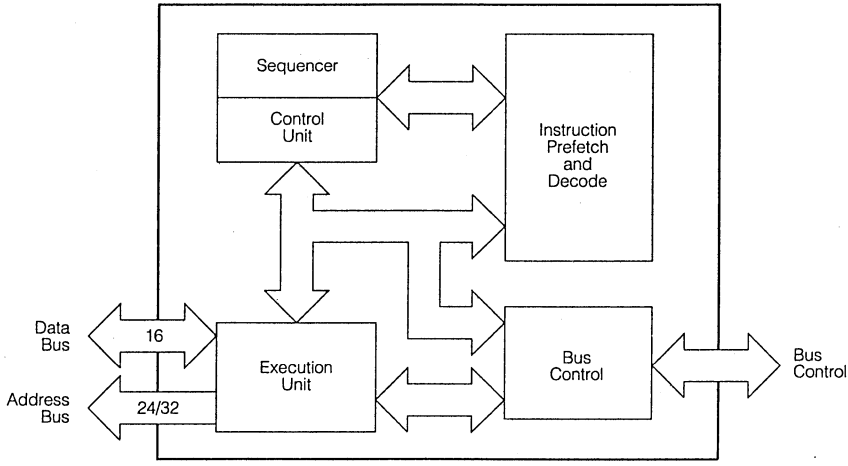


Figure 13 : CPU32 block diagram.

- separate program and data address spaces,
- full interrupt processing,
- fully upward object code compatible with 68000 family,
- virtual memory implementation,
- loop mode of instruction execution,
- fast multiply, divide, and shift instructions,
- fast bus interface with dynamic bus port sizing,
- improved exception handling for controller applications
- enhanced addressing modes :
  - scaled index,
  - address register indirect with base displacement and index,
  - expanded PC relative modes 32-bit branch displacements.
- instruction set enhancements :
  - high-precision multiply and divide,
  - trap on condition codes,
  - upper and lower bounds checking,
  - enhanced breakpoint instruction.
- trace on change of flow,
- table lookup and interpolate instruction,
- low power stop instruction,
- hardware breakpoint signal, background mode,
- 16.78 MHz operating frequency at – 55°C to + 125°C,
- fully static implementation.

6.2.3 · Programmer's model

The programming model of the CPU32 consists of two groups of registers : user model and supervisor model, which correspond to the user and supervisor privilege levels. Executing at the user privilege level, user programs can only use the registers of the user model. Executing at the supervisor level, system software uses the control registers of the supervisor level to perform supervisor functions.

The supervisor level has higher privileges than the user level. Not all instructions are permitted to execute in the lower privileged user level, but all instructions are available at the supervisor level. This scheme allows a separation of supervisor and user levels, and so the supervisor can protect system resources from uncontrolled access. The processor uses the privilege level indicated by the S bit in the status register to select either the user or supervisor privilege level and either the USP or SSP for stack operations.

The user programming model remains unchanged from previous 68000 family microprocessors. The supervisor programming model, which supplements the user programming model is used exclusively by the CPU32 system programmers who utilize the supervisor privilege level to implement sensitive operationg system functions. The supervisor programming model contains all the controls to access and enable the special features of the CPU32. All application software, written to run at the nonprivileged user level, migrates to the CPU32 from any 68000 platform without modification. The programming models are shown in Figures 14 and 15.

6.2.4 · Registers

Registers D7-D0 are used as data registers and readily support 8-bit (byte), 16-bit (word) and 32-bit (long word) operand lengths for all operations. Registers A6-A0 and the user and supervisor stack pointers are address registers that may be used as software stack pointers or base address registers. Register A7 is a register designation that applies to the user stack pointer in the user privilege level and to the supervisor stack pointer in the user privilege level. In addition, the address registers may be used for word and long-word operations. All of the 16 general-purpose registers (D7-D0, A7-A0) may be used as index registers.

The PC contains the address of the next instruction to be executed by the CPU32.

The status register (SR) stores the processor status. It contains the condition codes that reflect the results of a previous operation and can be used for conditional instruction execution in a program.

The vector base register (VBR) contains the base address of the exception vector table in memory. The displacement of an exception vector is added to the value in this register to access the vector table.

Alternate function code registers (SFC and DFC) contain 3-bit function codes. Function codes can be considered extensions of the 24-bit linear address that optionally provide as many as eight 16 Mbyte address spaces. These address spaces are designated as either user or supervisor space and as either program or data space. There is a CPU space to allow the CPU to acquire specific control information not usually associated with read or write bus cycles. The function code signals FC2-FC0 select the appropriate address space.

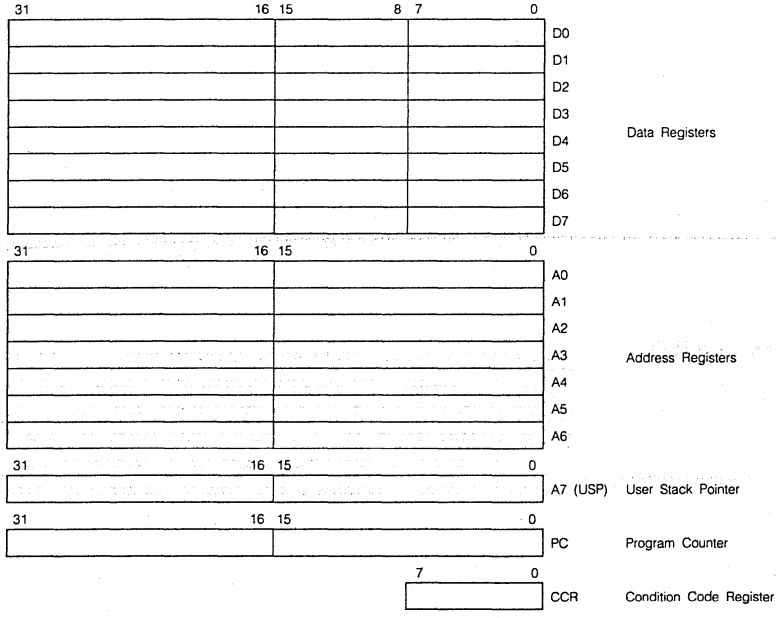


Figure 14 : User programming model.

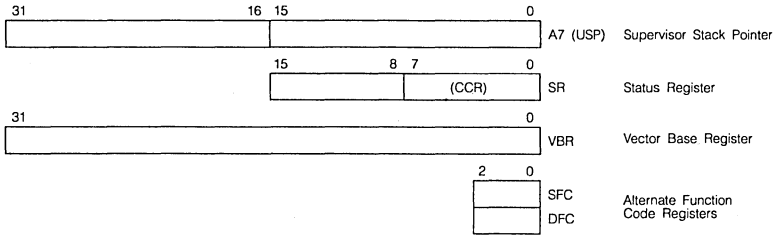


Figure 15 : Supervisor programming model supplement.

6.2.5 · Data types

Six basic data types are supported :

- bits,
- packaged binary-coded decimal digits,
- byte integers (8 bits),
- word integers (16 bits),
- long-word integers (32 bits),
- quad-word integers (64 bits).

6.2.5.1 · Organisation in registers

The eight data registers can store data operands of 1, 8, 16, 32 and 64 bits and addresses of 16 or 32 bits. The seven address registers and the two stack pointers are used for address operands of 16 or 32 bits. The PC is 32 bits wide.

6.2.6 · System features

The CPU32 includes a number of features to aid system implementation. These include a privilege mechanism, separation of address spaces, multilevel priority interrupts, trap instructions, and a trace facility.

The privilege mechanism provides user and supervisor privilege states, privileged instructions, and external distinction of user and supervisor state references. The processor separates references between program and data space. This permits sharing of code segments that access separate data segments.

The CPU32 supports seven priority levels for 199 memory vectored interrupts. For each interrupt, the vector location can be provided externally or generated internally. The seventh level provides a non-maskable interrupt capability.

To simplify system development, instructions are provided to check internal processor conditions and allow software traps. The trace facility allows instruction-by-instruction tracing of program execution without alteration of the program or special hardware.

6.2.7 · Virtual memory

The full addressing range of the CPU32 on the TS 68332 is 16 Mbyte in each on eight address spaces. Even though most systems implement a smaller physical memory, the system can be made to appear to have a full 16 Mbyte of memory available to each user program by using virtual memory techniques.

6.2.8 · Loop mode instruction execution

The CPU32 has several features that provide efficient execution of program loops. One of these features is the DBcc looping primitive instruction. To increase the performance of the CPU32, a loop mode has been added to the processor. The loop mode is used by any single word instruction that does not change program flow. Loop mode is implemented in conjunction with the DBcc instruction. Once in loop mode, the processor performs only the data cycles associated with the instruction and suppresses all instruction fetches.

6.2.9 · Vector base register

The VBR contains the base address of the 1024-byte exception vector table, consisting of 256 exception vectors. Exception vectors contain memory addresses of routines that begin execution at the completion of exception processing, e.g. an interrupt routine.

6.2.10 · Processing states

The processor is always in one of four processing states : normal, exception, halted, or background. The normal processing state is that associated with instruction execution ; the bus is used to fetch instructions and operands and to store results. The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated explicitly by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, a bus error, or a reset. The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. The background processing state is initiated by breakpoints, execution of special instructions, or a double bus fault. Background processing allows interactive debugging of the system via a simple serial interface.

6.2.11 · Addressing modes

Addressing in the CPU32 is register-oriented. Most instructions allow the results of the specified operation to be placed either in a register or directly in memory ; this flexibility eliminates the need for extra instructions to store register contents in memory.

The seven basic addressing modes are as follows :

- register direct,
- register indirect,
- register indirect with index,
- program counter indirect with displacement
- program counter indirect with index,
- absolute,
- immediate

Included in the register indirect addressing modes are the capabilities to post-increment, pre-decrement, and offset. The program counter relative mode also has index and offset capabilities. In addition to these addressing modes, many instructions implicity specify the use of the status register, stack pointer, and/or program counter.

6.2.12 · Instructions

6.2.12.1 · 68000 family compatibility

It is the philosophy of the 68000 family that all user-mode programs can execute unchanged on a more advanced processor, and supervisor-mode programs and exception handlers should require only minimal alteration.

The CPU32 can be thought of as an intermediate member of the 68000 family. Object code from an TS 68000 or 68010 may be executed on the CPU32, and many of the instruction and addressing mode extensions of the TS 68020 are also supported. Refer to the CPU 32 reference manual for a detailed comparison of the CPU32 and TS 68020 instruction set (see also Table 7).

6.2.12.2 · New instructions

Two new instruction have been added to the TS 68000 instruction set for use in controller applications. They are low power stop (LPSTOP) and table lookup and interpolate (TBL).

Low Power Stop (LPSTOP)
In applications where power consumption is a consideration, the CPU32 forces the device into a low-power standby mode when immediate processing is not required. The low-power stop mode is entered by executing the LPSTOP instruction. The processor will remain in this mode until a user-specification (or higher) interrupt level or reset occurs.

Table lookup and interpolate (TBL)
To maximize throughput for real-time applications, reference data is often «pre-calculated» and stored in memory for quick access. The storage of each data point would require an inordinate amount of memory. The table instruction requires only a sample of data points stored in the array, reducing memory requirements. This single instruction allows intermediate values to be recovered by linear interpolation, thus significantly increasing CPU throughput compared with earlier interpolation methods which used several instructions. The results are optionally rounded with the round-to-nearest algorithm.

6.2.13 · Development support

The following features have been implemented on the CPU32 to enhance the instrumentation and development environment :

- 68000 family development support,
- background debug mode,
- deterministic opcode tracking,
- hardware breakpoints.

6.2.13.1 · 68000 family development support

All 68000 family members include features to facilitate applications development. These features include the following :

Trace on Instruction execution - 68000 family processors include an instruction-by-instruction tracing facility as an aid to program development. The CPU32 also allows the user to trace only those instructions causing a change in program flow.

Breakpoint instruction - An emulator may insert software breakpoints into the target code to indicate when a breakpoint has occurred. On the CPU32, this function is provided via illegal instructions, $4848 – $484F, to serve as breakpoint instructions.

Unimplemented instruction emulation - During instruction execution, when an attempt is made to execute an illegal instruction, an illegal instruction exception occurs. Unimplemented instructions (F-line, A-line,...) utilize separate exception vectors to permit efficient emulation of unimplemented instructions in software.

6.2.13.2 · Background debug mode

Microcomputer systems generally provide a debugger, implemented in software, for system analysis at the lowest level. The background debug mode on the CPU32 is unique in that the debugger has been implemented in CPU microcode. Registers can be viewed and/or altered, memory can be read or written to, and test features can be invoked. Incorporating these capabilities on-chip simplifies the environnement in which the in-circuit emulator operates.

6.2.13.3 - Deterministic opcode tracking

CPU 32 function code outputs are augmented by two supplementary signals to monitor the instruction pipeline. The instruction pipe (PIPE) output indicates the start of each new instruction and each mid-instruction pipeline advance. The instruction fetch (FETCH) output identifies the bus cycles in which the operand is loaded into the instruction pipeline. Pipeline flushes are also signalled with IFETCH. Monitoring these two signals allows a bus analyzer to synchronize itself to the instruction stream and monitor its activity.

6.2.13.4 - On-chip breakpoint hardware

An external breakpoint input allows a breakpoint trap on any memory access.

Table 7 - Instruction set summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
ADDX	Add with Extend
AND	Logical AND
ANDI	Logical AND Immediate
ASL, ASR	Arithmetic Shift Left and Right
Bcc	Branch Conditionally
BCHG	Test Bit and Change
BCLR	Test Bit and Clear
BGND	Background
BKPT	Breakpoint
BRA	Branch
BSET	Test Bit and Set
BSR	Branch to Subroutine
BTST	Test Bit
CHK, CHK2	Check Register Against Upper and Lower Bounds
CLR	Clear
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory to Memory
CMP2	Compare Register Against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LPSTOP	Low Power Stop
LSL, LSR	Logical Shift Left and Right

Mnemonic	Description
MOVE	Move
MOVE CCR	Move Condition Code Register
MOVE SR	Move Status Register
MOVE USP	Move User Stack Pointer
MOVEA	Move Address
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral
MOVEQ	Move Quick
MOVES	Move Alternate Addree Space
MULS, MULS.L	Signed Multiply
MULU, MULU.L	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and De-allocate
RTE	Return from Exception
RTR	Return and Restore Codes
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Register Words
TBLS, TBLSN	Signed/Unsigned Table Lookup
TBLU, TBLUN	and Interpolate
TAS	Test Operand and Set
TRAP	Trap
TRAPcc	Trap Conditionally
TRAPV	Trap on Overflow
TST	Test Operand
UNLK	Unlink

6.3 - Bus operation

This section provides a functional description of the bus and the signals that control it. Operation of the bus is the same whether the MCU or an external device is the bus master ; the names and descriptions of bus cycles are from the point of view of the bus master. The MCU architecture supports byte, word, and long-word operands, allowing access to 8-bit and 16-bit data ports through use of asynchronous cycles controlled by the data transfer (SIZ1 and SIZ0) and data size acknowledge pins ($\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$).

6.3.1 · Function codes

The function code signals (FC2-FC0) select one of eight 16 Mbyte address space to which the address applies.

6.3.2 · Address bus

The address bus signals (A23-A0) define the address of the byte (or the most significant byte) to be transferred during a bus cycle. The address is valid while $\overline{AS}$ asserted.

6.3.3 · Address strobe

The Address Strobe ($\overline{AS}$) is a timing signal that indicates the validity of an address on the address bus and of many control signals.

6.3.4 · Data bus

The data signals (D15-D0) comprise a bidirectional, non-multiplexed parallel bus that contains the data being transferred to or from the MCU. A read or write operation may transfer 8 or 16 bits of data (1 or 2 bytes) in one bus cycle.

6.3.5 · Data strobe

The Data Strobe ($\overline{DS}$) is a timing signal that applies to the data bus. For a read cycle, the MCU asserts $\overline{DS}$ to signal the external device to place data on the bus. For a write cycle, $\overline{DS}$ signals to the external device that the data to be written is valid on the bus.

6.3.6 · Bus control signals

The MCU initiates a bus cycle by driving the address, size, function code, and read/write outputs. At the beginning of a bus cycle, the size signals (SIZ1, SIZ0) are driven along with the function code signals. SIZ1 and SIZ0 indicate the number of bytes remaining to be transferred during an operand cycle (consisting of one or more bus cycles). Table 8 shows the encoding of SIZ1 and SIZ0. The read/write ($\overline{R/W}$) signal determines the direction of the transfer during a bus cycle. The read-modify-write cycle signal ($\overline{RMC}$) is asserted at the beginning of the first bus cycle of a read-modify-write operation, and remains asserted until completion of the final bus cycle of the operation.

Table 8 · Size signal encoding

SIZ1	SIZ2	Transfer Size
0	1	Byte
1	0	Word
1	1	3 Byte
0	0	Long Word

6

6.3.7 · Bus cycle termination signals

During bus cycles, external devices assert the data transfer and size acknowledge signals $\overline{DSACK1}$ and/or $\overline{DSACK0}$ as part of the bus protocol. During a read cycle, this signals the MCU to terminate the bus cycle and to latch the data. During a write cycle, this indicates that the external device has sucessfully stored the data and that the cycle may terminate. These signals also indicate to the MCU the size of the port for the bus cycle just completed.

The bus error ($\overline{BERR}$) signal is also a bus cycle termination indicator and can be used in the absence of $\overline{DSACKx}$ to indicate a bus error condition. It can also be asserted in conjunction with $\overline{DSACKx}$ to indicate a bus error condition, provided it meets the appropriate timing. Additionally, the $\overline{BERR}$ and $\overline{HALT}$ signals can be asserted simultaneously, in lieu of, or in conjunction with, the $\overline{DSACKx}$ signals.

The internal bus monitor can be used to generate the $\overline{BERR}$ signal for internal and internal-to-external transfers. An external bus master must provide its own $\overline{BERR}$ generation and drive the $\overline{BERR}$ pin, since the internal $\overline{BERR}$ monitor has no information about transfers initiated by an external bus master.

Finally the autovector ($\overline{AVEC}$) signal can be used to terminate interrupt acknowledge cycles, indicating that the MCU should internally generate a vector number to locate an interrupt handler routine. $\overline{AVEC}$ is ignored during all other bus cycles.

6.3.8 · Dynamic bus sizing

The MCU dynamically interprets the port size of the addressed device during each bus cycle, allowing operand transfers to or from 8- and 16-bit ports. During an operand transfer cycle, the slave device signals its port size (byte or word) and indicates completion of the bus cycle to the MCU through the use of the $\overline{DSACKx}$ encodings and assertion results. Refer to Table 9 for $\overline{DSACKx}$ encodings and assertion results. For example, if the MCU is executing an instruction that reads a long-word operand from a 16-bit port, the MCU latches the 16 bits of valid data and runs another bus cycle to obtain the other 16 bits.

Dynamic bus sizing requires that the portion of the data bus for a transfer to or from a particular port size be fixed. For example an 8 bit port must reside on data bus bits 15-8.

The $\overline{SIZx}$ signals also from part of the bus sizing protocol. These outputs indicate the remaining number or bytes to be transferred during the current bus cycle.

Table 9 - DSACK codes and results

$\overline{DSACK1}$	$\overline{DSACK0}$	Result
1 (Negated)	1 (Negated)	Insert wait states in current bus cycle
1 (Negated)	0 (Asserted)	Complete cycle - Data bus port size is 8 bits
0 (Asserted)	1 (Negated)	Complete cycle - Data bus port size is 16 bits
0 (Asserted)	0 (Asserted)	Reserved

6.3.9 - Bus operation

The MCU bus is used in an asynchronous manner. The external devices connected to the bus can operate at clock frequencies different from the clock for the MCU. Bus operation uses the handshake lines ($\overline{AS}$, $\overline{DS}$, $\overline{DSACK1}$, $\overline{DSACK0}$, $\overline{BERR}$ and $\overline{HALT}$) to control data transfers. Decoding the size outputs and lower address line A0 provides strobes that select the active portion of the data bus. The slave device (memory or peripheral) then responds by placing the requested data on the correct portion of the data bus for a read cycle or latching the data on a write cycle, and asserting the $\overline{DSACK1}$/$\overline{DSACK0}$ combination that corresponds to the port size to end the cycle. If no slave responds or the access is invalid, external control logic asserts the $\overline{BERR}$, or $\overline{BERR}$ and $\overline{HALT}$ signal(s) to abort or retry the bus cycle, respectively.

6.3.10 - Fast termination cycles

With an external device that has a fast access time, the chip-select circuit fast-termination option can provide a two-cycle external bus transfer. Since the chip select circuits are driven from the system clock, the bus cycle termination is inherently synchronized with the system clock.

6.3.11 - Bux exception control cycles

The bus architecture requires assertion of $\overline{DSACKx}$ from an external device to signal that a bus cycle is complete. $\overline{DSACKx}$ or $\overline{AVEC}$ is not asserted in these cases :

- The external device does not respond,
- No interrupt vector is provided,
- Various other application-dependent errors occur.

This MCU has a bus error input ($\overline{BERR}$) when no device responds by asserting $\overline{DSACKx}$ or $\overline{AVEC}$ within an appropriate period of time after the MCU asserts the $\overline{AS}$. This allows the cycle to terminate and the MCU to enter exception processing for the error condition. Another signal that is used for bus exception control is the halt signal ($\overline{HALT}$). This signal can be asserted by an external device for debugging purposes to cause single bus operation or (in combination with $\overline{BERR}$) a retry of a bus cycle in error.

6.3.12 - Bus arbitration

The bus design of the MCU provides for a single bus master at any one time : either the MCU or an external device. One or more of the external devices on the bus can have the capability of becoming bus master. Bus arbitration is the protocol by which an external device becomes bus master ; the bus controller in the MCU manages the bus arbitration signals so that the MCU has the lowest priority. External devices that need to obtain the bus must assert the bus arbitration signals in a certain sequence. Systems that include several devices that can become bus master require external circuitry to assign priorities to the devices, so that when two or more external devices attempt to become bus master at the same time, the one having the highest priority becomes bus master first. The protocol is explained fully in the SIM manual, however here is the basic sequence of events :

- An external device asserts the bus request signal ($\overline{BR}$),
- The MCU asserts the bus grant signal to indicate that the bus is available ($\overline{BG}$),
- The external device asserts the bus grant acknowledge signal ($\overline{BGACK}$) to indicate that it has assumed bus mastership.

Bus arbitration requests are recognized during normal processing, HALT assertion, when the CPU has halted due to a double bus fault.

6.3.13 - Reset operation

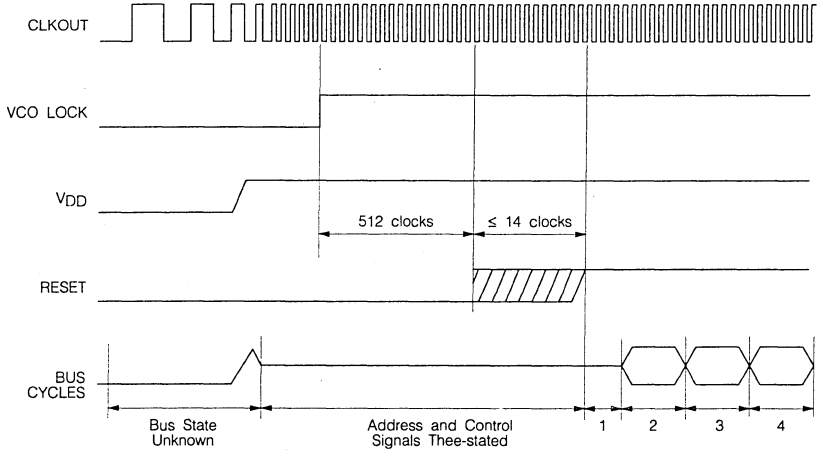
The MCU has reset control logic to determine the cause of reset and synchronize it if necessary. If an external device drives the $\overline{RESET}$ pin low, the reset control logic holds $\overline{RESET}$ asserted internally until the external $\overline{RESET}$ is released. When the reset control logic detects that the external $\overline{RESET}$ is no longer being driven, it drives $\overline{RESET}$ low for an additional 512 cycles to guarantee this length of reset to the entire system.

If $\overline{RESET}$ is asserted from any other source, the reset control logic asserts $\overline{RESET}$ for a minimum of 512 cycles and until the source of reset is negated.

Figure 16 is a timing diagram of the power-up reset operation, showing the relationships between $\overline{RESET}$, V_{DD}, and bus signals. During the reset period, the entire bus (except for non-tri-statable signals, which are driven to their inactive state three-states. Once $\overline{RESET}$ negates, all control signals are driven to their inactive state, the data bus is in read mode, and the address bus is driven. After this, the first bus cycle for $\overline{RESET}$ exception processing begins.

$\overline{RESET}$ should be asserted for at least 590 clock periods to ensure that the MCU resets. Resetting the MCU causes any bus cycle in progress to terminate as if $\overline{DSACKx}$ or $\overline{BERR}$ has been asserted. In addition, the MCU initializes registers appropriately for a reset exception.

For further information refer to the System Integration Modul Manual.



Notes

1) Internal startup time.
2) SSP read here.
3) PC read here.
4) First instruction fetched here.

Figure 16 : Initial reset operation timing.

6.4 · System integration module

The TS 68332 system integration module (SIM) consists of five submodules that control the microcontroller unit (MCU) system start-up, initialization, configuration, and external bus with a minimum of external devices. The fives submodules that make up the SIM, shown in Figure 17, are as follows :

- System configuration and protection,
- Clock synthesizer,
- Chip selects,
- External bus interface,
- System test.

6.4.1 · System configuration and protection submodule

The SIM module allows the user to control some features of system configuration by writing bits in the Module Configuration Register. This register also contains read-only status bits that show the state of some of the SIM features.

This MCU is designed with the concept of providing maximum system safe-guards. Many of the functions that normally must be provided in external circuits are incorporated in this MCU. The features provided in the system configuration and protection submodule are as follows :

System configuration
The module configuration register allows the user to configure the system according to the particular system requirements.

Internal bus monitor
The MCU provides an internal bus monitor to monitor the $\overline{DSACKx}$ response time for all internal bus accesses. An option allows the monitoring of internal to external bus accesses. There are four selectable response times that allow for the response speed of peripherals used in the system. A bus error ($\overline{BERR}$) signal is asserted internally if the $\overline{DSACKx}$ response time is exceeded. When operating as a bus master, the $\overline{BERR}$ signal is not asserted externally.

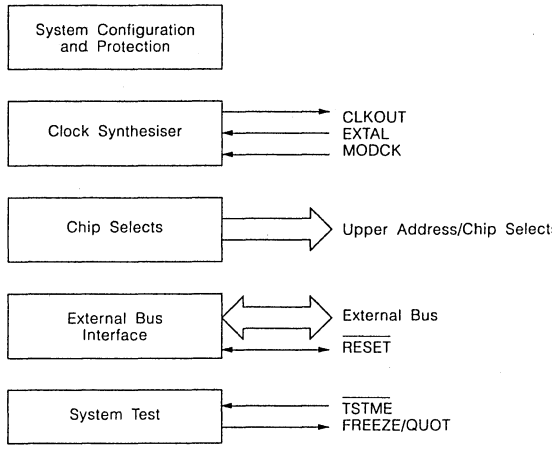


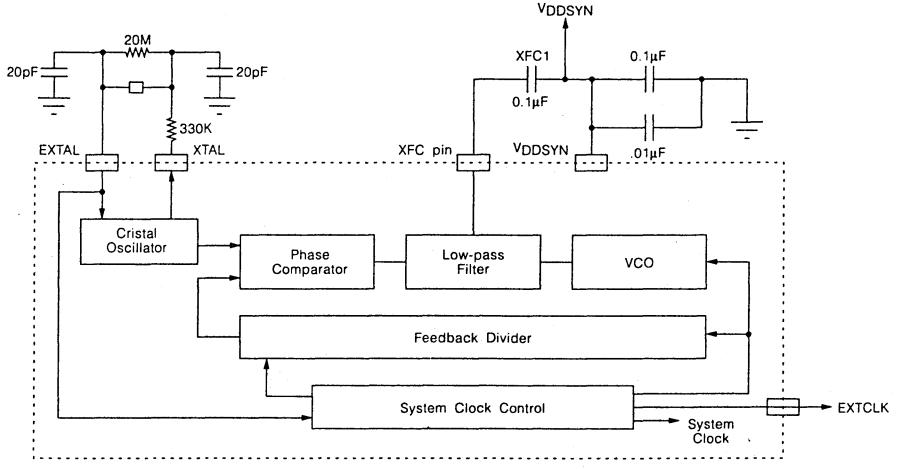
Figure 17 : System integration module block diagram.

Halt monitor
A halt monitor causes a reset to occur if the internal halt ($\overline{HALT}$) is asserted by the CPU.

Spurious interrupt monitor
If no interrupt arbitration occurs during an interrupt acknowledge (IACK) cycle, the $\overline{BERR}$ signal is asserted internally.

Software watchdog
The watchdog asserts $\overline{RESET}$ if the software fails to service the software watchdog for a designated period of time (presumably because it is trapped in a loop or lost). There are four selectable timeout periods, and a prescaler may be used for long timeout periods.

Periodic interrupt timer
The MCU provides a timer to generate periodic interrupts. The periodic interrupt time period can vary from 122 μs - 15.94 s (with a 32.768 kHz crystal used to generate the system clock).



Note : Must be low leakage capacitor.

Figure 18 : Clock submodule block diagram.

6.4.3 · Clock synthesiser

The clock synthesizer (Figure 18) can operate from an on-chip phase locked loop (PLL) using an external crystal connected between the EXTAL and XTAL pins as a reference frequency source. A 32.768 kHz watch crystal provides an inexpensive reference, but the reference crystal frequency can be any frequency from 25-50 kHz. Outside the 25-50 kHz range, an external oscillator can be used with the on-chip synthesiser and VCO, or the frequency can be driven directly into the EXTAL pin (the XTAL pin should be left floating for this case).

The system clock frequency is programmable from 131 kHz to the maximum clock frequency with a resolution of 131 kHz. A separate power pin (V_{DDSYN}) is used to allow the clock circuits to run with the rest of the MCU powered down and to provide increased noise immunity for the clock circuits. If for some reason the external crystal signal is removed from the device then the clock synthesiser will generate its own internal clock signal to allow the device to enter some kind of error recovery routine. This is known as LIMP mode. The clock frequency generated will not have an associated timing spec but should be around 9 MHz.

6.4.4 · Chip-select submodule

Typical microcomputer systems require external hardware to provide select signals to external peripherals. This MCU integrates these functions on-chip in order to provide the cost, speed, and reliability benefits of a higher level of integration. The chip-select signals can also be programmed as output enable, read or write strobe, or IACK signals.

Since initialization software would probably reside in a peripheral memory device controlled by the chip-select circuits, a CSBOOT register provides default reset values to support bottstrap operation.

The chip-select submodule supports the following programmable features :

Twelve programmable chip-select circuits
Twelve chip select signals are available ($\overline{CSBOOT}$ and $\overline{CS10}$ tro $\overline{CS0}$). These signals use the $\overline{CSBOOT}$ pin, bus arbitration pins $\overline{BR}$, $\overline{BG}$, and $\overline{BGACK}$, function code pins FC2-FC0, and address pins A23-A19. The $\overline{CSBOOT}$ pin is dedicated to a single function because it must function after a reset with no initialization, the other chip select circuits share functions on their output pins. All 12 chip select circuits are independently programmable from the same list of selectable features. Each chip select circuit has an individual base register and option register which contain the programmable characteristics of that chip select. Using these address lines as chip select signals does not restrict the large linear address space of the MCU since the chip select logic always uses the internal address lines.

Variable block sizes
The block size starting from the specified base address can be programmed as 2 K, 8 K, 16 K, 64 K, 128 K, 256 K, 512 Kbytes or 1 Mbyte.

Both 8-bit and 16-bit ports supported
Eight-bit ports are accessible on both odd and even addresses when connected to data bus bits 15-8. Sixteen-bit ports can be accessed as odd bytes, even bytes, or words.

Read only, write only, or read/write capability
Chip selects can be asserted synchronized with read, write, or both read and write.

Address strobe and data strobe timing option
Chip-select signals can be synchronized with either address strobe or data strobe, so that control signals such as output enable or write enable can be easily generated.

Internal $\overline{DSACK}$ generation with wait states
The port size programmed in the pin assignment register can be referenced for generating $\overline{DSACK}$ and the proper number of wait states for a particular device programmed by the user.

Address space checking
Supervisor, user, and CPU space accesses can be optionally checked.

Interrupt priority level checking
In the IACK cycle, the acknowledged interrupt level can be compared with the user-specified level programmed in the option field. If autovector option is selected, $\overline{AVEC}$ is internally asserted.

Discrete output
Port C pins A22-A19 and FC2-FC0 can be programmed for discrete output, with data stored in the pin data register (CSPDR).

68000-type peripheral support
6800-type peripherals that require an E clock for synchronization can be supported. Chip select is asserted, synchronized with the E clock on pin A23, providing correct data bus timing for the MCU.

6.4.5 · Test submodule

The test submodule is a primary tool to support all types of testing, such as production test and user self-test, that is integrated into the MCU. The submodule supports scan-based testing of the various modules in the MCU. The scan test employed here consists of the test submodule performing the following steps :

- serially shifting stimulus data to an idle module under test (MUT),
- activating the module under test,
- serially shifting response data back from the module under test,
- latching the response data for interrogation by the bus master.

The further information to the System Integration Module Manual.

6.5 · QSM Queued Serial Module

The queued serial module (QSM) provides the micro-controller unit (MCU) with two serial communication interfaces divided into two submodules : the queued serial peripheral interface (QSPI) and the serial communications interface (SCI). The QSPI is a full-duplex, synchronous serial interface for communicating with peripherals and other MCUs. It is enhanced by the addition of a RAM queue for receive and transmit data. The SCI is a full-duplex universal asynchronous receiver transmitter (UART) serial interface. These submodules operate independently (see Figure 19).

6.5.1 · QSM pins

The QSM has nine external pins. Eight of these pins can be used as general-purpose I/O pins, if the pin is not being user for its submodule function. The ninth pin, RXD, is an input-only pin used exclusively by the SCI submodule. The pins are identified as follows :

MISO - Master In Slave Out,

MOSI - Master Out Slave In,

SCK - Serial Clock,

PCS0/SS - Peripheral Chip Select 0/ Slave Select,

PCS3-PCS1 - Peripheral Chip Selects 3-1,

TXD - Transmit Data,

RXD - Receive Data.

6.5.2 · QSPI submodule

The QSPI submodule communicates with external peripherals and other MCUs via a synchronous serial bus. The QSPI is fully compatible with the serial peripheral interface (SPI) systems found on other TCS devices such as the 68HC11 and 68HC05 families. It has all of the capabilities of the standard SPI system as well as several new features. The following paragraphs describe the main features of the QSPI.

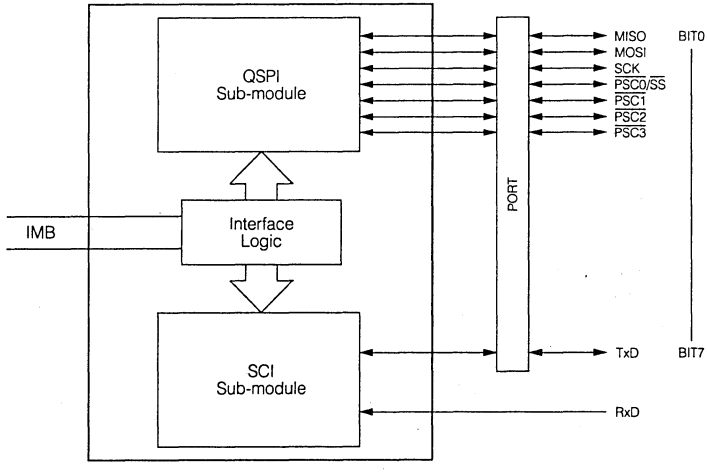


Figure 19 : QSM block diagram.

6.5.3 · QSPI features

Standard SPI features are listed below, followed by a list of the additional features offered on the QSPI :

- full duplex, three-wire synchronous transfers,
- half-duplex, two-wire synchronous transfers,
- master or slave operation,
- programmable master bit rates,
- programmable clock polarity and phase,
- end-of-transmission interrupt flag,
- master-master mode fault flag,
- easily interfaces to simple expansion parts (A/D converters, EEPROMs, display drivers, etc.).

6.5.3.1 - QSPI enhanced features

Programmable queue
A programmable queue allows the QSPI to perform up to 16 serial transfers without CPU intervention. Each transfer corresponds to a queue entry containing all the information needed by the QSPI to independently complete one serial transfer. This unique feature greatly reduces CPU/QSPI interaction, resulting in increased CPU and system throughput.

Once the CPU has set up the queue of QSPI commands and enabled the QSPI, the QSPI operates independently of the CPU. The QSPI executes all of the commands in its queue, sets a flag indicating that it has finished, and then either interrupts the CPU or waits for CPU intervention.

Programmable peripheral chip selects
Four peripheral chip-select pins allow the QSPI to access up to 16 independent peripherals by decoding the four peripheral chip-select signals. Up to four independent peripherals can be selected by direct connection to a chip-select pin. The peripheral chip selects simplify interfacing to two or more serial peripherals by providing dedicated peripheral chip-select signals and thus alleviating the need for CPU intervention.

Wraparound transfer mode
Wraparound transfer mode allows for automatic, continuous re-execution of the preprogrammed queue entries.Newly transferred data replaces previously transferred data. Wraparound simplifies interfacing with A/D converters by automatically providing the CPU with the latest conversions in the QSPI RAM. Consequently, serial peripherals appear as memory-mapped parallel devices to the CPU.

Programmable transfer length
The number of bits in a serial transfer is programmable from 8 to 16 bits, inclusive. For example, 10 bits could be used for communicating with an external 10-bit A/D convertor. Likewise, a vacuum fluorescent display driver might require a 12-bit serial transfer. The programmable length simplifies interfacing to serial peripherals that require different data lengths.

Programmable transfer delay
An inter-transfer delay may be programmed from approximately 1 to 500 μs (using a 16.78 MHz system clock). For example, an A/D convertor may require time between transfers to complete a new conversion. The default delay is 1 μs. The programmable length of delay simplifies interfacing to serial peripherals that require delay time between data transfers.

Programmable queue pointer
The QSPI has a pointer that points to the queue location containing the data for the next serial transfer. The CPU can switch from one task to another in the QSPI by writing to the queue pointer, changing the location in the queue that is to be transferred next. Otherwise, the pointer increments after each serial transfer. By segmenting the queue, multiple-task support can be provided by the QSPI.

Continuous transfer mode
The continuous transfer mode allows the user to exchange an uninterrupted bit stream with a peripheral. A minimum of 8 bits and a maximum of 256 bits may be transferred in a single burst without CPU intervention. Longer transfers are possible ; however, minimal CPU intervention is required to prevent loss of data. A 1 microsecond pause (using a 16.78 MHz system clock) is inserted between each entry transfer.

QSPI RAM
The QSPI uses an 80-byte block of dual-access static RAM that can be accessed by both the QSPI and the CPU. Because of sharing, the length of time taken by the CPU to access the QSPI RAM, when the QSPI is enabled, may be longer than when the QSPI is disabled. From one to four CPU wait states may be inserted by the QSPI in the process of reading or writing.

The RAM is divided into three segments : receive data, transmit data, and command control. Receive data is information received from a serial device external to the MCU. Transmit data is information stored by the CPU for transmission to an external peripheral chip. Command control contains all the information needed by the QSPI to perform the transfer. Figure 20 illustrates the organization of the RAM.

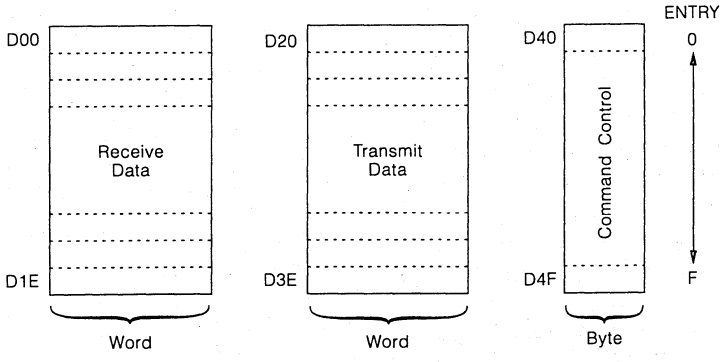


Figure 20 : Organization of the QSPI RAM.

6.5.4 · SCI Submodule

The SCI submodule is used to communicate with external devices and other MCUs via an asynchronous serial bus. The SCI is fully compatible with the SCI systems found on other TCS MCUs such as the 68HC11 and 68HC05 Families. It has all of the capabilities of previous SCI systems as well as several significant new features.

6.5.4.1 · Features

Standard SCI features are listed below, followed by a list of additional features offered :

Standard SCI two-wire systems features
- standard Non Return to Zero (NRZ) mark/space format,
- advanced error detection mechanism (detects noise duration up to 1/16 of a bit-time),
- full-duplex operation,
- software selectable word length (8- or 9-bit words),
- separate transmitter and receiver enable bits,
- may be interrupt driven,
- four separate interrupt enable bits.

Standard SCI receiver features
- receiver wake up function (idle or address mark bit),
- idle-line detect,
- framing error detect,
- noise detect,
- overrun detect,
- receive data register full flag.

Standard SCI transmitter features
- transmit data register empty flag,
- transmit complete flag,
- send break.

QSM-enhanced SCI two-wire systems features
- 13-bit programmable baud rate modulus counter,
- even/odd parity generation and detection.

QSM-enhanced SCI receiver features
- two idle-line detect modes,
- receiver active flag.

13-bit programmable baud rate modulus counter
A baud rate modulus counter has been added to provide the user with more flexibility in choosing the crystal frequency for the system clock. The modulus counter allows the SCI baud rate generator to produce standard transmission frequencies for a wide range of system clocks. The user is no longer constrained to select crystal frequencies based on the desired serial baud rate. This counter provides baud rates from 64 baud to 524 baud with a 16.78 MHz system clock.

Even/odd parity generation and detection
The user now has the choice either of seven or eight data bits plus one parity bit, or of eight or nine data bits with no parity bit. Even or odd parity is available. The transmitter automatically generates the parity bit for a transmitted byte. The receiver detects when a parity error has occured on a received byte and sets a parity error flag.

Two idle-line detect modes
Standard TCS SCI systems detect an idle line when 10 or 11 consecutive bit-times are all ones. Used with the receiver wake up mode, the receiver can be awakened permaturely if the message preceding the start of the idle line contained ones in advance of its stop bit. The new (second) idle-line detect mode only starts counting idle time after a valid stop bit is received, which ensures correct idle-line detection.

Receiver Active Flag (RAF)
RAF indicates the status of the receiver. It is set when a possible start bit is detected and is cleared when an idle line is detected. RAF is also cleared if the start bit is determined to be line noise. This flag can be used to prevent collisions in systems with multiple masters.

For further information refer to the System Integration Module Manual.

6.6 · Standby RAM (with TPU emulation)

The TS 68332 contains 2 K bytes of standby RAM. This section describes the operation and control of the RAM module.

6.6.1 · Overview

The RAM module contains 2048 bytes of fully static RAM, powered by V_{DD} in normal operation. The entire array may be used as standby RAM if power is supplied to the V_{STBY} pin. Switching between V_{DD} and V_{STBY} occurs automatically.

The RAM may be used as general-purpose memory for the microntroller unit (MCU), providing fast, two-clock accesses to the CPU. Typically, the RAM is used for program control stacks and frequently modified data variables. The CPU may read or write byte, word, or long-word data.

The RAM may also be used as microcode control memory for the time processor unit (TPU). The TPU must be placed in emulation mode to use the RAM in this manner which allows users to develop their own TPU microcode primitives.

6.6.2 · RAM array addressing

The RAM array can be placed anywhere in the address map of the MCU by means of the array base address (RAMBAR), provided that it is placed on a 2 kbyte boundary and does not overlap the three RAM module control registers used for control and testing. RAMBAR can be written only once after reset. This prevents the RAM array from being accidentally remapped by software.

6.6.3 · TPU emulation mode operation

The RAM array may be used as the microcode control store for the TPU module. This mode of operation is selected from whithin the TPU. See **Development support** in the TPU manual for a complete description.

The TPU is connected to the RAM via a dedicated bus. While in emulation mode, the access timing of the RAM module matches the timing of the TPU microinstruction ROM to ensure accurate emulation. Normal accesses via the IMB are inhibited and the control register have to effect, allowing external RAM to emulate the 2 K RAM array at the same addresses.

The further information refer to the System Integration Module Manual.

6.7 · TPU overview

The time processing unit (TPU) performs simple as well as complex timing tasks, independently from the CPU, making it the latest advance in timer systems. Viewed as a special purpose microcomputer, this processor performs two operations, match and capture, on one operand : TIME. Every occurrence of either action is called an event. The servicing of these events by the TPU replaces the servicing of interrupts by the host central processing unit (CPU). The timing functions currently synthesized are the following :

- discrete input/output,
- input capture/input transition counter,
- output compare,
- pulse width modulation,
- synchronised pulse width modulation,
- period measurement with additional transition detect,
- period measurement with missing transition detect,
- position-synchronized pulse generator,
- stepper motor,
- period/pulse-width accumulator.

The advanced TPU affords for the first time high-resolution timing and multiple time function capability (flexibility) in the timer system pins.

6.7.1 · High-resolution timing

High-resolution timing is limited by CPU overhead required for servicing timing tasks such as period measurement, pulse measurement, pulse-width modulated waveform generation, etc. On the TPU, high-resolution timing is achieved by two main capabilities :

- reduced latency,
- reduced service time, which free the CPU to focus on other responsibilities.

The TPU provides a higher resolution than the CPU could achieve, and creates no CPU overhead for servicing timing tasks.

6.7.1.1 · Latency

Latency is the interval of time from an even to the start of event servicing. The ability of the TPU to service its own interrupts or events reduces latency and the CPU is not required to service each input transition capture that occurs on a pin, or to determine each match time required for waveform synthesis. Once configured by the host CPU, the self-contained TPU performs complex time functions requiring high resolution with little or no CPU intervention.

6.7.1.2 · Service time

Service time is the time expended servicing an event. In older microcontroller unit (MCU) timer functions, the service time is constrained because the MCU instruction set is not optimized for time function synthesis. The TPU instruction set is optimized, and time functions are synthesized with fewer instructions than the CPU. Instructions execute faster and service time is reduced. Instructions executed by the TPU are not user software, but firmware, special-purpose microcode written by TCS to perform as set of time functions. Microcode is placed into the TPU control store (ROM) when the device is manufactured.

6.7.2 · Features

- 16 channels ; each channel associated with a pin.
- Each channel can perform any time function,
- Each time function may be assigned to more than one channel at a given time.
- Each channel has an event register comprised of the following :
  - 16-bit capture register,
  - 16-bit compare/match register,
  - 16-bit greater-than or equal-to comparator.
- Each channel can be synchronized to one or both of the two 16-bit free-runnning timer count registers (TCR1 and TCR2).

– TCR1 is clocked from the output of a prescaler. The prescaler's input is the internal TPU system clock divided by either 4 or 32. The four settings of the prescaler are divide by 1, 2, 4 and 8. Channels using TCR1 have the capability to resolve down to the TPU system clock divided by four.

– TCR2 is clocked from the output of a prescaler. The prescaler's input is the external TCR2 pin. The four settings of the prescaler are divide by 1, 2, 4 and 8. Channels using TCR2 have the capability to resolve down to the TPU system clock divided by 8.

– TCR2 may be used as a hardware pulse accumulator clocked from the external TCR2 pin, or as a gated pulse accumulator of the clock that increments TCR1.

– All channels have at least six 16-bit parameter registers. Channels 14 and 15 each have eight 16-bit parameter registers. All parameter registers are contained in a dual-port RAM, accessible from both the TPU and CPU.

– A scheduler with three priority levels segregates high, middle, and low-priority time functions. Any channel may be assigned to one of these three priority levels.

– All time functions are microcoded.

– Emulation and development support is provided for all time function features such as breakpoint, freeze and single step, giving internal register accessibility.

– Coherent transfer capability for two parameter is provided in hardware.

– Coherent transfer capability for N parameters may be performed as a TPU microcode function. (Refer to Development support in the TPU reference manual for further details on this feature).

6.7.3 · General concept

The TPU is an intelligent, semi-autonomous peripheral dedicated to timing control. Its intelligence enables the servicing of timing events without CPU intervention. This device uses a private microengine for a processor, a scheduler, input/output channels, ROM instructions, and shared-access data RAM to operate independently and simultaneously with the CPU (see Figure 21). Consequently, the setup and service time for each timer event is minimized.

A «time-of-delay» approach is used where all time functions are related to one of two 16-bit free-running TCRs. Time functions are synthesized by combining the two time primitives, match and capture events. By performing these time primitives in hardware, the TPU can precisely determine the time when a match event is to occur and then specify the state of the output pin accordingly. The TPU can also accurately record the time at which an input transition occurs and can perform calculations based on the time of the occurence. An event register for each channel provides for simultaneity of match/capture-event occurences on all channels.

When a match or input capture event requiring service occurs on a channel, the channel generates a service request to the scheduler. The scheduler prioritizes the request with other pending service requests. When the microengine is idle, the scheduler causes the microengine to execute a microcode sequence. When the microengine is busy, the new sequence begins when the code being executed ends. The microengine performs the function, which is defined by the content of the control store, using parameters from the parameter RAM and from the event registers, etc., as needed. Following is an example.

Channel X is generating a periodic waveform and presently the output is high. When the value of the TCR used by that channel increments to match the value of the event register of channel X, a match event occurs. The event switches the output to low and generates a new service request to the scheduler. The scheduler then schedules and initiates service of channel X by the microengine.

When execution of the sequence begins, the microengine uses the execution unit :

– to obtain (from the parameter RAM) the value representing the duration of counts for which channel X should remain low, and

– to add to this value the value from the content of the event register of channel X. The content of the event register is then replaced by this sum ; the channel control is set for a match event on the same TCR ; and the pin control is set to cause the output pin for channel X to switch high when the event occurs. A channel interrupt, which signals the end of service to the CPU, may be asserted (if the time function provides for it and the interrupt is enabled). The microengine is then free to service the next event determinated by the scheduler.

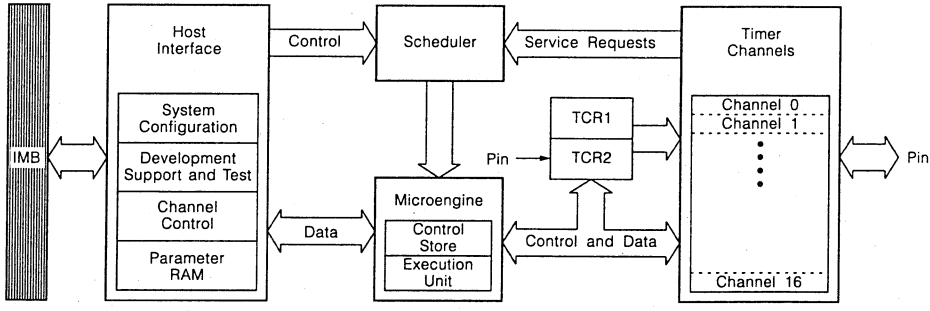


Figure 21 : TPU simplified block diagram.

6.7.4 · Flexibility

The TPU has the flexibility to be configured to directly solve the user's timer requirements. This flexibility is attained through five capabilities :

- channel orthogonality,
- inter-channel communication,
- programmable channel service priority,
- selection of timing functions,
- emulation capability.

6.7.4.1 · Channel orthogonality

Traditionally, timer systems have been limited by the specific functions of channel pins dedicated to perform time functions such as input capture, output compare, or pulse accumulation. All channels of the TPU contain identical hardware and are functionally equivalent in operation, such that any channel can be configured to perform any time function. The user controls the combination of time functions ; the only constraint is the number of pins available for timing functions.

6.7.4.2 · Inter-channel communication

The TPU's ability service itself requires a continuous flow of direct and indirect communication. Direct communication is accomplished through a «change channel» feature in which any channel of the TPU can operate an another channel to affect its state. Indirect communication is provided by a link feature in which any channel can lonk to one more channels, including itself, to signal a need for future service. As a result, the user can reference the operation of one channel to the occurrence of a specific action on another channel.

6.7.4.3 · Programmable channel service priority

Applications may require different priorities of event service. The channel service priority may be programmed to one of three levels : high, middle, and low. The scheduler allows calculation of worst-case latency for event servicing and ensures servicing of all channels by preventing permanent blockage.

6.7.4.4 · Selection of timing functions

The available timing functions can be programmed to operate on any channel. Parameter registers associated with each channel are used as general-purpose time operands.

6.7.4.5 · Emulation capability

The TPU cannot resolve all timer problems using predefined time functions alone ; therefore, development of user-defined time functions is allowed in emulation mode. Using the RAM module of the MCU as a «writable control store» provides TPU emulation. In TPU emulation mode, an auxiliary bus connection is made between the RAM module and the TPU module, and access to the RAM module via the intermodule bus is disabled. A 9-bit address bus, a 32-bit data bus, and control lines transfer information between the modules. To ensure exact emulation, the access timing of the RAM module remains consistent with the TPU ROM control store.

6

6.7.5 · Applications

The TPU's high speed, versatile architecture, and time functions facilitate its use in many control applications, such as stepper motors and angle-based engine control. Control of a stepper motor or an angle-based automotive engine usually requires high CPU overhead. These applications show how the SM, PMA/PPM, and PSP time functions minimize the overhead associated with these applications, and provide sophistication and flexibility for a wide variety of applications.

Further detailed information on the TPU is found in the TPU reference manuel.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510.

7.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or TCS standard and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

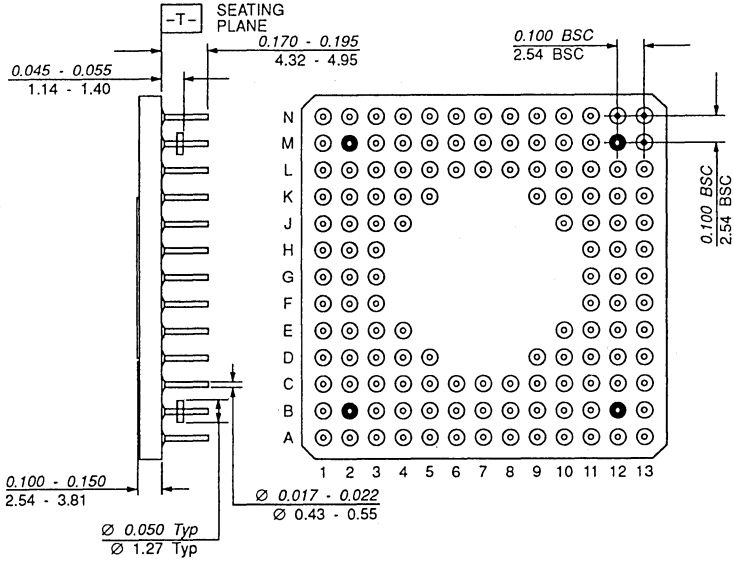
8 · HANDLING

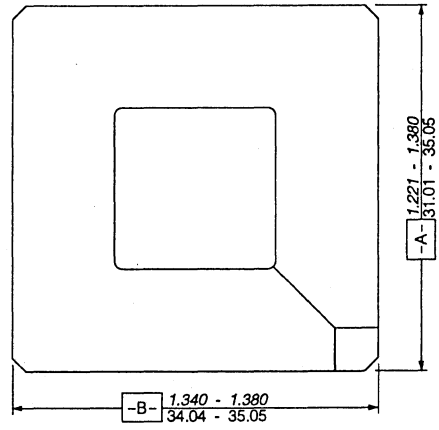
MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devise should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if practical.

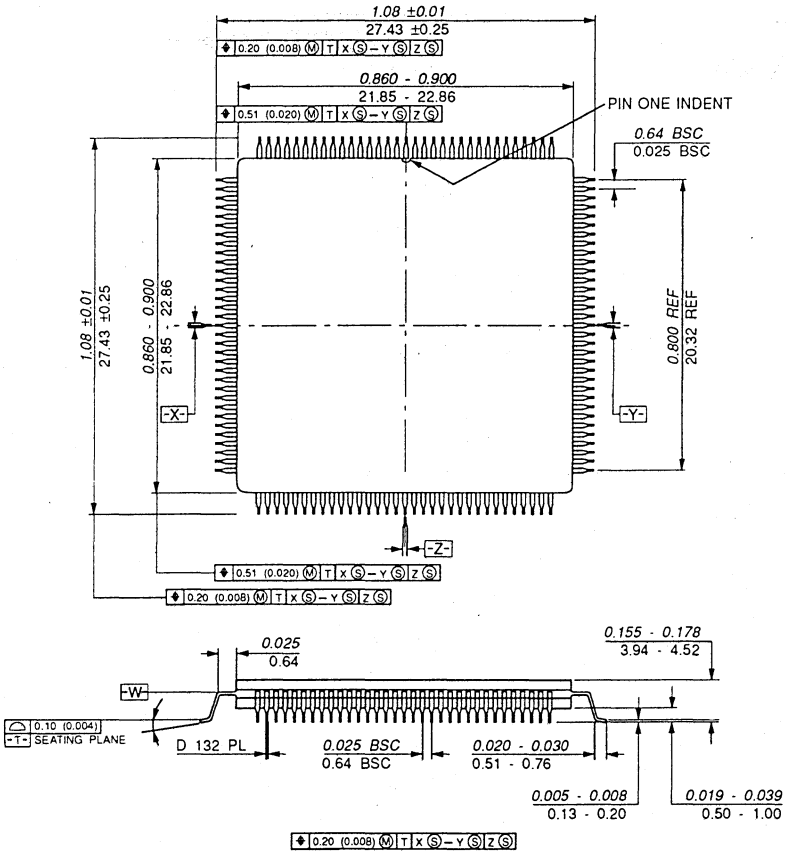
9 - PACKAGE MECHANICAL DATA

9.1 - 132 pins - Ceramic Pin Grid Array





9.2 · 132 pins · Ceramic



Note 1 : Dimensionning and tolerancing per ansi Y14.5M, 1982.
Note 2 : Controlling dimensions : inch.
Note 3 : Dim A and B define maximum ceramic body dimensions including glass protrusion and mismatch of ceramic body top and bottom.
Note 4 : Datum plane - W - is located at the underside of leads where leads exit package body.
Note 5 : Datums X-Y and Z to be determined where center leads exit package body at datum - W -.
Note 6 : Dim S and V to be determined at seating plane, datum - T -.
Note 7 : Dim A and B to be determined at datum plane - T -.

10. · TERMINAL CONNECTIONS

10.1 · 132 pins · Ceramic Pin Grid Array

See Figure 2.1 page 4.

10.2 · 132 pins · Ceramic Leaded Chip Carrier

See Figure 2.2 page 4.

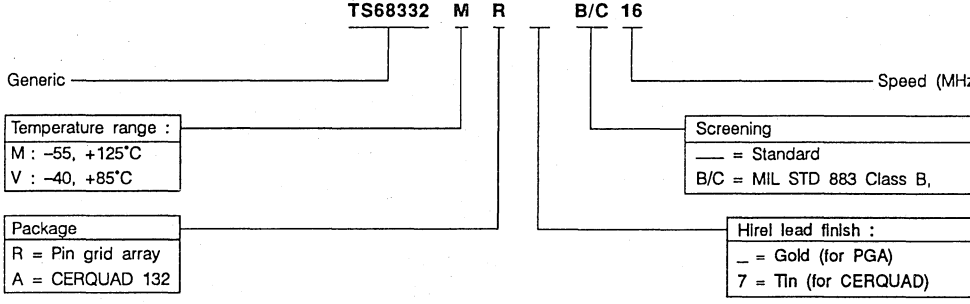
11 - ORDERING INFORMATION

11.1 - Hi-REL product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68332MRB/C16	MIL-STD-883	PGA 132	−55 / +125	16.78	TCS data-sheet
TS68332MA7B/C16	MIL-STD-883	CERQUAD 132	−55 / +125	16.78	TCS data-sheet
TS68332DESCxC	DESC	PGA 132	−55 / +125	16.78	5962-91501
TS68332DESCxA	DESC	CERQUAD 132	−55 / +125	16.78	5962-91501
TSX68332MRD/T	BURNIN	PGA 132	−55 / +125	16.78	TCS data-sheet
TSX68332MA7D/T	BURNIN	CERQUAD 132	−55 / +125	16.78	TCS data-sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPEFICIQUES.					

11.2 - Standard product

Commercial TCS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
TS68332VR16	TCS Standard	PGA 132	−40 / +85	16.78	TCS data-sheet
TS68332MR16	TCS Standard	PGA 132	−55 / +125	16.78	TCS data-sheet
TS68332VA16	TCS Standard	CERQUAD 132	−40 / +85	16.78	TCS data-sheet
TS68332MA16	TCS Standard	CERQUAD 132	−55 / +125	16.78	TCS data-sheet
TSX68332MR16	BURNIN	PGA 132	−55 / +125	16.78	TCS data-sheet
TSX68332MA16	BURNIN	CERQUAD 132	−55 / +125	16.78	TCS data-sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					



ADVANCE INFORMATION

TS68EN360

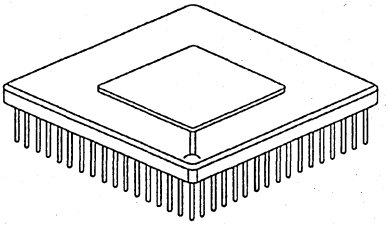
32:BIT QUAD INTEGRATED COMMUNICATION CONTROLLER

DESCRIPTION

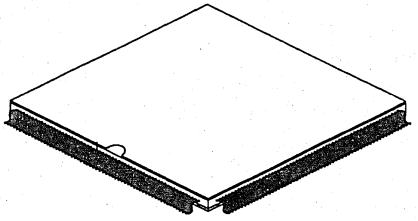
The TS 68360 QUad Integrated Communication Controller (QUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities. The QUICC (pronounced "quick") can be described as a next-generation TS 68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration. The term "quad" comes from the fact that there are four serial communications controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one seral peripheral interface (SPI).

MAIN FEATURES

- CPU32+ Processor (4.5 MIPS at 25 MHz)
  - 32-Bit Version of the CPU32 Core (Fully Compatible with the CPU32)
  - Background Debug Mode
  - Byte-Misaligned Addressing
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)
- Up to 32 Address Lines (At Least 28 Always Available)
- Complete Static Design (0-25 MHz Operation)
- Slave Mode To Disable CPU32+ (Allows Use with External Processors)
  - Multiple QUICCs Can Share One System Bus (One Master)
  - TS68040 Companion Mode Allows QUICC To Be an TS68040 Companion Chip and Intelligent Peripheral (22 MIPS at 25 MHz)
- Four General-Purpose Timers
  - Superset of MC68302 Timers
  - Four 16-Bit Timers or Two 32-Bit Timers
  - Gate Mode Can Enable/Disable Counting
- Two Independent DMAs (IDMAs)
- System Integration Module (SIM60)
- Communications Processor Module (CPM)
- Four Baud Rate Generators
- Four SCCs (Ethernet/IEEE 802.3 Optional on SCC1-Full 10-Mbps Support)
- Two SMC
- V_{CC} = +5 V ± 5 %
- f_{max} = 25 MHz
- Military temperature range : –55°C < T_C < +125°C
- P_D = 1.8 W



R suffix
PGA 241
Ceramic Pin Grid Array
Cavity down



A suffix
CERQUAD 240
Ceramic Leaded Chip Carrier

SCREENING / QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 (class B)
- DESC (planned)
- or according to TCS standard

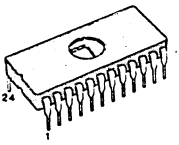
6

MEMORIES

7

16K (2K × 8) NMOS UV ERASABLE PROM

- 2048 × 8 ORGANIZATION
- 525 MW MAX ACTIVE POWER, 132 MW MAX STANDBY POWER
- LOW POWER DURING PROGRAMMING
- ACCESS TIME M/ET2716-1, 350ns; M/ET2716, 450ns
- SINGLE 5V POWER SUPPLY
- STATIC-NO CLOCKS REQUIRED
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- EXTENDED TEMPERATURE RANGE (F6)



Q/F
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M/ET2716 is high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M/ET2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

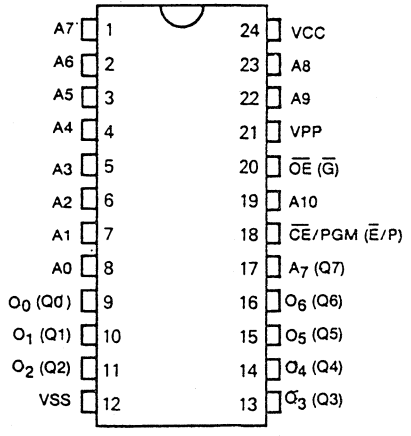
This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

PIN NAMES

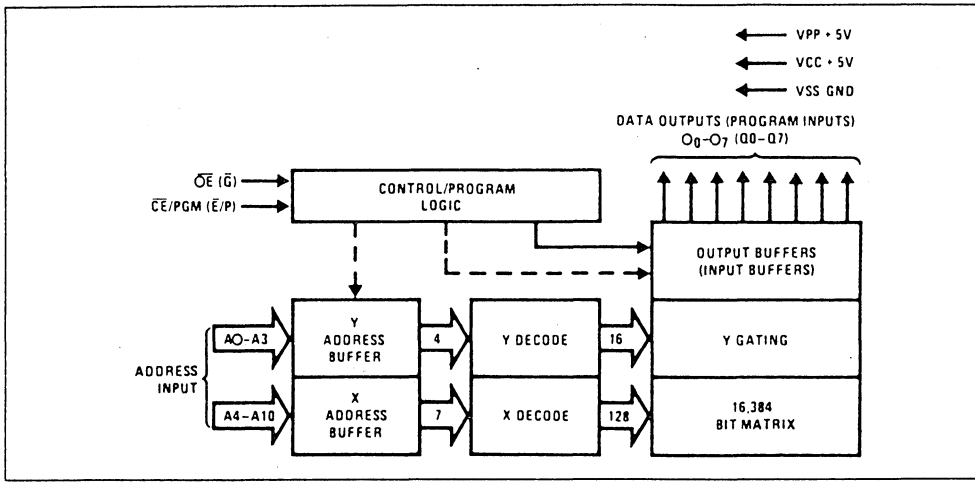
A0—A10	ADDRESS INPUTS
O_0—O_7 (Q0—Q7)	DATA OUTPUTS
$\overline{CE}$/PGM ($\overline{E}$/P)	CHIP ENABLE/PROGRAM
$\overline{OE}$ (G)	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	POWER (5V)
V_{SS}	GROUND

Note: Symbols in parentheses are proposed JEDEC standard

PIN CONNECTIONS



BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}/PGM$ ($\overline{E}/P$) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	5	5	D_{OUT}
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

* Symbols in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias (Extended Temperature Range)	−10 to +80 (−50 to +95)	°C °C
T_{stg}	Storage Temperature	−65 to +125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to −0.3	V
V_{in}	All Input or Output Voltages with Respect to V_{SS}	6V to −0.3	V
P_D	Power Dissipation	1.5	W
	Lead Temperature (Soldering 10 seconds)	+300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS[1] $T_A = 0°C$ to $+ 70°C$[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current	$V_{IN} = 5.25V$ ORVIN $= V_{IL}$	—	—	10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$, $\overline{CE}/PGM = 5V$	—	—	10	µA
I_{PP1}	V_{PP} Supply Current	$V_{PP} = 5.25V$	—	—	5	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{CE}/PGM = V_{IH}$, $\overline{OE} = V_{IL}$	—	10	25	mA
I_{CC2}	V_{CC} Supply Current (Active)	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	—	57	100	mA
V_{IL}	Input Low Voltage		−0.1	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC}+1$	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$ C[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified).

Symbol		Parameter	Test Conditions	M/ET2716-1		M/ET2716		Unit
Standard	Jedec			Min.	Max.	Min.	Max.	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	—	350	—	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$	—	120	—	120	ns
t_{DF} (Note 5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}/PGM = V_{IL}$	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}/PGM = \overline{OE} = V_{IL}$	0	—	0	—	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE} = V_{IL}$	0	100	0	100	ns

CAPACITANCE [4] $T_A = 25°C$, $f = 1$ MHz

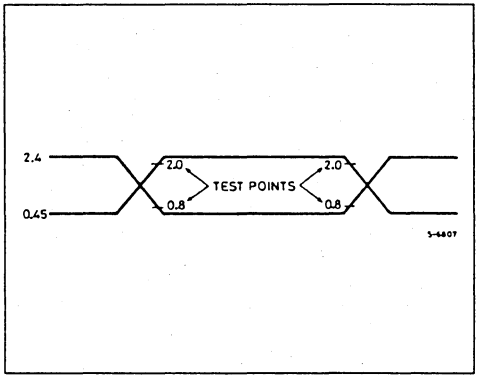
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. VCC must be applied at the same time or before VPP and removed after or at the same time as V_{PP}
2. Typical conditions are for operation at: T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = OV
3. VPP may be connected to VCC except during program.
4. Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz.
5. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ wich ever occurs first. This parameter as only sampled and not 100% tested.
6. T_A = − 40°C To + 85°C for the F6 version (extended To range).

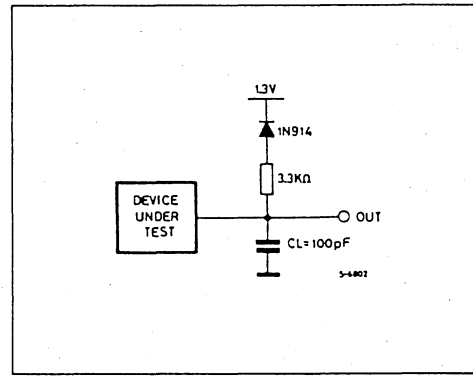
AC TEST CONDITIONS

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times ≤ 20 ns
Input pulse levels: 0.45V to 2.4V
Timing Measurement Reference Level
Inputs, Outputs 0.8V and 2V

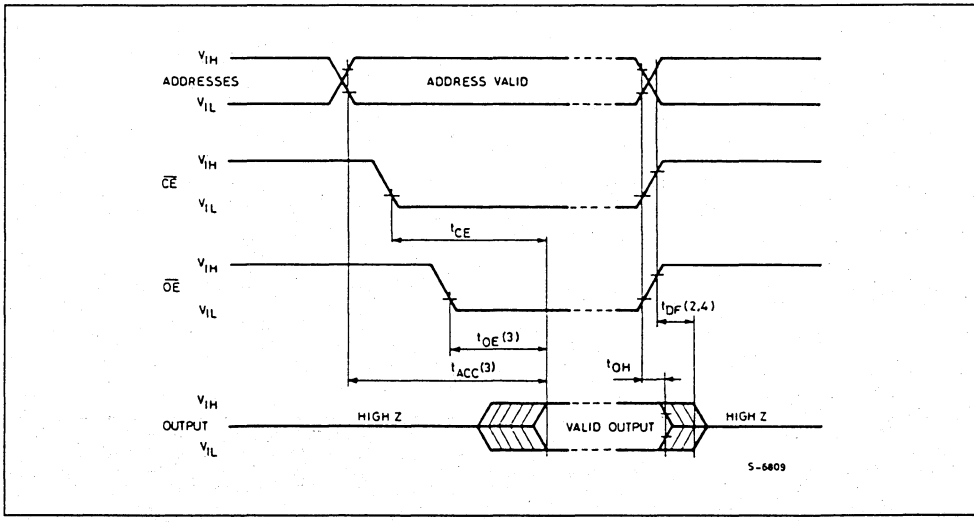
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The M/ET2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

READ MODE

The M/ET2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PCM = VIL and that addresses A0 – A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on wich is limiting.

DESELECT MODE

The M/ET2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the adresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more M/ET2716's for memory expansion.

STANDBY MODE (Power Down)

The M/ET2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintened at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The M/ET2716 is shipped from SGS-THOMSON-completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The M/ET2716 is programmed by introducing "0" s into the desidered locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is:

TABLE I. OPERATING MODES ($V_{CC} = V_{PP} = 5V$)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	D_{OUT}
DESELECT	Don't Care	V_{IH}	Hi-Z
STANDBY	V_{IH}	Don't Care	Hi-Z

With V_{PP} = 25V, VCC = 5V, $\overline{OE}$ = V_{IH} and $\overline{CE}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins. (V_{IL} = "0" and V_{IL} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. M/ET2716's may be programmed in parallel with the same data in this mode.

PROGRAM VERIFY MODE

The programming of the M/ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with V_{PP} = 25V (or 5V) in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several M/ET2716's simultaneously with different data for each one by controlling wich ones receive the program pulse. All similar inputs of the M/ET2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = V_{IH} will put its outputs in the Hi-Z state.

TABLE II. PROGRAMMING MODES ($V_{CC} = 5V$)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	OUTPUTS 9—11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25(5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

ERASING

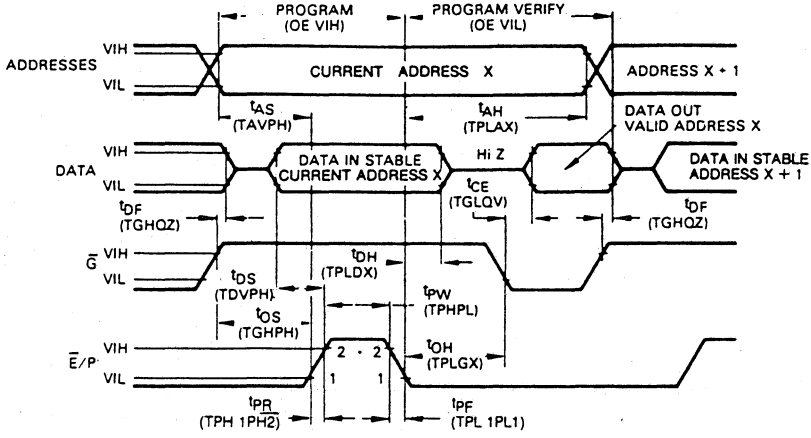
The M/ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M/ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 A yelding a total integrated dosage of 15 watt-seconds/cm² power rating is used. The M/ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

TIMING DIAGRAM

PROGRAM MODE



Note: Symbols in parentheses are proposed JEDEC standard

PROGRAMMING OPERATION

DC AND OPERATING CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$) Notes 1 and 2

Symbol	Parameter	Min.	Max.	Units
I_{LI}	Input Leakage Current (Note 3)	—	10	μA
V_{IL}	Input Low Level	−0.1	0.8	V
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V
I_{CC}	V_{CC} Power Supply Current	–	100	mA
I_{PP1}	V_{PP} Supply Current	—	5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse (Note 5)	—	30	mA

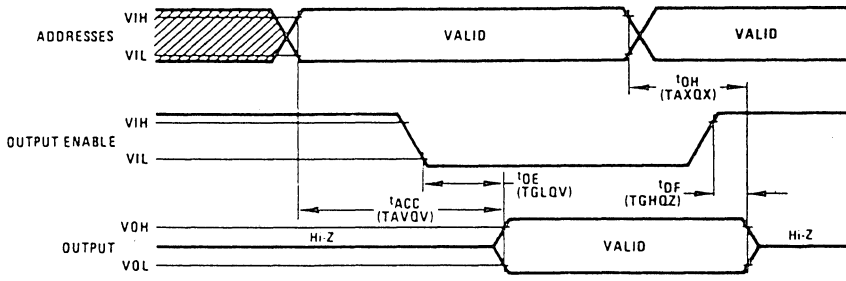
AC CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$) Notes 1, 2 and 6

Symbol		Parameter	Min.	Typ.	Max.	Units
Standard	Jedec					
t_{AS}	TAVPH	Address Setup Time	2	—	—	μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2	—	—	μs
t_{DS}	TDVPH	Data Setup Time	2	—	—	μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2	—	—	μs
t_{DH}	TPLDX	Data Hold Time	2	—	—	μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0	—	100	ns
t_{OE}	TGLQV	Output Enable to Output Delay (Note 4)	—	—	120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5	—	—	ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5	—	—	ns

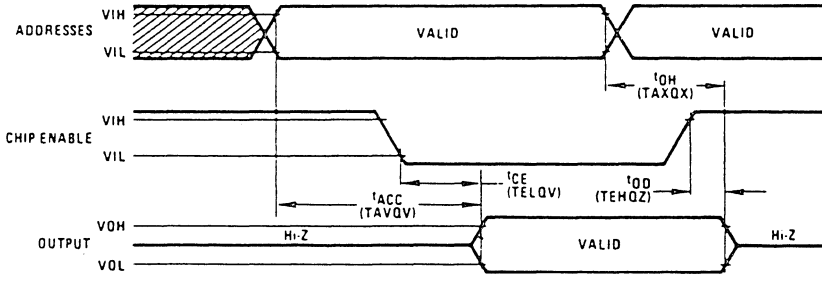
Notes 1. VCC must be applied at the same time of before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be insereted into a board with power applied.
2. Care must be taken to prevent overshoot of the VPP supply when switching + 25V
3. $0.45V \leq VIN < 5.25V$
4. CE/PGM = VIL, VPP = VCC
5. VPP = 26 V
6. Transition times ≤ 20 ns unless otherwise noted

SWITCHING TIME WAVEFORMS

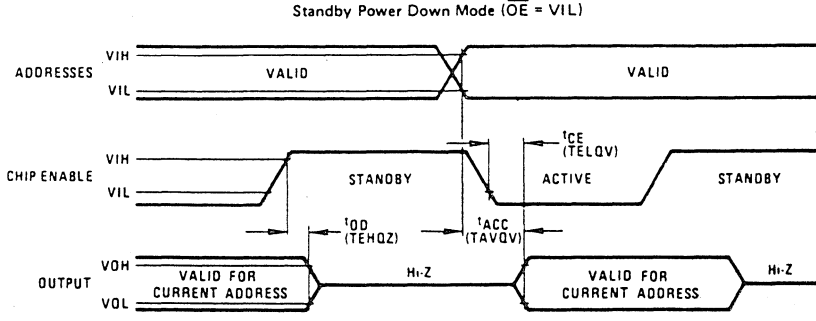
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



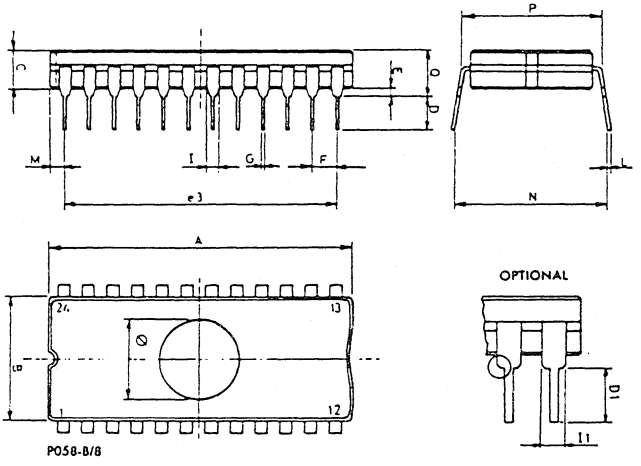
Symbols in parentheses are proposed JEDEC standard

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ET2716Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ET2716-Q1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F1	450 ns	5V ± 5%	0 to +70°C	DIP-24
M2716-1F1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F6	450 ns	5V ± 5%	−40 to +85°C	DIP-24
M2716-1F6	350 ns	5V ± 10%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1(1)	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1(1)	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

Note: 1. Optional see drawing

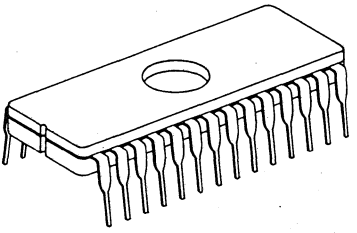
CMOS 65, 536 BIT (8192 x 8) UV ERASABLE PROM MEMORY

DESCRIPTION

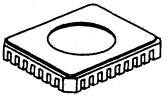
The 27C64 is a high-speed 64 K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The 27C64 is packaged in a 28-pin dual-in-line or 32-pad LCCC, with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

All inputs/outputs are fully TTL compatible.



28 pins CERDIP / Q suffix



32 pins LCCC / EQ suffix

MAIN FEATURES

- Fast access time = 250 ns and 300 ns.
- Compatible to high speed microprocessors zero wait state.
- 28-pin / 32-pin JEDEC approved pin-out.
- Low power consumption :
  active : 30 mA (max)
  standby : 1 mA (max)
- Programming voltage : 12.5 V.
- High speed programming (< 1 minute).
- Electronic signature.
- Also available in (OTP) version on request (One Time Programming).
- Military temperature range :
  T_C = −55°C / +125°C.
- Power supply : V_{CC} = 5 V_{DC} ± 10 %.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 B.
- TMS STANDARD.

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The 27C64 series are 65, 536-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using. HCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use fo external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C64 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (Q suffix) and LCCC (EQ suffix) rated for operation from $-55°C$ to $+125°C$.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C64. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C64 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 165 mW at 5 V.

Maximum standby power dissipation : 6 mW at 5 V.

This memory has static operation : no clocks no refresh.

Max access / Min cycle time :
27C64-25 : 250 ns 27C64-30 : 300 ns.

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

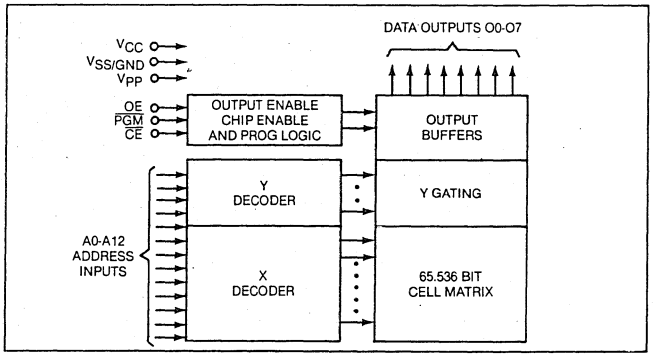
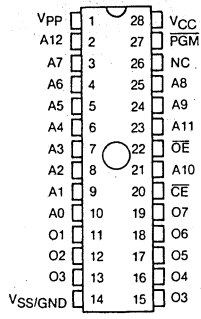


FIGURE 1 - 27C64 BLOCK DIAGRAM.

2 - PIN ASSIGNEMENTS

CERDIP PACKAGE



LCCC PACKAGE

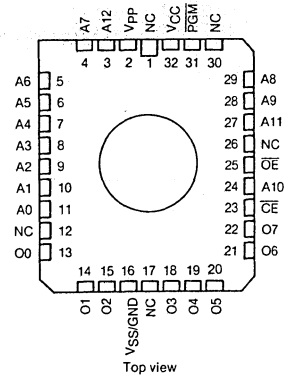


FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbol of each terminal of the device are given in the Figure 3 below.

A0-A12	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0-O7	Outputs
$\overline{PGM}$	Program
NC	Non Connected

FIGURE 3

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C64, in compliance either with MIL-STD-883 class B rev C or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

2.2 - CECC 90000

1) CECC 90000
2) Specification 9011x-0xx

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510, Tin Dipped.

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 28 lead DIL : dual in line D.10
- 32 lead LCCC : C 12A rectangular leadless chip carrier.

The precise case outlines are described into MIL-M-38510.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 1 - Absolute maximum ratings

Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Figure 3.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		−0.6	7	V
V_{PP}	Programming supply voltage		−0.6	14	V
V_I	Input voltage	(Except A9)	−0.6	6.5	V
		(A9)	−0.6	13.5	V
V_O	Output voltage		−0.6	V_{CC} +1	V
V_{OZ}	Off-state voltage		−0.6	V_{CC} +1	V
I_O	Output current			5	mA
I_I	Input current			15	mA
P_D max.	Max. power dissipation			165	mW
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−65	+150	°C
T_{lead}	Lead temperature (soldering : 10 s)			+300	°C

Note : «Maximum ratings» are those values beyond which the safety of the device cannot be guaranteed. Except for «Operating temperature range» they are not meant to imply that the devices should be operated at these limits. The table of «Electrical characteristics» provides conditions for actual device operation.

3.3.2 - Recommanded conditions of use

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

All voltages are referenced to a reference terminal (V_{SS}, GND, etc...).

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} +1	V
T_{case}	Operating temperature	−55	+125	°C

3.4 · Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
CERDIP DIL 28		**Thermal resistance - Ceramic**		
	θ_{J-A}	Junction-to-Ambient	60	°C/W
	θ_{J-C}	Junction-to-Case	12	°C/W
LCCC 32		**Thermal resistance - Ceramic**		
	θ_{J-A}	Junction-to-Ambient	73	°C/W
	θ_{J-C}	Junction-to-Case	20	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883 (non applicable)

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 9011x-0xx. Group C inspection is performed on a periodic basis in accordance with CECC 9011x-0xx.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 4 : Static electrical characteristics for the electrical variants.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Table 5).

5.2 - Static characteristics

All voltages are referenced to GND.

Table 4

$-55°C < T_{case} < +125°C$ $V_{CC} = 5\ V \pm 10\ \%$ $V_{SS} = 0\ V$

Symbol	Parameter	Condition	Min	Max	Unit
I_{CC1}	Maximum supply current(s) for – Normal mode	V_{CC} max. Minimum cycle time		30	mA
I_{CC2} TTL / CMOS	– Power down	V_{CC} max.		1 / 100	mA / µA
V_{IH}	High level input voltage	V_{CC}	2	$V_{CC}+1$	V
V_{IL}	Low level input voltage	V_{CC}		0.8	V
V_{OH}	High level output voltage (Note 2)	V_{CC} I_{OHA}	2.4		V
V_{OL}	Low level output voltage (Note 2)	V_{CC} I_{OLA}		0.45	V
I_{IH}	High level input or leakage current	V_{CC} max. V_{IHB}		10	µA
I_{IL}	Low level input or leakage current	V_{CC} max. V_{ILA}		10	µA
I_{OH}	High level output current (Note 2)	V_{CC} V_{OHB}	400		µA
I_{OL}	Low level output current (Note 2)	V_{CC} V_{OLA}		2.1	mA
I_{OHZ}	High level output leakage current at three-state outputs (Note 2)	V_{CC} V_{OHB}		10	µA
I_{OLZ}	Low level output leakage current at three-state outputs (Note 2)	V_{CC} V_{OLA}		10	µA
I_{OS}	Output short circuit current (Notes 1 and 2)	V_{CC} $V_O = 0$		NA	mA
V_{PP}	V_{PP} read voltage	$V_{CC} - 0.7$	—	V_{CC}	V
I_{PP1}	V_{PP} read current ($V_{PP} = V_{CC} = 5.5\ V$)		—	100	µA

Note 1 : One input in turn during 1 s.
Note 2 : For measurement of this characteristic it may be necessary to programme the device.

5.3 · Dynamic characteristics

Table 5

V_{CC} = 5 V ± 10 % $-55°C \leqslant T_C < +125°C$

Symbol	Parameter	Test conditions	27C64 -25		27C64 -30		Unit
			Min	Max	Min	Max	
t_{ACC}	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		300	ns
t_{EC}	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		250		300	ns
t_{OE}	Output enable to output delay	$\overline{CE} = V_{IL}$		100		120	ns
t_{DF}	$\overline{OE}$ or $\overline{CE}$ high to output float (Notes 1 and 2)		0	60	0	105	ns
t_{OH}	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

Note 1 : The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured $V_{OH}(DC) - 0.1$ V.
Low to THREE-STATE, the measured $V_{OL}(DC) + 0.1$ V.

Note 2 : t_{DF}, is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100 % tested.

5.4 · AC test conditions specific to the device

Output load ..... 1 TTL gate and CL = 100 pF
Input rise and fall times ..... ⩽ 20 ns
Input pulse levels ..... 0.45 V to 2.4 V
Timing measurement reference level inputs, outputs ..... 0.8 V and 2 V

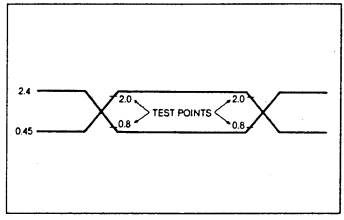


FIGURE 4 - AC TESTING INPUT / OUPUT WAVEFORM.

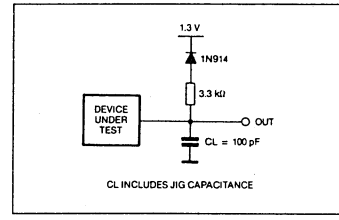
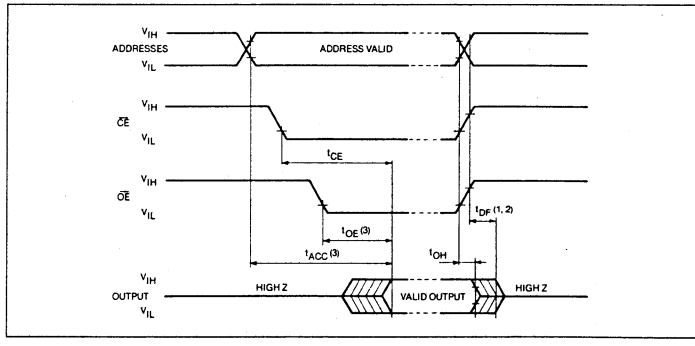


FIGURE 5 - AC TESTING LOAD CIRCUIT.



Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.

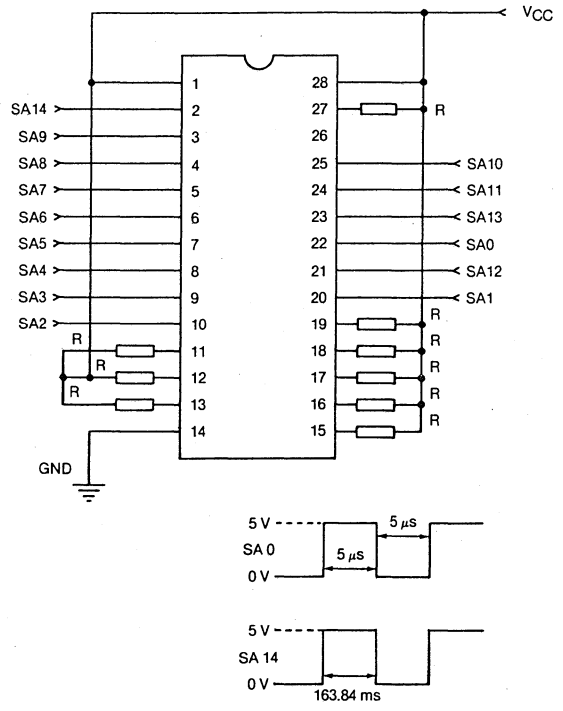
FIGURE 6 - AC WAVEFORMS.

5.5 · Capacitance

Table 6 (See note)

Symbol	Parameter	Min	Typ	Max	Unit
C_{in}	Input capacitance (V_{in} = 0 V)	—	4	6	pF
C_{out}	Output capacitance (V_{out} = 0 V)	—	8	12	pF
Note : Capacitance is guaranteed by periodic testing. T_{amb} = 25°C, f = 1 MHz.					

5.6 · Burn-in conditions



R = 3 kΩ
SA0 = 10 µs
SA1 = 20 µs
SA2 = 40 µs
SA3 = 80 µs
SA4 = 160 µs
SA5 = 320 µs
SA6 = 640 µs
SA7 = 1,28 ms
SA8 = 2,56 ms
SA9 = 5,12 ms
SA10 = 10,24 ms
SA11 = 20,48 ms
SA12 = 40,96 ms
SA13 = 81,92 ms
SA14 = 163,84 ms

FIGURE 7

6 · FUNCTIONAL DESCRIPTION

6.1 · Device operation

The seven modes of operation of the 27C64 are listed in the Operating Modes table. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Read mode

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for a least t_{ACC}-t_{CE}.

Standby mode

The 27C64 has a standby mode which reduces the maximum power dissipation to 5.5 mW. The 27C64 is placed in the standby mode by applying a TTL high signal to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{CE}$ input.

Output or-tying

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation, and

b) complete assurance that output contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

6.2 · Programming modes

Caution : Exceeding 14 V on pin 1 (V_{PP}) will damage the 27C64.

Initially, and after each erasure, all bits of the 27C64 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be presented in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure.

The 27C64 is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. It is required that a 0.1 μF capacitor be placed across V_{PP}. V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple 27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel 27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled 27C64s.

High speed programming

The high speed programming algorithm described in the flow chart rapidity programs 27C64 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

Program inhibit

Programming of multiple 27C64s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other 27C64s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 27C64s may be common. A TTL low-level pulse applied to a 27C64 $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5 V will program that 27C64.

Program verify

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5 V.

Electronic signature mode

Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the 27C64. To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 (pin 24) of the 27C64. Two bytes may then be sequenced from the device outputs by toggling address line AO (pin 107) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

Table 7 : Table of the programming characteristics to apply

DC programming characteristics

V_{CC} = 6 V ±0.25 V ; T_{amb} = +25°C ±5°C ; V_{pp} = 12.5 V ±0.3 V (See note)

Symbol	Parameter	Min	Typ	Max	Unit
I_I	Input current (all inputs - V_I = V_{IL} or V_{IH}	—	—	10	µA
V_{IL}	Input low level (all inputs)	−0.1	—	0.8	V
V_{IH}	Input high level	2.0	—	V_{CC} +1	V
V_{OL}	Output low voltage during verify (I_{OL} = 2.1 mA)	—	—	0.45	V
V_{OH}	Output high voltage during verify (I_{OH} = −400 µA)	2.4	—	—	V
I_{CC3}	V_{CC} supply current (program & verify)	—	—	30	mA
I_{PP2}	V_{PP} supply current (program - $\overline{CE}$ = V_{IL} = $\overline{PGM}$)	—	—	30	mA

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC programming characteristics

V_{CC} = 6 V ±0.25 V ; T_{amb} = +25°C ±5°C ; V_{pp} = 12.5 V ±0.3 V (See note 1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{AS}	Address set-up time	2	—	—	µs
t_{OES}	OE set-up time	2	—	—	µs
t_{DS}	Data set-up time	2	—	—	µs
t_{AH}	Address hold time	0	—	—	µs
t_{DH}	Data hold time	2	—	—	µs
t_{DF}	Output enable to output float delay	0	—	130	ns
t_{VPS}	V_{PP} set-up time	2	—	—	µs
t_{VCS}	V_{CC} set-up time	2	—	—	µs
t_{PW}	$\overline{PGM}$ initial program pulse width	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ overprogram pulse width (Note 2)	2.85	—	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	2	—	—	µs
t_{OE}	Data valid from $\overline{OE}$	—	—	1.50	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : t_{OPW} is defined in flow chart.

7

6.3 · High speed programming

6.3.1 · Flow chart

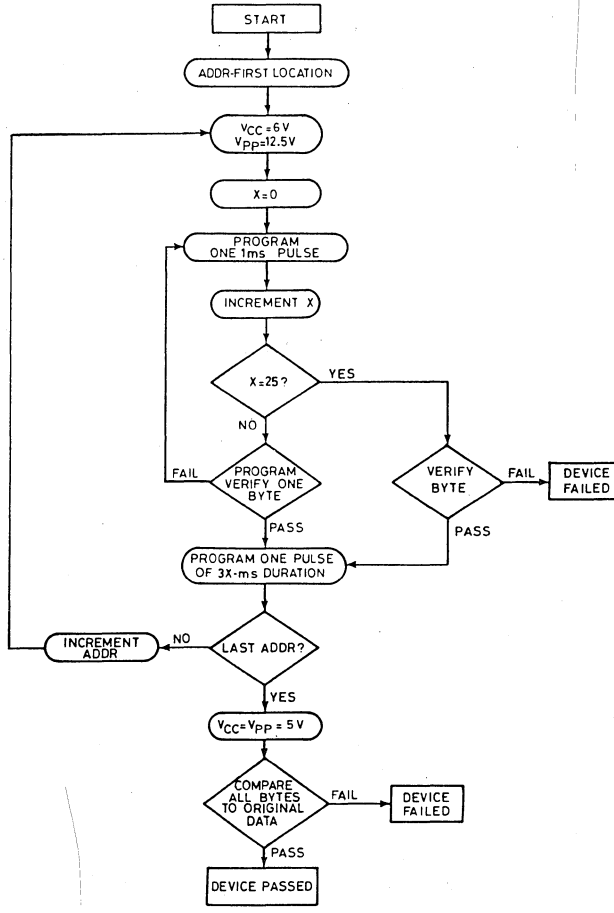
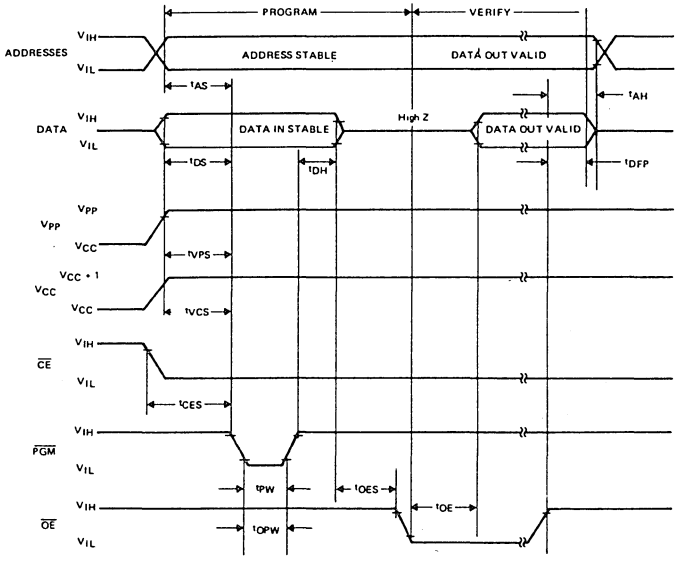


FIGURE 8

6.3.2 - Wave forms



Note 1 : The input timing reference level is 0.8 V for V_{IL} and 2.0 V for V_{IH}.

Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Note 3 : When programming 27C64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 9 - HIGH SPEED PROGRAMMING WAVE FORMS

7

6.4 - Erasing

The 27C64 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the 27C64 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if this product is to be operated under these lighting conditions. Coverting the window also reduces ICC due to photodiode currents. An ultraviolet source of 2537A yielding a total integrated of dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12.000 μW/cm² power rating is used. The 27C64 to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The disance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have ben erroneously suspected when incomplete erasure was the basic problem.

6.5 · Function table

Table 8

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13 15-19)
Read	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	D_{OUT}
High speed programming	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
Electronic signature (Note 1)	V_{IL}	V_{IL}	V_H (Note 2)	V_{IH}	V_{CC}	V_{CC}	CODE

Note 1 : All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code : 9B) to V_{IH} (type code : 08).
Note 2 : $V_H = 12.0\ V \pm 0.5\ V$.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

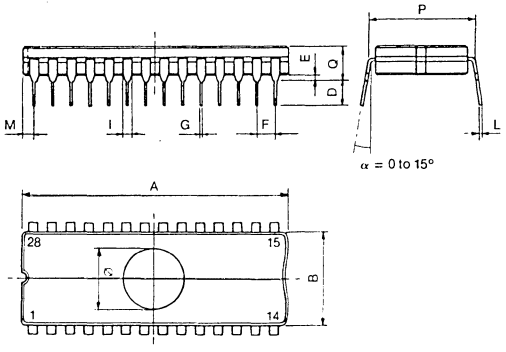
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent if practical.

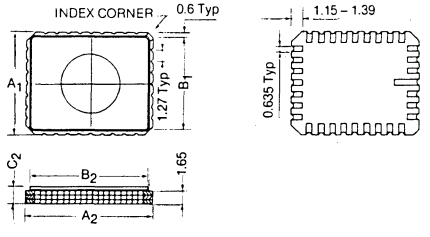
9 - PACKAGE MECHANICAL DATA

9.1 - DIL CERDIP with window package 28 pins



Symbol	Millimeters		
	Min	Typ	Max
A			37.85
B	12.7		15.49
D	3.81		
E	0.38		1.52
F	2.29		2.79
G	0.35		0.58
I	0.96		1.65
L	0.20		0.33
M			2.54
P	14.98		15.75
Q			5.89
∅		7.11	

9.2 - 32 pins leadless chip carrier



Symbol	Millimeters	
	Min	Max
A_1	11.23	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92

7

10 - ORDERING INFORMATION

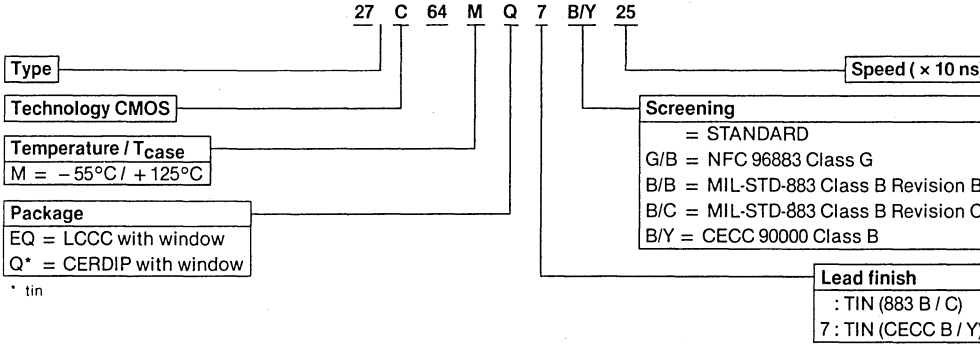
10.1 - HI-REL product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (ns)	Drawing number
27C64MQG/B25	NFC 96883 - Class G	Cerdip 28	−55 / +125	250	Data sheet
27C64MQG/B30	NFC 96883 - Class G	Cerdip 28	−55 / +125	300	Data sheet
27C64MQB/B25	MIL-STD-883 B - Class B	Cerdip 28	−55 / +125	250	Data sheet
27C64MEQ1B/B25	MIL-STD-883 B - Class B	LCCC 32	−55 / +125	250	Data sheet
27C64MQB/C25	MIL-STD-883 C - Class B	Cerdip 28	−55 / +125	250	Data sheet
27C64MEQ1B/C25	MIL-STD-883 C - Class B	LCCC 32	−55 / +125	250	Data sheet
27C64MQ7B/Y25	CECC 90000	Cerdip 28	−55 / +125	250	CECC 90113-00x
27C64MEQ7B/Y25	CECC 90000	LCCC 32	−55 / +125	250	CECC 90113-00x

(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

10.2 · Standard product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (ns)	Drawing number
27C64MQ25	TMS Standard	Cerdip 28	−55 / +125	250	Internal
27C64MQ30	TMS Standard	Cerdip 28	−55 / +125	300	Internal
27C64MEQ25	TMS Standard	LCCC 32	−55 / +125	250	Internal
(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					



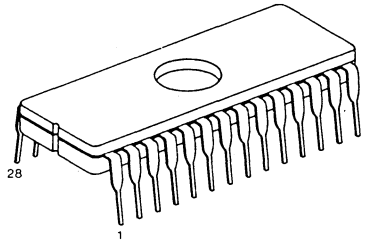
256 K (32 K x 8) CMOS UV ERASABLE PROM

DESCRIPTION

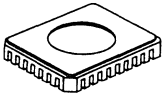
The 27C256 is a high speed 262, 144 bit ultraviolet erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The 27C256 is packaged in 28 pin Window Ceramic Freat Seal package (Cerdip). The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

All inputs/outputs are fully TTL compatible.



Q suffix
28 pins CERDIP
Dual in line glass sealed package



EQ suffix
32 pins LCCC
(Leadless Ceramic Chip Carrier with window)

MAIN FEATURES

- Organized 8 K x 8 : JEDEC Standard Pinouts :
  - 28 Pin Dual in Line Package,
  - 32 Pin Chip Carrier (Leadless Ceramic).
- Very fast access time : 150, 200 and 250 ns.
- Compatible to high speed microprocessors zero wait state.
- Low «CMOS» consumption :
  - active current : 100 mA max,
  - standby current : 1 mA max.
- Programming voltage : 12.5 V.
- Electronic signature for automated programming.
- Programming times in the 3 seconds range (PRESTO II algorithm).
- Military temperature range : $T_C = -55, +125°C$.
- Power supply : 5 V_{DC} ± 10 %.
- Also available in OTP version on request (One Time Programmable).

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- TMS STANDARD.
- MIL-STD-883C (to be introduced).

7

SUMMARY

A · GENERAL DESCRIPTION

INTRODUCTION

The following characteristics shall apply over the full operating temperature range and the supply voltage range V_{CC} = 5 V ± 10 %.

The 27C256 series are 262, 144-bit, ultraviolet-light, erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (Q suffix) and LCCC (EQ suffix) rated for operation from − 55°C to + 125°C for T_C.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C256. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C256 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 250 mW at 5 V at $T_C \geq 25°C$ / 500 mW at 5 V at $T_C < 25°C$.

Maximum standby power dissipation : 5 mW at 5 V.

This memory has static operation : no clocks no refresh.

Max access / Min cycle time :
27C256-15 : 150 ns
27C256-20 : 200 ns
27C256-25 : 250 ns

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 · DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

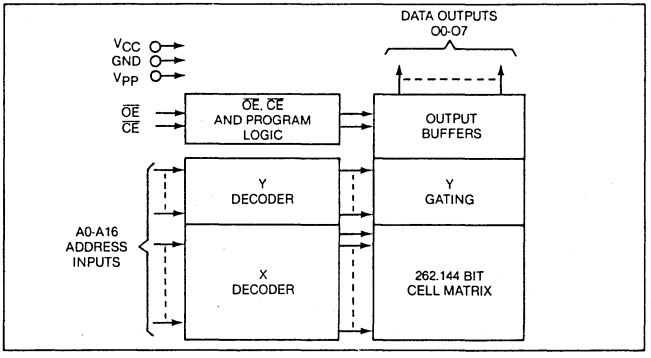
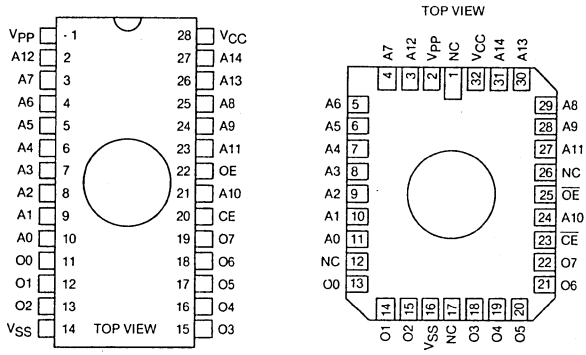


FIGURE 1 · 27C256 BLOCK DIAGRAM.

2 - PIN ASSIGNEMENTS



• Pin 1 indicator on top of package.

FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbols of each terminal of the device are given in the Figure 3 below.

A0-A14	Address Input
CE	Chip Enable Input
OE	Output Enable
O0-O7	Data Input / Output
NC	Non Connected

FIGURE 3 - PIN FUNCTION.

4 - OPERATING MODES

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A9	VPP	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output disable	L	H	X	V_{CC}	High Z
Standby	H	X	X	V_{CC}	High Z
Program	L	H	X	V_{PP}	D_{IN}
Program verify	H	L	X	V_{PP}	D_{OUT}
Program inhibit	H	H	X	V_{PP}	High Z
Electronic signature	L	L	V_H	VCC	CODE

Notes : X = Don't care ; V_H = 12 V ±0.5 V ; H = High ; L = Low.

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C256 150 ns, 200 ns and 250 ns access time with MIL-STD-883 class B rev C or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883 (non applicable)

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

2.2 - CECC 90000

1) CECC 90000
2) Specification 90113-001 UTEC 86-252-001

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 3.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510.

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- Cerdip 28
- 32 LCCC with window.

The precise case outlines are described into MIL-M-38510.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 1 - Absolute maximum ratings
Unless otherwise stated all voltages are referenced to the reference terminal as defined in Figure 3 of this specification.
Limiting conditions (ratings) are not for inspection purposes.
All voltages are referenced to GND.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		−0.6	7	V
V_{PP}	Programming supply voltage		−0.6	14	V
V_I	Input voltage	(Except A9)	−0.6	6.5	V
		(A9)	−0.6	13.5	V
V_O	Output voltage		−0.6	V_{CC} +1	V
V_{OZ}	Off-state voltage		−0.6	V_{CC} +1	V
I_O	Output current			5	mA
I_I	Input current			15	mA
P_D max.	Max. power dissipation			550	mW
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−65		°C

Note : Stresses above those listed under «Absolute maximum ratings» may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3.2 - Recommanded conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined is this specification in guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

Table 2 - Recommended conditions of use
All voltages are referenced to a reference terminal (V_{SS}, GND, etc...)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} +0.5	V
T_{case}	Operating temperature	−55	+125	°C

3.4 · Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
CERDIP DIL 28	θ_{J-A} θ_{J-C}	**Thermal resistance - Ceramic** Junction-to-Ambient Junction-to-Case	 55 10	 °C/W °C/W
LCCC 32	θ_{J-A} θ_{J-C}	**Thermal resistance - Ceramic** Junction-to-Ambient Junction-to-Case	 60 15	 °C/W °C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 - QUALITY CONFORMANCE INSPECTION

4.1 - DESC / MIL-STD-883 (non applicable)

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 90113-001. Group C inspection is performed on a periodic basis in accordance with CECC 90113-001.

5 - ELECTRICAL CHARACTERISTICS

5.1 - General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below :

- Table 4 : Static electrical characteristics.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

5.2 - Static characteristics

$V_{CC} = 5.0\ V_{dc} \pm 10\ \%$; GND = $0\ V_{dc}$; $T_C = -55 / +125°C$

All voltages are referenced to GND.

Table 4

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = 5.5\ V$		10	µA
I_{LO}	Output leakage current	$V_{OUT} = 5.5\ V$		10	µA
I_{CC1}	V_{CC} active current $\overline{CE} = \overline{OE} = V_{IL}$ to f = 8 MHz	V_{CC} max I_{OUT} = 0 mA (open output) - T < 25°C - T ⩾ 25°C		 100 50	 mA mA
I_{CC2}	V_{CC} standby current	$CE = V_{IH}$, V_{CC} max		1	mA
I_{PP1}	V_{PP} read current	$V_{PP} = V_{CC}$		0.1	mA
V_{IL}	Input low voltage	V_{CC}		0.8	V
V_{IH}	Input high voltage	V_{CC}	2		V
V_{OL}	Output low voltage (see Note)	$I_{OL} = 2.1\ mA$		0.45	V
V_{OH}	Ouput high voltage (see Note)	$I_{OH} = -400\ \mu A$	2.4		V
Note : For measurement of this characteristic it may be necessary to programme the device.					

5.3 - Dynamic characteristics

$V_{CC} = 5.0\ V_{dc} \pm 10\ \%$; GND = $0\ V_{dc}$; $T_C = -55 / +125°C$

Table 5

Symbol	Parameter	V_{CC} ±10 %	27C256-15		27C256-20		27C256-25		Unit
		Test conditions	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address access time	$\overline{CE} = \overline{OE} = V_{IL}$ (see Note 1)		150		200		250	ns
t_{CE}	Chip enable access time	$\overline{OE} = V_{IL}$ (see Note 1)		150		200		250	ns
t_{OE}	Output enable access time	$\overline{CE} = V_{IL}$ (see Note 1)		50		60		70	ns
t_{DF}	Output disable float time	(see Note 2)	0	40	0	50	0	60	ns
t_{OH}	Output hold time	$\overline{CE} = \overline{OE} = V_{IL}$ (see Note 1)	0		0		0		ns

Note 1 : Loading circuit (see Figure 4) input pulse levels : 0 V to 3 V.
Note 2 : t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whatever occurs first.

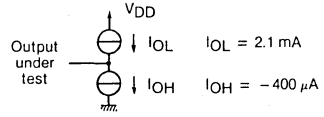


FIGURE 4 - AC LOADING CIRCUIT.

5.4 · AC test conditions specific to the device

Input rise and fall times ..... ⩽ 20 ns
Input pulse levels ..... 0 V to 3 V
Timing measurement reference level inputs, outputs ..... 0.8 V and 2 V

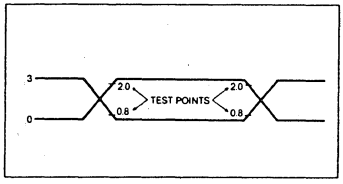


FIGURE 5 - AC TESTING INPUT / OUPUT WAVEFORM.

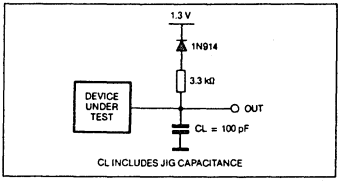
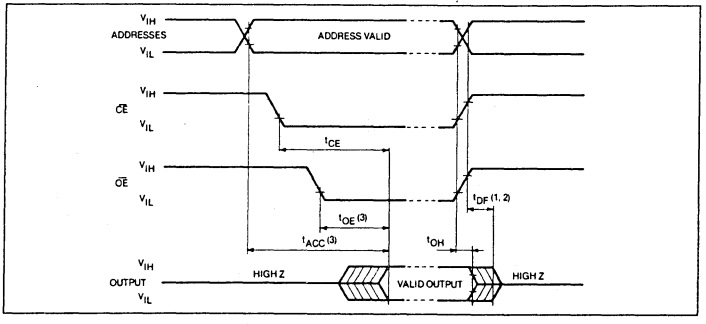


FIGURE 6 - AC TESTING LOAD CIRCUIT.



Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.

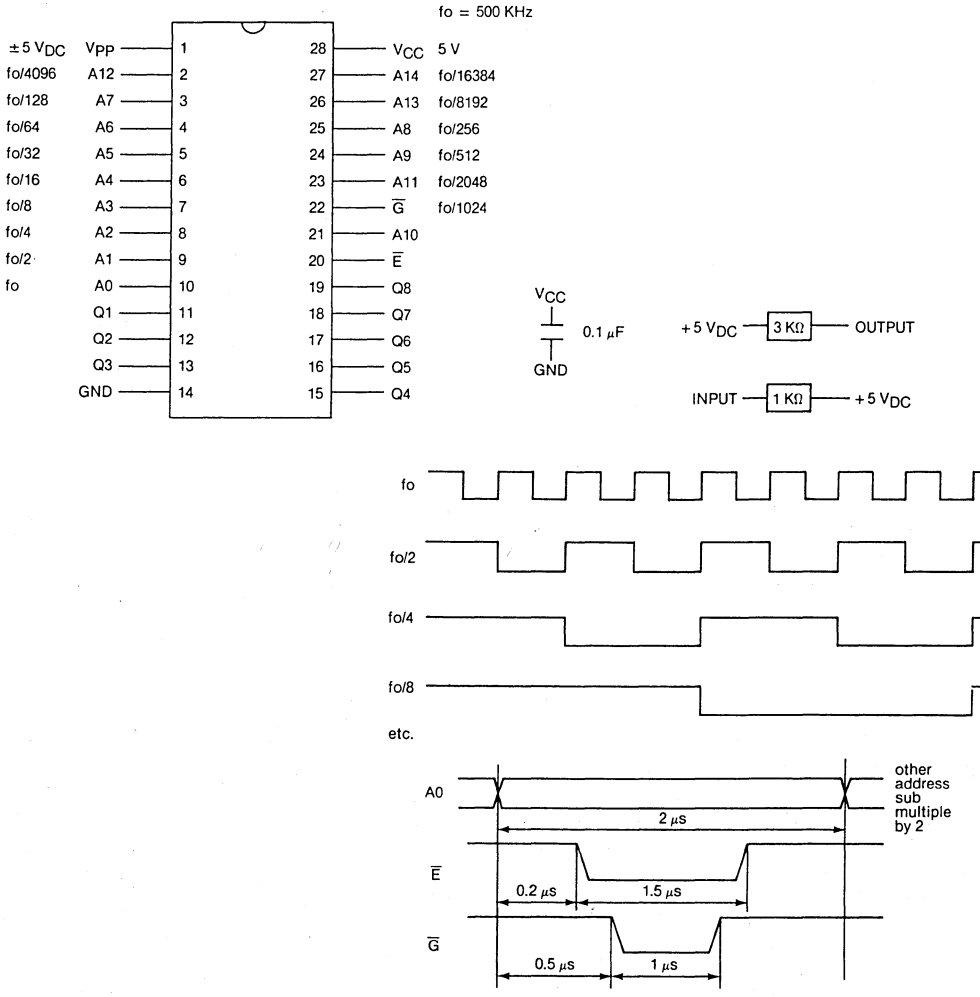
FIGURE 7 - AC WAVEFORMS.

5.5 · Capacitance

Table 6 - T_{amb} = +25°C, f = 1 MHz (see note)

Symbol	Parameter	Test Conditions	Min	Typ. (Note)	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		8	12	pF
Note : Capacitance is guaranteed by periodic testing, T_{amb} = +25°C, f = 1 MHz.						

5.6 · Burn-in conditions for DIL package



6 · FUNCTIONAL DESCRIPTION

6.1 · Function description

The 27C256 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 262, 144 bits organized as 32, 768 words of 8 bits length.

When the outputs of two or more 27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the 27C256, a low-level signal is applied to the E and G pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

Active I_{CC} current can be reduced by applying a high TTL signal to the E pin. In this mode all outputs are in the high-impedance state.

6.2 · Function table

Table 7

Functions (pins)	Mode						
	Read	Output disable	Standby	Programming	Verify	Program inhibit	Signature mode
$\overline{CE}$ (20)	0	0	1	0	1	1	0
$\overline{OE}$ (22)	0	1	X	1	0	1	0
A9 (24)	X	X	X	X	X	X	V_H*
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11-13, 15-19)	Q	HI-Z	HI-Z	D	Q	HI-Z	Code

* V_H = 12 V ± 0.5 V.

6.3 · Device operation

The modes of operations of the 27C256 are listed in the Operating Modes. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for 12 V on A9 for Electronic Signature.

Read mode

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that CE has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby mode

The 27C256 has a standby mode which reduces the maximum active current from 50 mA to 1 mA. The 27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System considerations

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks

is dependent on the ouput capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.

The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

7 · PROGRAMMING MODES

Caution : exceeding 14 V on Vpp pin will permanently damage the 27C256.

When delivered, and after each erasure, all bits of the 27C256 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be present in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure. The 27C256 is in the programming mode when the V_{PP} input is at 12.75 V and $\overline{CE}$ is at TTL-low.

The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

7.1 · Very fast and reliable programming algorithm = PRESTO II

PRESTO II programming algorithm, available for the 27C256, is an enhancement of the PRESTO algorithm used for the 27C1024.

During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 3 seconds.

Program inhibit

Programming of multiple 27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel 27C256 may be common. A TTL low-level pulse applied to a 27C256's $\overline{CE}$ input, with V_{PP} at 12.75 V, will program that 27C256. A high level $\overline{CE}$ input inhibits the other 27C256s from being programmed. V_{CC} is specified to be 6.25 V ± 0.25 V.

Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH}, V_{PP} at 12.75 V and V_{CC} at 6.25 V ± 0.25 V.

7.2 · Electronic signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C256. To activate this mode, the programming equipment must force 11.5 V to 12.5 V on address line A9 of the 27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the TMS 27C256, these two identifier bytes are given here below, and can be read-out on outputs Q1 to Q8.

Table 8 · Electronic signature mode

Identifier \ Pins	A0	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Hex
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	1	0	0	0	1	1	0	1	8D

Notes : A9 = 12 V ± 0.5 V ; CE, OE = V_{IL} ; A1-A8, A10-A14 = V_{IL}.

7.3 · Erasure operation

The erasure characteristic of the 27C256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom A. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical 27C256 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the 27C256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the 27C256 window to prevent unintentional erasure. The recommended erasure procedure for the 27C256 is exposure to short wave ultraviolet light which has wavelength 2537 A. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The 27C256 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

7.4 · Programming operation

Table 9 - DC and operating characteristic
T_A = 25°C ±5°C, V_{CC} (1) = 6.25 V ±0.25 V, V_{PP} (1) = 12.75 V ±0.25 V

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input low level (all inputs)		−0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} +0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = −400 µA	2.4		V
I_{CC2}	V_{CC} supply current			50	mA
I_{PP2}	V_{PP} supply current (program)	CE = V_{IL}		50	mA
V_{ID}	A9 electronic signature voltage		11.5	12.5	V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10 - AC characteristics

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
t_{AS}	Address setup time		2		µs
t_{OES}	OE setup time		2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time		0		µs
t_{DH}	Data hold time		2		µs
t_{DFP} (see Note 2)	Output enable output float delay		0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{PW}	Initial program pulse width		95	105	µs
t_{OE}	Data valid from OE			100	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

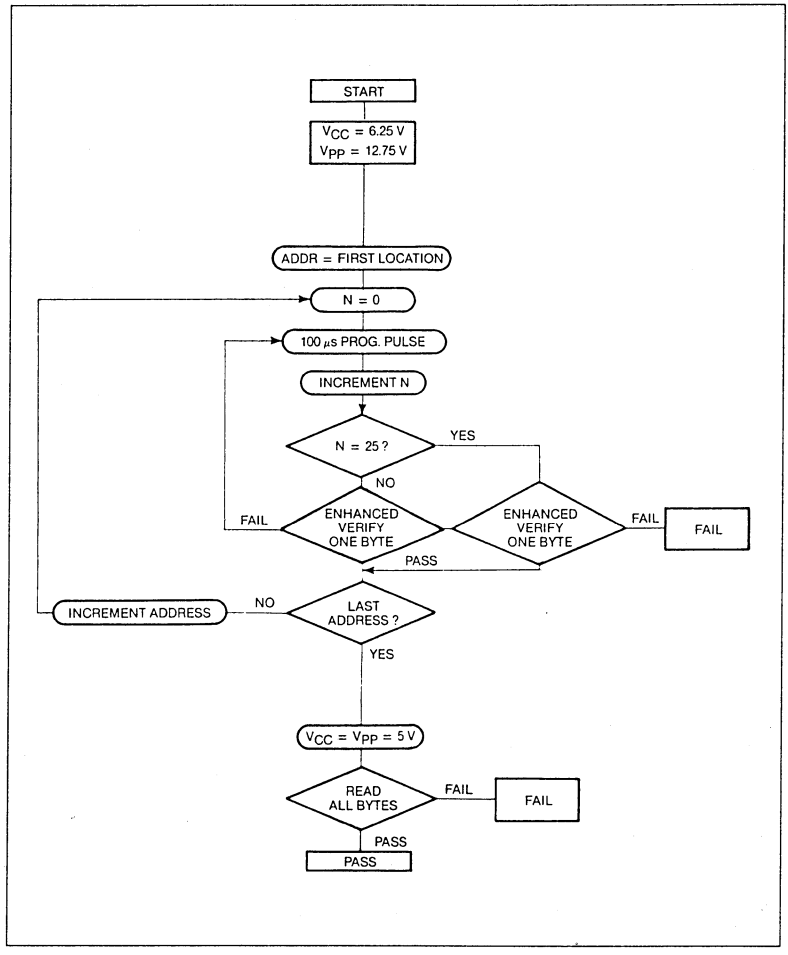
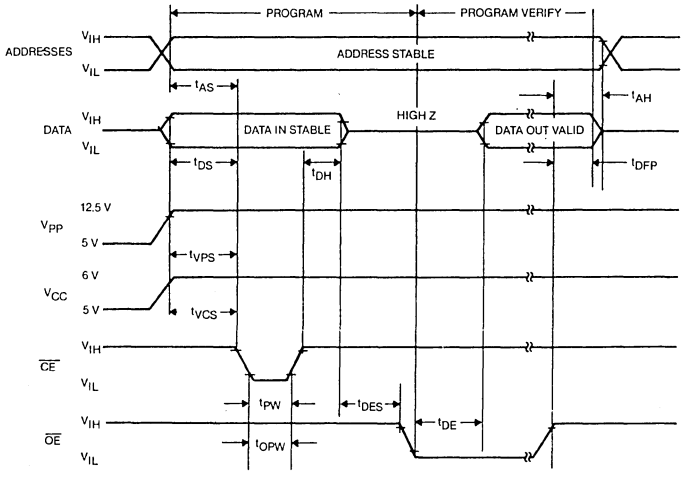


FIGURE 8 - PRESTO II PROGRAMMING ALGORITHM FLOWCHART.



Note 1 : The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
Note 3 : When programming the 27C256, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 9 - PROGRAMMING WAVEFORMS

8 - PREPARATION FOR DELIVERY

8.1 - Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

8.2 - Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperature for the entire temperature range.

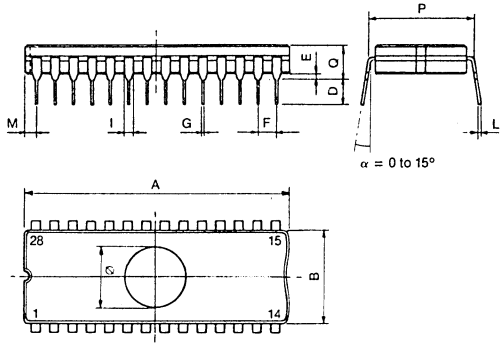
9 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent, if practical.

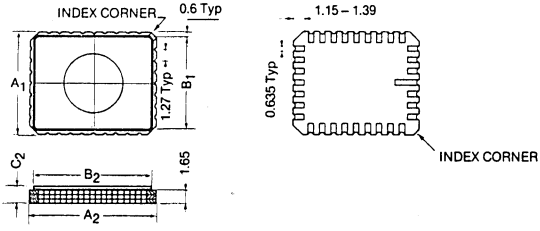
10 · PACKAGE MECHANICAL DATA

10.1 · 28 pins · DIL Cerdip with window



Symbol	Millimeters		
	Min	Typ	Max
A			37.85
B	12.7		15.49
D	3.81		
E	0.38		1.52
F	2.29		2.79
G	0.35		0.58
I	0.96		1.65
L	0.20		0.38
M			2.54
P	14.98		15.75
Q			5.89
∅		7.11	

10.2 · 32 pins · Leadless Ceramic Chip Carrier with window



Symbol	Millimeters	
	Min	Max
A_1	11.3	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92

11 · ORDERING INFORMATION

11.1 · HI-REL product

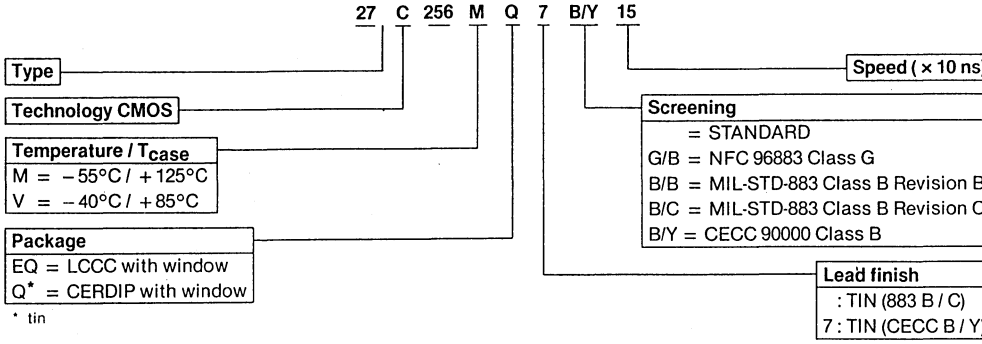
TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (μs)	Drawing number
27C256MQG/B15	NFC 96883 - Class G	Cerdip 28	−55 / +125	150	TMS data sheet
27C256MQG/B20	NFC 96883 - Class G	Cerdip 28	−55 / +125	200	TMS data sheet
27C256MQG/B25	NFC 96883 - Class G	Cerdip 28	−55 / +125	250	TMS data sheet
27C256MEQG/B15	NFC 96883 - Class G	LCCC 32	−55 / +125	150	TMS data sheet
27C256MEQG/B20	NFC 96883 - Class G	LCCC 32	−55 / +125	200	TMS data sheet
27C256MEQG/B25	NFC 96883 - Class G	LCCC 32	−55 / +125	250	TMS data sheet
27C256MQ7B/Y15	CECC 90000	Cerdip 28	−55 / +125	150	CECC 90113-001
27C256MQ7B/Y20	CECC 90000	Cerdip 28	−55 / +125	200	CECC 90113-001
27C256MQ7B/Y25	CECC 90000	Cerdip 28	−55 / +125	250	CECC 90113-001
27C256MEQ7B/Y15	CECC 90000	LCCC 32	−55 / +125	150	CECC 90113-001
27C256MEQ7B/Y20	CECC 90000	LCCC 32	−55 / +125	200	CECC 90113-001
27C256MEQ7B/Y25	CECC 90000	LCCC 32	−55 / +125	250	CECC 90113-001
27C256MQB/C15	MIL-STD-883 C	Cerdip 28	−55 / +125	150	TMS data sheet
27C256MQB/C20	MIL-STD-883 C	Cerdip 28	−55 / +125	200	TMS data sheet
27C256MQB/C25	MIL-STD-883 C	Cerdip 28	−55 / +125	250	TMS data sheet
27C256MEQ1B/C15	MIL-STD-883 C	LCCC 32	−55 / +125	150	TMS data sheet
27C256MEQ1B/C20	MIL-STD-883 C	LCCC 32	−55 / +125	200	TMS data sheet
27C256MEQ1B/C25	MIL-STD-883 C	LCCC 32	−55 / +125	250	TMS data sheet

(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.

11.2 · Standard product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (μs)	Drawing number
27C256MQ15	TMS Standard	Cerdip 28	−55 / +125	150	
27C256MQ20	TMS Standard	Cerdip 28	−55 / +125	200	
27C256MQ25	TMS Standard	Cerdip 28	−55 / +125	250	
27C256MEQ15	TMS Standard	LCCC 32	−55 / +125	150	
27C256MEQ20	TMS Standard	LCCC 32	−55 / +125	200	
27C256MEQ25	TMS Standard	LCCC 32	−55 / +125	250	

(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.


27 C 256 M Q 7 B/Y 15
Type
Technology CMOS
Temperature / Tcase
M = −55°C / +125°C
V = −40°C / +85°C
Package
EQ = LCCC with window
Q* = CERDIP with window
* tin
Screening
= STANDARD
G/B = NFC 96883 Class G
B/B = MIL-STD-883 Class B Revision B
B/C = MIL-STD-883 Class B Revision C
B/Y = CECC 90000 Class B
Speed (x 10 ns)
Lead finish
: TIN (883 B / C)
7 : TIN (CECC B / Y)

1024 K (128 K x 8) CMOS UV ERASABLE PROM

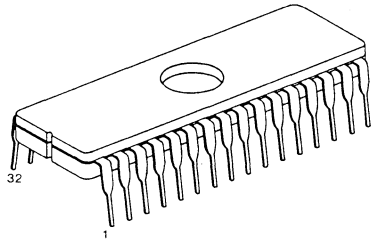
DESCRIPTION

The 27C1001 is a high speed 1 Mbit ultraviolet erasable and electrically programmable EPROM ideally suited for 8-bit microprocessors systems requiring large programs.

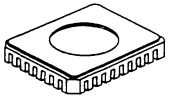
It is organized as 131072 words by 8 bits, and packaged in a 32 pin Window Ceramic Frit-Seal package or in a 32 pin LCCC. The 27C1001 has a single +5 V power supply and an access time of 150 ns.

The 27C1001 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 50 mA while the maximum standby current is only 1 mA. The standby mode is achieved by applying a TTL-high signal to the CE input. The 27C1001 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the 27C1001s high density, and new advanced microprocessors having mega-bit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The 27C1001 large storage capability enables it to function as a high density software carrier. The 27C1001 has an «Electronic Signature» that allows programmers to automatically identify type and pinout.



32 pins CERDIP / Q suffix



32 pins LCCC / EQ suffix

MAIN FEATURES

- Very fast access time : 150 ns.
- Compatible to high speed microprocessors zero wait state.
- Low «CMOS» consumption :
  active current : 100 mA max
  standby current : 1 mA max
- Programming voltage : 12.5 V.
- Electronic signature for automated programming.
- Programming time in the 6 seconds range (PRESTO II algorithm).
- 32 pins JEDEC approved pin out.
- Power supply : V_{CC} = 5 V_{DC} ± 10 %.
- Military temperature range : T_C = −55, +125°C.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 B.
- TMS STANDARD.

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The 27C1001 series are 131072 words by 8-bit ultraviolet-light, erasable, electrically programmable read-only memories. These devices are fabricated using. CMOS E4 technology for high speed and simple interface with MOS and bipolar circuits. The data outputs are three-state for connecting multiple devices to a common bus. The 27C1001 is pin compatible with existing 32-pin EPROMs. It is offered in both and leadless chip carrier dual-in-line ceramic package (Q and EQ suffix) rated for operation from $-55°C$ to $+125°C$.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C1001. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C1001 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 550 mW at $T_C = -55°C$ / 275 mW at $T_C = +125°C$.

Maximum standby power dissipation : 5 mW at 5 V.

This memory has static operation : no clocks no refresh.

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

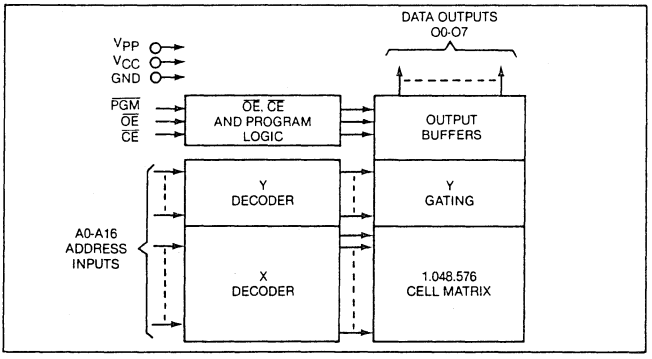
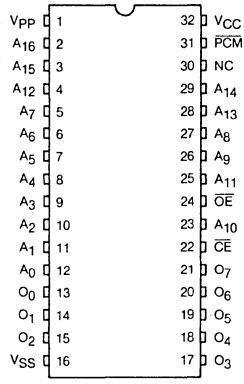


FIGURE 1 - 27C1001 BLOCK DIAGRAM.

2 - PIN ASSIGNEMENTS

CERDIP PACKAGE



LCCC PACKAGE

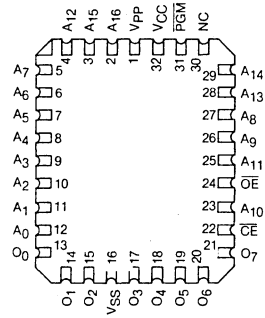


FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbol of each terminal of the device are given in the Figure 3 below.

PIN FUNCTIONS

A0-A16	Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
O0-O7	Data Input / Output
NC	No Connected

FIGURE 3

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C1001, in compliance either with MIL-M-38510 rev C or CECC 90000.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

2.2 - CECC 90000

1) CECC 90000
2) Specification 9011x-0xx

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 tin dipped.

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 32 lead DIL
- 32 lead LCCC, style C12.

The precise case outlines are described into MIL-M-38510.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 1 · Absolute maximum ratings
Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Figure 3.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		−0.6	7	V
V_{PP}	Programming supply voltage		−0.6	14	V
V_I	Input voltage	(Except A9)	−0.6	6.5	V
		(A9)	−0.6	13.5	V
V_O	Output voltage		−0.6	V_{CC} +1	V
V_{OZ}	Off-state voltage		−0.6	V_{CC} +1	V
I_O	Output current			5	mA
I_I	Input current			15	mA
P_D max.	Max. power-dissipation	T_C = 25°C / −55°C		550	mW
		T_C = 125°C		275	mW
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−65	+150	°C
T_{lead}	Lead temperature (soldering : 10 s)			+300	°C

Note : Stresses above those listed under «Absolute maximum ratings» may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3.2 · Recommanded conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification in guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 10).

Table 2

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} +0.5	V
T_{case}	Operating temperature	−55	+125	°C

3.4 · Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
		Thermal resistance · Ceramic		
CERDIP DIL 28	$\theta_{J\text{-}A}$ $\theta_{J\text{-}C}$	Junction-to-Ambient Junction-to-Case	50 7	°C/W °C/W
		Thermal resistance · Ceramic		
LCCC 32	$\theta_{J\text{-}A}$ $\theta_{J\text{-}C}$	Junction-to-Ambient Junction-to-Case	55 15	°C/W °C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 · CECC

is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 9011x-0xx. Group C inspection is performed on a periodic basis in accordance with CECC 9011x-0xx.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below :

- Table 4 : Static electrical characteristics for the electrical variants.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Table 5).

5.2 · Static characteristics

All voltages are referenced to GND.

Table 4 - DC and operating characteristics

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 10\,\%$

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input load current	$V_{IN} = 5.5\,V$		10	μA
I_{LO}	Output leakage current	$V_{OUT} = 5.5\,V$		10	μA
I_{CC1}	V_{CC} active current	$\overline{CE} = \overline{OE} = V_{IL}$ @ f = 8 MHz $I_{OUT} = 0\,mA$ (Open Outputs)		100	mA
I_{CC2}	V_{CC} standby current	$\overline{CE} = V_{IH}$		1	mA
I_{PP1}	V_{PP} read current	$V_{PP} = V_{CC}$		0.1	mA
V_{IL}	Input low voltage		−0.1	0.8	V
V_{IH}	Input high voltage		2.0	$V_{CC}+0.5$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\,mA$		0.45	V
V_{OH}	Ouput high voltage	$I_{OH} = -400\,\mu A$	2.4		V
V_{PP}	V_{PP} read voltage	$V_{CC} - 0.7\,V$	—	V_{CC}	V

5.3 · Dynamic characteristics

Table 5

$-55°C \leqslant T_C \leqslant +125°C$; $V_{CC} = 5\,V \pm 10\,\%$

Symbol	Parameter	Test conditions	27C1001Mx15		27C1001Mx20		27C1001Mx25		Unit
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to output delay	$\overline{CE} = V_{IL}$		65		70		100	ns
t_{DF}	$\overline{OE}$ high to output float (see Note)	$\overline{CE} = V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Note : This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven-see timing diagram.

5.4 · Test conditions specific to the device

Output load	1 TTL gate and CL = 100 pF
Input rise and fall times	⩽ 20 ns
Input pulse levels	0.45 V to 2.4 V
Timing measurement reference level inputs, outputs	0.8 V and 2 V

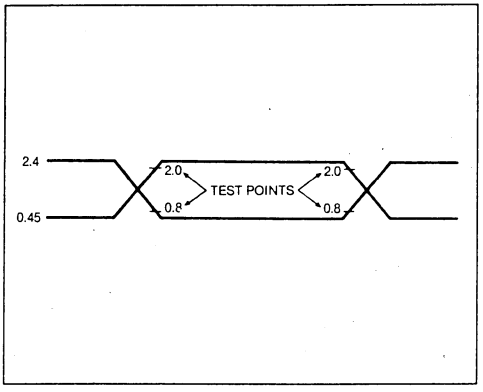


FIGURE 4 · AC TESTING INPUT / OUPUT WAVEFORM.

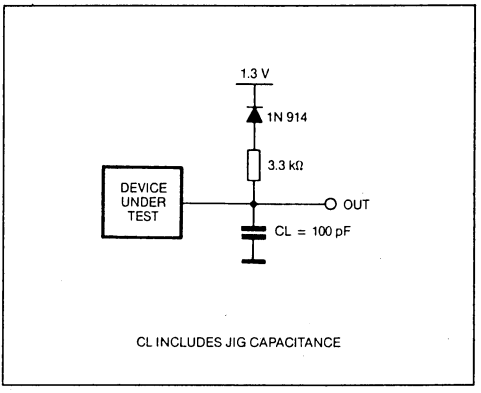


FIGURE 5 · AC TESTING LOAD CIRCUIT.

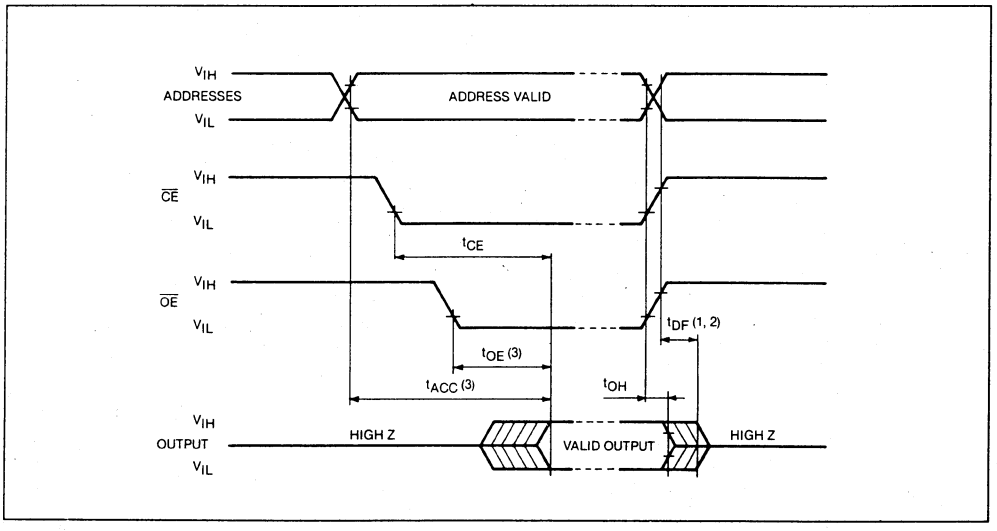


FIGURE 6 · AC WAVEFORMS.

Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.

5.5 - Capacitance (see note)
T_{amb} = 25°C, f = 1 MHz.

Symbol	Parameter	Test Conditions	Min	Typ. (Note)	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		8	12	pF
Note : Typical values are for T_{amb} = 25°C and nominal supply voltages.						

Note : This parameter is only sampled and not 100 % tested.

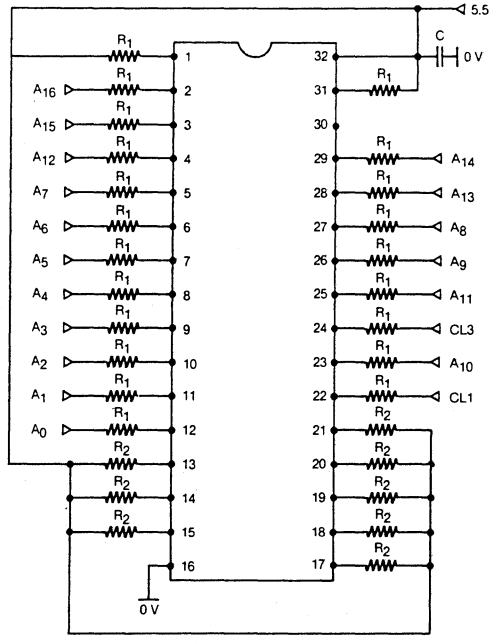
5.6 - Burn-in conditions

5.6.1 - In Cerdip

Power :
V_{SS} = 0 V V_{CC} = 5.5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5 V

5.6.2 - In LCCC

Power :
V_{SS} = 0 V V_{CC} = 5.5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5.5 V



R_1 = 1 kΩ
R_2 = 3 kΩ
C = 0.1 µF / case

FIGURE 7

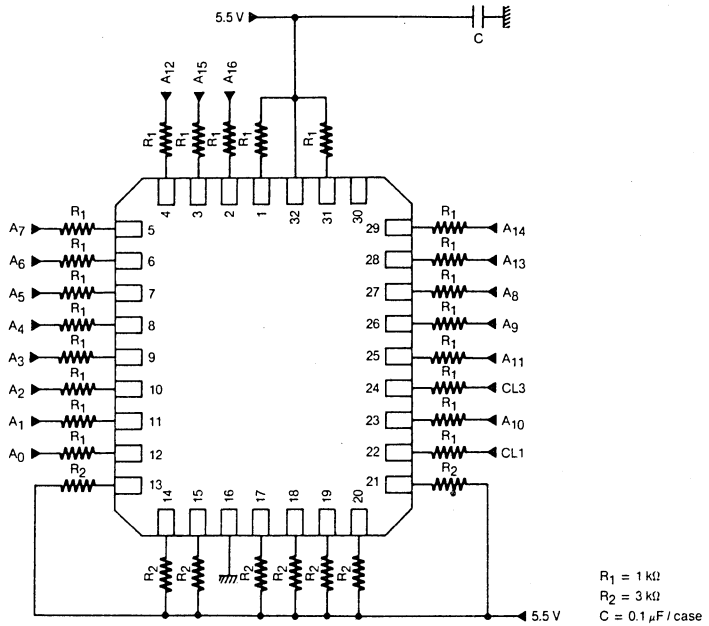


FIGURE 8

7

6 · FUNCTIONAL DESCRIPTION

6.1 · Device operation

The modes of operations of the 27C1001 are listed in the function table (see § 6.5). A single 5 V power supply is required in the read mode. All inputs are TTL levels except for 12 V on A9 for Electronic Signature.

Read mode (See § 5.1)

The 27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby mode

The 27C1001 has a standby mode which reduces the maximum active current from 50 mA to 1 mA. The 27C1001 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System considerations

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the ouput capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.

The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

6.2 · Programming

Caution : exceeding 14 V on V_{PP} pin will permanently damage the 27C1001.

When delivered, and after each erasure, all bits of the 27C1001 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be present in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure.

The 27C1001 is in the programming mode when the V_{PP} input is at 12.75 V and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Very fast and reliable programming algorithm = PRESTO II

PRESTO II programming algorithm is available for the 27C1001.

During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 12 seconds.

Program inhibit

Programming of multiple 27C1001s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel 27C1001 may be common. A TTL low-level pulse applied to a 27C1001's $\overline{CE}$ input, with V_{PP} at 12.5 V, will program that 27C1001. A high level $\overline{CE}$ input inhibits the other 27C1001s from being programmed. V_{CC} is specified to be 6.25 V ±0.25 V.

Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5 V and V_{CC} at 6.25 V ±0.25 V.

Electronic signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the 27C1001. To activate this mode, the programming equipment must force 11.5 V to 12.5 V on address line A9 of the 27C1001. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the TMS 27C1101, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ELECTRONIC SIGNATURE MODE

Identifier \ Pins	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	0	0	0	0	0	1	0	1	05

Notes : A9 = 12 V ±0.5 V ; $\overline{CE}$, $\overline{OE}$ = V_{IL} ; A1-A8, A10-A16 = V_{IL}.

6.3 - High speed programming

6.3.1 - PRESTO II programming algorithm flow chart

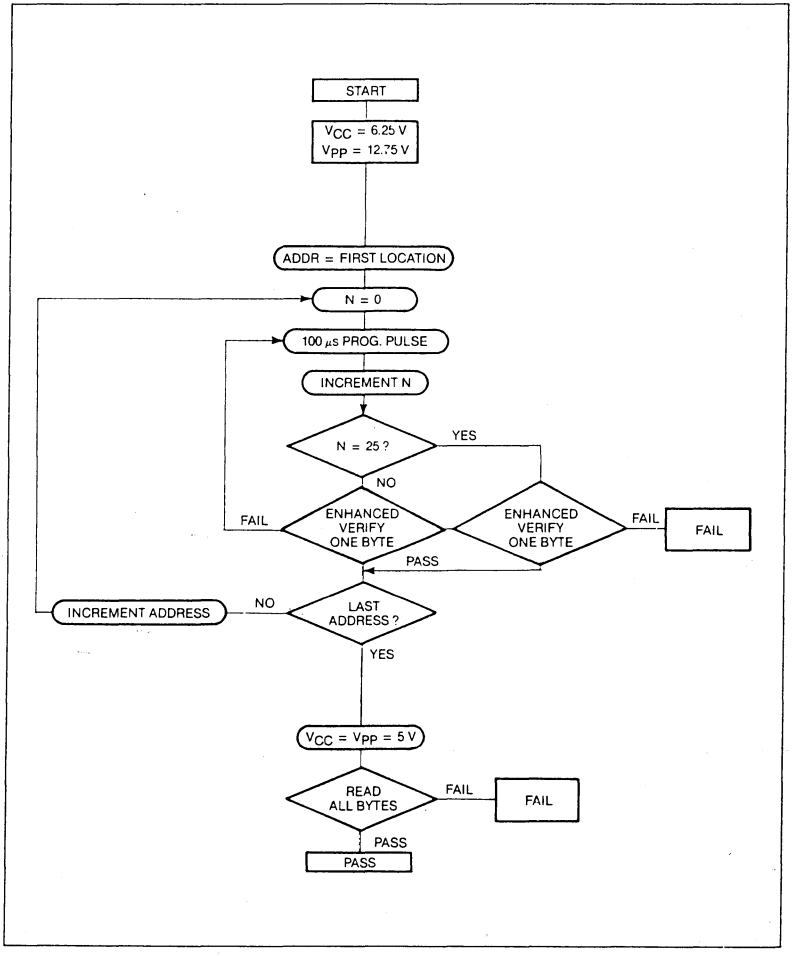


FIGURE 9

PROGRAMMING OPERATION (T_C = 25°C ±5°C, V_{CC} (1) = 6.25 V ±0.25 V, V_{PP} (1) = 12.75 V ±0.25 V)

DC and operating characteristic

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input low level (all inputs)		−0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} +0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = −400 µA	2.4		V
I_{CC2}	V_{CC} supply current			50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 electronic signature voltage		11.5	12.5	V

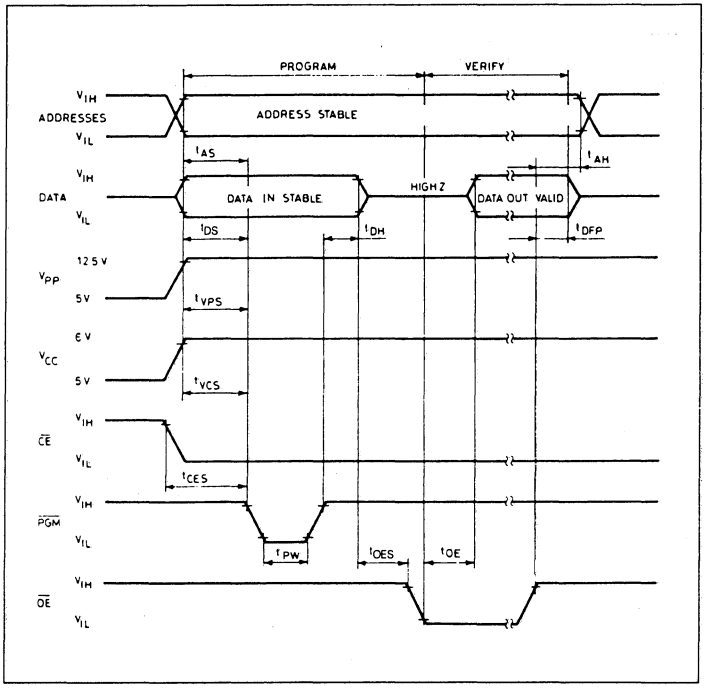
Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC characteristics

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
t_{AS}	Address setup time		2		µs
t_{OES}	OE setup time		2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time		0		µs
t_{DH}	Data hold time		2		µs
t_{DFP} (see Note 2)	Output enable output float delay		0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{CES}	CE setup time		2		µs
t_{PW}	PGM initial program pulse width		95	105	µs
t_{OE}	Data valid from OE			100	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

6.3.2 - Wave forms



Note 1 : The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.

Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Note 3 : When programming the 27C1001, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 10 - PROGRAMMING WAVEFORMS

7

6.4 - Erasure operation

The erasure characteristic of the 27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom A. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical 27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the 27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the 27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the 27C1001 is exposure to short wave ultraviolet light which has wavelength 2537 A. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm² power rating. The 27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

6.5 · Function table

OPERATING MODES

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUTS
Read	L	L	X	X	V_{CC}	D_{OUT}
Output disable	L	H	X	X	V_{CC}	High Z
Standby	H	X	X	X	V_{CC}	High Z
Program	L	X	X	L	V_{PP}	D_{IN}
Program verify	L	L	X	H	V_{PP}	D_{OUT}
Program inhibit	H	X	X	X	V_{PP}	High Z
Electronic signature	L	L	V_H	H	V_{CC}	CODE

Notes : X = Don't care ; V_H = 12 V ±0.5 V ; H = High ; L = Low.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperature for the entire temperature range.

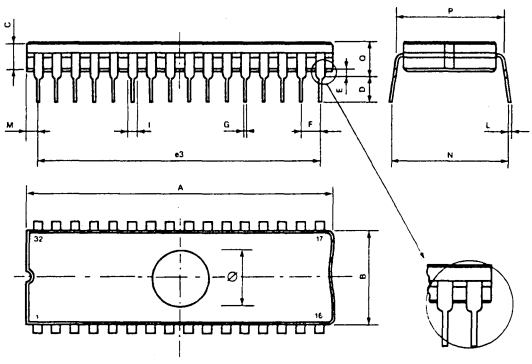
8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent, if practical.

9 - PACKAGE MECHANICAL DATA

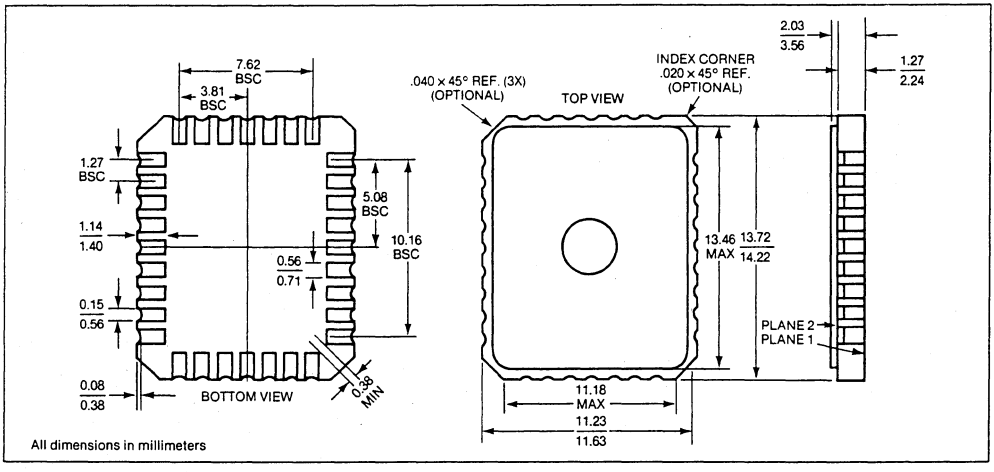
9.1 - DIL CERDIP with window package 32 pins



Symbol	Millimeters		
	Min	Typ	Max
A			42.78
B	14.50		14.90
C	3.55		4.70
D	3.40		5.08
E	0.50		1.78
e3		38.10	
F	2.29		2.79
G	0.40		0.55
I	1.27		1.52
L	0.22		0.31
M			2.49
N	15.62		17.78
P	15.40		15.75
Q			5.71
K	7.90		8.38
∅		9.65	

FIGURE 11 - 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)

9.2 - 32 pins leadless ceramic chip carrier



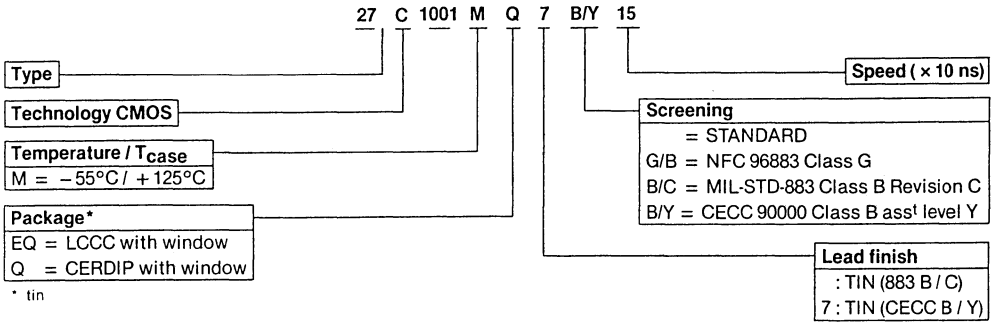
10 · ORDERING INFORMATION

10.1 · HI-REL product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (μs)	Drawing number
27C1001MQG/B15	NFC 96883 - Class G	Cerdip 32	– 55 / + 125	150	Internal
27C1001MQG/B20	NFC 96883 - Class G	Cerdip 32	– 55 / + 125	200	Internal
27C1001MQB/C15	MIL-STD-883 C - Class B	Cerdip 32	– 55 / + 125	150	Non available
27C1001MQB/C20	MIL-STD-883 C - Class B	Cerdip 32	– 55 / + 125	200	Non available
27C1001MEQ1B/C15	MIL-STD-883 C - Class B	LCCC 32	– 55 / + 125	150	Non available
27C1001MEQ1B/C20	MIL-STD-883 C - Class B	LCCC 32	– 55 / + 125	200	Non available
27C1001MQ7B/Y15	CECC 90000	Cerdip 32	– 55 / + 125	150	TBD
27C1001MQ7B/Y20	CECC 90000	Cerdip 32	– 55 / + 125	200	TBD
27C1001MEQ7B/Y15	CECC 90000	LCCC 32	– 55 / + 125	150	TBD
27C1001MEQ7B/Y20	CECC 90000	LCCC 32	– 55 / + 125	200	TBD
(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

10.2 · Standard product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (μs)	Drawing number
27C1001MQ15	TMS Standard	Cerdip 32	– 55 / + 125	150	Internal
27C1001MQ20	TMS Standard	Cerdip 32	– 55 / + 125	200	Internal
27C1001MQ25	TMS Standard	Cerdip 32	– 55 / + 125	250	Internal
27C1001MEQ15	TMS Standard	LCCC 32	– 55 / + 125	150	Internal
27C1001MEQ20	TMS Standard	LCCC 32	– 55 / + 125	200	Internal
27C1001MEQ25	TMS Standard	LCCC 32	– 55 / + 125	250	Internal
(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					


27 C 1001 M Q 7 B/Y 15
Type
Technology CMOS
Temperature / Tcase
M = −55°C / +125°C
Package*
EQ = LCCC with window
Q = CERDIP with window
* tin
Speed (x 10 ns)
Screening
= STANDARD
G/B = NFC 96883 Class G
B/C = MIL-STD-883 Class B Revision C
B/Y = CECC 90000 Class B asst level Y
Lead finish
: TIN (883 B / C)
7 : TIN (CECC B / Y)

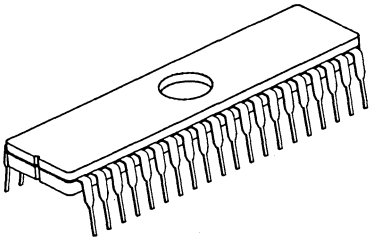
7

1024 K (64 K x 16) CMOS UV ERASABLE AND OPT ROM PROM

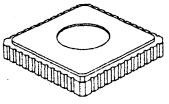
DESCRIPTION

The 27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits. The 27C1024 with its single + 5 V power supply and with an access time of 80 ns, is ideal for use in 16 bit microprocessor system allowing full speed operation without WAIT states. In high performance CPU's (10 MHz), the 27C1024 has an important feature which is to separate the output control, Output Enable (OE) from the Chip Enable control (CE). The OE control eliminates bus contention in multiple bus microprocessor systems. The 27C1024 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 40 mA while the maximum standby current is only 0.2 mA. The standby mode is achieved by applying a TTL-high signal to the CE input. The 27C1024 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the 27C1024s high density, and new advanced microprocessors having mega-bit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The 27C1024 large storage capability enables it to function as a high density software carrier. The 27C1024 has an «Electronic Signature» that allows programmers to automatically identify device type and pinout.



Q suffix
40 pins CERDIP



EQ suffix
44 pins LCCC

MAIN FEATURES

- Very fast access time : 80 ns.
- Compatible to high speed microprocessors zero wait state.
- Low «CMOS» consumption :
  active current : 40 mA max.
  standby current : 0.2 mA max.
- Programming voltage : 12.5 V.
- Electronic signature for automated programming.
- Programming time in the 6 seconds range (presto II algorithm).
- 40/44 pins JEDEC approved pin-out.
- Power supply : V_{CC} = 5 V_{DC} ± 10 %.
- Military temperature range : T_C = −55, +125°C.

SCREENING / QUALITY

This product is manufactured according to :

- MIL-STD-883C, class B.
- TCS Standard.

SUMMARY

A - GENERAL DESCRIPTION

INTRODUCTION

The 27C1024 series are 1,048 576-bit, ultraviolet-light, erasable, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C1024 is pin compatible with existing 40-pin ROMs and EPROMs. It is offered in both dual-in-line and leadless chip carrier ceramic package (Q and EQ suffix) rated for operation from $-55°C$ to $+125°C$.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C1024. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C1024 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 500 mW at 5 V.

Maximum standby power dissipation : 1 mW at 5 V.

This memory has static operation : no clocks no refresh.

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

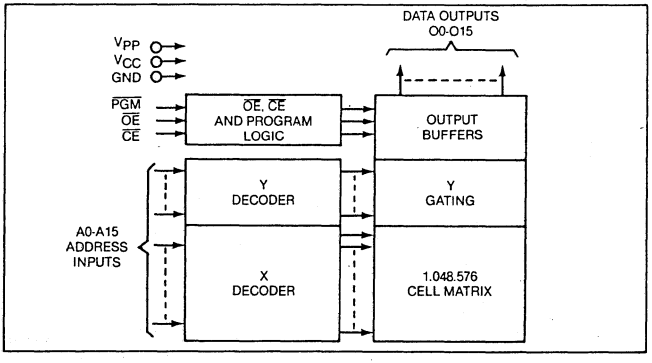
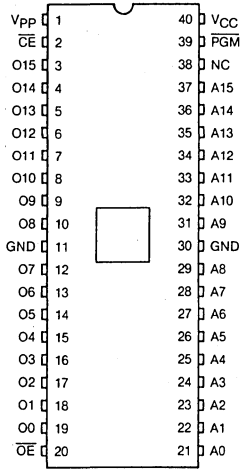


FIGURE 1 - 27C1024 BLOCK DIAGRAM.

7

2 - PIN ASSIGNEMENTS

CERDIP PACKAGE



LCCC PACKAGE

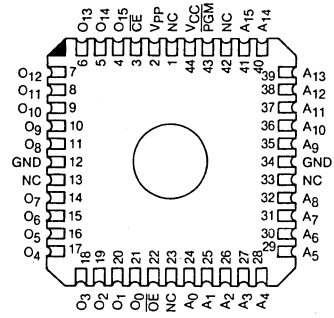


FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbol of each terminal of the device are given in the Figure 3 below.

PIN FUNCTIONS

A0-A15	Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
O0-O15	Data Input / Output
NC	No Connected

FIGURE 3

B - DETAILED SPECIFICATIONS

1 - SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C1024, in compliance either with MIL-STD-883 class B rev C.

2 - APPLICABLE DOCUMENTS

2.1 - MIL-STD-883

1) MIL-STD-883 : Test methods and procedures for electronics
2) MIL-PRF-38535 : Integrated circuits (micro-circuits) manufacturing.

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 2.

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835 tin dipped.

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-STD-1835 :

- 40 lead DIL, Dual In Line,
- 44 lead LCCC.

The precise case outlines are described into MIL-STD-1835, and also § 9.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 1 - Absolute maximum ratings
Unless otherwise stated, all voltages are referenced to the reference terminal as defined in Figure 3.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		−0.6	7	V
V_{PP}	Programming supply voltage		−0.6	14	V
V_I	Input voltages	(Except A9)	−0.6	6.5	V
		(A9)	−0.6	13.5	V
V_O	Output voltages		−0.6	V_{CC} +1	V
V_{OZ}	Off-state voltage		−0.6	V_{CC} +1	V
I_O	Output currents			5	mA
I_I	Input currents			15	mA
P_D max.	Max. power-dissipation			250	mW
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−65	+150	°C
T_{lead}	Lead temperature (soldering : 10 s)			+300	°C

Note : Stresses above those listed under «Absolute maximum ratings» may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3.2 - Recommanded conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification in guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

The conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test (Table 4).

All voltages are referenced to a reference terminal (V_{SS}, GND, etc...).

Table 2

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} +0.5	V
T_{case}	Operating temperature	−55	+125	°C

3.4 · Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
CERDIP DIL 40	$\theta_{J\text{-}A}$ $\theta_{J\text{-}C}$	**Thermal resistance · Ceramic** Junction-to-Ambient Junction-to-Case	 45 5	 °C/W °C/W
LCCC 44	$\theta_{J\text{-}A}$ $\theta_{J\text{-}C}$	**Thermal resistance · Ceramic** Junction-to-Ambient Junction-to-Case	 50 10	 °C/W °C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-PRF-38535 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 4 : Static electrical characteristics for the electrical variants.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to clause § 5.4 of this specification (Table 5).

5.2 · Static characteristics

All voltages are referenced to GND.

Table 4 · Read mode DC characteristics Note 1

$-55°C \leqslant T_C \leqslant +125°C$ $\quad V_{CC} = 5\,V \pm 10\,\%$

Symbol	Parameter	Test conditions	Min	Max	Unit
I_{LI}	Input leakage current	$0\,V \leqslant V_{IN} \leqslant V_{CC}$		± 10	µA
I_{LO}	Output leakage current	$0\,V \leqslant V_{OUT} \leqslant V_{CC}$		± 10	µA
I_{CC}	Supply current	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$, $I_{OUT} = 0\,mA, f = 5\,MHz$		40	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply cuurent (standby) CMOS	$\overline{E} > V_{CC} - 0.2\,V$		200	µA
I_{PP}	Program current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input low voltage		−0.3	0.8	V
V_{IH} Note 2	Input high voltage		2	$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\,mA$		0.45	V
V_{OH}	Output high voltage TTL	$I_{OH} = -400\,\mu A$	2.4		V
	Ouput high voltage CMOS	$I_{OH} = -100\,\mu A$	$V_{CC}-0.7$		V

Note 1 : V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Maximum DC voltage on output is $V_{CC} + 0.5$ V.

5.3 · Dynamic characteristics

Table 5A · Read mode AC characteristics Note 1
$-55°C \leqslant T_C \leqslant +125°C$ $V_{CC} = 5\,V \pm 10\,\%$

Symbol	Alt	Parameter	Test conditions	27C1024						Unit
				−80		−90		−10		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		90		100	ns
t_{ELQV}	t_{CE}	Chip enable low to output valid	$\overline{G} = V_{IL}$		80		90		100	ns
t_{GLQV}	t_{OE}	Output enable low to output valid	$\overline{E} = V_{IL}$		40		45		50	ns
t_{EHQZ} Note 2	t_{DF}	Chip enable high to output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	ns
t_{GHQZ} Note 2	t_{DF}	Output enable high to output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address transition to ouptut transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Note 1 : V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Sampled only, not 100 % tested.

Table 5B · Read mode AC characteristics Note 1
$-55°C \leqslant T_C \leqslant +125°C$ $V_{CC} = 5\,V \pm 10\,\%$

Symbol	Alt	Parameter	Test conditions	27C1024						Unit
				−12		−15		−20 / −25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip enable low to output valid	$\overline{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output enable low to output valid	$\overline{E} = V_{IL}$		60		60		70	ns
t_{EHQZ} Note 2	t_{DF}	Chip enable high to output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	50	0	60	ns
t_{GHQZ} Note 2	t_{DF}	Output enable high to output Hi-Z	$\overline{E} = V_{IL}$	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address transition to ouptut transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Note 1 : V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
Note 2 : Sampled only, not 100 % tested.

5.4 · Test conditions specific to the device

Output load	1 TTL gate and CL = 100 pF
Input rise and fall times	⩽ 10 ns
Input pulse levels	0.45 V to 2.4 V
Timing measurement reference level inputs, outputs	0.8 V and 2 V

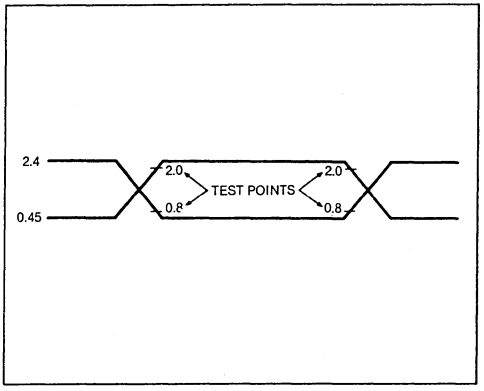


FIGURE 4 - AC TESTING INPUT / OUPUT WAVEFORM.

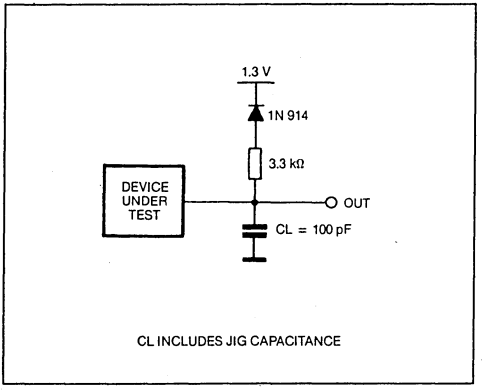


FIGURE 5 - AC TESTING LOAD CIRCUIT.

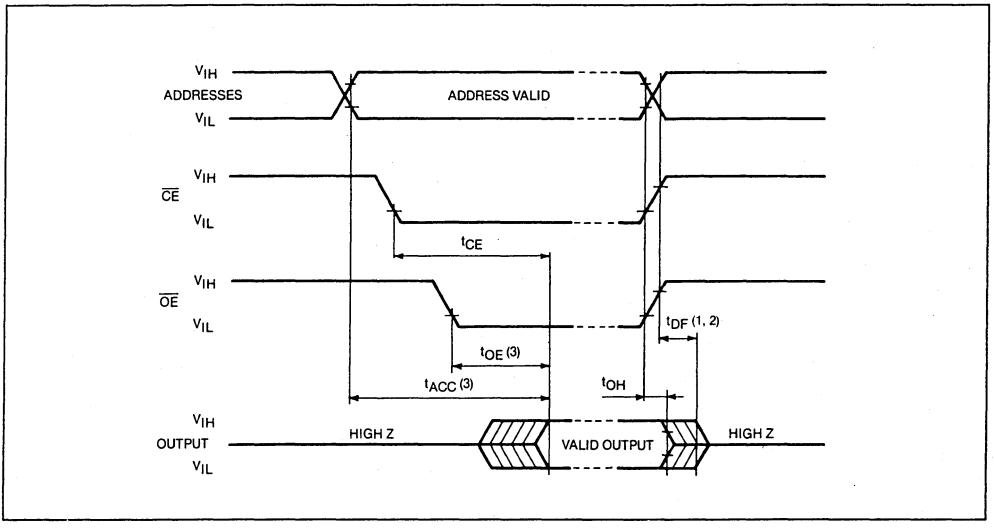


FIGURE 6 - AC WAVEFORMS.

Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.

5.5 · Capacitance (see note)
(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test conditions	Min	Typ. (Note)	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		8	12	pF

Note : Typical values are for T_{amb} = 25°C and nominal supply voltages.
These parameters are only sampled and not 100 % tested.

5.6 · Burn-in conditions

5.6.1 · In Cerdip

Power :
V_{SS} = 0 V V_{CC} = 5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5 V

5.6.2 · In LCCC

Power :
V_{SS} = 0 V V_{CC} = 5.5 V
Frequency : 500 kHz Level «0» : 0 V Level «1» : 5.5 V

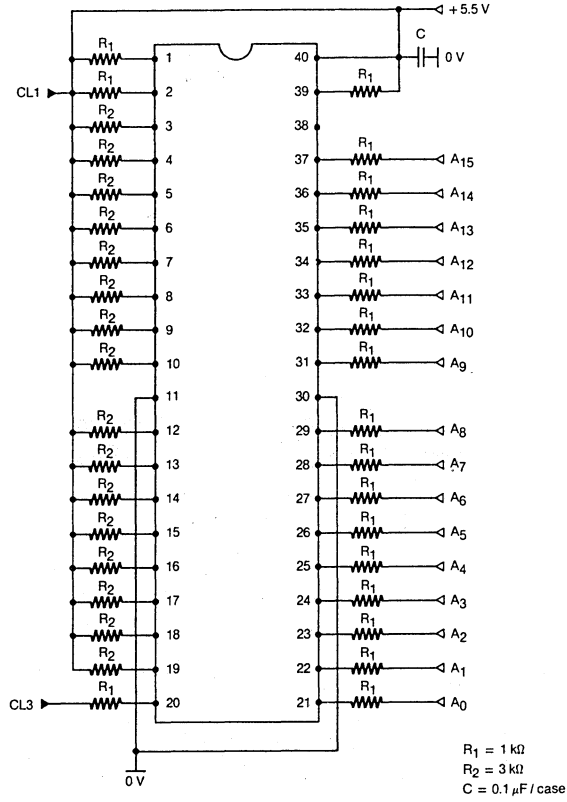


FIGURE 7

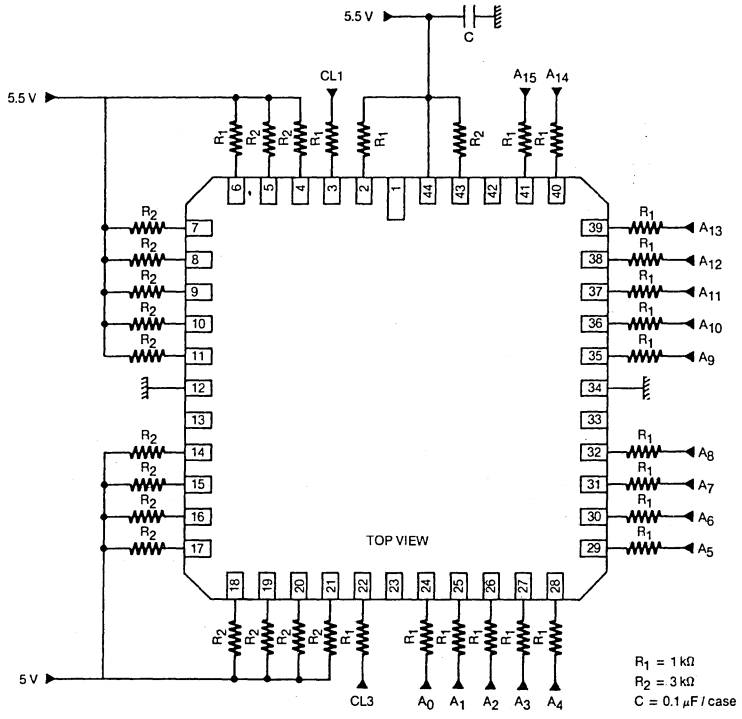


FIGURE 8

7

6 - FUNCTIONAL DESCRIPTION

6.1 - Device operation

The modes of operation of the 27C1024 are listed in the function table (see § 6.5). A single 5 V power supply is required in the read mode. All inputs are TTL levels except for 12 V on A9 for Electronic Signature.

Read mode

The 27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby mode

The 27C1024 has a standby mode which reduces the maximum active current from 40 mA to 0.2 mA. The 27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

System considerations

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the actice current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the ouput capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.

The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

6.2 · Programming

Caution : exceeding 14 V on V_{PP} pin will permanently damage the 27C1024.

When delivered, and after each erasure, all bits of the 27C1024 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be present in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure.

The 27C1024 is in the programming mode when the V_{PP} input is at 12.75 V and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data iputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Very fast and reliable programming algorithm = PRESTO II

PRESTO II programming algorithm is available for the 27C1024.

During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 6 seconds.

Program inhibit

Programming of multiple 27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel 27C1024 may be common. A TTL low-level pulse applied to a 27C1024's $\overline{CE}$ input, with V_{PP} at 12.75 V, will program that 27C1024. A high level $\overline{CE}$ input inhibits the order 27C1024s from being programmed. V_{CC} is specified to be 6.25 V ± 0.25 V.

Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.75 V and V_{CC} at 6.25 V ± 0.25 V.

Electronic signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its mannufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C1024. To activate this mode the programming equipment must force 11.5 V to 12.5 V on address line A9 of the 27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the TCS 27C1024, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7 while outputs O_8 to O_{15} are don't care.

ELECTRONIC SIGNATURE MODE

Identifier \ Pins	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	1	0	0	0	1	1	0	0	8C
Notes : A9 = 12 V ±0.5 V ; $\overline{CE}$, $\overline{OE}$ = V_{IL} ; A1-A8, A10-A15 = V_{IL}.										

PROGRAMMING OPERATION (T_C = 25°C ±5°C, V_{CC} (1) = 6.25 V ±0.25 V, V_{PP} (1) = 12.75 V ±0.25 V)
DC and operating characteristic

Symbol	Parameter	Test conditions see Note	Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input low level (all inputs)		−0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} +0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = −400 µA	2.4		V
I_{CC2}	V_{CC} supply current			50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 electronic signature voltage		11.5	12.5	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC characteristics

Symbol	Parameter	Test conditions Note 1	Min	Max	Unit
t_{AS}	Address setup time		2		µs
t_{OES}	$\overline{OE}$ setup time		2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time		0		µs
t_{DH}	Data hold time		2		µs
t_{DFP} Note 2	Output enable output float delay		0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{CES}	$\overline{CE}$ setup time		2		µs
t_{PW}	$\overline{PGM}$ initial program puls width		95	105	µs
t_{OE}	Data valid from $\overline{OE}$			100	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

7

6.3 · High speed programming

6.3.1 · PRESTO II programming algorithm flow chart

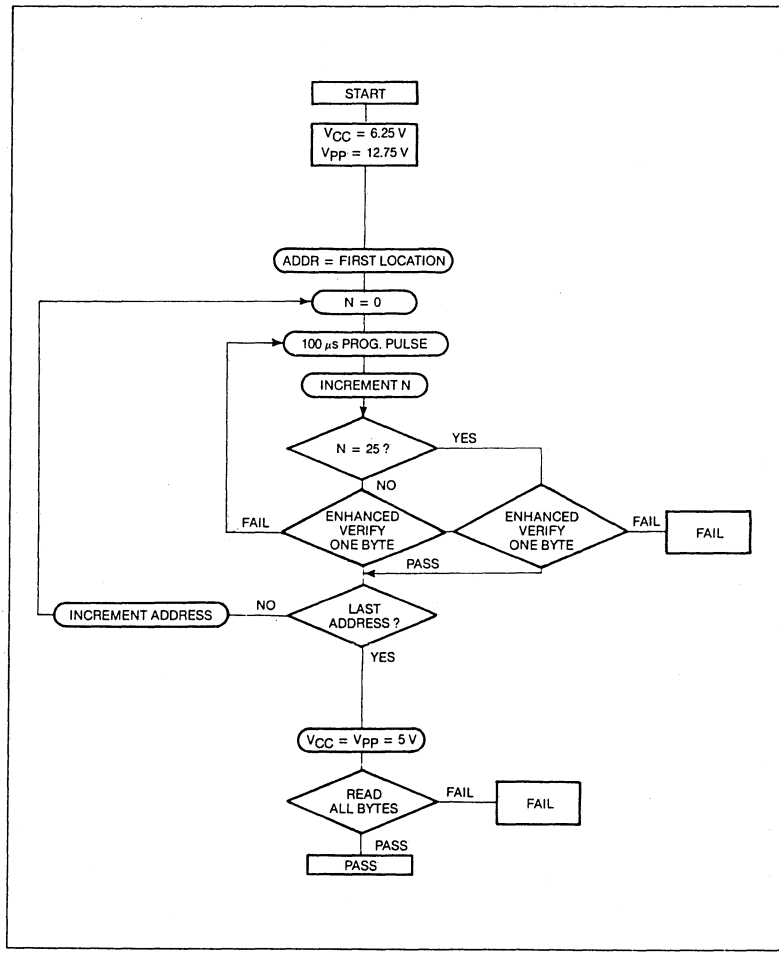
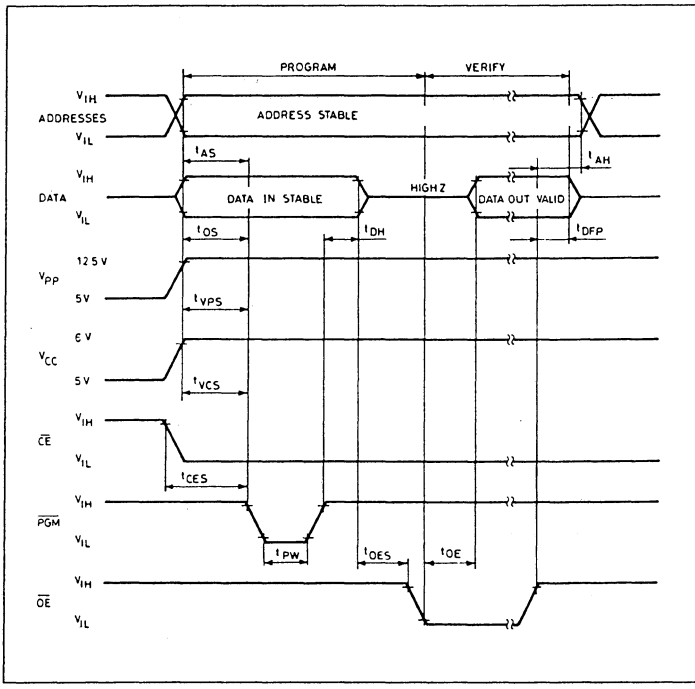


FIGURE 9

6.3.2 - Wave forms



Note 1 : The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.

Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Note 3 : When programming the 27C1024, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 10 - PROGRAMMING WAVEFORMS

7

6.4 - Erasing

The erasure characteristic of the 27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom A. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical 27C1024 in about 3 years, while it would take approximately 1 week cause erasure when expose to direct sunlight. If the 27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the 27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the 27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 A. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The 27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

6.5 · Function table

OPERATING MODES

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUTS
Read	L	L	X	H	V_{CC}	D_{OUT}
Output disable	L	H	X	X	V_{CC}	High Z
Standby	H	X	X	X	V_{CC}	High Z
Program	L	X	X	L	V_{PP}	D_{IN}
Program verify	L	L	X	H	V_{PP}	D_{OUT}
Program inhibit	H	X	X	X	V_{PP}	High Z
Electronic signature	L	L	V_H	H	V_{CC}	CODE

Notes : X = Don't care ; V_H = 12 V ±0.5 V ; H = High ; L = Low.

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-STD-883.

7.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surface.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

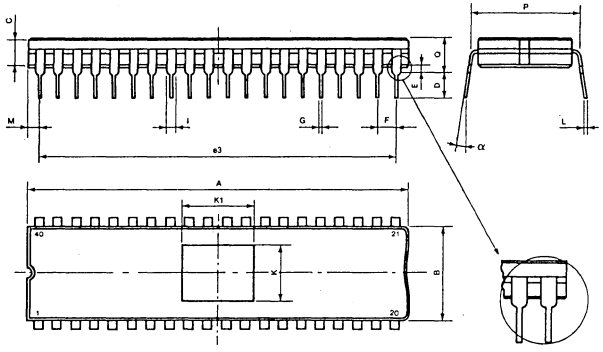
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 percent if practical.

9 - PACKAGE MECHANICAL DATA

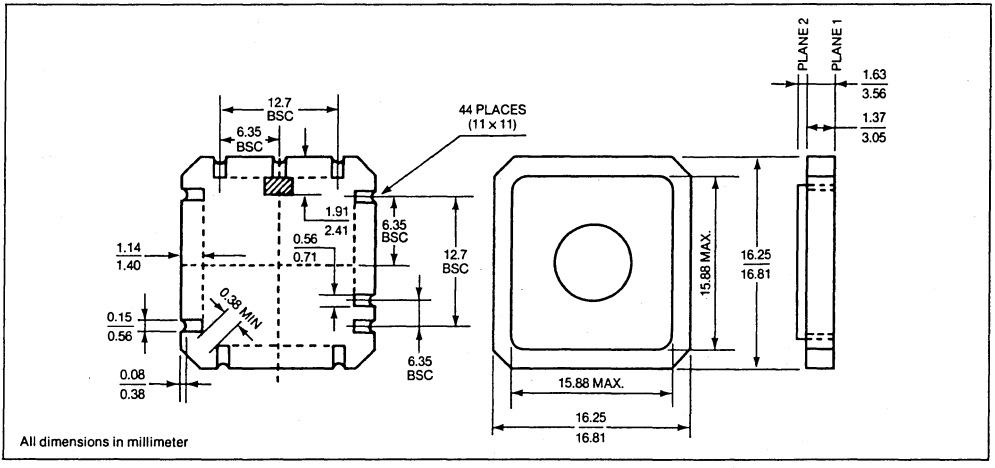
9.1 - DIL CERDIP with window package 40 pins



Symbol	Millimeters		
	Min	Typ	Max
A			53.24
B	12.95		15.75
C	3.90		5.08
D	3.18		5
E	0.38		1.78
e3		48.26	
F		2.54	
G	0.36		0.58
I	0.96		1.65
L	0.20		0.38
M			2.49
P	14.90		16
Q			5.71
K	7.90		8.38
K1	10.41		10.92
α	0		15°

FIGURE 11 - 40-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)

9.2 - 44 pins Leadless Ceramic Chip Carrier



7

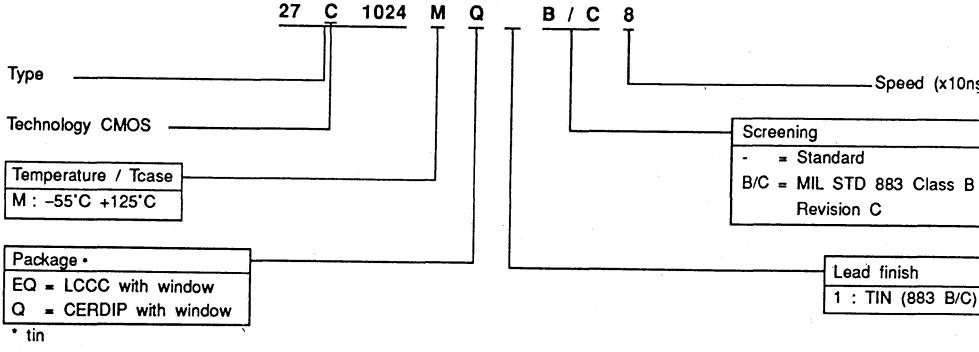
10 · ORDERING INFORMATION

10.1 · HI-REL product

TCS part-number see Note	Norms	Package	Temperature range T_C (°C)	T_{ACC} (ns)	Drawing number
27C1024MQB/C15	MIL-STD-883 C - Class B	Cerdip 40	−55 / +125	150	Non available
27C1024MQB/C20	MIL-STD-883 C - Class B	Cerdip 40	−55 / +125	200	Non available
27C1024MEQ1B/C15	MIL-STD-883 C - Class B	LCCC 44	−55 / +125	150	Non available
27C1024MEQ1B/C20	MIL-STD-883 C - Class B	LCCC 44	−55 / +125	200	Non available
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

10.2 · Standard product

TCS part-number see Note	Norms	Package	Temperature range T_C (°C)	T_{ACC} (ns)	Drawing number
27C1024MQ15	TCS Standard	Cerdip 40	−55 / +125	150	Internal
27C1024MQ20	TCS Standard	Cerdip 40	−55 / +125	200	Internal
27C1024MQ25	TCS Standard	Cerdip 40	−55 / +125	250	Internal
27C1024MEQ15	TCS Standard	LCCC 44	−55 / +125	150	Internal
27C1024MEQ20	TCS Standard	LCCC 44	−55 / +125	200	Internal
27C1024MEQ25	TCS Standard	LCCC 44	−55 / +125	250	Internal
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

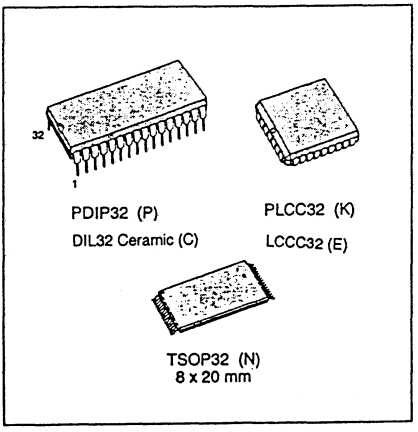


PRELIMINARY

M29F040

CMOS 4 Megabit (512K x 8, 8 sectors) SINGLE SUPPLY FLASH MEMORY

- VERY FAST ACCESS TIME : 70 ns
- 5 V ± 10 % SUPPLY VOLTAGE for PROGRAM and ERASE OPERATIONS
- 5 V ± 10 % SUPPLY VOLTAGE in READ OPERATIONS
- 10 µs TYPICAL PROGRAMMING TIME
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E.C. Status
- MEMORY ERASE in SECTORS
  - 8 Sectors of 64K Bytes each
  - Sector Protection
  - Multisector Erase
- ERASE SUSPEND and RESUME
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- LOW POWER CONSUMPTION
  - 25 µA Typical in Standby
- STANDARD EPROM/OTP MEMORY PACKAGES : TSOP32, PLCC32 and PDIP32, CERAMIC DIL32, LCCC32
- EXTENDED TEMPERATURE RANGES
  - 55 to + 125° C, MIL STD 883 quality level



DESCRIPTION

The M29F040 is a non-volatile memory that may be erased electrically at the sector level, and programmed Byte-by-Byte.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

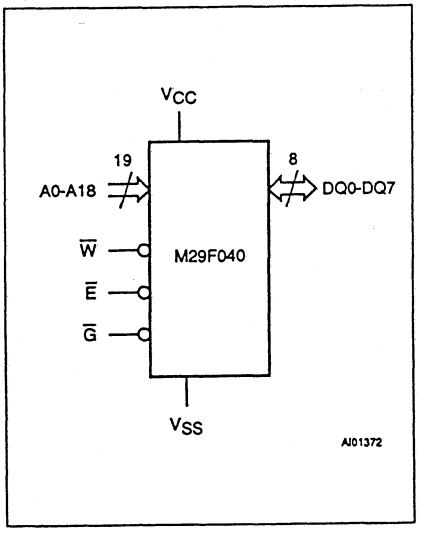


Figure 2A. DIP Pin Connections

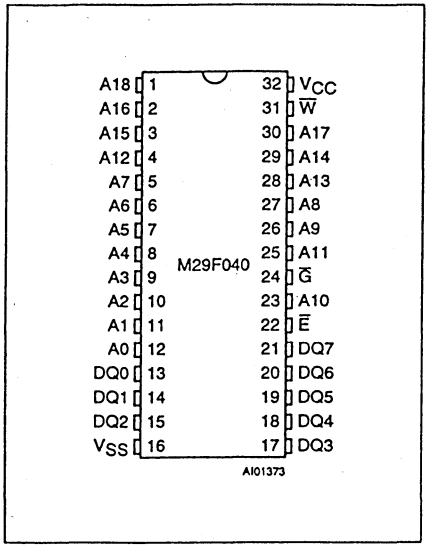


Figure 2B. LCC Pin Connections

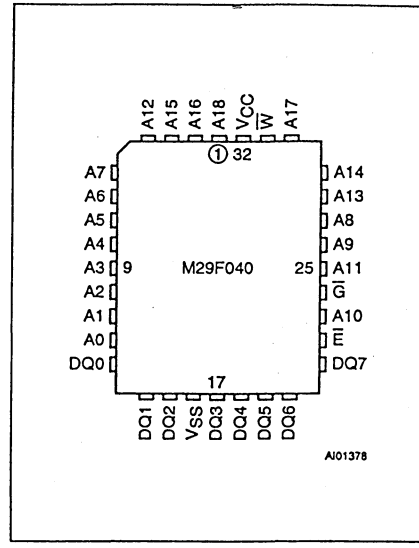
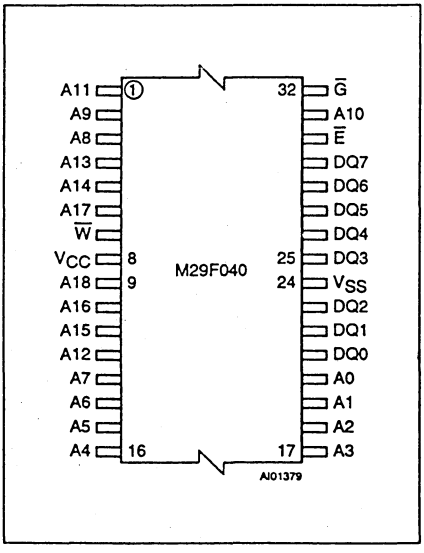


Figure 2C. TSOP Pin Connections



DESCRIPTION (cont'd)

The interface is directly compatible with most microprocessors. PDIP32, PLCC32 and TSOP32 (8 x 20mm) packages are used. Both normal and reverse pin outs are available for the TSOP32 package.

Organisation

The Organisation is 512K x 8 bits with Address lines A0-A18 and Data Inputs/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable Inputs.

Erase and Program are performed through the internal Program/Erase Controller (P/E.C.).

Data Outputs bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Sectors

Erasure of the memory is in sectors. There are 8 sectors of 64K bytes each in the memory address space. Erasure of each sector takes typically 1.5 seconds and each sector can be programmed and erased over 100,000 cycles. Each sector may separately be protected and unprotected against program and erase. Sector erasure may be sus-

Table 2. Absolute Maximum Ratings(1)

Symbol	Parameter	Value	Unit
T_C	Case temperature	–55 to +125	°C
T_{STG}	Storage temperature	–65 to 150	°C
V_{IO}(2)	Input or Output voltages	–0.6 to 7	V
V_{CC}	Supply voltage	–0.6 to 7	V
V_{A9}(2)	A9 voltage	–0.6 to 13.5	V

Note : 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ragings" may cause permanent damage to the device. These are stess ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposutre to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to –2 V during transisiton and for less than 20 ns.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}

pended, while data is read from other blocks of the memory, and then resumed.

Bus Operations

Seven operations can be performed by the appropriate bus cycles, Read Array, Read Electronic Signature, Output Disable, Standby, Protect Sector, Unprotect Sector, and Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface (C.I.) latch to perform Reading (from the Array or Electronic Signature), Erasure or Programming. For added data protection, command execution starts after 4 or 6 command cycles. First, second, fourth and fifth cycles are used to input a code sequence to the Command Interface (C.I.). This sequence is equal for all P/E.C. instructions. Command itself and its confirmation - if it applies - are given on the third and fourth cycles.

Instructions

Seven instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Program, Sector Auto Erase, Auto Bulk Erase, Sector Erase Suspend and Sector Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle, and Status data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two input a code sequence to the Command Interface which is common to all P/E. C. instructions (see Table 7 for Command Descriptions). The third cycle inputs the instruction set up command instruction to the Command Interface. Subsequent cycles output the addressed data for Read operations. For added data protection, the instructions for program and sector or bulk erase require further command inputs. For a Program instruction, the

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E2h

Table 5. Sector Protection Status

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A16	A17	A18	Other Addresses	DQ0 - DQ7
Protected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	01h
Unprotected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	00h

Note: SA = Address of sector being checked

DESCRIPTION (cont'd)

fourth command cycle inputs the address and data to be programmed. For an Erase instruction (sector or bulk), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs while erase is performed in typically 1.5 seconds.

Erasure of a memory sector may be suspended, in order to read data from another sector, and then resumed. Data Polling, Toggle and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address inputs for the memory array are latched during a write operation. The A9 address input is used also for the Electronic Signature read and Sector Protect verification. When A9 is raised to V_{ID}, either a Read Manufacturer Code, Read Device Code or Verify Sector Proctection is enabled depending on the combination of levels on A0, A1 and A6. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read, when A0 is High and A1 and A6 are Low, the Device code is read, and when A1 is High and A0 and A6 are low, the Sector Protection Status is read.

DQ0-DQ7 Data Input/Outputs. The data input a byte to be programmed or a command written to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (DQ7), the Toggle Bit (DQ6), the Error bit (DQ5) or the Erase Timer bit (DQ3). Ouputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{E}$ while datas on the rising edge of $\overline{E}$.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation. $\overline{G}$ is forced to V_{ID} level during Sector Protect and Sector Unprotect operations.

$\overline{W}$ Write Enable. This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Table 6A. Instructions

Mne.	Instr.	Cyc.	1st Cycle			2nd Cycle			3rd Cycle			4th Cycle		
			Op.	Addr. [1,5]	Data	Op.	Addr. [1,5]	Data	Op.	Addr. [1,5]	Data	Op.	Addr. [1]	Data
RD	Read/ Reset Memory Array	1+	Write	X	0F0h	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0F0h	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read [2,3]	Signature Address	Signature
RSP	Read Sector Protection	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read [2,4]	Protection Address	Protect Status [6]
PG	Program	4	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0A0h	Write	Address	Data Input
SE	Sector Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h [6]	0AAh
BE	Bulk Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h [6]	0AAh
ES	Erase Suspend	1	Write	X	0B0h	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase.								
ER	Erase Resume	1	Write	X	30h	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes:
1. X = Don't Care.
2. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
3. Signature Address bits A0, A1, A6 at V_L will output Manufacturer code (20h). Address bits A0 at V_H and A1, A6 at V_L will output Device code (0E2h).
4. Protection Address: A0, A6 at V_L and A1 at V_H, other addresses within the sector to be checked A16, A17, A18 define this Sector Address.
5. Address bits A16, A17, A18 are don't care for coded address inputs
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed.

Table 6B. Instructions

Mne.	Instr.	Cyc.	5th Cycle			6th Cycle			7th Cycle		
			Op.	Addr. [1]	Data	Op.	Addr.	Data Out.	Op.	Addr.	Data Out.
RD	Read/ Reset Memory Array	1+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Read [2,3]	Signature Address	Signature	Read [2,3]	Signature Adress	Signature	Read [2,3]	Signature Adress	Signature
RSP	Read Sector Protection	3+	Read [2,4]	Protection Address	Protect Status [6]	Read [2,4]	Protection Address	Protect Status [6]	Read [2,4]	Protection Address	Protect Status [6]
PG	Program	4	Read Data Polling or Toggle Bit until Program completes								
SE	Sector Erase	6	Write	x2AAAh [5]	55h	Write	Sector Address	30h	Write [6]	Additional Sector	30h
BE	Bulk Erase	6	Write	x2AAAh [5]	55h	Write	x5555h [5]	10h	Read Data Polling or Toggle bit until Erase completes or Erase is suspended another time		
ES	Erase Suspend	1	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase.								
ER	Erase Resume	1	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes:
1. X = Don't Care.
2. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
3. Signature Address bits A0, A1, A6 at V_L will output Manufacturer code (20h). Address bits A0 at V_H and A1, A6 at V_L will output Device code (0E2h).
4. Protection Address: A0, A6 at V_L and A1 at V_H, other addresses within the sector to be checked A16, A17, A18 define this Sector Address.
5. Address bits A16, A17, A18 are don't care for coded address inputs
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed.

Memory Sectors

The memory sectors of the M29F040 are shown in Figure 5. The memory array is divided in 8 sectors of 64K bytes. Each sector can be erased separately or any combination of sectors can be erased simultaneously. The Sector Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any another sector, and then resumed.

Sector Protection provides additional data security. Each sector can be separately protected or unprotected against Program or Erase. Bringing A9 and $\overline{G}$ to V_{ID} initiates protection, while bringing A9, $\overline{G}$ and $\overline{E}$ to V_{ID} cancels the protection. The sector affected is addressed by the inputs on A16, A17, and A18.

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Bulk Erase Confirm
30h	Sector Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Sector protection Status
0A0h	Program
0B0h	Erase Suspend
0F0h	Read Array/Reset

Table 8. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase on Going	
		DQ	Program Complete	
		$\overline{DQ}$	Program on Going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program on Going	Sucessive read output complementary datas on DQ6 while Programming or Erase operations are going on. DQ6 remain at constant level when P/E.C. operations are completed.
		'-0-0-0-0-0-0-0-'	Program ('0' on DQ6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on DQ6) Complete	
5	Error Bit	'1'	Program or Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
		'0'	Program or Erase Success	
4		'1'		
		'0'		
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). Additional sector to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period on Going	
2				
1				
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Table 9. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

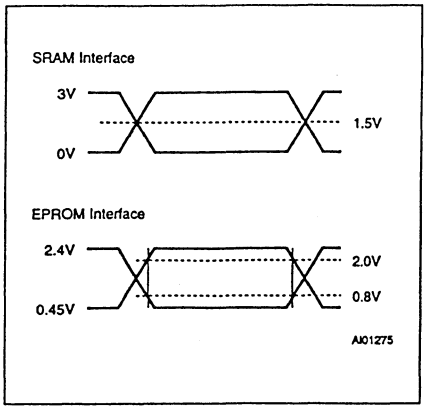


Figure 4. AC Testing Load Circuit

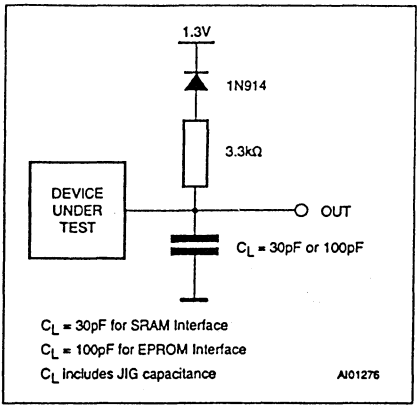


Table 10. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

7

Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, Sector Protect/Unprotect, Sector Protection Check and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD and RSIG, and Status Bits).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs last.

Figure 5. Memory Map and Sector Address Table

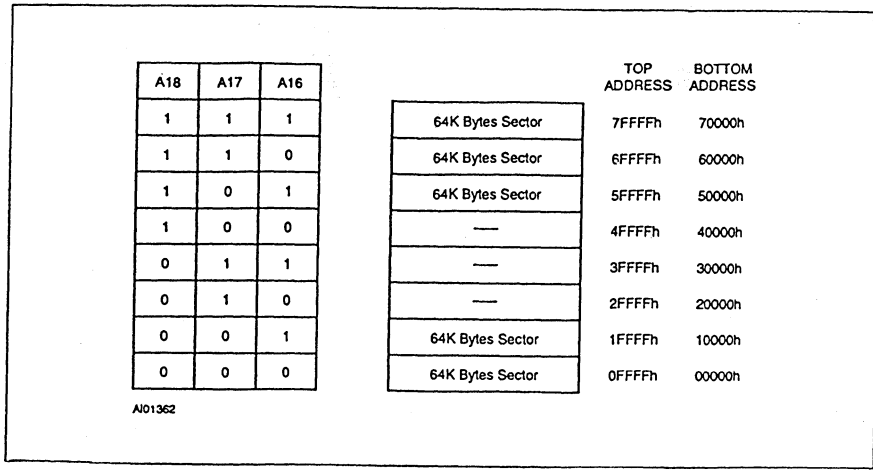


Table 11. DC Charecterlstics
(T_C = –55 to +125° C ; VCC = 5 V ± 10 %)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 6MHz		40	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Sector or Bulk Erase in progress		60	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
		I_{OH} = –2.5mA	0.85 x V_{CC}		V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		50	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		3.2	4.2	V

Table 12A. Read AC Characteristics
(T_C = –55 to +125°C)

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from dhe memory, the manufacturer's code for TCS is 20h, and the device codes is E2h for the M29F040. These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 and A6 are at low. The manufacturer code is output when the Address Input A0 is Low and the device code when this input is High. Other Address Inputs are ignored. The codes are output on DQ0 DQ7. This is shown in Table 4.

The Electronic Signature can also be read, without raising A9 to V_{ID} by giving the memory the instruction RSIG (see below).

Sector Protection. Each sector can be separately protected against Program or Erase. Sector Protection provides additional data security, as it disables all program or erase operations. This

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-70		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	70		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 12B. Read AC Characteristics
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-120		-150		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

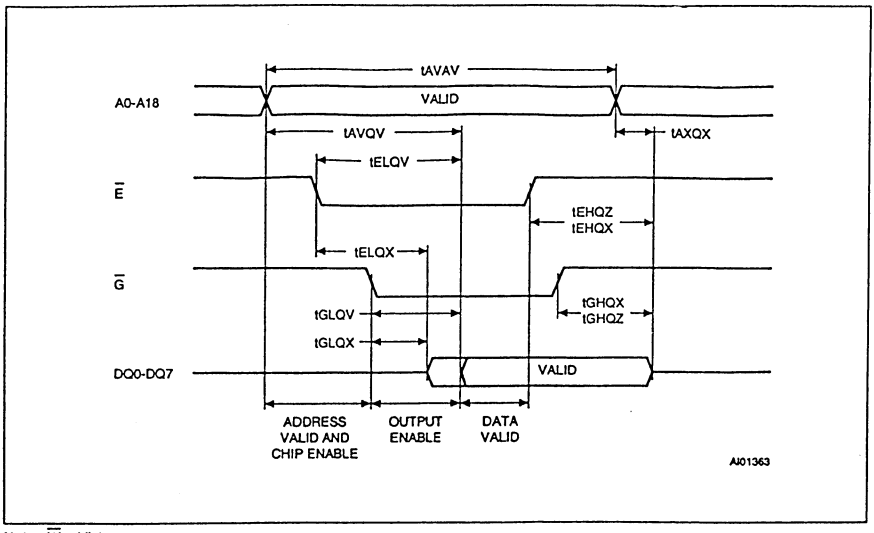
Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

DEVICE OPERATION (cont'd)

mode is activated when both A9 and $\overline{G}$ are set to V_{ID} and the sector address is applied on A16, A17 and A18. Sector protection is programmed using a Presto F program like algorithm. Protection is initiated by edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100us, the edge of $\overline{W}$ rising to V_{IH} will end the protection operation. Protection verify is achieved by bringing $\overline{G}$, $\overline{E}$ and A6 to V_{IL} while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the sector defined by the inputs on A16, A17 and A18 is protected. Any attempt to program or erase a protected sector will be ignored by the device.

Any protected sector can be unprotected to allow content updating. All sectors must be protected before an unprotect operation. Sector unprotect is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID}. The addresses inputs A6, A16, A12 must be maintained at V_{IH}. Sector unprotect is performed through a Presto F Erase like algorithm. Unprotect is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the edge of $\overline{W}$ rising to V_{IH} will end the unprotection operation. Unprotect verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A6 and $\overline{W}$ are at V_{IH} and A9 at V_{ID}. In these conditions, reading the output data will yield 00h if the sector defined by the inputs on A16, A17 and A18 is protected. All combinations of A16, A17 and A18 must be addressed in order to ensure that all of the 8 sectors have been unprotected. Sector Protection Status is shown in Table 5.

Figure 6. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Electronic Signature, Sector Erase, Bulk Erase, Program, Sector Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ and data is latched on the rising of $\overline{W}$ or $\overline{E}$. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialised by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceeded by the two coded cycles.

P/E.C. status is indicated during command execution by Data Polling on DQ7, detection of Toggle on DQ6, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output those four bits. The P/E.C. automatically sets bits DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1, DQ2 and DQ4) are reserved for future use and should be masked.

Data Polling Bit DQ7. When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it will outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. It must be performed at the address being programmed or at an address within the sector being erased. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ7 will set to data complement for about 100µs for erase, and then return to previous addressed memory data. The programming of a protection sector is ignored. See Figure 9 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms.

7

Table 13A. Write AC Characteristics, Write Enable Controlled
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		45		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQV} + t_{QVQV}$

Toggle Bit DQ6. When Programming operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$ or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ6 will toggle for about 2µs for programming and 100us for erase and then stop toggling and return back to Read. See Figure 11 for Toggle Bit flowchart and Figure 12 for Toggle Bit waveforms.

Error bit DQ5. This bit is set to '1' by the P/E.C when there is a failure of byte programming, sector erase, or bulk erase that results in invalid data being programmed in the memory sector. In case of error in sector erase or byte program, the sector in which the error occured or to which the programmed byte belongs, must be discarded. Other sectors may still be used. Error bit resets to '0' after Read/Reset (RD) instruction.

Erase Timer bit DQ3. This bit is set to '0' by the P/E.C. when the last Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the waiting period is finished, DQ3 returns back to '1'.

Coded Cycles. The two coded cycles unlock the Command Interface. They are followed by a com-

Table 13B. Write AC Characteristics, Write Enable Controlled
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQTV} + t_{QTVQV}$

mand input or a comand confirmation. They consist in writing the data 0AAh at address 5555h during first cycle and data 55h at address 2AAAh during second cycle. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ while data is latched on the rising edge of $\overline{W}$ or $\overline{E}$. They happen on first and second cycles of the command write or on the fourth and fifth cycle.

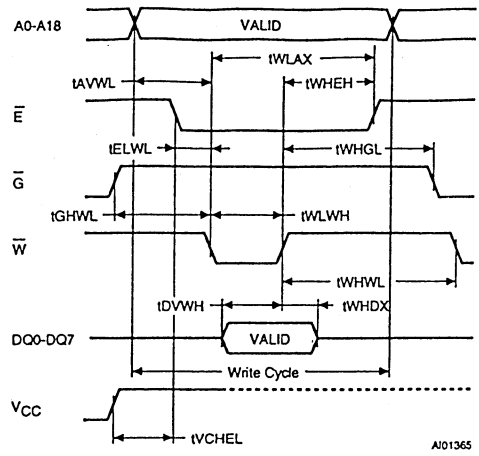
Read (RD) Instruction. The Read instruction consists of one write operation giving the command 0F0h at address 2555h. It can be optionally preceded by the two coded cycles. Subsequent read operations will read the memory array addressed and output the read byte.

Read Electronic Signature (RSIG) instruction. This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. Subsequent read will output the manufacturer code, the device code or the sector protection status depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, 0E2h is output when A0 is High with A1 and A6 Low.

Read Sector Protection. The use of Read Electronic Signature (RSIG) command also allows access to the sector protection status verify. After

7

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

DEVICE OPERATION (cont'd)

giving the RSIG command, A0 and A6 are set to V_{IL} with A1 at V_{IH}, while A16, A17 and A18 define the sector of the sector to be verified. A read in these conditions will output a 01h if sector is protected and a 00h if sector is not protected.

Bulk Erase (BE) instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Bulk Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle Bit DQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Sector Erase (SE) instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Sector Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During

Table 14A. Write AC Characteristics, Chip Enable Controlled
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		45		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	30		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

7

the input of the second command an address within the sector to be erased is given and latched into the memory. Additional Sector Erase confirm commands and sector addresses can be written subsequently to erase other sectors in parallel without further coded cycles. The erase will start after an Erase timeout period of about 100us. Thus, additional Sector Erase commands must be given within this delay. The input of a new Sector Erase command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Sector Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C is erasing the sector(s). If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the sector with 00h as the P/E.C. will do this automatically before to erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) instruction. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle Bit DQ6 toggles during erase operation. It stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed.

Table 14B. Write AC Characteristics, Chip Enable Controlled
(T_C= –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQV1} + t_{QVQV}$

Program (PG) instruction. This instruction uses four write cycles. The Program command A0h is written on third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on its rising edge and starts the P/E.C. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a Byte.

Erase Suspend (ES) instruction. The Sector Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another sector while erase is in progress. Erase suspend is accepted only during the Sector Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle Bit DQ6 stops toggling when the P/E.C. is suspended. Toggle Bit status must be monitored at an address out of the sector being erased. During the suspension the memory will respond only to Read (RD), or Erase Resume (ER) instructions. Read operations initially output the status bits while erase is suspended but, following a Read instruction, data from other sectors of the memory can be read.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycle.

Table 15A. Data Polling and Toggle Bit AC Characteristics(1)
(T_C = –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Erase $\overline{W}$ Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program E Controller		10		10	µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Erase $\overline{E}$ Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		30		35	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Programing. The memory can be programmed byte-by-byte. The program sequence is started by two coded cycles, followed by writing the Program command (0A0h) to the Command Interface, this is followed by writing the address and data byte to the memory. The Program/Erase Controller automatically starts and performs the programming after the fourth write operation. During programming the memory status is checked by reading the status bits DQ3, DQ5, DQ6 and DQ7 which shows the status of the P/E.C. DQ6 and DQ7 determine if programming is on going or has completed and DQ5 allows a check to be made for any possible error.

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ should be tied to V_{IH} to allow maximum security. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

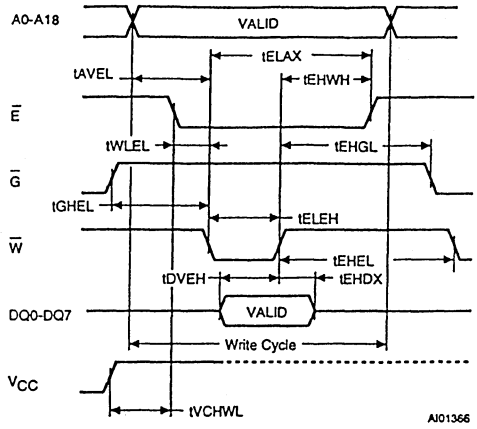
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 15B. Data Polling and Toggle Bit AC Characteristics(1)
(T_C= –55 to +125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Erase $\overline{W}$ Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program E Controller		10		10	µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Erase $\overline{E}$ Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Figure 9. Data Polling Flow-chart

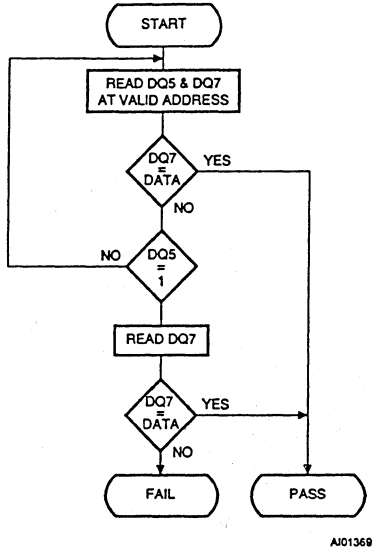
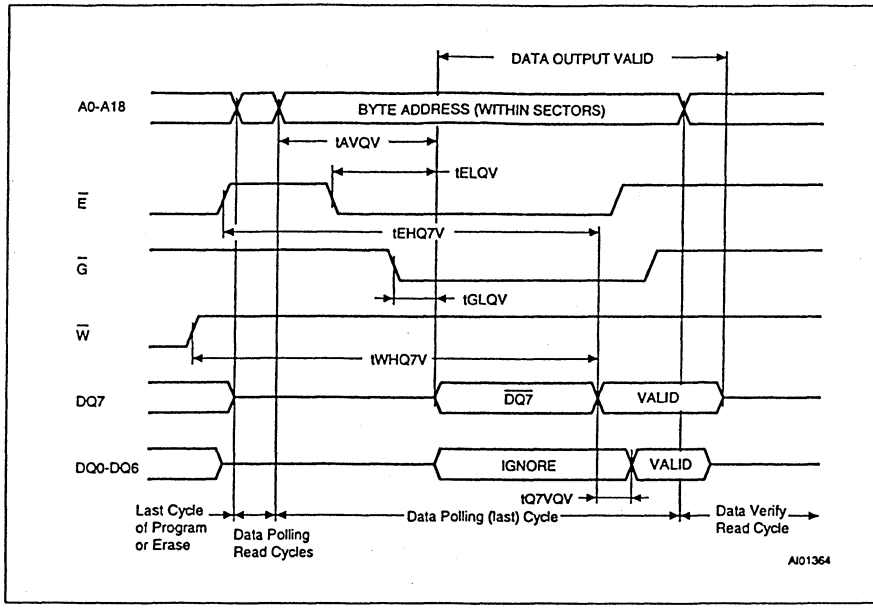


Figure 10. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased.

Figure 11. Data Toggle Flow-chart

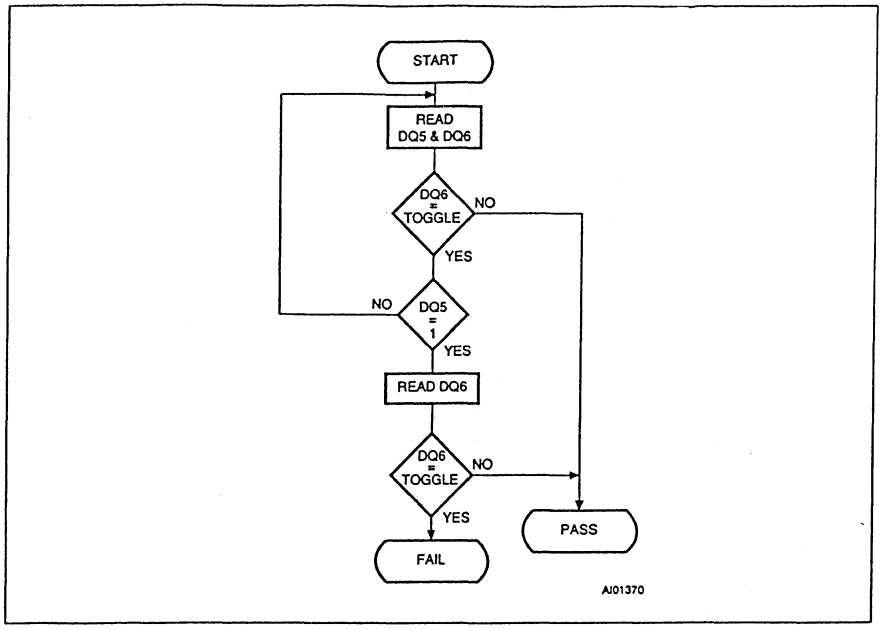
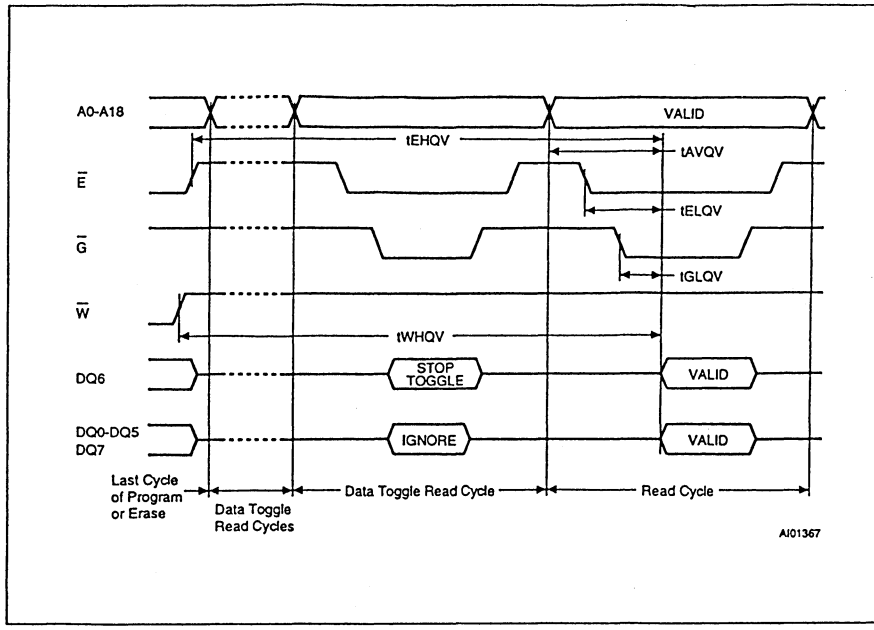


Figure 12. Data Toggle DQ6 AC Waveforms



Note: All other timings are as a normal Read cycle.

Table 16. Program, Erase Times and Program, Erase Endurance Cycles
(T_C = –55 to +125°C)

Parameter	M29F040			Unit
	Min	Typ	Max	
Chip Program (Byte)		8.5		sec
Bulk or Sector Erase		1.5	30	sec
Byte Program		10		µs
Program/Erase Cycles	100,000			cycles

Figure 13. Sector Protection Flow-chart

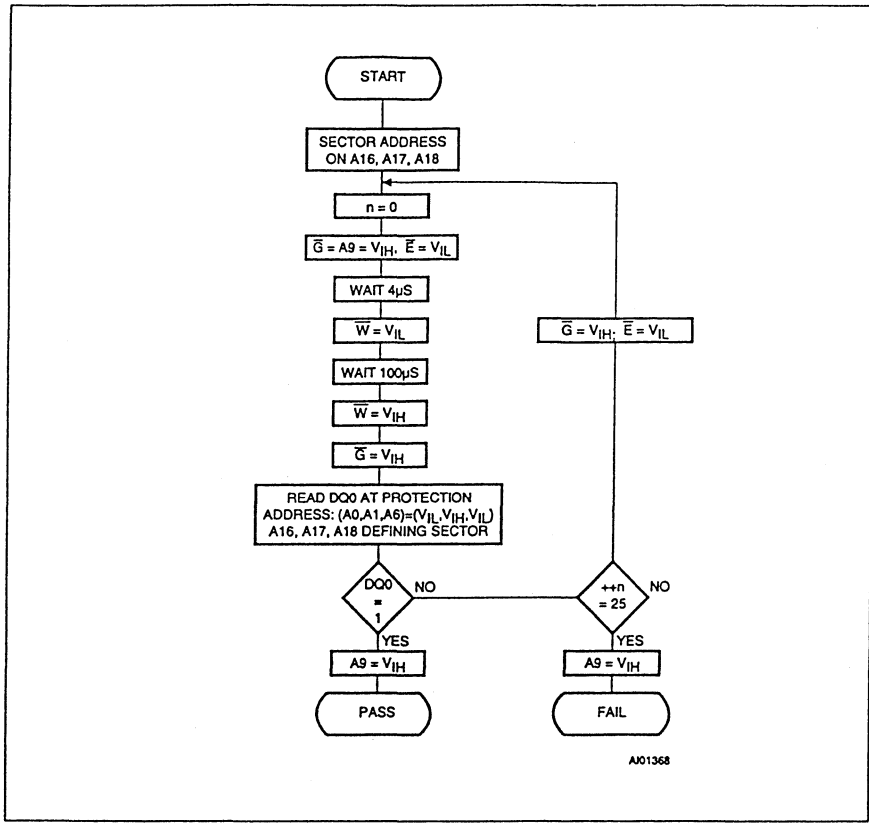
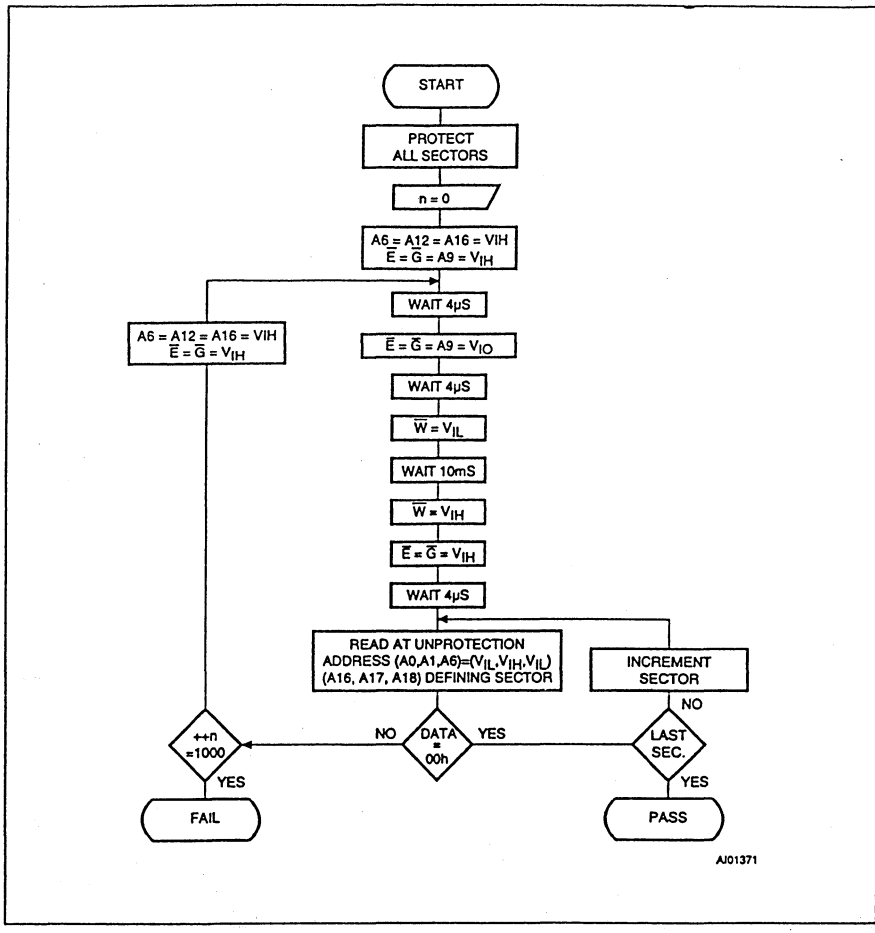
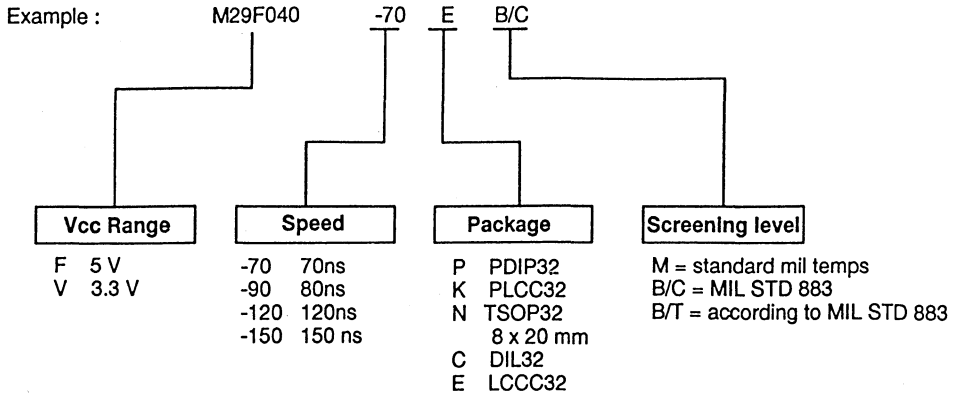


Figure 14. Sector Unprotecting Flow-chart



ORDERING INFORMATION SCHEME



Full data on the 3V product, M29V040, will be added to this document in the near future.

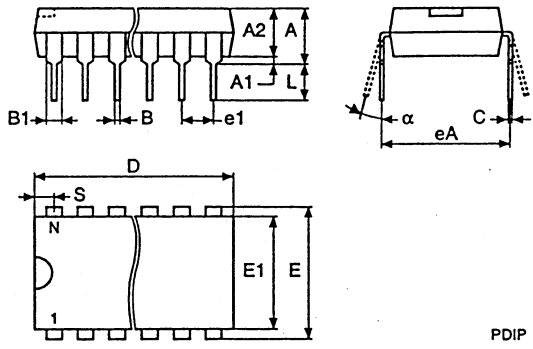
For further information on any aspect of this device, please contact THOMSON-CSF SEMICONDUCTORS SPECIFIQUES Sales Office nearest to you.

7

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



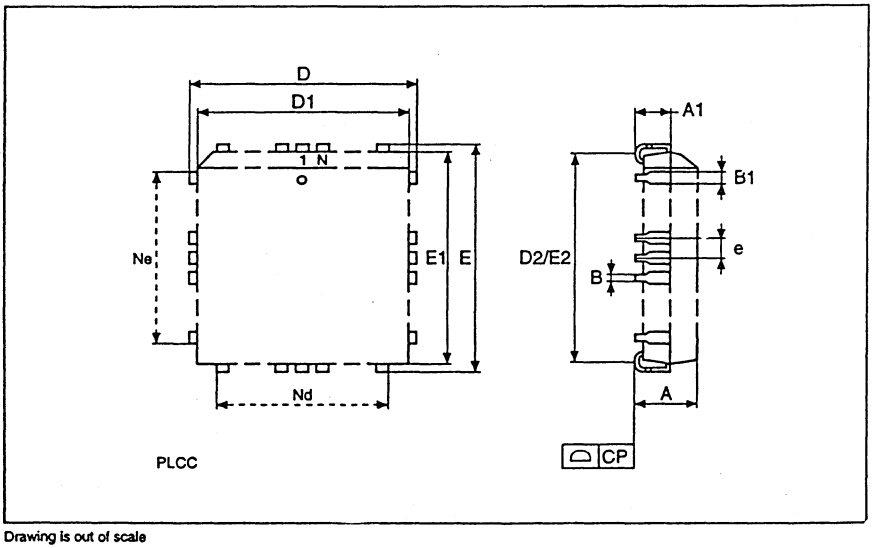
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

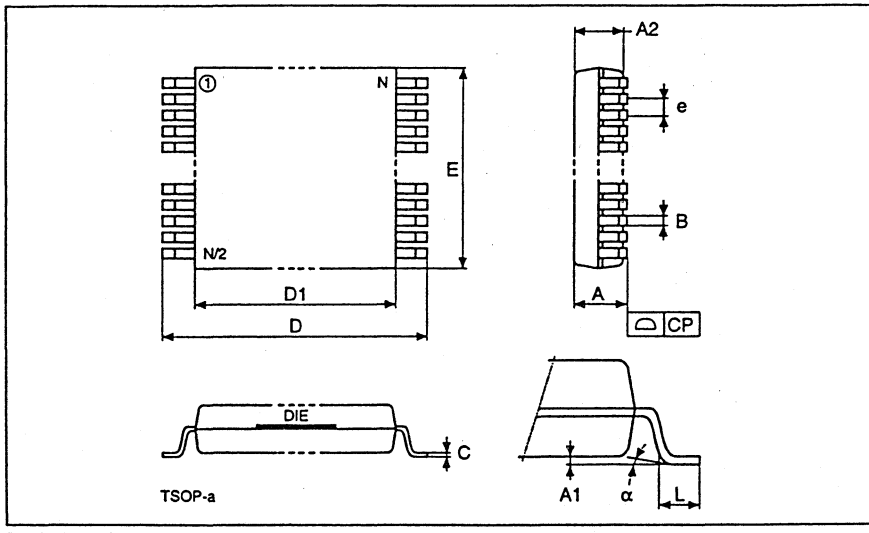


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20 mm

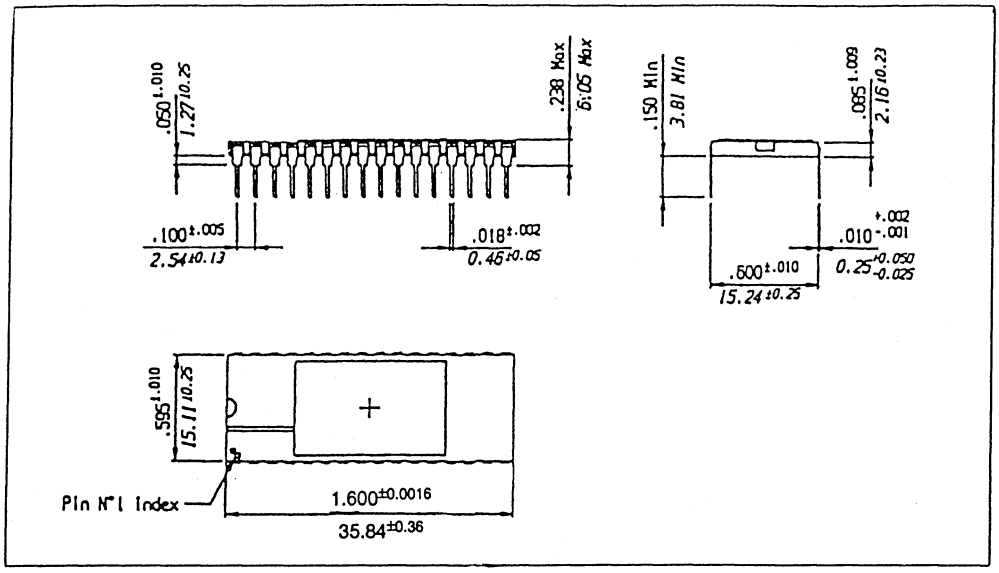
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0 °C	5 °C		0 °C	5 °C
N		32			32	
CP			0.10			0.004

TSOP32



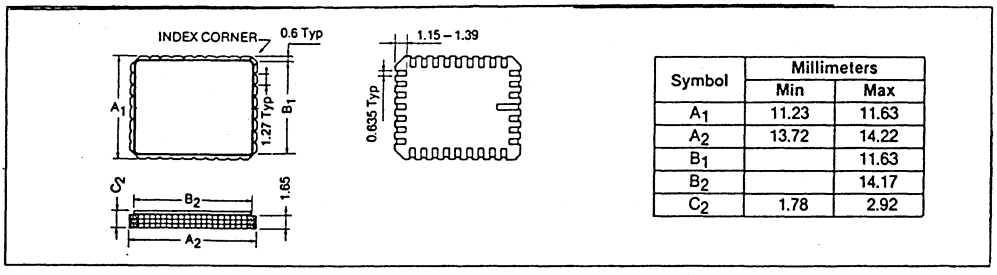
Drawing is out of scale

DIL 32 - 32 pin Ceramic DIL, 600 mils width



7

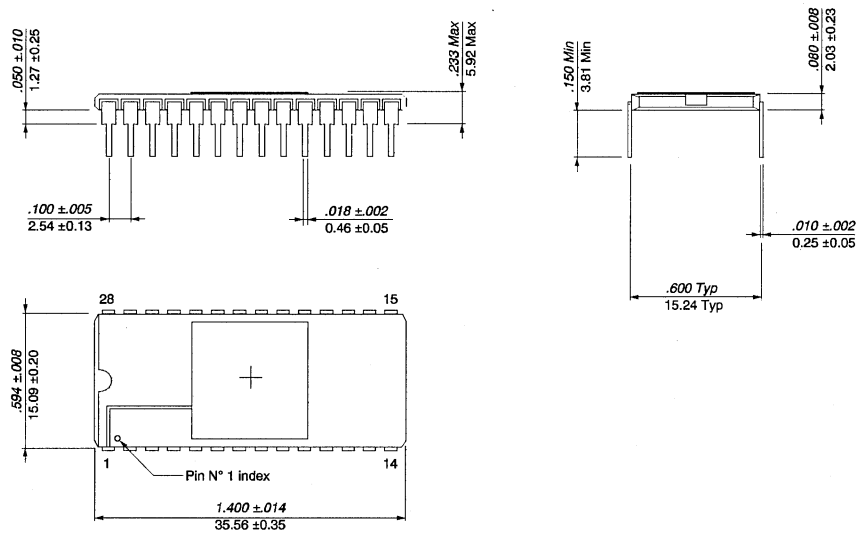
LCCC 32 - lead Leaded Ceramic Chip Carrier, rectangular



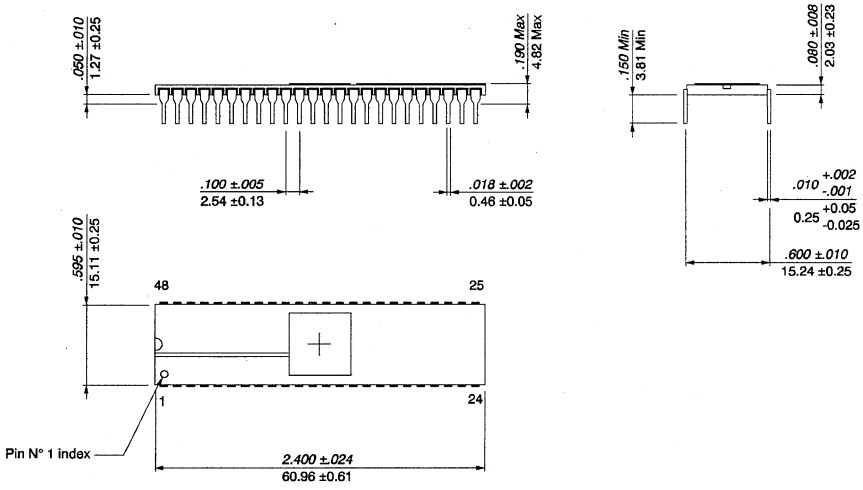
Symbol	Millimeters	
	Min	Max
A_1	11.23	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92

Dimensions in *inches* / mm

DIL 28



DIL 48

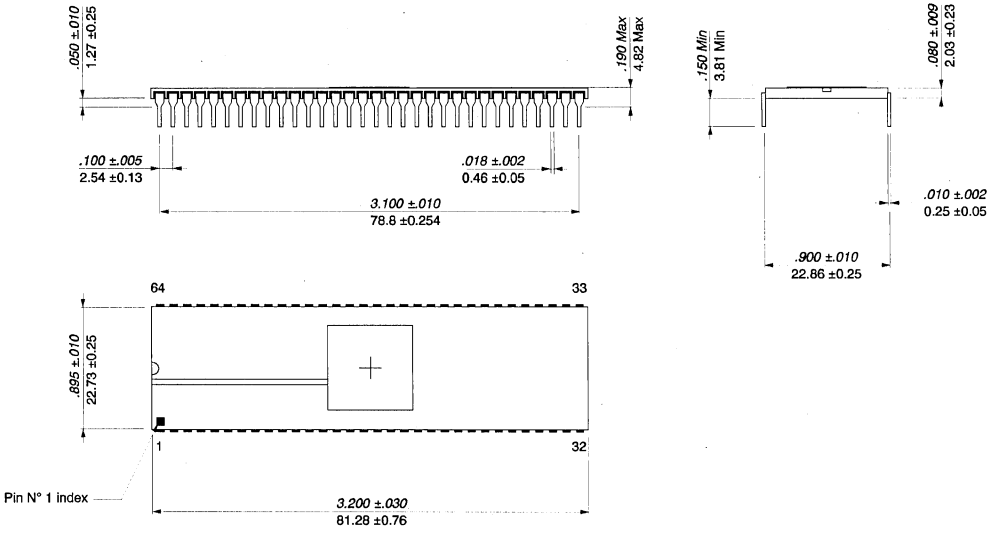


8

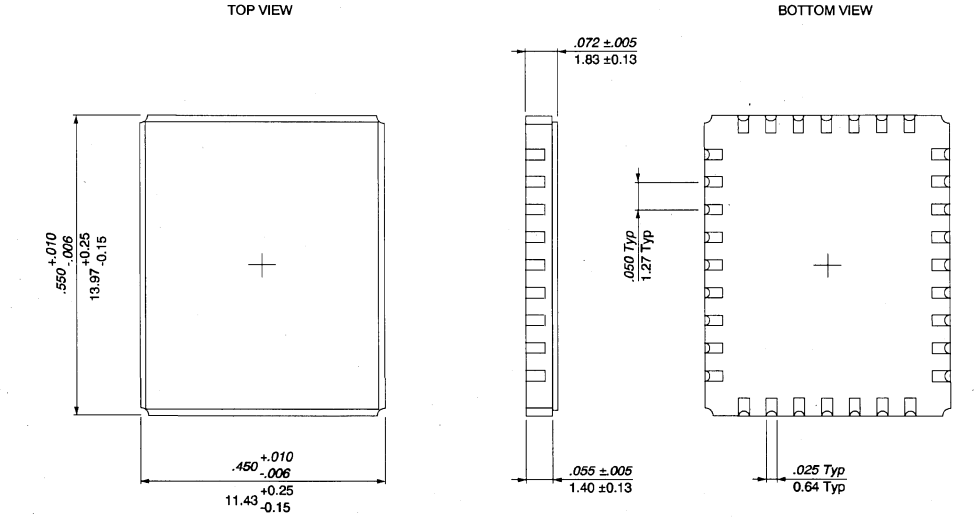
PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

DIL 64

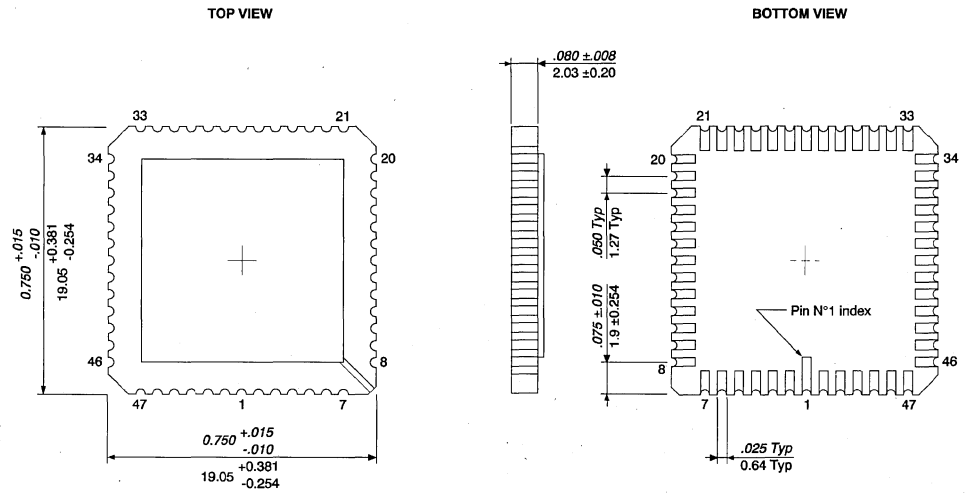


LCCC 32

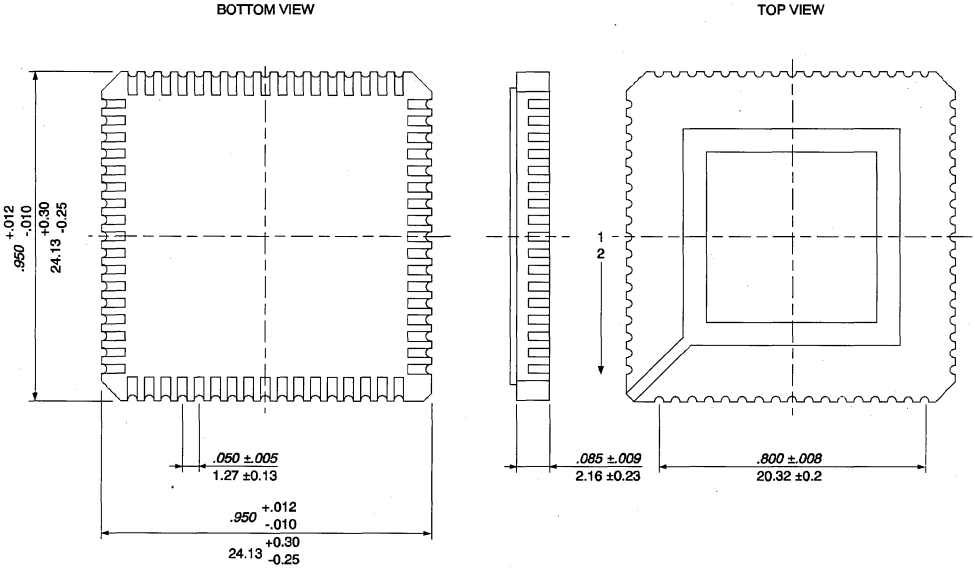


Dimensions in $\frac{inches}{mm}$

LCCC 52



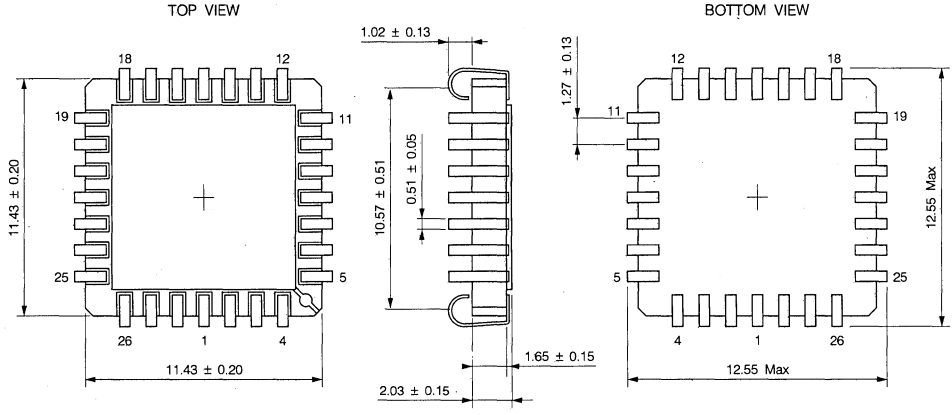
LCCC 68



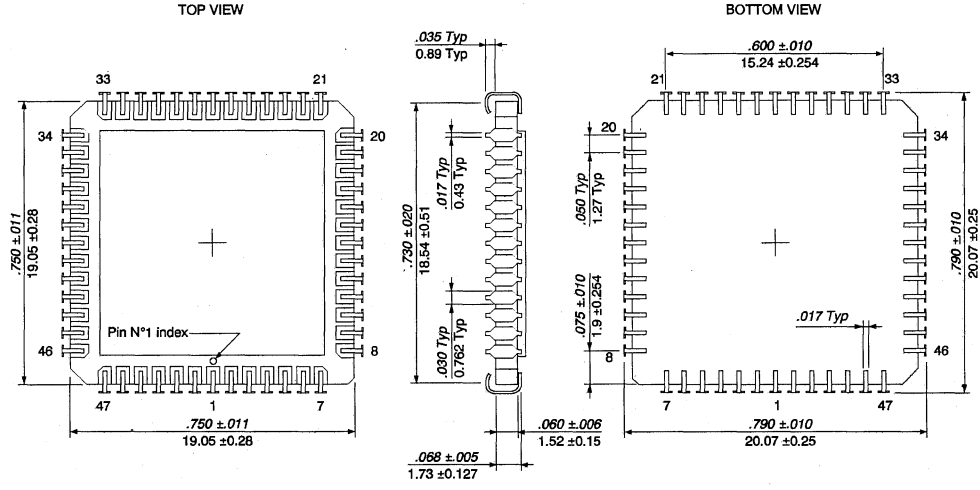
PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

LDCC 28

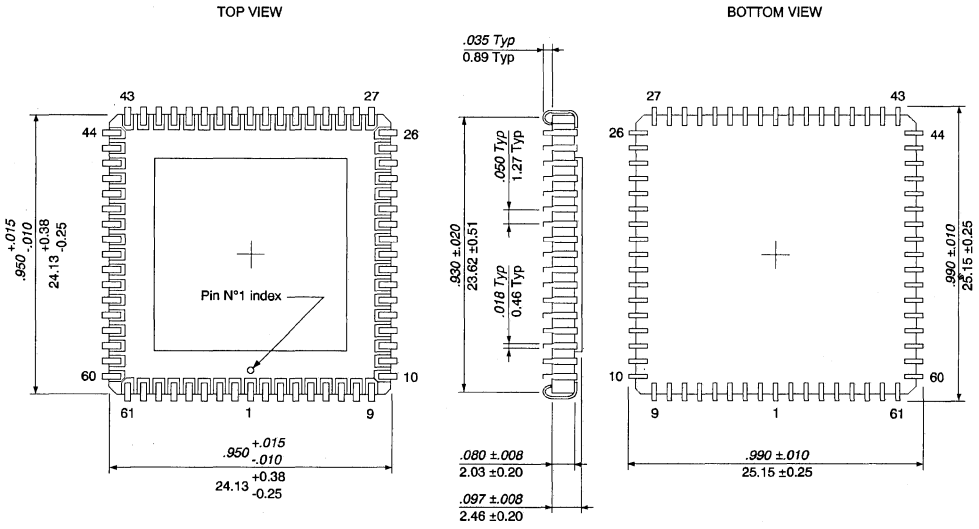


LDCC 52



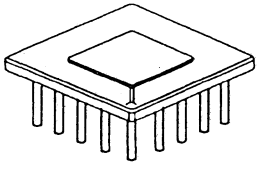
Dimensions in $\frac{inches}{mm}$

LDCC 68



8

PGA 29

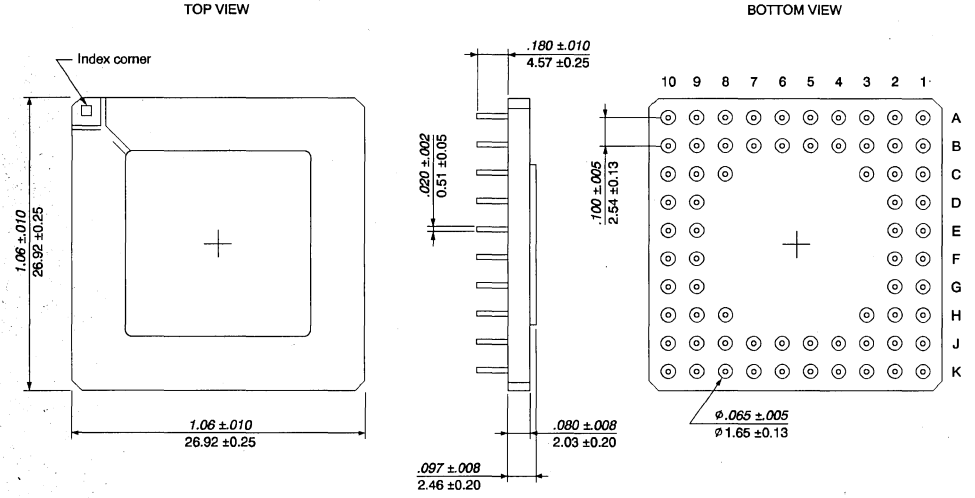


To be defined

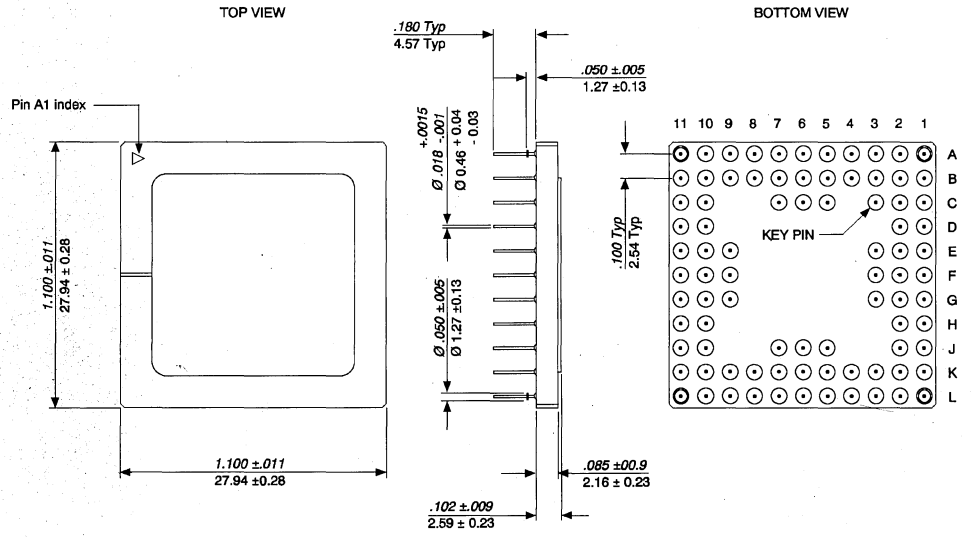
PACKAGE OUTLINES

Dimensions in *inches* / mm

PGA 68

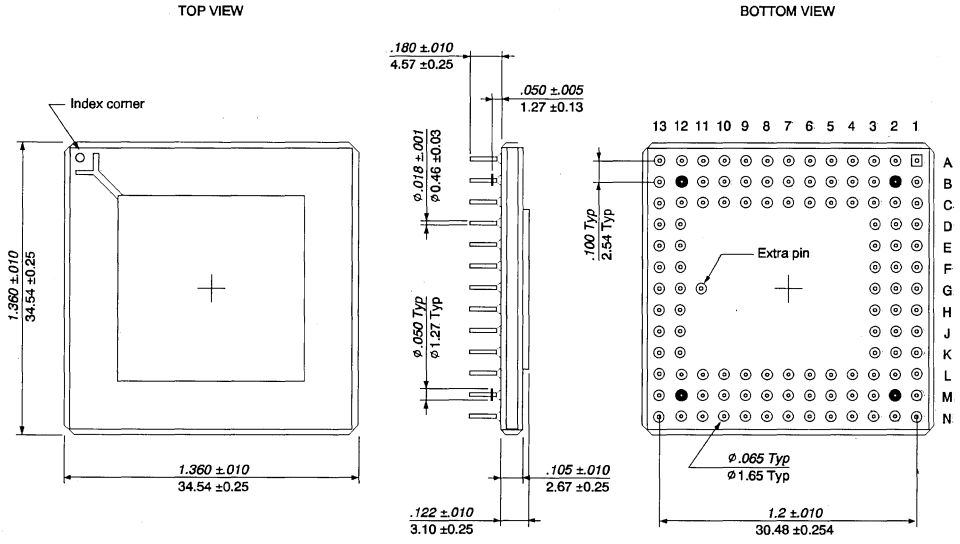


PGA 84



Dimensions in $\frac{inches}{mm}$

PGA 114

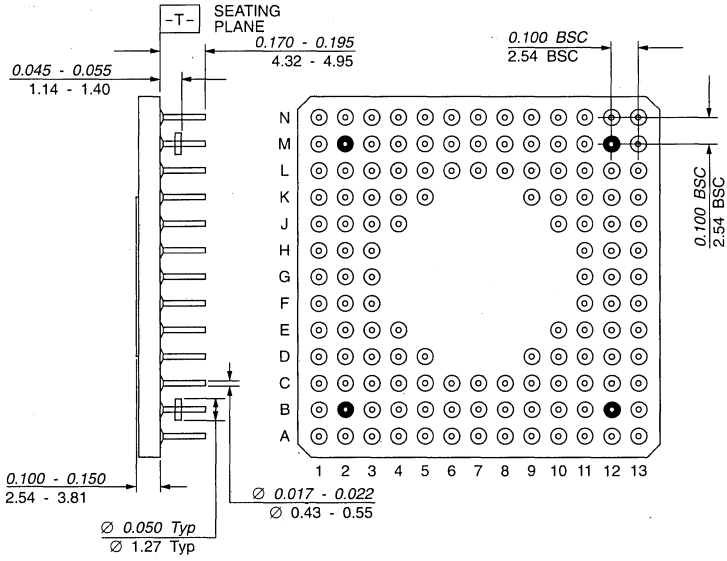


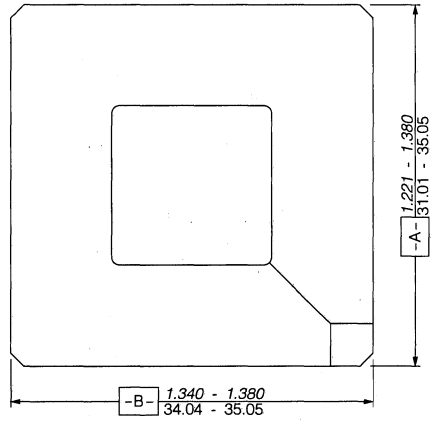
8

PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

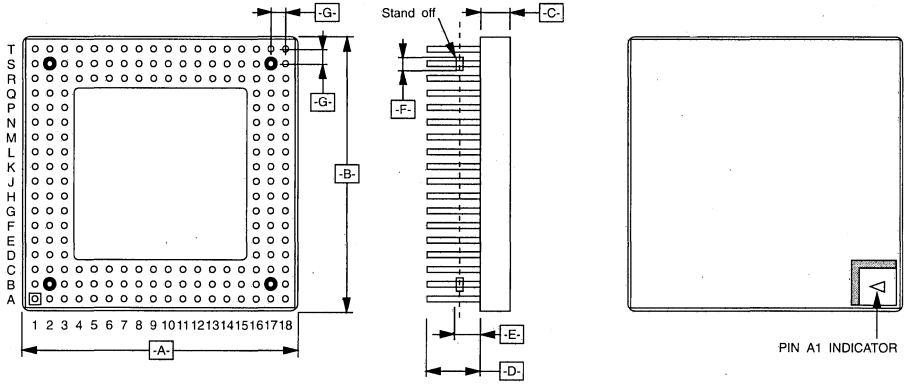
PGA 132





Dimensions in $\frac{inches}{mm}$

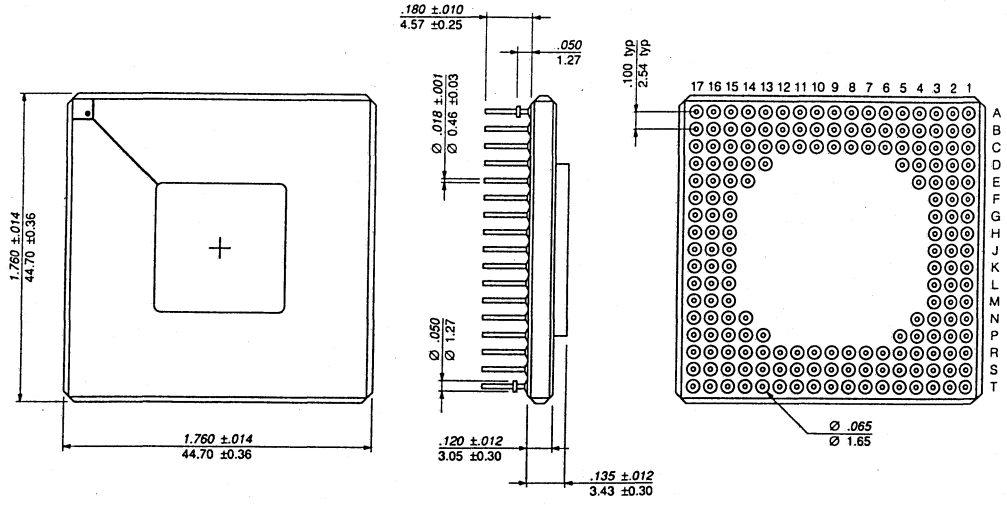
PGA 179



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	46.863	47.625	1.845	1.875
B	46.863	47.625	1.845	1.875
C	2.3876	1.875	0.094	0.116
D	4.318	4.826	0.170	0.190
E	1.143	1.4	0.045	0.055
F	1.143	1.4	0.045	0.055
G	2.54 BSC		0.100 BSC	

8

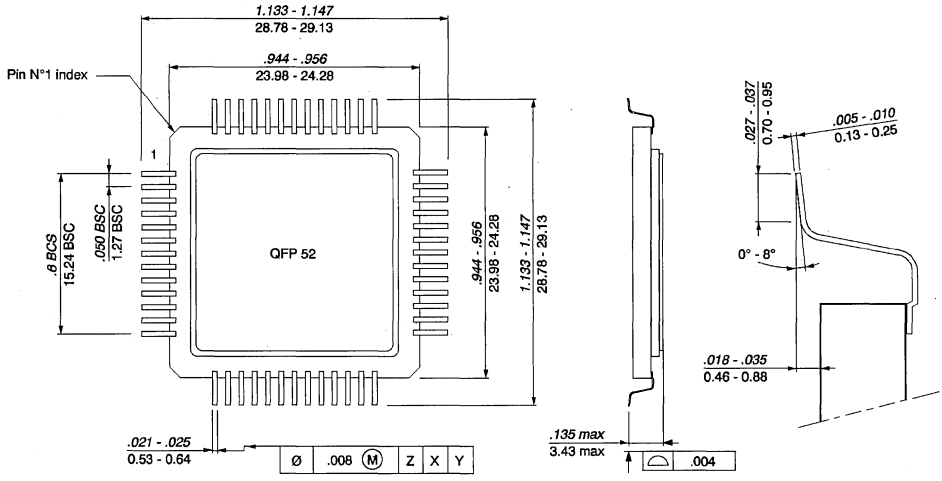
PGA 181



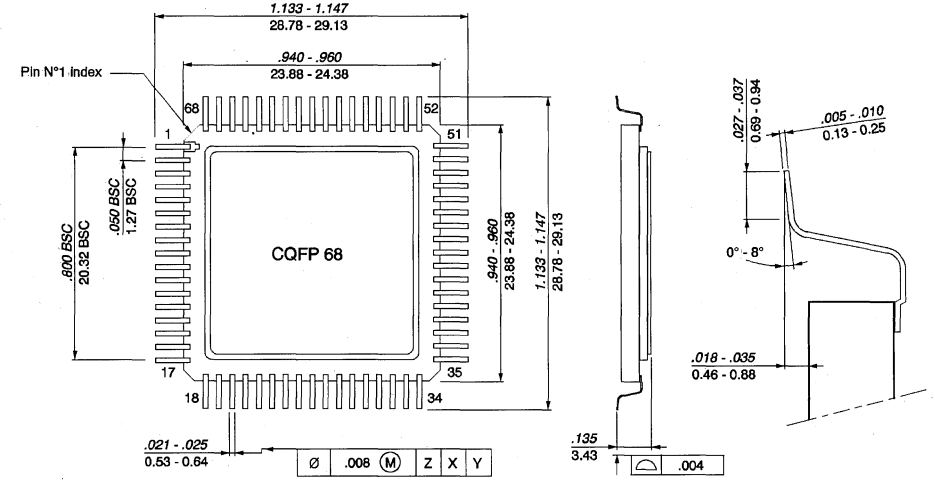
PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

CQFP 52

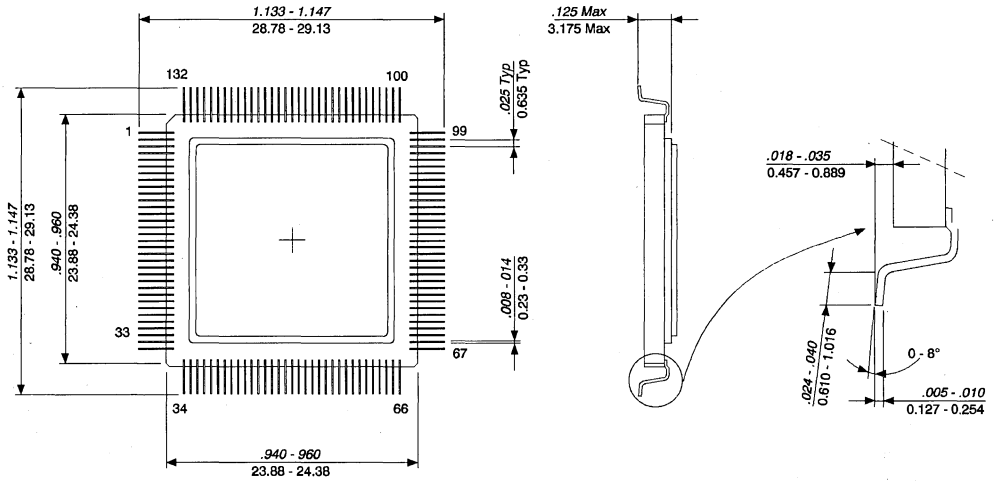


CQFP 68

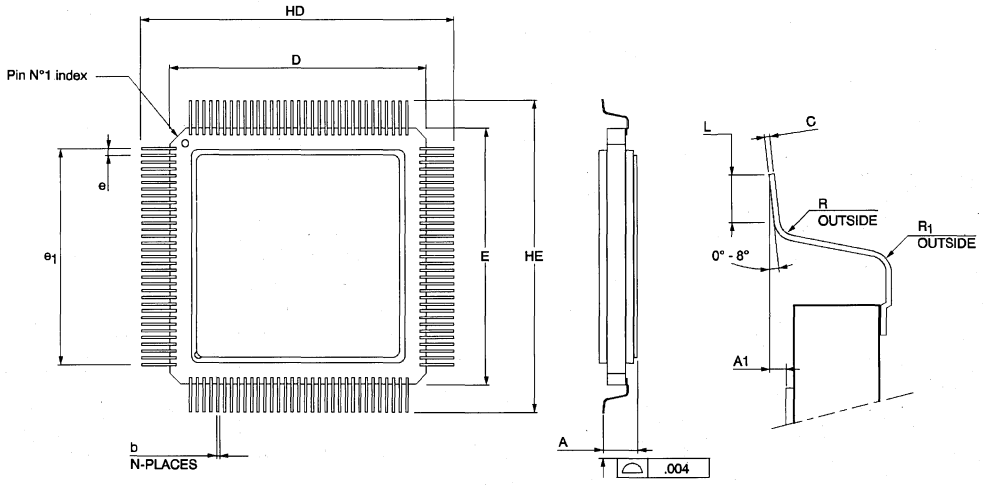


Dimensions in $\frac{inches}{mm}$

CQFP 132



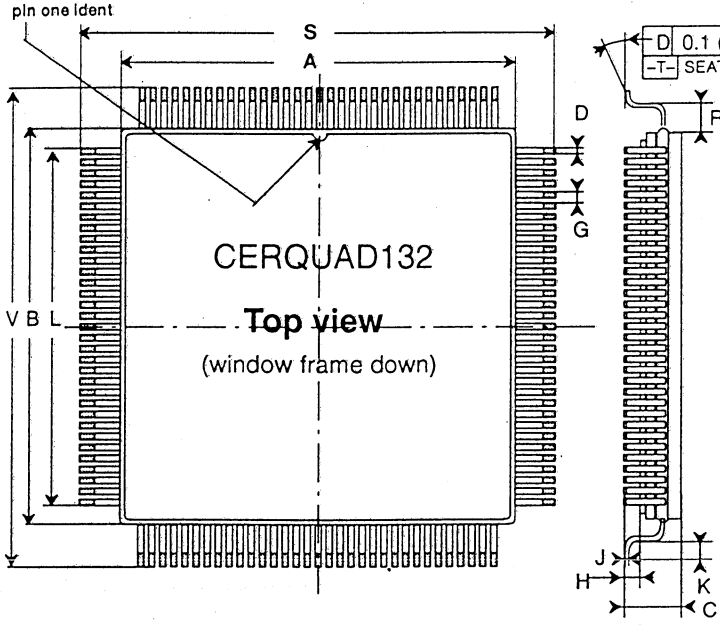
CQFP 196



PACKAGE OUTLINES

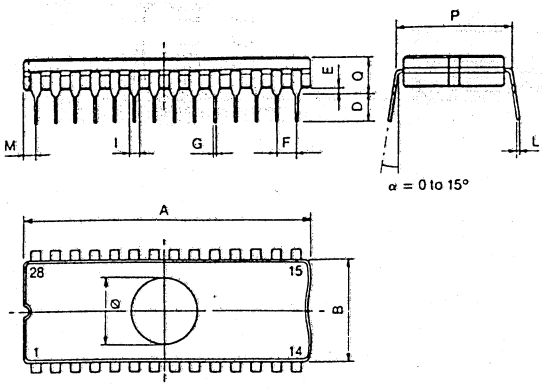
Dimensions in $\frac{inches}{mm}$

CERQUAD 132



	Milimeters		Inches	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.86	0.90
B	21.85	22.86	0.86	0.90
C	3.94	4.52	0.155	0.178
D	0.204	0.292	0.008	0.0115
G	0 64	BSC	0.025	BSC
H	0.5	1.0	0.019	0.039
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
L	20.32	REF	0.800	REF
R	0.64	–	0.025	–
S	27.26	27.6	1.073	1.087
V	27.26	27.6	1.073	1.087

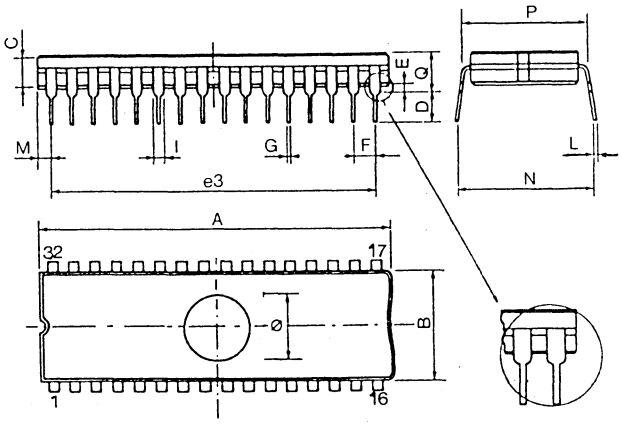
CERDIP 28



Symbol	Millimeters		
	Min	Typ	Max
A			37.85
B	12.7		15.49
D	3.81		
E	0.38		1.52
F	2.29		2.79
G	0.35		0.58
I	0.96		1.65
L	0.20		0.38
M			2.54
P	14.98		15.75
Q			5.89
⌀		7.11	

Dimensions in $\frac{inches}{mm}$

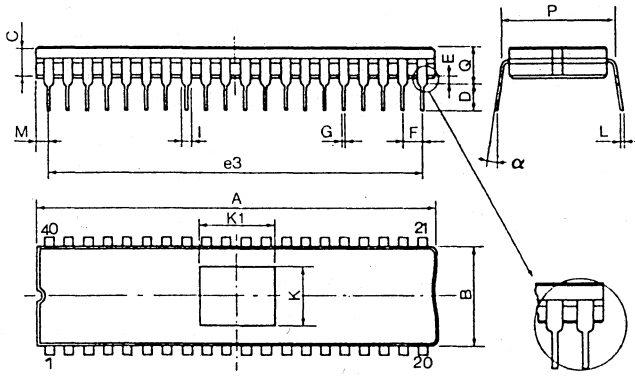
CERDIP 32



Symbol	Millimeters		
	Min	Typ	Max
A			42.78
B	14.50		14.90
C	3.55		4.70
D	3.40		5.08
E	0.50		1.78
e3		38.10	
F	2.29		2.79
G	0.40		0.55
I	1.27		1.52
L	0.22		0.31
M			2.49
N	15.62		17.78
P	15.40		15.75
Q			5.71
K	7.90		8.38
Ø		9.65	

8

CERDIP 40

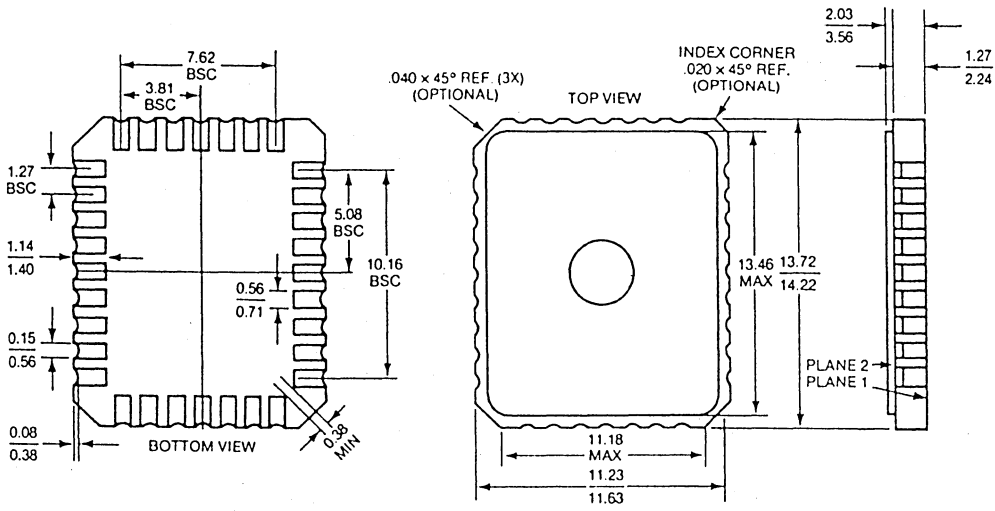


Symbol	Millimeters		
	Min	Typ	Max
A			53.24
B	12.95		15.75
C	3.90		5.08
D	3.18		5
E	0.38		1.78
e3		48.26	
F		2.54	
G	0.36		0.58
I	0.96		1.65
L	0.20		0.38
M			2.49
P	14.90		16
Q			5.71
K	7.90		8.38
K1	10.41		10.92
α	0		15°

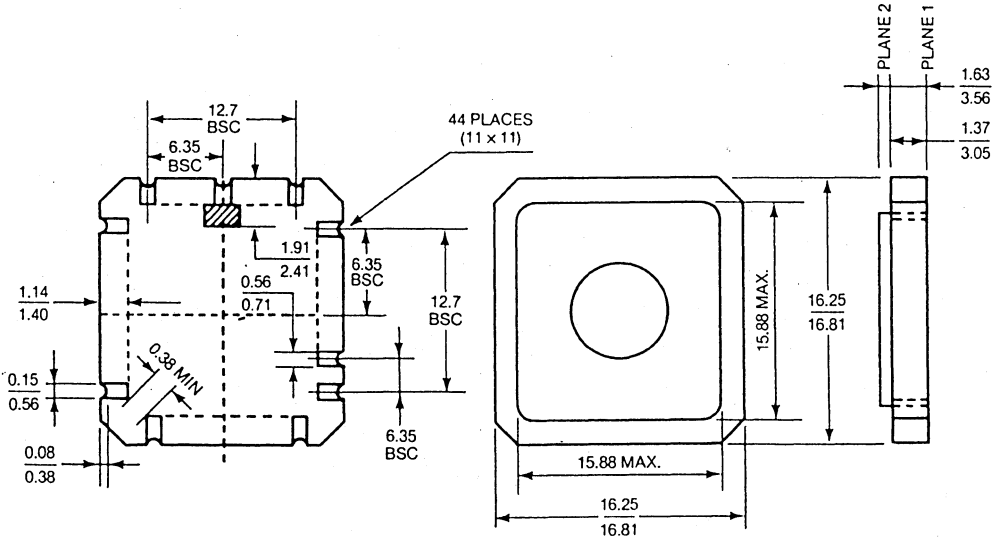
PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

LCCC 32

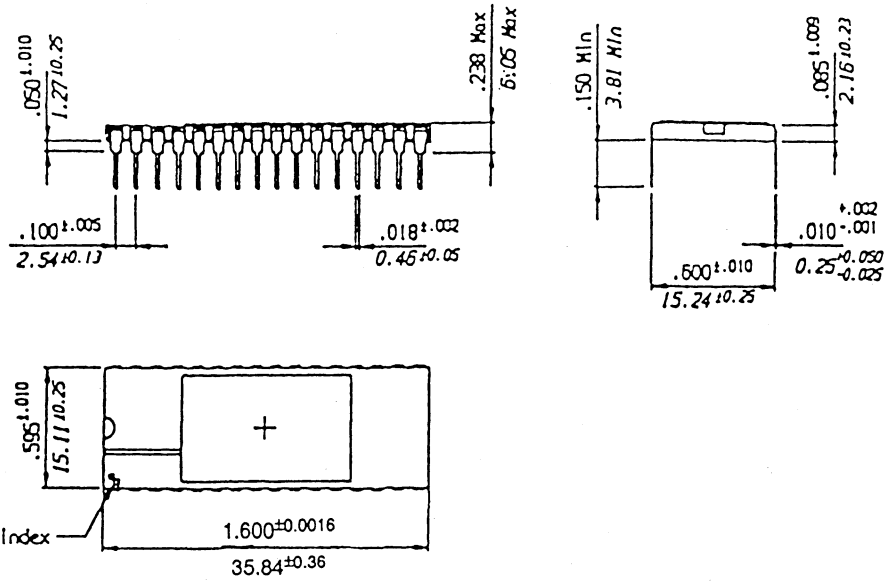


LCCC 44

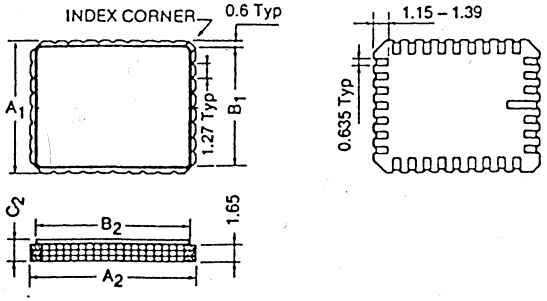


Dimensions in $\frac{inches}{mm}$

PDIP 32



PLCC 32



Symbol	Millimeters	
	Min	Max
A_1	11.23	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92

8

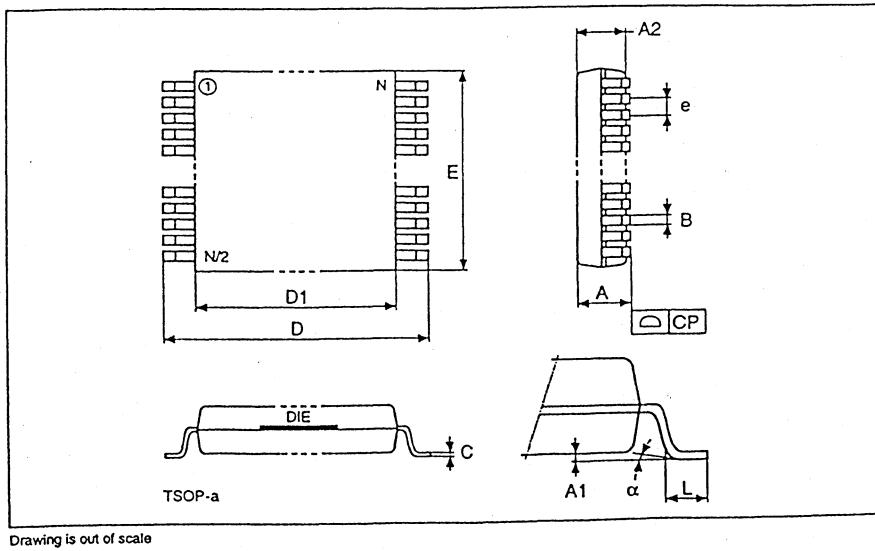
PACKAGE OUTLINES

Dimensions in $\frac{inches}{mm}$

TSOP 32

Symb	mm			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0 °C	5 °C		0 °C	5 °C
N		32			32	
CP			0.10			0.004

TSOP32



TSOP-a

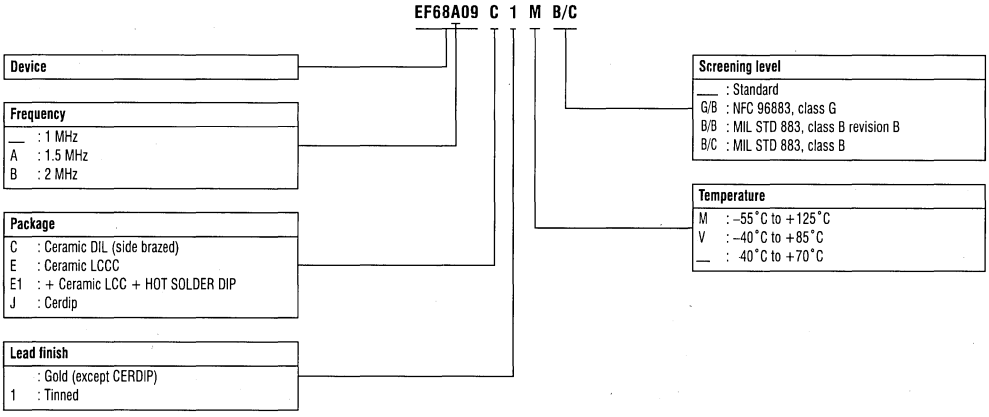
Drawing is out of scale

ORDERING INFORMATION

9

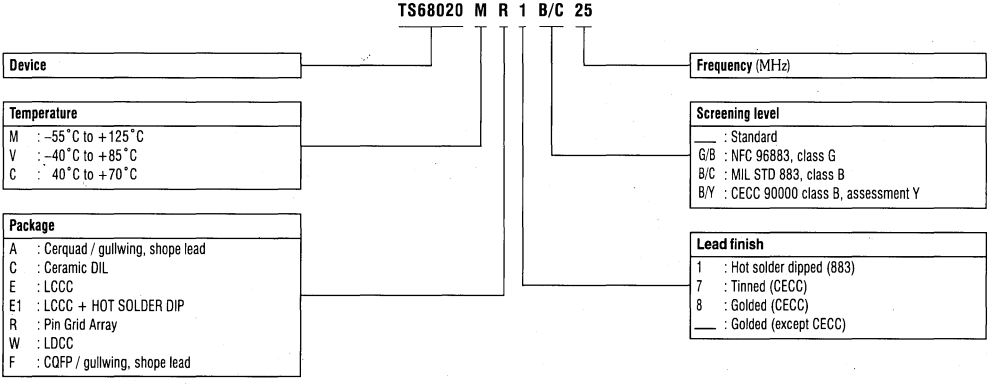
Microprocessors : 8-bits / ARINC communication processors

Internal standard - MIL STD 883



Microprocessors : 16-32-bits

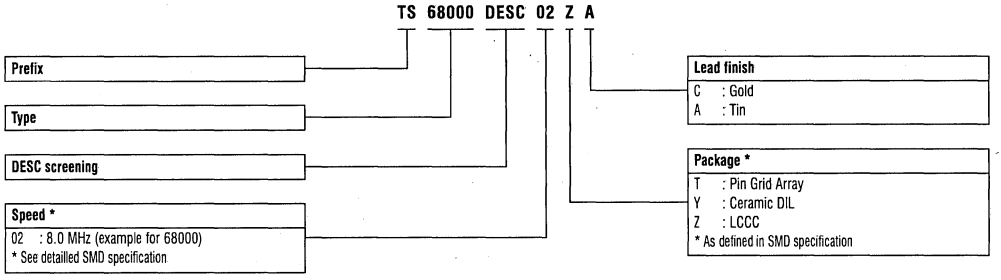
Internal standard - MIL STD 883 - CECC



ORDERING INFORMATION

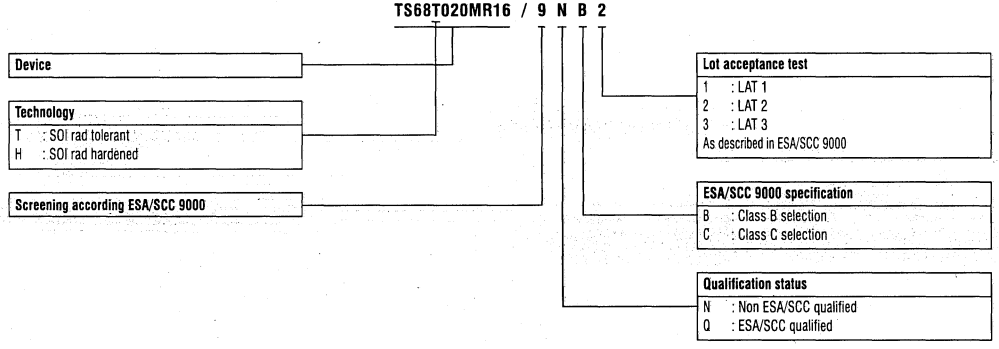
Microprocessors : 16-32-bits

DESC/SMD

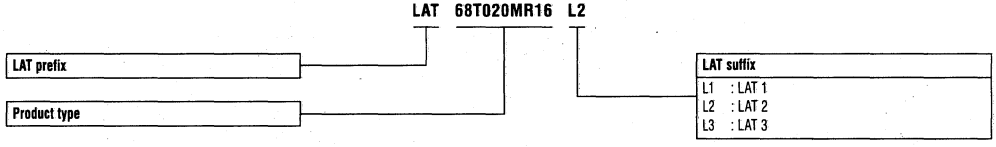


These products are double marked. (TCS part number and DESC part number).

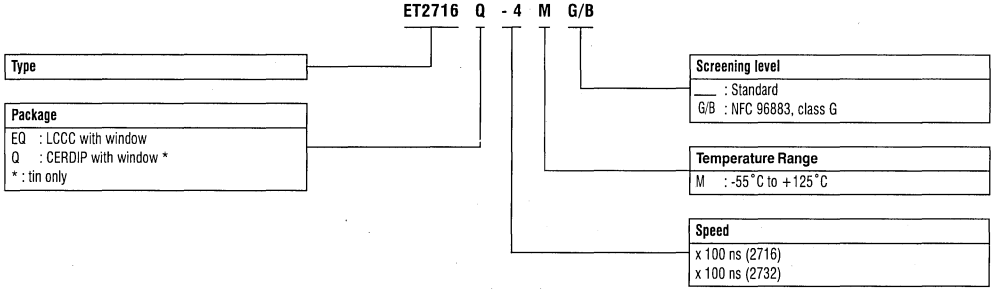
SPACE GRADE



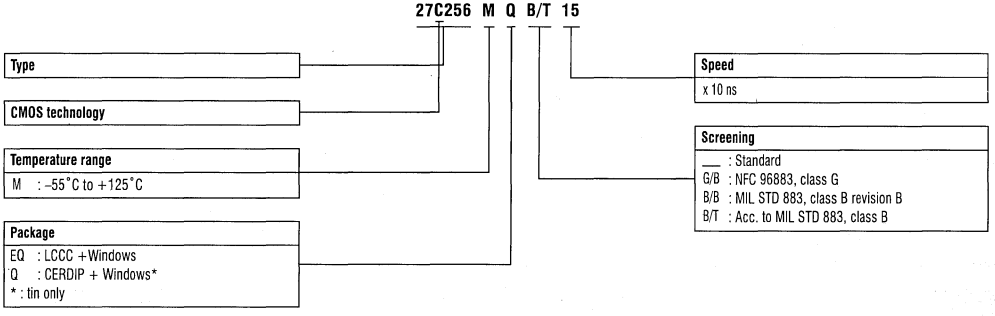
Lot acceptance test



Memories : 16 K UV EPROM'S

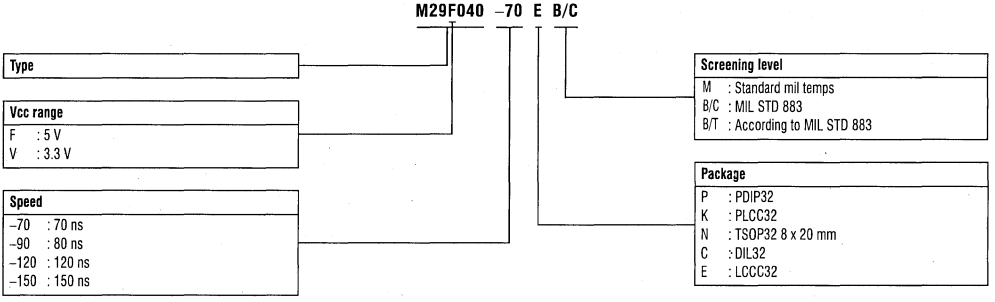


Memories : UV EPROM'S > 64 K



9

Memories : Flash EPROM'S



QUALITY ASSURANCE AND SCREENING FLOWS

10

QUALITY ASSURANCE

1 - TCS QUALITY & RELIABILITY PHILOSOPHY

Quality has been defined by the International Standardization Organization as the totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs (ISO 8402).

At this stage, the key word is «CUSTOMER».

Having recognized the central importance of the customer, another issue is raised : achieving satisfactory quality under optimum economic conditions. To achieve both customer satisfaction and cost-effectiveness, a coherent quality policy must be defined and implemented.

Thomson TCS executive management has expressed its overall quality philosophy and objectives in the Quality Manual, which is based on the ISO definition of quality and on our economic performance goals. This formal policy also encompasses quality strategy, by defining collective and individual management responsibilities, and by providing the motivational framework required to achieve the objectives.

Thomson TCS quality strategy also defines the main directions and resources which encompass the quality function in the company. A specific Quality Department exists in order to implement this strategy.

The following paragraphs offer a detailed explanation of implementation of this quality strategy and the related responsibilities throughout the organization. These responsibilities span the entire company and every task performed by the company - from senior executives to first line personnel. As such, this philosophy reflects a Total Quality approach.

2 - TCS QUALITY SYSTEM

By defining the quality management structures, responsibilities, methods and ressources needed to implement the quality strategy, the executive management has also defined a specific quality system.

The quality system is based upon the quality function principle which states that every member of TCS is responsible for the quality of his or her work.

Two other key elements of the quality system are a dedicated team - Quality Department - and a set of organized, written rules.

2.1 - Total quality

Total quality covers all the actions which lead to providing optimum answers to the requirements expressed by the customer.

In the quality manual, the description of TCS' organization also states very clearly the quality function of each department.

In addition to product quality, defined in either standards or internal specifications, service quality is one of the key items of the quality policy.

Beyond these basic principles and to establish a privileged relationship (partnership), TCS may conclude a specific agreement with a customer. This agreement lists all the quality requirements and services that the customer wishes in addition to TCS' standard quality assurance system.

This customer quality contract is based upon one ore more of the following elements :

- customer quality requirements,
- specific quality plan,
- contract quality follow-up by a quality engineer.

The main missions of TCS quality managers are :

- negociating quality clauses,
- overseeing contract review,
- contract quality follow-up.

2.2 - The Quality Department

The Quality Department is the driving force behind the above-mentioned quality functions. It therefore covers **ALL** the quality and reliability aspects of TCS, and its structure is modeled on TCS' operational mode and customer interface.

The Quality Manager reports directly to the General Manager, is a member of the Executive Committee and holds the exclusive power for conformity and qualification decisions.

2.3 - Written rules

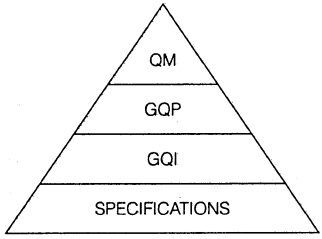
No system can work without a set of organized written rules.
The organization of these rules is hierarchical.

At the highest level, the **QUALITY MANUAL** (QM) describes the TCS mission, with a particular focus on operating mode, quality function and customer interface.

At the next level, General Quality Procedures (GQP) set out the policy and strategy which must drive the actions in a given area (Documentation, R & D, Production, Design, etc.). When too large in volume, GQP's may be split into several General Quality Instructions (GQI). This upper level system is supported by the entire set of specifications categorized by area : Quality Specification (SQ), Manufacturing Specifications (SF), Control Specification (SC), etc. These written rules are subject to exacting and traceable controls.

In order to avoid the drawbacks of a pyramid structure, cross-referenced documents may also exist such as MIL-I-38535 QAP (Quality Assurance Program), specific product or line QA plans, etc.

The documentation system may be represented as follows :



3 - CUSTOMER REQUEST AND TCS ANSWER

3.1 - Customer request

The customer's request may relate either to components listed in the TCS databook or to products specific to the customer.

In this latter case, the contractual document defining the product will be the customer's specification usually related to a databook product and subject to a specific process or add-on.

TCS offers different screenings including :

- a screening flow comparable to either level B or level C of modified ESA/SCC 9000,
- a screening based upon the generic flow of MIL-STD-883 paragraph 1.2.1 (see paragraph 3.2).

Whatever the customer's request, for space, military, or other application, the procedure is the same :

- The customer contacts the commercial network which restates the customer requirements and passes them onto the production department for analysis.

A specification review is carried out in order to :

- verify that the customer's requirements are well defined and complete,
- identify the differences between requirements and proposals, and study how to meet the customer's demands.

When an agreement is reached, a special commercial designation is created whenever the agreed specification deviates from TCS standard offering (customer specifications are dealt with by way of special designations). The order can then be validated.

3.2 - TCS standardized screening levels

TCS offers a wide range of products which are manufactured, tested and controlled either in compliance with international standards or according to internally defined standards in order to satisfy market needs.

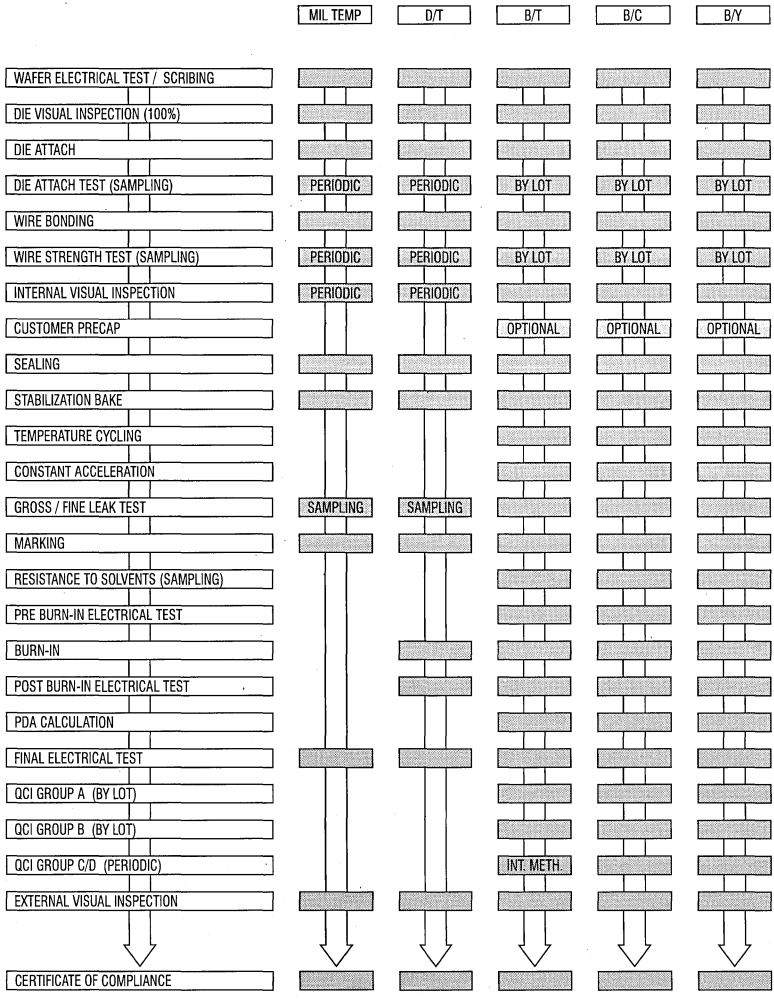
The international standards covered by TCS are :

- ESA/SCC 9000 (class B & C),
- MIL-STD-883, compliant non JAN devices (paragraph 1.2.1).

Following internal standards have been defined to conform as close as possible to widely accepted international rules :

- B/T for high reliability military applications ; B/T has a quality & reliability level comparable to MIL-STD-883 and guideline is test method 5005,
- D/T products screened with a 168 hours / 125°C burn-in,
- Standard products guaranteed to operate over the specific temperature range and covered by general QA procedures.

SCREENING-QUALITY ASSURANCE LEVEL



MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

BASIC SCREENING FLOW FOR IC's

OPERATION	SAMPLING LEVEL	APPLICABLE METHOD	CONDITIONS
Wafer electrical test	100 %	Internal	
Scribing	100 %	Internal	
Die visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Die attach	100 %	Internal	
Die attach test	Periodically, 2 parts / 0 defect	MIL STD 883, method 2019	
Wire bonding	100 %	Internal	
Wire strength test	Periodically, 4 parts / LTPD = 15	MIL STD 883, method 2011	
Internal visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Customer precap	N/A		
Sealing	100 %	Internal	
Stabilization bake	100 %	MIL STD 883, method 1008, cond. C	24 hrs, 150°C
Temperature cycling	N/A		
Constant acceleration	N/A		
Fine leak test	Lot by lot, LTPD = 7	MIL STD 883, method 1014, cond. A	5.10 E-8 to 1.10 E-7 atm.cc/s see Note
Gross leak test	Lot by lot, LTPD = 7	MIL STD 883, method 1014, cond. C	
Marking	100 %	Internal	
Resistance to solvents	N/A		
Pre burn-in electrical test	N/A		
Burn-in	N/A		160 hrs, 125°C
Post burn-in electrical test	N/A		
PDA calculation	N/A		
Final electrical test	100 %	Internal device specification	
QCI group A	N/A		
QCI group B	N/A		
QCI group C	N/A		
QCI group D	N/A		
External visual inspection	100 %	MIL STD 883, method 2009	
Packing	100 %	Internal	
Certificate of compliance	Lot by lot	Internal	
Lot history retention	Lot by lot	Internal	1 year

* Military, industrial or commercial temperature range.

N/A : Not available or not applicable.

QCI : Quality Conformance Inspection.

Note : Function of the package.

MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

D/T SCREENING FLOW FOR IC's

OPERATION	SAMPLING LEVEL	APPLICABLE METHOD	CONDITIONS
Wafer electrical test	100 %	Internal	
Scribing	100 %	Internal	
Die visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Die attach	100 %	Internal	
Die attach test	Periodically, 2 parts / 0 defect	MIL STD 883, method 2019	
Wire bonding	100 %	Internal	
Wire strength test	Periodically, 4 parts / LTPD = 15	MIL STD 883, method 2011	
Internal visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Customer precap	N/A		
Sealing	100 %	Internal	
Stabilization bake	100 %	MIL STD 883, method 1008, cond. C	24 hrs, 150°C
Temperature cycling	N/A		
Constant acceleration	N/A		
Fine leak test	Lot by lot, LTPD = 7	MIL STD 883, method 1014, cond. A	5.10 E-8 to 1.10 E-7 atm.cc/s see Note
Gross leak test	Lot by lot, LTPD = 7	MIL STD 883, method 1014, cond. C	
Marking	100 %	Internal	
Resistance to solvents	N/A		
Pre burn-in electrical test	N/A		
Burn-in	100	MIL STD 883, method 1015	160 hrs, 125°C
Post burn-in electrical test	100 %	Internal device specification.	
PDA calculation	N/A		
Final electrical test	100 %	Internal device specification	
QCI group A	N/A		
QCI group B	N/A		
QCI group C	N/A		
QCI group D	N/A		
External visual inspection	100 %	MIL STD 883, method 2009	
Packing	100 %	Internal	
Certificate of compliance	Lot by lot	Internal	
Lot history retention	Lot by lot	Internal	1 year

N/A : Not available or not applicable.

QCI : Quality Conformance Inspection.

Note : Function of the package.

MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

B/C AND B/T SCREENING FLOW FOR IC's

OPERATION	SAMPLING LEVEL	APPLICABLE METHOD	CONDITIONS
Wafer electrical test	100 %	Internal	
Scribing	100 %	Internal	
Die visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Die attach	100 %	Internal	
Die attach test	Lot by lot, 2 parts / 0 defect	MIL STD 883, method 2019	
Wire bonding	100 %	Internal	
Wire strength test	Lot by lot, 4 parts / LTPD = 15	MIL STD 883, method 2011	
Internal visual inspection	100 %	MIL STD 883, method 2010, cond. B	
Customer precap	On customer request	MIL STD 883, method 2010, cond. B	
Sealing	100 %	Internal	
Stabilization bake	100 %	MIL STD 883, method 1008, cond. C	24 hrs, 150°C
Temperature cycling	100 %	MIL STD 883, method 1010, cond. C	10 cycles, −65°C / +150°C
Constant acceleration	100 %	MIL STD 883, method 2001	30 000 g - Note 1
Fine leak test	100 %	MIL STD 883, method 1014, cond. A	5.10 E-8 to 1.10 E-7 atm.cc/s Note 2
Gross leak test	100 %	MIL STD 883, method 1014, cond. C	
Marking	100 %	MIL-M-38510, paragraph 3.6 - Note 3	
Resistance to solvents	Lot by lot, 4 parts / 0 defect	MIL STD 883, method 2015	
Pre burn-in electrical test	100 %	Internal device specification	
Burn-in	100 %	MIL STD 883, method 1015	160 hrs, 125°C
Post burn-in electrical test	100 %	Internal device specification	
PDA calculation	Lot by lot	MIL STD 883, method 5004	PDA = 5 %
Final electrical test	100 %	Internal device specification	
QCI group A	Lot by lot	MIL STD 883, method 5005 or 5010	
QCI group B	Lot by lot	MIL STD 883, method 5005 or 5010	
QCI group C	Periodically	MIL STD 883, method 5005 or 5010 Note 3	
QCI group D	Periodically	MIL STD 883, method 5005 or 5010 Note 3	
External visual inspection	100 %	MIL STD 883, method 2009	
Packing	100 %	Internal	
Certificate of compliance	Lot by lot	Internal	
Lot history retention	Lot by lot	Internal	5 years

N/A : Not available or not applicable.
QCI : Quality Conformance Inspection.
Note 1 : 20 000 g for heavy package (> 5 grams).
Note 2 : Function of the package.
Note 3 : Internal methods for B/T.

Selection classes

TCS offers 7 selection classes :

A - Electrical probe test only : consult TCS.

V - 100 % visual inspection.

N - Same as V + qualification by sampling lot with electrical testing.

T - Same as N + burn-in on the sampling lot.

W - Same as T + 1 000 hours life-test on the sampling lot.

Z - Same as W + serialization of the sampling lot + SEM (as ESA PSS 01.608 issue 2. § 3.3.4.2.2).

ZP - Double sampling lot.

For N, T, W and Z levels, a qualification lot is assembled from a sampling of dice within the lot to be delivered. This qualification lot then undergoes specific screening steps as defined in the table below.

Quality assurance and screening procedure*

PART NUMBER		QUALITY LEVEL				
		V	N	T	W	Z / ZP
Wafer probe at room temperature		●	●	●	●	●
Wafer inspection		●	●	●	●	●
SEM inspection - Scanning electron beam microscope (active only)						●
Sawing		●	●	●	●	●
1 - Die visual inspection (100 %)	Note 1	●	●	●	●	●
2 - Die visual inspection (sampling) - LTPD = 5	Note 1	●	●	●	●	●
Sampling batch (N, T, W, Z).			●	●	●	●
Assembly (38 parts standard) - Stabilization bake			●	●	●	●
Precap inspection 100 %	Note 1		●	●	●	●
Bond pull test (sampling) - IC.s : LTPD = 10	Note 2		●	●	●	●
Die shear test (sampling) - 3 parts no reject allowed	Note 3		●	●	●	●
Sealing			●	●	●	●
Serialization						●
Electrical measurement - + 25°C. T_{max}, T_{min} 1 reject allowed	Note 4		●	●	●	●
Burn-in T, W : 160 h - Z : 240 h 125°C				●	●	●
Electrical measurement + 25°C 2 rejects allowed	Note 4			●	●	●
Drift calculation						●
Life test 1 000 hours					●	●
Electrical measurement + 25°C - 1 reject allowed	Note 4				●	●
Test report			●	●	●	●
Final acceptance and certificate of compliance		●	●	●	●	●

* Done according to TCS SQ.32.S.0101 internal procedure except otherwise specified.

Note 1 : IC's / V, N, T, W : MIL TSD 883 Method 2010 Cond B ; Z : MIL STD 883 Method 2010 Cond A.

Note 2 : MIL STD 883 Method 2011.

Note 3 : MIL STD 883 Method 2019.

Note 4 : Electrical measurement N, T, W : go-no go ; Z : read and record.

● *Available.*

Qualification lot

TEST	QUALITY LEVEL	
Electrical* test at 3 temperatures	N, T, W, Z	38 pcs 1 reject allowed LTPD = 10
Electrical test after burn-in at 25°C	T, W, Z	37 pcs 2 rejects allowed
Electrical test after life test at 25°C	W, Z	35 pcs 1 reject allowed

* Done in accordance with the package product data sheet.

The packages used for the above tests are those indicated on the revelant data sheet.

Product specifications

For each die the following information is indicated in the data sheet :

- Mechanical information :
  - pad layout,
  - pad size,
  - die size,
  - die thickness,
  - metallization,
  - passivation.
- Electrical information :
  - maximum ratings,
  - electrical parameters at 25°C,
  - die back side bias if applicable.

Documentation

All die shipments from TCS are bundled with the following documentation.

Die lot : Certificate of compliance (COC).

Qualification lot (level N, T, W, Z) :
- certificate of compliance,
- test report (N, T, W),
- test data for each individual serialization part (Z).

4 - QUALITY & RELIABILITY TOOLS

Once a quality policy is defined, one of the elements of the strategy is the choice of the tools to be used.

The main principle is, of course, to enhance prevention and reduce detection. Nevertheless detection tools like quality control (QC or SQC) are still valuable tools in defined (or required as in standards) circumstances.

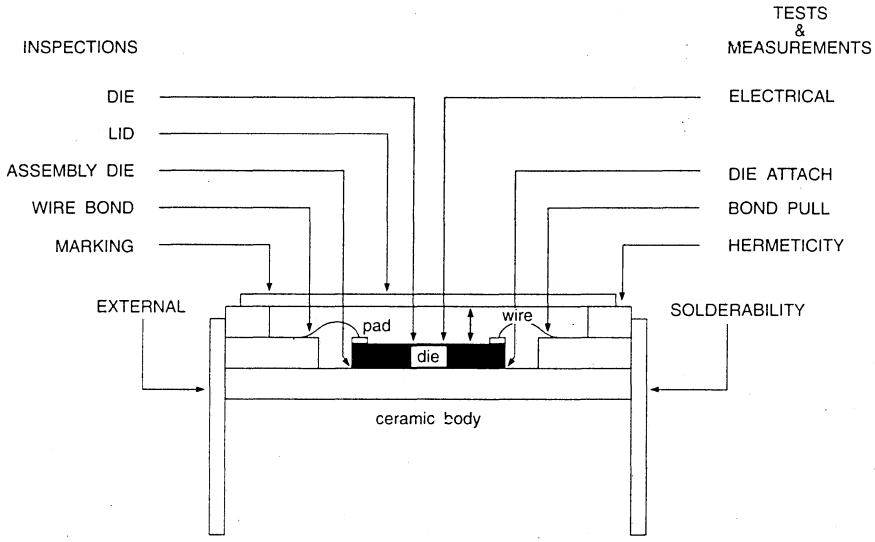
Q & R tools may be divided into three main families :

- Quality control monitoring,
- Quality assurance,
- Quality engineering.

4.1 - Q & R Control & Monitoring

Q & R Control steps are defined as mandatory steps in conjunction within the production flow, meaning that no lot may undergo a further process (or be shipped) without having successfully passed any given control.

4.1.1 - Example of quality control



4.1.2 - Reliability control

Reliability is built in by design. Nevertheless, control steps are mandatory. This means that products will undergo reliability tests (life test, environmental, mechanical, etc.) with an associated sampling plan with accept/reject criteria.

The reliability control is designated QUALIFICATION and is defined in a General Quality Procedure. The results of qualification tests may be converted into a failure rate estimation for a product or product family.

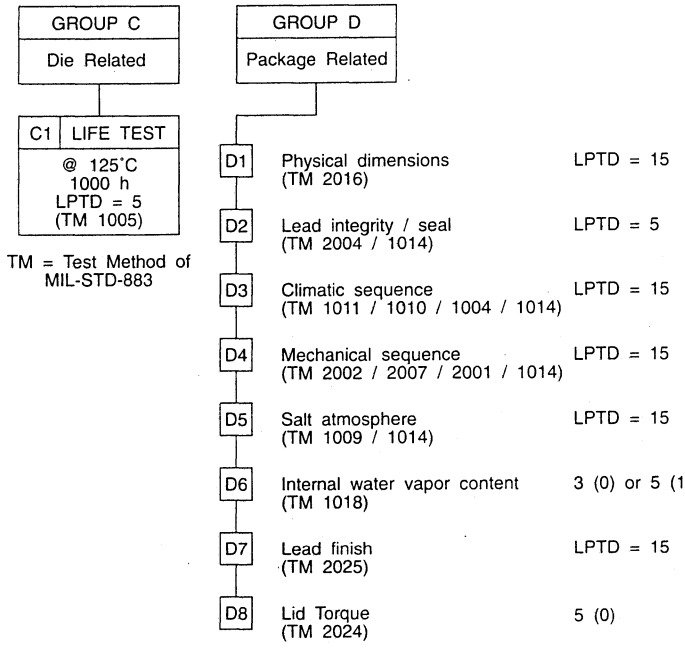
Two qualification types exist : RECURRENT and NON-RECURRENT qualification.

Non recurrent qualifications are performed in case of initial introduction, major changes, etc. In this case, specific qualification plans are issued.

After the non-recurrent qualification release, the related product, product family or technology enters a sustaining qualification phase. This means that the products will undergo periodical reliability control, hence the designation «recurrent qualification».

Recurrent qualifications are based upon MIL-STD-883, method 5005.

The basic current qualification plan is outlined in Table I.



Periodical compilations of the results obtained are used in order to determine failure rates.

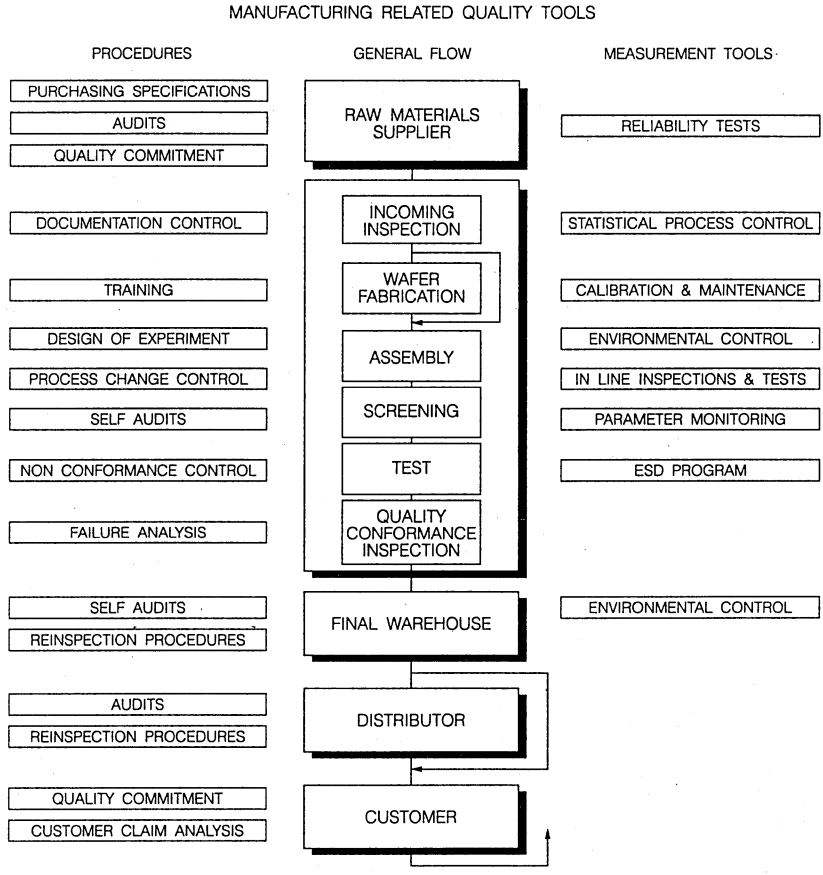
4.2 - Quality & Reliability Assurance

The word «assurance» is related to prevention methodology. Q & R assurance is grouping all the tools to avoid expensive detection. Statistical Process Control, Parameter Monitoring, Design of Experiment, Technology Validations, etc., belong to this category, as well as more «people oriented» tools such as audits, training, etc.

10

4.2.1 · Quality Assurance

Quality Assurance covers following items in the general manufacturing flow.



All the above mentioned quality tools - doc control, audits, SPC, etc. - are implemented through procedures, methods or defined actions at all levels of manufacturing.

They are grouped into five conventional families : methods, materials, machines, people, medium (environment), called the «5M cause-effect tree».

A sixth family has also been added : customer-oriented quality tools. These include customer supplies, quality contracts, customer inspections, contract reviews, field failure return program, change notification, etc.

4.2.2 · Reliability Assurance

The fundamentals of reliability assurance rely upon a twofold action : reliability construction (by design and simulation) and intrinsic reliability measurement.

During this phase, products are no longer considered as being «black-boxes», but intrinsic, real and physical failure mechanisms are traced, analyzed and modelized.

When a technology is introduced, reliability assurance is performed by a formal validation plan.

4.3 - Quality and reliability engineering

When methods, procedures and tools are used in the Q & R strategy, they belong either to Q & R control or assurance, as described in the previous paragraph.

As quality is a fast developping area, new tools periodically emerge.

Evaluating or creating new Q & R tools, deciding whether they are useful or not and implementing the chosen tools in the relevant area fall within the scope of Q & R engineering.

For example, when SPC was introduced, the applicability, training and implementation of this tool was performed by the Quality Department as part of Quality Engineering.

Once the SPC systems was implemented, it became part of the production tool and functions under quality assurance.

5 - QUALIFICATION, CERTIFICATION AND TRACEABILITY

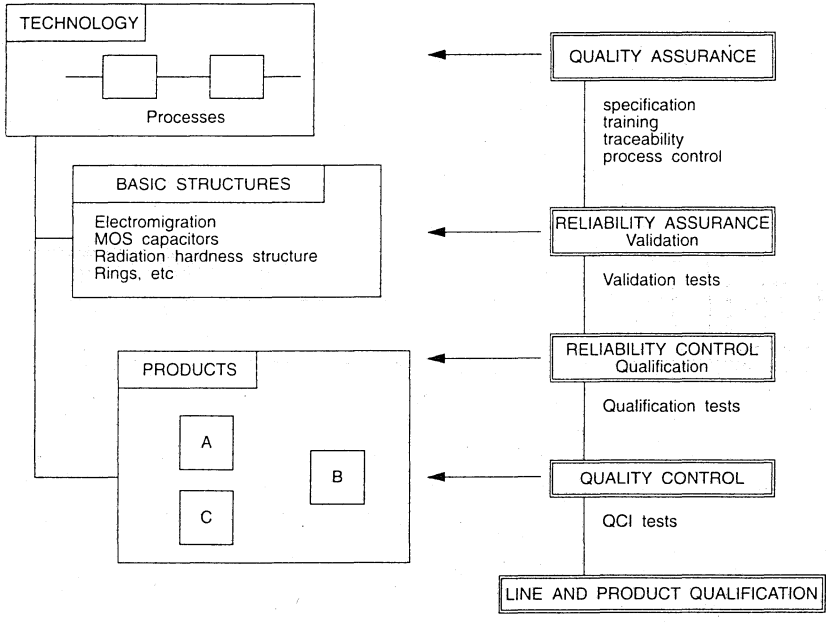
Except for prototypes, any product shipped to customers is said to be qualified and certified. The underlying issue is how a product (and/or technology, material, process) is qualified and finallly certified ?

Qualification is the internal result of the Q & R assurance & control, as explained in previous paragraphs.

When a product (material, process, technology) is introduced, it goes through a validation phase (intrinsic reliability) and a qualification phase (reliability control).

This is not sufficient to deliver the qualification. Indeed, not only must the product be subjected to Q & R assurance and control : the production tool must also be covered by these controls, starting from design and through final inspection and conditioning. In concrete terms, equipment must be calibrated and under control, personnel must be trained, all related procedures must exist and be applied, etc.

The following diagram summarizes the conditions required for qualification. The qualification ends with a formal document called Qualification Report, signed by the Reliability Manager after acceptance by the Quality Production Manager.



However this is not sufficient to ship the product to customer since the product has to be individually certified. Certification is an administrative step performed by signing of the Certificate of Compliance (COC).

The Director of Quality is the only person in TCS who is authorized to sign a COC. He may delegate this responsibility to members of the Quality Department designated by an official memo.

This raises the question of the Qualifying Activity. According to external and internal rules, the qualifying activity is the Quality Department, except for products under external surveillance and listed on official national on international QPLs.

Once the product is shipped, traceability is guaranteed. The lot travelers are stored during 1 year for standard products, 5 years for military products and 10 years for space products.

6 · TCS QUALIFICATION · CERTIFICATION RECOGNITION

- ISO 9001,
- AQAP1..,
- DESC...

The complete quality system is periodically audited either by customer on third-parties. Among these third-parties, we are proud to emphasize :

- the ISO 9001 certification (by the french administration AFAQ),
- the RAQ1 (AQAP1) certification (by the french army SIAR),
- that several MIL-STD-883 products are listed on DESC PPL,
- that several products designed in space applications are listed on CNES PPL.

MICROPROCESSORS AND MEMORIES
OBSOLETE DEVICES

11

MICROPROCESSORS

The following devices have been obsoleted.
For information : please contact your sales office.

4-bit bipolar family

PRODUCT	DESCRIPTION	OBSOLETE SINCE
TS 2901C	4-bit bipolar microprocessor slice	08/95
TS 2902A	High-speed look-ahead carry generator	08/95
TS 2909A	Microprogram sequencer	08/95
TS 2910	Microprogram controller	08/95
TS 2911A	Microprogram sequencer	08/95
TS 2914	Vectored priority interrupt controller	08/95
TS 2915A	Quad three-state bus transceiver with interface logic	08/95
TS 2918	Quad receiver with standard and three-state outputs	08/95
TS 2919	Quad register with dual three-state outputs	08/95

8-bit NMOS family

PRODUCT	DESCRIPTION	OBSOLETE SINCE
EF 6800	8-bit microprocessing unit	12/95
EF 6802	Microprocessor with clock and RAM	12/95
EF 6803	ROMless MCU	12/95
EF 6810	128 × 8-bit static RAM	12/95
EF 6852	Synchronous serial data adapter	12/95
EF 6854	Advanced data-link controller	12/95

16-bit NMOS family

PRODUCT	DESCRIPTION	OBSOLETE SINCE
TS 68008	16-bit MPU with 8-bit data bus 8 MHz	12/95
TS 68000	16-bit MPU	12/96
TS 68483	Graphic and alphanumerical controller 15 MHz	12/95

MEMORIES

PRODUCT	DESCRIPTION	OBSOLETE SINCE
ETC 2716	2 K × 8 CMOS (550 ns)	03/96
ETC 2732	4 K × 8 CMOS (550 ns)	03/96

SALES NETWORK

CONSULT TCS ON INTERNET
http://www.tcs.thomson.csf.com

Subsidiaries

FRANCE
THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES
Route départementale 128
B.P 46
91401 ORSAY Cedex
Tel. : (33) 01 69 33 00 00
Fax : (33) 01 69 33 03 21
Telex : THOM 616780 F

GERMANY
THOMSON BAUELEMENTE GmbH
Perchtinger Strasse 3
D-81319 MÜNCHEN
Tel. : (49 89) 78 79 0
Fax : (49 89) 78 79 145
Telex : 522 916 CSF D

INDIA
THOMSON TUBES ELECTRONIQUES
M 26 Commercial Complex
Greater Kailash II
NEW DELHI 110048
Tel. : (91 11) 644 78 83
Fax : (91 11) 648 26 84
Telex : 31.71.443 BCS IN

UNITED KINGDOM
THOMSON ELECTRONIC COMPONENTS Ltd
Unit 4, Cartel Business Centre
Stroudley Road
BASINGSTOKE, Hants
RG 24 OUG
Tel. : (44 1 256) 84 33 23
Fax : (44 1 256) 84 29 70
Telex : 858121 TECLUK G

USA
THOMSON COMPONENTS AND TUBES CORPORATION
40 G Commerce Way
Po Box 540
TOTOWA, NJ 07511-0540
Tel. : (1 201) 812.9000
Fax : (1 201) 812.9050
Telex : TWX (710) 9877901

Europe/Asia : representative sales offices

FINLAND
LAIKKO OY
Kolmas Linja 16 B 22
SF - 00530 HELSINKI 53
FINLAND
Tel. : 358.0.750.414
Fax : 358.0.701.73.96

ITALY
SPACEREP SRL
Via M. Gonzaga 4
20123 MILANO
ITALY
Tel. : 39.2.878.894
Fax : 39.2.864.60.219

JAPAN
DEFENSE & SPACE SEMICONDUCTOR Co., Ltd
(DASCO)
Park Grace Bldg. #303
4-32-6 Nishishinjuku
Shinjuku-Ku. TOKYO 160
Tel. : (81.3).5351.1184
Fax : (81.3) 5351.1986

SOUTH AFRICA
ALTECH INSTRUMENTS Ltd
Cnr.Brakpan & Van Dyk Roads
Boksburg, 1459
PO. Box 2097, Boksburg 1460
REPUBLIC OF SOUTH AFRICA
Tel. : 27.11.914.4525
Fax : 27.11.914.1475

SALES NETWORK

Europe/Asia : distribution sales offices

BELGIUM
MCATRONIX
Avenue des Noisetiers
Parc du Sart Tilman
B - 4900 ANGLEUR
BELGIQUE
Tel. : 32.41.67.42.08
Fax : 32.41.67.63.31

DENMARK
C-88 AS
101 Kokkedal Industripark
DK- 2980 KODDEDAL
DENMARK
Tel. : 45.42.24.48.88
Fax : 45.42.24.48.89

FRANCE
EURODIC-TCDIS
30, avenue de l'Épi d'Or
94807 VILLEJUIF Cedex
FRANCE
Tel. : (33) 01 46 87 22 24
Fax : (33) 01 46 87 04 48

GERMANY
JERMYN
Stuttgarter Str. 35
D-71083 HERRENBERG
Tel. : (49) 732.94.74.11
Fax : (49) 732.94.74.33

NORWAY
TAHONIC AS
Postboks 4554 TORSHOV
0404 OSLO
NORWAY
Tel. : 47.22.37.41.40
Fax : 47.22.37.07.20

SPAIN
UNITRONICS COMPONENTES SA
Plaza de España 18
28008 MADRID
SPAIN
Tel. : 34.1.542.52.04
Fax : 34.1.548.42.28

SWEDEN
ARROW TH's AB
Datavägen 12A
S-43632 ASKIM
SWEDEN
Tel. : 46.31.68.38.00
Fax : 46.31.68.11.15

UNITED KINGDOM
ARROW-ZEUS Ltd
Vestry Estate
Sevenoaks
Kent
TN14 SEU
UNITED KINGDOM
Tel. : 44.01732 592 869
Fax : 44.01732 592 864

EURODIS-HB ELECTRONIC
Lever Street
Bolton
Lancashire
BL3 6BJ
UNITED KINGDOM
Tel. : 44.01204 555000
Fax : 44.01204 384911

North America : representative sales offices

ALABAMA
TECHNOLOGY MARKETING ASSOC. - TMA
1019 Old Monrovia Road
Suite 100
Huntsville AL 35806
Tel. : 205.776.3057
Fax : 205.776.2413

ARIZONA
TECHNI-SOURCE Inc.
145 East chilton Drive
Suite 101
Chandler AZ 85225
Tel. : 602.497.0711
Fax : 602.497.1077

CALIFORNIA
Northern : (ZIP : 94xxx-95xxx)
BROADBAND TECHNICAL SALES
100 W. Rincon Avenue
P.O. Box 518, Suite 215
Campbell CA 95009-0518
Tel. : 408.376.0500 Main / 0538 VM
Fax : 408.376.0505

Southern : (ZIP : 90xxx-93xxx)
UNITEC SALES, Inc.
15735 Barranca Parkway
Suite J-104
Irvine CA 92718
Tel. : 714.789.7550 Main / 7552 VM
Fax : 714.789.7555

CONNECTICUT
E.C.S.I. / Shain Assoc.
423 Saw Mill Road
Guilford CT 06437
Tel. : 203.458.3666
Fax : 203.458.3670

District of Columbia
TRI-MARK, Inc.
1410 Crain Highway
Suite 4B
Glen Burnie MD 21061
Tel. : 410.761.6000
Fax : 410.761.6006

FLORIDA
Northeast
QXI Inc.
127 West Church Avenue
Longwood FL 32750
Tel. : 407.831.8131
Fax : 407.831.8112

Western
QXI Inc.
1510 - 9th Street North
St. Petersburg FL 33704
Tel. : 813.894.4556
Fax : 813.894.3989

Southern
QXI Inc.
7305 West Sample Road
Suite 207
Coral Springs FL 33065
Tel. : 954.341.1440
Fax : 954.341.1430

GEORGIA
TECHNOLOGY MARKETING Assoc. - TMA
1870 The Exchange
Suite 100
Atlanta GA 30339
Tel. : 770.928.4245
Fax : 770.928.4468

IOWA
DELTRON Co., Inc.
1930 St. Andrews NE
Cedar Rapids IA 52402
Tel. : 319.393.0075
Fax : 319.393.0058

ILLINOIS
Northern (ZIP : 600xx-611xx & 613xx)
Gassner & Clark Company
339 West River Road
Suite 307
Elgin IL 60123
Tel. : 708.695.9540
Fax : 708.695.0148

Southern (ZIP : 612xx-631xx)
DELTRON Co., Inc.
3600 Afshari Circle
Florissant MO 63034
Tel. : 314.839.0033
Fax : 314.839.4290

KANSAS
DELTRON Co., Inc.
3600 Afshari Circle
Florissant MO 63034
Tel. : 314.839.0033
Fax : 314.839.4290

MARYLAND
TRI-MARK, Inc.
1410 Crain Highway
Suite 4B
Glen Burnie MD 21061
Tel. : 410.761.6000
Fax : 410.761.6006

MASSACHUSETTS
SHAIN ASSOCIATES Inc.
45 Accord Park Drive
Norwell MA 02061
Tel. : 617.982.1474
Fax : 617.982.1503

MAINE
SHAIN ASSOCIATES Inc.
P.O. Box 748
Bethel ME04217-3021
Tel. : 207.836.3020

MICHIGAN
ELECTRONIC SOURCES Inc.
8002 W. Grand River Road
Suite B
Brighton MI 48116
Tel. : 810.227.3598
Fax : 810.227.5655

MINNESOTA
HORIZON TECHNOLOGIES
8120 Penn Avenue, #156
Bloomington MN 44531
Tel. : 612.884.6515
Fax : 612.884.3063

MISSOURI
DELTRON Co., Inc.
3600 Afshari Circle
Florissant MO 63034
Tel. : 314.839.0033
Fax : 314.839.4290

NEBRASKA
DELTRON Co., Inc.
3600 Afshari Circle
Florissant MO 63034
Tel. : 314.839.0033
Fax : 314.839.4290

NEW HAMPSHIRE
SHAIN ASSOCIATES
One Chestnut Street
Suite 302
Nashua NH 03060
Tel. : 603.881.4881
Fax : 603.881.8924

SALES NETWORK

NEW JERSEY

Northern
J-Square Marketing
P.O. Box 103
Jericho NY 11753
Tel. : 516.935.3200
Fax : 516.935.0029

NEW MEXICO

TECHNI-SOURCE Inc.
145 East chilton Drive
Suite 101
Chandler AZ 85225
Tel. : 602.497.0711
Fax : 602.497.1077

Las Cruces
TECHNI-SOURCE Inc.
5959 Gateway West
Suite 330
El Paso TX 79925
Tel. : 915.779.7810
Fax : 915.779.7811

NEVADA

Reno area
Broadband Technical Sales
100 W. Rincon Avenue
P.O. Box 518, Suite 215
Campbell CA 95009-0518
Tel. : 408.376.0500 Main 0538 VM
Fax : 408.376.0505

Las Vegas area
TECHNI-SOURCE Inc.
145 East chilton Drive
Suite 101
Chandler AZ 85225
Tel. : 602.497.0711
Fax : 602.497.1077

NEW YORK
Representatives

Upstate : (ZIP : 12xxx-14xxx)
ZIMMERMAN Sales
111 Marsh Road
Pittsford NY 14534
Tel. : 716.381.3186
Fax : 716.385.2103

Lower NY/LI : (ZIP : 10xxx-11xxx)
J-SQUARE MARKETING
P.O. Box 103
Jericho NY 11753
Tel. : 516.935.3200
Fax : 516.935.0029

NORTH CAROLINA

TECHNOLOGY MARKETING Assoc. - TMA
3125 Poplarwood Court
Raleigh NC 27604
Tel : 919.872.5104
Fax : 919.872.5086

NORTH DAKOTA

HORIZON TECHNOLOGIES
8120 Penn Avenue, #156
Bloomington MN 44531
Tel. : 612.884.6515
Fax : 612.884.3063

RHODE ISLAND

SHAIN ASSOCIATES Inc.
45 Accord Park Drive
Norwell MA 02061
Tel. : 617.982.1474
Fax : 617.982.1503

SOUTH DAKOTA

HORIZON TECHNOLOGIES
8120 Penn Avenue, #156
Bloomington MN 44531
Tel. : 612.884.6515
Fax : 612.884.3063

TENNESSEE

Knoxville, Chattanoog, Oakridge
TECHNOLOGY MARKETING Assoc. - TMA
1870 The Exchange
Suite 100
Atlanta GA 30339
Tel. : 770.928.4245
Fax : 770.928.4468

Menphis, Nashville
TECHNOLOGY MARKETING Assoc. - TMA
1019 Old Monrovia Road
Suite 100
Huntsville AL 35806
Tel. : 205.776.3057
Fax : 205.776.2413

TEXAS

Austin area
TECHNOLOGY REPRESENTATIVES Inc. - TR.I.
7801 N. Lamar
Suite D-96
Austin TX 78752
Tel. : 512.452.2110
Fax : 512.452.9184

Dallas area
TECHNOLOGY REPRESENTATIVES Inc. - TR.I.
17311 Dallas Parkway
Suite 140
Dallas TX 75248
Tel. : 214.713.9027
Fax : 214.931.6159

Houston area
TECHNOLOGY REPRESENTATIVES Inc. - TR.I.
2437 Bay Area Blvd., Box 396
P.O. Box 58960
Houston TX 77248-8960
Tel. : 713.486.7533
Fax : 713.486.7533

El Paso aera
TECHNI-SOURCE Inc.
5959 Gateway West
Suite 330
El Paso TX 79925
Tel. : 915.779.7810
Fax : 915.779.7811

WISCONSIN

Eastern
GASSNER & CLARK COMPANY
339 West River Road
Suite 307
Elgin IL 60123
Tel. : 708.695.9540
Fax : 708.695.0148

Western
HORIZON TECHNOLOGIES
8120 Penn Avenue, #156
Bloomington MN 44531
Tel. : 612.884.6515
Fax : 612.884.3063

CANADA

Montreal area
WEISS COMPANY
19100 Trans Canada Highway
Baie D'Urfe Quebec H9X 3S4
Tel. : 514.457.1177
Fax : 514.457.6950

Toronto area
WEISS COMPANY
7330 Bramalea Road
Units 6 & 7
Mississauga Ontario L5S 1N6
Tel. : 905.673.0011
Fax : 905.673.1270

Ottawa area
WEISS COMPANY
56-B Antares Drive
Nepean Ontario K2E 7V3
Tel. : 613.225.1810
Fax : 613.228.0179

Alberta
WEISS COMPANY
P.O. Box 52256
Edmonton Trail (R.P.O.)
Calgary Alberta T2E 8K9
Tel. : 403.543.3533
Fax : 403.543.3534

British Columbia
WEISS COMPANY
4381 Fraser Street
Suite 202
Vancouver B.C. V5V 4G4
Tel. : 604.873.1112
Fax : 604.873.1120

North America : distribution sales offices

FUTURE ELECTRONICS CORP.

Corporate Office
237 Hymus Blvd
Pointe Claire Quebec H9R 5C7
Tel. : 514.694.7710
Fax : 514.695.3707

Contact the Future Corporate Office for additional branch locations

CALIFORNIA branch
27489 West Agoura Road
Suite 300
Agoura Hills CA 91301
Tel. : 818.865.0040
Fax : 818.865.1340

FLORIDA branch
2200 Tall Pines Drive
Suite 108
Largo FL 34641
Tel. : 813.530.1222
Fax : 813.538.9598

MASSACHUSETTS branch
41 Main Street
Bolton MA 01740
Tel. : 508.779.3000
Fax : 508.779.3050

MICHIGAN branch
4505 Broadmorr SE
Grand Rapids MI 48150
Tel. : 313.261.5270
Fax : 313.261.8175

NEW JERSEY branch
1259 Route 46 East
Parsippany NJ 07054
Tel. : 201.299.0400
Fax : 201.299.1377

NEW YORK branch
801 Motor Parkway
Hauppauge NY 11788
Tel. : 516.234.4000
Fax : 516.234.6183

OHIO
1430 Oak Court
Suite 203
Beavercreek OH 45430
Tel. : 513.426.0090
Fax : 513.426.8490

NU HORIZONS

Corporate Office
6000 New Horizons Blvd.
Amityville NY 11701
Tel. : 516.226.6000
Fax : 516.226.6140

Contact the Nu Horizons Corporate Office for additional branch locations

NEW JERSEY branch
39 Route 46 East
Pine Brook NJ 07058
Tel. : 201.882.8300
Fax : 201.882.8398

GEORGIA branch
100 Pinnacle Way
Suite 155
Norcross GA 30071
Tel. : 770.416.8666
Fax : 770.416.9060

NO. FLORIDA branch
600 South North Lake Blvd.
Suite 270
Altamont Spring FL 22701
Tel. : 407.831.8008
Fax : 407.831.8862

SALES NETWORK

MARYLAND branch
8965 Guillford Road
Suite 160
Columbia MD 21046
Tel. : 410.995.6330
Fax : 410.995.6332

PHILADELPHIA branch
18000 Horizon Way
Suite 200
Mt. Laurel NJ 08054

ZEUS ELECTRONICS
Corporate Office
100 Midland Avenue
Port Chester NY 10573
Tel. : 914.937.7400
Fax : 914.937.2553

Contact the Zeus Corporate Office for additional branch locations

CALIFORNIA branches
6 Cromwell Street
Suite 100
Irvine CA 92718
Tel. : 714.581.4622
Fax : 714.454.4355

6276 San Ignacio Avenue
Suite E
San Jose CA 95119
Tel. : 408.629.4789
Fax : 408.629.4792

FLORIDA branch
37 Skyline Drive
Bldg. D, Suite 3101
Lake Mary FL 32746
Tel. : 407.333.3055
Fax : 407.333.9681

ILLINOIS branch
1164 Springlake Drive
Itasca IL 60143
Tel. : 708.595.9730
Fax : 708.595.9896

MASSACHUSETTS branch
25 Upton Drive
Wilmington MA 01887
Tel. : 508.658.4776
Fax : 508.694.2199

TEXAS branch
3220 Commander Drive
Carrollton TX 75006
Tel. : 214.380.4330
Fax : 214.447.2222

SALES CONDITIONS

1. General : The terms and conditions contained herein shall apply, unless otherwise duly accepted in a written agreement, to both export sales and domestic sales made by our company (hereinafter the "Vendor").

The sending of an order by the Buyer constitutes his acceptance in their entirety of the General Conditions of Sale herein contained.

Information contained within the commercial documents issued by the Vendor may be modified by the Vendor at any time and without prior notice in order to take into account technical development or economic conditions.

2. Sale Contract : The Vendor is only bound by the terms expressly written in his quotation and in the acknowledgement of order. If the Vendor has given a period of time for acceptance of his quotation, he is bound till expiration of such period of time; if he has not given any period of time, he may withdraw his quotation at any time by notice to the Buyer.

It is only after written acceptance of the Buyer's order by the Vendor in the form of an acknowledgement of order that the two parties shall be bound by the Sale Contract.

3. Price : The price is Ex-Works (Incoterms 1990), and excludes all taxes, custom duties and other charges or duties imposed by public authorities which shall be borne by the Buyer. The cost of packaging is not included and special packaging is separately invoiced.

Prices are based on current economic and financial conditions at the date of quotation; they may be adjusted at any time to take account of any fluctuation in these economic or financial conditions (for example the price of rare or precious metals).

4. Delivery :

4.1 The delivery schedule quoted by the Vendor are estimates only and take effect as from the date of Vendor's acknowledgement of order. Unless otherwise agreed in writing by the Vendor, failure to deliver within the time quoted shall entail neither cancellation of the order nor any compensation.

4.2 Unless otherwise agreed by reference to other Incoterms (1990) delivery shall be deemed to be made Ex-Works in the Vendor's factory or warehouse as per Incoterms 1990. Delivery shall be made by taking over of the Products at the Vendor's factory or warehouse either by the Buyer or by a shipper or carrier appointed by the Buyer, or in the absence of such an appointment, chosen by the Vendor.

5. Force majeure : Any event of force majeure shall have the effect of suspending performance of Vendor's obligations until such event has ceased. For the purposes of these Conditions of Sale, force majeure is defined as any event, foreseeable or not, which the effects could not be reasonably prevented by the Vendor and which are of such a nature as to prevent the performance of its obligations. The following events, among others, are considered as cases of force majeure : fire, flood, stoppage or delay of transportation, failure of supplier or subcontractor, strikes of any nature, machine breaking...

6. Transport, Insurance : Carriage of the Products shall be at the Buyer's own risk. It is for the latter to check them on arrival and, if necessary, to notify any damage to the carriers. On receipt of special instructions from the Buyer, shipments may be insured by the Vendor, who will then correspondingly invoice for the additional insurance costs.

7. Conditions of acceptance of deliveries by the Buyer :

7.1 The characteristics of the Products shall be defined as those published in the most recent version of the Vendor's specifications, unless different characteristics are expressly agreed between the Vendor and the Buyer.

7.2 Any complaints regarding the non conformity of the Products supplied to the above mentioned specifications must, in order to be admitted and to allow the provisions contained in this paragraph and in 7.3 below to be carried out, be made within one month after the date of delivery.

Upon receipt of a complaint, the Vendor shall then have one month to notify the Buyer if he requires an expertise to arrive at a conclusion.

No complaint shall be admissible once the Products have undergone modifications or deterioration caused by the Buyer or anyone else, especially during storage, inspection, installation, dismounting, etc.

7.3 Whereasoever the validity of the Buyer's complaints is established or recognised as such by the Vendor, the latter undertakes to accept the return, at his charge and at his option, either of the whole of the faulty delivery or the individual defective Products, nevertheless provided that each defective Product is accompanied by the corresponding test report and that the returns are made in their original packaging and in good condition.

7.4 No return may be made without the prior written consent of the Vendor.

7.5 Where a return is accepted, the Vendor will, at his option, either replace, repair or issue a credit for the Products admitted by him to be defective, to the exclusion of any other form of compensation. In any case, the Buyer cannot claim that such a return allows him to cease any payment whatsoever which he owes to the Vendor nor cancel, in whole or in part, any order whatsoever which is in the course of being fulfilled.

7.6 The provisions of paragraphs 7.2 to 7.5 do not apply to goods supplied having undergone acceptance in the Vendor's factory or having satisfied the rules of the relevant Quality Assurance Procedure (the French C.C.Q. system or the European C.E.C.C. system as the case may be) and which are consequently deemed to conform to the specifications.

8. Conditions of payment : Payment shall be made to the Vendor for Products supplied within 30 days from the date of invoicing in accordance with the conditions laid down by the Vendor in the quotation or at the time of the acknowledgement of order. Invoicing shall be made once the Products ordered have been delivered.

Failure to pay an invoice shall permit the Vendor, without prejudice to any other rights he may have, to suspend any delivery, whatever be the conditions of the relevant order, until full payment. The Vendor shall be also entitled to charge, ipso jure and without prior notice, interest at a rate equal to 1.5 times the French yearly official rate ("taux d'intérêt légal") in force for the full duration of the payment delay.

No discount rate is applicable in case of anticipated payment.

9. Reservation of title : Property in the Products shall remain in the Vendor until he has received the corresponding full payment, notwithstanding delivery to the Buyer. Upon the Buyer's failure to make payment by any due date, the Vendor may retake possession of the Products delivered.

Notwithstanding the above, the buyer will be responsible for all damages and losses arising after delivery.

10. Guarantee : Vendor guarantees that the Products shall have, for one year from the date of delivery, the characteristics as defined in paragraph7.1 above. This guarantee shall not apply:

- if the Products have been damaged in transit or have not been stored by the Buyer in accordance with the specifications;

or,

- if the Products have been submitted to abnormal conditions (mechanical, electrical or thermal) during installation or use;

or,

- if the defectiveness of the Products has resulted from exceeding the maximum values for usage (temperature limit, maximum voltage, etc...) defined by Vendor, from an incorrect choice of application or from a design made by the Buyer.

Vendor's guarantee is limited, at the Vendor's option, to either the replacement or the repair of the Product accepted by him as being defective to the exclusion of any other form of compensation. In no event shall Vendor be liable for any damages, direct or indirect, arising out of or in connection with the use, performance or failure of a Product supplied by the Vendor, whether or not the Vendor has been advised of the possibility of occurence of such damages.

Notwithstanding the foregoing, Vendor gives no guarantee whatsoever with regard to experimental, developmental or non-qualified Products.

The foregoing constitutes the whole and sole guarantee given by the Vendor and shall be in lieu of any other guarantee; in particular, the Vendor does not warrant the suitability or fitness of the Products for a particular purpose, nor that the functions of the Products may be used in any application or combination which the Buyer may choose.

11. Industrial property rights : Sale of Products does not confer to Buyer any license or other rights under any patent, statutory rights or know how attached to the said Products.

Because of the complexity of design and manufacturing techniques for electronic components and of the industrial property rights appertaining thereto, the Vendor is not able to declare that his Products do not infringe the industrial property rights of any third party. In case that a third party shall make a claim alleging that the Products delivered to the Buyer infringe his industrial property rights, the Vendor undertakes at his option and his charge, to defend the claim or to effect a compromise; if an unfavourable definitive judgement is given against the Vendor, the latter shall, at his option, take out a licence from the above mentioned third party or shall modify the offending Products in such a way as to avoid the infringement or, if such a solution shall be impracticable for economic and/or technical reasons, shall accept the return of the Products supplied and shall reimburse the Buyer at the buying price.

The above undertaking shall only apply if the Buyer immediately informs the Vendor in writing of any infringement claim concerning the Product supplied by the Vendor.

The responsibility of the Vendor is expressly excluded if the infringement results from the combination of the Products supplied with any other product, from a modification made other than by the Vendor, or results from technical drawings, designs, formulae, specifications or instructions supplied by the Buyer; in such cases, Buyer shall hold Vendor harmless against and shall indemnify Vendor from any financial consequences whatsoever Vendor may incur as a result of any action or claim for infringement made by a third party.

Furthermore, the Vendor shall not be held responsible for any costs or expense incurred by the Buyer without his authorisation nor for damages, direct or indirect, which may result from any loss of use whatsoever of the Products supplied, whether or not Vendor has been advised of the possibility of occurence of such damages.

The above provisions constitute the entire undertaking of the Vendor towards the Buyer in the event of industrial property rights claims of a third party with regard to the Products supplied by Vendor.

12. Jurisdiction and applicable Law : In case of dispute, and in the absence of an amicable settlement, the only competent jurisdiction shall be that of the Tribunal de Commerce de Paris (France), whatever be the conditions of sale and method of payment which have been accepted, even in the case of claim of third parties or in case of multiple defendants.

The applicable law shall be the French law.

13. Export Control : With regard to the Products, the Buyer undertakes to comply with all applicable laws and regulations concerning the Control of Final DesTination.

NOTES

Cover design : GAYAL
Layout and typesetting : GRAPHIC EXPRESS
Printed in France : July 1996

These products are manufactured by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - 38521 SAINT-EGREVE / FRANCE.

For further information please contact : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - Route Départementale 128 - B.P. 46 - 91401 ORSAY Cedex / FRANCE - Tél. : (33) 01 69 33 00 00 / Téléfax : (33) 01 69 33 03 21.

THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

Route départementale 128 - B.P. 46 - 91401 ORSAY Cedex / France
Tél. : +33 - 01 69 33 00 00 - Fax : +33 - 01 69 33 03 21 - Télex : 616780 F

Design : Pilote image • Illustration Gayal 3D • DB Micro/Memories - 07.96