

TMS320C1x DIGITAL SIGNAL PROCESSOR Programmer's Reference Card



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Instruction Symbols

Symbol	Meaning
AR	Auxiliary register
ARP	Auxiliary register pointer
B	Bit code
BR	Branch address
D	Data memory address or indirect addressing control bits (see below)
dma	Data memory address
I	Indirect/direct addressing mode 1 = indirect; 0 = direct addressing
ind	Indirect address: {'+'+'-'}
K	Immediate value
PA	Port address
pma	Program memory address
S	Shift count
< >	User-defined items
[]	Optional items

Indirect Addressing Control Bits

6	5	4	3	2	1	0
0	INC	DEC	NAR	0	0	ARP

INC Increment flag; 1 increments auxiliary register
 DEC Decrement flag; 1 decrements auxiliary register (INC and DEC cannot both be 1's)
 NAR New auxiliary register control bit; 0 loads bit0 as new ARP
 ARP If NAR = 0, ARP contains new ARP value.

Instruction Format Description

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	OPCODE																
2	OPCODE										1	D					
	BRANCH ADDRESS																
3	OPCODE										I	D					
4	OPCODE					SHIFT					I	D					
5	OPCODE										R	I	D				
6	OPCODE					PA					I	D					
7	OPCODE					SACH/L					I	D					
8	1	0	0														K
9	OPCODE										K						
10	OPCODE					AR					K						
11	OPCODE															K	

Status Register Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OV	OVM	INTM	1	1	1	1	ARP	1	1	1	1	1	0	DP	

OV Accumulator overflow flag bit
 OVM Overflow mode bit
 INTM Interrupt mask bit
 ARP Auxiliary register pointer
 DP Data memory page pointer

Instruction Set Summary

Instr	Description	Cyc/Wd	Operand Options	Opcode	Format
ABS	Absolute value of accumulator	1/1	None	7F88h	1
ADD	Add to accumulator with shift	1/1	<dma>[,<shift>] <ind>[,<shift>[,<next ARP>]]	0000h	4
ADDH	Add to high accumulator	1/1	<dma>; <ind>[,<next ARP>]	6000h	3
ADDS	Add to low accumulator with no sign extension	1/1	<dma> <ind>[,<next ARP>]	6100h	3
AND	AND with accumulator	1/1	<dma>; <ind>[,<next ARP>]	7900h	3
APAC	Add P register to accumulator	1/1	None	7F8Fh	1
B	Branch unconditionally	2/2	<pma>	F900h	2
BANZ	Branch on auxiliary register not 0	2/2	<pma>	F400h	2
BGEZ	Branch if accumulator \geq 0	2/2	<pma>	FD00h	2
BGZ	Branch if accumulator $>$ 0	2/2	<pma>	FC00h	2
BIOZ	Branch on I/O status = 0	2/2	<pma>	F600h	2
BLEZ	Branch if accumulator \leq 0	2/2	<pma>	FB00h	2
BLZ	Branch if accumulator $<$ 0	2/2	<pma>	FA00h	2
BNZ	Branch if accumulator \neq 0	2/2	<pma>	FE00h	2
BV	Branch on overflow	2/2	<pma>	F500h	2
BZ	Branch if accumulator = 0	2/2	<pma>	FF00h	2
CALA	Call subroutine indirect	2/1	None	7F8Ch	1
CALL	Call subroutine	2/2	<pma>	F800h	2
DINT	Disable interrupt	1/1	None	7F81h	1
DMOV	Data move in data memory	1/1	<dma>; <ind>[,<next ARP>]	6900h	3

Instruction Set Summary (Concluded)

Instr	Description	Cyc/Wd	Operand Options	Opcode	Format
EINT	Enable interrupt	1/1	None	7F82h	1
IN	Input data from port	2/1	<dma>, <PA> <ind>, <PA> [, <next ARP>]	4000h	6
LAC	Load accumulator with shift	1/1	<dma> [, <shift>] <ind> [, <shift> [, <next ARP>]]	2000h	4
LACK	Load accumulator immediate	1/1	<constant>	7E00h	9
LAR	Load auxiliary register	1/1	<AR>, <dma> <AR>, <ind> [, <next ARP>]	3800h	5
LARK	Load auxiliary register immediate	1/1	<AR>, <constant>	7000h	10
LARP	Load auxiliary register pointer	1/1	<constant>	6880h	11
LDP	Load data memory page pointer	1/1	<dma> <ind> [, <next ARP>]	6F00h	3
LDPK	Load data memory page pointer immediate	1/1	<constant>	6E00h	11
LST	Load status register	1/1	<dma> <ind> [, <next ARP>]	7B00h	3
LT	Load T register	1/1	<dma> <ind> [, <next ARP>]	6A00h	3
LTA	Load T register and accumulate previous product	1/1	<dma> <ind> [, <next ARP>]	6C00h	3
LTD	Load T register, accumulate previous product, move data	1/1	<dma> <ind> [, <next ARP>]	6B00h	3
MAR	Modify auxiliary register	1/1	<dma> <ind> [, <next ARP>]	6800h	3
MPY	Multiply (with T register, store product in P register)	1/1	<dma> <ind> [, <next ARP>]	6D00h	3
MPYK	Multiply immediate	1/1	<constant>	8000h	8
NOP	No operation	1/1	None	7F80h	1
OR	OR with accumulator	1/1	<dma> <ind> [, <next ARP>]	7A00h	3
OUT	Output data to port	2/1	<dma>, <PA> <ind>, <PA> [, <next ARP>]	4800h	6
PAC	Load accumulator with P register	1/1	None	7F8Eh	1
POP	Pop top of stack to low accumulator	2/1	None	7F9Dh	1
PUSH	Push low accumulator onto stack	2/1	None	7F9Ch	1
RET	Return from subroutine	2/1	None	7F8Dh	1
ROVM	Reset overflow mode	1/1	None	7F8Ah	1
SACH	Store high accumulator with shift	1/1	<dma> [, <shift>] <ind> [, <shift> [, <next ARP>]]	5800h	7
SACL	Store low accumulator	1/1	<dma> <ind> [, <0> [, <next ARP>]]	5000h	3
SAR	Store auxiliary register	1/1	<AR>, <dma> <AR>, <ind> [, <next ARP>]	3600h	5
SOVM	Set overflow mode	1/1	None	7F8Bh	1
SPAC	Subtract P register from accumulator	1/1	None	7F90h	1
SST	Store status register	1/1	<dma>; <ind> [, <next ARP>]	7C00h	3
SUB	Subtract from accumulator with shift	1/1	<dma> [, <shift>] <ind> [, <shift> [, <next ARP>]]	1000h	4
SUBC	Conditional subtract	1/1	<dma>; <ind> [, <next ARP>]	6400h	3
SUBH	Subtract from high accumulator	1/1	<dma>; <ind> [, <next ARP>]	6200h	3
SUBS	Subtract from low accumulator with no sign extension	1/1	<dma> <ind> [, <next ARP>]	6300h	3
TBLR	Table read	3/1	<dma>; <ind> [, <next ARP>]	6700h	3
TBLW	Table write	3/1	<dma>; <ind> [, <next ARP>]	7D00h	3
XOR	Exclusive-OR with accumulator	1/1	<dma>; <ind> [, <next ARP>]	7800h	3
ZAC	Zero accumulator	1/1	None	7F89h	1
ZALH	Zero low accumulator and load high accumulator	1/1	<dma> <ind> [, <next ARP>]	6500h	3
ZALS	Zero accumulator, load low accumulator with no sign extension	1/1	<dma> <ind> [, <next ARP>]	6600h	3