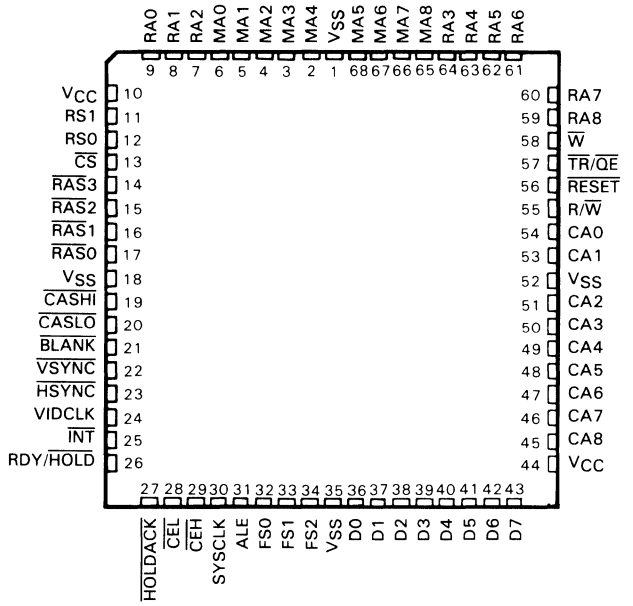
TMS34061
VIDEO SYSTEM CONTROLLER

FEBRUARY 1985 – REVISED JANUARY 1986

- **Generates User-Programmable Control Signals (Horizontal Sync, Vertical Sync, and Blanking) Which Support a Broad Range of Raster-Scan Display Systems with Varying Resolutions and Scan Rates**
- **Provides Memory Refresh at User Programmable Rates**
- **When Combined with the TMS4161 VRAM, Memory Availability to the Host is Virtually Unlimited, Since Display Access and Dynamic RAM Refresh Require Less than Six Percent of the Memory Bandwidth**
- **Directly Drives up to 64 TMS4161 VRAMs or Conventional DRAM Memories with No External Buffering**
- **Synchronizes to an External Video Source, Which Allows Superimposing of an Image upon an Externally Generated Source**
- **Independent Video and System Clocks Allow the Video System and the Host Processor to Run Asynchronously**
- **Supports Both Interlaced and Noninterlaced Displays**
- **Interfaces Easily to a Wide Variety of Microprocessors (8, 16, 20, and 32-Bit Data Bus Widths)**
- **Can Be Configured to Support Dot Rates from 5 MHz up to 130 MHz, When Used in Conjunction with the TMS4161**

FN PACKAGE
(TOP VIEW)



- **X-Y Mode Supports Processors with Limited Addressing Range and More Efficient Drawing Algorithms**
- **21 Address Bits Directly Access a 2 Megaword Address Space with Arbitrary Word Width**
- **10 MHz Clock Rate**

description

The high-performance Video System Controller (VSC) has been developed to control the video display and main memory subsystems of a bit-mapped graphics system. A monolithic NMOS device, the VSC controls the TMS4161 Multiport Video RAM (VRAM) and 256K Multiport Video RAM, as well as the conventional 64K and 256K dynamic RAMs.

Most delays caused by conflicts with display update functions are eliminated by the VSC. The host is relieved of system memory control, the video memory refresh, and VRAM internal shift register reload for bit-mapped displays.

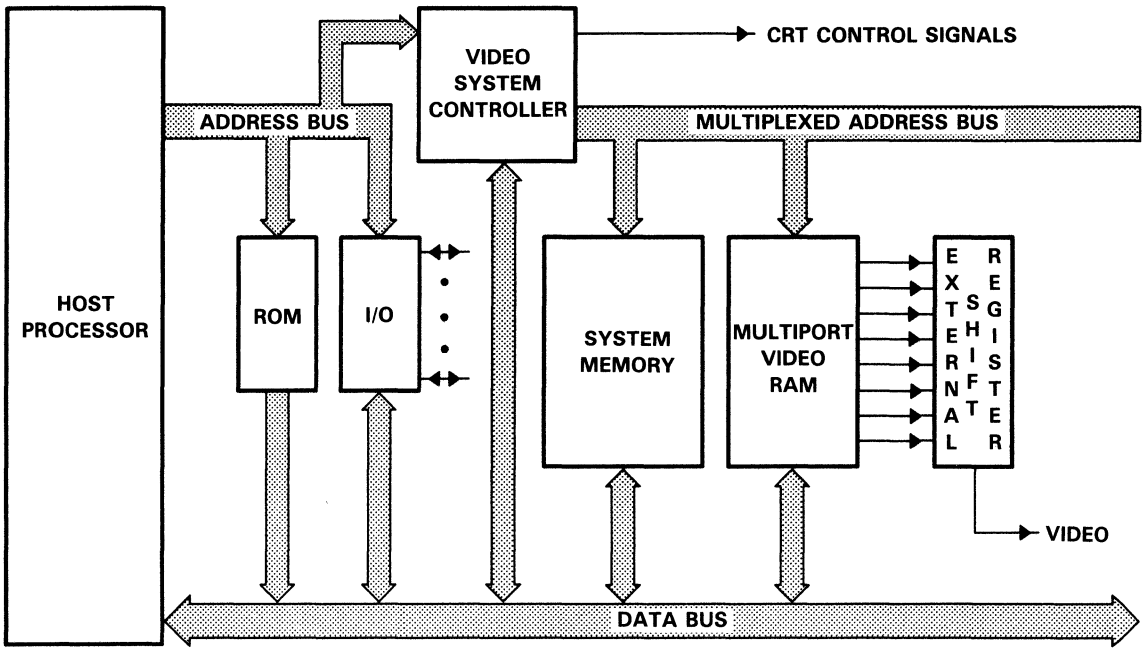
Highly programmable, the VSC supports a broad range of raster-scan display systems with various resolutions and scan rates.

The VSC performs four major functions:

1) Allows the host virtually unimpeded access to VRAMs, directly (host direct) or indirectly (X-Y)
2) Automatically generates the DRAM-refresh cycles needed to maintain data stored within the DRAMs
3) Performs display-update cycles needed to periodically load new video data into the VRAM shift registers
4) Generates sync and blanking signals necessary for monitor control.

All VSC inputs and outputs are TTL compatible. The VSC is guaranteed for operation from 0°C to 70°C.

typical system block diagram



functional block diagram

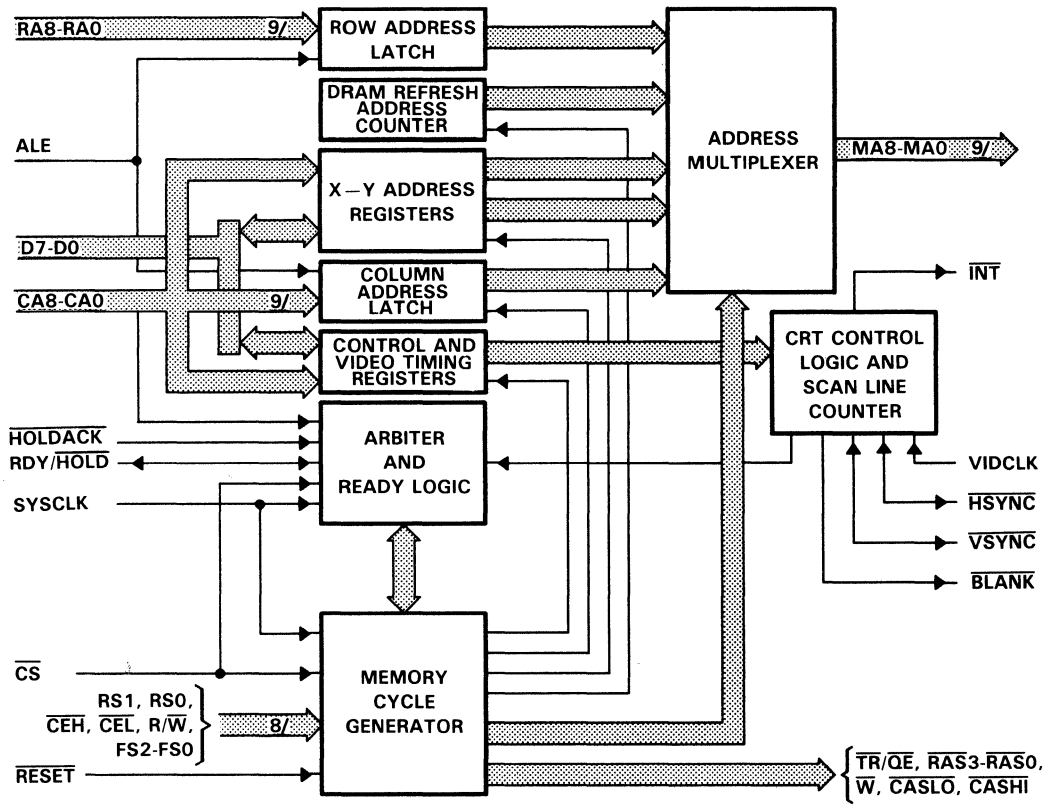


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TABLE 1. PIN DESCRIPTIONS

NAME	PIN	I/O	DESCRIPTION
MA8-MA0	65-68, 2-6	O	Memory Address. These memory address outputs are multiplexed address lines designed to interface directly to TMS4161 VRAMs, as well as conventional DRAMs. MA0 is the LSB.
RA8-RA0	59-64, 7-9	I	Row Address. These address inputs are multiplexed to memory address pins MA8-MA0 during row address time when a host-initiated memory access cycle is executed. For host-initiated shift register-transfer cycles, these inputs are multiplexed to MA8-MA0 during column address time. RA0 is the LSB.
CA8-CA0	45-51, 53,54	I	Column Address. These address inputs are multiplexed to memory address pins MA8-MA0 during column address time when a host-initiated memory access cycle is executed. For a host-initiated shift register-transfer cycle, these inputs are multiplexed to MA8-MA0 during row address time. CA0 is the LSB.
RS1,RS0	11, 12	I	Row Address Strobe Selects. During host-direct cycles and shift register transfer cycles, these signals determine which of the four row address strobes, $\overline{RAS}$3-$\overline{RAS}$0, is driven active low. If extended $\overline{RAS}$ mode is enabled, these inputs are ignored.
$\overline{CEH}$	29	I	Column Address Enable High. An active low from this signal enables $\overline{CASHI}$ during a host-initiated memory cycle.
$\overline{CEL}$	28	I	Column Address Enable Low. An active low from this signal enables $\overline{CASLO}$ during a host-initiated memory access cycle. $\overline{CEL}$ also strobes data into the internal registers during register write cycles and enables register data onto D7-D0 during register read cycles.
ALE	31	I	Address Latch Enable. The high-to-low transition of ALE latches the $\overline{CS}$, RA8-RA0, CA8-CA0, RS1-RS0, and FS2-FS0 inputs and is interpreted by the VSC as a command from the host to initiate the cycle specified by the values latched at these inputs.
R/$\overline{W}$	55	I	Read/Write. During a host initiated memory cycle or internal register access, R/$\overline{W}$ determines the direction of data transfer (high for read, low for write). By appropriately controlling the state of the R/$\overline{W}$ input, the system is allowed to execute the following cycles: read, write, early write, or read-modify-write.
$\overline{INT}$	25	O	Interrupt Request. The interrupt-request output indicates that an interrupt condition previously enabled by the host processor has occurred. $\overline{INT}$ will remain active until the host processor initiates a read of the Status Register.
D7-D0	43-36	I/O	Data Bus. The host accesses the internal registers of the VSC through this 8-bit bidirectional data bus. Each host accessible register within the VSC must be accessed one byte at a time via D7-D0. D0 is the LSB.
RDY/$\overline{HOLD}$	26	O	Ready or Hold. The operation and timing of RDY/$\overline{HOLD}$ is defined by two control bits contained in Control Register 2. RDY/$\overline{HOLD}$ can be configured to operate in "ready," "wait," or "hold" modes to accommodate various host processor interfaces.
$\overline{HOLDACK}$	27	I	Hold Acknowledge. When the VSC is configured in hold/hold acknowledge mode, the host issues a handshaking signal by driving $\overline{HOLDACK}$ low. The VSC can perform an internally requested cycle (display update or DRAM refresh) in this mode only when a handshaking acknowledgment has been received. $\overline{HOLDACK}$ is also used to configure the active level of RDY/$\overline{HOLD}$ at system power up.
$\overline{CS}$	13	I	Chip Select. This input operates as a master chip select. Before any host-initiated access involving the VSC can begin, $\overline{CS}$ must be active low.
FS2-FS0	34-32	I	Function Select. The three-bit function select code input on FS2-FS0 indicates the type of cycle requested by the host processor.

TABLE 1. PIN DESCRIPTIONS (CONCLUDED)

NAME	PIN	I/O	DESCRIPTION
SYSCLK	30	I	System Clock. This input is used to generate the timing of signals output to the memory, and the timing of the $\overline{INT}$ and the RDY/$\overline{HOLD}$ signals output to the host. All host interface signals input to the VSC must be synchronous to SYSCLK.
$\overline{RESET}$	56	I	Reset. An active-low $\overline{RESET}$ places the VSC in a known initial state. While $\overline{RESET}$ is low, the internal registers are forced to their default values, and all VRAM control outputs are forced to their inactive levels. $\overline{RESET}$ should be driven low when power is first applied and remain low for at least 1 ms.
$\overline{RAS3}$-$\overline{RAS0}$	14-17	O	Row Address Strobes. These active-low outputs are designed to drive the $\overline{RAS}$ inputs on both the TMS4161 VRAM and conventional DRAMs. During display update and refresh cycles, all four $\overline{RAS}$ outputs are driven active low in the default mode of operation.
$\overline{CASHI}$	19	O	Column Address Strobe High. This active-low output is designed to directly drive the $\overline{CAS}$ inputs on both the TMS4161 VRAM and conventional DRAMs. During memory cycles initiated by the host, $\overline{CASHI}$ becomes active only after the $\overline{CEH}$ input is driven active low.
$\overline{CASLO}$	20	O	Column Address Strobe Low. The operation of $\overline{CASLO}$ is similar to that of $\overline{CASHI}$, as described above, except that $\overline{CASLO}$ is enabled by an active low on $\overline{CEL}$ rather than $\overline{CEH}$.
$\overline{W}$	58	O	Write Control. This signal is used to drive the $\overline{W}$ inputs on both the TMS4161 VRAM and conventional DRAMs. $\overline{W}$ is driven active low during write cycles requested by the host.
$\overline{TR/QE}$	57	O	Shift Register Transfer and Output Enable. The $\overline{TR/QE}$ output directly drives the $\overline{TR/QE}$ inputs on the TMS4161 VRAM. Signals used to enable shift register transfer cycles and VRAM output buffers during read cycles are multiplexed over this single pin.
$\overline{BLANK}$	21	O	Video Blanking. The $\overline{BLANK}$ output is used to disable video data to the CRT monitor. $\overline{BLANK}$ is driven active low during both horizontal and vertical blanking intervals.
$\overline{HSYNC}$	23	I/O	Horizontal Sync. $\overline{HSYNC}$ generates the horizontal sync pulses used to control a CRT monitor. It operates as an output, except when the external sync mode is enabled.
$\overline{VSYNC}$	22	I/O	Vertical Sync. $\overline{VSYNC}$ generates the vertical sync pulses used to control a CRT monitor and operates as an output, except when the external sync mode is enabled.
VIDCLK	24	I	Video Clock. The video input clock drives the logic within the VSC chip that is responsible for generating the timing for the sync and blanking signals. VIDCLK also drives the logic responsible for generating internal requests for display update and VRAM refresh cycles.
V_{CC}	10, 44		5-volt supply input.
V_{SS}	1, 18, 35, 52		Ground.

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programmable registers

The programmable registers in the TMS34061 allow configuration of the CRT timings, system CPU interface, and X-Y address parameters. Most of these registers contain bits that are not currently implemented; these bits are designated in the following tables by an "X." To maintain compatibility with future device upgrades, a logical zero should be written to these bits.

TABLE 2. VIDEO TIMING REGISTERS

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
Horizontal End Sync	XXXXAAAA	AAAAAAAA	00000	Identifies the end of horizontal sync interval. Contents = horizontal sync width − 1 VIDCLK unit
Horizontal End Blank	XXXXAAAA	AAAAAAAA	00001	Identifies the end of horizontal blank interval. Contents = horizontal sync width + horizontal back porch − 1 VIDCLK unit
Horizontal Start Blank	XXXXAAAA	AAAAAAAA	00010	Identifies the start of horizontal blank interval. Contents = horizontal sync width + horizontal back porch + horizontal active screen − 1 VIDCLK unit
Horizontal Total	XXXXAAAA	AAAAAAAA	00011	Identifies the start of horizontal sync interval. Contents = total line time − 1 VIDCLK unit
Vertical End Sync	XXXXAAAA	AAAAAAAA	00100	Identifies the end of vertical sync interval. Contents = vertical sync width − 1 horizontal total units
Vertical End Blank	XXXXAAAA	AAAAAAAA	00101	Identifies the end of vertical blanking interval. Contents = vertical sync width + vertical back porch − 1
Vertical Start Blank	XXXXAAAA	AAAAAAAA	00110	Identifies the start of vertical blank interval. Contents = vertical sync + vertical back porch + vertical active − 1 horizontal total units
Vertical Total	XXXXAAAA	AAAAAAAA	00111	Identifies the start of vertical sync interval. Contents = number of horizontal lines − 1 horizontal total units.

NOTE: "A" = active register bit, "X" = bit not implemented.

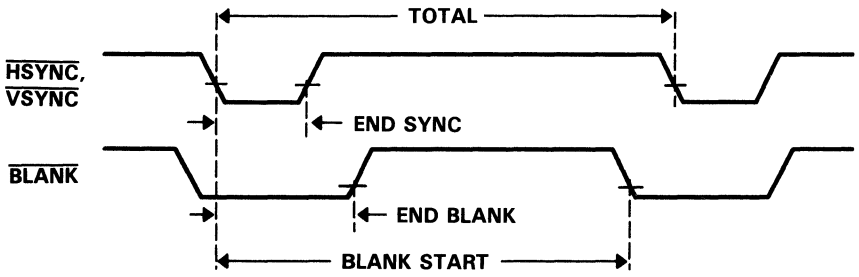

FIGURE 1. SYNC AND BLANK RELATIONSHIP

The following equations show the derivation of the various parameters required to initialize the VSC to interface to any CRT monitor:

Horizontal End Sync = Horizontal Sync Width − 1
Horizontal End Blank = Horizontal Sync Width + Horizontal Back Porch − 1
Horizontal Start Blank = Horizontal Sync Width + Horizontal Back Porch + Horizontal Active Screen − 1
Horizontal Total = Total Line Time − 1
Vertical End Sync = Vertical Sync Width − 1
Vertical End Blank = Vertical Sync Width + Vertical Back Porch − 1
Vertical Start Blank = Vertical Sync Width + Vertical Back Porch + Vertical Active Screen − 1
Vertical Total = Number of Horizontal Lines − 1

All horizontal timing parameters are in VIDCLK unit, and all vertical timing parameters are in horizontal line time units.

TABLE 3. CPU INTERFACE REGISTERS

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
Control Register 1	XAAAAAAA	AAAXAAAA	01011	Controls the behavior of host interface signals, the timing of display-update cycles, the enabling of interrupt requests, the frequency of DRAM-refresh cycles, and the configuration of video timing signals
Control Register 2	XAAAAAAA	AAAAAAAA	01100	

TABLE 4. CONTROL REGISTER 1 BIT DEFINITIONS

BITS	NAME
B3-B0	Line Count Limit
B4	Reserved
B5	Display-Update Inhibit
B6	Display-Update Direction
B7	Display-Update $\overline{RAS}$ Mode
B8	External Sync Enable
B9	Interlace Enable
B10	Vertical Interrupt Enable
B11	Error Interrupt Enable
B12-B14	Refresh Burst Length
B15	Reserved

TABLE 5. CONTROL REGISTER 2 BIT DEFINITIONS

BITS	NAME
B1-B0	Extended $\overline{RAS}$-Mode Select Bits
B5-B2	$\overline{RAS}$ Overrides
B6	Extended $\overline{RAS}$ Mode
B7	X-Y Address Pointer $\overline{RAS}$ Mode
B10-B8	Wait State Limit
B12-B11	RDY/$\overline{HOLD}$ Mode Select
B13	Blank Entire Display
B14	Early RDY Enable
B15	Reserved

TABLE 6. STATUS REGISTER

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
Status	XXXXXXXX	XXXXXAAA	01101	An error condition or vertical interrupt has occurred

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TABLE 7. STATUS REGISTER BIT DEFINITIONS

BITS	NAME
B0	Vertical Interrupt
B1	Display Error
B2	Refresh Error

TABLE 8. VERTICAL INTERRUPT REGISTER

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
Vertical Interrupt	XXXXAAAA	AAAAAAAA	01010	Generates a vertical interrupt when contents are equal to Vertical Counter

TABLE 9. CRT CONTROL REGISTERS

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
Display Address	XXXXAAAA	AAAAAAAA	10000	Contains the address to be output during the next automatic display-update cycle
Display Update	XXXXXXXX	XXXXAAAA	01000	Contains the value by which the display address is incremented
Display Start	XXXXAAAA	AAAAAAAA	01001	Specifies the memory location to be displayed at the upper left of the screen

TABLE 10. X-Y REGISTERS

REGISTER NAME	UPPER BYTE CA1 = 1	LOWER BYTE CA1 = 0	ADDRESS CA6-CA2	DESCRIPTION
X-Y Address	AAAAAAAA	AAAAAAAA	01111	Contains address for host-indirect memory accesses
X-Y Offset	XXXXAAAA	AAAAAAAA	01110	Defines the boundary between the X-Y portions of the X-Y Address Register and contains the initial value of the two $\overline{RAS}$-select bits and the two independent multiplexed address bits

address multiplexer

The address multiplexer provides the Multiport VRAM array with row, column, and internal addresses at the proper times. Its inputs are from the host system, the display address register, the X-Y indirect address register, and the DRAM refresh address counter. The specific source of the address is controlled by the arbiter, and the RA or CA portion of the address is controlled by the memory cycle generator. Eighteen multiplexed address signals are provided by the 9-bit MA address outputs. The address multiplexer directly drives inputs for up to 64 TMS4161 Multiport VRAM devices or conventional dynamic RAM devices of up to 256K bits.

DRAM refresh counters

Programmable DRAM refresh cycles allow the VSC to relieve the host of refresh burden. The refresh burst length is determined by bits 14-12 in Control Register 1. These three bits output a binary number from 000 to 111 which indicates the number of DRAM refresh cycles, from 0 to 7 per horizontal line. This binary number is then counted by the Refresh Burst Counter (host inaccessible). The Refresh Burst Counter outputs a 9-bit row address to the Address Multiplexers during DRAM refresh cycles, while the Memory Cycle Generator increments the DRAM Refresh Register (host inaccessible) to the next 9-bit row address to be output.

X-Y address capability

X-Y addressing is particularly useful when the linear addressing range of the host is insufficient to provide proper access of all pixels on the screen. The contents of the X-Y registers replace the RA and CA outputs as source of the memory address. A 4-bit code on inputs CA4-CA1 determines address adjustment (increment, decrement, clear, no change). X-Y capability relieves the host from calculating the address of the next pixel to be modified.

arbiter

The arbiter determines whether the host processor, the video shift-register reload logic, or the dynamic-RAM refresh logic can access the memory or start a reload or refresh cycle. Since the display and refresh functions of the VSC normally use less than six percent of the available memory cycles, the arbiter usually grants immediate memory access to the host. When a conflict arises, the arbiter grants priority as follows:

1) Any cycle in progress
2) A display update cycle (internally granted request)
3) A DRAM-refresh cycle that has been delayed for more than 1/2 horizontal line
4) Any host-requested cycle
5) DRAM-refresh cycle.

memory cycle generator

Various memory cycles requested by the arbiter are performed by the Memory Cycle Generator, which also provides the DRAM array with the $\overline{RAS}$, $\overline{CAS}$, $\overline{TR/QE}$, and $\overline{W}$ signals. It controls the multiplexer during all cycles in order to meet the address and control line-setup and hold requirements. Cycles generated:

- Host-requested cycles
  - Read
  - Write
  - Early write
  - Read-modify-write
  - Memory-to-shift register
  - Shift register-to-memory
- Delayed host-requested cycles
- Internally requested shift register transfer
- Internally requested refresh cycle

CRT control

The VSC generates the $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ signals used to drive a CRT monitor in a bit-mapped graphics system. These signals are synchronous to the Video Input Clock (VIDCLK). $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are programmed through eight host accessible video timing registers, which are easily configured to accommodate a variety of display resolutions and CRT monitors in either interlaced or non-interlaced modes. Two additional registers, clocked by VIDCLK, maintain the current horizontal and vertical counts.

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The values in these two counters are compared with the values in the eight video timing registers to determine the limits of the sync and blanking intervals. Programmed synchronization of external sync signals allows the VSC to superimpose an image upon an externally generated video source.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 7 V
Off-state output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions†

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	$\overline{VSYNC}$, $\overline{HSYNC}$, $\overline{BLANK}$ $\overline{INT}$, RDY/$\overline{HOLD}$, D7-D0			−370	μA
I_{OL}	Low-level output current	$\overline{VSYNC}$, $\overline{HSYNC}$, $\overline{BLANK}$, $\overline{INT}$, RDY/$\overline{HOLD}$, D7-D0			3.2	mA
T_A	Operating free-air temperature		0		70	°C

†Case temperature must be maintained below 95°C. $R_{\theta JA}$ = 46.4°C/W; $R_{\theta JC}$ = 11.1°C/W.

electrical characteristics over recommended free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MAX, I_{OL} = MAX				0.4	V
I_{CC}	Supply current	V_{CC} = MAX			200	275	mA
		V_{CC} = MAX, T_C = 95°C, t_{cSC} = MAX			170	200	mA
I_O	High-impedance output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Input current	V_I = V_{SS} to V_{CC}				±20	μA
	Output loading	$\overline{RAS3}$-$\overline{RAS0}$, $\overline{CASLO}$, $\overline{CASHI}$, MA0-MA8, $\overline{TR/QE}$				350	pF
		$\overline{W}$				670	

system clock timing parameters

PARAMETER		MIN	MAX	UNIT
t_{cSC}	SYSCLK clock period	100	500	ns
$t_{w(SCH)}$	SYSCLK clock high pulse duration	45	246	ns
$t_{w(SCL)}$	SYSCLK clock low pulse duration	45	246	ns

NOTES: 2. SYSCLK frequency must be greater than one-half the VIDCLK frequency.
3. All switching characteristics are measured between the maximum low level and the minimum high level using the 10 percent and the 90 percent points.

memory and host interface timing parameters

PARAMETER		MIN	MAX	UNIT
$t_{w(RSTL)}$	Reset active (low) pulse duration	1		ms
$t_{h(RSTH-ALEH)}$	Reset wait period after a reset low-to-high transition pulse and prior to the first host-requested memory cycle	1		ms
$t_{su(ALE-SCH)}$	Setup time of ALE low or high to SYSCLK no longer low (Note 4)	20		ns
$t_{h(SCH-ALE)}$	Hold time of ALE low or high after SYSCLK high (Note 4)	10		ns
$t_{w(ALEH)}$	Pulse duration of ALE high	40		ns
$t_{su(CE-SCH)}$	Setup time of $\overline{CEL}$ or $\overline{CEH}$ low or high to SYSCLK no longer low (Note 4)	20		ns
$t_{h(SCH-CE)}$	Hold time of $\overline{CEL}$ or $\overline{CEH}$ low or high after SYSCLK high (Note 4)	10		ns
$t_{su(ADDR-ALEL)}$	Setup time of RA, CA, RS, or $\overline{CS}$ input valid before ALE no longer high	35		ns
$t_{h(ALEL-ADDR)}$	Hold time of RA, CA, FS, RS, or $\overline{CS}$ input valid after ALE low	10		ns
$t_{d(SCH-RMA)H}$	Delay from SYSCLK high to row memory address valid, host initiated memory cycle (Note 5)		75	ns
$t_{h(SCH-RMA)}$	Hold time of row address valid after SYSCLK no longer low†	10	60	ns
$t_{d(SCH-CMA)}$	Delay from SYSCLK high to column memory address valid (Note 5)	20	75	ns
$t_{h(ALEH-CMA)}$	Hold time of column memory address valid after ALE	0		ns
$t_{d(SCL-RASL)}$	Delay from SYSCLK low to $\overline{RAS}$ low (Note 5)†	20	70	ns
$t_{d(ALEH-RASH)}$	Delay from ALE high to $\overline{RAS}$ high (Note 5)	20	70	ns
$t_{d(SCH-RASH)}$	Delay from SYSCLK high to $\overline{RAS}$ high in display update and DRAM refresh (Note 5)	20	70	ns
$t_{d(ALEL-RDYL)}$	Delay from ALE low to RDY/$\overline{HOLD}$ at "not ready" level		35	ns
$t_{d(SCL-RDYH)}$	Delay from SYSCLK low to RDY/$\overline{HOLD}$ at "ready" level (Note 6)		70	ns
$t_{d(SCH-RDYH)}$	Delay from SYSCLK high to RDY/$\overline{HOLD}$ at "ready" level (Note 6)		70	ns

†Row address hold time guaranteed by $t_{h(RMA)}$ parameter.

NOTES: 4. ALE, $\overline{CEH}$, and $\overline{CEL}$ inputs are synchronous to SYSCLK and must meet the required setup and hold times specified with respect to each SYSCLK low-to-high transition in order to guarantee correct operation.
5. This timing is based on a load circuit equivalent to 64 TMS4161 VRAMS being driven by the VSC. Each of the following outputs drive a 350-pF capacitance to V_{SS}: MA8-MA0, $\overline{CASLO}$, $\overline{CASHI}$, $\overline{RAS3}$-$\overline{RAS0}$, $\overline{TR}/\overline{QE}$. The $\overline{W}$ output drives a 670-pF capacitance to ground. All other outputs drive a 560-ohm resistor tied to a 2.2-volt source with a 100 pF capacitance load tied to V_{SS}.
6. All references made to the RDY/$\overline{HOLD}$ signal in the timing spec assumes an active high level.

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memory and host interface timing parameters (continued)

	PARAMETER	MIN	MAX	UNIT
$t_{d(ALEH-RDYZ)}$	Delay from ALE no longer low to RDY/$\overline{HOLD}$ high-impedance level starting from RDY/$\overline{HOLD}$ (Note 6)		40	ns
$t_{d(SCL-CASL)}$	Delay from SYSCLK low to $\overline{CAS}$ low to $\overline{CASLO}$ or $\overline{CASHI}$ (Note 5)	20	75	ns
$t_{d(ALEH-CASH)}$	Delay from ALE, $\overline{CEH}$, or $\overline{CEL}$ high to $\overline{CASLO}$ or $\overline{CASHI}$ (Note 5)	20	60	ns
$t_{d(SCL-TRL)}$	Delay from SYSCLK low to $\overline{TR/QE}$ low (Note 5)	20	75	ns
$t_{d(ALEH-TRH)}$	Delay from ALE, $\overline{CEH}$ or $\overline{CEL}$ high to $\overline{TR/QE}$ high (Note 5)	20	60	ns
$t_{d(SCH-WL)HX}$	Delay from SYSCLK high to $\overline{W}$ low (Note 5), host direct or X-Y indirect cycle	20	85	ns
$t_{d(ALEH-WH)}$	Delay from ALE high to $\overline{W}$ high (Note 5)	20	80	ns
$t_{d(RWL-WL)}$	Delay from R/$\overline{W}$ low to $\overline{W}$ low (Note 5)	20	85	ns
$t_{d(RWH-WH)}$	Delay from R/$\overline{W}$ high to $\overline{W}$ high (Note 5)	20	85	ns
$t_{d(SCH-WL)SR}$	Delay from SYSCLK high to $\overline{W}$ or $\overline{TR/QE}$ low, shift register transfer cycles (Note 5)	20	85	ns
$t_{h(ALEL-CELH)}$	Hold time of $\overline{CEL}$ high after ALE no longer high, register cycle	0		ns
$t_{h(CELH-ALEL)}$	Hold time of ALE low after $\overline{CEL}$ no longer low, register cycle	0		ns
$t_{su(RW-CELL)}$	Setup time of R/$\overline{W}$ valid to $\overline{CEL}$ no longer high, register cycle	30		ns
$t_{h(CELH-RW)}$	Hold time of R/$\overline{W}$ valid after $\overline{CEL}$ high, register cycle	10		ns
$t_{d(CELL-D)}$	Delay time from $\overline{CEL}$ low to D7-D0 valid all but status, register cycle	30	130	ns
$t_{d(SCH-D)}$	Data valid after next SYSCLK rising edge following $\overline{CEL}$ low for status read cycle only		130	ns
$t_{d(CELH-DZ)}$	Delay from $\overline{CEL}$ high to D7-D0 high impedance, register cycle		105	ns
$t_{d(CELL-RDYH)}$	Delay from $\overline{CEL}$ low to RDY/$\overline{HOLD}$ "ready" level, register cycle (Note 6)		70	ns
$t_{su(D-CELH)}$	Setup time of D7-D0 valid to $\overline{CEL}$ no longer low, register write	60		ns
$t_{h(CELH-D)}$	Hold time of D7-D0 valid after $\overline{CEL}$ high, register write	10		nss
$t_{su(RWL-CELH)}$	Setup time of R/$\overline{W}$ low to $\overline{CEL}$ no longer low, register write	80		ns
$t_{d(RWL-DZ)}$	Delay from R/$\overline{W}$ low to D7-D0 high impedance, register read-modify-write		105	ns
$t_{d(SCH-RMA)D}$	Delay from SYSCLK high to row memory address valid, display update cycle (Note 5)		70	ns
$t_{(SCH-CMA)}$	Hold time of column address valid after SYSCLK no longer low, display update cycle (Note 5)	0		ns
$t_{d(SCH-CASH)}$	Delay from SYSCLK high to $\overline{CAS}$ high (Note 5)	20	70	ns
$t_{d(SCH-TRL)}$	Delay from SYSCLK high to $\overline{TR/QE}$ low, display-update cycle (Note 5)	20	65	ns
$t_{d(SCL-TRH)}$	Delay from SYSCLK high to $\overline{TR/QE}$ high, display-update cycle (Note 5)	20	75	ns

†Row address hold time guaranteed by $t_{h(RMA)}$ parameter.

NOTES: 4. ALE, $\overline{CEH}$, and $\overline{CEL}$ inputs are synchronous to SYSCLK and must meet the required setup and hold times specified with respect to each SYSCLK low-to-high transition in order to guarantee correct operation.

5. This timing is based on a load circuit equivalent to 64 TMS4161 VRAMS being driven by the VSC. Each of the following outputs drive a 350-pF capacitance to V_{SS}: MA8-MA0, $\overline{CASLO}$, $\overline{CASHI}$, $\overline{RAS3}$-$\overline{RAS0}$, $\overline{TR/QE}$. The $\overline{W}$ output drives a 670-pF capacitance to ground. All other outputs drive a 560-ohm resistor tied to a 2.2-volt source with a 100 pF capacitance load tied to V_{SS}.

6. All references made to the RDY/$\overline{HOLD}$ signal in the timing spec assumes an active high level.

memory and host interface timing parameters (concluded)

	PARAMETER	MIN	MAX	UNIT
$t_{d(SCH-WL)}$	Delay from SYSCLK high to $\overline{W}$ low, display-update cycle (Note 5)	20	85	ns
$t_{d(SCH-WH)}$	Delay from SYSCLK high to $\overline{W}$ high, display-update cycle (Note 5)	20	85	ns
$t_{h(CASL-TRL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{CAS}$ no longer high	75		ns
$t_{su(TRH-RASH)}$	Setup time of $\overline{TR}/\overline{QE}$ high before $\overline{RAS}$ no longer low	15		ns
$t_{d(SCH-RDY)}$	Delay from SYSCLK high to RDY/$\overline{HOLD}$ valid (hold mode)		75	ns
$t_{h(SCH-HA)}$	Hold time of valid $\overline{HOLDACK}$ after SYSCLK high, hold mode only (Note 4)	10		ns
$t_{su(HA-SCH)}$	Setup time of $\overline{HOLDACK}$ low or high before SYSCLK no longer low, hold mode only (Note 4)	20		ns
$t_{d(SCH-INT)}$	Delay from SYSCLK high to $\overline{INT}$ low or high		55	ns
$t_{su(RMA)}$	Row memory address setup before $\overline{RAS}$ no longer high	0		ns
$t_{su(CMA)}$	Column memory address setup before $\overline{CAS}$ no longer high	0		ns
$t_{su(TR)}$	$\overline{W}$ or $\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ no longer high, shift register transfer, display update	0		ns
$t_{h(RMA)}$	Row memory address hold time from $\overline{RAS}$ low	35		ns
$t_{su(HA-RSTH)}$	Setup of $\overline{HOLDACK}$ prior to $\overline{RESET}$ going high, ready and wait modes only	50		ns
$t_{h(RSTH-HA)}$	Hold time of $\overline{HOLDACK}$ after $\overline{RESET}$ high, ready and wait modes only	50		ns

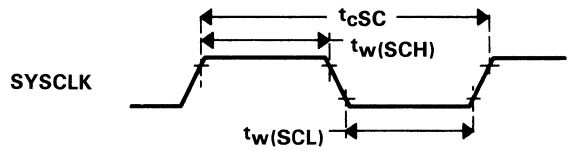
† Row address hold time guaranteed by $t_{h(RMA)}$ parameter.

NOTES: 4. ALE, $\overline{CEH}$, and $\overline{CEL}$ inputs are synchronous to SYSCLK and must meet the required setup and hold times specified with respect to each SYSCLK low-to-high transition in order to guarantee correct operation.

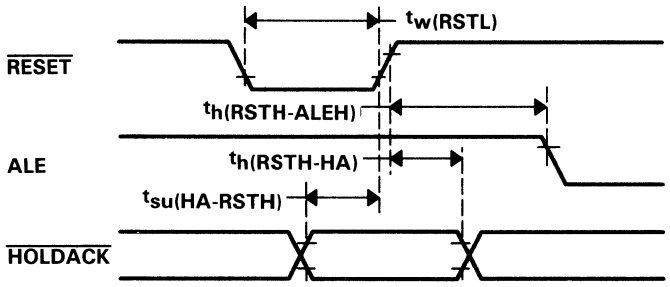
5. This timing is based on a load circuit equivalent to 64 TMS4161 VRAMS being driven by the VSC. Each of the following outputs drive a 350-pF capacitance to V_{SS}: MA8-MA0, $\overline{CASLO}$, $\overline{CASHI}$, $\overline{RAS3}$-$\overline{RAS0}$, $\overline{TR}/\overline{QE}$. The $\overline{W}$ output drives a 670-pF capacitance to ground. All other outputs drive a 560-ohm resistor tied to a 2.2-volt source with a 100 pF capacitance load tied to V_{SS}.

6. All references made to the RDY/$\overline{HOLD}$ signal in the timing spec assumes an active high level.

system clock timing



reset timing



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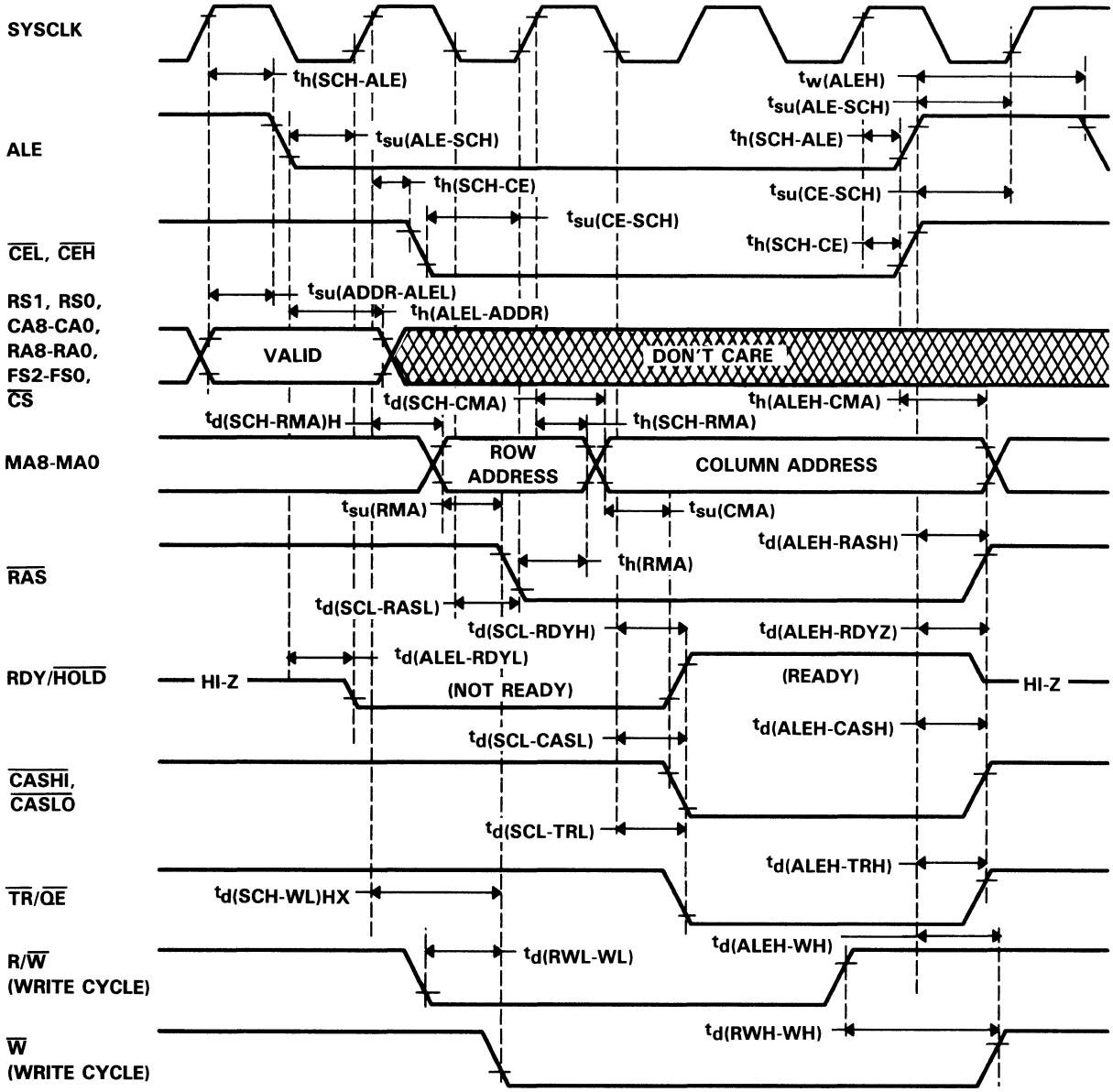
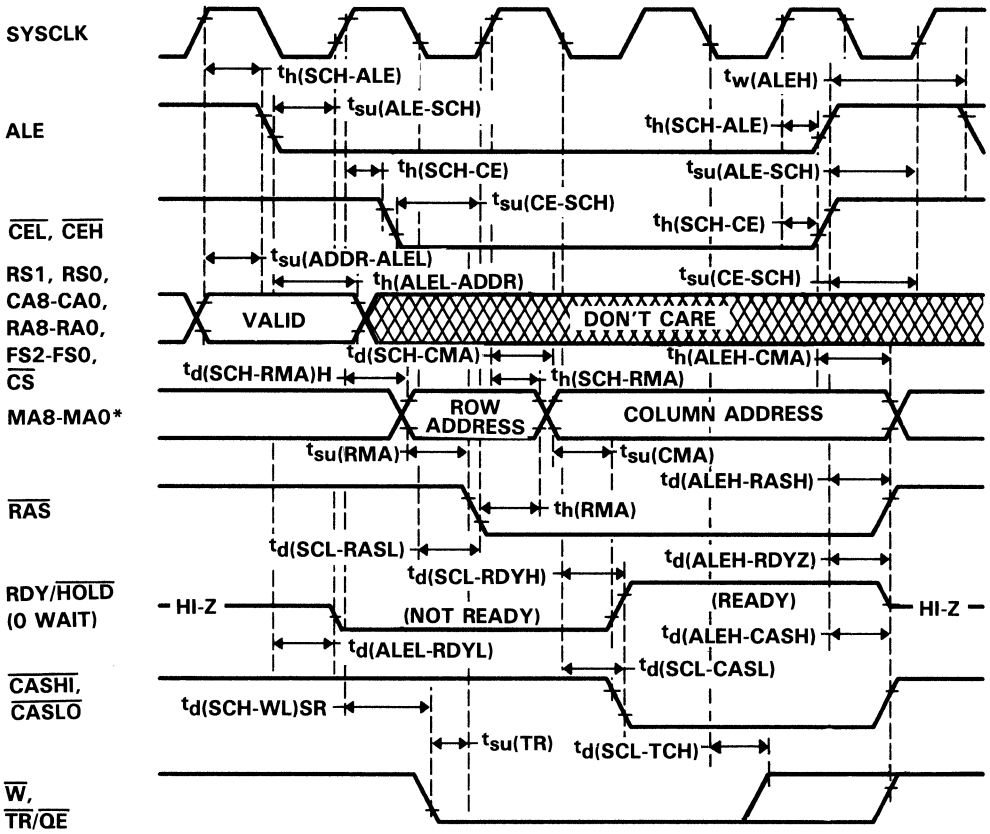
host direct or X-Y indirect cycle timing

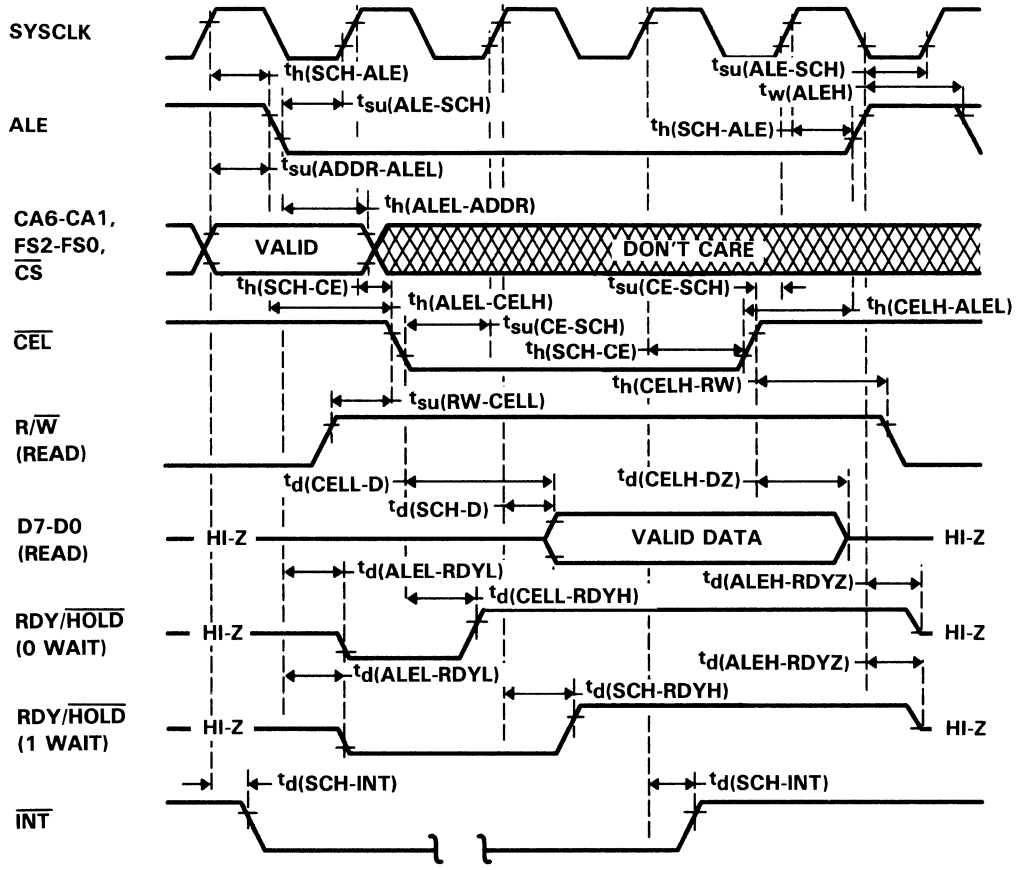


shift-register-transfer cycle timing

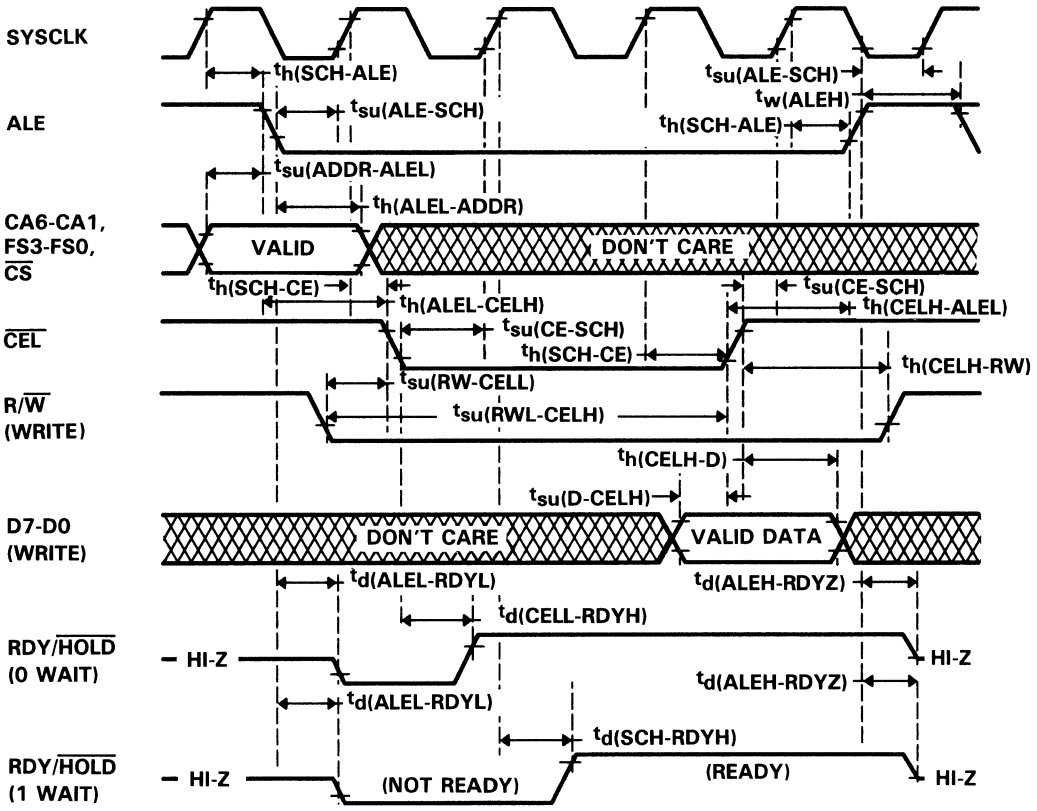


* During a shift-register cycle the nine bits of address input on CA8-CA0 are output on MA8-MA0 at row address time, and the nine bits of address input on RA8-RA0 are output on MA8-MA0 at column address time. This multiplexing of the row and column addresses is intended to reduce memory address map requirement.

register read cycle timing



register write cycle timing



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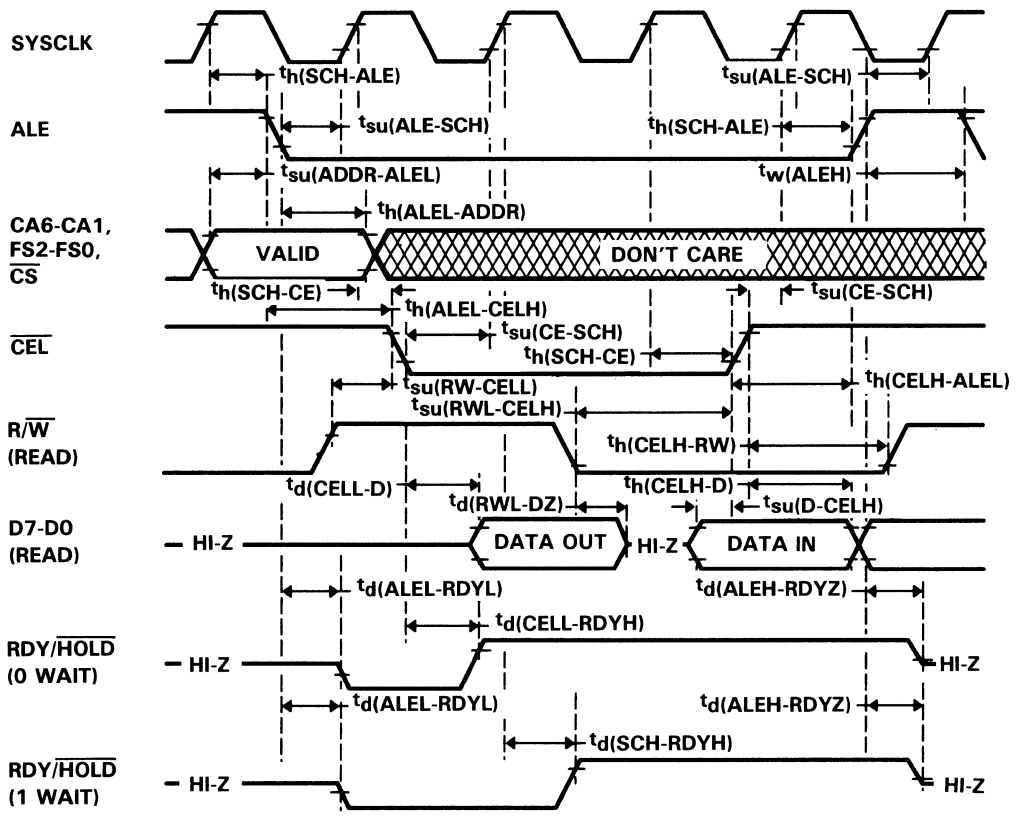
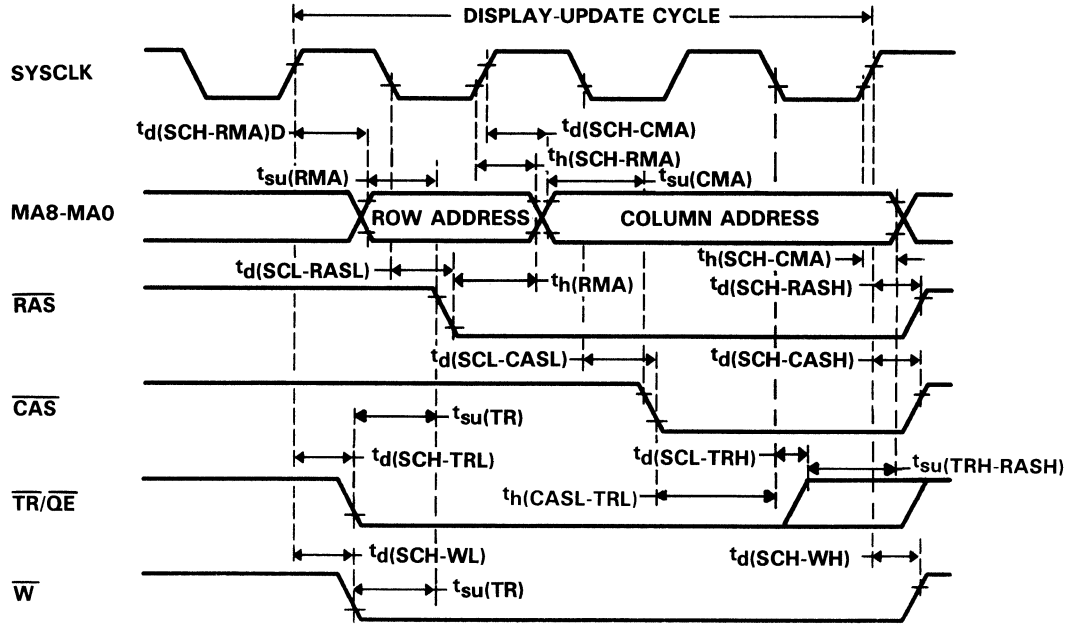
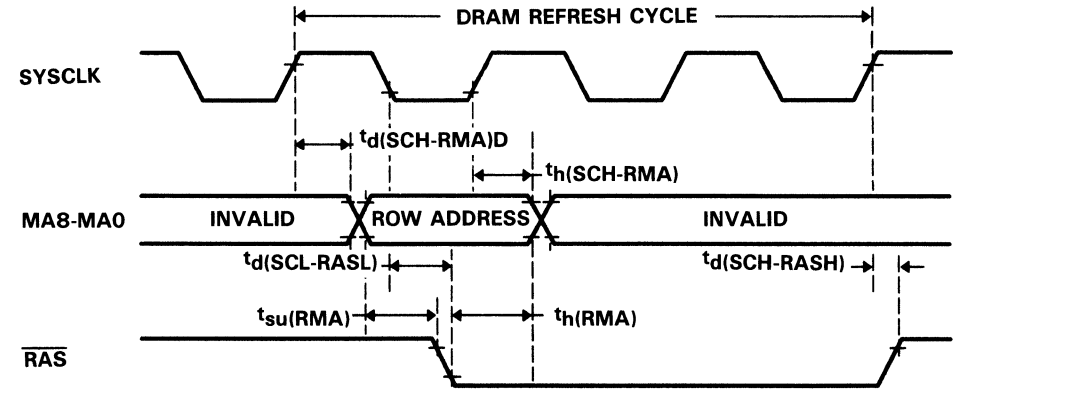
register read-modify-write cycle timing



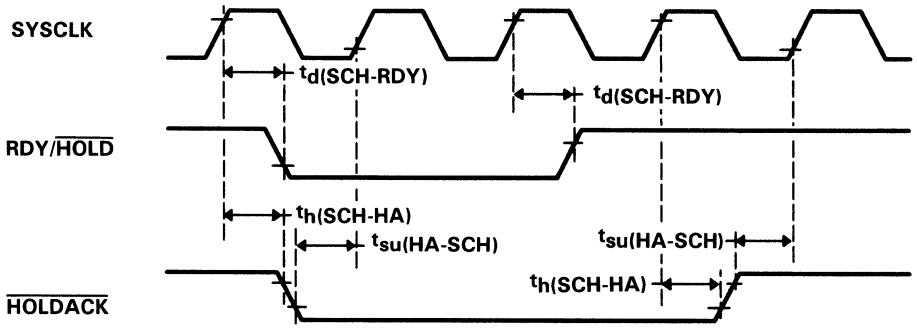
display-update cycle timing



DRAM-refresh cycle timing



hold/hold acknowledge timing



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video interface timing parameters

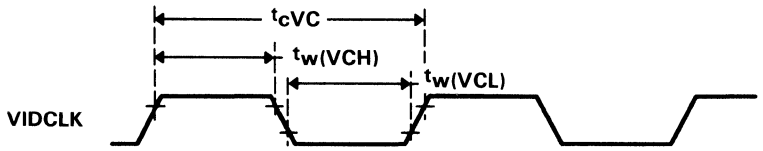
The timing parameters for VSC video interface signals are presented below. This interface includes the following VSC pins: VIDCLK(video input clock), $\overline{\text{BLANK}}$ (blanking), $\overline{\text{HSYNC}}$ (horizontal sync, bidirectional) and $\overline{\text{VSYNC}}$ (vertical sync, bidirectional). $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are inputs only if external sync mode is enabled; if not, they are outputs.

video interface signals timing parameters

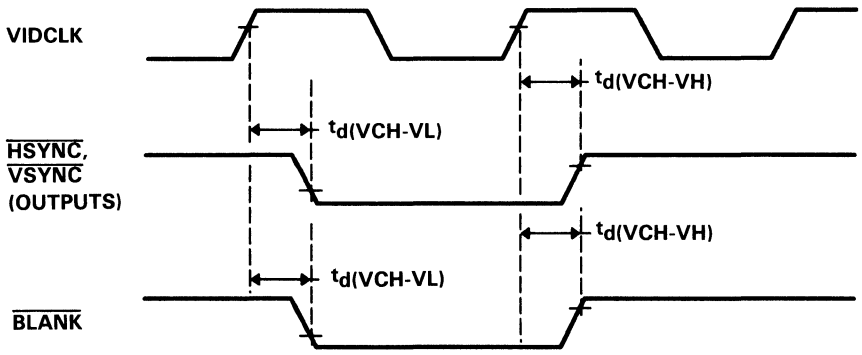
PARAMETER		MIN	MAX	UNIT
t_{cVC}	Period of input clock VIDCLK (Note 7)	155	500	ns
$t_{w(VCH)}$	Pulse duration of VIDCLK high	73	246	ns
$t_{w(VCL)}$	Pulse duration of VIDCLK low	73	246	ns
$t_{d(VCH-VL)}$	Delay from VIDCLK high to sync low or blanking output low	20	80	ns
$t_{d(VCH-VH)}$	Delay from VIDCLK high to sync or blanking output high	20	80	ns
$t_{su(XS-VCH)}$	Setup time of external sync low or high VIDCLK no longer low (Note 8)	20		ns
$t_{h(VCH-XS)}$	Hold time of external sync low or high after VIDCLK high (Note 8)	15		ns

NOTES: 7. If HTOTAL-HSBLANK is equal to 1, then the VIDCLK frequency must be less than 4 MHz. If HTOTAL-HSBLANK is equal to or greater than 2, then the VIDCLK frequency can operate up to a maximum of 6.5 MHz.
8. Specified setup and hold times on asynchronous inputs are required only to guarantee recognition at indicated clock edge.

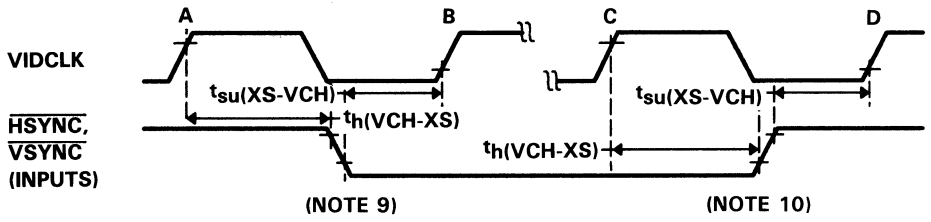
video clock input timing



output signal timing



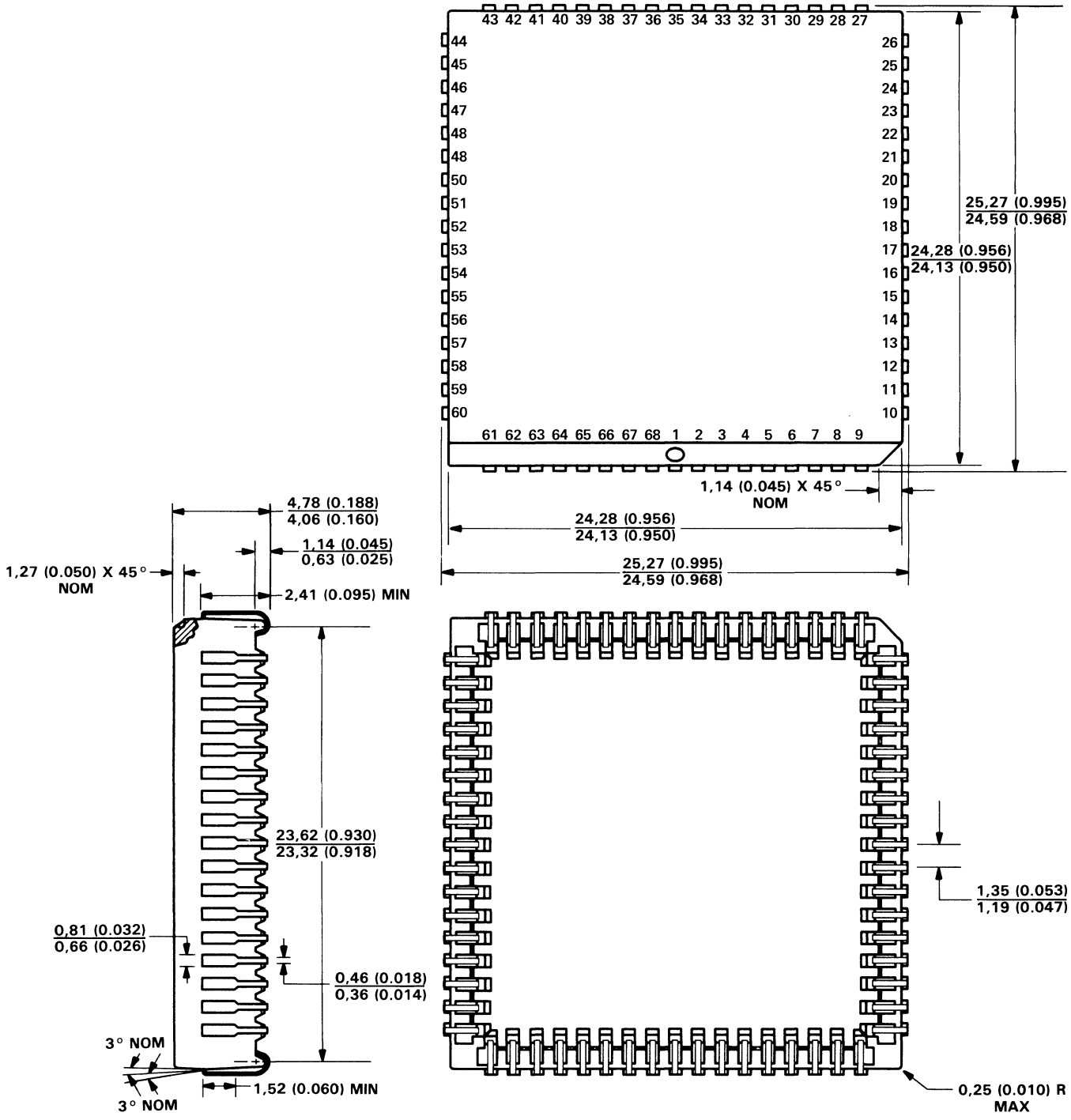
external sync input timing



NOTES: 9. If the falling edge of the sync signal occurs more than 10 ns past VIDCLK edge A, and at least 20 ns before edge B, the transition will be detected at edge B rather than at edge A.

10. If the rising edge of the sync signal occurs more than 10 ns past VIDCLK edge C, and at least 20 ns before edge D, the transition will be detected at edge D rather than at edge C.

MECHANICAL DATA



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