TMS34061 User's Guide

TEXAS INSTRUMENTS

1. Introduction

The TMS34061 Video System Controller (VSC) is a high-performance NMOS device that controls the video display and the dynamic memory of a bit-mapped graphics system. Although primarily designed to provide control of multiport Video RAMs (VRAMs), such as the TMS4161 and 256K video RAMs, the TMS34061 is also compatible with conventional 64K and 256K DRAMs and easily configures to a variety of CPUs. The sync and blanking signals necessary to interface to a raster-scan CRT display are generated by the TMS34061, which is the only device currently available that combines VRAM and DRAM control and CRT control on a single chip.

The principal role of the VSC is to provide an external processor with virtually unlimited access to video memory, eliminating delays caused by conflicts with display update functions. Using the TMS34061, the system CPU is relieved of the burden of controlling the system memory, refreshing video memory, and reloading VRAM internal shift registers for bit-mapped displays.

Highly programmable, the TMS34061 supports a broad range of raster-scan display systems with various resolutions and scan rates. Some of the major functions of the TMS34061 VSC are:

- Generates all control signals necessary to control VRAM devices, as well as those necessary to control conventional 64K and 256K DRAMs.
- Generates the video synchronization and blanking signals necessary to control a CRT monitor.
- Accommodates processor data paths of arbitrary width. The TMS34061 works equally well with 8-, 16-, 20-, and 32-bit processors.
- Supports both interlaced and non-interlaced displays of essentially any display resolution (from 256 to greater than 4096 pixels per line).
- Automatically generates the special display-update cycles required by VRAM memories to maintain the CRT display.
- X-Y indirect addressing improves the performance of graphics primitives as well as supporting host processors with limited addressing range.
- Automatically performs periodic DRAM refresh cycles necessary to maintain data stored in the VRAMs, as well as in conventional 64K and 256K DRAMs.
- Universally programmable interface and READY/WAIT logic provides for efficient communication with all leading microprocessors as well as high-speed bit slice processors.

The block diagram of a typical system using the TMS34061 with the TMS4161 VRAM is shown in Figure 1-1.

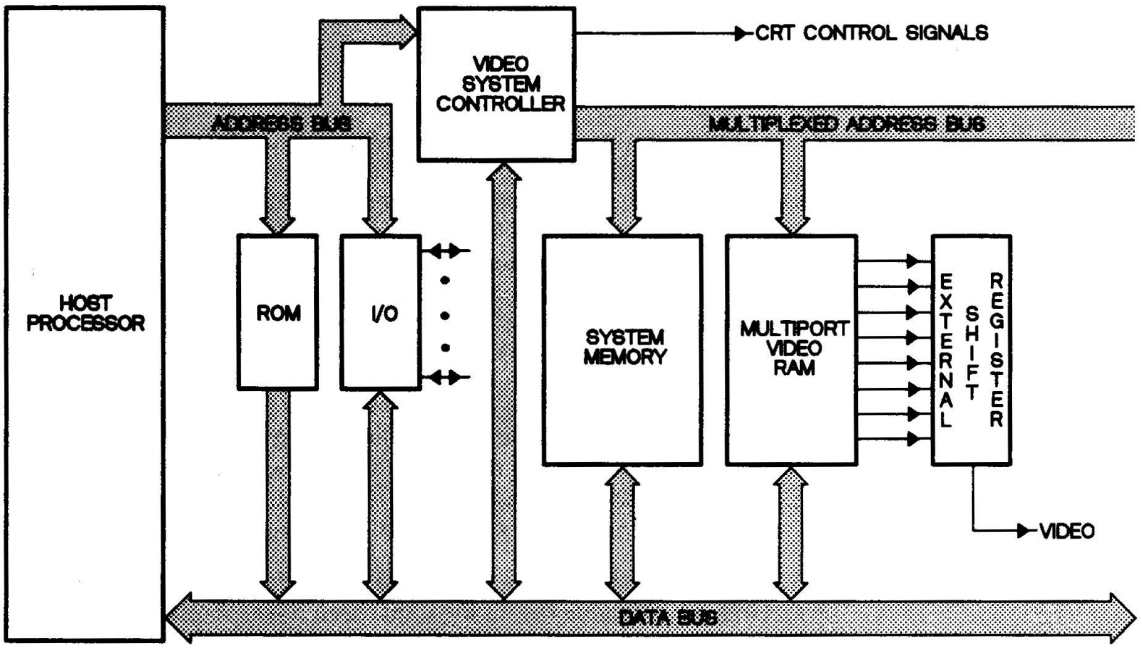


Figure 1-1. Block Diagram of Typical TMS34061 VSC System

1.1 Typical Applications

- Business and Personal Computer Systems
- Bit-Mapped Terminals
- CAD/CAM/CAE Workstations
- Instrumentation
- Printers (Laser)
- Plotters

1.2 Key Features

- Virtually constant availability of the memory to the host processor, since display access and dynamic RAM refresh require less than 6% of the total memory bandwidth.
- Controls bidirectional data transfer in the TMS4161 VRAM's internal shift register; from shift register to memory and from memory to shift register.
- Each TMS34061 can directly drive up to 64 VRAM or DRAM devices and can control more than 64 with external hardware.
- Provides shift-register reload for the TMS4161's internal shift register at a completely user-programmable rate.
- Generates user-programmable control signals (horizontal sync, vertical sync, and blanking) which support a broad range of raster-scan display systems with varying resolutions and scan rates.
- Provides dynamic RAM refreshing for VRAM and system DRAM at user-selectable rates.
- Synchronizes to an external sync source, allowing images to be superimposed on externally generated sources.
- Separate video and system clocks allow the video system and the host processor to run asynchronously.

2. Pinout and Signal Descriptions

The pin number assignments and signal names for the TMS34061 are given in Figure 2-1. A description of each signal is given in Table 2-1.

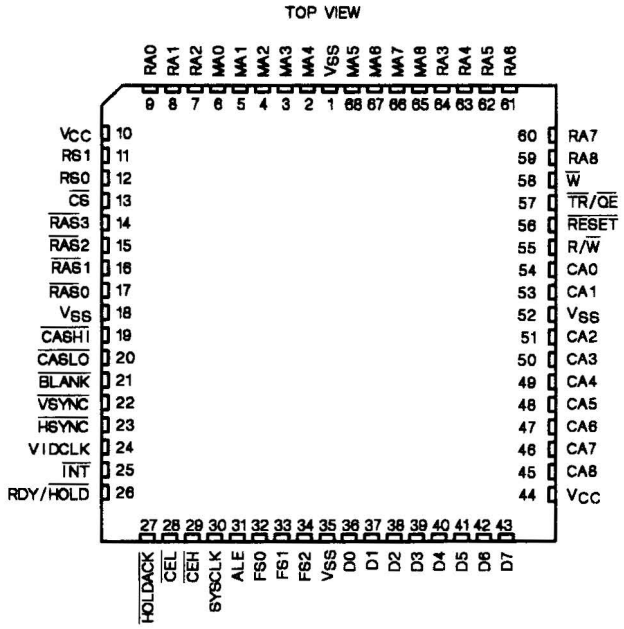


Figure 2-1. TMS34061 Pin Assignments and Signal Names

The TMS34061 comes in a 68-terminal, J-leaded chip carrier plastic (PLCC) package.

Table 2-1. TMS34061 Signal Descriptions

SIGNAL	PIN	I/O	DESCRIPTION
MA8-MA0	65-68, 2-6	O	Memory Address 8-0. The nine memory address outputs are multiplexed address lines designed to interface directly to TMS4161 VRAMs, as well as conventional DRAMs. The TMS34061 multiplexes up to nine row and nine column address bits over these lines. A 256K DRAM that requires nine bits of row and column addresses utilizes all nine outputs. A 64K DRAM requires only eight bits of row and column addresses and therefore utilizes only eight outputs (MA7-MA0). MA0 is the LSB.
RA8-RA0	59-64, 7-9	I	Row Address 8-0. These nine address inputs are mutiplexed to memory address pins MA8-MA0 during row address time when a host-direct memory access cycle is executed. On host-initiated shift-register-transfer cycles, these inputs are multiplexed on MA8-MA0 during column address time. While ALE is high and no internal cycle is taking place, the MA8-MA0 outputs follow the RA8-RA0 inputs, which are latched by the high-to-low transition of ALE. RA0 is the LSB.
CA8-CA0	45-51, 53, 54	I	Column Address 8-0. These nine address inputs are multiplexed to memory address pins MA8-MA0 during column address time when a host-initiated memory cycle is performed. When the host accesses a TMS34061 internal register, the code input on CA6-CA2 determines which register is selected, and the value input on CA1 selects the upper or lower byte of the register. During an X-Y address cycle, the value input on CA4-CA1 determines the manner in which the X-Y address stored within the TMS34061 is incremented or decremented following completion of the cycle. On host-initiated shift-register-transfer cycles, these inputs are multiplexed on MA8-MA0 during column address time. These inputs are latched by the high-to-low transition of ALE. CA0 is the LSB.
RS1, RS0	11, 12	I	Row Address Strobe Selects 1 and 0. During host-direct cycles and shift register transfer cycles, these two pins determine which of the four row address strobes $\overline{\text{RAS}}$3-$\overline{\text{RAS}}$0 is driven active low. RS1-RS0 are latched by the trailing edge of ALE. If extended RAS mode is enabled, these inputs are ignored.
$\overline{\text{CEH}}$	29	I	Column Address Enable High Byte. When active low, this signal enables the $\overline{\text{CASHI}}$ output during a host-direct memory cycle or a host-initiated shift-register-transfer cycle.

Table 2-1. TMS34061 Signal Descriptions (Continued)

SIGNAL	PIN	I/O	DESCRIPTION
$\overline{CEL}$	28	I	Column Address Enable Low Byte. When active low, this signal enables the $\overline{CASLO}$ output during a host-direct memory cycle or a host-initated shift-register-transfer cycle. $\overline{CEL}$ also strobes data into the internal registers during register write cycles and enables register data onto D7-D0 during register read cycles.
ALE	31	I	Address Latch Enable. The high-to-low transition of ALE latches the $\overline{CS}$, RA8-RA0, CA8-CA0, RS1-RS0, and FS2-FS0 inputs, and is interpreted by the TMS34061 as a command from the host to initiate the cycle specified by the values latched at these inputs. ALE must be synchronous with SYSCLK and must meet setup and hold times specified with regard to each low-to-high SYSCLK transition.
R/$\overline{W}$	55	I	Read/Write. During a memory cycle initiated by the host, R/$\overline{W}$ determines the direction of the data transfer (high for read, low for write) and determines the state of the $\overline{W}$ signal output from the TMS34061 to the memory. By appropriately controlling the state of the R/$\overline{W}$ input, the system is allowed to execute the following cycles: read, write, early write, or read-modify write. Similarly, during an access of an internal register by the host, R/$\overline{W}$ indicates whether the data is transferred to or from the register. At the beginning of the register access cycle, R/$\overline{W}$ is required to be valid prior to the high-to-low transition on the $\overline{CEL}$ input.
$\overline{INT}$	25	O	Interrupt Request Low. This output indicates that an interrupt condition previously enabled by the host processor has occurred. $\overline{INT}$ will remain active until the host processor initiates a read of the status register. The TMS34061 can be programmed to generate an interrupt at the start of a particular scan line in each vertical field and also when either a DRAM-refresh error or display-update error has occurred.
D7-D0	43-36	I/O	Data Bus Pins 7-0. The host accesses the internal registers of the TMS34061 through this eight-bit bi-directional data bus. Each register within the TMS34061 that is host accessible must be accessed one byte at a time via D7-D0. D0 is the LSB.
RDY/$\overline{HOLD}$	26	O	Ready or Hold. The operation and timing of RDY/$\overline{HOLD}$ is configured by several control bits contained in Control Register 2 and also by the state of the $\overline{HOLDACK}$ input at the end of reset. With the TMS34061 configured in the Wait or Ready mode, the RDY/$\overline{HOLD}$ pin remains in high impedance until the host requests a memory cycle. In Hold/Hold-Acknowledge mode, this pin is always driven low.

Table 2-1. TMS34061 Signal Descriptions (Continued)

SIGNAL	PIN	I/O	DESCRIPTION
$\overline{\text{HOLDACK}}$	27	I	Hold Acknowledge. When the TMS34061 is configured in Hold/Hold-Acknowledge mode, the host responds to the TMS34061's hold request issuing a handshaking signal by driving $\overline{\text{HOLDACK}}$ low. The TMS34061 can perform an internally requested cycle (display update or DRAM refresh) in this mode only when a handshaking acknowledgment has been received. The $\overline{\text{HOLDACK}}$ pin is also used to dictate active level of the TMS34061's RDY/$\overline{\text{HOLD}}$ pin at system powerup. The input level of the $\overline{\text{HOLDACK}}$ pin just prior to the end of reset determines if the RDY/$\overline{\text{HOLD}}$ output is initially configured as active high or active low. If $\overline{\text{HOLDACK}}$ is high at the end of reset and the TMS34061 remains in Ready or Wait mode, the RDY/$\overline{\text{HOLD}}$ output is active low (a low signifies "ready," while a high signifies "not ready"). The meaning of the high and low levels of RDY/$\overline{\text{HOLD}}$ is reversed if $\overline{\text{HOLDACK}}$ is low at the end of reset. However, if the TMS34061 is in the Hold/Hold-Acknowledge mode, the meaning of the output levels of RDY/$\overline{\text{HOLD}}$ are fixed independent of the $\overline{\text{HOLDACK}}$ level at the end of reset.
$\overline{\text{CS}}$	13	I	Chip Select. This input operates as a master chip select. Before any host-initiated access involving the TMS34061 can begin, $\overline{\text{CS}}$ must be active low. This includes access of both TMS34061 internal registers and the memory system controlled by the TMS34061.
FS2-FS0	34-32	I	Function Select 2-0. The three-bit function select code input on FS2-FS0 indicates the type of cycle requested by the host processor. All cycles initiated by the host begin on the falling edge of ALE.
SYSCLK	30	I	System Clock. SYSCLK is the system clock input used to generate the timing of signals output to the memory and the timing of the $\overline{\text{INT}}$ and the RDY/$\overline{\text{HOLD}}$ signals output to the host. All host interface signals input to the TMS34061 must be synchronous to SYSCLK.
$\overline{\text{RESET}}$	56	I	Reset. An active low $\overline{\text{RESET}}$ places the TMS34061 in a known initial state. While $\overline{\text{RESET}}$ is low, the internal registers are forced to their default values, and all VRAM control outputs are forced to their inactive levels. $\overline{\text{RESET}}$ should be driven low when power is first applied and remain low for at least 1 ms. After $\overline{\text{RESET}}$ is brought inactive high, the host should wait 1 ms before accessing TMS34061 or the memory it controls. This time is required to allow the TMS34061 to perform at least eight RAS-only VRAM (or DRAM) refresh cycles, thus bringing the VRAMs (or DRAMs) up to their current initial state, as described in the specifications for the TMS4161 VRAM and the TMS4164 DRAM. After the required time has elapsed, the registers internal to the TMS34061 should be loaded with the values appropriate to the application.

Table 2-1. TMS34061 Signal Descriptions (Continued)

SIGNAL	PIN	I/O	DESCRIPTION
$\overline{RAS}3$-$\overline{RAS}0$	14-17	O	Row Address Strobe 3-0. These active-low outputs are designed to drive the $\overline{RAS}$ inputs on both the TMS4161 VRAM and conventional DRAMs. During a host-direct memory or shift-register-transfer cycle, $\overline{RAS}3$-$\overline{RAS}0$ are controlled by the RS1-RS0 inputs in default-mode operation. The two-bit code input on RS1-RS0 determines which of the four $\overline{RAS}$ outputs is driven active low during the cycle. Alternately, bits B1-B0 of Control Register 2 can be used to replace the values on RS1-RS0 when the extended RAS mode is selected. Furthermore, the RAS overrides can be set in Control Register 2, forcing the corresponding $\overline{RAS}$ output to be active on host-direct memory and shift-register-transfer cycles and internal X-Y cycles. During a DRAM refresh cycle, all four $\overline{RAS}$ outputs are driven active low in the default mode of operation. If B7 of Control Register 1 is set to 1, only one $\overline{RAS}$ output will be active at one time. In this mode the active $\overline{RAS}$ output is determined by the value in the Display Address register.
$\overline{CASHI}$	19	O	Column Address Strobe High Byte. This active low output is designed to directly drive the $\overline{CAS}$ inputs on both the TMS4161 VRAM and conventional DRAMs. During memory cycles initiated by the host, $\overline{CASHI}$ becomes active only after the $\overline{CEH}$ input is driven active low. In 16-bit systems $\overline{CASHI}$ is typically used to enable a read or write to the high byte (eight MSBs) of the memory data bus. $\overline{CASHI}$ is driven low during internally-requested display-update cycles, and remains inactive during VRAM refresh cycles.
$\overline{CASLO}$	20	O	Column Address Strobe Low Byte. The operation of $\overline{CASLO}$ is similar to that of $\overline{CASHI}$, as described above, except that $\overline{CASLO}$ is enabled by an active low on $\overline{CEL}$ rather than $\overline{CEH}$. In 16-bit systems, $\overline{CASLO}$ is typically used to enable the low byte (eight LSBs) of the memory data bus. $\overline{CASLO}$ is driven active low during internally-requested display-update cycles and remains active high during VRAM refresh cycles.
$\overline{W}$	58	O	Write Control. This signal is used to drive the $\overline{W}$ inputs to both the TMS4161 VRAM and conventional DRAMs. $\overline{W}$ follows the R/$\overline{W}$ pin on host-direct memory cycles. On host-initiated shift-register-transfer cycles, the state of $\overline{W}$ is determined by the FS0 code. During internally-initiated display-update cycles, $\overline{W}$ is driven low if a write is indicated by bit B6 in Control Register 1.

Table 2-1. TMS34061 Signal Descriptions (Concluded)

SIGNAL	PIN	I/O	DESCRIPTION
$\overline{TR}/\overline{QE}$	57	O	Shift Register Transfer and Output Enable. The $\overline{TR}/\overline{QE}$ output can directly drive the $\overline{TR}/\overline{QE}$ inputs on the TMS4161 VRAM. The signals used to enable shift-register transfer cycles and VRAM output buffers during read cycles are multiplexed over this single pin.
$\overline{BLANK}$	21	O	Video Blanking. The $\overline{BLANK}$ output controls the blanking input on a CRT monitor. $\overline{BLANK}$ is driven active low during both horizontal and vertical blanking intervals. This output is TTL-compatible. The entire screen is blanked immediately following reset, and the active portions of the screen are unblanked only after control bit 13 in Control Register 2 is set.
$\overline{HSYNC}$	23	I/O	Horizontal Sync. $\overline{HSYNC}$ generates the horizontal sync pulses used to control a CRT monitor. It operates as an output except when the External Sync mode is enabled. $\overline{HSYNC}$ is driven active low during horizontal sync intervals whose timing is determined by the values programmed in the TMS34061's horizontal timing registers. In External Sync mode, $\overline{HSYNC}$ is an input and an active low on $\overline{HSYNC}$ resets the Horizontal counter register to zero.
$\overline{VSYNC}$	22	I/O	Vertical Sync. $\overline{VSYNC}$ generates the vertical sync pulses used to control a CRT monitor and operates as an output except when the external sync mode is enabled. $\overline{VSYNC}$ is driven active low during vertical sync intervals whose timing is determined by the values programmed in the TMS34061's vertical timing registers. In External Sync mode, $\overline{VSYNC}$ is an input, and an active low on $\overline{VSYNC}$ resets the vertical counter register to zero.
VIDCLK	24	I	Video Clock. The video input clock drives the logic within the TMS34061 chip that is responsible for generating the timing for the sync and blanking signals. VIDCLK also drives the logic responsible for generating internal requests for display-update and VRAM refresh cycles. Typically, VIDCLK is harmonically related to the dot (or pixel) clock used to stream video data from the external shift registers in the memory system to the CRT monitor.
V_{CC}	10, 44		+5 volt supply input.
V_{SS}	1, 18, 35, 52		Ground.

3. Architecture

The TMS34061 consists of ten basic functional blocks (see Figure 3-1):

- Address multiplexer
- Row address latches
- Column address latches
- DRAM refresh counters
- X-Y address registers (internal)
- Status, control, video timing, display update registers, and scan line counter (internal)
- Arbiter
- Memory cycle generator
- CRT control
- Universal host interface and ready logic

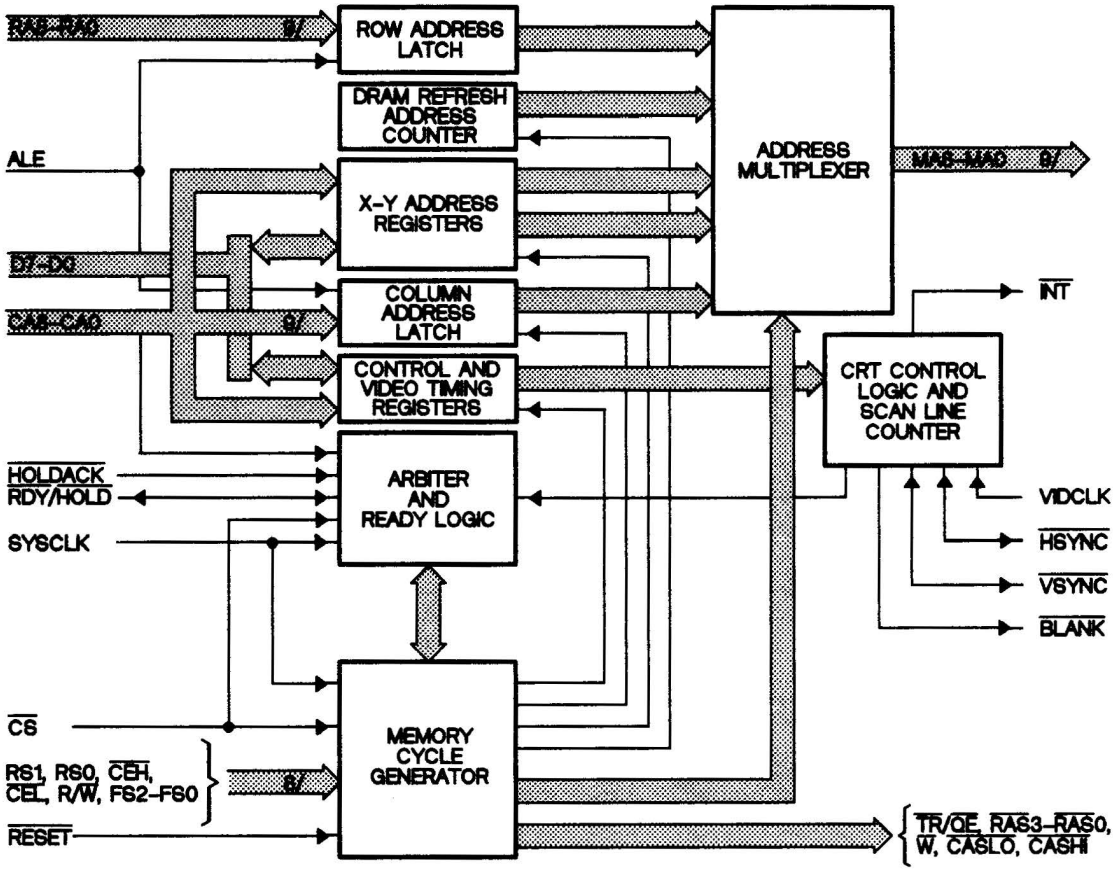


Figure 3-1. TMS34061 Internal Architecture Block Diagram

3.1 Address Multiplexer

The address multiplexer provides the Multiport VRAM array with row and column addresses at the proper times. Its inputs come from the host system, X-Y indirect address register, the display address register, and the DRAM refresh address counter. The specific source of the address is controlled by the arbiter, and the RA or CA portion of the address is controlled by the memory cycle generator. The 9-bit MA address outputs provide 18 multiplexed address signals. The address multiplexer can directly drive inputs for up to 64 TMS4161 Multiport VRAM devices or conventional dynamic RAM devices of up to 256K bits.

3.2 Row and Column Address Latches

The address latches allow the TMS34061 to be used without external latches in systems that multiplex address and data on the same bus. The row latches are transparent, which means that while Address Latch Enable (ALE) is high, the outputs MA0-MA8 follow the address input on RA0-RA8 (assuming an internal cycle is not in progress). The falling edge of ALE internally latches the row and column inputs from the host before being multiplexed to the Memory Address Outputs.

3.3 DRAM Refresh Counters

The TMS34061 has a 9-bit refresh counter which can be programmed to perform a varying number of DRAM refresh cycles per horizontal line. The refresh burst length is determined by bits B14-B12 in Control Register 1. These three bits select from zero to seven refresh cycles per horizontal line. During a refresh cycle, the refresh address counter outputs a 9-bit row address on the MA0-MA8 pins during the row address time.

3.4 Internal Registers

> **Note:**
>
> Section 4 discusses all internal registers in greater detail.

3.4.1 X-Y Address Registers

X-Y addressing capability is especially useful when the linear addressing range of the host is too limited to provide proper access to all pixels on the screen. The contents of the X-Y registers replace the RA0-RA8 and CA0-CA8 inputs as the source for the MA0-MA8 memory address outputs when an X-Y operation is selected. A 4-bit code on the inputs CA4-CA1 of the TMS34061 during X-Y cycles determines how the address is adjusted on completion of the X-Y operation (see Section 4.4 for details). X-Y capability relieves the host from calculating the address of the next pixel to be modified.

X-Y Address Register The X-Y Address Register contains 16 host-accessible bits that eventually become part of the 20-bit X-Y Address Pointer. Various graphic memory configurations can be tailored by the eight combinations of programmable X(LSB) and Y(MSB) boundaries.

X-Y Offset Register

The 16-bit X-Y Offset Register utilizes only 11 bits, B10-B0. Bits B7-B0 define boundaries between the X and Y portions of the X-Y Address Register. The B8-B9 expansion bits determine which of the four row address strobes ($\overline{RAS}$ 3-$\overline{RAS}$ 0) will be active during the X-Y indirect cycle. B11 (row address bit) and B10 (column address bit) are multiplexed on MA8 output.

X-Y Address Pointer

The TMS34061 has a 20-bit X-Y Address Pointer constructed from all 16 bits of the X-Y Address Register and 4 bits of the X-Y Offset Register. Two of the four bits of the X-Y Offset Register control the $\overline{RAS}$ 0-$\overline{RAS}$ 3 outputs. These two bits can be programmed (via B7 of Control Register 2) to be the least significant bits or the most significant bits of the X-Y address. Figure 3-2 and Figure 3-3 show how the 20-bit X-Y Address Pointer Register is constructed from the X-Y Address Register and the X-Y Offset Register and how it is output on the TMS34061's memory bus. Bits B17-B0 of the X-Y Address Pointer effectively form an 18-bit counter, each bit adjusted by the X-Y adjustment codes. Bits B19-B18 are not modified by the X-Y adjustment codes.

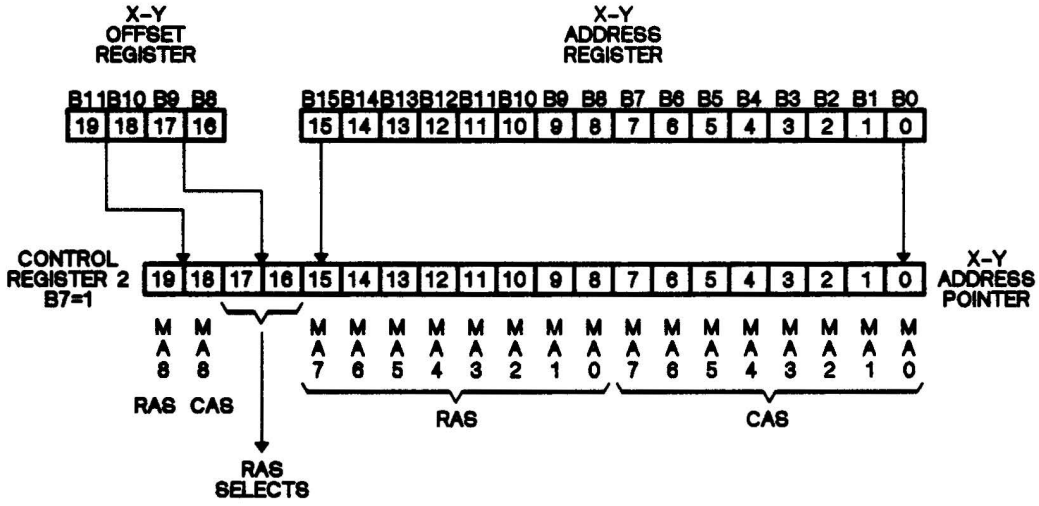


Figure 3-2. X-Y Address Pointer Register Construction

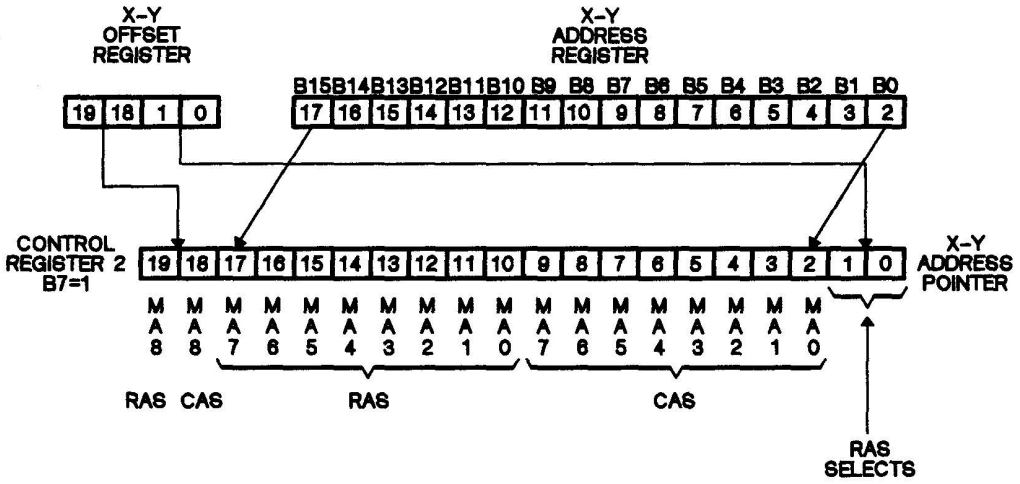


Figure 3-3. X-Y Address Pointer Register Output

3.4.2 Control Registers 1 and 2

The TMS34061 has two 16-bit host-programmable internal Control Registers which dictate TMS34061 operation. Each register may be read from and written to by the host. Video functions governed by the Control Registers include DRAM refresh frequencies, display-update timing cycles, and configuration of video timing functions. Enabling of interrupt requests and some host interface signals are also controlled by these registers.

3.4.3 Status Register

The Status Register is responsible for three conditions within the TMS34061 that may require host interrupts. This three-bit register can be read from but not written to by the host. After reading the register, all bits are reset to zero. Each register bit represents the status of one of three different conditions (logic "high" in the bit indicates the condition has been detected). When detection has occurred, the TMS34061 sends an interrupt request by driving $\overline{INT}$ active low. If interrupts are enabled, two interrupt enable bits in Control Register 1 determine which interrupt sources are able to set the interrupt output.

3.4.4 Video Timing Registers

Horizontal and vertical sync and blanking interval timing is controlled by ten Video Timing registers. Four timing registers along with a horizontal counter generate horizontal timing signals, while four timing registers coupled with a video counter are responsible for the vertical timing signals. Another register, the Vertical Interrupt, sends an interrupt request to the host when a specified scan line is reached. The following registers comprise the Video Timing section:

- Horizontal End Sync
- Horizontal End Blank
- Horizontal Start Blank
- Horizontal Total
- Horizontal Counter
- Vertical End Sync
- Vertical End Blank
- Vertical Start Blank
- Vertical Total
- Vertical Counter
- Vertical Interrupt

3.4.5 Display Update Registers

The video information, which the CRT receives for a specific scan line, is transferred during the horizontal blanking interval immediately preceding that line. This transfer is accomplished by means of a display-update cycle, which the TMS34061 performs automatically. The data is first moved from a specific row in VRAM to a shift register internal to VRAM. The contents of this shift register are output during the horizontal active period. The three display update registers then program the address output during each display update cycle.

Display Address This 12-bit register stores the address of the data to be output on the next display update cycle. Bits 9-2 are output on MA7-MA0 as the row address; MA8 is driven low during this time. Bits 1 and 0 are output on MA7-MA6 as the column address; MA8 and MA5-MA0 are driven low during this time. In the default mode operation, all four $\overline{RAS}$ strobes are active during a display-upeate cycle, and bits B11-B10 have no effect on the $\overline{RAS}$ strobes. When the display-update RAS-mode bit (B7 in Control Register 1) is set to one, the active $\overline{RAS}$ strobe during a display-update cycle is selected by bits B11-B10.

Display Address Update The four-bit Display Address Update Register may be read from or written to by the host. The data stored in this register control how the address is incremented after an update cycle has completed. The four LSBs of the Display Updatae Register are added to the Display Address Register to create the address output for the next display-update cycle.

Display Start This 12-bit register may be read from or written to by the host. The Display Start Register specifies the memory location which is displayed at the upper left of the screen. At the beginning of each vertical blanking

interval, the contents stored in this register are loaded into the Display Address Register.

3.5 Arbiter

The arbiter determines whether the host processor, the video shift-register reload logic, or the dynamic RAM refresh logic can access the memory. Since the display and refresh functions of the TMS34061 normally use less than 6% of the available memory cycles, the arbiter usually grants memory access to the host. When a conflict arises, the arbiter grants priority as follows:

1) Any cycle in progress
2) A display-update cycle (internally granted request)
3) A DRAM refresh cycle that has been delayed for more than ½ horizontal line
4) Any host-requested cycle
5) DRAM-refresh cycle

Three modes can inform the host processor of an internal cycle:

- Synchronous Ready mode
- Wait mode
- Hold/Hold Acknowledge mode

These modes determine the TMS34061's response to the host's request for a memory cycle and to conflicting requests for memory cycles. In all modes of operation, the TMS34061 reports its inability to execute the requested display and refresh cycles by setting bit 2 of the Status Register to one. The TMS34061's host operating mode is selected by B11 and B12 of Control Register 2.

3.5.1 READY/WAIT Operating Modes

Synchronous Ready

In the Synchronous Ready Mode, the TMS34061 responds to each host request for a memory cycle by bringing RDY/$\overline{\text{HOLD}}$ to its inactive level from a high-impedance state. When N SYSCLK transitions occur (where N is the value set by bits B10-B8 of Control Register 2) after $\overline{\text{CASHI}}$ or $\overline{\text{CASLO}}$ becomes active in a host-requested memory cycle, the RDY/$\overline{\text{HOLD}}$ pin switches to the active ready state. Bit B14 in Control Register 2 allows the RDY/$\overline{\text{HOLD}}$ pin to trigger off $\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$ instead of $\overline{\text{CASLO}}$ or $\overline{\text{CASHI}}$. The active level of the RDY/$\overline{\text{HOLD}}$ pin is determined by the state of the $\overline{\text{HOLDACK}}$ pin at the end of Reset. If $\overline{\text{HOLDACK}}$ is low at the end of Reset, the RDY/$\overline{\text{HOLD}}$ pin will be active low when the TMS34061 is not ready. If $\overline{\text{HOLDACK}}$ is high, the RDY/$\overline{\text{HOLD}}$ pin will be active high when the TMS34061 is not ready.

Wait

The Wait Mode is similar to the Ready Mode, except that the READY/$\overline{\text{HOLD}}$ line becomes active WAIT only if the host is requested to wait for the completion of its requested memory cycle. If the host system requests access during an internally-requested cycle, WAIT

immediately goes to the active state. It remains there until the completion of the internal cycle, 1½ SYSCLK periods before $\overline{RAS0}$-$\overline{RAS3}$ goes active during execution of the host requested cycle.

Hold/Hold Acknowledge This mode of operation is intended for use with host systems which do not allow wait states once a memory-access cycle has been initiated. In the Hold/Hold Acknowledge mode, the TMS34061 tests the state of the $\overline{HOLDACK}$ pin to determine if the system is in a hold condition when it is time for a shift register transfer or refresh cycle. If $\overline{HOLDACK}$ is low, the TMS34061 requests a hold state by bringing RDY/$\overline{HOLD}$ from a high-impedance state to its active level. The TMS34061 then waits for the $\overline{HOLDACK}$ input to go low before initiating the shift-register transfer and refresh cycles. Once $\overline{HOLD}$ has been granted, $\overline{HOLDACK}$ can be removed only after $\overline{HOLD}$ has returned to its active high state. It is important to note that in this mode of operation the TMS34061 must be granted the hold state prior to the end of the horizontal blanking interval. If it is not, the error flag in the status register is set and the update cycle may be missed.

3.6 Memory Cycle Generator

The Memory Cycle Generator processes the various memory cycles as requested by the arbiter and provides the external memory array with the $\overline{RAS}$, $\overline{CAS}$, $\overline{TR}/\overline{QE}$, and $\overline{W}$ signals. It controls the multiplexer during all of its cycles so that the address and control line setup and hold requirements are met. The cycles generated by the memory cycle generator are listed below.

- Host-requested cycles
  - Host-direct random access
  - Host-indirect X-Y random access
  - Memory-to-shift register transfer
  - Shift register-to-memory transfer
- Delayed host-requested cycles
- Internally-requested memory-to-shift register transfer
- Internally-requested refresh cycle.

3.7 CRT Control

The TMS34061 generates the $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ signals used to drive a CRT monitor in a bit-mapped graphics system. These signals are synchronous to the Video Input Clock (VIDCLK). $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are programmed through eight host-accessible video timing registers, which are easily configured to accommodate a variety of display resolutions and CRT monitors in either interlaced or non-interlaced modes. Two additional registers, clocked by VIDCLK, maintain the current horizontal and vertical counts. The values in these two counters are compared with the values in the eight video timing registers to determine the limits of the sync

and blanking intervals. The TMS34061 can be configured to accept $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ as inputs allowing synchronization to an external video source.

4. Programmable Registers

This section explains the addressing and programming of the TMS34061's registers.

- Default register values after reset
- CPU interface registers
  - Status Register
  - Control Registers 1 and 2
  - Vertical Interrupt Register
- CRT Control Registers
  - Display-Update Registers
  - Video Timing Registers
- X-Y Address Pointer
  - X-Y Address Register
  - X-Y Offset Register

The TMS34061 contains 18 programmable registers. Each register is nominally 16 bits wide and can be written to and read from by the host processor through an 8-bit data path one byte at a time. Other registers internal to the TMS34061 are inaccessible to the host processor; these are also discussed in this section. The bit-numbering convention to be used for all registers is shown in Figure 4-1.

The host processor accesses the programmable registers within the VSC by means of special read and write cycles. A register-access cycle is selected by setting the function-select input pins FS2-FS0 to one of two 3-bit codes, either 000 or 010. One of 18 registers is selected by the 5-bit register address input on column-address input pins CA6-CA2, as indicated in Figure 4-2. Binary codes 00000 through 10001 are valid register addresses. Codes 10010 through 11111 are reserved. The high or low byte of the register is selected by the value input on CA1. If CA1 is zero, the register low byte is selected; otherwise, the register high byte is selected. In Figure 4-2, the active bits in each 16-bit register location are indicated by the letter "A." The unimplemented bits, indicated as "X," are always read as zeroes.

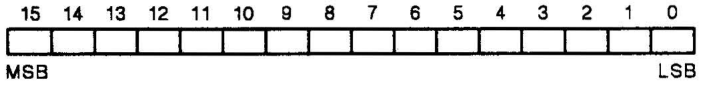
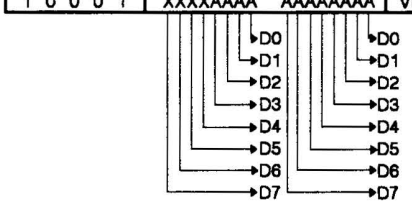


Figure 4-1. Register Bit-Numbering Convention

INPUT PIN VALUES							REGISTER NAME
CA6	CA5	CA4	CA3	CA2	UPPER BYTE (CA1=1)	LOWER BYTE (CA1=0)	
0	0	0	0	0	XXXXAAAA	AAAAAAAA	HORIZONTAL END SYNC
0	0	0	0	1	XXXXAAAA	AAAAAAAA	HORIZONTAL END BLANK
0	0	0	1	0	XXXXAAAA	AAAAAAAA	HORIZONTAL START BLANK
0	0	0	1	1	XXXXAAAA	AAAAAAAA	HORIZONTAL TOTAL
0	0	1	0	0	XXXXAAAA	AAAAAAAA	VERTICAL END SYNC
0	0	1	0	1	XXXXAAAA	AAAAAAAA	VERTICAL END BLANK
0	0	1	1	0	XXXXAAAA	AAAAAAAA	VERTICAL START BLANK
0	0	1	1	1	XXXXAAAA	AAAAAAAA	VERTICAL TOTAL
0	1	0	0	0	XXXXXXXX	XXXXAAAA	DISPLAY UPDATE
0	1	0	0	1	XXXXAAAA	AAAAAAAA	DISPLAY START
0	1	0	1	0	XXXXAAAA	AAAAAAAA	VERTICAL INTERRUPT
0	1	0	1	1	XAAAAAAA	AAAXAAAA	CONTROL REGISTER 1
0	1	1	0	0	XXAAAAAA	AAAAAAAA	CONTROL REGISTER 2
0	1	1	0	1	XXXXXXXX	XXXXXAAA	STATUS REGISTER
0	1	1	1	0	XXXXAAAA	AAAAAAAA	X-Y OFFSET REGISTER
0	1	1	1	1	AAAAAAAA	AAAAAAAA	X-Y ADDRESS REGISTER
1	0	0	0	0	XXXXAAAA	AAAAAAAA	DISPLAY ADDRESS REGISTER
1	0	0	0	1	XXXXAAAA	AAAAAAAA	VERTICAL COUNT REGISTER



NOTE: "A" = ACTIVE REGISTER BIT, "X" = BIT NOT IMPLEMENTED.

Figure 4-2. Programmable Register Address Map

4.1 Default Register Values After Reset

Host-accessible registers are set to the values indicated in Table 4-1 immediately following reset.

B14-B12 of Control Register 1, the Refresh Burst Length bits, are all set to ones immediately after reset. This configures the TMS34061 to the maximum number of DRAM-refresh cycles per horizontal scan line. The video timing registers are also set to non-zero default values. This is necessary because of the manner in which the scheduling of DRAM-refresh cycles is tied to the video timing. The row address output from the VSC during the first DRAM-refresh cycle following reset will be all zeros.

The three wait-state limit bits, B10-B8 of Control Register 2, contain the binary code 110 (decimal 6) immediately following reset. This configures the VSC to insert a delay of six SYSCLK edges into each cycle initiated by the host processor.

Table 4-1. Host-Accessible Registers After Reset

REGISTER NAME	VALUE AFTER RESET			
Horizontal End Sync	xxxx	0000	0001	0000
Horizontal End Blank	xxxx	0000	0010	0000
Horizontal Start Blank	xxxx	0001	1111	0000
Horizontal Total	xxxx	0010	0000	0000
Vertical End Sync	xxxx	0000	0000	0100
Vertical End Blank	xxxx	0000	0001	0000
Vertical Start Blank	xxxx	0000	1111	0000
Vertical Total	xxxx	0001	0000	0000
Display Update Register	xxxx	xxxx	xxxx	0000
Display Start Register	xxxx	0000	0000	0000
Vertical Interrupt	xxxx	0000	0000	0000
Control Register 1	x111	0000	000x	0000
Control Register 2	x000	0110	0000	0000
Status Register	xxxx	xxxx	xxxx	x000
X-Y Offset Register	xxxx	0000	0001	0x00
X-Y Address Register	0000	0000	0000	0000
Display Address Register	xxxx	0000	0000	0000
Vertical Counter	xxxx	0000	0000	0000

Note: Bits indicated as "x" are not implemented and are always read as zeros.

Host-inaccessible registers are set to the values indicated below, immediately following reset.

Table 4-2. Host-Inaccessible Registers After Reset

REGISTER NAME	VALUE AFTER RESET			
Horizontal Counter	xxxx	0000	0000	0000
Refresh Address	xxxx	xxx0	0000	0000
Refresh Burst Counter	xxxx	xxxx	xxxx	x111
Scan Line Counter	xxxx	xxxx	xxxx	0000

Note: Bits indicated as "x" are not implemented.

4.2 CPU Interface Registers

The TMS34061 VSC contains two directly-accessible control registers, a status register, and an interrupt register that are programmed by the host processor to configure the operation of the VSC. The functions controlled by these registers include:

- The behavior of host interface signals
- The timing of display-update cycles
- Enabling of interrupt requests
- Frequency of DRAM-refresh cycles
- Configuration of video timing functions
- Interrupt control

Control Registers 1 and 2 are both 16-bit registers. Both may be read from and written to by the host processor. The functions assigned to the individual bits within these registers are indicated in the following definitions. The bit-numbering convention shown in Figure 4-1 is used. Control Registers 1 and 2 are forced to the default values indicated in Table 4-1 during reset.

4.2.1 Control Register 1

B15	B14–B12	B11	B10	B9	B8	B7	B6	B5	B4	B3–B0
RESERVED 0	REFRESH BURST LENGTH	ERROR INTERRUPT ENABLE	VERTICAL INTERRUPT ENABLE	INTERLACE ENABLE	EXTERNAL SYNC ENABLE	DISPLAY UPDATE RAS MODE	DISPLAY UPDATE DIRECTION	DISPLAY UPDATE INHIBIT	RESERVED 0	LINE COUNT LIMIT

Figure 4-3. Control Register 1

Bits	*Function*
B3-B0	Line Count Limit. The Line Count Limit determines the number of horizontal lines that are counted by the Scan Line Counter before a display-update cycle is granted. The Scan Line Counter repeatedly cycles from zero to the limit value specified in bits B3-B0, incrementing at the end of each horizontal scan line and comparing the count to the value stored in bits B3-B0. When equal, a display-update cycle is granted on that horizontal line during the blanking interval and the Scan Line Counter is zeroed. When the line count limit is set to zero, display-update cycles occur on every scan line.

B3	B2	B1	B0	PERFORM DISPLAY UPDATE ...
0	0	0	0	After each scan line
0	0	0	1	After every other scan line
0	0	1	0	After every 3rd scan line
0	0	1	1	After every 4th scan line
0	1	0	0	After every 5th scan line
0	1	0	1	After every 6th scan line
0	1	1	0	After every 7th scan line
:	:	:	:	:
:	:	:	:	:
1	1	1	1	After every 16th scan line

B4 Reserved - always 0.

B5 Display Update Inhibit.
When B5 is **one**, display-update cycles are inhibited and do not occur. When B5 is **zero**, display-update cycles are enabled. B5 overrides all other display update parameters.

B6 Display Update Direction.
When B6 is **one**, display-update cycles transfer data from the shift register to the memory cell array of each TMS4161 Multiport VRAM. When B6 is **zero**, display-update cycles transfer data from the memory cell array to the shift register.

B7 Display-Update RAS Mode.
When B7 is **zero**, all four row address strobe pins, $\overline{RAS}3$-$\overline{RAS}0$, are active during a display-update cycle. When B7 is **one**, only one of the four strobes is active during a display-update cycle. The active strobe is selected by the value contained in the two MSBs (bits B11-B10) of the Display Address Register.

B8 External Sync Enable.
When B8 is **zero**, the external video sync mode is disabled. This turns the $\overline{HSYNC}$ and $\overline{VSYNC}$ into outputs, and horizontal and vertical sync and vertical timing is generated within the TMS34061. When B8 is one, external sync mode is enabled. The $\overline{HSYNC}$ and $\overline{VSYNC}$ pins are now configured as inputs and the VSC locks on to the externally-generated sync signals.

B9 Interlace Enable.
When B9 is **zero**, the VSC is configured for non-interlaced scan. When B9 is **one**, the VSC is configured for interlaced scan.

B10 Vertical Interrupt Enable.
When B10 is **zero**, the setting of the Vertical Interrupt Flag in the Status Register does not cause an interrupt request to the host processor. When B10 is **one**, the interrupt request is enabled.

B11 Error Interrupt Enable.
When B11 is **zero**, the setting of an error interrupt flag in the Status Register does not cause the TMS34061 to send an interrupt request to the host processor. When B11 is **one**, the setting of either display or refresh error interrupt flag causes an interrupt request.

B14-B12 Refresh Burst Length.
B14-B12 contains a three-bit binary number specifying the number of DRAM-refresh cycles generated per horizontal scan line. If the number is specified as **zero**, no DRAM-refresh cycles occur. The encoding of these bits is indicated below:

B14	B13	B12	REFRESH BURST LENGTH
0	0	0	No DRAM-refresh cycles
0	0	1	1 cycle per scan line
0	1	0	2 cycles per scan line
0	1	1	3 cycles per scan line
1	0	0	4 cycles per scan line
1	0	1	5 cycles per scan line
1	1	0	6 cycles per scan line
1	1	1	7 cycles per scan line

B15 Reserved - always 0.
When read, B15 returns a **zero**.

> **Note:**
>
> When programming the TMS34061 in External Sync Enable mode (B8 in Control Register 1 is set to one), the lower byte of Control Register 1 (bits B7-B0) has logic in this path to prevent the non-host-accessible memory controller timing register from being updated asynchronously. The contents of the lower byte of Control Register 1 are transferred to the memory controller timing register on the Start of Blank interval internal to the TMS34061. Therefore, when external sync is being input, a front porch interval ($\overline{\text{BLANK}}$ output active low before the sync input is active low) is necessary for the lower byte of Control Register 1 to be transferred to the memory controller. The contents of the lower byte of Control Register 1 are updated immediately, but the transfer to the memory controller timing register occurs only during this Start of Blank interval.

4.2.2 Control Register 2

B15	B14	B13	B12–B11	B10–B8	B7	B6	B5–B2	B1–B0
RESERVED 0	RAS/CAS READY	BLANK ENTIRE DISPLAY	RDY/$\overline{\text{HOLD}}$ MODE SELECT	WAIT STATE LIMIT	X-Y ADDR. POINTER RAS MODE	EXTENDED RAS MODE	RAS OVERRIDES	EXTENDED RAS SELECT

Figure 4-4. Control Register 2

Bits	*Function*
B1-B0	Extended RAS Select Bits. When bit B6 of Control Register 2 is **one**, the two-bit value in B1-B0 replaces the value input on the RS1-RS0 inputs during a host-direct or shift-register transfer cycle and determines which of the four RAS outputs is driven active-low during the cycle. The encoding of B1-B0 is as follows:

B1	B0	ACTIVE STROBE
0	0	$\overline{RAS0}$
0	1	$\overline{RAS1}$
1	0	$\overline{RAS2}$
1	1	$\overline{RAS3}$

B5-B2 RAS Overrides.
Each of the four RAS-override bits, B5-B2, is dedicated to one of the four RAS outputs, $\overline{RAS3}$ to $\overline{RAS0}$. When an override bit is set to **one**, the corresponding RAS output is forced to its active-low level during the following four types of cycles:

- Host-direct write,
- X-Y-indirect write,
- Shift-register write,
- Shift-register read cycles.

When an override bit is **zero**, the corresponding RAS output is controlled by other means. Namely, during host-direct write cycles, RS1-RS0 or B1-B0 are used to select one of four row address strobes to be activated, and during X-Y-indirect write cycles, the RAS-select bits from either the two MSBs or the two LSBs of the X-Y Address Pointer are used. In other words, the four RAS-override enables are logically-ORed with the result of the decode of the two designated RAS-select bits. The RAS-override bits never affect host-direct read cycles, X-Y indirect read cycles, or cycles initiated internally by the VSC. The individual RAS-override enables are assigned as follows:

BIT	FUNCTION
B2	Force $\overline{RAS0}$ active
B3	Force $\overline{RAS1}$ active
B4	Force $\overline{RAS2}$ active
B5	Force $\overline{RAS3}$ active

B6 Extended RAS Mode.
When B6 is **zero**, the values input on the RS1-RS0 pins select one of the four RAS outputs during a host-direct or shift-register transfer cycle. When B6 is **one**, the two-bit code in B1-B0 selects one of the strobes.

B7 X-Y Address Pointer RAS Mode.
When B7 is **one**, bits B8-B9 of the X-Y Offset Register become the two MSBs in the X-Y Address Pointer which selects one of the four RAS outputs during a X-Y-indirect cycle. When B7 is **zero**, these two X-Y Offset Register bits become the LSBs which enable one of the four RAS outputs.

B10-B8 Wait State Limit.
The 3-bit code in B10-B8 determines the number of wait states inserted into cycles initiated by the host processor. A wait state is a delay of one-half of a SYSCLK clock period inserted into a cycle to increase its duration. The cycle is delayed by postponing the ready signal to the host processor. B10-B8 are encoded as follows:

B10	B9	B8	INSERT DELAY OF...
0	0	0	0 wait states
0	0	1	1 wait state
0	1	0	2 wait states
0	1	1	3 wait states
1	0	0	4 wait states
1	0	1	5 wait states
1	1	0	6 wait states
1	1	1	7 wait states

B12-B11 RDY/$\overline{\text{HOLD}}$ Mode Select.
The RDY/$\overline{\text{HOLD}}$ output is configured by B12-B11 to operate as a "ready," "wait," or "hold" signal to accommodate the interfacing requirements of a variety of host processors. B12-B11 are encoded as follows:

B12	B11	MODE SELECTED
0	0	Ready signal
0	1	Wait signal
1	0	Hold signal
1	1	Reserved

B13 Screen Enable.
When B13 is **zero**, the $\overline{\text{BLANK}}$ driven output is active-low continuously. When B13 is **one**, the $\overline{\text{BLANK}}$ output is driven low only during horizontal and vertical blanking intervals.

B14 RAS/CAS Ready Enable
When B14 is zero, $\overline{\text{CASLO}}$ or $\overline{\text{CASHI}}$ enables the ready timing. When B14 is a one, $\overline{\text{RAS3}}$-$\overline{\text{RAS0}}$ enables the ready timing.

B15 Reserved - always 0.

4.2.3 Status Register

The Status Register contains three bits, each representing a particular internal condition. A bit value of one indicates presence of the corresponding condition described in Table 4-3. When one of the bits is set and the corresponding interrupt-enable bit in Control Register 1 is set to a one, the TMS34061 sends an interrupt request to the host processor by driving the $\overline{\text{INT}}$ output to its active-low level. The Status Register can be read, but not written to, by the host processor. A read of the Status Register will cause all of the bits to be reset to zero, thereby clearing the interrupt request, if one has been active.

In all modes of operation, the VSC sets an error flag to alert the host processor that it cannot complete an internally-requested cycle. For example, if a display-update cycle requested at the beginning of a horizontal blanking interval is not completed by the time the horizontal blanking interval ends, bit 1 of the Status Register is set to one. If the Error Interrupt Enable bit in Control Register 1 is also one, the VSC sends an interrupt request to the host processor. Similarly, if all DRAM-refresh cycles scheduled to occur during a scan line have not been completed by the start of the next horizontal blanking interval, bit 2 of the Status Register is set to one. Again, this causes the TMS34061 to send an interrupt request to the host processor if the

Error Interrupt Enable bit is one. When the host processor reads the Status Register, all three bits are cleared, thereby removing the interrupt request.

Table 4-3. Status Register Bit Definitions

BIT	FUNCTION
B0	Vertical Interrupt. A one in this bit indicates that the vertical interrupt condition has occurred.
B1	Display Error. A one in this bit Indicates that the TMS34061 was unable to perform a display-update cycle requested during the horizontal blanking interval.
B2	Refresh Error. A one in this bit indicates that the TMS34061 was unable execute the designated number of cycles before the beginning of the next horizontal blanking interval.

4.2.4 Vertical Interrupt Register

The contents of the 12-bit Vertical Interrupt Register are compared to the Vertical Counter. If these are equal and the vertical interrupt is enabled, then at the end of the current scan line the VSC sends an interrupt request to the host processor by driving the $\overline{INT}$ pin active low. The high-to-low transition of $\overline{INT}$ occurs one to two SYSCLK periods from the start of horizontal sync. $\overline{INT}$ then remains active low until the host processor responds by reading the Status Register. An active $\overline{RESET}$ signal forces the Vertical Interrupt Register to >000. The contents of this register may be read or written to by the host processor.

4.3 CRT Control Registers

4.3.1 Display-Update Registers

The TMS34061 is designed to work with the TMS4161 Multiport VRAM, which contains both a 256-by-256 memory cell array and a 256-bit shift register whose contents are shifted out serially and transmitted to the CRT monitor. A typical bit-mapped graphics system may contain 16, 32, or more TMS4161 VRAMs. The video data to be transmitted to the CRT monitor during an active scan line is transferred from a selected row within the memory cell array to the shift register during the horizontal blanking interval preceding the scan line. The transfer (by means of a display-update cycle) is performed automatically by the VSC. The address output during each display-update cycle is programmed through the three Display-Update Registers shown in Figure 4-5, Figure 4-6, and Figure 4-7: Display Address, Display Address Update, and Display Address Start Registers. A fourth register, the Scan Line Counter, is used to count the number of horizontal scan lines output between successive display-update cycles.

Display Address. The 12-bit Display Address Register contains the address to be output during the next automatic display-update cycle. **Bits B9-B2** are output on MA7-MA0 as the row address, and MA8 is driven to zero in this interval. **Bits B1-B0** are output on MA7-MA6 as the two MSBs of the column address; MA8 and MA5-MA0 are 0 in this interval. **Bits B1-B0** select one of four tap points in the shift register of the TMS4161 VRAM. **Bits B11-B10** select one of the four row address strobes in the event that the Display Update RAS Mode bit (B7 in Control Register 1) is one. The Display Address Register can be read from or written to by the host processor.

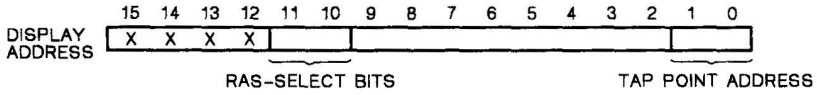


Figure 4-5. Display Address Register

The host can access this register in two ways:

- By performing multiple consecutive read cycles to guarantee the integrity of the returned data.
- Through the use of vertical interrupt. After a vertical interrupt occurs the host should wait for a period equal to the duration of one horizontal sync interval plus the back porch interval before attempting any access. At this time the host has the entire active scan line interval for either read or write accesses.

Display Address Update. This 4-bit register may be read and written to by the host. It contains the value by which the display address is incremented. Valid increment values are 0, 1, 2, 4, and 8.

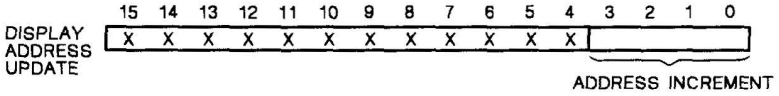


Figure 4-6. Display Address Update Register

Non-Interlaced Mode Operation. Following completion of an automatic display-update cycle requested at the beginning of horizontal blanking, the contents of the Display Update Register are added to the four LSBs of the Display Address Register. This generates the address to be output during the next display-update cycle.

Interlaced Mode Operation. In interlaced mode operation, the TMS34061 becomes a field machine. Therefore, at the start of the vertical blanking interval preceding each odd field, one-half the value contained in the Display Address Update register is added to the Display Address register, following its being loaded from the Display Start register. This causes the even lines to fall directly in between the odd lines. Since in interlaced mode every other scan line is displayed in the active field, the value placed in the Display Update register must be doubled in comparison with the value stored in this register in non-interlaced mode to generate the same effective display output from the memory frame buffer.

Display Start. The contents of the 12-bit Display Start Register are loaded into the Display Address Register at the beginning of each vertical blanking interval. The Display Start Register specifies the location in memory to be displayed at the upper left of the screen. The Display Start Register may be both read and written to by the host.

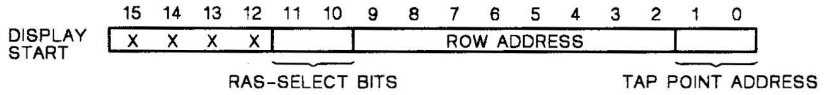


Figure 4-7. Display Start Register

Scan Line Counter. The Scan Line Counter is a 4-bit register, inaccessible to the host processor, that is used in conjunction with the display control registers to determine the manner in which video data output to the CRT monitor is updated between active horizontal scan lines. The Scan Line Counter is incremented at the end of each scan line until it reaches the count limit specified in bits 3-0 of Control Register 1, at which point it is reset to zero and begins counting up again. The line count is forced to zero at the beginning of each vertical scan.

A display-update cycle may be programmed not to occur during the horizontal blanking interval preceding an active scan line. The 4-bit Scan Line Counter is used to control the number of active horizontal scan lines output to the CRT monitor between successive display-update cycles. For example, a TMS34061-based graphics memory may be constructed such that a single display-update cycle loads the shift registers with sufficient video data for three complete scan lines. Only after this data has been output to the display need the shift registers be loaded with new data from the memory.

For the example above, the line count limit in B3-B0 of Control Register 1 should be loaded with the value 2. This causes the Scan Line Counter to increment at the end of each scan line, cycling through the values 0, 1, 2, 0, ... With the VSC configured in this manner, a display-update cycle is performed prior to each scan line for which the count is 0. No display-update cycle is performed prior to those scan lines for which the count is 1 or 2.

4.3.2 Video Timing Registers

Timing for the horizontal sync and blanking intervals is generated using the four horizontal video timing registers, in conjunction with the Horizontal Counter. Similarly, the four vertical timing registers are used in conjunction with the Vertical Counter to generate the vertical sync and blanking signals. The operation of the individual video timing registers is explained in detail below.

Horizontal Counter. The 12-bit Horizontal Counter increments on each VIDCLK falling edge and serves as the timing base for determining the limits of the horizontal sync and blanking intervals. The value of the Horizontal Counter is compared to the value of the four horizontal timing registers in order to generate the signals output on $\overline{\text{HSYNC}}$ and $\overline{\text{BLANK}}$.

When the Horizontal Counter reaches the value in the Horizontal Total Register, the Horizontal Counter resets to zero and begins counting again. When the TMS34061 is configured in external sync mode, $\overline{\text{HSYNC}}$ is an input, and the Horizontal Counter is forced to zero after a delay from the falling edge of $\overline{\text{HSYNC}}$. An active $\overline{\text{RESET}}$ signal forces the Horizontal Counter to zero. This register is not accessible to the host processor.

Horizontal End Sync. The contents of the 12-bit Horizontal End Sync Register are compared to the Horizontal Counter to identify the end of the horizontal sync interval. If the comparison shows they are equal, the VSC drives its $\overline{\text{HSYNC}}$ output pin inactive-high. The minimum Horizontal End Sync value is one, and the maximum value is one less than the value in the Horizontal End Blank Register. The value of the Horizontal End Sync Register should be set to one less than the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse. An active $\overline{\text{RESET}}$ signal forces the Horizontal End Sync Register to >010. The contents of this register may be read from or written to by the host processor.

Horizontal End Blank. The contents of the 12-bit Horizontal End Blank Register are compared to the Horizontal Counter to identify the end of the horizontal blanking interval. If the comparison shows they are equal, the TMS34061 drives its $\overline{\text{BLANK}}$ output inactive-high on the next rising edge of VIDCLK (unless vertical blanking is active). The minimum Horizontal End Blank Register value is one greater than the value of Horizontal End Sync Register, and the maximum value is one less than the value in the Horizontal Start Blank Register. An active $\overline{\text{RESET}}$ signal forces the Horizontal End Blank Register to >020. The contents of this register may be read or written to by the host processor.

Horizontal Start Blank. The contents of the 12-bit Horizontal Start Blank Register are compared to the Horizontal Counter to identify the start of the horizontal blanking interval. If the comparison shows they are equal, the VSC drives its $\overline{\text{BLANK}}$ output pin active-low (unless it has already been forced to this state by active vertical blanking). The minimum Horizontal Start Blank value is one plus one-half the Horizontal Total, and the maximum value is one less than the value in the Horizontal Total Register. The contents of the Horizontal Start Blank Register should be set to one less than the number of VIDCLK periods corresponding to the interval from the beginning of horizontal sync to the beginning of horizontal blanking. An active $\overline{\text{RESET}}$ signal forces the Horizontal Start Blank Register to >1F0. The contents of this register may be read from or written to by the host processor.

> **Note:**
>
> If HTOTAL-HSBLANK is equal to 1, the VIDCLK frequency must be less than 4 MHz. If HTOTAL-HSBLANK is equal to or greater than 2, the VIDCLK frequency can be up to a maximum of 6.45 MHz.

Horizontal Total. The contents of the 12-bit Horizontal Total Register are compared to the Horizontal Counter to identify the start of the horizontal sync interval. If the comparison shows they are equal, the TMS34061 resets the Horizontal Counter to zero and drives its $\overline{\text{HSYNC}}$ output active-low on the next rising edge of VIDCLK. The contents of the Horizontal Total Register should be set to one less than the number of VIDCLK periods contained in a horizontal scan line. The maximum Horizontal Total Register value is >FFF. For proper interlaced-mode operation, this register should be set to an even number (i.e., LSB = 0). An active $\overline{\text{RESET}}$ signal

forces the Horizontal Total Register to >200. The contents of this register may be read from or written to by the host processor.

Vertical Counter. The 12-bit Vertical Counter Register counts the horizontal lines in the video display and serves as the timing base for determining the limits of the vertical sync and blanking intervals. The contents of the Vertical Counter are compared with the values in the vertical timing registers to mark off the vertical sync and blanking intervals. The count is incremented by one at the beginning of each horizontal sync interval with one exception: during the vertical front porch and sync intervals of an odd field in an interlaced frame, the increment of the vertical counter occurs at midpoint where the count in the horizontal counter is equal to one-half the value in the Horizontal Total Register. The Vertical Counter Register is reset to zero upon reaching the value in the Vertical Total Register or on the next falling edge of VIDCLK after a high-to-low transition on the $\overline{\text{VSYNC}}$ input while the VSC is configured in external sync mode. An active $\overline{\text{RESET}}$ signal forces the Vertical Counter Register to zero. This register may be read by the host processor during the intervals between increments but may not be written to. Multiple read cycles are recommended for reading this register. Two consecutive reads returning the same data information indicate the host access is in an interval between increments.

Vertical End Sync. The contents of the 12-bit Vertical End Sync Register are compared to the Vertical Counter to identify the end of the vertical sync interval. If the comparison shows they are equal, the TMS34061 drives its $\overline{\text{VSYNC}}$ output inactive-high. The Vertical End Sync value should be set to one less than the number of horizontal scan lines corresponding to the duration of active $\overline{\text{VSYNC}}$. The minimum vertical end sync value is one less than the value in the Vertical End Blank Register. An active $\overline{\text{RESET}}$ signal forces the Vertical End Sync Register to >004. The contents of this register may be read from or written to by the host processor.

Vertical End blank. The contents of the 12-bit Vertical End Blank Register are compared to the Vertical Counter to identify the end of the vertical blanking interval. The minimum vertical end blank value is one greater than the value of vertical end sync, and the maximum value is one less than the value in the Vertical Start Blank Register. The vertical end blank value is one less than the number of horizontal scan lines corresponding to the interval from the start of vertical sync to the end of vertical blanking. An active $\overline{\text{RESET}}$ signal forces the Vertical End Blank Register to >010. The contents of this register may be read from or written to by the host processor.

Vertical Start Blank. The contents of the 12-bit Vertical Start Blank Register are compared to the Vertical Counter to identify the start of the vertical blanking interval. The minimum Vertical start blank value is one plus the vertical end blank value. The contents of the Vertical Start Blank Register will be one less than the number of horizontal scan lines corresponding to the interval from the beginning of vertical sync to the beginning of vertical blanking. An active $\overline{\text{RESET}}$ signal forces the Vertical Start Blank Register to >0F0. The contents of this register may be read from or written to by the host processor.

Vertical Total. The contents of the 12-bit Vertical Total Register are compared to the Vertical Counter to identify the start of the vertical sync interval. If the comparison shows they are equal, the TMS34061 resets the Vertical Counter to zero and drives its $\overline{\text{VSYNC}}$ output active-low on the next rising edge of VIDCLK. The maximum vertical total value is >FFF. In non-interlaced mode the actual contents of the Vertical Total Register should be set to one less than the number of horizontal scan lines corresponding to the duration of the vertical interval. In interlaced mode, the Vertical Total Register should be an even number that is the vertical total for two

fields minus one, then divided by two. Each field has the number of lines in the Vertical Total Register plus one half line. For example, if 525 lines are desired for interlaced mode, the Vertical Total should be set to (>525-1)/2, or >106 (262 decimal). This will result in a display of 262½ horizontal lines per field. An active $\overline{\text{RESET}}$ signal forces the Vertical Total Register to >100. The contents of this register can be read or written to by the host processor.

4.4 X-Y Addressing

X-Y addressing is particularly useful in applications in which the linear addressing range of the host processor is too limited to provide easy access to all pixels within the active display area. A memory read or write cycle that utilizes the contents of the X-Y Address Pointer for the memory address is called an X-Y-indirect cycle.

During an X-Y-indirect cycle, the host processor accesses a word in memory indirectly through a 20-bit X-Y Address Pointer stored within the TMS34061. This pointer represents the concatenation of the X and Y coordinates of a word (containing one or more pixels) on the screen. The X coordinate forms the LSBs of the address and the Y coordinate forms the MSBs of the word address. The location of the boundary between the X and Y coordinates of the address is programmable. X increases moving from left to right on the screen, and Y increases moving from top to bottom.

The X and Y displacements at the origin, located in the upper left corner of the screen, are both zero only in the special case in which the pixel displayed in the upper left corner of the screen resides in the word located at memory address zero. In manipulating X-Y addresses through the VSC, software must compensate for a non-zero offset of the upper left corner of the screen from the start of memory.

During an X-Y-indirect cycle, the contents of the X-Y Address Pointer are used in place of the row and column addresses supplied on the RA8-RA0 and CA8-CA0 input pins. The 4-bit code input on CA4-CA1 during an X-Y-indirect cycle determines the manner in which the contents of the X-Y Address Register are updated following completion of the X-Y-indirect cycle, as indicated in Table 4-4. Table 4-4 defines the X-Y adjustment codes through which the X and Y coordinates of the address can be incremented, decremented, or cleared independently. For example, by incrementing Y and clearing X, the X-Y address is updated to point to the leftmost word in the next horizontal scan line. (This assumes that an X value of zero indicates a location on the left edge of the screen, which is a likely case.)

Following completion of each X-Y indirect cycle, the address adjustment specified in Table 4-4 is performed automatically by special hardware contained in the VSC. This mechanism permits convenient access to an arbitrary sequence of adjacent pixels without incurring the overhead of having to load new values into the X-Y Address Pointer prior to each access. As a result, the VSC is capable of performing incremental graphics operations such as line drawing, polygon filling, and custom-character generation at hardware-assisted speeds.

Table 4-4. X-Y Adjustment Codes

INPUT PINS CA4	CA3	CA2	CA1	X-Y ADJUST FUNCTION	
0	0	0	0	No adjustment	
0	0	0	1	Increment X	
0	0	1	0	Decrement X	
0	0	1	1	Clear X	
0	1	0	0		Increment Y
0	1	0	1	Increment X	Increment Y
0	1	1	0	Decrement X	Increment Y
0	1	1	1	Clear X	Increment Y
1	0	0	0		Decrement Y
1	0	0	1	Increment X	Decrement Y
1	0	1	0	Decrement X	Decrement Y
1	0	1	1	Clear X	Decrement Y
1	1	0	0		Clear Y
1	1	0	1	Increment X	Clear Y
1	1	1	0	Decrement X	Clear Y
1	1	1	1	Clear X	Clear Y

4.5 X-Y Address Pointer

The X-Y Address Pointer can be conceptually viewed as a 20-bit pointer comprised of two parts. The first part consists of four host-accessible bits stored in the X-Y Offset Register. Two of these bits, B11-B10, are driven out on the MA8 output on X-Y cycles. These two bits are not affected by the X-Y adjustment code input on CA4-CA1. These bits are of little use when using 64K and 256K VRAMs because those devices do not use this address input; therefore, the 18 remaining bits comprise the workable X-Y Address Pointer for 64K and 256K VRAMs. The other two bits, B9-B8, from the X-Y Offset Register control the $\overline{RAS}3$-$\overline{RAS}0$ selects and can be used as most significant bits or least significant bits, depending on how bit B7 of Control Register 2 is set.

The second part of the X-Y Address Pointer consists of the 16-bit X-Y Address Register. Figure 4-8 and Figure 4-9 show how these two registers are concatenated to form the 20-bit X-Y Pointer Register and how they drive the corresponding MA8-MA0 and $\overline{RAS}3$-$\overline{RAS}0$ outputs of the TMS34061.

When B7 of Control Register 2 is a logical one, the RAS select bits B9-B8 are the most significant bits of the 18-bit effective X-Y Address Pointer. When B7 of the Control Register is a logical zero, the RAS select bits are the least significant bits of the 18-bit effective X-Y Address Pointer. These two bits and the X-Y Address Register form the 18-bit portion of the 20-bit X-Y Address Pointer, which is affected by the X-Y Adjustment code. These 18 bits in the X-Y Address Pointer are linked such that carries or borrows from the MSB of the X coordinates ripple into the LSB of the Y coordinate only when the Y coordinate is not itself being explicitly adjusted on that X-Y operation. Upon reset, the state of B7 in Control Register 2 defaults to zero. The two configurations if the X-Y Address Pointer are illustrated in Figure 4-8 and Figure 4-9.

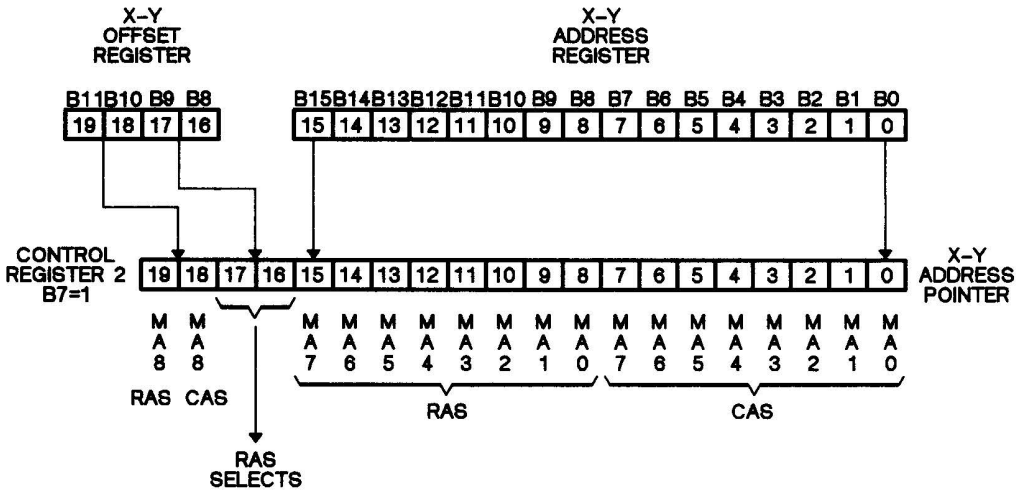


Figure 4-8. X-Y Address Pointer RAS Selects as MSBs

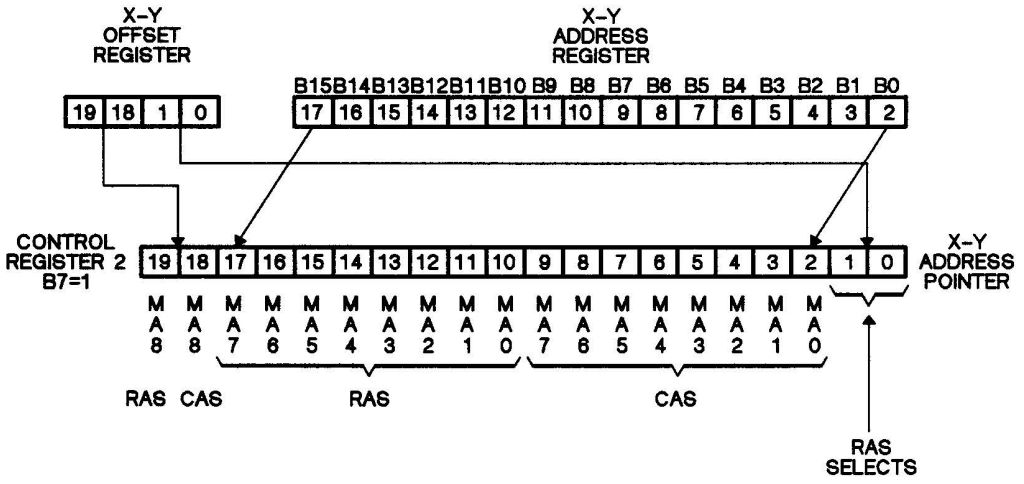


Figure 4-9. X-Y Address Pointer RAS Selects as LSBs

A write to either the X or Y portions of the X-Y Address Register will transfer the contents of bits B9-B8 of the X-Y Offset Register to either the two LSBs of the X coordinate or the two MSBs of the Y coordinate of the X-Y Address Pointer, respectively, regardless of the state of B7 in the Control Register 2. A read to the X-Y Offset Register will always return the current value of the enabled X or Y expansion bits in data bits D1-D0 but not the value stored in B9-B8. This is illustrated in Figure 4-10.

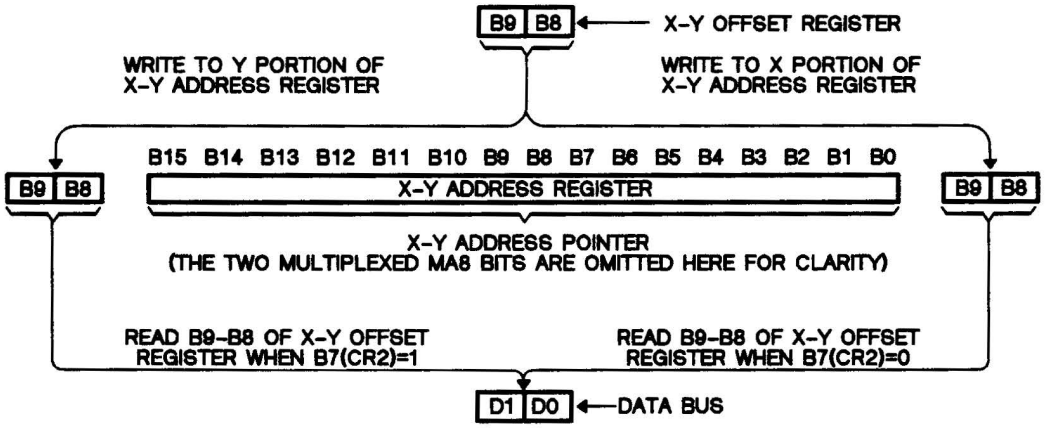


Figure 4-10. X-Y Address Pointer RAS-Select Bits Configuration

To insure proper operation, the X-Y Offset Register should always be loaded prior to loading the X-Y Address Register to allow the two expansion bits to be loaded correctly. These expansion bits will be used to determine which one of the four row address strobes, $\overline{RAS3}$ to $\overline{RAS0}$, is active during an X-Y-indirect cycle. The encoding of these bits is indicated in Table 4-5.

Table 4-5. Decoding of RAS-Select Bits In X-Y Offset Register

B9	B8	ACTIVE STROBE
0	0	$\overline{RAS0}$
0	1	$\overline{RAS1}$
1	0	$\overline{RAS2}$
1	1	$\overline{RAS3}$

4.5.1 X-Y Address Register

The X-Y Address Register contains 16 host-accessible bits that become part of the 20-bit X-Y Address Pointer. The boundary between the X and Y portions in this register is programmable to accommodate the needs of various graphics memory configurations. The X portion occupies from two to nine LSBs of the register. The remaining bits form part of the Y portion. The eight possible boundary conditions between the X and Y portions of this register are shown in Figure 4-11. Case 7 is the most useful for the majority of applications.

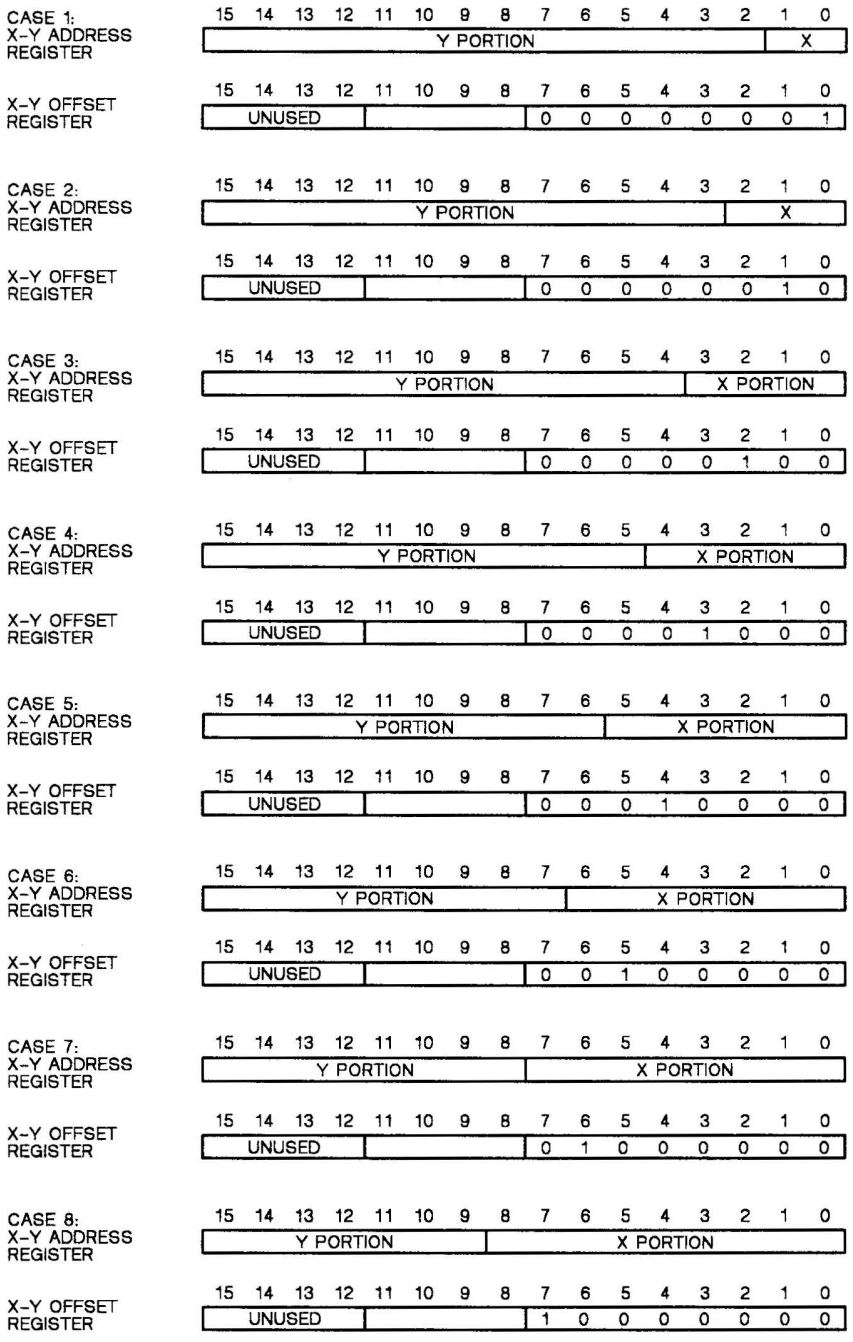
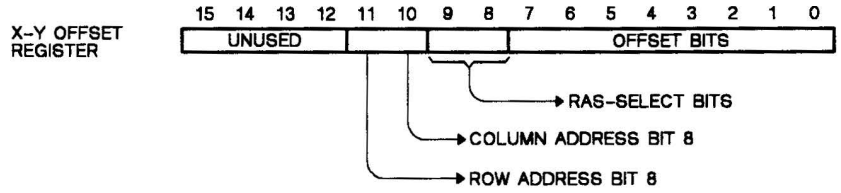


Figure 4-11. X-Y Address Register Bit Definition

4.5.2 X-Y Offset Register

The X-Y Offset Register, shown in Figure 4-12, defines the boundary between the X and Y portions of the X-Y Address Register and contains the initial value of the two RAS-select bits and the two independent bits for MA8, the multiplexed address bit. The eight LSBs of the X-Y Offset Register, B7-B0, specify the boundary between the X and Y portions of the address contained within the X-Y Address Register, as indicated in Figure 4-11.



Note: Only one of the offset bits must always be set.

Figure 4-12. X-Y Offset Register Bit Definitions

Bits B9-B8 of the X-Y Offset Register store the initial values that are loaded into the expansion bits of the X-Y Address Pointer during a host-initiated write cycle to either the X or Y portions of the X-Y Address Register. These two bits are not affected by the adjustment code input on the CA4-CA1 during an X-Y-indirect cycle. Only the transferred expansion bits in the X-Y Address Pointer are changed accordingly. A read of the X-Y Offset Register returns the current value of the expansion bits of the X-Y Address Pointer instead of the initial value of bits B9-B8 of the X-Y Offset Register (see Figure 4-10).

X-Y Offset Register bit B11 is output on MA8 during the row address time, and bit B10 is output on MA8 during the column address time. These two bits are also unaffected by increments or decrements of the X-Y address pointer. Any bit in the X-Y Offset Register indicated as "unused" in Figure 4-12 is read as a zero.

4.5.3 Mechanics of X-Y Addressing

The host processor initiates an X-Y-indirect cycle by setting the FS2-FS0 pin inputs to the function code 001. The memory is then either read or written, as specified by the R/$\overline{W}$ line. The contents of the X-Y Address Pointer can be adjusted after each X-Y-indirect cycle to point to the adjacent word to be accessed during the next X-Y-indirect cycle.

Fifteen different adjustments are available for the X-Y Address Pointer. These adjustments are selected by inputs to CA4-CA1 during an X-Y-indirect cycle, as specified in Table 4-4. The specified adjustment occurs following completion of the cycle, in anticipation of the next X-Y-indirect cycle.

The X-Y Address Pointer points to a word containing one or more pixels, where the number of pixels is determined by the width of the host processor's data path and the number of bits per pixel. The boundary between the X and Y portions of the address is programmable to accommodate a variety of memory configurations. During an X-Y access of the video memory, the VSC uses the address contained in the X-Y Address Pointer in place of the address applied externally at the RA8-RA0 and CA8-CA0 inputs. The eight MSBs of the 16 bits contained in the X-Y Address Register are output on MA7-MA0 as the row address, and the eight LSBs are output

on MA7-MA0 as the column address. The bits B11-B10 of the X-Y Offset Register are also independently multiplexed on MA8 as row and column addresses. The two RAS-select bits, not accessible to the host, are used in place of the RS1-RS0 inputs to determine which of the four row address strobes, $\overline{RAS}$3-$\overline{RAS}$0, will become active during the cycle.

X-Y addressing is flexible in allowing the programmer to customize the X and Y screen dimensions to his application. As indicated in Figure 4-11, the X portion of the address can occupy the lower two to nine bits of the X-Y Address Register, while the Y portion occupies the remainder of the X-Y Address Register. The $\overline{RAS}$ select bits are concatenated to the either X or Y portions according to the state of bit B7 of the Control Register 2.

8.1 Calculating Video Timing

by Jeff Bond

The TMS34061's internal registers must be programmed with values that are dependent on screen format and monitor characteristics.

The dot clock rate, which is the undivided crystal frequency, is applied to the high speed shift register which transfers one pixel at a time to the CRT (see Figure 8-1). After passing through the High Speed Control Logic, this clock is also applied to the TMS34061 in a divided form called VIDCLK. Because dot clock frequencies can exceed 130 MHz, the dot clock must be divided before being applied to the TMS34061, as per the TMS34061 timing specifications. The function of the High Speed Logic in Figure 8-1 is to condition clocks that control the TMS34061, video memories, and the high-speed shift registers.

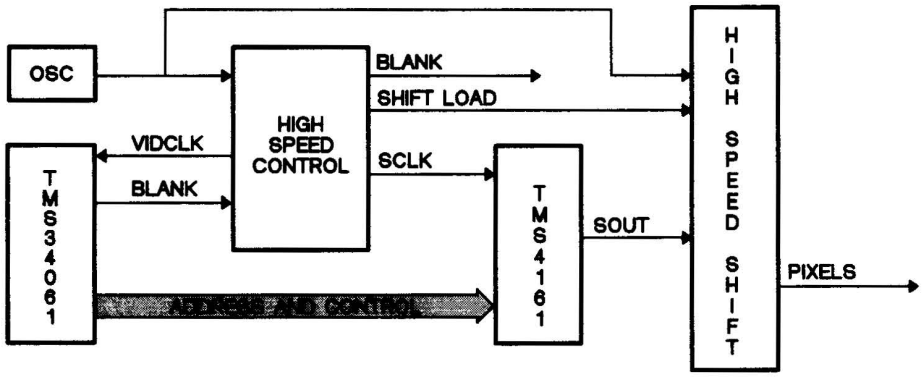


Figure 8-1. TMS34061 High Speed Logic

The first step in designing the video system is to determine the screen format. Display resolutions can range from 262 lines for home TV to about 500 lines for a typical business system to 1000 or more lines in a CAD/CAM monitor. For 80 characters across the screen using a 7 × 9 font, at least 640 pixels are required. If two pixels are desired between each character, a 720-pixel resolution might be used.

Each horizontal line sweeps the electron beam in the CRT from the left margin of the screen to the right, then returns the beam at an accelerated rate to the left. The scan to the right is called the raster line (active region). The return path is known as the horizontal retrace (blanking region). During the active period, the video data is shifted out of the Multiport VRAM through the high-speed shift registers to the CRT. During the blanking period, the TMS34061 loads the internal shift registers of the Multiport VRAM with the next scan line of video data. The horizontal scan rate is comprised of the active time plus the blanked time.

Each vertical scan line sweeps the electron beam of the CRT to the bottom of the screen, then returns to the top at an accelerated rate. During the active period the data is displayed, and during the blanked period the retrace takes place. The active period combined with the blanked period comprise the vertical frame rate. Common broadcast frame rates are 60 Hz (NTSC) and 50 Hz (PAL), while a high resolution monitor may use 60 Hz (non-interlaced) or 30 Hz (interlaced).

Interlacing is a technique used to eliminate screen flicker. In an interlaced display, the odd lines (1, 3, 5, 7, etc.) are scanned first. The beam then returns to the top

of the screen and scans the even lines (0, 2, 4, 6, etc.). The interlaced lines tend to merge and the screen appears to be free of any flicker. The scan rate appears to be twice as fast as it actually is. One completed scan is referred to as a field, and two field scans comprise a frame. Interlacing reduces by half the bandwidth needed to shift the data to the screen; doubling the amount of data which can be displayed without increasing bandwidth.

For an example, a resolution of 640 x 480 pixels with 16 colors will be used.

A monitor must now be selected that supports the required format. The monitor specification gives the required blanking time before sync (front porch - Fp), the required sync width, and blanking time before the next active line (back porch - Bp).

tHb = tHFp + tHs + tHBp	Hb = Horizontal blanking
tHorz = tHact + tHb	HFp = Horizontal front porch
fHorz = 1 / tHorz	Hact = Horizontal active
	HBp = Horizontal back porch
	Hs = Horizontal sync

The monitor specification also gives the requirements for the vertical front porch (tVFp), vertical sync (tVs), vertical back porch (tVBp), and vertical blanking (tVb).

tVb = tVFp + tVs + tVBp	Vb = Vertical blanking
tVert = tVact + tVb	VFp = Vertical front porch
fVert = 1 / tVert	Vact = Vertical active
	VBp = Vertical back porch
	Vs = Vertical sync

Table 8-1. Monitor Specifications

fHorz	= 31.5 kHz
Hb	= 8 µs
HFp	= 2 µs
Hs	= 2.5 µs
HBp	= 3.5 µs
Hact	= 23.75 µs
fVert	= 60 Hz
Vb	= 1 ms
VFp	= 2 Horizontal lines
Vs	= 0.2 ms
Vact	= 15.75 ms

8.1.1 Video Timing Calculation Procedures

1) Calculate the number of horizontal active units (Hact) for each shift register load. In this example the horizontal resolution is 640 pixels. The high-speed shift register performs a load every eight pixels, which yields a total of 80 high-speed shift register loads during the active time of every line.

Hact = # horz pixels / clk divider
Hact = 640 / 8
Hact = 80 units

2) Calculate the time for each horizontal line, which is a requirement of the monitor specification. A nominal value and an acceptable deviation are given in the specification. This nominal value is used for calculations and then later verified to see if that value is within the acceptable limits.

tHorz = 1 / fHorz
tHorz = 1 / 31.5 kHz
tHorz = 31.75 µs

3) Calculate the active display time for each horizontal line. The active time is the total horizontal scan time minus the blanking time given in the monitor specifications.

tHact = tHorz - tHb
tHact = 31.75 µs - 8 µs
tHact = 23.75 µs

4) Calculate memory shift clock time (tLd). As shown below, tLd equals horizontal active time divided by the number of horizontal units. This will be used to determine the memory shift clock (SCLK) frequency and the TMS34061 (VIDCLK) frequency.

tLd = tHact / Hact
tLd = 23.75 µs / 80
tLd = 296.875 ns

5) Calculate the clock frequency (fVSC) to the TMS34061 (VIDCLK). As shown below, fVSC equals one divided by the shift-register reload period calculated in step 4. This number must be compared to the maximum clock frequency given in the TMS34061 specification. If this frequency is greater than the maximum VSC VIDCLK specification, a larger dot clock divider must be used.

fVSC = 1 / tLd
fVSC = 1 / 296.875 ns
fVSC = 3.37 MHz

6) Calculate the horizontal timing parameters. This includes the front porch, horizontal sync, and back porch. The monitor specifies these parameters in microseconds, while the TMS34061 defines them in terms of VIDCLK cycles. To calculate the register values, divide the given time by the VIDCLK period, which is the same as the shift register load time tLd. These values should be rounded up to guarantee that the minimum requirements are met.

HFp = 2.0 µs from monitor specification
HFp (in lines) = HFp (in time units) / tLd
= 2.0 µs / 296.875 ns
= 6.74, round to 7 lines

Hs = 2.5 µs from monitor specification
Hs (in lines) = Hs (in time units) / tLd
= 2.5 µs / 296.875 ns
= 8.43, round to 9 lines

HBp = 3.5 µs from monitor specification
HBp (in lines) = HBp (in time units) / tLd
= 3.5 µs / 296.875 ns
= 11.80 µs, round to 12 lines

7) After calculating all the horizontal parameters, verify that the actual horizontal scan frequency is within the monitor's capability by adding up all the VIDCLK cycles per line and multiplying this sum by the VIDCLK period. The reciprocal of this period gives the horizontal scanning frequency.

Hlines = Hact + HFp + Hs + HBp
(each is expressed in lines)
Hlines = 80 + 7 + 9 + 12
Hlines = 108

tHorz = Hlines × tLd
tHorz = 108 × 296.875 ns
tHorz = 32.06 µs
fHorz = 1 / tHorz

fHorz = 1 / 32.06 µs
fHorz = 31.2 kHz

8) Calculate vertical timing. These values can be specified in several ways, such as time or number of horizontal lines, as shown in the vertical sync example below. Horizontal lines are also used in the vertical front porch in this example. Still another way is to give a minimum blanking period front porch and sync width. The back porch is then calculated by subtracting the sync and front porch from the total blanking time. The TMS34061 requires these parameters to be specified in horizontal scan lines.

Vs = 0.2 ms from monitor specification
Vs (in lines) = Vs (in time units) / tHorz
= 0.20 ms / 32.06 µs
= 6.24, round to 7 lines

VFp = 2 lines from monitor specification
VFp (in lines) = VFp (in time units) / tHorz

VBp (in lines) = [Vb (in time units) / tHorz] - VFp - Vs
VBp = [1 ms / 32.06 µs] - 2 - 7
VBp = 22.19, round to 23 (in total horizontal lines)

9) Make sure the vertical scan frequency is within the monitor limits by adding all the horizontal lines, active and blanked, and multiplying the sum by the horizontal scan frequency.

Vlines = Vact + VFp + Vs + VBp (all in lines)
Vlines = 480 + 2 + 7 + 23
Vlines = 512
tVert = Vlines × tHorz
tVert = 512 × 32.06 µs
tVert = 16.41 ms

fVert = 1 / tVert
fVert = 1 / 16.41 ms
fVert = 60.92 Hz

8.1.2 Calculating Video Timing Register Values

The calculated timing parameters must now be converted into register values. Horizontal and vertical timing information is generated by two counters located within the TMS34061. The Horizontal Counter counts VIDCLKs and outputs horizontal timing data, while the Vertical Counter counts horizontal lines and outputs vertical timing data. The initial value of the counters is zero and is defined as the start of sync. The counters are first compared to the end of sync value. When this value is reached, the sync output is driven high and the comparator is switched to the End Blank Register. When this second value is reached, the BLANK output is driven high. The comparator then monitors the Start Blank Register. When this value is reached, the Blank Output is driven active. The final value is the Total Count, which drives the SYNC output active and clears the counter to zero. The sequence is then repeated.

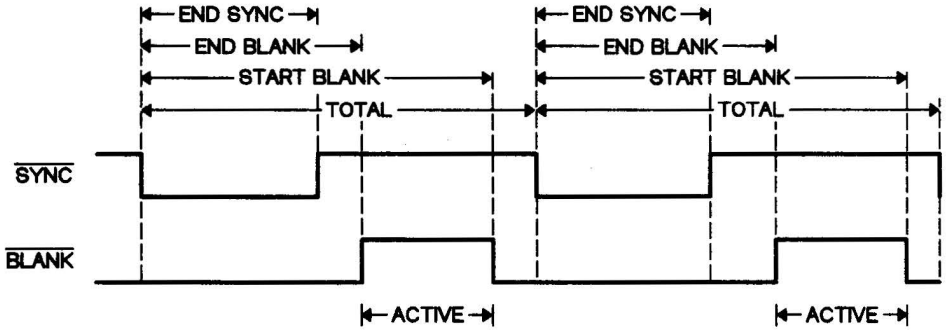


Figure 8-2. Horizontal and Vertical Timing Information

Horizontal End Sync. The Horizontal End Sync Register defines the width of the horizontal sync pulse. The minimum Horizontal End Sync value is one, and the maximum value is one less than the value in the Horizontal End Blank Register. The value of the Horizontal End Sync Register should be set to one less than the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse.

Horz End Sync = Sync Width - 1
= 9 - 1 = 8 (decimal)
= 8 (hex)

Horizontal End Blank. The Horizontal End Blank Register defines the width of the horizontal back porch. The minimum Horizontal End Blank value is one greater than the value of the Horizontal End Sync Register, and the maximum value is one less than the value in the Horizontal Start Blank Register. The value of the Horizontal End Blank Register should be set to one less than the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse plus the horizontal back porch.

Horz End Blank = Sync Width + Back Porch - 1
= 9 + 12 - 1 = 20 (decimal)
= 14 (hex)

Horizontal Start Blank. The Horizontal Start Blank Register defines the horizontal active time. The minimum Horizontal Start Blank value is one less than 1/2 the horizontal total. The maximum value is one less than the value in the Horizontal Total Register. The contents of the Horizontal Start Blank Register should be set to one less than the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse plus the horizontal back porch plus the active time.

Horz Start Blank = Sync Width + Back Porch + Active - 1
= 9 + 12 + 80 - 1 = 100 (decimal)
= 64 (hex)

Horizontal Total. The Horizontal Total Register defines the duration of the horizontal front porch. The contents of the Horizontal Total Register should be set to one less than the number of VIDCLK periods in a horizontal scan line. This is the sum of the horizontal front porch, horizontal sync, horizontal back porch, and horizontal active time minus one in VIDCLK units.

Horz Total = Sync Width + Back Porch + Active + Front Porch - 1
= 9 + 12 + 80 + 7 - 1 = 107 (decimal)
= 6B (hex)

Blanking Skew. It is required to generate a blank signal from the TMS34061 one VIDCLK period before it is actually required. The TMS34061 blank signal is then conditioned by clocking it through a flip-flop on the next VIDCLK edge. This provides a blank signal with a small delay from VIDCLK. To skew the blank signal one clock period forward, the End Blank and Start Blank registers must be one count less than without the skew.

Vertical End Sync. The Vertical End Sync Register defines the width of the vertical sync pulse. The Vertical End Sync value should be set to one less than the number of horizontal scan lines corresponding to the duration of vertical sync pulse. The minimum Vertical End Sync value is one less than the value in the Vertical End Blank Register.

Vert End Sync = Sync Width - 1
= 7 - 1 = 6 (decimal)
= 6 (hex)

Vertical End Blank. The contents of the Vertical End Blank Register define the end of the vertical blanking interval. The minimum Vertical End Blank value is one greater than the value of Vertical End Sync, and the maximum value is one less than the value in the Vertical Start Blank Register. The Vertical End Blank value is one less than the number of horizontal scan lines corresponding to vertical sync width plus the vertical back porch.

Vert End Blank = Sync Width + Back Porch - 1
= 7 + 23 - 1 = 30 (decimal)
= 1D (hex)

Vertical Start Blank. The contents of the Vertical Start Blank register define the vertical active time. The minimum Vertical Start Blank value is one plus the Vertical End Blank value. The contents of the Vertical Start Blank Register will be one less than the number of horizontal scan lines corresponding to the vertical sync width plus the vertical back porch plus the active time.

Vert Start Blank = Sync Width + Back Porch + Active - 1
= 7 + 23 + 480 - 1 = 509 (decimal)
= 1FD (hex)

Vertical Total. The contents of the Vertical Total Register define the duration of the vertical front porch. With the TMS34061 configured for non-interlaced video, the contents of the Vertical Total Register should be set to one less than the the number of horizontal scan lines corresponding to the duration of each frame. In interlaced mode, the total number of lines in each field is equal to the contents of:

Vert Total = Sync Width + Back Porch + Active + Front Porch - 1
= 7 + 23 + 480 + 2 - 1 = 511 (decimal)
= 1FF (hex)

Note:

No two registers can have the same value. If calculations result in the same value, one must be adjusted.