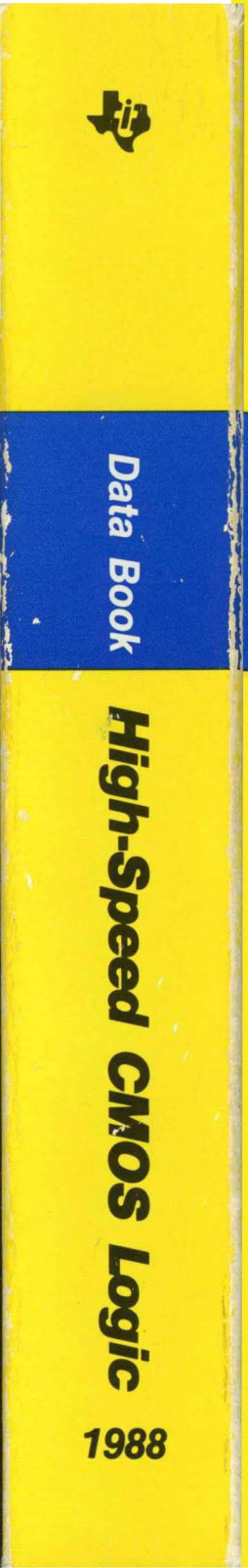

TEXAS INSTRUMENTS

High-Speed CMOS Logic

Data Book

1988

High-Speed CMOS Logic Data Book

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Information contained herein supersedes data published in the *High-Speed CMOS Logic Data Book,* 1984, SCLD001A.

INTRODUCTION

The high-speed silicon-gate CMOS (HCMOS) logic family from Texas Instruments offers a broad range of functions from basic gates and flip-flops to bus-compatible complex devices. The devices in this family are pin-for-pin and functionally compatible with the corresponding devices in the popular LSTTL family while offering a significant power savings. Both CMOS voltage-compatible functions, SN54/74HC', and TTL voltage-compatible functions, SN54/74HCT' are included in TI's HCMOS logic family.

The HCMOS logic devices included in this book offer speed and drive capability comparable to LS but with lower power dissipation for applications where power must be minimized. The availability of these devices in surface mount packaging, both SO and LCC, also makes them especially attractive for use in systems where board space is critical.

High-speeds and low power consumption have been made possible by the 3-μm self-aligned poly-silicon-gate CMOS process. This self-aligning process permits smaller channel lengths, hence an increase in switching speeds and less gate capacitance.

Through the successful execution of an aggressive design-in reliability program, Texas Instruments is able to offer a HCMOS logic family with reliability consistent with that of more mature technologies. Reliability improvement programs are ongoing. Further, a quality watch program to continually monitor the quality and reliability of production devices is in place and guarantees a consistent product of the highest quality.

This book contains pertinent technical information on available HCMOS devices. The general information section includes a functional and numerical index, and parameter measurement information. The mechanical section provides packaging information on all devices included in this book. A detailed discussion of interchangeability, electrostatic discharge (ESD) protection, latch-up circuitry, design considerations, interfacing, and other pertinent subjects regarding this family can be found in the designer's information section.

Complete technical data for any Texas Instruments semiconductor/component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to:

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We sincerely hope that you will find the new HCMOS Logic Data Book a meaningful addition to your technical library.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields, however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

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NUMERICAL INDEX

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8-Bit Shift Registers	Serial/Parallel, Clear, Clock Inhibit, Shift/Load	2 Serial	'HC165	2-219
	2 Serial, Clear	Parallel	'HC164	2-215
	Serial/Parallel, Clear, Clock Inhibit, Shift/Load	Serial	'HC166	2-225
8-Bit Shift Registers with Output Registers	Serial	Parallel	'HC594	2-533
		3-State Parallel	'HC595	2-539
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	Q only	'HC77	2-105
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Octal D-type Latches	Q only, 3-State	'HC373	2-413
		'HC573	2-507
	$\overline{Q}$ only, 3-State	'HC533	2-457
		'HC563	2-489
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		'HCT563	2-493
8-Bit Addressable Latches	Q only	'HC4724	2-731
		'HC259	2-349

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DESCRIPTION	OUTPUT CONFIGURATION	OTHER FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
Dual D-type Flip-Flops with Preset and Clear	Complementary	Independent clocks, Preset, and Clear	'HC74	2-89
			'HCT74	2-93
Dual D-type Flip-Flops with 2-Input NAND/NOR Gates	Complementary	Independent clocks, Preset, and Clear	'HC7074	2-761
Quad D-type Flip-Flops with Common Clocks	Complementary	Common Clear	'HC175	2-237
		Output Enable	'HC379	2-437
Hex D-type Flip-Flops with Common Clocks	Q only	Common Clear	'HC174	2-237
		Output Enable	'HC378	2-437
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		Output Enable	'HC377	2-437
	3-State, Q only	Output control	'HC374	2-423
			'HC574	2-517
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			'HCT574	2-523
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DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
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	'HC107	2-121
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Dual J-K Flip-Flops with Preset, Common Clock, and Common Clear	'HC78	2-109
	'HC114	2-137
Dual J-K Flip-Flops with Preset and Clear	'HC76	2-107
	'HC112	2-129
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear	'HC109	2-125

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DESCRIPTION	OUTPUT DATA	CONTROL INPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
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			'HC126	2-141
Quad Bus Transceivers	Inverting	Independent Enables	'HC242	2-305
	True	for A or B Buses	'HC243	2-305
Hex Bus Drivers/Receivers	True	Common Enables	'HC365	2-407
	Inverting		'HC366	2-407
	True	Symmetrical Enables	'HC367	2-407
	Inverting		'HC368	2-407
Octal Bus Drivers/Receivers	Inverting	Symmetrical Enables	'HC240	2-295
		2 Enables	'HC540	2-477
	True	Complementary Enables	'HC241	2-295
		Symmetrical Enables	'HC244	2-315
		2 Enables	'HC541	2-477
Octal Bus Transceivers	Inverting	Independent Enables	'HC620	2-551
	True	for A or B Buses	'HC623	2-551
	Inverting	Enable and Direction Control	'HC640	2-559
	True and Inverting		'HC643	2-559
	True		'HC645	2-559
			'HC245	2-323
Octal Bus Transceivers with Registers	True	Enable and Direction Control	'HC646	2-571
	Inverting		'HC648	2-571
	Inverting	Independent Enables	'HC651	2-585
	True	for A or B Buses	'HC652	2-585
8-/9-Bit Bus Transceivers with Parity Checker/Generator	True	Enable and Direction Control	'HC659	2-599
	Inverting		'HC658	2-599
	True	Independent Enables	'HC665	2-615
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BUS DRIVERS AND TRANSCEIVERS WITH 3-STATE OUTPUTS AND TTL-COMPATIBLE INPUTS

DESCRIPTION	OUTPUT DATA	CONTROL INPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
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	True		'HCT243	2-311
Octal Bus Drivers/Receivers	Inverting	Symmetrical Enables	'HCT240	2-301
		2 Enables	'HCT540	2-483
	True	Complementary Enables	'HCT241	2-301
		Symmetrical Enables	'HCT244	2-319
		2 Enables	'HCT541	2-483
Octal Bus Transceivers	Inverting	Independent Enables for A and B Buses	'HCT620	2-555
	True		'HCT623	2-565
	Inverting	Enable and Direction Control	'HCT640	2-565
	True and Inverting		'HCT643	2-565
	True		'HCT645	2-565
			'HCT245	2-327
Octal Bus Transceivers with Registers	True	Enable and Direction Control	'HCT646	2-579
	Inverting		'HCT648	2-579
	Inverting	Independent Enables for A and B Buses	'HCT651	2-593
	True		'HCT652	2-593
8-/9-Bit Bus Transceivers with Parity Checker/Generator	True	Enable and Direction Control	'HCT659	2-609
	Inverting		'HCT658	2-609
	True	Independent Enables for A and B Buses	'HCT665	2-625
	Inverting		'HCT664	2-625

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DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
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12-Bit Binary Counters		'HC4040	2-697
14-Bit Binary Counters		'HC4020	2-689
	On-Chip Oscillator	'HC4060	2-701
Dual Decade Counters	Biquinary or BCD	'HC390	2-445
	Set-to-9 input	'HC490	2-453
Dual 4-Bit Binary Counters		'HC393	2-445

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DESCRIPTION	FEATURES		DEVICE TYPE	DESCRIPTIVE INFORMATION
Decade	Async Clear	Synchronous Load	'HC160	2-201
	Sync Clear		'HC162	2-201
Decade Up/Down	Clock Inhibit	Asynchronous Load	'HC190	2-247
	Async Clear		'HC192	2-255
Divide-by-8 Johnson Counter	Sync Clear		'HC7022	2-751
Divide-by-10 Johnson Counter	Async Clear		'HC4017	2-683
4-Bit Binary	Async Clear	Synchronous Load	'HC161	2-201
	Sync Clear		'HC163	2-201
4-Bit Binary Up/Down	Clock Inhibit	Asynchronous Load	'HC191	2-247
	Async Clear		'HC193	2-255
8-Bit Binary with Output Registers	Sync Clear	3-State Outputs	'HC590A	2-527

MAGNITUDE COMPARATORS, PARITY GENERATORS/CHECKERS, AND PARITY ENCODERS

DESCRIPTION	FEATURES		DEVICE TYPE	DESCRIPTIVE INFORMATION
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8-Bit Magnitude Comparators	$\overline{P} = \overline{Q}$, $\overline{P} > \overline{Q}$ Outputs		'HC682	2-647
			'HC684	
	$\overline{P} = \overline{Q}$ Outputs	Enable Inputs	'HC688	2-651
9-Bit Odd/Even Parity Generators/Checkers	Even, Odd Inputs		'HC180	2-243
			'HC280	2-363
8-/9-Bit Bus Transceivers with Parity Generators/Checkers	True Outputs	Enable and Direction Control	'HC659	2-599
			'HCT659	2-609
	Inverting Outputs		'HC658	2-599
			'HCT658	2-609
	True Outputs	Independent Enables for A and B Buses	'HC665	2-615
			'HCT665	2-625
	Inverting Outputs		'HC664	2-615
			'HCT664	2-625
8-Line to 3-Line Priority Encoders	Enable Inputs and Outputs		'HC148	2-175
10-Line Decimal to 4-Line BCD Priority Encoders			'HC147	2-175

ADDRESS COMPARATORS

DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
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ARITHMETIC CIRCUITS

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DESCRIPTION	INPUTS	OUTPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
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		Complementary 3-State	'HC251	2-331
	Transparent Latches, Enable		'HC354	2-395
	Registers, Enable		'HC356	2-401
Dual 4-Line to 1-Line	Independent Enables	True, 3-State	'HC253	2-337
		Inverting, 3-State	'HC353	2-389
		True	'HC153	2-189
		Inverting	'HC352	2-383
Quad 2-Line to 1-Line	Common Enable	True	'HC157	2-197
		Inverting	'HC158	2-197
		True, 3-State	'HC257	2-343
		Inverting, 3-State	'HC258	2-343
Quad 2-Line to 1-Line with Storage		True	'HC298	2-373
Octal 2-Line to 1-Line	Input Registers	True, 3-State	'HC604	2-545

DECODERS/DEMULTIPLEXERS

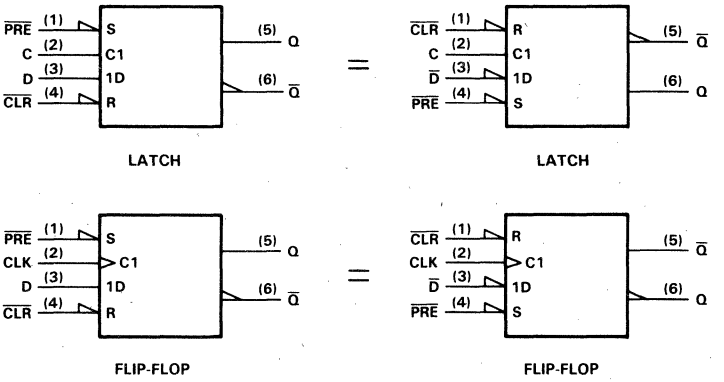
DESCRIPTION	FEATURES	OUTPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
4-Line to 16-Line	2 Enables	Inverting	'HC154	2-193
	Input Latches, Output Enable	True	'HC4514	2-725
		Inverting	'HC4515	2-725
4-Line to 10-Line BCD-to-Decimal			'HC42	2-77
3-Line to 8-Line	3 Enables	True	'HC238	2-283
			'HCT238	2-287
		Inverting	'HC138	2-163
			'HCT138	2-167
	3 Enables, Address Latches	True	'HC237	2-275
			'HCT237	2-279
		Inverting	'HC137	2-155
			'HCT137	2-159
Dual 2-Line to 4-Line	Independent Enables	Inverting	'HC139	2-171
		True	'HC239	2-291

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device.

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. ($t_{dis} = t_{PHZ}$ or t_{PLZ}).

*Current out of a terminal is given as a negative value.

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}.)

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

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t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Trasnition time (general)**

The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**

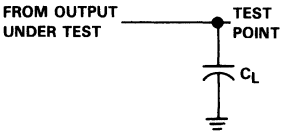
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

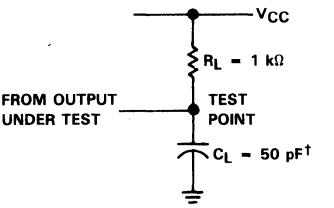


LOAD CIRCUIT

PARAMETER		C_L†
or t_{pd} / t_t	Standard outputs	50 pF
	High-current outputs‡	50 pF or 150 pF

†C_L includes probe and test fixture capacitance.
‡High-current outputs are indicated by the ▷ in the logic symbol.

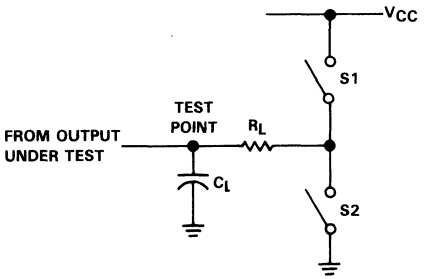
FIGURE 1. TOTEM-POLE OUTPUTS



LOAD CIRCUIT

†C_L includes probe and test fixture capacitance.

FIGURE 2. OPEN-DRAIN OUTPUTS

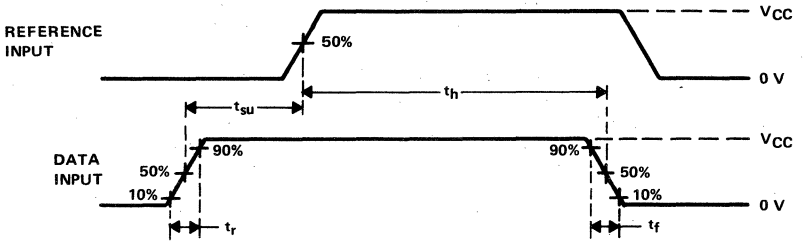


LOAD CIRCUIT

PARAMETER		R_L	C_L†	S_1	S_2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	OPEN	CLOSED
	t_{PZL}			CLOSED	OPEN
t_{dis}	t_{PHZ}	1 kΩ	50 pF	OPEN	CLOSED
	t_{PLZ}			CLOSED	OPEN
t_{pd} or t_t		—	50 pF or 150 pF	OPEN	OPEN

†C_L includes probe and test fixture capacitance.

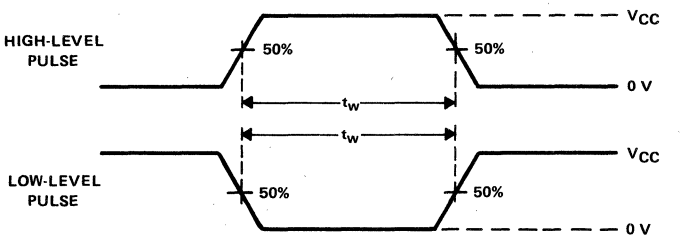
FIGURE 3. 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

NOTE 1: Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

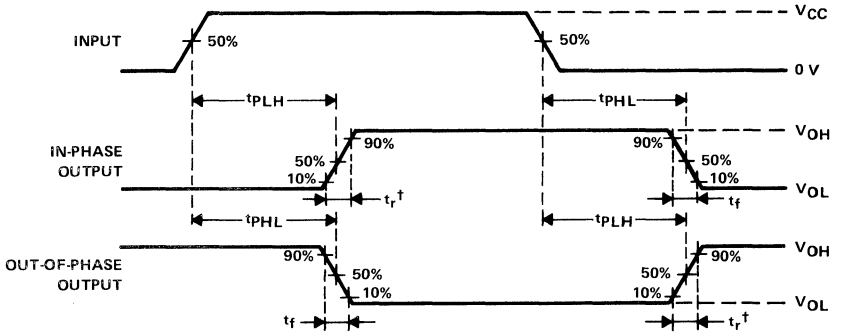
FIGURE 4. HC AND HCU — SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

NOTES: 1. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
2. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

FIGURE 5. HC AND HCU — PULSE DURATIONS

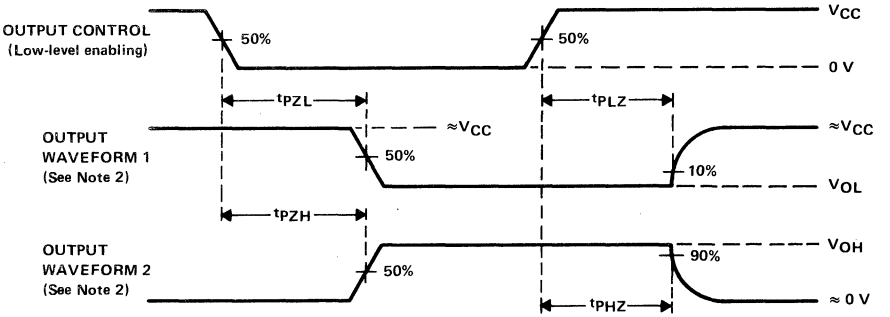


VOLTAGE WAVEFORMS

†t_r is not applicable to SN54/74HCU' devices.

NOTE 1: Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 6. HC AND HCU — PROPAGATION DELAY TIMES AND OUTPUT TRANSITION TIMES

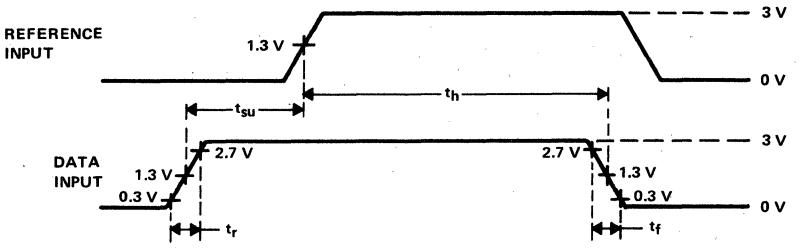


VOLTAGE WAVEFORMS

NOTES: 1. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

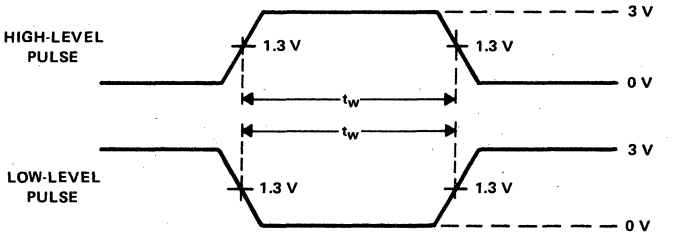
FIGURE 7. HC AND HCU — ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

NOTE 1: Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

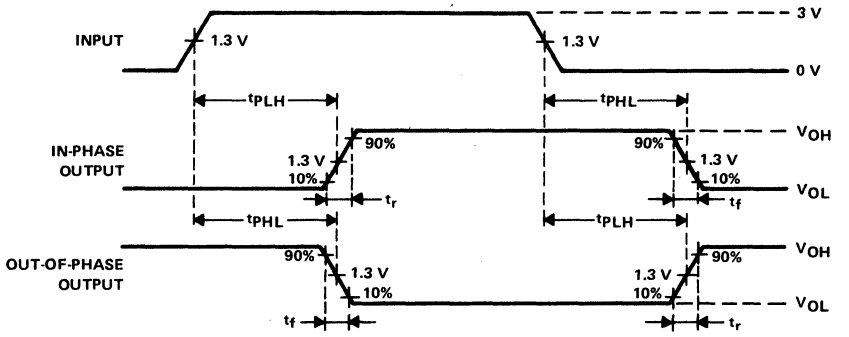
FIGURE 8. HCT — SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

NOTES: 1. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.
2. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

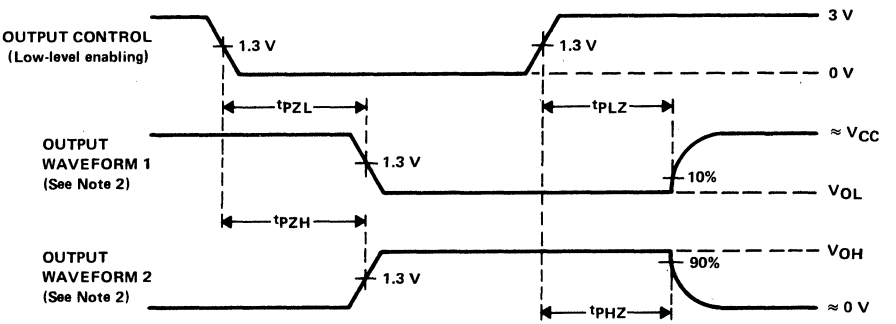
FIGURE 9. HCT — PULSE DURATIONS



VOLTAGE WAVEFORMS

NOTE 1: Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 10. HCT — PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

NOTES: 1. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 11. HCT — ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

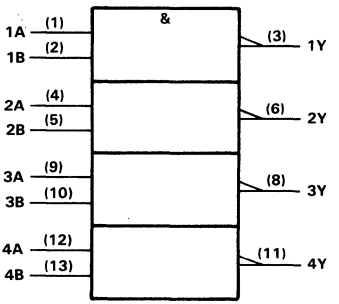
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC00 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

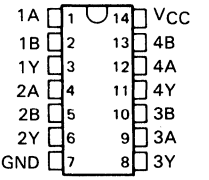
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

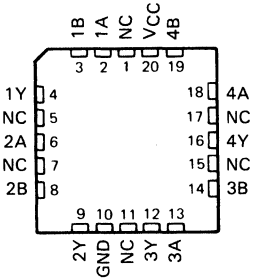


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, or N packages.

SN54HC00 . . . J PACKAGE
SN74HC00 . . . D OR N PACKAGE
(TOP VIEW)

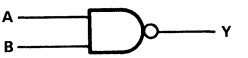


SN54HC00 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (each gate)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC00			SN74HC00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

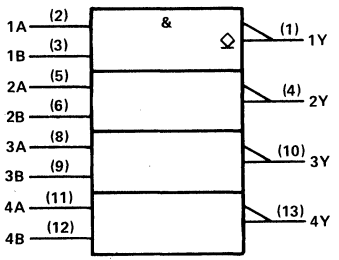
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC01 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC01 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

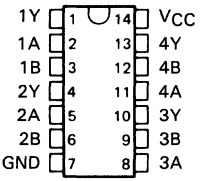
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

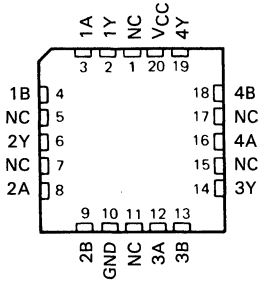


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC01 . . . J PACKAGE
SN74HC01 . . . D OR N PACKAGE
(TOP VIEW)

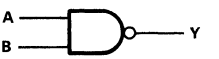


SN54HC01 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC01			SN74HC01			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC01		SN74HC01		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = 0 or V_{CC}	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), R_L = 1 kΩ, C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC01		SN74HC01		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	105		155		131	ns
			4.5 V		13	25		36		31	
			6 V		10	23		31		27	
t_{PHL}			2 V		50	100		150		125	
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

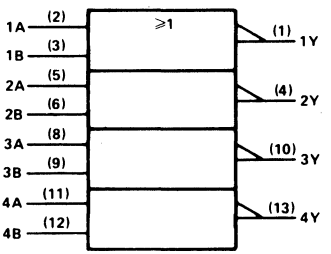
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC02 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

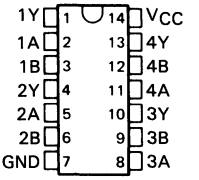
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

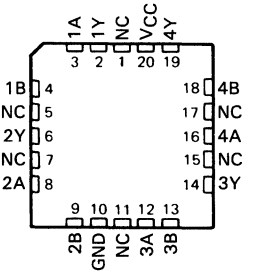


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC02 . . . J PACKAGE
SN74HC02 . . . D OR N PACKAGE
(TOP VIEW)

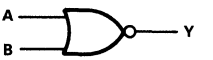


SN54HC02 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC02			SN74HC02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC02		SN74HC02		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = 0 or V_{CC}	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC02		SN74HC02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	22 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

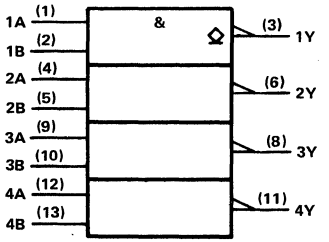
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC03 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC03 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

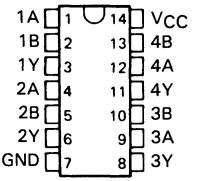
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

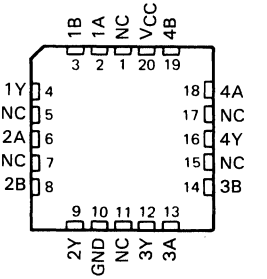


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC03 . . . J PACKAGE
SN74HC03 . . . D OR N PACKAGE
(TOP VIEW)

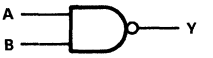


SN54HC03 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC03			SN74HC03			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC03		SN74HC03		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), R_L = 1 kΩ, C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC03		SN74HC03		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	105		155		131	ns
			4.5 V		13	25		36		31	
			6 V		10	23		31		27	
t_{PHL}			2 V		50	100		150		125	
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

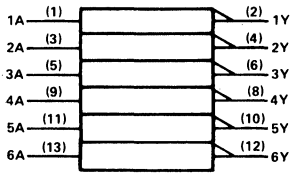
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54HC04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

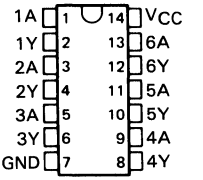
INPUT	OUTPUT
A	Y
H	L
L	H

logic symbols†

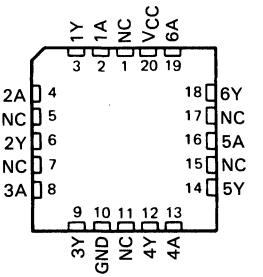


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC04 . . . J PACKAGE
SN74HC04 . . . D OR N PACKAGE
(TOP VIEW)

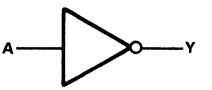


SN54HC04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC04			SN74HC04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = 0 or V_{CC}	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		45	95		145		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2953, JULY 1986—SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

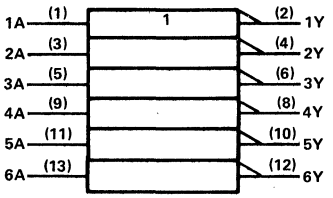
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54HCT04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

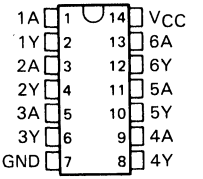
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

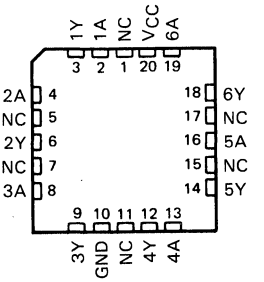


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HCT04 . . . J PACKAGE
SN74HCT04 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT04			SN74HCT04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT04		SN74HCT04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT04		SN74HCT04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		14	20		30		25	ns
			5.5 V		13	18		27		23	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Unbuffered Outputs**
- **Dependable Texas Instruments Quality and Reliability**

description

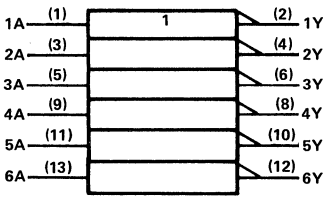
These devices contain six independent inverters. They perform the Boolean function $Y = A$.

The SN54HCU04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCU04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

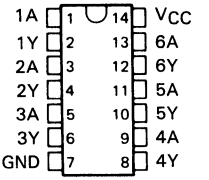
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

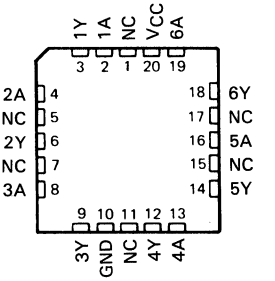


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for D, J, and N packages.

SN54HCU04 . . . J PACKAGE
SN74HCU04 . . . D OR N PACKAGE
(TOP VIEW)

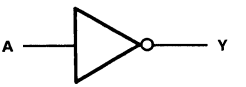


SN54HCU04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCU04			SN74HCU04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.7			1.7			V
	V_{CC} = 4.5 V	3.6			3.6			
	V_{CC} = 6 V	4.8			4.8			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.8	0		0.8	
	V_{CC} = 6 V	0		1.1	0		1.1	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.8			1.8		1.8		V
		4.5 V	4			4		4		
		6 V	5.5			5.5		5.5		
	V_I = V_{CC} or GND, I_{OH} = −4 mA	4.5 V	3.98			3.7		3.84		
	V_I = V_{CC} or GND, I_{OH} = −5.2 mA	6 V	5.48			5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V			0.2		0.2		0.2	V
		4.5 V			0.5		0.5		0.5	
		6 V			0.5		0.5		0.5	
	V_I = V_{CC} or GND, I_{OL} = 4 mA	4.5 V			0.26		0.4		0.33	
	V_I = V_{CC} or GND, I_{OL} = 5.2 mA	6 V			0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V			±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

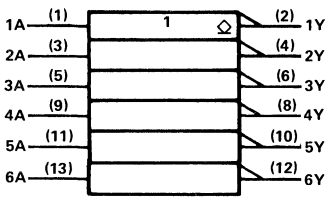
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC05 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC05 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each inverter)

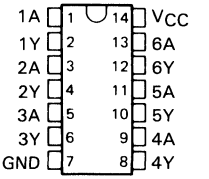
INPUT	OUTPUT
A	Y
H	L
L	H

logic symbol†

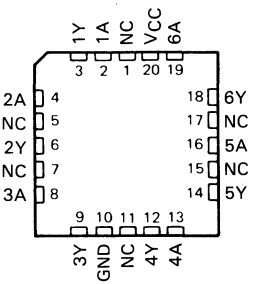


† This symbol is in accordance with ANSI/IEEE Std-91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC05 . . . J PACKAGE
SN74HC05 . . . D OR N PACKAGE
(TOP VIEW)

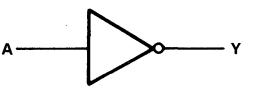


SN54HC05 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC05			SN74HC05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC05		SN74HC05		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2 V		60	115		175		145	ns
			4.5 V		13	23		35		29	
			6 V		10	20		30		25	
t_{PHL}	A	Y	2 V		45	85		130		105	ns
			4.5 V		9	17		26		21	
			6 V		8	14		22		18	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

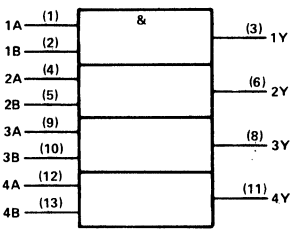
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54HC08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC08 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

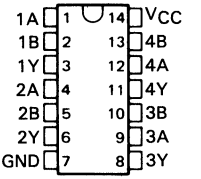
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

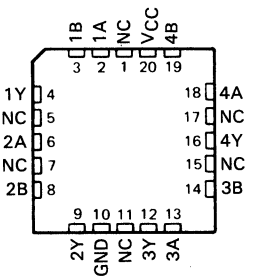


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC08 . . . J PACKAGE
SN74HC08 . . . D OR N PACKAGE
(TOP VIEW)

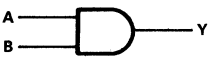


SN54HC08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC08			SN74HC08			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC08		SN74HC08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC08		SN74HC08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

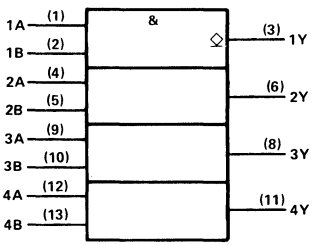
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC09 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC09 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

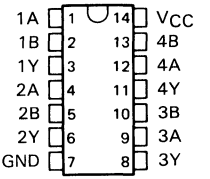
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

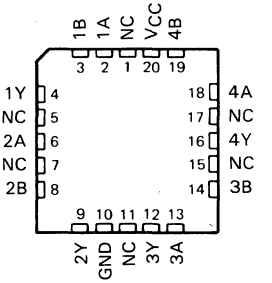


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC09 . . . J PACKAGE
SN74HC09 . . . D OR N PACKAGE
(TOP VIEW)

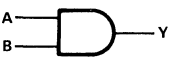


SN54HC09 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC09			SN74HC09			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C		SN54HC09	SN74HC09	UNIT
			MIN TYP	MAX	MAX	MAX	
I_{OH}	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V	0.01	0.5	10	.5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V	0.002	0.1	0.1	0.1	V
		4.5 V	0.001	0.1	0.1	0.1	
		6 V	0.001	0.1	0.1	0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V	0.17	0.26	0.4	0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V	0.15	0.26	0.4	0.33	
I_I	V_I = V_{CC} or 0	6 V	±0.1	±100	±1000	±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V		2	40	20	μA
C_i		2 to 6 V	3	10	10	10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), R_L = 1 kΩ, C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC09		SN74HC09		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	105		155		131	ns
			4.5 V		13	25		36		31	
			6 V		10	23		31		27	
t_{PHL}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

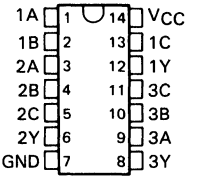
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54HC10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC10 is characterized for operation from −40°C to 85°C.

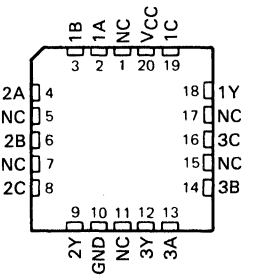
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54HC10 . . . J PACKAGE
SN74HC10 . . . D OR N PACKAGE
(TOP VIEW)

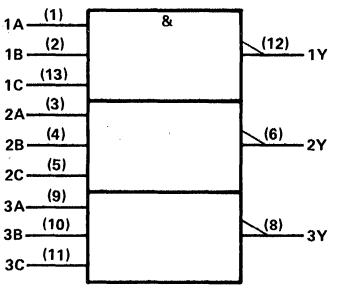


SN54HC10 . . . FK PACKAGE
(TOP VIEW)



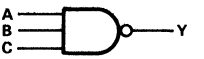
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC10			SN74HC10			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC10		SN74HC10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC10		SN74HC10		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	95		145		120	ns
			4.5 V		10	19		29		24	
			6 V		9	16		25		20	
t_t		Y	2 V		23	75		110		95	ns
			4.5 V		6	15		22		19	
			6 V		5	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

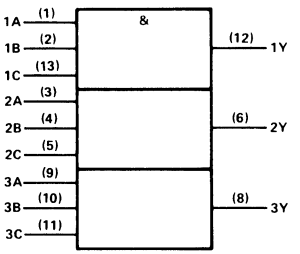
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54HC11 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC11 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

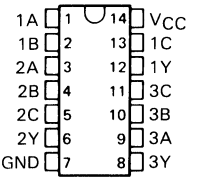
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

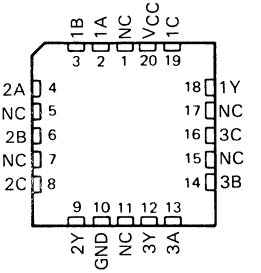


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC11 . . . J PACKAGE
SN74HC11 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC11 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC11			SN74HC11			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC11		SN74HC11		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC11		SN74HC11		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		25	75		110		95	ns
			4.5 V		7	15		22		19	
			6 V		5	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

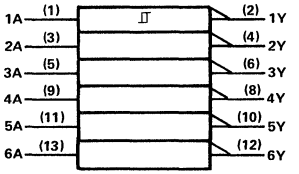
These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54HC14 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC14 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

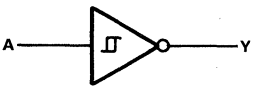
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

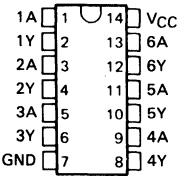


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

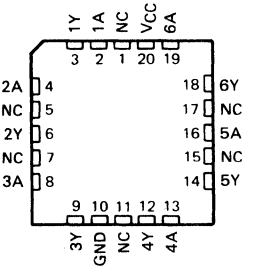
logic diagram (positive logic)



SN54HC14 . . . J PACKAGE
SN74HC14 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC14 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC14			SN74HC14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}		2 V	0.70	1.2	1.50	0.70	1.50	0.70	1.50	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
		6 V	2.10	3.3	4.20	2.10	4.20	2.10	4.20	
V_{T-}		2 V	0.30	0.6	1.00	0.30	1.00	0.30	1.00	V
		4.5 V	0.90	1.6	2.45	0.90	2.45	0.90	2.45	
		6 V	1.20	2.0	3.20	1.20	3.20	1.20	3.20	
$V_{T+} - V_{T-}$		2 V	0.20	0.6	1.20	0.20	1.20	0.20	1.20	V
		4.5 V	0.40	0.9	2.10	0.40	2.10	0.40	2.10	
		6 V	0.50	1.3	2.50	0.50	2.50	0.50	2.50	
I_I	V_I = V_{CC} or 0	6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		32		26	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

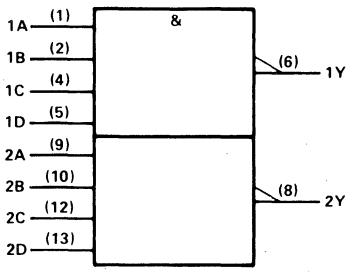
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54HC20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC20 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

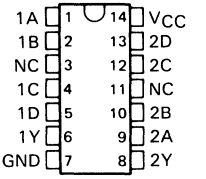
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†

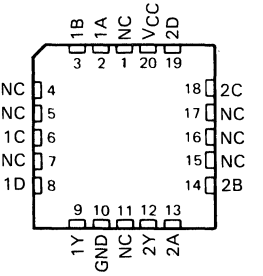


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC20 . . . J PACKAGE
SN74HC20 . . . D OR N PACKAGE
(TOP VIEW)

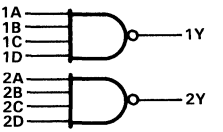


SN54HC20 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC20			SN74HC20			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC20		SN74HC20		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC20		SN74HC20		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	2 V		45	110		165		140	ns
			4.5 V		14	22		33		28	
			6 V		11	19		28		24	
t_t		Y	2 V		27	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		7	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

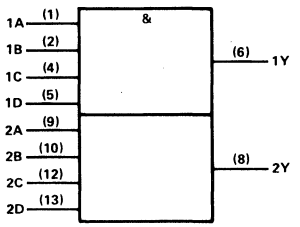
These devices contain two independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

The SN54HC21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC21 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

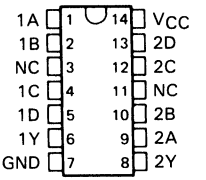
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†

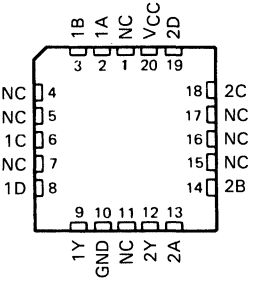


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC21 . . . J PACKAGE
SN74HC21 . . . D OR N PACKAGE
(TOP VIEW)

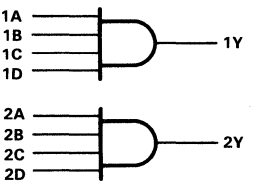


SN54HC21 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input diode current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output diode current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC21			SN74HC21			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC21		SN74HC21		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC21		SN74HC21		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	2 V		44	110		165		140	ns
			4.5 V		14	22		33		28	
			6 V		11	19		28		24	
t_t		Y	2 V		29	75		110		95	ns
			4.5 V		10	15		22		19	
			6 V		8	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

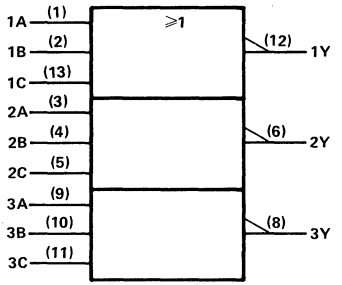
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54HC27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC27 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

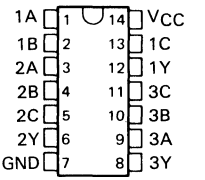
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†

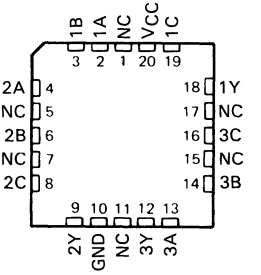


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC27 . . . J PACKAGE
SN74HC27 . . . D OR N PACKAGE
(TOP VIEW)

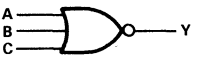


SN54HC27 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC27			SN74HC27			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC27		SN74HC27		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC27		SN74HC27		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	90		135		115	ns
			4.5 V		10	18		27		23	
			6 V		9	15		23		20	
t_t		Y	2 V		27	75		110		95	ns
			4.5 V		7	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

or

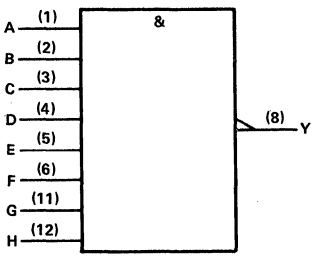
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54HC30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC30 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

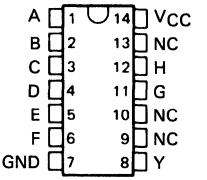
INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†

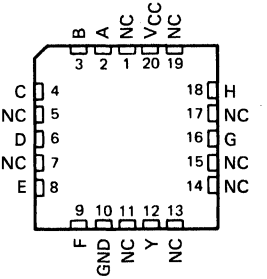


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC30 . . . J PACKAGE
SN74HC30 . . . D OR N PACKAGE
(TOP VIEW)

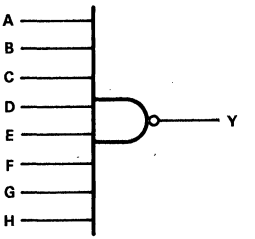


SN54HC30 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC30			SN74HC30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC30		SN74HC30		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC30		SN74HC30		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A thru H	Y	2 V		51	130		195		165	ns
			4.5 V		15	26		39		33	
			6 V		12	22		33		28	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	22 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

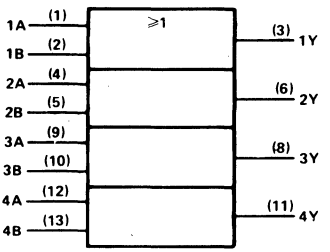
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54HC32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC32 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

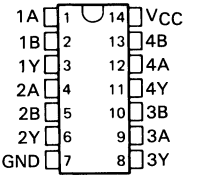
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

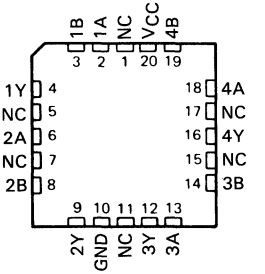


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC32 . . . J PACKAGE
SN74HC32 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC32 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC32			SN74HC32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC32		SN74HC32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC32		SN74HC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

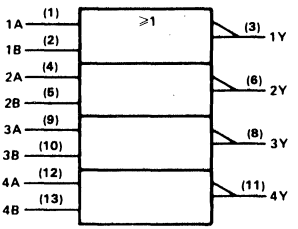
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54HC36 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC36 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

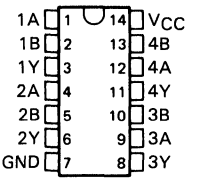
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

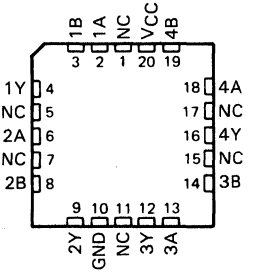


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC36 . . . J PACKAGE
SN74HC36 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC36 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC36			SN74HC36			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC36		SN74HC36		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC36		SN74HC36		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	110		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Full Decoding of Input Logic**
- **All Outputs are High for Invalid BCD Conditions**
- **Also for Application as 3-Line to 8-Line Decoders**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

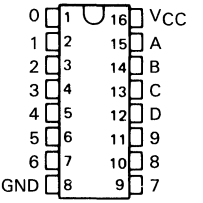
The SN54HC42 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC42 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

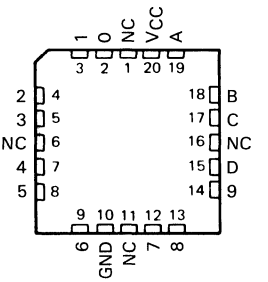
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

SN54HC42 . . . J PACKAGE
SN74HC42 . . . D/DW† OR N PACKAGE
(TOP VIEW)



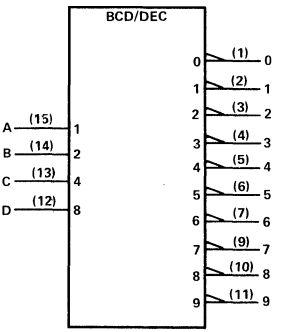
SN54HC42 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

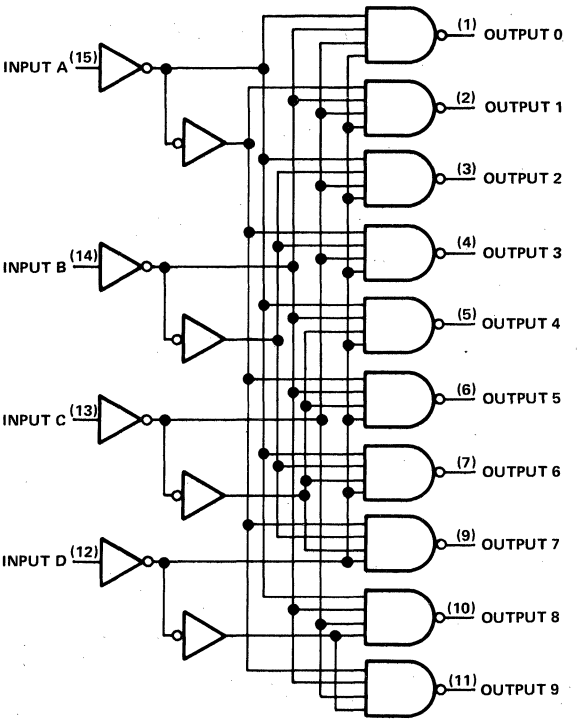
†Contact the factory for D or DW package availability.

logic symbol‡



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D/DW†, J, and N packages.

†Connect the factory for D or DW package availability.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC42			SN74HC42			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC42		SN74HC42		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC42		SN74HC42		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	0 thru 9	2 V		65	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		7	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	39 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The device performs the following Boolean functions:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

The SN54HC51 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC51 is characterized for operation from −40°C to 85°C.

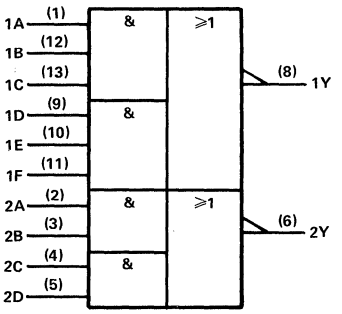
FUNCTION TABLES

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

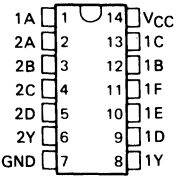
H = high level, L = low level, X = irrelevant

logic symbol†

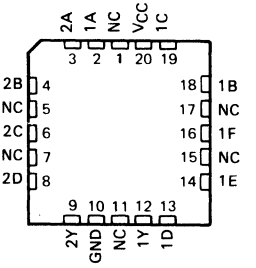


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC51 . . . J PACKAGE
SN74HC51 . . . D OR N PACKAGE
(TOP VIEW)

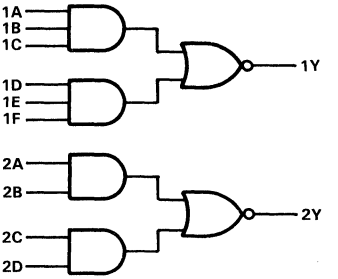


SN54HC51 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC51			SN74HC51			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC51		SN74HC51		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC51		SN74HC51		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any	Y	2 V		54	140		210		175	ns
			4.5 V		15	28		42		35	
			6 V		12	24		36		30	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

C_{pd}	Power dissipation capacitance per AOI gate	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

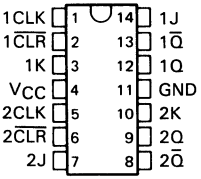
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Clear input resets the outputs regardless of the other inputs. When Clear is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These flip-flops can also perform as toggle flip-flops by tying J and K high.

The SN54HC73 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC73 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

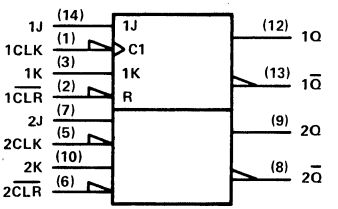
INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

SN54HC73 . . . J PACKAGE
SN74HC73 . . . D OR N PACKAGE
(TOP VIEW)



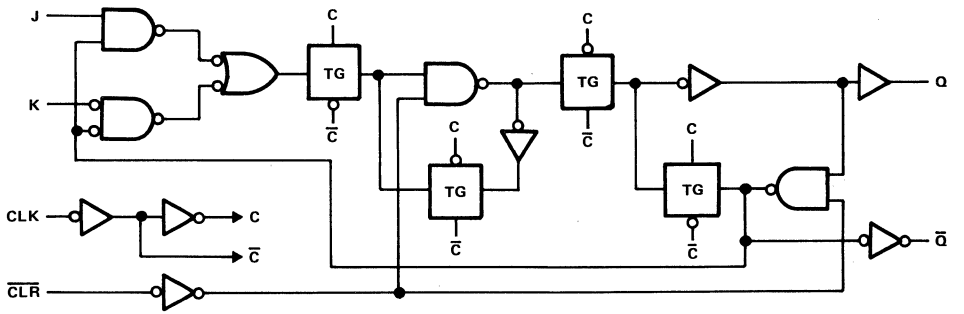
For functionally and electrically identical parts in chip carrier, see SN54HC107.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC73			SN74HC73			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC73		SN74HC73		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC73		SN74HC73		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, $\overline{CLR}$ inactive or data before CLK↓		2 V	100		150		125		ns
			4.5 V	25		35		30		
			6 V	20		30		25		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC73		SN74HC73		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	54		21		25		
			6 V	36	64		25		29		
t_{PHL}	$\overline{CLR}$	Q	2 V		78	155		250		194	ns
			4.5 V		16	31		47		39	
			6 V		13	26		40		32	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	2 V		78	155		250		194	ns
			4.5 V		16	31		47		39	
			6 V		13	26		40		32	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		63	126		185		160	ns
			4.5 V		13	25		37		32	
			6 V		11	21		32		27	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	30 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

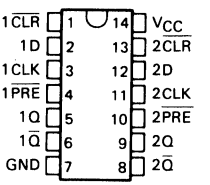
The SN54HC74 is characterized for operation over the full military temperature range −55°C to 125°C. The SN74HC74 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

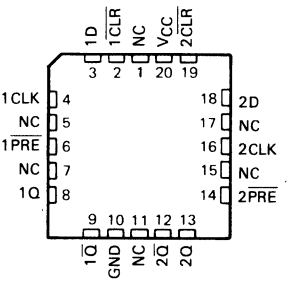
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when Preset or Clear returns to its inactive (high) level.

SN54HC74 . . . J PACKAGE
SN74HC74 . . . D OR N PACKAGE
(TOP VIEW)

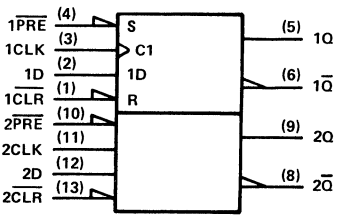


SN54HC74 . . . FK PACKAGE
(TOP VIEW)



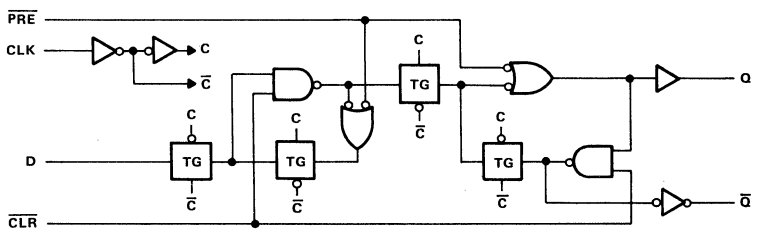
NC—No internal connection

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC74			SN74HC74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = 0 or V_{CC}	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = 0 or V_{CC}, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC74		SN74HC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su} Setup time before CLK↑	Data	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
		4.5 V	5		8		6		
		6 V	4		7		5		
t_h Hold time data after CLK↑		2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		70	230		345		290	ns
			4.5 V		20	46		69		58	
			6 V		15	39		59		49	
	CLK	Q or $\overline{Q}$	2 V		70	175		250		220	
			4.5 V		20	35		50		44	
			6 V		15	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

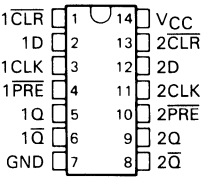
The SN54HCT74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT74 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

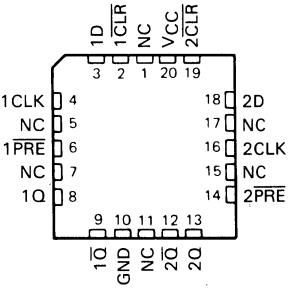
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when Preset or Clear returns to its inactive (high) level.

SN54HCT74 . . . J PACKAGE
SN74HCT74 . . . D OR N PACKAGE
(TOP VIEW)

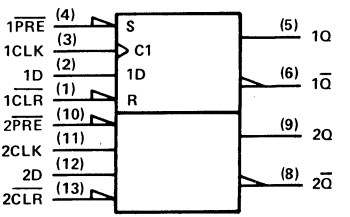


SN54HCT74 . . . FK PACKAGE
(TOP VIEW)



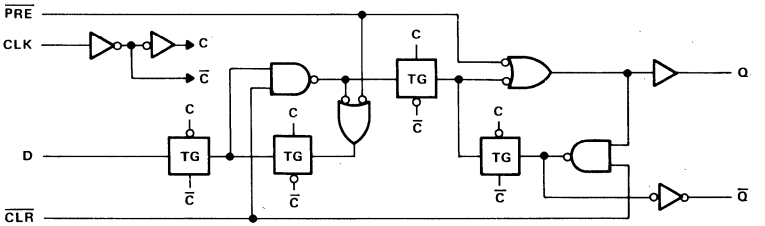
NC—No internal connection

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT74			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT74		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	27	0	18	0	22	MHz
			5.5 V	0	30	0	20	0	24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
		CLK high or low	4.5 V	18		27		23		
			5.5 V	16		24		21		
t_{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	4.5 V	0		0		0		
			5.5 V	0		0		0		
t_h	Hold time data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or Q	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\overline{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

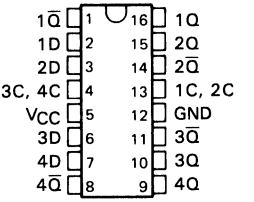
C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Complimentary Q and $\overline{Q}$ Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC75 . . . J PACKAGE
SN74HC75 . . . D OR N PACKAGE
(TOP VIEW)

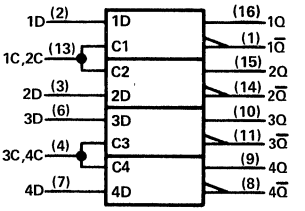


description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information, which was present at the data input at the time the transition occurred, is retained at the Q output until the enable is permitted to go high.

The SN54HC75 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC75 is characterized for operation from −40°C to 85°C.

logic symbol†

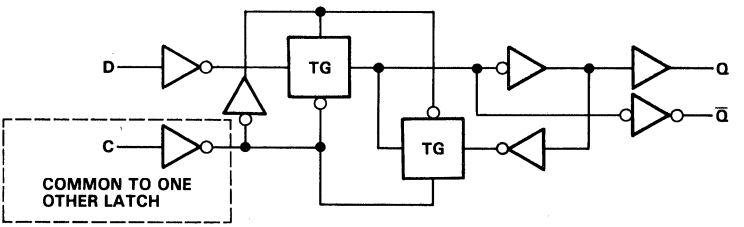


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each latch)

INPUTS		OUTPUT	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic diagram, each latch (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC75			SN74HC75			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC77		SN74HC77		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC75		SN74HC75		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before C↓	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC75		SN74HC75		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q or $\overline{Q}$	2 V		40	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{pd}	C	Q or $\overline{Q}$	2 V		44	130		195		165	ns
			4.5 V		15	26		39		33	
			6 V		12	22		33		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	46 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

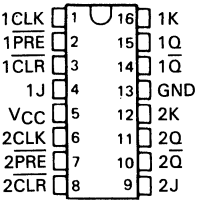
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can also perform as toggle flip-flops by tying J and K high.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

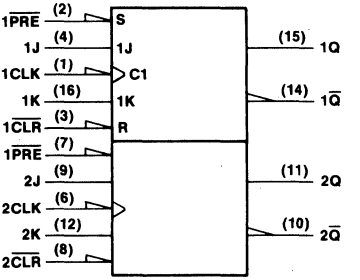
‡This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54HC76 . . . J PACKAGE
SN74HC76 . . . D OR N PACKAGE
(TOP VIEW)



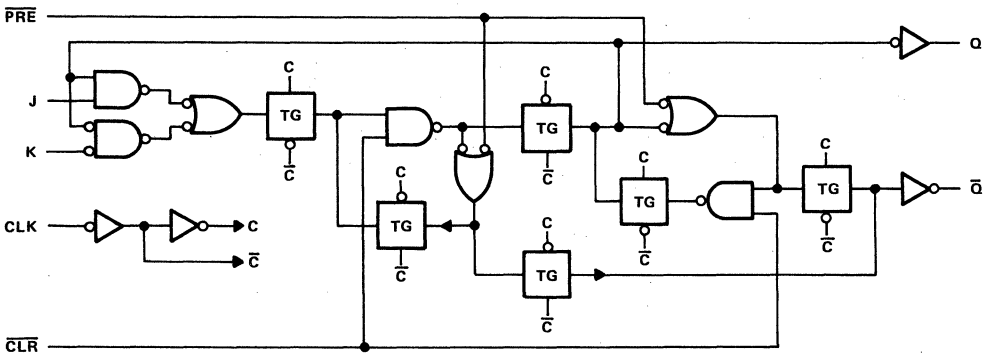
For functionally and electrically identical parts in chip carrier packages, see SN54HC112.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC76			SN74HC76			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC76		SN74HC76		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC76		SN74HC76		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↓	Data	2 V	150		225		190		ns
			4.5 V	30		45		38		
			6 V	25		38		32		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC76		SN74HC76		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	41		21		25		
			6 V	36	50		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		65	155		250		190	ns
			4.5 V		16	31		47		39	
			6 V		15	26		40		33	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		70	145		220		180	ns
			4.5 V		19	29		44		36	
			6 V		16	25		37		31	
t_t		Q or $\overline{Q}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	36 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

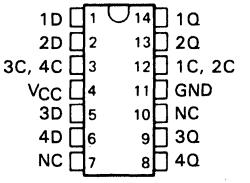
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information, which was present at the data input at the time the transition occurred, is retained at the Q output until the enable is permitted to go high.

The SN54HC77 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC77 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUT
D	C	Q
L	H	L
H	H	H
X	L	Q_0

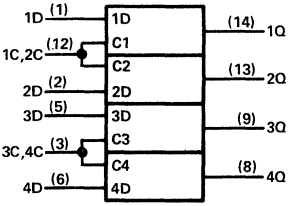
SN54HC77 . . . J PACKAGE
SN74HC77 . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

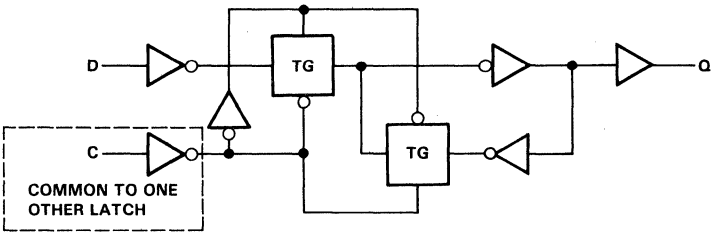
Not available in chip carrier package with JEDEC-Standard pinout. For chip carrier information, contact the factory.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each latch (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC77			SN74HC77			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC77		SN74HC77		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC77		SN74HC77		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before C↓	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC77		SN74HC77		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		40	120		180		150	ns
			4.5 V		12	24		36		30	
			6 V		10	20		31		26	
t_{pd}	C	Q	2 V		45	130		195		165	ns
			4.5 V		14	26		39		33	
			6 V		11	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	16 pF typ

- **Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

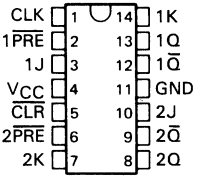
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When the Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

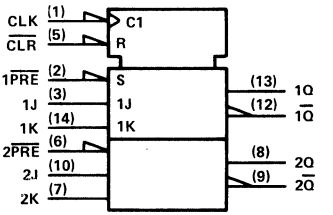
‡This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54HC78 . . . J PACKAGE
SN74HC78 . . . D OR N PACKAGE
(TOP VIEW)



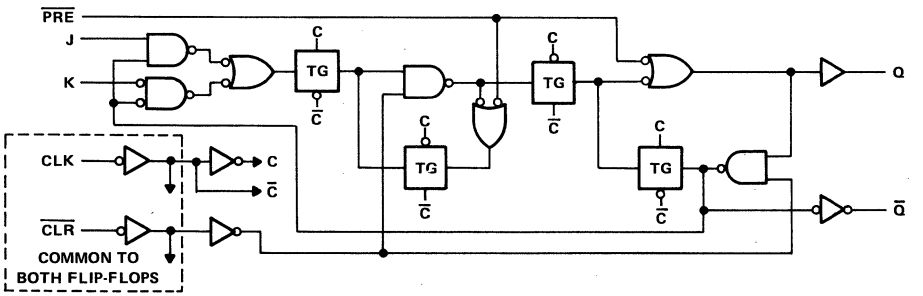
For functionally and electrically identical parts in chip carrier packages, see SN54HC114.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC78			SN74HC78			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC78		SN74HC78		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC78		SN74HC78		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	2 V	80		119		101		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		119		101		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↓	$\overline{CLR}$ or $\overline{PRE}$ inactive or data	2 V	100		150		125		ns
			4.5 V	25		35		30		
			6 V	20		30		25		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC78		SN74HC78		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		78	155		250		194	ns
			4.5 V		16	31		47		39	
			6 V		13	26		40		32	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		63	126		185		160	ns
			4.5 V		13	25		37		32	
			6 V		11	21		32		27	
t_t			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	30 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

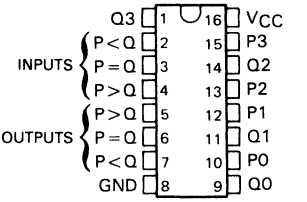
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

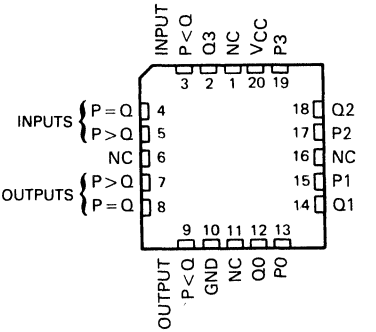
These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P, Q) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The P>Q, P<Q, and P=Q outputs of a stage handling less significant bits are connected to the corresponding P>Q, P<Q, and P= inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high-level voltage applied to the P=Q input. The cascading path of the 'HC85A is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

The SN54HC85A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC85A is characterized for operation from −40°C to 85°C.

SN54HC85A . . . J PACKAGE
SN74HC85A . . . D† OR N PACKAGE
(TOP VIEW)

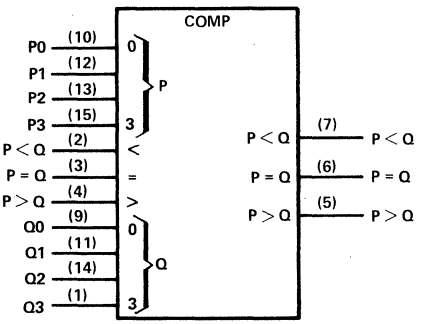


SN54HC85A . . . FK PACKAGE
(TOP VIEW)



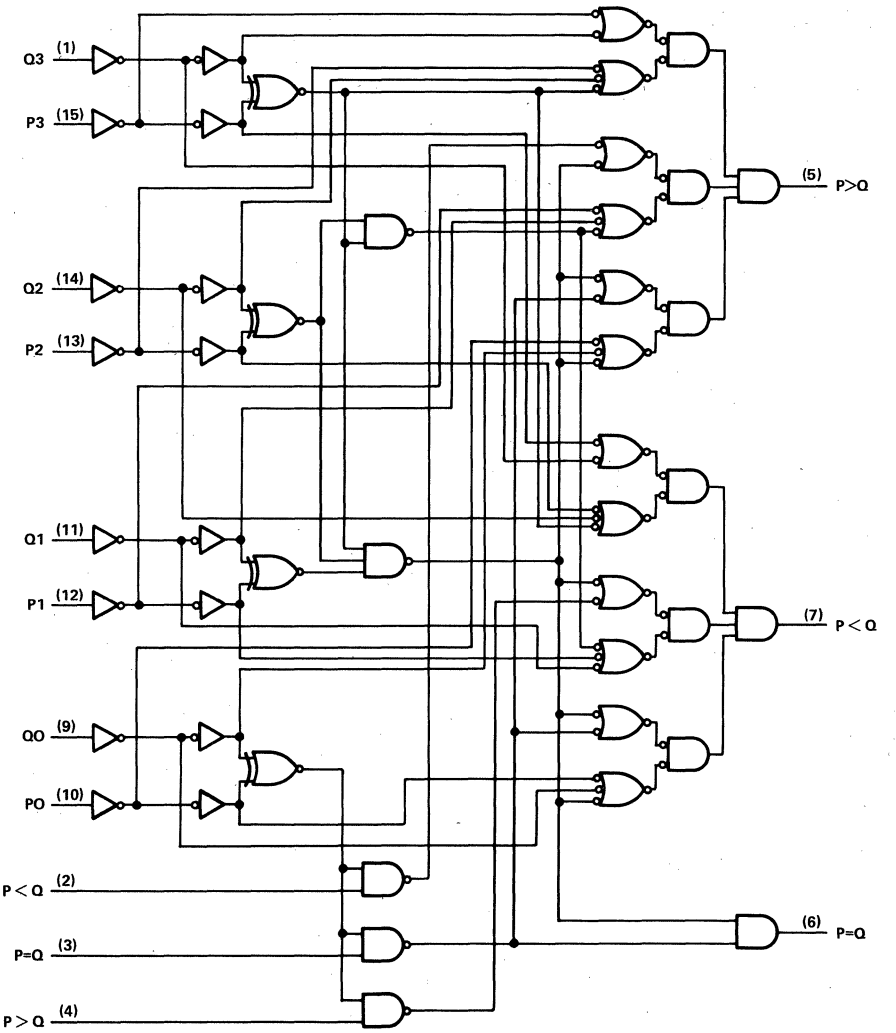
NC—No internal connection
†May be obtained in either D or DW version. Contact the factory for availability.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW†, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D/DW†, J, and N packages.

†May be obtained in either D or DW version. Contact the factory for availability.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	P2, Q2	P1, Q1	P0, Q0	P>Q	P<Q	P=Q	P>Q	P<Q	P=Q
P3>Q3	X	X	X	X	X	X	H	L	L
P3<Q3	X	X	X	X	X	X	L	H	L
P3=Q3	P2>Q2	X	X	X	X	X	H	L	L
P3=Q3	P2<Q2	X	X	X	X	X	L	H	L
P3=Q3	P2=Q2	P1>Q1	X	X	X	X	H	L	L
P3=Q3	P2=Q2	P1<Q1	X	X	X	X	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0>Q0	X	X	X	H	L	L
P3=Q3	P2=Q2	P1=Q1	P0<Q0	X	X	X	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	H	L	L	H	L	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	L	H	L	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	X	X	H	L	L	H
P3=Q3	P2=Q2	P1=Q1	P0=Q0	H	H	L	L	L	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	L	L	L	H	H	L

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW‡ or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ May be obtained in either D or DW version. Contact the factory for availablility.

recommended operating conditions

			SN54HC85A			SN74HC85A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC85A		SN74HC85A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC85A		SN74HC85A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P or Q	P>Q or P<Q	2 V		80	230		345		290	MHz
			4.5 V		26	46		69		58	
			6 V		22	39		59		49	
t_{pd}	Any P or Q	P=Q	2 V		66	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{pd}	P<Q or P=Q	P>Q	2 V		63	175		260		220	ns
			4.5 V		21	41		58		50	
			6 V		18	33		46		39	
t_{pd}	P>Q or P=Q	P<Q	2 V		72	175		260		220	ns
			4.5 V		24	41		58		50	
			6 V		20	33		46		39	
t_{pd}	P=Q	P=Q	2 V		51	145		215		185	ns
			4.5 V		17	29		43		37	
			6 V		14	25		37		31	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	80 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

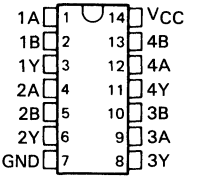
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC86 is characterized for operation from −40°C to 85°C.

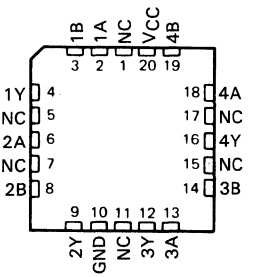
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54HC86 . . . J PACKAGE
SN74HC86 . . . D OR N PACKAGE
(TOP VIEW)

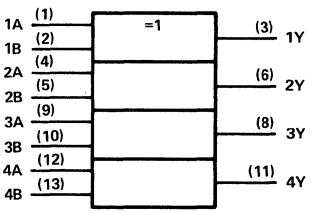


SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†

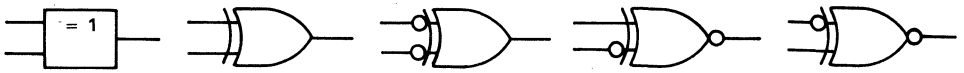


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

exclusive-OR logic

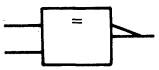
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



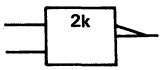
These are five equivalent Exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



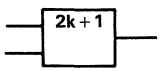
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC86			SN74HC86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH} (Totem-pole outputs)	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

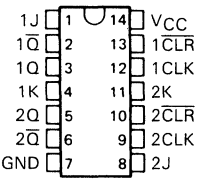
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC107 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC107 is characterized for operation from −40°C to 85°C.

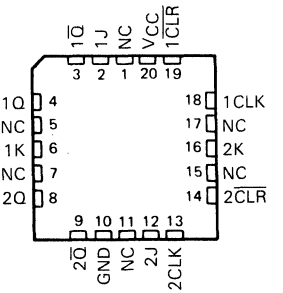
FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

SN54HC107 . . . J PACKAGE
SN74HC107 . . . D OR N PACKAGE
(TOP VIEW)

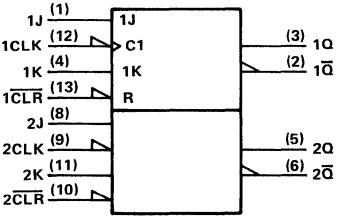


SN54HC107 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

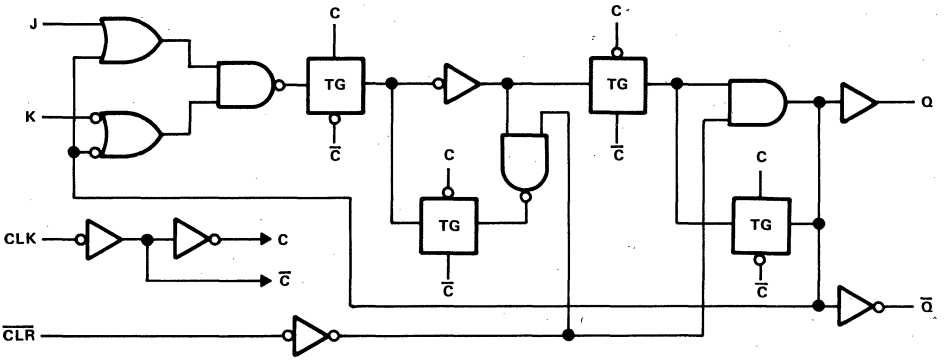
logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

2 HCMOS Devices

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC107			SN74HC107			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC20		SN74HC20		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC107		SN74HC107		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC107		SN74HC107		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	45		21		25		
			6 V	36	53		25		29		
t_{pd}	$\overline{CLR}$	Q or $\overline{Q}$	2 V		126	155		235		195	ns
			4.5 V		25	31		47		39	
			6 V		21	26		40		32	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		100	125		185		160	ns
			4.5 V		20	25		37		32	
			6 V		17	21		32		27	
t_t		Q or $\overline{Q}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-$\overline{K}$ negative-edge-triggered flip-flops. A low level at the Preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

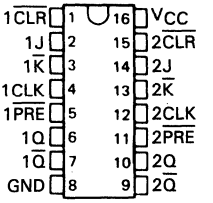
The SN54HC109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC109 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

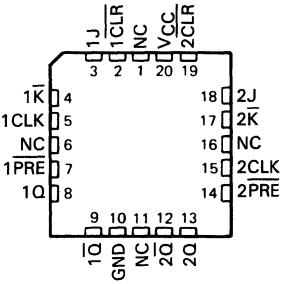
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

‡This configuration is nonstable; that is, it will not persist when Preset or Clear return to their inactive (high) level.

SN54HC109 . . . J PACKAGE
SN74HC109 . . . D OR N PACKAGE
(TOP VIEW)

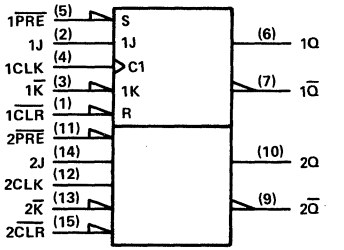


SN54HC109 . . . FK PACKAGE
(TOP VIEW)



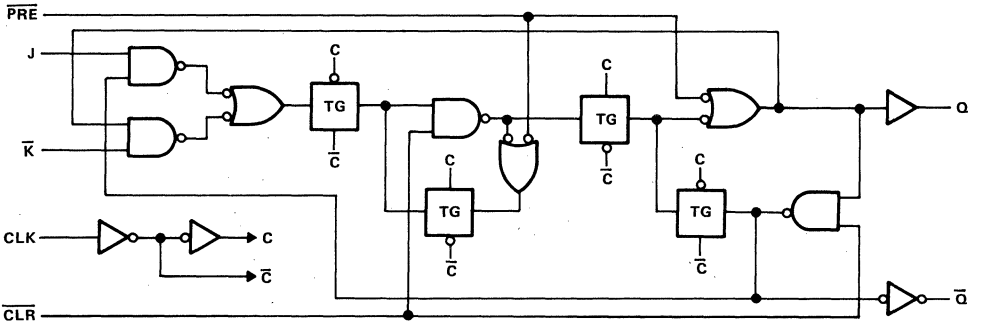
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC109			SN74HC109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_I		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC109		SN74HC109		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		60	230		345		290	ns
			4.5 V		15	46		69		58	
			6 V		12	39		59		49	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		50	175		250		220	ns
			4.5 V		15	35		50		44	
			6 V		12	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

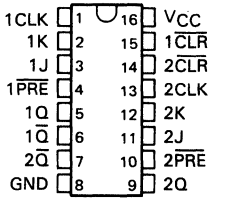
The SN54HC112 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC112 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

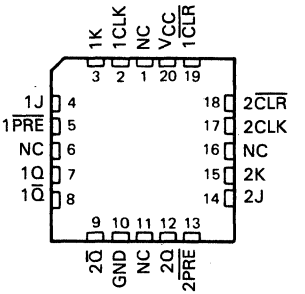
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

‡This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54HC112 . . . J PACKAGE
SN74HC112 . . . D OR N PACKAGE
(TOP VIEW)

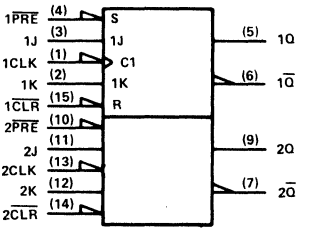


SN54HC112 . . . FK PACKAGE
(TOP VIEW)



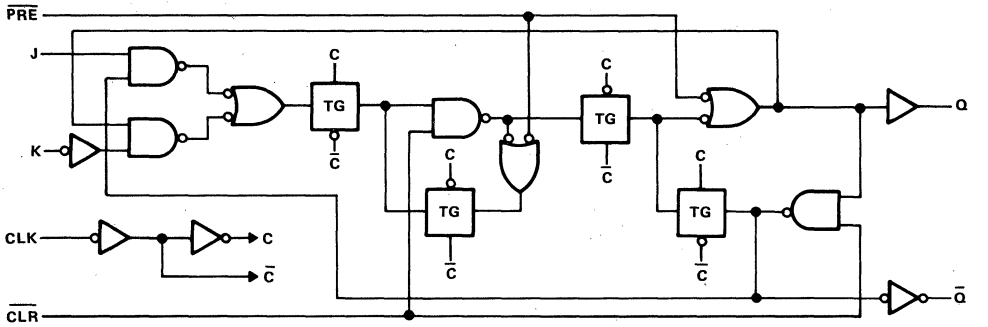
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC112			SN74HC112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC112		SN74HC112		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3.4	0	4	MHz
			4.5 V	0	25	0	17	0	20	
			6 V	0	29	0	20	0	24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	10		3.4		4		MHz
			4.5 V	25	50		17		20		
			6 V	29	60		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		54	165		245		205	ns
			4.5 V		16	33		49		41	
			6 V		13	28		42		35	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		56	125		185		155	ns
			4.5 V		16	25		37		31	
			6 V		13	21		31		26	
t_t		Q or $\overline{Q}$	2 V		29	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

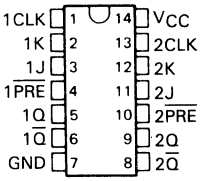
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC113 is characterized for operation from −40°C to 85°C.

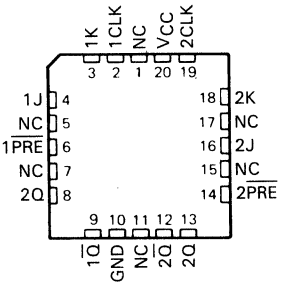
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

SN54HC113 . . . J PACKAGE
SN74HC113 . . . D OR N PACKAGE
(TOP VIEW)

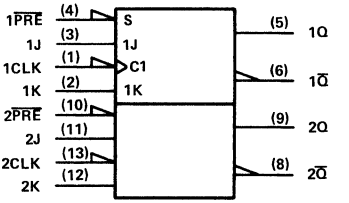


SN54HC113 . . . FK PACKAGE
(TOP VIEW)



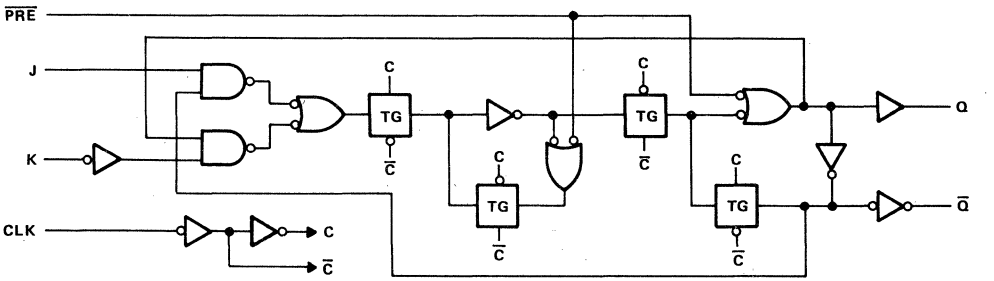
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC113			SN74HC113			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC113		SN74HC113		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC113		SN74HC113		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	$\overline{PRE}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC113		SN74HC113		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$	Q or $\overline{Q}$	2 V		60	165		250		205	ns
			4.5 V		18	33		50		41	
			6 V		15	28		43		35	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		85	140		211		175	ns
			4.5 V		19	28		42		35	
			6 V		16	24		36		30	
t_t		Q or Q	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When the Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

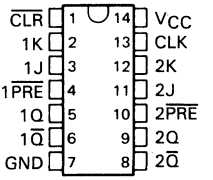
The SN54HC114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC114 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

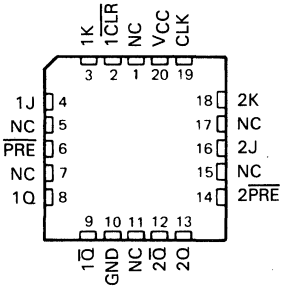
INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

‡This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54HC114 . . . J PACKAGE
SN74HC114 . . . D OR N PACKAGE
(TOP VIEW)

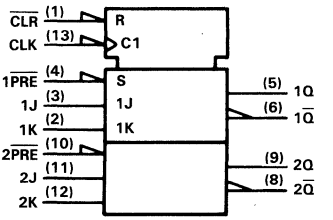


SN54HC114 . . . FK PACKAGE
(TOP VIEW)



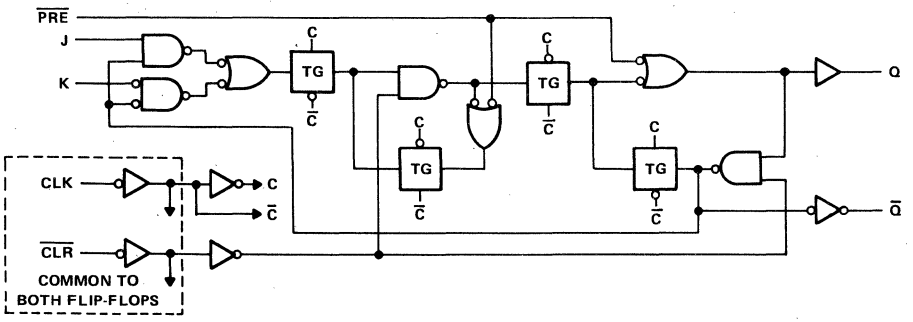
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC114			SN74HC114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC114		SN74HC114		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC114		SN74HC114		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3.4	0	4	MHz
			4.5 V	0	25	0	17	0	20	
			6 V	0	29	0	20	0	24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC114		SN74HC114		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	9		3.4		4		MHz
			4.5 V	25	45		17		20		
			6 V	29	50		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		75	175		250		220	ns
			4.5 V		20	35		50		44	
			6 V		17	30		42		37	
t_{pd}	CLK	Q or $\overline{Q}$	2 V		63	175		250		220	ns
			4.5 V		19	35		50		44	
			6 V		16	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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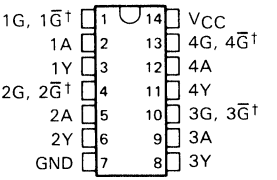
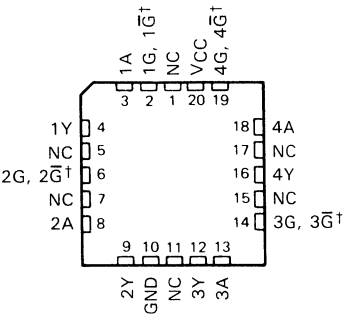
- **'High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC125, SN54HC126 . . . J PACKAGE
SN74HC125, SN74HC126 . . . N PACKAGE
(TOP VIEW)



SN54HC125, SN54HC126 . . . FK PACKAGE
(TOP VIEW)



†G̅ on 'HC125; G on 'HC126

NC – No internal connection

description

These bus buffers feature independent line drivers with three-state outputs. Each 'HC125 output is disabled when the associated G̅ is high, and each 'HC126 output is disabled when the associated G is low.

The SN54HC125 and SN54HC126 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC125 and SN74HC126 are characterized for operation from −40°C to 85°C.

FUNCTION TABLES

'HC125 (EACH BUFFER)

INPUTS		OUTPUT
G̅	A	Y
L	H	H
L	L	L
H	X	Z

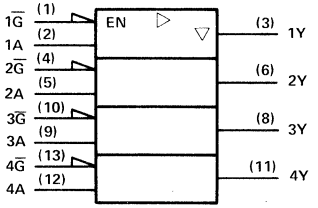
'HC126 (EACH BUFFER)

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

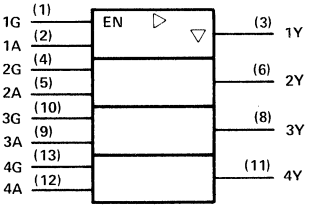
H = high level, L = low level, X = irrelevant

logic symbols†

'HC125



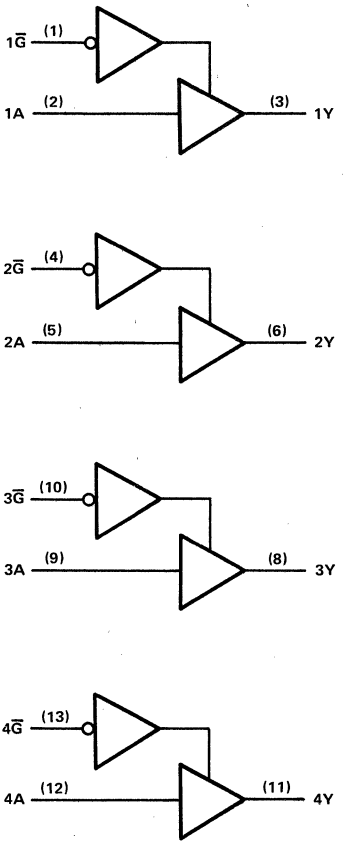
'HC126



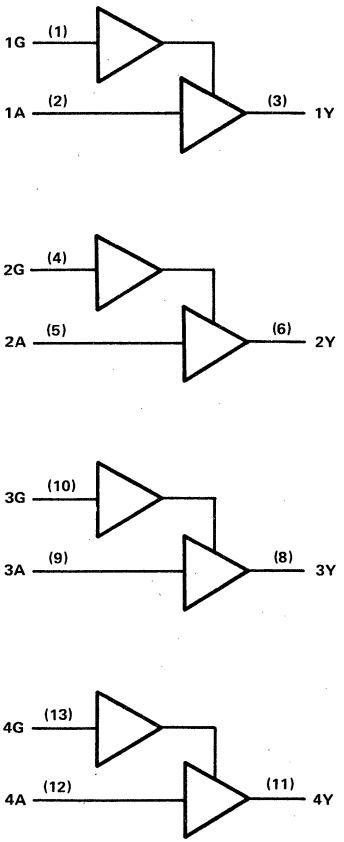
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'HC125



'HC126



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC125 SN54HC126			SN74HC125 SN74HC126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC125 SN54HC126		SN74HC125 SN74HC126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A † 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		48	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{en}	$\overline{G}$	Y	2 V		53	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{dis}	$\overline{G}$	Y	2 V		30	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		14	20		31		26	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	45 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		67	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		32	
t_{en}	$\overline{G}$	Y	2 V		100	135		200		170	ns
			4.5 V		20	27		40		34	
			6 V		17	23		34		29	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC126		SN74HC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		47	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{en}	G	Y	2 V		57	120		180		150	ns
			4.5 V		16	24		36		30	
			6 V		12	20		31		26	
t_{dis}	G	Y	2 V		35	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		15	20		31		26	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	45 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC126		SN74HC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		67	150		225		188	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		33	
t_{en}	G	Y	2 V		100	135		202		169	ns
			4.5 V		20	27		40		36	
			6 V		17	23		36		30	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: *Load circuit and voltage waveforms are shown in Section 1.*

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Operation from Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC00**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. It performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

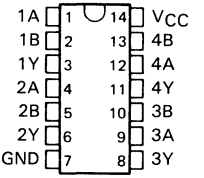
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC132 is characterized for operation from −40°C to 85°C.

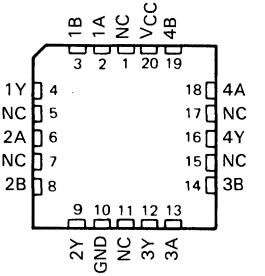
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54HC132 . . . J PACKAGE
SN74HC132 . . . D OR N PACKAGE
(TOP VIEW)

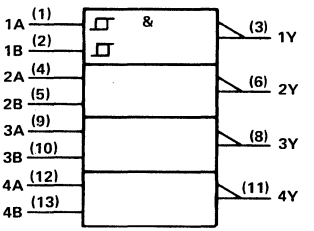


SN54HC132 . .. FK PACKAGE
(TOP VIEW)



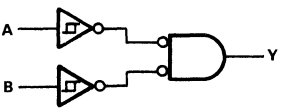
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC132			SN74HC132			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}		2 V	0.70	1.2	1.50	0.70	1.50	0.70	1.50	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
		6 V	2.10	3.3	4.20	2.10	4.20	2.10	4.20	
V_{T-}		2 V	0.30	0.6	1.00	0.30	1.00	0.30	1.00	V
		4.5 V	0.90	1.6	2.45	0.90	2.45	0.90	2.45	
		6 V	1.20	2.0	3.20	1.20	3.20	1.20	3.20	
$V_{T+} - V_{T-}$		2 V	0.20	0.6	1.20	0.20	1.20	0.20	1.20	V
		4.5 V	0.40	0.9	2.10	0.40	2.10	0.40	2.10	
		6 V	0.50	1.3	2.50	0.50	2.50	0.50	2.50	
I_I	V_I = V_{CC} or 0	6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	120		186		156	ns
			4.5 V		18	25		37		31	
			6 V		14	21		32		27	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 13-input NAND gate. They perform the Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M} \quad \text{or}$$

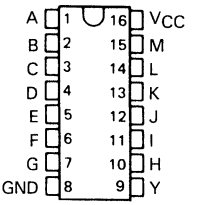
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54HC133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC133 is characterized for operation from −40°C to 85°C.

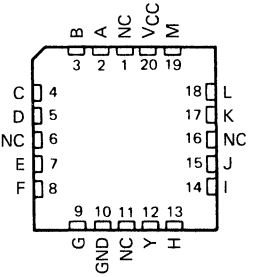
FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

SN54HC133 . . . J PACKAGE
SN74HC133 . . . D OR N PACKAGE
(TOP VIEW)

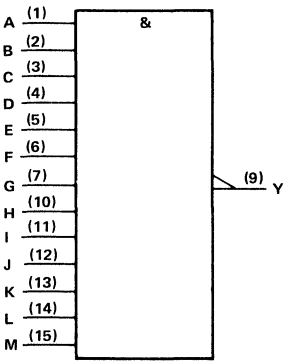


SN54HC133 . . . FK PACKAGE
(TOP VIEW)

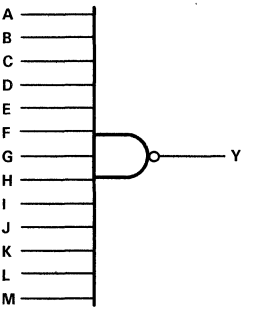


NC—No internal connection

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC133			SN74HC133			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC133		SN74HC133		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

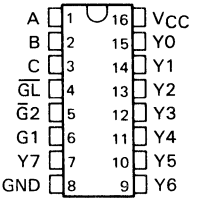
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC133		SN74HC133		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any	Y	2 V		70	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		13	26		38		33	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	24 pF typ

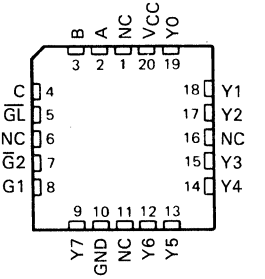
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC137 . . . J PACKAGE
SN74HC137 . . . D/DW‡ OR N PACKAGE
(TOP VIEW)



SN54HC137 . . . FK PACKAGE
(TOP VIEW)



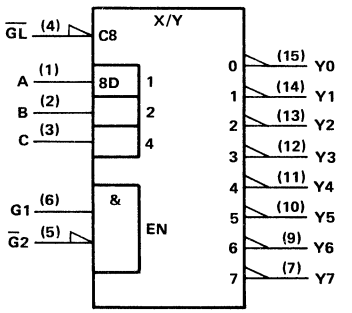
NC—No internal connection
‡Contact the factory for D/DW availability

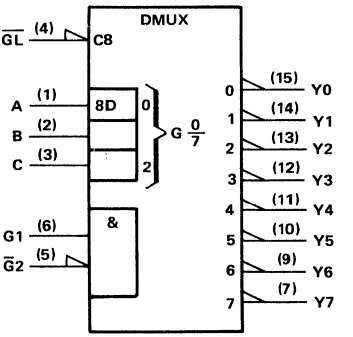
description

The 'HC137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HC137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HC137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HC137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC137 is characterized for operation from −40°C to 85°C.

logic symbols† (alternatives)



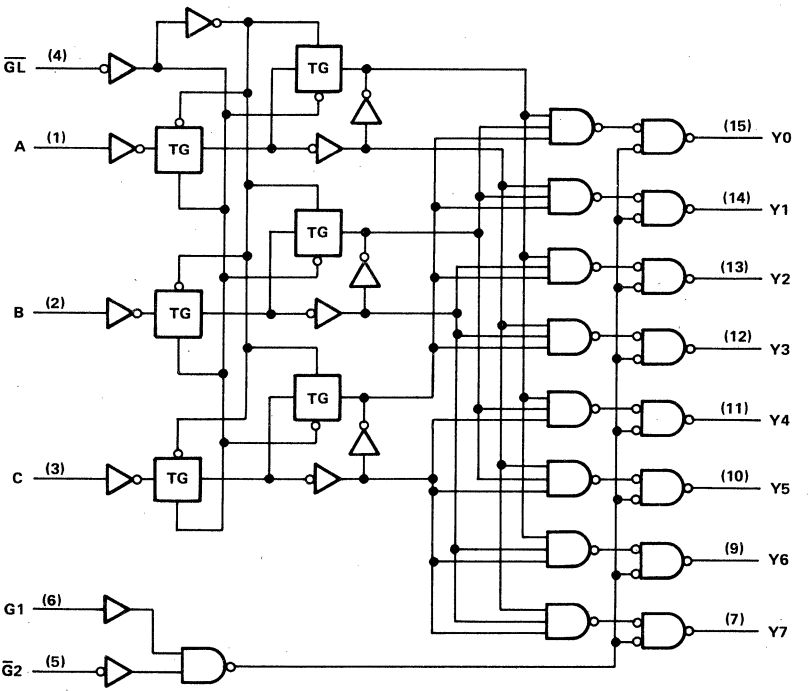


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW‡, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

logic diagram (positive logic)



Pin numbers shown are for D/DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC137			SN74HC137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC137		SN74HC137		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC137		SN74HC137		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{GL}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, A, B, and C before $\overline{GL}$↑	2 V	75		115		95		ns
		4.5 V	15		23		19		
		6 V	13		20		16		
t_h	Hold time, A, B, and C after $\overline{GL}$↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

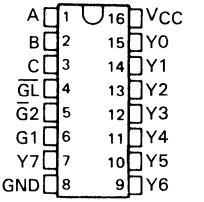
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC137		SN74HC137		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C	Y	2 V		82	190		285		240	ns
			4.5 V		23	38		57		48	
			6 V		19	32		48		41	
t_{pd}	$\overline{G2}$	Y	2 V		59	145		220		180	ns
			4.5 V		17	29		44		36	
			6 V		14	25		37		31	
t_{pd}	G1	Y	2 V		61	145		220		180	ns
			4.5 V		17	29		44		36	
			6 V		14	25		37		31	
t_{pd}	$\overline{GL}$	Y	2 V		77	190		285		240	ns
			4.5 V		22	38		57		48	
			6 V		19	32		48		41	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

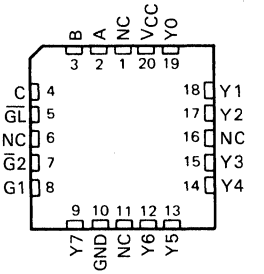
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT137 . . . J PACKAGE
SN74HCT137 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT137 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

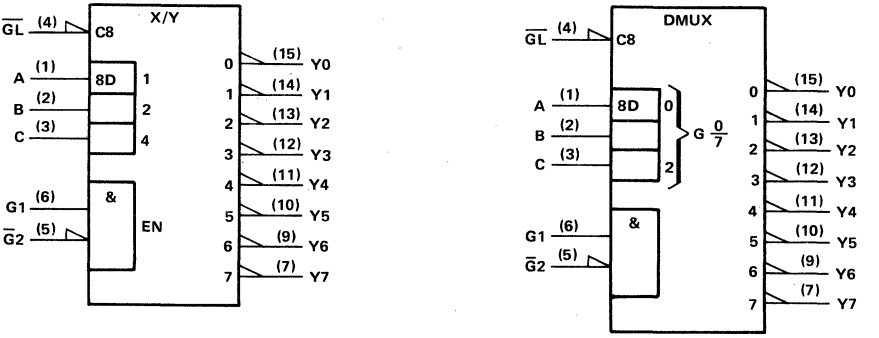
The 'HCT137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HCT137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HCT137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HCT137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT137 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

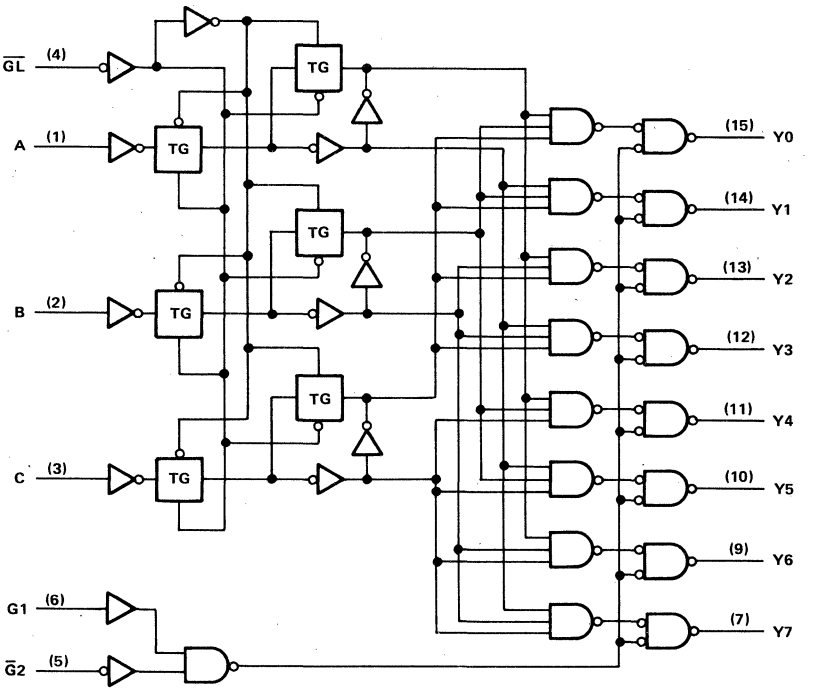
INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

logic symbol (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCT137			SN74HCT137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL} Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT137		SN74HCT137		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3.0		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	T_A = 25°C			SN54HCT137		SN74HCT137		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{GL}$ low	4.5 V	26			39		33		ns
		5.5 V	23			35		30		
t_{su}	Setup time, A, B, and C before $\overline{GL}$↑	4.5 V	15			23		19		ns
		5.5 V	14			21		17		
t_h	Hold time, A, B, and C after $\overline{GL}$↑	4.5 V	5			5		5		ns
		5.5 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT137		SN74HCT137		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C	Y	4.5 V		25	38		57		48	ns
			5.5 V		20	34		51		43	
t_{pd}	$\overline{G2}$	Y	4.5 V		20	29		44		36	ns
			5.5 V		17	25		40		32	
t_{pd}	G1	Y	4.5 V		20	29		44		36	ns
			5.5 V		17	25		40		32	
t_{pd}	$\overline{GL}$	Y	4.5 V		32	42		63		52	ns
			5.5 V		25	36		57		47	
t_t		Any	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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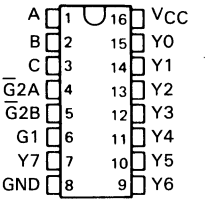
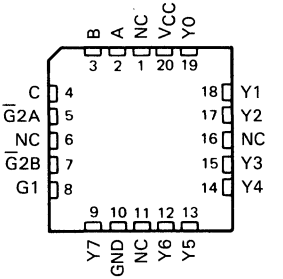
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC138 . . . J PACKAGE
SN74HC138 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

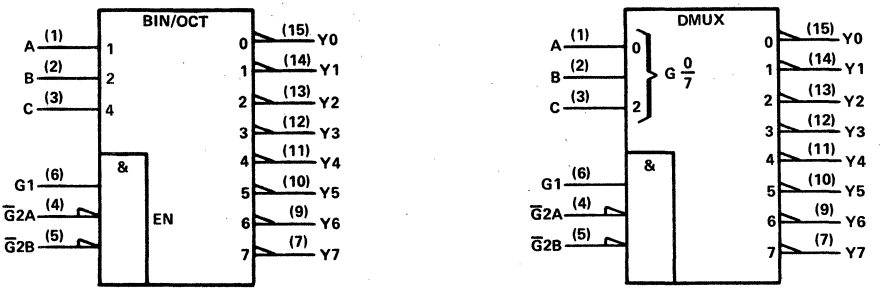
description

The 'HC138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs at the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

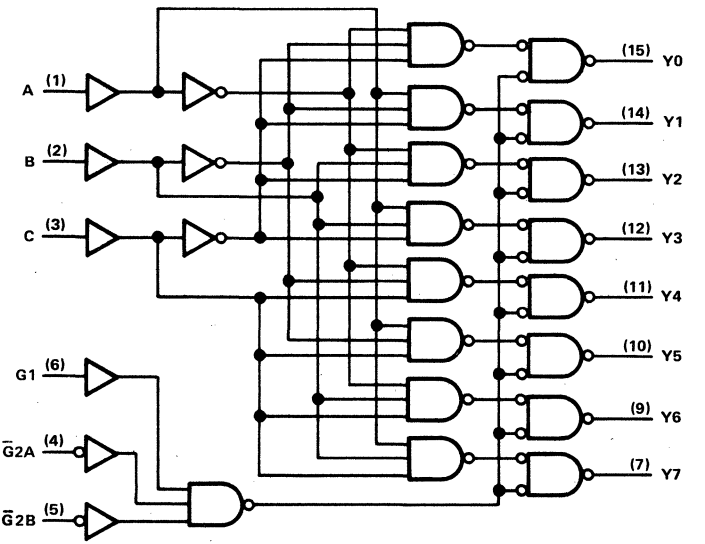
The SN54HC138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC138 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
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FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC138			SN74HC138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC138		SN74HC138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC138		SN74HC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	2 V		67	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		15	31		46		38	
t_{pd}	Enable	Any Y	2 V		66	155		235		195	ns
			4.5 V		18	31		47		39	
			6 V		15	26		40		33	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

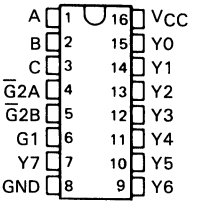
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

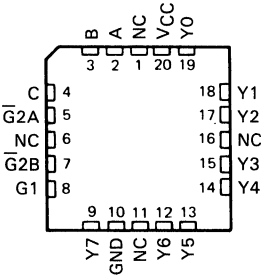
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT138 . . . J PACKAGE
SN74HCT138 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

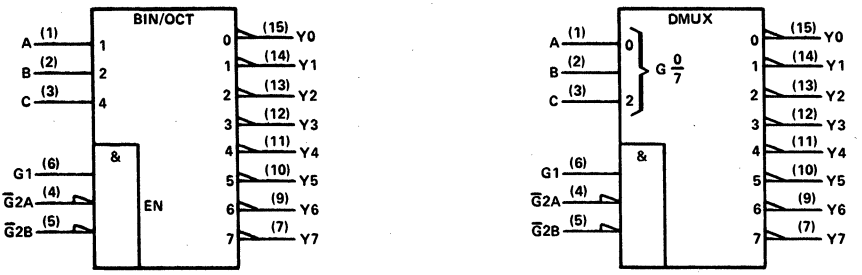
description

The 'HCT138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

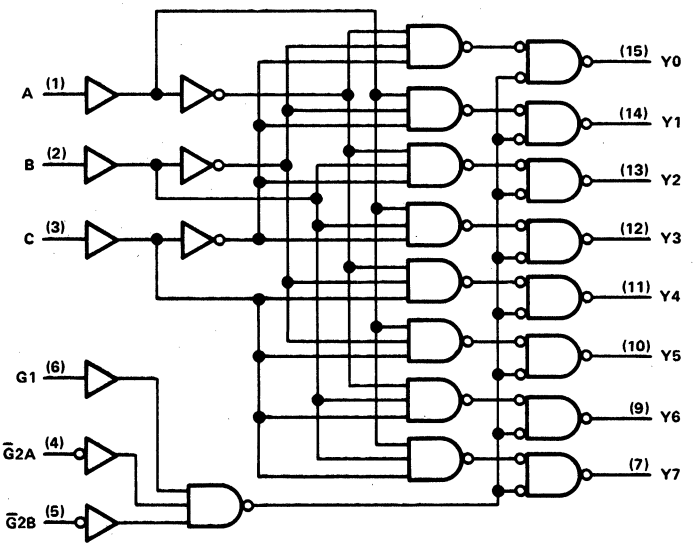
The SN54HCT138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT138 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/ or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCT138			SN74HCT138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL} Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3.0		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	4.5 V		23	36		54		45	ns
			5.5 V		17	32		49		34	
t_{pd}	Enable	Any Y	4.5 V		22	33		50		42	ns
			5.5 V		18	30		45		38	
t_t		Any	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

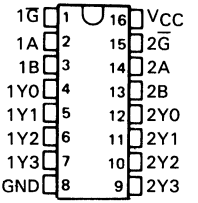
description

The 'HC139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

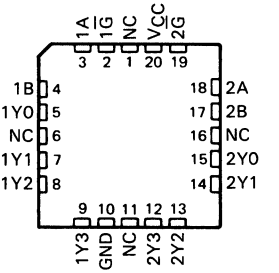
The 'HC139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HC139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC139 is characterized for operation from −40°C to 85°C.

SN54HC139 . . . J PACKAGE
SN74HC139 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC139 . . . FK PACKAGE
(TOP VIEW)



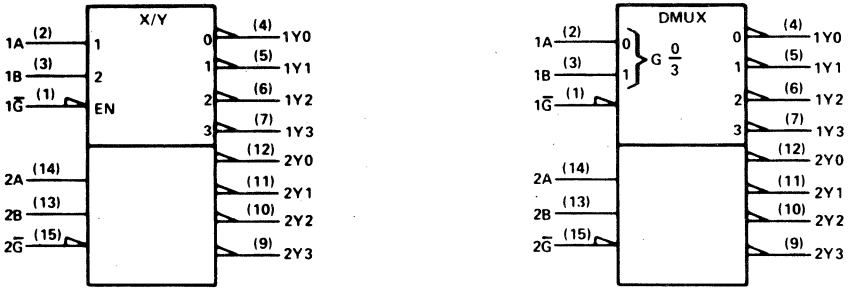
NC—No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

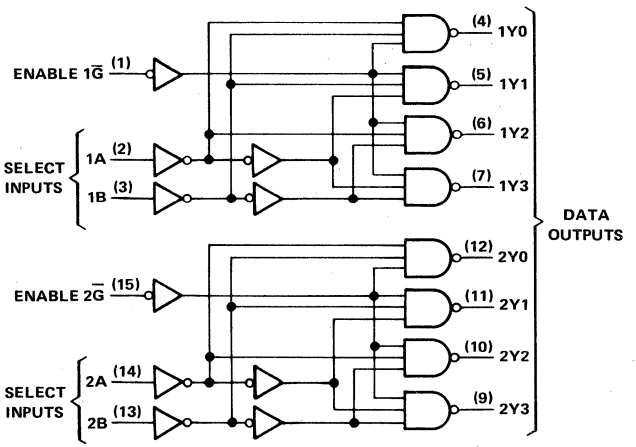
2 HCMOS Devices

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC139			SN74HC139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC139		SN74HC139		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC139		SN74HC139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		47	175		255		220	ns
			4.5 V		14	35		51		44	
			6 V		12	30		44		38	
t_{pd}	$\overline{G}$	Y	2 V		39	175		255		220	ns
			4.5 V		11	35		51		44	
			6 V		10	30		44		38	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per decoder	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

D2844, MARCH 1984—REVISED SEPTEMBER 1987

'HC147

- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:
  Keyboard Encoding
  Range Selection

'HC148

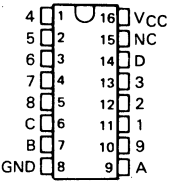
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  N-Bit Encoding
  Code Converters and Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

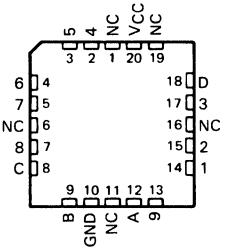
These encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'HC147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The 'HC148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

The SN54HC147 and SN54HC148 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC147 and SN74HC148 are characterized for operation from −40°C to 85°C.

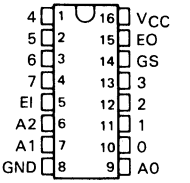
SN54HC147 . . . J PACKAGE
SN74HC147 . . . DW OR N PACKAGE
(TOP VIEW)



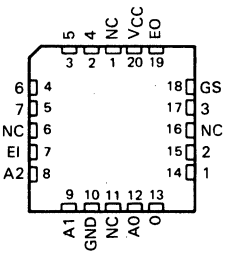
SN54HC147 . . . FK PACKAGE
(TOP VIEW)



SN54HC148 . . . J PACKAGE
SN74HC148 . . . D/DW† OR N PACKAGE
(TOP VIEW)



SN54HC148 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

†Contact the factory for D or DW availability.

'HC147
FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

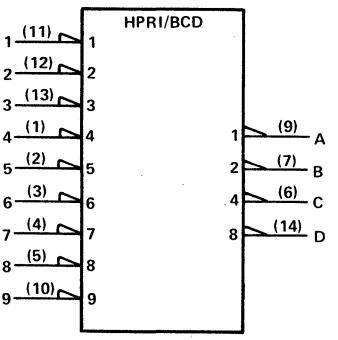
'HC148
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

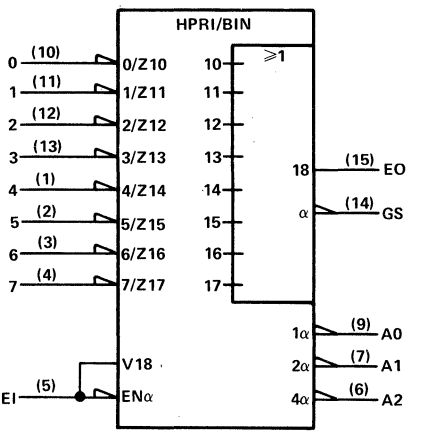
H = high logic level, L = low logic level, X = irrelevant

logic symbols†

'HC147



'HC148

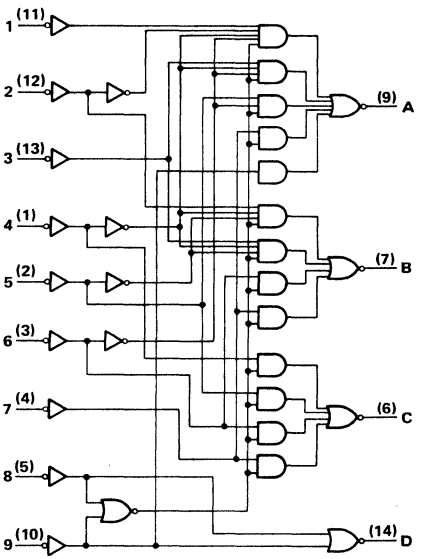


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW, J, and N packages.

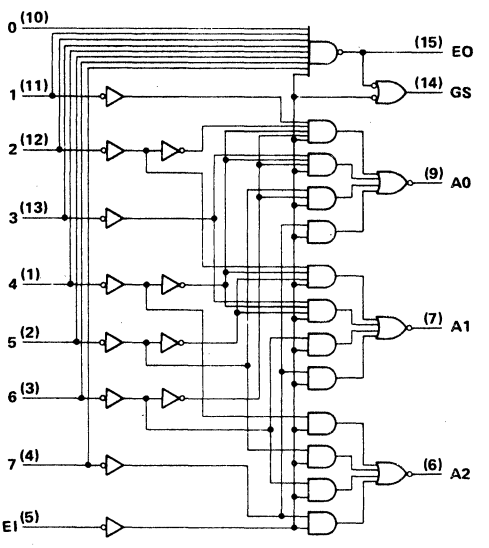
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic diagrams (positive logic)

'HC147



'HC148



Pin numbers shown are for D/DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC147 SN54HC148			SN74HC147 SN74HC148			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC147 SN54HC148		SN74HC147 SN74HC148		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

'HC147 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC147		SN74HC147		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any	Any	2 V		75	190		285		240	ns
			4.5 V		25	38		57		48	
			6 V		21	32		48		41	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

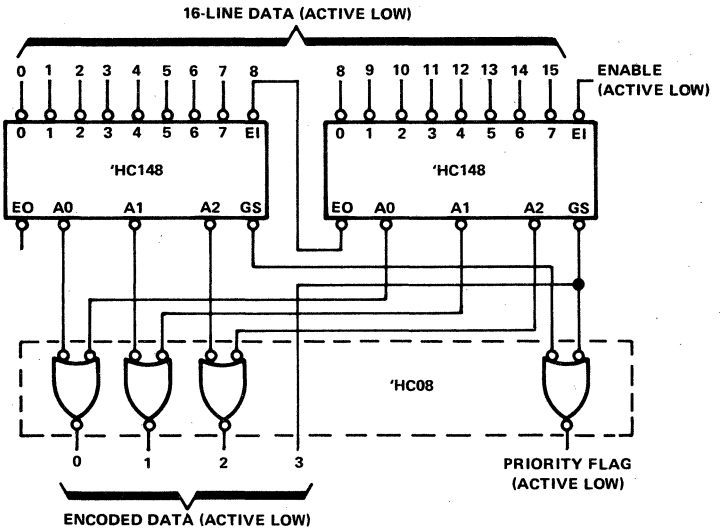
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

'HC148 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC148		SN74HC148		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	1−7	A0, A1, or A2	2 V		69	180		270		225	ns
			4.5 V		23	36		54		45	
			6 V		21	31		46		38	
t_{pd}	0−7	EO	2 V		60	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		17	26		38		33	
t_{pd}	0−7	GS	2 V		75	190		285		240	ns
			4.5 V		25	38		57		48	
			6 V		21	32		48		41	
t_{pd}	EI	A0, A1, or A2	2 V		78	195		295		245	ns
			4.5 V		26	39		59		49	
			6 V		22	33		50		42	
t_{pd}	EI	GS	2 V		57	145		220		180	ns
			4.5 V		19	29		44		36	
			6 V		16	25		38		31	
t_{pd}	EI	EO	2 V		66	165		250		205	ns
			4.5 V		22	33		50		41	
			6 V		19	28		43		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA



PRIORITY ENCODER FOR 16 BITS

Since the 'HC147 and 'HC148 are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the 'HC148, a change from high to low at input EI can cause a transient low on the GS output when all inputs are high. This must be considered when strobing the outputs.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **8-Line to 1-Line Multiplexers Can Perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Both Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-Mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

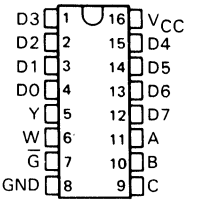
The SN54HC151 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC151 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

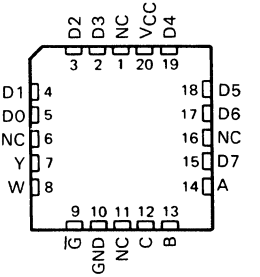
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

SN54HC151 . . . J PACKAGE
SN74HC151 . . . D OR N PACKAGE
(TOP VIEW)

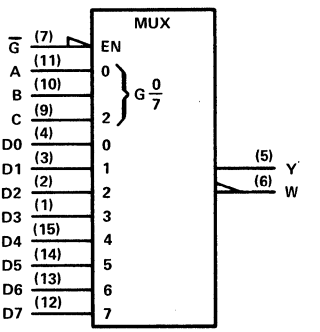


SN54HC151 . . . FK PACKAGE
(TOP VIEW)



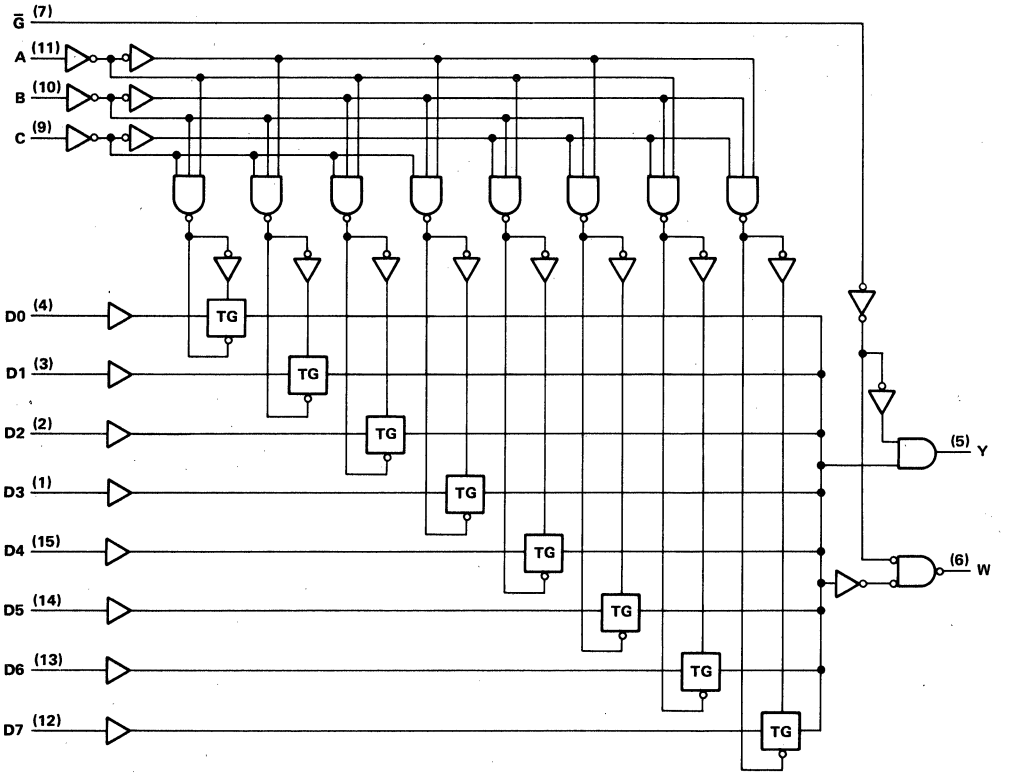
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC151			SN74HC151			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2 V		94	250		360		312	ns
			4.5 V		30	50		73		63	
			6 V		25	43		62		54	
t_{pd}	Any D	Y or W	2 V		74	195		283		244	ns
			4.5 V		23	39		57		49	
			6 V		20	33		48		41	
t_{pd}	$\overline{G}$	Y or W	2 V		49	127		185		159	ns
			4.5 V		15	25		37		32	
			6 V		13	22		32		28	
t_t			2 V		22	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	70 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2 V		107	350		525		440	ns
			4.5 V		33	70		105		88	
			6 V		30	59		89		76	
t_{pd}	Any D	Y or W	2 V		90	275		415		345	ns
			4.5 V		29	51		83		69	
			6 V		25	47		72		59	
t_{pd}	$\overline{G}$	Y or W	2 V		67	205		310		255	ns
			4.5 V		21	41		62		51	
			6 V		18	35		53		43	
t_t			2 V		51	210		315		265	ns
			4.5 V		16	42		63		53	
			6 V		14	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Selects One-of-Eight Data Sources**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired one-of-eight data sources.

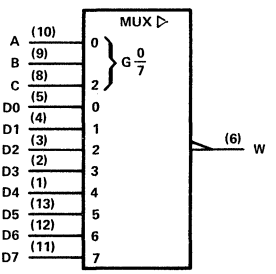
The SN54HC152 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC152 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

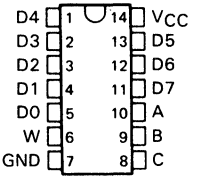
H = high level, L = low level

logic symbol†

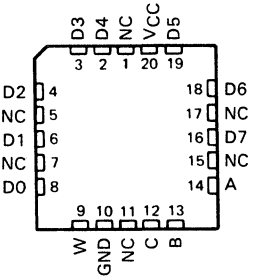


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC152 . . . J PACKAGE
SN74HC152 . . . D OR N PACKAGE
(TOP VIEW)

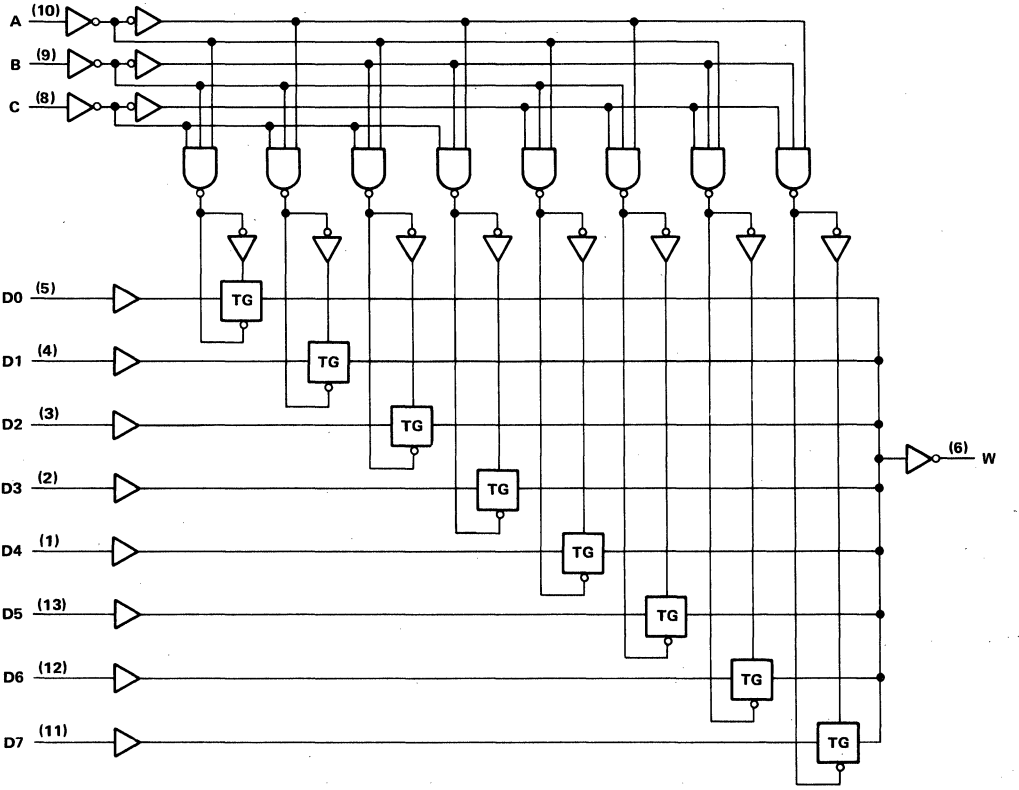


SN54HC152 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC152			SN74HC152			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC152		SN74HC152		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC152		SN74HC152		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W	2 V		50	170		255		213	ns
			4.5 V		18	34		51		43	
			6 V		16	29		43		36	
t_{pd}	Any D	W	2 V		38	130		195		163	ns
			4.5 V		14	26		39		33	
			6 V		12	22		33		28	
t_t		W	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	70 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC152		SN74HC152		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W	2 V		63	225		385		318	ns
			4.5 V		22	51		77		64	
			6 V		19	44		66		55	
t_{pd}	Any D	W	2 V		52	215		325		268	ns
			4.5 V		18	43		65		54	
			6 V		16	37		55		47	
t_t		W	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

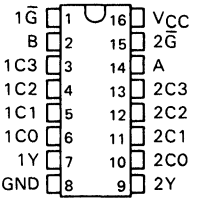
The SN54HC153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC153 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

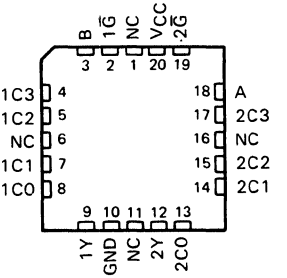
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

SN54HC153 . . . J PACKAGE
SN74HC153 . . . D/DW† OR N PACKAGE
(TOP VIEW)



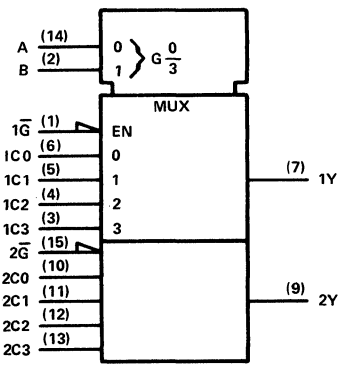
SN54HC153 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

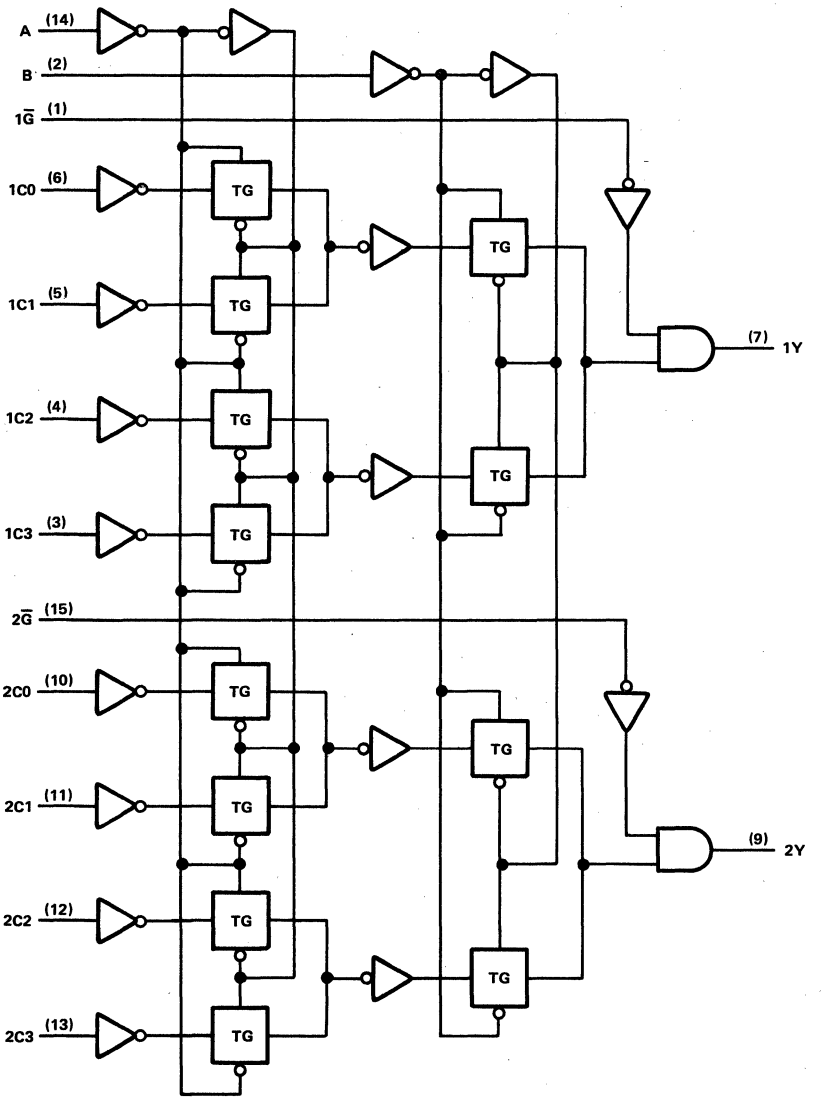
†Contact the factory for D or DW availability.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D/DW†, J, and N packages.

†Contact the factory for D or DW availability.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC153			SN74HC153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		90	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		17	26		38		32	
t_{pd}	Data (Any C)	Y	2 V		73	126		189		158	ns
			4.5 V		17	28		42		35	
			6 V		14	23		35		29	
t_{pd}	G	Y	2 V		38	95		150		125	ns
			4.5 V		11	19		28		24	
			6 V		9	16		24		20	
t_t		Y	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		105	235		355		295	ns
			4.5 V		27	47		71		59	
			6 V		21	41		60		51	
t_{pd}	Data (Any C)	Y	2 V		93	220		335		274	ns
			4.5 V		23	44		67		55	
			6 V		19	38		57		48	
t_{pd}	G	Y	2 V		60	185		280		230	ns
			4.5 V		17	37		56		46	
			6 V		14	32		48		40	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

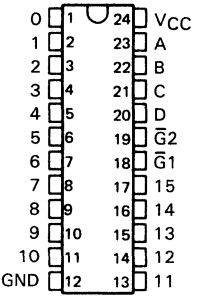
- **Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs**
- **Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

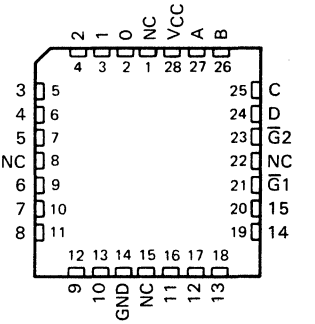
Each of these monolithic, 4-line to 16-line decoders decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders.

The SN54HC154 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC154 is characterized for operation from −40°C to 85°C.

SN54HC154 . . . JT PACKAGE
SN74HC154 . . . DW OR NT PACKAGE
(TOP VIEW)



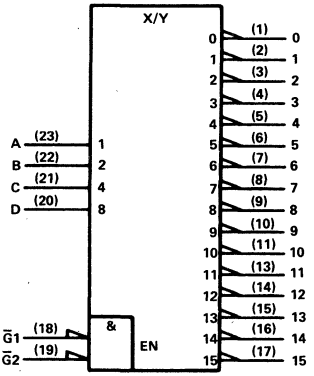
SN54HC154 . . . FK PACKAGE
(TOP VIEW)

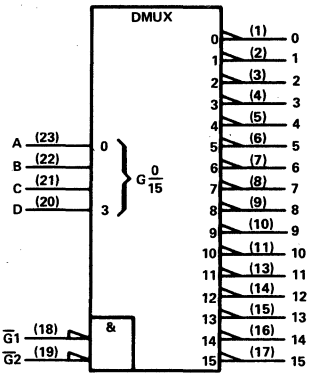


NC—No internal connection

2 HCMOS Devices

logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrevelant

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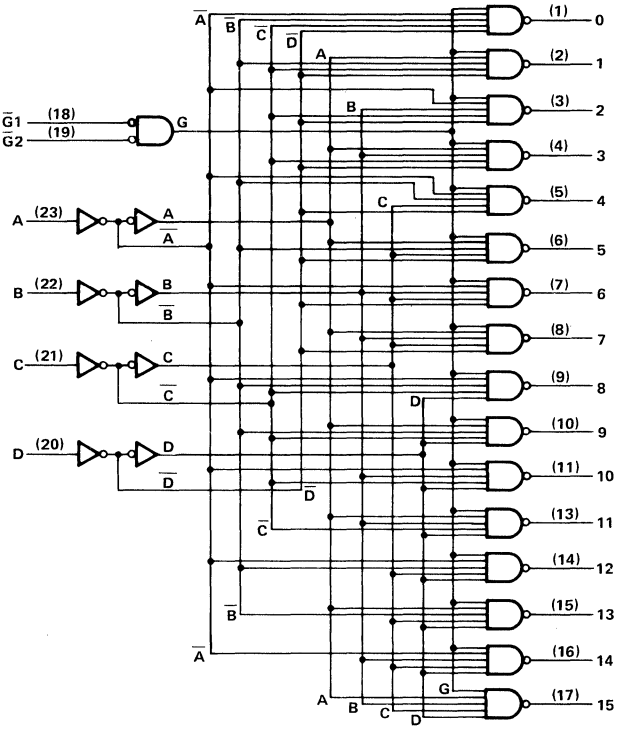
logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC154			SN74HC154			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC154		SN74HC154		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC154		SN74HC154		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Any	2 V		72	180		270		225	ns
			4.5 V		24	36		54		45	
			6 V		20	31		46		38	
t_{pd}	$\overline{G}1$ or $\overline{G}2$	Any	2 V		72	180		270		225	ns
			4.5 V		24	36		54		45	
			6 V		20	31		46		38	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	96 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'HC157 presents true data whereas the 'HC158 presents inverted data.

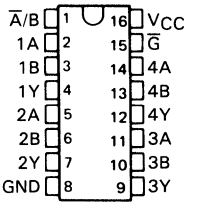
The SN54HC157 and SN54HC158 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC157 and SN74HC158 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

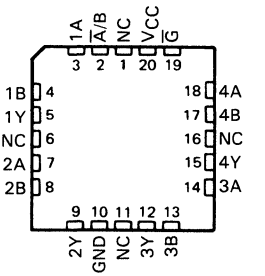
INPUTS				OUTPUT Y	
STROBE	SELECT	DATA		'HC157	'HC158
$\overline{G}$	$\overline{A}$/B	A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

SN54HC157, SN54HC158 . . . J PACKAGE
SN74HC157, SN74HC158 . . . D/DW† OR N PACKAGE
(TOP VIEW)



SN54HC157, SN54HC158 . . . FK PACKAGE
(TOP VIEW)

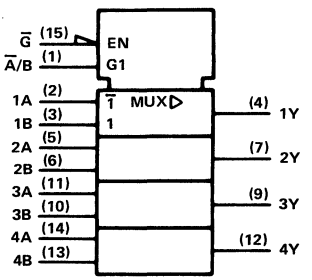


NC—No internal connection

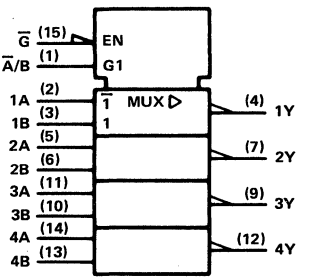
†Contact the factory for D or DW availability.

logic symbols‡

'HC157



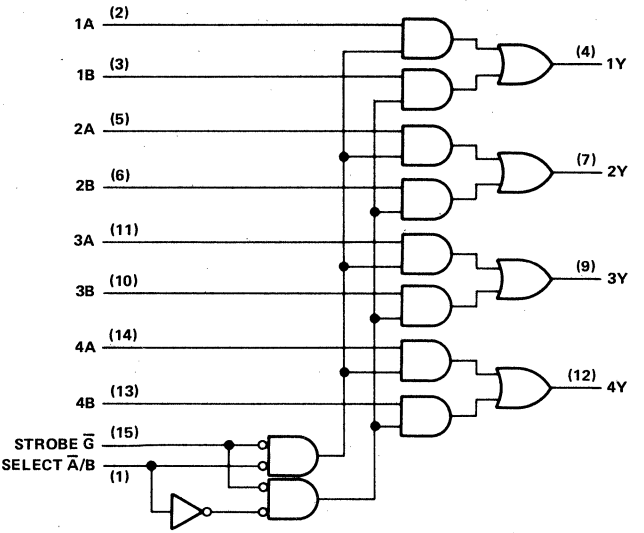
'HC158



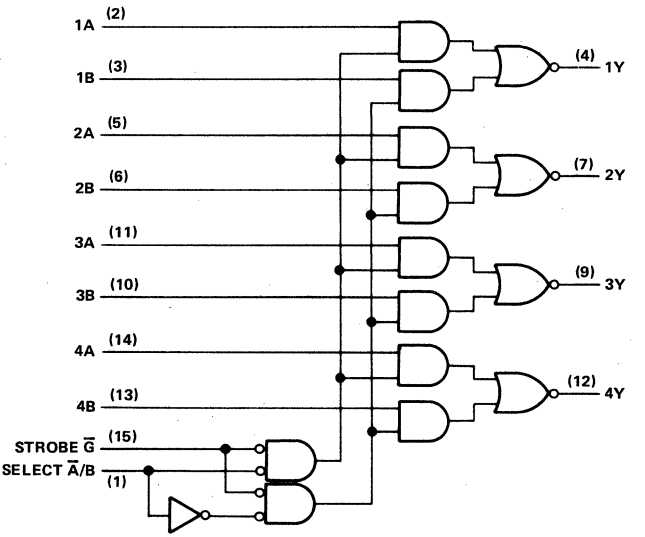
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW, J, and N packages.

logic diagrams (positive logic)

'HC157



'HC158



Pin numbers shown are for D/DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC157 SN54HC158			SN74HC157 SN74HC158			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC157 SN54HC158		SN74HC157 SN74HC158		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC157 SN54HC158		SN74HC157 SN74HC158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		63	125		190		160	ns
			4.5 V		13	25		38		32	
			6 V		11	21		32		27	
t_{pd}	$\overline{A}$/B	Y	2 V		67	125		190		160	ns
			4.5 V		18	25		38		31	
			6 V		14	21		32		27	
t_{pd}	$\overline{G}$	Y	2 V		59	115		170		145	ns
			4.5 V		16	23		34		29	
			6 V		13	20		29		25	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

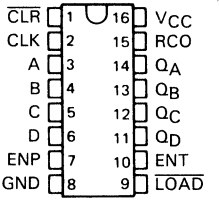
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC157 SN54HC158		SN74HC157 SN74HC158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		81	190		290		235	ns
			4.5 V		23	38		58		47	
			6 V		18	33		49		41	
t_{pd}	$\overline{A}$/B	Y	2 V		81	210		320		260	ns
			4.5 V		23	42		64		52	
			6 V		18	36		54		45	
t_{pd}	$\overline{G}$	Y	2 V		91	190		290		235	ns
			4.5 V		24	38		58		47	
			6 V		18	33		49		41	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

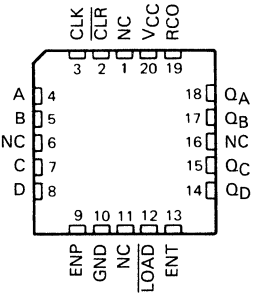
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Internal Look Ahead for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC' . . . J PACKAGE
SN74HC' . . . D OR N PACKAGE
(TOP VIEW)



SN54HC' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC160 and 'HC162 are decade counters, and the 'HC161 and 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'HC160 and 'HC161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'HC162 and 'HC163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock input, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bits synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54HC160 through SN54HC163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC160 through SN74HC163 are characterized for operation from −40°C to 85°C.

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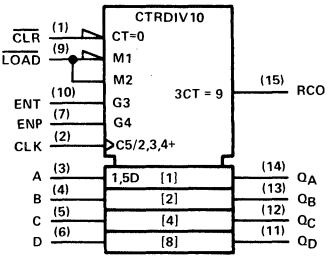
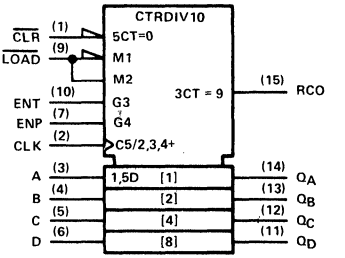
logic symbols†

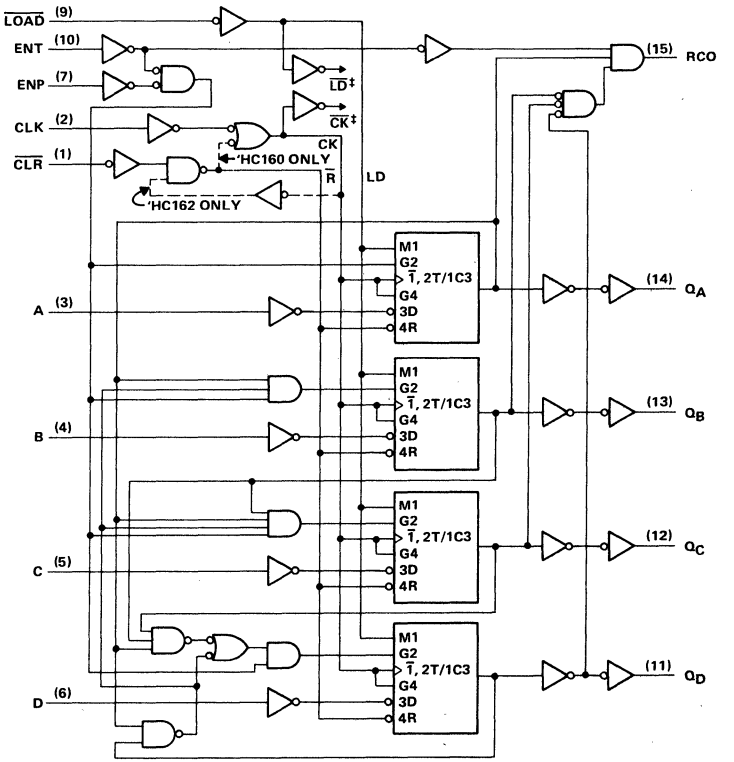
'HC160 DECADE COUNTER
WITH DIRECT CLEAR



'HC162 DECADE COUNTER
WITH SYNCHRONOUS CLEAR



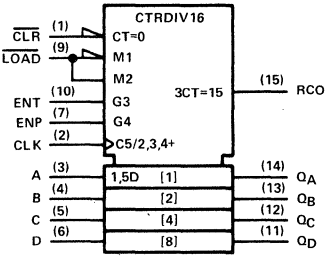
'HC160 and 'HC162 logic diagram (positive logic)



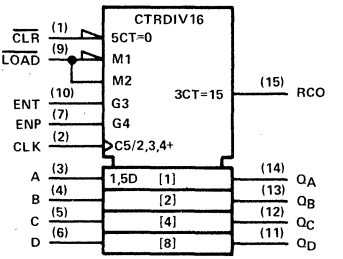
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
‡ For the sake of simplicity, the routing of the complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.
Pin numbers shown are for D, J, and N packages.

logic symbols†

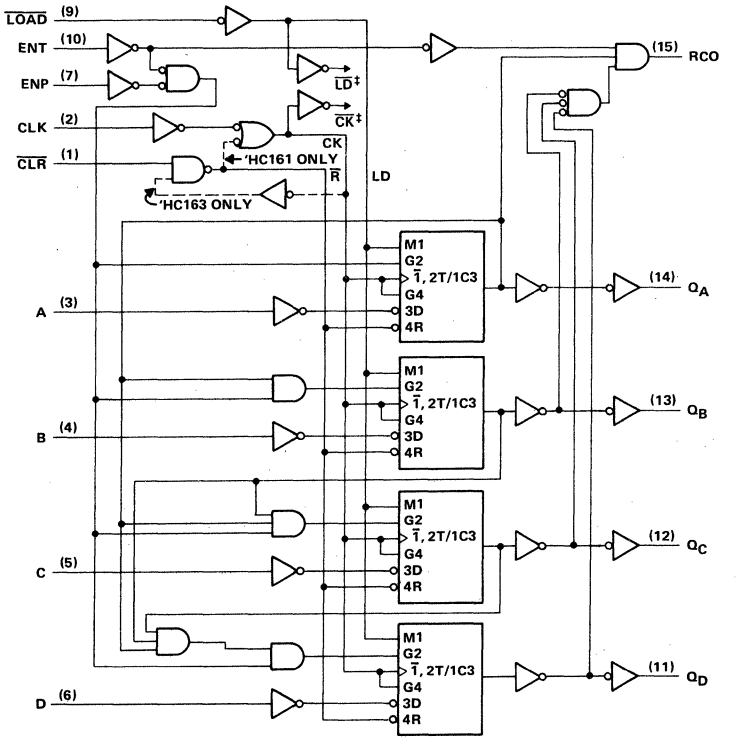
'HC161 BINARY COUNTER WITH DIRECT CLEAR



'HC163 BINARY COUNTER WITH SYNCHRONOUS CLEAR



'HC161 and 'HC163 logic diagram (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

‡ For the sake of simplicity, the routing of the complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for D, J, and N packages.

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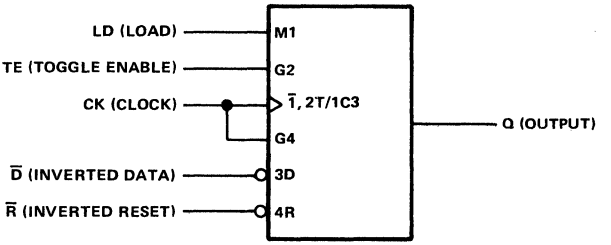
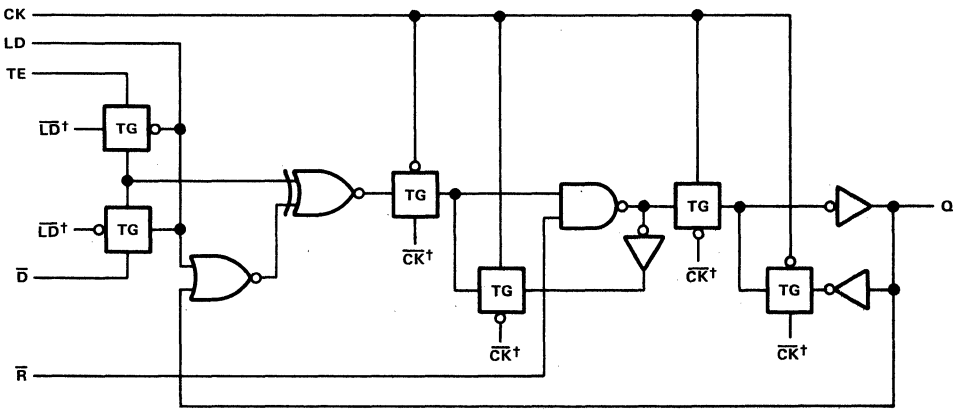
logic symbol, each D/T flip-flop (positive logic)



logic diagram, each D/T flip-flop (positive logic)

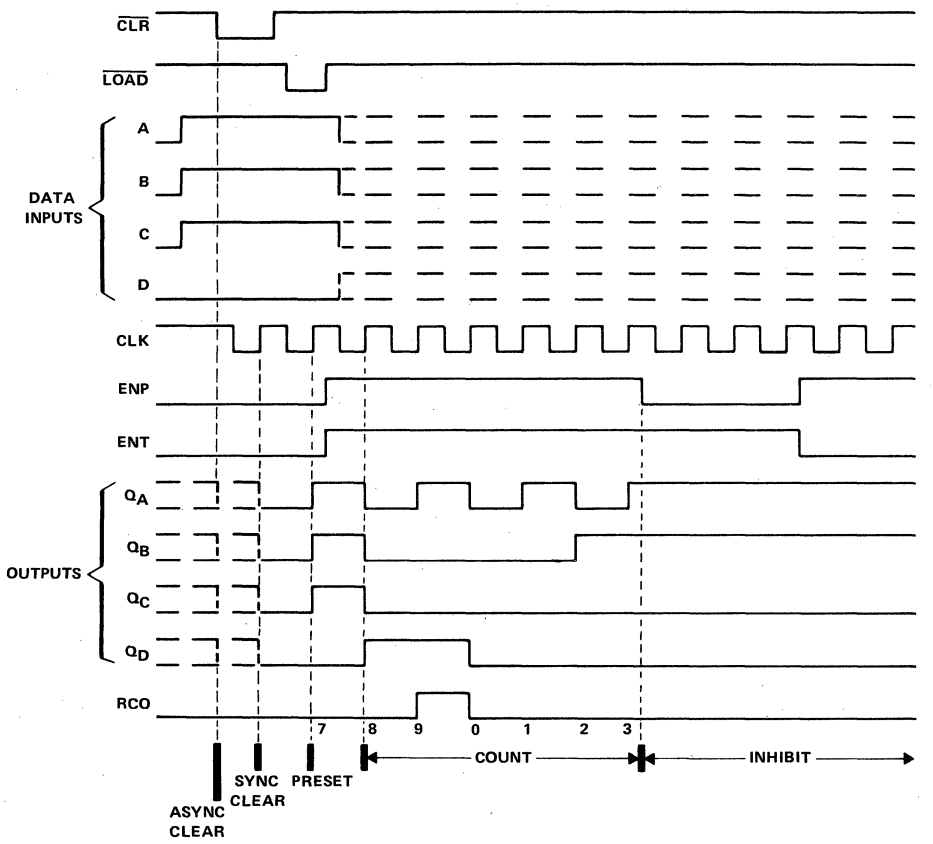


† The origins of the signals $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagrams of the overall devices.

'HC160 and 'HC162 output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC160 and SN74HC160 are asynchronous; SN54HC162 and SN74HC162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



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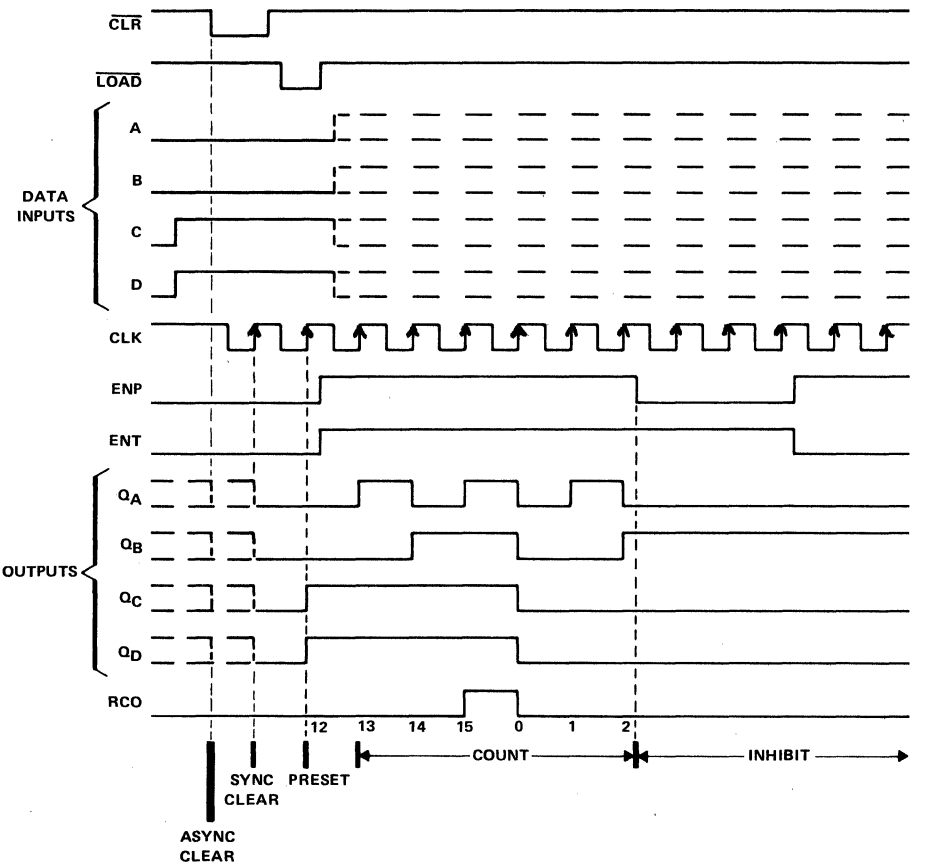
'HC161 and 'HC163 output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC161 and SN74HC161 are asynchronous; SN54HC163 and SN74HC163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC'			SN74HC'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC'		SN74HC'		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	T_A = 25°C		SN54HC160 THRU SN54HC163		SN74HC160 THRU SN74HC163		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{CLR}$ low ('HC160, 'HC161)	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, before CLK↑	A, B, C, or D	2 V	150		225		190		ns
			4.5 V	30		45		38		
			6 V	26		38		32		
		$\overline{LOAD}$ low	2 V	135		205		170		
			4.5 V	27		41		34		
			6 V	23		35		29		
		ENP, ENT	2 V	170		255		215		
			4.5 V	34		51		43		
			6 V	29		43		37		
		$\overline{CLR}$ inactive ('HC160, 'HC161)	2 V	125		190		155		
			4.5 V	25		38		31		
			6 V	21		32		26		
		$\overline{CLR}$ low ('HC162, 'HC163)	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
		$\overline{CLR}$ inactive ('HC162, 'HC163)	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
t_h	Hold time, all synchronous inputs after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC160 SN54HC161		SN74HC160 SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	14		4.2		5		MHz
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t_{pd}	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
t_{pd}	CLK	Any Q	2 V		80	205		310		255	ns
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
t_{pd}	ENT	RCO	2 V		62	195		295		245	ns
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t_{PHL}	$\overline{CLR}$	Any Q	2 V		105	210		315		265	ns
			4.5 V		21	42		63		53	
			6 V		18	36		54		45	
t_{PHL}	$\overline{CLR}$	RCO	2 V		110	220		330		275	ns
			4.5 V		22	44		66		55	
			6 V		19	37		56		47	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC162 SN54HC163		SN74HC162 SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	14		4.2		5		MHz
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t_{pd}	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
t_{pd}	CLK	Any Q	2 V		80	205		310		255	ns
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
t_{pd}	ENT	RCO	2 V		62	195		295		245	ns
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

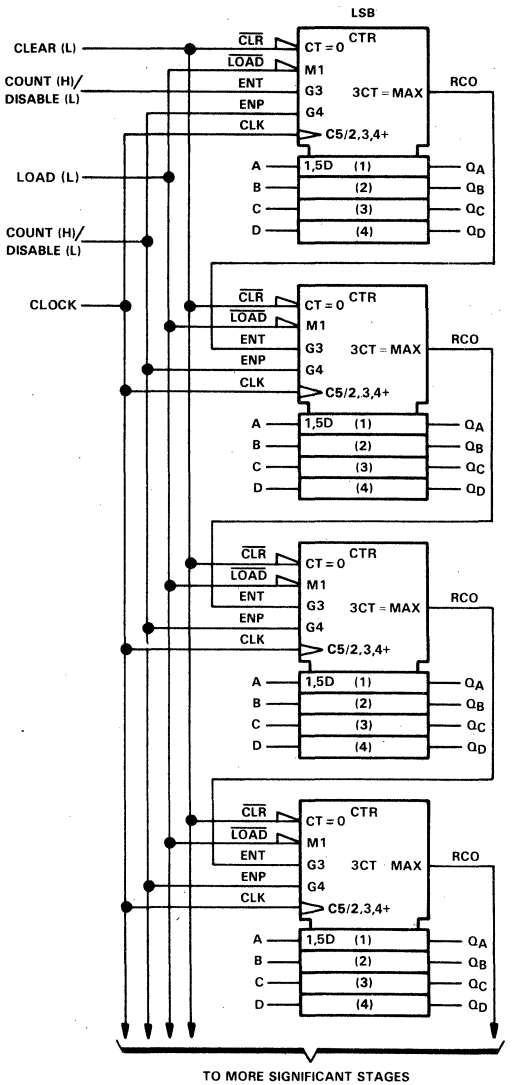
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC160 and 'HC162 will count in BCD, and the 'HC161 and 'HC163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



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The application circuit shown on the preceding page is not valid for clock frequencies above 18 MHz (at 25 °C and 4.5 V V_{CC}). The reason for this is that there is a "glitch" that is produced on the second stage's RCO output and every succeeding stage's RCO output. This glitch is common to all HC vendors that Texas Instruments has evaluated in addition to the bipolar equivalents ('LS, 'ALS, 'AS).

The glitch on RCO is caused because the propagation delay of the rising edge of Q_A of the second stage is shorter than the propagation delay of the falling edge of ENT. The RCO output is the product of ENT, Q_A, Q_B, Q_C, and Q_D ($ENT \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$). The resulting glitch is about 7-12 ns in duration. Figure 1 illustrates the condition in which the glitch occurs. For the purposes of simplicity, only two stages are being considered, but the results can be applied to other stages. Q_B, Q_C, and Q_D of the first and second stage are at logic one, and Q_A of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse, Q_A and RCO of the first stage will go high. On the rising edge of the third clock pulse Q_A and RCO of the first stage will return to a low level, and Q_A of the second stage will go to a high level. It is at this time that the glitch on the RCO of the second stage will appear because of the "race condition" inside the chip.

The glitch will cause a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than inverse of the sum of the clock-to-RCO propagation delay and the glitch duration (t_g). In other words, $f_{max} = 1/(t_{pd}$ CLK-to-RCO $+ t_g)$. For example, at 25 °C at 4.5 V V_{CC}, the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following table contains the f_{clock}, t_w, and f_{max} specifications for applications that use more than two 'HC160 family devices cascaded together.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	T_A = 25 °C		SN54HC160 thru SN54HC163		SN74HC160 thru SN74HC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	3.6	0	2.5	0	2.9	MHz
		4.5 V	0	18	0	12	0	14	
		6 V	0	21	0	14	0	17	
t_w	Pulse duration, CLK high or low	2 V	140		200		170		ns
		4.5 V	28		40		36		
		6 V	24		36		30		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			SN54HC160 thru SN54HC163		SN74HC160 thru SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	3.6			2.5		2.9		MHz
			4.5 V	18			12		14		
			6 V	21			14		17		

NOTE 1: These limits apply only to applications which use more than two 'HC160 family devices cascaded together.

If the 'HC160 family is used as a single unit or only two cascaded together, then the maximum clock frequency that the devices can use is not limited because of the glitch. In these situations, the devices can be operated at the maximum specifications.

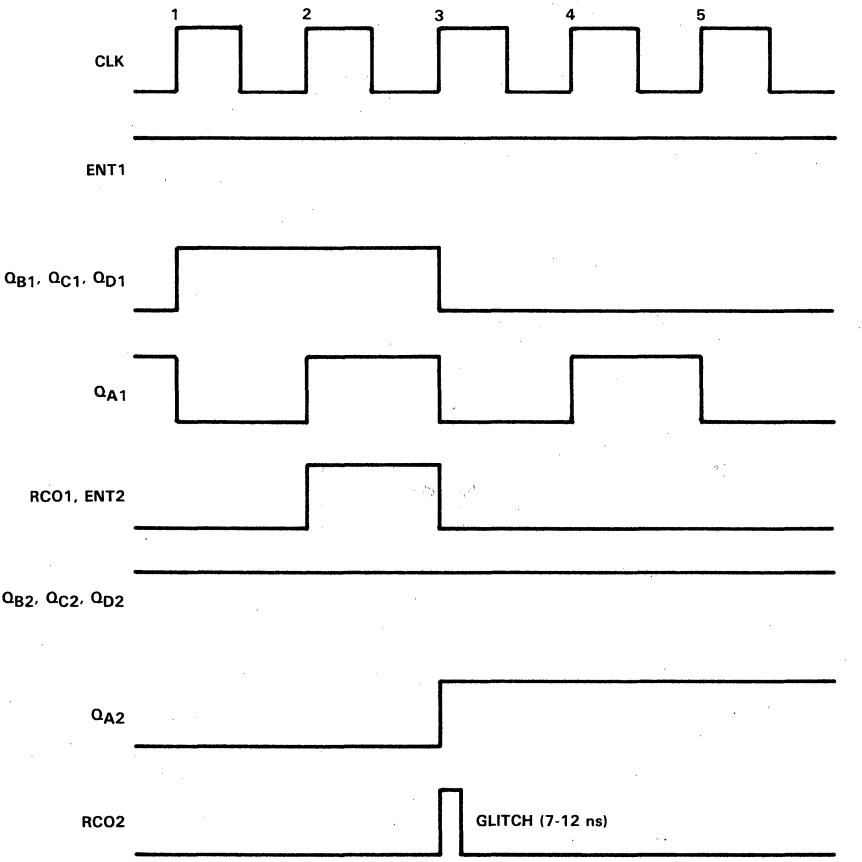

FIGURE 1

A glitch can appear on the RCO output of a single 'HC160 family device depending on the relationship of ENT to the clock input. Any application that uses the RCO output to drive any input except an ENT of another cascaded 'HC160 family device must take this into consideration.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous Clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

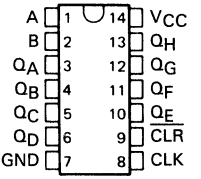
The SN54HC164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC164 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

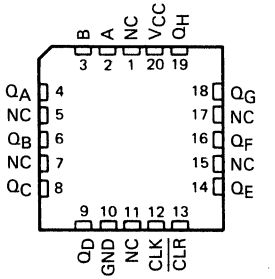
INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state). L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a one-bit shift.

SN54HC164 . . . J PACKAGE
SN74HC164 . . . N PACKAGE
(TOP VIEW)

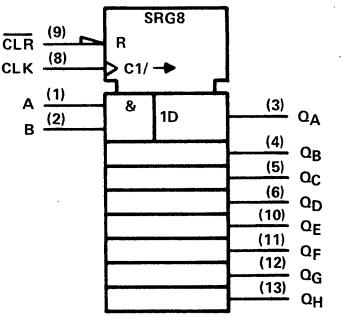


SN54HC164 . . . FK PACKAGE
(TOP VIEW)



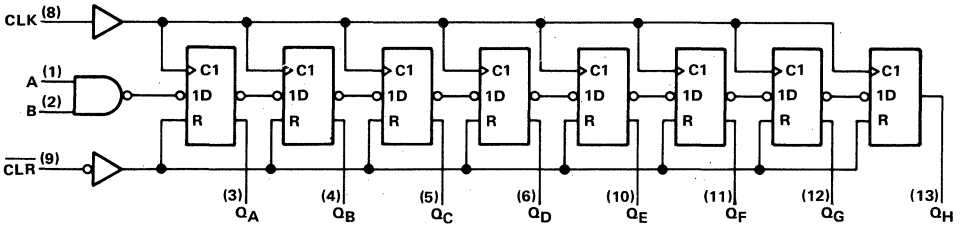
NC—No internal connection

logic symbol†



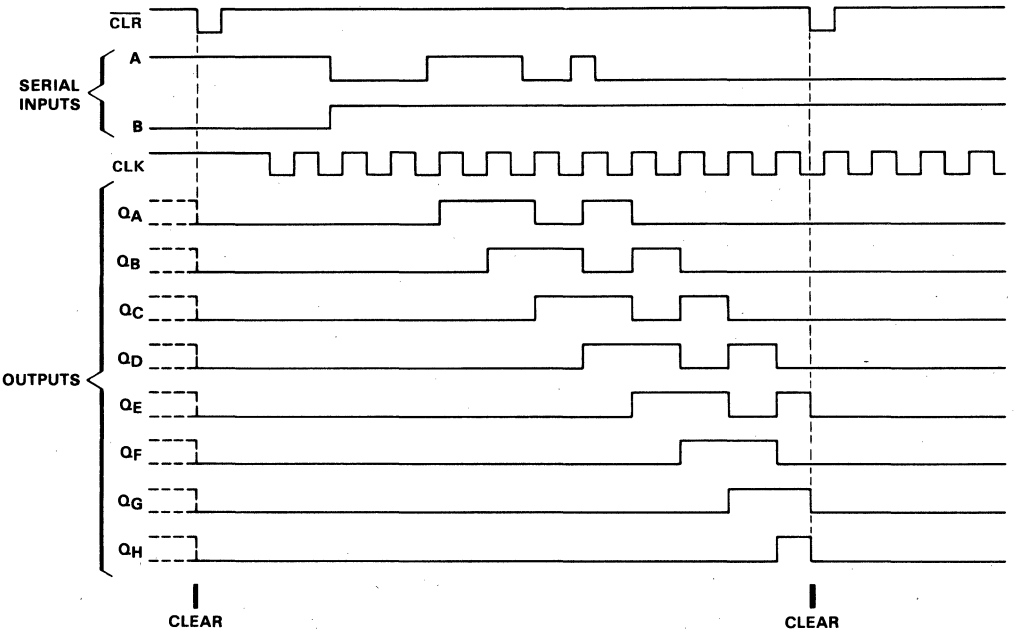
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers are for J and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC164			SN74HC164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC164		SN74HC164		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC164		SN74HC164		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	28	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC164		SN74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	54		21		25		
			6 V	36	62		25		28		
t_{PHL}	$\overline{CLR}$	Any Q	2 V		140	205		295		255	ns
			4.5 V		28	41		59		51	
			6 V		24	35		51		46	
t_{pd}	CLK	Any Q	2 V		115	175		265		220	ns
			4.5 V		23	35		53		44	
			6 V		20	30		45		38	
t_t			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	135 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The 'HC165 also features a clock inhibit function and a complementary serial output $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of CLK, CLK INH, or SER inputs.

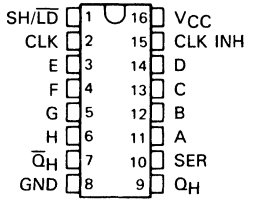
The SN54HC165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC165 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

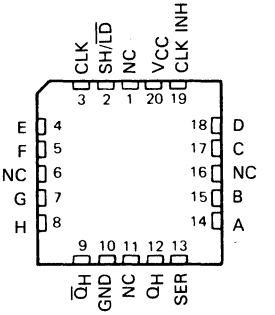
INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift
H	↑	L	Shift

Shift — content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

SN54HC165 . . . J PACKAGE
SN74HC165 . . . D OR N PACKAGE
(TOP VIEW)

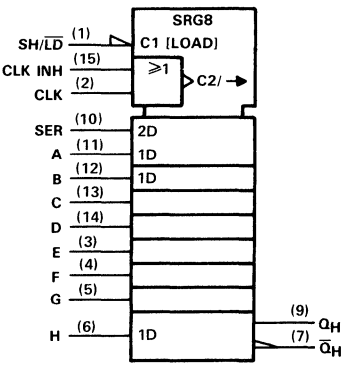


SN54HC165 . . . FK PACKAGE
(TOP VIEW)



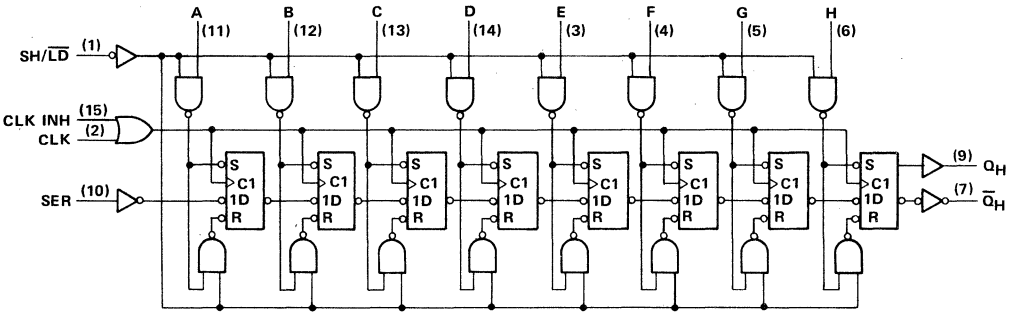
NC—No internal connection

logic symbol†



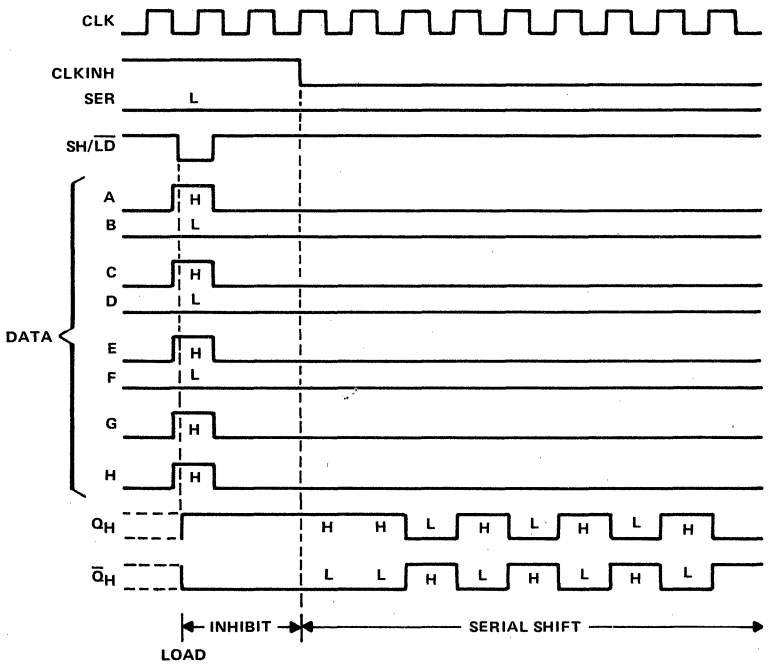
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical shift, load, and inhibit sequences



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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC165			SN74HC165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC165		SN74HC165		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	SH/$\overline{LD}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		SER before CLK↑	2 V	40		60		50		ns
			4.5 V	8		12		10		
			6 V	7		10		9		
		CLK INH low before CLK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK INH high before CLK↑	2 V	40		60		50		ns
			4.5 V	8		12		10		
			6 V	7		10		9		
		Data before SH/$\overline{LD}$↓	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time	SER data after CLK↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		PAR data after SH/$\overline{LD}$↓	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	13		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	62		25		29		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		16	26		38		32	
t_{pd}	CLK	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	H	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	75 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

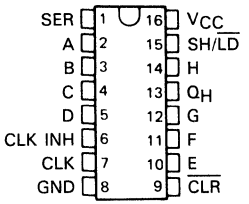
- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

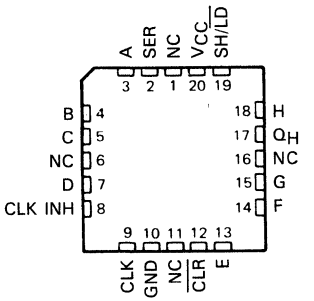
The 'HC166 parallel-in or serial-in, serial-out registers feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low,, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input overrides all other inputs, including the clock, and resets all flip-flops to zero.

The SN54HC166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC166 is characterized for operation from −40°C to 85°C.

SN54HC166 . . . J PACKAGE
SN74HC166 . . . D OR N PACKAGE
(TOP VIEW)

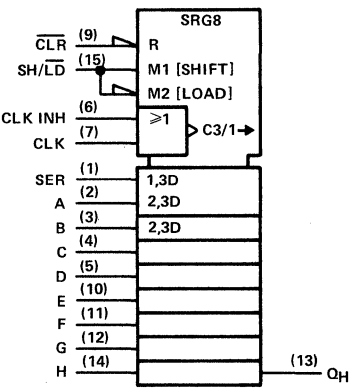


SN54HC166 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†

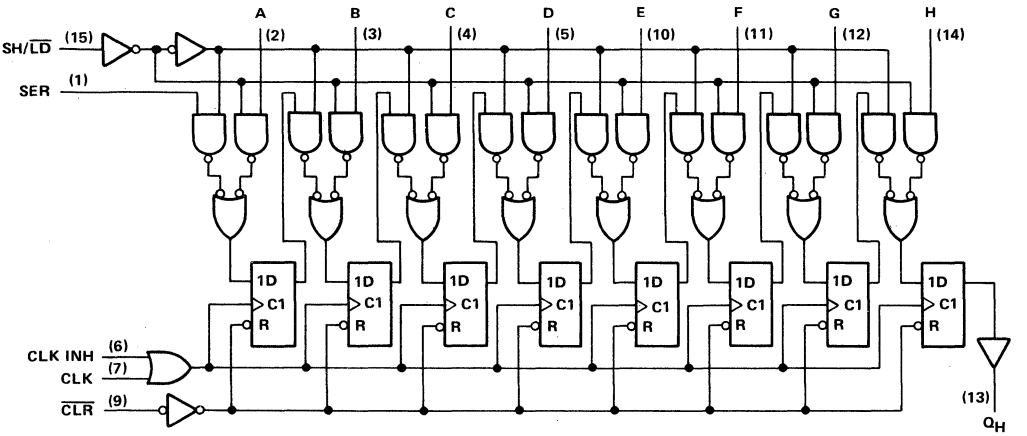


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

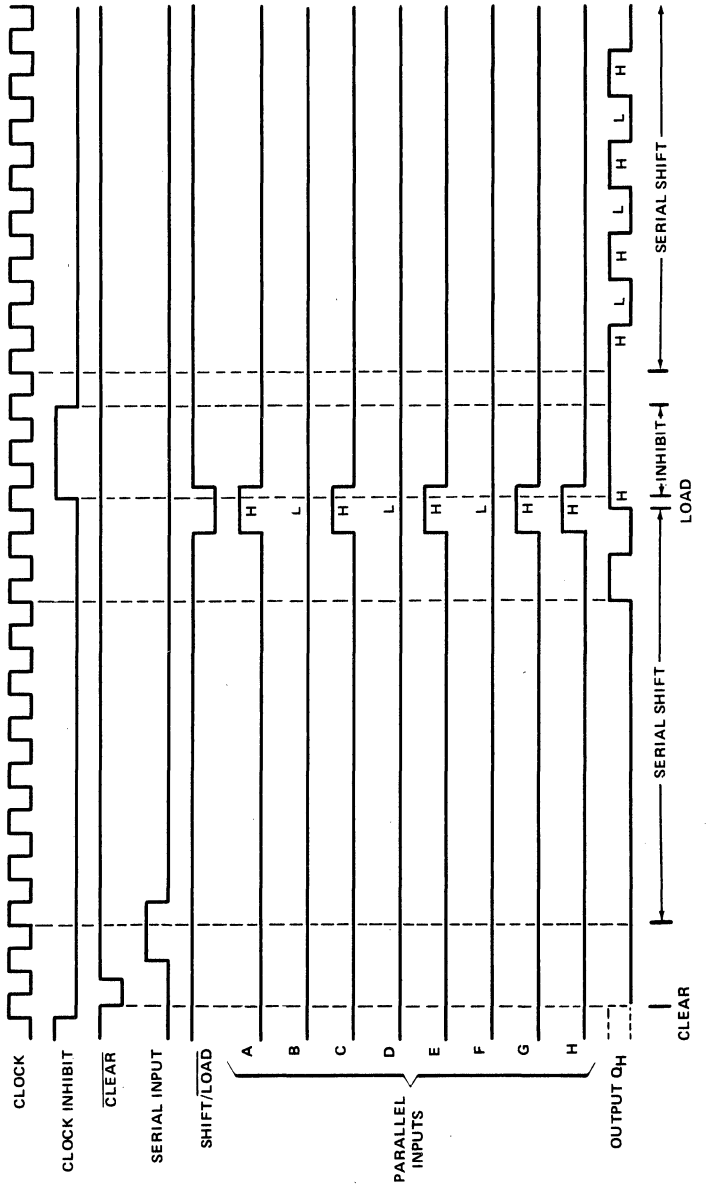
INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	H	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	G_{A0}	Q_{B0}	Q_{H0}

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC166			SN74HC166			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC166		SN74HC166		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC166		SN74HC166		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	2 V	145		220		180		ns
			4.5 V	29		44		36		
			6 V	25		38		31		
		SER before CLK↑	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK INH low before CLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
		Data before CLK↑	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{CLR}$ inactive before CLK↑	2 V	40		60		50		
			4.5 V	8		12		10		
			6 V	7		10		9		
t_h	Hold time	SH/$\overline{LD}$ high after CLK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		
		SER after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		CLK INH high after CLK↑	2 V	0		0		0		
			4.5 V	0		0		0		
			6 V	0		0		0		
		Data after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	36		21		25		
			6 V	36	45		25		29		
t_{PHL}	$\overline{CLR}$	Q_H	2 V		62	120		180		150	ns
			4.5 V		18	24		36		30	
			6 V		13	20		31		26	
t_{pd}	CLK	Q_H	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Gated Output-Control Lines for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

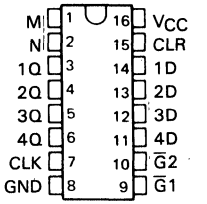
description

The 'HC173 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedence third state and increased drive provide these flip-flops with the capability of being connected directly to and driving the lines in a bus-organized system without need for interface or pull-up components.

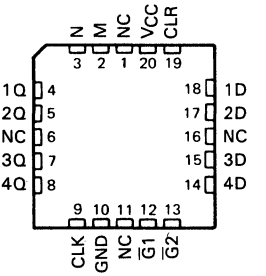
Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Gate output-control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54HC173 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC173 is characterized for operation from −40°C to 85°C.

SN54HC173 . . . J PACKAGE
SN74HC173 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC173 . . . FK PACKAGE
(TOP VIEW)



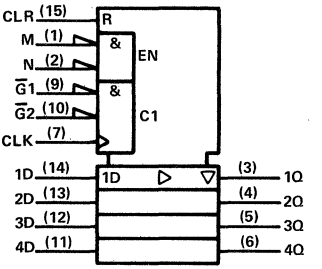
NC—No internal connection

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE		DATA	Q
		$\overline{G1}$	$\overline{G2}$	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

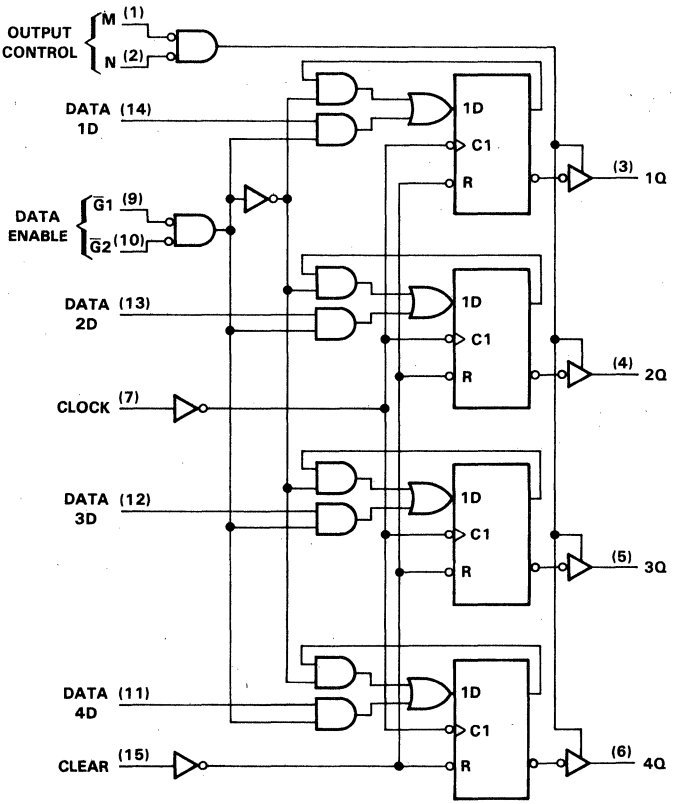
When either M or N (or both) is (are) high, the output is disabled to the high-impedence state; however, sequential operation of the flip-flops is not affected.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC173			SN74HC173			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC173		SN74HC173		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Input clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLR high	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	$\overline{G}1$ and $\overline{G}2$	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLR inactive	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		19		
t_h	Hold time after CLK↑	$\overline{G}1$ and $\overline{G}2$	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		
		Data	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	8		4.2		5		MHz
			4.5 V	31	46		21		25		
			6 V	36	55		25		29		
t_{PHL}	CLR	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t_{pd}	CLK	Any	2 V		78	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		20	26		38		32	
t_{en}	M or N	Any	2 V		78	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		15	26		38		32	
t_{dis}	M or N	Any	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		Any	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	29 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC173		SN74HC173		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_{pd}	CLR	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_{en}	M or N	Any	2 V		100	200		300		250	ns
			4.5 V		28	40		60		50	
			6 V		21	34		51		43	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **'HC174 Contains Six Flip-Flops with Single-Rail Outputs**
- **'HC175 Contains Four Flip-Flops with Double-Rail Outputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic, positive-edge triggered D-type flip-flops have a direct clear input, and the 'HC175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

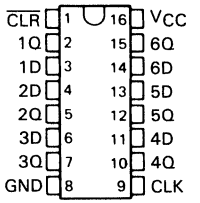
The SN54HC174 and SN54HC175 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC174 and SN74HC175 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

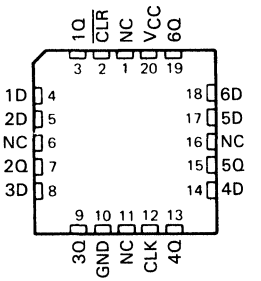
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	Q_0

†'HC175 only

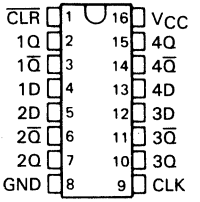
SN54HC174 . . . J PACKAGE
SN74HC174 . . . D OR N PACKAGE
(TOP VIEW)



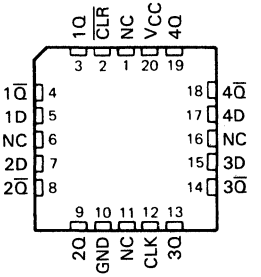
SN54HC174 . . . FK PACKAGE
(TOP VIEW)



SN54HC175 . . . J PACKAGE
SN74HC175 . . . D OR N PACKAGE
(TOP VIEW)



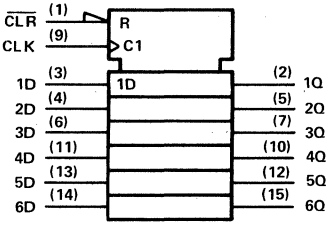
SN54HC175 . . . FK PACKAGE
(TOP VIEW)



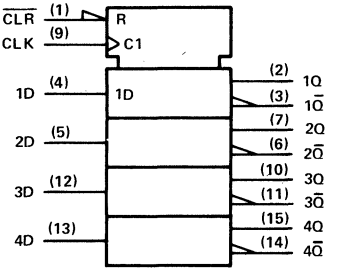
NC—No internal connection

logic symbols†

'HC174



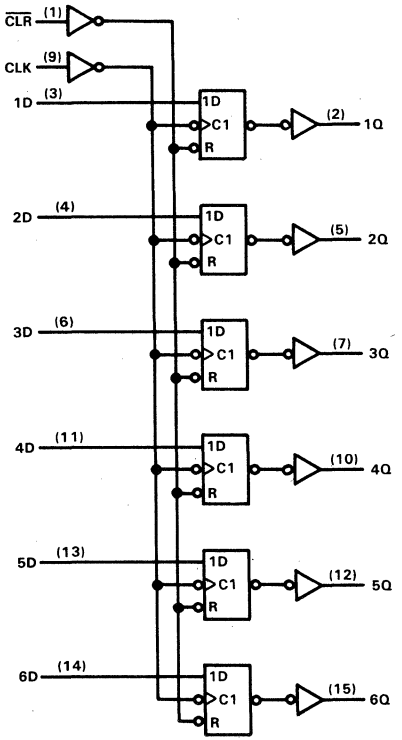
'HC175



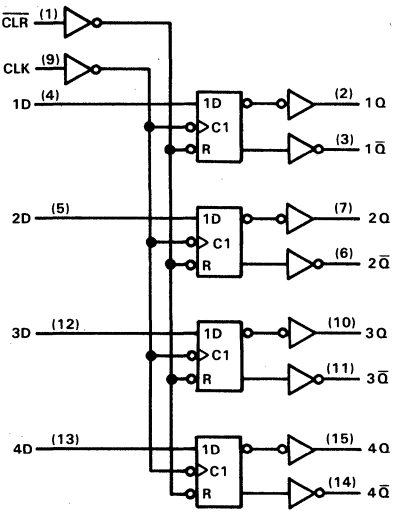
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)

'HC174



'HC175



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC174 SN54HC175			SN74HC174 SN74HC175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC174 SN54HC175		SN74HC174 SN74HC175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC174		SN74HC174		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	44		21		25		
			6 V	36	50		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		58	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	CLK	Any	2 V		58	160		240		200	
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	27 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC175		SN74HC175		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC175		SN74HC175		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		52	150		255		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	CLK	Any	2 V		58	150		255		190	
			4.5 V		16	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	30 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2484, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications, Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

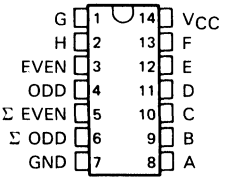
The SN54HC180 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC180 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

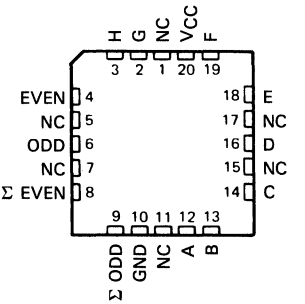
INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

SN54HC180 . . . J PACKAGE
SN74HC180 . . . D OR N PACKAGE
(TOP VIEW)

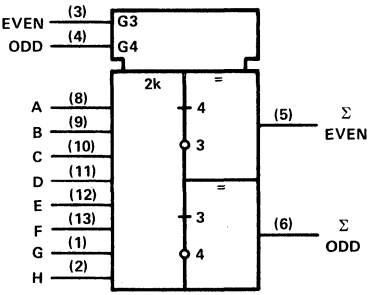


SN54HC180 . . . FK PACKAGE
(TOP VIEW)



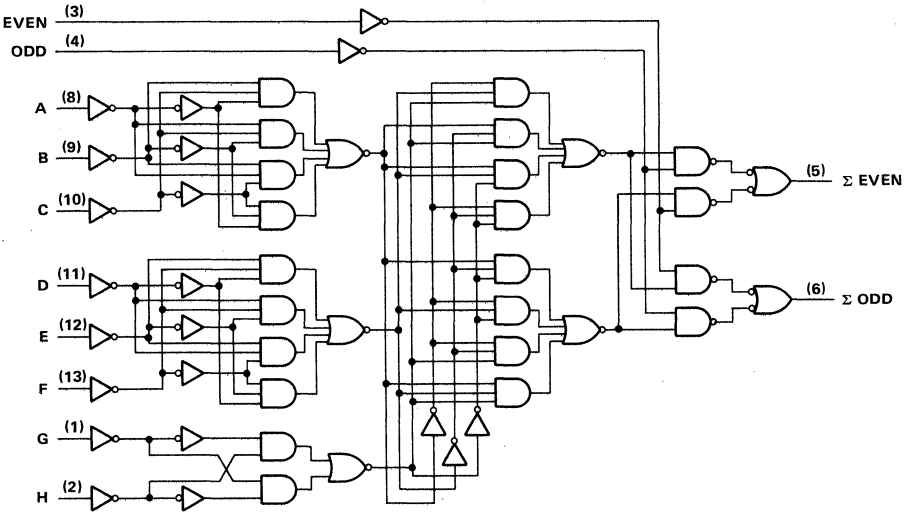
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC180			SN74HC180			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC180		SN74HC180		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC180		SN74HC180		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Data (odd = 0)	Even	2 V		119	260		390		325	ns
			4.5 V		36	52		78		65	
			6 V		32	44		66		55	
t_{pd}	Data (odd = 0)	Odd	2 V		113	245		370		305	ns
			4.5 V		33	49		74		61	
			6 V		13	42		63		52	
t_{pd}	Data (even = 0)	Even	2 V		119	260		390		325	ns
			4.5 V		36	52		78		65	
			6 V		32	44		66		55	
t_{pd}	Data (even = 0)	Odd	2 V		113	245		370		305	ns
			4.5 V		33	49		74		61	
			6 V		24	42		63		52	
t_{pd}	Even or Odd	Even or Odd	2 V		49	110		165		140	ns
			4.5 V		15	22		33		28	
			6 V		12	19		28		24	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

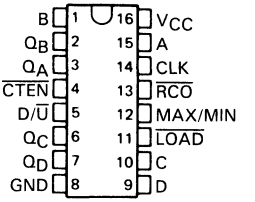
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

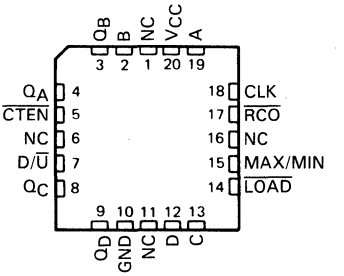
D2684, DECEMBER 1982 — REVISED SEPTEMBER 1987

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC190, SN54HC191 . . . J PACKAGE
SN74HC190, SN74HC191 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC190, SN54HC191 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'HC190 and 'HC191 are synchronous, reversible up/down counters. The 'HC190 is a 4-bit decade counter, and the 'HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up ($D/\overline{U}$) input. When $D/\overline{U}$ is low, the counter counts up, and when $D/\overline{U}$ is high, it counts down.

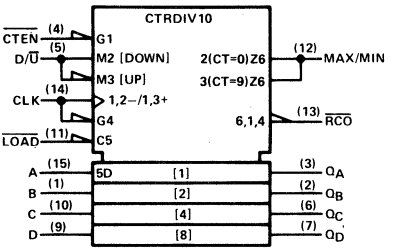
These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and $D/\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

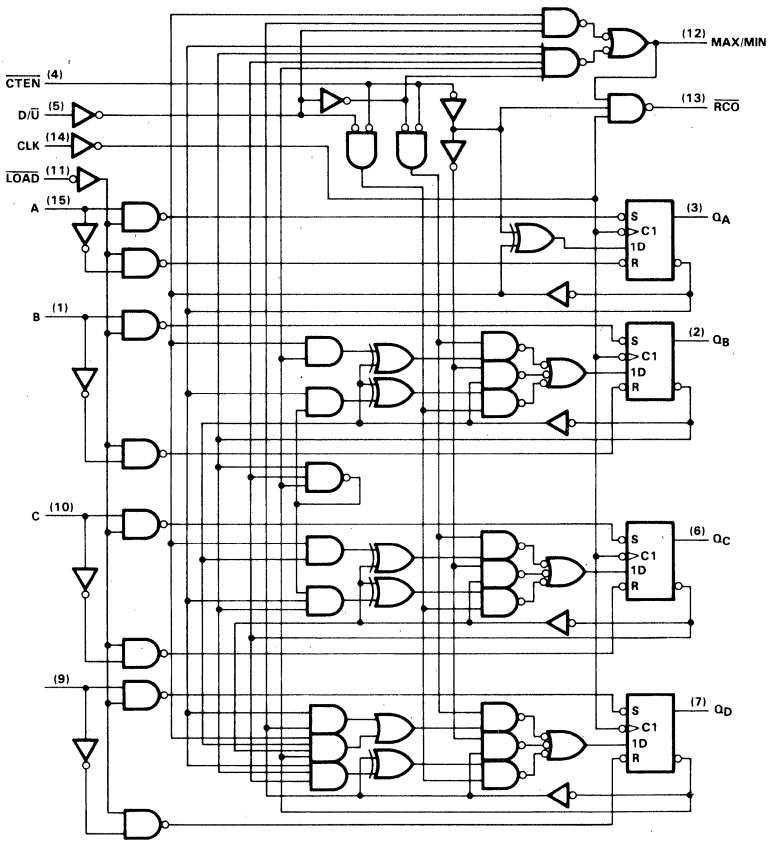
The SN54HC190 and SN54HC191 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC190 and SN74HC191 are characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers are for DW, J, and N packages.

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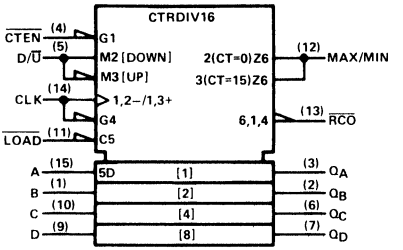
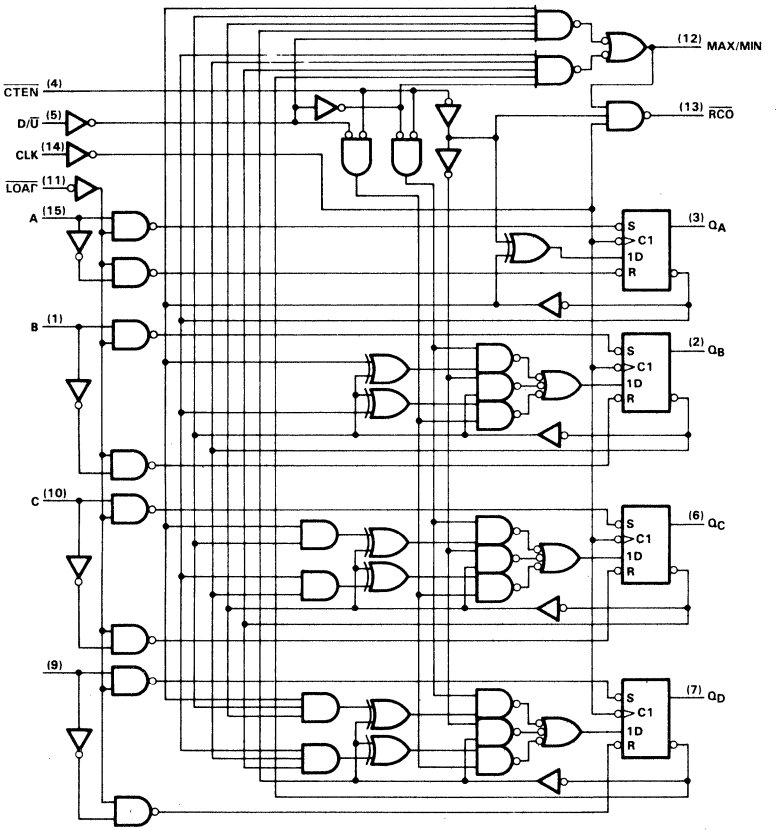
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

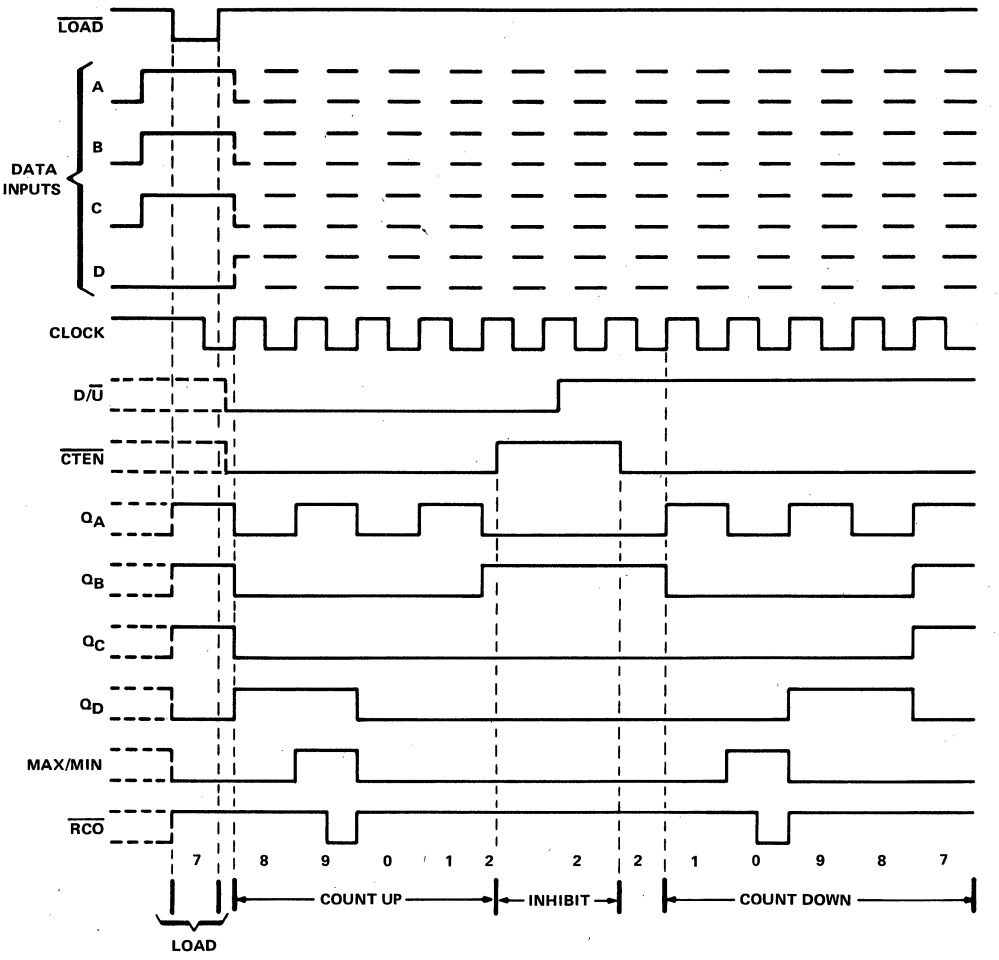


Pin numbers are for DW, J, and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven.



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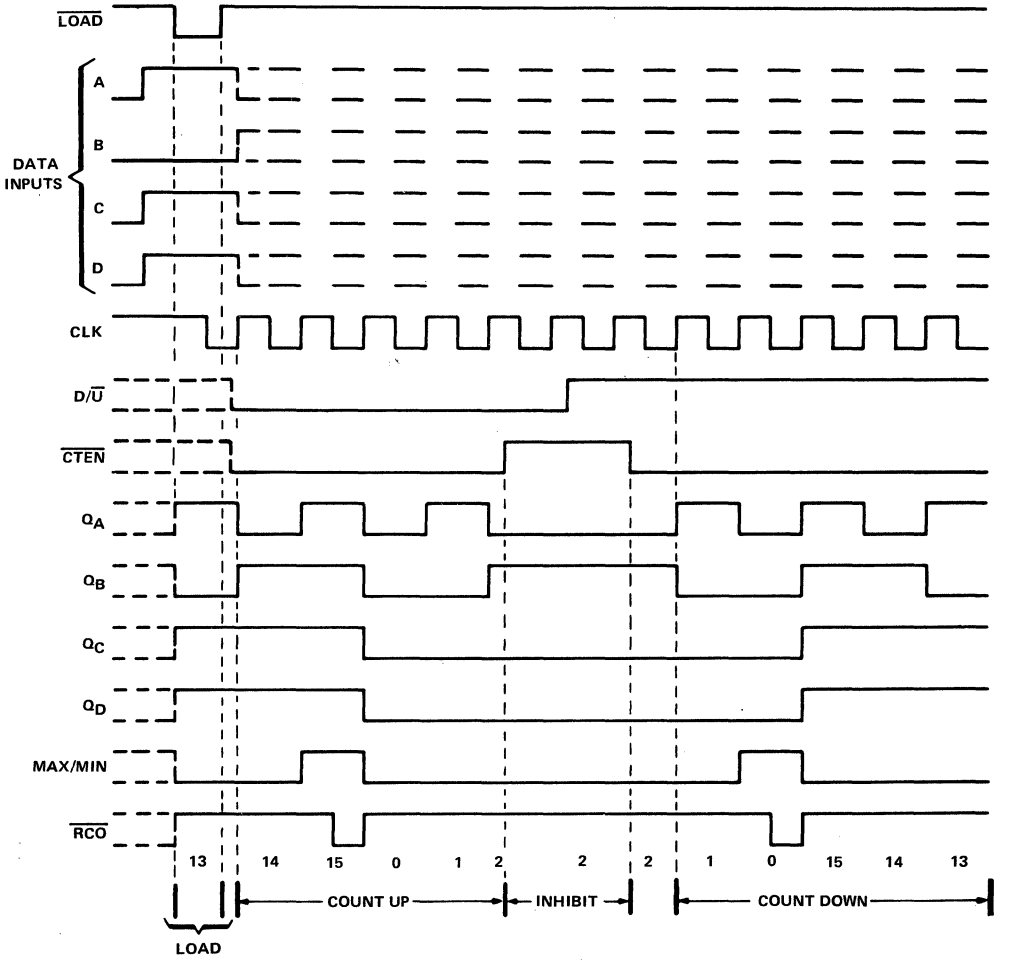
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC190 SN54HC191			SN74HC190 SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	$\overline{LOAD}$ low	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		CLk high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	2 V	150		256		188		ns
			4.5 V	30		46		38		
			6 V	25		38		32		
		$\overline{CTEN}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		D/$\overline{U}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		$\overline{LOAD}$ inactive before CLK↑	2 V	150		250		190		
			4.5 V	30		45		38		
			6 V	25		38		32		
t_h	Hold time	Data after $\overline{LOAD}$↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		$\overline{CTEN}$ after CLK↑	2V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		D/$\overline{U}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC190 SN54HC191		SN74HC190 SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	42		14		17		
			6 V	24	48		16		19		
t_{pd}	$\overline{LOAD}$	Any Q	2 V		130	264		396		330	ns
			4.5 V		40	53		79		66	
			6 V		33	45		67		56	
t_{pd}	A, B, C, or D	Q_A, Q_B Q_C, or Q_D	2 V		135	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		30	41		61		51	
t_{pd}	CLK	$\overline{RCO}$	2 V		58	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	21		31		26	
t_{pd}	CLK	Any Q	2 V		107	192		288		240	ns
			4.5 V		31	38		58		48	
			6 V		26	32		49		41	
t_{pd}	CLK	MAX/MIN	2 V		123	252		378		315	ns
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
t_{pd}	D/$\overline{U}$	$\overline{RCO}$	2 V		102	228		342		285	ns
			4.5 V		29	46		68		57	
			6 V		24	38		59		49	
t_{pd}	D/$\overline{U}$	MAX/MIN	2 V		86	192		288		240	ns
			4.5 V		24	38		58		48	
			6 V		20	32		49		41	
t_{pd}	$\overline{CTEN}$	$\overline{RCO}$	2 V		50	132		198		165	ns
			4.5 V		15	26		40		33	
			6 V		13	23		34		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

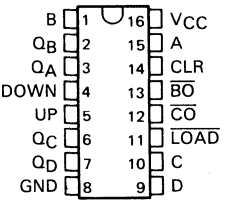
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

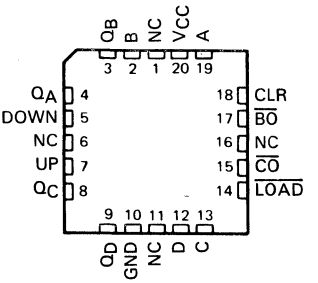
D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC192, SN54HC193 . . . J PACKAGE
SN74HC192, SN74HC193 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC192, SN54HC193 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'HC192 and 'HC193 are synchronous, reversible up/down counters. The 'HC192 is a 4-bit decade counter, and the 'HC193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

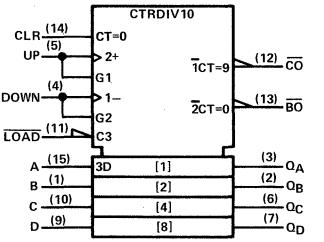
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

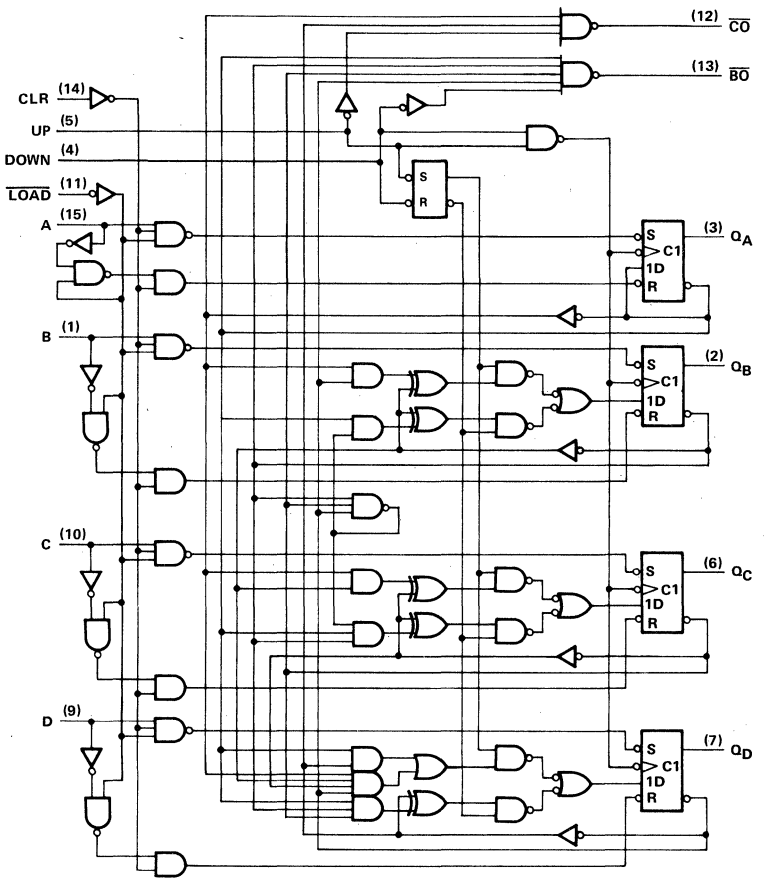
The SN54HC192 and SN54HC193 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC192 and SN74HC193 are characterized for operation from −40°C to 85°C.

logic symbol†



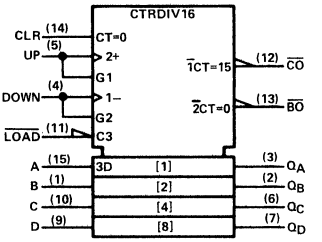
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



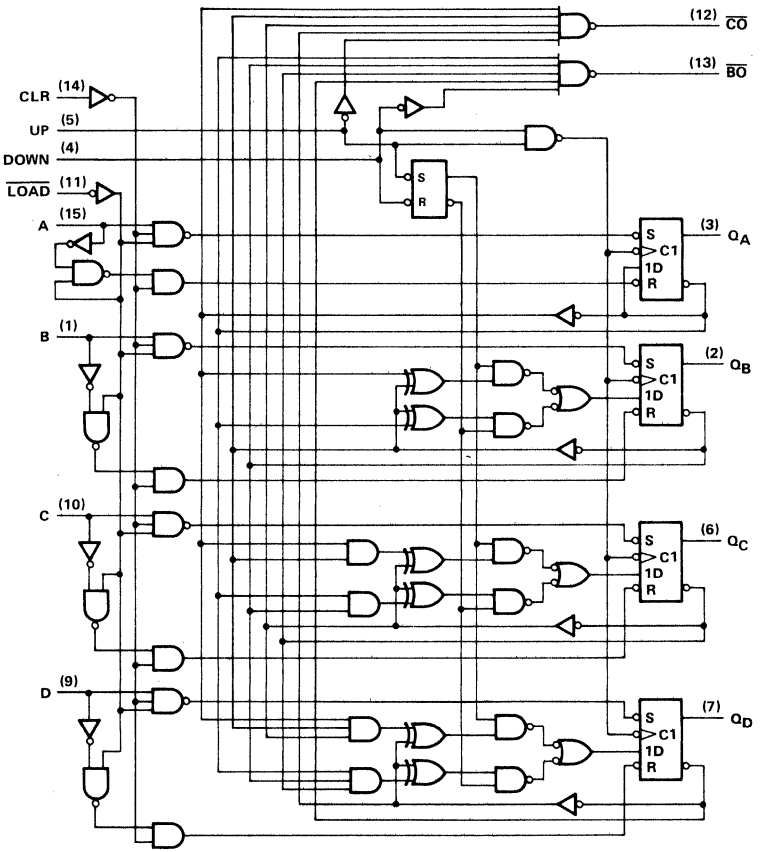
Pin numbers shown are for DW, J, and N packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

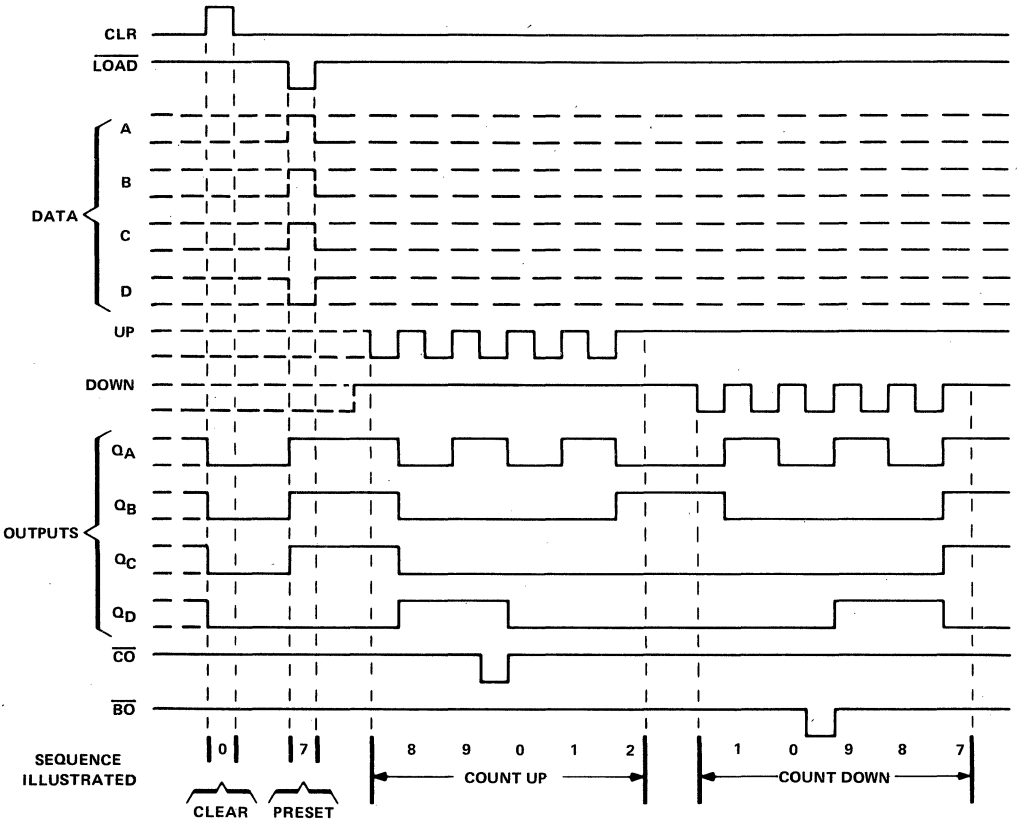


Pin numbers shown are for DW, J, and N packages.

typical clear, load, and count sequence:

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to BCD seven
3. Count up to eight, nine, carry, zero, one, and two
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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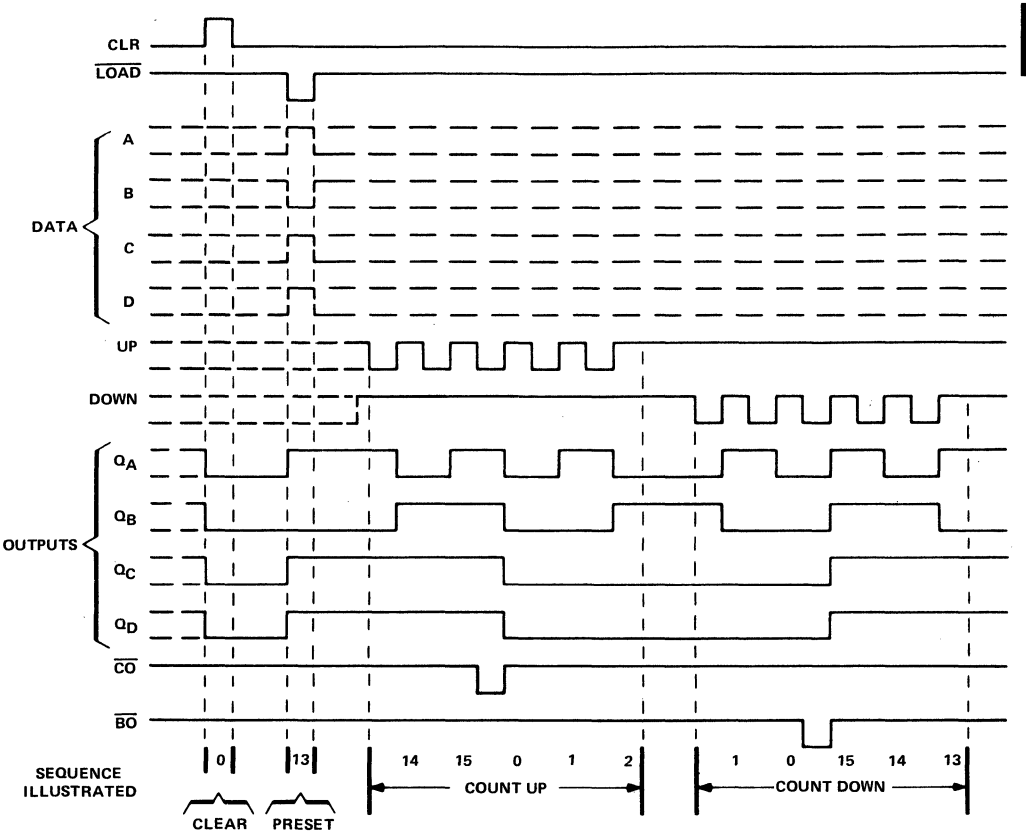
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen, carry, zero, one, and two
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC192 SN54HC193			SN74HC192 SN74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CLR high	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		$\overline{LOAD}$ low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
		UP or DOWN high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$ inactive	2 V	110		165		140		ns
			4.5 V	22		33		28		
			6 V	19		28		24		
		CLR inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
t_h	Hold time	Data after $\overline{LOAD}$ inactive	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
t_{pd}	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
t_{pd}	DOWN	$\overline{BO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
t_{pd}	UP or DOWN	Any Q	2 V		190	250		375		315	ns
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
t_{pd}	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	ns
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
t_{PHL}	CLR	ANY Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Parallel Inputs and Outputs**
- **Four Operating Modes:**
  - **Synchronous Parallel Load**
  - **Right Shift**
  - **Left Shift**
  - **Do Nothing**
- **Positive Edge-Triggered Clocking**
- **Direct Overriding Clear**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clocking (do nothing).

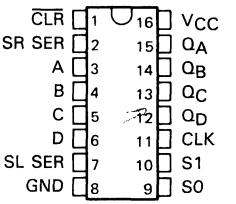
Synchronous parallel loading is accomplished by applying the 4 bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously, and new data is entered at the shift-left serial input.

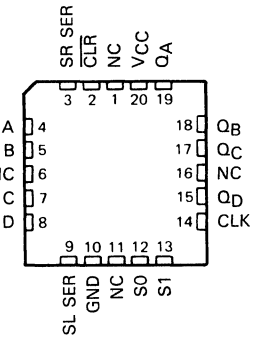
Clocking of the shift register is inhibited when both mode control inputs are low.

The SN54HC194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC194 is characterized for operation from −40°C to 85°C.

SN54HC194 . . . J PACKAGE
SN74HC194 . . . DW or N PACKAGE
(TOP VIEW)

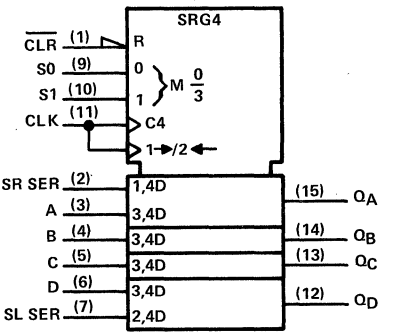


SN54HC194 . . . FK PACKAGE
(TOP VIEW)



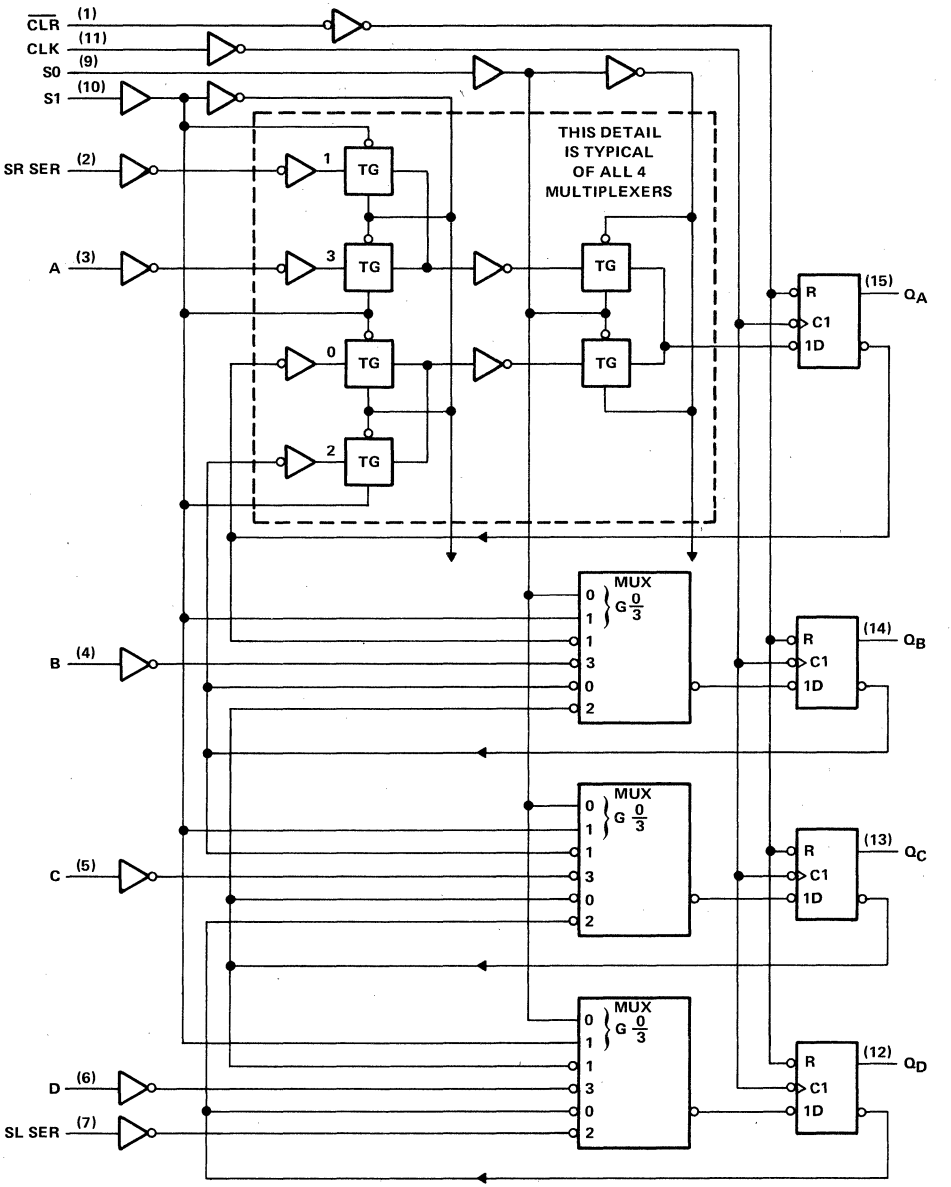
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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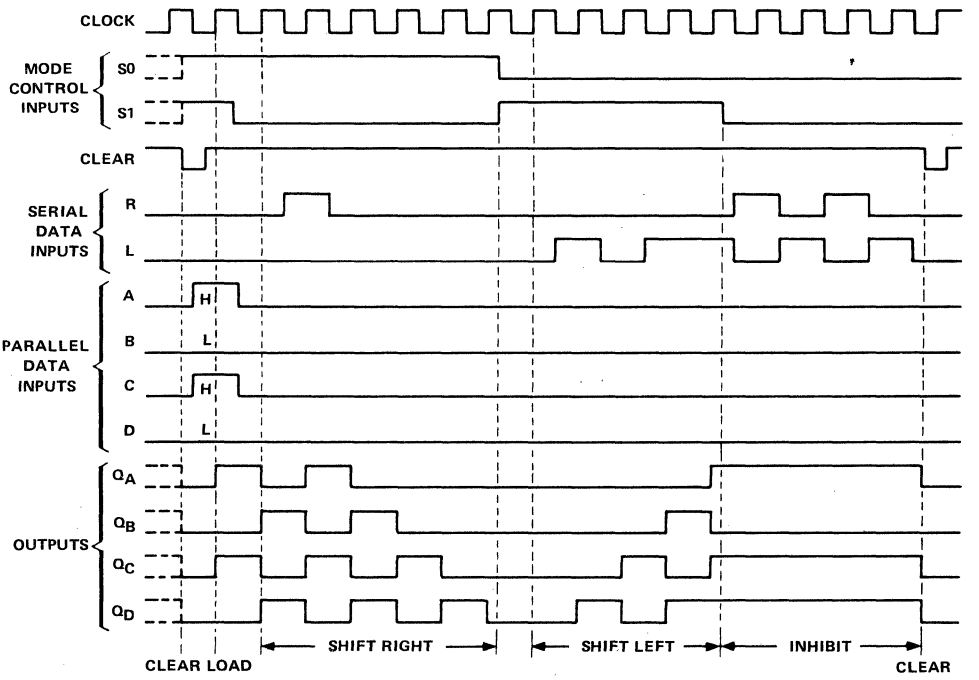
FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{D0}

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC194			SN74HC194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC194		SN74HC194		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC194		SN74HC194		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w Pulse duration	CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	$\overline{CLR}$ low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su} Setup time, any input before CLK↑		2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h Hold time, data after CLK↑		2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC194		SN74HC194		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6			4.2		5		MHz
			4.5 V	31			21		25		
			6 V	36			25		29		
t_{PHL}	$\overline{CLR}$	Any	2 V		67	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		37		31	
t_{pd}	CLK	Any	2 V		67	145		220		180	ns
			4.5 V		17	29		44		36	
			6 V		14	25		37		31	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	65 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Synchronous Parallel Load**
- **Positive-Edge-Triggered Clocking**
- **J and $\overline{K}$ Inputs to First Stage**
- **Complementary Outputs from Last Stage**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

description

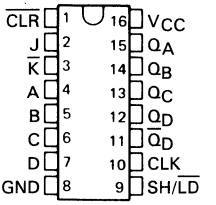
These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction Q_A and Q_D).

Parallel loading is accomplished by applying the 4-bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

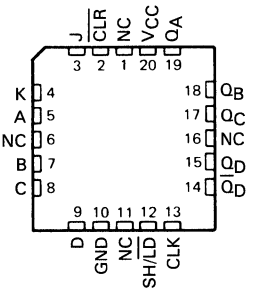
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$-, D-, or T-type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC195 is characterized for operation from −40°C to 85°C.

SN54HC195 . . . J PACKAGE
SN74HC195 . . . DW or N PACKAGE
(TOP VIEW)

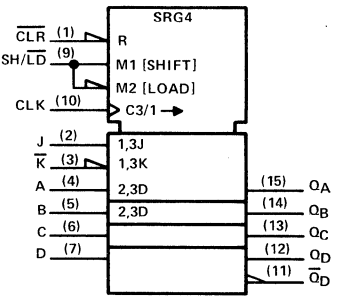


SN54HC195 . . . FK PACKAGE
(TOP VIEW)



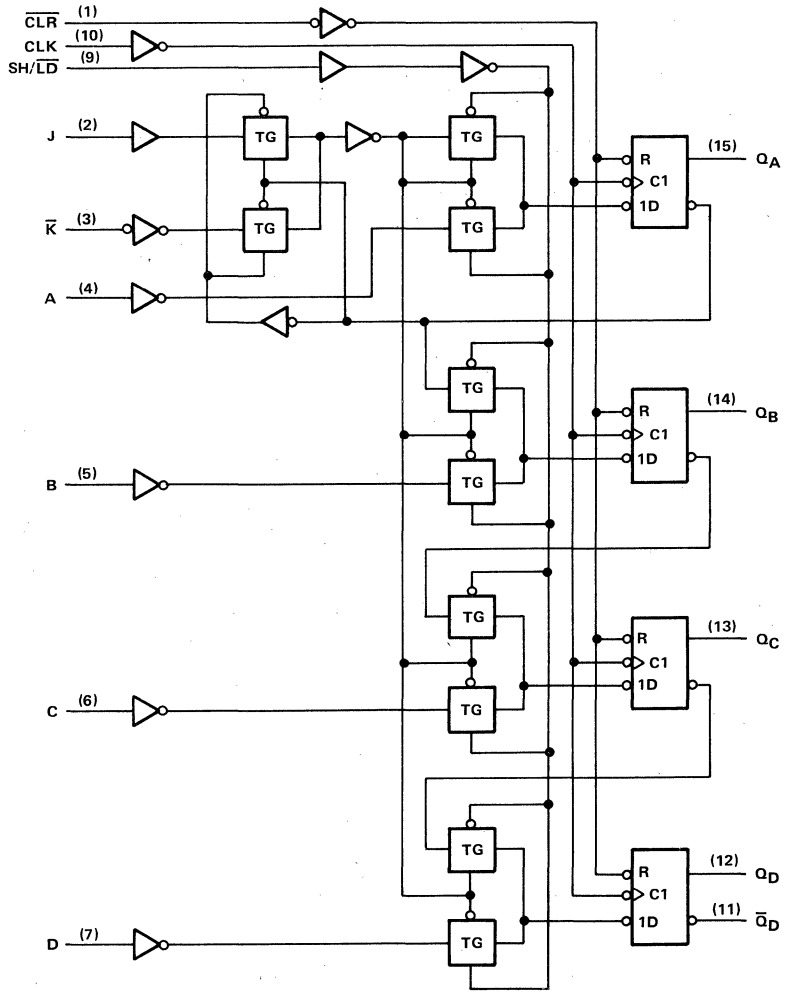
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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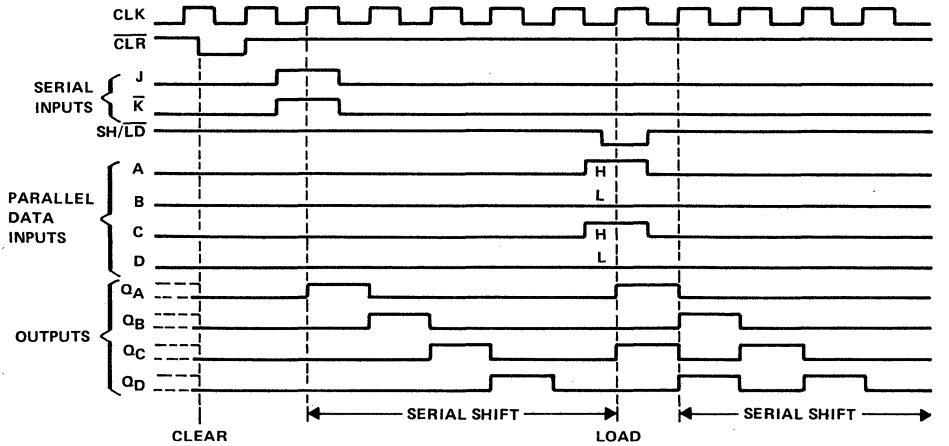
FUNCTION TABLE

INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
$\overline{CLR}$	SH/$\overline{LD}$	CLK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

typical clear, shift, and load sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC195			SN74HC195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC195		SN74HC195		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC195		SN74HC195		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{CLR}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, before CLK↑	SH/$\overline{LD}$, or serial and parallel data, or $\overline{CLR}$ inactive	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time, after CLK↑	SH/$\overline{LD}$ or serial and parallel data	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC195		SN74HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	CLK	Q_A thru Q_D or $\overline{Q}_D$	2 V		67	145		220		180	ns
			4.5 V		17	29		44		36	
			6 V		14	25		37		31	
t_{pd}	$\overline{CLR}$	Q_A thru Q_D or $\overline{Q}_D$	2 V		67	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

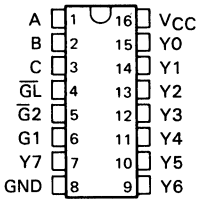
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	65 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

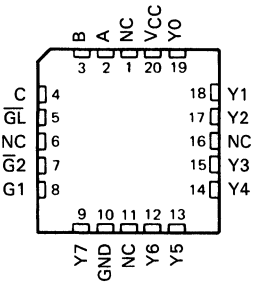
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC237 . . . J PACKAGE
SN74HC237 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC237 . . . FK PACKAGE
(TOP VIEW)



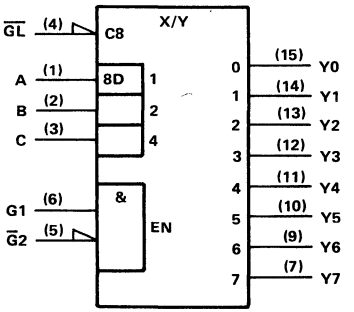
NC—No internal connection

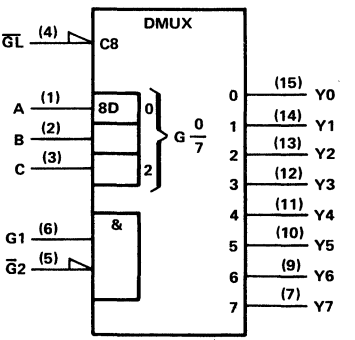
description

The 'HC237 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable ($\overline{GL}$) is low, the 'HC237 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced low if G1 is low or $\overline{G2}$ is high. The 'HC237 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HC237 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC237 is characterized for operation from −40°C to 85°C.

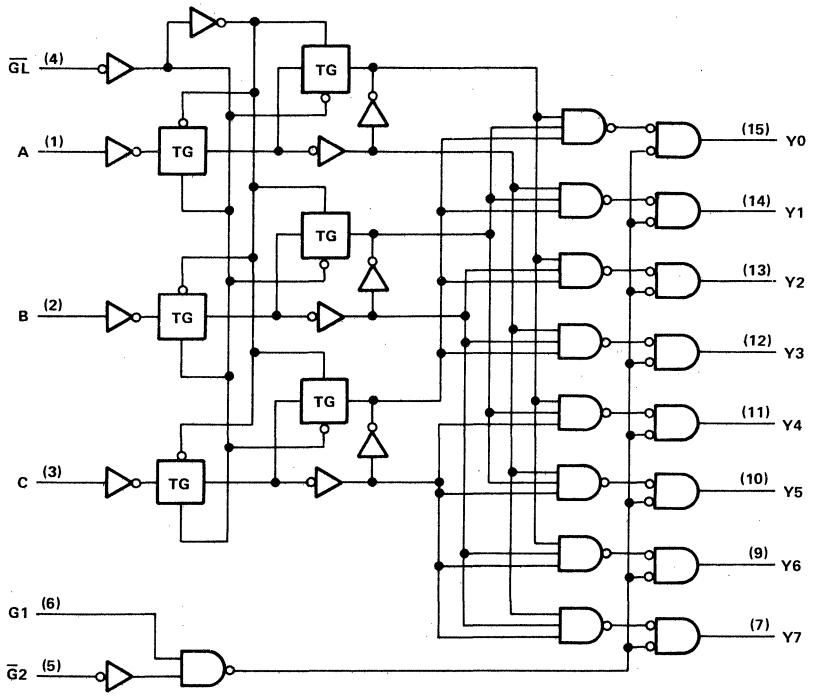
logic symbols (alternatives)†





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Outputs corresponding to stored address, L; all others, H							

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC237			SN74HC237			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC237		SN74HC237		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C			SN54HC237		SN74HC237		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{GL}$ low	2 V	80			120		100		ns
		4.5 V	16			24		20		
		6 V	14			20		17		
t_{su}	Setup time, A, B, or C before $\overline{GL}$↑	2 V	75			115		95		ns
		4.5 V	15			23		19		
		6 V	13			20		16		
t_h	Hold time, A, B, and C after $\overline{GL}$↑	2 V	5			5		5		ns
		4.5 V	5			5		5		
		6 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

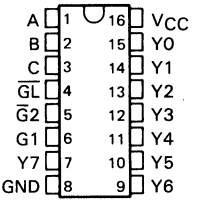
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC237		SN74HC237		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C	Any	2 V		91	190		285		240	ns
			4.5 V		23	38		57		48	
			6 V		17	32		48		41	
t_{pd}	$\overline{G2}$	Any	2 V		66	145		220		181	ns
			4.5 V		18	29		44		36	
			6 V		13	25		37		31	
t_{pd}	G1	Any	2 V		68	145		220		181	ns
			4.5 V		18	29		44		36	
			6 V		14	25		37		31	
t_{pd}	$\overline{GL}$	Any	2 V		92	190		285		240	ns
			4.5 V		24	38		57		48	
			6 V		19	32		48		41	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

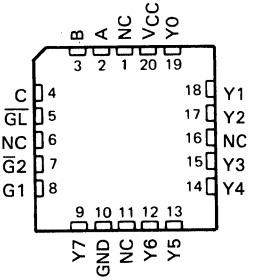
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT237 . . . J PACKAGE
SN74HCT237 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT237 . . . FK PACKAGE
(TOP VIEW)



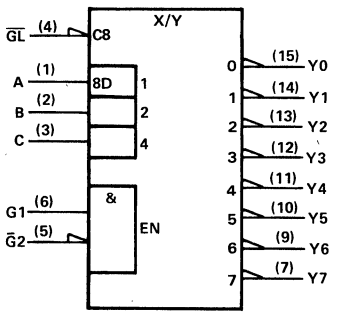
NC—No internal connection

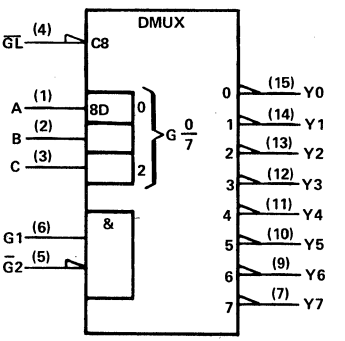
description

The 'HCT237 is a three-line to eight-line decoder/demultiplexer with latches on the three adress inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HCT237 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced low if G1 is low or $\overline{G2}$ is high. The 'HCT237 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HCT237 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT237 is characterized for operation from −40°C to 85°C.

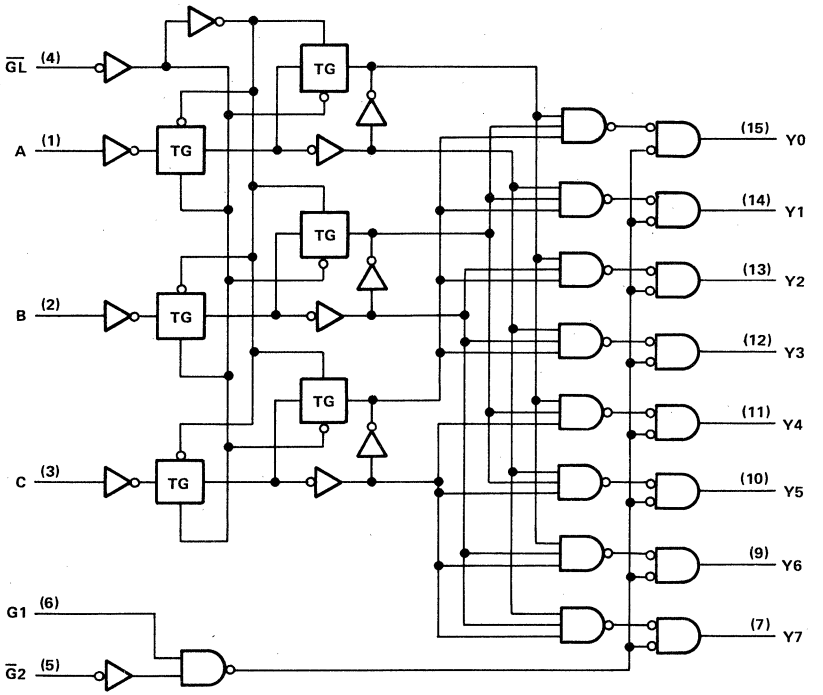
logic symbols (alternatives)†





†These symbols are in accordance with ANS/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT237			SN74HCT237			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT237		SN74HCT237		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3.0		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V_{CC}	T_A = 25°C		SN54HCT237		SN74HCT237		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, $\overline{GL}$ low	4.5 V	26		39		33		ns
	5.5 V	23		35		30		
t_{su} Setup time, A, B, and C before $\overline{GL}$↑	4.5 V	15		23		19		ns
	5.5 V	14		21		17		
t_h Hold time, A, B, and C after $\overline{GL}$↑	4.5 V	5		5		5		ns
	5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT237		SN74HCT237		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C	Any	4.5 V		24	38		57		48	ns
			5.5 V		20	34		51		43	
t_{pd}	$\overline{G2}$	Any	4.5 V		19	29		44		36	ns
			5.5 V		16	26		40		32	
t_{pd}	G1	Any	4.5 V		19	29		44		36	ns
			5.5 V		16	26		40		32	
t_{pd}	$\overline{GL}$	Any	4.5 V		29	42		63		52	ns
			5.5 V		25	36		57		47	
t_t		Any	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

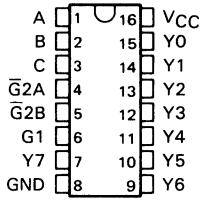
description

The 'HC238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of systems decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

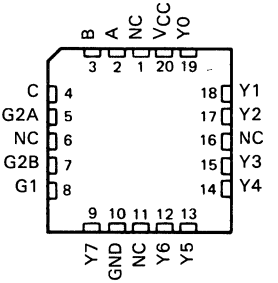
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54HC238 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC238 is characterized for operation from −40°C to 85°C.

SN54HC238 . . . J PACKAGE
SN74HC238 . . . DW OR N PACKAGE
(TOP VIEW)

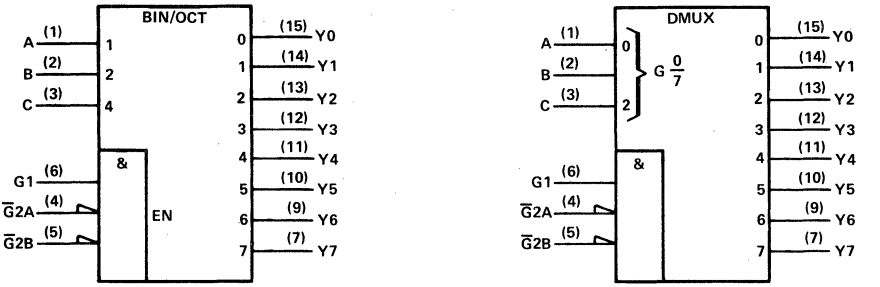


SN54HC238 . . . FK PACKAGE
(TOP VIEW)



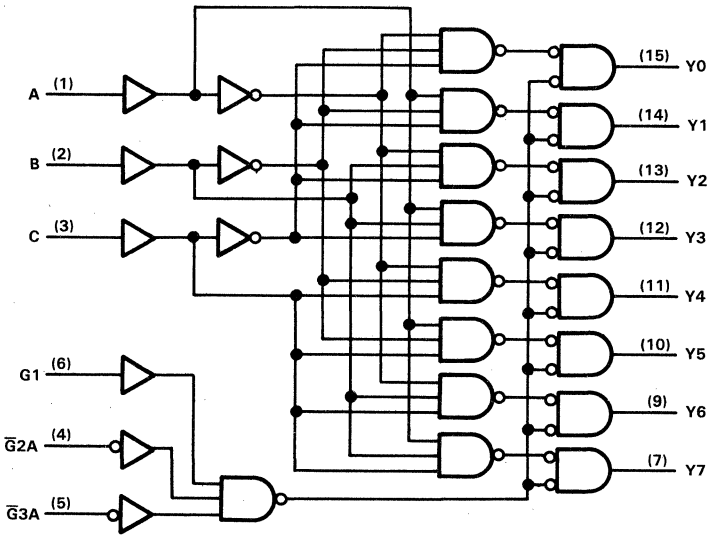
NC—No internal connection

logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC238			SN74HC238			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC238		SN74HC238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = − 5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC238		SN74HC238		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any	2 V		67	180		270		225	ns
			4.5 V		20	36		54		45	
			6 V		15	31		46		38	
t_{pd}	Enable	Any	2 V		60	155		235		195	ns
			4.5 V		17	31		47		39	
			6 V		13	26		40		33	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

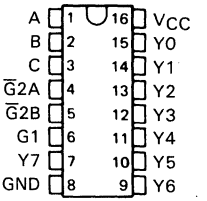
description

The 'HCT238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of systems decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

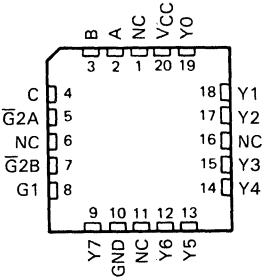
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54HCT238 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT238 is characterized for operation from −40°C to 85°C.

SN54HCT238 . . . J PACKAGE
SN74HCT238 . . . DW OR N PACKAGE
(TOP VIEW)



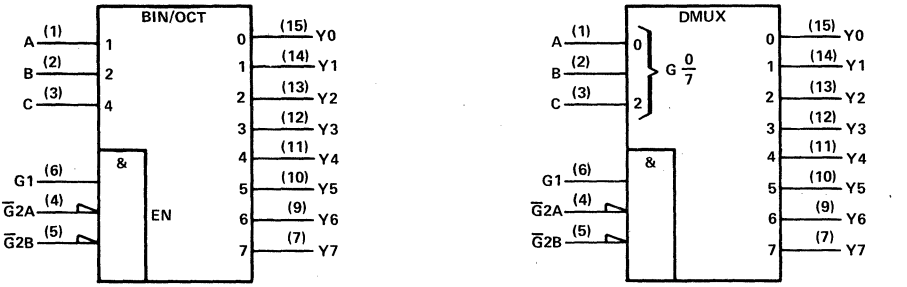
SN54HCT238 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

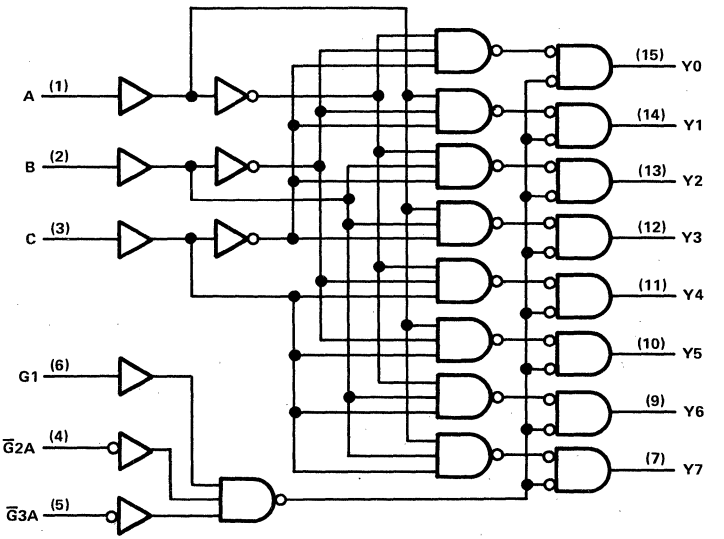
2 HCMOS Devices

logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT238			SN74HCT238			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT238		SN74HCT238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT238		SN74HCT238		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any	4.5 V		21	36		54		45	ns
			5.5 V		18	32		49		41	
t_{pd}	Enable	Any	4.5 V		21	33		50		42	ns
			5.5 V		17	30		45		38	
t_t		Any	4.5 V		11	15		22		19	ns
			5.5 V		9	14		20		17	

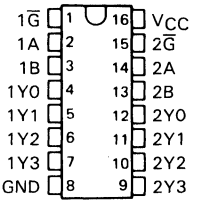
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

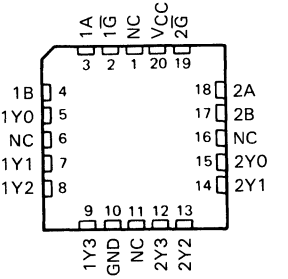
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC239 . . . J PACKAGE
SN74HC239 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC239 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

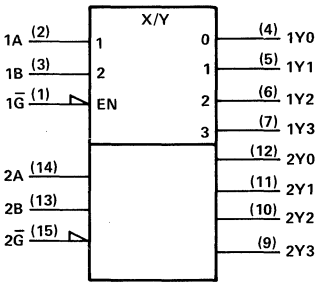
description

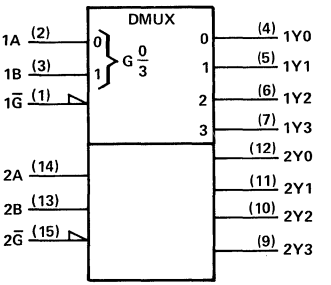
The 'HC239 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The 'HC239 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HC239 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC239 is characterized for operation from −40°C to 85°C.

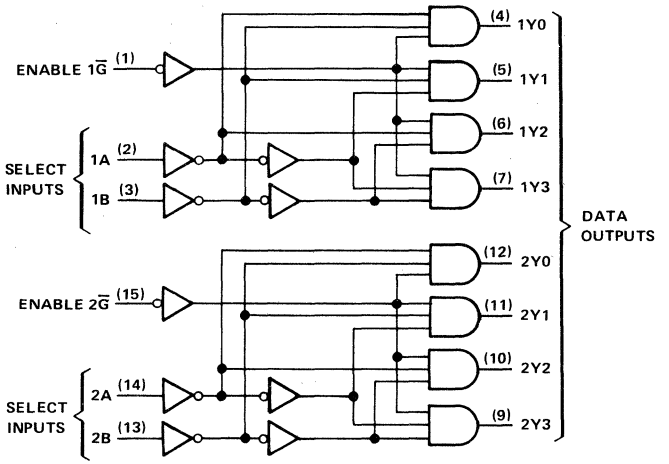
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HC239			SN74HC239			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC239		SN74HC239		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = − 5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC239		SN74HC239		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		62	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_{pd}	$\overline{G}$	Y	2 V		53	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{pd}		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per decoder	No load, T_A = 25°C	25 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

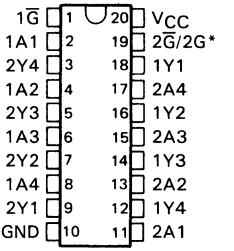
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

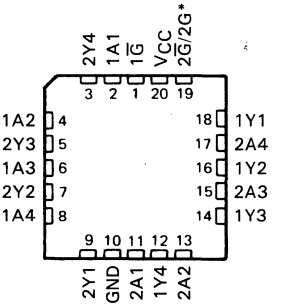
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.

SN54HC' . . . J PACKAGE
SN74HC' . . . DW OR N PACKAGE
(TOP VIEW)



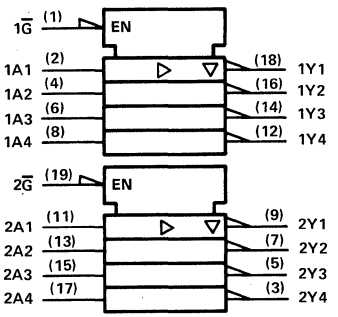
SN54HC' . . . FK PACKAGE
(TOP VIEW)



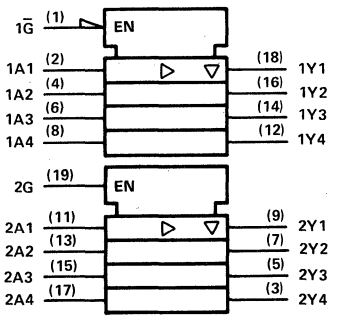
*$2\overline{G}$ for 'HC240, or 2G for 'HC241

logic symbols†

'HC240



'HC241



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLES

'HC240
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

'HC241
(EACH BUFFER IN FIRST SET)

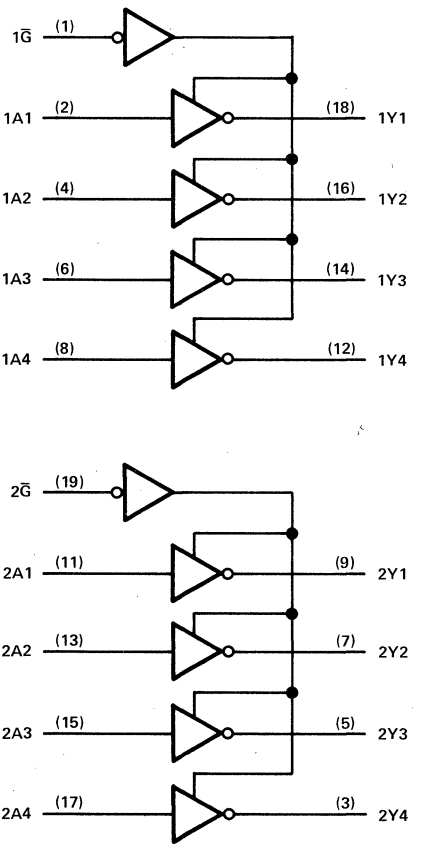
INPUTS		OUTPUT
$1\overline{G}$	1A	1Y
L	H	H
L	L	L
H	X	Z

'HC241
(EACH BUFFER IN SECOND SET)

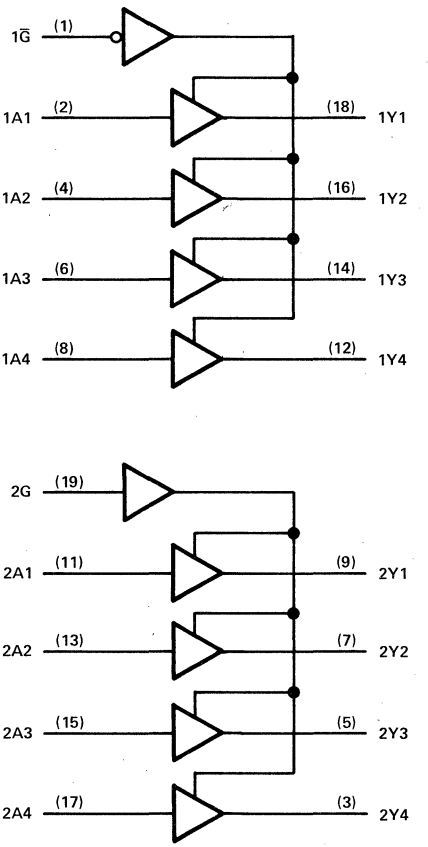
INPUTS		OUTPUT
2G	2A	2Y
H	H	H
H	L	L
L	X	Z

logic diagrams (positive logic)

'HC240



'HC241



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC240 SN54HC241			SN74HC240 SN74HC241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC240 SN54HC241		SN74HC240 SN74HC241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		V
	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
t_{en}	$\overline{G}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Y	2 V		44	150		225		190	ns
			4.5 V		22	30		45		38	
			6 V		21	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per buffer	No load, T_A = 25°C	35 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	$\overline{G}$	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		39	115		170		145	ns
			4.5 V		12	23		34		29	
			6 V		11	20		29		25	
t_{en}	$\overline{G}$ or G	Y	2 V		60	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		15	26		38		32	
t_{dis}	$\overline{G}$ or G	Y	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per buffer	No load, T_A = 25°C	35 pF typ

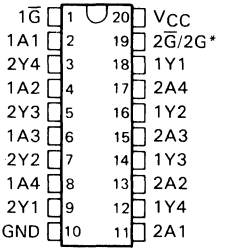
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	165		245		210	ns
			4.5 V		16	33		49		42	
			6 V		14	28		42		35	
t_{en}	$\overline{G}$ or G	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

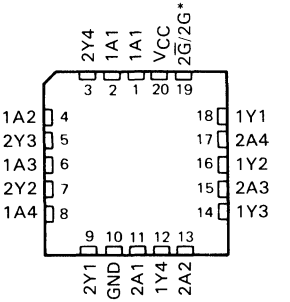
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT' . . . J PACKAGE
SN74HCT' . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT' . . . FK PACKAGE
(TOP VIEW)



*2G̅ for 'HCT240, or 2G for 'HCT241

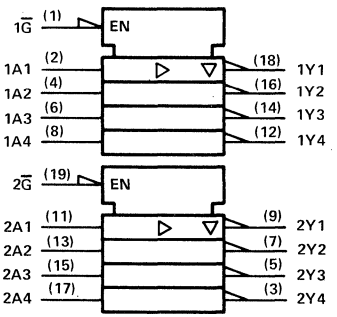
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G̅ (active-low output control) inputs, and complementary G and G̅ inputs. These devices feature high fan-out.

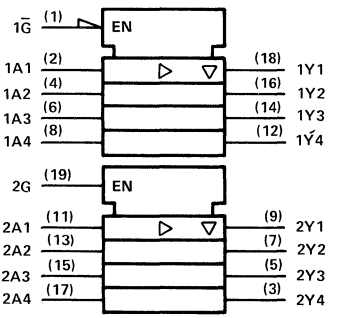
The SN54HCT' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT' family is characterized for operation from −40°C to 85°C.

logic symbols†

'HCT240



'HCT241



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLES

'HCT240
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

'HCT241
(EACH BUFFER IN FIRST SET)

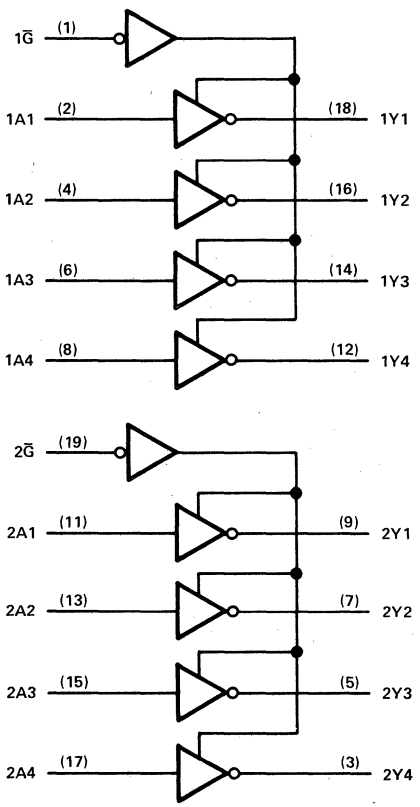
INPUTS		OUTPUT
$1\overline{G}$	1A	1Y
L	H	H
L	L	L
H	X	Z

'HCT241
(EACH BUFFER IN SECOND SET)

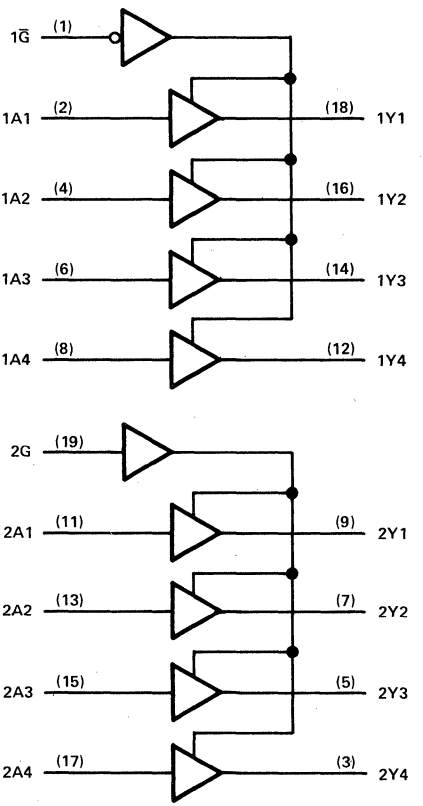
INPUTS		OUTPUT
2G	2A	2Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)

'HCT240



'HCT241



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT240 SN54HCT241			SN74HCT240 SN74HCT241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT240 SN54HCT241		SN74HCT240 SN74HCT241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20\ \mu A$	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -6$ mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 20\ \mu A$	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 6$ mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3.0		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT240 SN54HCT241		SN74HCT240 SN74HCT241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	25		37		32	ns
			5.5 V		12	23		33		29	
t_{en}	G or $\overline{G}$	Y	4.5 V		21	35		53		44	ns
			5.5 V		19	32		48		40	
t_{dis}	G or $\overline{G}$	Y	4.5 V		19	35		53		44	ns
			5.5 V		18	32		48		40	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance per buffer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT240 SN54HCT241		SN74HCT240 SN74HCT241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	42		63		53	ns
			5.5 V		19	38		56		48	
t_{en}	G or $\overline{G}$	Y	4.5 V		25	52		79		65	ns
			5.5 V		22	47		71		59	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **2-Way Asynchronous Communication Between Data Buses**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These four-data line tranceivers are designed for asynchronous two-way communications between data buses. The SN74HC' devices can be used to drive terminated lines down to 133 Ω.

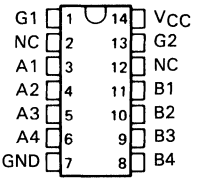
These parts differ from their TTL counterparts (LS, ALS, and AS) in that these CMOS parts do not have a bus-latching mode in which both the outputs are simultaneously enabled. Instead of this latched mode, the buses are isolated, thus preventing potential bus conflicts if both buses are active. However, with the exception of the fourth line of the function table, their functional operation is identical to their TTL counterparts. The two enables have been renamed G1 and G2 since they work together to determine the direction of transmission rather than each enable controlling one direction independently of the other. Whenever G1 and G2 are at opposite logic levels with respect to each other, isolation between buses results.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.

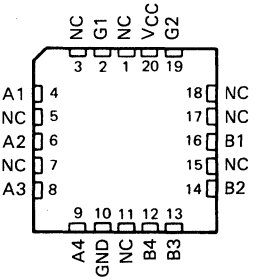
FUNCTION TABLE

INPUTS		'HC242	'HC243
G1	G2		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

SN54HC242, SN54HC243 . . . J PACKAGE
SN74HC242, SN74HC243 . . . D OR N PACKAGE
(TOP VIEW)



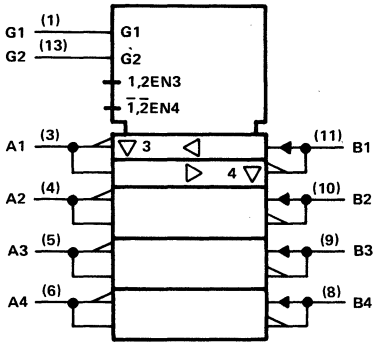
SN54HC242, SN54HC243 . . . FK PACKAGE
(TOP VIEW)



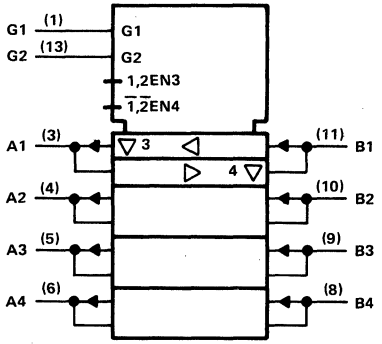
NC—No internal connection

logic symbols†

'HC242



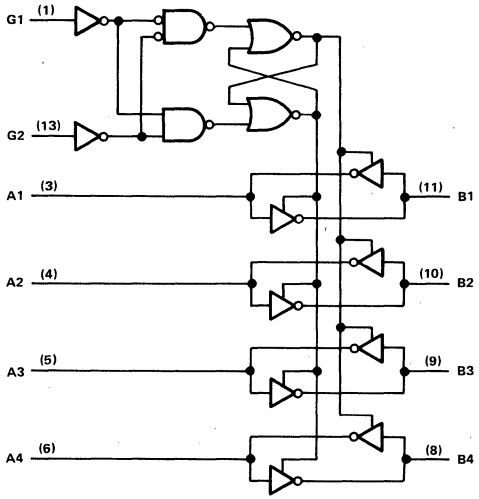
'HC243



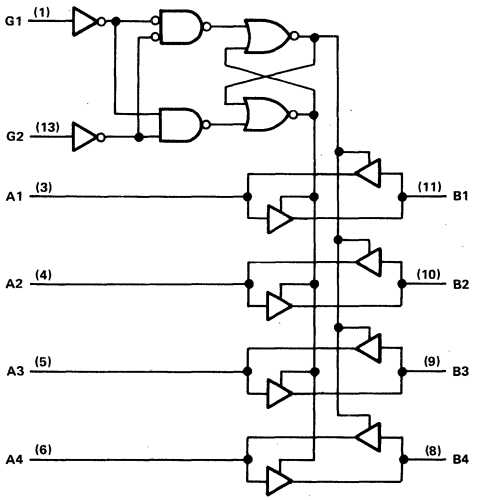
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagrams (positive logic)

'HC242



'HC243



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC242 SN54HC243			SN74HC242 SN74HC243			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}†	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i‡		2 to 6 V		3	10		10		10	pF

†For I/O ports, the parameter is included in the off-state output current.

‡This parameter C_i does not apply to I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		45	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		26		21	
t_{en}	G1 or G2	A or B	2 V		75	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		17	26		38		32	
t_{dis}	G1 or G2	A or B	2 V		48	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		20	26		38		32	
t_t		A or B	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	34 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC242 SN54HC243		SN74HC242 SN74HC243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		63	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		38		32	
t_{en}	G1 or G2	A or B	2 V		100	200		300		250	ns
			4.5 V		26	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2804, MARCH 1984 – REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **2-Way Asynchronous Communication Between Data Buses**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These four-data line tranceivers are designed for asynchronous two-way communications between data buses. The SN74HCT' devices can be used to drive terminated lines down to 133 Ω.

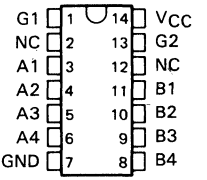
These parts differ from their TTL counterparts (LS, ALS, and AS) in that these CMOS parts do not have a bus-latching mode in which both the outputs are simultaneously enabled. Instead of this latched mode, the buses are isolated, thus preventing potential bus conflicts if both buses are active. However, with the exception of the fourth line of the function table, their functional operation is identical to their TTL counterparts. The two enables have been renamed G1 and G2 since they work together to determine the direction of transmission rather than each enable controlling one direction independently of the other. Whenever G1 and G2 are at opposite logic levels with respect to each other, isolation between buses results.

The SN54HCT'family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT' is characterized for operation from −40°C to 85°C.

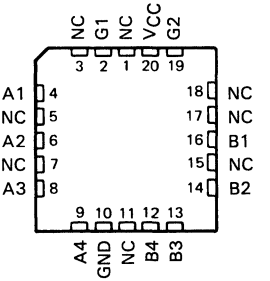
FUNCTION TABLE

INPUTS		'HCT242	'HCT243
G1	G2		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

SN54HCT242, SN54HCT243 . . . J PACKAGE
SN74HCT242, SN74HCT243 . . . D OR N PACKAGE
(TOP VIEW)



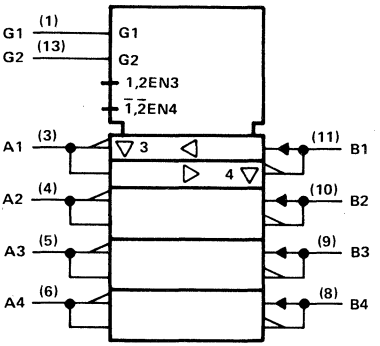
SN54HCT242, SN54HCT243 . . . FK PACKAGE
(TOP VIEW)



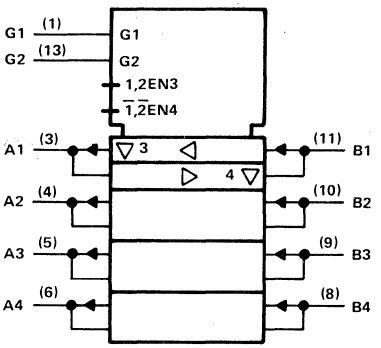
NC—No internal connection

logic symbols†

'HCT242



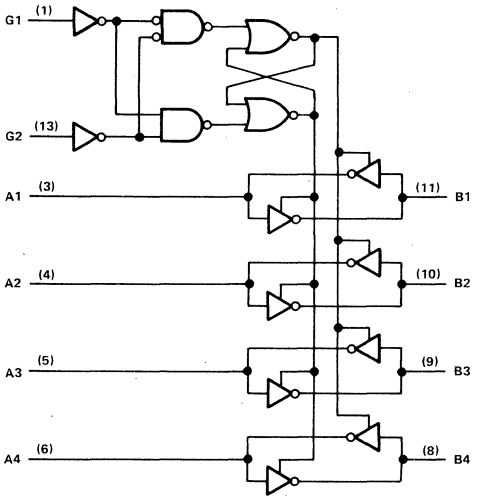
'HCT243



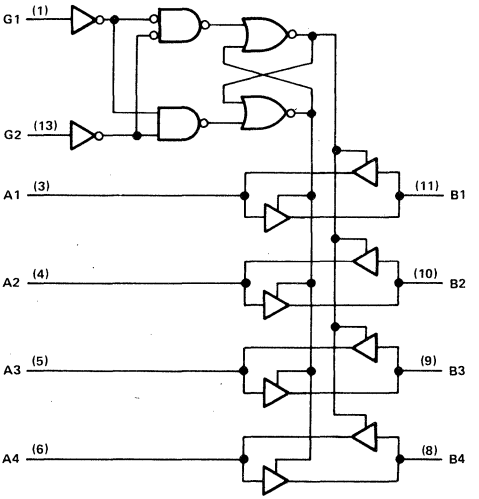
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'HCT242



'HCT243



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating contitions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT242 SN54HCT243			SN74HCT242 SN74HCT243			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	V
T_A	Operating free-air temperature		−55		125	−40		85	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT242 SN54HCT243		SN74HCT242 SN74HCT243		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = − 6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}‡	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		2.9		3	mA
C_i¶		4.5 to 5.5 V		3	10		10		10	pF

‡For I/O ports, the parameter is included in the off-state output current.
§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
¶This parameter, C_i, does not apply to transceiver I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT242 SN54HCT243		SN74HCT242 SN74HCT243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	30		45		38	ns
			5.5 V		13	27		41		34	
t_{en}	G1 or G2	A or B	4.5 V		21	40		60		50	ns
			5.5 V		19	36		54		45	
t_{dis}	G1 or G2	A or B	4.5 V		19	40		60		50	ns
			5.5 V		18	36		54		45	
t_t		A or B	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance per tranceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT242 SN54HCT243		SN74HCT242 SN74HCT243		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		21	47		71		59	ns
			5.5 V		18	42		64		53	
t_{en}	G1 or G2	A or B	4.5 V		27	57		86		71	ns
			5.5 V		24	51		77		64	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

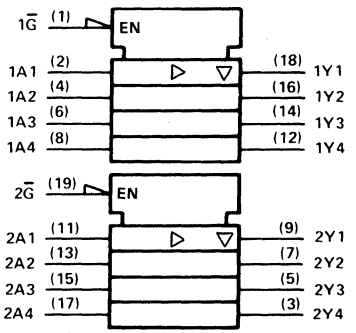
- **3-State Output Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of the three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'HC240 and 'HC241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs and complementary G and $\overline{G}$ inputs.

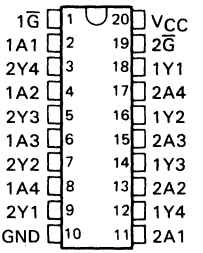
The SN54HC244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC244 is characterized for operation from −40°C to 85°C.

logic symbol†

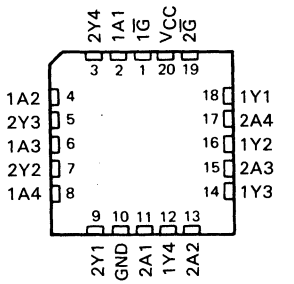


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

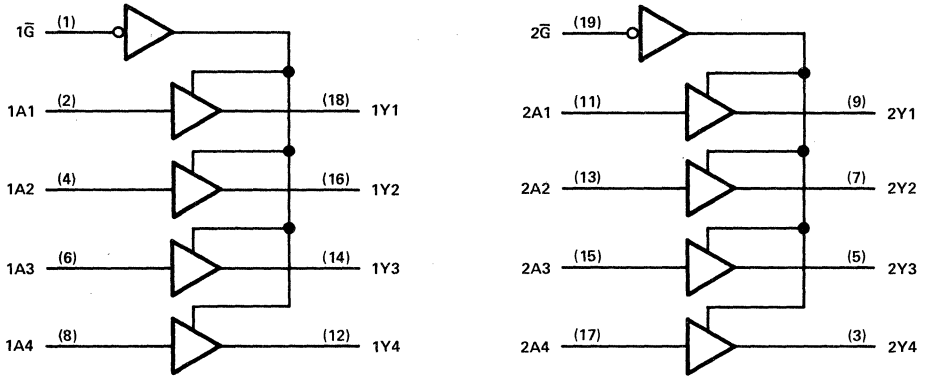
SN54HC244 . . . J PACKAGE
SN74HC244 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC244 . . . FK PACKAGE
(TOP VIEW)



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC244			SN74HC244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	115		170		145	ns
			4.5 V		13	23		34		29	
			6 V		11	20		29		25	
t_{en}	$\overline{G}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		56	165		245		210	ns
			4.5 V		18	33		49		42	
			6 V		15	28		42		35	
t_{en}	$\overline{G}$	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

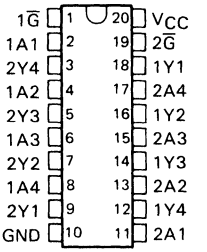
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

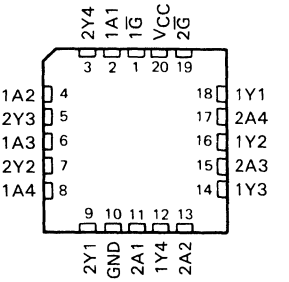
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT244 . . . J PACKAGE
SN74HCT244 . . . DW OR N PACKAGE
(TOP VIEW)



SN74HCT244 . . . FK PACKAGE
(TOP VIEW)

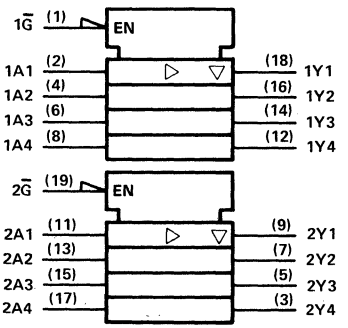


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'HCT240 and 'HCT241, these devices provide the choice of selected combinations of inverting outputs, symetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

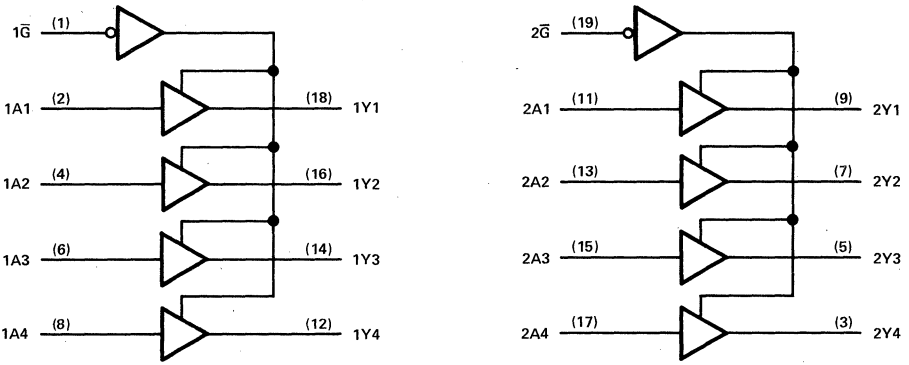
The SN54HCT244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT244 is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT244			SN74HCT244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		15	28		42		35	ns
			5.5 V		13	25		38		32	
t_{en}	$\overline{G}$	Y	4.5 V		21	35		53		44	ns
			5.5 V		19	32		48		40	
t_{dis}	$\overline{G}$	Y	4.5 V		19	35		53		44	ns
			5.5 V		18	32		48		40	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance per buffer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		21	45		68		56	ns
			5.5 V		18	40		61		51	
t_{en}	$\overline{G}$	Y	4.5 V		25	52		79		65	ns
			5.5 V		22	47		71		59	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

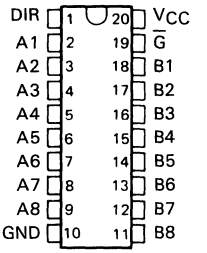
description

These octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

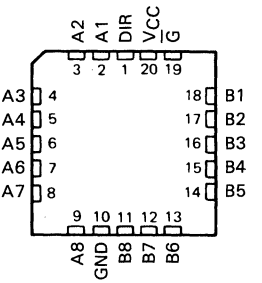
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54HC245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC245 is characterized for operation from −40°C to 85°C.

SN54HC245 . . . J PACKAGE
SN74HC245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC245 . . . FK PACKAGE
(TOP VIEW)



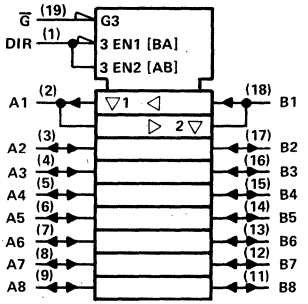
NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

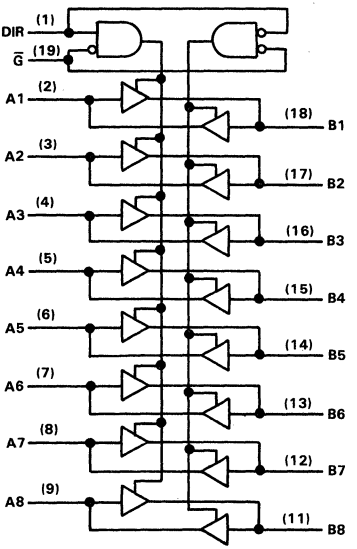
2 HCMOS Devices

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC245			SN74HC245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{G}$	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i	DIR or $\overline{G}$		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t_{en}	$\overline{G}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	$\overline{G}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

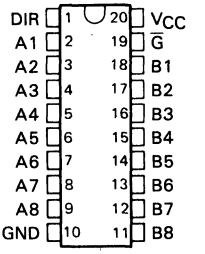
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54HCT245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT245 is characterized for operation from −40°C to 85°C.

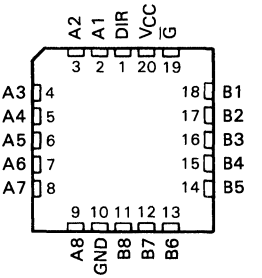
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

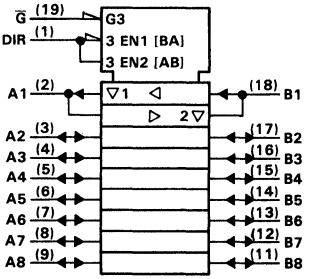
SN54HCT245 . . . J PACKAGE
SN74HCT245 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT245 . . . FK PACKAGE
(TOP VIEW)

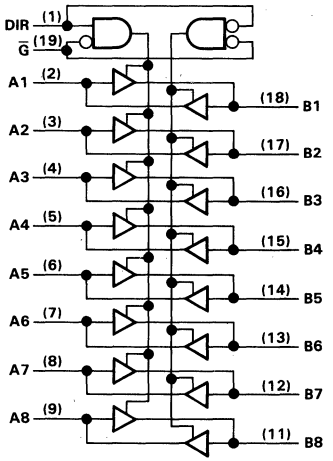


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT245			SN74HCT245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OL} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	01		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I DIR or $\overline{G}$	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ} A or B	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i DIR or $\overline{G}$‡		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
‡This parameter C_i does not apply to transceiver I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t_{en}	$\overline{G}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t_{dis}	$\overline{G}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{G}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **3-State Version of 'HC151**
- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

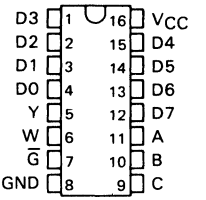
The SN54HC251 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC251 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

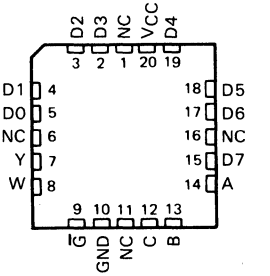
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0,D1 . . . D7 = the level of the respective D input.

SN54HC251 . . . J PACKAGE
SN74HC251 . . . D OR N PACKAGE
(TOP VIEW)

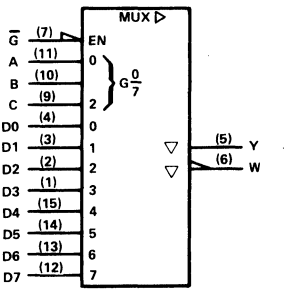


SN54HC251 . . . FK PACKAGE
(TOP VIEW)



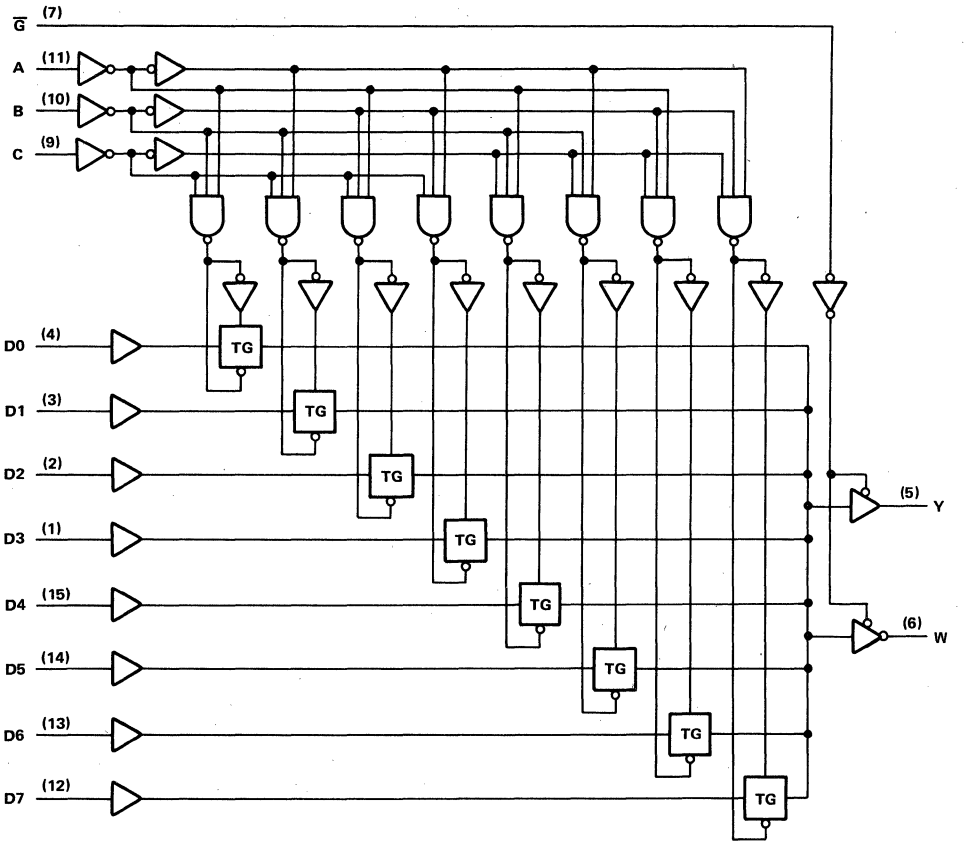
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC251			SN74HC251			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W or Y	2 V		58	205		300		256	ns
			4.5 V		21	41		60		51	
			6 V		19	35		51		44	
t_{pd}	Any D	W or Y	2 V		44	195		283		244	ns
			4.5 V		17	39		57		49	
			6 V		15	33		48		41	
t_{en}	$\overline{G}$	W or Y	2 V		30	145		210		181	ns
			4.5 V		10	29		42		36	
			6 V		9	25		36		31	
t_{dis}	$\overline{G}$	W or Y	2 V		25	195		283		244	ns
			4.5 V		15	39		57		49	
			6 V		14	33		48		41	
t_t			2 V		20	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	70 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W or Y	2 V		72	300		450		375	ns
			4.5 V		25	60		90		75	
			6 V		22	52		77		65	
t_{pd}	Any D	W or Y	2 V		59	300		450		375	ns
			4.5 V		21	60		90		75	
			6 V		18	52		77		65	
t_{en}	$\overline{G}$	W or Y	2 V		50	230		340		285	ns
			4.5 V		17	46		68		57	
			6 V		15	40		58		50	
t_t			2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **3-State Versions of 'HC153**
- **High-Current Inverting Outputs Drive Up to 15 LSTTL Loads**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

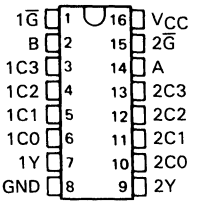
The SN54HC253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC253 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

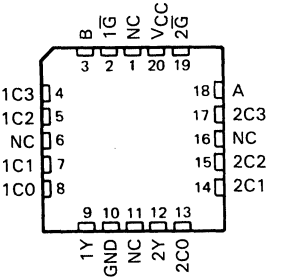
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

SN54HC253 . . . J PACKAGE
SN74HC253 . . . D/DW† OR N PACKAGE
(TOP VIEW)



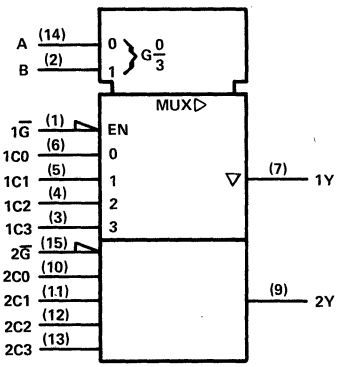
SN54HC253 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

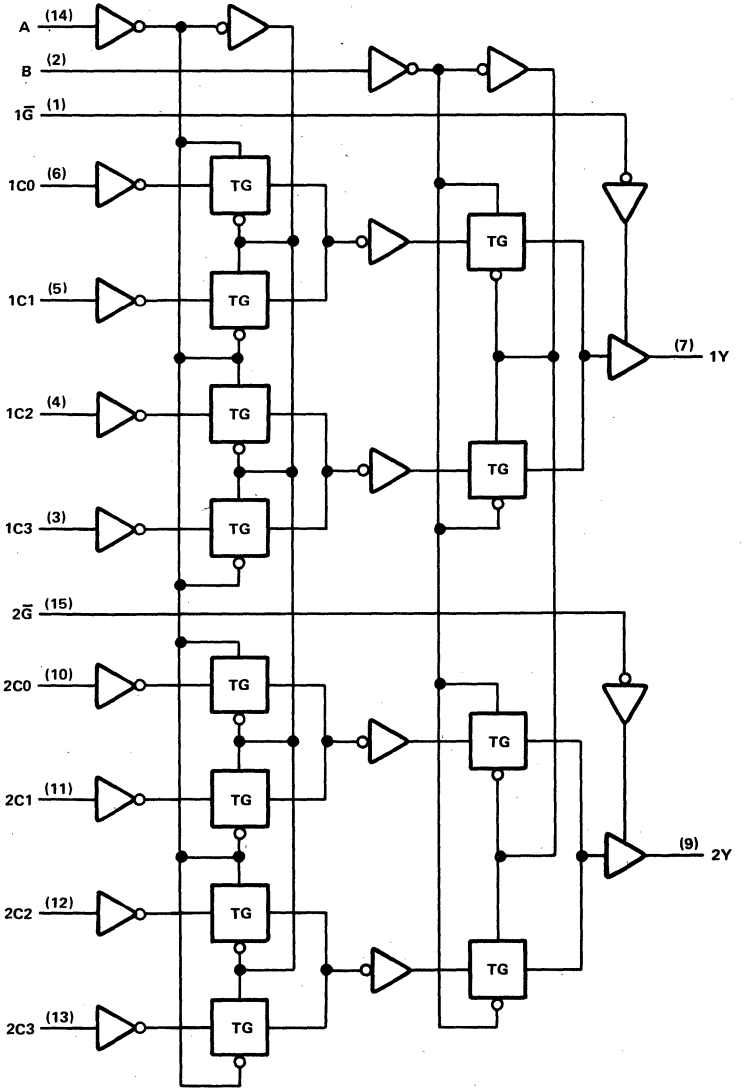
†Contact the factory for D or DW availability.

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D/DW†, J, and N packages

logic diagram (positive logic)



Pin numbers shown are for D/DW†, J, and N packages

†Contact the factory for D or DW availability

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D/DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC253			SN74HC253			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		62	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		16	26		38		32	
t_{pd}	Data (Any C)	Y	2 V		54	126		210		175	ns
			4.5 V		16	28		42		35	
			6 V		13	23		36		30	
t_{en}	$\overline{G}$	Y	2 V		28	100		150		125	ns
			4.5 V		11	20		30		25	
			6 V		9	17		26		21	
t_{dis}	$\overline{G}$	Y	2 V		21	135		203		170	ns
			4.5 V		14	30		45		38	
			6 V		12	35		38		31	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	45 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		76	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	41		60		51	
t_{pd}	Data (Any C)	Y	2 V		68	220		335		275	ns
			4.5 V		20	44		67		55	
			6 V		17	38		57		51	
t_{en}	$\overline{G}$	Y	2 V		44	185		280		230	ns
			4.5 V		16	37		56		46	
			6 V		14	32		48		40	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Provides Bus Interface from Multiple Sources in High Performance Systems**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

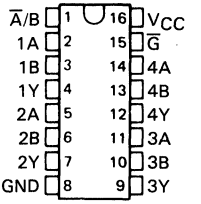
These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level.

The SN54HC257 and SN54HC258 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC257 and SN74HC258 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

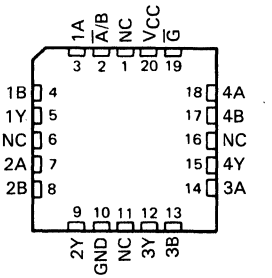
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	'HC257	'HC258
H	X	X	X	Z	$\overline{Z}$
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

SN54HC257, SN54HC258 . . . J PACKAGE
SN74HC257, SN74HC258 . . . D/DW† OR N PACKAGE
(TOP VIEW)



†Contact the factory for D or DW availability.

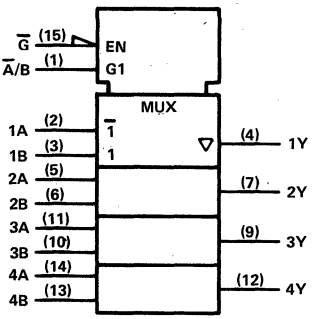
SN54HC257, SN54HC258 . . . FK PACKAGE
(TOP VIEW)



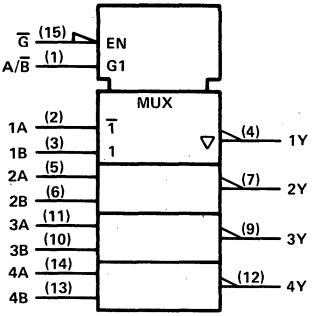
NC—No internal connection

logic symbols†

'HC257



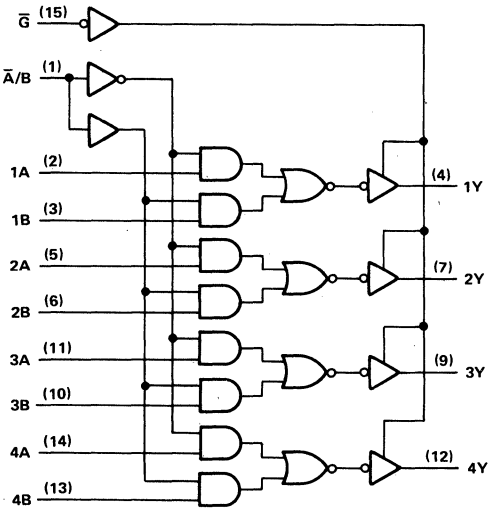
'HC258



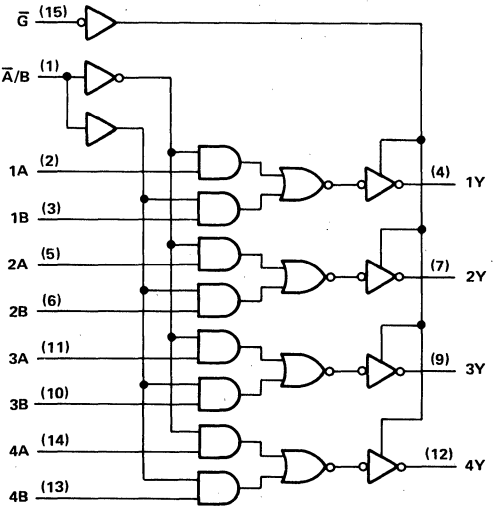
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'HC257



'HC258



Pin numbers shown are for D/DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D, DW, or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC257 SN54HC258			SN74HC257 SN74HC258			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC257 SN54HC258		SN74HC257 SN74HC258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
t_{pd}	$\overline{A}$/B	Any Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
t_{en}	$\overline{G}$	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC257		SN74HC257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		75	150		245		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	$\overline{A}$/B	Any Y	2 V		75	150		245		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	$\overline{G}$	Any Y	2 V		100	200		300		250	ns
			4.5 V		24	40		60		50	
			6 V		18	34		51		43	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		60	100		150		125	ns
			4.5 V		13	20		30		25	
			6 V		12	17		25		21	
t_{pd}	$\overline{A}$/B	Any Y	2 V		60	115		175		145	ns
			4.5 V		13	23		35		29	
			6 V		12	20		30		25	
t_{en}	$\overline{G}$	Any Y	2 V		70	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Any Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

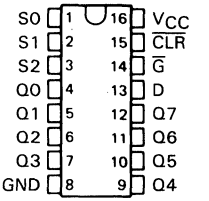
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC258		SN74HC258		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		95	150		245		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_{pd}	$\overline{A}$/B	Any Y	2 V		95	165		240		210	ns
			4.5 V		23	33		48		42	
			6 V		21	28		41		36	
t_{en}	$\overline{G}$	Any Y	2 V		100	200		300		250	ns
			4.5 V		24	40		60		50	
			6 V		18	34		51		43	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

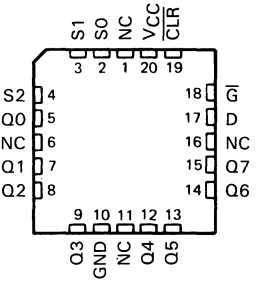
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC259 . . . J PACKAGE
SN74HC259 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC259 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers; serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC259 is characterized for operation from −40°C to 85°C.

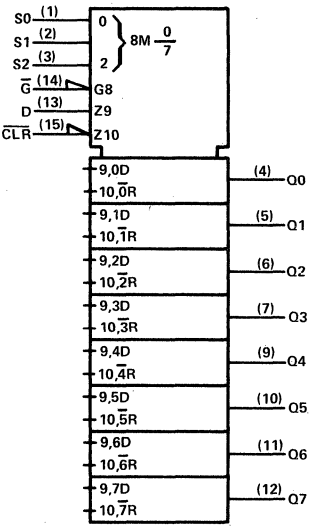
FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

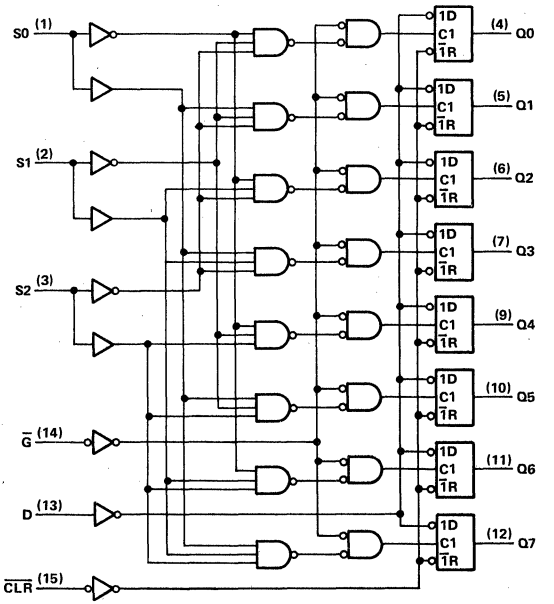
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

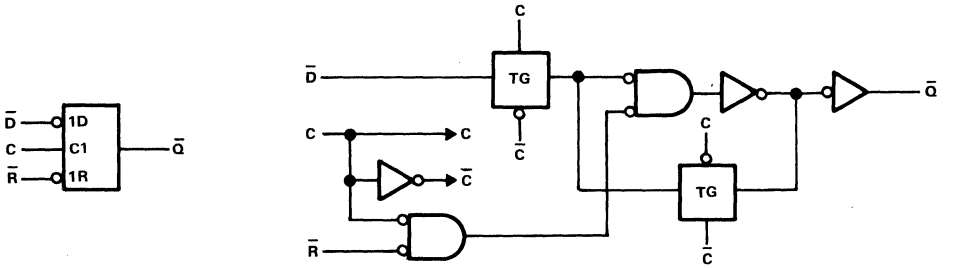
logic diagrams (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic symbol and logic diagram, each internal latch (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC259			SN74HC259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC259		SN74HC259		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC259		SN74HC259		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{G}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, data or address before $\overline{G}$↑		2 V	75		115		95		ns
			4.5 V	15		23		19		
			6 V	13		20		16		
t_h	Hold time, data or address after $\overline{G}$↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC259		SN74HC259		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	$\overline{CLR}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_{pd}	Data	Any Q	2 V		56	130		195		165	ns
			4.5 V		17	26		39		33	
			6 V		13	22		33		28	
t_{pd}	Address	Any Q	2 V		74	200		300		250	ns
			4.5 V		21	40		60		50	
			6 V		17	34		51		43	
t_{pd}	$\overline{G}$	Any Q	2 V		66	170		255		215	ns
			4.5 V		20	34		51		43	
			6 V		16	29		43		37	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	33 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

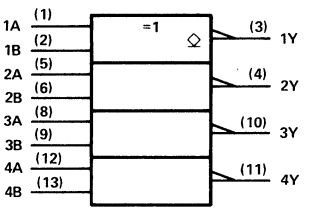
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices are composed of four independent 2-input exclusive-NOR gates and feature open-drain outputs. They perform the Boolean functions: $Y = \overline{A \oplus B} = \overline{A}\overline{B} + AB$ in positive logic.

The SN54HC266 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC266 is characterized for operation from −40°C to 85°C.

logic symbol†

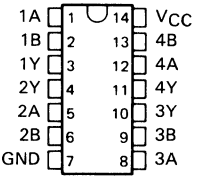


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

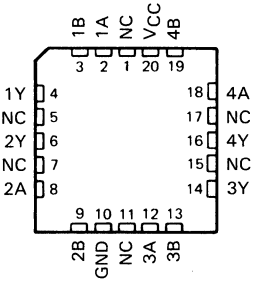
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

SN54HC266 . . . J PACKAGE
SN74HC266 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC266 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC266			SN74HC266			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC266		SN74HC266		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC266		SN74HC266		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	125		190		155	ns
			4.5 V		13	25		38		31	
			6 V		10	23		32		26	
t_{PHL}	A or B	Y	2 V		60	100		150		125	ns
			4.5 V		13	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

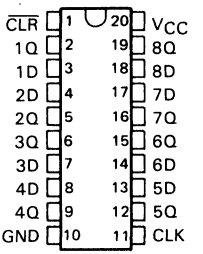
C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

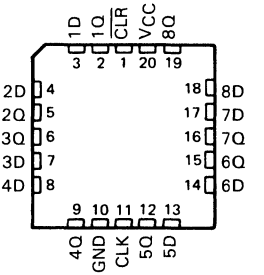
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Contains Eight Flip-Flops with Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC273 . . . J PACKAGE
SN74HC273 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC273 . . . FK PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear input.

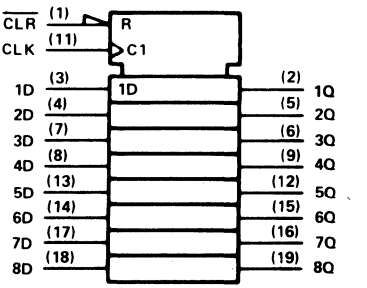
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54HC273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC273 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOPS)

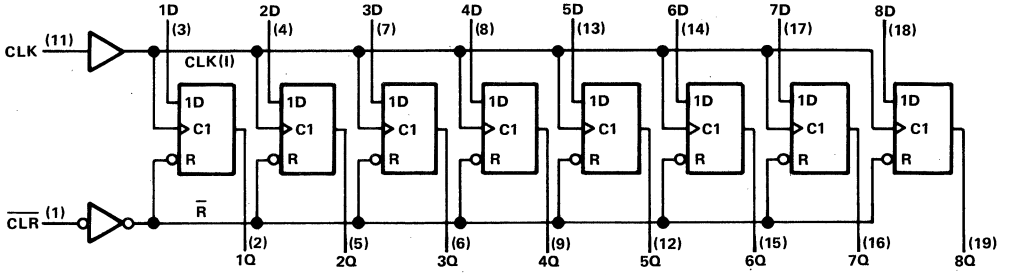
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†

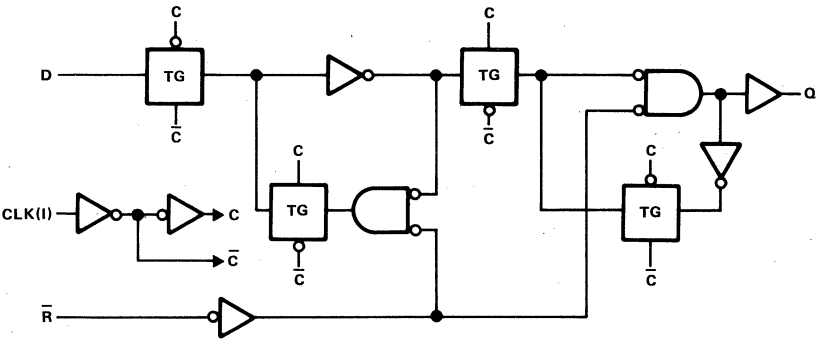


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, total device (positive logic)



logic diagram each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC273			SN74HC273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC273			SN74HC273			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9			1.9			V
		4.5 V	4.4	4.499		4.4			4.4			
		6 V	5.9	5.999		5.9			5.9			
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7			3.84			
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2			5.34			
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1			0.1			0.1	V
		4.5 V		0.001	0.1			0.1			0.1	
		6 V		0.001	0.1			0.1			0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26			0.4			0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26			0.4			0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100			±1000			±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8			160			80	μA
C_i		2 to 6 V		3	10			10			10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C			SN54HC273		SN74HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0		5	0	4	0	4	MHz
			4.5 V	0		27	0	18	0	21	
			6 V	0		32	0	21	0	25	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80			120		100		ns
			4.5 V	16			24		20		
			6 V	14			20		17		
		CLK high or low	2 V	80			120		100		ns
			4.5 V	16			24		20		
			6 V	14			20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100			150		125		ns
			4.5 V	20			30		25		
			6 V	17			25		21		
		$\overline{CLR}$ inactive	2 V	100			150		125		ns
			4.5 V	20			30		25		
			6 V	17			25		21		
t_h	Hold time, data after CLK↑		2 V	0			0		0		ns
			4.5 V	0			0		0		
			6 V	0			0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC273		SN74HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	11		4		4		MHz
			4.5 V	27	50		18		21		
			6 V	32	60		28		25		
t_{PHL}	$\overline{CLR}$	Any	2 V		55	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
t_{pd}	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		13	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits**
- **Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

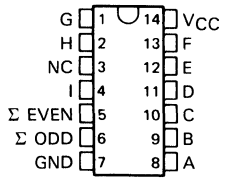
These universal, monolithic, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The SN54HC280 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC280 is characterized for operation from −40°C to 85°C.

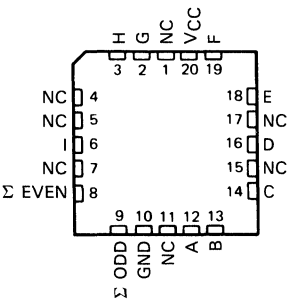
FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 2, 5, 7, 9	L	H

SN54HC280 . . . J PACKAGE
SN74HC280 . . . D OR N PACKAGE
(TOP VIEW)

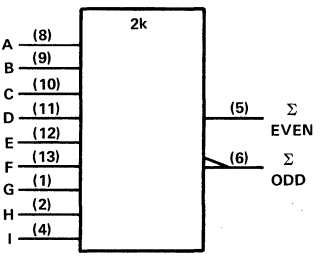


SN54HC280 . . . FK PACKAGE
(TOP VIEW)



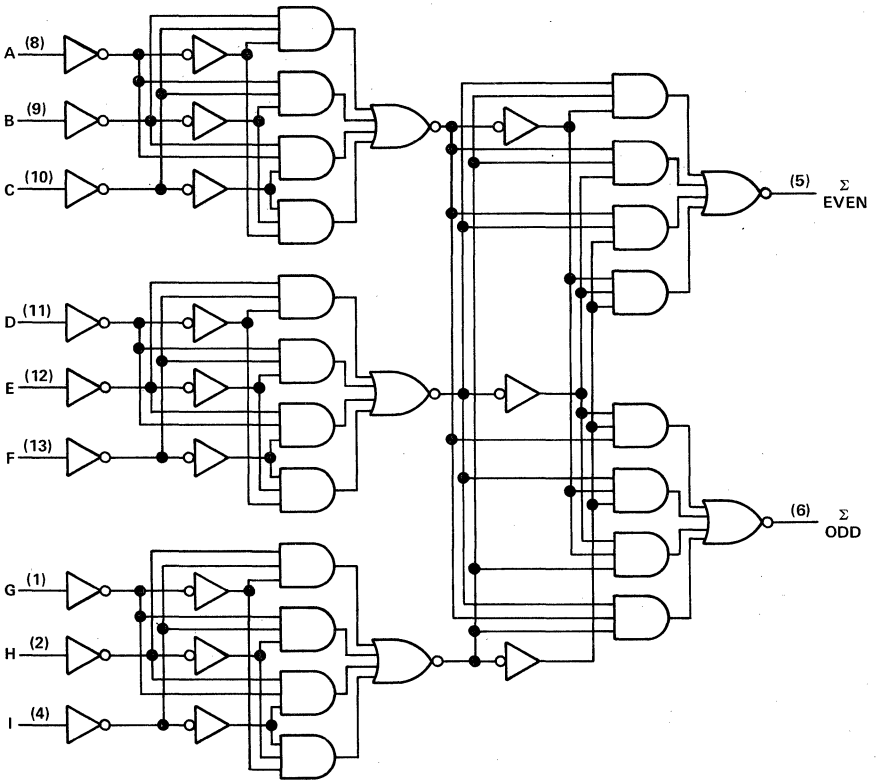
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HC280			SN74HC280			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC280			SN74HC280			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9			1.9			V
		4.5 V	4.4	4.499		4.4			4.4			
		6 V	5.9	5.999		5.9			5.9			
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7			3.84			
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2			5.34			
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1			0.1			0.1	V
		4.5 V		0.001	0.1			0.1			0.1	
		6 V		0.001	0.1			0.1			0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26			0.4			0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26			0.4			0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100			±1000			±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8			160			80	μA
C_i		2 to 6 V		3	10			10			10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC280		SN74HC280		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A thru I	Σ Even or Σ Odd	2 V		103	205		305		260	ns
			4.5 V		21	41		61		52	
			6 V		17	35		52		44	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

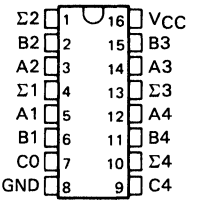
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

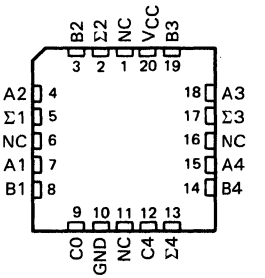
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**
- **Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC283 . . . J PACKAGE
SN74HC283 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC283 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit, and the resultant carry (C4) is obtained from the fourth bit.

These adders feature full internal look-ahead across all four bits generating the carry term. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

The SN54HC283 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC283 is characterized for operation from −40°C to 85°C.

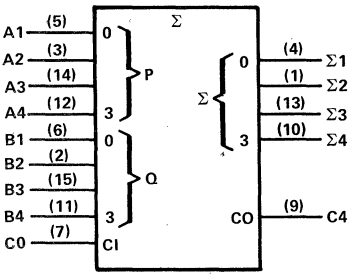
FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

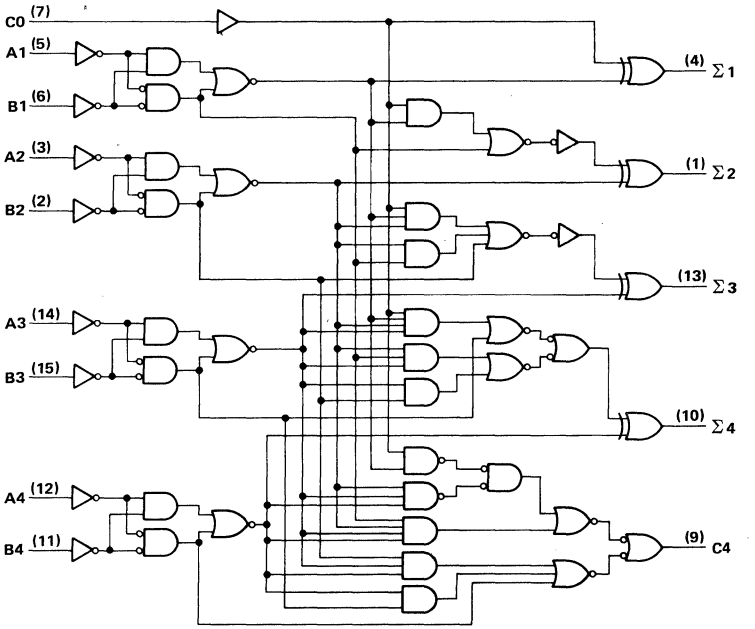
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC283			SN74HC283			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC283			SN74HC283			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9			1.9			V
		4.5 V	4.4	4.499		4.4			4.4			
		6 V	5.9	5.999		5.9			5.9			
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7			3.84			
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2			5.34			
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1			0.1			0.1	V
		4.5 V		0.001	0.1			0.1			0.1	
		6 V		0.001	0.1			0.1			0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26			0.4			0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26			0.4			0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100			±1000			±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8			160			80	μA
C_i		2 to 6 V		3	10			10			10	pF

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC283		SN74HC283		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CO	Any Σ	2 V		60	150		225		188	ns
			4.5 V		20	30		45		37	
			6 V		16	26		38		32	
t_{pd}	Ai or Bi	Σi	2 V		80	175		262		218	ns
			4.5 V		25	35		52		44	
			6 V		20	30		45		37	
t_{pd}	CO	C4	2 V		70	175		262		218	ns
			4.5 V		25	35		52		44	
			6 V		20	30		45		37	
t_{pd}	Ai or Bi	C4	2 V		90	175		262		218	ns
			4.5 V		26	35		52		44	
			6 V		21	30		45		37	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	90 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data**
- **Implements Separate Registers Capable of Parallel Exchange of Contents, Yet Retains External Load Capability**
- **Has Universal-Type Register for Implementing Various Shift Patterns**
- **Has Compound Left-Right Capability**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

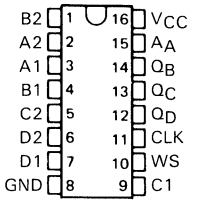
description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions ('HC157 and 'HC175) in a single 16-pin package.

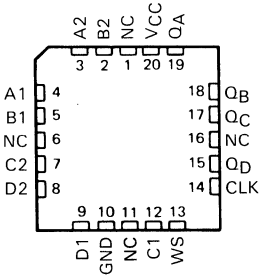
When the Word-Select (WS) input is low, word one (A1, B1, C1, D1) is applied to the flip-flops. A high Word-Select input causes word two (A2, B2, C2, D2) to be selected. The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

The SN54HC298 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC298 is characterized for operation from −40°C to 85°C.

SN54HC298 . . . J PACKAGE
SN74HC298 . . . DW OR N PACKAGE
(TOP VIEW)

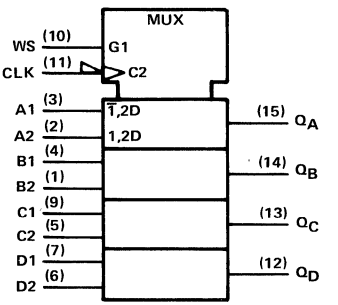


SN54HC298 . . . FK PACKAGE
(TOP VIEW)



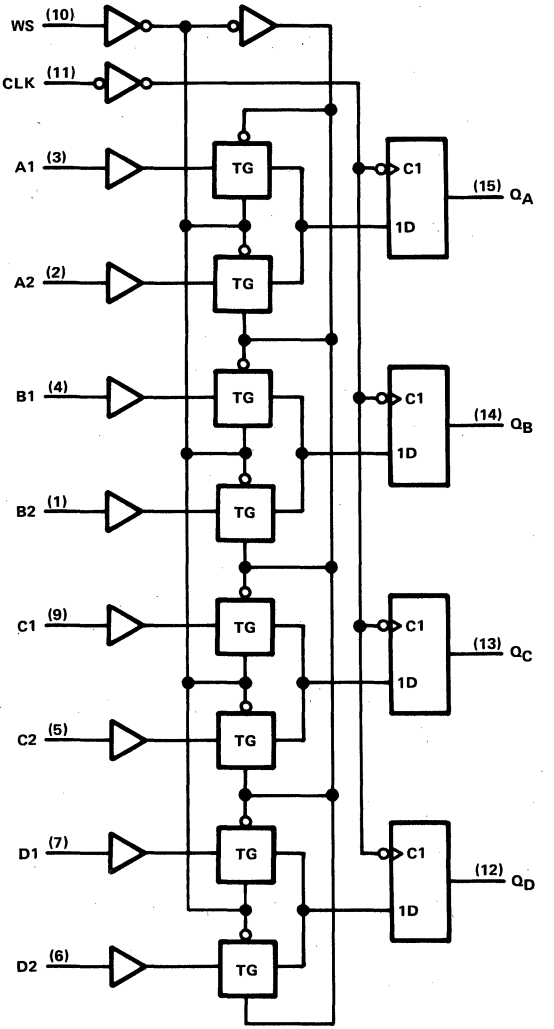
NC – No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC298			SN74HC298			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC298		SN74HC298		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC298		SN74HC298		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6.5		4.3		5.5	MHz
			4.5 V		33		22		27	
			6 V		38		25		31	
t_w	Pulse duration, CLK high or low		2 V	75		115		95		ns
			4.5 V	15		23		19		
			6 V	13		20		16		
t_{su}	Setup time	Data before CLK↓	2 V	80		125		105		ns
			4.5 V	16		25		21		
			6 V	14		21		18		
		WS before CLK↓	2 V	80		125		105		
			4.5 V	16		25		21		
			6 V	14		21		18		
t_h	Hold time	Data after CLK↓	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		
		WS after CLK↓	2 V	0		0		0		
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC298		SN74HC298		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6.5			4.3		5.5		MHz
			4.5 V	33			22		27		
			6 V	38			25		31		
t_{pd}	CLK	Any	2 V		46	125		190		155	ns
			4.5 V		15	25		38		31	
			6 V		12	21		32		26	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	33 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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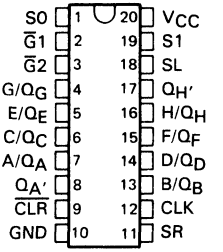
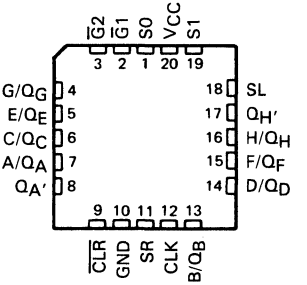
- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **High Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC299 . . . J PACKAGE
SN74HC299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC299 . . . FK PACKAGE
(TOP VIEW)



description

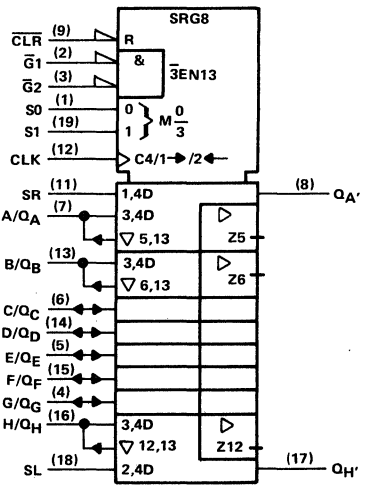
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit handling in a single 20-pin package. 'HC299 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but does not affect the shifting or storage of data.

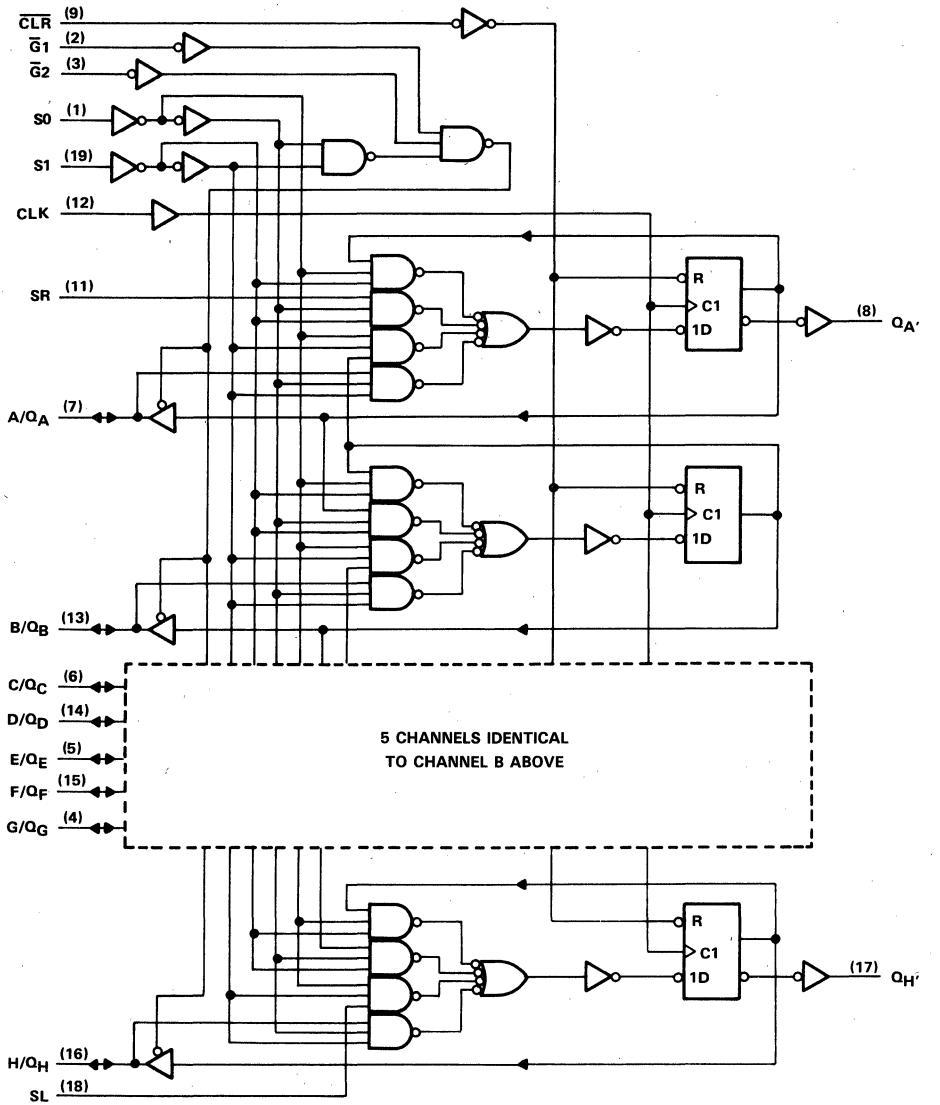
The SN54HC299 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC299 is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC299			SN74HC299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	Q_A, and Q_H, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		A/Q_n thru H/Q_n I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	Q_A, and Q_H, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		A/Q_n thru H/Q_n I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	Q_A, and Q_H, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		A/Q_n thru H/Q_n I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	Q_A, and Q_H I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		A/Q_n thru H/Q_H I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}†	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i‡			2 to 6 V		3	10		10		10	pF

†For I/O ports (Q_A through Q_H), the parameter I_I is included in the off-state output current.
‡This parameter, C_I, does not apply to transceiver I/O ports.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC299		SN74HC299		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high, CLK low, or $\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	S0 or S1	2 V	175		263		219		ns
			4.5 V	35		53		44		
			6 V	30		45		37		
		SL or SR	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		Data or $\overline{CLR}$ inactive	2 V	65		98		81		ns
			4.5 V	13		20		16		
			6 V	11		17		14		
t_h	Hold time after CLK↑	Select or data	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6			4.2		5		MHz
			4.5 V	31			21		25		
			6 V	36			25		29		
t_{pd}	CLK	$Q_{A'}$ or $Q_{H'}$	2 V		45	170		285		210	ns
			4.5 V		16	38		57		48	
			6 V		13	32		48		40	
		Q_A thru Q_H	2 V		42	170		285		210	ns
			4.5 V		16	38		57		48	
			6 V		12	32		48		40	
t_{en}	$\overline{G1}$ or $\overline{G2}$	Q_A thru Q_H	2 V		60	160		240		200	ns
			4.5 V		24	32		48		40	
			6 V		23	27		41		34	
	S0 or S1		2 V		115	300		450		375	ns
			4.5 V		44	60		90		75	
			6 V		39	51		77		64	
t_{dis}	$\overline{G1}$, or $\overline{G2}$	Q_A thru Q_H	2 V		60	160		240		200	ns
			4.5 V		24	32		48		40	
			6 V		23	27		41		34	
	S0 or S1		2 V		115	300		450		375	ns
			4.5 V		44	60		90		75	
			6 V		39	51		77		64	
t_{PHL}	$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$	2 V		41	210		315		250	ns
			4.5 V		17	42		63		53	
			6 V		13	36		54		45	
		Q_A thru Q_H	2 V		50	200		315		250	ns
			4.5 V		17	42		63		53	
			6 V		13	36		54		45	
t_t		$Q_{A'}$ or $Q_{H'}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		Q_A thru Q_H	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	100 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC299		SN74HC299		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Q_A thru Q_H	2 V		56	230		345		288	ns
			4.5 V		21	46		69		58	
			6 V		16	39		59		49	
t_{en}	$\overline{G}1$ or $\overline{G}2$	Q_A thru Q_H	2 V		94	220		330		275	ns
			4.5 V		38	44		66		55	
			6 V		33	37		56		47	
	S0 or S1		2 V		130	450		675		563	ns
			4.5 V		59	90		135		113	
			6 V		49	77		115		96	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H	2 V		63	260		390		325	ns
			4.5 V		21	52		78		65	
			6 V		17	44		66		55	
t_t		Q_A thru Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Inverting Versions of 'HC153**
- **High-Current Inverting Outputs Can Drive Up to 15 LSTTL Loads**
- **Permits Multiplexing from n Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Separate output enable inputs ($\overline{G}$) are provided for each of the two four-line sections of these data selectors/multiplexers.

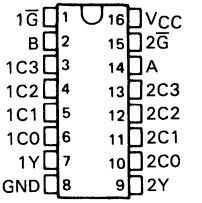
The SN54HC352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC352 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

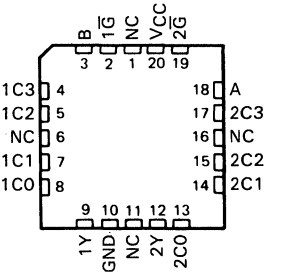
SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

SN54HC352 . . . J PACKAGE
SN74HC352 . . . DW OR N PACKAGE
(TOP VIEW)

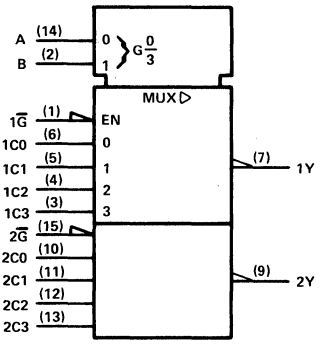


SN54HC352 . . . FK PACKAGE
(TOP VIEW)



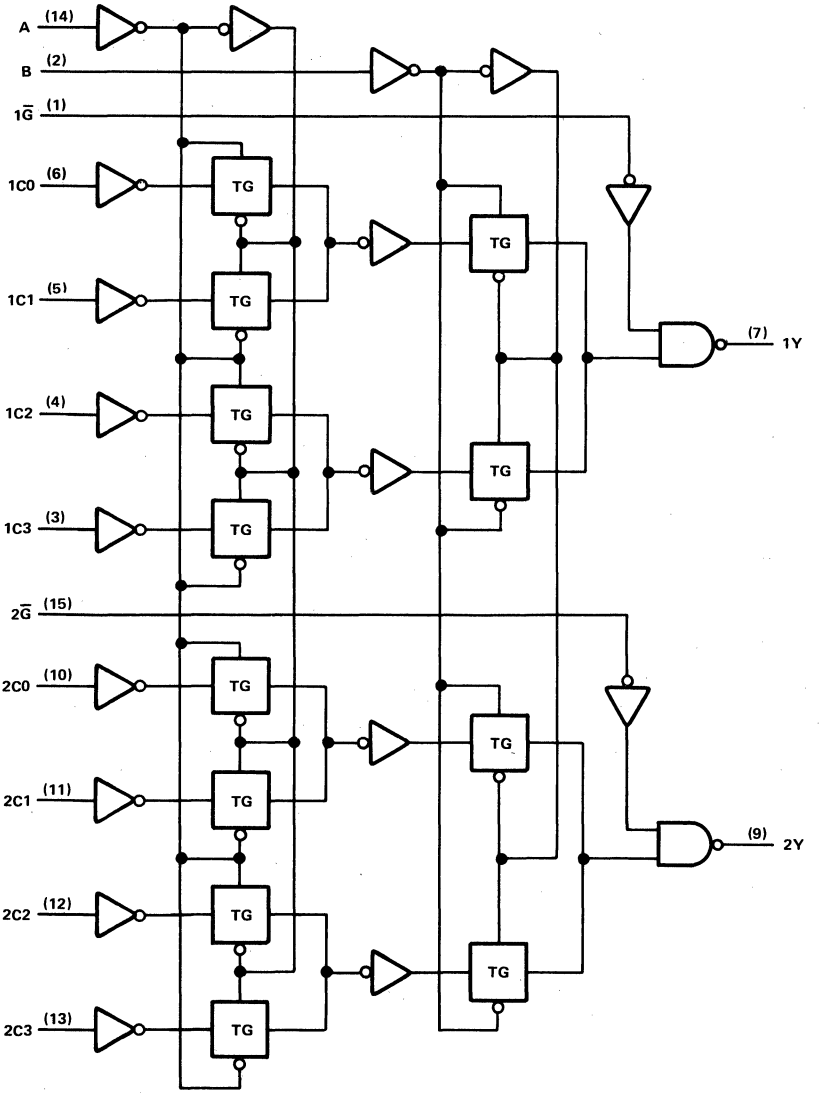
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC352			SN74HC352			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC352		SN74HC352		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, V_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	VI = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC352		SN74HC352		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		58	185		280		230	ns
			4.5 V		17	37		56		46	
			6 V		14	32		48		39	
t_{pd}	Data (Any C)	Y	2 V		47	175		265		220	ns
			4.5 V		14	35		53		44	
			6 V		12	30		45		37	
t_{pd}	$\overline{G}$	Y	2 V		27	135		205		170	ns
			4.5 V		10	27		41		34	
			6 V		8	23		35		29	
t_t		Y	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per data selector	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC352		SN74HC352		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		72	270		410		335	ns
			4.5 V		22	54		82		67	
			6 V		19	47		70		58	
t_{pd}	Data (Any C)	Y	2 V		62	260		395		325	ns
			4.5 V		19	52		79		63	
			6 V		16	45		67		56	
t_{pd}	$\overline{G}$	Y	2 V		43	220		335		275	ns
			4.5 V		14	44		67		55	
			6 V		12	38		57		48	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Inverting Versions of 'HC253**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Separate output enable inputs ($\overline{G}$) are provided for each of the two four-line sections of these data selectors/multiplexers.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enable output will drive the bus line to a high or low logic level. Each output has its own output enable ($\overline{G}$). The output is disabled when its output enable is high.

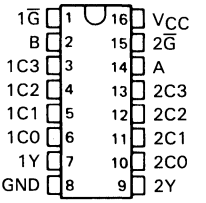
The SN54HC353 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC353 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

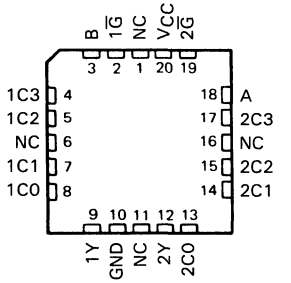
SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

SN54HC353 . . . J PACKAGE
SN74HC353 . . . DW OR N PACKAGE
(TOP VIEW)

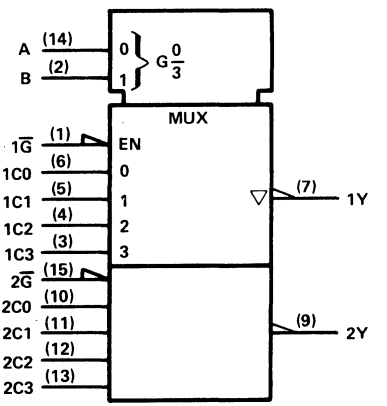


SN54HC353 . . . FK PACKAGE
(TOP VIEW)



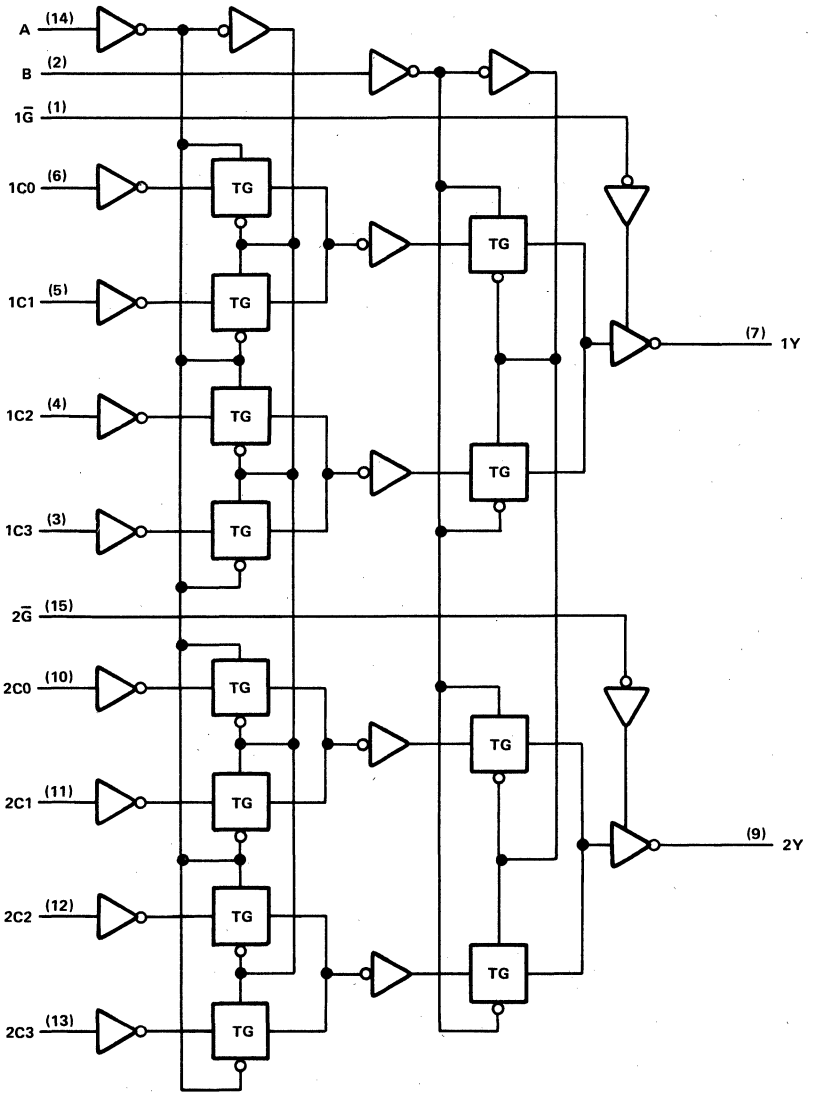
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC353			SN74HC353			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC353		SN74HC353		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, V_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC353		SN74HC353		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	185		280		230	ns
			4.5 V		17	37		56		46	
			6 V		14	32		48		39	
t_{pd}	Data (Any C)	Y	2 V		48	175		265		220	ns
			4.5 V		14	35		53		44	
			6 V		11	30		45		37	
t_{en}	$\overline{G}$	Y	2 V		37	135		205		170	ns
			4.5 V		11	27		41		34	
			6 V		9	23		35		29	
t_{dis}	$\overline{G}$	Y	2 V		22	135		205		170	ns
			4.5 V		13	27		41		34	
			6 V		11	23		35		29	
t_t		Any	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

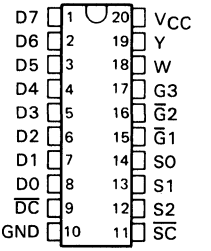
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC353		SN74HC353		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		75	270		410		335	ns
			4.5 V		21	54		82		67	
			6 V		18	47		70		58	
t_{pd}	Data (Any C)	Y	2 V		67	260		395		325	ns
			4.5 V		19	52		79		63	
			6 V		16	45		67		56	
t_{en}	$\overline{G}$	Y	2 V		54	220		335		275	ns
			4.5 V		16	44		67		55	
			6 V		14	38		57		48	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

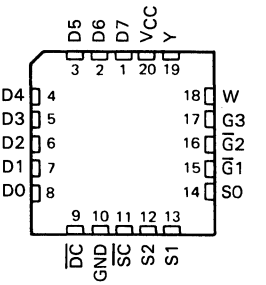
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Transparent Latches on Data Select Inputs**
- **Transparent Data Registers**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Complementary Outputs**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC354 . . . J PACKAGE
SN74HC354 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC354 . . . FK PACKAGE
(TOP VIEW)

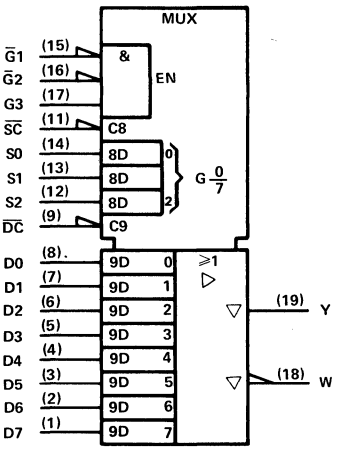


description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select is stored in transparent latches that are enabled by a low level on pin 11, $\overline{SC}$. A similar enable for data is obtained by a low level on pin 8, $\overline{DC}$.

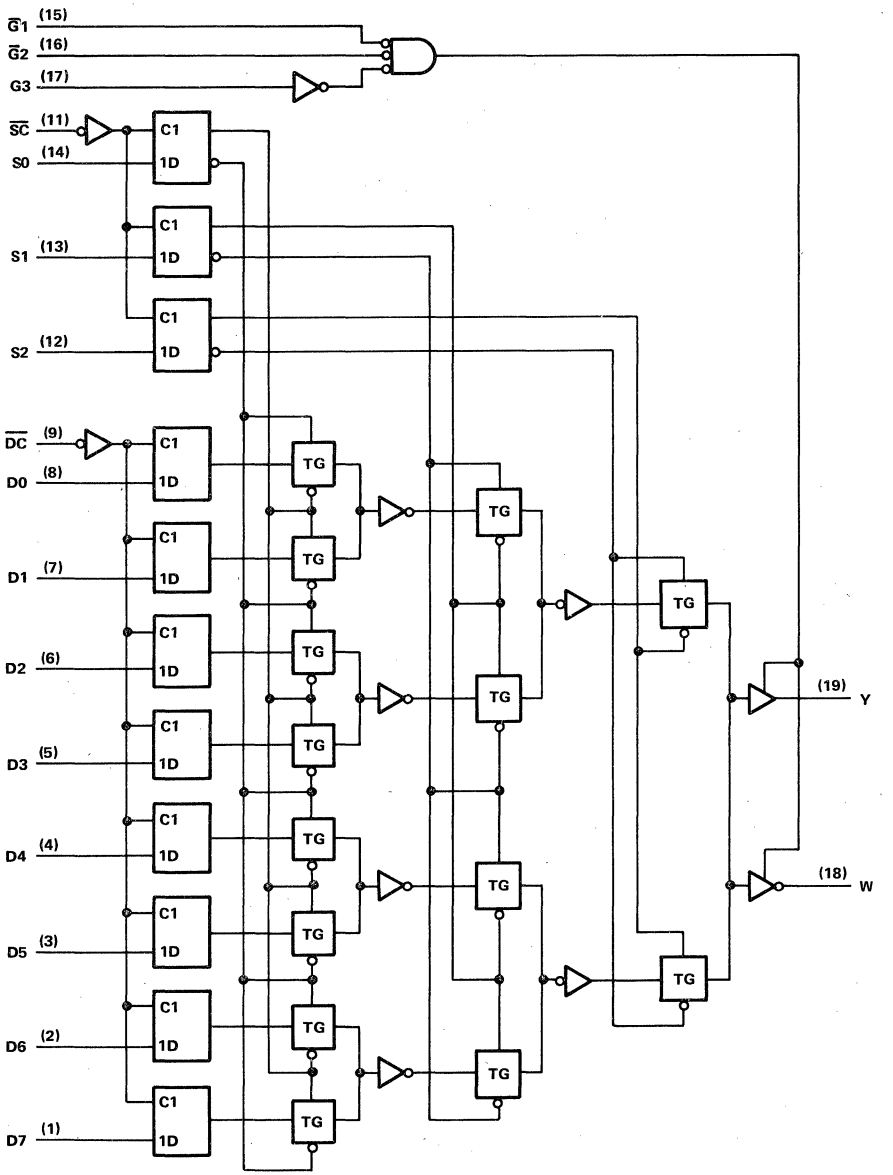
The SN54HC354 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC354 is characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUTS							OUTPUTS	
SELECT†			DATA CONTROL	OUTPUT ENABLES				
S2	S1	S0	$\overline{DC}$	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0 . . . D7 = the level of stead-state inputs at inputs D0 through D7, respectively
$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control
†This column shows the input address setup with $\overline{SC}$ low.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC354			SN74HC354			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC354		SN74HC354		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC354		SN74HC354		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration	$\overline{SC}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	$\overline{DC}$ low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su} Setup time	Data before $\overline{DC}\uparrow$	2 V	75		110		95		ns
		4.5 V	15		22		19		
		6 V	13		19		16		
	S0 thru S2 before $\overline{SC}\uparrow$	2 V	75		110		95		
		4.5 V	15		22		19		
		6 V	13		19		16		
t_h Hold time	Data after $\overline{DC}\uparrow$	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
	SO thru S2 after $\overline{SC}\uparrow$	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC354		SN74HC354		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any D	W or Y	2 V		90	235		352		295	ns
			4.5 V		29	47		71		59	
			6 V		25	40		60		50	
t_{pd}	$\overline{DC}$	W or Y	2 V		115	270		405		337	ns
			4.5 V		40	54		81		68	
			6 V		32	46		69		58	
t_{pd}	S0, S1, or S2	W or Y	2 V		120	285		427		355	ns
			4.5 V		42	57		86		71	
			6 V		34	48		72		60	
t_{pd}	$\overline{SC}$	W or Y	2 V		120	300		450		375	ns
			4.5 V		45	60		90		75	
			6 V		36	51		77		64	
t_{en}	$\overline{G1}$, $\overline{G2}$, or G3	W or Y	2 V		50	125		188		155	ns
			4.5 V		18	25		38		31	
			6 V		15	21		32		26	
t_{dis}	$\overline{G1}$, $\overline{G2}$, or G3	W or Y	2 V		68	165		248		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
t_t		W or Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	100 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

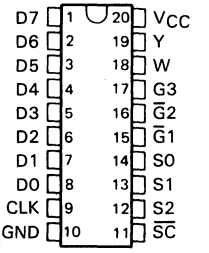
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC354		SN74HC354		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any D	W or Y	2 V		100	275		412		344	ns
			4.5 V		40	55		83		69	
			6 V		32	46		69		59	
t_{pd}	$\overline{DC}$	W or Y	2 V		125	310		465		387	ns
			4.5 V		46	62		93		78	
			6 V		38	52		78		66	
t_{pd}	S0, S1, or S2	W or Y	2 V		130	325		488		405	ns
			4.5 V		50	65		98		81	
			6 V		40	55		82		69	
t_{pd}	$\overline{SC}$	W or Y	2 V		110	340		510		425	ns
			4.5 V		52	68		102		85	
			6 V		42	58		87		72	
t_{en}	$\overline{G}1$, $\overline{G}2$, or G3	W or Y	2 V		60	165		248		205	ns
			4.5 V		25	33		50		41	
			6 V		21	28		42		35	
t_t		W or Y	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

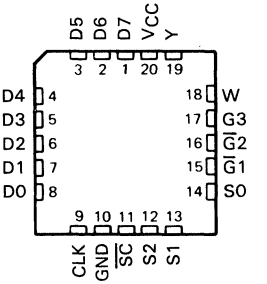
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

- **Transparent Latches on Data Select Inputs**
- **Edge-Triggered Data Registers**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Complementary Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC356 . . . J PACKAGE
SN74HC356 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC356 . . . FK PACKAGE
(TOP VIEW)

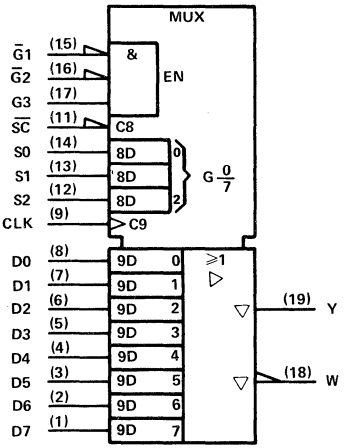


description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select address is stored in transparent latches that are enabled by a low level in pin 11, $\overline{SC}$. The edge-triggered data registers are clocked by a low-to-high transition on pin 9, CLK. Both true and complementary outputs are available.

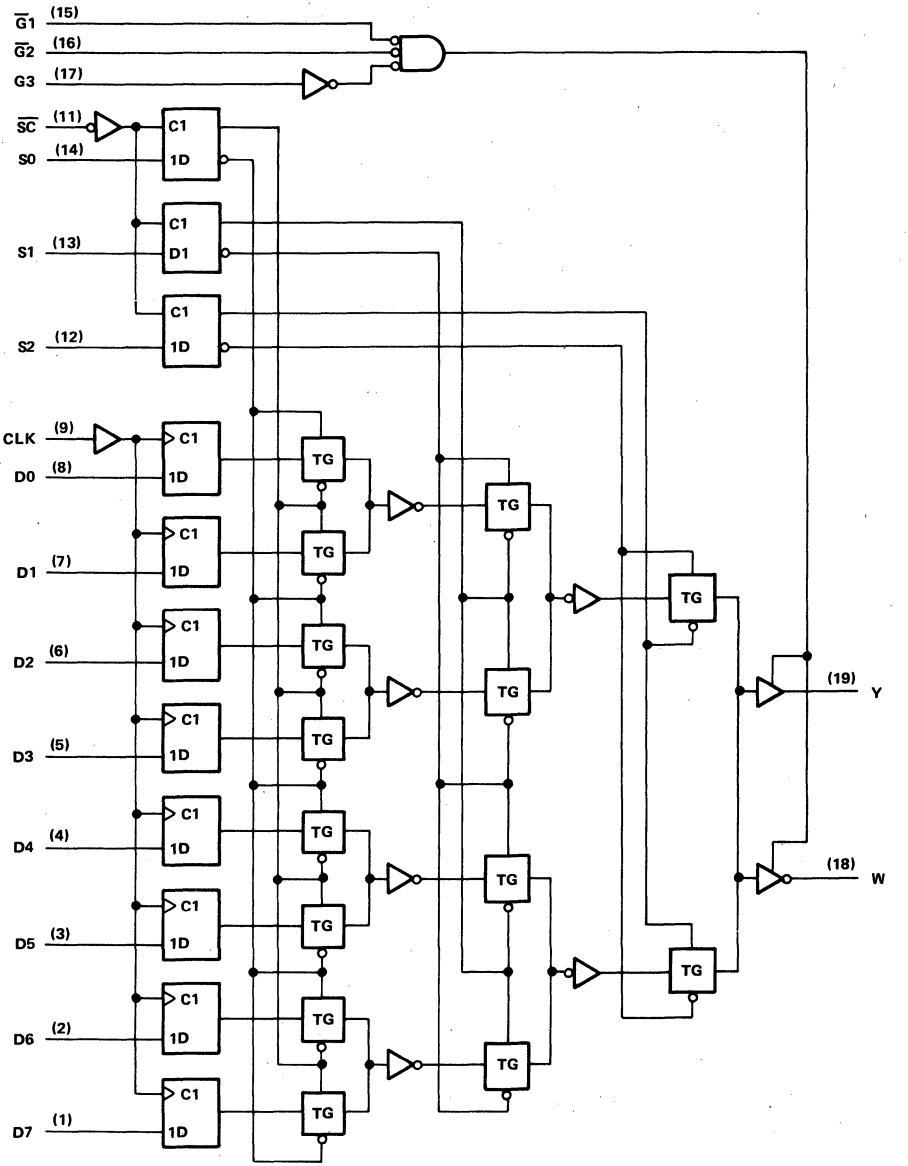
The SN54HC356 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC356 is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUTS							OUTPUTS	
SELECT†			CLOCK	OUTPUT ENABLES				
S2	S1	S0		$\overline{G}1$	$\overline{G}2$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D}0$	D0
L	L	L	H or L	L	L	H	$\overline{D}0_n$	$D0_n$
L	L	H	↑	L	L	H	$\overline{D}1$	D1
L	L	H	H or L	L	L	H	$\overline{D}1_n$	$D1_n$
L	H	L	↑	L	L	H	$\overline{D}2$	D2
L	H	L	H or L	L	L	H	$\overline{D}2_n$	$D2_n$
L	H	H	↑	L	L	H	$\overline{D}3$	D3
L	H	H	H or L	L	L	H	$\overline{D}3_n$	$D3_n$
H	L	L	↑	L	L	H	$\overline{D}4$	D4
H	L	L	H or L	L	L	H	$\overline{D}4_n$	$D4_n$
H	L	H	↑	L	L	H	$\overline{D}5$	D5
H	L	H	H or L	L	L	H	$\overline{D}5_n$	$D5_n$
H	H	L	↑	L	L	H	$\overline{D}6$	D6
H	H	L	H or L	L	L	H	$\overline{D}6_n$	$D6_n$
H	H	H	↑	L	L	H	$\overline{D}7$	D7
H	H	H	H or L	L	L	H	$\overline{D}7_n$	$D7_n$

†This column shows the input address setup with $\overline{SC}$ low.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC356			SN74HC356			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C		SN54HC356		SN74HC356		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998	1.9		1.9		V
		4.5 V	4.4	4.499	4.4		4.4		
		6 V	5.9	5.999	5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30	3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80	5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		V
		4.5 V		0.001	0.1		0.1		
		6 V		0.001	0.1		0.1		
	V_I = V_{IH} or V_{IL}, V_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC356		SN74HC356		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	33	0	25	0	28	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	15		20		18		
		$\overline{SC}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	15		20		18		
t_{su}	Setup time	Data before CLK↑	2 V	75		115		95		ns
			4.5 V	15		23		19		
			6 V	13		20		16		
		Select before $\overline{SC}$↑	2 V	75		115		95		
			4.5 V	15		23		19		
			6 V	13		20		16		
t_h	Hold time	Data after CLK↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		Select after $\overline{SC}$↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC356		SN74HC356		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLK		2 V	6			4.2		5		MHz
			4.5 V	31			21		25		
			6 V	33			25		28		
t_{pd}	CLK	W or Y	2 V		100	225		338		318	ns
			4.5 V		36	51		77		64	
			6 V		28	43		64		53	
t_{pd}	S0, S1 or S2	W or Y	2 V		120	285		427		355	ns
			4.5 V		42	57		86		71	
			6 V		34	48		72		60	
t_{pd}	$\overline{SC}$	W or Y	2 V		120	300		450		375	ns
			4.5 V		45	60		90		75	
			6 V		36	51		77		64	
t_{en}	$\overline{G}1$, $\overline{G}2$, or G3	W or Y	2 V		50	125		188		155	ns
			4.5 V		18	25		38		31	
			6 V		15	21		32		26	
t_{dis}	$\overline{G}1$, $\overline{G}2$, or G3	W or Y	2 V		68	165		248		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		42		35	
t_t		W or Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	100 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC356		SN74HC356		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	W or Y	2 V		110	295		442		365	ns
			4.5 V		42	59		89		73	
			6 V		34	50		75		62	
t_{pd}	S0, S1, S2	W or Y	2 V		130	325		485		405	ns
			4.5 V		50	65		97		81	
			6 V		40	55		82		69	
t_{pd}	$\overline{SC}$	W or Y	2 V		110	340		510		425	ns
			4.5 V		52	68		102		85	
			6 V		42	58		87		72	
t_{en}	$\overline{G}1$, $\overline{G}2$, or G3	W or Y	2 V		60	165		248		205	ns
			4.5 V		25	33		50		41	
			6 V		21	28		42		35	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or Up to 15 LSTTL Loads**
- **Choice of True or Inverting Outputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

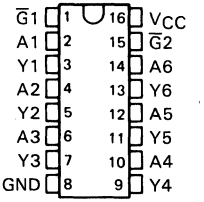
'HC365, HC367	**True Outputs**
'HC366, HC368	**Inverting Outputs**

description

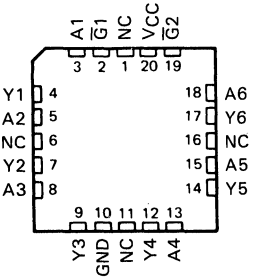
These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G (active-low control) inputs.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.

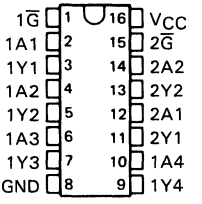
SN54HC365, SN54HC366 . . . J PACKAGE
SN74HC365, SN74HC366 . . . DW OR N PACKAGE
(TOP VIEW)



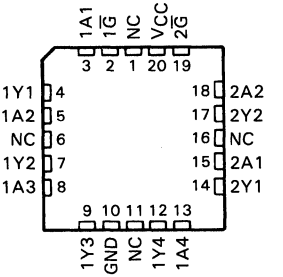
SN54HC365, SN54HC366 . . . FK PACKAGE
(TOP VIEW)



SN54HC367, SN54HC368 . . . J PACKAGE
SN74HC367, SN74HC368 . . . DW OR N PACKAGE
(TOP VIEW)



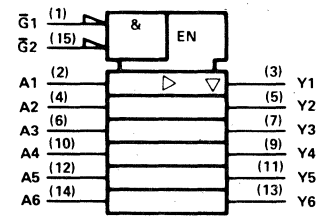
SN54HC367, SN54HC368 . . . FK PACKAGE
(TOP VIEW)



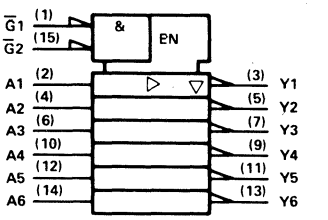
NC—No internal connection

logic symbols†

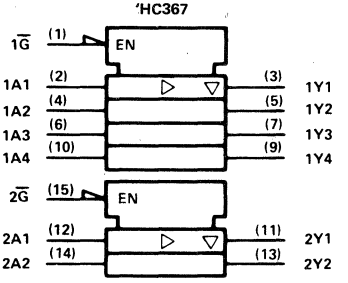
'HC365



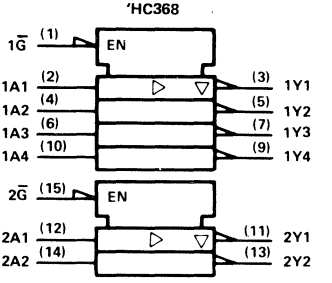
'HC366



'HC367

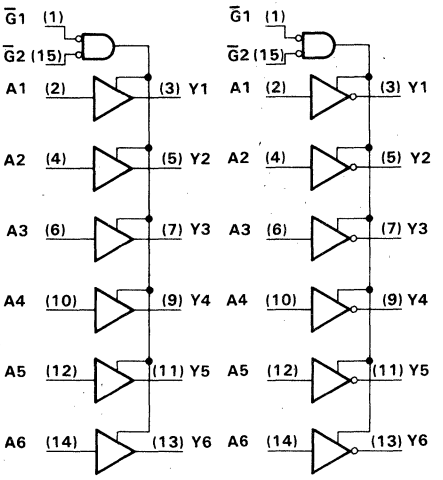


'HC368

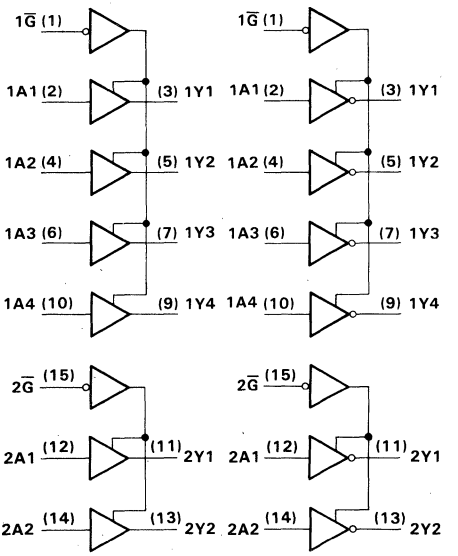


logic diagrams (positive logic)

'HC365 'HC366



'HC367 'HC368



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC365 thru SN54HC368			SN74HC365 thru SN74HC368			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC365 thru SN54HC368		SN74HC365 thru SN74HC368		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC'		SN74HC'		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	95		145		120	ns
			4.5 V		12	19		29		24	
			6 V		10	16		25		20	
t_{en}	$\overline{G}$	Y	2 V		100	190		285		238	ns
			4.5 V		26	38		57		48	
			6 V		21	32		48		41	
t_{dis}	$\overline{G}$	Y	2 V		50	175		265		240	ns
			4.5 V		21	35		53		48	
			6 V		19	30		45		41	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per driver	No load, T_A = 25°C	35 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC'		SN74HC'		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		70	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	20		31		25	
t_{en}	$\overline{G}$	Y	2 V		140	230		345		285	ns
			4.5 V		30	46		69		57	
			6 V		28	39		59		48	
t_t			2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **8 High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

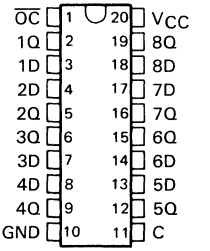
The eight latches of the 'HC373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

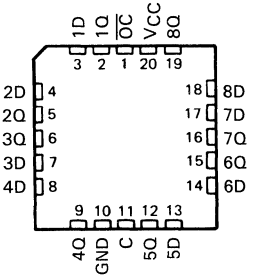
The output control ($\overline{OC}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC373 is characterized for operation from −40°C to 85°C.

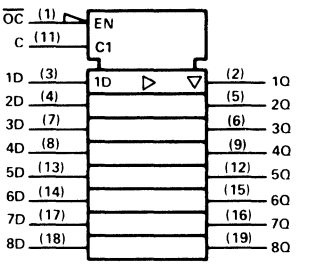
SN54HC373 . . . J PACKAGE
SN74HC373 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC373 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



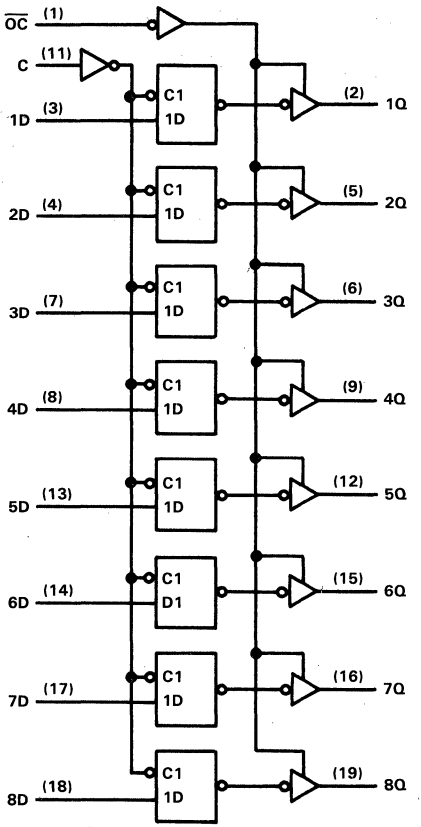
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, Z = low level, X = irrelevant

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC373			SN74HC373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 μA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 μA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 μA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 μA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC373		SN74HC373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before enable C↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after enable C↓	2 V	20		26		24		ns
		4.5 V	10		13		12		
		6 V	10		13		12		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		58	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	C	Any Q	2 V		73	175		265		220	ns
			4.5 V		18	35		53		44	
			6 V		15	30		45		38	
t_{en}	$\overline{OC}$	Any Q	2 V		65	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		38		32	
t_{dis}	$\overline{OC}$	Any Q	2 V		50	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	100 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

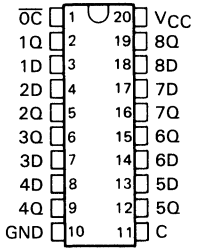
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		82	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{pd}	C	Any Q	2 V		100	225		335		285	ns
			4.5 V		24	45		67		57	
			6 V		20	38		57		48	
t_{en}	$\overline{OC}$	Any Q	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Any Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

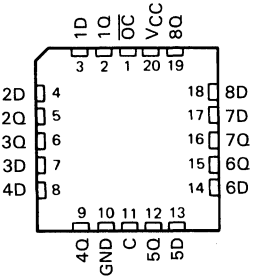
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **8 High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT373 . . . J PACKAGE
SN74HCT373 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT373 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HCT373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

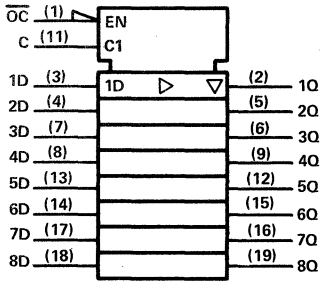
The output control ($\overline{OC}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HCT373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (EACH LATCH)

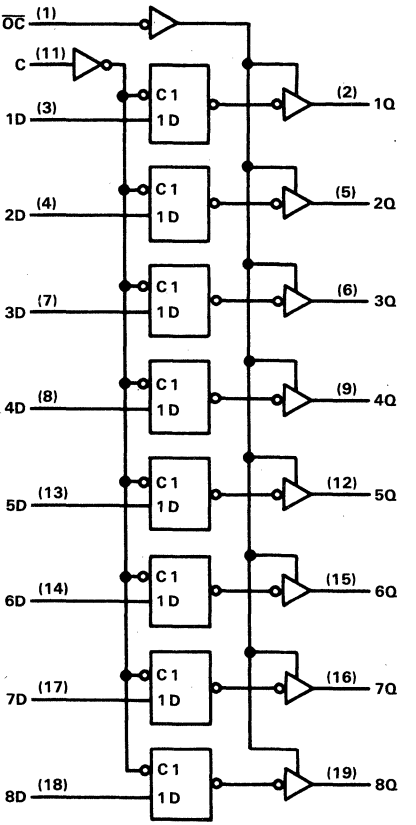
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT373			SN74HCT373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 V to 5.5 V		3	10		10		10	pF

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	4.5 V	20			30		25		ns
		5.5 V	17			27		23		
t_{su}	Setup time, data before enable C↓	4.5 V	10			15		13		ns
		5.5 V	9			14		12		
t_h	Hold time, data after enable C↓	4.5 V	10			10		10		ns
		5.5 V	10			10		10		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		25	35		53		44	ns
			5.5 V		21	32		48		40	
t_{pd}	C	Any Q	4.5 V		28	35		53		44	ns
			5.5 V		25	32		48		40	
t_{en}	$\overline{OC}$	Any Q	4.5 V		26	35		53		44	ns
			5.5 V		23	32		48		40	
t_{dis}	$\overline{OC}$	Any Q	4.5 V		23	35		53		44	ns
			5.5 V		22	32		48		40	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		32	52		79		65	ns
			5.5 V		27	47		71		59	
t_{pd}	C	Any Q	4.5 V		38	52		79		65	ns
			5.5 V		36	47		71		59	
t_{en}	$\overline{OC}$	Any Q	4.5 V		33	52		79		65	ns
			5.5 V		28	47		71		59	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **8 D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

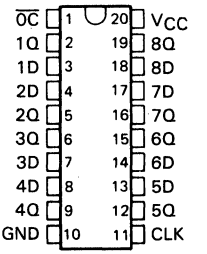
The eight flip-flops of the 'HC374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

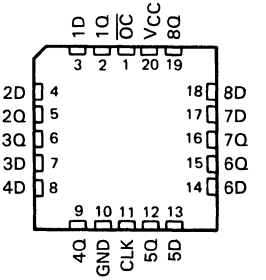
The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC374 is characterized for operation from −40°C to 85°C.

SN54HC374 . . . J PACKAGE
SN74HC374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)

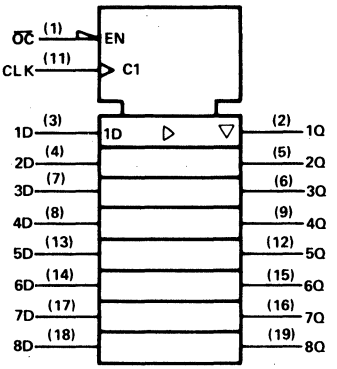


FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

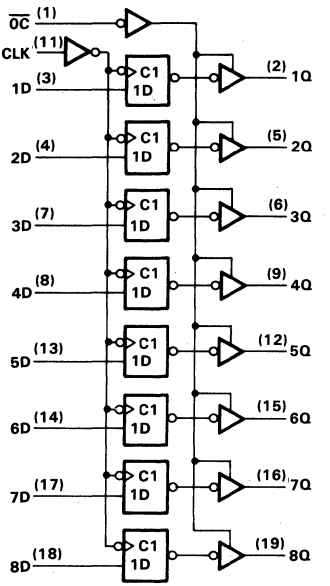
H = high level, L = low level. X = irrelevant.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC374			SN74HC374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0		6	0	4	0	5	MHz
			4.5 V	0		30	0	20	0	24	
			6 V	0		35	0	24	0	28	
t_w	Pulse duration	CLK high or low	2 V	80			120		100		ns
			4.5 V	16			24		20		
			6 V	14			20		17		
t_{su}	Setup time, data before CLK↑		2 V	100			150		125		ns
			4.5 V	20			30		25		
			6 V	17			25		21		
t_h	Hold time, data after CLK↑		2 V	10			13		12		ns
			4.5 V	5			5		5		
			6 V	5			5		5		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4		5		MHz
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t_{pd}	CLK	Any Q	2 V		63	180		270		225	ns
			4.5 V		17	36		54		45	
			6 V		15	31		46		38	
t_{en}	$\overline{OC}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		14	26		38		32	
t_{dis}	$\overline{OC}$	Any Q	2 V		36	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		16	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	100 pF typ

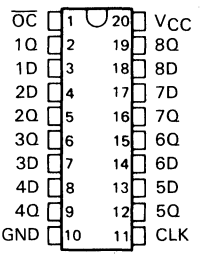
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4		5		MHz
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t_{pd}	CLK	Any Q	2 V		80	230		345		290	ns
			4.5 V		22	46		69		58	
			6 V		19	39		58		49	
t_{en}	$\overline{OC}$	Any Q	2 V		70	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		22	34		51		43	
t_t		Any Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

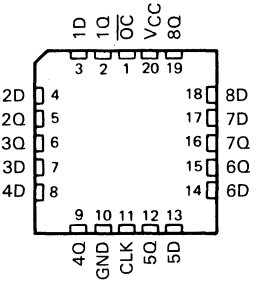
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **8 D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive Up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT374 . . . J PACKAGE
SN74HCT374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

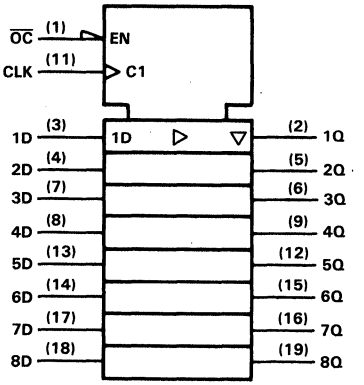
The SN54HCT374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT374 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

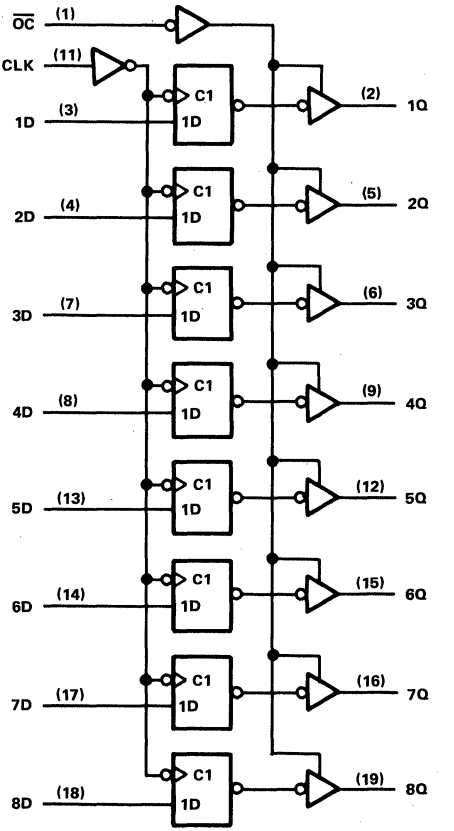
H = high level, L = low level, X = irrelevant

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT374			SN74HCT374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 V to 5.5 V		3	10		10		10	pF

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0		31	0	21	0	25	MHz
		5.5 V	0		36	0	23	0	28	
t_w	Pulse duration, CLK high or low	4.5 V	16			24		20		ns
		5.5 V	14			22		18		
t_{su}	Setup time, data before CLK↑	4.5 V	20			30		25		ns
		5.5 V	17			27		23		
t_h	Hold time, data after CLK↑	4.5 V	10			10		10		ns
		5.5 V	10			10		10		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	36		21		25		MHz
			5.5 V	36	40		23		28		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		49		41	
t_{en}	$\overline{OC}$	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	$\overline{OC}$	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	85 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any Q	4.5 V		40	46		69		58	ns
			5.5 V		35	41		62		52	
t_{en}	$\overline{OC}$	Any Q	4.5 V		34	40		60		50	ns
			5.5 V		29	36		54		45	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Th SN54HC375 and SN74HC375 bistable latches are electrically and functionally identical to the SN54HC75 and SN74HC75, respectively. Only the arrangement of the terminals has been changed in the SN54HC375 and SN74HC375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

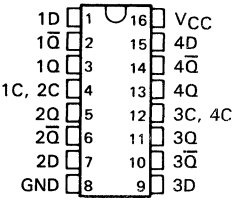
The SN54HC375 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC375 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH LATCH)

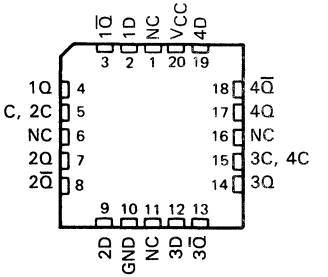
INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level. X = irrelevant.

SN54HC375 . . . J PACKAGE
SN74HC375 . . . D OR N PACKAGE
(TOP VIEW)

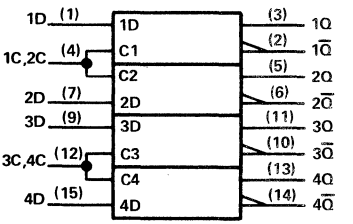


SN54HC375 . . . FK PACKAGE
(TOP VIEW)



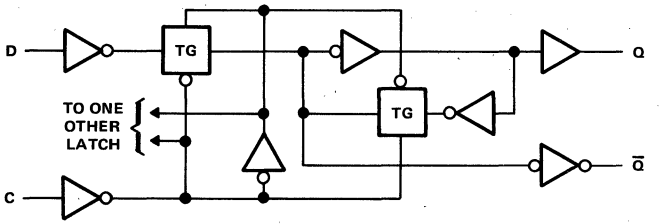
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC375			SN74HC375			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC375		SN74HC375		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC375		SN74HC375		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before C↓	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC375		SN74HC375		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q or $\overline{Q}$	2 V		40	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{pd}	C	Q or $\overline{Q}$	2 V		42	130		195		165	ns
			4.5 V		15	26		39		33	
			6 V		12	22		33		28	
t_t		Any Q or $\overline{Q}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			2 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	48 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **'HC377 and 'HC378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs**
- **'HC379 Contains Four Flip-Flops with Double-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

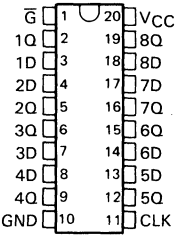
description

These circuits are positive-edge-triggered D-type flip-flops with an enable input. The 'HC377, 'HC378, and 'HC379 devices are similar to 'HC273, 'HC174, and 'HC175 respectively, but feature a latched clock enable ($\overline{G}$) instead of a common clear.

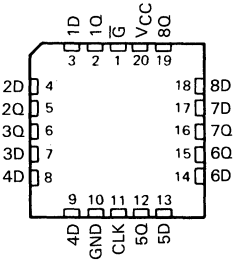
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

The SN54HC377, SN54HC378, and SN54HC379 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC377, SN74HC378, and SN74HC379 are characterized for operation from −40°C to 85°C.

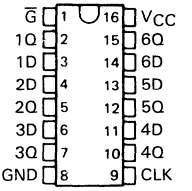
SN54HC377 . . . J PACKAGE
SN74HC377 . . . DW OR N PACKAGE
(TOP VIEW)



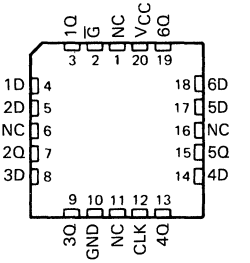
SN54HC377 . . . FK PACKAGE
(TOP VIEW)



SN54HC378 . . . J PACKAGE
SN74HC378 . . . D OR N PACKAGE
(TOP VIEW)

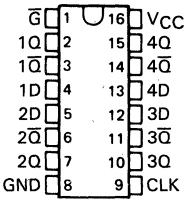


SN54HC378 . . . FK PACKAGE
(TOP VIEW)

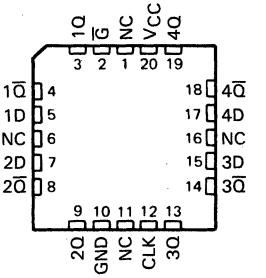


NC—No internal connection

SN54HC379 . . . J PACKAGE
SN74HC379 . . . D, J, OR N PACKAGE
(TOP VIEW)

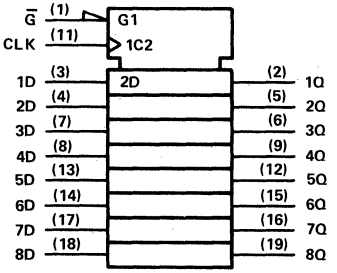


SN54HC379 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

'HC377 logic symbol†



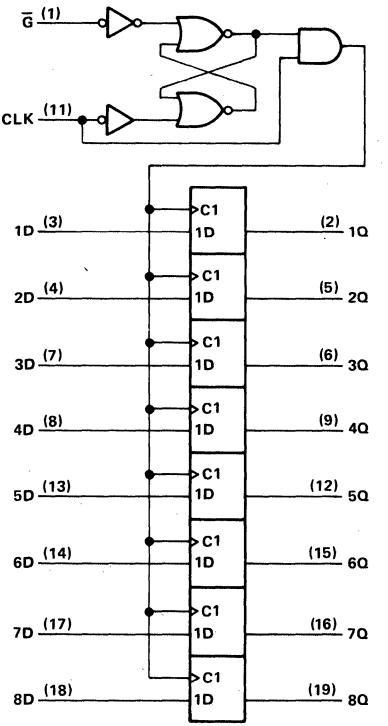
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

H = high level, L = low level, X = irrelevant

'HC377 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

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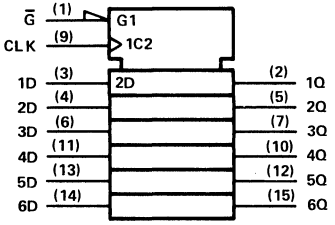
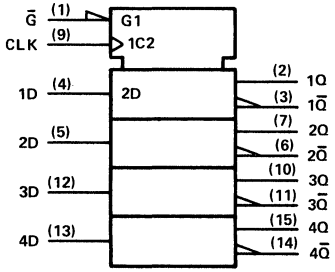
'HC378 logic symbol†



FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

'HC379 logic symbol†



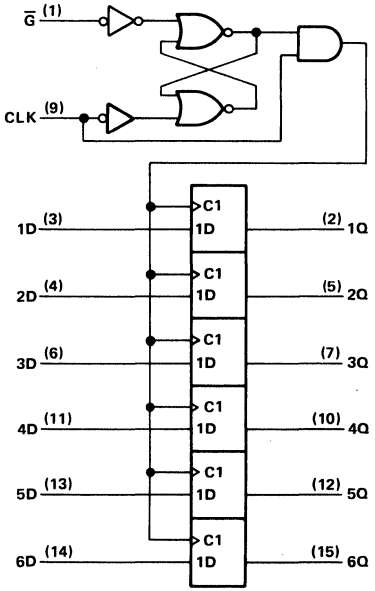
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

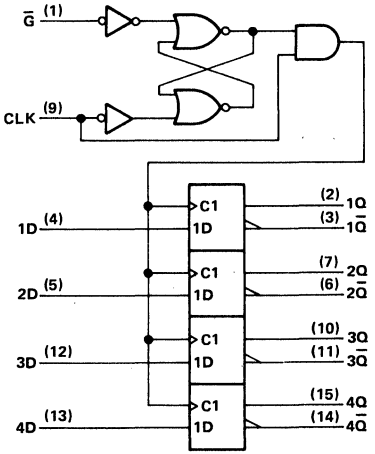
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for D, J, and N packages.

'HC378 logic diagram (positive logic)



'HC379 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D, DW, or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC377 SN54HC378 SN54HC379			SN74HC377 SN74HC378 SN74HC379			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3	0	4	MHz
			4.5 V	0	25	0	16	0	20	
			6 V	0	29	0	19	0	23	
t_w	Pulse duration, CLK high or low		2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Set up time before CLK↑	D	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{G}$ high or low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time $\overline{G}$ inactive after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	11		3		4		MHz
			4.5 V	25	54		16		20		
			6 V	29	64		19		23		
t_{pd}	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	30 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

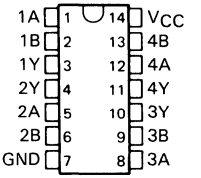
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

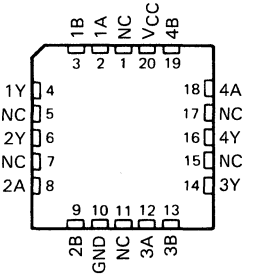
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC386 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC386 is characterized for operation from −40°C to 85°C.

SN54HC386 . . . J PACKAGE
SN74HC386 . . . D OR N PACKAGE
(TOP VIEW)

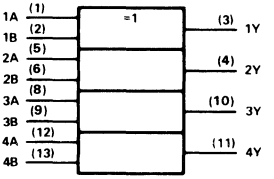


SN54HC386 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC386			SN74HC386			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC386		SN74HC386		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC386		SN74HC386		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	35 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

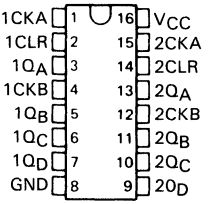
- **'HC390...Individual Clock for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters**
- **'HC393...Dual 4-Bit Binary Counter with Individual Clocks**
- **All Have Direct Clear for Each 4-Bit Counter**
- **Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

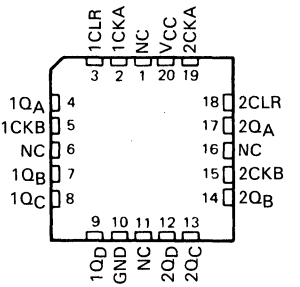
Each of these monolithic circuits contains eight flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'HC390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'HC393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'HC390 and 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

The SN54HC390 and SN54HC393 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC390 and SN74HC393 are characterized for operation from −40°C to 85°C.

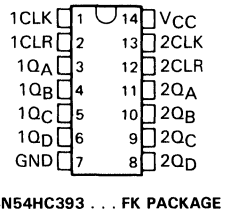
SN54HC390 . . . J PACKAGE
SN74HC390 . . . DW OR N PACKAGE
(TOP VIEW)



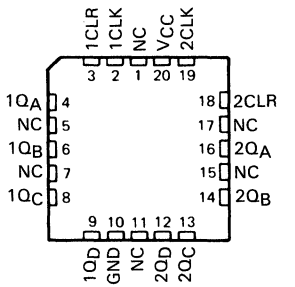
SN54HC390 . . . FK PACKAGE
(TOP VIEW)



SN54HC393 . . . J PACKAGE
SN74HC393 . . . N PACKAGE
(TOP VIEW)

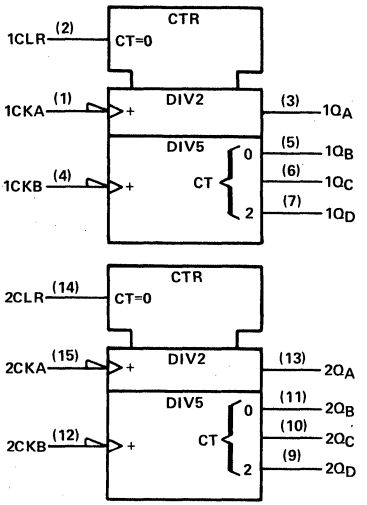


SN54HC393 . . . FK PACKAGE
(TOP VIEW)



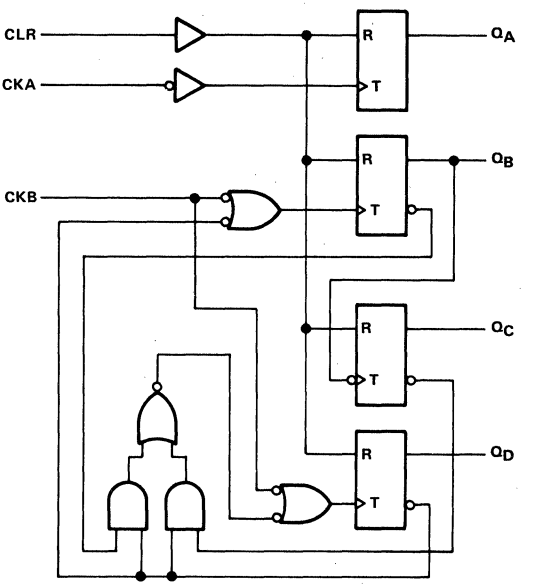
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram, each counter (positive logic)



FUNCTION TABLES

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BIQUINARY (5-2) (EACH COUNTER) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for biquinary count.
H = high level, L = low level.

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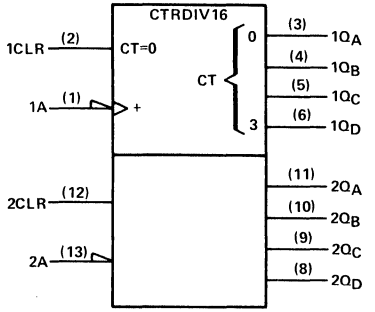
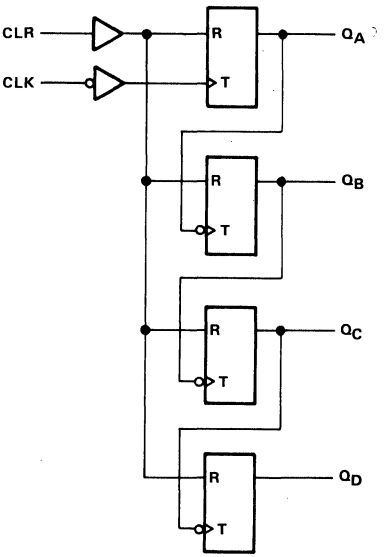
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

logic diagram, each counter (positive logic)



FUNCTION TABLE
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC390 SN54HC393			SN74HC390 SN74HC393			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC390 SN54HC393		SN74HC390 SN74HC393		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC390		SN74HC390		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CKA	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	20	0	25	
			6 V	0	36	0	25	0	28	
		CKB	2 V	0	6	0	4.2	0	5	
			4.5 V	0	31	0	20	0	25	
			6 V	0	36	0	25	0	28	
t_w	Pulse duration	CKA high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		18		
		CKB high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6V	14		20		18		
t_{su}	Setup time, CLR inactive		2 V	25		25		25		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC390		SN74HC390		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CKA	Q_A	2 V	6	10		4.2		5		MHz
			4.5 V	31	50		20		25		
			6 V	36	60		25		28		
	CKB	Q_B	2 V	6	10		4.2		5		
			4.5 V	31	50		20		25		
			6 V	36	60		25		28		
t_{pd}	CKA	Q_A	2 V		50	120		180		150	ns
			4.5 V		16	24		35		35	
			6 V		13	20		31		26	
t_{pd}	CKA	Q_C	2 V		100	290		430		365	ns
			4.5 V		35	58		87		72	
			6 V		30	50		74		62	
t_{pd}	CKB	Q_B	2 V		58	130		195		165	ns
			4.5 V		18	26		39		33	
			6V		15	22		33		28	
t_{pd}	CKB	Q_C	2 V		83	185		280		230	ns
			4.5 V		26	37		55		46	
			6V		21	32		48		40	
t_{pd}	CKB	Q_D	2 V		60	130		195		160	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_{PHL}	CLR	Any	2 V		45	165		250		205	ns
			4.5 V		17	33		49		41	
			6V		14	28		42		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC393		SN74HC393		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLK	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	28	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		18		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
t_{su}	Setup time, CLR inactive		2 V	25		25		25		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLK	Q_A	2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		28		
t_{pd}	CLK	Q_A	2 V		50	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		13	20		31		26	
t_{pd}	CLK	Q_B	2 V		72	190		285		240	ns
			4.5 V		22	38		57		47	
			6 V		18	32		48		40	
t_{pd}	CLK	Q_C	2 V		91	240		360		300	ns
			4.5 V		28	48		72		60	
			6 V		22	41		61		51	
t_{pd}	CLK	Q_D	2 V		100	290		430		360	ns
			4.5 V		32	58		87		72	
			6 V		24	50		74		62	
t_{PHL}	CLR	Any	2 V		45	165		250		205	ns
			4.5 V		17	33		49		41	
			6 V		14	28		42		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter**
- **Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single 'HC490. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

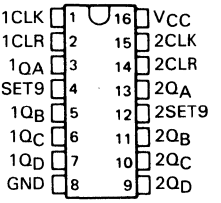
The SN54HC490 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC490 is characterized for operation from −40°C to 85°C.

CLEAR/SET-TO-9 FUNCTION TABLE (EACH COUNTER)

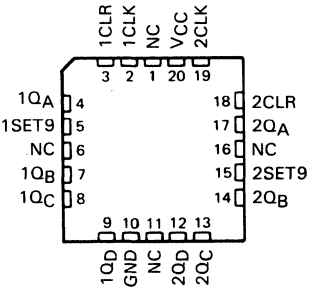
INPUTS		OUTPUT			
CLEAR	SET-TO-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

H = high level, L = low level.

SN54HC490 . . . J PACKAGE
SN74HC490 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC490 . . . FK PACKAGE
(TOP VIEW)

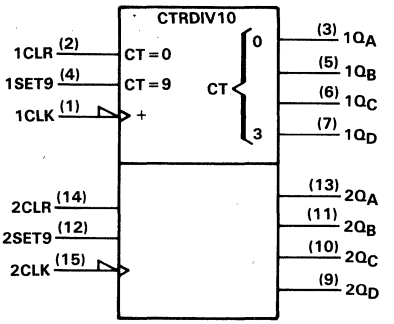


NC—No internal connection

BCD COUNT SEQUENCE (EACH COUNTER)

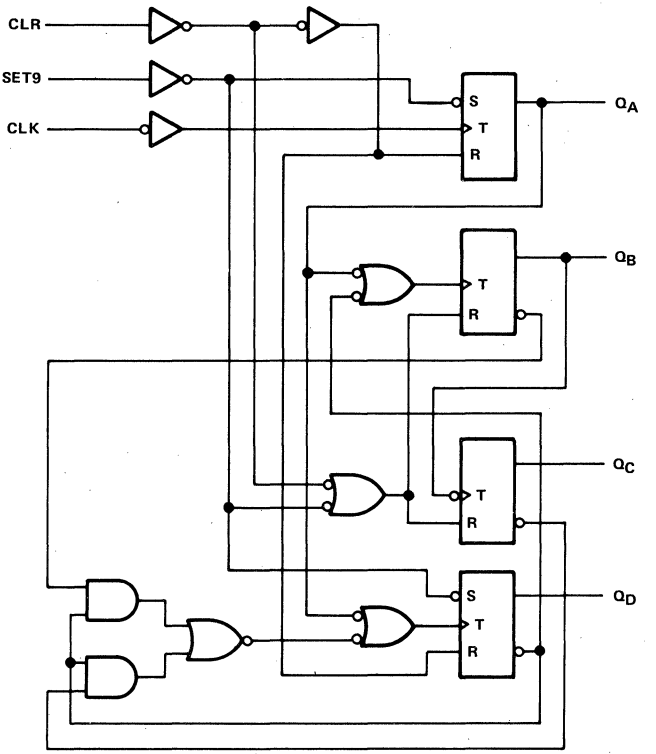
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram, each counter (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC490			SN74HC490			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC490		SN74HC490		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC490		SN74HC490		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	28	
t_w	Pulse duration, any input	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, CLR or set-to-9 inactive	2 V	25		25		25		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC490		SN74HC490		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6			4.2		5		MHz
			4.5 V	31			21		25		
			6 V	36			25		28		
t_{pd}	CLK	Q_A	2 V		50	125		190		155	ns
			4.5 V		15	25		38		31	
			6 V		12	21		32		26	
	CLK	Q_B, Q_D	2 V		80	185		280		230	
			4.5 V		23	37		56		46	
			6 V		18	31		48		39	
	CLK	Q_C	2 V		100	235		355		295	
			4.5 V		30	47		71		59	
			6 V		23	40		60		50	
t_{PLH}	Set-to-9	Q_A, Q_D	2 V		60	185		280		230	ns
			4.5 V		19	37		56		46	
			6V		16	31		48		39	
t_{PHL}	Set-to-9	Q_B, Q_C	2 V		54	140		210		175	
			4.5 V		18	28		42		35	
			6V		16	24		36		30	
	Clear	Any	2 V		50	130		195		165	
			4.5 V		17	26		39		33	
			6V		15	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **8 Latches in a Single Package**
- **High-Current 3-State Inverting Outputs Can Drive Up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

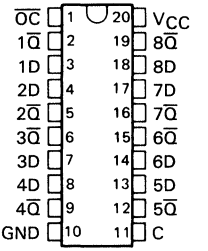
The eight latches of the 'HC533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'HC533 is functionally equivalent to the 'HC373 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

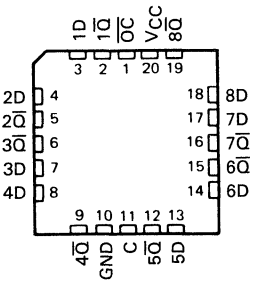
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC533 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC533 is characterized for operation from −40°C to 85°C.

SN54HC533 . . . J PACKAGE
SN74HC533 . . . DW OR N PACKAGE
(TOP VIEW)



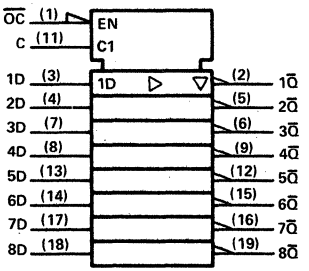
SN54HC533 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH LATCH)

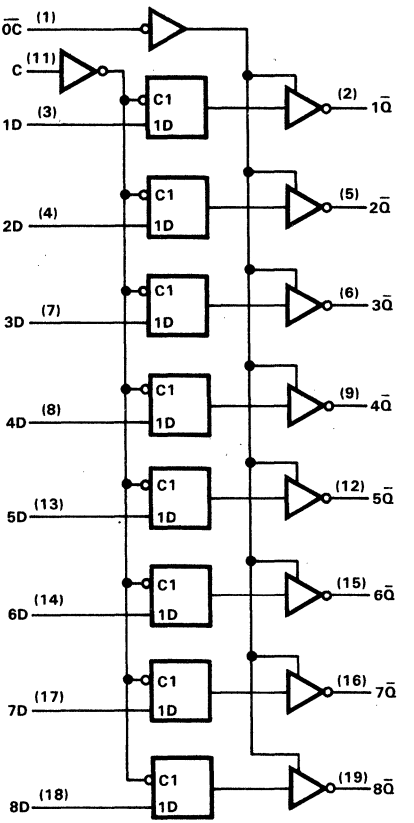
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC533			SN74HC533			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC533		SN74HC533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC533		SN74HC533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before enable C↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after enable C↓	2 V	20		26		24		ns
		4.5 V	10		13		12		
		6 V	10		13		12		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC533		SN74HC533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		77	150		225		185	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t_{pd}	C	Any $\overline{Q}$	2 V		87	175		265		220	ns
			4.5 V		27	35		53		44	
			6 V		23	30		45		38	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		68	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	2 V		47	150		225		190	
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6V		6	10		15		13	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC533		SN74HC533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
t_{pd}	C	Any $\overline{Q}$	2 V		103	225		335		280	ns
			4.5 V		33	45		67		56	
			6 V		29	38		57		48	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		28	34		51		43	
t_t		Any $\overline{Q}$	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	38		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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- Inputs are TTL-Voltage Compatible
- 8 Latches in a Single Package
- High-Current 3-State Inverting Outputs Can Drive Up to 15 LSTTL Loads
- Full Parallel Access for Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

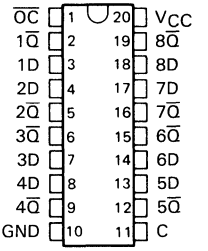
The eight latches of the 'HCT533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'HCT533 is functionally equivalent to the 'HCT373 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

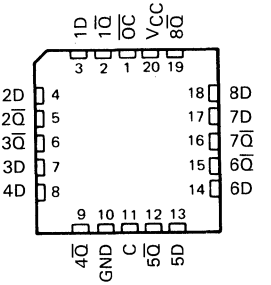
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HCT533 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT533 is characterized for operation from −40°C to 85°C.

SN54HCT533 . . . J PACKAGE
SN74HCT533 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT533 . . . FK PACKAGE
(TOP VIEW)

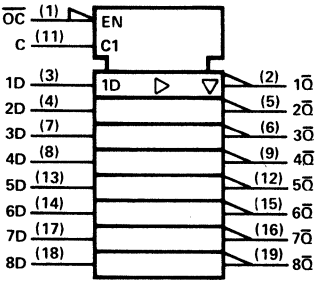


FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

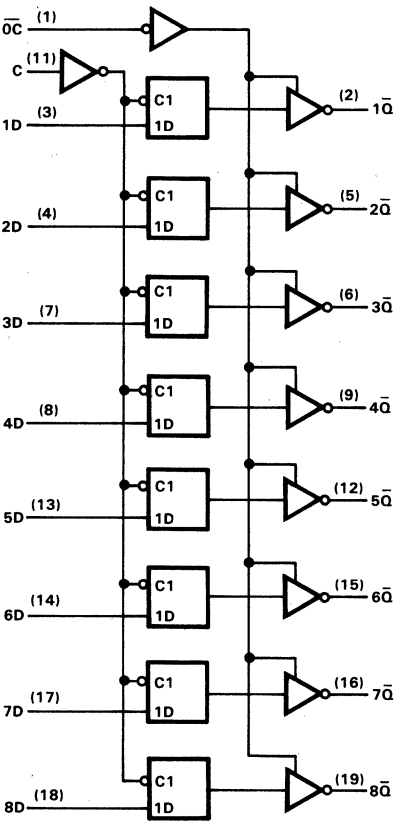
2 HCMOS Devices

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT533			SN74HCT533			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT533		SN74HCT533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OH} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT533		SN74HCT533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_{su}	Setup time, data before enable C↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t_h	Hold time, data after enable C↓	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT533		SN74HCT533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	4.5 V		38	35		53		44	ns
			5.5 V		24	32		48		40	
t_{pd}	C	Any $\overline{Q}$	4.5 V		30	35		53		44	ns
			5.5 V		28	32		48		40	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		29	35		53		44	ns
			5.5 V		25	32		48		40	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		25	35		53		44	ns
			5.5 V		24	32		48		40	
t_t		Any $\overline{Q}$	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT533		SN74HCT533		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	4.5 V		36	52		79		65	ns
			5.5 V		32	47		71		59	
t_{pd}	C	Any $\overline{Q}$	4.5 V		40	52		79		65	ns
			5.5 V		38	47		71		59	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		35	52		79		65	ns
			5.5 V		29	47		71		59	
t_t		Any $\overline{Q}$	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **High-Current 3-State Inverting Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-Mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

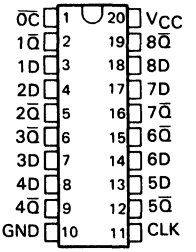
The eight flip-flops of the 'HC534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs. The 'HC534 is functionally equivalent to the 'HC374 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

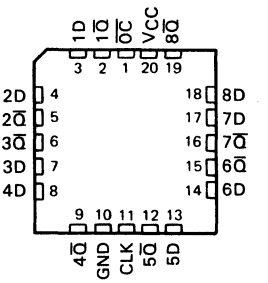
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC534 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC534 is characterized for operation from −40°C to 85°C.

SN54HC534 . . . J PACKAGE
SN74HC534 . . . DW OR N PACKAGE
(TOP VIEW)



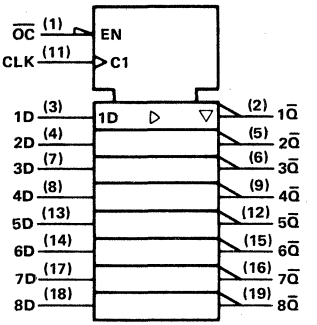
SN54HC534 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH FLIP-FLOP)

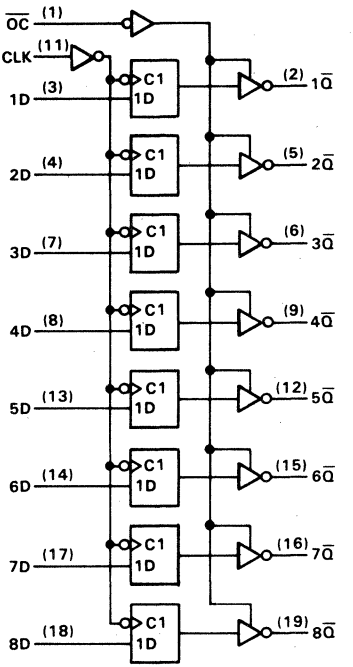
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC534			SN74HC534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC534		SN74HC534		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, data before CLK↑		2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	36		21		25		
			6 V	36	40		25		29		
t_{pd}	CLK	Any $\overline{Q}$	2 V		88	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	2 V		51	150		225		190	ns
			4.5 V		25	30		45		38	
			6 V		23	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation per flip-flop	No load, T_A = 25°C	100 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any $\overline{Q}$	2 V		105	230		345		290	ns
			4.5 V		35	46		69		58	
			6 V		31	39		58		49	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		95	200		300		250	ns
			4.5 V		32	40		60		50	
			6 V		29	34		51		43	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Inverting Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-Mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

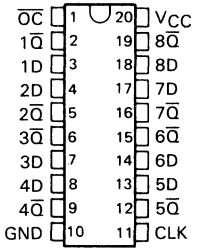
The eight flip-flops of the 'HCT534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs. The 'HCT534 is functionally equivalent to the 'HCT374 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

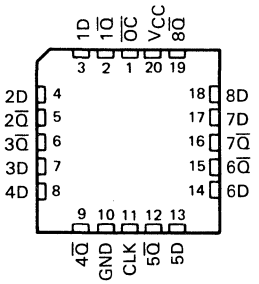
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54HCT534 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT534 is characterized for operation from −40°C to 85°C.

SN54HCT534 . . . J PACKAGE
SN74HCT534 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT534 . . . FK PACKAGE
(TOP VIEW)

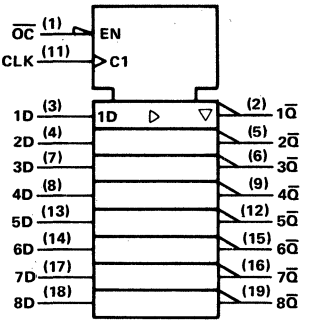


FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

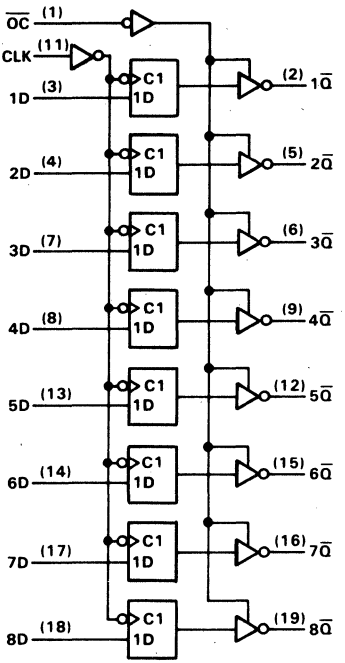
2 HCMOS Devices

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead Temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT534			SN74HCT534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT534		SN74HCT534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OH} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT534		SN74HCT534		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	31	0	21	0	25	MHz
			5.5 V	0	36	0	23	0	28	
t_w	Pulse duration	CLK high or low	4.5 V	16		24		20		ns
			5.5 V	14		22		18		
t_{su}	Setup time, data before CLK↑		4.5 V	20		30		25		ns
			5.5 V	17		27		23		
t_h	Hold time, data after CLK↑		4.5 V	5		5		5		ns
			5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT534		SN74HCT534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	36		21		25		MHz
			5.5 V	36	40		23		28		
t_{pd}	CLK	Any $\overline{Q}$	4.5 V		28	36		48		45	ns
			5.5 V		26	32		43		41	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		24	30		45		37	ns
			5.5 V		20	27		41		33	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		22	30		45		37	ns
			5.5 V		20	27		41		33	
t_t		Any $\overline{Q}$	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	93 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT534		SN74HCT534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any $\overline{Q}$	4.5 V		38	46		69		57	ns
			5.5 V		36	41		62		51	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		30	40		60		50	ns
			5.5 V		27	36		54		45	
t_t		Any $\overline{Q}$	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

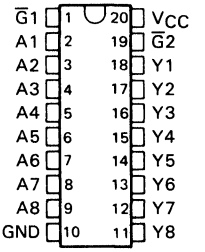
These octal buffers and line drivers are designed to have the performance of the popular SN54HC240/SN74HC240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR. If either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

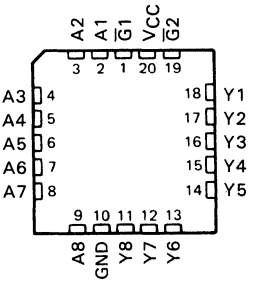
The 'HC540 provides inverted data and the 'HC541 provides true data at the outputs.

The SN54HC540 and SN54HC541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC540 and SN74HC541 are characterized for operation from −40°C to 85°C.

SN54HC540, SN54HC541 . . . J PACKAGE
SN74HC540, SN74HC541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC540, SN54HC541 . . . FK PACKAGE
(TOP VIEW)



'HC540
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

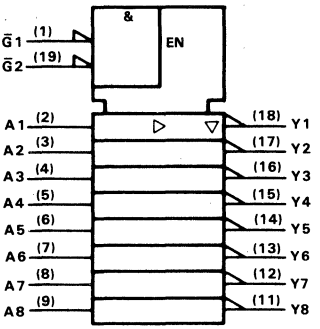
'HC541
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

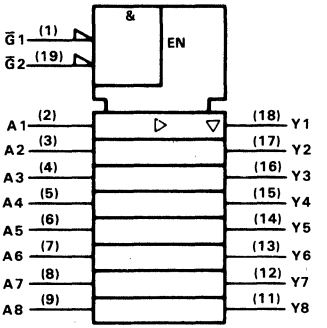
Z = High Impedance

logic symbols†

'HC540



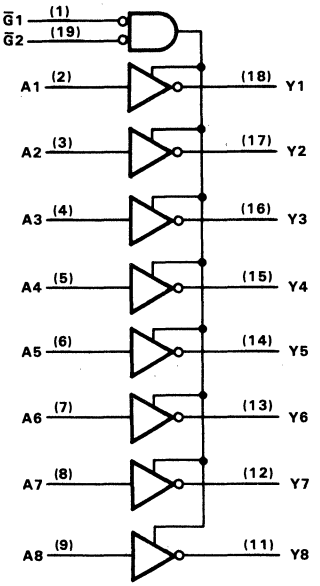
'HC541



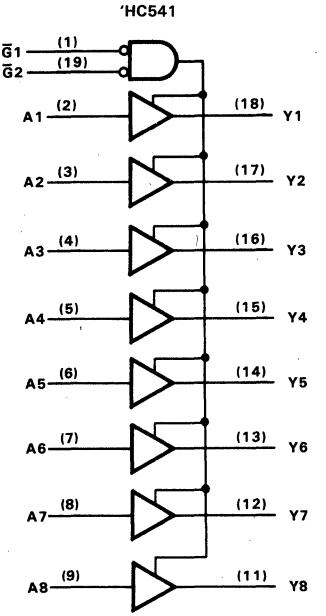
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'HC540



'HC541



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC540 SN54HC541			SN74HC540 SN74HC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC540 SN54HC541		SN74HC540 SN74HC541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 mA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

'HC540 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC540		SN74HC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		35	100		149		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_{en}	$\overline{G}$	Y	2 V		75	150		224		188	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Y	2 V		40	150		224		188	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	35 pF typ

'HC540 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC540		SN74HC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		60	150		224		188	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	$\overline{G}$	Y	2 V		100	200		298		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

'HC541 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC541		SN74HC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	115		171		144	ns
			4.5 V		12	23		34		29	
			6 V		10	20		29		25	
t_{en}	$\overline{G}$	Y	2 V		80	150		224		188	ns
			4.5 V		17	30		45		38	
			6 V		15	26		38		32	
t_{dis}	$\overline{G}$	Y	2 V		40	150		224		188	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	35 pF typ

'HC541 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC541		SN74HC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		65	165		246		206	ns
			4.5 V		16	33		49		41	
			6 V		14	28		42		35	
t_{en}	$\overline{G}$	Y	2 V		100	200		298		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

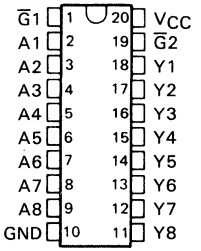
Note 1: Load circuits and voltage waveforms are shown in Section 1.

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

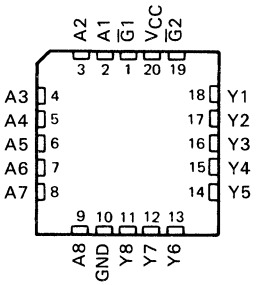
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive Up to 15 LSTTL Loads**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT540, SN54HCT541 . . . J PACKAGE
SN74HCT540, SN74HCT541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT540, SN54HCT541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54HCT240/SN74HCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR. If either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'HCT540 provides inverted data and the 'HCT541 provides true data at the outputs.

The SN54HCT540 and SN54HCT541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT540 and SN74HCT541 are characterized for operation from −40°C to 85°C.

'HCT540
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

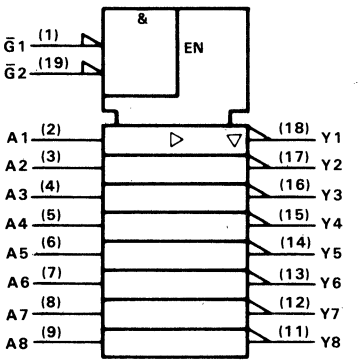
'HCT541
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

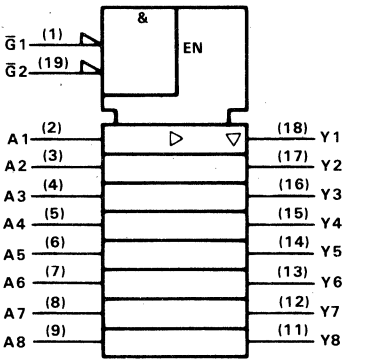
Z = High Impedance

logic symbols†

'HCT540



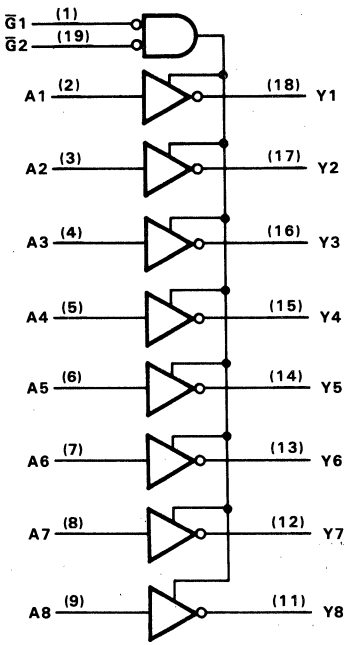
'HCT541



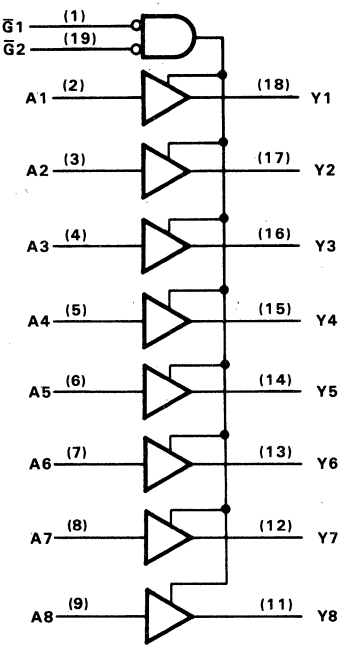
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'HCT540



'HCT541



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT540 SN54HCT541			SN74HCT540 SN74HCT541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT540 SN54HCT541		SN74HCT540 SN74HCT541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 mA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

'HCT540 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	20		30		25	ns
			5.5 V		12	18		27		23	
t_{en}	$\overline{G}$	Y	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{dis}	$\overline{G}$	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	35 pF typ

'HCT540 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	30		45		38	ns
			5.5 V		19	27		41		34	
t_{en}	$\overline{G}$	Y	4.5 V		26	40		60		50	ns
			5.5 V		25	36		54		45	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

'HCT541 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	23		34		29	ns
			5.5 V		12	21		31		26	
t_{en}	$\overline{G}$	Y	4.5 V		21	30		45		38	ns
			5.5 V		19	27		41		34	
t_{dis}	$\overline{G}$	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	35 pF typ

'HCT541 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	33		49		42	ns
			5.5 V		19	30		45		38	
t_{en}	$\overline{G}$	Y	4.5 V		26	40		60		50	ns
			5.5 V		25	36		54		45	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

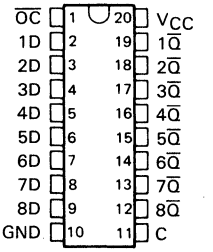
The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the outputs will be latched at the inverses of the levels that were set up at the D inputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

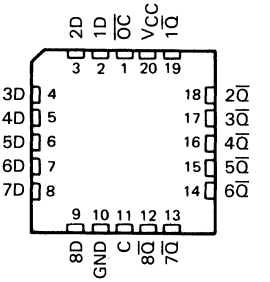
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC563 is characterized for operation from −40°C to 85°C.

SN54HC563 . . . J PACKAGE
SN74HC563 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC563 . . . FK PACKAGE
(TOP VIEW)

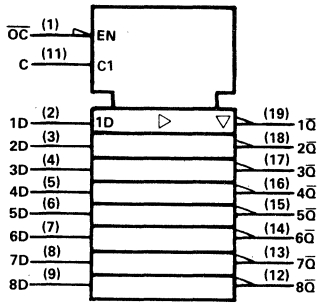


FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

2 HCMOS Devices

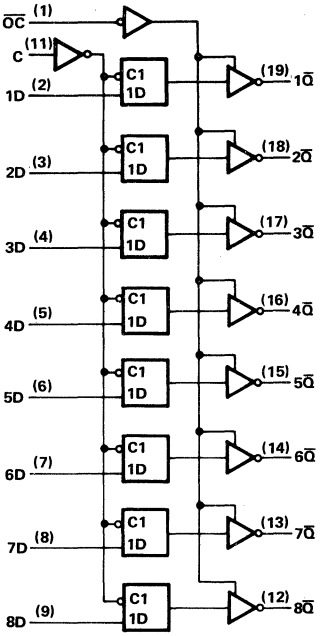
logic symbol



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			SN54HC563			SN74HC563			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC563		SN74HC563		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before enable C↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data afer enable C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		37	
t_{pd}	C	Any $\overline{Q}$	2 V		90	175		265		220	ns
			4.5 V		27	35		53		44	
			6 V		23	30		45		37	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		70	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		29	34		51		43	
t_{pd}	C	Any $\overline{Q}$	2 V		103	225		335		285	ns
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any $\overline{Q}$	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

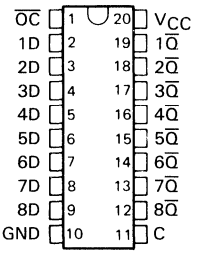
The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complement of data (D) inputs. When the enable is taken low the outputs will be latched at the inverses of the levels that were set up at the D inputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

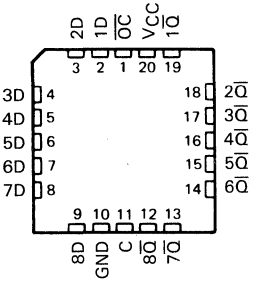
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT563 is characterized for operation from −40°C to 85°C.

SN54HCT563 . . . J PACKAGE
SN74HCT563 . . . DW OR N PACKAGE
(TOP VIEW)



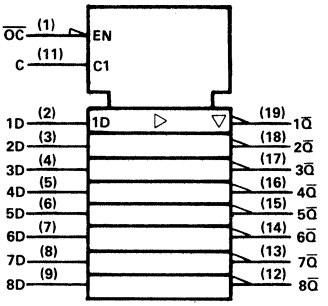
SN54HCT563 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

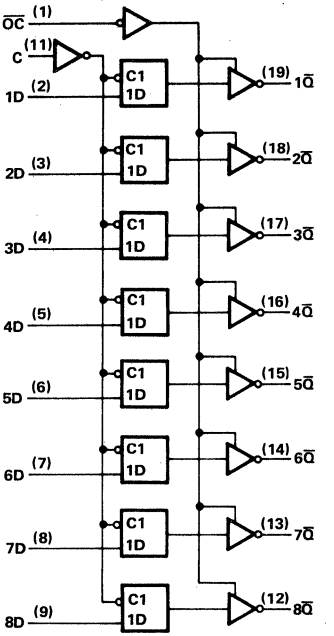
INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT563			SN74HCT563			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT563		SN74HCT563		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT563		SN74HCT563		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_{su}	Setup time, data before enable C↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t_h	Hold time, data afer enable C↓	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT563		SN74HCT563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	4.5 V		28	35		53		44	ns
			5.5 V		24	32		48		40	
t_{pd}	C	Any $\overline{Q}$	4.5 V		30	35		53		44	ns
			5.5 V		28	32		48		40	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		28	35		53		44	ns
			5.5 V		25	32		48		40	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		25	35		53		44	ns
			5.5 V		24	32		48		40	
t_t		Any $\overline{Q}$	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT563		SN74HCT563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	4.5 V		36	52		79		65	ns
			5.5 V		32	47		71		59	
t_{pd}	C	Any $\overline{Q}$	4.5 V		40	52		79		65	ns
			5.5 V		38	47		71		59	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		35	52		79		65	ns
			5.5 V		29	47		71		59	
t_t		Any $\overline{Q}$	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

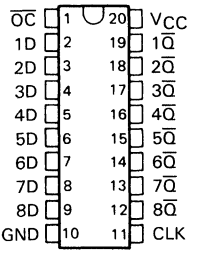
An output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC564 is characterized for operation from −40°C to 85°C.

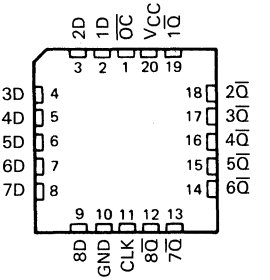
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

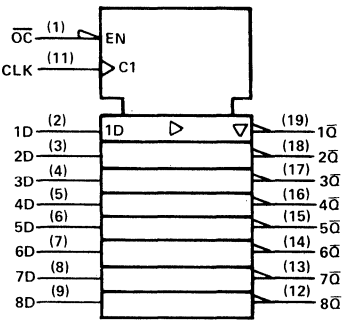
SN54HC564 . . . J PACKAGE
SN74HC564 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC564 . . . FK PACKAGE
(TOP VIEW)

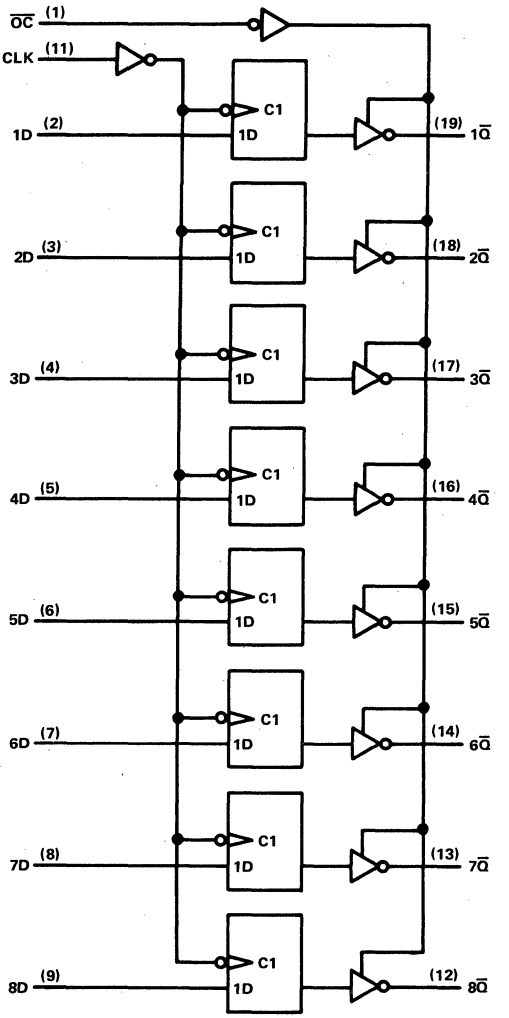


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC564			SN74HC564			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC564		SN74HC564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC564		SN74HC564		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before CLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC564		SN74HC564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	36		21		25		
			6 V	36	40		25		29		
t_{pd}	CLK	Any $\overline{Q}$	2 V		54	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		15	31		46		38	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		45	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	2 V		45	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	100 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC564		SN74HC564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Any $\overline{Q}$	2 V		75	230		345		290	ns
			4.5 V		24	46		69		58	
			6 V		21	34		58		49	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	2 V		57	200		300		250	ns
			4.5 V		19	40		60		50	
			6 V		17	34		51		43	
t_t		Any $\overline{Q}$	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

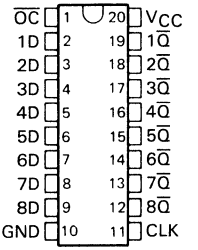
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT564 is characterized for operation from −40°C to 85°C.

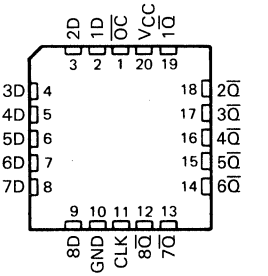
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

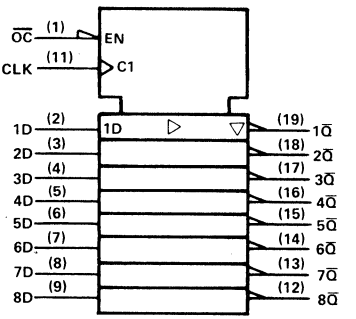
SN54HCT564 . . . J PACKAGE
SN74HCT564 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT564 . . . FK PACKAGE
(TOP VIEW)

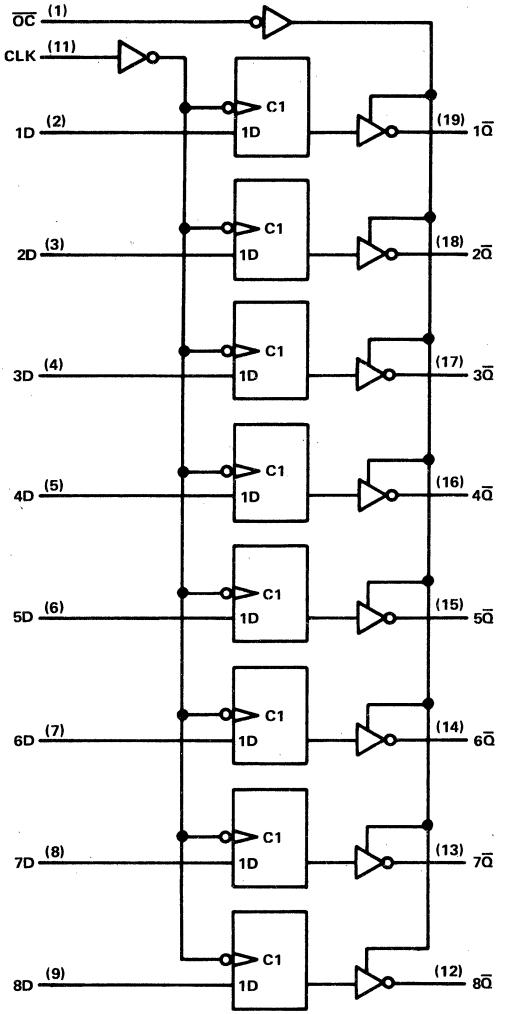


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT564			SN74HCT564			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT564		SN74HCT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT564		SN74HCT564		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	31		21		25	MHz
		5.5 V	0	36		23		28	
t_w	Pulse duration, CLK high or low	4.5 V	16		24		20		ns
		5.5 V	14		22		18		
t_{su}	Setup time, data before CLK↑	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_h	Hold time, data after CLK↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT564		SN74HCT564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	36		21		25		MHz
			5.5 V	36	40		23		28		
t_{pd}	CLK	Any $\overline{Q}$	4.5 V		18	36		54		45	ns
			5.5 V		16	32		48		41	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		14	30		45		38	ns
			5.5 V		10	27		41		34	
t_{dis}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		22	30		45		38	ns
			5.5 V		20	27		41		34	
t_t		Any $\overline{Q}$	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	93 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT564		SN74HCT564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any $\overline{Q}$	4.5 V		38	53		80		66	ns
			5.5 V		36	47		71		60	
t_{en}	$\overline{OC}$	Any $\overline{Q}$	4.5 V		30	47		71		59	ns
			5.5 V		27	39		59		49	
t_t		Any $\overline{Q}$	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the (Q) outputs will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

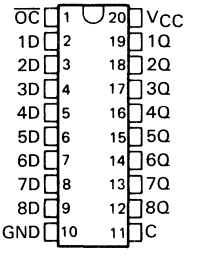
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC573 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC573 is characterized for operation from −40°C to 85°C.

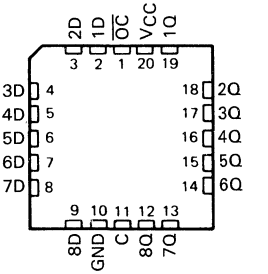
FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			Q
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

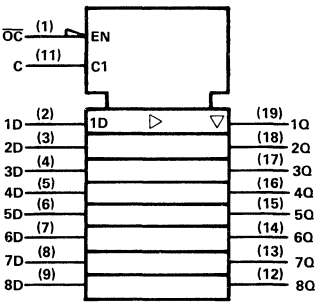
SN54HC573 . . . J PACKAGE
SN74HC573 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC573 . . . FK PACKAGE
(TOP VIEW)

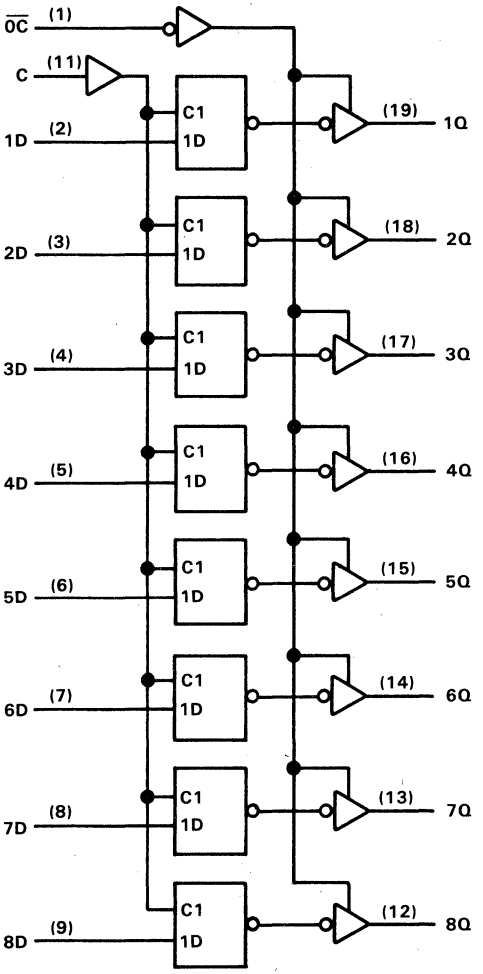


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC573			SN74HC573			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC573		SN74HC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC573		SN74HC573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before enable C↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data afer enable C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC573		SN74HC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		38	
t_{pd}	C	Any Q	2 V		87	175		265		220	ns
			4.5 V		27	35		53		44	
			6 V		23	30		45		38	
t_{en}	$\overline{OC}$	Any Q	2 V		68	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OC}$	Any Q	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC573		SN74HC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
t_{pd}	C	Any Q	2 V		103	225		335		285	ns
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OC}$	Any Q	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

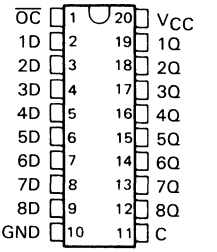
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

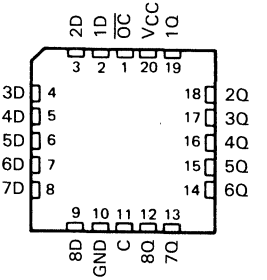
An output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs re in the high-impedance state.

The SN54HCT573 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT573 is characterized for operation from −40°C to 85°C.

SN54HCT573 . . . J PACKAGE
SN74HCT573 . . . DW OR N PACKAGE
(TOP VIEW)



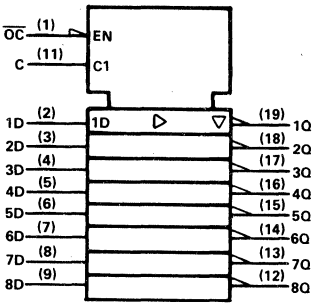
SN54HCT573 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH LATCH)

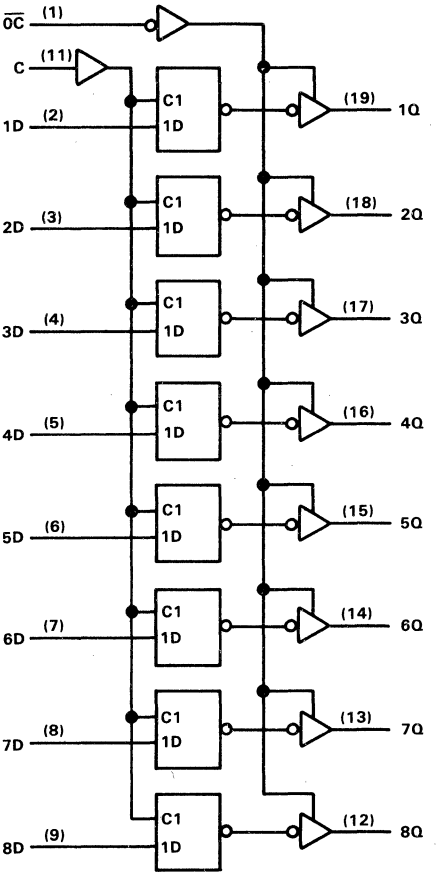
INPUTS			OUTPUT
ENABLE			Q
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic symbol (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HCT573			SN74HCT573			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT573		SN74HCT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT573		SN74HCT573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_{su}	Setup time, data before enable C↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t_h	Hold time, data afer enable C↓	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT573		SN74HCT573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		25	35		53		44	ns
			5.5 V		21	32		48		40	
t_{pd}	C	Any Q	4.5 V		28	35		53		44	ns
			5.5 V		25	32		48		40	
t_{en}	$\overline{OC}$	Any Q	4.5 V		26	35		53		44	ns
			5.5 V		23	32		48		40	
t_{dis}	$\overline{OC}$	Any Q	4.5 V		23	35		53		44	ns
			5.5 V		22	32		48		40	
t_t		Any Q	4.5 V		9	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT573		SN74HCT573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		32	52		79		65	ns
			5.5 V		27	47		71		59	
t_{pd}	C	Any Q	4.5 V		38	52		79		65	ns
			5.5 V		36	47		71		59	
t_{en}	$\overline{OC}$	Any Q	4.5 V		33	52		79		65	ns
			5.5 V		28	47		71		59	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	50 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **High-Current 3-State Noninverting Outputs Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

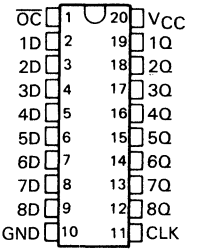
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC574 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC574 is characterized for operation from −40°C to 85°C.

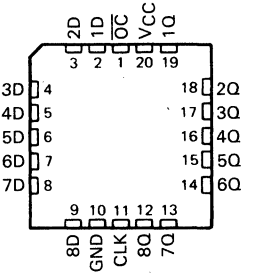
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

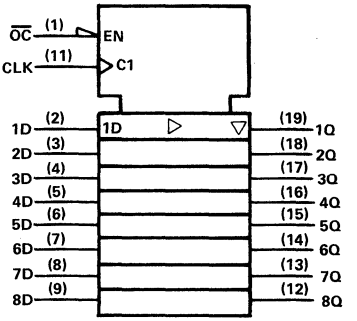
SN54HC574 . . . J PACKAGE
SN74HC574 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC574 . . . FK PACKAGE
(TOP VIEW)

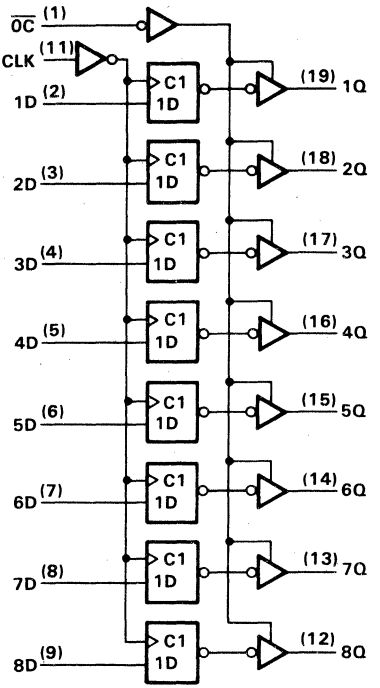


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC574			SN74HC574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC574		SN74HC574		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4	0	5	MHz
			4.5 V	0	30	0	20	0	24	
			6 V	0	38	0	24	0	28	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, data before CLK↑		2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4		5		MHz
			4.5 V	30	36		20		24		
			6 V	36	40		24		28		
t_{pd}	CLK	Any Q	2 V		90	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t_{en}	$\overline{OC}$	Any Q	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t_{dis}	$\overline{OC}$	Any Q	2 V		52	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		22	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	100 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6			4		5		MHz
			4.5 V	30			20		24		
			6 V	36			24		28		
t_{pd}	CLK	Any Q	2 V		105	265		400		330	ns
			4.5 V		36	53		80		66	
			6 V		31	46		68		57	
t_{en}	$\overline{OC}$	Any Q	2 V		95	235		355		295	ns
			4.5 V		32	47		71		59	
			6 V		28	41		60		51	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **High-Current 3-State Noninverting Outputs Drive Bus-Lines Directly or Up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

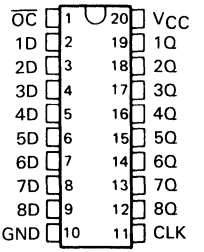
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT574 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT574 is characterized for operation from −40°C to 85°C.

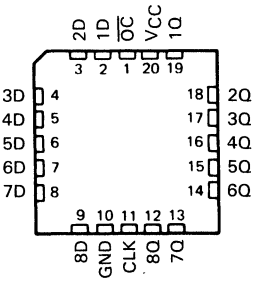
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

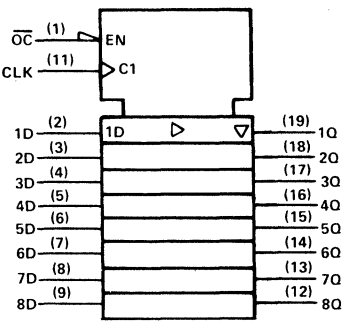
SN54HCT574 . . . J PACKAGE
SN74HCT574 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT574 . . . FK PACKAGE
(TOP VIEW)

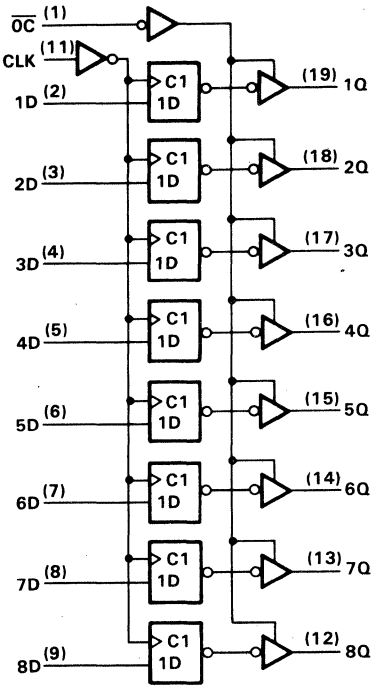


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT574			SN74HCT574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT574		SN74HCT574		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	30	0	20	0	24	MHz
			5.5 V	0	33	0	22	0	27	
t_w	Pulse duration	CLK high or low	4.5 V	16		24		20		ns
			5.5 V	14		22		18		
t_{su}	Setup time, data before CLK↑		4.5 V	20		30		25		ns
			5.5 V	17		27		23		
t_h	Hold time, data after CLK↑		4.5 V	5		5		5		ns
			5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		48		41	
t_{en}	$\overline{OC}$	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	$\overline{OC}$	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	93 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		40	53		80		66	ns
			5.5 V		35	47		71		60	
t_{en}	$\overline{OC}$	Any Q	4.5 V		34	47		71		59	ns
			5.5 V		29	39		94		78	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **8-Bit Counter with Register**
- **High-Current 3-State Parallel Register Outputs Can Drive Up to 15 LSTTL Loads**
- **Counter has Direct Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

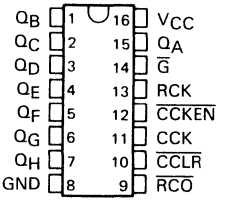
description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output RCO is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

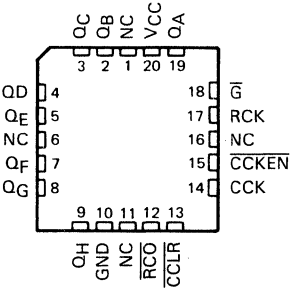
Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The SN54HC590A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC590A is characterized for operation from −40°C to 85°C.

SN54HC590A . . . J PACKAGE
SN74HC590A . . . DW OR N PACKAGE
(TOP VIEW)

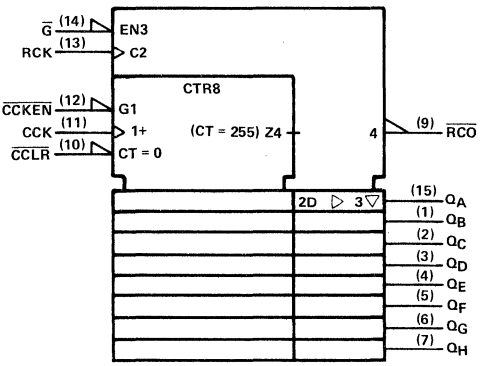


SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

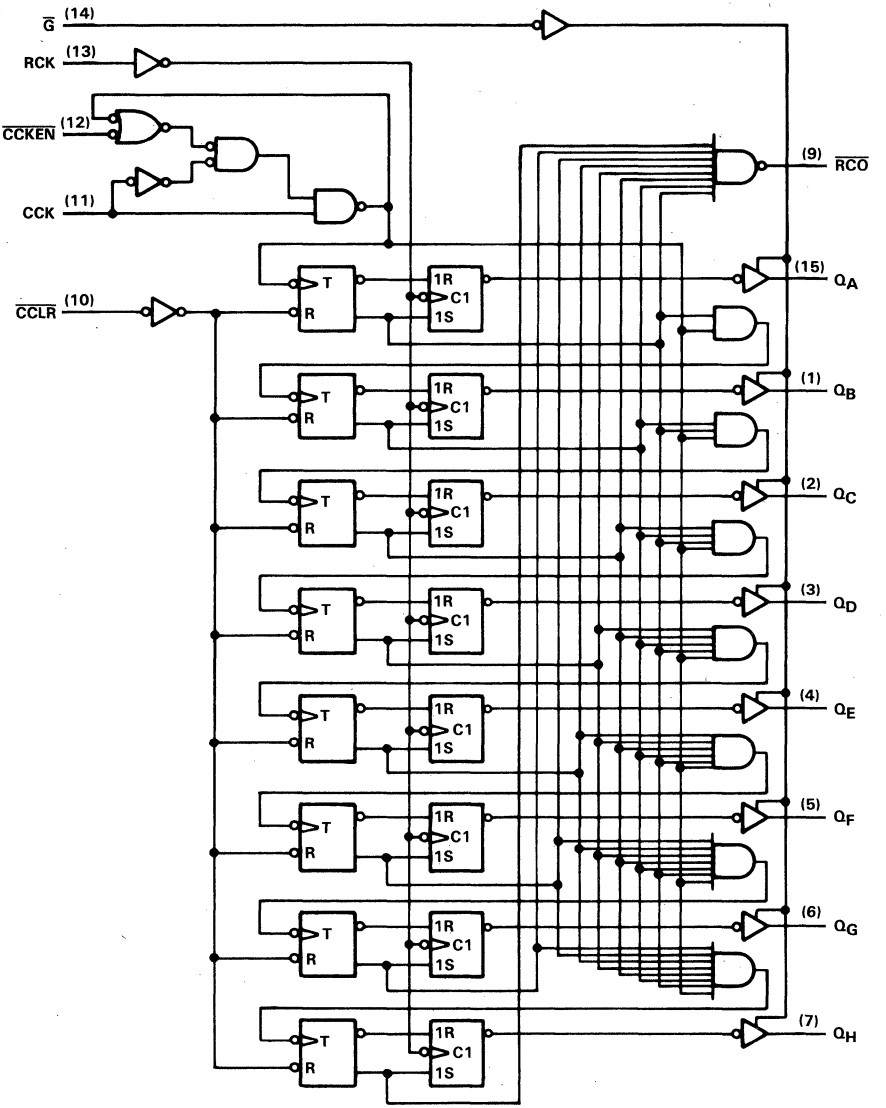
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC590A			SN74HC590A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	$\overline{RCO}$, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		Q_A-Q_H, I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	$\overline{RCO}$, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		Q_A-Q_H, I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	$\overline{RCO}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	$\overline{RCO}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC590A		SN74HC590A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CCK or RCK		2 V	0	4	0	2.5	0	3.2	MHz
			4.5 V	0	20	0	13		16	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CCK or RCK high or low	2 V	125		200		155		ns
			4.5 V	25		38		31		
			6 V	21		32		26		
		$\overline{CCLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		$\overline{CCLR}$ high (inactive) before CCK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6V	17		26		21		
		CLK↑ before RCK↑ (see Note 1)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		

Note 1: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register will be one clock pulse behind the counter.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CCK or RCK		2 V	4	8		2.5		3.2		MHz
			4.5 V	20	35		13		16		
			6 V	24	40		16		19		
t_{pd}	CCK↑	$\overline{RCO}$	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		15	26		38		33	
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		70	130		195		165	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_{pd}	RCK↑	Q	2 V		70	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_{en}	$\overline{G}$↓	Q	2 V		80	125		185		155	ns
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t_{dis}	$\overline{G}$↓	Q	2 V		80	125		185		155	ns
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t_t		$\overline{RCO}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
t_t		Q	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	250 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCK↑	Q	2 V		100	300		447		380	ns
			4.5 V		24	60		90		76	
			6 V		20	51		77		65	
t_{en}	$\overline{G}$	Q	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **8-Bit Serial-In, Parallel-Out Shift Registers with Storage**
- **Independent Direct-Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Both Shift and Storage Registers**
- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

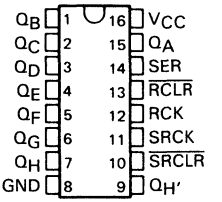
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct-overriding clears are provided on both the shift and storage registers. A serial output (Q_H') is provided for cascading purposes.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

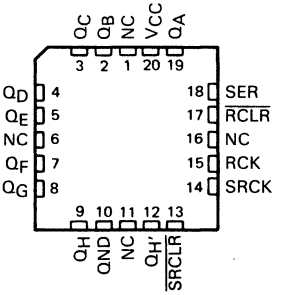
The parallel outputs (Q_A thru Q_H) have high-current capability; output Q_H' is a standard output.

The SN54HC594 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC594 is characterized for operation from −40°C to 85°C.

SN54HC594 . . . J PACKAGE
SN74HC594 . . . DW OR N PACKAGE
(TOP VIEW)

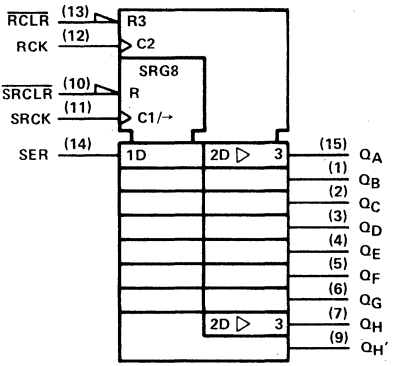


SN54HC594 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

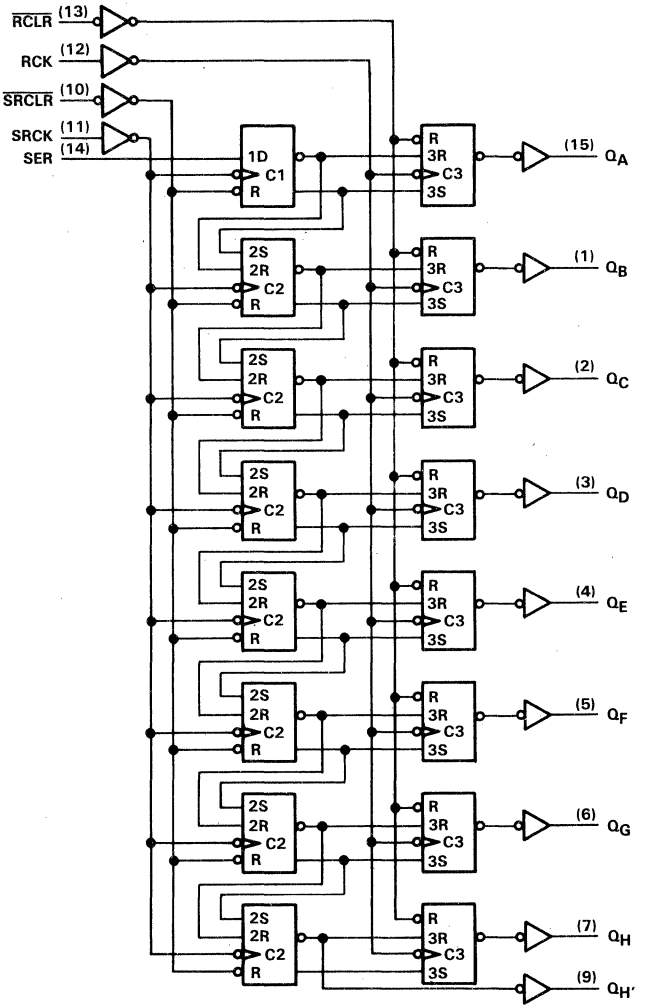
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC594			SN74HC594			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		Q_A-Q_H, I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		Q_A-Q_H, I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC594		SN74HC594		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, SRCK or RCK		2 V	0	5	0	3.3	0	4	MHz
			4.5 V	0	25	0	17	0	20	
			6 V	0	29	0	20	0	24	
t_w	Pulse duration	SRCK or RCK high or low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{SRCLR}$ or $\overline{RCLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time	SER before SRCK↑	2 V	90		135		110		ns
			4.5 V	18		27		22		
			6 V	15		23		19		
		SRCK↑ before RCK↑ (see Note 1)	2 V	90		135		110		ns
			4.5 V	18		27		22		
			6 V	15		23		19		
		$\overline{SRCLR}$ low before RCK↑	2 V	50		75		63		ns
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{SRCLR}$ high (inactive) before SRCK↑	2 V	20		20		20		ns
			4.5 V	10		10		10		
			6 V	10		10		10		
		$\overline{RCLR}$ high (inactive) before SRCK↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
t_h	Hold time	SER after SRCK↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

Note 1: This setup time ensures the output register will see stable data from the shift-register outputs. The clocks may be tied together in which case the output register will be one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SRCK or RCK		2 V	5	8		3.3		4		MHz
			4.5 V	25	35		17		20		
			6 V	29	40		20		24		
t_{pd}	SRCK	Q_H'	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t_{pd}	RCK	Q_A thru Q_H	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t_{PHL}	$\overline{SRCLR}$	Q_H'	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t_{PHL}	$\overline{RCLR}$	Q_A thru Q_H	2 V		50	125		185		155	ns
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t_t		Q_H'	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
t_t		Q_A thru Q_H	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	395 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCK	Q_A thru Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_{PHL}	$\overline{RCLR}$	Q_A thru Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A thru Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **8-Bit Serial-In, Parallel-Out Shift**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Shift Register has Direct Clear**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

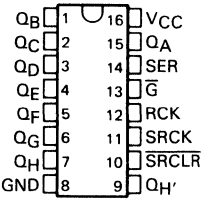
description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

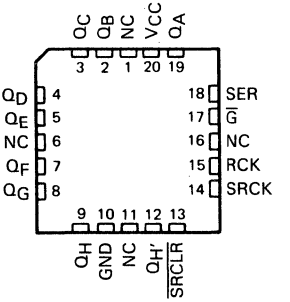
Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

The SN54HC595 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC595 is characterized for operation from −40°C to 85°C.

SN54HC595 . . . J PACKAGE
SN74HC595 . . . DW OR N PACKAGE
(TOP VIEW)

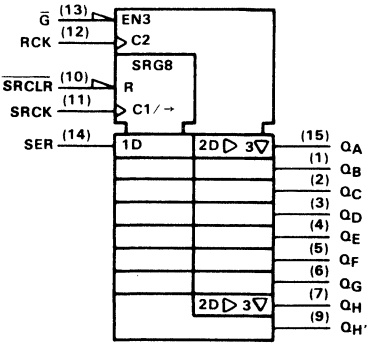


SN54HC595 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

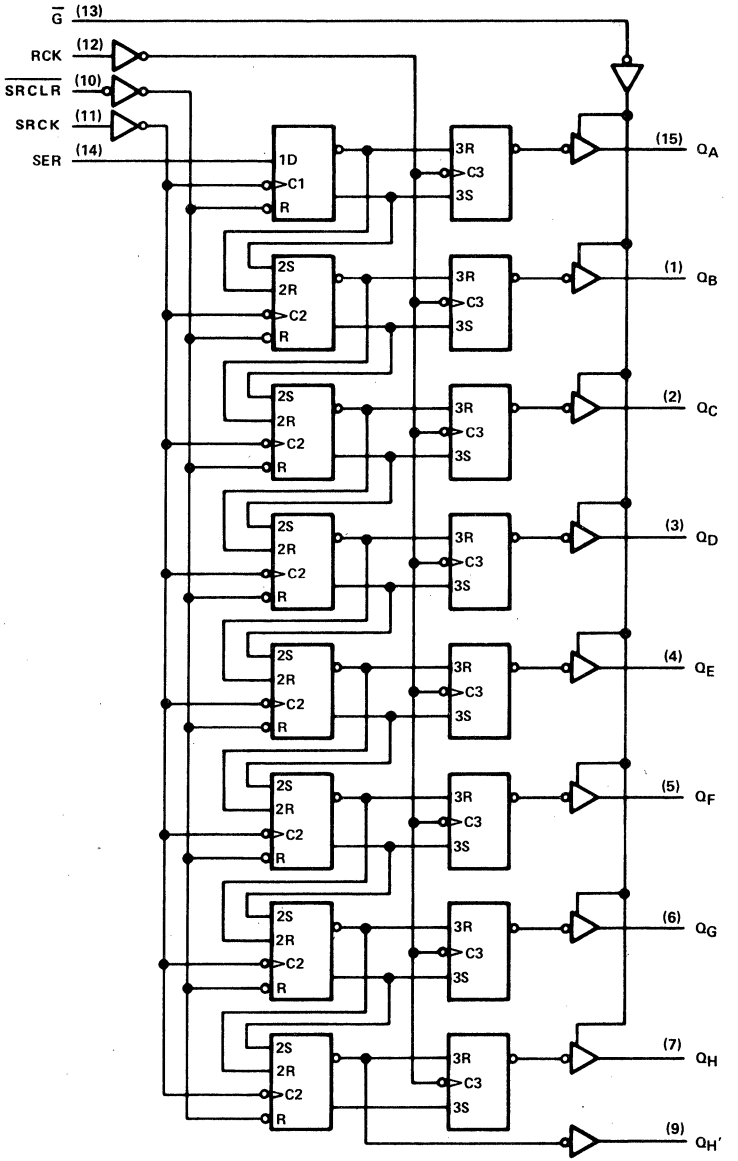
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		Q_A-Q_H, I_{OH} = −6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
		Q_A-Q_H, I_{OH} = −7.8 mA									
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 6 mA									
	V_I = V_{IH} or V_{IL}	Q_H', I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A-Q_H, I_{OL} = 7.8 mA									
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC595		SN74HC595		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	SRCK or RCK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{SRCLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SER before SRCK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		SRCK↑ before RCK↑ (see Note 1)	2 V	75		113		94		ns
			4.5 V	15		23		19		
			6 V	13		19		16		
		$\overline{SRCLR}$ low before RCK↑	2 V	50		75		65		ns
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{SRCLR}$ high (inactive) before SRCK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		
t_h	Hold time	SER after SRCK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

Note 1: This setup time ensures the output register will see stable data from the shift-register outputs. The clocks may be tied together in which case the output register will be one clock pulse behind the shift register.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	SRCK or RCK		2 V	6	26		4.2		5		MHz
			4.5 V	31	38		21		25		
			6 V	36	42		25		29		
t_{pd}	SRCK	Q_H'	2 V		50	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t_{pd}	RCK	Q_A to Q_H	2 V		50	150		225		187	ns
			4.5 V		17	30		45		37	
			6 V		14	26		38		32	
t_{PHL}	$\overline{SRCLR}$	Q_H'	2 V		51	175		261		219	ns
			4.5 V		18	35		52		44	
			6 V		15	30		44		37	
t_{en}	$\overline{G}$	Q_A to Q_H	2 V		40	150		225		187	ns
			4.5 V		15	30		45		37	
			6 V		13	26		38		32	
t_{dis}	$\overline{G}$	Q_A to Q_H	2 V		42	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		20	34		51		43	
t_t		Q_A to Q_H	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	
t_t		Q_H'	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	400 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCK	Q_A to Q_H	2 V		60	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{en}	$\overline{G}$	Q_A to Q_H	2 V		70	200		298		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A to Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **16 D-Type Registers, One for Each Data Input**
- **Multiplexer Selects Stored Data from Either A Bus or B Bus**
- **Application-Oriented for Maximum Speed**
- **Package Options Include Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC604 multiplexed latch is ideal for storing data from two input buses, A and B, and for providing the output bus with stored data from either the A or B register.

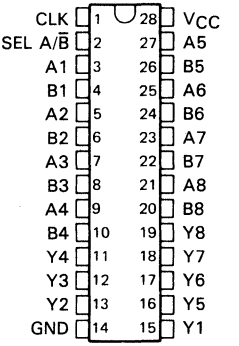
The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The device is optimized for high-speed operation.

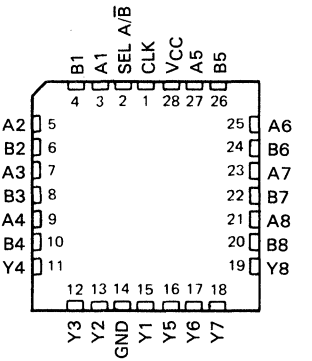
These functions are ideal for interfacing from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54HC604 is characterized for operation over the full military range of −55°C to 125°C. The SN74HC604 is characterized for operation from −40°C to 85°C.

SN54HC604 . . . J PACKAGE
SN74HC604 . . . N PACKAGE
(TOP VIEW)



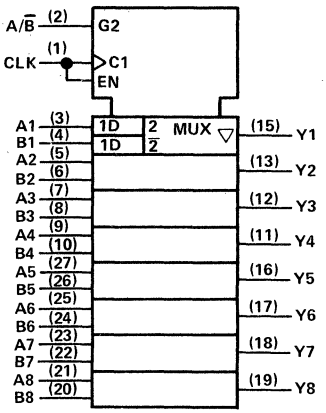
SN54HC604 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

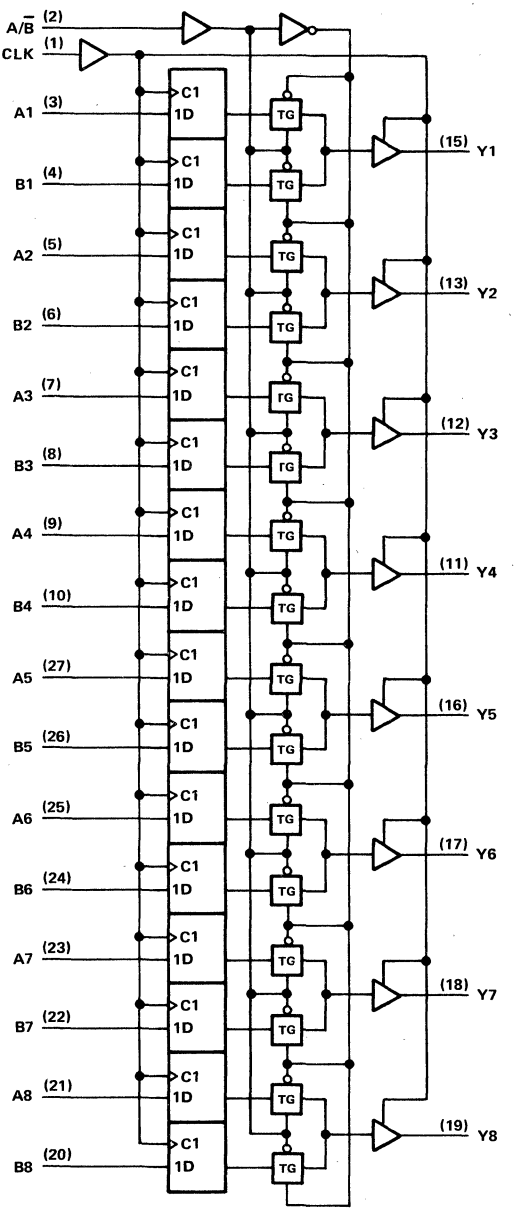
INPUTS				OUTPUTS
A1—A8	B1—B8	A/B̄	CLOCK	Y1—Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B register stored data
X	X	H	H	A register stored data

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC604			SN74HC604			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC604		SN74HC604		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or GND	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or GND	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC604		SN74HC604		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	5	0	3.3	0	4	MHz
		4.5 V	0	25	0	17	0	20	
		6 V	0	29	0	20	0	24	
t_w	Pulse duration, CLK high or low	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
t_{su}	Setup time, data before CLK↑	2 V	75		115		95		ns
		4.5 V	15		23		19		
		6 V	13		20		16		
t_h	Hold time, data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

TEXAS INSTRUMENTS
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC604		SN74HC604		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5			3.3		4		MHz
			4.5 V	25			17		20		
			6 V	29			20		24		
t_{pd}	A/$\overline{B}$	Y	2 V		92	170		255		215	ns
			4.5 V		23	34		51		43	
			6 V		17	29		43		37	
t_{en}	CLK	Y	2 V		96	195		295		245	ns
			4.5 V		25	39		59		49	
			6 V		19	33		50		42	
t_{dis}	CLK	Y	2 V		84	200		300		250	ns
			4.5 V		30	40		60		50	
			6 V		26	34		51		43	
t_t		Any	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	100 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC604		SN74HC604		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A/$\overline{B}$	Y	2 V		110	225		385		320	ns
			4.5 V		28	51		77		64	
			6 V		21	44		65		56	
t_{en}	CLK	Y	2 V		120	280		425		350	ns
			4.5 V		30	56		85		70	
			6 V		23	48		72		61	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

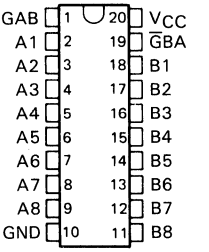
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

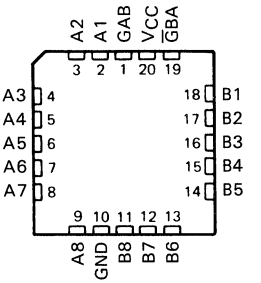
- **Lock Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC620	Inverting
'HC623	True

SN54HC' . . . J PACKAGE
SN74HC' . . . DW or N PACKAGE
(TOP VIEW)



SN54HC' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB.)

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HC623 or complementary for the 'HC620.

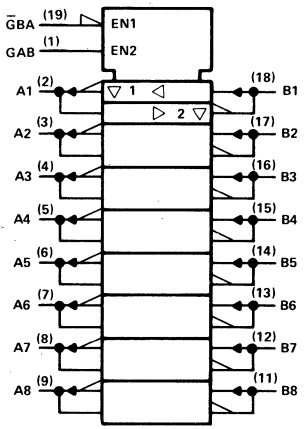
The SN54HC620 and SN54HC623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC620 and SN74HC623 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

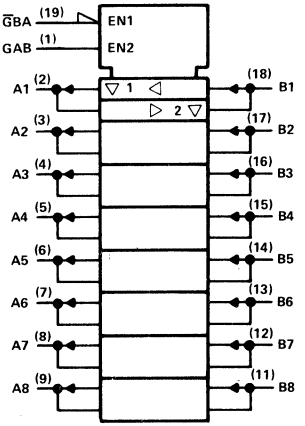
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'HC620	'HC623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols†

'HC620



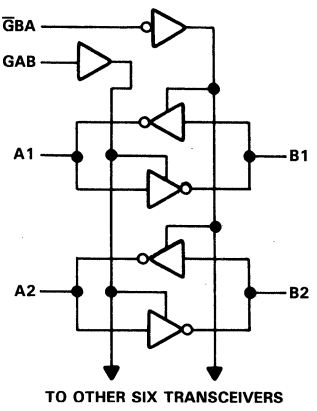
'HC623



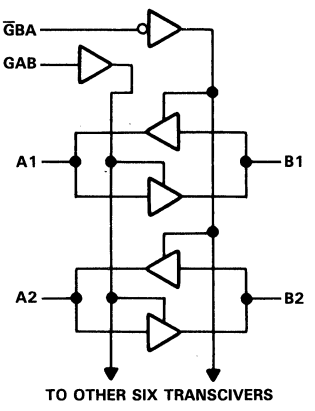
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'HC620



'HC623



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC620 SN54HC623			SN74HC620 SN74HC623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC620 SN54HC623		SN74HC620 SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		$V_I = V_{IH}$ or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		$V_I = V_{IH}$ or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	GAB or $\overline{GBA}$	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i	GAB or $\overline{GBA}$		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC620 SN54HC623		SN74HC620 SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		29	105		160		130	ns
			4.5 V		10	21		32		26	
			6 V		8	18		27		22	
t_{en}	$\overline{G}$BA	A	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t_{dis}	$\overline{G}$BA	A	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_{en}	GAB	B	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t_{dis}	GAB	B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC620 SN54HC623		SN74HC620 SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		44	135		200		170	ns
			4.5 V		14	27		40		34	
			6 V		11	23		34		29	
t_{en}	$\overline{G}$BA	A	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
t_{en}	GAB	B	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

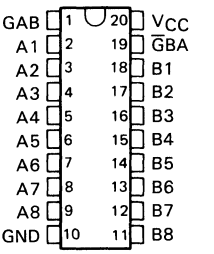
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

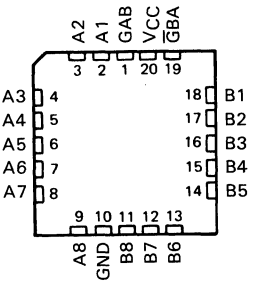
- **Inputs are TTL-Voltage Compatible**
- **Lock Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HCT620	Inverting
'HCT623	True

SN54HCT'. . . J PACKAGE
SN74HCT'. . . DW or N PACKAGE
(TOP VIEW)



SN54HCT'. . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB.)

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HCT623 or complementary for the 'HCT620.

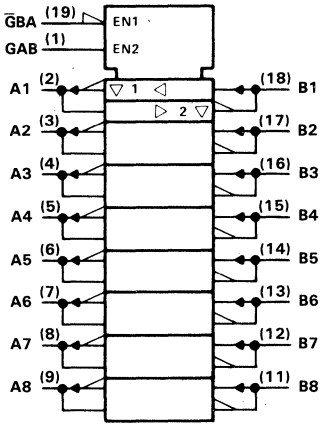
The SN54HCT620 and SN54HCT623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT620 and SN74HCT623 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

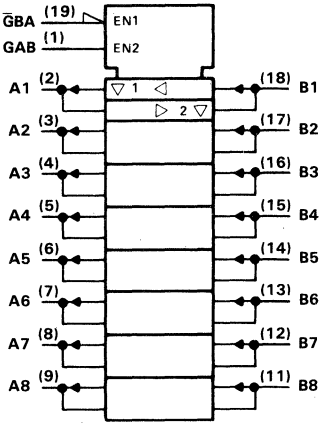
ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'HCT620	'HCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

logic symbols†

'HCT620



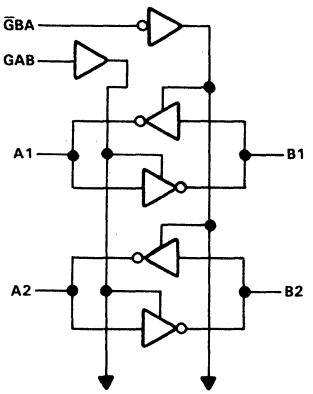
'HCT623



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

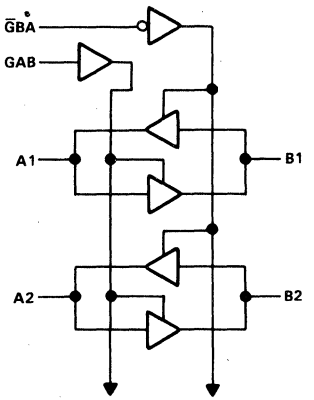
logic diagrams (positive logic)

'HCT620



TO OTHER SIX TRANSCEIVERS

'HCT623



TO OTHER SIX TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT620 SN54HCT623			SN74HCT620 SN74HCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT620 SN54HCT623		SN74HCT620 SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20\ \mu A$	4.5 V	4.4	4.499		4.4		4.4		V
		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -6$ mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 20\ \mu A$	4.5 V		0.001	0.1		0.1		0.1	V
		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 6$ mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	GAB or $\overline{GBA}$	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_I = V_{CC}$ or GND	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8		160		80	μA
ΔI_{CC}‡		One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3.0		2.9	mA
C_i	GAB or $\overline{GBA}$		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT620 SN54HCT623		SN74HCT620 SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	22		33		28	ns
			5.5 V		13	20		30		25	
t_{en}	$\overline{G}$BA	A	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	$\overline{G}$BA	A	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_{en}	GAB	B	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	GAB	B	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT620 SN54HCT623		SN74HCT620 SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		18	38		58		47	ns
			5.5 V		11	34		52		42	
t_{en}	$\overline{G}$BA	A	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_{en}	GAB	B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

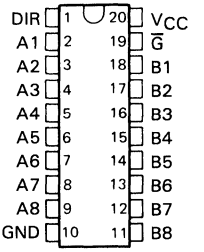
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

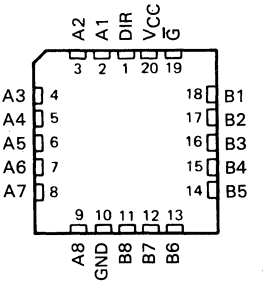
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC640	Inverting
'HC643	True and Inverting
'HC645	True

SN54HC' . . . J PACKAGE
SN74HC' . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

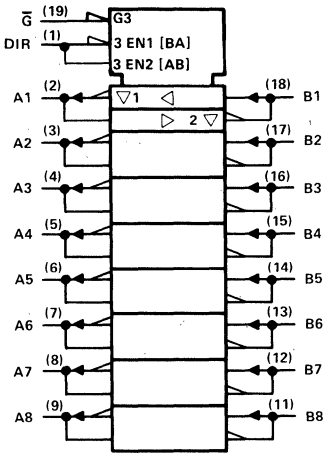
The SN54HC640, SN54HC643, and SN54HC645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC640, SN74HC643, and SN74HC645 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

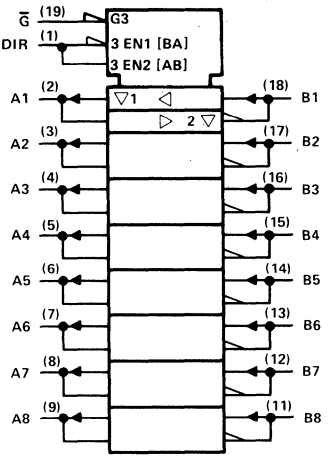
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'HC640	'HC643	'HC645
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols†

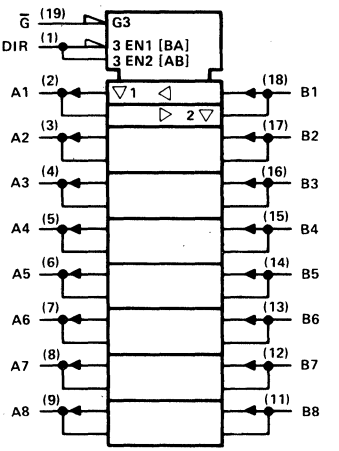
'HC640



'HC643



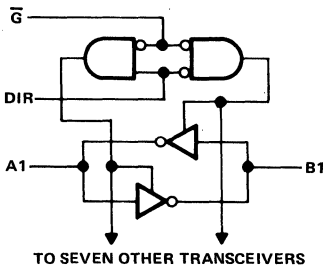
'HC645



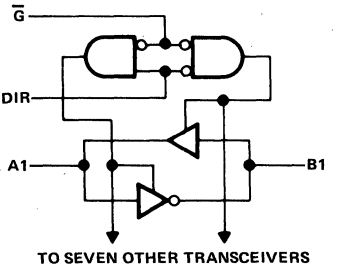
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

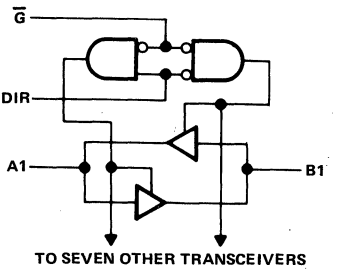
'HC640



'HC643



'HC645



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC640 SN54HC643 SN54HC645			SN74HC640 SN74HC643 SN74HC645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC640 SN54HC643 SN54HC645		SN74HC640 SN74HC643 SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{G}$	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i	DIR or $\overline{G}$		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC640		SN74HC640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		29	105		160		130	ns
			4.5 V		10	21		32		26	
			6 V		8	18		27		22	
t_{en}	$\overline{G}$	A or B	2 V		109	230		340		290	ns
			4.5 V		27	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC640		SN74HC640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		44	190		290		235	ns
			4.5 V		14	38		58		47	
			6 V		11	33		49		41	
t_{en}	$\overline{G}$	A or B	2 V		124	315		470		395	ns
			4.5 V		31	63		94		79	
			6 V		23	54		80		68	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC643		SN74HC643		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		29	110		165		140	ns
			4.5 V		10	22		33		28	
			6 V		8	19		28		24	
t_{en}	$\overline{G}$	A or B	2 V		109	230		340		290	ns
			4.5 V		27	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC643		SN74HC643		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		44	195		295		245	ns
			4.5 V		14	39		59		49	
			6 V		11	34		50		43	
t_{en}	$\overline{G}$	A or B	2 V		124	315		470		395	ns
			4.5 V		31	63		94		79	
			6 V		23	54		80		68	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t_{en}	$\overline{G}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{G}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	$\overline{G}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

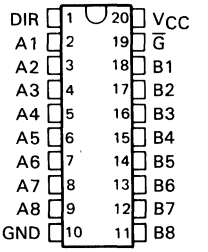
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2804, MARCH 1984—REVISED SEPTEMBER 1987

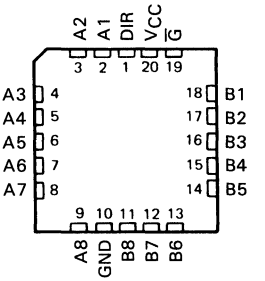
- **Inputs are TTL-Voltage Compatible**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HCT640	Inverting
'HCT643	True and Inverting
'HCT645	True

SN54HCT' . . . J PACKAGE
SN74HCT' . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT' . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

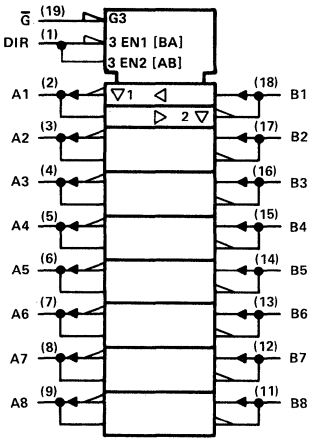
The SN54HCT640, SN54HCT643, and SN54HCT645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT640, SN74HCT643 and SN74HCT645 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

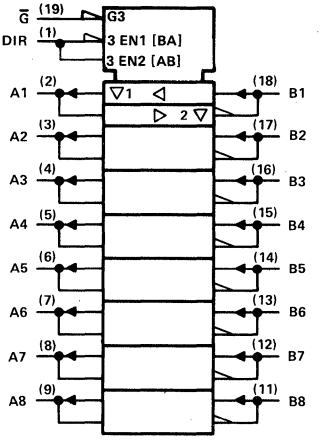
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'HCT640	'HCT643	'HCT645
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation	Isolation

logic symbols†

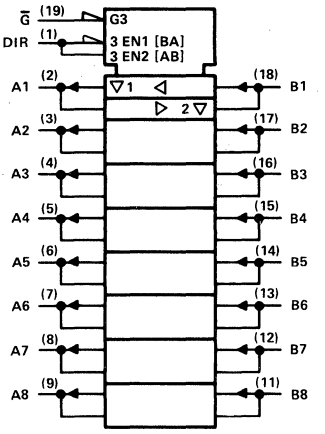
'HCT640



'HCT643



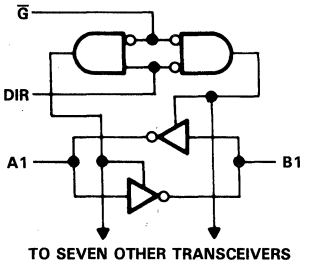
'HCT645



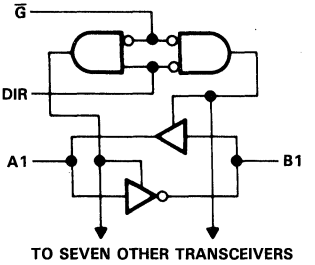
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

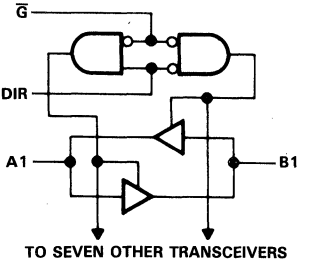
'HCT640



'HCT643



'HCT645



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT640 SN54HCT643 SN54HCT645			SN74HCT640 SN74HCT643 SN74HCT645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT640 SN54HCT643 SN54HCT645		SN74HCT640 SN74HCT643 SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	DIR or $\overline{G}$	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡		One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i	DIR or $\overline{G}$		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT640 SN54HCT643		SN74HCT640 SN74HCT643		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		14	21		32		25	ns
			5.5 V		12	18		27		23	
t_{en}	$\overline{G}$	A or B	4.5 V		27	35		53		44	ns
			5.5 V		24	32		47		39	
t_{dis}	$\overline{G}$	A or B	4.5 V		20	30		45		38	ns
			5.5 V		18	26		41		34	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT640 SN54HCT643		SN74HCT640 SN74HCT643		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		17	27		41		34	ns
			5.5 V		15	24		37		30	
t_{en}	$\overline{G}$	A or B	4.5 V		31	45		68		56	ns
			5.5 V		28	41		61		51	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t_{en}	$\overline{G}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t_{dis}	$\overline{G}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

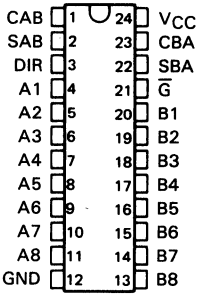
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{G}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

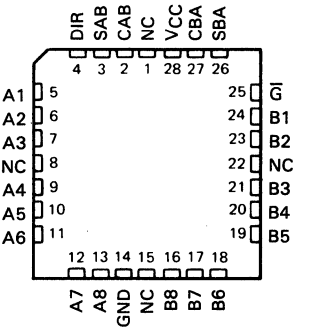
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC'. . . JT PACKAGE
SN74HC'. . . DW or NT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

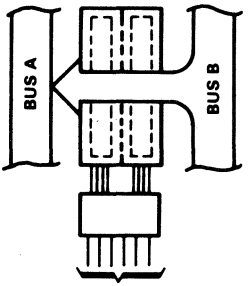
description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HC646 or 'HC648.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

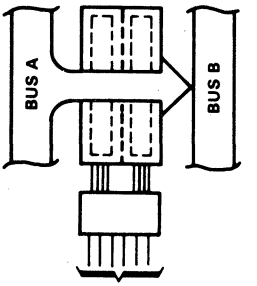
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.



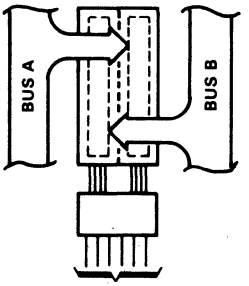
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



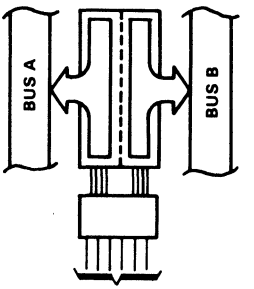
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A OR B

Pin numbers shown are for DW, JT, and NT packages.

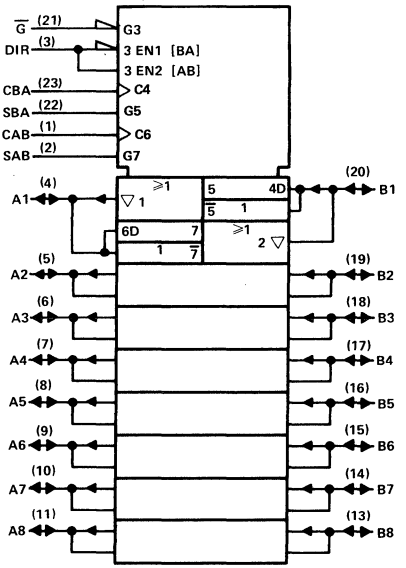
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HC646	'HC648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

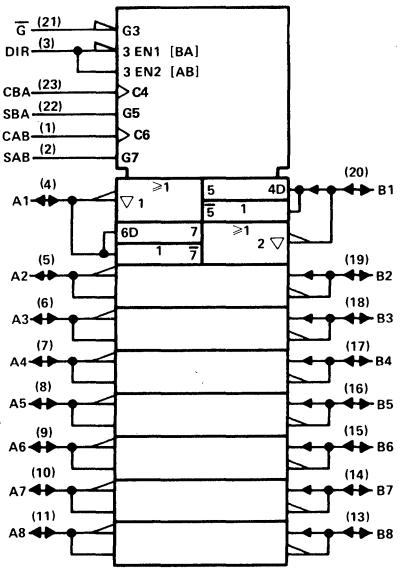
†The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled. i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡

'HC646



'HC648

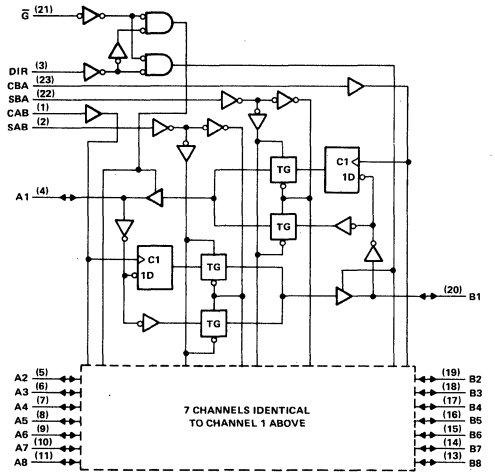


‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

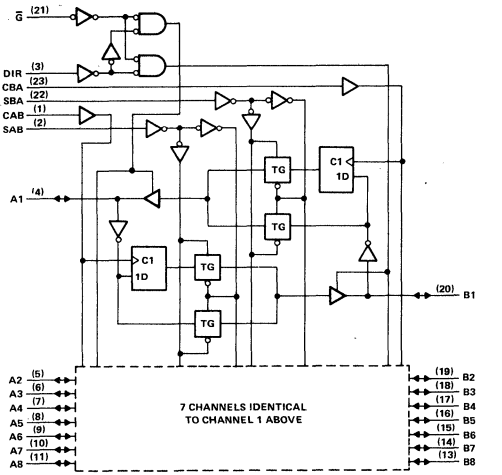
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'HC646



'HC648



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HC646 SN54HC648			SN74HC646 SN74HC648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC646 SN54HC648		SN74HC646 SN74HC648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	Control Inputs	V_I = V_{CC} or 0	6 V			±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V			±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i	Control Inputs		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC646 SN54HC648		SN74HC646 SN74HC648		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.3	0	5.5	MHz
		4.5 V	0	31	0	22	0	27	
		6 V	0	36	0	25	0	31	
t_w	Pulse duration, CBA or CAB high or low	2 V	80		115		95		ns
		4.5 V	16		23		19		
		6 V	14		20		16		
t_{su}	Setup time, A before CAB↑ or B before CBA↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, A after CAB↑ or B after CBA↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC646 SN54HC648		SN74HC646 SN74HC648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.4		5.5		MHz
			4.5 V	31	54		22		27		
			6 V	36	64		25		31		
t_{pd}	CBA or CAB	A or B	2 V		65	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		14	31		46		38	
t_{pd}	A or B	B or A	2 V		50	135		205		170	ns
			4.5 V		14	27		41		34	
			6 V		11	23		35		29	
t_{pd}	SBA or SAB†	A or B	2 V		70	190		285		240	ns
			4.5 V		20	38		57		48	
			6 V		16	32		48		41	
t_{en}	$\overline{G}$	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	$\overline{G}$	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{en}	DIR	A or B	2 V		80	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	DIR	A or B	2 V		80	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

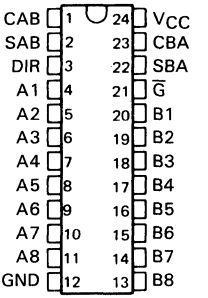
switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC646 SN54HC648		SN74HC646 SN74HC648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CBA or CAB	A or B	2 V		90	265		400		330	ns
			4.5 V		24	53		80		66	
			6 V		20	46		68		57	
t_{pd}	A or B	B or A	2 V		70	220		335		280	ns
			4.5 V		20	44		67		56	
			6 V		15	38		57		49	
t_{pd}	SBA or SAB†	A or B	2 V		80	275		415		345	ns
			4.5 V		24	55		83		69	
			6 V		20	47		70		60	
t_{en}	$\overline{G}$	A or B	2 V		113	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t_{en}	DIR	A or B	2 V		113	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		43	

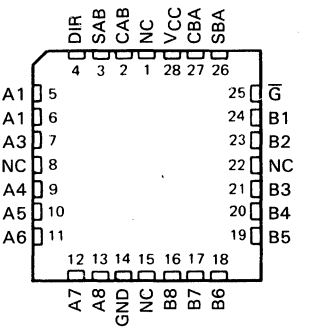
NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

- **Inputs are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT' . . . JT PACKAGE
SN74HCT' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

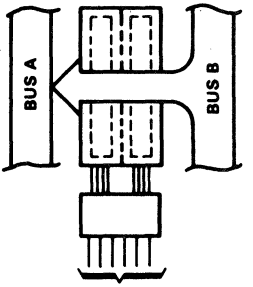
description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HCT646 or 'HCT648.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

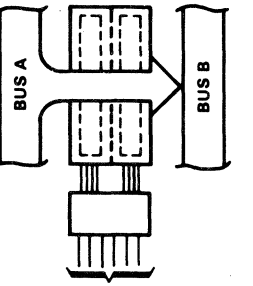
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54HCT' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT' family is characterized for operation from −40°C to 85°C.



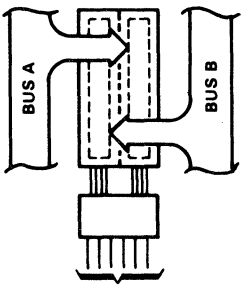
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



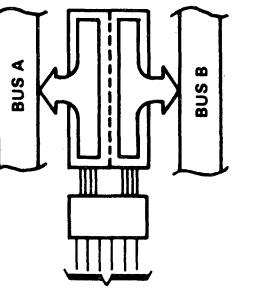
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A OR B

Pin numbers shown are for DW, JT, and NT packages.

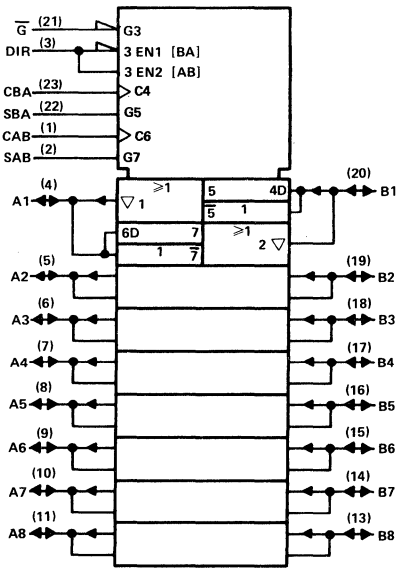
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HCT646	'HCT648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

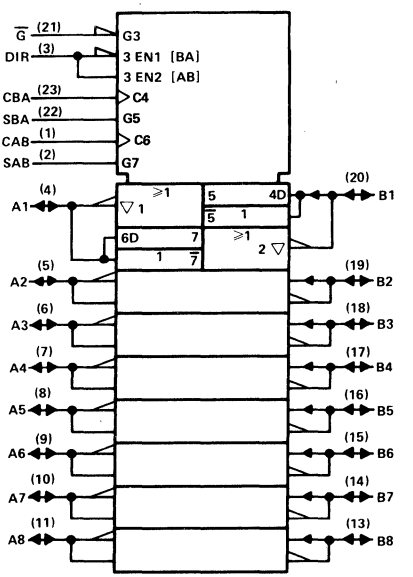
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡

'HCT646



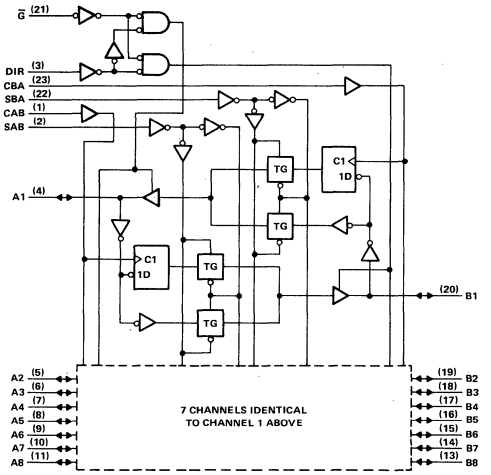
'HCT648



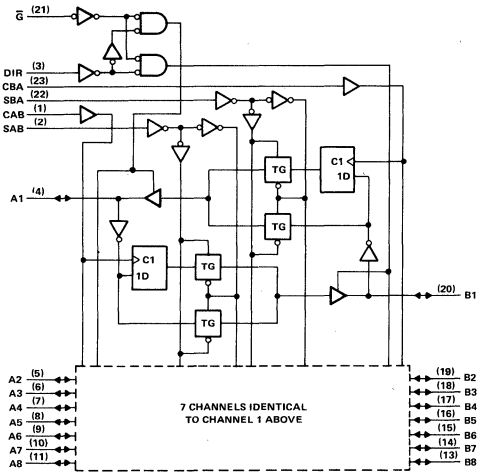
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'HCT646



'HCT648



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT646 SN54HCT648			SN74HCT646 SN74HCT648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	Control Inputs	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i	Control Inputs		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	31	0	22	0	27	MHz
		5.5 V	0	36	0	24	0	29	
t_w	Pulse duration, CBA or CAB high or low	4.5 V	16		23		19		ns
		5.5 V	14		21		17		
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t_h	Hold time, A after CAB↑ or B after CBA↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	54		22		27		MHz
			5.5 V	36	64		24		29		
t_{pd}	CBA or CAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
t_{pd}	A or B	B or A	4.5 V		14	27		41		34	ns
			5.5 V		12	24		37		31	
t_{pd}	SBA or SAB†	A or B	4.5 V		20	38		57		48	ns
			5.5 V		17	34		51		43	
t_{en}	$\overline{G}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{en}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

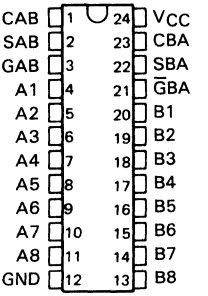
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CBA or CAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		52		60	
t_{pd}	A or B	B or A	4.5 V		22	44		67		55	ns
			5.5 V		20	39		60		50	
t_{pd}	SBA or SAB†	A or B	4.5 V		26	55		83		69	ns
			5.5 V		24	49		74		62	
t_{en}	$\overline{G}$	A or B	4.5 V		33	66		100		87	ns
			5.5 V		22	59		90		74	
t_{en}	DIR	A or B	4.5 V		33	66		100		87	ns
			5.5 V		22	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

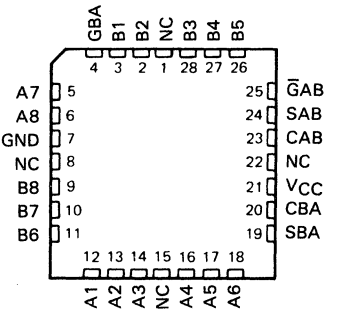
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Bus Transceivers and Registers**
- **Independent Registers and Enables for A and B Buses**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC651, SN54HC652 . . . JT PACKAGE
SN74HC651, SN74HC652 . . . DW or NT PACKAGE
(TOP VIEW)



SN54HC651, SN54HC652 . . . FK PACKAGE
(TOP VIEW)



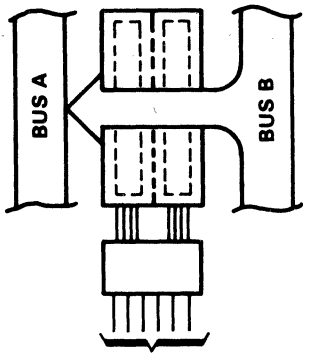
NC—No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HC651 and 'HC652.

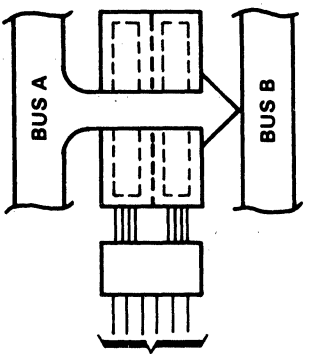
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54HC651 and SN54HC652 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC651 and SN74HC652 are characterized for operation from −40°C to 85°C.



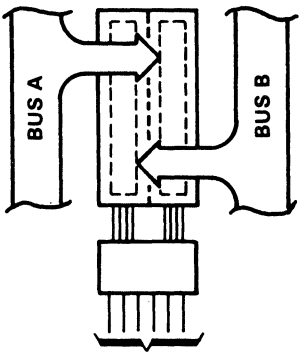
(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



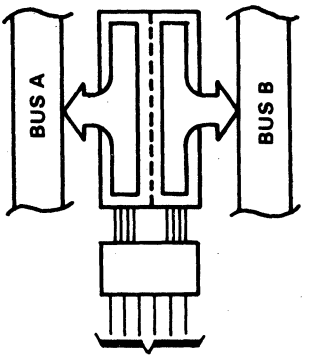
(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

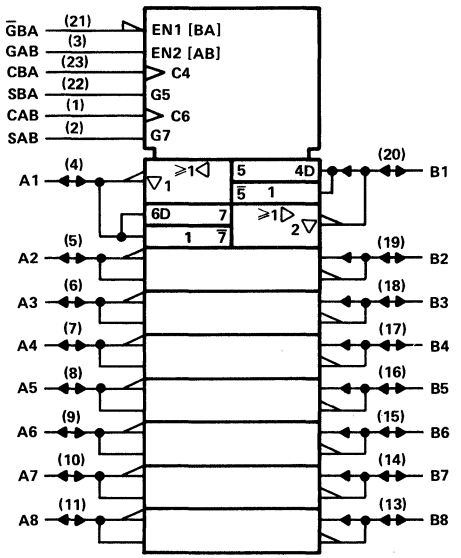
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HC651	'HC652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and	Stored A Data to B Bus and
								Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus

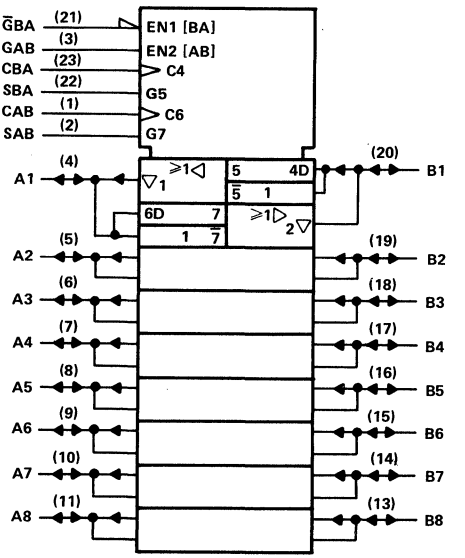
†The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡

'HC651



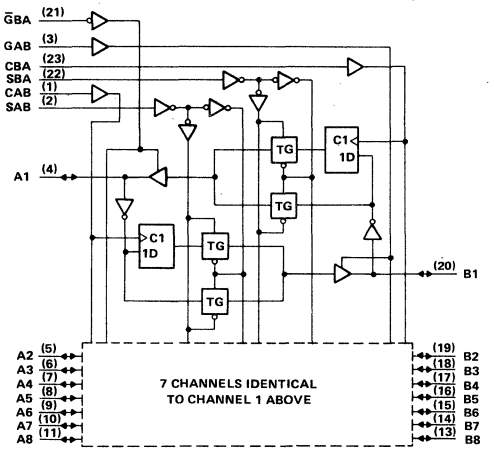
'HC652



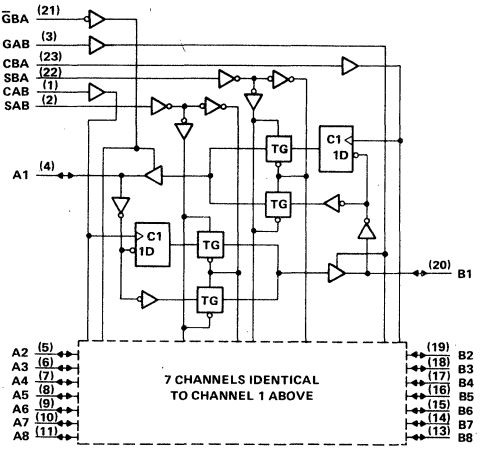
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'HC651



'HC652



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HCT651 SN54HCT652			SN74HCT651 SN74HCT652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	Control Inputs	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i	Control Inputs		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.3	0	5.5	MHz
		4.5 V	0	31	0	22	0	27	
		6 V	0	36	0	25	0	31	
t_w	Pulse duration, CBA or CAB high or low	2 V	80		115		95		ns
		4.5 V	16		23		19		
		6 V	14		20		16		
t_{su}	Setup time, A before CAB↑ or B before CBA↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, A after CAB↑ or B after CBA↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.3		5.5		MHz
			4.5 V	31	40		22		27		
			6 V	36	45		25		31		
t_{pd}	CBA or CAB	A or B	2 V		65	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		14	31		46		38	
t_{pd}	A or B	B or A	2 V		50	135		205		170	ns
			4.5 V		14	27		41		34	
			6 V		11	23		35		29	
t_{pd}	SBA or SAB†	A or B	2 V		70	190		285		240	ns
			4.5 V		20	38		57		48	
			6 V		16	32		48		41	
t_{en}	$\overline{G}$BA or GAB	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	$\overline{G}$BA or GAB	A or B	2 V		50	245		370		305	ns
			4.5 V		23	49		74		61	
			6 V		20	42		63		52	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

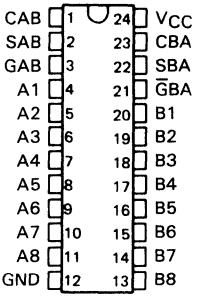
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CBA or CAB	A or B	2 V		90	265		400		330	ns
			4.5 V		24	53		80		66	
			6 V		18	46		68		57	
t_{pd}	A or B	B or A	2 V		70	220		335		275	ns
			4.5 V		20	44		70		55	
			6 V		15	38		57		48	
t_{pd}	SBA or SAB†	A or B	2 V		80	275		415		345	ns
			4.5 V		24	55		83		69	
			6 V		20	47		70		60	
t_{en}	$\overline{G}$BA or GAB	A or B	2 V		100	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		43	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

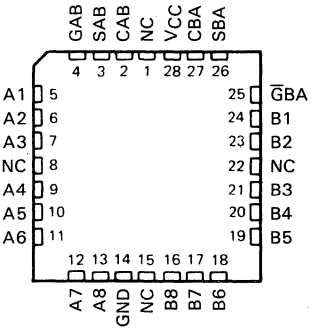
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- Bus Transceivers and Registers
- Independent Registers and Enables for A and B Buses
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HCT651, SN54HCT652 . . . JT PACKAGE
SN74HCT651, SN74HCT652 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT651, SN54HCT652 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

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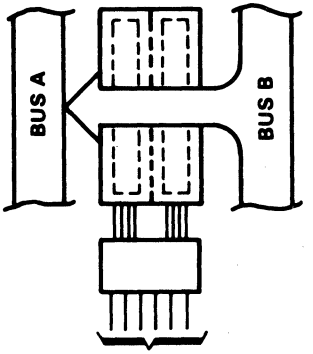
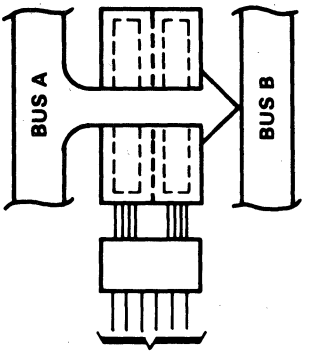
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{G}}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54HCT651 and SN54HCT652 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT651 and SN74HCT652 are characterized for operation from −40°C to 85°C.



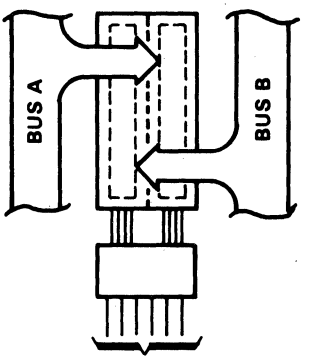
(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



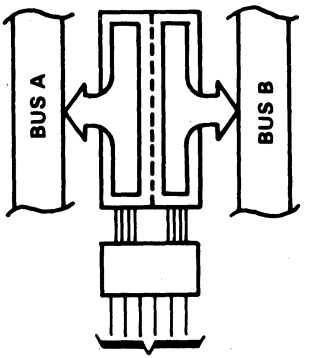
(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



(3) GAB	(21) $\overline{G}$BA	(1) CAB	(23) CBA	(2) SAB	(22) SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

Pin numbers shown are for DW, JT, and NT packages.

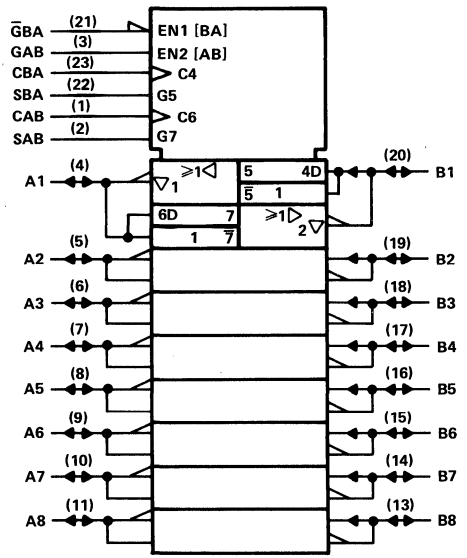
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HCT651	'HCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and	Stored A Data to B Bus and
								Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus

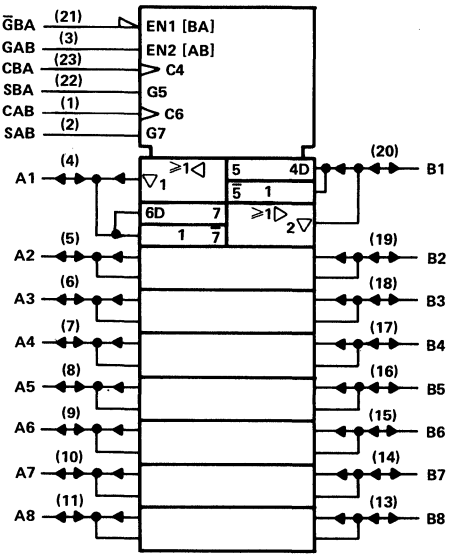
†The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡

'HCT651



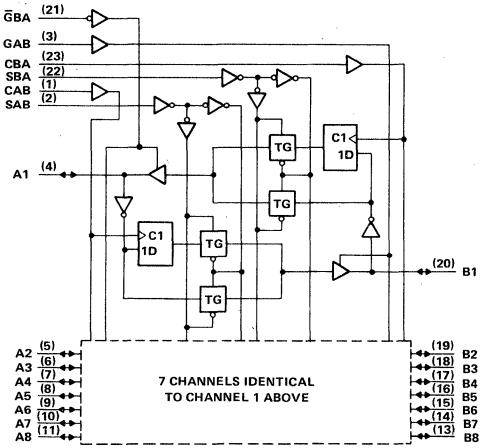
'HCT652



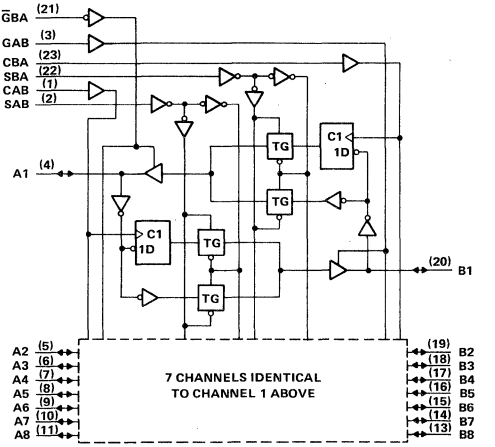
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'HCT651



'HCT652



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT651 SN54HCT652			SN74HCT651 SN74HCT652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	Control Inputs	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL} Data = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i	Control Inputs		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	25	0	17	0	20	MHz
		5.5 V	0	28	0	19	0	22	
t_w	Pulse duration, CBA or CAB high or low	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t_{su}	Setup time, A before CAB↑ or B before CBA↑	4.5 V	15		23		19		ns
		5.5 V	14		21		17		
t_h	Hold time, A after CAB↑ or B after CBA↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	25	35		17		20		MHz
			5.5 V	28	40		19		22		
t_{pd}	CBA or CAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
t_{pd}	A or B	B or A	4.5 V		14	27		41		34	ns
			5.5 V		12	24		37		31	
t_{pd}	SBA or SAB†	A or B	4.5 V		20	38		57		48	ns
			5.5 V		17	34		51		43	
t_{en}	$\overline{G}$BA or GAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	$\overline{G}$BA or GAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CBA or CAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		72		60	
t_{pd}	A or B	B or A	4.5 V		22	44		70		55	ns
			5.5 V		20	39		60		50	
t_{pd}	SBA or SAB†	A or B	4.5 V		26	55		83		69	ns
			5.5 V		24	49		74		62	
t_{en}	$\overline{G}$BA or GAB	A or B	4.5 V		33	66		100		82	ns
			5.5 V		30	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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D2839, MARCH 1984—REVISED SEPTEMBER 1987

- **Bus Transceivers with Inverting Outputs ('HC658) or True Outputs ('HC659)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

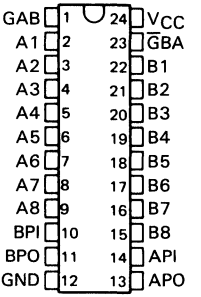
description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control inputs, GAB and $\overline{GBA}$. These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

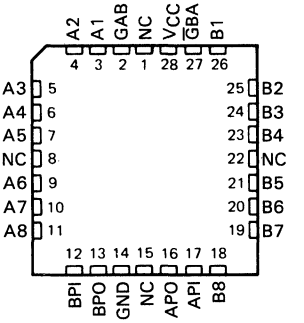
The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits. For futher information, see Typical Application Data.

The SN54HC658 and SN54HC659 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC658 and SN74HC659 are characterized for operation from −40°C to 85°C.

SN54HC658, SN54HC659 . . . JT PACKAGE
SN74HC658, SN74HC659 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC658, SN54HC659 . . . FK PACKAGE
(TOP VIEW)



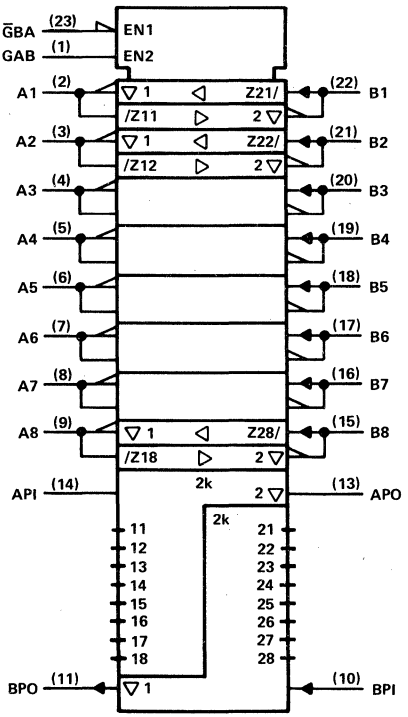
NC—No internal connection

FUNCTION TABLE

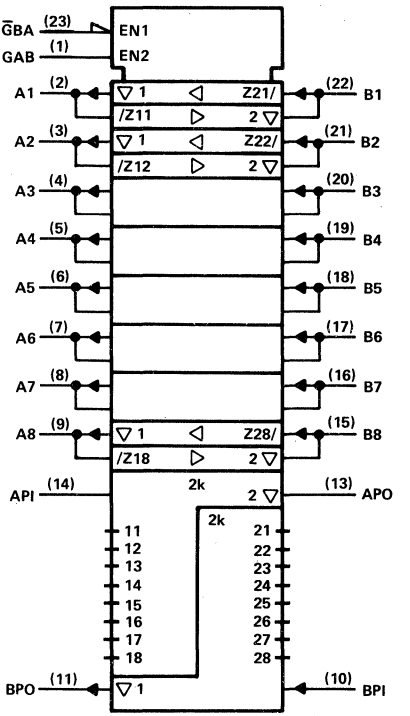
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{GBA}$	GAB			APO	BPO	'HC658	'HC659
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
L	H	X	0, 2, 4, 6, 8		H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus
		X	1, 3, 5, 7, 9		L		
		0, 2, 4, 6, 8	X	H			
		1, 3, 5, 7, 9	X	L			

logic symbols†

'HC658



'HC659



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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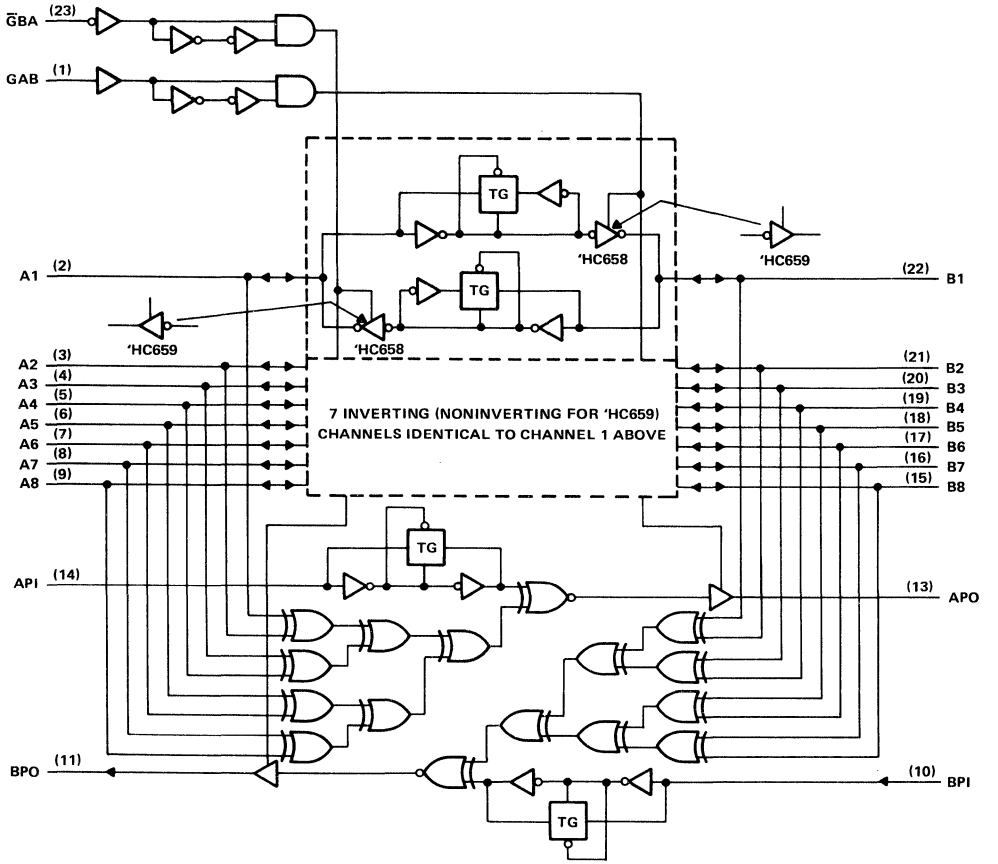
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC658 SN54HC659			SN74HC658 SN74HC659			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC658 SN54HC659		SN74HC658 SN74HC659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
V_{OH}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
V_{OL}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	GAB, $\overline{G}$BA, API or BPI	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i†			2 to 6 V		3	10		10		10	pF

†This parameter, C_i, does not apply to transceiver I/O ports.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC658		SN74HC658		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	2 V		117	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	40		60		50	
t_{dis}	GAB or $\overline{G}$BA	APO or BPO	2 V		117	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	40		60		50	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC658		SN74HC658		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		117	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	41		60		51	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	2 V		160	320		485		400	ns
			4.5 V		32	64		97		80	
			6 V		27	55		82		69	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC659		SN74HC659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		70	140		210		175	ns
			4.5 V		14	28		42		35	
			6 V		12	24		36		30	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	2 V		117	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	40		60		50	
t_{dis}	GAB or $\overline{G}$BA	APO or BPO	2 V		117	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	40		60		50	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC659		SN74HC659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		117	225		340		280	ns
			4.5 V		23	45		68		56	
			6 V		20	39		58		49	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	2 V		160	320		485		400	ns
			4.5 V		32	64		97		80	
			6 V		27	55		82		69	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION DATA

The unique structure used on the I/O ports and the parity inputs of these devices deserves some special consideration (see Figure 1). Only the input structure is shown. The conventional 3-state output structure associated with each I/O port has been omitted to facilitate understanding.

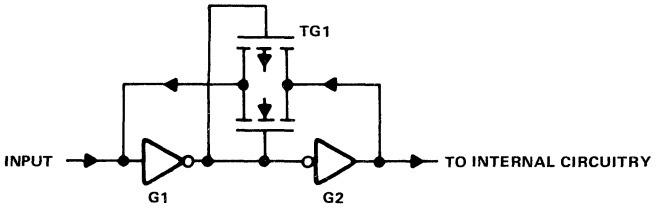

FIGURE 1: INPUT STRUCTURE

The two inverters (G1 and G2) have a transmission gate (TG1) connected in a feedback loop around them. This transmission gate is connected in an unusual fashion, that is, with the gates of both transistors connected to the output of G1. Thus, with the output of G1 at either a high or a low level, one or the other of the transistors will be turned on allowing feedback of the output of G2 to the input of G1. The effect of TG1 is that the input level will be maintained at whatever level existed prior to the bus being disabled or the level currently existing on the bus will be reinforced.

To understand the operation of this input, assume that initially the input is at a low logic level. As the input voltage is raised, TG1 sinks current to attempt to maintain the low level. However, TG1 consists of small geometry transistors and appears resistive as current flows thus allowing the input voltage to rise toward the threshold voltage of G1. When the threshold voltage is reached, G1 changes state causing G2 to change state. G2 then attempts to maintain a high level on the input through TG1. A similar operation occurs when the input voltage is decreased toward the threshold voltage of G1. G2 sources current through TG1 until the threshold is reached.

This characteristic of the input stage has some implications for the input current levels. With the input held at either V_{CC} or GND, there is no voltage across TG1 and negligible input current. However, as the input voltage is raised from GND or lowered from V_{CC}, the input current rises as the voltage across TG1 increases. The input current continues to rise until it reaches a maximum just as the threshold voltage of G1 is reached.

This configuration provides for minimum power dissipation when the bus is inactive (all outputs on the bus in the high-impedance state) and minimum susceptibility to noise on the bus during this time. The increase in input current may go unnoticed as it only occurs during transitions on the bus. Care must be taken when measuring input currents (e.g., at incoming inspection) to ensure that the input voltage is set to the correct value.

The use of these devices for interfacing to 8-, 16-, and 24-bit-wide memory arrays with parity is illustrated in Figures 2, 3 and 4.

TYPICAL APPLICATION DATA

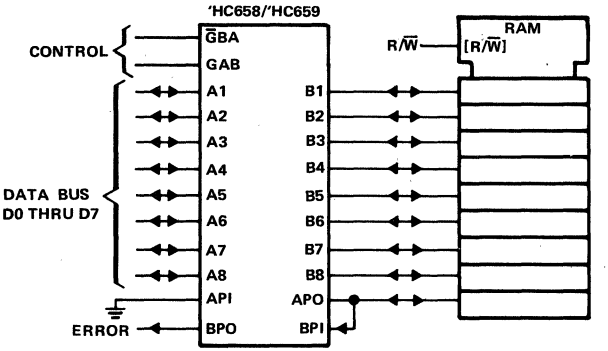

FIGURE 2. 8-BIT-WIDE MEMORY ARRAY WITH PARITY

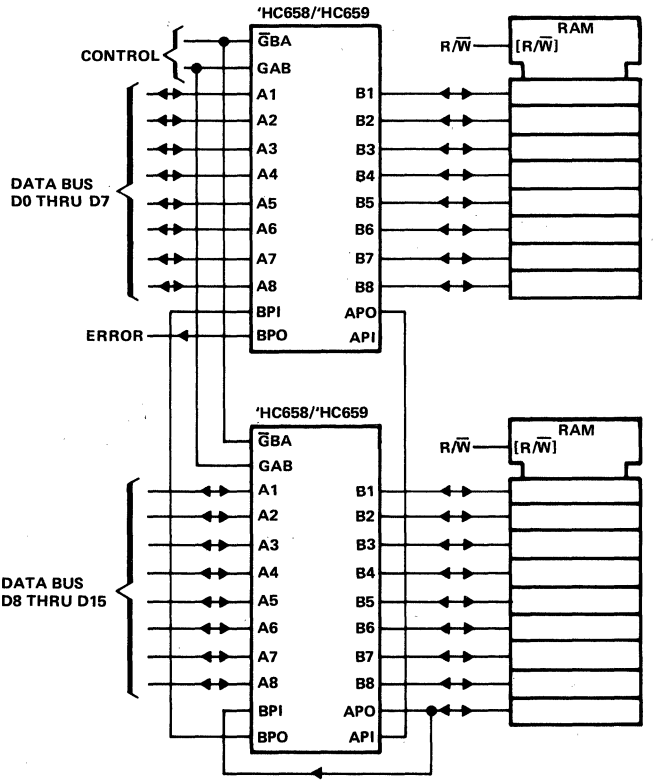

FIGURE 3. 16-BIT-WIDE MEMORY ARRAY WITH PARITY

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TYPICAL APPLICATION DATA

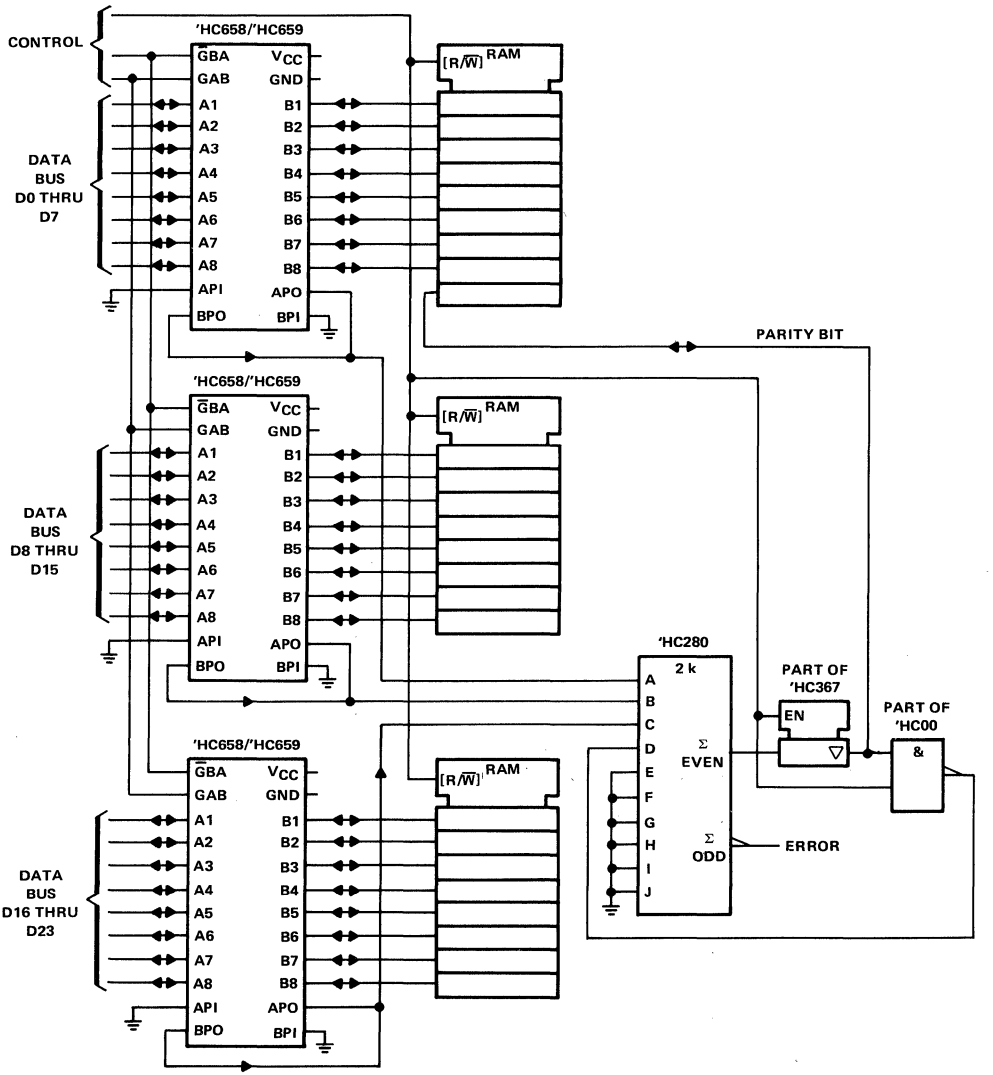

FIGURE 4. 24-BIT-WIDE MEMORY ARRAY WITH PARITY

NOTE: The 'HC280 eliminates ripple carry delays associated with Figures 2 and 3. However, in those two cases the delays are probably too small to be of concern.

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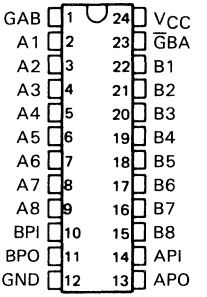
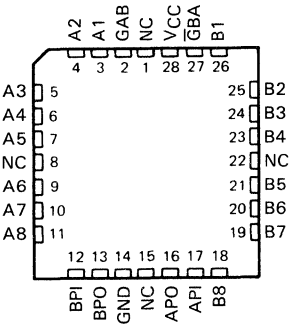
- Inputs are TTL-Voltage Compatible
- Bus Transceivers with Inverting Outputs ('HCT658) or True Outputs ('HCT659)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HCT658, SN54HCT659 . . . JT PACKAGE
SN74HCT658, SN74HCT659 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT658, SN54HCT659 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and $\overline{GBA}$. These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits. For futher information, see Typical Application Data in 'HC658 series data sheet.

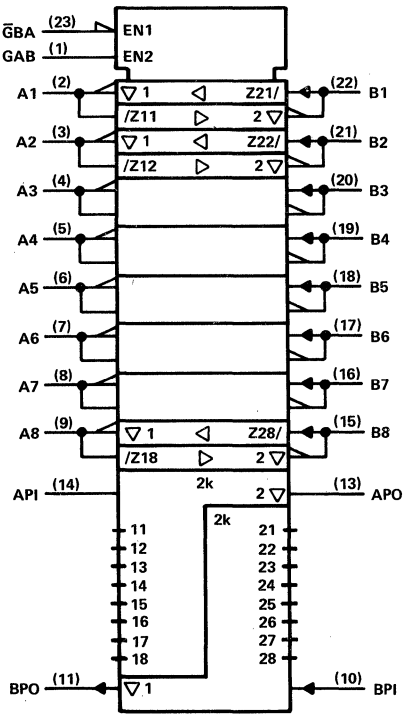
The SN54HCT658 and SN54HCT659 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT658 and SN74HCT659 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

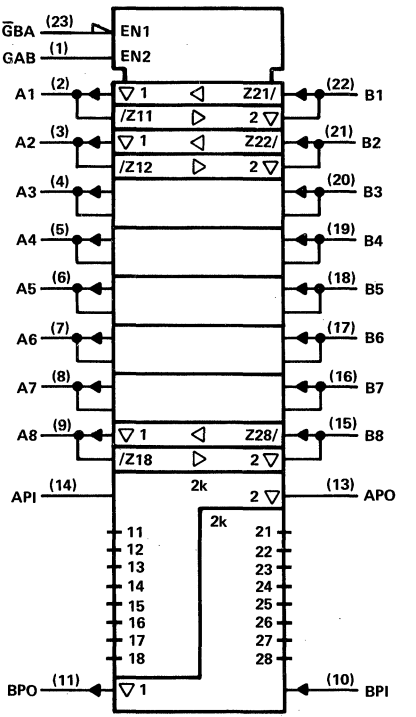
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\overline{GBA}$	GAB			APO	BPO	'HCT658	'HCT659
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
L	H	X	0, 2, 4, 6, 8		H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus
		X	1, 3, 5, 7, 9		L		
		0, 2, 4, 6, 8	X	H			
		1, 3, 5, 7, 9	X	L			

logic symbols†

'HCT658



'HCT659



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

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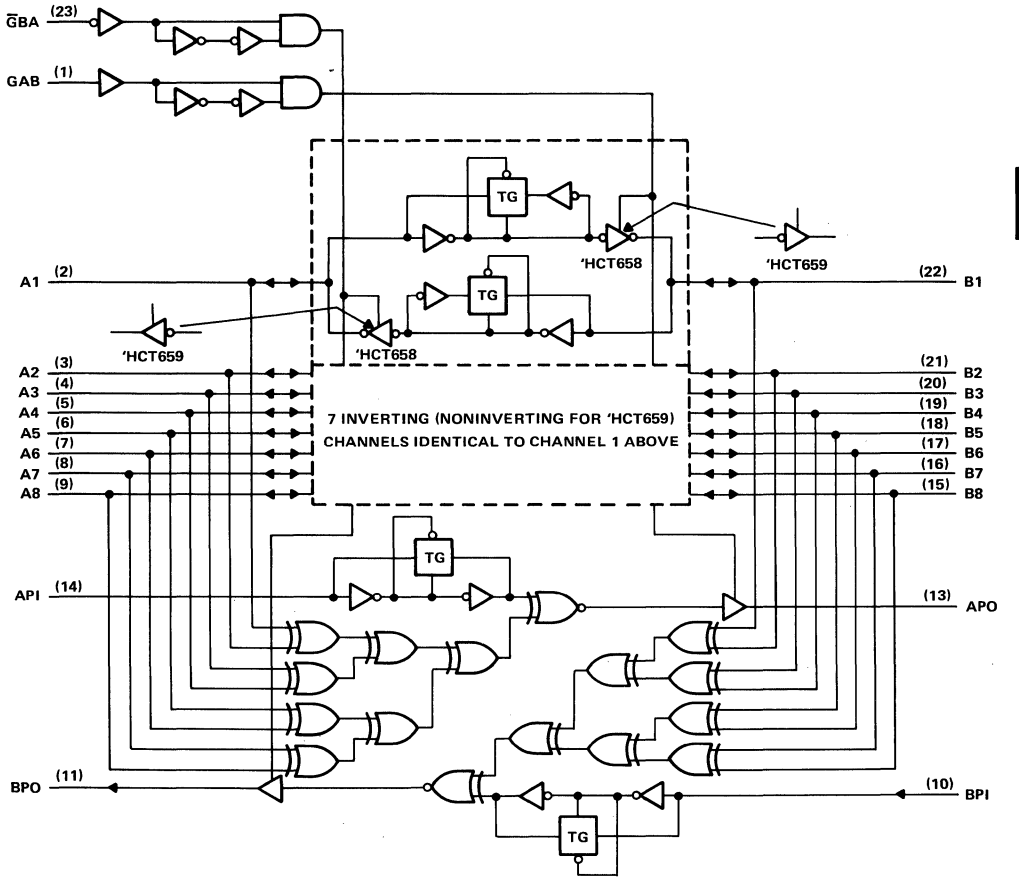
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT658 SN54HCT659			SN74HCT658 SN74HCT659			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT658 SN54HCT659		SN74HCT658 SN74HCT659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
V_{OH}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		V
V_{OH}	APO and BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		V
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
V_{OL}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	V
V_{OL}	APO and BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	V
I_I	GAB, $\overline{GBA}$, API OR BPI	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i‡			4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
‡This parameter, C_i, does not apply to I/O ports.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT658		SN74HCT658		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	30		45		38	ns
			5.5 V		13	27		41		34	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		24	47		71		59	ns
			5.5 V		21	42		64		53	
t_{dis}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		24	47		71		59	ns
			5.5 V		21	42		64		53	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT658		SN74HCT658		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		23	47		71		59	ns
			5.5 V		21	42		64		53	
t_{pd}	A or B	APO or BPO	4.5 V		31	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		32	64		97		80	ns
			5.5 V		28	57		87		72	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC658 series data sheet.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT659		SN74HCT659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		14	28		61		50	ns
			5.5 V		12	25		42		35	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		24	47		71		59	ns
			5.5 V		21	42		64		53	
t_{dis}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		24	47		71		59	ns
			5.5 V		21	42		64		53	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT659		SN74HCT659		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		23	45		84		67	ns
			5.5 V		20	40		68		56	
t_{pd}	A or B	APO or BPO	4.5 V		32	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	GAB or $\overline{G}$BA	APO or BPO	4.5 V		32	64		97		80	ns
			5.5 V		29	57		87		72	
t_t		Any	4.5 V		21	42		63		53	ns
			5.5 V		19	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC658 series data sheet.

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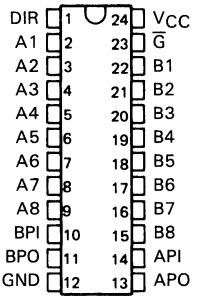
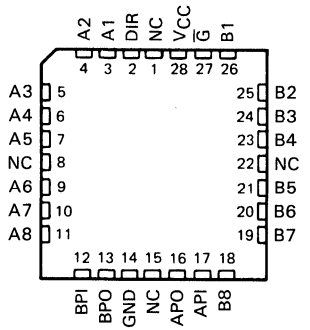
- **Bus Transceivers with Inverting Outputs ('HC664) or True Outputs ('HC665)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC664, SN54HC665 . . . JT PACKAGE
SN74HC664, SN74HC665 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC664, SN54HC665 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input $\overline{G}$, can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry. For futher information, see the Typical Application Data.

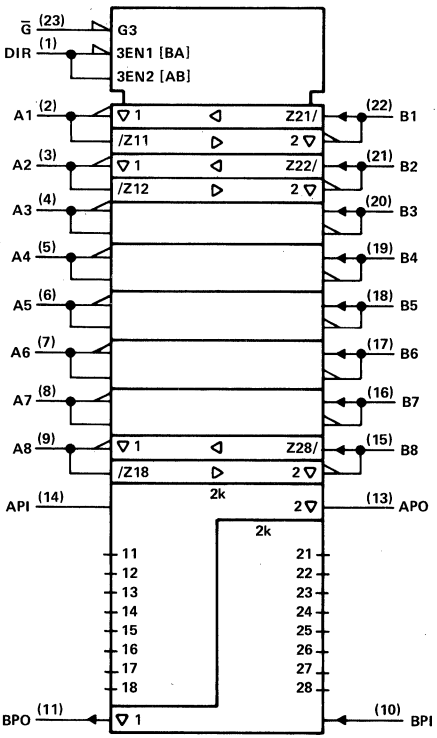
The SN54HC664 and SN54HC665 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC664 and SN74HC665 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

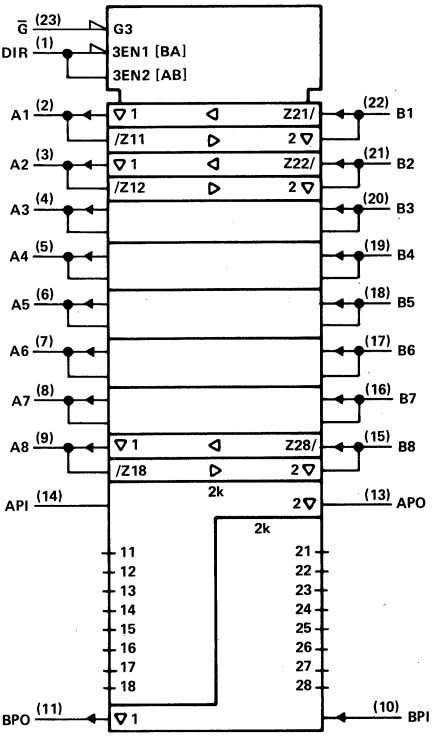
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION	
$\overline{G}$	DIR	A BUS AND API	B BUS AND BPI	APO	BPO	'HC664	'HC665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

logic symbols†

'HC664



'HC665



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
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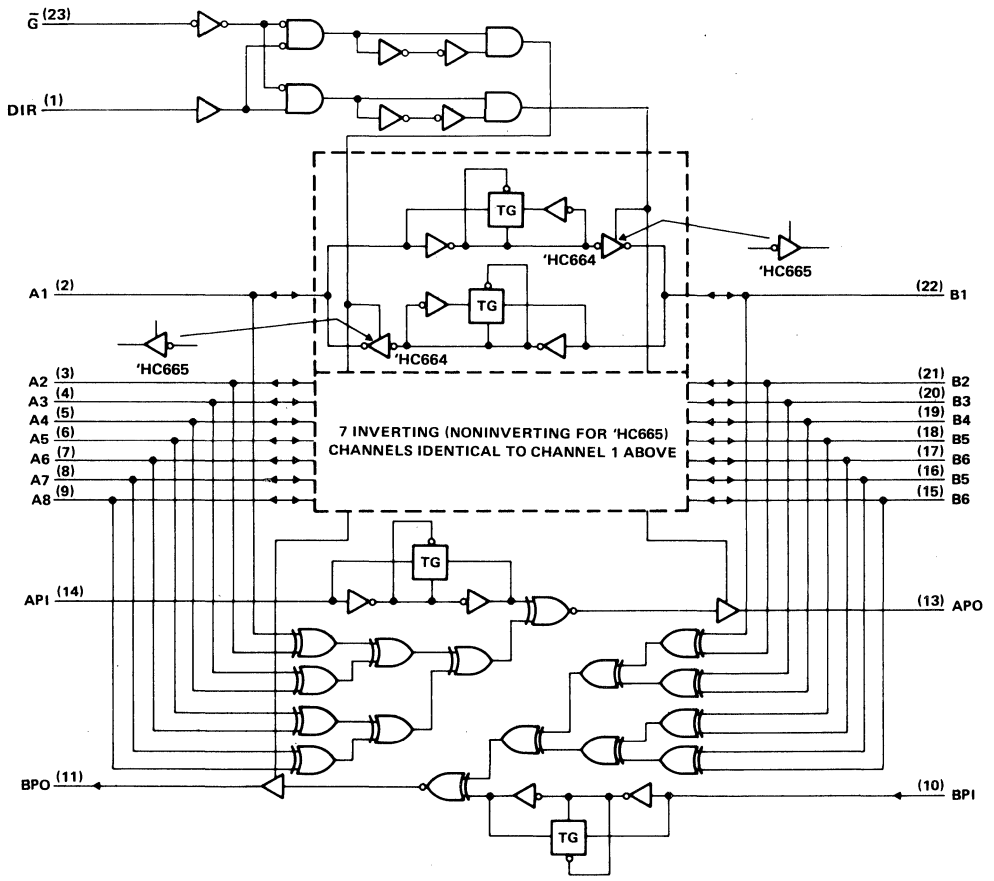
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC664 SN54HC665			SN74HC664 SN74HC665			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC664 SN54HC665		SN74HC664 SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
V_{OH}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
		V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
V_{OL}	All outputs except APO & BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
	APO or BPO	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$\overline{G}$, DIR, API or BPI	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i†			2 to 6 V		3	10		10		10	pF

†This parameter, C_i, does not apply to I/O ports.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC664		SN74HC664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_{dis}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC664		SN74HC664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		116	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	41		60		51	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		170	340		515		425	ns
			4.5 V		34	68		103		85	
			6 V		29	58		87		73	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC665		SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		70	140		210		175	ns
			4.5 V		14	28		42		35	
			6 V		12	24		36		30	
t_{pd}	A or B	APO or BPO	2 V		115	230		345		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		59		49	
t_{pd}	API or BPI	APO or BPO	2 V		77	155		235		195	ns
			4.5 V		15	31		47		39	
			6 V		13	26		40		33	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_{dis}	$\overline{G}$ or DIR	A or B	2 V		125	255		385		320	ns
			4.5 V		25	51		77		64	
			6 V		22	43		65		54	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	56 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC665		SN74HC665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		112	225		340		280	ns
			4.5 V		22	45		68		56	
			6 V		20	39		58		49	
t_{pd}	A or B	APO or BPO	2 V		157	315		475		395	ns
			4.5 V		31	63		95		79	
			6 V		27	54		81		68	
t_{pd}	API or BPI	APO or BPO	2 V		120	240		365		300	ns
			4.5 V		24	48		73		60	
			6 V		20	41		62		52	
t_{en}	$\overline{G}$ or DIR	A or B	2 V		170	340		515		425	ns
			4.5 V		34	68		103		85	
			6 V		29	58		87		73	
t_t		Any	2 V		37	210		315		265	ns
			4.5 V		12	42		63		53	
			6 V		10	36		53		45	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The unique structure used on the I/O ports and the parity inputs of these devices deserves some special consideration (see Figure 1). Only the input structure is shown. The conventional 3-state output structure associated with each I/O port has been omitted to facilitate understanding.

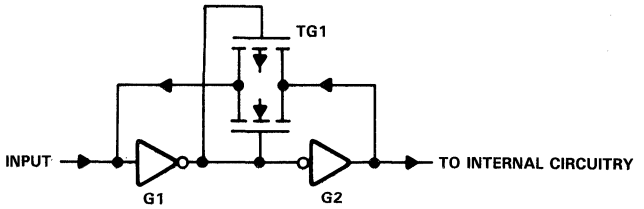

FIGURE 1. INPUT STRUCTURE

The two inverters (G1 and G2) have a transmission gate (TG1) connected in a feedback loop around them. This transmission gate is connected in an unusual fashion, that is, with the gates of both transistors connected to the output of G1. Thus, with the output of G1 at either a high or a low level, one or the other of the transistors will be turned on allowing feedback of the output of G2 to the input of G1. The effect of TG1 is that the input level will be maintained at whatever level existed prior to the bus being disabled or the level currently existing on the bus will be reinforced.

To understand the operation of this input, assume that initially the input is at a low logic level. As the input voltage is raised, TG1 sinks current to attempt to maintain the low level. However, TG1 consists of small geometry transistors and appears resistive as current flows thus allowing the input voltage to rise toward the threshold voltage of G1. When the threshold voltage is reached, G1 changes state causing G2 to change state. G2 then attempts to maintain a high level on the input through TG1. A similar operation occurs when the input voltage is decreased toward the threshold voltage of G1. G2 sources current through TG1 until the threshold is reached.

This characteristic of the input stage has some implications for the input current levels. With the input held at either V_{CC} or GND, there is no voltage across TG1 and negligible input current. However, as the input voltage is raised from GND or lowered from V_{CC}, the input current rises as the voltage across TG1 increases. The input current continues to rise until it reaches a maximum just as the threshold voltage of G1 is reached.

This configuration provides for minimum power dissipation when the bus is inactive (all outputs on the bus in the high-impedance state) and minimum susceptibility to noise on the bus during this time. The increase in input current may go unnoticed as it only occurs during transitions on the bus. Care must be taken when measuring input currents (e.g., at incoming inspection) to ensure that the input voltage is set to the correct value.

The use of these devices for interfacing to 8-, 16-, 24-bit-wide memory arrays with parity is illustrated in Figures 2, 3 and 4.

TYPICAL APPLICATION DATA

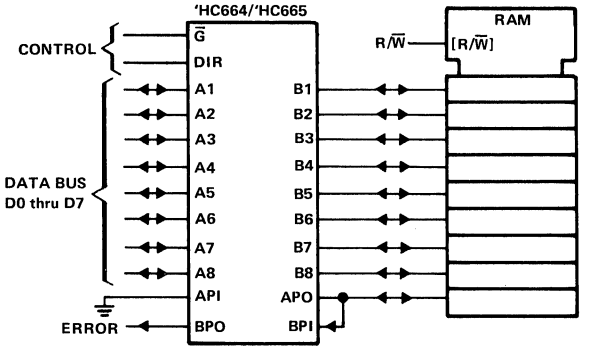

FIGURE 2. 8-BIT-WIDE MEMORY ARRAY WITH PARITY

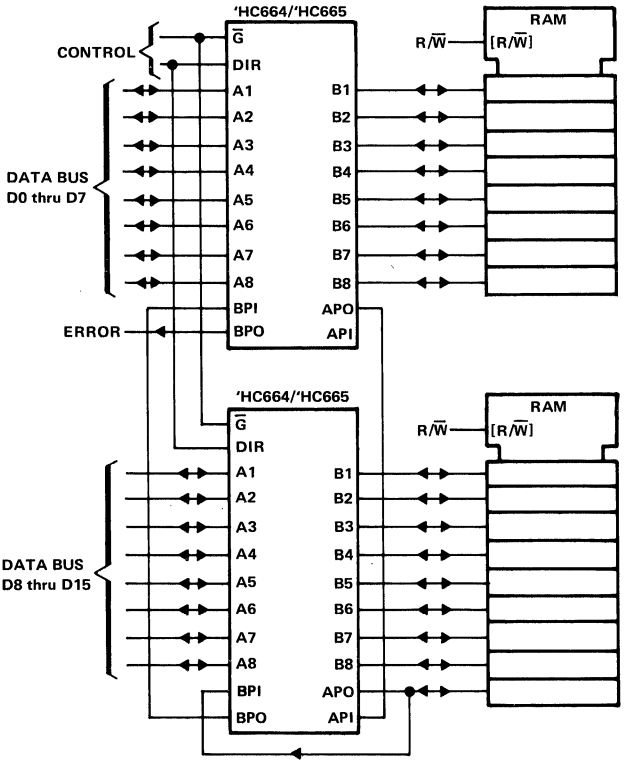

FIGURE 3. 16-BIT-WIDE MEMORY ARRAY WITH PARITY

TYPICAL APPLICATION DATA

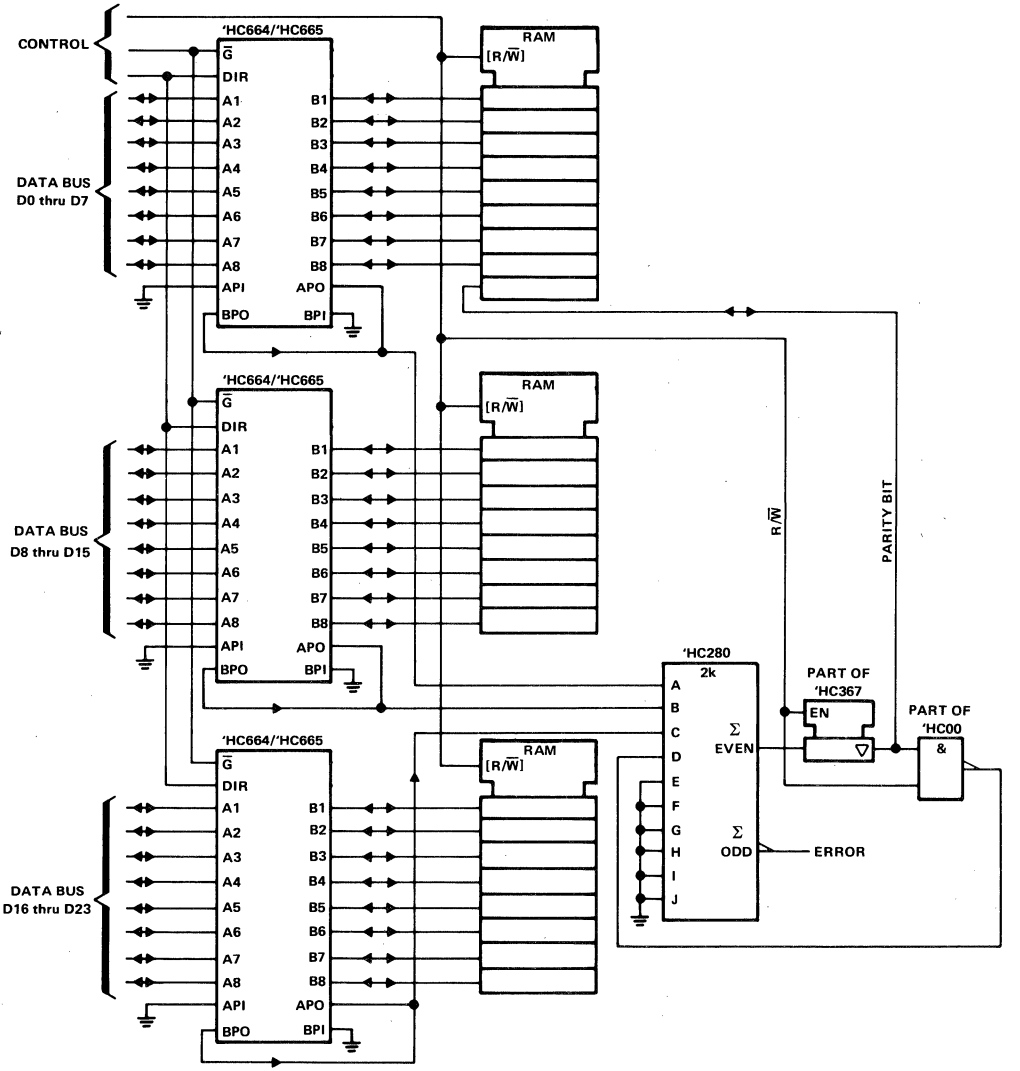

FIGURE 4. 24-BIT-WIDE MEMORY ARRAY WITH PARITY

NOTE: The 'HC280 eliminates ripple carry delays associated with Figures 2 and 3. However, in those two cases the delays are probably too small to be of concern.

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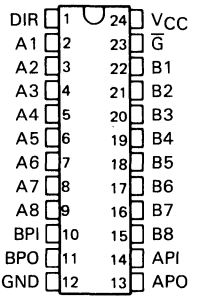
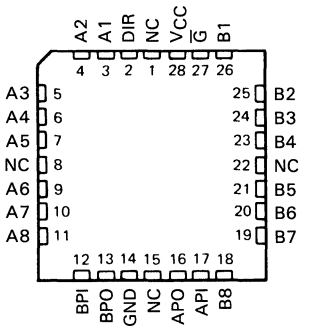
D2839, MARCH 1984—REVISED SEPTEMBER 1987

- **Inputs are TTL-Voltage Compatible**
- **Bus Transceivers with Inverting Outputs ('HCT664) or True Outputs ('HCT665)**
- **Generates a Parity Bit for A Bus and B Bus**
- **Easily Cascadable**
- **Internal Active Pull-Ups and Pull-Downs**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT664, SN54HCT665 . . . JT PACKAGE
SN74HCT664, SN74HCT665 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT664, SN54HCT665 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input, $\overline{G}$, can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry. For further information, see the Typical Application Data on the 'HC664, and 'HC665 data sheet.

The input threshold voltages on these devices are adjusted to be TTL compatible, allowing direct interface to TTL levels on the bus or to memories with TTL output voltage levels.

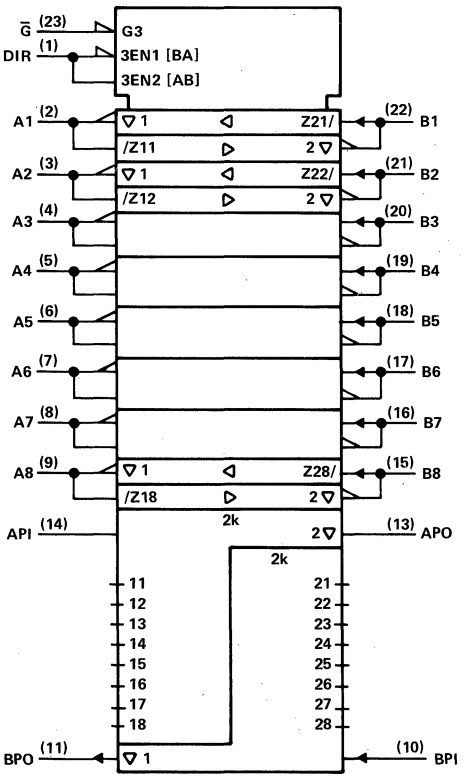
The SN54HCT664 and SN54HCT665 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT664 and SN74HCT665 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

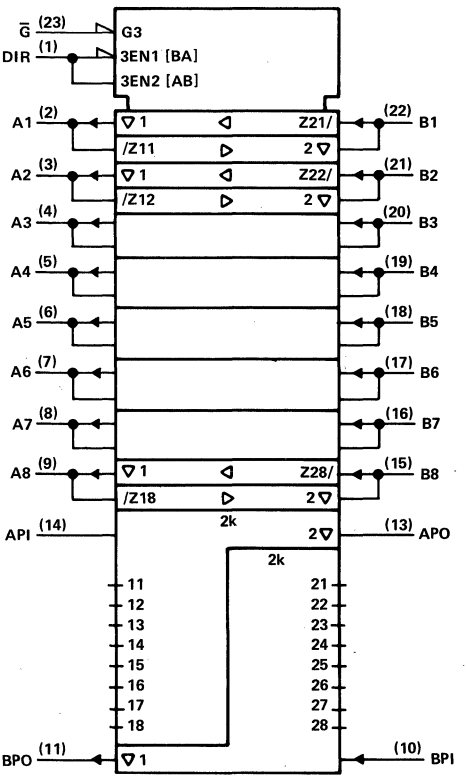
CONTROL INPUTS		NUMBER OF HIGH INPUTS ON	NUMBER OF HIGH INPUTS ON	OUTPUTS		OPERATION	
$\overline{G}$	DIR	B BUS AND BPI	A BUS AND API	APO	BPO	'HCT664	'HCT665
L	L	X	0, 2, 4, 6, 8	Z	H	$\overline{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\overline{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

logic symbols†

'HCT664



'HCT665



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
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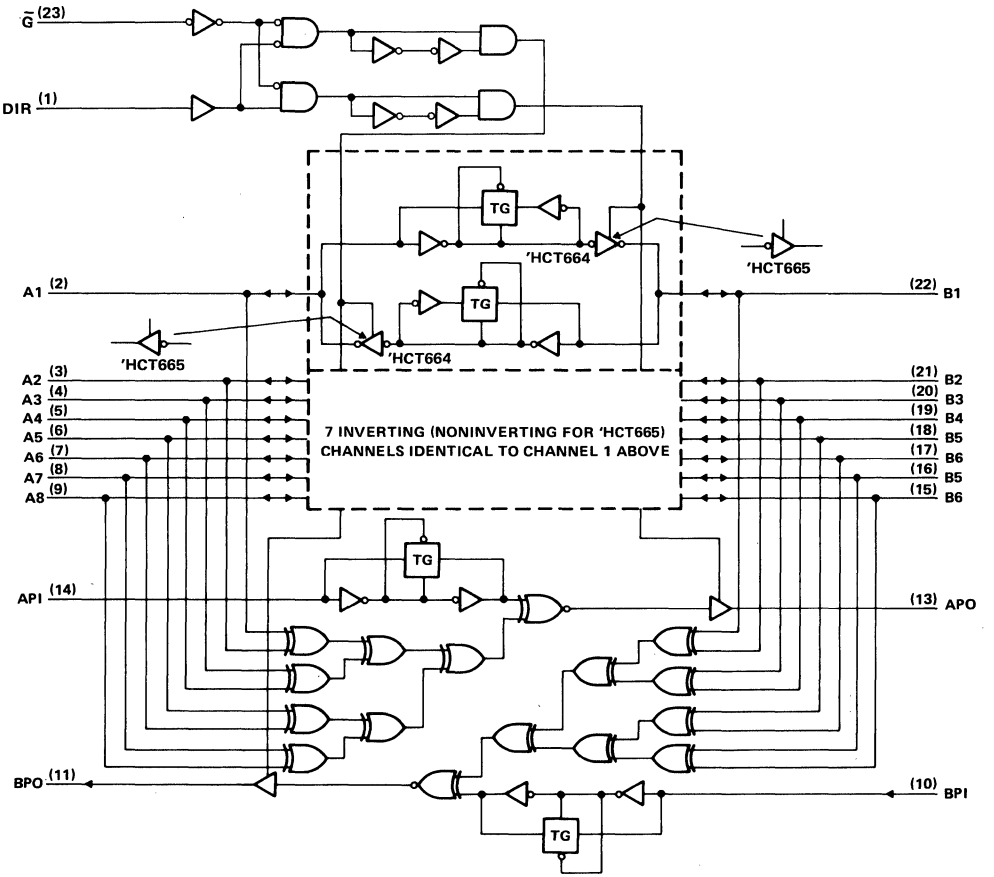
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HCT664 SN54HCT665			SN74HCT664 SN74HCT665			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT664 SN54HCT665		SN74HCT664 SN74HCT665		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i§		4.5 to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
§ This parameter, C_i, does not apply to I/O ports.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT664		SN74HCT664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	30		45		38	ns
			5.5 V		13	27		41		34	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{en}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT664		SN74HCT664		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		23	47		71		59	ns
			5.5 V		21	42		64		53	
t_{pd}	A or B	APO or BPO	4.5 V		31	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	$\overline{G}$	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_{en}	DIR	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC664 series data sheet.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT665		SN74HCT665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		14	28		61		50	ns
			5.5 V		12	25		42		35	
t_{pd}	A or B	APO or BPO	4.5 V		23	46		69		58	ns
			5.5 V		20	41		62		52	
t_{pd}	API or BPI	APO or BPO	4.5 V		15	31		47		39	ns
			5.5 V		14	28		42		35	
t_{en}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{en}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_{dis}	DIR	A or B	4.5 V		25	51		77		64	ns
			5.5 V		23	46		69		58	
t_t		Any	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	62 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT665		SN74HCT665		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		22	45		84		69	ns
			5.5 V		20	40		68		56	
t_{pd}	A or B	APO or BPO	4.5 V		31	63		95		79	ns
			5.5 V		28	56		85		71	
t_{pd}	API or BPI	APO or BPO	4.5 V		24	48		73		60	ns
			5.5 V		21	43		65		54	
t_{en}	$\overline{G}$	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_{en}	DIR	A or B	4.5 V		34	68		103		85	ns
			5.5 V		30	61		92		77	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

For typical application data and a description of the unique input structure, see the 'HC664 series data sheet.

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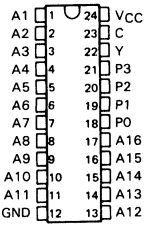
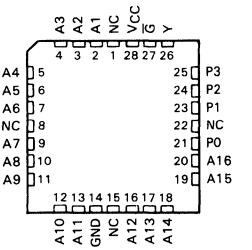
D2833, MARCH 1984—REVISED SEPTEMBER 1987

- **'HC677 is a 16-Bit Address Comparator with Enable**
- **'HC678 is a 16-Bit Address Comparator with Latch**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

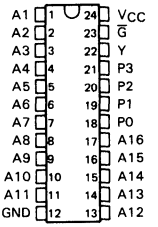
SN54HC677 . . . JT PACKAGE
SN74HC677 . . . DW OR NT PACKAGE
(TOP VIEW)



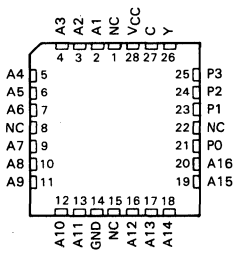
SN54HC677 . . . FK PACKAGE
(TOP VIEW)



SN54HC678 . . . JT PACKAGE
SN74HC678 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC678 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'HC677 and 'HC678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'HC677 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'HC678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

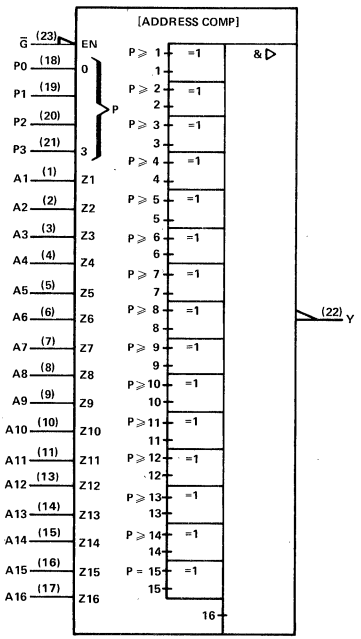
The SN54HC677 and SN54HC678 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC677 and SN74HC678 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

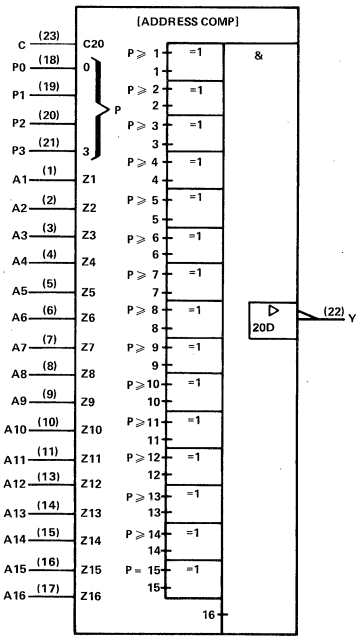
'HC677	'HC678	INPUTS COMMON TO 'HC677 AND 'HC678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		'HC677: Any combination																				H
	L	'HC678: Any combination																				Latched

logic symbols†

'HC677



'HC678



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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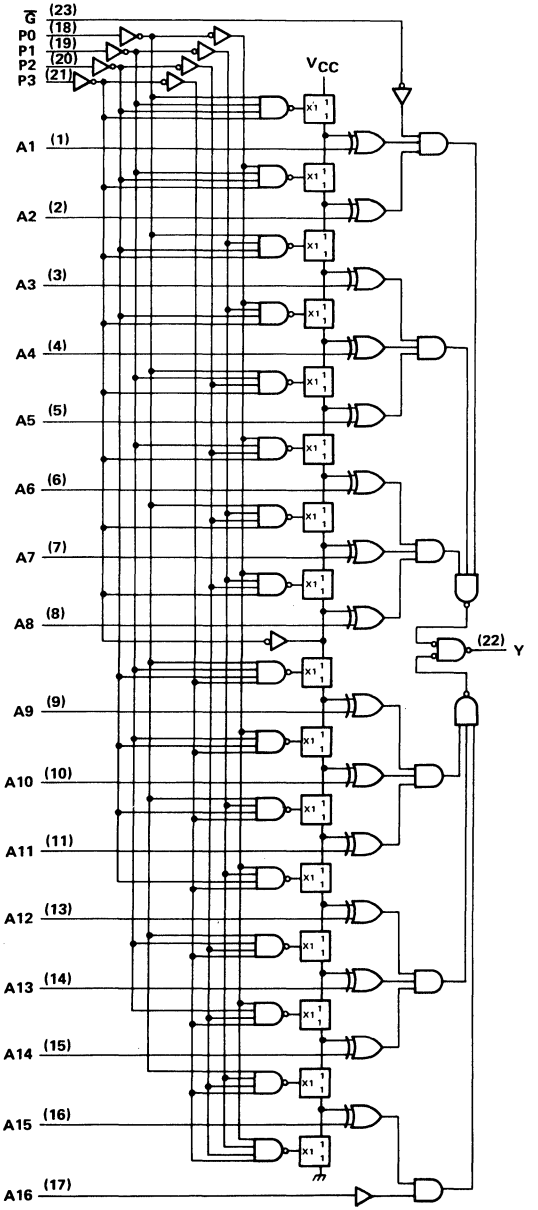
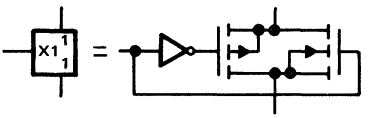
'HC677 logic diagram (positive logic)

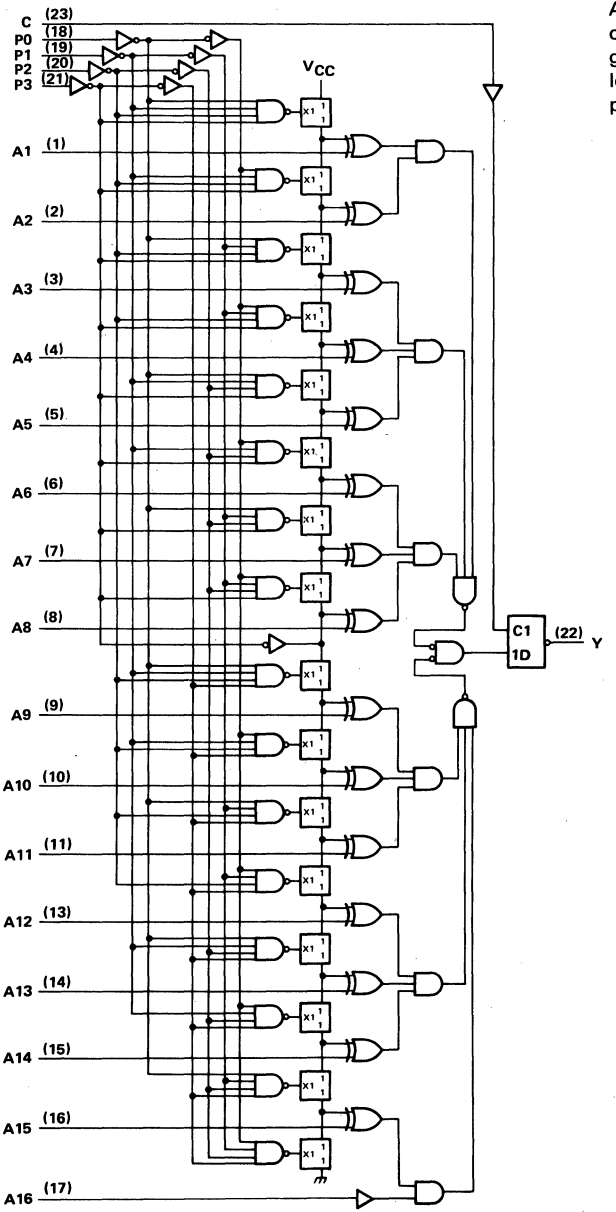


Pin numbers shown are for DW, JT, and NT packages.

In order to understand the implementation of this device, it is essential that the function of the vertical string of transmission gates be understood. A schematic of one of these gates is shown below. If the input to the transmission gate labeled "X1" is high, then the transmission path between the two ports labeled "1" is on. If the "X1" input is low, then the transmission path between the two ports labeled "1" is off. Only one of the 16 transmission gates can be off while the device is operating; which one is off is determined by inputs P0 through P3. The lines going from the string of transmission gates to the exclusive-OR gates located above the transmission gate that is off will be high. The lines going to the exclusive-OR gates located below that transmission gate will be low.



'HC678 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

An explanation of the function of the string of transmission gates appears with the 'HC677 logic diagram on the previous page.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC677 SN54HC678			SN74HC677 SN74HC678			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC677 SN54HC678		SN74HC677 SN74HC678		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC677		SN74HC677		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		130	625		937		781	ns
			4.5 V		50	125		187		156	
			6 V		40	112		169		141	
t_{pd}	Any A	Y	2 V		90	150		225		187	ns
			4.5 V		18	30		45		37	
			6 V		15	27		40		34	
t_{pd}	$\overline{G}$	Y	2 V		70	125		187		156	ns
			4.5 V		14	25		37		31	
			6 V		12	22		33		27	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

timing requirement over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C			SN54HC678		SN74HC678		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	75			112		94		ns
		4.5 V	15			23		19		
		6 V	13			19		16		
t_{su}	Setup time, P0 thru P3 before enable C↓	2 V	500			750		625		ns
		4.5 V	100			150		125		
		6 V	85			128		106		
t_{su}	Setup time, A1 thru A16 before enable C↓	2 V	100			150		125		ns
		4.5 V	20			30		25		
		6 V	18			27		22		
t_h	Hold time, P0 thru P3 or A1 thru A16 after enable C↓	2 V	5			5		5		ns
		4.5 V	5			5		5		
		6 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC678		SN74HC678		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		130	625		937		781	ns
			4.5 V		50	125		187		156	
			6 V		40	112		169		141	
t_{pd}	Any A	Y	2 V		115	175		262		219	ns
			4.5 V		23	35		52		44	
			6 V		21	31		46		39	
t_{pd}	C	Y	2 V		95	150		225		187	ns
			4.5 V		19	30		45		37	
			6 V		17	27		40		34	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'HC677 and 'HC678 can be wired to recognize any one of 2^{16} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made.

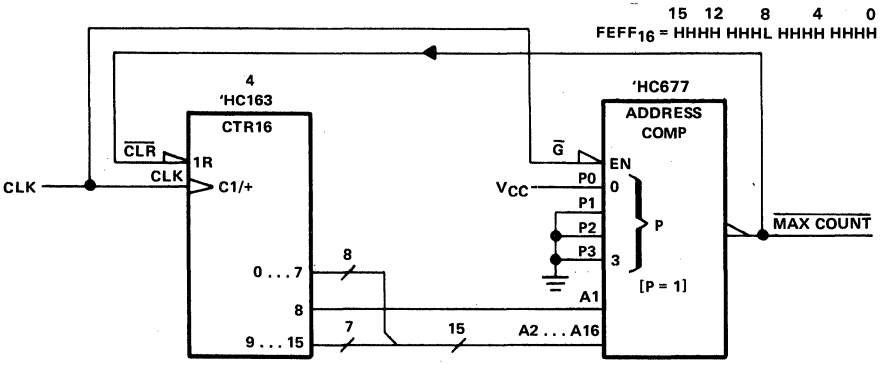
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining eight system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'HC163 is connected to provide a low-level clear signal when N = $FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER

D2833, MARCH 1984—REVISED SEPTEMBER 1987

- **'HC679 is a 12-Bit Address Comparator With Enable**
- **'HC680 is a 12-Bit Address Comparator With Latch**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

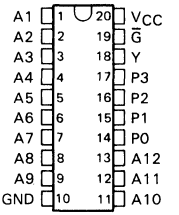
description

The 'HC679 and 'HC680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

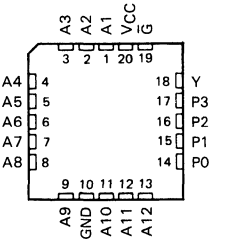
The 'HC679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'HC680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

The 'HC679 and :'HC680 are functionally unilaterally interchangeable with their TTL ALS counterparts, 'ALS679 and 'ALS680, in all cases of normal use as 12-bit address comparators. They differ in two respects. First, they may be programmed to recognize all A inputs low either by connecting all P inputs high (1111 = decimal 15), or by combination HHLL (1100 = 12), the latter option not being valid for the TTL ALS parts. Second, the combinations HHLH and HHHL (1101 = 13 and 1110 = 14) cannot be used (but are not needed) in address-comparator applications. These two combinations cause the outputs to be disabled (high).

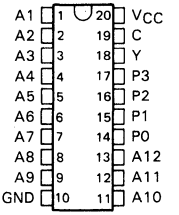
SN54HC679 . . . J PACKAGE
SN74HC679 . . . DW OR N PACKAGE
(TOP VIEW)



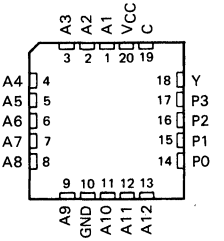
SN54HC679 . . . FK PACKAGE
(TOP VIEW)



SN54HC680 . . . J PACKAGE
SN74HC680 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC680 . . . FK PACKAGE
(TOP VIEW)



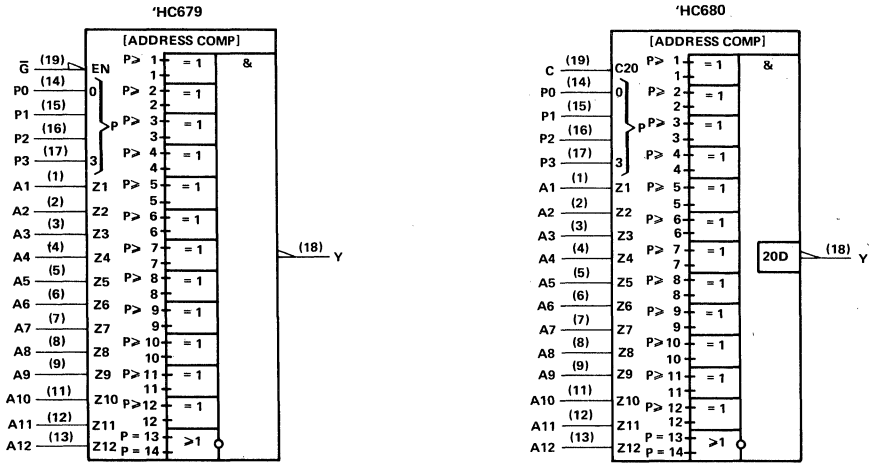
description (continued)

The SN54HC679 and SN54HC680 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC679 and SN74HC680 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

'HC679	'HC680	INPUTS COMMON TO 'HC679 AND 'HC680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'HC679: Any combination																H
	L	'HC680: Any combination																Latched

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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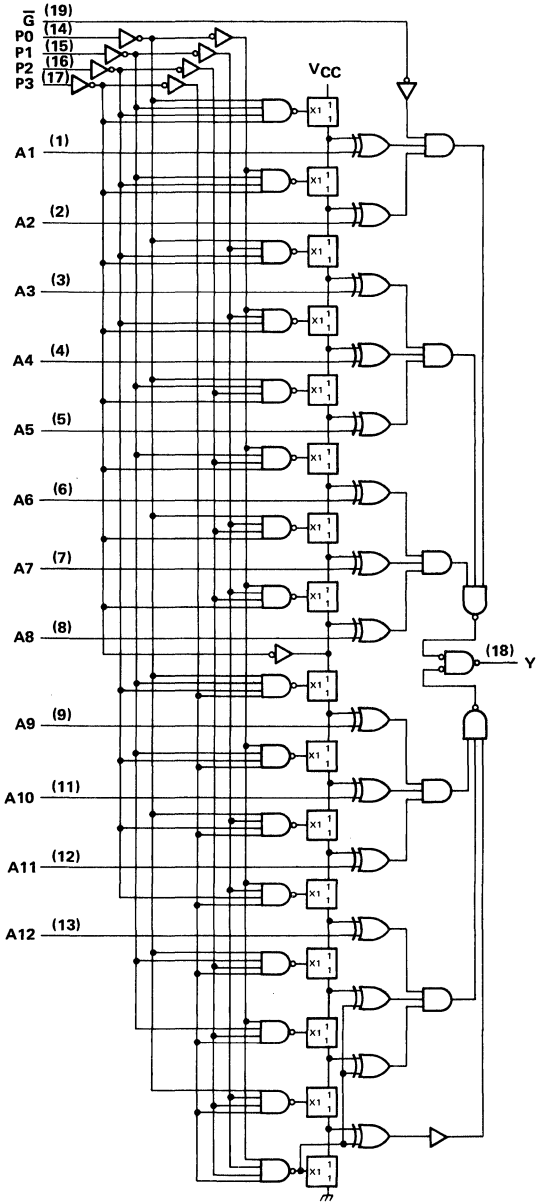
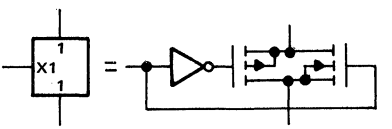
'HC679 logic diagram (positive logic)

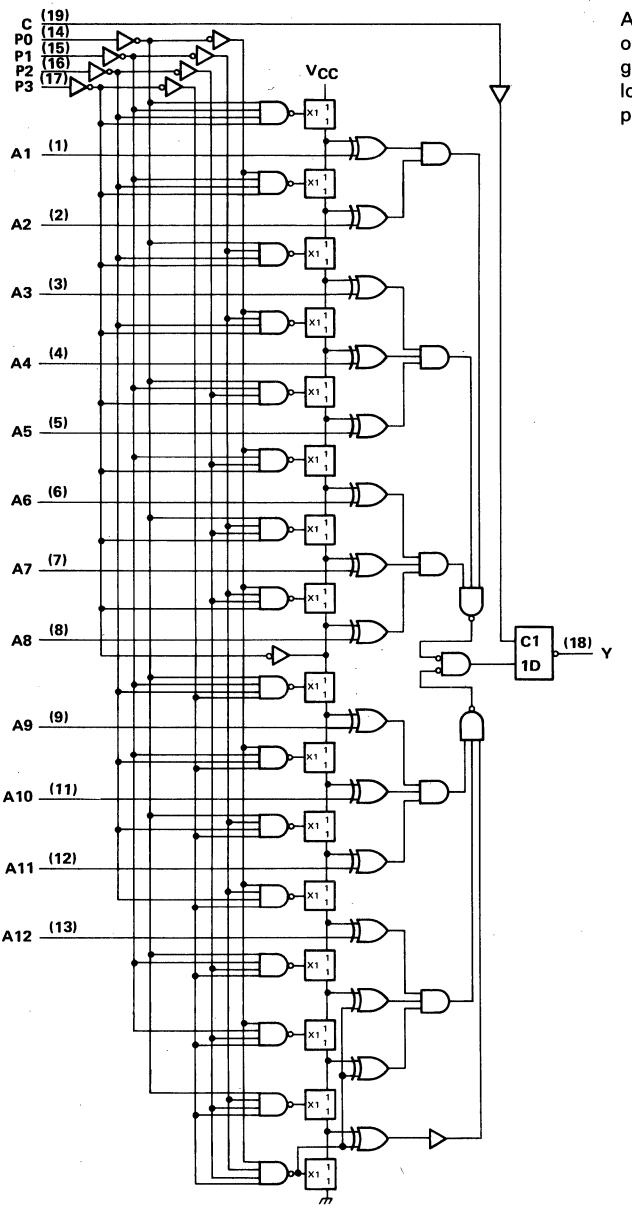


Pin numbers shown are for DW, J, and N packages.

In order to understand the implementation of this device, it is essential that the function of the vertical string of transmission gates be understood. A schematic of one of these gates is shown below. If the input to the transmission gate labeled "X1" is high, then the transmission path between the two ports labeled "1" is on. If the "X1" input is low, then the transmission path between the two ports labeled "1" is off. Only one of the 16 transmission gates can be off while the device is operating; which one is off is determined by inputs P0 through P3. The lines going from the string of transmission gates to the Exclusive-OR gates located above the transmission gate that is off will be high. The lines going to the Exclusive-OR gates located below that transmission gate will be low.



'HC680 logic diagram (positive logic)



An explanation of the function of the string of transmission gates appears with the 'HC679 logic diagram on the previous page.

Pin numbers shown are for DW, J, and N packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC679 SN54HC680			SN74HC679 SN74HC680			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC679 SN54HC680		SN74HC679 SN74HC680		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

'HC679 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC679		SN74HC679		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		185	300		450		375	ns
			4.5 V		37	60		90		75	
			6 V		31	51		76		64	
t_{pd}	Any A	Y	2 V		105	160		240		200	ns
			4.5 V		21	32		48		40	
			6 V		18	27		41		34	
t_{pd}	$\overline{G}$	Y	2 V		75	125		187		156	ns
			4.5 V		15	25		37		31	
			6 V		13	21		31		26	
t_t		Y	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

'HC680 timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC680		SN74HC680		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	2 V	75		112		94		ns
		4.5 V	15		23		19		
		6 V	13		20		16		
t_{su}	Setup time, A inputs before enable C↓	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_{su}	Setup time, P inputs before enable C↓	2 V	500		750		625		ns
		4.5 V	99		149		124		
		6 V	84		127		105		
t_h	Hold time, A or P inputs after enable C↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

'HC680 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC680		SN74HC680		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		185	300		450		375	ns
			4.5 V		37	60		90		75	
			6 V		31	51		76		64	
t_{pd}	Any A	Y	2 V		105	160		240		200	ns
			4.5 V		21	32		48		40	
			6 V		18	27		41		34	
t_{pd}	C	Y	2 V		75	125		187		156	ns
			4.5 V		15	25		37		31	
			6 V		13	21		31		26	
t_t		Y	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

TYPICAL APPLICATION INFORMATION

The 'HC679 and 'HC680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made.

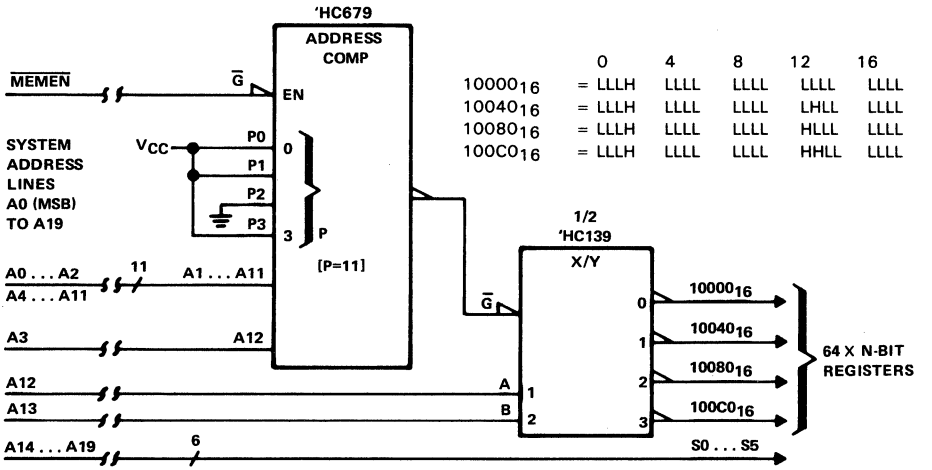
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



REGISTER BANK DECODER

- **Compares Two 8-Bit Words**
- **'HC682 has 100-kΩ Pullup Resistors on the Q Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

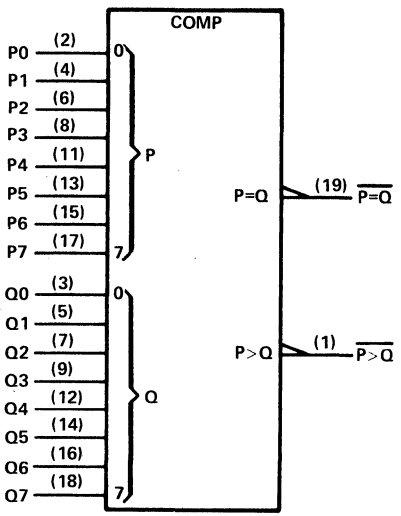
description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ and $\overline{P>Q}$ outputs. The 'HC682 features 100-kΩ pullup termination resistors on the Q inputs for analog or switch data.

The SN54HC682 and SN54HC684 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC682 and SN74HC684 are characterized for operation from −40°C to 85°C.

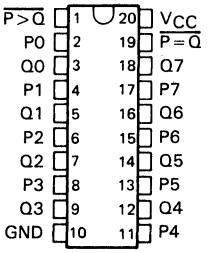
logic symbol†

'HC682‡, 'HC684

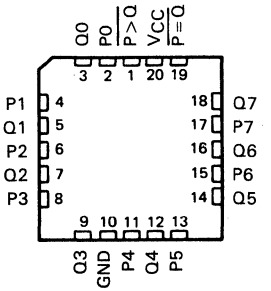


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
‡ HC682 has 100 kΩ pullup resistors on the Q inputs.

SN54HC682, SN54HC684 . . . J PACKAGE
SN74HC682, SN74HC684 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC682, SN54HC684 . . . FK PACKAGE
(TOP VIEW)

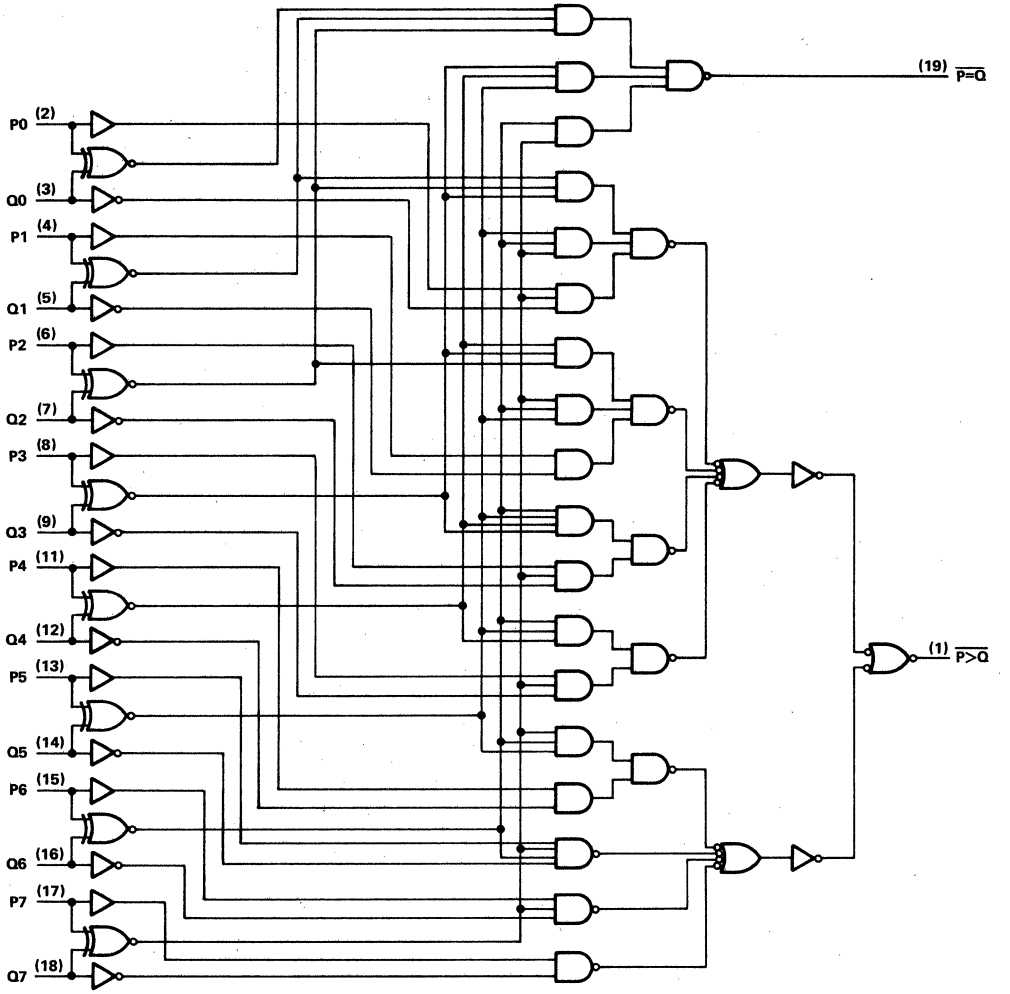


FUNCTION TABLE

INPUTS DATA	OUTPUTS	
P, Q	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

NOTE: The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC682 SN54HC684			SN74HC682 SN74HC684			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC682 SN54HC684		SN74HC682 SN74HC684		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA		4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA		6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA		2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA		4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA		6 V		0.15	0.26		0.4		0.33	
I_{IH}	V_I = V_{CC}		6 V		0.1	100		1000		1000	nA
I_{IL}	V_I = 0	Q Inputs, 'HC682	6 V		−50	−90		−160		−140	μA
		All other inputs	6 V		−0.1	−100		−1000		−1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	'HC682	6 V		480	700		1300		1100	μA
		'HC684	6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC682 SN54HC684		SN74HC682 SN74HC684		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	P or Q	Any	2 V		130	275		413		344	ns
			4.5 V		26	55		88		69	
			6 V		22	47		70		58	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

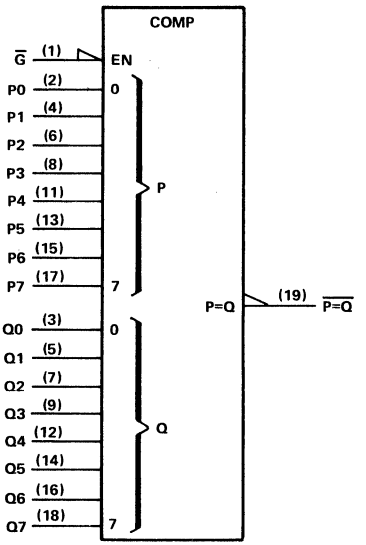
- **Compares Two 8-Bit Words**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These identity comparators perform comparisons of two eight-bit binary or BCD words. An enable input ($\overline{G}$) may be used to force the output to the high level.

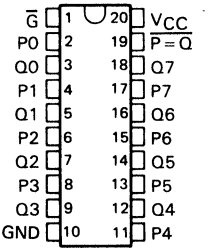
The SN54HC688 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC688 is characterized for operation from −40°C to 85°C.

logic symbol†

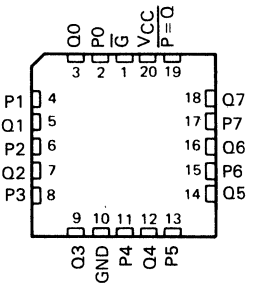


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54HC688 . . . J PACKAGE
SN74HC688 . . . DW OR N PACKAGE
(TOP VIEW)



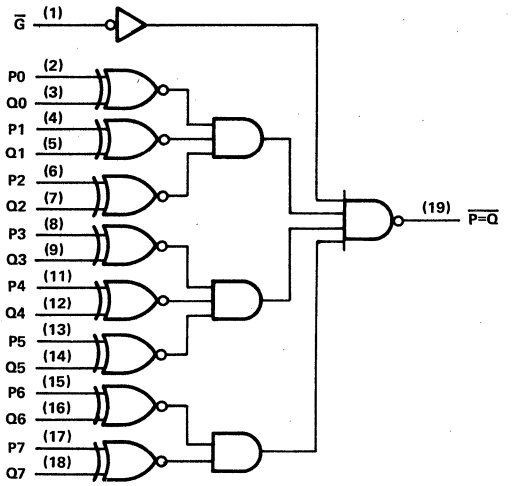
SN54HC688 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P=Q	L	L
P>Q	X	H
P<Q	X	H
X	H	H

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC688			SN74HC688			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC688		SN74HC688		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC688		SN74HC688		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	P or Q	$\overline{P=Q}$	2 V		113	210		313		265	ns
			4.5 V		30	42		63		53	
			6 V		24	36		53		45	
t_{pd}	G	$\overline{P=Q}$	2 V		66	120		179		151	ns
			4.5 V		16	24		36		30	
			6 V		14	20		30		26	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

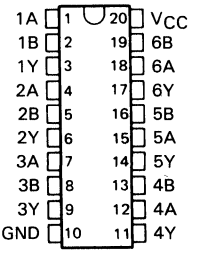
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC804 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC804 is characterized for operation from −40°C to 85°C.

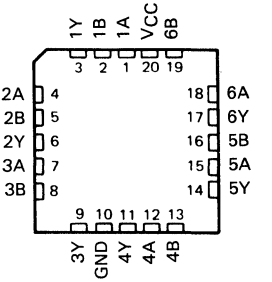
FUNCTION TABLE
(EACH DRIVER)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

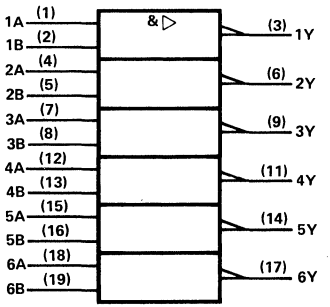
SN54HC804 . . . J PACKAGE
SN74HC804 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC804 . . . FK PACKAGE
(TOP VIEW)

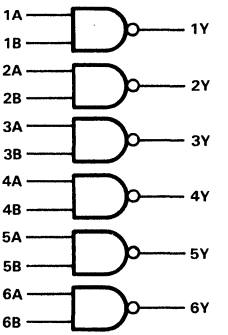


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC804			SN74HC804			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC804		SN74HC804		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC804		SN74HC804		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		26		22	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC804		SN74HC804		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	185		280		230	ns
			4.5 V		20	37		56		46	
			6 V		16	32		48		41	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

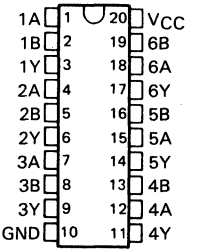
These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC805 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC805 is characterized for operation from −40°C to 85°C.

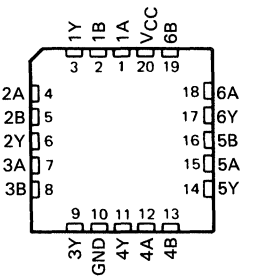
FUNCTION TABLE
(EACH DRIVER)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

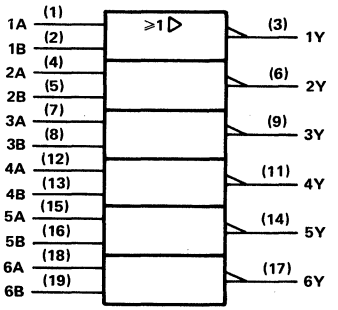
SN54HC805 . . . J PACKAGE
SN74HC805 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC805 . . . FK PACKAGE
(TOP VIEW)

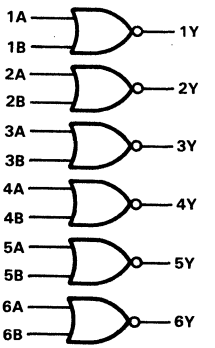


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC805			SN74HC805			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC805		SN74HC805		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC805		SN74HC805		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		31	95		145		120	ns
			4.5 V		10	19		29		24	
			6 V		8	16		25		20	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	40 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC805		SN74HC805		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		44	180		275		225	ns
			4.5 V		14	36		55		45	
			6 V		11	31		47		39	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

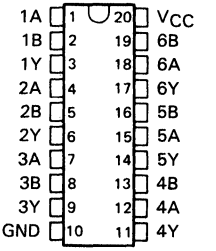
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54HC808 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC808 is characterized for operation from −40°C to 85°C.

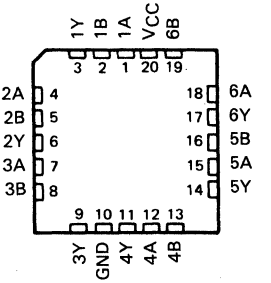
FUNCTION TABLE
(EACH DRIVER)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

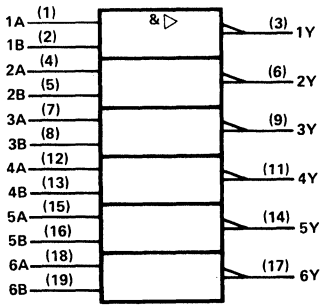
SN54HC808 . . . J PACKAGE
SN74HC808 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC808 . . . FK PACKAGE
(TOP VIEW)

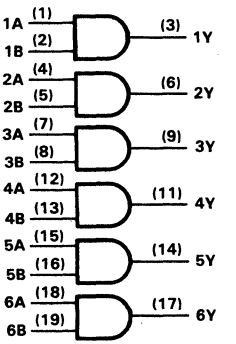


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC808			SN74HC808			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC808		SN74HC808		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC808		SN74HC808		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **High-Current Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

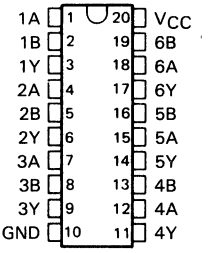
These devices contain six independent 2-input OR drivers. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54HC832 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC832 is characterized for operation from −40°C to 85°C.

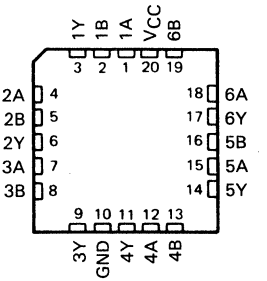
FUNCTION TABLE
(EACH DRIVER)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

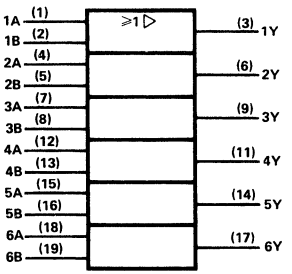
SN54HC832 . . . J PACKAGE
SN74HC832 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC832 . . . FK PACKAGE
(TOP VIEW)

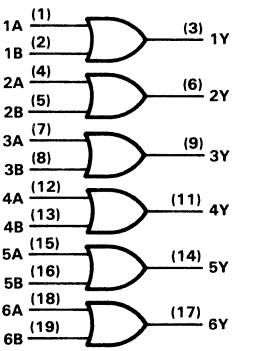


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC832			SN74HC832			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC832		SN74HC832		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −7.8 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC832		SN74HC832		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent 4-input positive NOR gates. They perform the Boolean functions:

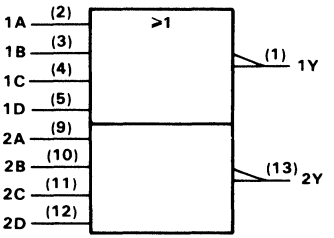
$Y = \overline{A + B + C + D}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ in positive logic.

The SN54HC4002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4002 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

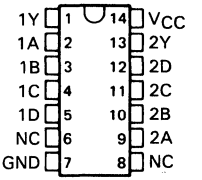
logic symbol†



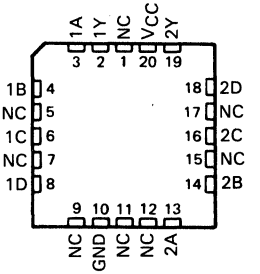
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC4002 . . . J PACKAGE
SN74HC4002 . . . D OR N PACKAGE
(TOP VIEW)

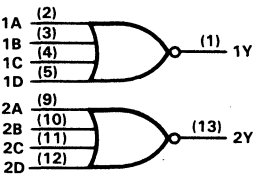


SN54HC4002 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4002			SN74HC4002			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4002		SN74HC4002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4002		SN74HC4002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A thru D	Y	2 V		44	110		165		140	ns
			4.5 V		12	22		33		28	
			6 V		11	19		28		24	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

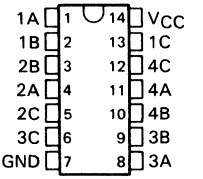
C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2922, JANUARY 1986

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance of 50 Ohms Typ at V_{CC} = 9 V
- Individual Switch Controls
- Extremely Low Input Current

SN54HC4016 . . . J OR N PACKAGE
TLC4016I . . . D OR N PACKAGE
(TOP VIEW)



description

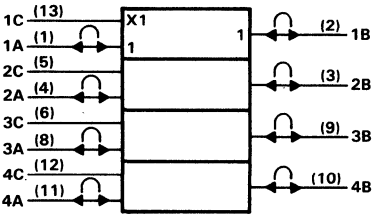
The TLC4016 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

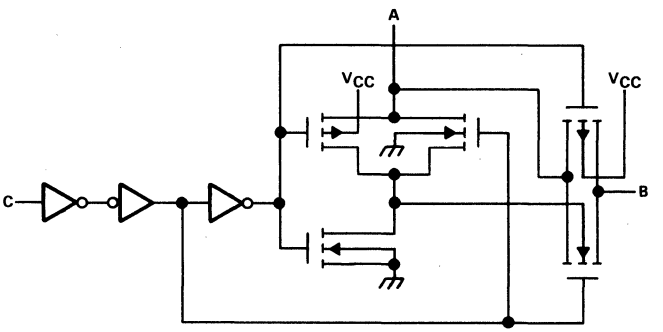
The SN54HC4016 is characterized for operation from −55°C to 125°C, and the TLC4016I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} < V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: SN54HC4016 . . . . . −55°C to 125°C
TLC4016I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating
	25°C	85°C	125°C	Factor
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	SN54HC4016	−55		125	°C
	TLC4016I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	V_{CC}	SN54HC4016			TLC4016I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	120		50	105	
				12 V		30	100		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V to 6 V			±1			±1	μA
			V_I = 0 or V_{CC}, T_A = 25°C				±0.1			±0.1	
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54HC4016			TLC4016I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		25	62	ns
			4.5 V		5	15		5	13	
			9 V		4	14		4	12	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V		180				180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

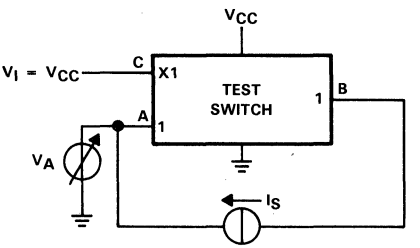
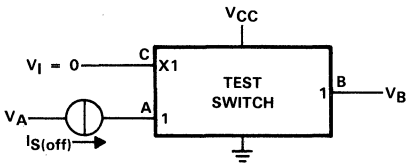


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

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PARAMETER MEASUREMENT INFORMATION

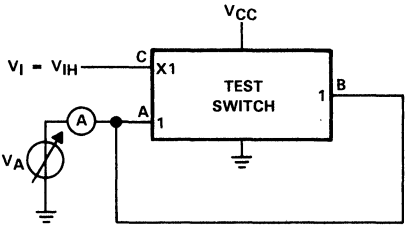
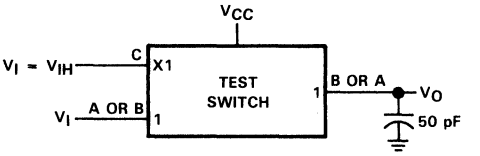
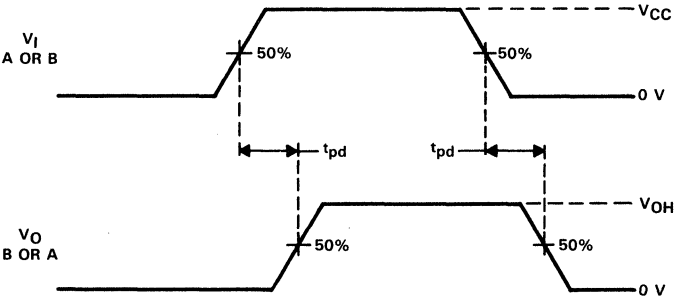


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



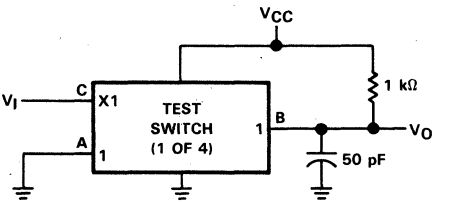
TEST CIRCUIT



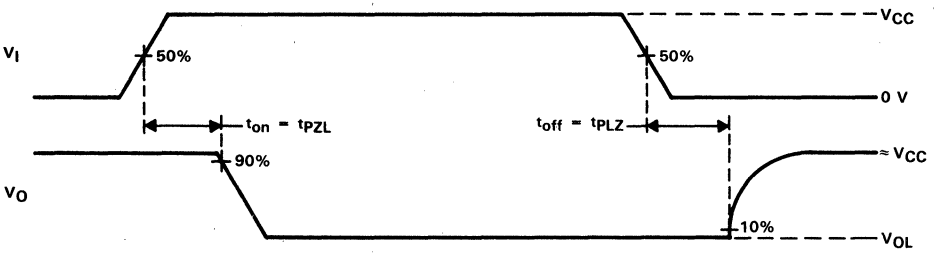
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



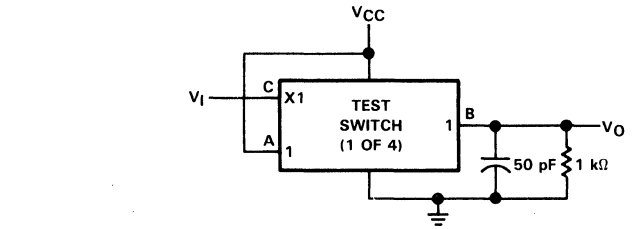
TEST CIRCUIT



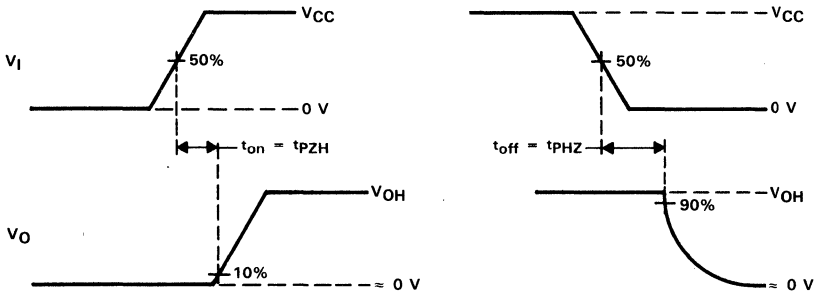
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

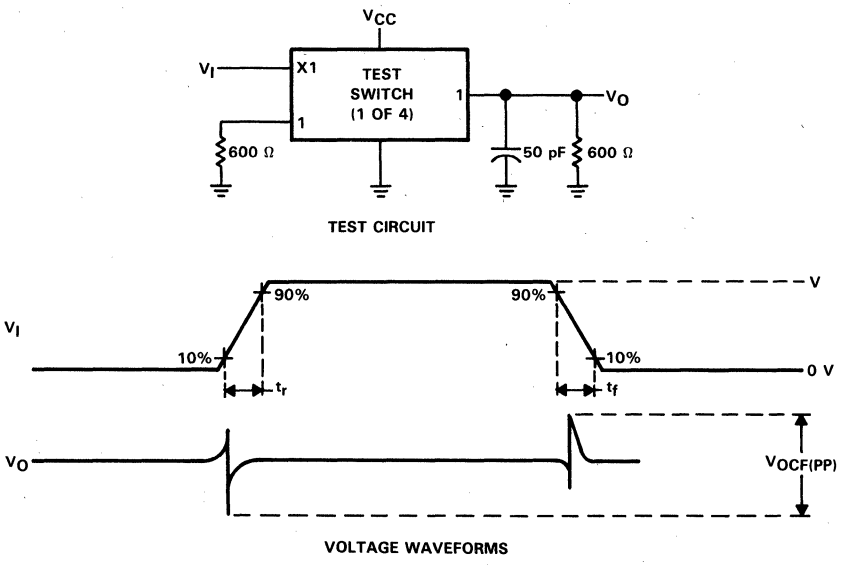
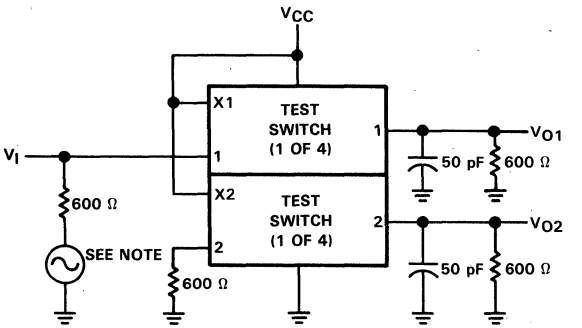


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Carry-Out Output for Cascading**
- **Divide-by-N Counting**
- **DC Clock Input Circuit Allows Slow Rise Times**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

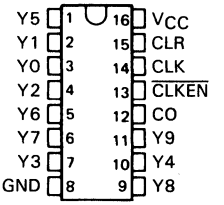
description

The 'HC4017 is a 5-stage divide-by-10 Johnson counter with ten decoded outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson decade counter configuration.

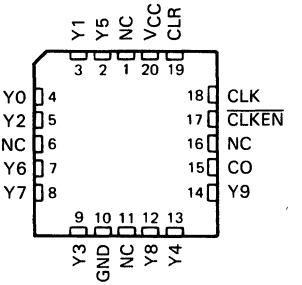
The ten decoded outputs are normally low and go high only at their respective decimal time periods. A high signal on CLR asynchronously clears the decade counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output CO is high while Y0, Y1, Y2, Y3, or Y4 is high, then is low while Y5, Y6, Y7, Y8, or Y9 is high.

The SN54HC4017 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4017 is characterized for operation from −40°C to 85°C.

SN54HC4017 . . . J PACKAGE
SN74HC4017 . . . DW OR N PACKAGE
(TOP VIEW)

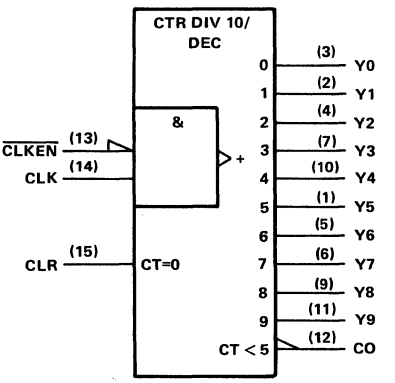


SN54HC4017 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

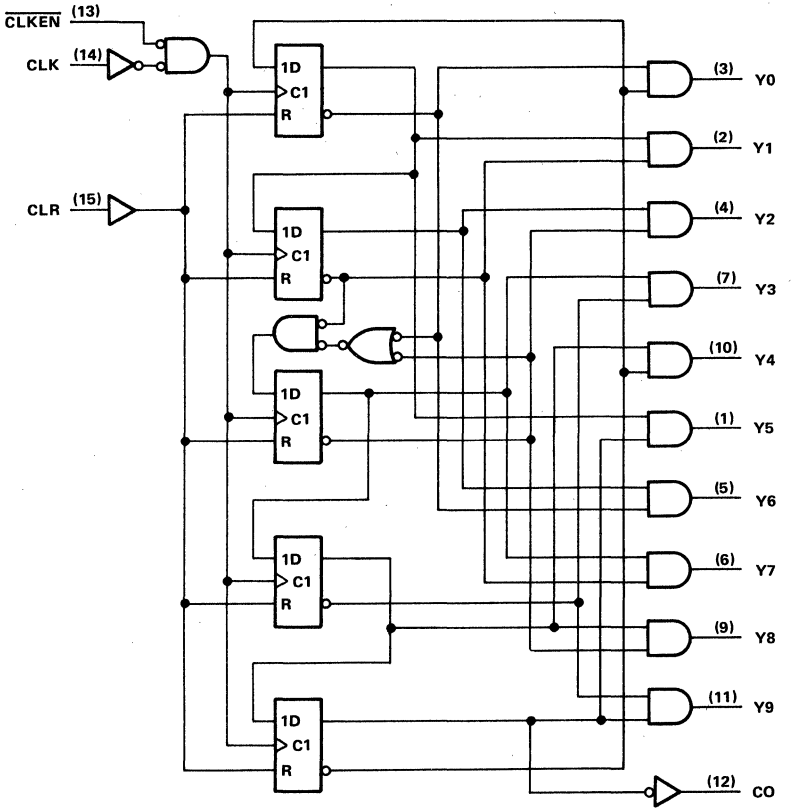
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

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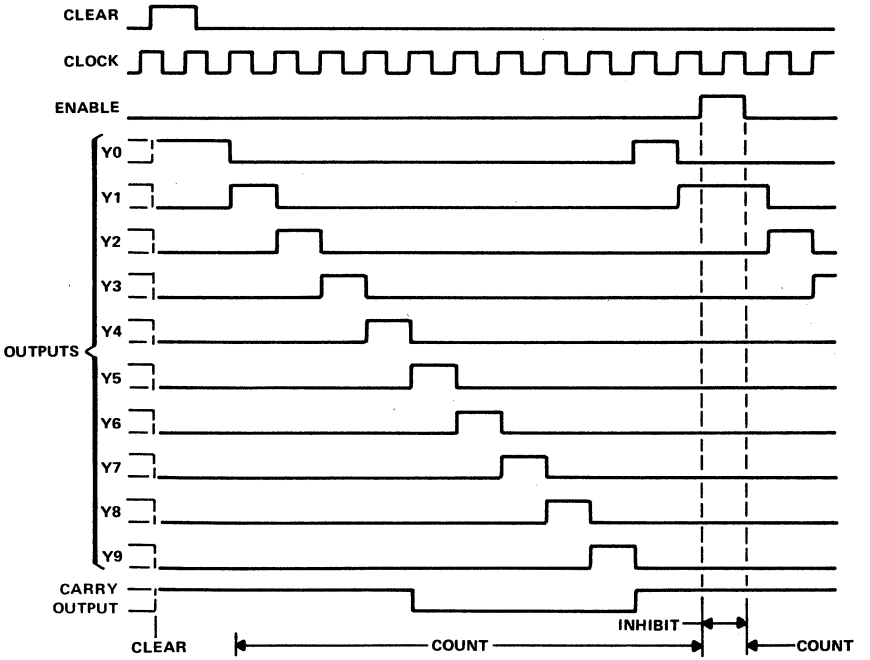
typical clear, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4017			SN74HC4017			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4017		SN74HC4017		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	T_A = 25°C		SN54HC4017		SN74HC4017		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLK† or $\overline{CLKEN}$‡	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	20	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low† or $\overline{CLKEN}$ high or low‡	2 V	80		120		100		ns
			4.5 V	16		25		20		
			6 V	14		20		17		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	$\overline{CLKEN}$ low before CLK↑† or CLK high before $\overline{CLKEN}$↓‡	2 V	50		75		63		ns
			4.5 V	10		15		13		
			6 V	9		13		11		
		CLR inactive before CLK↑† or $\overline{CLKEN}$↓‡	2 V	50		75		63		
			4.5 V	10		15		13		
			6 V	9		13		11		
t_h	Hold time	$\overline{CLKEN}$ low after CLK↑† or CLK high after $\overline{CLKEN}$↓‡	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

†These conditions apply if clocking is being performed via the CLK input.
‡These conditions apply if clocking is being performed via the $\overline{CLKEN}$ input.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4017		SN74HC4017		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		20		25		
			6 V	36	55		25		29		
t_{pd}	CLK	Any Y or CO	2 V		90	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{pd}	$\overline{CLKEN}$	Any Y or CO	2 V		125	250		373		315	ns
			4.5 V		25	50		75		63	
			6 V		21	43		63		54	
t_{pd}	CLR	Any Y	2 V		90	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{PLH}	CLR	CO	2 V		90	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_t		Any output	2 V		38	75		110		95	ns
			4.5 V		8	15		22		18	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

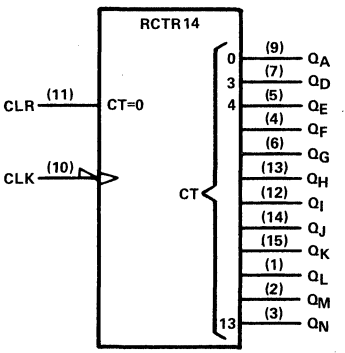
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock when CLR goes high.

The SN54HC4020 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4020 is characterized for operation from −40°C to 85°C.

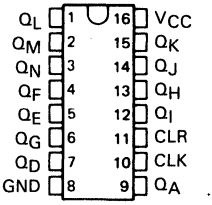
logic symbol†



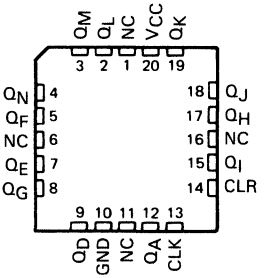
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

SN54HC4020 . . . J PACKAGE
SN74HC4020 . . . DW OR N PACKAGE
(TOP VIEW)

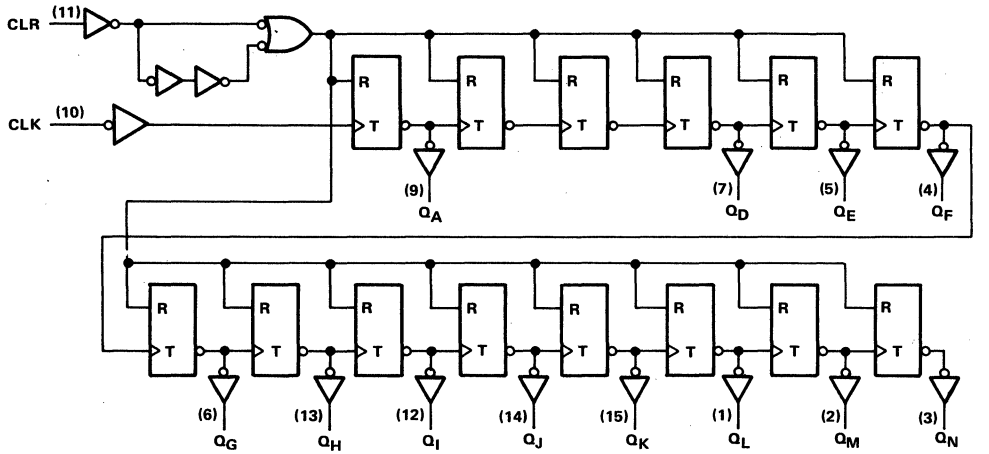


SN54HC4020 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4020			SN74HC4020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4020		SN74HC4020		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.3	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	33	0	22	0	25	
t_w	Pulse duration	CLK high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	70		105		90		ns
			4.5 V	14		21		18		
			6 V	12		18		25		
t_{su}	Setup time, CLR inactive before CLK↓		2 V	60		90		75		ns
			4.5 V	12		18		15		
			6 V	10		15		13		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLK	Q_A	2 V		62	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		12	26		38		32	
t_{PHL}	CLR	Any	2 V		63	140		210		175	ns
			4.5 V		17	28		42		35	
			6 V		13	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	88 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

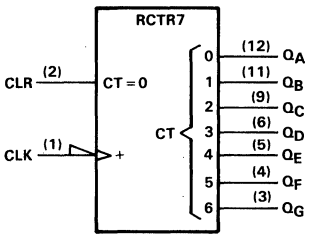
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC4024 is an asynchronous 7-stage binary counter designed with an input pulse-shaping circuit. The outputs of all stages are available externally. A high clear signal asynchronously clears the counter and resets all outputs low. The count is advanced on the high-to-low transition of the clock pulse. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN54HC4024 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4024 is characterized for operation from −40°C to 85°C.

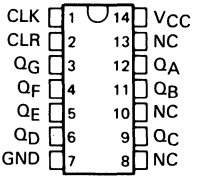
logic symbol†



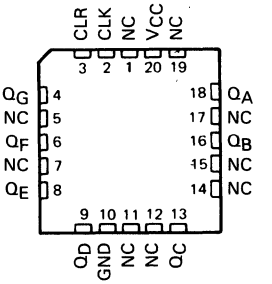
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC4024 . . . J PACKAGE
SN74HC4024 . . . D OR N PACKAGE
(TOP VIEW)

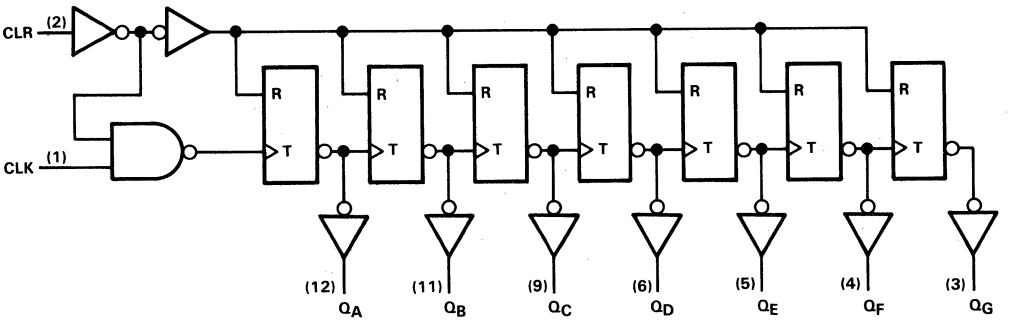


SN54HC4024 . . . FK PACKAGE
(TOP VIEW)



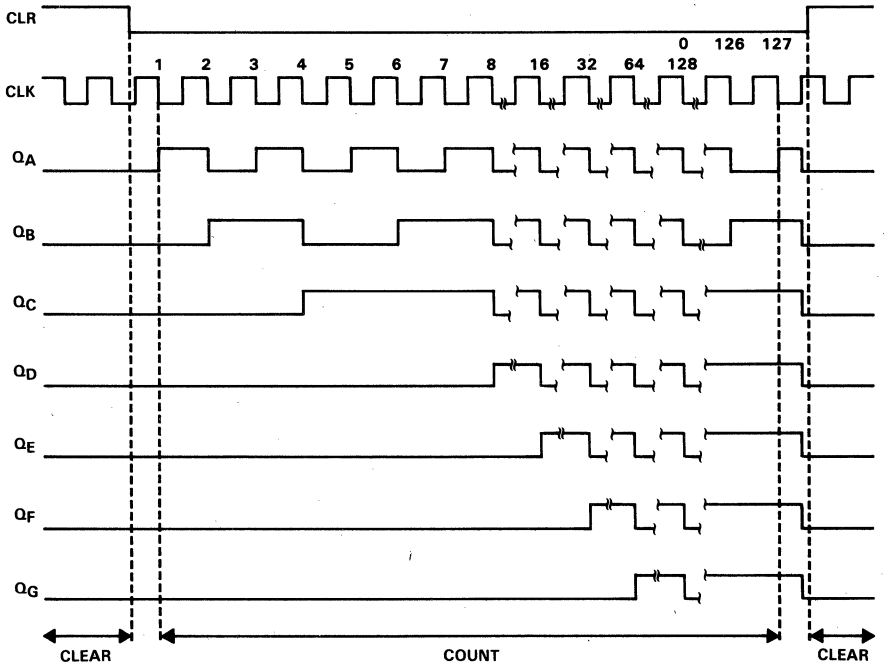
NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

typical clear and count sequence



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4024			SN74HC4024			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4024		SN74HC4024		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4024		SN74HC4024		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2V	0	5.5	0	3.7	0	4.3	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	33	0	22	0	25	
t_w	Pulse duration	CLK high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, CLR low before CLK↓		2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4024		SN74HC4024		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	50		19		22		
			6 V	33	60		22		26		
t_{pd}	CLK	Q_A	2 V		56	120		180		150	ns
			4.5 V		16	24		36		30	
			6 V		12	20		31		26	
t_{PHL}	CLR	Any	2 V		61	130		195		165	ns
			4.5 V		17	26		39		32	
			6 V		13	22		33		28	
t_t			2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

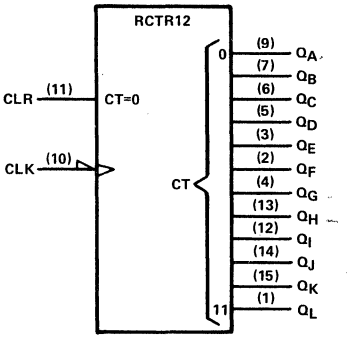
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

This device is an asynchronous 12-stage binary counter with the outputs of all stages available externally. A high level at CLR asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at CLK. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

The SN54HC4040 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4040 is characterized for operation from −40°C to 85°C.

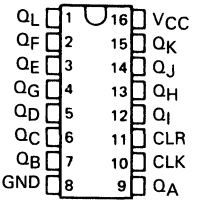
logic symbol†



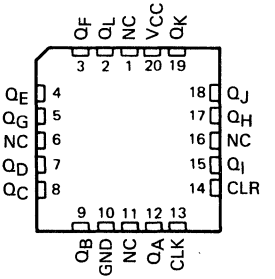
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

SN54HC4040 . . . J PACKAGE
SN74HC4040 . . . DW OR N PACKAGE
(TOP VIEW)

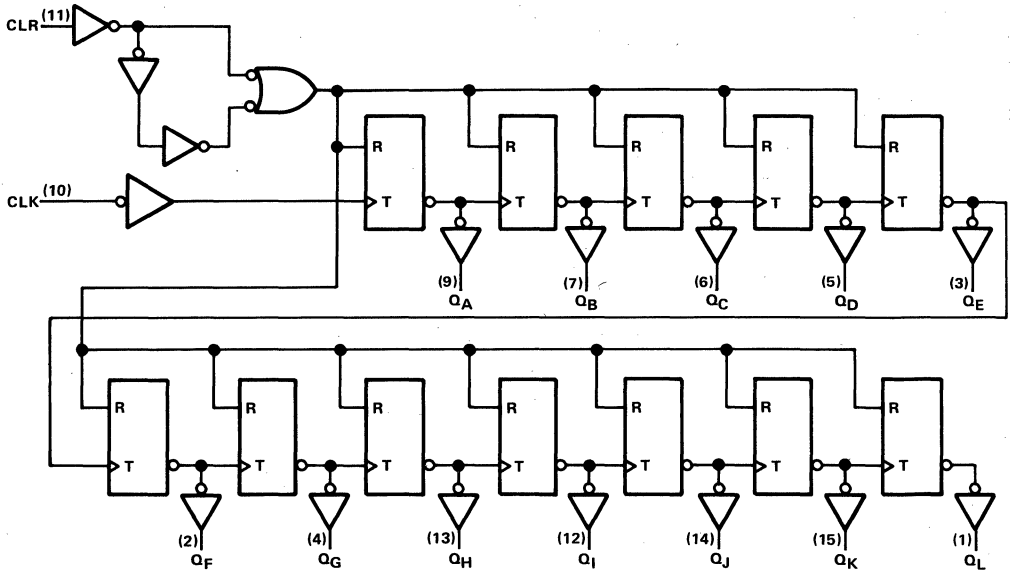


SN54HC4040 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54HC4040			SN74HC4040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4040		SN74HC4040		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4040		SN74HC4040		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2V	0	5.5	0	3.7	0	4.3	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	33	0	22	0	25	
t_w	Pulse duration	CLK high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	70		105		90		ns
			4.5 V	14		21		18		
			6 V	12		18		15		
t_{su}	Setup time, CLR inactive before CLK↑		2 V	60		90		75		ns
			4.5 V	12		18		15		
			6 V	10		15		13		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4040		SN74HC4040		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLK	Q_A	2 V		62	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		12	26		38		32	
t_{PHL}	CLR	Any	2 V		63	140		210		175	ns
			4.5 V		17	28		42		35	
			6 V		13	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	30		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	88 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

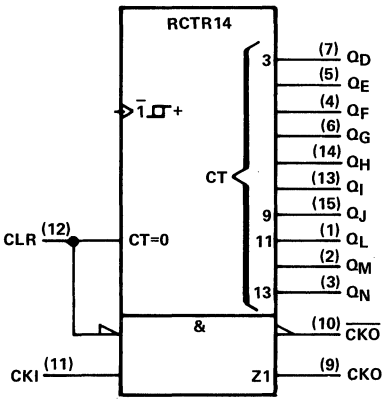
- **Allows Design of Either RC or Crystal Oscillator Circuits**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC4060 consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A high-to-low transition on the clock input increments the counter. A high level at CLR disables the oscillator ($\overline{CKO}$ goes high and CKO goes low) and resets the counter to zero (all Q outputs low).

The SN54HC4060 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4060 is characterized for operation from −40°C to 85°C.

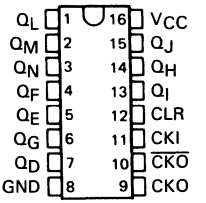
logic symbol†



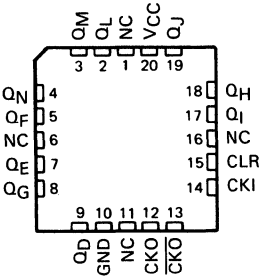
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

SN54HC4060 . . . J PACKAGE
SN74HC4060 . . . DW OR N PACKAGE
(TOP VIEW)

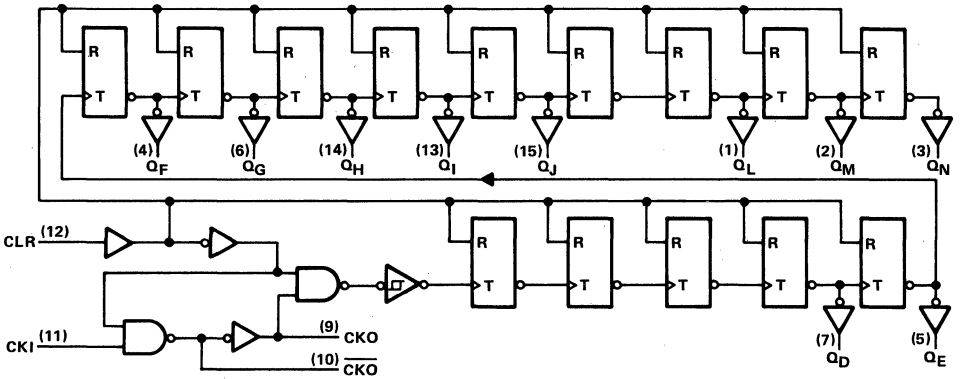


SN54HC4060 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4060			SN74HC4060			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All Outputs	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20\ \mu A$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
	Q Outputs	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -4$ mA	4.5 V	3.98	4.30		3.7		3.84		
		$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -5.2$ mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	All Outputs	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 20\ \mu A$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
	Q Outputs	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
		$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I		$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}		$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i			2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4060		SN74HC4060		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.3	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	33	0	22	0	25	
t_w	Pulse duration	CKI high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
t_{su}	Setup time, CLR inactive before CKI↓		2 V	160		240		200		ns
			4.5 V	32		48		40		
			6 V	27		41		34		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CKI	Q_D	2 V		240	490		735		615	ns
			4.5 V		58	98		147		123	
			6 V		42	83		125		105	
t_{PHL}	CLR	Any Q	2 V		66	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

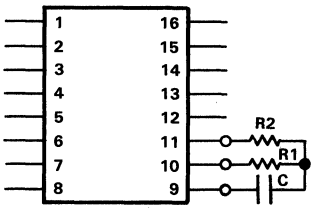
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	88 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

CONNECTING AN RC OSCILLATOR CIRCUIT TO THE 'HC4060

The 'HC4060 consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits.

When a RC oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the chip as follows:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency f, the following formula is used:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\ R2 + 0.693}{R1 + R2}\right)}$$

If R2 >> R1 (i.e. R2 = 10R1), then the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

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D2804, MARCH 1984—REVISED SEPTEMBER 1987

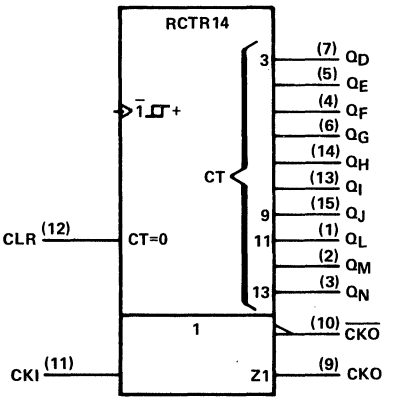
- **Allows Design of Either RC or Crystal Oscillator Circuits**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'HC4061 consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A high-to-low transition on the clock input increments the counter. A high level at CLR resets the counter to zero (all Q outputs low) but has no effect on the oscillator.

The SN54HC4061 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4061 is characterized for operation from −40°C to 85°C.

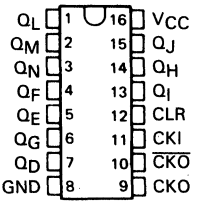
logic symbol†



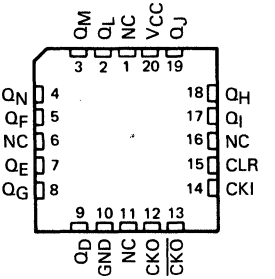
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

SN54HC4061 . . . J PACKAGE
SN74HC4061 . . . DW OR N PACKAGE
(TOP VIEW)

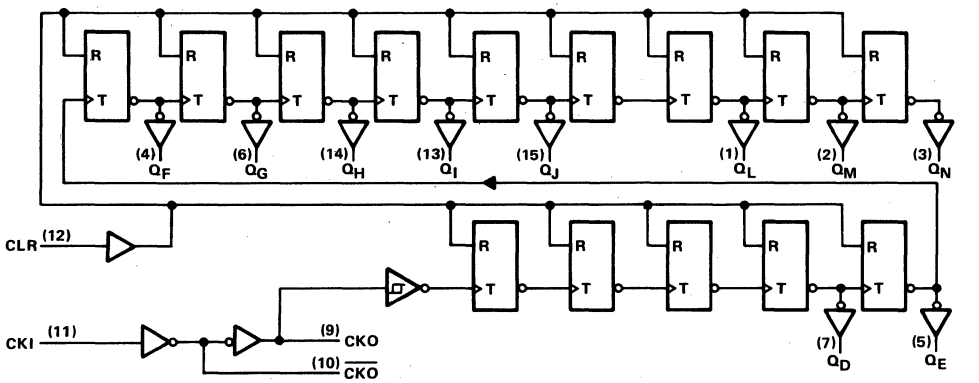


SN54HC4061 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4061			SN74HC4061			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4061		SN74HC4061		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20\ \mu A$	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -4$ mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -5.2$ mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 20\ \mu A$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, $I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4061		SN74HC4061		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		5.5		3.7		4.3	MHz
			4.5 V		28		19		22	
			6 V		33		22		25	
t_w	Pulse duration	CKI high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
t_{su}	Setup time, CLR inactive before CKI↓		2 V	160		240		200		ns
			4.5 V	32		48		40		
			6 V	27		41		34		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4061		SN74HC4061		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CKI	Q_D	2 V		240	490		735		615	ns
			4.5 V		58	98		147		123	
			6 V		42	83		125		105	
t_{PHL}	CLR	Any Q	2 V		66	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

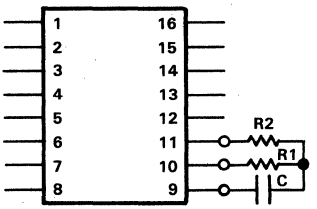
C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	88 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

CONNECTING AN RC OSCILLATOR CIRCUIT TO THE 'HC4061

The 'HC4061 consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits.

When a RC oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the chip as follows:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency f, the following formula is used:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\ R2\ +\ 0.693}{R1\ +\ R2}\right)}$$

If $R2 > R1$ (i.e. $R2 = 10R1$), then the above formula simplifies to:

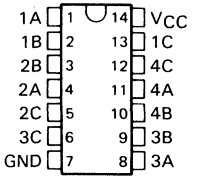
$$f = \frac{0.455}{(R1)(C)}$$

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2922, JANUARY 1986

- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . .Typically 30 Ohms at V_{CC} = 12 V
- Individual Switch Controls
- Extremely Low Input Current
- Functionally Interchangeable with National Semiconductor MM54/74HC4066, Motorola MC54/74HC4066, and RCA CD4066A

SN54HC4066 . . . J OR N PACKAGE
TLC4066I . . . D OR N PACKAGE
(TOP VIEW)



description

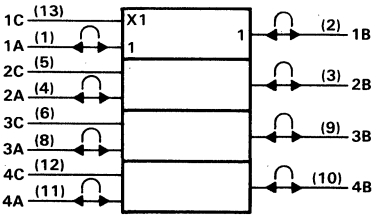
The TLC4066 is a silicon-gate CMOS quadruple analog switch integrated circuit designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 12 volts peak to be transmitted in either direction.

Each switch section has its own enable input control. A high-level voltage applied to this control terminal turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

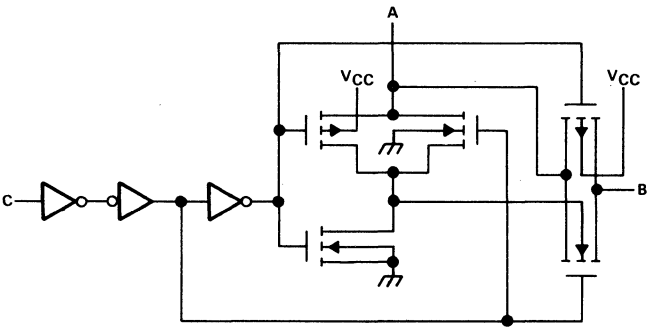
The SN54HC4066 is characterized for operation from −55°C to 125°C, and the TLC4066I is characterized from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range (see Note 1) . . . . . −0.5 V to 15 V
Control-input diode current ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
I/O port diode current ($V_I < 0$ or $V_{I/O} < V_{CC}$) . . . . . ±20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
D package . . . . . 950 mW
J package . . . . . 1025 mW
N package . . . . . 875 mW
Operating free-air temperature, T_A: SN54HC4066 . . . . . −55°C to 125°C
TLC4066I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

Package	Maximum Power Dissipation			Derating Factor
	25°C	85°C	125°C	
D	950 mW	494 mW		7.6 mW/°C
J	1025 mW	533 mW	205 mW	8.2 mW/°C
N	875 mW	455 mW	175 mW	7.0 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2†	5	12	V
I/O port voltage, $V_{I/O}$		0		V_{CC}	V
High-level input voltage, V_{IH}	V_{CC} = 2 V	1.5		V_{CC}	V
	V_{CC} = 4.5 V	3.15		V_{CC}	
	V_{CC} = 9 V	6.3		V_{CC}	
	V_{CC} = 12 V	8.4		V_{CC}	
Low-level input voltage, V_{IL}	V_{CC} = 2 V	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	
	V_{CC} = 9 V	0		1.8	
	V_{CC} = 12 V	0		2.4	
Input rise time, t_r	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Input fall time, t_f	V_{CC} = 2 V			1000	ns
	V_{CC} = 4.5 V			500	
	V_{CC} = 9 V			400	
Operating free-air temperature, T_A	SN54HC4066	−55		125	°C
	TLC4066I	−40		85	

†With supply voltages at or near 2 volts, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	SN54HC4066			TLC4066I			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
r_{Son}	On-state switch resistance		I_S = 1 mA, V_A = 0 to V_{CC}, See Figure 1	4.5 V		100	220		100	200	Ω
				9 V		50	110		50	105	
				12 V		30	90		30	85	
			I_S = 1 mA, V_A = 0 or V_{CC}, See Figure 1	2 V		120	240		120	215	
				4.5 V		50	120		50	100	
				9 V		35	80		35	75	
				12 V		20	70		20	60	
	On-state switch resistance matching		V_A = 0 to V_{CC}, See Figure 1	4.5 V		10	20		10	20	Ω
				9 V		5	15		5	15	
				12 V		5	15		5	15	
I_I	Control input current		V_I = 0 or V_{CC}	2 V or 6 V			±1			±1	μA
I_{Soff}	Off-state switch leakage current		V_S = ±V_{CC}, See Figure 2	5.5 V		±10	±600		±10	±600	nA
				9 V		±15	±800		±15	±800	
				12 V		±20	±1000		±20	±1000	
I_{Son}	On-state switch leakage current		V_A = 0 or V_{CC}, See Figure 3	5.5 V		±10	±150		±10	±150	nA
				9 V		±15	±200		±15	±200	
				12 V		±20	±300		±20	±300	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	5.5 V		2	40		2	20	μA
				9 V		8	160		8	80	
				12 V		16	320		16	160	
C_i	Input capacitance	A or B		2 V to 12 V		15			15		pF
		C				5	10		5	10	
C_f	Feedthrough capacitance	A to B	V_I = 0	2 V to 12 V		5			5		pF

†All typical values are at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54HC4066			TLC4066I			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Propagation delay time, A to B or B to A	See Figure 4	2 V		25	75		15	30	ns
			4.5 V		5	15		5	13	
			9 V		4	12		4	10	
			12 V		3	13		3	11	
t_{on}	Switch turn-on time	R_L = 1 kΩ, See Figures 5 and 6	2 V		32	150		32	125	ns
			4.5 V		8	30		8	25	
			9 V		6	18		6	15	
			12 V		5	15		5	13	
t_{off}	Switch turn-off time	R_L = 1 kΩ, See Figures 5 and 6	2 V		45	252		45	210	ns
			4.5 V		15	54		15	45	
			9 V		10	48		10	40	
			12 V		8	45		8	38	
f_{co}	Switch cutoff frequency (channel loss = 3 dB)		4.5 V		100			100		MHz
			9 V		120			120		
$V_{OCF(PP)}$	Control feedthrough voltage to any switch, peak to peak	See Figure 7	4.5 V		180				180	mV
	Frequency at which crosstalk attenuation between any two switches equals 50 dB	See Figure 8	4.5 V		1			1		MHz

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

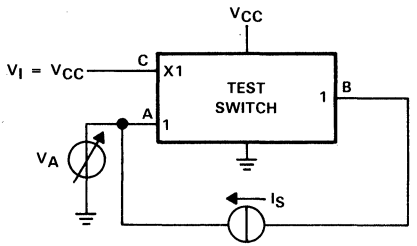
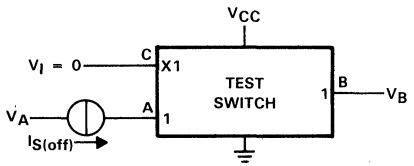


FIGURE 1. ON-STATE RESISTANCE TEST CIRCUIT



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, V_B = 0

FIGURE 2. OFF-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

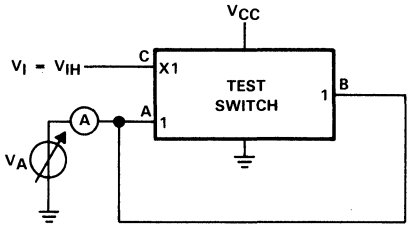
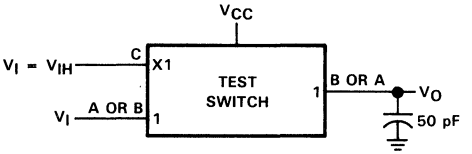
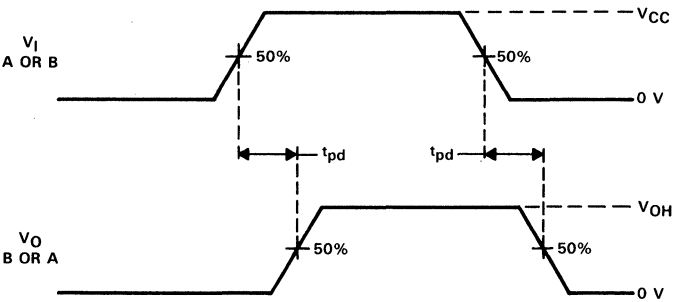


FIGURE 3. ON-STATE SWITCH LEAKAGE CURRENT TEST CIRCUIT



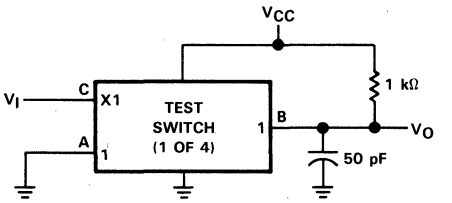
TEST CIRCUIT



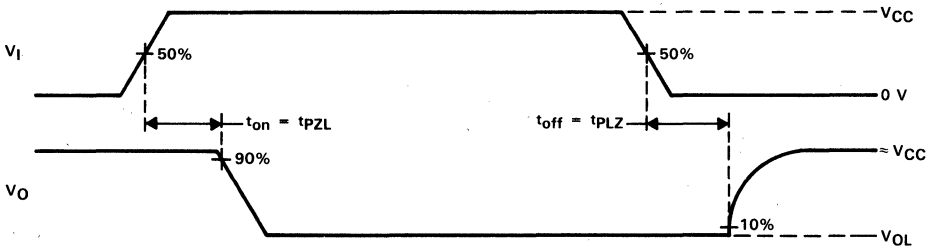
VOLTAGE WAVEFORMS

FIGURE 4. PROPAGATION DELAY TIME, SIGNAL INPUT TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



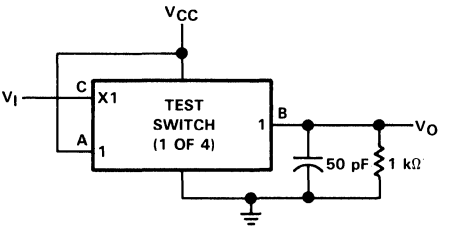
TEST CIRCUIT



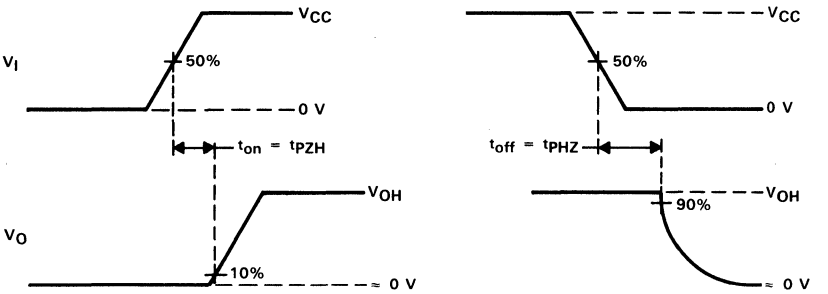
VOLTAGE WAVEFORMS

FIGURE 5. SWITCHING TIME (t_{PZL}, t_{PLZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 6. SWITCHING TIME (t_{PZH}, t_{PHZ}), CONTROL TO SIGNAL OUTPUT

PARAMETER MEASUREMENT INFORMATION

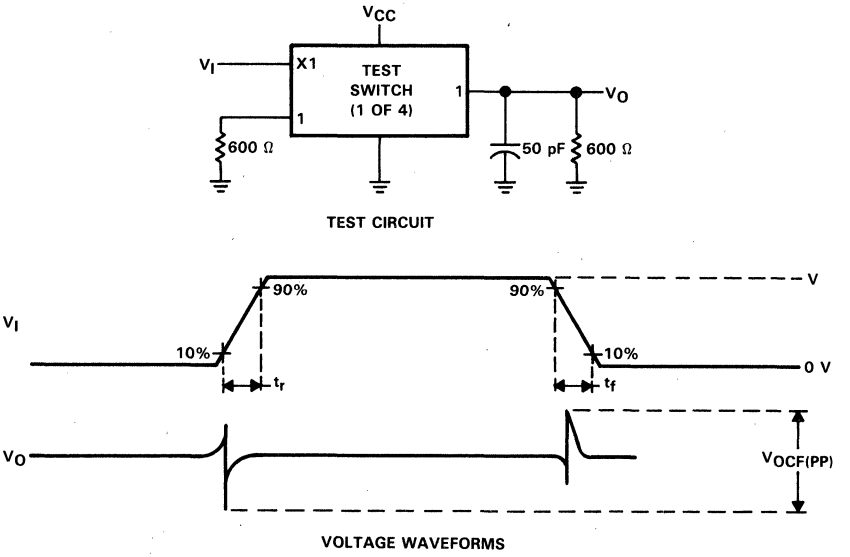
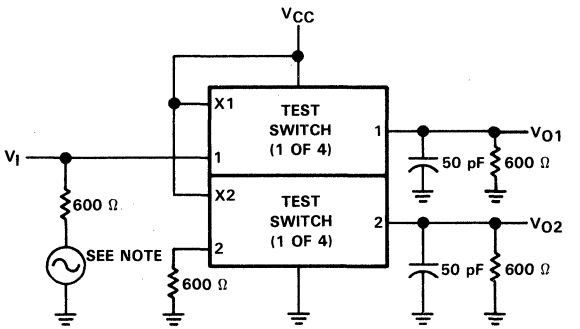


FIGURE 7. CONTROL FEEDTHROUGH VOLTAGE



NOTE: ADJUST f for $a_X = \frac{V_{O2}}{V_{O1}} = 50$ dB.

FIGURE 8. CROSSTALK BETWEEN ANY TWO SWITCHES, TEST CIRCUIT

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

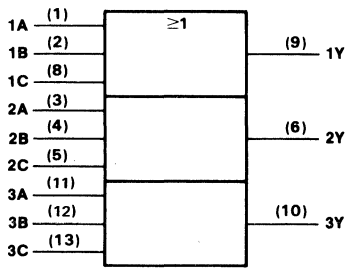
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain three independent 3-input OR gates and perform the Boolean functions $Y = A + B + C$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54HC4075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4075 is characterized for operation from −40°C to 85°C.

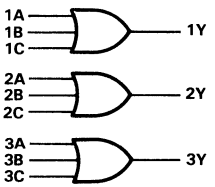
logic symbol†



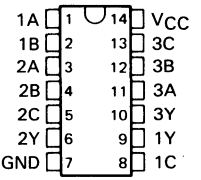
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

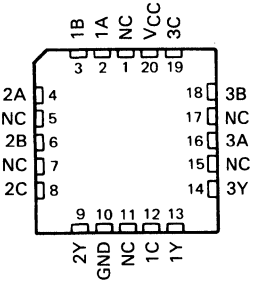
logic diagram (positive logic)



SN54HC4075 . . . J PACKAGE
SN74HC4075 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC4075 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

2 HCMOS Devices

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4075			SN74HC4075			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4075		SN74HC4075		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4075		SN74HC4075		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		38	100		150		125	ns
			4.5 V		11	20		30		25	
			6 V		9	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	26 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input OR/NOR gate and perform the following Boolean functions in positive logic:

$$W = \overline{A + B + C + D + E + F + G + H}$$

or

$$W = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{H}$$

and

$$Y = A + B + C + D + E + F + G + H$$

or

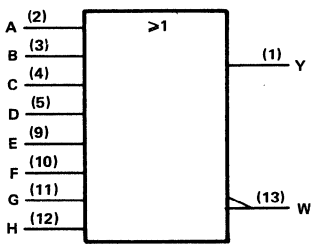
$$Y = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{H}}$$

The SN54HC4078A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4078A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUTS W	OUTPUTS Y
One or more inputs H	L	H
All inputs L	H	L

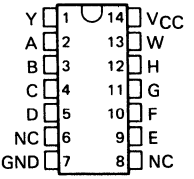
logic symbol†



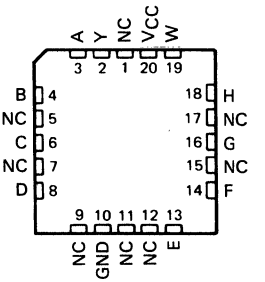
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC4078A . . . J PACKAGE
SN74HC4078A . . . D OR N PACKAGE
(TOP VIEW)

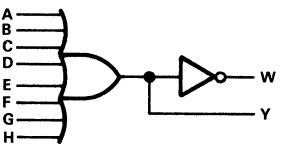


SN54HC4078A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



2 HCMOS Devices

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4078A			SN74HC4078A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4078A		SN74HC4078A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4078A		SN74HC4078A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A thru H	Y/W	2 V		40	130		195		165	ns
			4.5 V		12	26		39		33	
			6 V		10	22		33		28	
t_t		Y/W	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	25 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **Two Output Options:**
  'HC4514 Has Active-High Outputs
  'HC4515 Has Active-Low Outputs
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

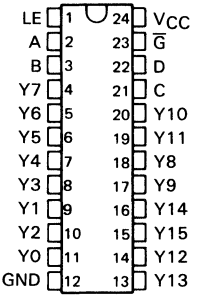
description

These devices present two output options of a 4-line to 16-line decoder with latched inputs. The 'HC4514 presents a high level at the selected output. The 'HC4515 presents a low level at the selected output.

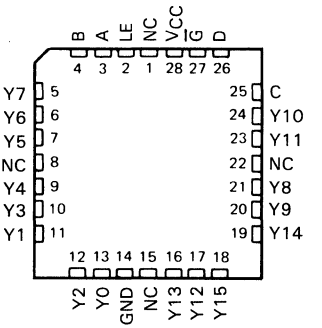
These devices consist of four storage latches with common latch enable (LE) and inhibit ($\overline{G}$) inputs. When a low signal is applied to the LE input, the input data is stored, decoded, and presented to the output. When $\overline{G}$ is high, all sixteen 'HC4514 outputs are at a low logic level, or all 'HC4515 outputs are at a high logic level.

The SN54HC4514 and the SN54HC4515 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4514 and SN74HC4515 are characterized for operation from −40°C to 85°C.

SN54HC' . . . JT PACKAGE
SN74HC' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC' . . . FK PACKAGE
(TOP VIEW)

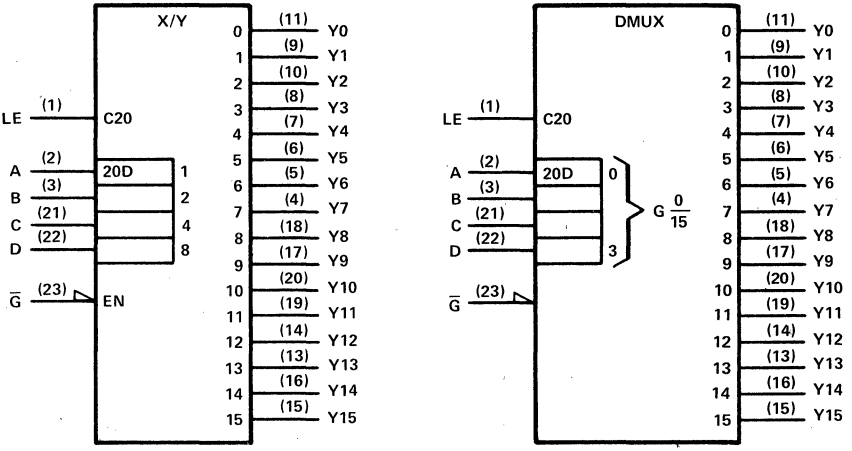


NC—No internal connection

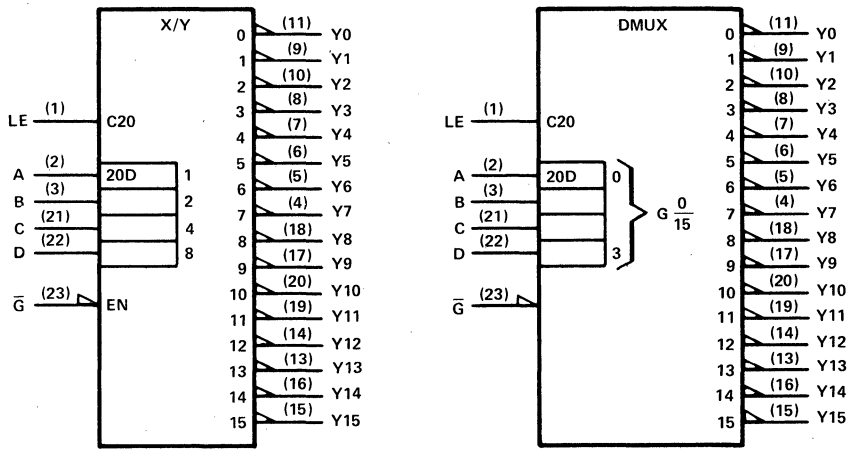
FUNCTION TABLE

INPUTS						OUTPUT	OUTPUTS	
LE	$\overline{G}$	D	C	B	A	SELECTED	'HC4514	'HC4515
H	L	L	L	L	L	0		
H	L	L	L	L	H	1		
H	L	L	L	H	L	2		
H	L	L	L	H	H	3		
H	L	L	H	L	L	4		
H	L	L	H	L	H	5	Selected	Selected
H	L	L	H	H	L	6	Output = H	Output = L
H	L	L	H	H	H	7	All others = L	All outputs = H
H	L	H	L	L	L	8		
H	L	H	L	L	H	9		
H	L	H	L	H	L	10		
H	L	H	L	H	H	11		
H	L	H	H	L	L	12		
H	L	H	H	L	H	13		
H	L	H	H	H	L	14		
H	L	H	H	H	H	15		
X	H	X	X	X	X		All = L	All = H
L	L	X	X	X	X	All outputs remain in state existing before LE↓		

'HC4514 logic symbols (alternatives)†



'HC4515 logic symbols (alternatives)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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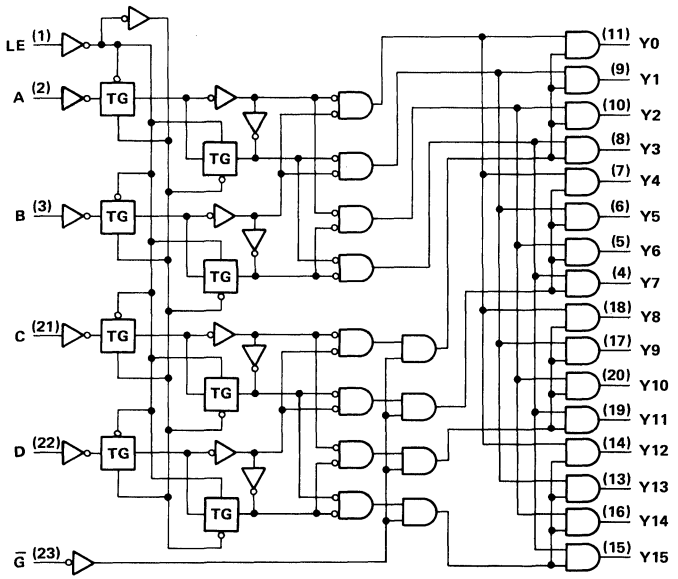
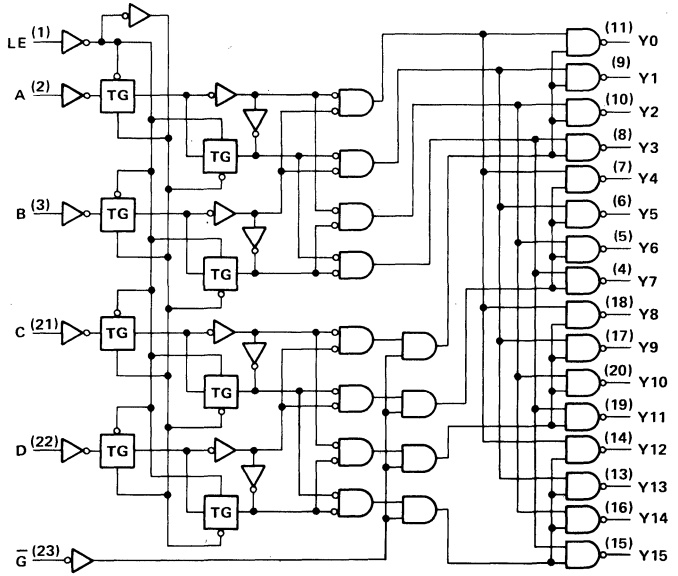
'HC4514 logic diagram (positive logic)



'HC4515 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4514 SN54HC4515			SN74HC4514 SN74HC4515			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4514 SN54HC4515		SN74HC4514 SN74HC4515		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	T_A = 25°C		SN54HC4514 SN54HC4515		SN74HC4514 SN74HC4515		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		119		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, A thru D before LE↓	2 V	100		149		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
t_h	Hold time, A thru D before LE↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4514 SN54HC4515		SN74HC4514 SN74HC4515		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A thru D	Any	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{pd}	LE	Any	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{pd}	$\overline{G}$	Any	2 V		88	175		261		221	ns
			4.5 V		18	35		52		44	
			6 V		15	30		44		37	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage**
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable Input Simplifies Expansion**
- **Expandable for N-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

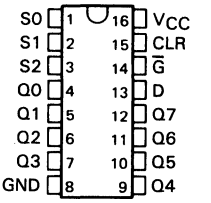
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

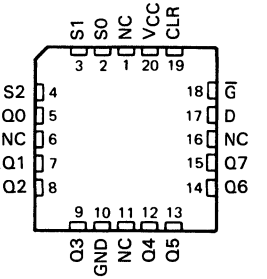
Four distinct modes of operation are selectable by controlling the clear (CLR) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC4724 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4724 is characterized for operation from −40°C to 85°C.

SN54HC4724 . . . J PACKAGE
SN74HC4724 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC4724 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

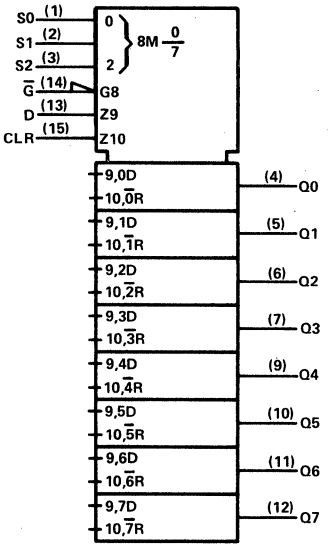
FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLR	$\overline{G}$			
L	L	D	Q_{i0}	Addressable Latch
L	H	Q_{i0}	Q_{i0}	Memory
H	L	D	L	8-Line Demultiplexer
H	H	L	L	Clear

LATCH SELECTION TABLE

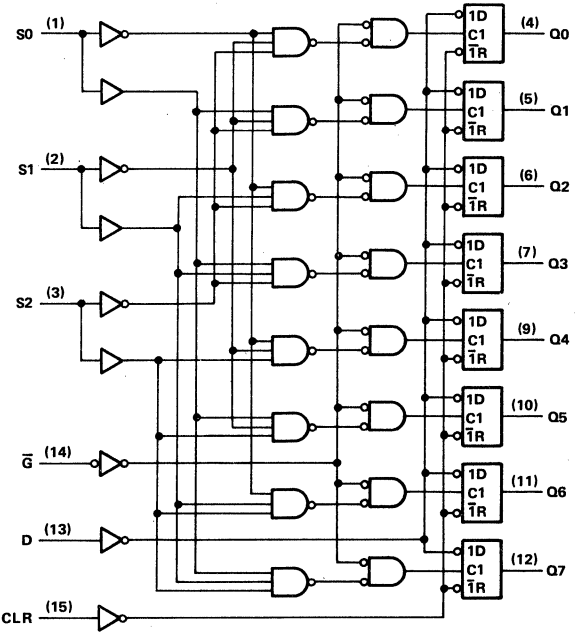
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†



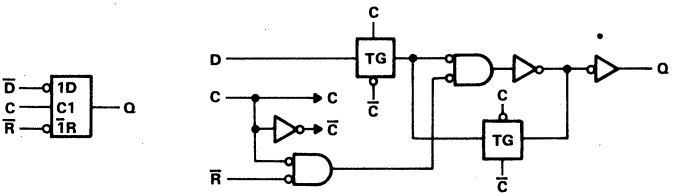
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

logic symbol and logic diagram, each internal latch (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC4724			SN74HC4724			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC4724		SN74HC4724		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC4724		SN74HC4724		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration	CLR high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	$\overline{G}$ low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su} Setup time, data or address before $\overline{G}$↑		2 V	75		115		95		ns
		4.5 V	15		23		19		
		6 V	13		20		16		
t_h Hold time, data or address after $\overline{G}$↑		2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4724		SN74HC4724		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	CLR	Any Q	2 V		60	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_{pd}	Data	Any Q	2 V		56	130		195		165	ns
			4.5 V		17	26		39		33	
			6 V		13	22		33		28	
t_{pd}	Address	Any Q	2 V		74	200		300		250	ns
			4.5 V		21	40		60		50	
			6 V		17	34		51		43	
t_{pd}	$\overline{G}$	Any Q	2 V		66	170		255		215	ns
			4.5 V		20	34		51		43	
			6 V		16	29		43		37	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	33 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- **Operation from Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC08**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

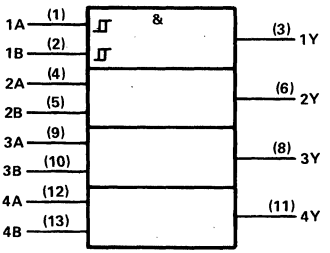
description

Each circuit functions as a quadruple AND gate. They perform the Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

The circuits are temperature compensated and can be triggered from the slowest of input ramps and will still give clean jitter-free output signals.

The SN54HC7001 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7001 is characterized for operation from −40°C to 85°C.

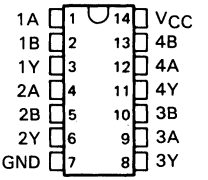
logic symbol†



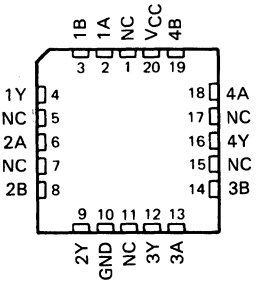
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC7001 . . . J PACKAGE
SN74HC7001 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7001 . . . FK PACKAGE
(TOP VIEW)

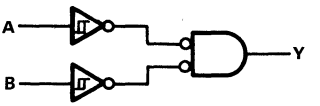


NC—No internal connection

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7001			SN74HC7001			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7001		SN74HC7001		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}		2 V	0.70	1.2	1.50	0.70	1.50	0.70	1.50	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
		6 V	2.10	3.3	4.20	2.10	4.20	2.10	4.20	
V_{T-}		2 V	0.30	0.6	1.00	0.30	1.00	0.30	1.00	V
		4.5 V	0.90	1.6	2.45	0.90	2.45	0.90	2.45	
		6 V	1.20	2.0	3.20	1.20	3.20	1.20	3.20	
$V_{T+} - V_{T-}$		2 V	0.20	0.6	1.20	0.20	1.20	0.20	1.20	V
		4.5 V	0.40	0.9	2.10	0.40	2.10	0.40	2.10	
		6 V	0.50	1.3	2.50	0.50	2.50	0.50	2.50	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7001		SN74HC7001		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- **Operation from Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC36**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

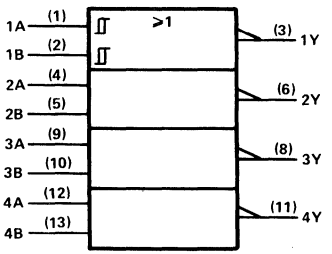
description

Each circuit functions as a quadruple NOR gate. They perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

The circuits are temperature compensated and can be triggered from the slowest of input ramps and will still give clean jitter-free output signals.

The SN54HC7002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7002 is characterized for operation from −40°C to 85°C.

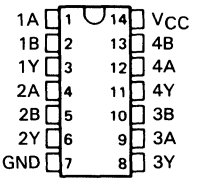
logic symbol†



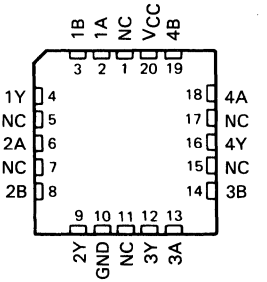
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC7002 . . . J PACKAGE
SN74HC7002 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7002 . . . FK PACKAGE
(TOP VIEW)

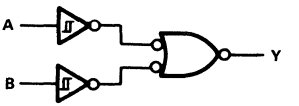


NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7002			SN74HC7002			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		−55		125	−40		85	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7002		SN74HC7002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}		2 V	0.70	1.2	1.50	0.70	1.50	0.70	1.50	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
		6 V	2.10	3.3	4.20	2.10	4.20	2.10	4.20	
V_{T-}		2 V	0.30	0.6	1.00	0.30	1.00	0.30	1.00	V
		4.5 V	0.90	1.6	2.45	0.90	2.45	0.90	2.45	
		6 V	1.20	2.0	3.20	1.20	3.20	1.20	3.20	
$V_{T+} - V_{T-}$		2 V	0.20	0.6	1.20	0.20	1.20	0.20	1.20	V
		4.5 V	0.40	0.9	2.10	0.40	2.10	0.40	2.10	
		6 V	0.50	1.3	2.50	0.50	2.50	0.50	2.50	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7002		SN74HC7002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

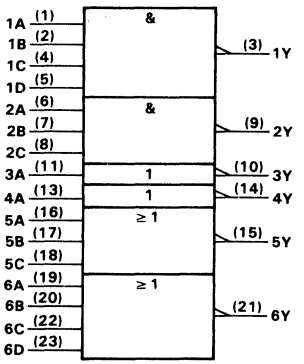
The SN54HC7006 and SN74HC7006 are each comprised of the following sections:

One 3-input NAND gate
One 4-input NAND gate
One 3-input NOR gate
One 4-input NOR gate
Two inverters

They perform the Boolean functions shown under each function table.

The SN54HC7006 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7006 is characterized for operation from −40°C to 85°C.

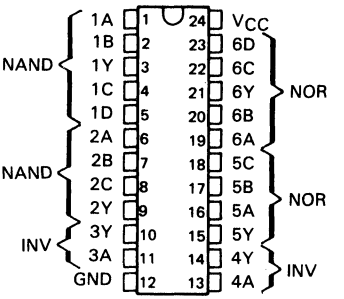
logic symbol†



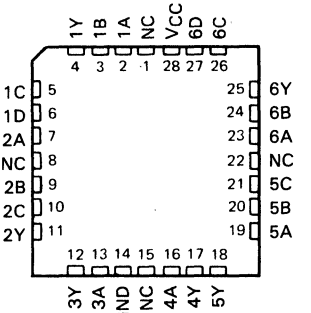
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

SN54HC7006 . . . JT PACKAGE
SN74HC7006 . . . DW OR NT PACKAGE
(TOP VIEW)



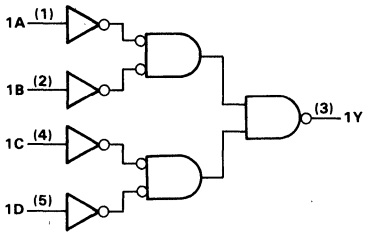
SN54HC7006 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagrams (positive logic)

4-INPUT NAND GATE

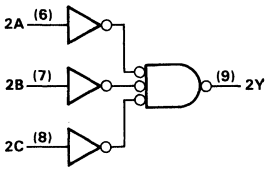


FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

positive logic: $Y = \overline{A \cdot B \cdot C \cdot D}$ or
$Y = \overline{A}+\overline{B}+\overline{C}+\overline{D}$

3-INPUT NAND GATE

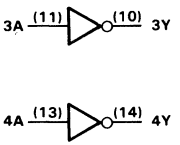


FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

positive logic: $Y = \overline{A \cdot B \cdot C}$ or
$Y = \overline{A}+\overline{B}+\overline{C}$

INVERTERS

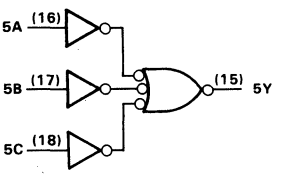


FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

3-INPUT NOR GATE



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

positive logic: $Y = \overline{A+B+C}$ or
$Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$

Pin numbers shown are for DW, JT, and NT packages.

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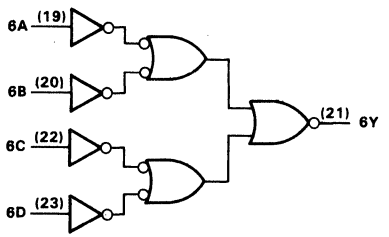
logic diagram (positive logic)

4-INPUT NOR GATE



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

positive logic: $Y = \overline{A+B+C+D}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7006			SN74HC7006			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7006		SN74HC7006		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

NAND/NOR gates

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7006		SN74HC7006		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C or D	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

inverters

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7006		SN74HC7006		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		45	95		145		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2880, MARCH 1985—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

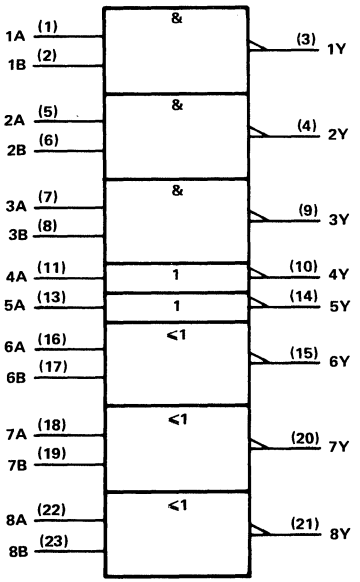
The SN54HC7008 and SN74HC7008 are each comprised of the following sections:

Three 2-input NAND gates
Three 2-input NOR gates
Two inverters

They perform the Boolean functions shown under each function table.

The SN54HC7008 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7008 is characterized for operation from −40°C to 85°C.

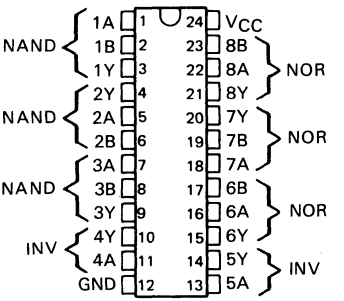
logic symbol†



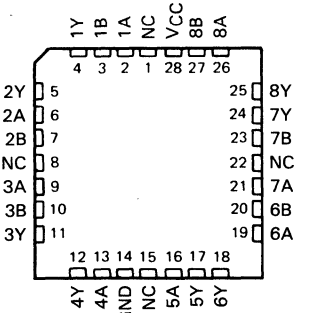
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

SN54HC70008 . . . JT PACKAGE
SN74HC7008 . . . DW OR NT PACKAGE
(TOP VIEW)



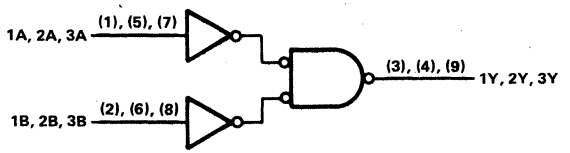
SN54HC7008 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagrams (positive logic)

2-INPUT NAND GATES



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

positive logic: $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

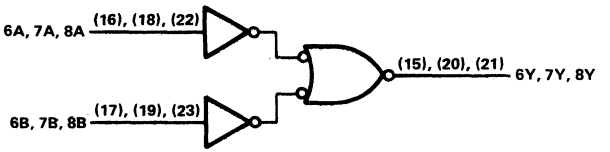
INVERTERS

FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

2-INPUT NOR GATES



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic: $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7008			SN74HC7008			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7008		SN74HC7008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

NAND/NOR gates

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7008		SN74HC7008		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

inverters

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7008		SN74HC7008		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		45	95		145		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- **Carry-Out Output for Cascading**
- **Divide-by-N Counting**
- **DC Clock Input Circuit Allows Slow Rise Times**
- **Power-Up Reset**
- **Pin-Out Compatible with 'HC4022**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

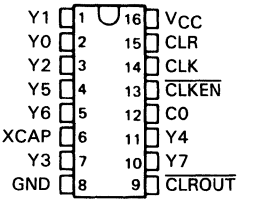
The 'HC7022 is a four-stage divide-by-8 Johnson counter with eight decoder outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson octal counter configuration.

The eight decoder outputs are normally low and go high only at their respective octal time periods. A high signal on CLR asynchronously clears the octal counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output C0 is high while Y0, Y1, Y2, or Y3 is high, then is low while Y4, Y5, Y6, or Y7 is high.

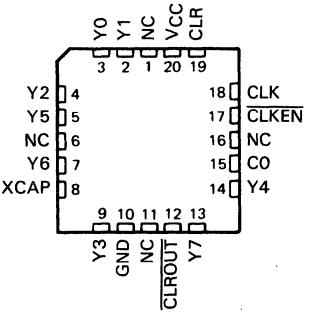
This part is similar to the 'HC4022; the main difference is that it includes a power-up-clear circuit to reset the counter during the power-up of the device. The active-low open-drain clear output, $\overline{\text{CLROUT}}$, can be used to clear or rest external circuitry. The pulse duration of the power-up reset circuit can be controlled with an external capacitor C_{ext} connected to pin XCAP. If XCAP is connected to V_{CC}, the power-up reset function is bypassed.

The SN54HC7022 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7022 is characterized for operation from −40°C to 85°C.

SN54HC7022 . . . J PACKAGE
SN74HC7022 . . . DW OR N PACKAGE
(TOP VIEW)

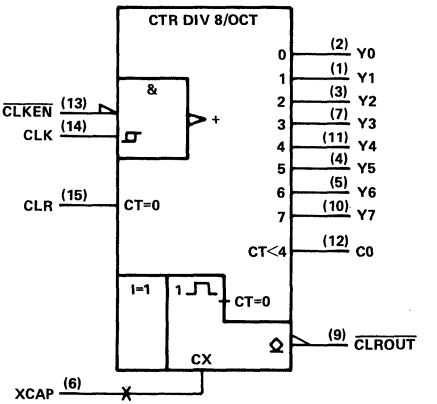


SN54HC7022 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

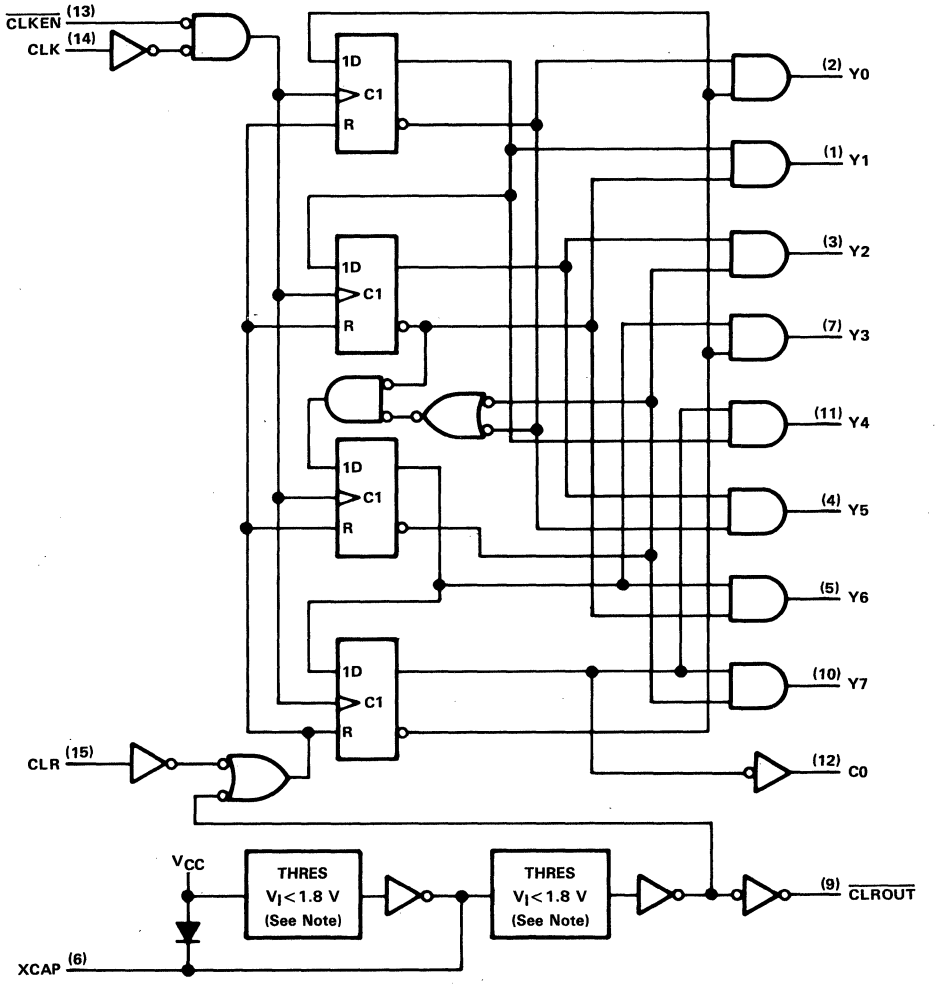
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

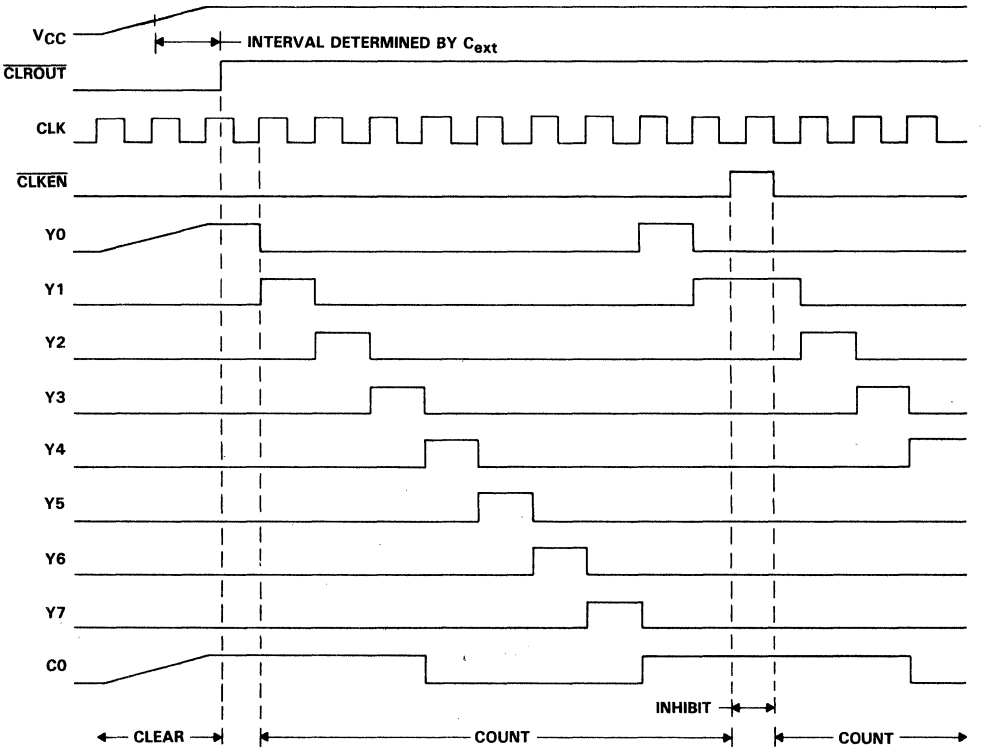
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Note: The output of each threshold detector is logically high until the input voltage exceeds the threshold level, typically 1.7 volts.
Pin numbers shown are for DW, J, and N packages.

typical power-up clear, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7022			SN74HC7022			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7022		SN74HC7022		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH} (Totem-pole outputs)	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
I_{OH} (Open-drain outputs)	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

TEXAS INSTRUMENTS
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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7022		SN74HC7022		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLK† or $\overline{CLKEN}$‡	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low† or $\overline{CLKEN}$ high or low‡	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	$\overline{CLKEN}$ low before CLK↑† or CLK high before $\overline{CLKEN}$↓‡	2 V	50		75		63		ns
			4.5 V	10		15		13		
			6V	9		13		11		
		CLR inactive before CLK↑‡ $\overline{CLKEN}$↓‡	2 V	50		75		63		
			4.5 V	10		15		13		
			6 V	9		13		11		
t_h	Hold time	$\overline{CLKEN}$ low after CLK↑† or CLK high after $\overline{CLKEN}$↓‡	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6V	5		5		5		

†These conditions apply if clocking is being performed via the CLK input.
‡These conditions apply if clocking is being performed via the $\overline{CLKEN}$ input.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7022		SN74HC7022		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	55		25		29		
t_{pd}	CLK	Any Y or CO	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{pd}	$\overline{CLKEN}$	Any Y or CO	2 V		125	250		373		315	ns
			4.5 V		25	50		75		63	
			6 V		21	43		63		54	
t_{pd}	CLR	Any Y	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{PLH}	CLR	CO	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_t		Any output	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- Operation from Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC32
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

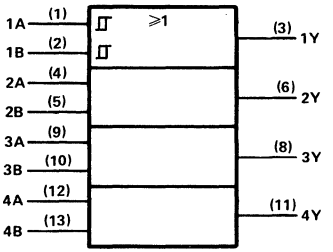
description

Each circuit functions as a quadruple OR gate. They perform the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

The circuits are temperature compensated and can be triggered from the slowest of input ramps and will still give clean jitter-free output signals.

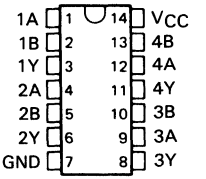
The SN54HC7032 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7032 is characterized for operation from −40°C to 85°C.

logic symbol†

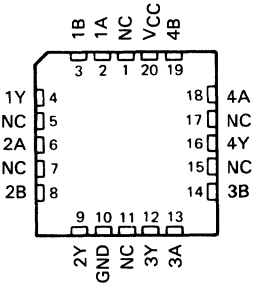


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC7032 . . . J PACKAGE
SN74HC7032 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7032 . . . FK PACKAGE
(TOP VIEW)

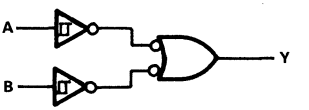


NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7032			SN74HC7032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7032		SN74HC7032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}		2 V	0.70	1.2	1.50	0.70	1.50	0.70	1.50	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
		6 V	2.10	3.3	4.20	2.10	4.20	2.10	4.20	
V_{T-}		2 V	0.30	0.6	1.00	0.30	1.00	0.30	1.00	V
		4.5 V	0.90	1.6	2.45	0.90	2.45	0.90	2.45	
		6 V	1.20	2.0	3.20	1.20	3.20	1.20	3.20	
$V_{T+} - V_{T-}$		2 V	0.20	0.6	1.20	0.20	1.20	0.20	1.20	V
		4.5 V	0.40	0.9	2.10	0.40	2.10	0.40	2.10	
		6 V	0.50	1.3	2.50	0.50	2.50	0.50	2.50	
I_I	V_I = V_{CC} or 0	6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7032		SN74HC7032		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- **Contains D-type Flip-Flops with Preset and Clear, NAND, NOR, and Inverter Gates**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54HC7074 and SN74HC7074 are each comprised of the following sections:

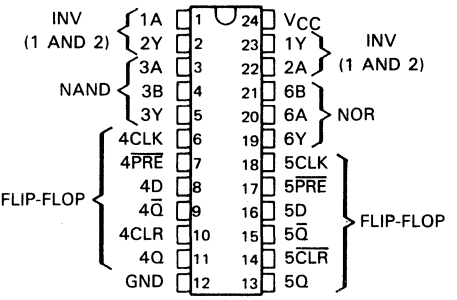
Two inverters
One 2-input NOR gate
One 2-input NAND gate
Two D-type flip-flops

They perform the Boolean functions shown under the respective function table.

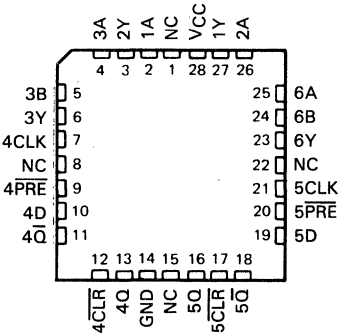
The D-type flip-flops are positive-edge-triggered and are functionally similar to the SN54HC74 and SN74HC74. A low level at the $\overline{PRE}$ or $\overline{CLR}$ inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HC7074 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7074 is characterized for operation from −40°C to 85°C.

SN54HC7074 . . . JT PACKAGE
SN74HC7074 . . . DW OR NT PACKAGE
(TOP VIEW)

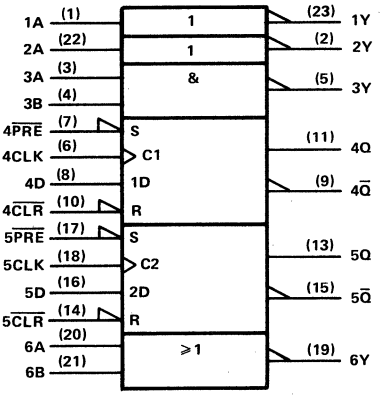


SN54HC7074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

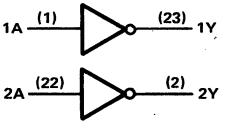
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

INVERTERS

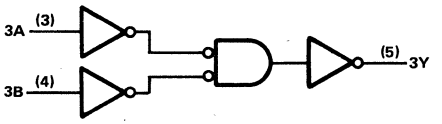


FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

2-INPUT NAND GATE



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

positive logic: $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

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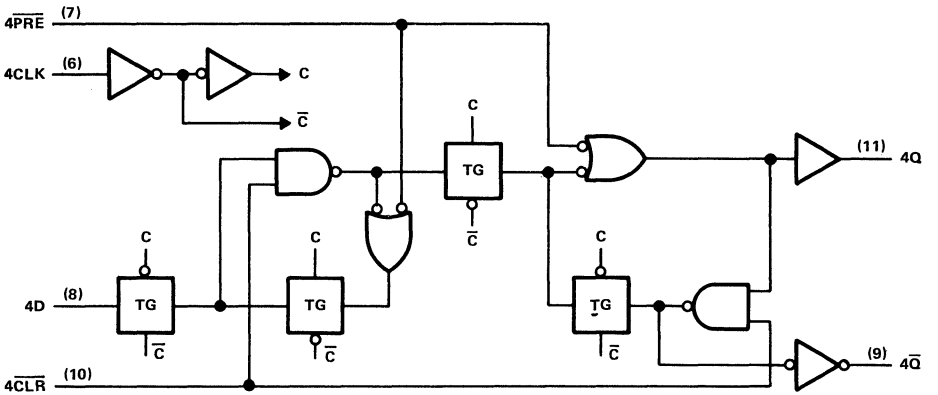
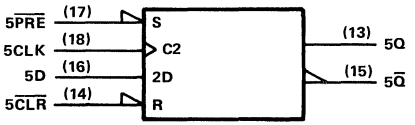
logic diagrams (positive logic)

D-TYPE FLIP-FLOPS





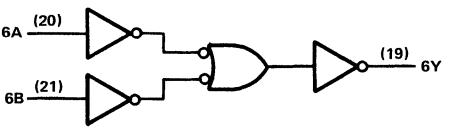
The detail above, and the composite logic symbol to the left, apply to both flip-flops.

FUNCTION TABLE
(EACH D FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; i.e., it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

2-INPUT NOR GATE



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic: $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC} . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC7074			SN74HC7074			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
	V_{CC} = 4.5 V	3.15			3.15			
	V_{CC} = 6 V	4.2			4.2			
V_{IL} Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
	V_{CC} = 4.5 V	0		0.9	0		0.9	
	V_{CC} = 6 V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
	V_{CC} = 4.5 V	0		500	0		500	
	V_{CC} = 6 V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7074		SN74HC7074		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.5	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	31	0	21	0	25	
t_w	Pulse duration	CLK high or CLR low	2 V	90		135		110		ns
			4.5 V	18		26		23		
			6 V	16		24		20		
		$\overline{PRE}$ low or $\overline{CLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ high or $\overline{PRE}$ low	2 V	25		38		31		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.5		MHz
			4.5 V	28	50		19		22		
			6 V	31	60		21		25		
t_{pd}	CLK	Q or $\overline{Q}$	2 V		45	175		263		219	ns
			4.5 V		15	35		53		44	
			6 V		13	30		45		38	
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		45	230		345		288	ns
			4.5 V		15	46		69		58	
			6 V		13	39		59		49	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	40 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics for gates and inverters over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7074		SN74HC7074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		24	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		7	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per NAND or NOR gate	No load, T_A = 25°C	27 pF typ
	Power dissipation capacitance per inverter		20 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

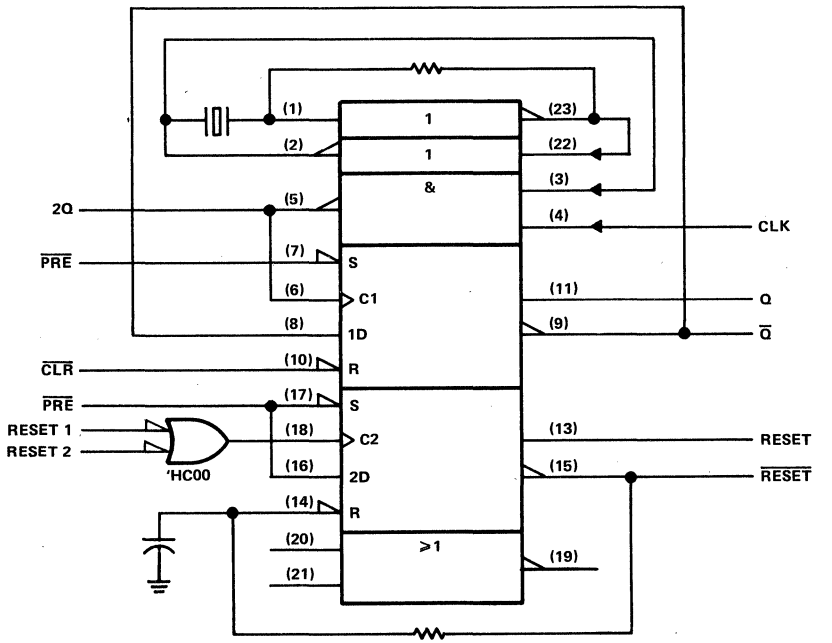

FIGURE 1. CLOCK AND RESET GENERATION FOR MICROPROCESSOR-BASED SYSTEM

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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54HC7075 and SN74HC7075 are each comprised of the following sections:

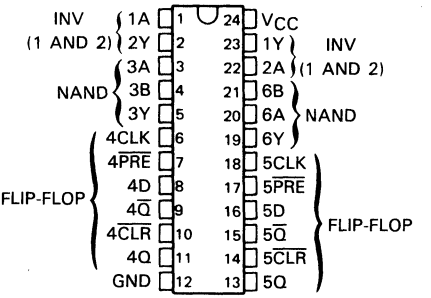
Two inverters
Two 2-input NAND gates
Two D-type flip-flops

They perform the Boolean functions shown under the respective function table.

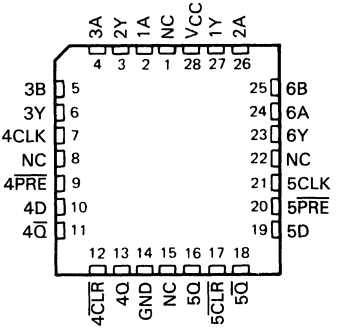
The D-type flip-flops are positive-edge-triggered and are functionally similar to the SN54HC74 and SN74HC74. A low level at the $\overline{PRE}$ or $\overline{CLR}$ inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ or $\overline{CLR}$ are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HC7075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7075 is characterized for operation from −40°C to 85°C.

SN54HC7075 . . . JT PACKAGE
SN74HC7075 . . . DW OR NT PACKAGE
(TOP VIEW)

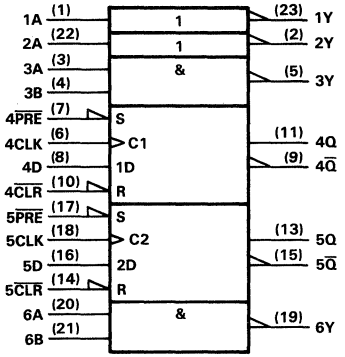


SN54HC7075 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

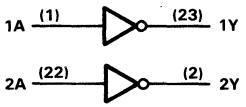
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

INVERTERS

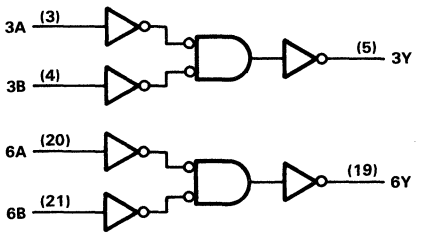


FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

2-INPUT NAND GATES



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

positive logic: $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

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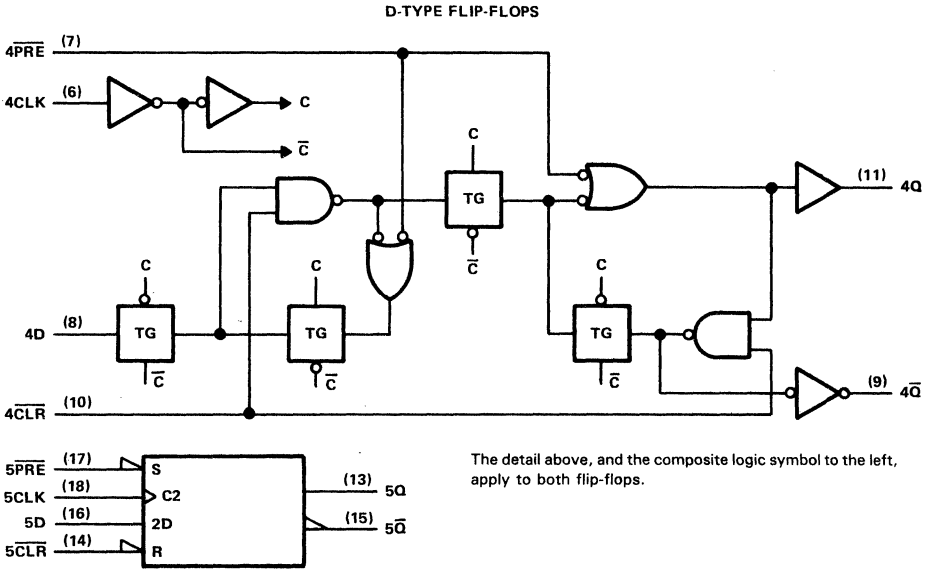
logic diagram (positive logic)



The detail above, and the composite logic symbol to the left, apply to both flip-flops.

FUNCTION TABLE
(EACH D FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable: i.e., it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7075			SN74HC7075			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7075		SN74HC7075		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7075		SN74HC7075		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.5	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	31	0	21	0	25	
t_w	Pulse duration	CLK high or CLK low	2 V	90		135		110		ns
			4.5 V	18		26		23		
			6 V	16		24		20		
		$\overline{PRE}$ low or $\overline{CLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6V	17		25		21		
		$\overline{PRE}$ high or $\overline{CLK}$ high	2 V	25		38		31		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7075		SN74HC7075		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.5		MHz
			4.5 V	28	50		19		22		
			6 V	31	60		21		25		
t_{pd}	CLK	Q or $\overline{Q}$	2 V		45	175		263		219	ns
			4.5 V		15	35		53		44	
			6 V		13	30		45		38	
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		45	230		345		288	ns
			4.5 V		15	46		69		58	
			6 V		13	39		59		49	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	40 pF typ

switching characteristics for gates and inverters over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7075		SN74HC7075		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		24	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		7	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per NAND gate	No load, T_A = 25°C	27 pF typ
	Power dissipation capacitance per inverter		20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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- **Contains D-type Flip-Flops with Preset and Clear, NOR and Inverter Gates**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

The SN54HC7076 and SN74HC7076 are each comprised of the following sections:

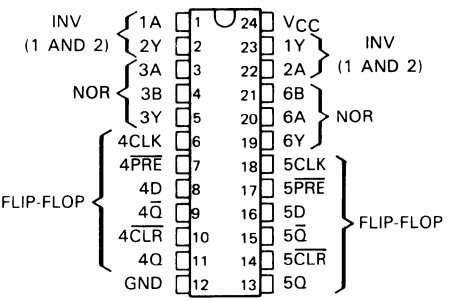
Two inverters
Two 2-input NOR gates
Two D-type flip-flops

They perform the Boolean functions shown under the respective function table.

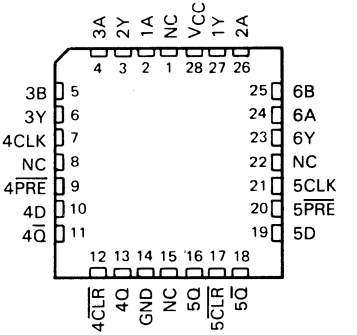
The D-type flip-flops are positive-edge-triggered and are functionally similar to the SN54HC74 and SN74HC74. A low level at the $\overline{PRE}$ or $\overline{CLR}$ inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HC7076 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7076 is characterized for operation from −40°C to 85°C.

SN54HC7076 . . . JT PACKAGE
SN74HC7076 . . . DW OR NT PACKAGE
(TOP VIEW)

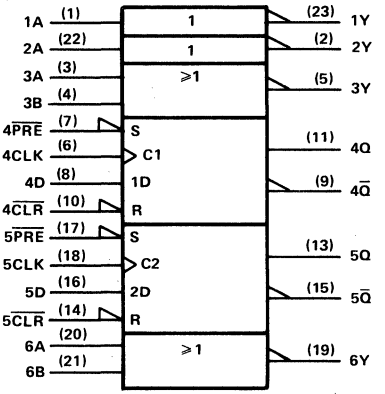


SN54HC7076 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

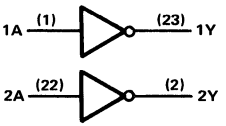
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

INVERTERS

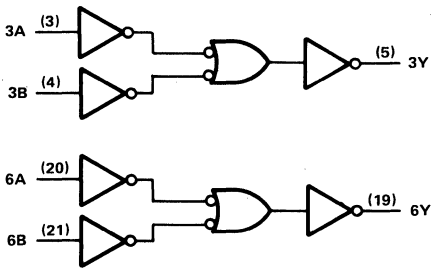


FUNCTION TABLE
(EACH INVERTER)

INPUT	OUTPUT
A	Y
H	L
L	H

positive logic: $Y = \overline{A}$

2-INPUT NOR GATES



FUNCTION TABLE

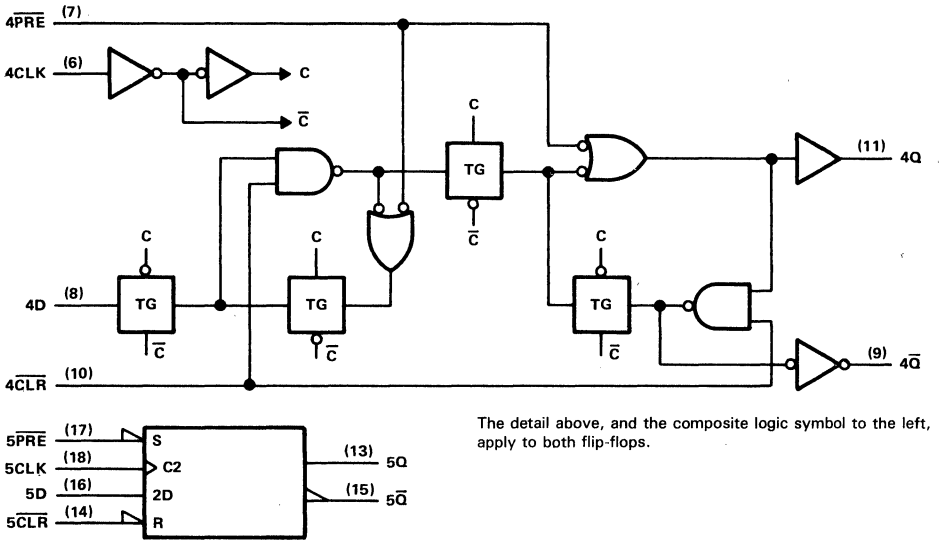
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic: $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

D-TYPE FLIP-FLOPS



The detail above, and the composite logic symbol to the left, apply to both flip-flops.

FUNCTION TABLE
(EACH D FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable: i.e., it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7076			SN74HC7076			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7076		SN74HC7076		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			4		80		40	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7076		SN74HC7076		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.6	0	3.8	0	4.5	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	31	0	21	0	25	
t_w	Pulse duration	CLK high or CLK low	2 V	90		135		110		ns
			4.5 V	18		26		23		
			6 V	16		24		20		
		$\overline{PRE}$ low or $\overline{CLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6V	17		25		21		
		$\overline{PRE}$ high or $\overline{CLR}$ high	2 V	25		38		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4,5 V	5		5		5		
			6 V	5		5		5		

switching characteristics for each D-type flip-flop over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7076		SN74HC7076		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.6	10		3.8		4.5		MHz
			4.5 V	28	50		19		22		
			6 V	31	60		21		25		
t_{pd}	CLK	Q or $\overline{Q}$	2 V		45	175		263		219	ns
			4.5 V		15	35		53		44	
			6 V		13	30		45		38	
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		45	230		345		288	ns
			4.5 V		15	46		69		58	
			6 V		13	39		59		49	

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	40 pF typ

switching characteristics for gates and inverters over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7076		SN74HC7076		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		24	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		7	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per NOR gate	No load, T_A = 25°C	27 pF typ
	Power dissipation capacitance per inverter		20 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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D2804, MARCH 1984—REVISED SEPTEMBER 1987

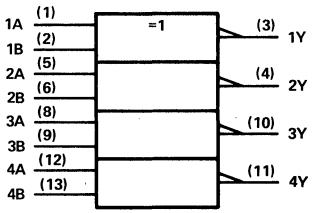
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**
- **Totem-Pole Version of 'HC266**

description

These devices are composed of four independent 2-input exclusive-NOR gates. They perform the Boolean functions:
$Y = \overline{A \oplus B} = \overline{A}\overline{B} + AB$ in positive logic.

The SN54HC7266 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7266 is characterized for operation from −40°C to 85°C.

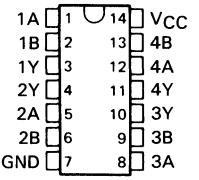
logic symbol†



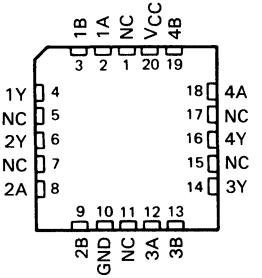
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J or N packages.

logic symbol (each gate, positive logic)

SN54HC7266 . . . J PACKAGE
SN74HC7266 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7266 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

2 HCMOS Devices

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7266			SN74HC7266			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7266		SN74HC7266		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			2		40		20	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7266		SN74HC7266		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	35 pF typ

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

3 Explanation of Logic Symbols†

3.1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in section 3.4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, IEC Technical Committee TC-3 has approved a new document (Publication 617-12) that consolidates the original work started in the mid 1960s and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations, and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables to further help that understanding.

3.2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbol is not significant. As shown in Figure 3-1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 3-1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 3-11.

† Written by F. A. Mann.

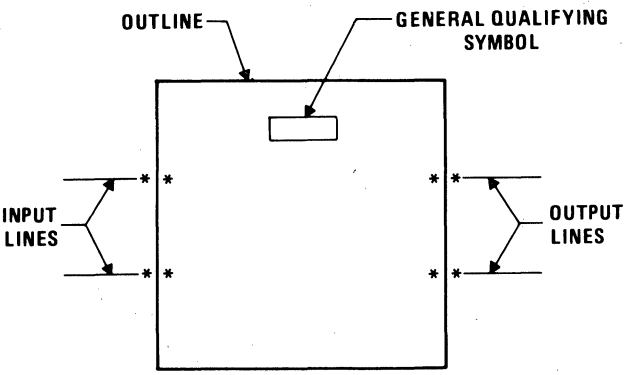


Figure 3-1. Symbol Composition

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols, and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 3-2 shows that, unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition, the common-output element may have other inputs as shown in Figure 3-3. The function of the common-output element must be shown by use of a general qualifying symbol.

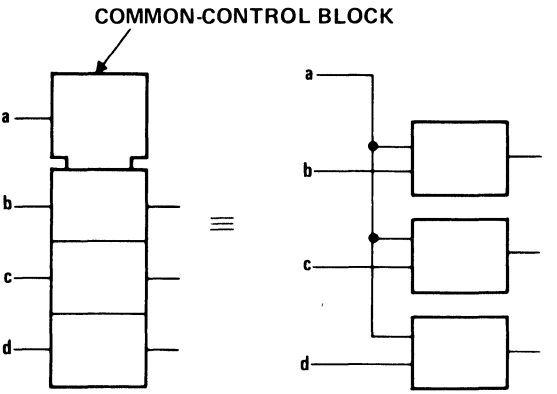


Figure 3-2. Common-Control Block

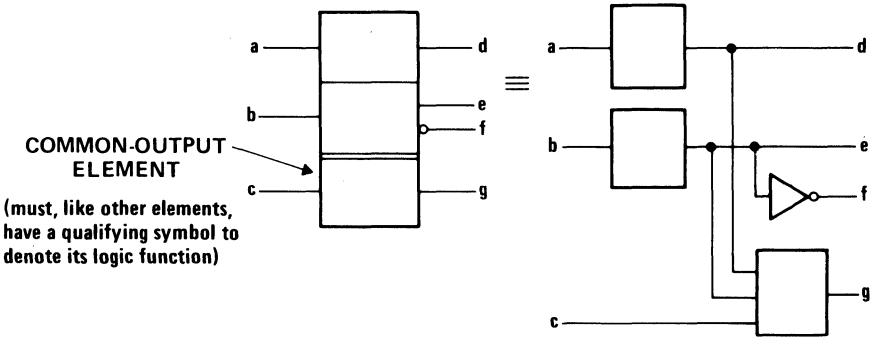


Figure 3-3. Common-Output Element

3.3 Qualifying Symbols

3.3.1 General Qualifying Symbols

Table 3-1 shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

Table 3-1. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k + 1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⊓	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OCT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	*	SN74LS385
CPG	Look-ahead carry generator.	'HC182	SN74182
π	Multiplier.	*	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⌐⌐	Retriggerable monostable.	'HC123	SN74LS422
1⌐⌐	Nonretriggerable monostable (one-shot).	'HC221	SN74121
G ⌐⌐	Astable element. Showing waveform is optional.	*	SN74LS320
!G ⌐⌐	Synchronously starting astable.	*	SN74LS624
G! ⌐⌐	Astable element that stops with a completed pulse.	*	*
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m	'HC4020	*

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table 3-1. General Qualifying Symobls (Continued)

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
ROM	Read-only memory.	*	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	*	SN74LS222
I = 0	Element powers up cleared to 0 state.	*	SN74AS877
I = 1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*	SM74LS608

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

3.3.2 General Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 3-2, and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table 3-2. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line, and, if confusion can arise about the number of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in section 3.4.

Table 3-2. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

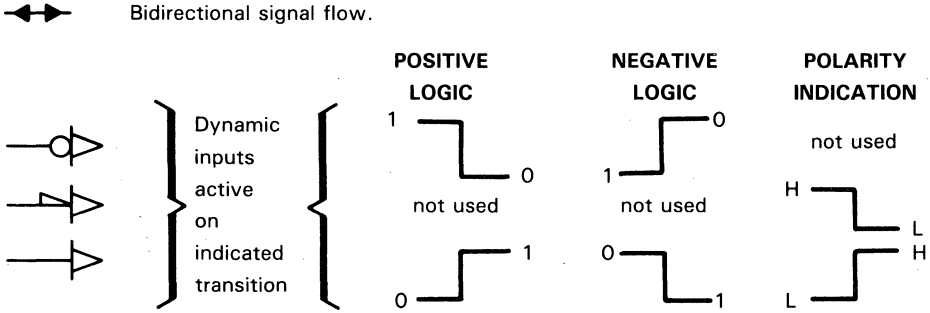
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 3-14).

Input for digital signals (on an analog symbol) (see Figure 3-14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, then these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

3.3.3 Symbols Inside the Outline

Table 3-3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 3.4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state, it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in section 3.8. Binary-weighted inputs are arranged in order, and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document, weights of input and output lines will usually be represented by powers of two only when the binary grouping symbol is used; otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 3-31). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs, and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally, these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 3-3. Symbols Inside the Outline

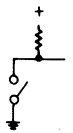
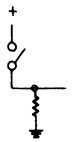
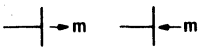
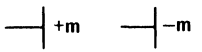
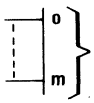
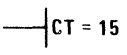
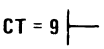
	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See paragraph 3.5.
	Bi-threshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	Three-state output.
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are in the high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S	Usual meanings associated with flip-flops (e.g., R = reset to 0, S = reset to 1).
	Toggle input causes internal state of output to change to its complement.
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.

Table 3-3. Symbols Inside the Outline (Continued)

	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

3.4 Dependency Notation

3.4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined, and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table 3-4 following 3.4.12.

Section	Dependency Type or Other Subject
3.4.2	G, AND
3.4.3	General Rules for Dependency Notation
3.4.4	V, OR
3.4.5	N, Negate (Exclusive-OR)
3.4.6	Z, Interconnection
3.4.7	X, Transmission
3.4.8	C, Control
3.4.9	S, Set and R, Reset
3.4.10	EN, Enable
3.4.11	M, Mode
3.4.12	A, Address

3.4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 3-4 input **b** is ANDed with input **a**, and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

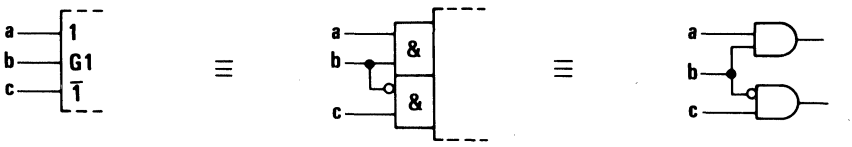


Figure 3-4. G Dependency Between Inputs

In Figure 3-5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 3-6 shows input **a** to be ANDed with a dynamic input **b**.

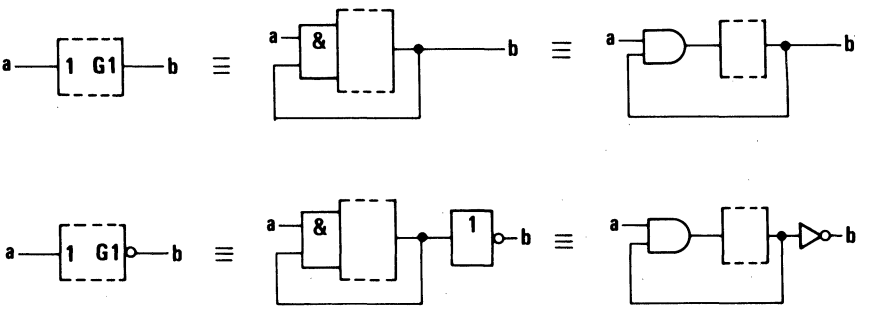


Figure 3-5. G Dependency Between Outputs and Inputs

Figure 3-6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

> When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

3.4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 3-4).

If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR relationship to each other (Figure 3-7).

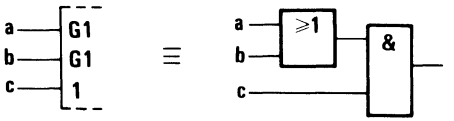


Figure 3-7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 3-15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label

of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 3-15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs may be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 3-8).

Figure 3-8. Substitution for Numbers

3.4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 3-9).

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

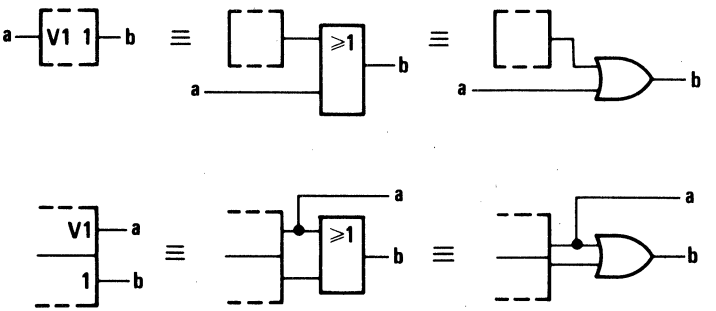


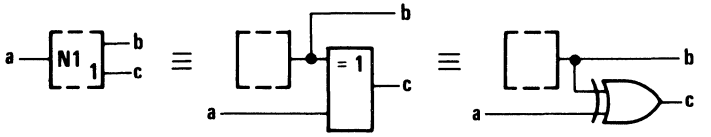
Figure 3-9. V (OR) Dependency

3.4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 3-10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of

what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.



If a = 0, then c = b
If a = 1, then c = $\bar{b}$

Figure 3-10. N (Negate) (Exclusive-OR) Dependency

3.4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 3-11).

3.4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 3-12).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 3-12, 3-13, and 3-14 are omitted.

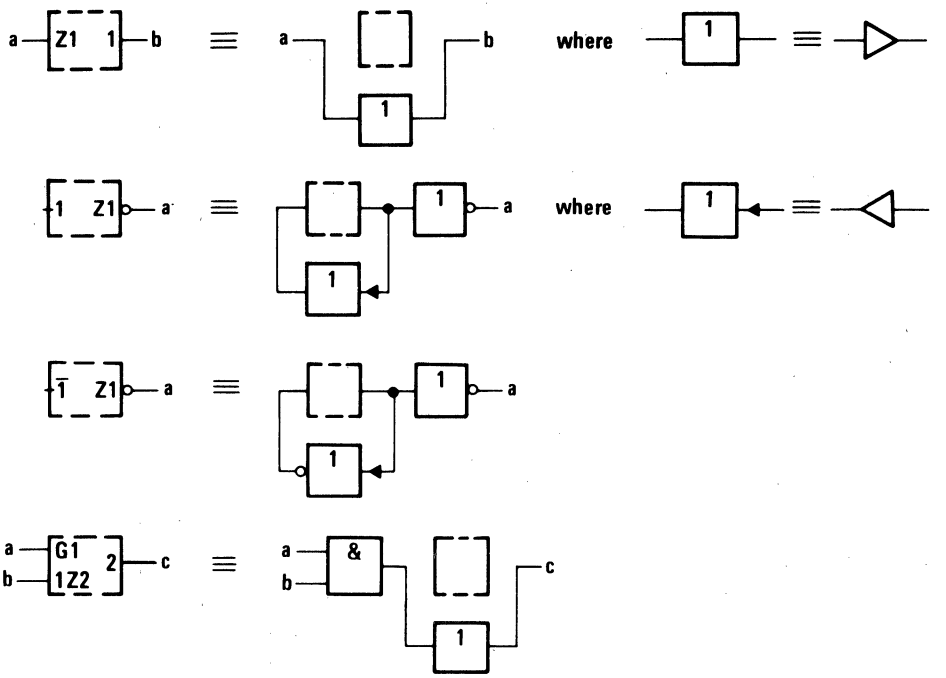
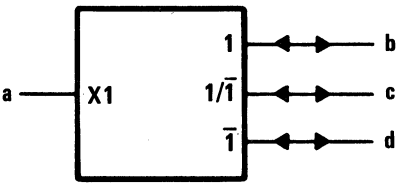


Figure 3-11. Z (Interconnection) Dependency



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 3-12. X (Transmission) Dependency

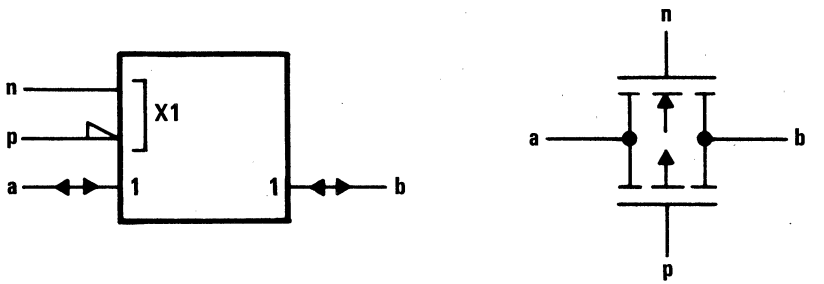


Figure 3-13. CMOS Transmission Gate Symbol and Schematic

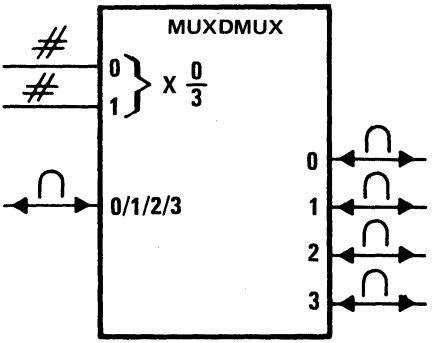


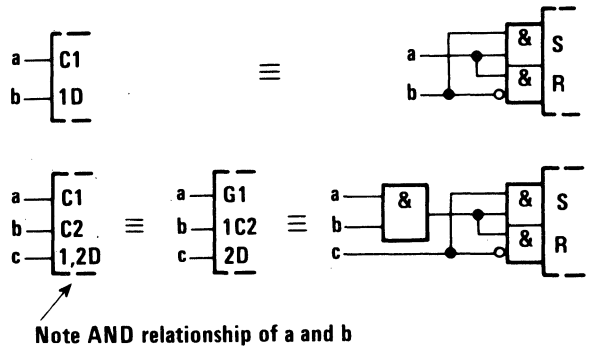
Figure 3-14. Analog Data Selector (Multiplexer/Demultiplexer)

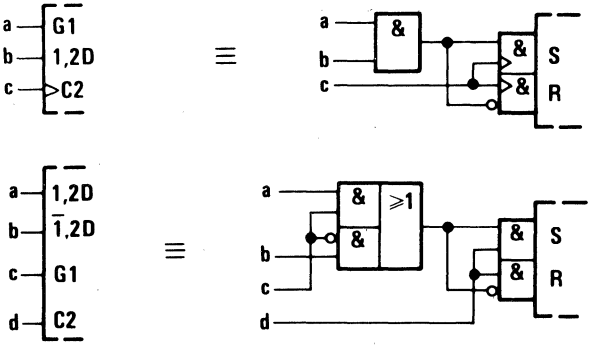
3.4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case, the dynamic input symbol is used as shown in the third example of Figure 3-15.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element; i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.





Input c selects which of a or b is stored when d goes low.

Figure 3-15. C (Control) Dependency

3.4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 3-16 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 3-16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 3-16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.

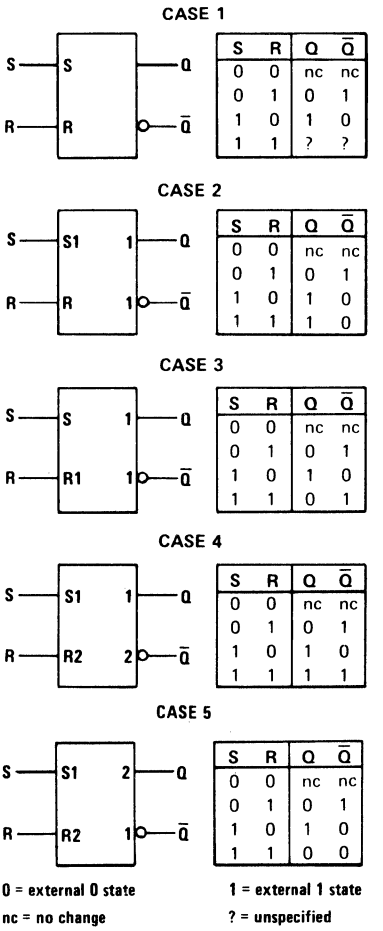
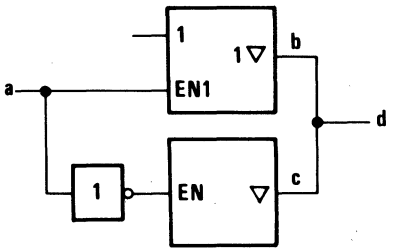


Figure 3-16. S (Set) and R (Reset) Dependencies

3.4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 3-17).



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

Figure 3-17. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element, and the outputs affected by this input stand at their normally defined internal logic states; i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

3.4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

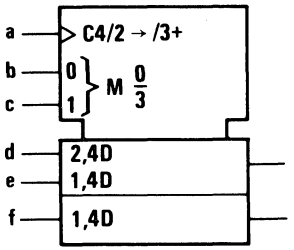
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 3-22).

3.4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element; i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 3-18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading), and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 3-18. M (Mode) Dependency Affecting Inputs

3.4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states; i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 3-19 shows a symbol for a device whose output can behave as either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state, and, in that case, the three-state symbol applies, and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect, and the open-element symbol applies.

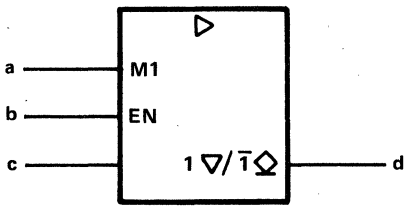


Figure 3-19. Type of Output Determined by Mode

In Figure 3-20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

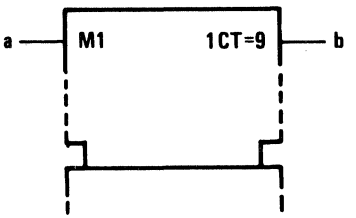


Figure 3-20. An Output of the Common-Control Block

In Figure 3-21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

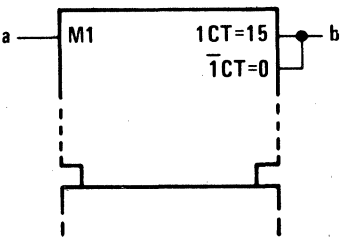


Figure 3-21. Determining an Output's Function

In Figure 3-22, inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

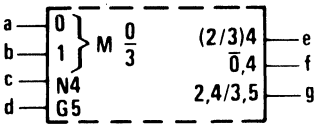


Figure 3-22. Dependent Relationships Affected by Mode

At output **e**, the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1, this output stands at its normally defined state as if it had no labels. At output **f**, the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0, the label set has no effect so the output stands at its normally defined state. In this example, $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g**, there are two label sets: the first set, causing negation (if **c** = 1), is effective only in mode 2; the second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

3.4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multildimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

Figure 3-23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs; i.e., only those enabled by the active EN functions.

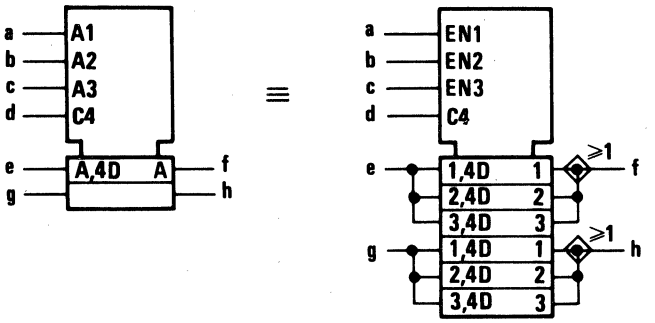


Figure 3-23. A (Address) Dependency

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency inputs (e.g., G, V, N, . . .), because, in the general section presented by the symbol, they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Since they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 3-24 is another illustration of the concept.

3.5 Bistable Elements

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 3-5). The first column shows the essential distinguishing features; the other columns show examples.

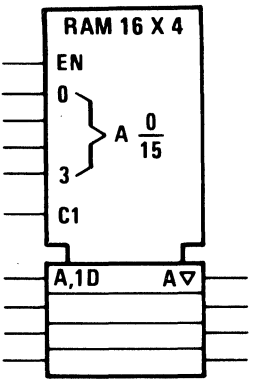


Figure 3-24. Array of 16 Sections of Four Transparent Latches with 3-State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table 3-4. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 3.3.3.

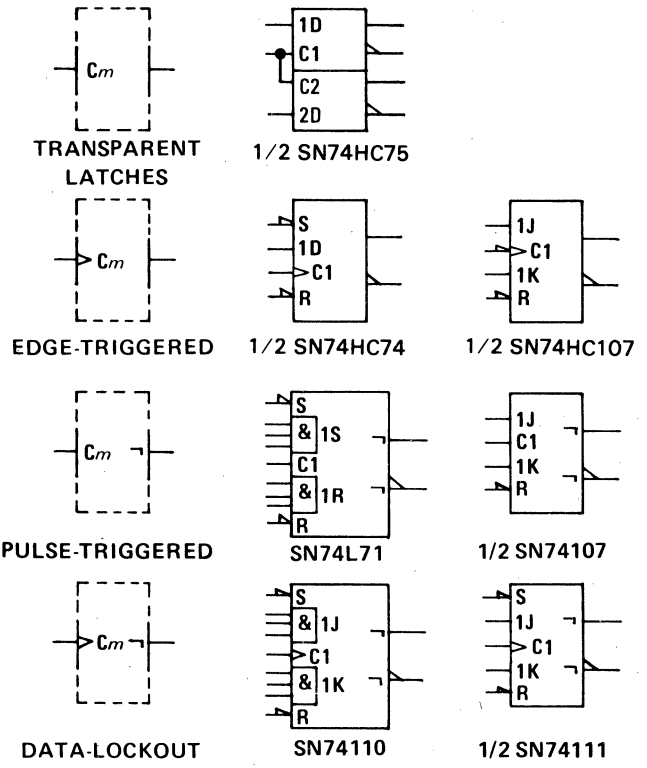


Figure 3-25. Four Types of Bistable Circuits

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lockout element is similar to the pulse-triggered version except that the C input is considered dynamic in that, shortly after C goes through its active transition, the data inputs are disabled, and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

3.6 Coders

The general symbol for a coder or code converter is shown in Figure 3-26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

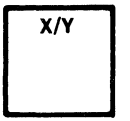


Figure 3-26. Coder General Symbol

Indication of code conversion is based on the following rule:

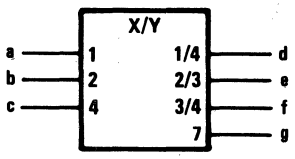
> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case, the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 3-27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency



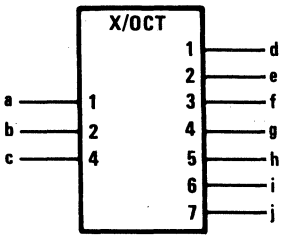
TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 3-27. An X/Y Code Converter

(see section 3.7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by

2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 3-28.



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 3-28. An X/Octal Code Converter

Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.

3.7 Use of a Coder to Produce Affecting Inputs

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case, use can be made of the symbol for a coder as an embedded symbol (Figure 3-29).

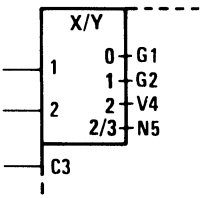


Figure 3-29. Producing Various Types of Dependencies

If all affecting inputs produced by a coder are of the same type as their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 3-30).

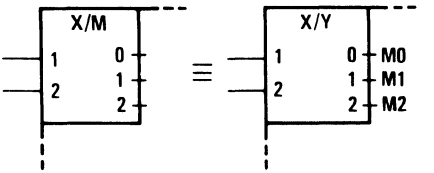


Figure 3-30. Producing One Type of Dependency

3.8 Use of Binary Grouping to Produce Affecting Inputs

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. *k* external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 3-31.

3.9 Sequence of Input Labels

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of

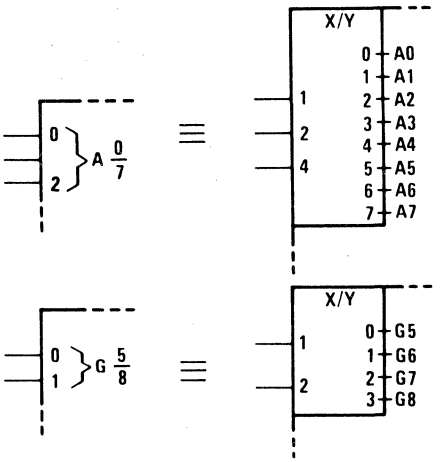


Figure 3-31. Use of the Binary Grouping Symbol

presentation is not advantageous. In those cases, the input may be shown once with the different sets of labels separated by solidi (Figure 3-32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed, and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 3-33).

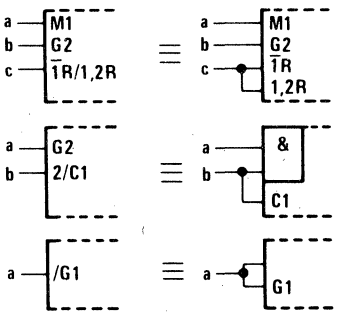


Figure 3-32. Input Labels

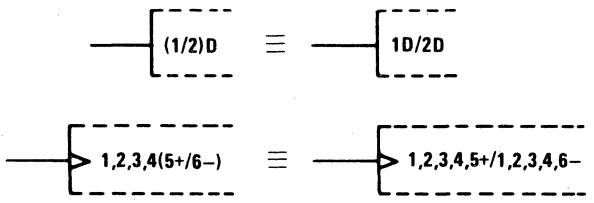


Figure 3-33. Factoring Input Labels

3.10 Sequence of Output Labels

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 3-34).

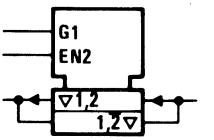


Figure 3-34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases, the output may be shown once with the different sets of labels separated by solidi (Figure 3-35).

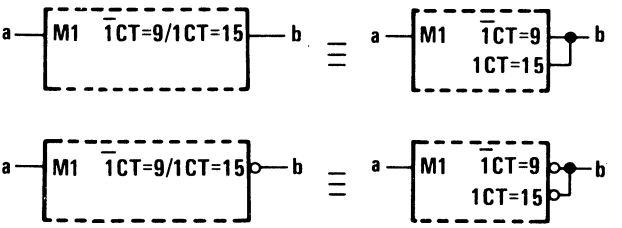


Figure 3-35. Output Labels

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 3-36).

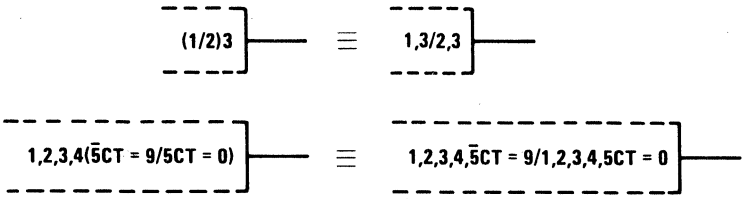


Figure 3-36. Factoring Output Labels

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F.A. Mann, MS 49
P.O. Box 655012
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New York, N.Y. 10018

HCMOS DESIGN CONSIDERATIONS

Present HCMOS data sheets specify, under Recommended Operating Conditions, Input tt = 1000 ns, (10%–90%) for V_{CC} = 2 V. Since devices can be in the threshold region from V_{IL} MAX = 0.3 V to V_{IH} MIN = 1.5 V (this translates into 750 ns), there is a potential for clocked devices to go into the wrong state from any induced ground glitch causing double clocking of the device while in the threshold region. Note that operation of devices with input tt = 1000 ns at V_{CC} = 2 V will not damage the device, however, functionality is not guaranteed for CLK inputs while in the Shift, Count, or Toggle operating modes.

Devices susceptible to the above condition are:

HC107	HC160	HC166	HC194
HC109	HC161	HC190	HC195
HC112	HC163	HC191	HC390
HC113	HC164	HC192	HC393
HC114	HC165	HC193	HC4024

DESIGNER'S INFORMATION

CMOS Circuitry

The elementary CMOS building blocks are the inverter and the transmission gate. Each uses a complementary pair of one n-channel and one p-channel enhancement-type field-effect transistor. Figures 1 and 2 show these together with various logic symbols† used in this book to represent them.

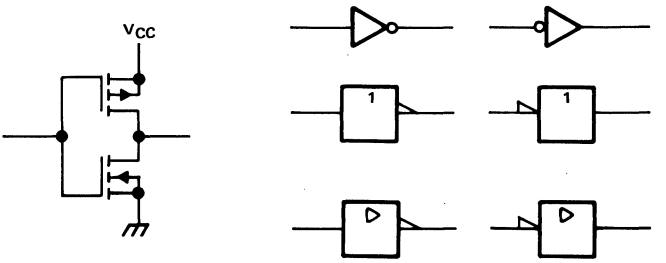


Figure 1. Inverters

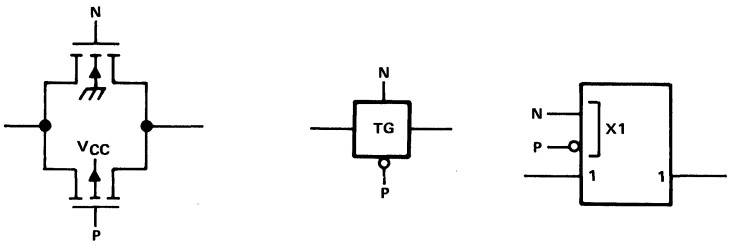


Figure 2. Transmission Gates

Logic gates are created by transistors added in parallel or series to the transistors making up the elementary inverter. Thus the simplest gates are inverting. See Figure 3. An odd number of additional inverters are sometimes added to the outputs of gates to make them noninverting. Basic CMOS gates usually have no more than three inputs. Arrays of gates are used when more than three signals are ANDed or ORed.

The Exclusive-OR or Exclusive-NOR gate is most easily implemented using two inverters and two transmission gates as shown in Figure 4. In complex chains of gates, the inverters may be made unnecessary by complementary signals being already available.

† The various logic symbols are equivalent. The distinctive-shape form of the inverter and gate symbols and the "TG" form of the transmission gate are usually used in the device logic diagrams. The logic inversion symbol (○) is shown at the input or the output, whichever maintains logical consistency with the driving output or the driven input, and this technique is used to indicate the true/complement levels of the signal as it progresses through the circuit. For example, see Figure 7 in this section. The rectangular forms of the inverter and gate symbols and the polarity indicator (◺) replacing the inversion symbol are usually used in this book only in the device logic symbols. The ▷ indicates a high-current output.

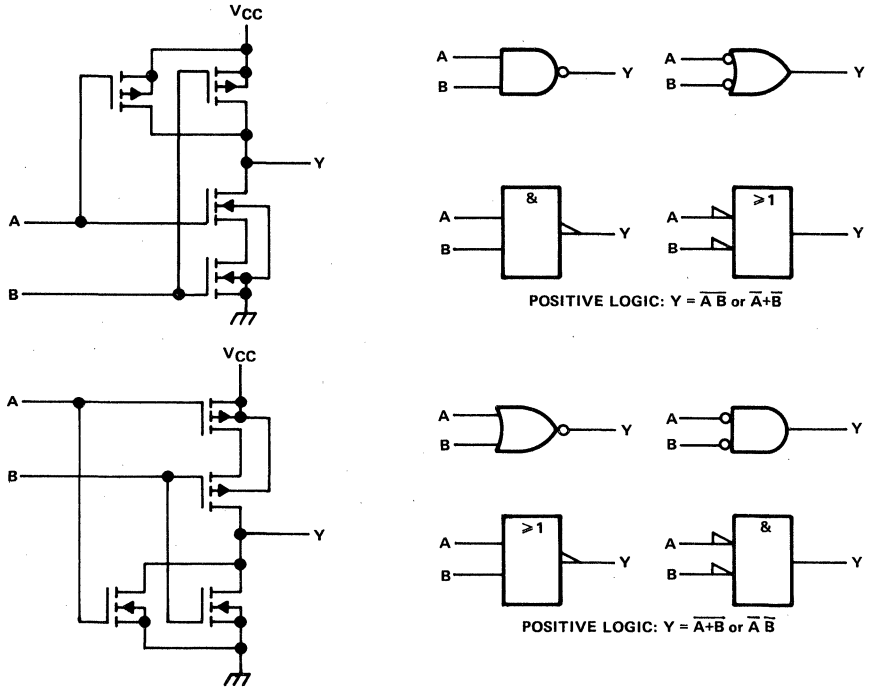


Figure 3. Gates

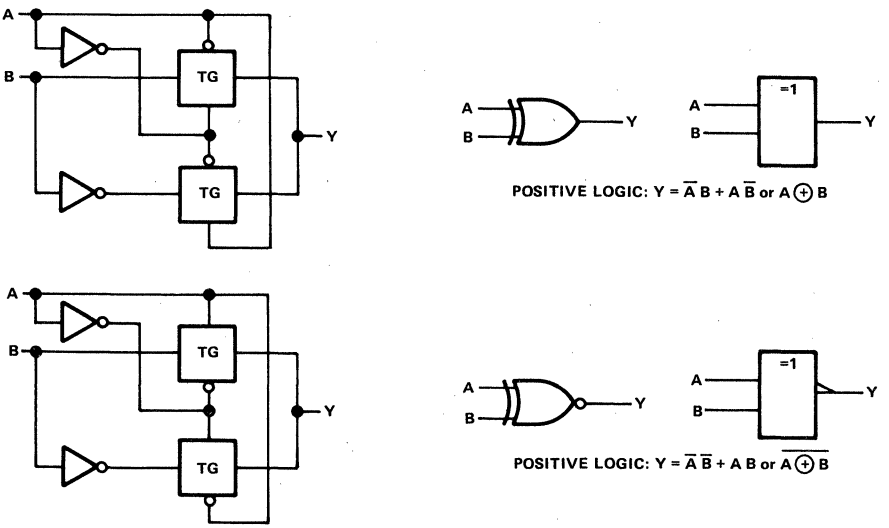


Figure 4. Exclusive-OR/NOR Gates

The three-state output buffer has logic elements in the gate connections to each of the transistors in the final inverter so that both may be turned off under the control of an enable function. Figure 5 illustrates an inverting output buffer.

The transparent latch is typically implemented as shown in Figure 6. This is the simplest form. Logic diagrams in this book show that additional inverters may be added as buffers or to optimize timing. The true and complementary outputs (Q and $\overline{Q}$) may be taken off at other points. Outputs brought out to terminals are always buffered to minimize any feedback effects. The one exception to this is the 'HCU device, which has unbuffered outputs.

Putting two transparent latches in series produces the edge-triggered D-type flip-flop. The inverters can be converted to two-input gates to provide asynchronous set and reset functions. Figure 7 illustrates a negative-edge-triggered circuit. Exchanging the connections of C and $\overline{C}$ produces a positive-edge-triggered version.

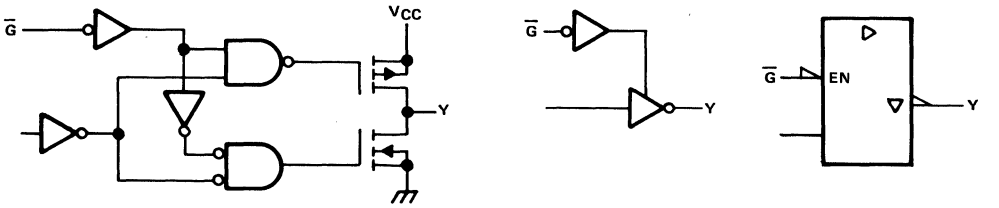


Figure 5. Inverting Three-State Output Buffer with Active-Low Enable

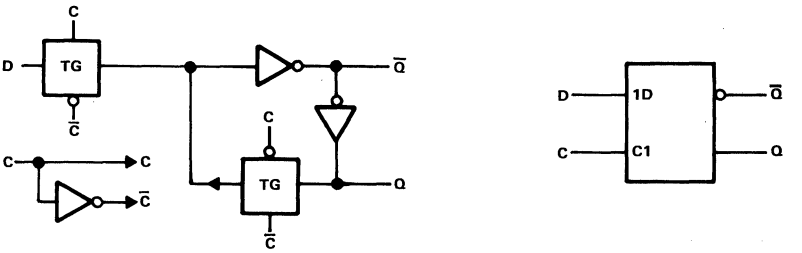


Figure 6. Transparent Latches

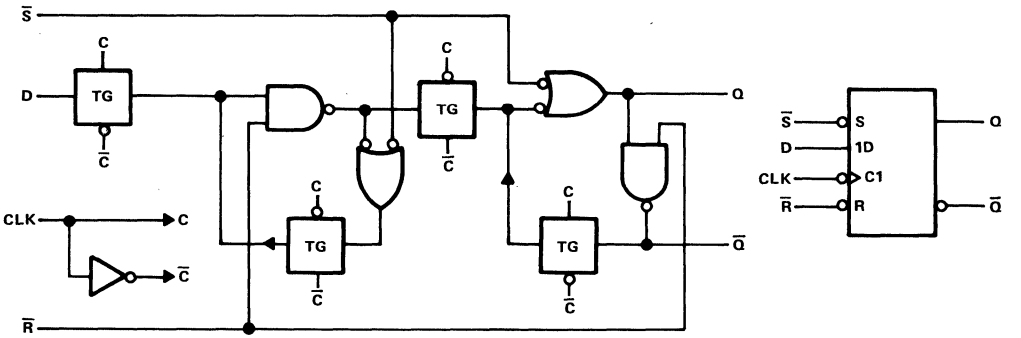


Figure 7. Negative-Edge-Triggered D-Type Flip-Flops

Detailed logic diagrams for flip-flops are given on the data sheets in this book when useful to illustrate special features such as synchronous clearing, J/K inputs, and toggle enabling.

In general the logic diagrams in this book have been simplified. They are believed to correctly indicate the logic implementation but should not be used to predict dynamic performance. Inverters existing in series may be combined or eliminated in the diagram as shown in Figure 8.

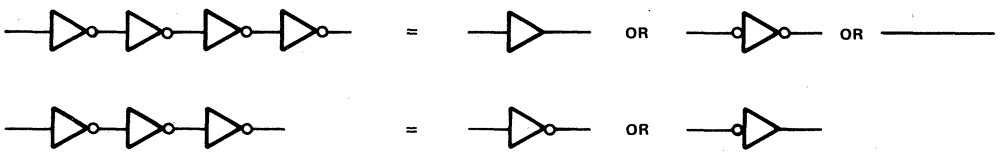


Figure 8. Simplification of Diagrams by Combining Inverters

High-Speed CMOS Characteristics

Table 1 compares the main characteristics of the high-speed CMOS family with those of standard TTL, LSTTL, STTL, ALSTTL, ASTTL, and metal-gate CMOS.

Table 1. Performance Comparison of High-Speed CMOS with Several Other Logic Families

TECHNOLOGY‡	SILICON-GATE CMOS	METAL GATE CMOS	STD TTL	LOW-POWER SCHOTTKY TTL	SCHOTTKY TTL	ADVANCED LOW-POWER SCHOTTKY TTL	ADVANCED SCHOTTKY TTL
Device series	SN74HC	4000	SN74	SN74LS	SN74AS	SN74ALS	SN74AS
Power dissipation per gate (mW)							
Static	0.0000025	0.001	10	2	19	1	8.5
At 100 kHz	0.17	0.1	10	2	19	1	8.5
Propagation delay time (ns) (C_L = 15 pF)	8	105	10	10	3	4	1.5
Maximum clock frequency (MHz) (C_L = 15 pF)	40	12	35	40	125	70	200
Speed/Power product (pJ) (at 100 kHz)	1.4	11	100	20	57	4	13
Minimum output drive (mA) (V_O = 0.4 V)							
Standard outputs	4	1.6	16	8	20	8	20
High-current outputs	6	1.6	48	24	64	24/48	48/64
Fan-out (LS loads)							
Standard outputs	10	4	40	20	50	20	50
High-current outputs	15	4	120	60	160	60/120	120/160
Maximum input current, I_{IL} (mA) (V_I = 0.4 V)	±0.001	−0.001	−1.6	−0.4	−2.0	−0.1	−0.5

‡ Family characteristics at 25 °C, V_{CC} = 5 V; all values typical unless otherwise noted. This table is provided for broad comparisons only. Parameters for specific devices within a family may vary. For detailed comparisons, please consult the appropriate data book.

The major advantages of high-speed CMOS can be summarized as follows:

1. The high-speed CMOS family can operate at speeds comparable to LSTTL. The high-speed CMOS family has ac parameters guaranteed at a supply voltage of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load (also, 150 pF for high-current outputs). Note that at the higher operating frequencies, the power consumption is also comparable to LSTTL (Figure 9).

2. Figure 9 also shows that the high-speed CMOS family covers a wide range of applications: low power drain for low-speed systems, and a slightly higher drain for higher speed systems.

3. Minimum system power — only the gates that are switching contribute to system power consumption. This reduces the size of the power supply required, hence provides lower system cost and improved reliability through lower heat dissipation.

   As mentioned previously, the power consumption for an individual gate at the maximum speed is comparable to LSTTL. However in typical systems, only a fraction of the gates are switching at the clock frequency; therefore, significant power savings can be realized. On a system level where the individual gate switching frequencies are distributed between zero and the system clock frequency (Figure 10), the power saved with high-speed CMOS can be quite significant, as illustrated in Figure 11. The total system power is the area under each curve. The graph in Figure 11 is obtained by multiplying the individual gate characteristics (Figure 9) by the frequency distribution in Figure 10.

4. High-speed CMOS is ideal for battery-operated systems, or systems requiring battery back-up, because there is virtually no static power dissipation (Figure 9).

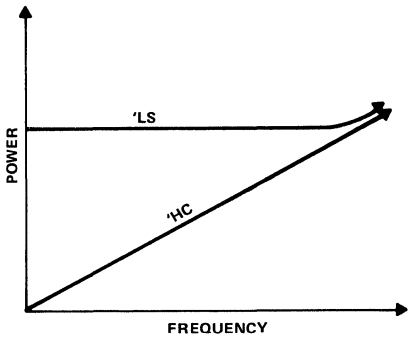


Figure 9. Power Consumed Versus Frequency for High-Speed CMOS Compared to LSTTL

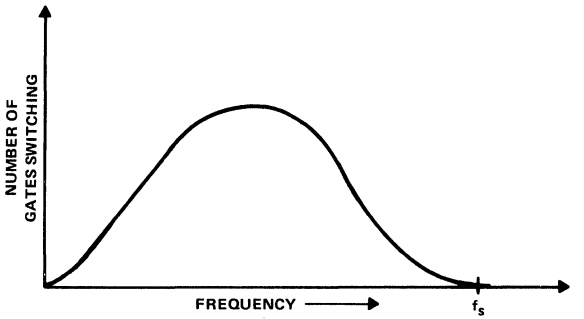


Figure 10. Typical Distribution of Switching Frequencies for Gates within a System with Maximum Clock Frequency, f_S

5. Improved noise immunity over bipolar devices is due to the rail-to-rail (V_{CC} to ground) output voltage swings. Figure 12 illustrates the noise immunity provided by the high-speed CMOS family as it compares to the LSTTL family. This noise immunity makes it ideal for high-noise environments. Minimum and maximum output voltages are guaranteed at 4 mA (6 mA for high-current devices). If the output currents exceed these limits, the noise immunity will be impaired. 'HCT devices have similar input noise margins to LSTTL because their inputs are TTL-voltage compatible. The outputs of 'HCT are the same as standard 'HC outputs.

6. High-speed CMOS devices can drive up to 10 LSTTL loads (15 LSTTL loads for high-current outputs) while maintaining good noise immunity. Although V_{OH}min and V_{OL}max are guaranteed for output currents up to 4 mA (6 mA for high-current outputs), currents up to ±25 mA (±35 mA for high-current outputs) can be obtained to drive LEDs or relays (see Driving LEDs and Relays in this section.)

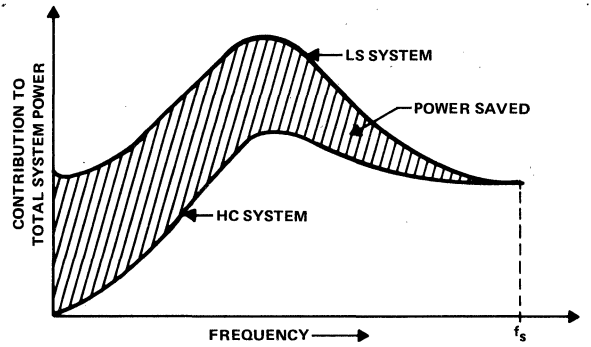


Figure 11. Contribution to Total Power by Gates Running at Frequencies from 0 to f_s

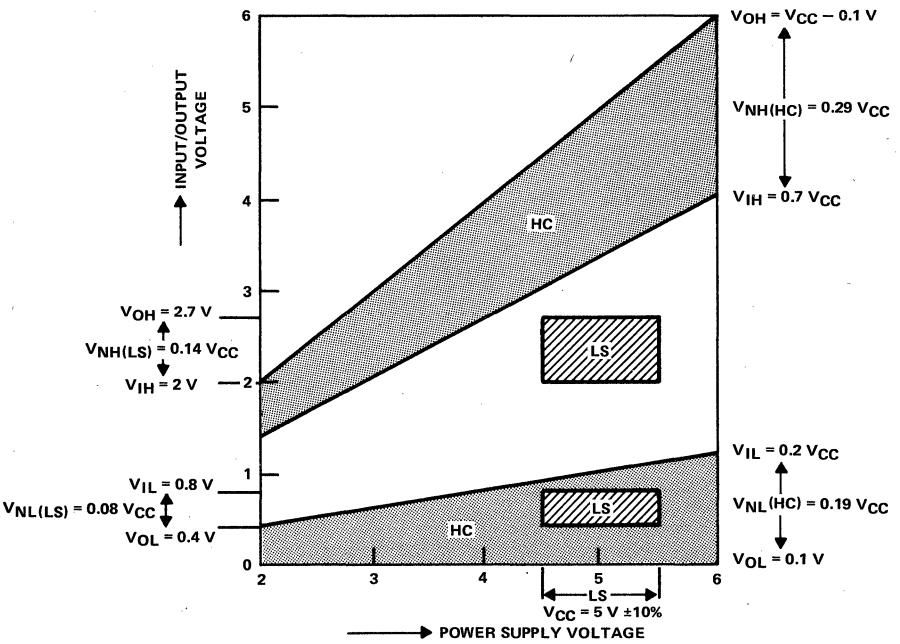


Figure 12. High-Speed CMOS and LS Noise Margins

7. High-speed CMOS devices are guaranteed over an extended temperature range:

SN54HC/HCT'	−55 °C to 125 °C	(military)
SN74HC/HCT'	−40 °C to 85 °C	(industrial)

All specified ac and dc characteristics are guaranteed over this range with the exception of Power Dissipation Capacitance (C_{pd}), which is specified as a typical value at 25 °C.

Protection Circuitry

Electrostatic discharge (ESD) and latch-up are two traditional causes of CMOS device failure. In order to protect HCMOS devices from ESD and latch-up, additional circuitry has been implemented on the inputs and outputs.

ESD PROTECTION

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. The end effect is the ESD causes a short between the two surfaces. These damaged devices (walking-wounded) may still pass normal data sheet tests, but will eventually fail. The unique input protection circuitry designed by Texas Instruments provides immunity to typically 4500 V on the inputs and 3000 V on the outputs, which exceeds MIL-STD-883B, Method 3015, requirements for ESD protection (2000 V, 1.5 kΩ, 100 pF).

Figure 13 shows the circuitry implemented to provide protection for the input gates against ESD. The diode is forward biased for input voltages greater than V_{CC} + 0.5 V. The two transistors and resistor (actually one transistor diffused across a resistor) act as a resistor-diode network against negative-going transients. As illustrated in Figure 14, the ESD protection for the output consists of an additional diffused diode (D3) from the output to V_{CC}. The other diodes (D1 and D2) are parasitics. For further information on handling CMOS devices, see Guidelines for Handling ESDS Devices and Assemblies in this section.

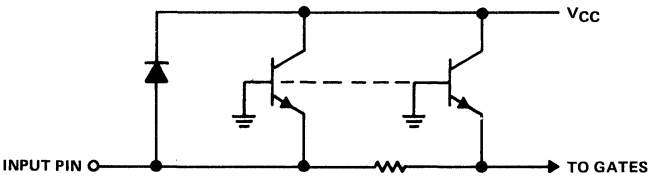


Figure 13. ESD Input Protection Circuitry

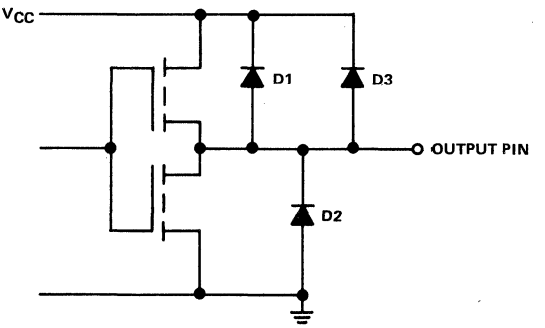


Figure 14. ESD Output Protection Circuitry. D1 and D2 are Parasitic Diodes

LATCH-UP PROTECTION

Internal to most all CMOS devices are two parasitic bipolar transistors; one p-n-p and one n-p-n. Figure 15 shows the cross section of a typical CMOS inverter with the parasitic bipolar transistors. Note that, as shown in Figure 16, these parasitic bipolar transistors are naturally configured as a thyristor or SCR. These transistors conduct when one or more of the p-n junctions become forward biased. When this happens, each parasitic transistor supplies the necessary base current for the other to remain in saturation. This is known as the "latch-up" condition and could possibly destroy the device if the supply current is not limited.

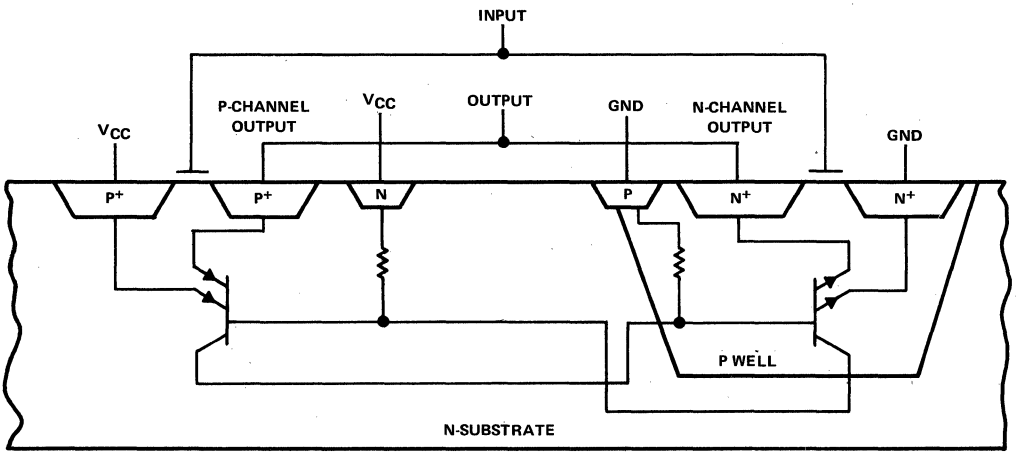


Figure 15. Parasitic Bipolar Transistors in CMOS

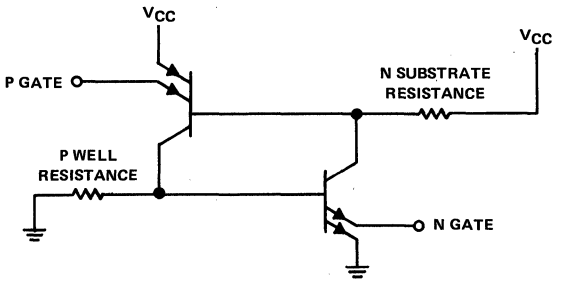


Figure 16. Schematic of Parasitic SCR — P Gate and N Gate Electrodes are Connected Together

A conventional thyristor is fired (turned on) by applying a voltage to the base of the n-p-n transistor, but the parasitic CMOS thyristor is fired by applying a voltage to the emitter of either transistor. One emitter of the p-n-p transistor is connected to an emitter of the n-p-n transistor, which is also the output of the CMOS gate. The other two emitters of the p-n-p and n-p-n transistors are connected to V_{CC} and ground, respectively. Therefore, to trigger the thyristor there must be a voltage greater than V_{CC} + 0.5 V or less than −0.5 V and there has to be sufficient current to cause the latch-up condition.

Latch-up cannot be completely eliminated! The alternative is to impede the thyristor from triggering. Texas Instruments has improved the circuit design by adding four additional diffusions or guard rings alternately connected to V_{CC} and ground as shown in Figure 17. The guard rings provide isolation between the device pins and any p-n junction that is not isolated by a transistor gate. All internal p-n junctions are separated by two guard rings. Tests have shown effective latch-up protection ranges from 450 mA to greater than 1 A at 25 °C, and typically greater than 250 mA at 125 °C.

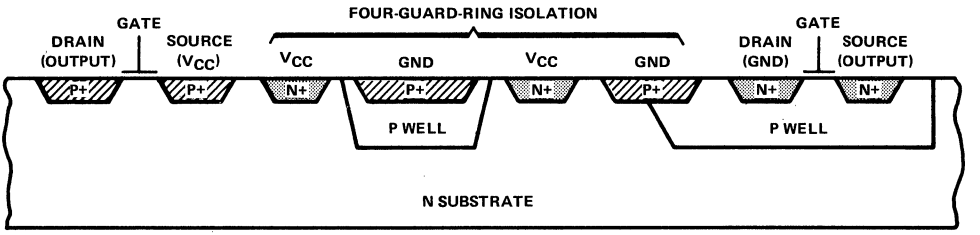


Figure 17. Unique Latch-Up Suppression Utilizes Guard Rings to Virtually Eliminate Latch-Up

Fan-Out and Capacitance Loading Effects

High-Speed CMOS is capable of driving up to 10 LSTTL loads from a single standard output, or 15 loads from a high-current output. From the dc values in Table I on page 2-4, the fan-out of high-speed CMOS devices is unlimited for all practical purposes. However, from an ac point of view, there is a definite limit to the fan-out. The limiting constraint is the input rise time.

With a worst-case model, about 15 pF of capacitance is associated with the input of a high-speed CMOS device (10 pF from the device itself plus 5 pF of stray capacitance; typically the input capacitance is 3 pF for all devices except the transceivers, which are 6 pF). The input resistance, r_I, can be approximated with the following equation using the information in Table I on page 2-4.

$$r_I = V_I/I_I$$

where

$V_I = V_{CC} = 6$ V
$I_I = 0.1$ nA

The output resistance can also be calculated from the values in Table I, page 2-4 and the following equation:

$$r_O = (V_{CC} - V_{OH})/I_{OH}$$

where

$V_{CC} = 4.5$ V
$V_{OH} = 4.3$ V (typical)
$I_{OH} = 4$ mA

The calculated input resistance is about 60 MΩ and the maximum output resistance is approximately 50 Ω. Figure 18 shows the schematic of the output and the input models using the values previously determined.

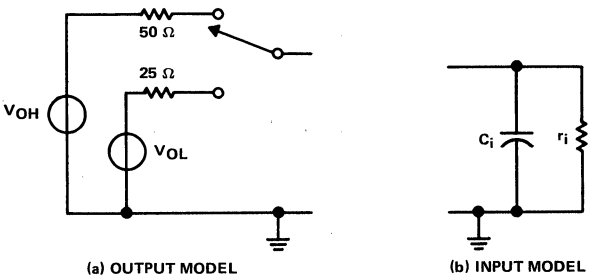


Figure 18. Worst-Case Output and Input Circuits of High-Speed CMOS

For a fan-out of n high-speed CMOS devices, the input capacitance will be (n × 15) pF (capacitances are in parallel). When the driving device switches its output from the low level to the high level, the input capacitance of all devices in the fan-out must be charged up and reach V_{IH}min within 500 ns (the recommended rise time). Therefore,

$$V_{IH}\text{min} = V_{OH}\text{typ}\ (1 - e^{-t/RC})$$

where

R = 50 Ω
C = (15 × n) pF
t = 500 ns
n = number of devices in the fan-out

Taking the natural log of both sides:

$$-t/RC = \ln(1 - V_{IH}\text{min}/V_{OH}\text{typ})$$

Substituting in the appropriate values and solving for n indicates that the maximum fan-out of high-speed CMOS devices is approximately 505. Alternately, solving for t in terms of n shows that each high-speed CMOS device added to the fan-out will increase the propagation delay from input of the driving device to the input of the driven devices by about 0.989 ns. This corresponds to approximately 0.066 ns/pF of added delay. Table 2 contains typical values of fan-out and capacitive loading effects at different values of V_{CC}.

Table 2. Typical Fan-Out of High-Speed CMOS Devices and Propagation Delay per pF at Various Values of V_{CC}

V_{CC}	V_{OH}min	V_{IH}min	n	t_{pd}/pF
2 V	1.9 V	1.4 V	936	0.0667 ns
4.5 V	4.4 V	3.15 V	993	0.0629 ns
6 V	5.9 V	4.2 V	1004	0.0623 ns

NOTE:

$$n = \frac{-t/RC}{\ln\left[1 - \frac{V_{IH}\text{min}}{V_{OH}\text{min}}\right]}$$

where

R = 50 Ω
C = 8 pF
n = number of devices in the fan-out

$$t_{pd}/pF = \frac{500\ \text{ns}}{n \times 8\ \text{pF}}$$

Power Dissipation

The power dissipation of high-speed CMOS devices can be separated into three components: (1) quiescent power dissipation, P_Q; (2) transient power dissipation, P_T; and (3) capacitive power dissipation, P_C. The total power dissipation is the sum of the three components, $P_Q + P_T + P_C$.

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (on the order of a few nA), which makes the quiescent power almost insignificant. However, for circuits that are in static conditions for long periods of time, the quiescent power becomes a factor to be considered.

The transient power is due to the current that flows only during the time the transistors are switching from one logic level to the other. During this time both transistors are partially on (one turning off, the other turning on), which produces a low-impedance path between V_{CC} and ground and results in a current spike. The rise (and fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal goes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise time of the input signal. This component can be calculated using the following equation:

$$P_T = C_{pd} \times V_{CC}^2 \times f_i$$

where

C_{pd} = power dissipation capacitance (specified on each data sheet)
V_{CC} = supply voltage
f_i = input signal frequency

Additional capacitive power dissipation is caused by the charging and discharging of the external load capacitance and is dependent on the switching frequency. To calculate this power, the following equation may be used:

$$P_C = C_L \times V_{CC}^2 \times f_o$$

where

C_L = external (load) capacitance
V_{CC} = supply voltage
f_o = output signal frequency

'HCT POWER DISSIPATION

'HCT devices are primarily used to interface TTL output signals to high-speed CMOS inputs. To make the inputs of the 'HCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption compared to the equivalent 'HC device, however 'HCT still provides a considerable savings in power over TTL. The increase in power consumption is due to the fact that the TTL input levels cause both transistors in the transistor pair to be partially turned on. Included in the dc tables for 'HCT devices (Tables V through VIII in Section 2) is a parameter ΔI_{CC}, which enables the designer to compute how much additional current the 'HCT device draws per input when at a TTL voltage level.

Power Supply Decoupling

When an SN54HC/74HC gate switches, there is a brief period (on the order of a nanosecond) during which both transistors in the gate output buffer (Figure 19) are partially on. In this interval, the device draws a substantial supply current, producing a current spike on the V_{CC} and ground leads to the gate. This spike may exhibit di/dt as high as 5000 A/s. These spikes will react with the distributed inductance of the supply wiring to produce significant voltage transients on V_{CC} and ground unless adequate supply decoupling is provided. These transients, if allowed, will couple directly into the gate outputs, which in normal usage switch from rail-to-rail.

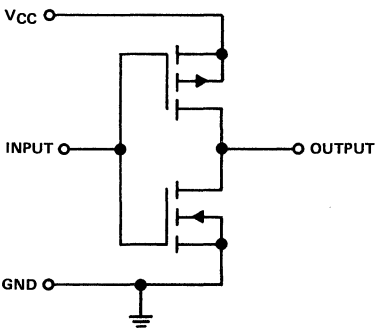


Figure 19. Gate Output Buffer

DECOUPLING PROCEDURE

Figure 20 illustrates a circuit for testing the effectiveness of decoupling. In this test circuit, the V_{CC} and ground connections consist of two parallel runs of one-eighth inch copper on a G-10 epoxy-glass circuit board. As a 0.01-μF decoupling capacitor between V_{CC} and ground is physically moved away from a driven gate in 1.5-inch increments, V_{CC} transients increase as shown in Figure 21.

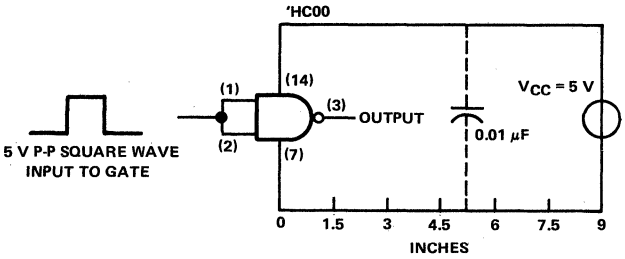


Figure 20. Test Circuit for Decoupling Effects

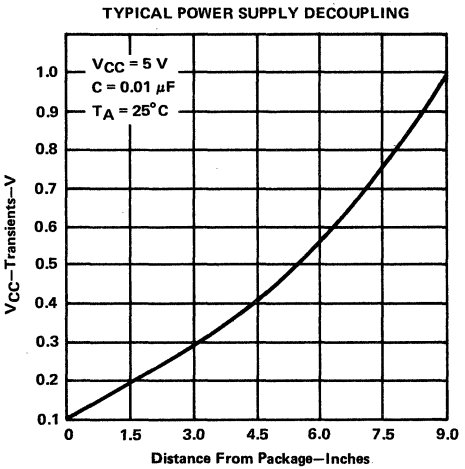


Figure 21. V_{CC} Transients vs Decoupling Capacitor Distance from DIP

The results indicate the importance of adequate decoupling, and illustrate the correct procedure for obtaining it. This procedure consists of locating decoupling capacitors as close as possible to the integrated circuit package, in order to maximize noise margins.

Connecting Unused Inputs

Unused inputs should be tied to V_{CC} or ground to prevent the input from floating. If left to float, the power consumption of the device will increase.

Matching

Another factor to consider when designing with high-speed CMOS is the V_{OH}min-to-V_I matching. This is important when the V_{OH}min of the driving device exceeds the V_{CC} + 0.5 V of the driven device. If this occurs, the ESD protection diode on the inputs will be forward biased. At this point, the driving device will attempt to "power-up" the driven device's power supply. No damage will occur to the driven device, provided the current flowing through the diode does not exceed 20 mA.

Powering Up/Down Sequence for High-Speed CMOS

To avoid any possible damage and reliability problems to the high-speed CMOS devices when applying power, the following steps should be followed:

1. Connect ground
2. Connect V_{CC}
3. Connect the input signal

When powering down a high-speed CMOS device, follow the above steps in reverse order.

High-Speed CMOS Interfacing

INTRODUCTION

The High-Speed CMOS logic family from Texas Instruments contains a broad spectrum of SSI/MSI functions. Within this family are TTL functions, HCT devices, HC4000 series, and an HCU device.[1] Entire CMOS systems may be implemented using this logic family. There is also a broad range of CMOS-system to non-CMOS-system interfaces that need to be considered. The design engineer will inevitably encounter these interfaces. To develop the necessary interfaces, a thorough understanding of data sheet parameters of both systems and an organized approach is recommended. This report uses basic examples to present one possible approach to the SN54/74HC interface solution.

There are two types of interfacing that must be considered: (1) interfacing CMOS system signals to non-CMOS systems and (2) interfacing non-CMOS system signals to CMOS systems. The first type requires an understanding of the CMOS output parameters and the non-CMOS input parameters and vice versa for the second type. In both cases, a model of the inputs and outputs of both systems may be useful.

GENERAL INTERFACING SOLUTION

An interfacing problem arises when the output logic levels and/or the current requirements of the driving system (or device) are different from the input logic levels and/or the current requirements of the driven system (or device). When determining the compatibility of the systems (or devices), the most important system/device parameters are V_{IH},V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, and V_{OL}.

Figure 22 is the voltage transfer characteristic of a typical unloaded inverter showing the various input and output voltage parameters. Loading the output of the inverter will tend to lower V_{OH} and raise V_{OL}. The tables of electrical characteristics specify minimum V_{OH} and maximum V_{OL} for various loads.

Noise Margin

There are two noise margins to be considered: the low-voltage noise margin and the high-voltage noise margin. The voltage difference between V_{IL}max of the driven system/device and V_{OL}max of the driving system/device is the low-voltage noise margin. The voltage difference between V_{OH}min of the driving system/device and V_{IH}min of the driven system/device is the high-voltage noise margin (Figure 23).

[1] HCT devices are explained later. The HC4000 series devices are pin-for-pin functionally compatible, but not electrically compatible, with the older metal-gate CMOS devices. The HCU device is unbuffered.

It is desirable to have the noise margin as large as possible and the uncertain region (the difference between V_{IH}min and V_{IL}max) as small as possible. When an input voltage falls into the uncertain region, we do not know how the output in conjuction with other inputs driven by that output will respond. The problem with small noise margins is that any noise on the output of the driving system or device will cause the signal to fall into the uncertain region and possibly cause a bit error in the system. There are various sources of noise in digital systems. Three possible internal sources are inductive and resistive drops, capacitive coupling from another logic node, and mutual inductance with another logic node. Radio signals are possible external sources of noise.

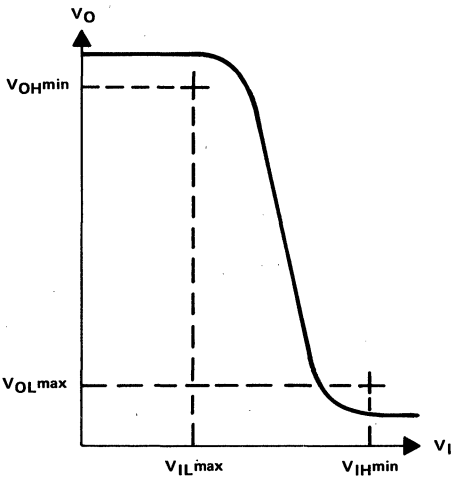


Figure 22. Voltage Transfer Characteristic of a Typical Inverter

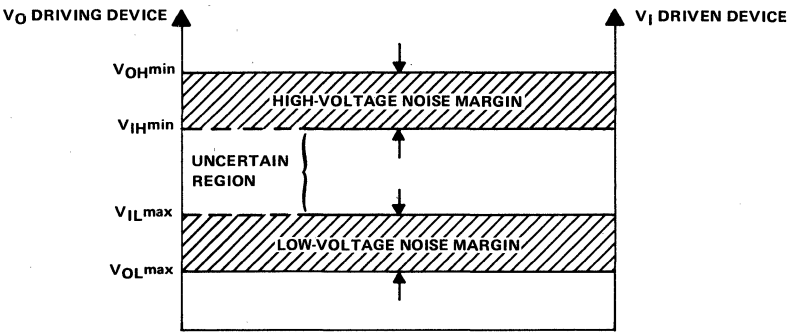


Figure 23. Noise Margins

As an aid for interfacing between the various TTL families, the eight parameters previously defined are shown in Table 3. The values are for V_{CC} = 5 V and T_A = 25°C (worst-case device parameters — the device will perform at least this well). All currents are designated positive when flowing into the device.

Table 3. Worst-Case Values of Primary Interfacing Parameters

PARAMETER	74HCMOS	74TTL	74LSTTL	74ASTTL	74ALSTTL
V_{IH}min	3.5 V	2 V	2 V	2 V	2 V
V_{IL}max	1 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{OH}min	4.9 V	2.4 V	2.7 V	2.7 V	2.7 V
V_{OL}max	0.1 V	0.4 V	0.4 V	0.4 V	0.4 V
I_{IH}max	1 μA	40 μA	20 μA	200 μA	20 μA
I_{IL}max	−1 μA	−1.6 mA	−400 μA	−2 mA	−100 μA
I_{OH}max	−4 mA	−400 μA	−400 μA	−2 mA	−400 μA
I_{OL}max	4 mA	16 mA	8 mA	20 mA	4 mA

Driving Gate Output Model

Figure 24 shows the model of a driving gate derived from the data sheet specifications. $V_{OH(nl)}$ (nl = no load) is the high-level output voltage expected when the output gate is unloaded. $V_{OL(nl)}$ is the low-level output voltage expected when the output gate is unloaded. The values for these two voltages are usually not given on the data sheets. As a rule of thumb for MOS devices, the output switches between the power rails $V_{OH(nl)} = V_{CC}$ and $V_{OL(nl)} = GND$; for bipolar devices (e.g., the TTL Family) $V_{OL(nl)}$ is about V_{CC}(sat) or about 0.3 V. Within the TTL family $V_{OH(nl)}$ varies. Standard TTL has a $V_{OH(nl)}$ within two base-emitter drops of V_{CC}($V_{OH(nl)} = V_{CC} - 1.2$ V); LSTTL has a $V_{OH(nl)}$ within one base-emitter drop of V_{CC}($V_{OH(nl)} = V_{CC} - 0.6$ V). The data sheets specify V_{OH}max and V_{OL}max at a nonzero I_{OH} and I_{OL}, respectively. Therefore to calculate the approximate series resistances, the following two equations may be used:

$$R_{OH} = \frac{|V_{OH(nl)} - V_{OH}\text{min}|}{I_{OH}}$$

$$R_{OL} = \frac{|V_{OL(nl)} - V_{OL}\text{max}|}{I_{OL}}$$

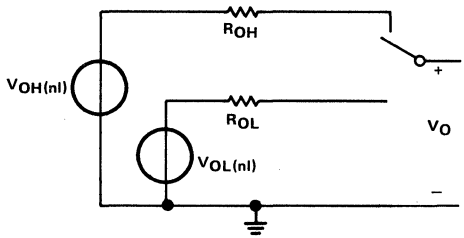


Figure 24. Output Model of a Driving Gate

Input Gate Circuit

A simplified schematic of a high-speed CMOS input gate is shown in Figure 25. The diode D1 and the transistors Q1 and Q2 provide static discharge and input transient clamping for the device. Any inputs higher than V_{CC} + 0.5 V or lower than −0.5 V will clamp the input. The capacitors C1 and C2 represent the parasitic capacitances present at the gate input. The data sheet specifices that the input capacitance (C1 + C2) will not exceed 10 pF (typical is about 5 pF). The input capacitance is split between V_{CC} and ground of the device and provides a feedback path between V_{CC} and the input. If the input is driven by a high-impedance source, then any transient noise on V_{CC} may be coupled back into the input.

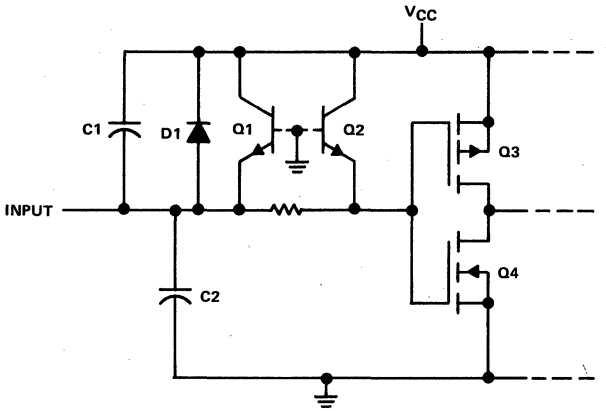


Figure 25. SN54/74HC Input Gate

CMOS-to-STANDARD-TTL INTERFACE

CMOS devices can drive TTL loads with no additional interfacing required. The output voltages of CMOS devices are compatible with the input voltage requirements of TTL devices. The input current requirements of the TTL devices does place a strict limitation on the number of TTL devices that CMOS devices can drive from a single output (the fan-out).

Figure 26 is a schematic of a CMOS output gate driving a TTL input gate. When the CMOS gate drives the emitter of Q3 low, a current will flow into the CMOS gate from R1 and the emitter of the TTL gate. The maximum guaranteed current that the CMOS device can sink is 4 mA. However, the device can sink up to 25 mA, but the output voltage is not guaranteed above 4 mA. Therefore, the maximum TTL fan-out that a device can drive without exceeding the specified limit is two (I_{IL} for TTL is -1.6 mA).

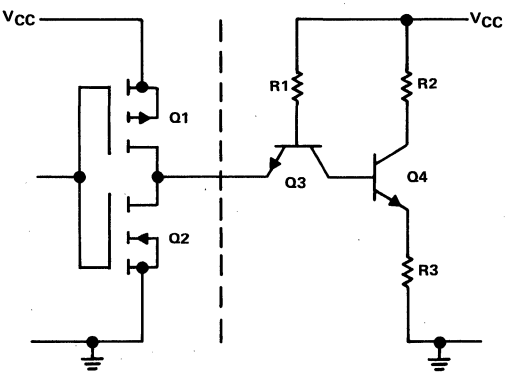


Figure 26. SN54/74HC to TTL Interface

STANDARD TTL-to-CMOS INTERFACE

The interface for TTL driving CMOS is not as simple as the CMOS-to-Standard-TTL interface. Taking the voltage le from Table 3, it can be seen they are not compatible as far as V_{OH}min of the TTL device and V_{IH}min of the CMOS dev Figure 27 shows the schematic of TTL to CMOS interface. The pull-up resistor R_P eliminates the voltage incompatibi

The lower limit of the pull-up resistor is determined by the current-sinking capability of the driving device (TTL for this interface). When the TTL device output goes low, Q3 (Figure 27) will be required to sink a current of (V_{CC}-V_{OL}max)/R_P in addition to the sum of the output currents of the driven devices I_{IL} worse case. All of this is shown in the following equation:

$$R_P\text{min} = \frac{V_{CC} - V_{OL}\text{max (TTL)}}{I_{OL}\text{(TTL)} + n\ I_{IL}\text{(load)}}$$

where n is the number of loads being driven, and V_{CC} is the voltage applied to the pull-up resistor.

Example: An SN74LS00 is driving three SN74HC00 devices. V_{CC}min = 4.75 V, V_{OL}max = 0.4 V, I_{OL} = 8 mA, I_{IL} = 1 μA, n = 3, therefore $R_P$min = 543 Ω.

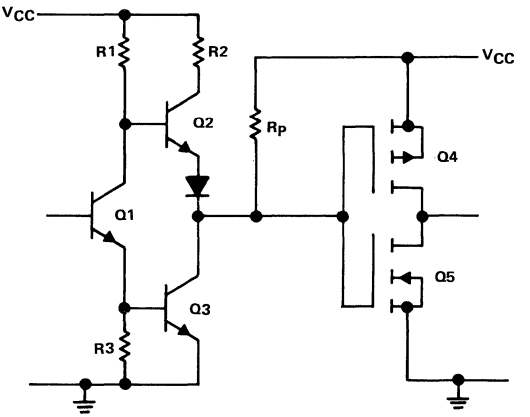


Figure 27. TTL to SN54/74HC Interface with a Pull-Up Resistor

The upper limit of the pull-up resistor is determined by two factors: (1) the total input capacitance of the loads and (2) the total high-level input currents of the loads. When the TTL output goes high, Q_2 is turned off due to the pull-up resistor. Therefore, all the current that flows into the devices that are being driven flows through the pull-up resistor R_P. The input voltage of the CMOS devices will therefore rise exponentially with a time constant of R_PCi (C_i = 10 pF max). The time constant cannot exceed the 500-ns rise time requirement of the CMOS device. Along with this limitation, the total input currents must not cause the voltage drop across the pull-up resistor to exceed V_{IH}min for the CMOS devices. Bringing all this into play, the following equation may be used to determine $R_P$max.

$$R_P\text{max} = \frac{V_{CC} - V_{IH}\text{min (load)}}{\left|n\ I_{IH}\text{(load)} - I_{OH}\text{(driver)}\right|}$$

where n is the number of loads being driven, and V_{CC} is the voltage applied to the pull-up resistor.

Example: An SN74LS00 is driving three SN74HC00 devices. V_{CC} = 5.25 V, V_{IH}min = 3.675 V, I_{IH} = 1 μA, I_{OH} = 0, n = 3, therefore $R_P$max = 525 kΩ.

However, if the rise time is calculated using this value of $R_P max$, the recommended 500 ns will be exceeded.

From the relationship:

$$V_{IH}min = V_{CC}max\ (1 - e^{-t/R_PC_i})$$

with

$$V_{IH}min = 3.675\ V \text{ and } V_{CC}max = 5.25\ V$$

then

$$R_P = \frac{t}{1.2\ C_i} = 13.8\ k\Omega \text{ for } t = 500\ ns \text{ and } C_i = 30\ pF$$

Generally, this rise-time constraint is the limiting factor on the upper limit of the pull-up resistor.

CMOS-to-LSTTL INTERFACE

The interface of CMOS to LSTTL is very similar to the interface of CMOS to TTL. Figure 28 shows a schematic of the interface. As can be seen, there is no pull-up resistor required. When the LSTTL input is pulled low, the current will flow through R1 and D2 into the CMOS output. In the worst-case condition, this current is about 0.4 mA. Because the CMOS output parameter I_{OL} specifies a 4-mA current sink for the device, the maximum LSTTL fan-out is ten.

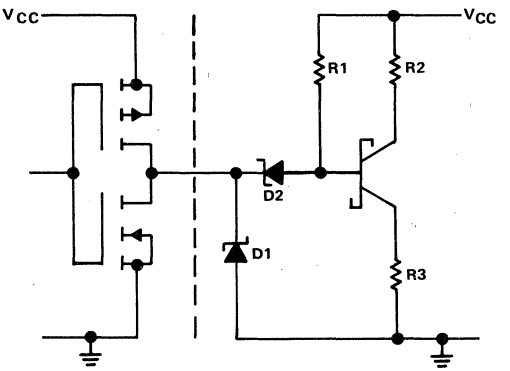


Figure 28. SN54/74HC to LSTTL Interface

LSTTL-to-CMOS INTERFACE

For an LSTTL device to drive a CMOS device, a pull-up resistor must be used because the $V_{OH}min$ of the LSTTL is less than the specified $V_{IH}min$ of the CMOS device. Figure 29 shows the schematic of the LSTTL/CMOS interface. The upper and lower limits of the pull-up resistor are determined in the same method as the TTL/CMOS interface. Remember the upper limit of the pull-up resistor is limited by the input currents and the input capacitance.

CMOS-to-ALSTTL INTERFACE

The output logic level of CMOS devices are completely compatible with the input logic levels of ALSTTL devices. The interface structure with ALSTTL is shown in Figure 30. As with the other CMOS-to-TTL interfaces, there is no pull-up resistor required. The fan-out of ALSTTL devices is determined by the amount of current that flows through Q3 into the

CMOS device, and the amount of current the CMOS device can sink. When the input of the ALSTTL device is low, there is 0.1 mA flowing though Q2. The maximum current that the CMOS device can sink (according to the parameters) is 4 mA. This corresponds to a ALSTTL fan-out of 40.

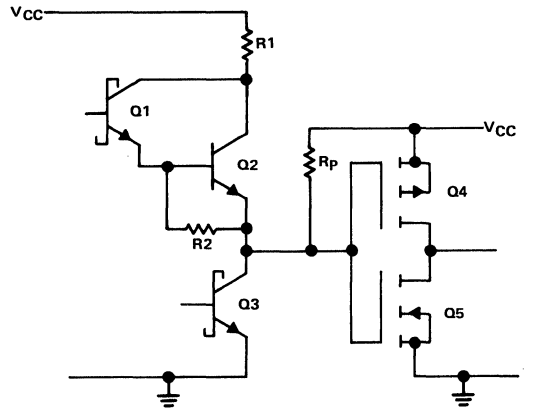


Figure 29. LSTTL to SN54/74HC Interface with a Pull-Up Resistor

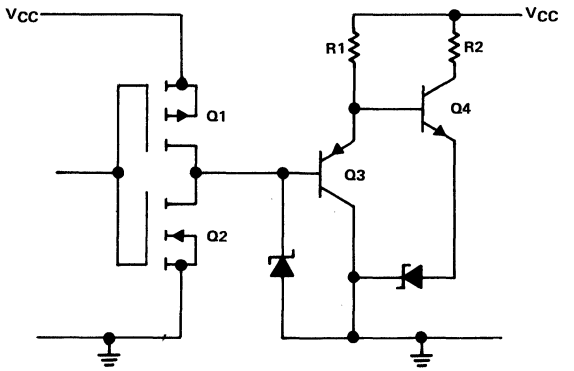


Figure 30. SN54/74HC to ALSTTL Interface

ALSTTL-to-CMOS INTERFACE

The high-level output voltage of ALSTTL devices is incompatible with the required high-level input voltage of CMOS devices. Because of this incompatibility, a pull-up resistor is required to make the two voltage levels compatible. The method of determining the upper and lower limits of the pull-up resistor is the same as the other two TTL-to-CMOS interfaces. Figure 31 shows a schematic of the interface.

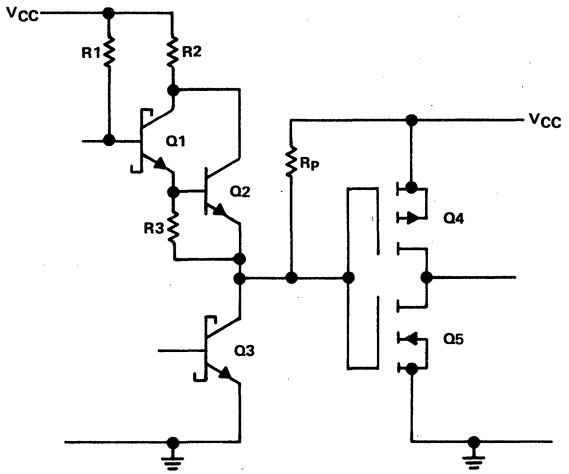


Figure 31. Interface with a Pull-Up Resistor

CMOS-to-ASTTL INTERFACE

As in the case of the other CMOS-to-TTL interfaces, no pull-up resistor is required (Figure 32) because the input voltage levels of ASTTL are compatible with the output voltage levels of CMOS. The fan-out of ASTTL devices is limited by the low-level input current (I_{IL}) of ASTTL and the current sinking capability of CMOS (I_{OL}). I_{IL} for the ASTTL is 2 mA, and the current sink limit of CMOS is 4 mA. Therefore, the fan-out is two ASTTL devices.

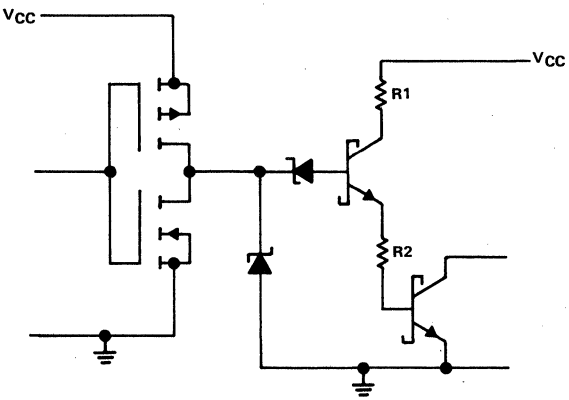


Figure 32. SN54/74HC to ASTTL Interface

ASTTL-to-CMOS INTERFACE

Not all the ouput logic levels of ASTTL are compatible with the input logic levels of CMOS. Table 3 shows there is incompatibility between the V_{OH} of ASTTL and V_{IH} of CMOS. As with other TTL-to-CMOS interfaces, a pull-up resistor is required (Figure 33). The appropriate value of the pull-up resistor is determined by the same procedure previously explained.

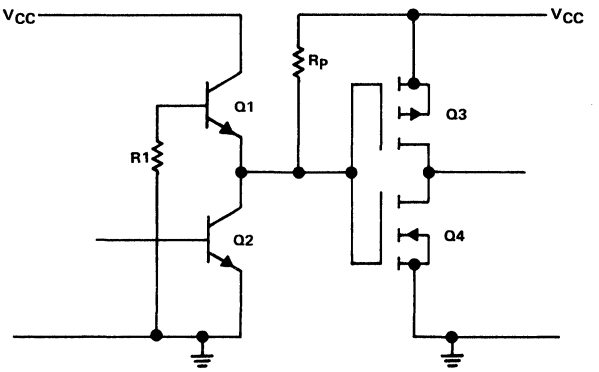


Figure 33. ASTTL to SN54/74HC Interface with a Pull-Up Resistor

CMOS-to-NMOS INTERFACE

NMOS is used extensively in large-scale-integration products such as microprocessors, microcomputers, and memories. The logic levels of NMOS are usually TTL-compatible. CMOS devices can drive NMOS devices with no pull-up resistors. The input impedance of NMOS is very high, which is similar to the input impedance of CMOS.

NMOS-to-CMOS INTERFACE

A pull-up resistor may be necessary when an NMOS device drives a CMOS device. The method of determining the value range of the pull-up resistor is the same as the method described previously for TTL. A quick look at NMOS output parameters and CMOS input parameters will determine if a pull-up resistor will be required.

USING HCT DEVICES TO INTERFACE TO CMOS FROM TTL

To interface from a TTL system (standard TTL, LSTTL, ASTTL, ALSTTL), there are two methods: (1) the use of pull-up resistors (as previously described) and (2) the use of HCT devices. Using HCT devices is by far the easier method. The HCT device inputs are TTL compatible, while the outputs are both TTL and CMOS compatible. Therefore, all the interface requires is to connect the TTL system output into the HCT device, and the output of the HCT device can then be used for the input of the CMOS system.

Oscillators

RC OSCILLATORS

Simple oscillator circuits using a minimum number of components can be designed with high-speed CMOS devices, e.g., two 'HC04, 'HCU04, 'HC00, or 'HC02 gates. These oscillators generate a period of approximately 1.8 RC seconds (Figure 34).

CRYSTAL-CONTROLLED OSCILLATORS

A crystal or ceramic resonator may be used to set the oscillator period (Figure 35). The value of the resistor, typically 100 kΩ, may require special selection to ensure oscillation at the desired fundamental resonator frequency. The capacitor, typically 100 pF, is required to dampen parasitic oscillations in the 30-MHz to 50-MHz range.

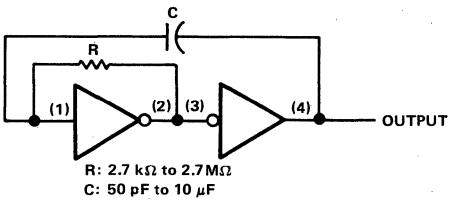


Figure 34. Simple RC Oscillator Using Two 'HC04 Gates

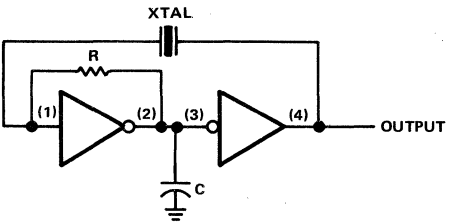


Figure 35. Oscillator Circuit Using a Crystal to Set the Period

VOLTAGE-CONTROLLED OSCILLATORS

Voltage-controlled oscillators (VCOs) can also be designed using a minimal number of components. Figure 36 shows a VCO using NAND and inverter gates. This VCO design exploits the phenomena of the slight variations in the propagation delay of an 'HC gate with changes in the supply voltage. The 'HC00 is connected as a three-stage ring oscillator with a buffer. As the control (supply) voltage V_C is varied, the ring oscillator's frequency changes according to the following:

$$f_{out} \approx 5.8 \times V_C$$

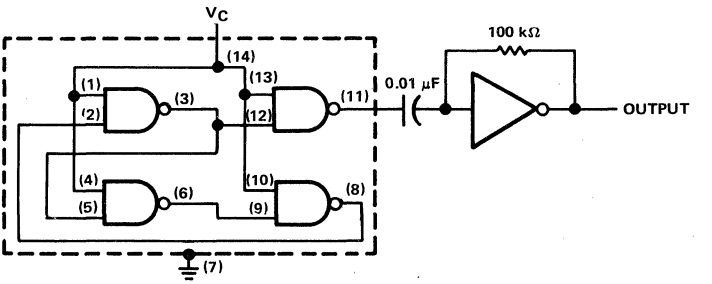


Figure 36. Voltage-Controlled Oscillator (VCO)

The inverter, which is powered by a separate voltage source, serves to restore the oscillator output voltage to 5 V peak-to-peak. This function is required, because the 'HC00 switches from rail-to-rail (as do all HC devices). The magnitude of the oscillator output voltage is thus dependent on V_C. The 100-kΩ resistor across the inverter provides bias such that operation will be within the linear operating region of the gate. The capacitor serves to ac-couple the oscillator to the inverter.

The VCO output is linear for control voltages in the range of 1.5 to 4.5 V (Figure 37).

To prevent oscillator "bleed-through" onto the V_{CC} line, adequate decoupling of the 'HC device power supply is required.

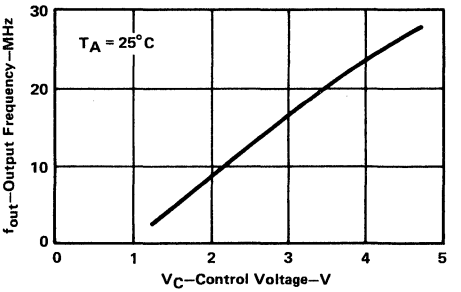


Figure 37. VCO Output Frequency vs Input Voltage

Drivers for LEDs and Relays

INTRODUCTION

SN54/74HC devices are capable of sinking or sourcing up to 25 mA (35 mA for high-current devices) per gate. As the device sinks or sources more current, V_{OH}min or V_{OL}max levels will begin to fall or rise respectively.

Because of these characteristics, SN54/74HC devices can be used to drive LEDs and relays.

DRIVING LEDs

Figure 38 shows an 'HC04 driving a TIL221 gallium phosphide light-emitting diode. The resistor performs the function of current limiter. The luminous intensity of the LED depends on the amount of forward current.

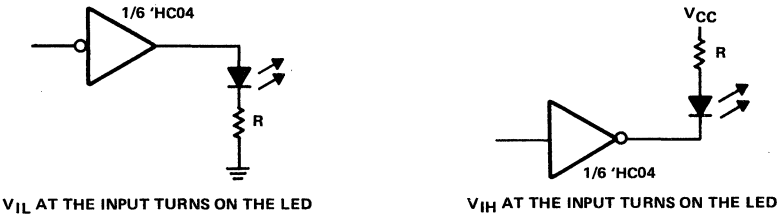


Figure 38. 'HC04 Driving a LED

Example: Using 10 mA forward current and 2.2 V forward voltage, the value of the current-limiting resistor can be calculated using the following equations:

$$\text{[for Figure 38(a)]}\quad R = \frac{V_{OH} - 2.2\ V}{10\ mA}$$

$$\text{[for Figure 38(b)]}\quad R = \frac{V_{CC} - 2.2\ V - V_{OL}}{10\ mA}$$

It should be noted that as used here, V_{OH} and V_{OL} are not the V_{OH}min and V_{OL}max specified in the data book. Figures 39 and 40 show typical values for V_{OH} and V_{OL} for an 'HC00.

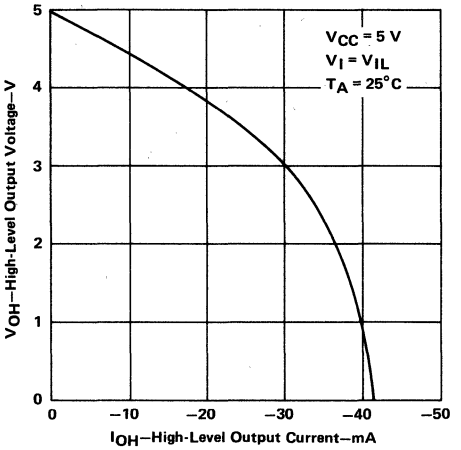


Figure 39. Typical Values for V_{OH}

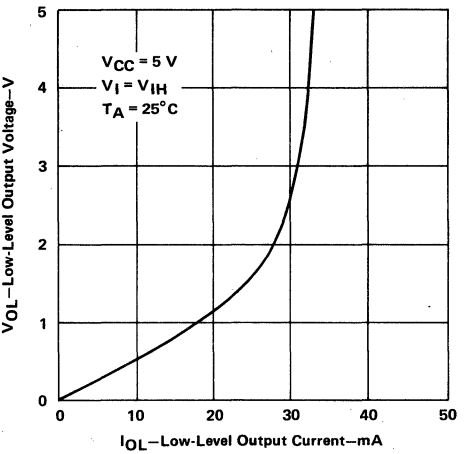


Figure 40. Typical Values for V_{OL}

DRIVING RELAYS

Multiple gates can be connected in parallel to increase the current sinking or sourcing capability of SN54/74HC devices. Figure 41 shows two 'HC04 gates connected in parallel for relay driver application.

Precautions should be taken to prevent one gate from "hogging" the current. Small resistors (typically 50 Ω) in series with the output gate will limit the possibility of "current hogging" by any one gate.

In all applications in which the SN54/74HC output is required to source or sink substantial current (6 mA to 25 mA), particular attention should be paid to providing adequate power supply decoupling for the driving device.

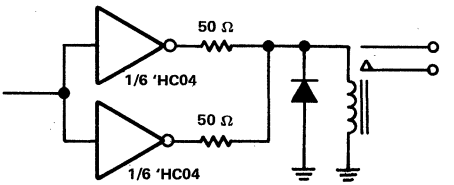


Figure 41. SN54/74HC04 Gates Connected in Parallel to Drive a Relay

SN54HC/SN74HC Interchangeability Guide

INTRODUCTION

The following has been prepared as a guide to interchanging devices from other logic families, both bipolar and CMOS, with those from the SN54HC/SN74HC family. This is not intended to be a comprehensive guide since interchangeability can depend on many factors, and only careful data sheet comparisons can provide definitive answers. The considerations listed below are based upon information accumulated in answering a large number of inquiries in this area.

First, a brief review is given on each logic technology, and second, discussion is given on the various aspects involved in attempting to interchange that technology with the SN54HC/SN74HC family.

TTL: Transistor-Transistor Logic

TTL is the generic name for several bipolar families that have evolved over the past 20 years. Low-Power Schottky (LSTTL) is the most widely used bipolar logic family today. Other families, e.g., Schottky (STTL), Advanced Schottky (ASTTL or AS), and Advanced Low-Power Schottky (ALSTTL or ALS) are also used, depending on the speed versus power performance required by a given system design.

4000 Series: Metal-Gate CMOS Logic

The device type numbers in this series have a variety of prefixes, although "CD" is probably the most widely recognized. The suffix "B" is frequently used, indicating an improvement over the original family, i.e., buffered outputs and typical output sink and source current capabilities of ± 1 mA. This logic family became popular because it offered very low power consumption, even though it is slower than TTL with a typical operating frequency of about 5 MHz, has a low level of ESD protection, and is latch-up prone.

40H00 Series: Metal-Gate CMOS Logic

This series was designed to overcome the speed limitations of the original 4000 family. Even though these devices are somewhat faster, they are still slow when compared to LSTTL.

74C00 Series: Metal-Gate CMOS Logic

The distinguishing feature of this family is that the pinouts correspond to those of TTL, making interchangeability easier. The devices, however, exhibit many of the same speed/power limitations as those of the 4000 series. The fan-out is typically higher than the 4000 series, however, with typical output sink and source capabilities of ± 1.75 mA.

74SC00 Series: Silicon-Gate CMOS Logic

This series was the forerunner to the SN54HC/SN74HC family, or more closely, to the SN54HCT/SN74HCT family. The 74SC family was designed to overcome many of the 4000 series deficiencies, particularly the slower speed and the lower drive capability.

Note: The "SC" designation should not be confused with that of Texas Instruments new Standard Cell family (SN54SC/SN74SC series).

INTERCHANGEABILITY CONSIDERATIONS

Listed below are the highlights of benefits derived from replacing other logic families with SN54HC/SN74HC; also listed are important considerations that may affect the feasibility or desirability of such replacement. All comparisons are by necessity general in nature.

LSTTL

Considerations:

1. SN54HC/SN74HC high-level input voltage is not TTL-compatible. In a mixed family system (LS output driving HC input) it will be necessary to use SN54HCT/SN74HCT, pull-up resistors, or level shifters.
2. SN54HC/SN74HC has less drive capability than some LSTTL functions.
3. LSTTL open-collector outputs have higher breakdowns than SN54HC/SN74HC open-drain equivalent functions.

HCMOS advantages:

1. Lower system power consumption
2. Improved noise immunity
3. Wider supply voltage range.

Other TTL Families

Considerations:

1. SN54HC/SN74HC high-level input voltage is not TTL-compatible. In a mixed family system (TTL output driving HC input) it will be necessary to use SN54HCT/SN74HCT, pull-up resistors, or level shifters.
2. SN54HC/SN74HC has less drive capability than some TTL functions.
3. TTL open-collector outputs have higher breakdowns than SN54HC/SN74HC open-drain equivalent functions.
4. Some of the TTL families offer greater operating speed, e.g., STTL, AS, and ALS.

HCMOS advantages:

1. Lower system power consumption
2. Improved noise immunity
3. Wider supply voltage range.

4000 Series and 74C00 Series

Considerations:

1. Although most applications use a 5-V supply, these older families operate in the 3-V to 15-V range.
2. SN54HC/SN74HC must be operated with a supply voltage in the 2-V to 6-V range.

HCMOS advantages:

1. Higher frequency of operation
2. Improved ESD protection and latch-up performance
3. Higher output drive capability.

40H00 Series

Considerations:

1. Although most applications use a 5-V supply, this family will operate in the 2-V to 8-V range.
2. SN54HC/SN74HC must be operated with a supply voltage in the 2-V to 6-V range.

HCMOS advantages:

1. Higher frequency of operation
2. Improved ESD protection and latch-up performance
3. Higher output drive capability
4. Multiple-sourced family.

As a quick reference guide, Table 4 shows highlights of interchanging other logic families with high-speed CMOS.

CONCLUSION

Within the constraints given above, the SN54HC/SN74HC family can be regarded as pin-for-pin equivalents to the other logic families. The rapidly-expanding SN54HC/SN74HC family is ideally suited for system upgrading, system shrinking, or especially, new system design.

Table 4. Highlights of Interchangeability

	TTL FAMILY (TTL, LSTTL, STTL, ALS, AS)	METAL-GATE CMOS
Power	HCMOS offers lower system power consumption than any of the TTL families.	Power consumption of HCMOS is less than metal-gate CMOS.
Speed	HCMOS operating speed is comparable to LSTTL. Some TTL families (STTL, AS, and ALS) offer greater operating speed.	HCMOS operating speed is much faster than metal-gate CMOS.
Input Voltage	The V_{IH}min of HCMOS is not compatible with the V_{OH}min of TTL. In a mixed family system, it is necessary to use 'HCT devices, pull-up resistors, or level shifters.	HCMOS input voltage levels are compatible with metal-gate CMOS outputs only when the power supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Output Voltage	The output voltages of HCMOS are TTL-compatible.	HCMOS output voltage levels are compatible with metal-gate CMOS inputs only when the power supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Drive Capability	The output current capability of HCMOS is not as large as the TTL family.	HCMOS has a higher current drive capability.
Fan-out (LS devices)	HCMOS has a smaller fan-out to LS devices than the TTL family.	HCMOS has a higher fan-out to LS devices.
Supply Voltage	HCMOS has a wide operating supply voltage range (2 V to 6 V).	Operating supply range of metal-gate is larger than HCMOS (from 3 V to 15 V).
ESD and Latch-Up	TTL family devices are not as vulnerable to ESD and latch-up damage.	HCMOS has an improved protection circuitry against ESD and latch-up.

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
2) Junction field-effect transistors (JFET)
3) Bipolar digital and linear circuits
4) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5) Hybrid microcircuits and assemblies containing any of the types of devices listed
6) Printed circuit boards and any other type of assembly containing static-sensitive devices.

Definitions

1. Antistatic material: ESD protective material having a surface resistivity between 10^9 and 10^{14} Ω/square.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^9 Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.

4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type packaging required to adequately protect them.

1) Device electrostatic sensitivity:

Category	ESD Sensitivity (V)	Minimum Protective Packaging
A	20-2000	Antistatic Magazine & Conductive Bag/Box
B	> 2000	Antistatic Magazine & Antistatic Bag

2) Devices are to be categorized by their sensitivity
3) Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls.

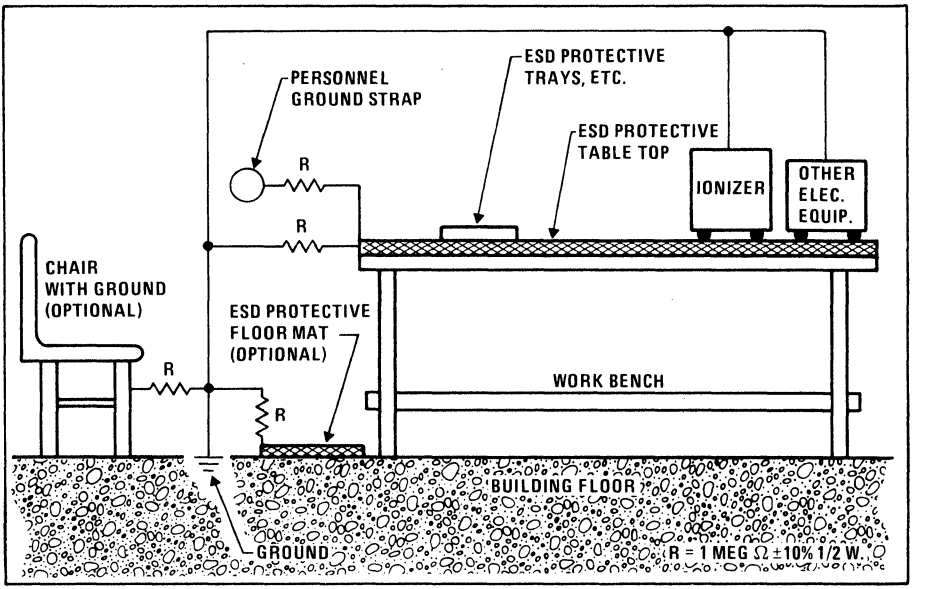
1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with an ESD protective material attached to ground through a 1 MΩ ±10% resistor, an attached grounding wrist strap with integral 1 MΩ ±10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the ESD protective material. Ground shall utilize the standard building earth ground, refer to Figure 42. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 5.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the conductive table top.

NOTE: Earth ground is not computer ground or RF ground or any other limited type ground.

Figure 42. Static-Free Work Station

Table 5. General Grounding Requirements

	TREATED WITH ANTISTATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Equipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubes	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, and voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 50%-65% (ref. Ashrae, 55—74), within ±5% to avoid static voltage monitor variations.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a conductive work surface connected to ground through a 1 MΩ ±10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free work station (Figure 42). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the grouding wrist strap. If possible, operators should avoid touching leads or contacts even though grounded.

CAUTION

Personnel shall never be attached to ground without the presence of the 1 MΩ ±10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas.**
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Spervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION**. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS,** item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum ot once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week).

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ±10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week).

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week).

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week).

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month).

Conductive floors must have a resistance of not less than 25 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 25 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 56.

Records

Written records must be kept of all these QC audits.

TRAINING

Training is applicable for all areas where individuals come in contact with ESDS (category A) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

Uses and Limitations of the SN54/74HCT CMOS Logic Family

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes in the devices or the device specifications identified in this publication without notice. TI advises its customers to obtain the latest version of device specifications to verify, before placing orders, that the information being relied upon by the customer is current.

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INTRODUCTION

To aid in interfacing TTL system signals to High-speed CMOS (HCMOS) systems, Texas Instruments has included in its HCMOS family a subfamily of 'HCT devices. While functionally identical to their 'HC counterparts, the input voltage thresholds of the 'HCT subfamily are designed to recognize TTL-level voltages. The output voltages of the 'HCT devices are identical to those of the 'HC devices, i.e., rail-to-rail.

TTL to HCMOS Interface

There is an incompatibility between TTL output voltages and the HCMOS input voltages, specifically the V_{OH} of TTL and V_{IH} of HCMOS. To overcome this incompatibility there are at least three methods to interface TTL signals to HCMOS. The first method is to use the HCMOS subfamily 'HCT. The second method involves using a pull-up resistor to pull-up the V_{OH} of the TTL gate to a voltage that is greater than the V_{IH} of the HCMOS device. The final method is to use a voltage level shifter.

Using the 'HCT devices is by far the easiest. The 'HCT devices were designed specifically for this type of application. Use of 'HCT devices enables the system designer to reduce the number of discrete components (no pull-up resistors), and receive the benefits of HCMOS.

Using pull-up resistors to interface the TTL signals to HCMOS requires the system designer to calculate the range of acceptable values for the pull-up resistor. The lower limit is determined by the current sinking capability of the driving gate.

$$R_p \text{ min} \geq \frac{V_{CC} - V_{OL} \text{ max}}{I_{OL} + nI_{IL}}$$

Where n is the number of gates in the fanout.

Determining the upper limit of the pull-up resistor is not as simple. The upper limit must satisfy two constraints. The first is limited by the input current of the driven gate. Since the driven gate is HCMOS the input current will be extremely small (on the order of a nanoamp).

$$R_p \text{ max} = \frac{V_{CC} - V_{IH} \text{ min}}{nI_{IH}}$$

Where n is the number of gates in the fanout

In this equation, I_{OH} of the driving gate has been omitted because all the current is being supplied through the pull-up resistor. For the second constraint, R_p max is derived through the following equation:

$$V_{IH} = V_{CC}(1 - e^{-t/R_pC})$$

Where

t is the maximum rise time requirement of 500 ns
C is the input capacitance of 3 pF typ., 10 pF max

Rearranging the equation:

$$e^{-t/R_pC} = 1 - (V_{IH}/V_{CC})$$

Solving for R_p:

$$R_p = \frac{-t}{C \ln(1 - V_{IH}/V_{CC})}$$

Therefore $R_p \text{ max} \leq \frac{V_{CC} - V_{IH}}{nI_{IL}}$

and $$R_p \text{ max} \leq \frac{-t}{C \ln(1 - V_{IH}/V_{CC})}$$

The upper limit to the pull-up resistor will be most influenced by the rise time requirement of the input signal. The larger the resistor, the longer the rise time of the input signal. This will adversely affect the propagation delay of the input signal. By reducing the value of the pull-up resistor, the rise time of the input signal will benefit, but the current through the pull-up resistor will be increased. This will have an adverse effect on the system power consumption.

The last method uses a voltage level shifter to make the TTL signals HCMOS compatible. This method has a major drawback, in that the level shifter performs no logic function. Therefore additional logic will have to be added to the system, increasing the board area.

From a designer's point of view, using 'HCT devices to interface TTL signal to HCMOS is by far the easiest and most efficient method. 'HCT devices provide the voltage-level shifting and the logic function in a single chip. In addition, there is no need to compromise between the input signal rise time and the pull-up resistor current.

'HCT Operating Voltages

The 'HCT devices have a limited V_{CC} operating range due to the fact that these devices must be able to recognize TTL-level voltages. Although the 'HCT devices will operate from 2 V to 6 V (same as 'HC devices), there are two major disadvantages in addition to the fact that there are no guaranteed specifications for operation outside the 4.5 V to 5.5 V V_{CC} range. First, the noise margins, especially the low-voltage noise margin, will become smaller and smaller as the V_{CC} is decreased. Second, the input voltage thresholds will no longer remain TTL-level compatible, which is the primary function of 'HCT.

'HCT Noise Immunity

Noise immunity is an important criterion in system designs. Noise immunity has two components: high-voltage noise margin and low-voltage noise margin. High-voltage noise margin is the voltage difference between the guaranteed V_{OH} of the driving gate and the guaranteed V_{IH} of the driven gate. Low-voltage noise margin is the voltage difference between the guaranteed V_{IL} of the driven gate and the guaranteed V_{OL} of the driving gate. These two components of noise immunity are illustrated in Figure 1.

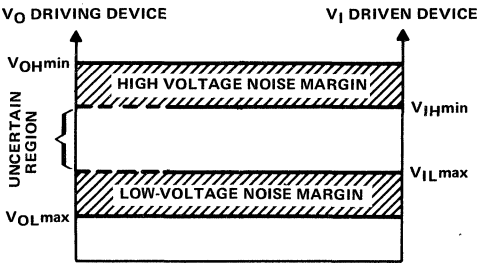


Figure 1. Noise Margins

It is desirable to have both noise margins as large as possible, and the area in between (the uncertain region) as small as possible. If the noise margins are not large enough for a particular application, noise from any internal or external source will cause the input/output signal to fall into the uncertain region and possibly cause a bit error to enter the system. Three possible sources of internal noise are inductive and resistive drops, capacitive coupling from another logic node, and mutual inductance with another logic node. External noise sources are mainly radio signals.

Figure 2 illustrates the guaranteed noise margins of 'HC, 'HCT and 'LS devices. As can be seen, 'HC devices have high- and low-voltage noise margins of 29% and 19% of V_{CC} respectively. A comparision of these noise margins to those of 'LS devices, shows that 'HC devices have more than twice the guaranteed noise margins than 'LS devices. The 'HCT devices seem to have a larger noise margins than the 'HC devices. However, this is slightly deceiving. The only configuration to achieve the large high-voltage noise margin is to have the input of the 'HCT device be driven from either another 'HCT device or an 'HC device. Although this may be advantageous for noise margins, the 'HCT device is in the wrong application. The 'HCT devices are designed to interface from TTL-level signals to HCMOS-level signals. Using the 'HCT device in its appropriate application, i.e., an 'HCT device driven by an LSTTL device, the noise margins will be identical to those of 'LS. The 'HC noise margins allow a greater magnitude of noise within the system without causing errors. This is very beneficial for applications in high noise environments. Figure 3 illustrates the noise margins of 'HC and 'HCT with respect to the devices' actual switching threshold voltages. The switching threshold voltage is the voltage to which the input transistors "compare" the voltage on the input pin. If the input voltage is greater than the threshold voltage, then the input transistors recognize this input as a logic 1. If the input voltage is less

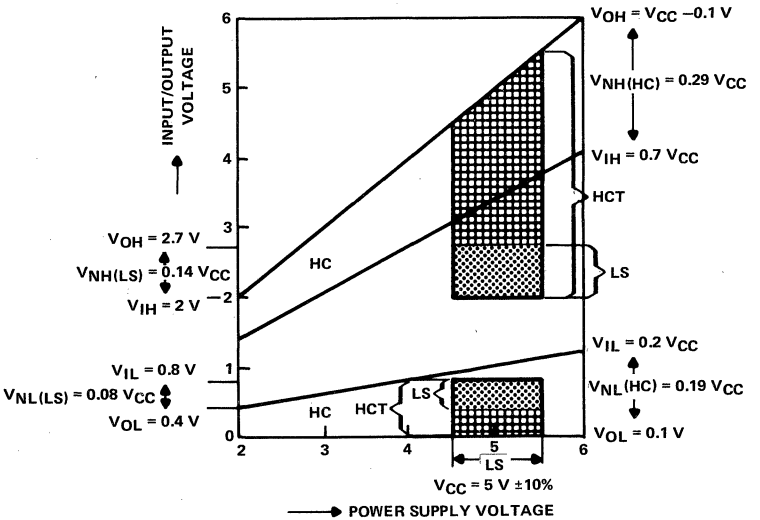


Figure 2. Guaranteed Noise Margins for 'HC and 'LS Devices

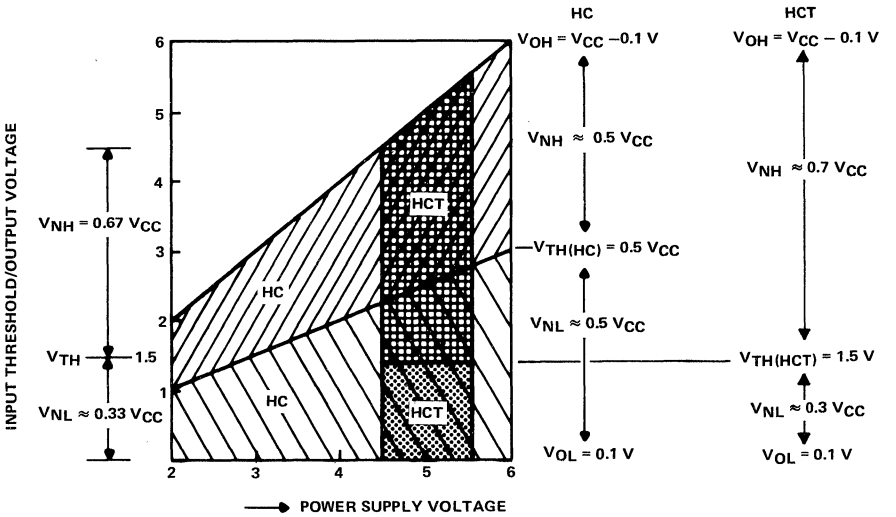


Figure 3. Typical Noise Margins Based on Threshold Voltages for 'HC and 'HCT Devices

than the threshold voltage, the input transistors recognize the input as a logic 0. This figure again presents slightly deceiving 'HCT noise margins for the same reasons as previously explained. Note that while both 'HC and 'HCT noise margins have been enlarged, the 'HC noise margins approach the ideal situation, 50% of V_{CC}. 'HCT, on the other hand, although exhibiting a larger high-voltage noise margin than 'HC, has a smaller low-voltage noise margin. In an 'HC system, both the high- and low-voltage noise margins are almost 50% of V_{CC}, and consequently, in an actual system environment, there is very little possibility for noise to introduce a bit error into the system.

For the best overall noise margins in a system, a combination of 'HCT and 'HC devices are used. The 'HCT devices are used to interface the TTL-level signals to the HCMOS. The 'HC devices are for the other parts of the system not involved with TTL-level input signals.

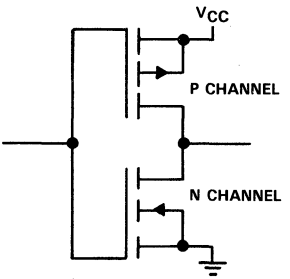
'HCT Power Consumption

To enable the 'HCT devices to recognize the TTL logic levels, the input transistor pair geometries were altered. In an 'HC device, the width of the gate of the input P-channel transistor is approximately twice the width of the gate of the N-channel transistor. For 'HCT devices, this configuration has been changed so that the N-channel transistor gate is approximately seven times wider than the P-channel transistor gate. This is illustrated in Figure 4. It should be noted that the gate width is the parameter that changes, not the gate length, which remains 3 μm in both the 'HC and 'HCT devices. The end result achieved with this new input structure configuration is the capability of turning on the N-channel transistor at a lower input voltage.

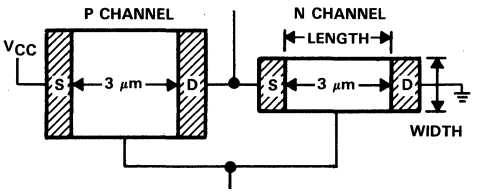
To achieve the above results, however, trade-offs are required. A major advantage of the HCMOS structure is its low-power consumption. Because of the larger N-channel transistor in the input structure of 'HCT device, more supply current is drawn by these devices. This is due to the N-channel transistor not completely turning off when a TTL-level voltage is applied to the input, an effect especially apparent when a TTL V_{OL} level is applied. To aid the system designer in using 'HCT devices, Texas Instruments includes in the dc tables of the 1984 High-Speed CMOS data book for 'HCT devices a parameter, ΔI_{CC}, which is the additional supply current drawn by the device when one input is at the specified TTL-level voltage rather than at 0 V or V_{CC}. Typical and maximum values are specified.

Figure 5 illustrates this increase in supply current by comparing I_{CC} for a 'HCT243 with TTL-voltage levels on one input versus TTL-voltage levels on four inputs. For this test, each output is loaded with a 50-pF capacitor and the input signal was a 0.5-V to 2.4-V peak-to-peak square wave with a 50% duty cycle. Figure 6 shows the supply current drawn by an 'HCT243 in the same circuit but with a 0-V to 5-V square wave with a 50% duty cycle. When the input to an 'HCT device is rail-to-rail, the 'HCT device draws no more current than is drawn by an 'HC device under the same conditions. Figure 7 shows a comparison of supply current drawn by an 'HCT device when subjected to TTL-voltage level inputs versus rail-to-rail inputs, with all four inputs being switched simultaneously.

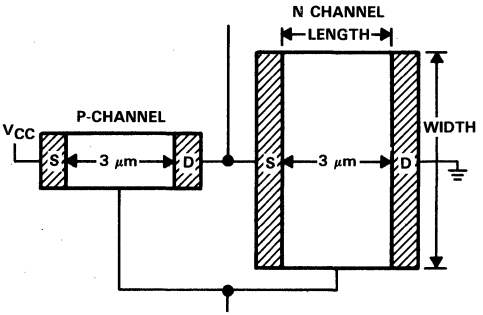
At frequencies above 5 MHz, the additional supply current is relatively insignificant (approximately 2 mA), but at lower operating frequencies the difference in the total supply current as a percentage becomes much more



a. SCHEMATIC OF INPUT TRANSISTOR PAIR



b. HC GATE: P-CHANNEL GATE WIDTH
2 TIMES N-CHANNEL GATE



c. HCT GATE: N-CHANNEL GATE WIDTH
7 TIMES P-CHANNEL GATE

Figure 4. Comparison of 'HC and 'HCT Input Gates

significant. Because of this, the use of 'HCT devices may not seem to be a particularly desirable solution for interfacing TTL-level voltages to HCMOS. The TTL-level inputs in Figure 7 were the guaranteed V_{OH} and V_{OL}. These guaranteed voltages are for a specified current being sinked or sourced by the TTL device. In fact, because 'HC and 'HCT devices are voltage level sensitive (i.e., they require no input current), the V_{OH} of the driving TTL gate, when driving HCMOS, will be much higher than the guaranteed voltage. Typically, the V_{OH} of an 'LS gate will be approximately one V_{BE} plus a $V_{CE(sat)}$ below V_{CC}, and the V_{OL} of an 'LS gate will be approximately one $V_{CE(sat)}$ above ground. Due to this,

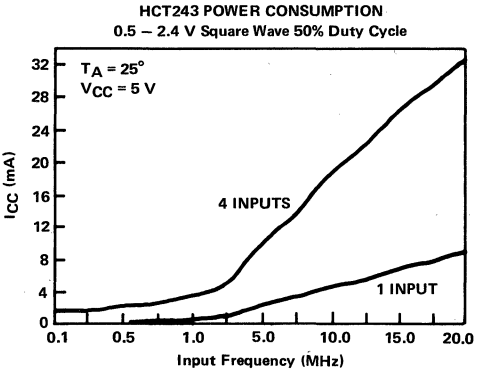


Figure 5. 'HCT243 Power Consumption with TTL Level Voltages on the Inputs

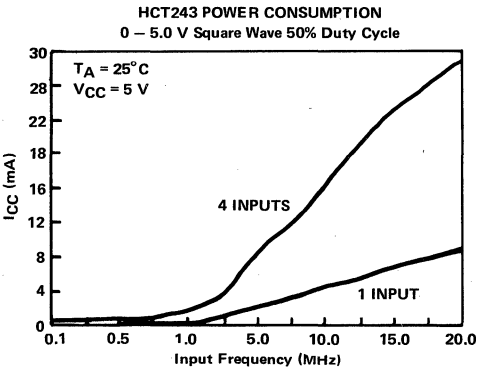


Figure 6. 'HCT243 Power Consumption with "Rail-to-Rail" Voltages on the Inputs

the additional I_{CC} drawn by the 'HCT gate will not be as significant.

By comparison, an alternative method for interfacing TTL signals to 'HC is the use of pull-up resistors (See Note 1), but here again trade-offs will have to be made. Using larger value pull-up resistors decreases the amount of additional supply current drawn, but degrades the rise time of the input signal to the 'HC gate, limiting the use of this method in high-speed systems. Decreasing the value of the pull-up resistor will shorten the rise time, but will cause the supply current to increase. The best overall solution is the use of 'HCT devices, which reduces also the number of discrete components required in the circuit.

Note 1: A complete description on how to interface TTL systems to HCMOS systems, and vice versa, is given in the Texas Instruments High-Speed Silicon-Gate CMOS data book.

Overall, the 'HCT devices provide a simple and efficient means for a system designer to interface TTL-level voltages to HCMOS systems, and gain many of the advantages of HCMOS.

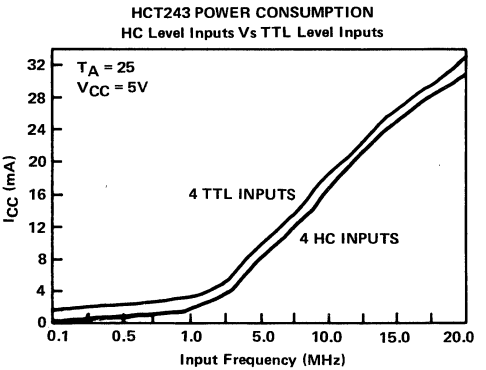


Figure 7. 'HCT243 Power Consumption Comparison of TTL Level Inputs to "Rail-to-Rail" Inputs

Propagation delays

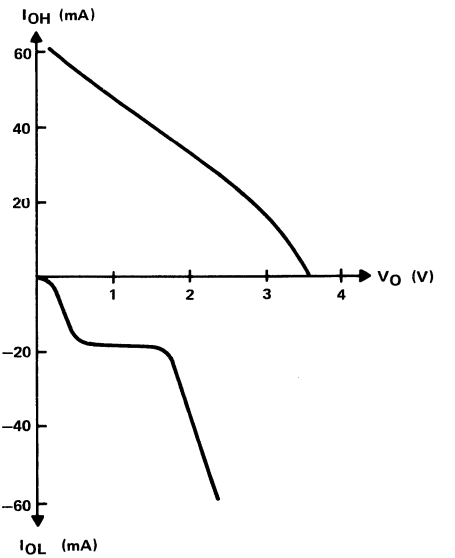
One other drawback to the use of 'HCT is the added propagation delay. Although there are no additional stages in an 'HCT device, compared to an 'HC device, the relatively small p-channel device has more difficulty charging and discharging the capacitance associated with the relatively large n-channel device. This results in an increase in propagation delay of approximately 1 to 2 ns for each 'HCT input.

'HCT Bergeron Analysis

Within a logic system, it is important to know whether or not a signal sent from one subsystem will cause incident wave or reflected wave switching on the input of the receiving subsystem. The incident wave or reflected wave switching issue is important because the transition times of the outputs are as fast or faster than the propagation times within the system's buses, causing the system buses to have characteristics similar to those of transmission lines. This in conjunction with impedance discontinuities, will cause signal reflections on the system's buses. These signal reflections may produce additional propagation delays, ringing, and overshoot.

Due to the fact that digital logic devices do not have linear input and output characteristics, the basic transmission line equations are not easily applied. What is needed is a simple method that will produce reasonably accurate results. Using Bergeron diagrams, the digital logic interconnections can be analyzed through a simple graphics technique.

To illustrate the graphical technique, we are using an example of an 'ALS00 driving an 'HCT245 through a 30-Ω transmission line. The first step is to plot the V_{OL}-I_{OL} and V_{OH}-I_{OH} characteristics of the driving gate and the V_{IL}-I_{IL} and V_{IH}-I_{IH} characteristic of the driven gate as illustrated in Figure 8. For switching from a logic 1 to a logic 0, the next step is to draw a line from the V_{OH} point (Point t_0 in Figure 9) on the V_O axis toward the output characteristic of the driving gate. The slope of the line is $-1/Z$, where Z is the impedance of the transmission line. At the intersection of the $-1/Z$ line and the output characteristic (Point t_1 in Figure 9), a new line is drawn toward the V_O axis. The slope of this line is $+1/Z$. the second V_O axis intersection (Point t_2 in Figure 9) or the intersection with the input characteristic, is the voltage seen by the driven gate. If this voltage is less than the switching threshold voltage, then incident wave switching will be achieved. If the second V_O axis intersection is not less than the switching threshold voltage then reflected wave switching will occur.



Note: The input characteristics of 'HC and 'HCT will have no effect on the results of the analysis, and therefore have been omitted.

Figure 8. Output Characteristics of Driving Gate ('ALS00)

For switching from logic 0 to logic 1 the same procedure previously described is followed except the V_{OH}-I_{OH} characteristic of the driving gate and the V_{IH}-I_{IH} characteristic of the driven gate are used (see Figure 10). The initial $-1/Z$ line is drawn from the V_{OL} point (Point t_0 in Figure 10) on the V_O axis toward the output characteristic (Point t_1 on Figure 10). The same criterion for incident wave switching is used; the second V_O axis intersection (Point t_2 on Figure 10) must be greater than the switching threshold voltage.

In the preceding example, the switching threshold voltage was used as the criterion for incident versus

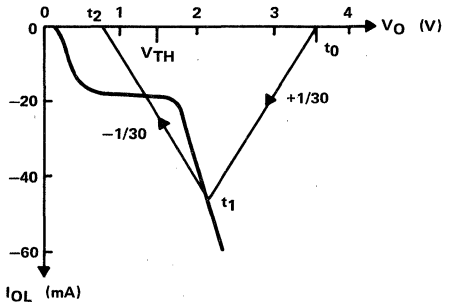


Figure 9. Bergeron Diagram for Switching from a Logic 1 to a Logic 0 Using an 'ALS00 Driving an 'HCT Device

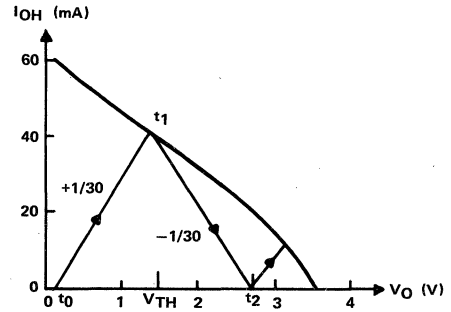


Figure 10. Bergeron Diagram for Switching from a Logic 0 to a Logic 1 Using an 'ALS00 Driving an 'HCT Device

reflected wave switching. The switching threshold voltage is where the device decides if the voltage on the input is low enough for a logic 0, or high enough for a logic 1. For 'HCT devices this voltage will be around 1.5 V, and for 'HC devices the threshold voltage will be around one half of V_{CC}. To be guaranteed that the receiving gate will switch, the load lines must intersect the V_O axis at a voltage less than the guaranteed V_{IL} or greater than the guaranteed V_{IH}.

Using the same analysis method, it can be seen (see Figure 11) that an 'HCT device driving another 'HCT device will have difficulty achieving incident wave switching on low-impedance transmission line (see the load lines for the 30-Ω line for a logic 1 to logic 0 transition). Because 'HC and 'HCT have the same output characteristics, and because 'HC has its thresholds at a higher voltage, the 'HC device can achieve incident wave switching on the low-impedance line.

In order to maintain the ability to drive low-impedance transmission lines throughout the system, 'HCT devices should be used only at the TTL interface, and 'HC devices should be used elsewhere.

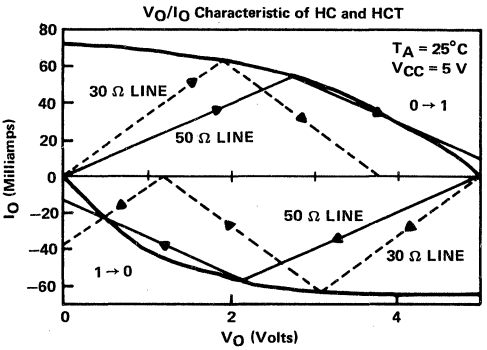


Figure 11. Bergeron Diagram of 'HC/'HCT Driving 'HC/'HCT Device

Summary

The major application of 'HCT is to provide the interface between TTL signals and HCMOS. Due to the fact that the input transistor pair geometries were altered to provide TTL compatibility, there were some inherent drawbacks. For this reason 'HCT should be used only at the TTL interface, and elsewhere 'HC should be used. This will result in optimum system performance.

As the HCMOS technology progresses, more and more systems will be designed in Silicon-Gate CMOS, especially with more LSI functions being offered (e.g., memories and microprocessors). Consequently the trend is expected towards CMOS levels on the interconnecting buses. Once this occurs, the need for 'HCT functions will diminish rapidly.

SN74HC Input/Output Voltage Specifications

TEXAS INSTRUMENTS

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INTRODUCTION

There is considerable confusion over the maximum input and output voltage specifications for the '74HC devices. Basically there are two questions: what exactly do the specifications mean; and why do different manufacturers have different specifications? This report answers these questions by considering the input and output structures of '74HC devices.

INPUT STRUCTURES

The maximum input and output voltages and currents that can be applied to a '74HC device are primarily determined by the ESD structures. Figure 1 illustrates the input structure used on Texas Instruments SN74HC family,

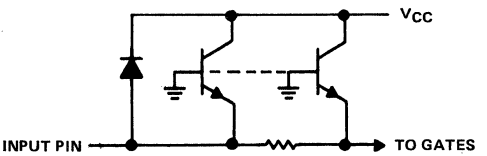


Figure 1. TI's ESD Input Protection Circuitry

and Figure 2 illustrates the structure commonly used by other manufacturers of the '74HC product line. It is beyond the scope of this report to discuss the relative merits of each structure from an ESD protection standpoint. Therefore, how the specifications are affected by each structure is discussed.

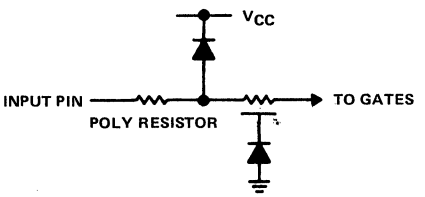


Figure 2. Other Manufacturers' ESD Input Protection Circuitry

From Figure 1 it can be seen that in the Texas Instruments' input structure, a voltage in excess of V_{CC} will be clamped to a V_{BE} above V_{CC} by the protection diode. A voltage below ground will be similarly clamped to a V_{BE} below ground, this time by the base-emitter junction of the distributed n-p-n transistor. Therefore, when the input voltage is taken outside the V_{CC} or ground rails, the characteristics of a forward-biased diode can be seen. Thus, it is meaningless to specify a maximum input voltage (either positive or negative). It is the current through the forward-biased diode which is the limiting parameter. If this current becomes too large, there is the possibility of damage to the device either from blowing the bond wire or excessively heating the diode (or transistor).

The JEDEC committee does indeed recommend a maximum input voltage of V_{CC} + 0.5 V (in the positive direction) and −0.5 V (in the negative direction). This parameter can best be regarded as an indication that the protection devices are present rather than a "traditional" maximum voltage specification. For this reason Texas Instruments does not include this parameter on the data sheet.

The key parameter included on the Texas Instruments data sheet is the input diode current, and this diode current corresponds to the JEDEC recommended limit. The parameter, I_{IK}, has a maximum value of ±20 mA, which is the maximum current that can be allowed to flow continuously through the input protection structures. The peak value of this current has a much higher value and is usually limited by the degree of latch-up protection existing on the input.

The structure shown in Figure 2 is different from the Texas Instruments protection circuitry. In this configuration a polysilicon resistor is located in series with the protection diodes. The affect of this resistor on the input voltage parameters is to limit the current flowing through the protection diodes. The existence of this diode is the reason why some manufacturers have chosen to specify the maximum input voltage as V_{CC} + 1.5 V (positive) and −1.5 V (negative). Since the input voltage corresponds to the V_{BE} of the protection diode plus the IR drop across the resistor, this maximum input voltage specification ensures the current flowing through the input structure is limited to the JEDEC 20 mA value.

OUTPUT STRUCTURES

The output structure is illustrated in Figure 3. In this case it is the same for all manufacturers. Since two of the diodes are parasitic in the output transistors, no alternative is possible. The same considerations discussed earlier for the inputs are true for the outputs. Therefore, the output voltage will also be clamped to a V_{BE} above the supply and below the ground rails. A specification similar to the input diode current exists for the output diode current (I_{OK}). The maximum value is also ±20 mA, corresponding to the JEDEC recommendation. JEDEC also has a recommended maximum output voltage specification of V_{CC} + 0.5 V or −0.5 V. The manufacturers use these same limits when output voltages are specified. As with the maximum input voltage specification, this parameter has limited usefulness.

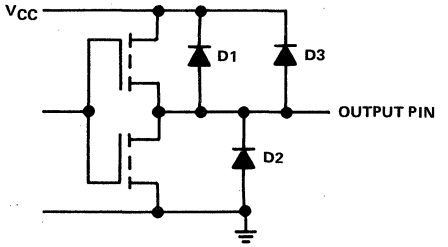


Figure 3. ESD Output Protection Circuitry
D1 AND D2 ARE PARASITIC DIODES

APPLICATION CONSIDERATIONS

Now that the input and output structures and the parameters associated with them have been discussed, their effects in an application will be examined. It is convenient to consider transient effects and steady-state effects individually.

In the steady state, if two systems or subsystems are interconnected, and each has its own power supply, the protection structures limit the difference between the two supply voltages. If this difference exceeds a V_{BE}, then excessive supply current will be drawn from the higher of the two supplies through the input protection structures of devices powered from the other supply (Figure 4). If this

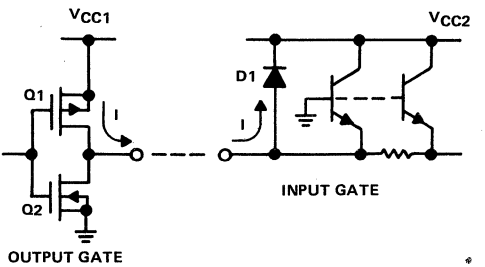
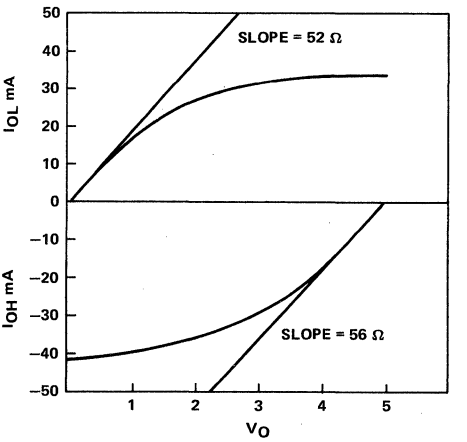


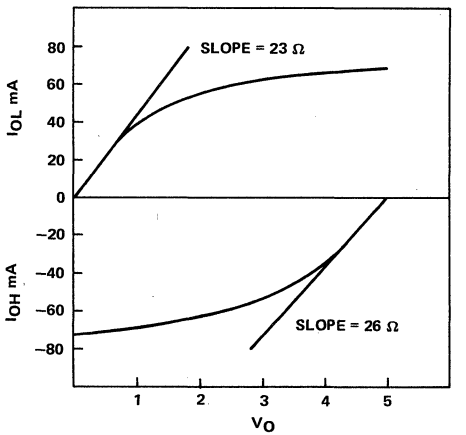
Figure 4. Interconnected Structures with Separate Supplies

current is not limited to a safe value, there is the potential to damage the devices. However, in almost all applications, the increase in supply current will be undesirable. It should be noted in this case that neither of the two input structures offers an advantage over the other as the output protection structures limit the difference in supply voltage. This is the only steady-state effect likely to be of interest in most applications. The only other possibility is that voltages may be applied to '74HC inputs from sources external to the system, and these voltages exceed V_{CC}. In this case, additional resistors will be required in series with the inputs, regardless of the input structure used, in order to limit the input current to a safe value. This situation should be avoided whenever possible as the advantage of the '74HC family's high input impedance will be lost.

Under certain transient load conditions, particularly when driving high capacitances or unterminated transmission lines, undershoot or overshoot can occur. The output impedance of the SN74HC family is approximately 50 Ω for standard outputs, and approximately 25 Ω for high current outputs (Figure 5). This output impedance is symmetrical, having about the same slope regardless of whether the output is in a high or a low state. This alone overcomes many of the transient problems experienced with bipolar circuits, since the SN74HC family's output impedance tends to damp out any overshoot or undershoot.



(a) STANDARD OUTPUT



(b) HIGH-CURRENT OUTPUT

Figure 5. SN74HC Output Impedances (V_{CC} = 5 V, T_A = 25°C)

In an HC system, if undershoot or overshoot is present or exceeds the turn-on voltage of the protection structures, then an excess current will flow for the same reasons discussed. However, this time it will only be a transient current and it is possible to exceed the maximum I_{IK} or I_{OK} ratings without causing damage to the device (I_{IK} and I_{OK} are continuous ratings). Unfortunately there is no peak current limit in the existing specifications. However, in practice the maximum limit is determined by the degree of latch-up immunity offered by the devices being used. This is to be expected since transients of this nature are the major cause of latch-up problems. Therefore the manufacturer's latch-up specifications should be carefully studied to determine how much overshoot or undershoot can be tolerated. A review of the specifications will reveal a considerable variation between manufacturers. Some do not even specify any degree of latch-up suppression. For this reason Texas Instruments developed latch-up suppression circuitry capable of withstanding in excess of 250 mA at 25 °C, or in excess of 100 mA at 125 °C.

Referring to the schematics for the input protection structures (Figures 1 and 2), it will be seen that the version shown in Figure 2 does offer an advantage in the transient mode of operation as the poly resistor will inhibit the current flowing through the diodes. However, the output structures are again the limiting parameter as the outputs are also susceptible to the transients and are capable of latching up under extreme conditions.

In summary, under transient conditions, external current limiting will not be required for most applications unless severe overshoot or undershoot is present which would result in input or output currents comparable to the trigger currents of the parasitic SCRs inherent in HC devices.

CONCLUSION

As a result of the use of different ESD protection structures, manufacturers specify different absolute maximum voltage ratings for the input of HC devices. This difference is of little importance to the system designer. The maximum input current is really the key input parameter which determines whether or not a device will be damaged. The output ESD protection structures, which are inherent in the output transistors, set the lower limit on the maximum voltage that can be withstood on the outputs without forward biasing these protection structures. Such forward biasing may result in excessive current drain or, in extreme cases, device damage.

Using High-Speed CMOS and Advanced CMOS Logic in Systems with Multiple V_{CC} Supplies or Partial Power-Down

Rick Curtis

TEXAS INSTRUMENTS

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TI warrants performance of its semiconductor products to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems such testing necessary to support this warranty. Unless mandated by government requirements, specific testing of all parameters of each device is not necessarily performed.

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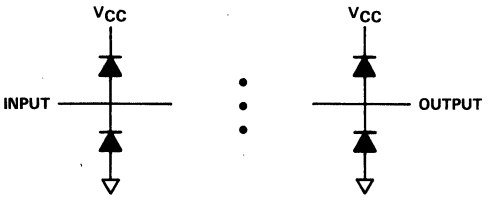
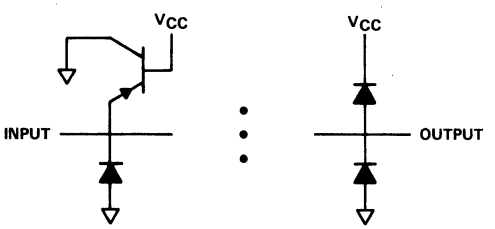
CMOS devices offer a designer many desirable features, the most important one being a low power consumption. However, in some systems a designer will find that even the low power consumption of CMOS is insufficient to meet his power supply constraints. Therefore, some designers will utilize partial system power-down or multiple V_{CC} supplies to meet their system power requirements.

Whenever a system incorporates the use of multiple V_{CC} supplies or partial power-down, the designer must take into account several important device parameters if he is using High-Speed CMOS (HC) or Advanced CMOS (ACL) devices. This is necessary to avoid excessive power dissipation and prevent damage to a device that could lead to a degradation in the reliability of the device. These parameters are the continuous input and output diode currents (I_{IK} and I_{OK}) and the continuous output current (I_O). I_{IK} and I_{OK} refer to the continuous current that is flowing through the input and output electrostatic discharge (ESD) protection circuits (Figure 1 shows functionally equivalent schematics of the ESD structures for HC and ACL devices).



(a) HC EQUIVALENT ESD STRUCTURE



(b) ACL EQUIVALENT ESD STRUCTURE

Figure 1. Simplified ESD Structures for HC and ACL Devices

I_O is the continuous current flowing through one of the two output transistors. Table 1 shows the absolute maximum ratings for I_{IK}, I_{OK}, and I_O for both HC and ACL devices, as listed on device data sheets.

Table 1. Absolute Maximum Values for I_O, I_{IK} and I_{OK}

PARAMETER	ABSOLUTE MAXIMUM	
	HIGH-SPEED CMOS (HC)	ADVANCED CMOS (ACL)
I_O	±25 mA (Standard) ±35 mA (High-Current)	±50 mA
I_{IK}	±20 mA	±20 mA
I_{OK}	±20 mA	±20 mA

To understand how I_{IK}, I_{OK}, and I_O can affect a system design, consider an example of a partial system power-down. Figure 2 illustrates a partial power-down situation where a device powered with V_{CC} = 5 V is driving a device without power applied. The input voltage to the non-powered device exceeds V_{CC} by more than the threshold voltage (0.6 to 0.8 volts), causing the ESD protection structure to conduct whenever the output of the driver is in a high state. Therefore, the driving device will power-up the receiving device and any other device sharing the same V_{CC} line. If no current limiting is provided, then the maximum I_O of the driving device and the maximum I_{IK} of the receiving device could be exceeded.

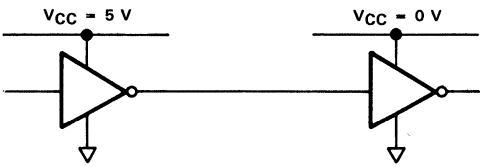
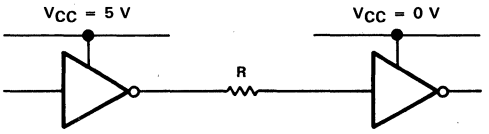
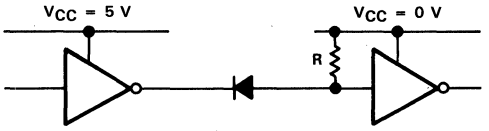


Figure 2. Example of Partial System Power-Down

Several methods are available to protect the driving and receiving devices during partial system power-down. If the driving device has three-state outputs, then placing the outputs in a high-impedance state will provide the best solution. However, if this is not a viable option, then some method of current limiting must be provided. Figure 3 shows several methods that can be used, with current-limiting series resistors being the simplest. The value of the resistor is chosen to limit the current into the receiving device to less than 20 mA. The major drawback to using a current-limiting resistor is power dissipation. Another drawback is the effect that the resistor has on the input transition time at the receiving device during normal system operation. If the total capacitance of the interconnects and receiving devices is high (i.e., a high-capacitance bus), then a current-limiting resistor will increase the input transition time. A system designer will have to ensure that the addition of the resistor will not increase the input transition time above the maximum input transition time of the receiving device.



(a) RESISTOR CURRENT LIMITING



(b) RESISTOR-DIODE CURRENT LIMITING

Figure 3. Current Limiting for a Partial System Power-Down

A second method of current limiting shown in Figure 3 involves the use of a pull-up resistor and a diode. The advantage of this method is that it allows for the use of a large resistor, thereby holding power dissipation to a minimum. The disadvantage of this method is that it requires the use of additional components and results in a higher value of V_{IL} at the receiving device.

A second example of how a partial power-down can cause unwanted operation is the case of two drivers connected to the same bus with one device powered down, as shown in Figure 4. In this case, the first bus driver will attempt to power-up the second bus driver and any other devices sharing the same V_{CC} line through the output ESD structure of the unpowered device.

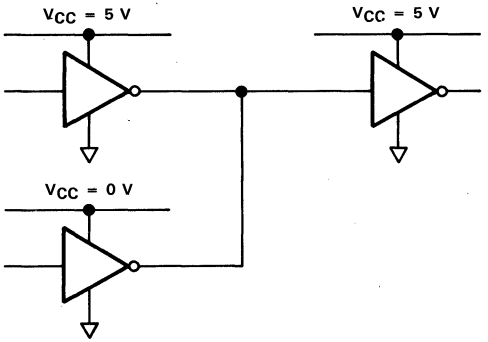
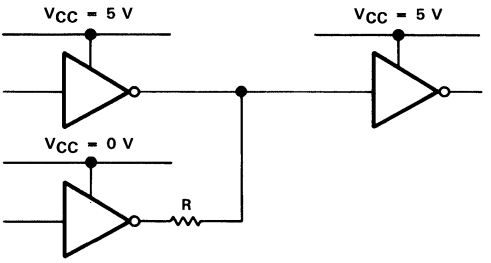


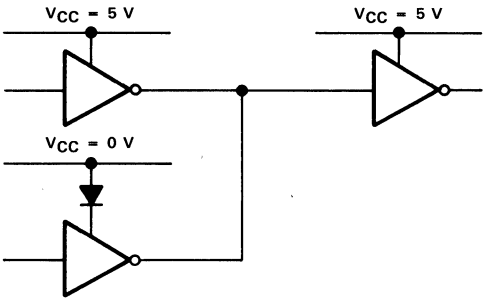
Figure 4. Partial Power-Down with Bus Drivers

Several methods are available to solve this type of problem. One method is simply to use a current limiting resistor as outlined above. Another solution is to isolate the unpowered driver from the V_{CC} line by means of a diode between the power pin and the V_{CC} supply. If the unpowered device is a transceiver, then pull-up or pull-down resistors are required on the output control inputs to disable the outputs. Not disabling the transceiver outputs would allow the transceiver to power up the unpowered devices that are driven by its outputs. Whenever an isolating diode is used, the V_{CC} at the driver will always be a diode forward drop below the voltage of the supply, resulting in a degradation of V_{OH}. Figure 5 illustrates these circuit solutions.

Another example of a system that could require current limiting protection is one that uses multiple V_{CC} supplies, or provides each card with its own on-board voltage regulator. If the V_{CC} supplies of two connecting devices differ by more than 0.5 V dc, then a current limiting scheme should be considered if the driving device is a CMOS device and is connected to the higher V_{CC}. This is necessary because V_{OH} of a CMOS device will be the same as V_{CC} whenever the I_{OH} requirement is very small. Therefore the input ESD protection diode could conduct if the V_{CC} of the driver (or V_{OH}) exceeds the V_{CC} of the receiver by more than 0.5 V dc. It should be pointed out that it is the resulting current flow that causes the degradation of the diode, not the voltage. Note: This applies only to supplies that vary by more than 0.5 V dc. Dynamic switching currents could cause transient voltage spiking on V_{CC} lines such that a 0.5 V difference between supplies could easily exist. These transients will not cause a problem as long as their duration is short (less than 20 ns).



(a) CURRENT LIMITING RESISTOR



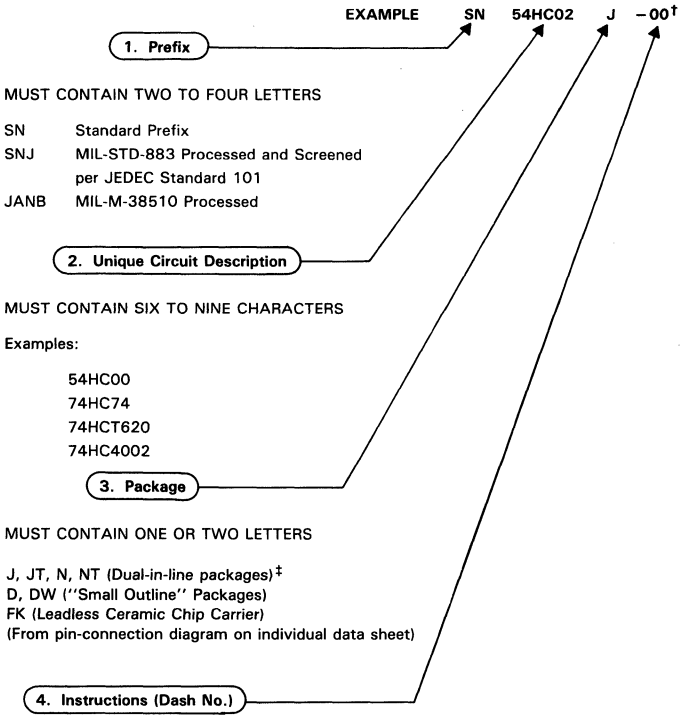
(b) DIODE ISOLATION (FOR A TRANSCEIVER, DISABLE OUTPUTS)

Figure 5. Current Limiting for Bus Drivers During Partial Power-Down

Partial system power-down offers a designer a convenient method to save on system power consumption. However, when a partial power-down scheme is used, a designer must take steps to ensure that no damage occurs to devices and to avoid excessive power dissipation. He must also take similar precautions when using multiple V_{CC} supplies if the supplies of two connecting devices differ by more than 0.5 V dc.

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



†For tape and reel information refer to page 15 of this section.

‡These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

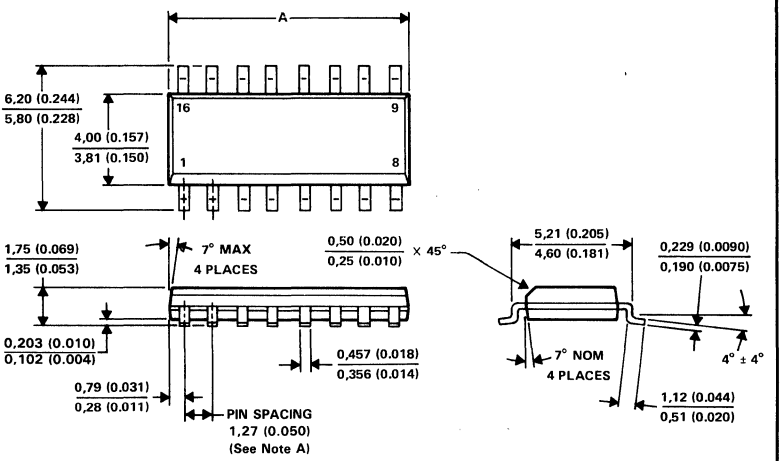
Dual-in-line (J, JT, N, NT)

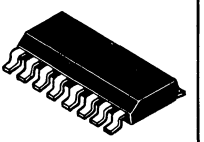
- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier (N only)
- Sectioned Cardboard Box
- Individual Plastic Box

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D PLASTIC PACKAGE
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

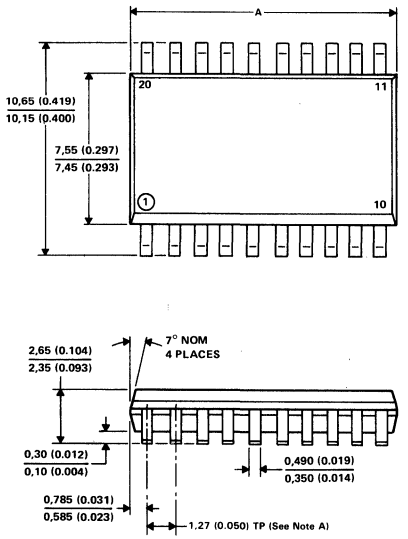
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

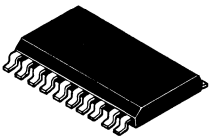
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW PLASTIC PACKAGE
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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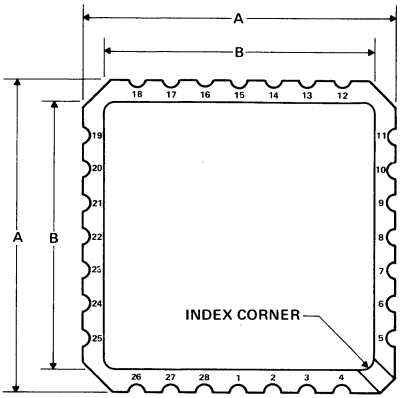
FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

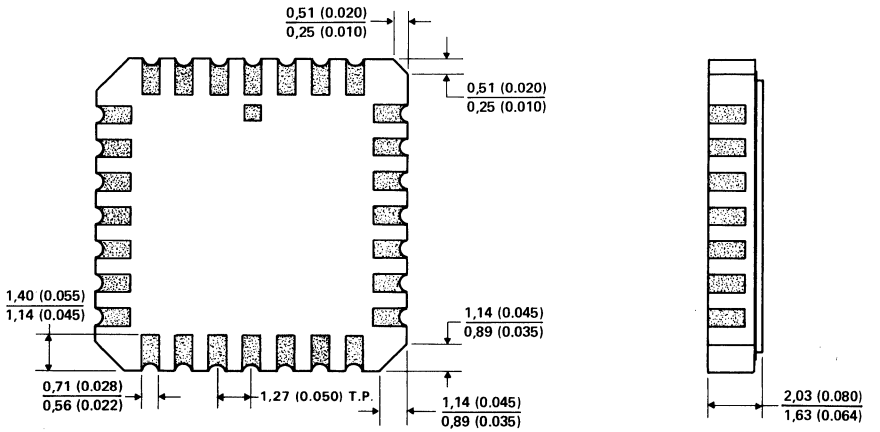
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

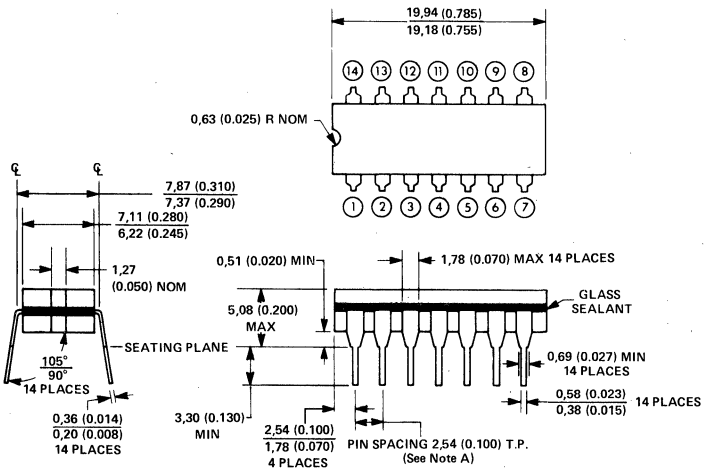


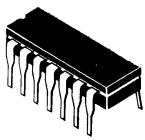
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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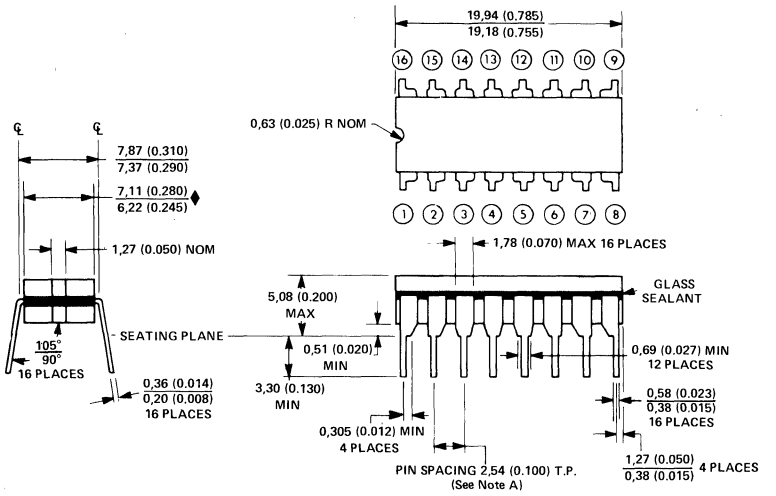
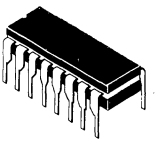
J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

16-PIN J CERAMIC





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

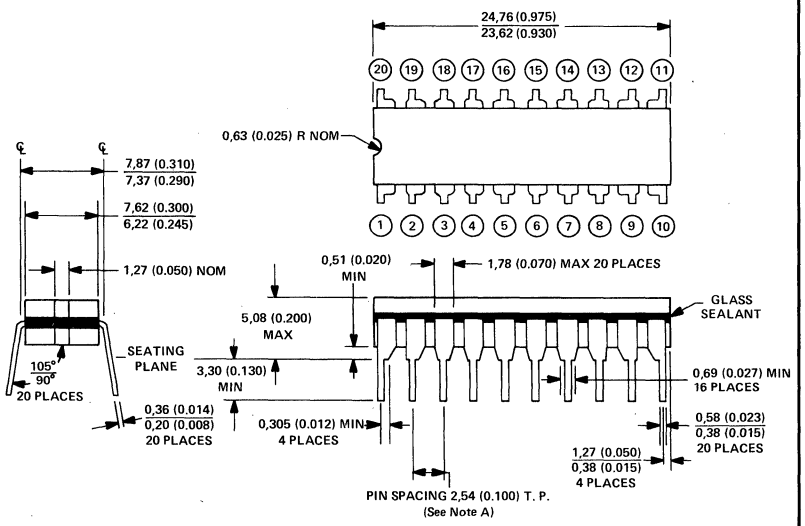
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

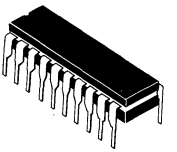
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

20-PIN J CERAMIC





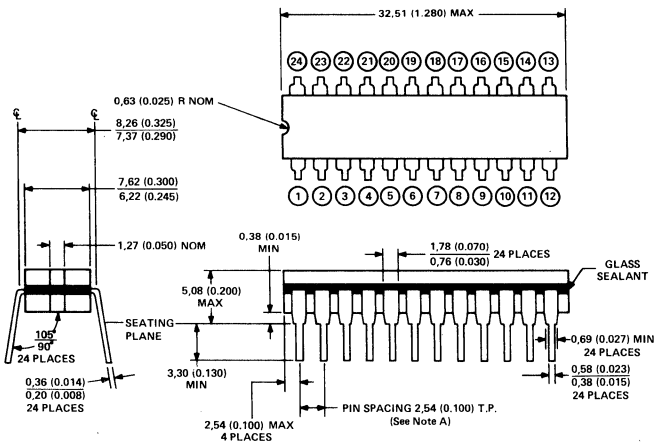
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

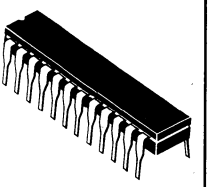
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-diped'') pins require no additional cleaning or processing when used in soldered assembly.

24-PIN JT CERAMIC





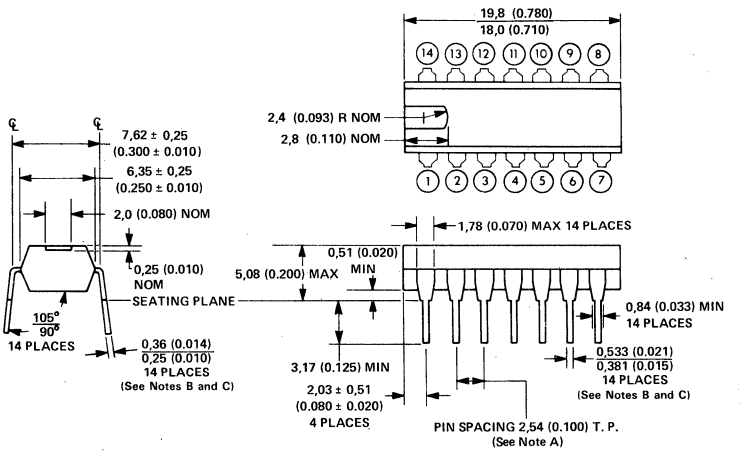
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

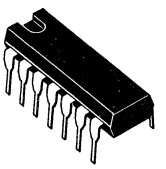
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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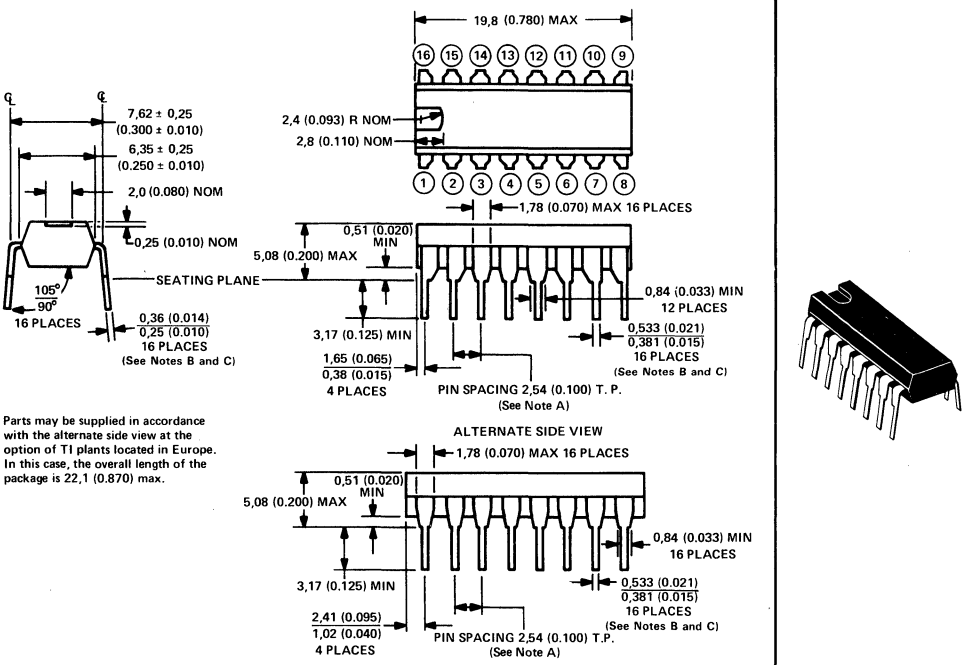
N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN N PLASTIC



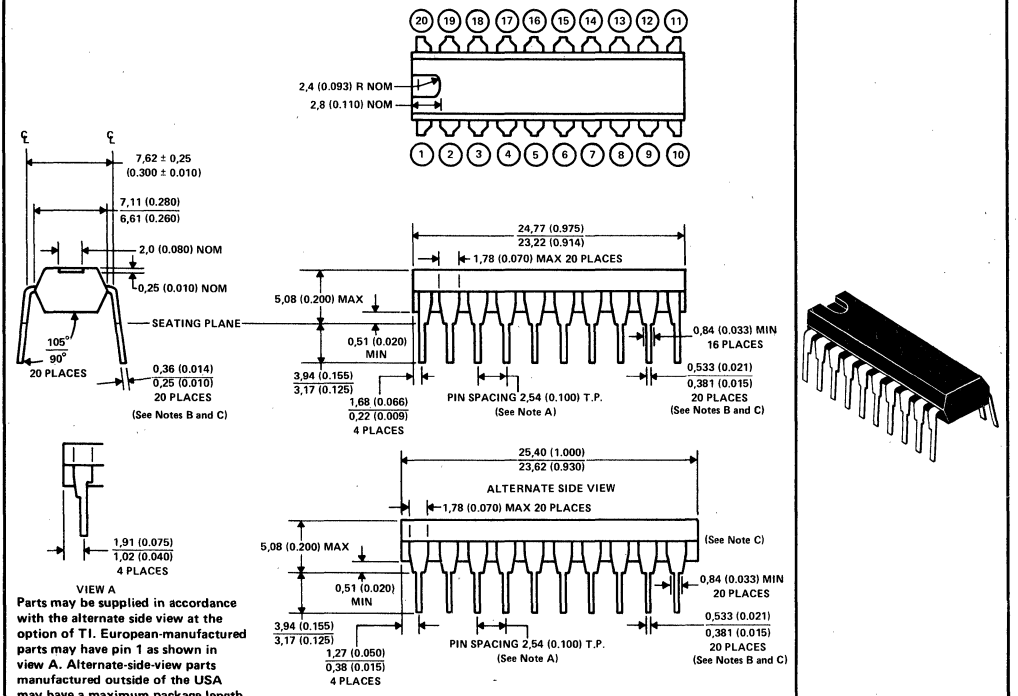
ALL LINEAR DIMFNSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN N PLASTIC



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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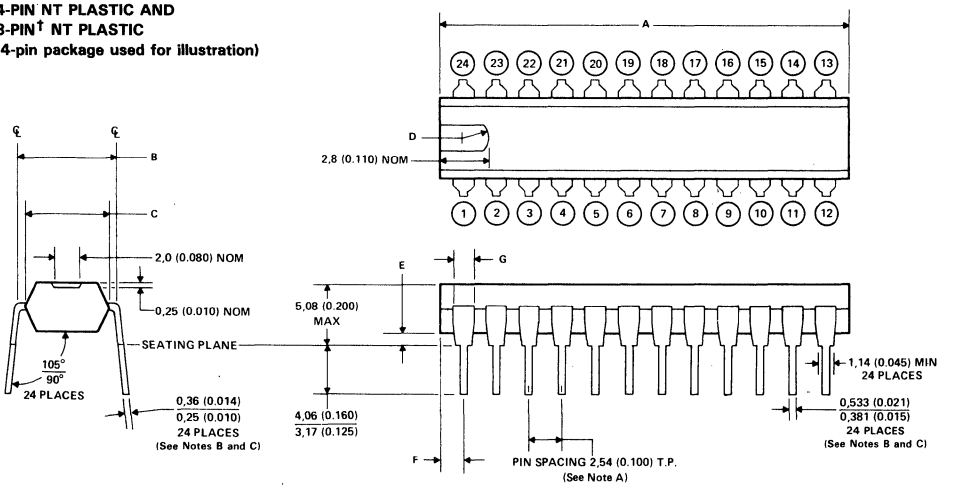
NT plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

24-PIN NT PLASTIC AND
28-PIN† NT PLASTIC
(24-pin package used for illustration)



DIM / DESIGNATION	A MIN	A MAX	B	C MAX	D R NOM	E MIN	F MIN	F MAX	G MIN	G MAX
NT024	28,6 (1.125)	31,8 (1.250)	7,62 ± 0,25 (0.300 ± 0.010)	7,1 (0.280)	2,4 (0.093)	0.38 (0.015)	0,71 (0.028)	2,16 (0.085)	1,14 (0.045)	1,78 (0.070)
NT028†	34,0 (1.338)	37,1 (1.462)	7,88 ± 0,25 (0.310 ± 0.010)	6,86 (0.270)	1,02 (0.040)	0,51 (0.020)	0,51 (0.020)	2,03 (0.080)	1,02 (0.040)	1,78 (0.070)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Each pin centerline is located within 0.25 mm (0.010 inch) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

Tape and Reel Information

A new packaging system, *SMti*™ Tape and Reel, has emerged along with the introduction of surface-mount semiconductor packages by Texas Instruments.

Benefits

SMti Tape and Reel not only offers a new shipping method that protects components from mechanical and electrical damage, but also includes the benefits of automated inventory control, ship to stock, and total compatibility with today's automated placement systems. *SMti* Tape and Reel continues the trend towards industry automation and cost reduction and contributes to the overall goal of electronic system quality and reliability.

Features

The features of *SMti* Tape and Reel packaging are as follows.

- *SMti* Tape and Reel packaging is in full compliance with EIA Standard 481-A, "Taping of Surface-Mount Components for Automatic Placement."
- Industry-compatible tape format allows second sourcing without costly and time-consuming equipment changeovers and record-keeping changes.
- Static-inhibiting materials, used in carrier tape manufacture, provide device protection from static damage.
- Rigid, dust-free polystyrene reels provide mechanical protection and clean room compatibility for optimum equipment operation and manufacturing yield.
- Completely compatible with dereeling equipment currently available on most high-speed automated placement systems.
- Medium-density Code 39 bar coding enables inventory and manufacturing automation, as well as complete component traceability prior to, during, and after system manufacture.
- Efficient packaging offers savings in storage space and manufacturing overhead.

SMti SURFACE MOUNT TEXAS INSTRUMENTS and *SMti* are trademarks of Texas Instruments Incorporated.

General Description

***SMti* Tape and Reel offers users of surface-mounted semiconductor devices a new and efficient method of component handling. Tape and reel consists of three major elements: a carrier tape, a cover tape, and a reel.**

Carrier Tape

The carrier tape is a conductive material with custom-embossed pockets for a particular surface-mount package. Components are oriented in the embossed pockets per EIA 481-A specification "Taping of Surface-Mount Components for Automatic Placement."

Cover Tape

With each component in its embossment and protected from mechanical and static damage, a continuous opaque cover tape is heat sealed over the entire length of the carrier tape, isolating each component from the outside environment. This heat-sealing process guarantees sufficient seal strength to prevent components from falling from the pockets before use. The cover tape has a peel strength of 40 ±30 grams in compliance with EIA 481-A and sufficient strength to ensure consistency during dereeling operations.

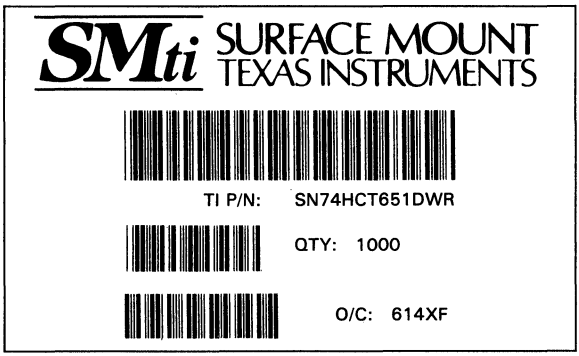
Reel

The entire assemblage is wound on a high-strength polystyrene-based reel. The reel provides a means of easy storage and handling as well as a method for feeding large quantities of packages to high-speed placement systems. In addition, *SMti* Tape and Reel offers a factory-automation alternative through the use of medium-density Code 39 bar coding on all reel assemblies. The bar code provides source, part number, date code, and quantity.

Bar-Code Labeling

Each reel of *SMti* components is labeled with a "man-and-machine" readable label that uses a medium-density Code 39 bar code in combination with alphanumeric characters.

Figure 1 ***Bar-Code Label***



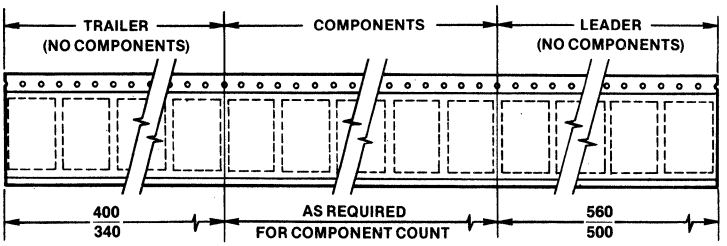
Note

1. Sample labels are available for system compatibility testing.

Specification

***SMti* Tape and Reel components are available in formats that are compatible with most industry standard component loading and tape drive equipment. Figures 2 through 5 and Tables 1 through 6 provide information regarding these formats. All dimensions are given in millimeters.**

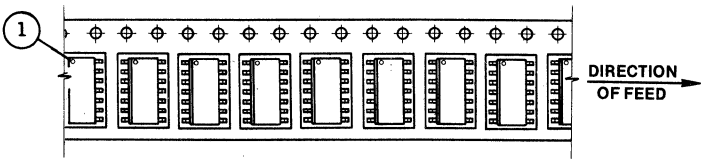
Figure 2 ***Tape Format***



Notes

1. Carrier tape is conductive with a resistivity value of less than 1×10^5 ohms per square.
2. Cover tape is sealed over the entire length of the carrier tape.

Figure 3 ***Component Format*** *(All components are packaged per Note 1.)*



Note

1. Pin 1 orientation.

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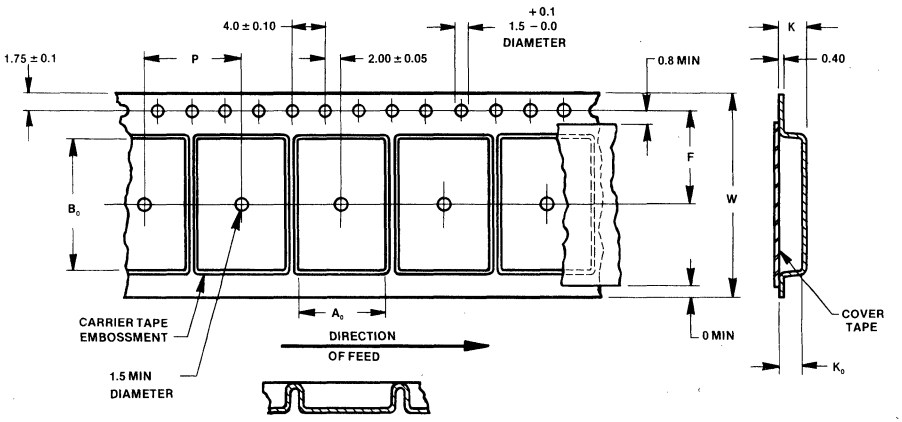
Specification (Continued)

Variables are used in Figure 4 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 4 ***Single-Sprocket Tape Dimensions***



Notes

1. Tape widths are 12, 16, and 24 mm.
2. Camber per EIA Standard 481-A.
3. Minimum bending radius per EIA Standard 481-A.

Specification (Continued)

Table 1 *Single-Sprocket Variable Tape Dimensions*

Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
SO-14	D	16	8	6.5	9.5	2.1	2.5	7.5
SO-16	D	16	8	6.5	10.3	2.1	2.5	7.5
SO-16L	DW	16	12	10.9	10.7	3.0	3.4	7.5
SO-20L	DW	24	12	10.9	13.2	3.0	3.4	11.5
SO-24L	DW	24	12	10.9	15.8	3.0	3.4	11.5
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

Specification (Continued)

Variables are used in Figure 5 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Figure 5 ***Reel Dimensions***

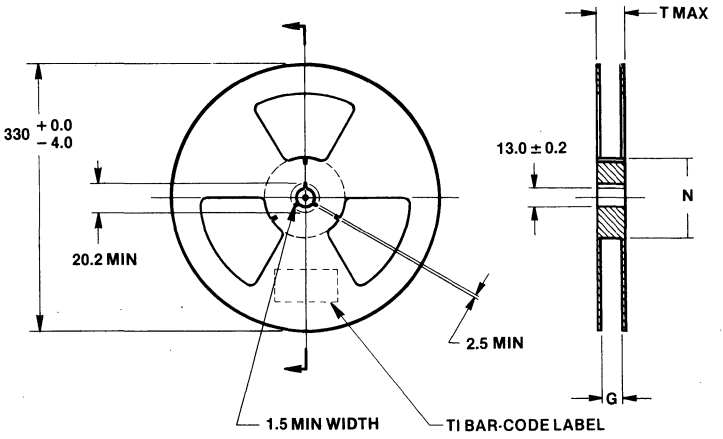


Table 2 ***Variable Reel Dimensions***

Package Type	Package Designator	Dimension G	T	N
SO-14	D	16.4	22.4	100
SO-16	D	16.4	22.4	100
SO-16L	DW	16.4	22.4	100
SO-20L	DW	24.4	30.4	100
SO-24L	DW	24.4	30.4	100

Specification (Continued)

All dimensions are given in millimeters.

Table 3 *Tape and Reel Format Summary*

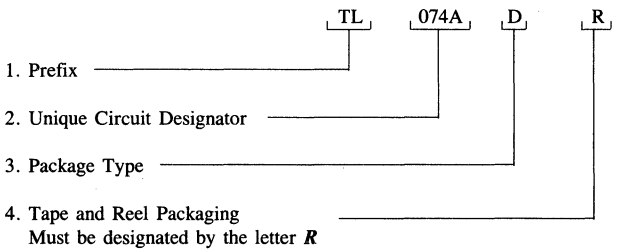
Package Type	Package Designator	Tape Width	Package Pitch	Pocket Width	Dimensions Length	Depth	Reel Diameter	Reel Hub Diameter	Parts Per Reel
SO-14	D	16	8	6.5	9.0	2.1	330	100	2500
SO-16	D	16	8	6.5	10.3	2.1	330	100	2500
SO-16L	DW	16	12	10.9	10.7	3.0	330	100	1000
SO-20L	DW	24	12	10.9	13.2	3.0	330	100	1000
SO-24L	DW	24	12	10.9	15.8	3.0	330	100	1000

Ordering Information

To order tape and reel components, you need to provide information about part numbers, quantities, shipping, and sample package applications.

Ordering by Part Number

When ordering tape and reel components, add the letter ***R*** as a suffix to the part number. An example of the ordering sequence follows.



Formats and Quantities

All orders for tape and reel packaging **must be for whole reels.** For example, if a customer requires 9,900 TL074s in Tape and Reel packaging, he needs to place the order for a quantity of 10,000 TL074s. The order will be filled and shipped on four reels containing 2,500 parts per reel.

Note: TI reserves the right to provide a smaller quantity of devices per reel to preserve date code integrity.

A list of package and tape formats and the quantity of devices per reel is provided in Table 4.

Shipping

Taped and reeled components are shipped in individual packing boxes measuring approximately 14'' × 14''. The depth of each box is tailored to the tape width. Individual boxes are packed in a larger box whose size depends on the quantity of components ordered.

Ordering Information (Continued)

All dimensions are given in millimeters.

Table 4 *Condensed Tape and Reel Formats*

Package Type	Package Designator	Tape Width	Package Pitch	Reel Diameter	Parts Per Reel
SO-14	D	16	8	330	2500
SO-16	D	16	8	330	2500
SO-16L	DW	16	12	330	1000
SO-20L	DW	24	12	330	1000
SO-24L	DW	24	12	330	1000

Sample Package Applications

Sample components are available for a number of applications, such as standard mechanical sample packages, "daisy-chained" bars, and K-factor bars. Table 5 provides sample ordering information.

Table 5 *Sample Package Applications*

Package Type	Package Designator	Mechanical Sample	Daisy Chain	K Factor
SO-14	D	SN72197	SN200054	SN200060
SO-16	D	SN72198	SN200055	SN200061
SO-16L	DW	N/A	N/A	N/A
SO-20L	DW	SN72199	SN200056	SN200062
SO-24L	DW	SN72200	SN200057	SN200063

More Information

As a major manufacturer of SMCs, TI is committed to helping you make the transition to surface-mount as easy and as economical as possible. Getting started in SMT—switching from older and less efficient methods of PCB fabrication—means learning some new manufacturing techniques, and it entails some capital outlay. But in volume production, it can actually reduce your capital and space costs by up to 50 percent.

Ship-to-Stock Eliminates Incoming Inspection

As your usage per surface-mount component (SMC) grows, TI can implement its ship-to stock program for you. With all the necessary quality-control procedures built into our standard testing process, your SMCs can be shipped directly to you in tape and reel or in factory-sealed boxes. Benefits to you:

- Incoming inspection, scrap, and rework reduced or eliminated.
- Inventory reduced.
- Quality levels maximized.

Learn by Doing

To help you realize the advantages of surface-mount technology (SMT), Texas Instruments maintains a surface-mount laboratory. There you can gain hands-on experience and guidance in building a surface-mount board from start to finish. To schedule an appointment, contact your TI Field Sales Engineer or call (800) 232-3200 for the address of the TI Field Sales Office nearest you.

Outside Help Available

You can also find assistance among the growing number of SMT assembly houses, consultants, and associations. They can help you reduce the costs of converting to SMT, while supplying some valuable information on the latest technological advances and industry standards.

Suppliers of assembly equipment such as pick-and-place machines and soldering and test equipment can also help you make the transition to SMT board fabrication.

Want to Learn More?

How to Use Surface Mount Technology is available free of charge from Texas Instruments. This technical summary includes chapters on the process and the tooling required to implement it; the wide variety of available SMCs; inspection, testing, and repair; quality and reliability; and how to mix SMCs with standard DIP packages.

For additional information on the availability of TI's growing line of SMCs, contact your local TI Field Sales Office or distributor.

If you would like to have your name placed on our mailing list for additional SMT information as it becomes available from TI, please write Texas Instruments Incorporated, Dept. SSP05, P.O. Box 809066, Dallas, Texas 75380-9066.

INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-in-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Quad In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outlilne	J Lead
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3
Attleboro, Massachusetts 02703
Telephone: (617) 699-5242/5375
TELEX: 92-7708

PERFORMANCE SPECIFICATIONS

Mechanical

Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

Electrical

Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

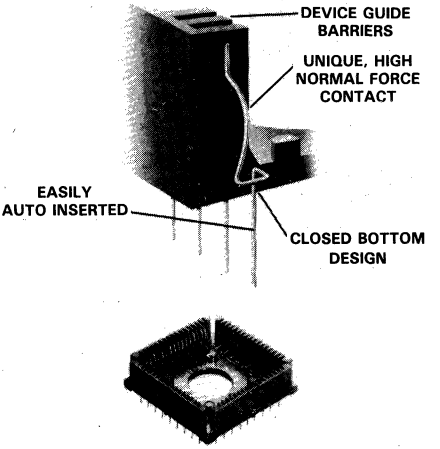
Environmental

Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS

Body – Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts – CDA 510 spring temper
Contact finish – 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information

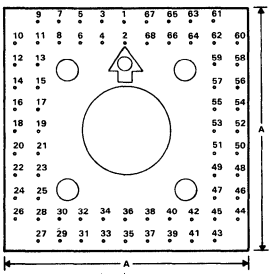


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

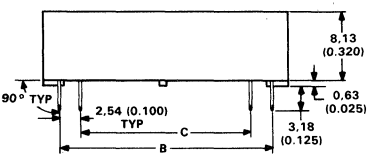
- O: Contact surface 1 – tin/lead plating
- X: Contact spacing 1 - 0.050 in
- XXX: Number of pos (044, 052, 068, 084)
- PH: Plated thru hole, solder tail
- CPR: TI socket Series, Plastic leaded chip carrier

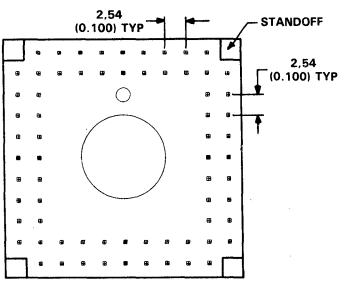
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

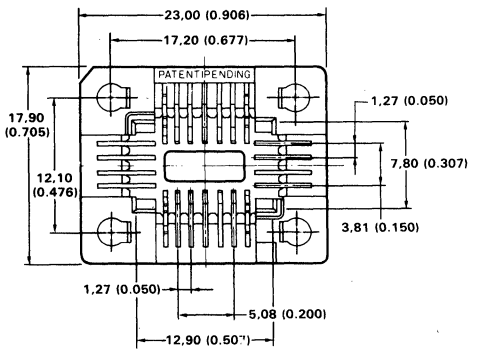
Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

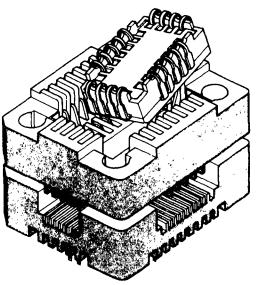
Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PLCC BURN-IN/TEST SOCKETS CPJ SERIES



Dimensions in parentheses are inches
Contact factory for detailed information

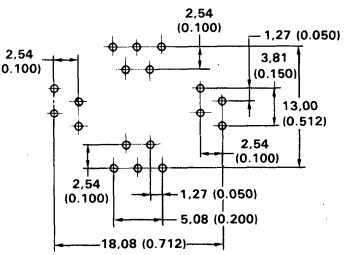


PART NUMBER SYSTEM

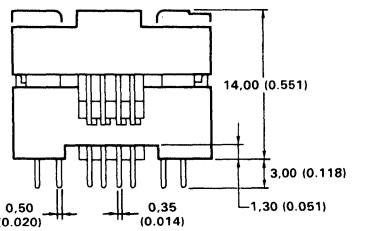
CPJ XX XX X – XXX – B

- CPJ: TI Burn-in PLCC series
- XX: Material — AA = copper alloy
- XX: Contact finish — 33 = overall gold plate
- X: Pitch — A = 0.050
- XXX: Number of contacts
- B

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



PERFORMANCE SPECIFICATIONS†

Mechanical
Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

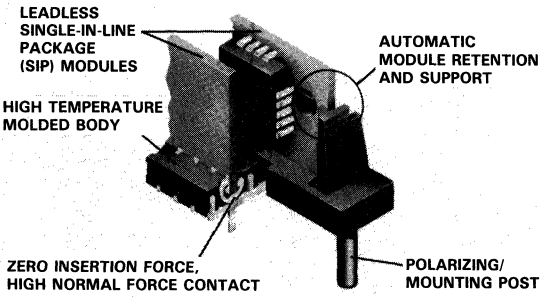
Electrical
Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

Environmental
(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS
Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 μin tin/lead over min 50μin nickel overall
Post plate min 30 μin hard gold over min 75 μin nickel overall

For additional plating options contact the factory.



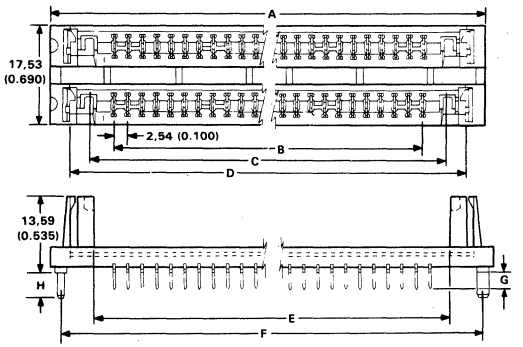
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

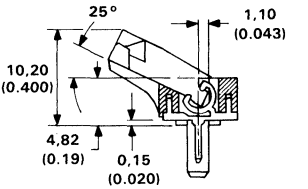
- XX (last) — Variations: 00 — standard product
- XX — Size (number of contacts per row)
- X — Housing material: A — PES
- XX — Contact base material/plating: 01—C17000/30 μin gold; 02—CA510/30 μin gold; 03—C17000/200 μin tin/lead; 04—CA510/200 μin tin/lead
- XX — Configuration/row-to-row spacing: 01—single row/N/A; 03—dual row/0.300 in; 04—dual row/0.400 in; 05—dual row/0.500 in
- TS8X — Series number denotes: 0—0.100 in pitch, vertical mount; 1—0.100 in pitch, low-profile (25°) mount

Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



SINGLE ROW LOW PROFILE



Ckt. Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Contact factory for detailed information

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

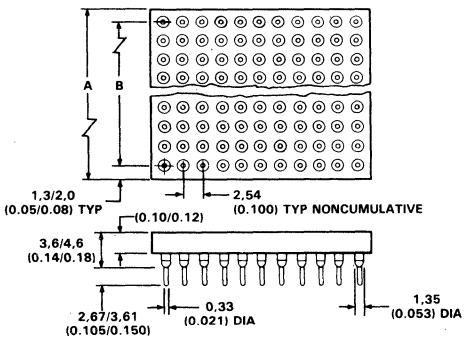
Environmental

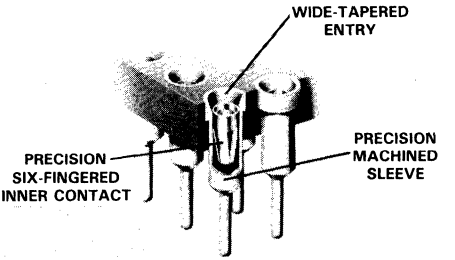
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX – XXX X X – X X

Pin Length

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

Plating

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

Body Style and Orientation
Contact Loading Pattern
Number of Pins 024 to 324
Overall Grid Size 5×5=05 to 18×18=18
BODY MATERIAL
G — Glass Filled Epoxy
P — PBT Polyester
TI Socket
Pin Grid Array

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

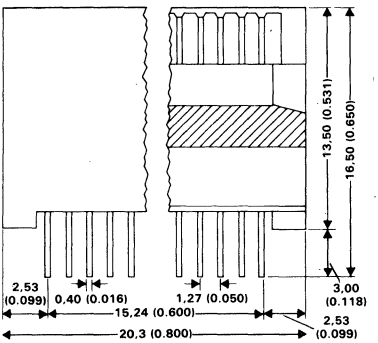
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

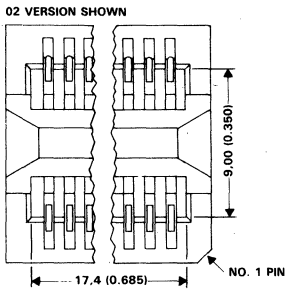
Environmental

Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

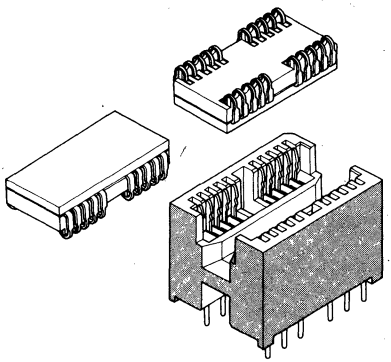
MATERIALS

Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating





Dimensions in parentheses are inches
Contact factory for detailed information



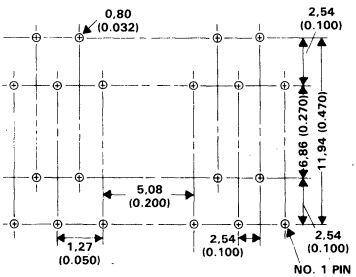
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT — TI SOJ series
- XXX — Number of Contacts
- XX — Contact Finish
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX — Body Variation
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X — Body Material
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

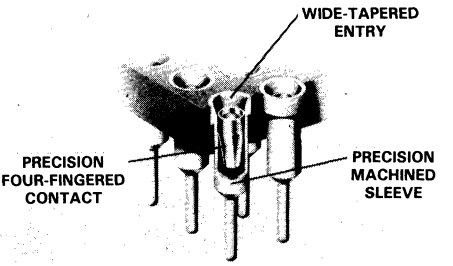
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

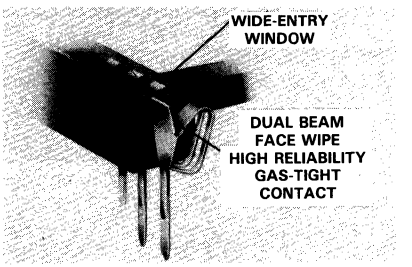


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX – X X

- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail
- (X): S — Single-in-line package (where applicable)
- XX: Number of Positions
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- X: Variations
  - Solder Tail : 9 Pin length 0.125 Typ
  - Wire Wrap : 3 Pin length 0.510

C86 SERIES — STAMPED AND FORMED

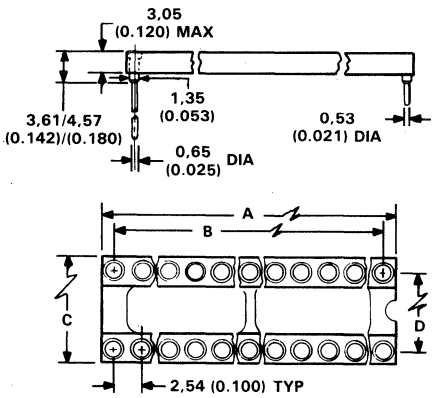


C86 SERIES PART NUMBER SYSTEM

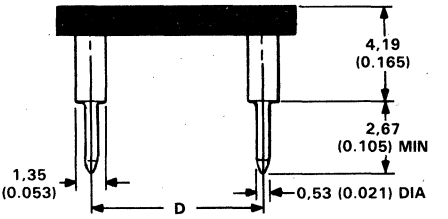
C 86 XX – 01

- C: TI Socket Series
- 86: Tin Dual Beam Face Wipe
- XX: Number of positions
- 01: Variation
  - 01 — Standard product

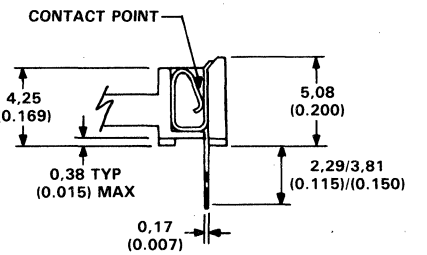
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles — CM Series, 5K cycles — CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

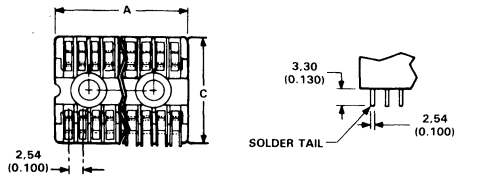
Operating temperature: −65°C to 170°C — CP/CM Series,
−65°C to 150°C — CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

MATERIALS

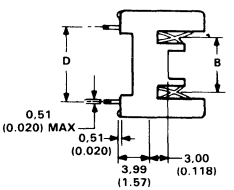
Body — PPS (polyphenylen sulfide) UL 94 V-0
Contacts — Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

†For additional plating options consult the factory

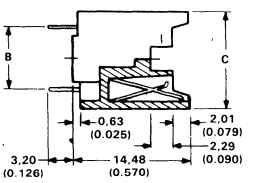
BURN-IN/TEST DIP SOCKETS



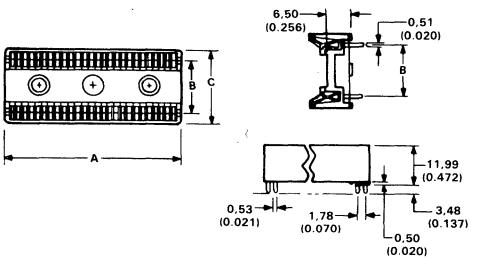
CQ37 SERIES



CP37 SERIES



CM37 SERIES



PART NUMBER SYSTEM

C X 37 XX – 22 S X

- C — TI Socket Series
- X — Series Features: Q — Auto unloadable; P — High density mounting; M — Shrink 0.070 centers
- 37 — Overall gold plate
- XX — Number of positions
- 22 — Copper nickel alloy Soldertail
- S — PPS high temperature body material
- X — Pin to pin: A — 0.100 centers; B — 0.070 centers

CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)			
16	22,35 (0.880)	12,70	15,24	7,62
18	24,89 (0.980)	(0.500)	(0.600)	(0.300)
20	27,43 (1.080)			
24	32,51 (1,280)			
28	37,59 (1.480)	19,05	22,86	15,24
40	52,83 (2.080)	(0.750)	(0.900)	(0.600)
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)		
14	17,78 (0.700)	7,62	12,70
16	20,32 (0.800)	(0.300)	(0.500)
18	22,86 (0.900)		
20	25,40 (1.000)		
24	30,48 (1.200)	15,24	20,32
28	35,56 (1.400)	(0.600)	(0.800)
40	50,80 (2.000)		

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)		
42	39,62 (1.560)	16,51 (0.650)	23,11 (0.910)
54	50,29 (1.980)		
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

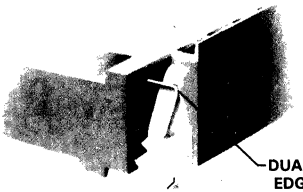
Dimensions in parentheses are inches
Contact factory for detailed information

PERFORMANCE SPECIFICATIONS

Insertion force: 16 oz (454 g) per pin max
Withdrawal force: 1.5 oz (42 g) per pin min
Operating temperature: −40°C to 100°C, tin/lead
Accommodates IC leads 0.011 ± 0.0003 in by 0.018 ± 0.003 in
Contact rating: 1 A per contact

MATERIALS

Body — PBT polyester UL 94 V-0
C4S & CxW Contacts — Copper alloy
Contact finish — Reflow tin plating, 40 µin min



PART NUMBER SYSTEM FOR CxW SERIES

C X W XX − 11

- XX — Number of contacts (42, 52, 64)
- W — Staggered leads
- X — 5 − 64 contacts; 6 − 42, 52 contacts
- C — TI Socket Series

QUAD-IN-LINE (CxW SERIES)

Product Number	A Max Length	B Row to Row	C Max Row to Row
C5W64-11	41,90 (1.65)	22,90 (0.950)	19,05 (0.750)
C6W42-11	27,90 (1.10)	22,90 (0.900)	17,80 (0.700)
C6W52-11	34,30 (1.35)	22,90 (0.900)	17,80 (0.700)

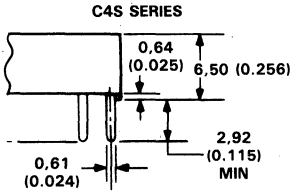
Dimensions in parentheses are inches
Contact factory for detailed information

PART NUMBER SYSTEM† FOR C4S SERIES

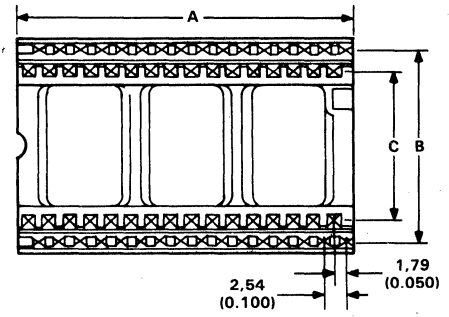
C 4 S XX − 02

- XX — Number of contacts 28, 40, 42, 52, 54, 64
- S — Shrink Pack (0.070 in pin-to-pin contact spacing)
- 4 — Reflow tin plating
- C — TI Socket Series

†Also available in screw machine contacts



QUAD-IN-LINE (CxW SERIES)

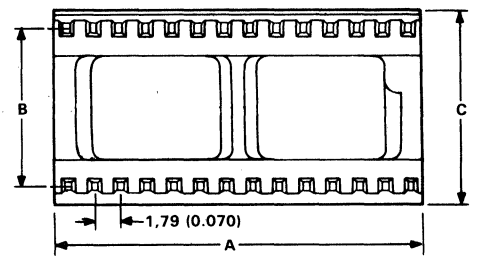


C4S SERIES

Positions	A Max Length	B Row to Row	C Max Width
28	25,02 (0.985)	10,16 (0.400)	13,00 (0.512)
40	35,69 (1.405)	15,24 (0.600)	17,98 (0.708)
64	57,07 (2.247)	19,05 (0.750)	21,62 (0.851)

Dimensions in parentheses are inches

SHRINK PACK DIP (C4S SERIES)



TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 5000 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

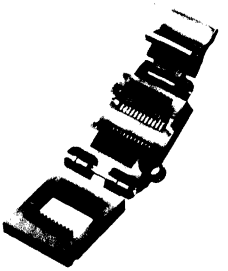
Operating temperature: −65°C to 170°C
Humidity: 10 mΩ max contact resistance change when tested per MIL-STD 202, Method 103B
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — CFP Series — PES (polyether sulfone) glass filled UL 94 V-0
Temperature: −65°C to 170°C
Contact — Beryllium copper
Plating:† Overall gold plate min 4 μin over min 70 μin nickel plating

†For additional plating option consult the factory.
Dimensional drawings available from factory.

SMALL OUTLINE FLAT PACK (CFPH/K SERIES)

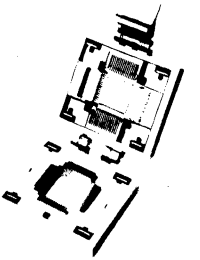


PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C: TI Series socket
- XX: Style FP — Flat pack
- X: Configuration
  - H — 14, 16, 18, 20 Positions
  - K — 24, 28 Positions
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01

QUAD FLAT PACK (CFPM SERIES)

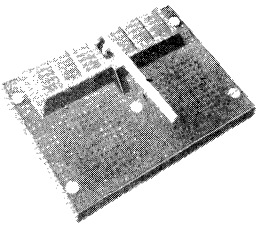


PART NUMBER SYSTEM

CXX X – XXX – XX – 01X

- CXX: TI socket
  - Style PF — Flat pack
- X: Configuration
  - M — Quad pack
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01X: Variations
  - A — 1.0 mm ℄ contact spacing
  - B — 0.8 mm ℄ contact spacing

PIN GRID ARRAY (CZFW SERIES)



PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C: TI Series socket
- XX: Style ZF — Zero force
- X: Configuration
  - W — 11 × 11 × 2
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01

AVAILABLE SIZES

CFPH Series 14, 16, 18, 20 CFPK Series 24, 28	Small Outline Flat Pack
CFPM Series 64, 80	Quad Flat Pack
CZFW Series 11 × 11 × 2	Pin Grid Array

Contact factory for detailed information

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