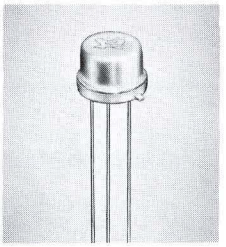
N-P-N TYPES 2N1302, 2N1304, 2N1306, 2N1308
P-N-P TYPES 2N1303, 2N1305, 2N1307, 2N1309
COMPLEMENTARY ALLOY-JUNCTION GERMANIUM TRANSISTOR

TPYES 2N1302, 2N1304, 2N1306, 2N1308
TYPES 2N1303, 2N1305, 2N1307, 2N1309
BULLETIN NO. DL-S 1136, AUGUST 1959

High-Frequency Transistors for Computer and Switching Applications



ACTUAL SIZE

Close parameter control and the JEDEC TO-5 welded package ensure device reliability and stable characteristics

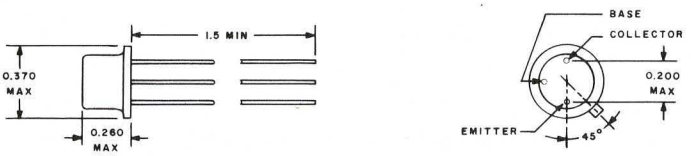
qualification testing

To ensure maximum reliability, stability, and long life, all units are aged at 100°C for 100 hours minimum prior to electrical characterization. All transistors are thoroughly tested for complete adherence to specified design characteristics. In addition, continuous qualification tests are made comprising temperature-humidity cycling, shock, and vacuum leak testing under rigid in-process control procedures.

mechanical data

Metal case with glass-to-metal hermetic seal between case and leads. Unit weight is approximately 1 gram. These units meet JEDEC outline TO-5 and E3-44 base dimensions.

THE BASE IS CONNECTED INTERNALLY TO THE CASE.



ALL DIMENSIONS IN INCHES

maximum ratings at 25°C Case Temperature (unless otherwise noted)

POLARITIES SHOWN ARE FOR P-N-P TYPES

	2N1302, 3	2N1304, 5	2N1306, 7	2N1308, 9	Units
Collector-Base Voltage*	(25) −30	(25) −30	(25) −30	(25) −30	v
Emitter-Base Voltage	−25	−25	−25	−25	v
Collector-Emitter Voltage	−25	−20	−15	−15	v
Collector Current	−300	−300	−300	−300	ma
Total Device Dissipationt	300	300	300	300	mw
Storage Temperature Range	−65 to +100				°C

* Values in parentheses apply to N-P-N devices only.
† Derate 5.0 mw/°C increase in case temperature over 25°C. The power rating in free air at 25°C is 150 mw.

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DESIGN CHARACTERISTICS

AT 25°C

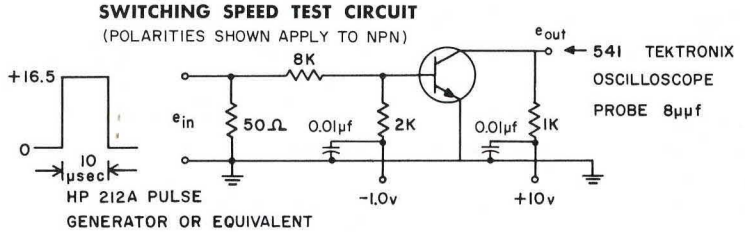
N-P-N

PARAMETER AND TEST CONDITIONS		2N1302			2N1304			2N1306			2N1308			Unit
		Min.	Design Center	Max.	Min.	Design Center	Max.	Min.	Design Center	Max.	Min.	Design Center	Max.	
V_{PT}	Punch-Through Voltage*	+25			+20			+15			+15			v
I_{CBO}	Collector Reverse Current $V_{CB}=+25v; I_E=0$		+3	+6		+3	+6		+3	+6		+3	+6	μa
I_{EBO}	Emitter Reverse Current $V_{EB}=+25v; I_C=0$		+2	+6		+2	+6		+2	+6		+2	+6	μa
I_{BX}	Total Base Reverse Current $V_{CB}=+20v; V_{EB}=+10v$		+3	+8		+3	+8		+3	+8		+3	+8	μa
h_{FE}	dc Forward Current Transfer Ratio $I_C=10ma; V_{CE}=1v$	20	50		40	70	200	60	100	300	80	150		
h_{FE}	dc Forward Current Transfer Ratio $I_C=200ma; V_{CE}=0.35v$	10			15			20			20			
V_{BE}	Base-Emitter Voltage $I_C=10ma; I_B=0.5ma$	+0.25	+0.35	+0.40	+0.20	+0.30	+0.35	+0.20	+0.26	+0.32	+0.20	+0.24	+0.30	v
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage $I_C=10ma; I_B=0.5ma$ $I_C=10ma; I_B=0.25ma$ $I_C=10ma; I_B=0.17ma$ $I_C=10ma; I_B=0.13ma$		+0.10	+0.20		+0.10	+0.20		+0.10	+0.20		+0.10	+0.15	v v v v
C_{ob}	Output Capacitance $V_{CB}=+5v; I_E=0; f=1mc$			20			20			20			20	μμf
C_{ib}	Off Input Capacitance $V_{EB}=5v; I_C=0; f=1mc$		10			10			10			10		μμf
$f_{\alpha b}$	Alpha-Cutoff Frequency $V_{CB}=+5v; I_E=1ma$	3	4.5		5	8		10	12		15	20		mc
Switching Speeds (measured in Switching Speed and Stored Base Charge test circuits shown)														
t_d	Delay Time		.12			.10			.08			.08		μsec
t_r	Rise Time		.70			.45			.22			.22		μsec
t_s	Storage Time		.50			.50			.50			.50		μsec
t_f	Fall Time		.80			.60			.50			.40		μsec
t_t	Total Switching Time		2.0			1.6			1.3			1.1		μsec
Q_s	Stored Base Charge		1000			720			660			600		μμcoul

*V_{PT} is determined by measuring the emitter floating potential V_{EBF}. The collector voltage, V_{CB}, is increased until $V_{EBF}=+1$ volt; this value $V_{CB}=V_{PT}$.

SWITCHING SPEED TEST CIRCUIT

(POLARITIES SHOWN APPLY TO NPN)



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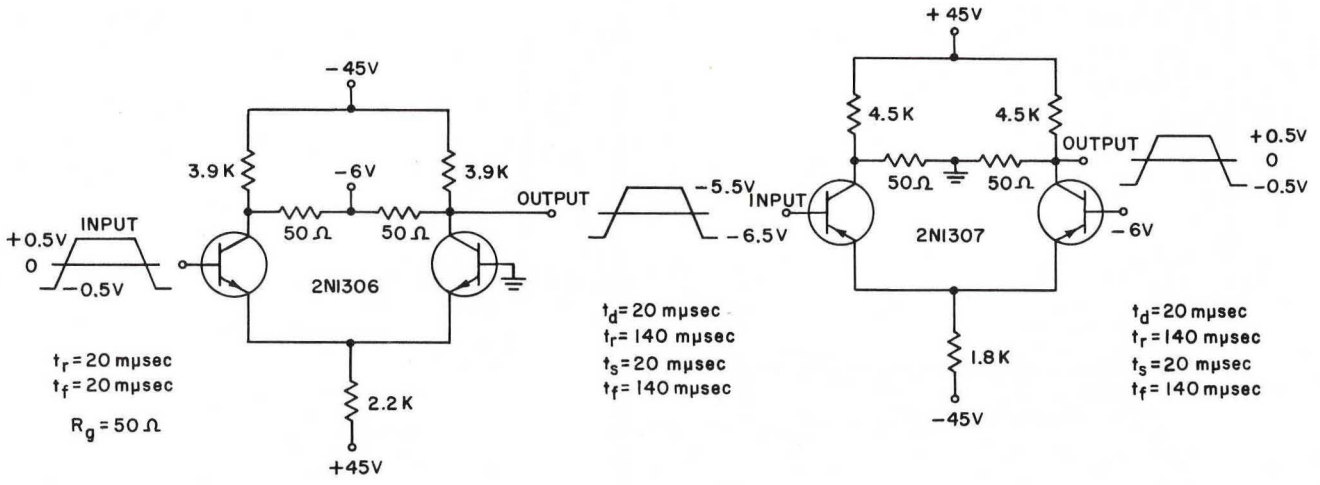
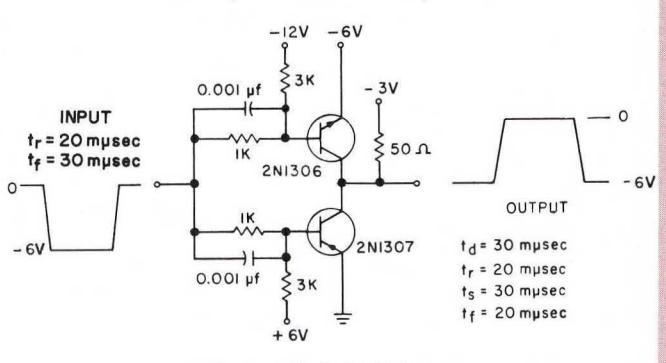
CIRCUIT APPLICATIONS

COMPLEMENTARY CURRENT MODE SWITCHES (TYPICAL NON-SATURATING SWITCH CASCADE CAPABLE OF OPERATION AT A 3mc RATE)

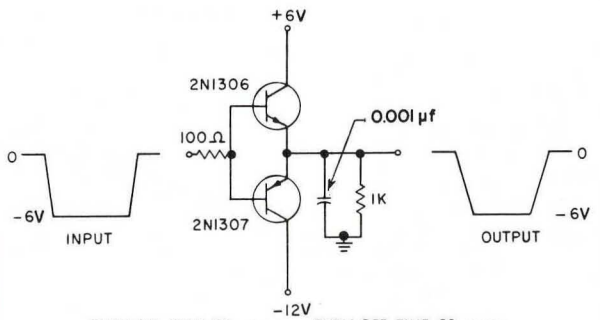


COMPLEMENTARY INVERTER (HIGH SPEED INVERTER)



TOTAL SWITCHING TIME 100 mμsec

COMPLEMENTARY EMITTER FOLLOWER (POSITIVE TRANSISTOR ACTION ON BOTH RISE AND FALL)



TURN-ON TIME 80 mμsec
$t_d + t_r$

TURN-OFF TIME 80 mμsec
$t_s + t_f$

Turn-off time without N-P-N: 2.5 μsec

DESIGN CHARACTERISTICS

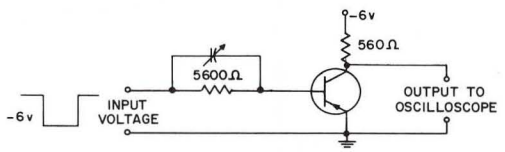
AT 25°C

P-N-P

PARAMETER AND TEST CONDITIONS		2N1303			2N1305			2N1307			2N1309			
		Min.	Design Center	Max.	Min.	Design Center	Max.	Min.	Design Center	Max.	Min.	Design Center	Max.	Unit
V_{PT}	Punch-Through Voltage*	−25			−20			−15			−15			v
I_{CBO}	Collector Reverse Current V_{CB} = −25v; I_E = 0		−3	−6		−3	−6		−3	−6		−3	−6	μa
I_{EBO}	Emitter Reverse Current V_{EB} = −25v; I_C = 0		−2	−6		−2	−6		−2	−6		−2	−6	μa
I_{BX}	Total Base Reverse Current V_{CB} = −20v; V_{EB} = −10v		−3	−8		−3	−8		−3	−8		−3	−8	μa
h_{FE}	dc Forward Current Transfer Ratio I_E = −10ma; V_{CE} = −1v	20	50		40	70	200	60	100	300	80	150		
h_{FE}	dc Forward Current Transfer Ratio I_C = −200ma; V_{CE} = −0.35v	10			15			20			20			
V_{BE}	Base-Emitter Voltage I_C = −10ma; I_B = −0.5ma	−0.25	−0.35	−0.40	−0.20	−0.30	−0.35	−0.20	−0.26	−0.32	−0.20	−0.24	−0.30	v
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage I_C = −10ma; I_B = −0.5ma		−0.10	−0.20										v
	I_C = −10ma; I_B = −0.25ma					−0.10	−0.20							v
	I_C = −10ma; I_B = −0.17ma								−0.10	−0.20				v
	I_C = −10ma; I_B = −0.13ma											−0.10	−0.15	v
C_{ob}	Output Capacitance V_{CB} = −5v; I_E = 0; f = 1mc			20			20			20			20	μμf
C_{ib}	Off Input Capacitance V_{EB} = −5v; I_C = 0; f = 1mc		7			7			7			7		μμf
$f_{\alpha b}$	Alpha-Cutoff Frequency V_{CB} = −5v; I_E = 1ma	3	4.5		5	8		10	12		15	20		mc
Switching Speeds (measured in Switching Speed and Stored Base Charge test circuits shown)														
t_d	Delay Time		.10			.08			.06			.05		μsec
t_r	Rise Time		.40			.28			.20			.15		μsec
t_s	Storage Time		.90			.80			.80			.70		μsec
t_f	Fall Time		.60			.45			.35			.25		μsec
t_t	Total Switching Time		2.0			1.6			1.3			1.1		μsec
Q_s	Stored Base Charge		1200			1000			800			700		μμcoul

*V_{PT} is determined by measuring the emitter floating potential V_{EBF}. The collector voltage, V_{CB}, is increased until V_{EBF} = −1 volt; this value $V_{CB} = V_{PT}$.

CIRCUIT FOR DETERMINING VALUE OF STORED BASE CHARGE



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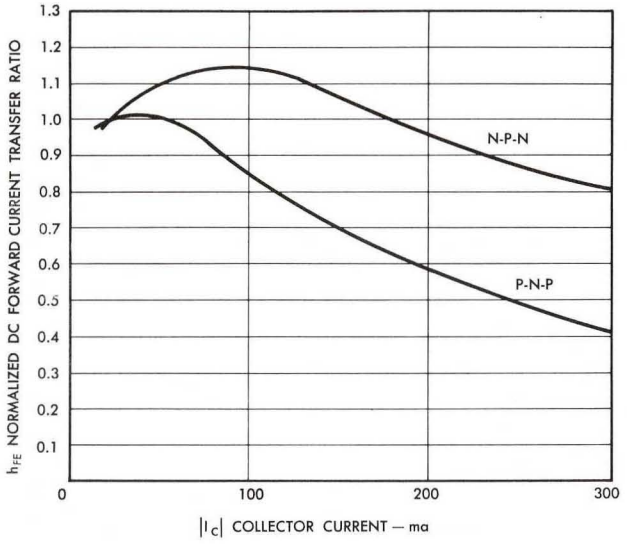
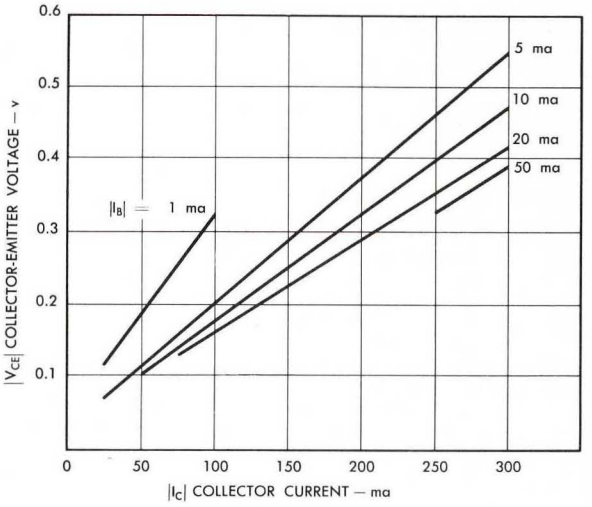
DESIGN CHARACTERISTICS

(All curves apply to both P-N-P and N-P-N except where otherwise indicated)

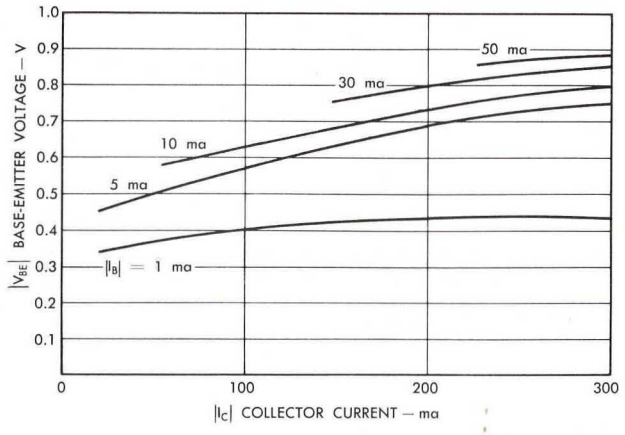
NORMALIZED DC FORWARD CURRENT TRANSFER RATIO vs. COLLECTOR CURRENT (h_{FE} NORMALIZED TO UNITY AT $I_C = 25$ ma)



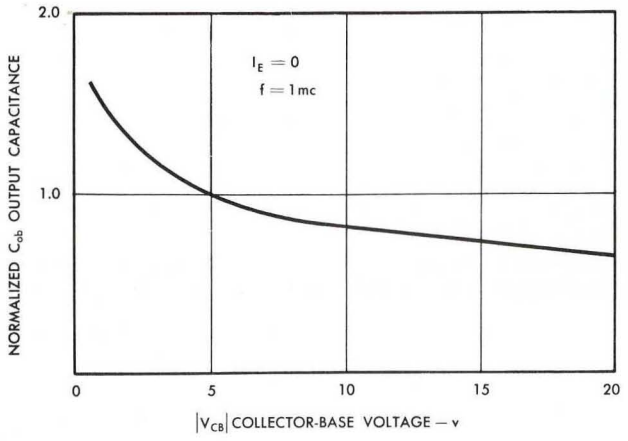
COLLECTOR-EMITTER VOLTAGE vs. COLLECTOR CURRENT (WITH BASE CURRENT AS A PARAMETER)



BASE-EMITTER VOLTAGE vs. COLLECTOR CURRENT (WITH BASE CURRENT AS A PARAMETER)



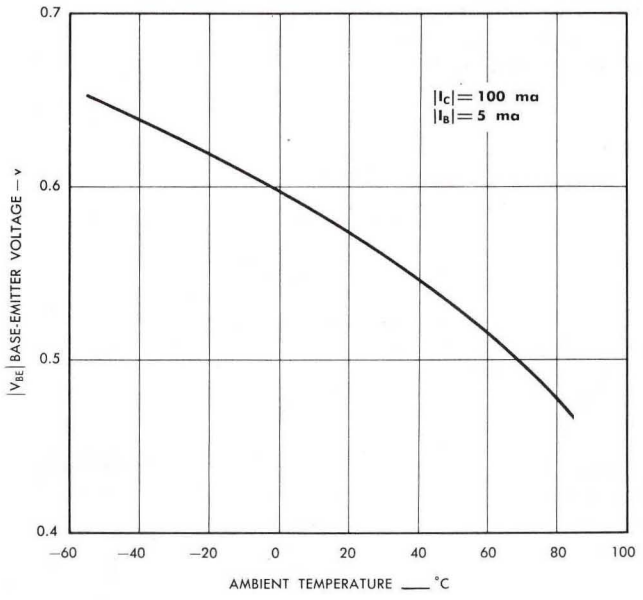
NORMALIZED OUTPUT CAPACITANCE vs. COLLECTOR-BASE VOLTAGE (C_{ob} NORMALIZED TO UNITY AT $|V_{CB}| = 5$v)



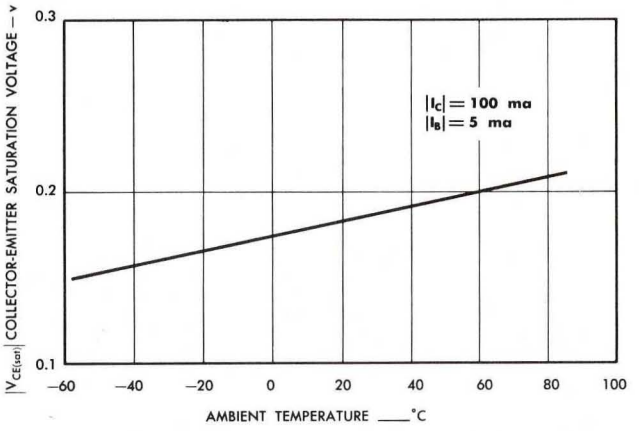
DESIGN CHARACTERISTICS

(All curves apply to both P-N-P and N-P-N except where otherwise indicated)

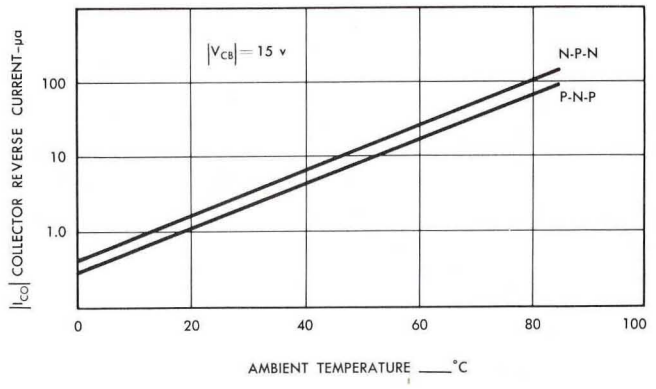
BASE-EMITTER VOLTAGE vs. AMBIENT TEMPERATURE



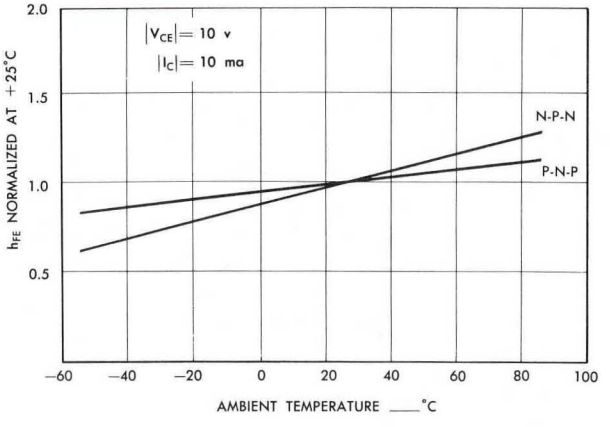
COLLECTOR-EMITTER SATURATION VOLTAGE vs. AMBIENT TEMPERATURE



COLLECTOR REVERSE CURRENT
vs.
AMBIENT TEMPERATURE



NORMALIZED DC FORWARD CURRENT TRANSFER RATIO
vs.
AMBIENT TEMPERATURE
(h_{FE} NORMALIZED TO UNITY AT 25°C)



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