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Static RAM/ Non-volatile Memory

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TOSHIBA

Static RAM
Non-Volatile Memory
1996

Standard Static RAM

High Speed Static RAM

High Speed Synchronous RAM

Non-Volatile Memory

Package: P = Plastic DIP, F = Flat package (SOP), SP = Slim Plastic DIP, FW = Flat Wide package
FT = Forward bend TSOP, TR = Reverse bend TSOP, J = SOJ

Notes

Standard SRAM

TC55257DPL/DFL/DFTL-55L/70L/85L

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 55ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3μA typically. The TC55257DPL has two control inputs. Chip Enable ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257DPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC55257DPL is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

Features

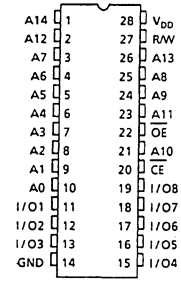
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC55257DPL/DFL/DFTL		
	-55L	-70L	-85L
Access Time	55ns	70ns	85ns
$\overline{CE}$ Access Time	55ns	70ns	85ns
$\overline{OE}$ Access Time	30ns	35ns	45ns

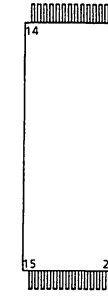
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC55257DPL : DIP28-P-600
  TC55257DFL : SOP28-P-450
  TC55257DFTL : TSOP28-P

Pin Connection (Top View)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP (forward type)



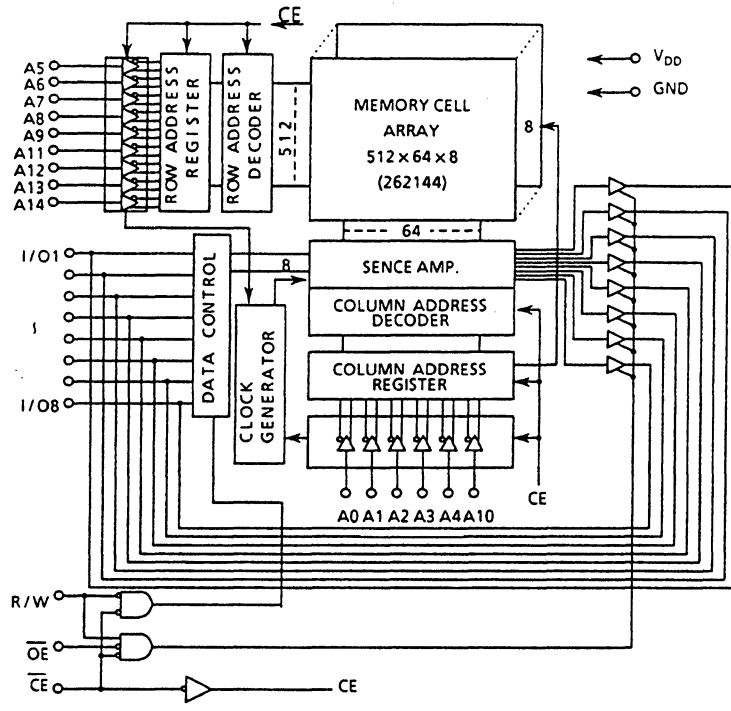
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 50ns
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1µs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1µs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	–	–	20	µA
			Ta = 25°C	–	0.3	2	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55L		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	–	70	–	85	–	ns
t_{ACC}	Address Access Time	–	55	–	70	–	85	
t_{CO}	$\overline{CE}$ Access Time	–	55	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	30	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	20	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	20	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

Write Cycle

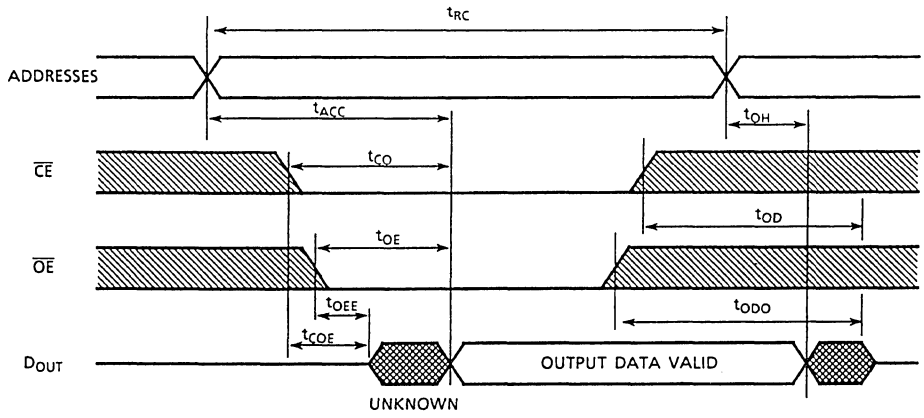
SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55L		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	–	70	–	85	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	60	–	
t_{CW}	Chip Selection to End of Write	50	–	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	20	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t_{DS}	Data Setup Time	25	–	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC Test Conditions

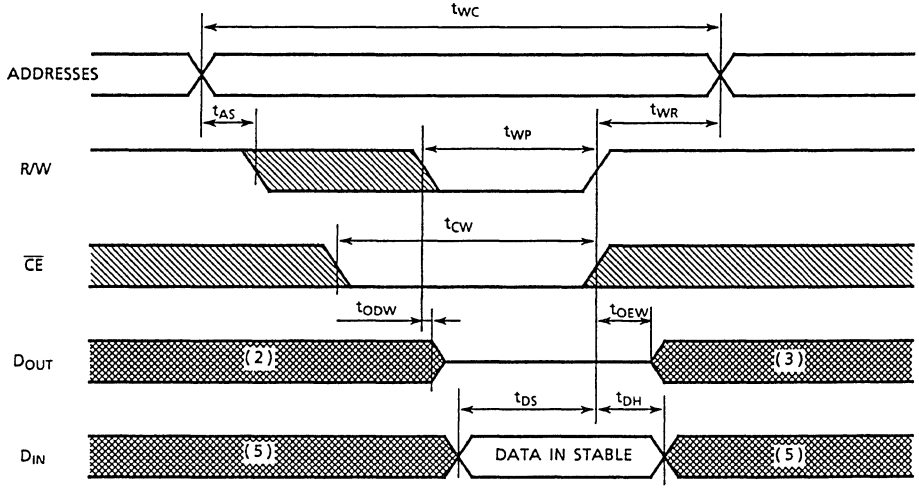
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 30pF (-55L) 1 TTL Gate and C_L = 100pF (-70L, -85L)

Timing Waveforms

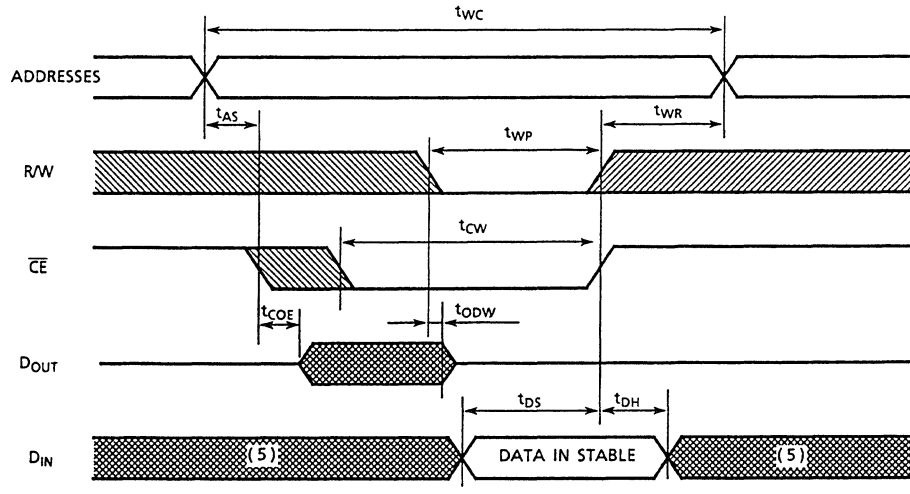
Read Cycle [1]



Write Cycle 1 [4] (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is High for read cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a write cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; input signals of opposite phase must not be applied.

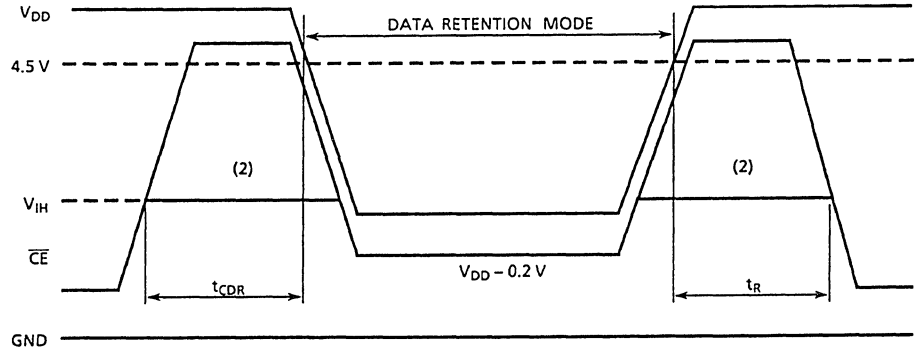
Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	10*	µA
		V_{DH} = 5.5V	–	–	20	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

*: 2µA (Max.) Ta = 0 ~ 40°C

Note (1): Read Cycle Time

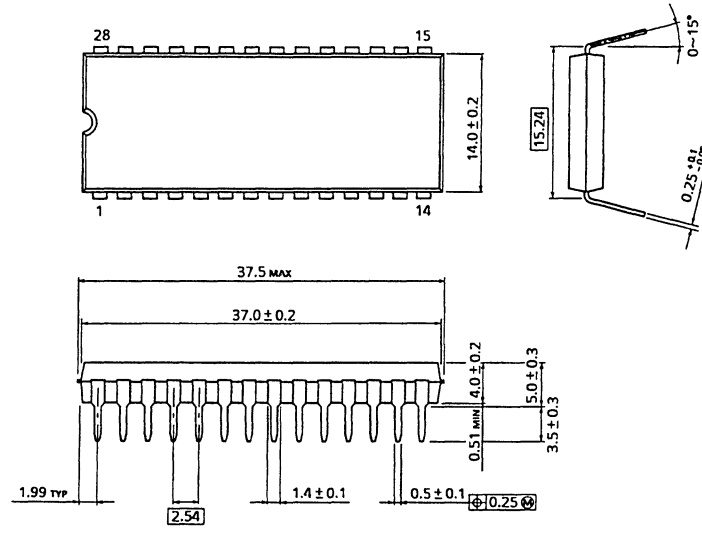
$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

Outline Drawing

DIP28-P-600 Unit in mm

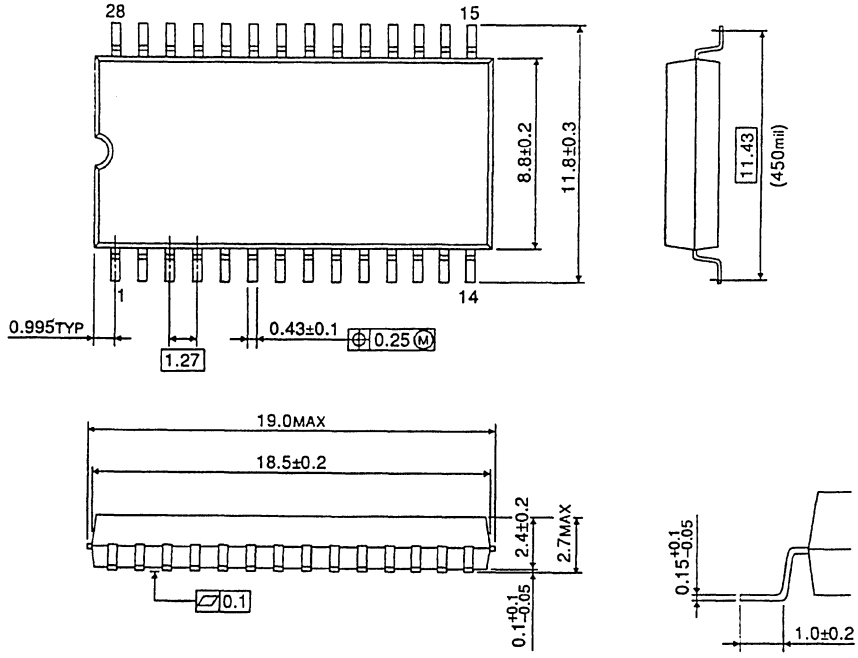


Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450

Unit in mm

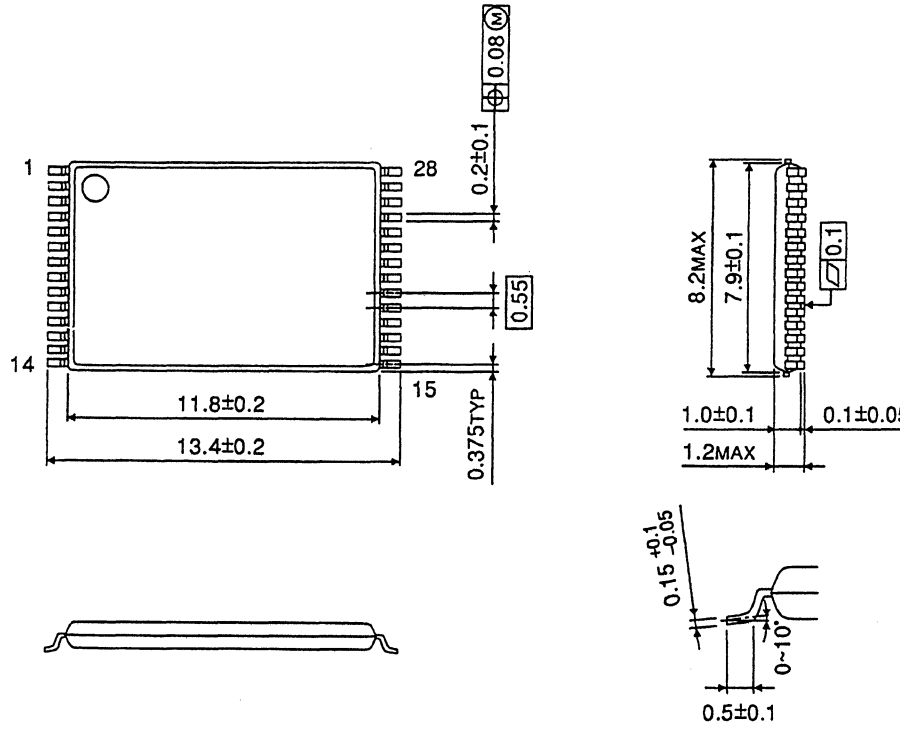


Weight : 0.79g (Typ.)

Outline Drawing

TSOP29-P

Unit in mm



Weight : 0.22g (Typ.)

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SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPI is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3μA typically. The TC55257DPI has two control inputs. Chip Enable ($\overline{CE}$) allows for device selection and data retention control, and an Output Enable input ($\overline{OE}$) provides fast memory access. The TC55257DPI is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC55257DPI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC55257DPI is suitable for use in wide operating temperature systems.

The TC55257DPI is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

Features

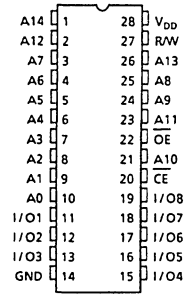
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC55257DPI/DFI/DFTI	
	-70L	-85L
Access Time	70ns	85ns
$\overline{CE}$ Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

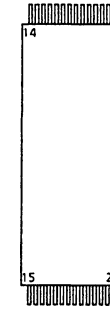
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package TC55257DPI : DIP28-P-600
  TC55257DFI : SOP28-P-450
  TC55257DFTI : TSOP28-P

Pin Connection (Top View)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP (forward type)

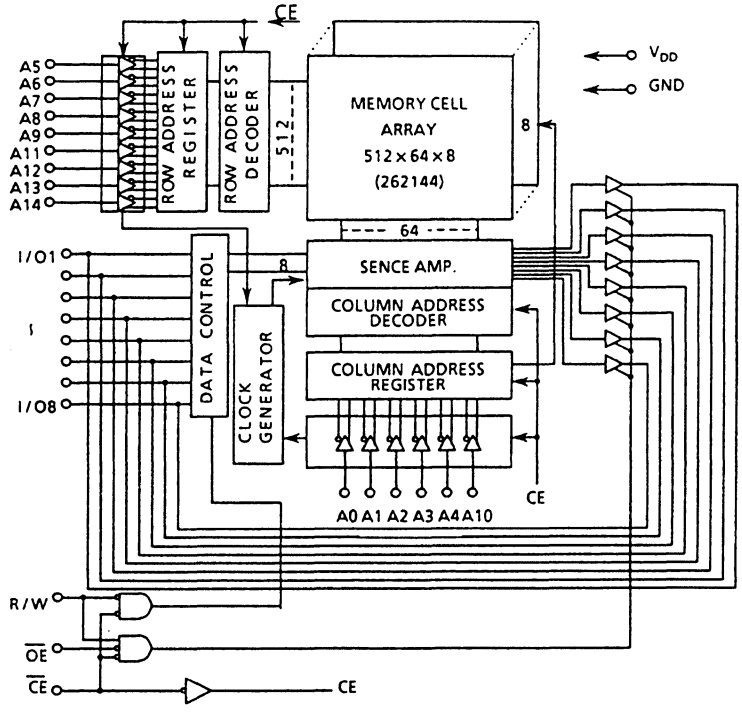


Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 50ns
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1µs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1µs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	30	µA
			Ta = 25°C	–	0.3	2	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO}	$\overline{CE}$ Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

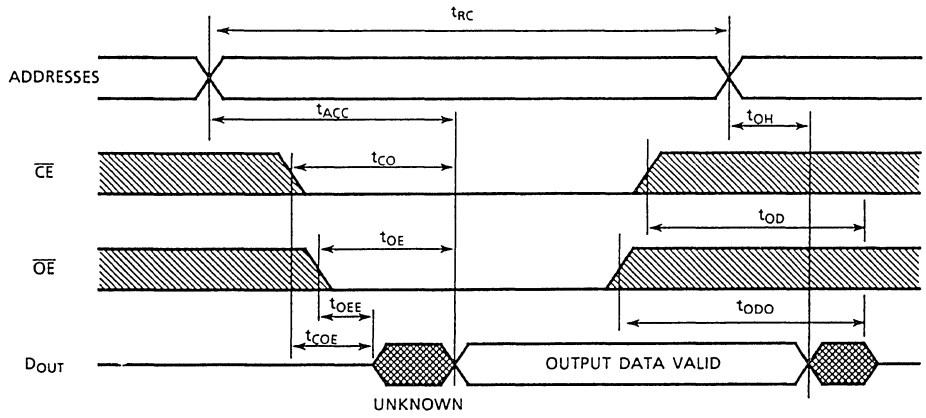
SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

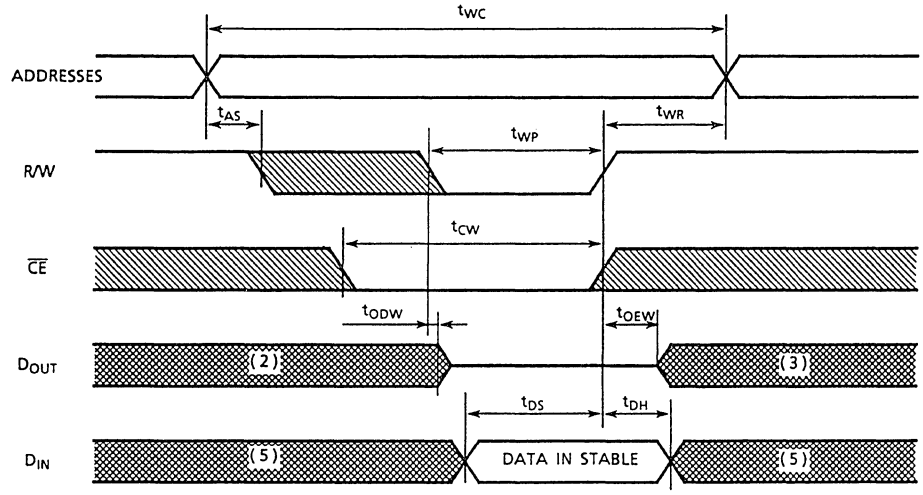
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

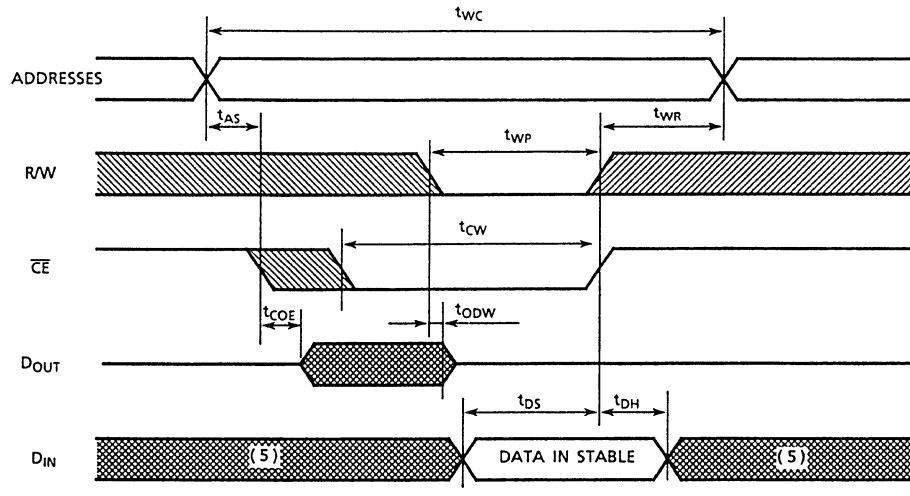
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is High for read cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W high transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a write cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; input signals of opposite phase must not be applied.

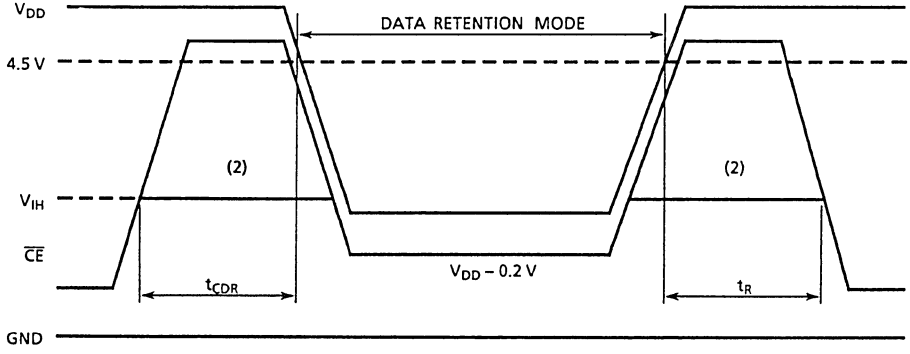
Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	15*	µA
		V_{DH} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time

*2µA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode

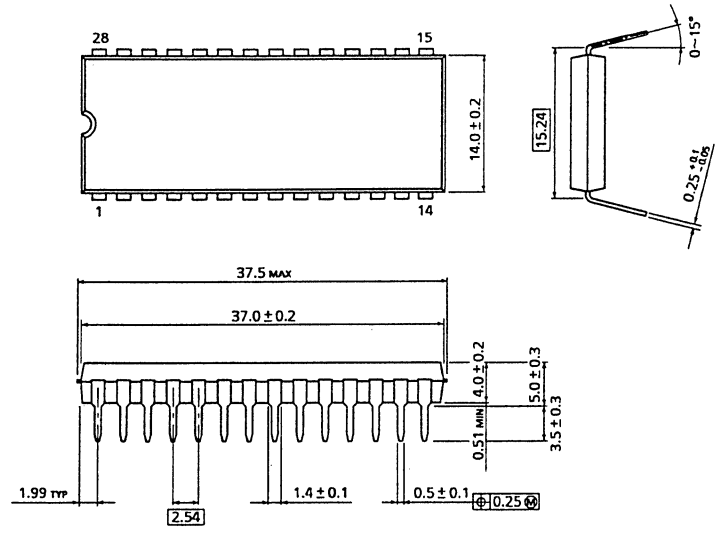


Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

Outline Drawing

DIP28-P-600

Unit in mm

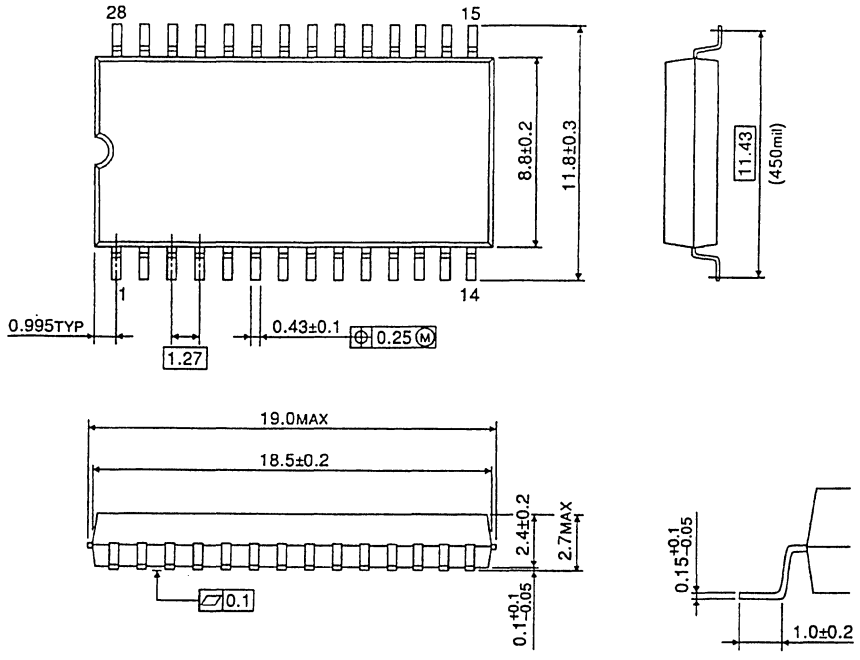


Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450

Unit in mm

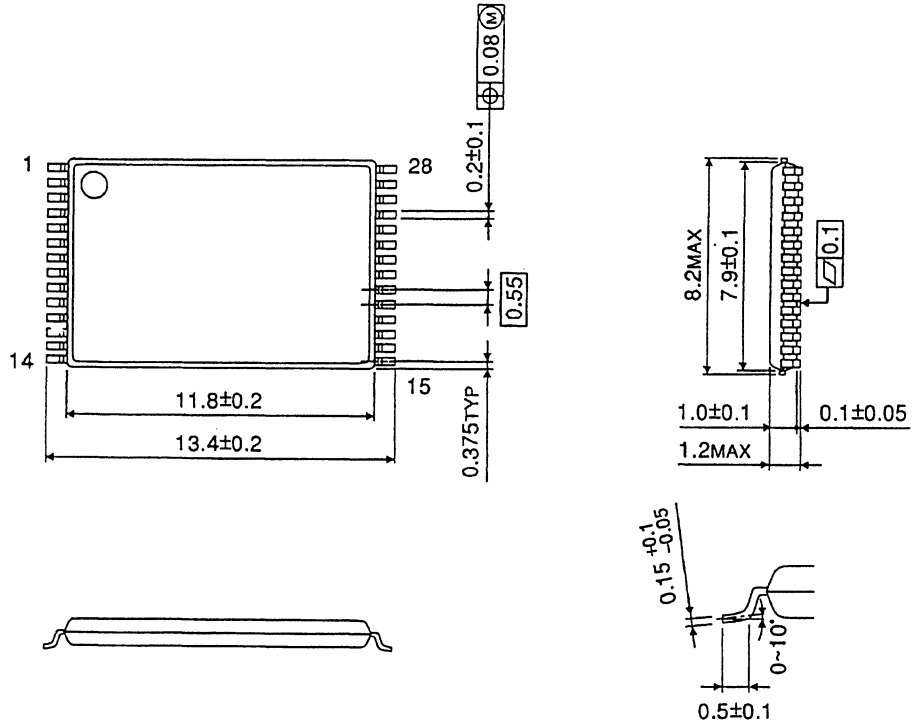


Weight : 0.79g (Typ.)

Outline Drawing

TSOP28-P

Unit in mm



Weight : 0.22g (Typ.)

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TC55257DPI/DFI/DFTI-70V/85V

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPI is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 2.7 ~ 5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3μA typically. The TC55257DPI has two control inputs. Chip Enable ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC55257DPI is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC55257DPI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC55257DPI is suitable for use in wide operating temperature systems.

The TC55257DPI is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

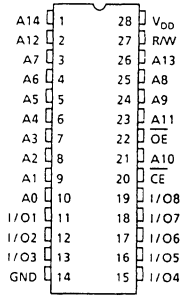
Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- Single 2.7 ~ 5.5V power supply
- Access time (max.)

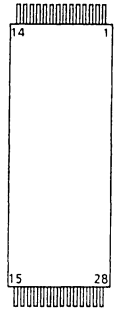
	5V±10%		2.7 ~ 5.5V	
	-70V	-85V	-70V	-85V
Access Time	70ns	85ns	120ns	150ns
$\overline{CE}$ Access Time	70ns	85ns	120ns	150ns
$\overline{OE}$ Access Time	35ns	45ns	70ns	75ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package TC55257DPI : DIP28-P-600
  TC55257DFI : SOP28-P-450
  TC55257DFTI : TSOP28-P

o 28 PIN DIP & SOP



o 28 PIN TSOP (forward type)



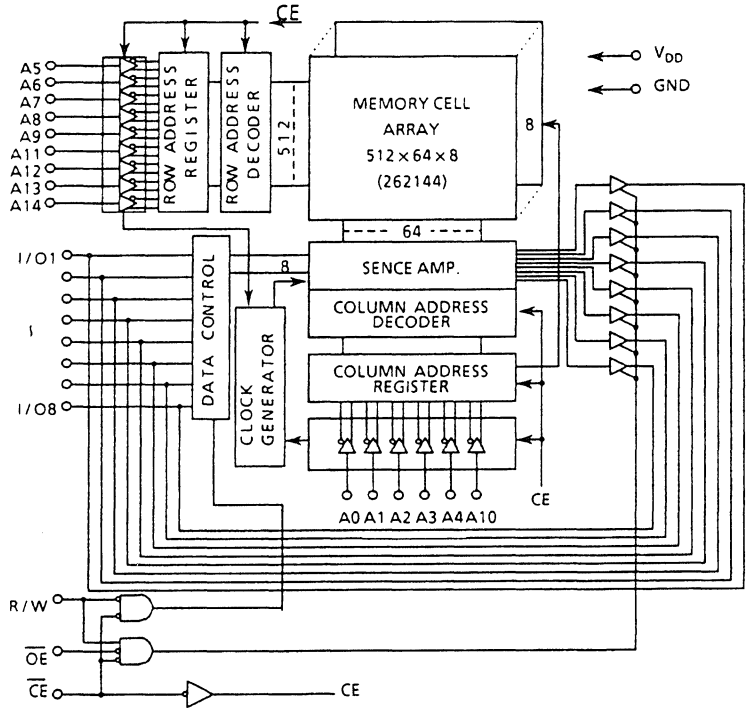
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 50ns
** SOP

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	5V ±10%			2.2 ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	MIN.	MAX.	
V_{DD}	Power Supply Voltage	4.5	–	5.5	2.7	–	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V at pulse width at 50ns Max.

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1µs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V, R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1µs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	30	µA
			Ta = 25°C	–	0.3	2	

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 3V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = V_{DD} - 2.0V			-0.1	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V			0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V, R/W = V_{DD} = 2.0V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle}	Min.	–	–	20	mA
				1µs	–	–	5	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 3V ± 10%	Ta = -40 ~ 85°C	–	–	20	µA
				Ta = 25°C	–	1	1.5	
			V_{DD} = 3.0V	Ta = -40 ~ 40°C	–	–	2	
				Ta = 25°C	–	–	1	
				Ta = -40 ~ 85°C	–	–	15	

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO}	$\overline{CE}$ Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 30pF (-55V) 1 TTL Gate and C_L = 100pF (-70V, -85V)

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 2.7 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	120	–	150	–	ns
t_{ACC}	Address Access Time	–	120	–	150	
t_{CO}	$\overline{CE}$ Access Time	–	120	–	150	
t_{OE}	Output Enable to Output in Valid	–	70	–	75	
t_{COE}	Chip Enable to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable to Output in High-Z	–	50	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	50	–	50	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

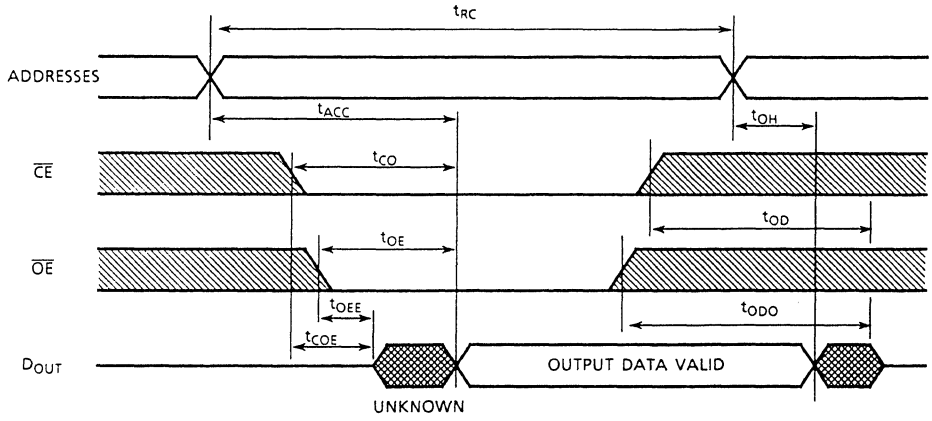
SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	120	–	150	–	ns
t_{WP}	Write Pulse Width	80	–	100	–	
t_{CW}	Chip Selection to End of Write	100	–	120	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	50	–	50	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	50	–	60	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

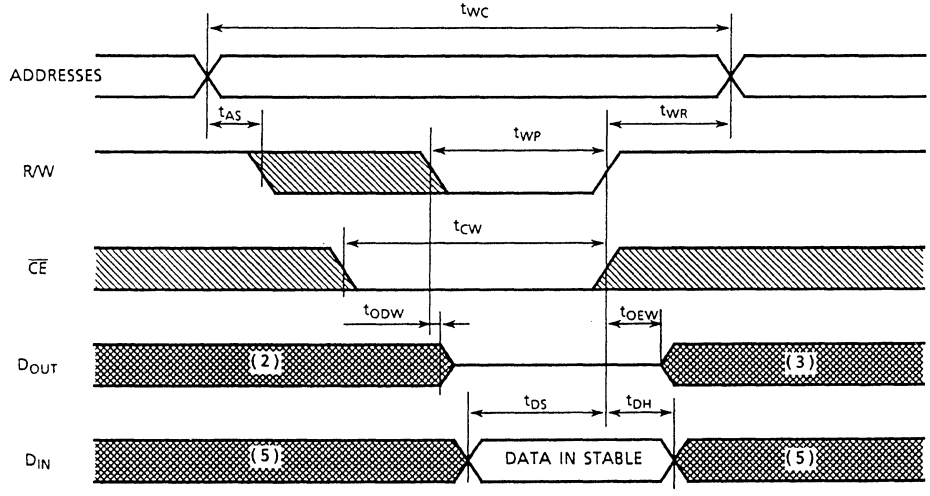
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	C_L = 100pF (Include Jig)

Timing Waveforms

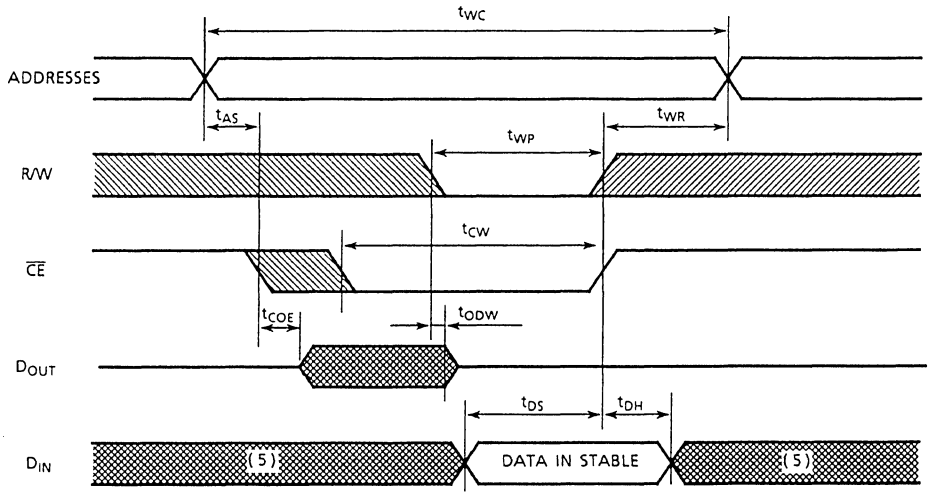
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is High for read cycle.
2. Assuming that the $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

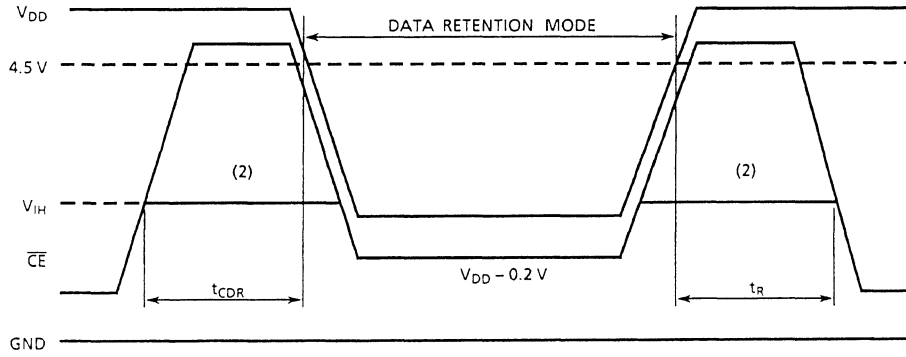
Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	15*	µA
		V_{DH} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time

* 2µA (max.) Ta = -40 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode

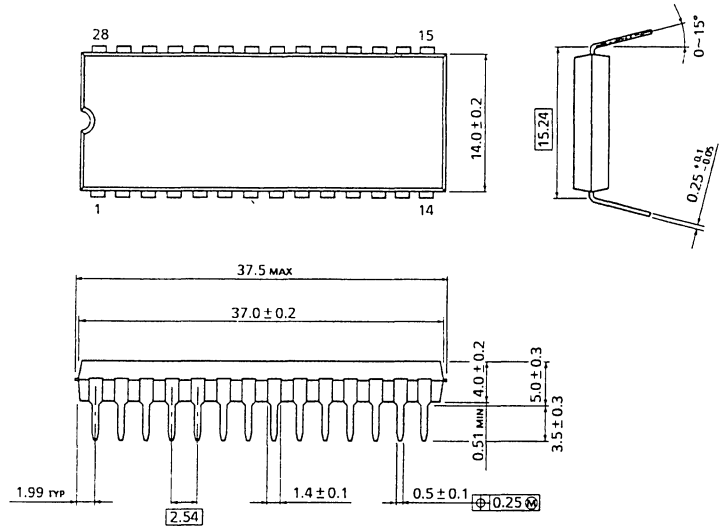


Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

Outline Drawing

DIP28-P-600

Unit in mm

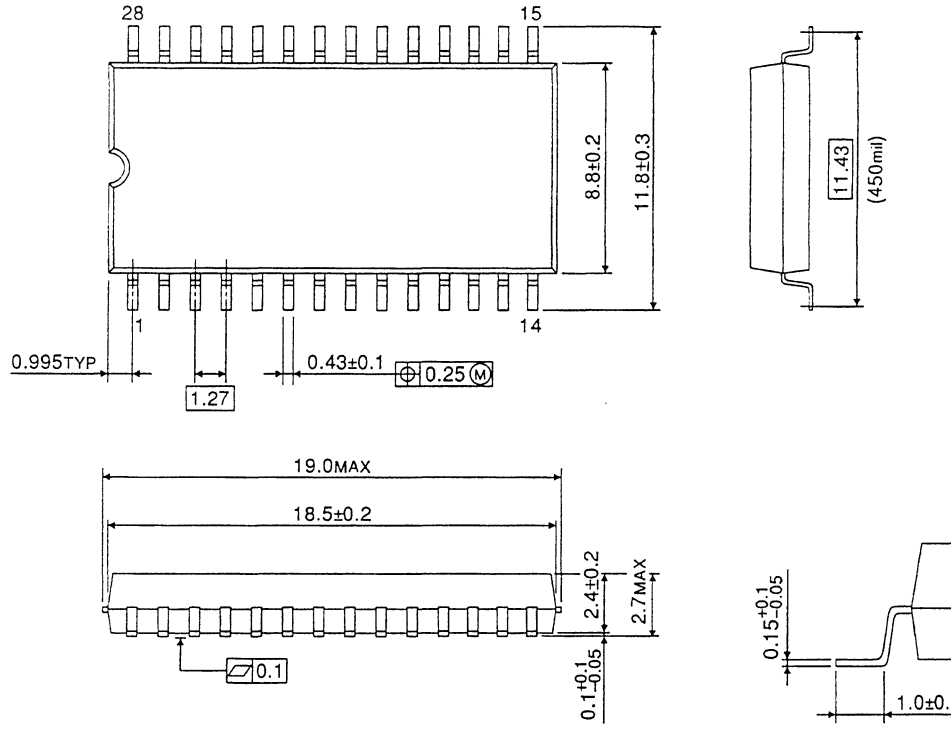


Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450

Unit in mm

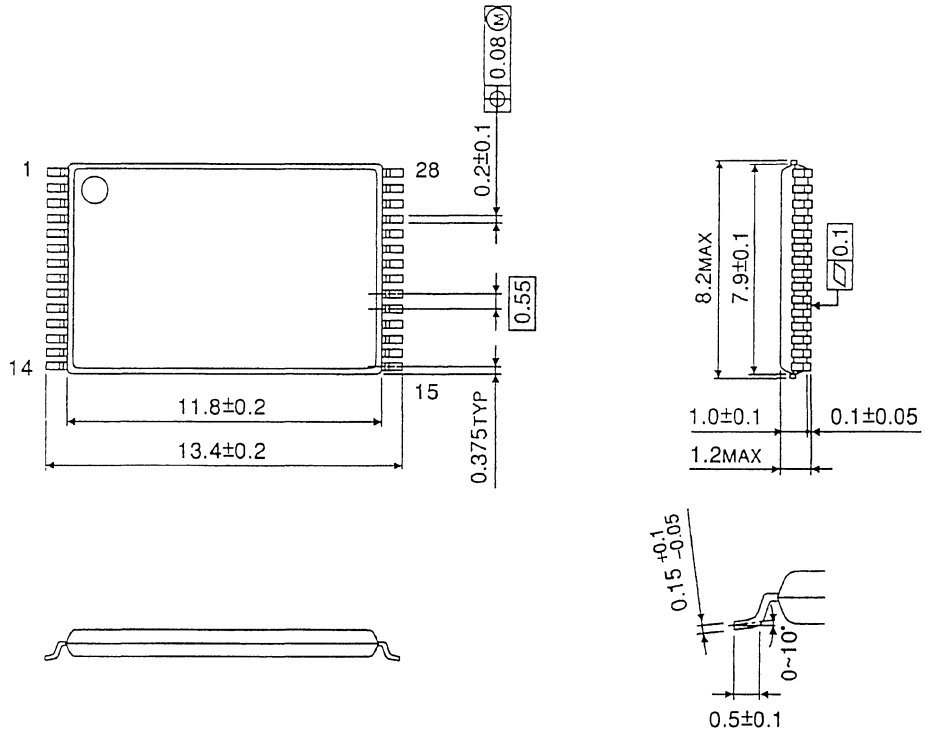


Weight : 0.79g (Typ.)

Outline Drawing

TSOP29-P

Unit in mm



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TC55257DPL/DFL/DFTL-55V/70V/85V

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 2.7 ~ 5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 55ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3μA at room temperature. The TC55257DPL has two control inputs. Chip Enable ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC55257DPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC55257DPL is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

Features

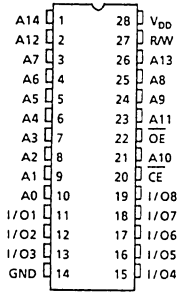
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- Single 2.7 ~ 5.5V power supply
- Access time (max.)

	5V ± 10%			2.7 ~ 5.5V
	-55V	-70V	-85V	-55V/70V/85V
Access Time	70ns	85ns	100ns	150ns
$\overline{CE}$ Access Time	70ns	85ns	100ns	150ns
$\overline{OE}$ Access Time	35ns	45ns	50ns	75ns

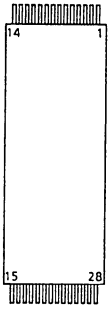
- Power down feature: $\overline{CE}$
- Data retention supply voltage:2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC55257DPL: DIP28-P-600
  TC55257DFL : SOP28-P-450
  TC55257DFTL : TSOP28-P

Pin Connection (Top View)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP (forward type)



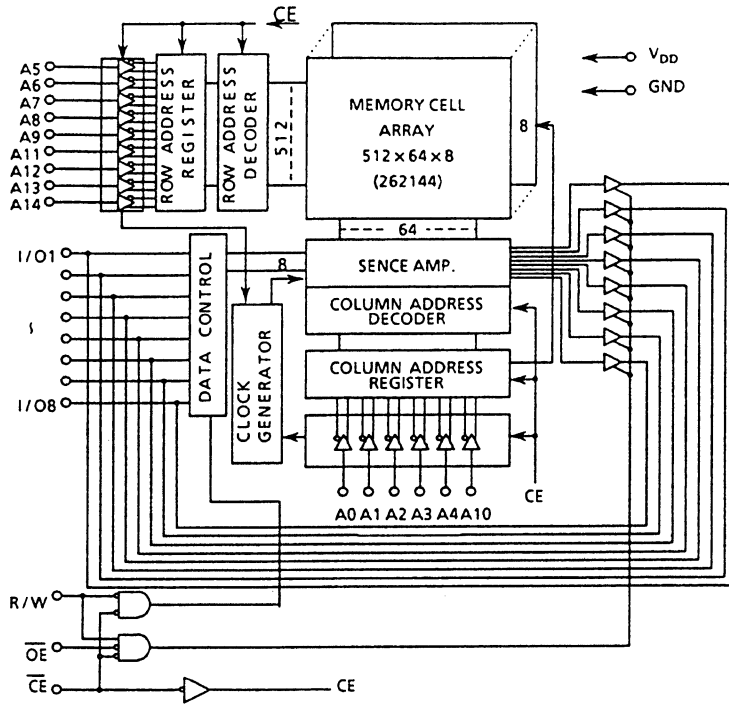
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power
GND	Ground

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 50ns
** SOP

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	5V ±10%			2.2 ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	MIN.	MAX.	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	–	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V at pulse width at 50ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1μs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1μs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V, V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	20	μA
			Ta = 25°C	–	0.3	2	

DC and Operating Characteristics (Ta = -0 ~ 70°C, V_{DD} = 3V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} - 2.0V			-0.1	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V			0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V R/W = V_{DD} = 2.0V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle}	Min.	–	–	20	mA
				1μs	–	–	5	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V or CE2 = 0.2V	V_{DD} = 3V ± 10%	Ta = -0 ~ 70°C	–	–	15	μA
				Ta = 25°C	–	1	1.5	
			V_{DD} = 3.0V	Ta = 0 ~ 70°C	–	–	10	
				Ta = 0 ~ 40°C	–	–	2	
				Ta = 25°C	–	–	1	

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55V		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	–	70	–	85	–	ns
t_{ACC}	Address Access Time	–	55	–	70	–	85	
t_{CO}	CE Access Time	–	55	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	30	–	35	–	45	
t_{COE}	Chip Enable to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable to Output in High-Z	–	20	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	20	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55V		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	–	70	–	85	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	60	–	
t_{CW}	Chip Selection to End of Write	50	–	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	20	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t_{DS}	Data Setup Time	25	–	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 30pF (-55V) 1 TTL Gate and C_L = 100pF (-70V, -85V)

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 2.7 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO}	CE Access Time	–	150	
t_{OE}	Output Enable to Output in Valid	–	75	
t_{COE}	Chip Enable CE to Output in Low-Z	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	
t_{OD}	Chip Enable CE to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	50	
t_{OH}	Output Data Hold Time	10	–	

Write Cycle

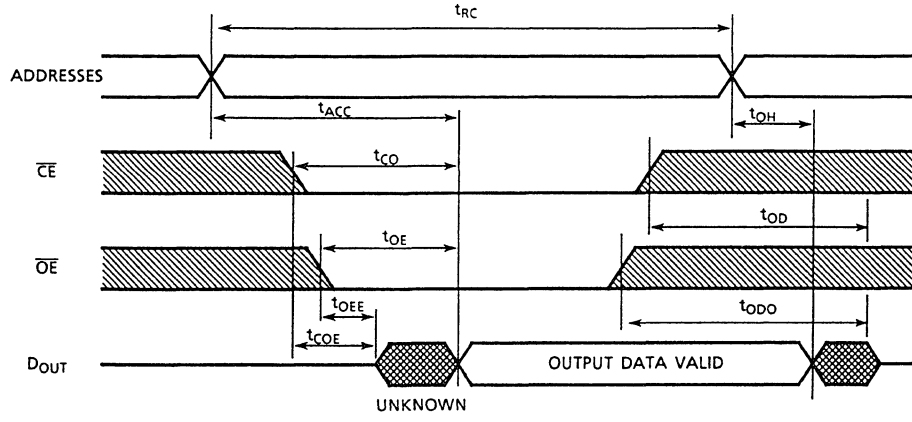
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Selection to End of Write	120	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{ODW}	R/W to Output in High-Z	–	50	
t_{OEW}	R/W to Output in Low-Z	5	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	

AC Test Conditions

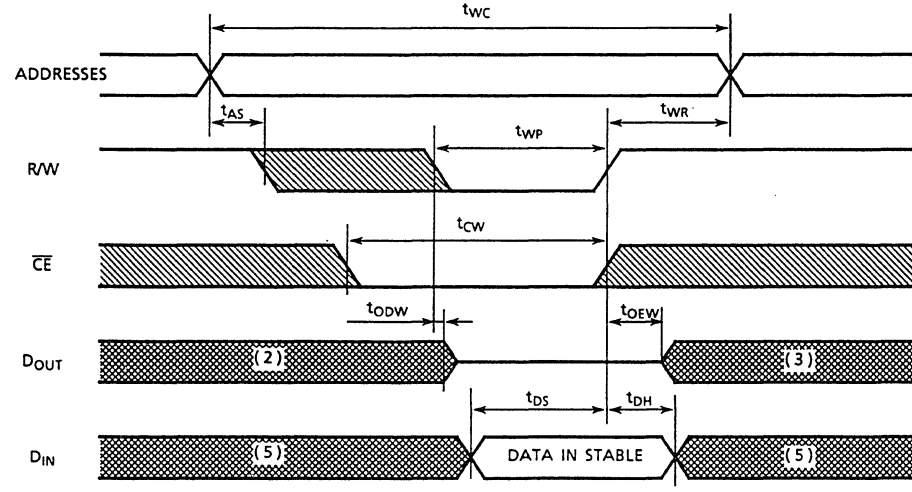
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	C_L = 100pF (Include Jig)

Timing Waveforms

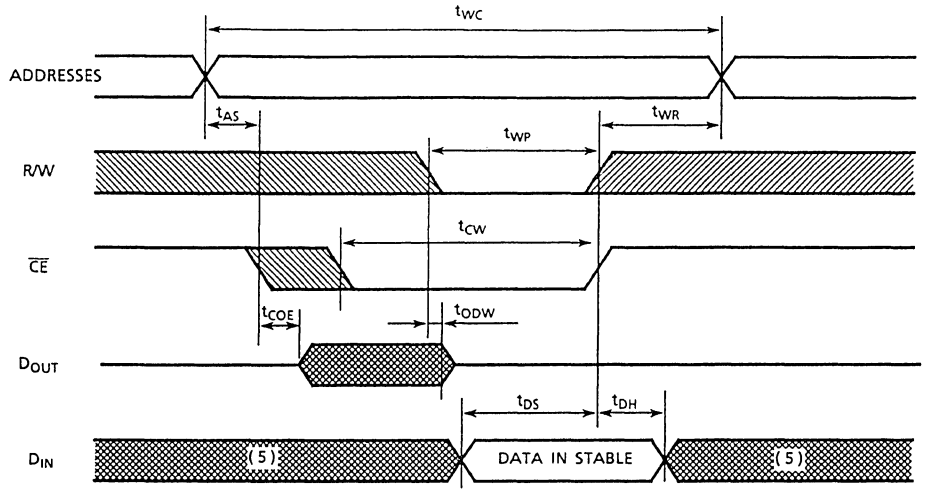
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is High for read cycle.
2. Assuming that $\overline{CE}$ low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a Write Cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; input signals of opposite phase must not be applied.

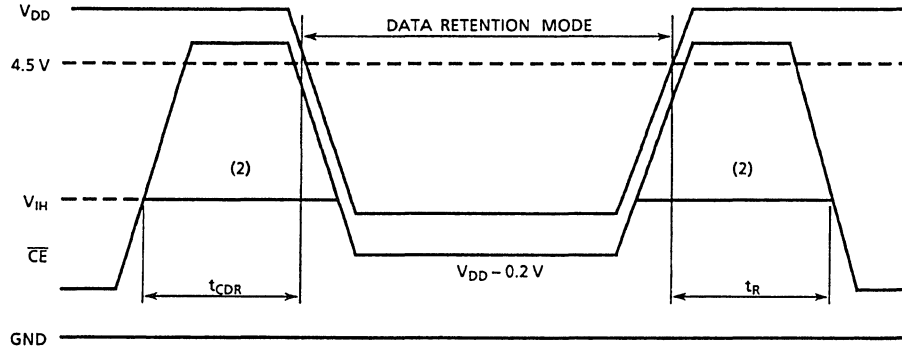
Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	10*	µA
		V_{DH} = 5.5V	–	–	20	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time

*2µA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode

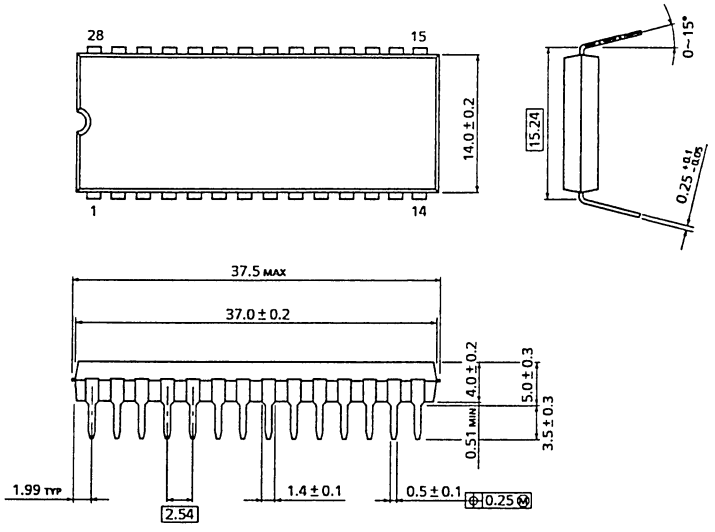


Note (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

Outline Drawing

DIP28-P-600

Unit in mm

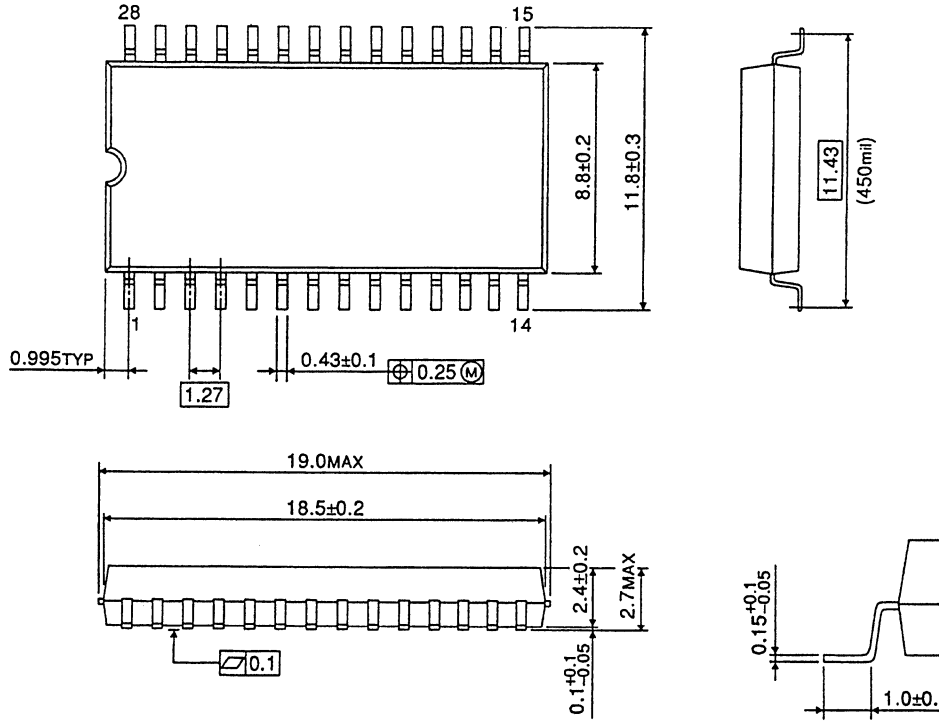


Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450

Unit in mm

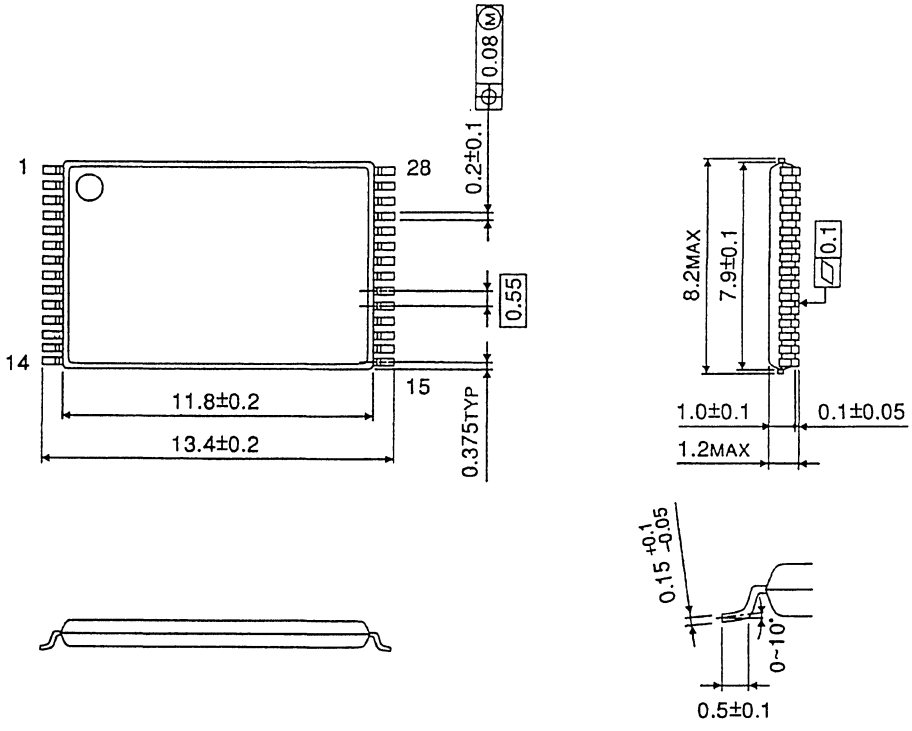


Weight : 0.79g (Typ.)

Outline Drawing

TSOP29-P

Unit in mm



Weight : 0.22g (Typ.)

Notes

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SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bit static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

Features

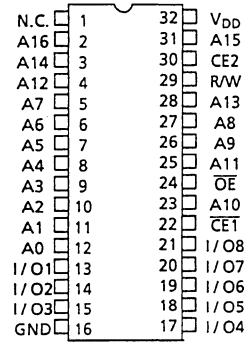
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100μA (max.)
- 5V single power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL	
	-70	-85
Access Time	70ns	85ns
$\overline{CE1}$ Access Time	70ns	85ns
CE2 Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC551001BPL : DIP32-P-600
  TC551001BFL : SOP32-P-525
  TC551001BFTL : TSOP32-P-0820
  TC551001BTRL : TSOP32-P-0820A

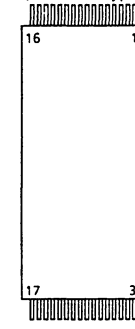
Pin Connection (Top View)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP

(forward type)



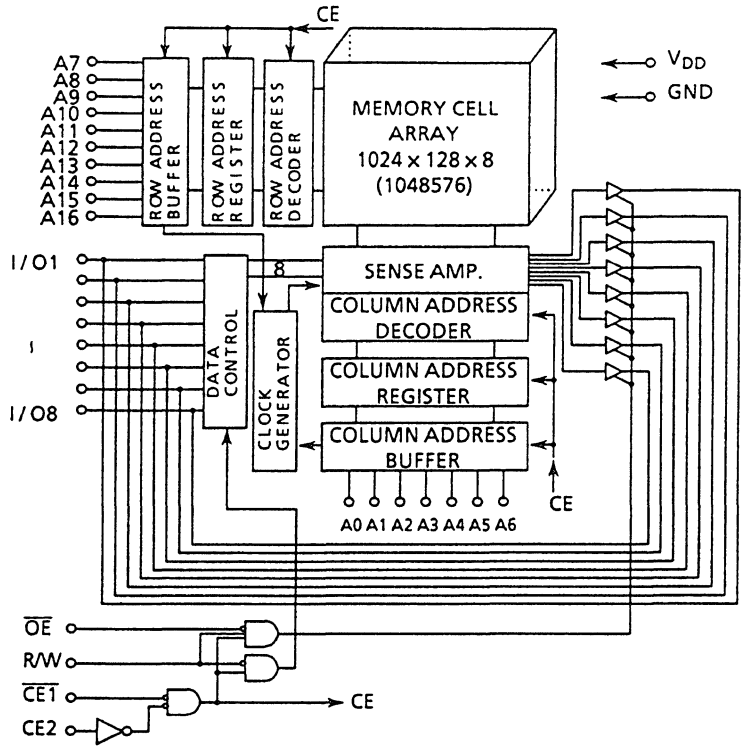
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 50ns Max.
** SOP

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 50ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
				1µs	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} - 0.2V I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	Min.	–	–	60	
				1µs	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			–	–	3	mA
I_{DDS2}(1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V, Ta = 0 ~ 70°C			–	2	100	µA

Note (1): In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, these specification limits are guaranteed under the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70		-85		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	
t_{CO2}	CE2 Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

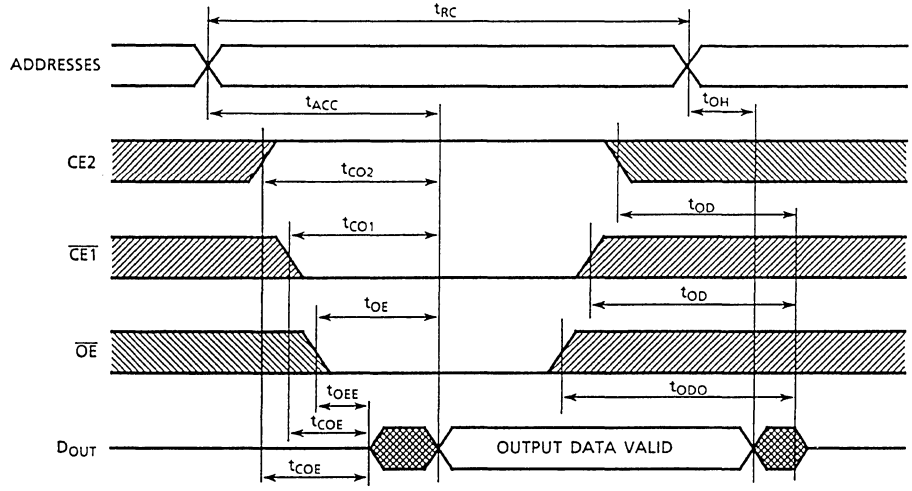
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70		-85		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

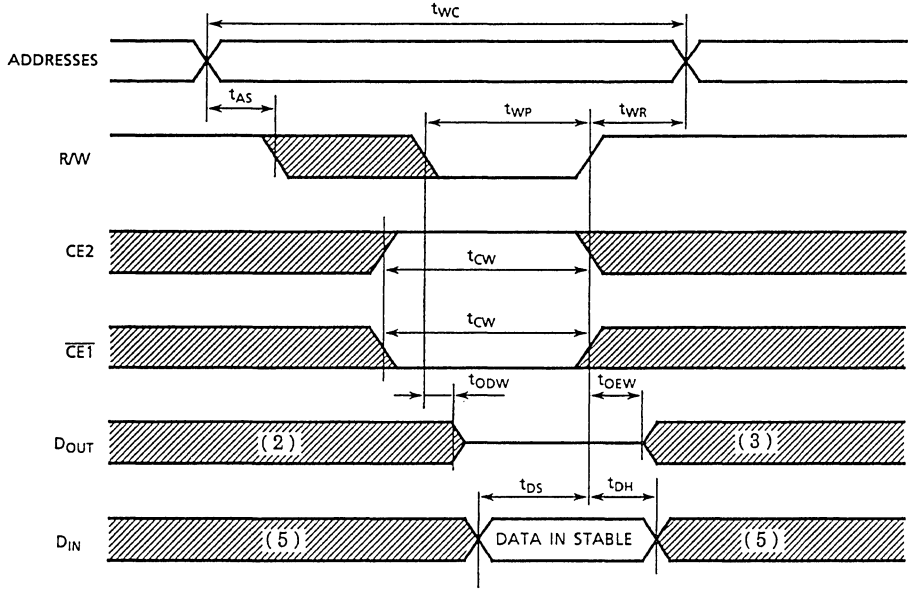
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

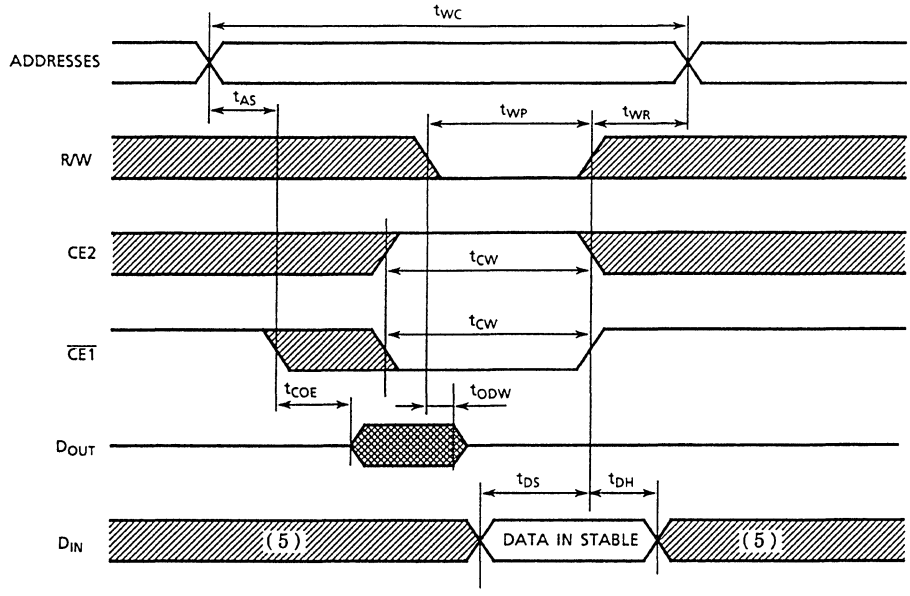
Read Cycle [1]



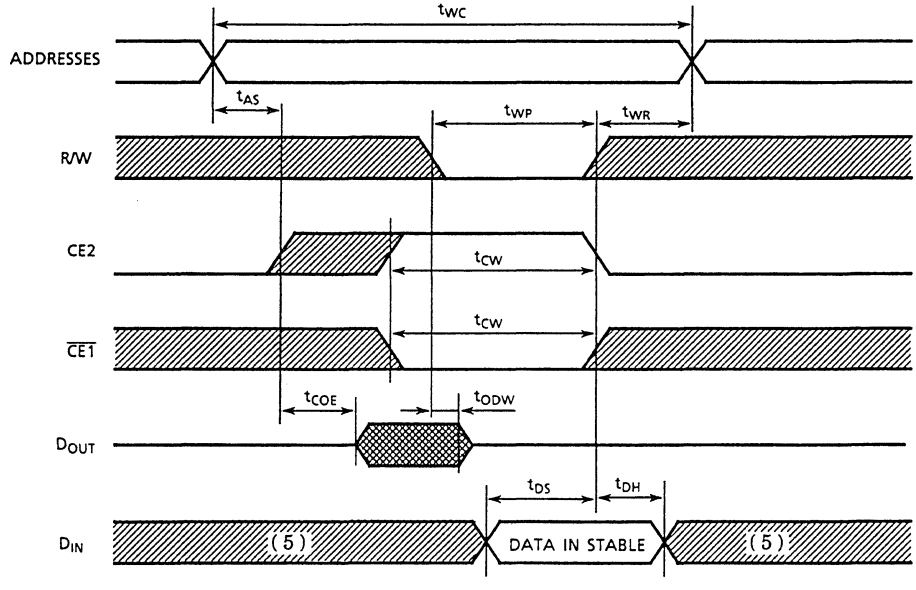
Write Cycle 1 [4] (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

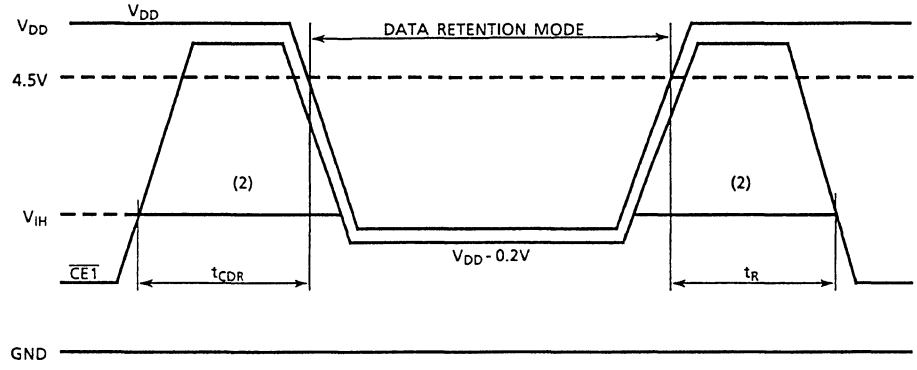
4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.

5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

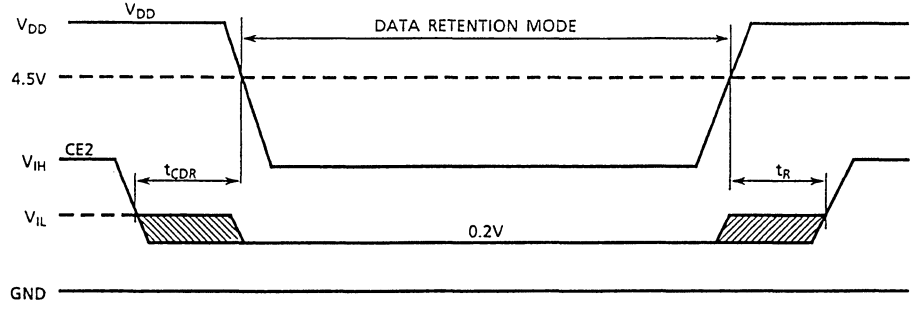
Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	50	µA
		V_{DD} = 5.5V	–	–	100	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

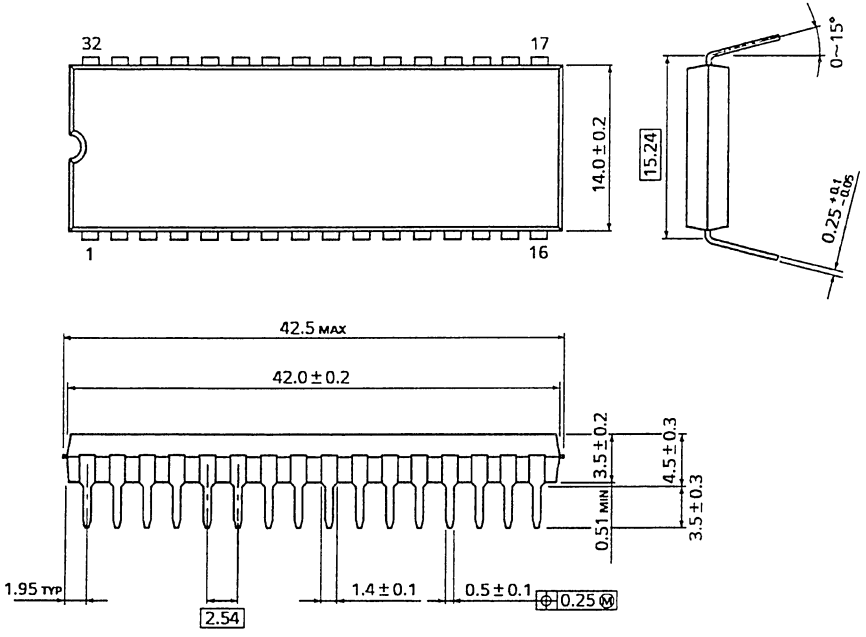
1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

2. If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V.

Outline Drawing

DIP32-P-600 Unit in mm

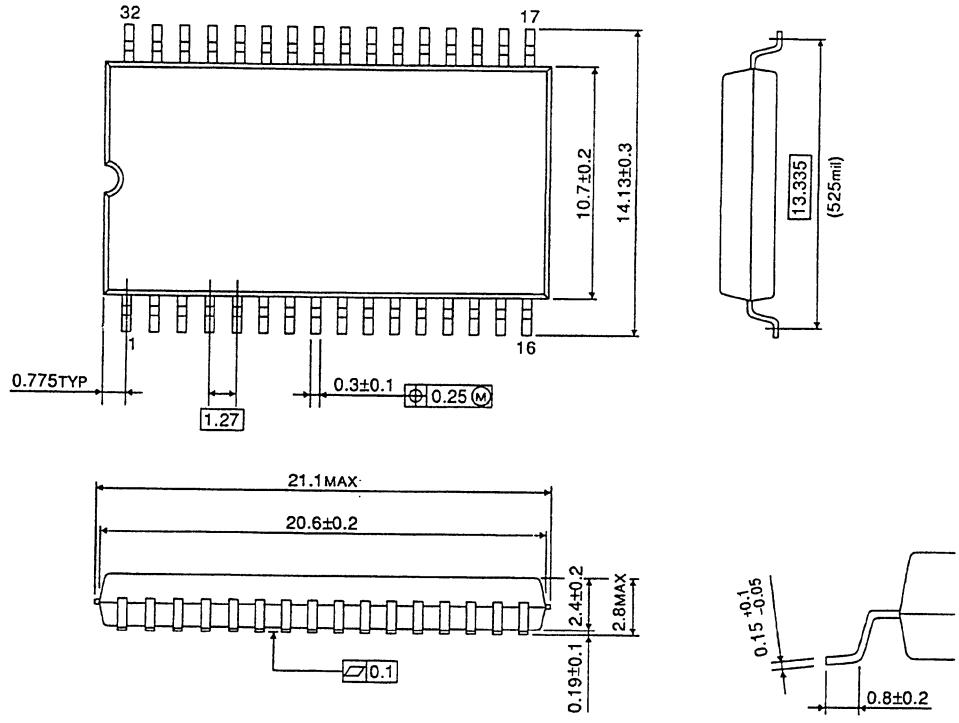


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

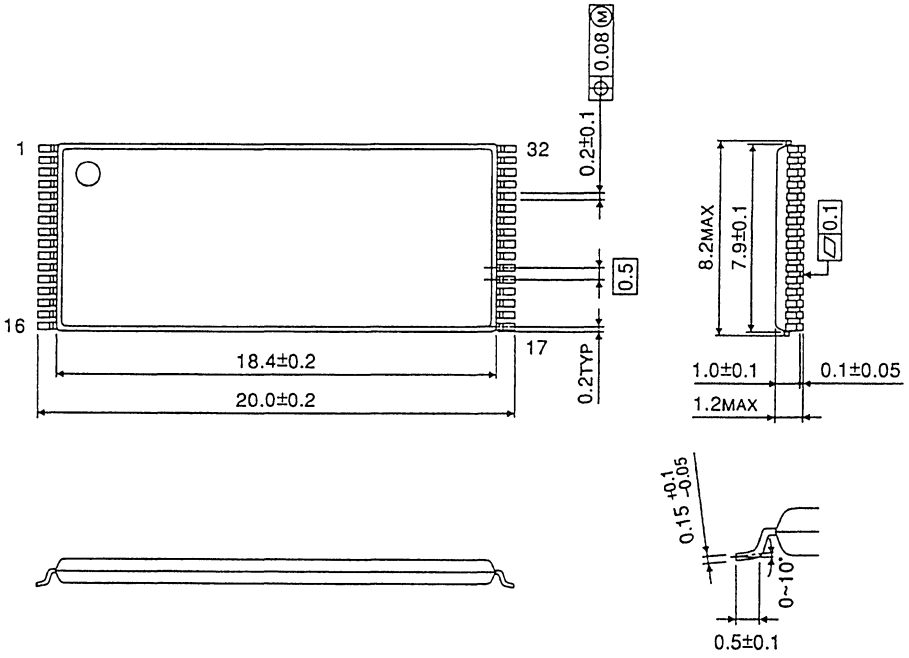


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

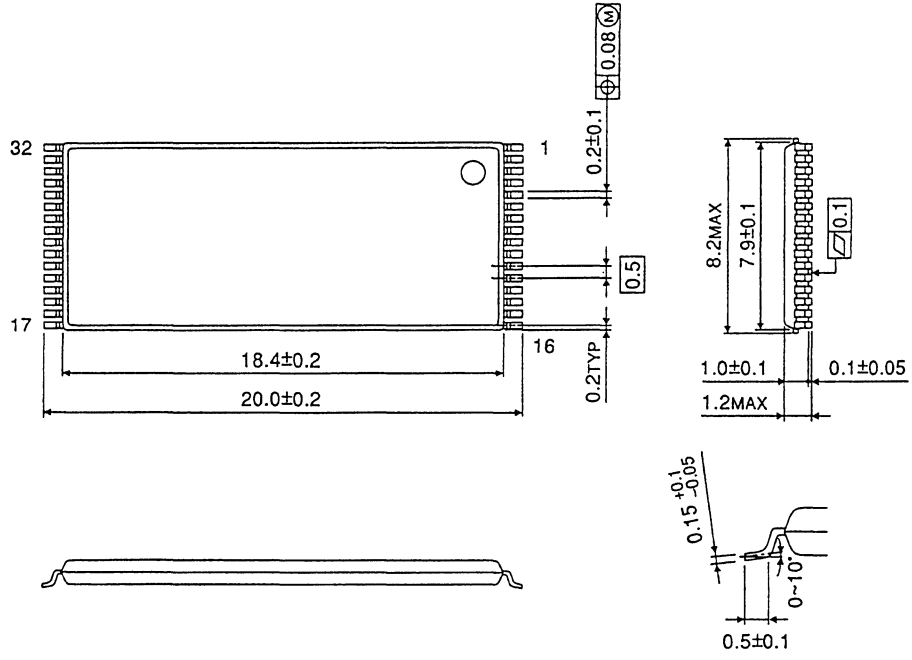


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

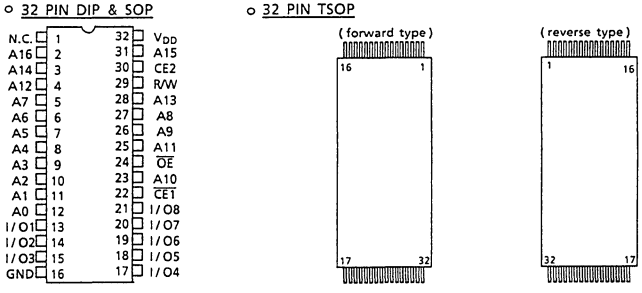
Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC551001BPL/BFL/BFTL/BTRL	
	-70L	-85L
Access Time	70ns	85ns
$\overline{CE1}$ Access Time	70ns	85ns
CE2 Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC551001BPL : DIP32-P-600
  TC551001BFL : SOP32-P-525
  TC551001BFTL : TSOP32-P-0820
  TC551001BTRL : TSOP32-P-0820A

Pin Connection (Top View)



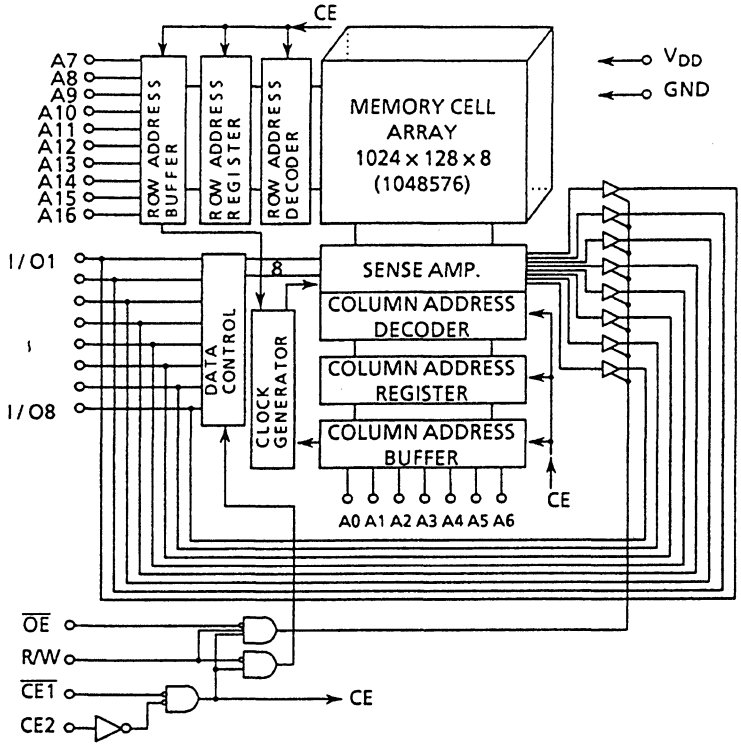
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width of 50ns Max
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width of 50ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
				1μs	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} - 0.2V I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	Min.	–	–	60	
				1μs	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			–	–	3	mA
I_{DDS2}(1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C		–	–	30	μA
			Ta = 25°C		–	2	4	

Note: (1) In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	
t_{CO2}	CE2 Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

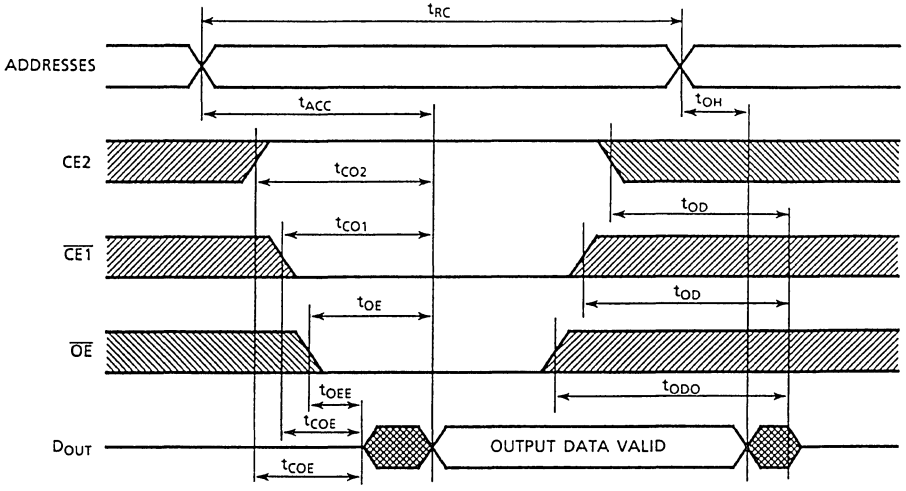
SYMBOL	PARAMETER	TC551001BPL/BFL/BFTL/BTRL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

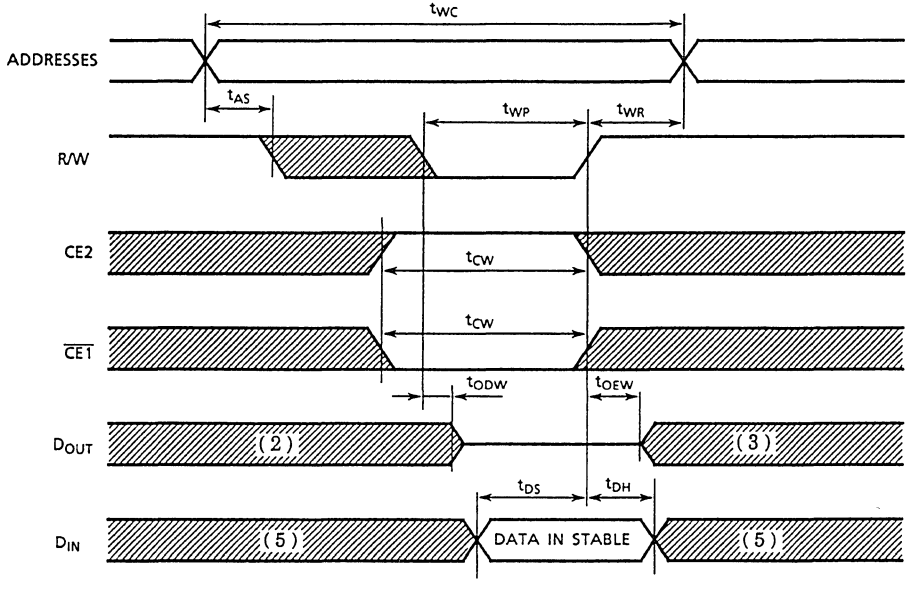
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

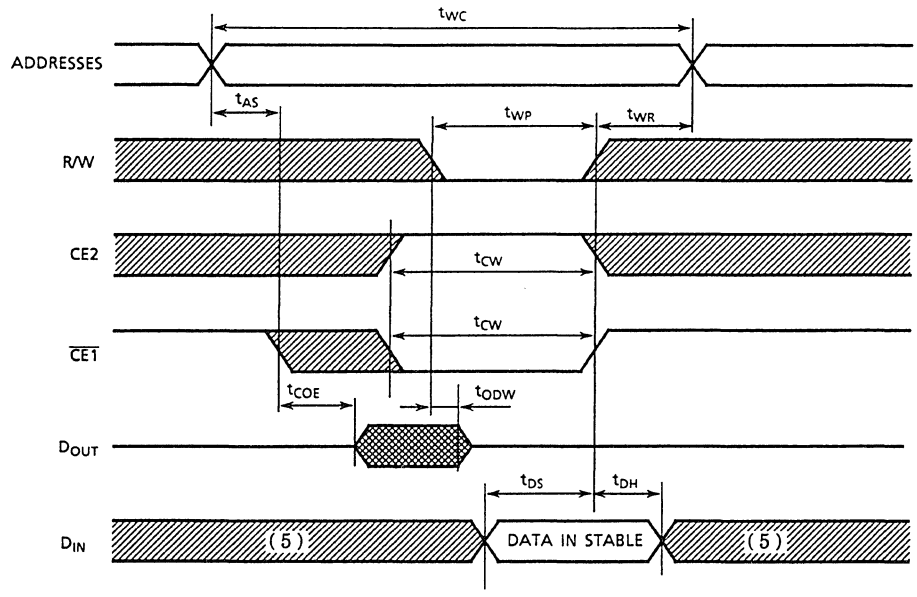
Read Cycle (1)



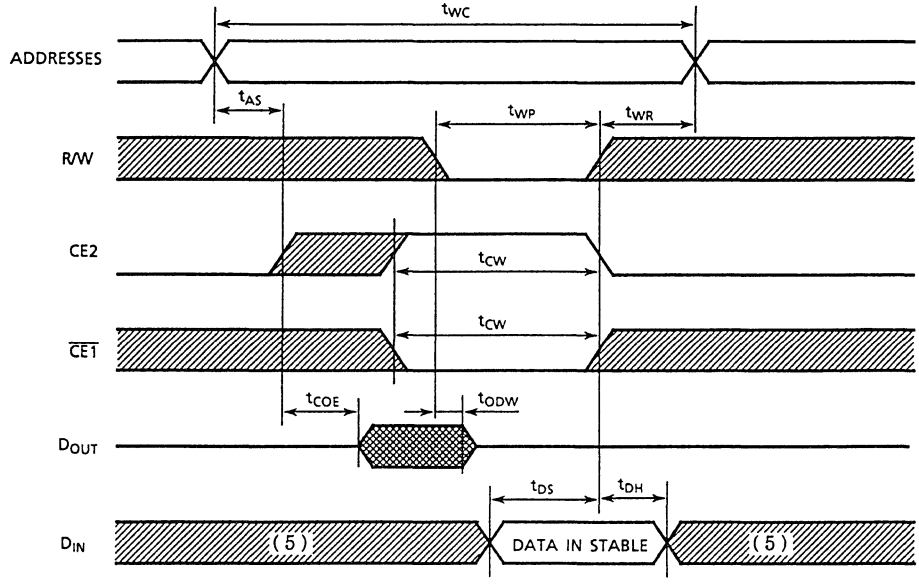
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W high transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.

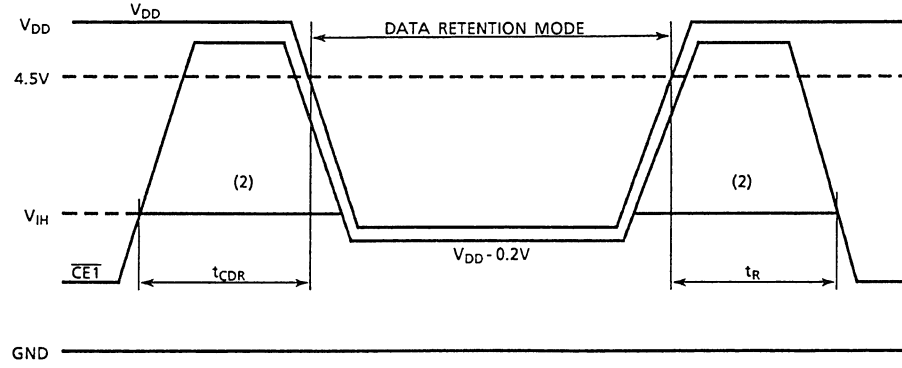
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

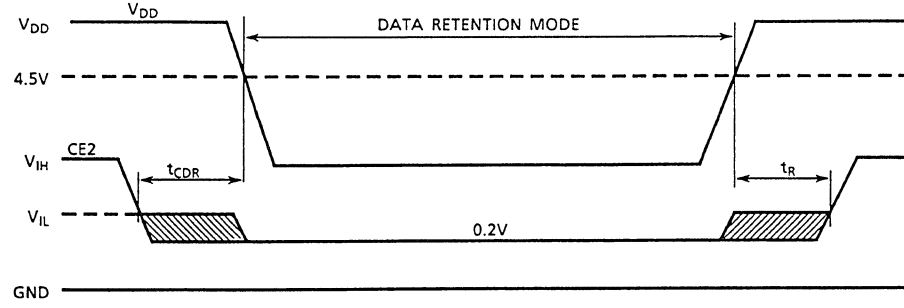
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	15*	µA
		V_{DD} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*3µA (max.) Ta = 0 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

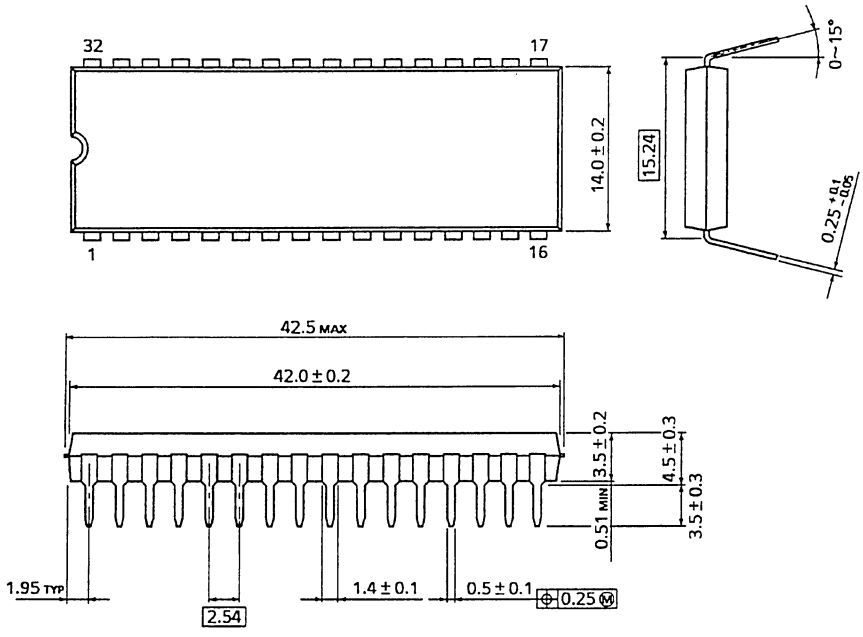
2. If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V.

Outline Drawing

DIP32-P-600

Unit in mm

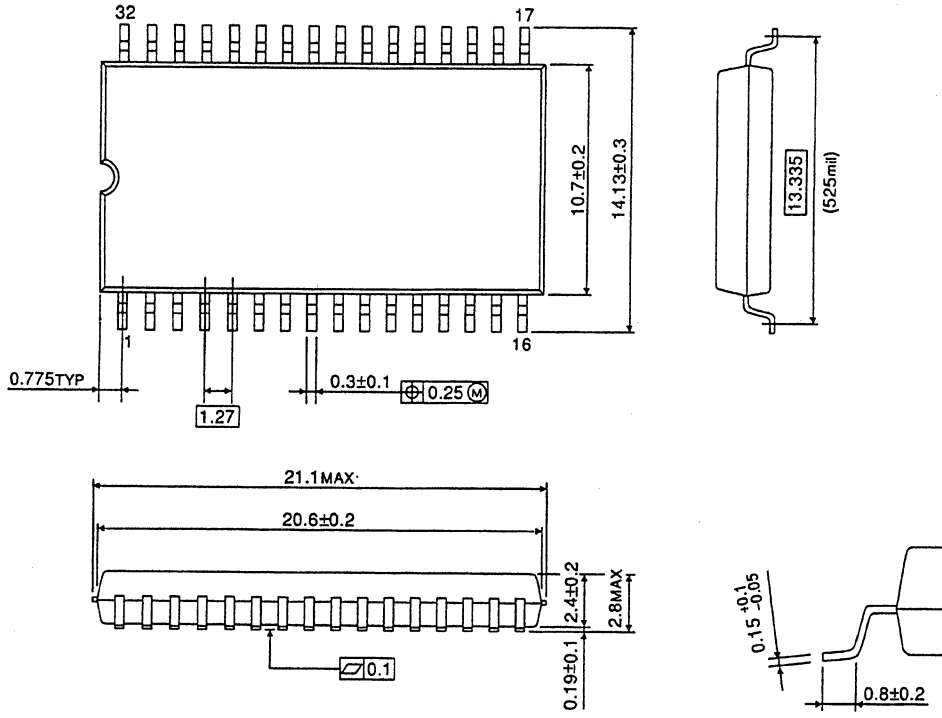


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

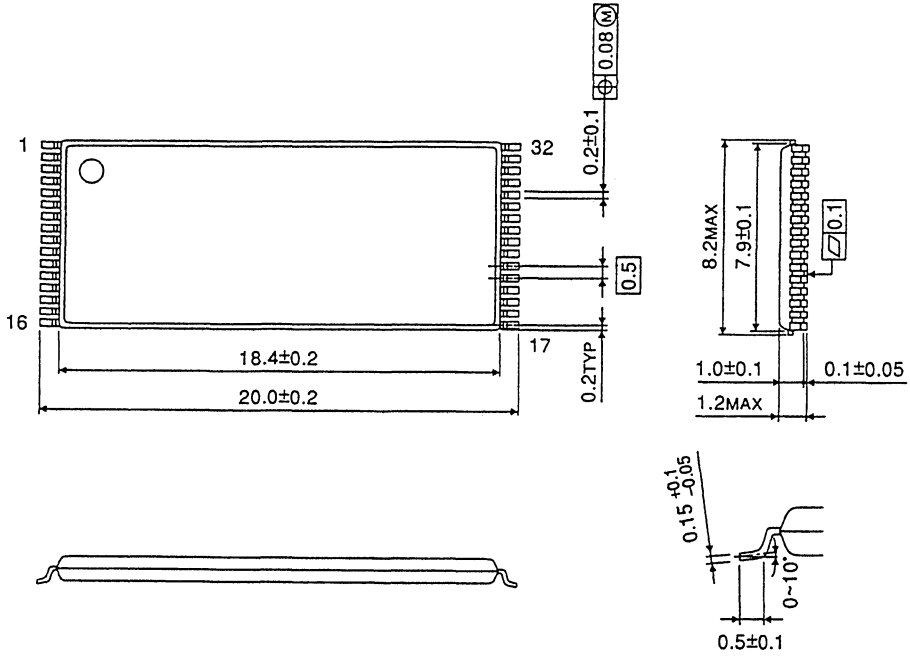


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

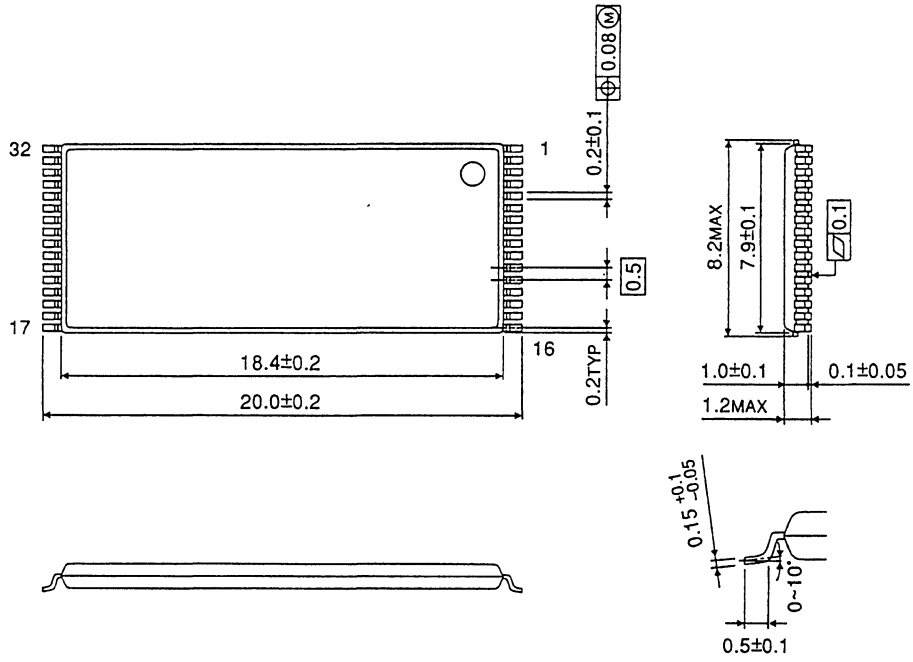


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC551001BPI guarantees -40 ~ 85°C operating temperature so TC551001BPI is suitable for use in wide operating temperature system.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

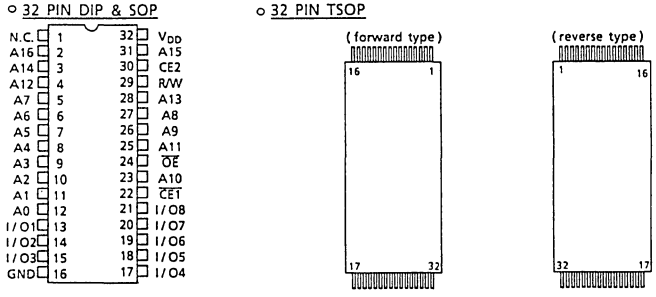
Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 200μA (max.)
- 5V single power supply
- Access time (max.)

	TC551001BPI/BFI/BFTI/BTRI	
	-85	-10
Access Time	85ns	100ns
$\overline{CE1}$ Access Time	85ns	100ns
CE2 Access Time	85ns	100ns
$\overline{OE}$ Access Time	45ns	50ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package TC551001BPI : DIP32-P-600
  TC551001BFI : SOP32-P-525
  TC551001BFTI : TSOP32-P-0820
  TC551001BTRI : TSOP32-P-0820A

Pin Connection (Top View)



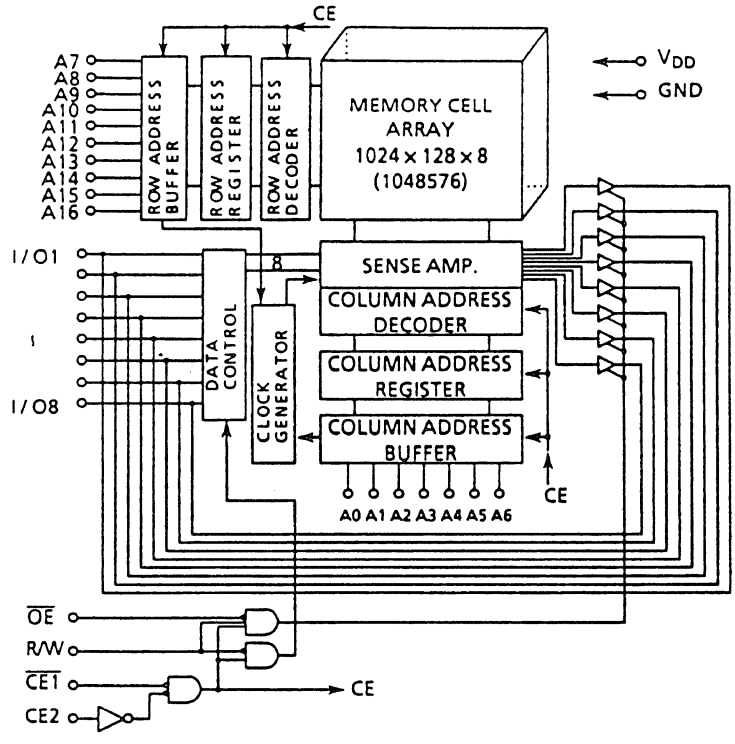
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 50ns Max.
** SOP

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns Max.

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
				1μs	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} - 0.2V I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	Min.	–	–	60	
				1μs	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			–	–	3	mA
I_{DDS2}(1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V, Ta = -40 ~ 85°C			–	2	200	μA

Note: (1) In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	85	–	100	
t_{CO2}	CE2 Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	35	–	40	
t_{ODO}	Output Enable to Output in High-Z	–	35	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

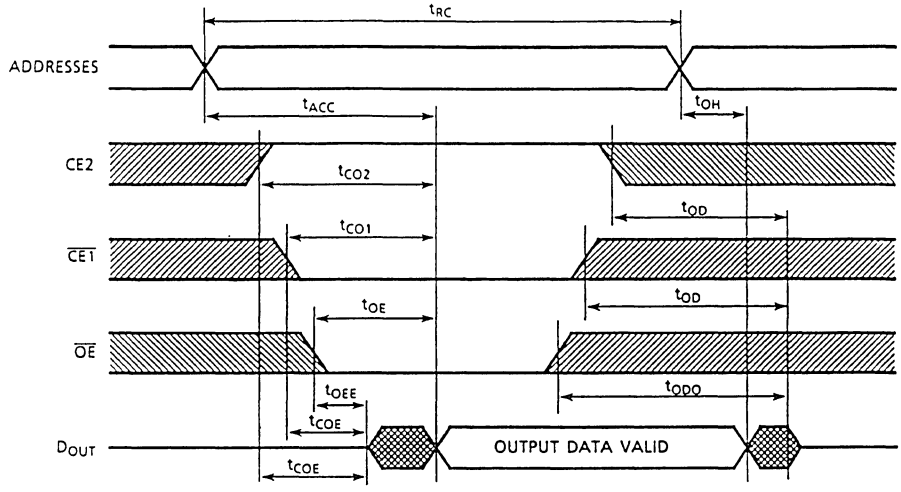
SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	60	–	
t_{CW}	Chip Selection to End of Write	75	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	35	–	40	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

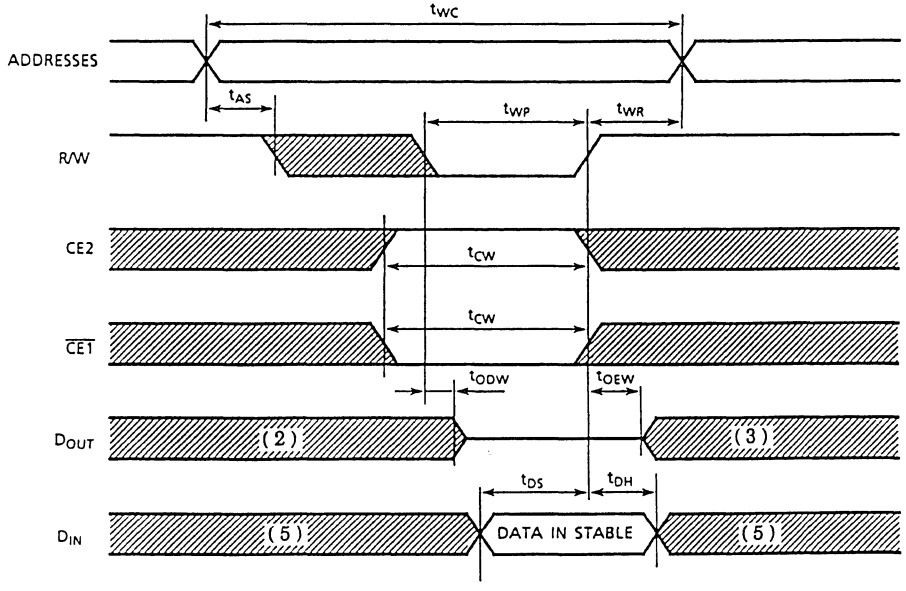
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

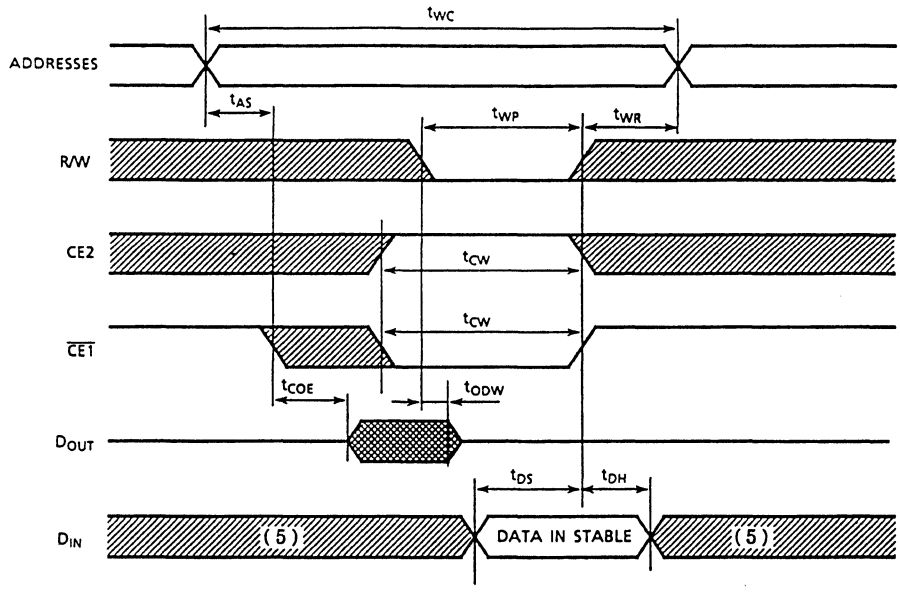
Read Cycle (1)



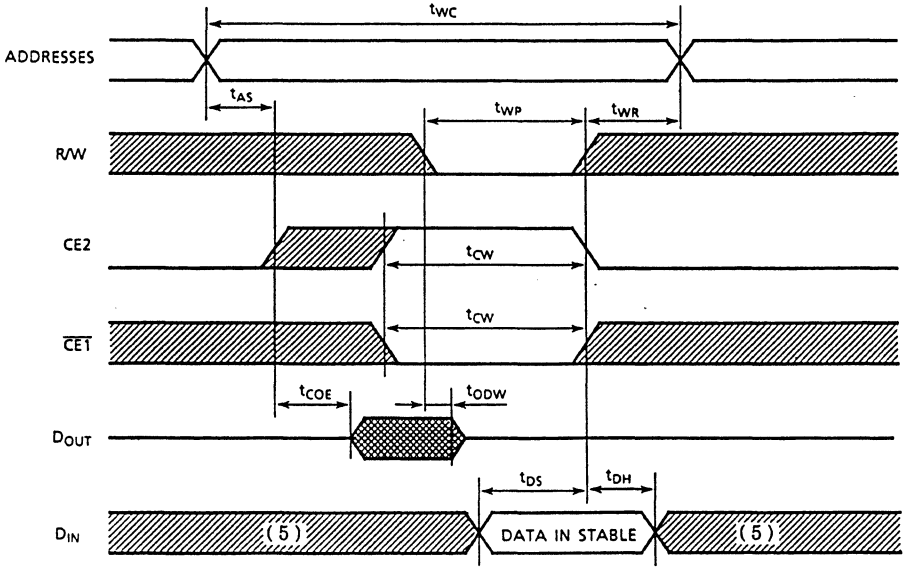
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is high for Read Cycle.

2. If the $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. If the $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

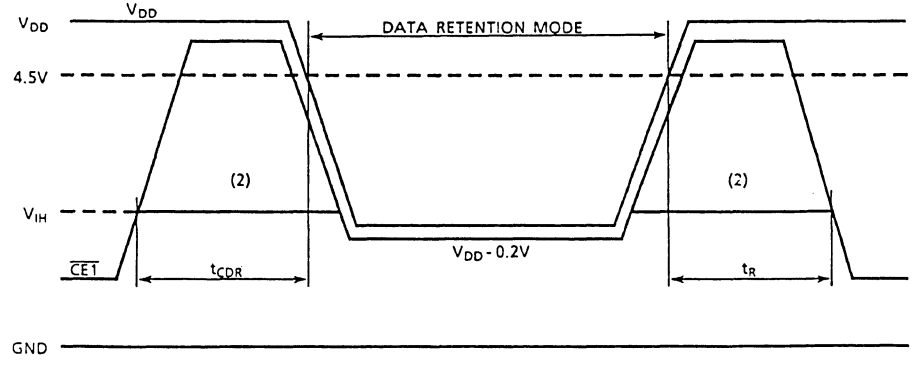
4. Assuming that $\overline{OE}$ is High for a write cycle, Outputs are in a high impedance state during this period.

5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

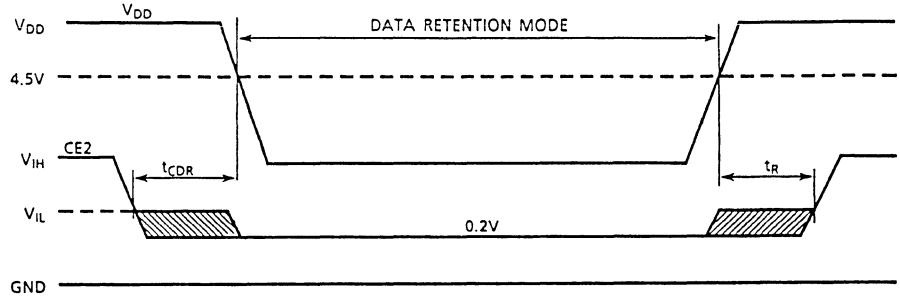
Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	100	µA
		V_{DD} = 5.5V	–	–	200	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

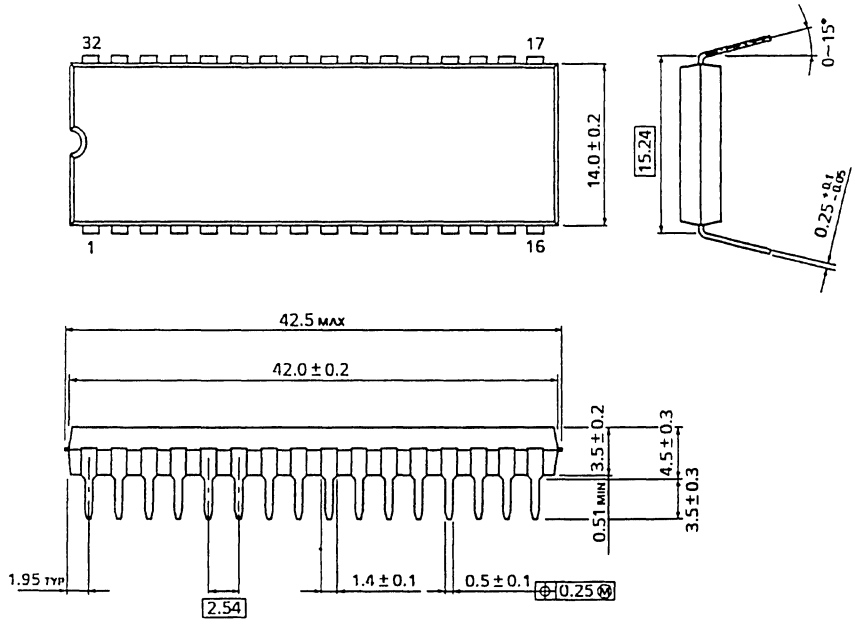
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V.

Outline Drawing

DIP32-P-600

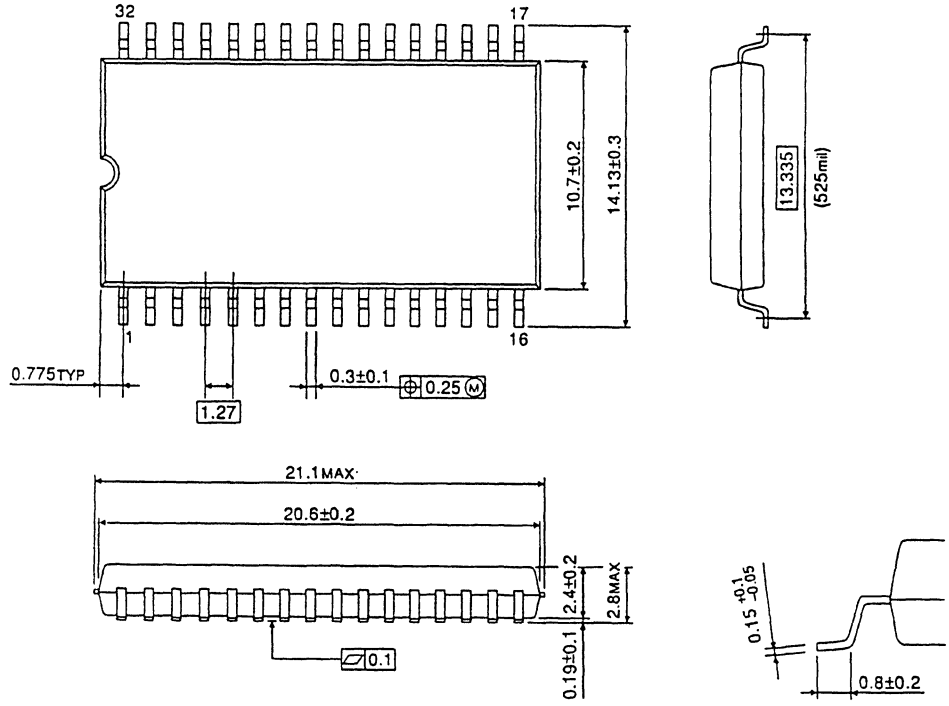
Unit in mm



Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525 Unit in mm

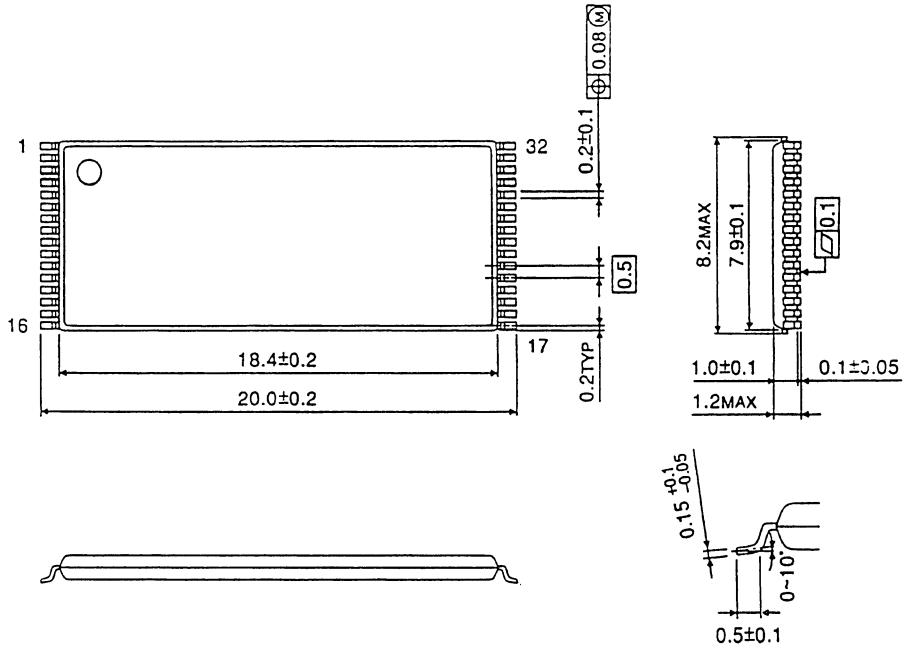


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

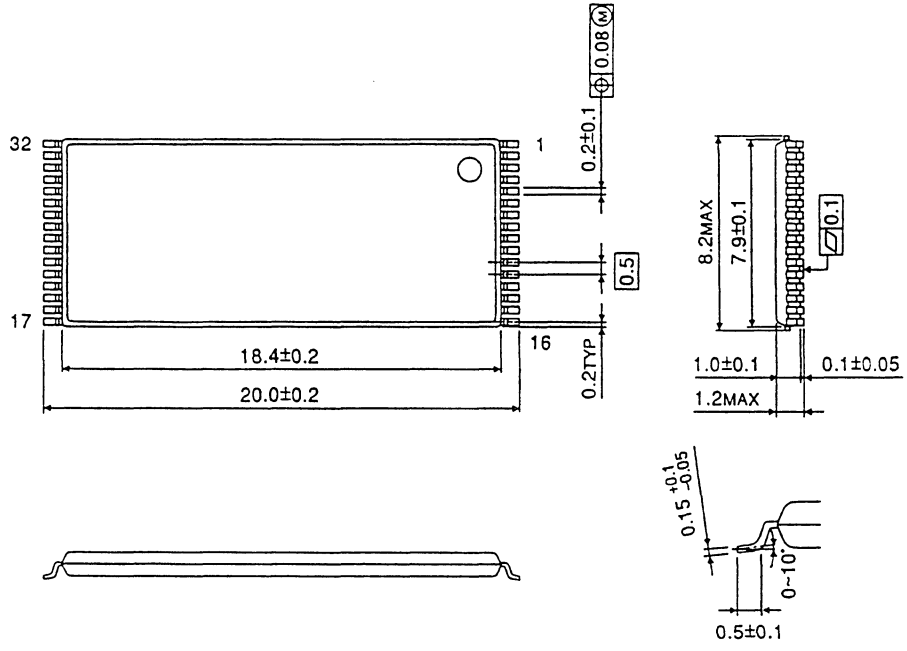


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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TC551001BPI/BFI/BFTI/BTRI-85L/10L

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC551001BPI guarantees -40 ~ 85°C operating temperature so TC551001BPI is suitable for use in wide operating temperature system.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

Features

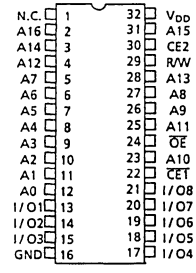
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC551001BPI/BFI/BFTI/BTRI	
	-85L	-10L
Access Time	85ns	100ns
$\overline{CE1}$ Access Time	85ns	100ns
CE2 Access Time	85ns	100ns
$\overline{OE}$ Access Time	45ns	50ns

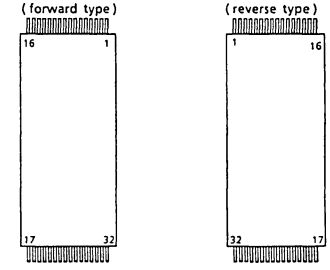
- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package TC551001BPI : DIP32-P-600
  TC551001BFI : SOP32-P-525
  TC551001BFTI : TSOP32-P-0820
  TC551001BTRI : TSOP32-P-0820A

Pin Connection (Top View)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP



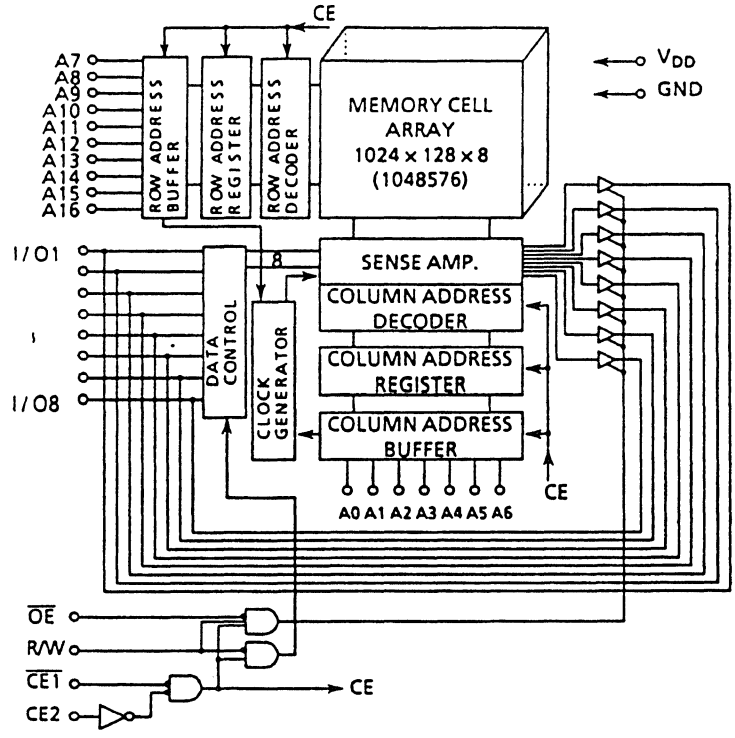
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 50ns Max.
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns Max.

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	70	mA
				1μs	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} - 0.2V I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	Min.	–	–	60	
				1μs	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			–	–	3	mA
I_{DDS2}(1)		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C		–	–	70	μA
			Ta = 25°C		–	2	4	

Note (1): In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, the specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO1}	$\overline{CE1}$ Access Time	–	85	–	100	
t_{CO2}	CE2 Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	35	–	40	
t_{ODO}	Output Enable to Output in High-Z	–	35	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

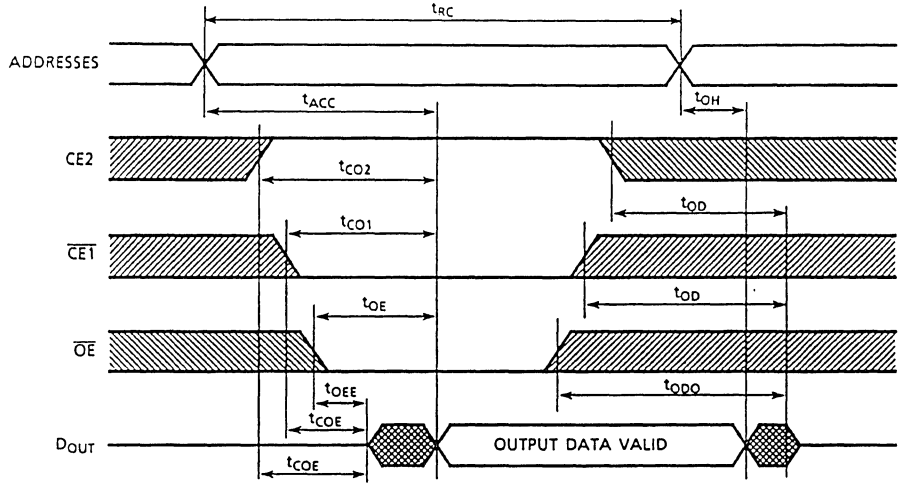
SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	60	–	
t_{CW}	Chip Selection to End of Write	75	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	35	–	40	
t_{OEW}	R/W to Output in Low-Z	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

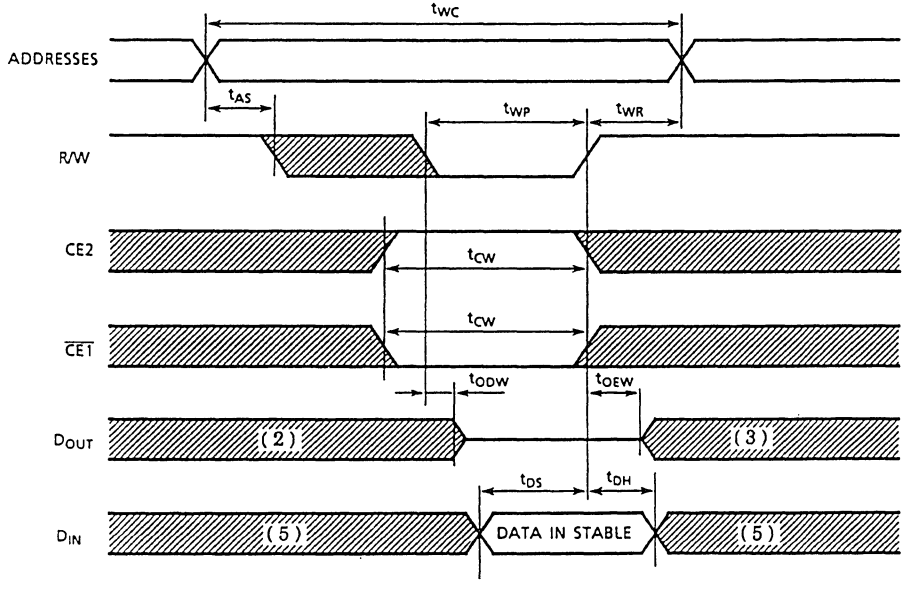
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

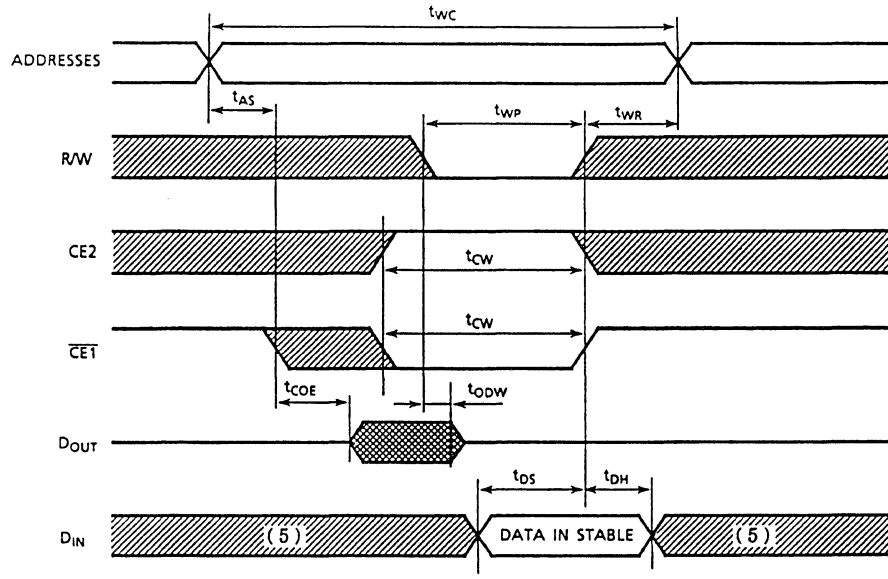
Read Cycle [1]



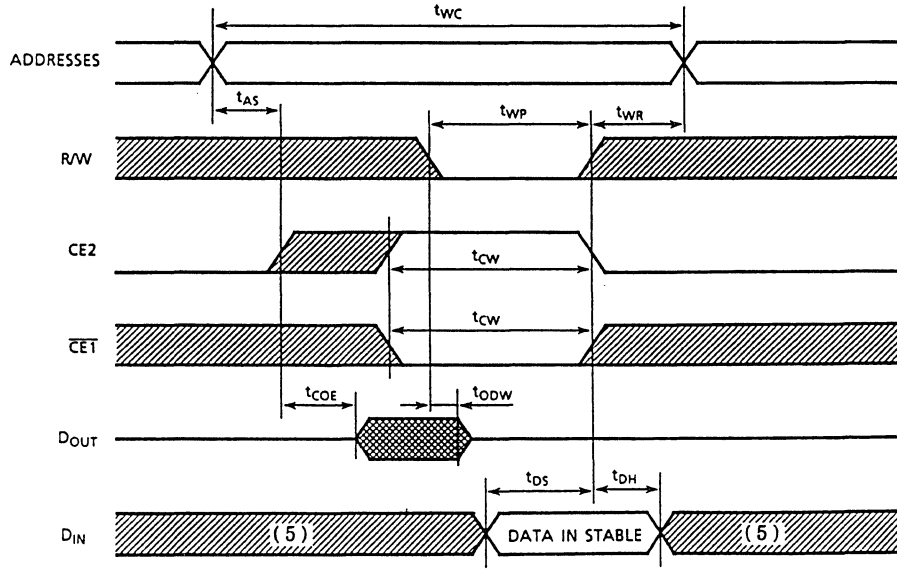
Write Cycle 1 [4] (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is high for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. If the $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a write cycle, outputs are in a high impedance state during this period.

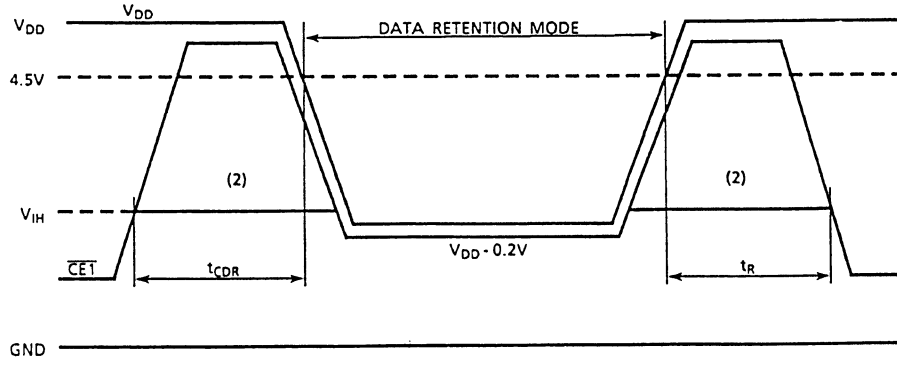
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

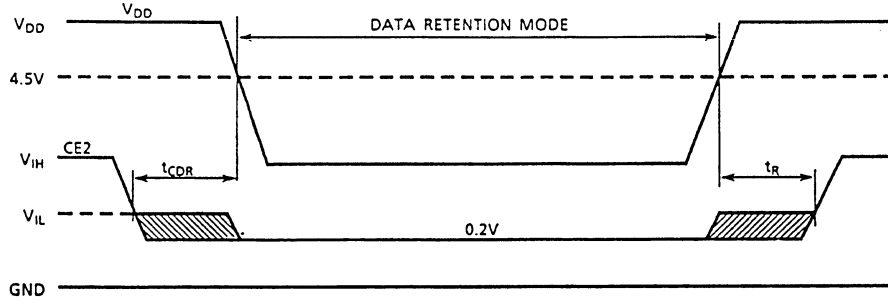
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	35*	µA
		V_{DD} = 5.5V	–	–	70	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*3µA (max.) Ta = -40 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

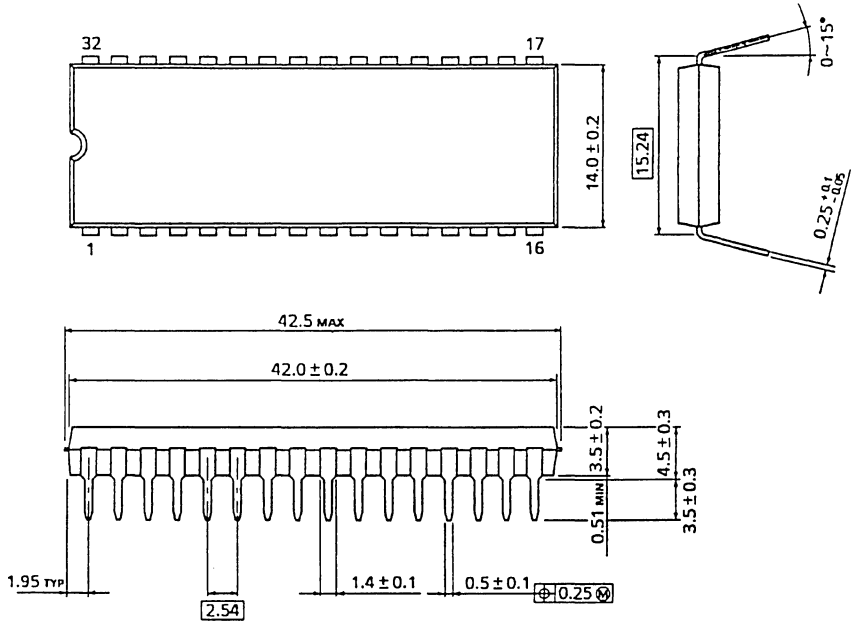
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition CE2 ≤ 0.2V.

Outline Drawing

DIP32-P-600

Unit in mm

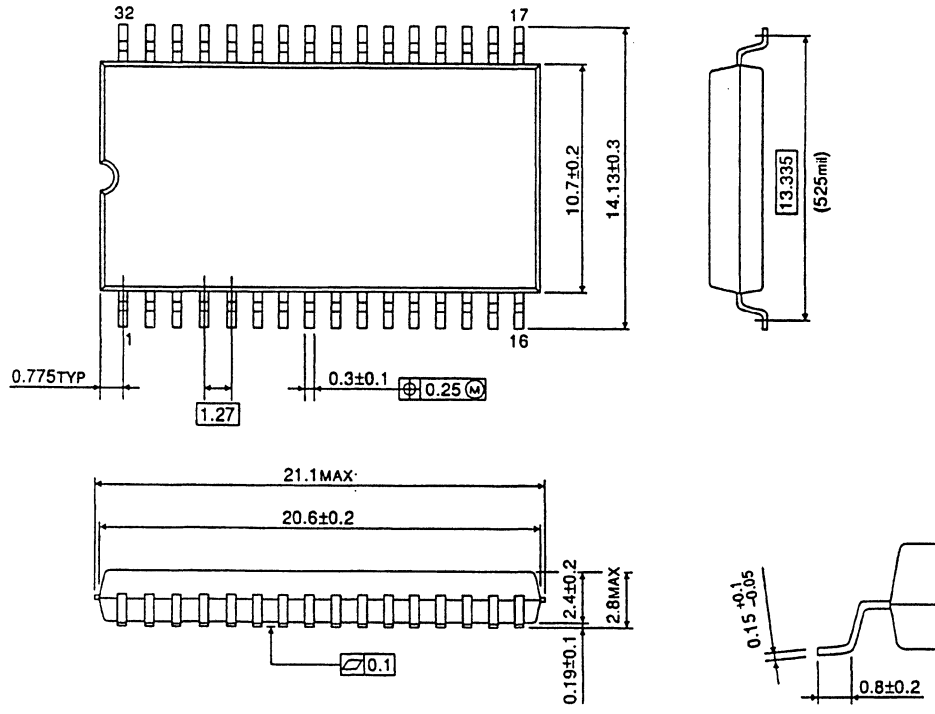


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

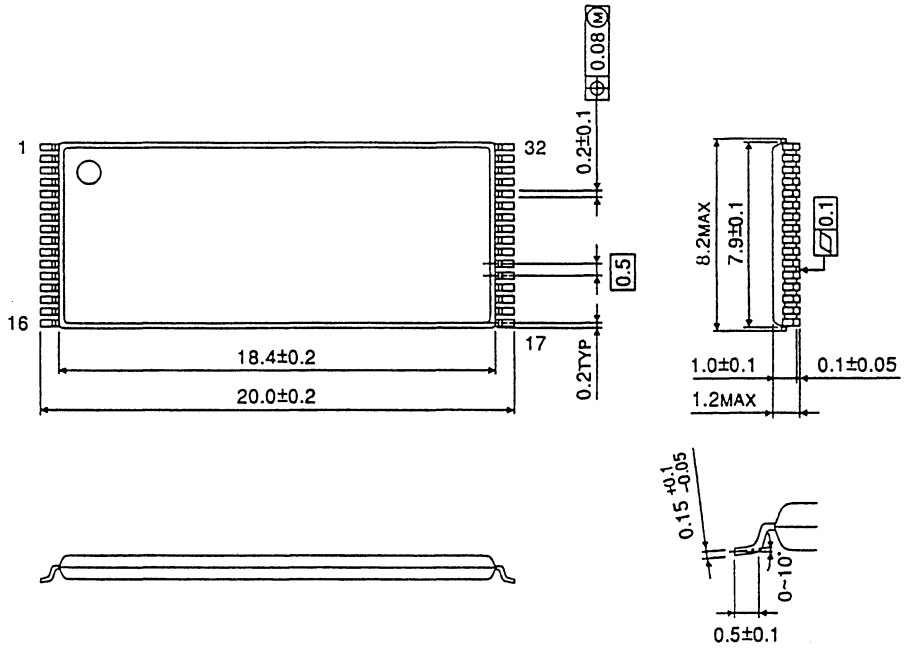


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

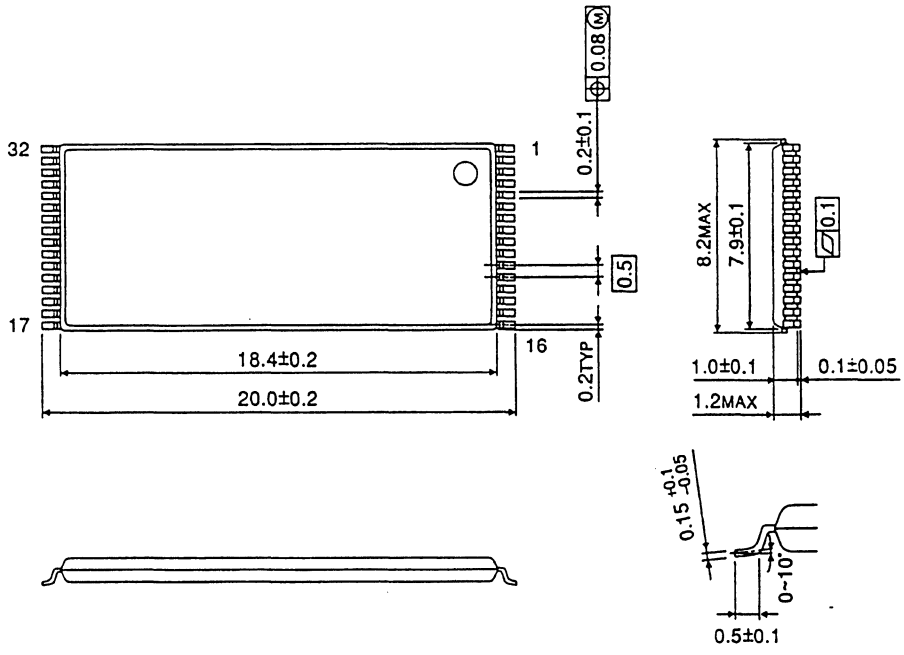


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



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TC551001BPI/BFI/BFTI/BTRI-85V/10V

SILICON GATE CMOS

PRELIMINARY

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC551001BPI guarantees -40 ~ 85°C operating temperature so TC551001BPI is suitable for use in wide operating temperature system.

The TC551001BPL is offered in a standard dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

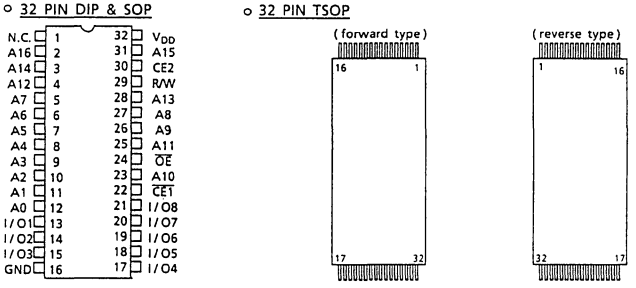
Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4μA (max.) at Ta = 25°C
- Single 2.7 ~ 5.5V power supply
- Access time (max.)

	5V±10%		2.7 ~ 5.5V
	-85V	-10V	-85V/-10V
Access Time	85ns	100ns	200ns
$\overline{CE1}$ Access Time	85ns	100ns	200ns
CE2 Access Time	85ns	100ns	200ns
$\overline{OE}$ Access Time	45ns	50ns	100ns

- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package TC551001BPI : DIP32-P-600
  TC551001BFI : SOP32-P-525
  TC551001BFTI : TSOP32-P-0820
  TC551001BTRI : TSOP32-P-0820A

Pin Connection (Top View)



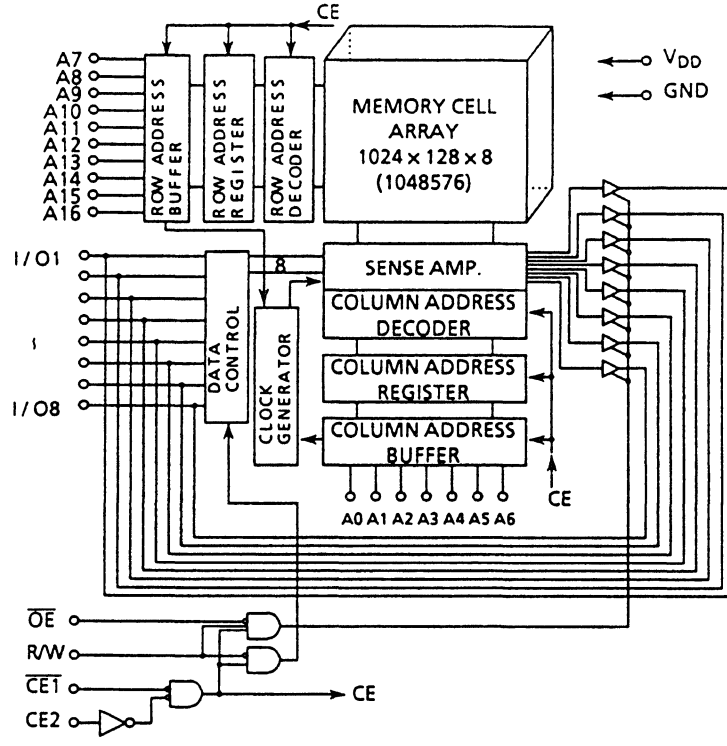
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 50ns Max.
** SOP

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	5V ±10%			2.2 ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	MIN.	MAX.	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	–	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V with a pulse width of 50ns Max.

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1μs	–	–	70	mA
			t_{cycle} = Min. cycle	–	–	20	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1μs	–	–	60	
			t_{cycle} = Min. cycle	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	70	μA
			Ta = 25°C	–	2	4	

Note (1): In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, the specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

DC and Operating Characteristics (Ta =-40 ~ 85°C, V_{DD} = 3V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} - 2.0V			-0.1	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V			0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V R/W = V_{DD} = 2.0V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle}	Min.	–	–	20	mA
				1μs	–	–	5	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 3V ± 10%	Ta = -40 ~ 85°C	–	–	40	μA
				Ta = 25°C	–	1	2	
			V_{DD} = 3.0V	Ta = -40 ~ 85°C	–	–	35	
				Ta = -40 ~ 40°C	–	–	3	
				Ta = 25°C	–	1	–	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	CE Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	–	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t_{OD}	Chip Enable (CE1, CE2) to Output in High-Z	–	35	–	40	
t_{ODO}	Output Enable to Output in High-Z	–	35	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	60	–	
t_{CW}	Chip Selection to End of Write	75	–	80	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	35	–	40	
t_{OEW}	R/W to Output in Low-Z	0	–	5	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 2.7 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	–	ns
t_{ACC}	Address Access Time	–	200	
t_{CO1}	CE1 Access Time	–	200	
t_{CO2}	CE2 Access Time	–	200	
t_{OE}	Output Enable to Output in Valid	–	100	
t_{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	
t_{OD}	Chip Enable (CE1, CE2) to Output in High-Z	–	60	
t_{ODO}	Output Enable to Output in High-Z	–	60	
t_{OH}	Output Data Hold Time	10	–	

Write Cycle

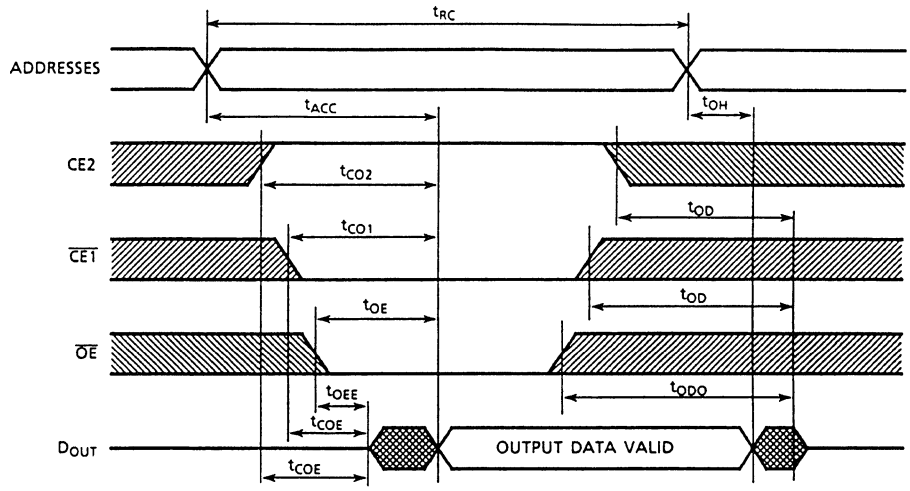
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	–	ns
t_{WP}	Write Pulse Width	120	–	
t_{CW}	Chip Selection to End of Write	150	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{ODW}	R/W to Output in High-Z	–	60	
t_{OEW}	R/W to Output in Low-Z	0	–	
t_{DS}	Data Setup Time	80	–	
t_{DH}	Data Hold Time	0	–	

AC Test Conditions

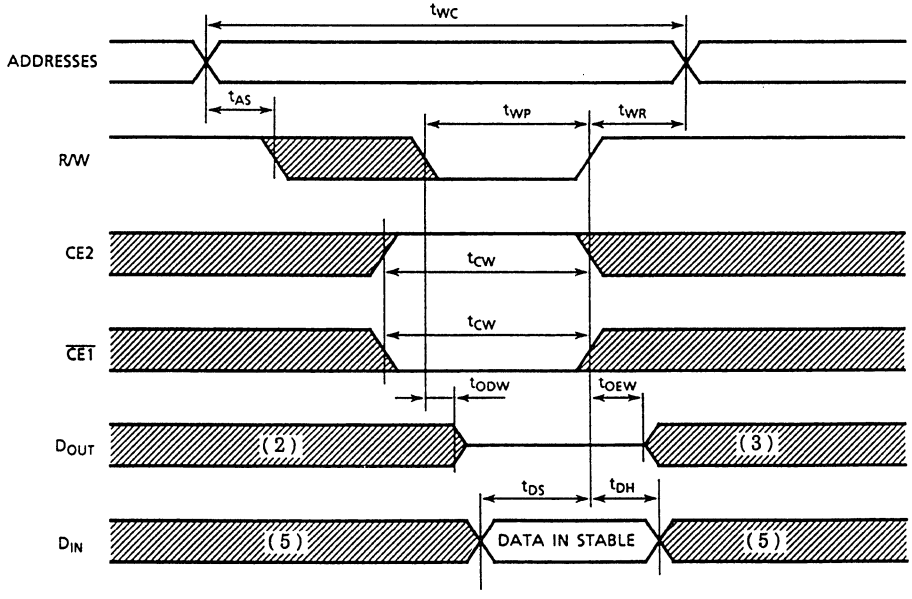
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	C_L = 100pF (Include Jig)

Timing Waveforms

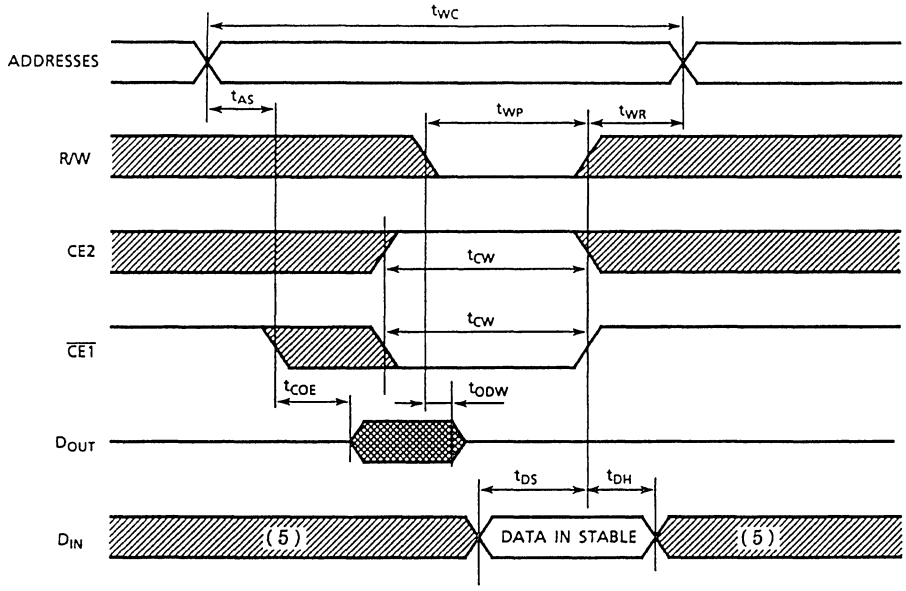
Read Cycle (1)



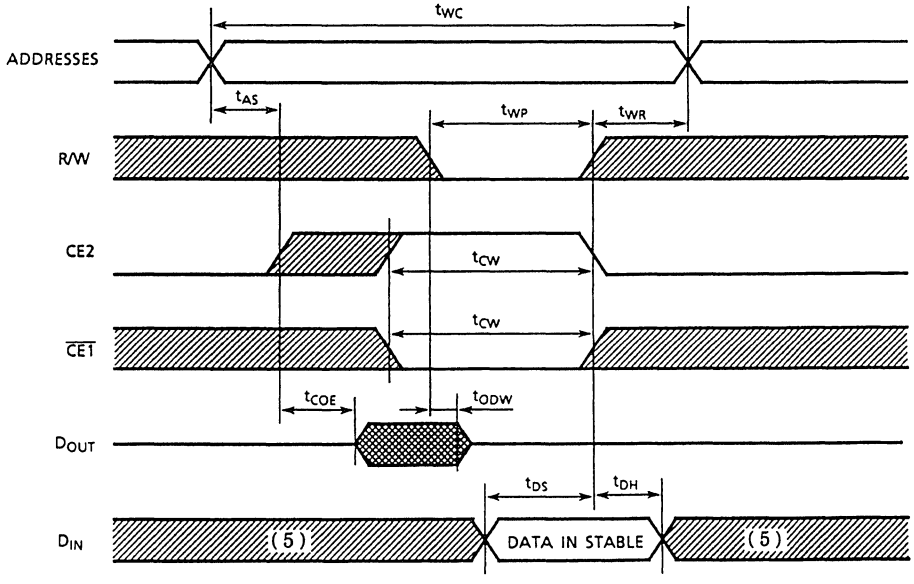
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE1}$ Controlled Write)



Write Cycle 3 [4] (CE2 Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.

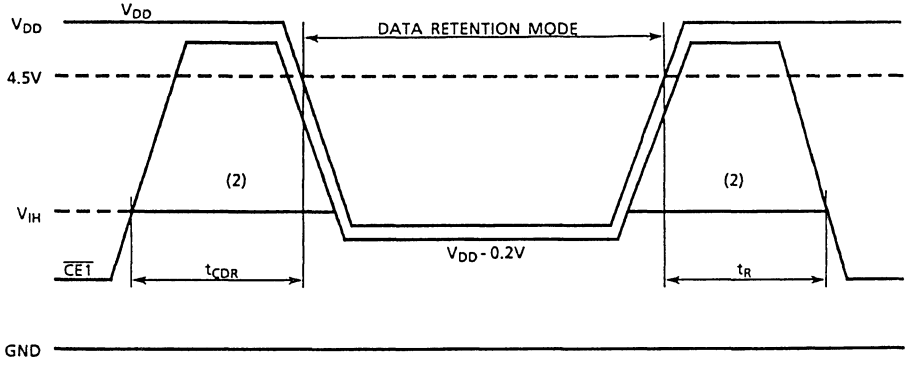
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

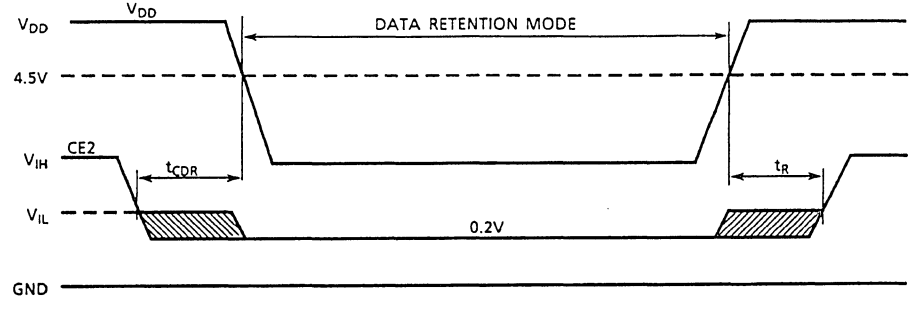
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	35*	µA
		V_{DD} = 5.5V	–	–	70	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*3µA (max.) Ta = -40 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V.

3.3V Operation

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3	–	0.2	

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}				–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}				–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} - 2.0V				-0.1	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V				0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V, R/W = V_{DD} = 2.0V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA		t_{cycle}	Min.	–	–	25	mA
					1μs	–	–	5	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 3.3V ± 0.3V	Ta = -40 ~ 85°C		–	–	45	μA
				Ta = 25°C		–	2	3	
			V_{DD} = 3.3V	Ta = -40 ~ 85°C		–	–	40	
				Ta = -40 ~ 40°C		–	–	5	
				Ta = 25°C		–	2	–	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter periodically sampled is not 100% tested.

3.3V Operation

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 3.3V±0.3V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO1}	CE1 Access Time	–	150	
t_{CO2}	CE2 Access Time	–	150	
t_{OE}	Output Enable to Output in Valid	–	75	
t_{COE}	Chip Enable CE to Output in Low-Z	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	
t_{OD}	Chip Enable CE to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	50	
t_{OH}	Output Data Hold Time	10	–	

Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Selection to End of Write	120	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{ODW}	R/W to Output in High-Z	–	50	
t_{OEW}	R/W to Output in Low-Z	0	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	

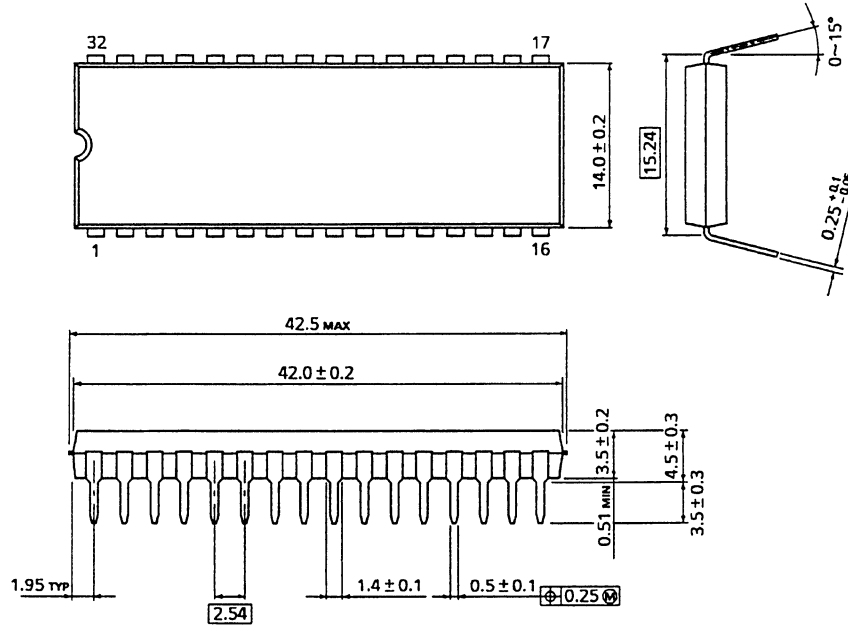
AC Test Conditions

Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	C_L = 100pF (Include Jig)

Outline Drawing

DIP32-P-600

Unit in mm

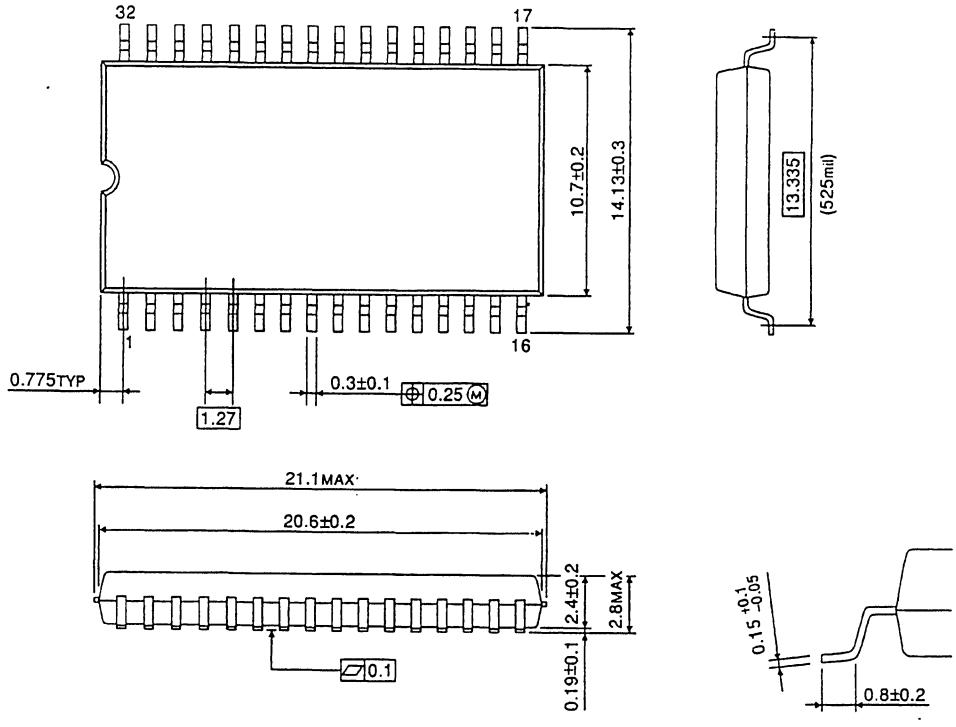


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

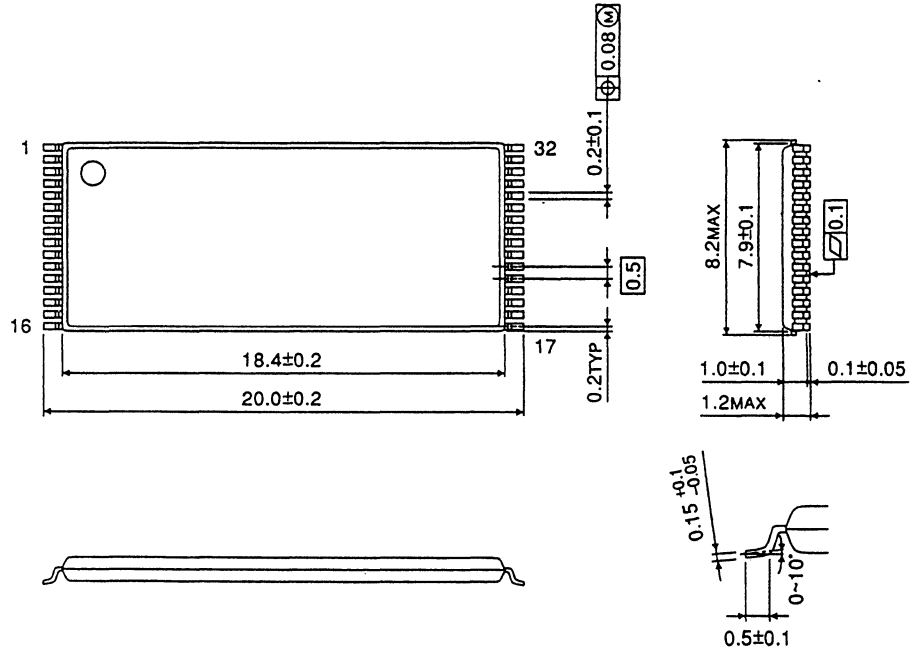


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

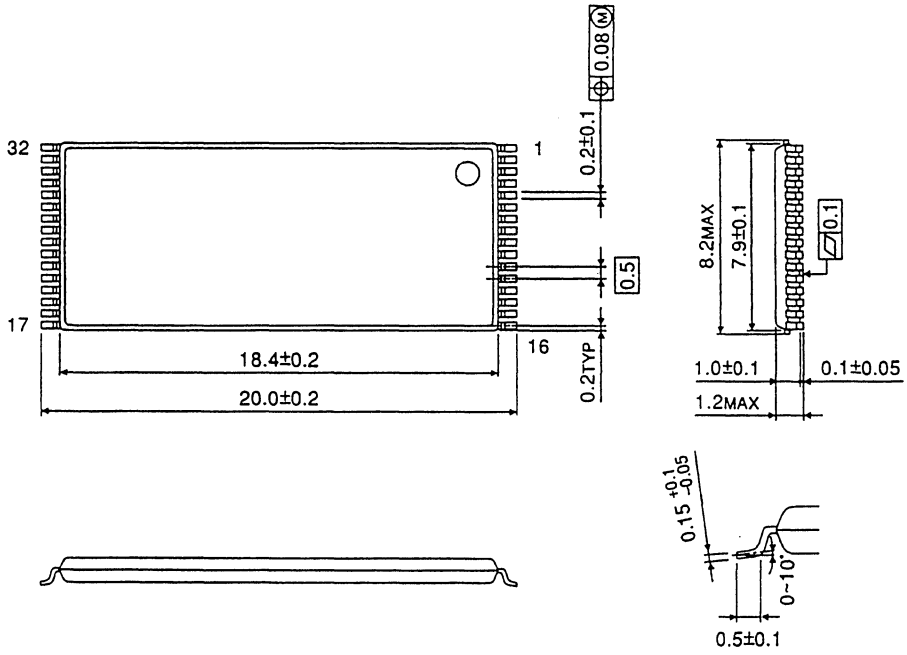


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

Notes

SILICON GATE CMOS

131,072 WORD x 8 BIT STATIC RAM

Description

The TC551001BPL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE1}$ is a logical high, or CE2 is low, the device is placed in a low power standby mode in which the standby current is 2μA typically. The TC551001BPL has three control inputs. Chip Enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. The TC551001BPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC551001BPL is offered in a dual-in-line 32-pin plastic package, a small outline plastic package, and a thin small outline plastic package (forward, reverse type).

Features

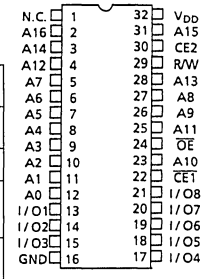
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 4μA (max.) at Ta = 25°C
- Single 2.7 ~ 5.5V power supply
- Access time (max.)

	5V ±10%		2.7 ~ 5.5
	-70V	-85V	-70V/-85V
Access Time	85ns	100ns	200ns
$\overline{CE1}$ Access Time	85ns	100ns	200ns
$\overline{CE2}$ Access Time	85ns	100ns	200ns
$\overline{OE}$ Access Time	45ns	50ns	100ns

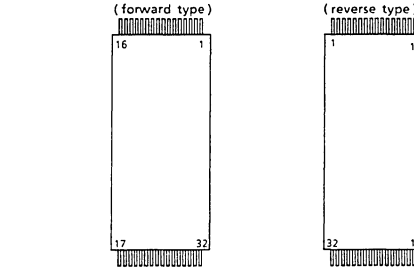
- Power down feature: $\overline{CE1}$, CE2
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC551001BPL : DIP32-P-600
  TC551001BFL : SOP32-P-525
  TC551001BFTL : TSOP32-P-0820
  OP32-P-0820A

Pin Connection (Top View)

○ 32 PIN DIP & SOP



○ 32 PIN TSOP



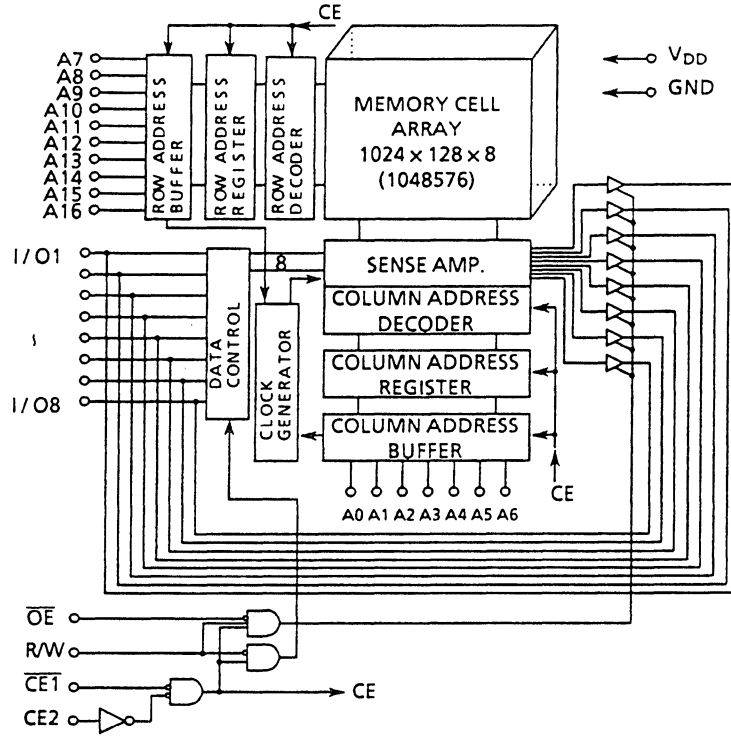
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power
GND	Ground
N.C.	No Connection

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	NC	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns
** SOP

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	5V ± 10%			2.2 ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	MIN.	MAX.	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	–	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V at pulse width at 50ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH} and R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1μs	–	–	70	mA
			t_{cycle} = Min. cycle	–	–	20	
I_{DDO2}		$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2 R/W = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1μs	–	–	60	
			t_{cycle} = Min. cycle	–	–	10	
I_{DDS1}	Standby Current	$\overline{CE1}$ = V_{IH} and CE2 = V_{IL}		–	–	3	mA
I_{DDS2}		$\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	–	–	30	μA
			Ta = 25°C	–	2	4	

Note: (1) In standby mode with $\overline{CE1}$ ≥ V_{DD} - 0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

DC and Operating Characteristics (Ta = -0 ~ 70°C, V_{DD} = 3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}				–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or RW $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}				–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} - 2.0V				-0.1	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.2V				0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE1}$ = 0.2V and CE2 = V_{DD} - 0.2V R/W = V_{DD} = 2.0V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle}	Min.		–	–	20	mA
				1μs		–	–	5	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V or CE2 = 0.2V	V_{DD} = 2.5 ~3V	Ta = 0 ~ 70°C		–	–	20	μA
				Ta = 25°C		–	1	2	
			V_{DD} = 3.0V	Ta = 0 ~ 70°C		–	–	15	
				Ta = 0 ~ 40°C		–	–	3	
				Ta = 25°C		–	1	–	

Capacitance (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO1}	$\overline{CE1}$ Access Time	–	70	–	85	
t_{CO2}	CE2 Access Time	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	60	–	
t_{CW}	Chip Selection to End of Write	60	–	75	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 2.7 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO1}	CE1 Access Time	–	150	
t_{CO2}	CE2 Access Time	–	150	
t_{OE}	Output Enable to Output in Valid	–	75	
t_{COE}	Chip Enable (CE1, CE2) to Output in Low-Z	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	
t_{OD}	Chip Enable (CE1, CE2) to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	50	
t_{OH}	Output Data Hold Time	10	–	

Write Cycle

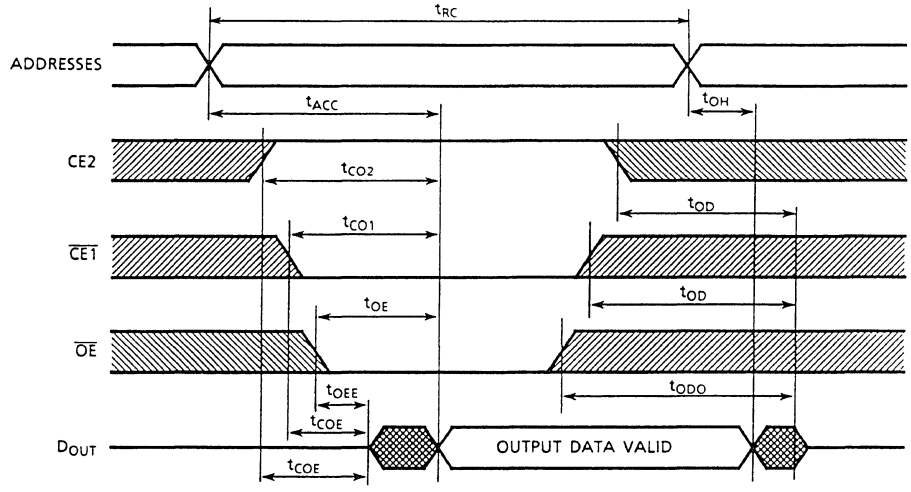
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Selection to End of Write	120	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{ODW}	R/W to Output in High-Z	–	50	
t_{OEW}	R/W to Output in Low-Z	5	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	

AC Test Conditions

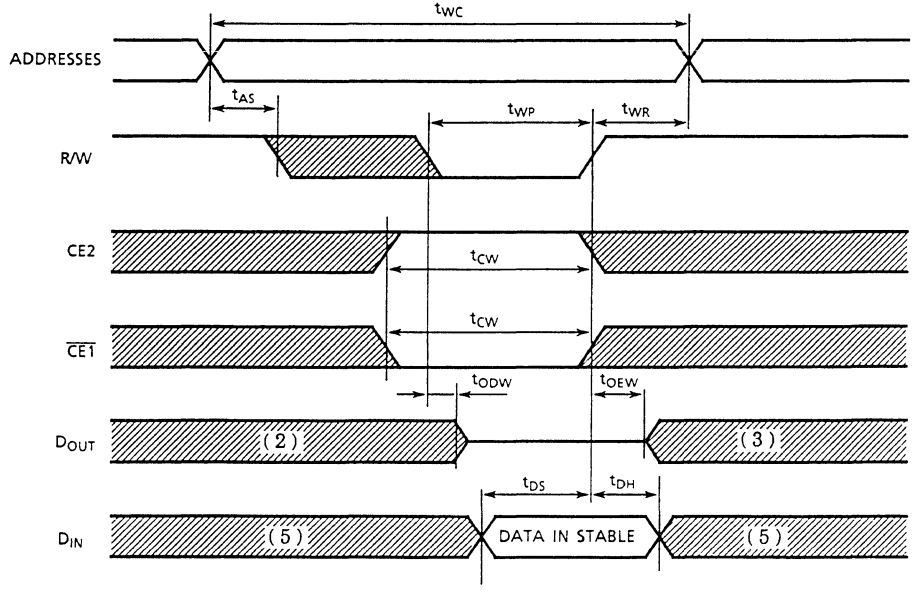
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	C_L = 100pF (Include Jig)

Timing Waveforms

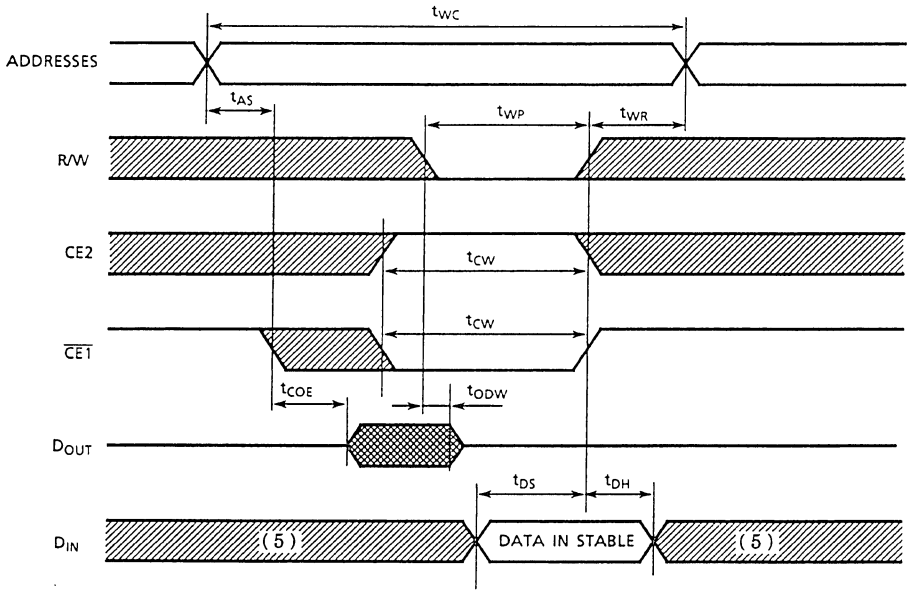
Read Cycle (1)



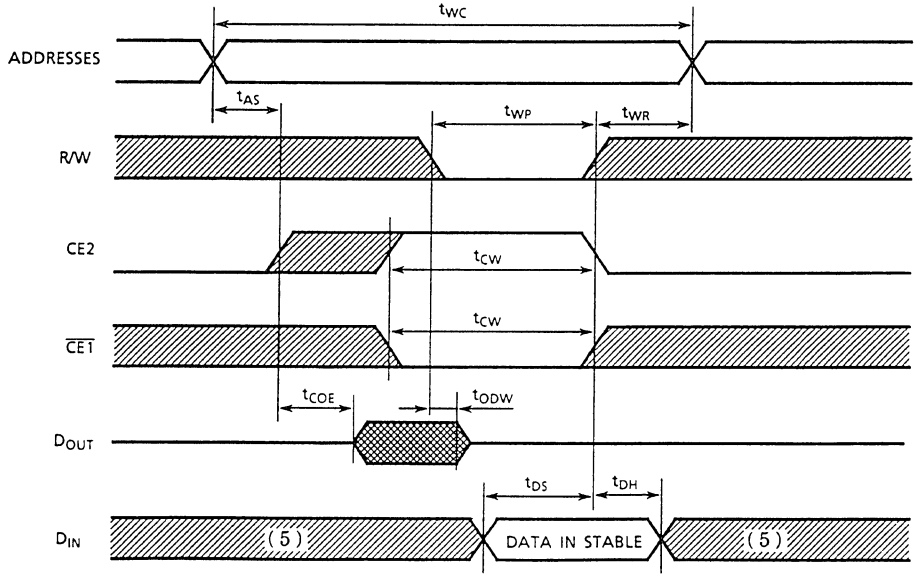
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE1}$ Controlled Write)



Write Cycle 3 (4) (CE2 Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, the outputs are in a high impedance state during this period.

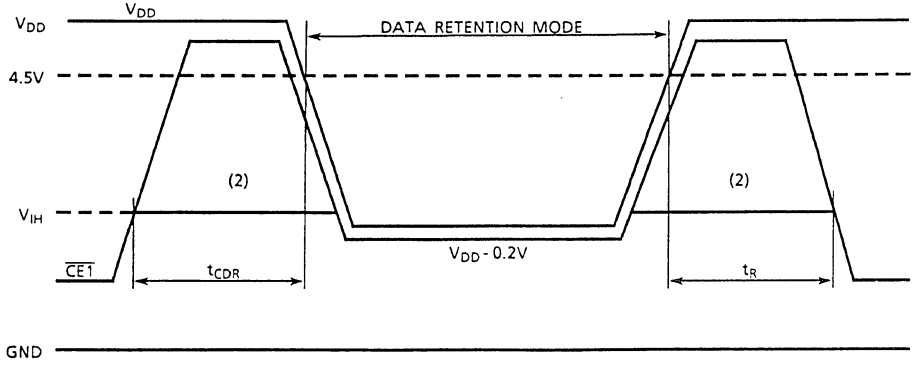
5. In I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

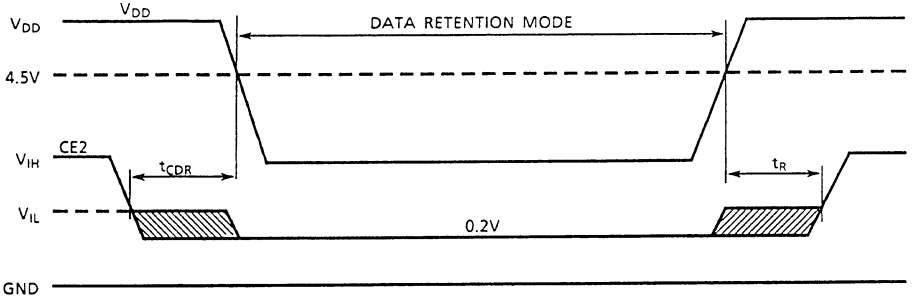
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	15*	µA
		V_{DD} = 5.5V	–	–	30	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*3µA (max.) Ta = -40 ~ 40°C

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Notes:

1. In the $\overline{CE1}$ controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V or CE2 ≥ V_{DD} - 0.2V.

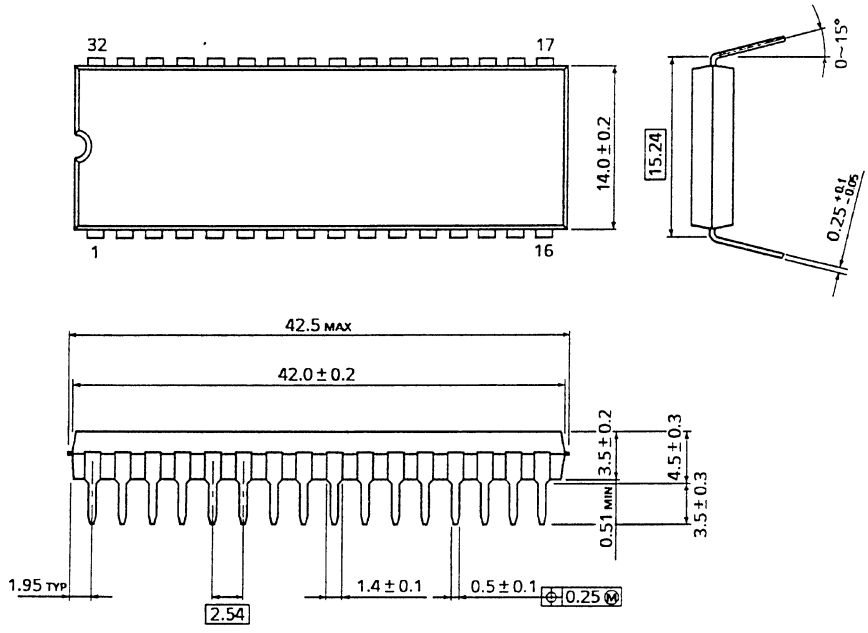
2. If the V_{IH} of $\overline{CE1}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

3. In the CE2 controlled data retention mode, minimum standby current is achieved under the condition of CE2 ≤ 0.2V.

Outline Drawing

DIP32-P-600

Unit in mm

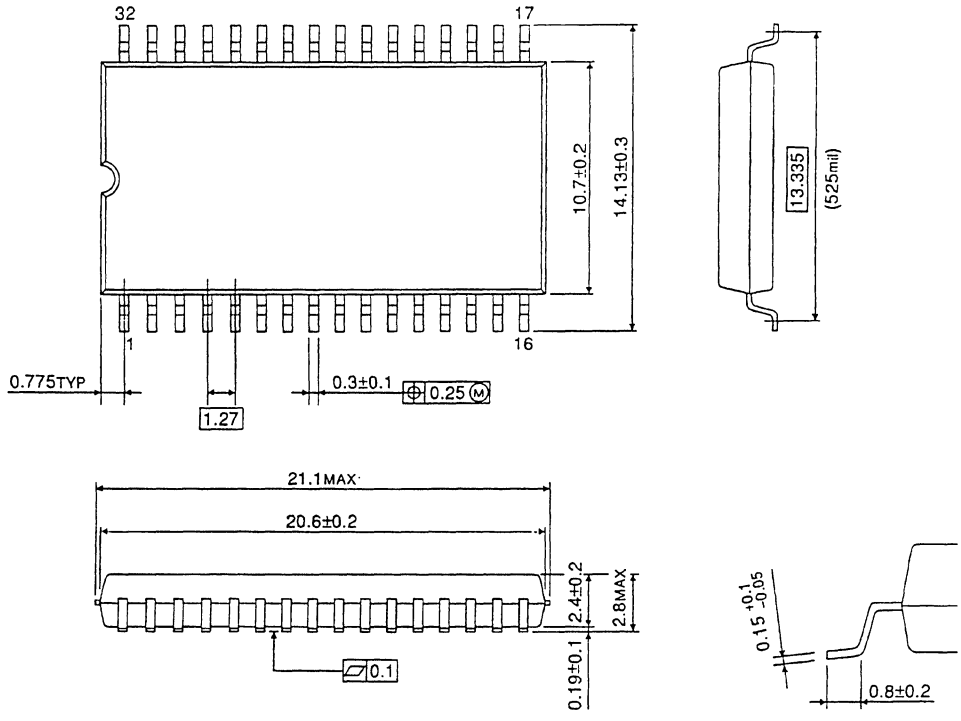


Weight : 4.45 g (Typ.)

Outline Drawing

SOP32-P-525

Unit in mm

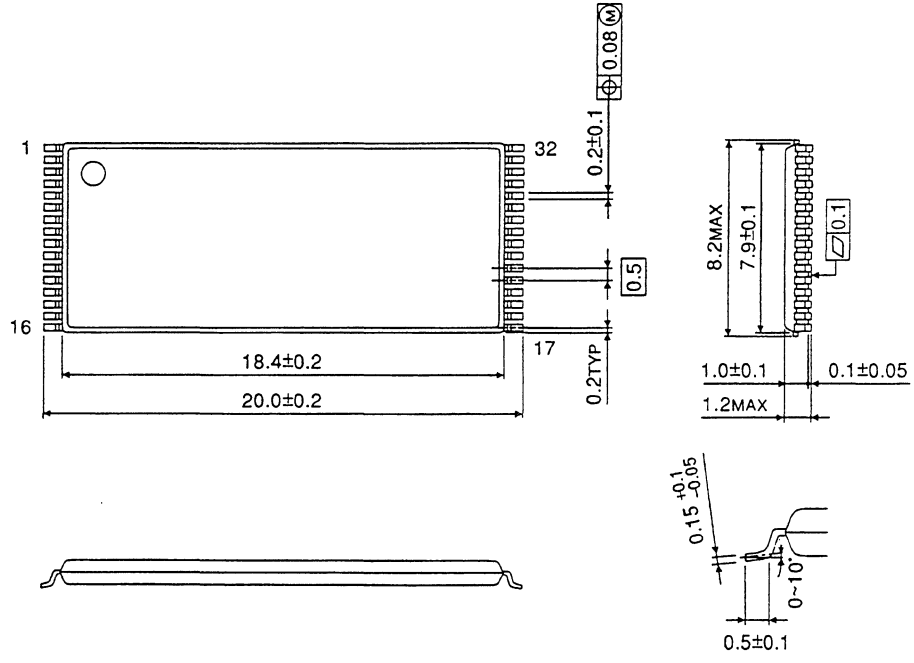


Weight : 1.04 g (Typ.)

Outline Drawing

TSOP32-P-0820

Unit in mm

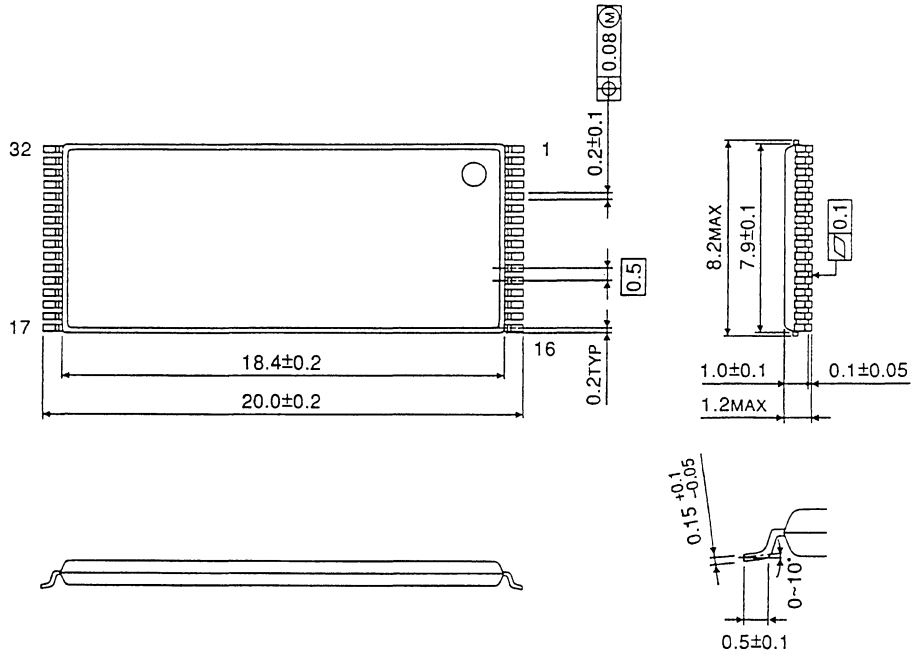


Weight : 0.34 g (Typ.)

Outline Drawing

TSOP32-P-0820A

Unit in mm



Weight : 0.34 g (Typ.)

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SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTL is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 100μA (max.). The TC554161FTL has two control inputs. A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC554161FTL is offered in a 54-pin thin small outline plastic package.

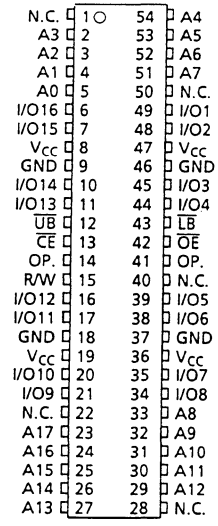
Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 100μA (max.)
- 5V single power supply
- Access time (max.)

	TC554161FTL	
	-70	-85
Access Time	70ns	85ns
$\overline{CE}$ Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC554161FTL : TSOP54-P-400

Pin Connection (Top View)

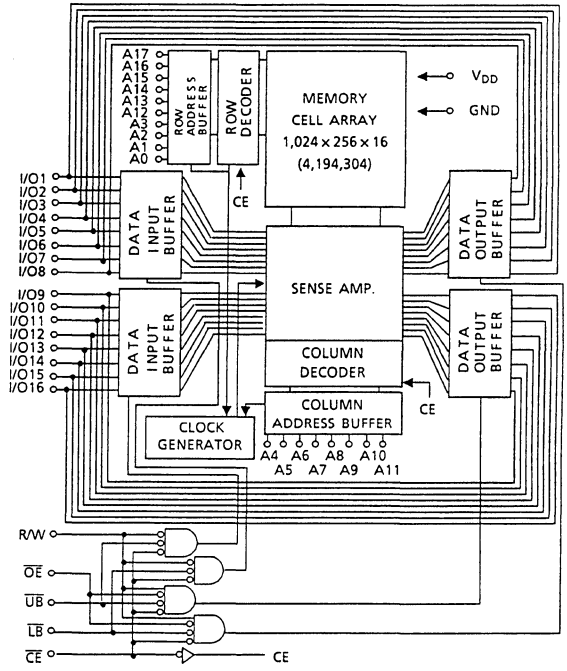


Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Input/Output
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP.	Option

* OP. pin must be connected to GND or open.

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/01 ~ I/08	I/09 ~ I/016	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 30ns MAx

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 30ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	110	mA
				85ns	–	–	100	
				1μs	–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	100	
				85ns	–	–	90	
				1μs	–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V			–	–	100	μA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTL				UNIT
		-70		-85		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO}	CE Access Time	–	70	–	85	
t_{OE}	OE Access Time	–	35	–	45	
t_{BA}	UB, LB Access Time	–	35	–	45	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	10	–	10	–	
t_{OEE}	Output Enable Time from OE	5	–	5	–	
t_{BE}	Output Enable Time from UB, LB	5	–	5	–	
t_{OD}	Output Disable Time from CE	–	25	–	30	
t_{ODO}	Output Disable Time from OE	–	25	–	30	
t_{BD}	Output Disable Time from UB, LB	–	25	–	30	

Write Cycle

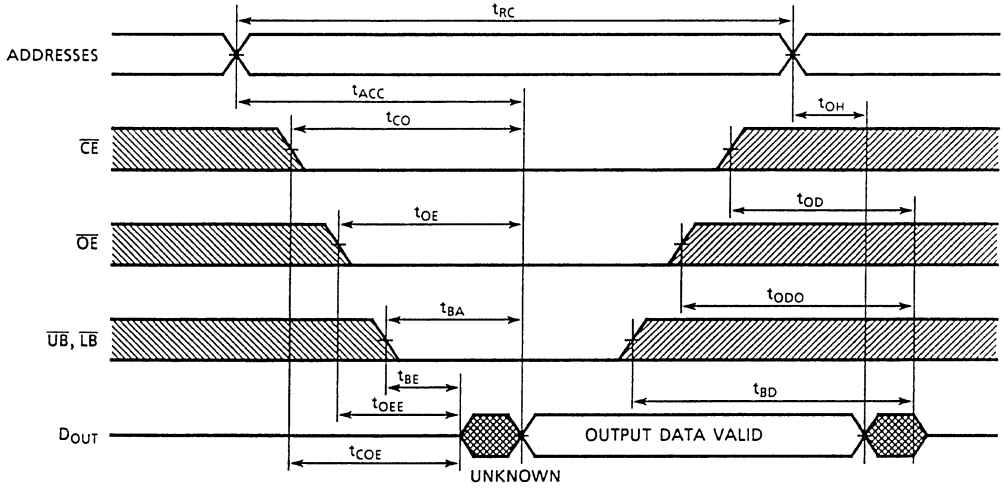
SYMBOL	PARAMETER	TC554161FTL				UNIT
		-70		-85		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	
t_{BW}	UB, LB Enable to End of Write	50	–	55	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	5	–	5	–	
t_{ODW}	Output Disable Time from R/W	–	25	–	30	

AC Test Conditions

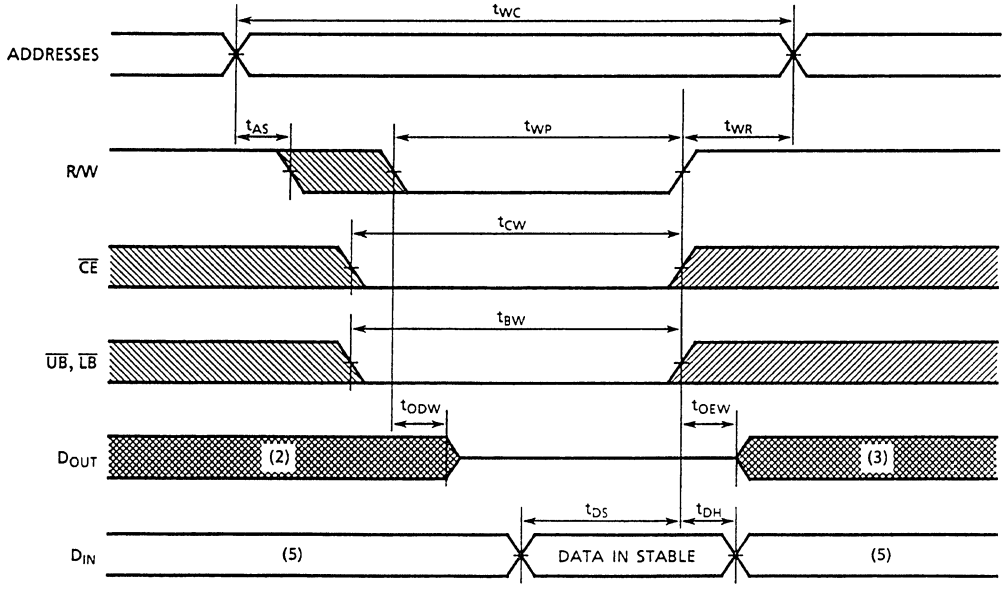
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

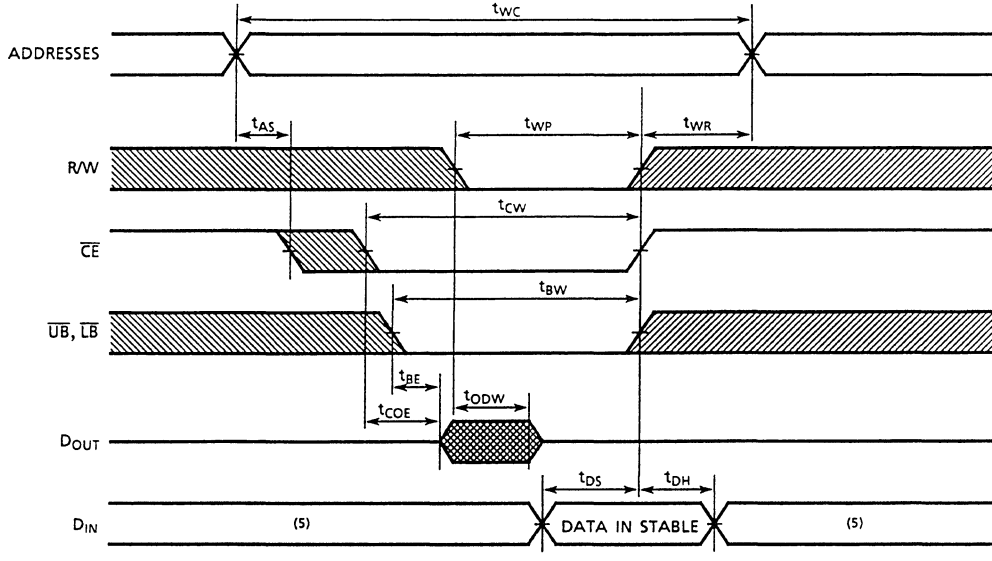
Read Cycle (1)



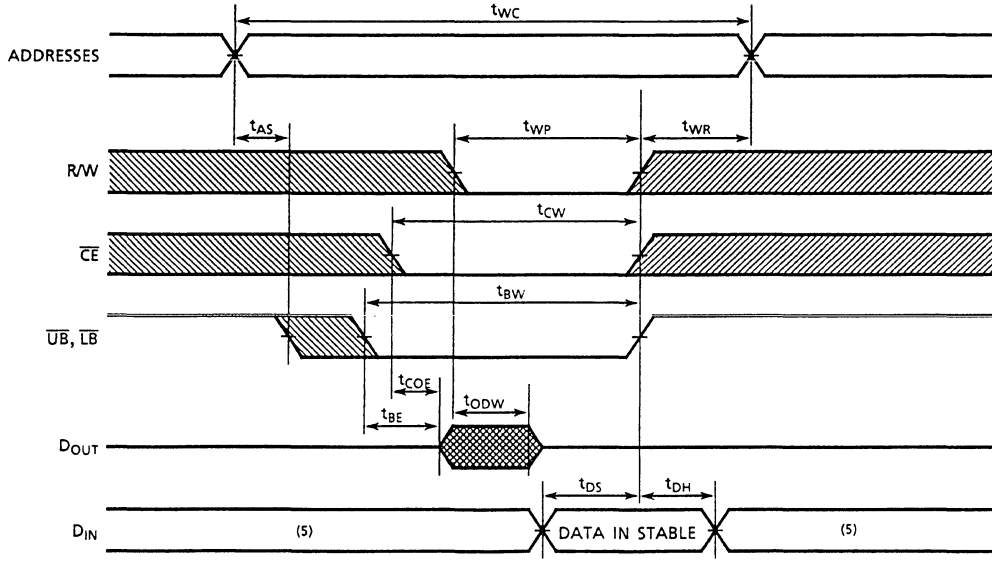
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Write Cycle 3 [4] ($\overline{UB}$, $\overline{LB}$ Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

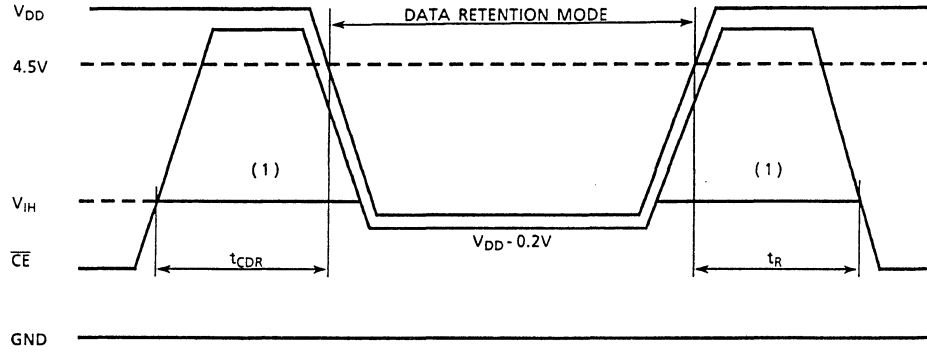
4. Assuming that $\overline{OE}$ is high for a Write Cycle, Outputs are in a high impedance state during this period.

5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	50	μA
		V_{DD} = 5.5V	–	–	100	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

$\overline{CE}$ Controlled Data Retention Mode



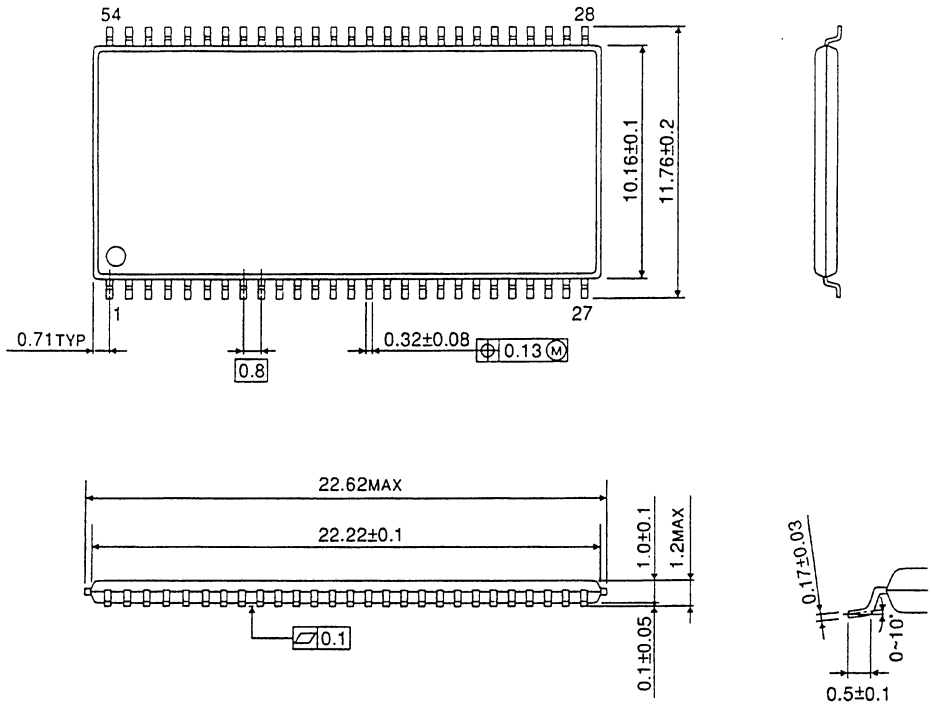
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



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SILICON GATE CMOS

PRELIMINARY

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTL is a 4,194,304 bit static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 60μA (max.). The TC554161FTL has two control inputs. A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC554161FTL is offered in a 54-pin thin small outline plastic package.

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 8μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC554161FTL	
	-70L	-85L
Access Time	70ns	85ns
$\overline{CE}$ Access Time	70ns	85ns
$\overline{OE}$ Access Time	35ns	45ns

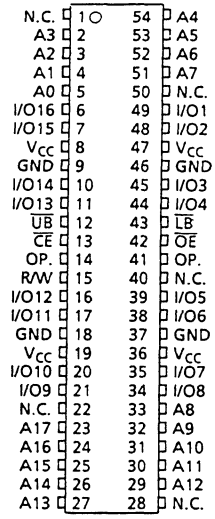
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC554161FTL : TSOP54-P-400

Pin Names

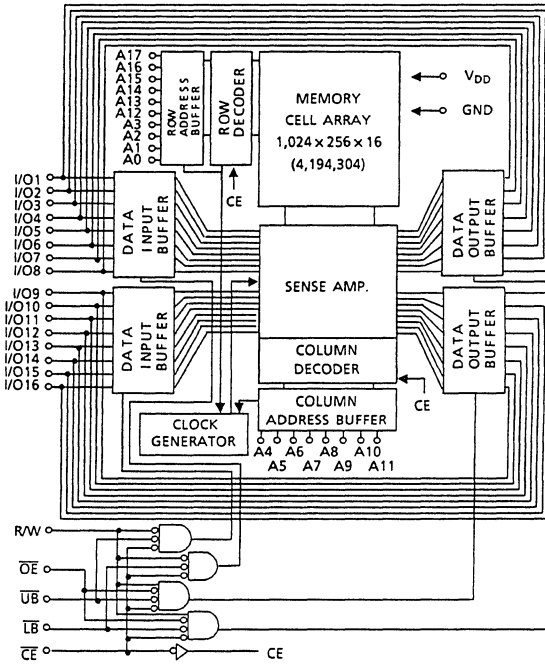
A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP.*	Option

* OP. pin must be connected to GND or open.

Pin Connection (Top View)



Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 30ns Max.

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 30ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	110	mA
				85ns	–	–	100	
				1μs	–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	100	
				85ns	–	–	90	
				1μs	–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C		–	–	60	μA
			Ta = 25°C		–	4	8	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO}	CE Access Time	–	70	–	85	
t_{OE}	OE Access Time	–	35	–	45	
t_{BA}	UB, LB Access Time	–	35	–	45	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	10	–	10	–	
t_{OEE}	Output Enable Time from OE	5	–	5	–	
t_{BE}	Output Enable Time from UB, LB	5	–	5	–	
t_{OD}	Output Disable Time from CE	–	25	–	30	
t_{ODO}	Output Disable Time from OE	–	25	–	30	
t_{BD}	Output Disable Time from UB, LB	–	25	–	30	

Write Cycle

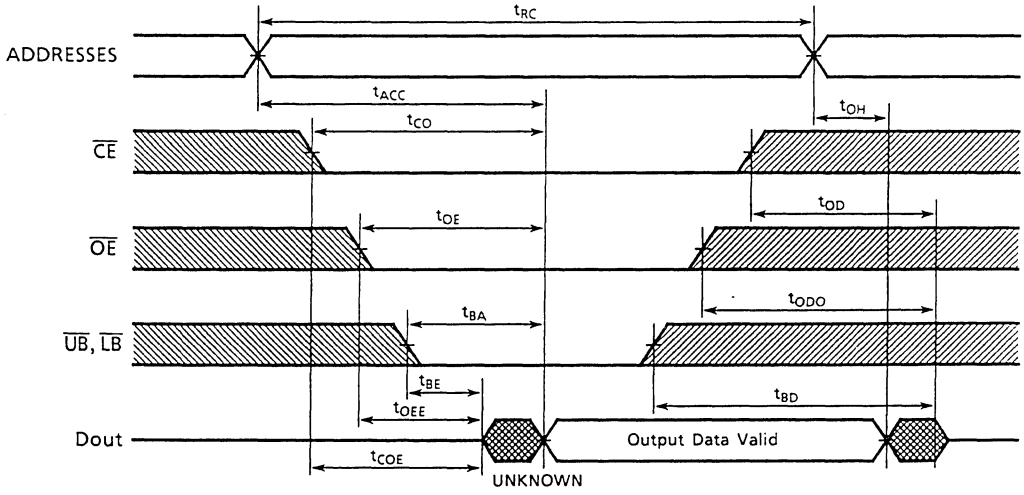
SYMBOL	PARAMETER	TC554161FTL				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	
t_{BW}	UB, LB Enable to End of Write	50	–	55	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	5	–	5	–	
t_{ODW}	Output Disable Time from R/W	–	25	–	30	

AC Test Conditions

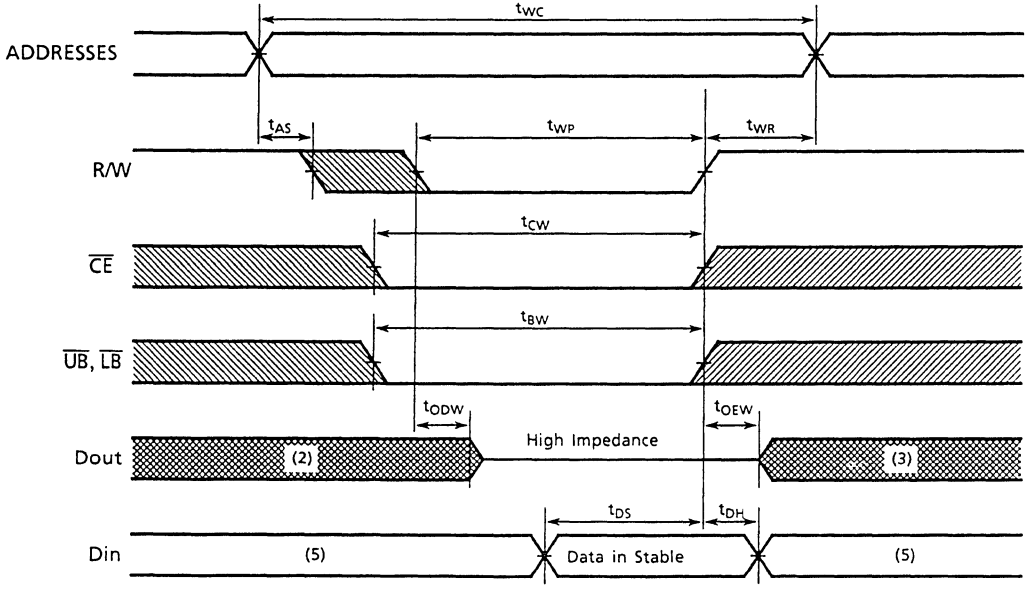
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

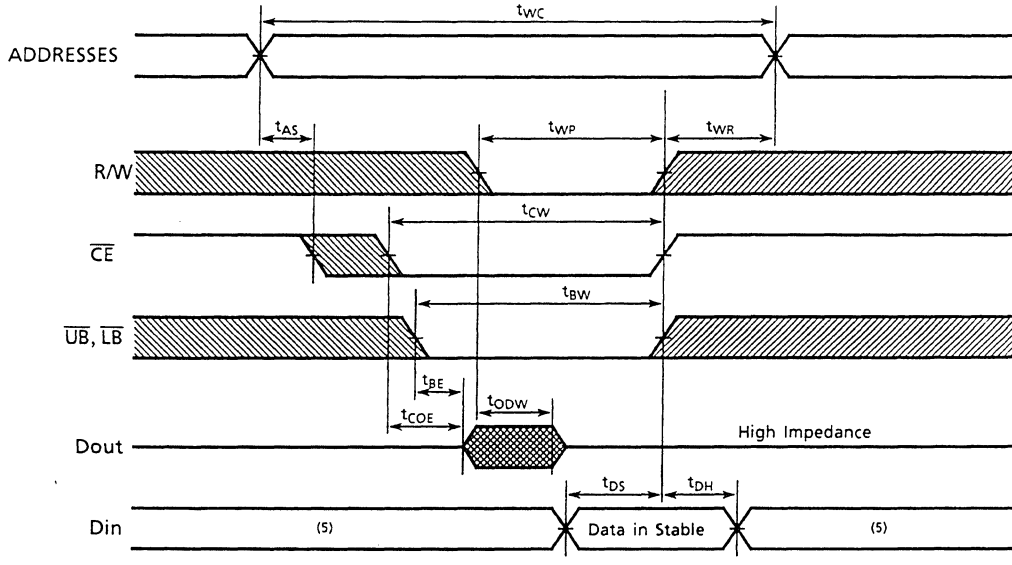
Read Cycle (1)



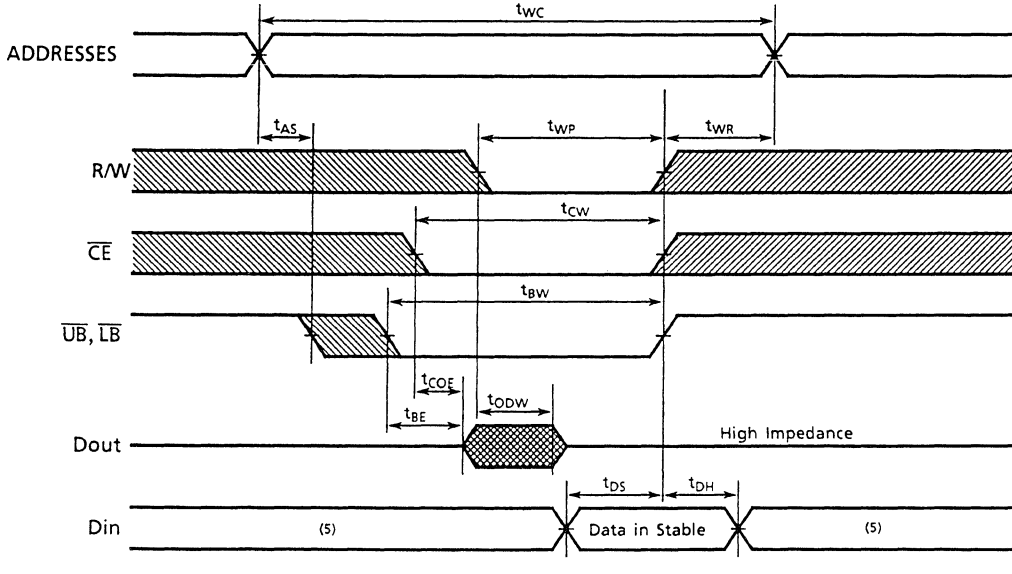
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Write Cycle 3 (4) ($\overline{UB}$, $\overline{LB}$ Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a write cycle, the Outputs are in a high impedance state during this period.

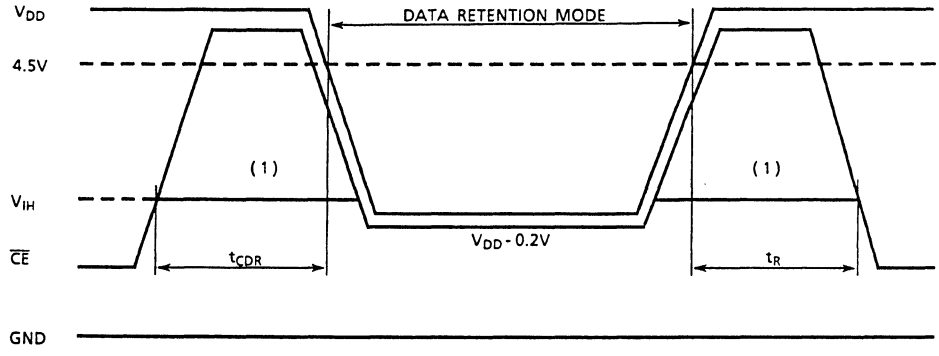
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	30*	µA
		V_{DD} = 5.5V	–	–	60	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*6µA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode



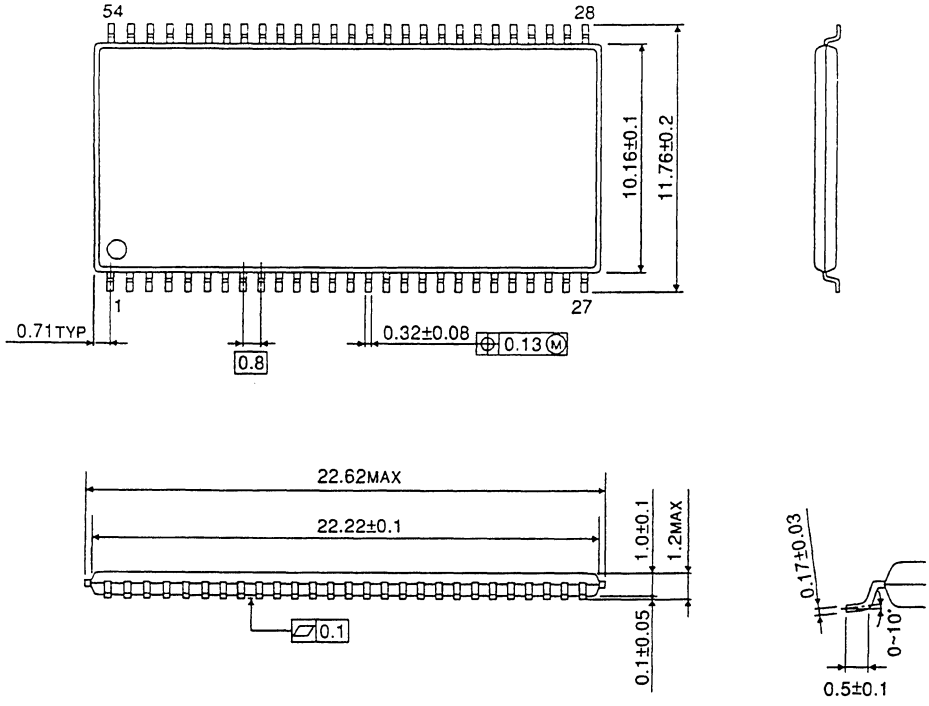
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



Notes

SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTI is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 200μA (max.). The TC554161FTI has two control inputs. A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTI is suitable for use in microprocessor application systems where high speed, low power, battery backup are required, and wide operating temperature system for TC554161FTI guarantees -40 ~ 85°C operating temperature.

The TC554161FTI is offered in a 54-pin thin small outline plastic package.

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 200μA (max.)
- 5V single power supply
- Access time (max.)

	TC554161FTI	
	-85	-10
Access Time	85ns	100ns
$\overline{CE}$ Access Time	85ns	100ns
$\overline{OE}$ Access Time	45ns	50ns

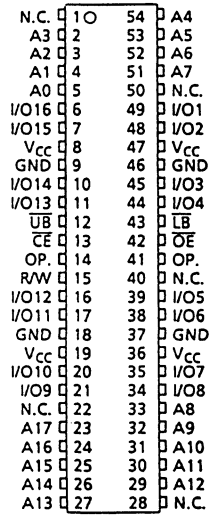
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC554161FTI : TSOP54-P-400
- Wide temperature operating: -40 ~ 85°C

Pin Names

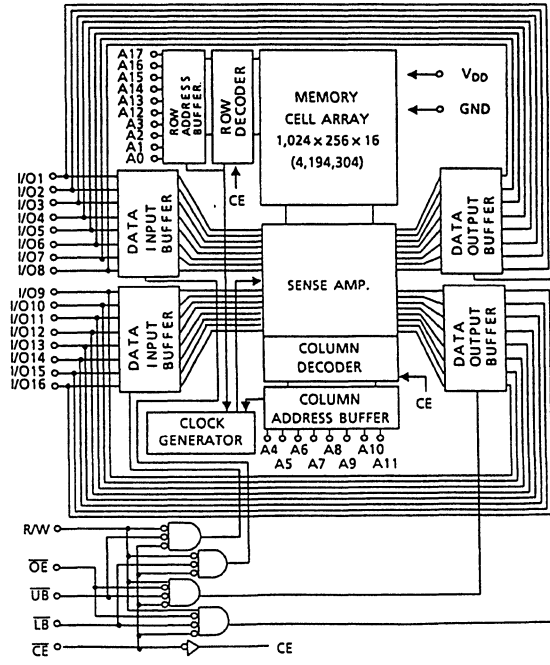
A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP.	Option

* OP. pin must be connected to GND or open.

Pin Connection (Top View)



Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 30ns Max.

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 30ns Max.

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	110	mA
				85ns, 10ns	–	–	100	
				1μs	–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	100	
				85ns, 10ns	–	–	90	
				1μs	–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V			–	–	200	μA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	CE Access Time	–	85	–	100	
t_{OE}	OE Access Time	–	45	–	50	
t_{BA}	UB, LB Access Time	–	45	–	50	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	5	–	5	–	
t_{OEE}	Output Enable Time from OE	0	–	0	–	
t_{BE}	Output Enable Time from UB, LB	0	–	0	–	
t_{OD}	Output Disable Time from CE	–	35	–	40	
t_{ODO}	Output Disable Time from OE	–	35	–	40	
t_{BD}	Output Disable Time from UB, LB	–	35	–	40	

Write Cycle

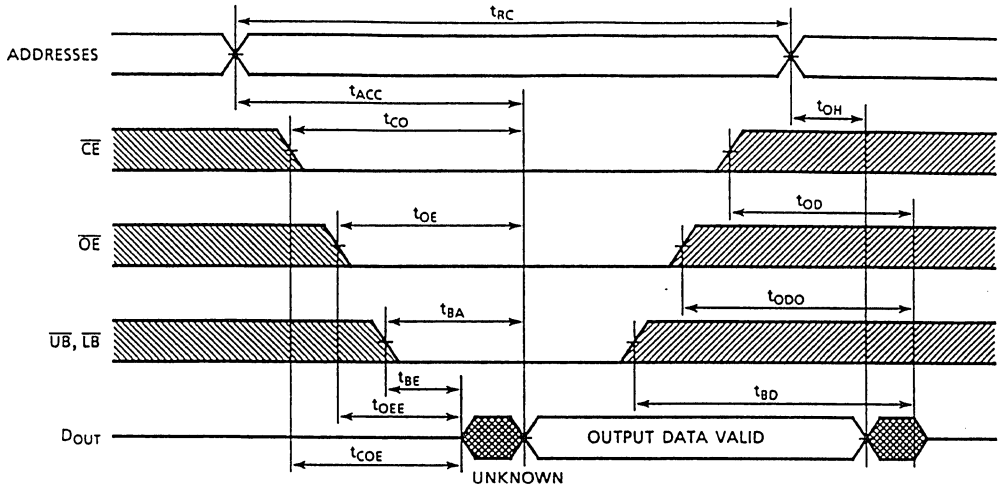
SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	
t_{CW}	Chip Enable to End of Write	70	–	80	–	
t_{BW}	UB, LB Enable to End of Write	55	–	60	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	0	–	
t_{ODW}	Output Disable Time from R/W	–	35	–	40	

AC Test Conditions

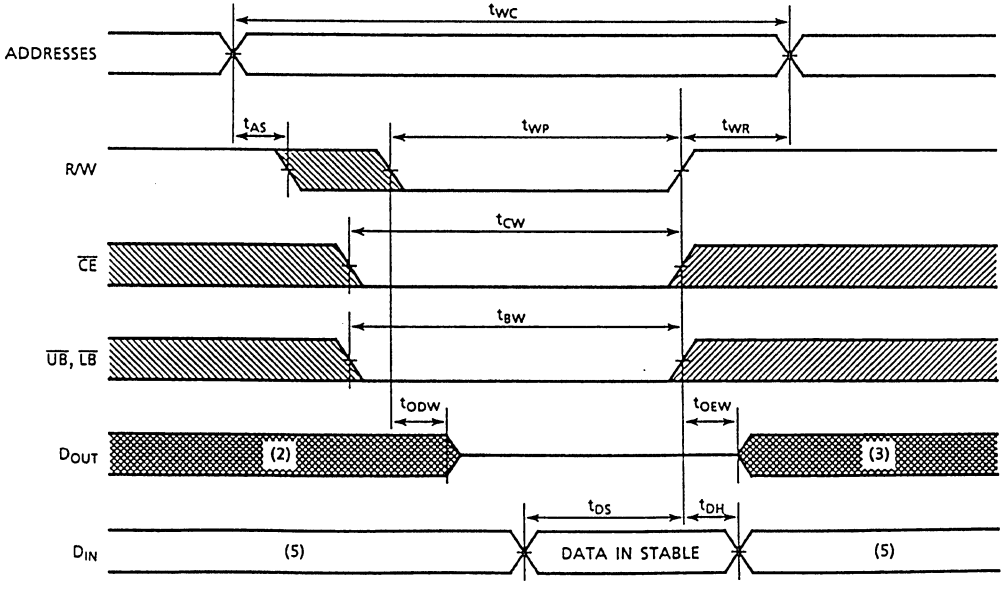
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

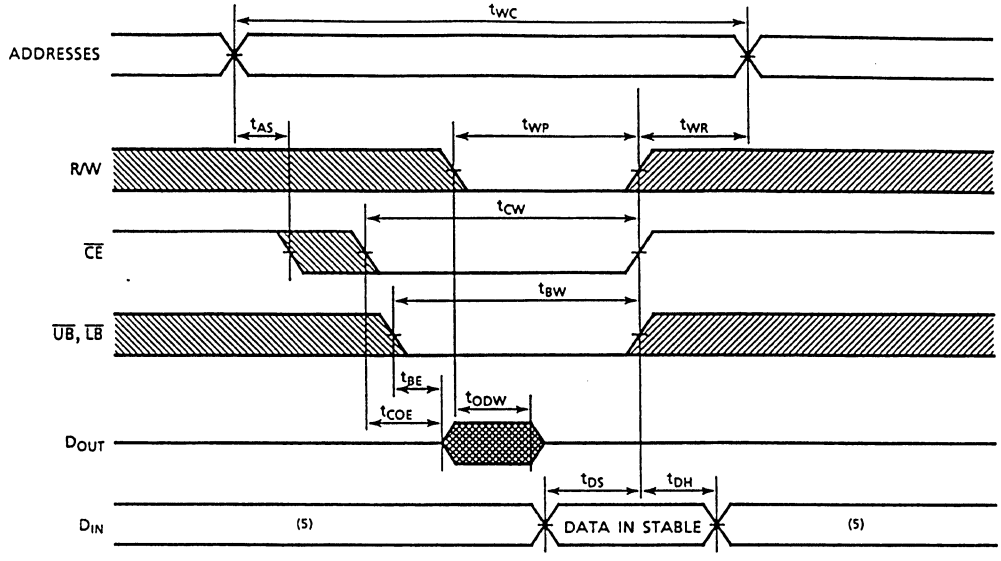
Read Cycle (1)



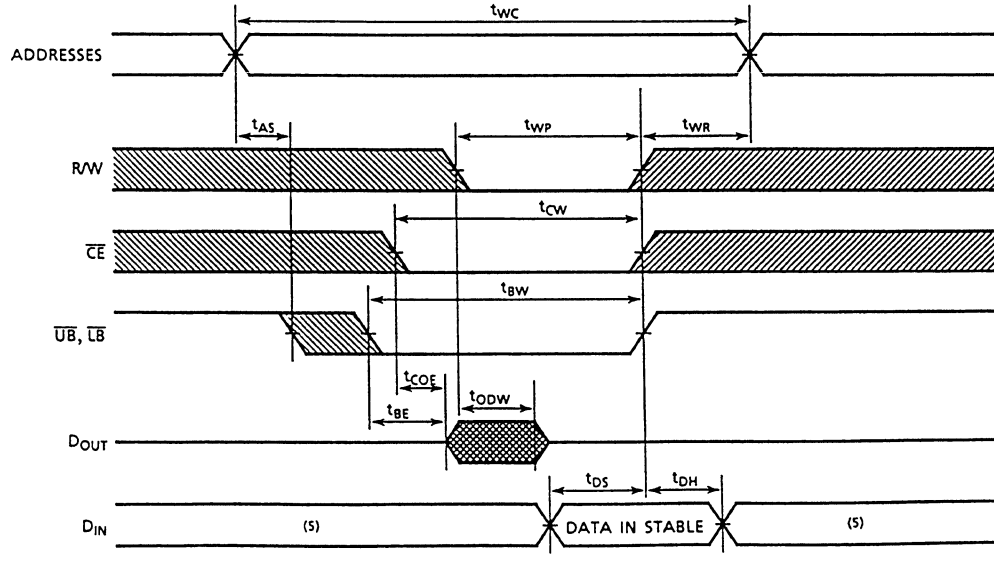
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Write Cycle 3 [4] ($\overline{UB}$, $\overline{LB}$ Controlled Write)



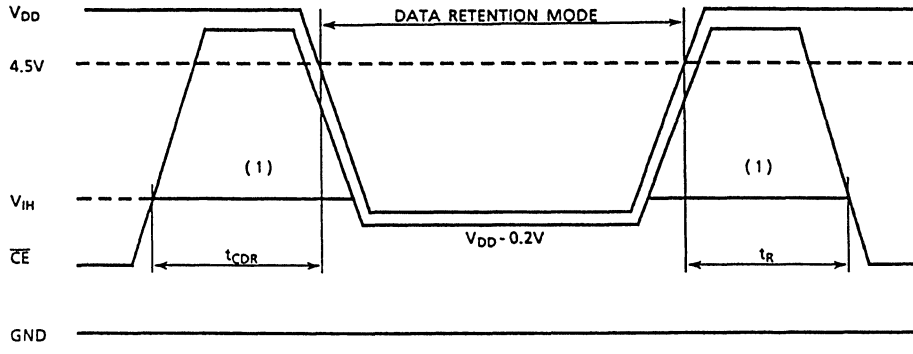
Notes:

1. R/W is High for Read Cycle.
2. Assuming that the $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that is High for a Write Cycle, Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	–	–	100	µA
		V_{DD} = 5.5V	–	–	200	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

$\overline{CE}$ Controlled Data Retention Mode



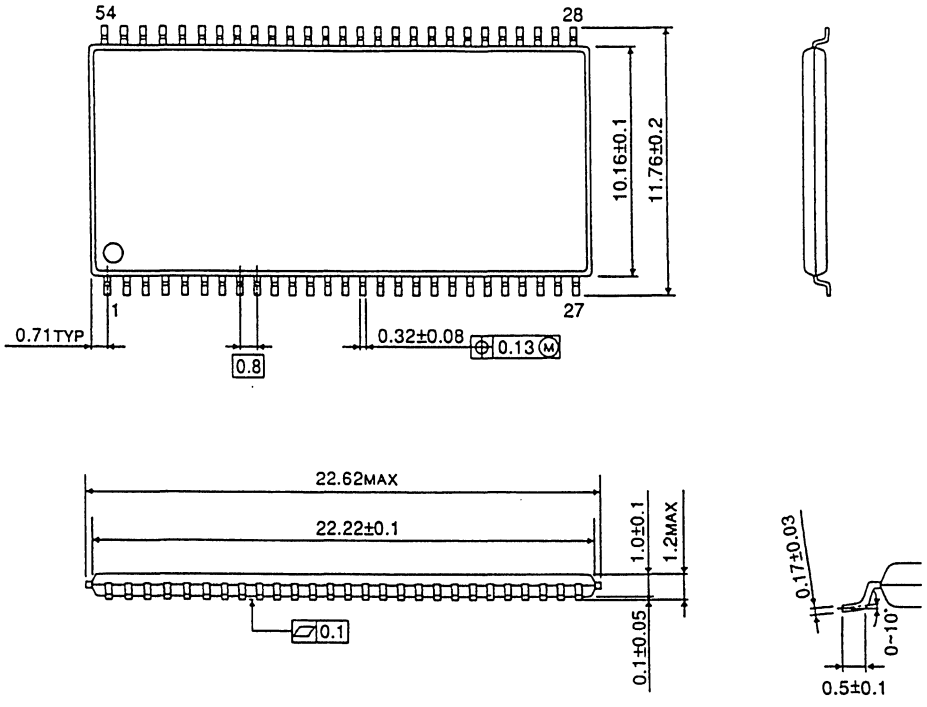
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



Notes

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SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTI is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 140μA (max.). The TC554161FTI has two control inputs. A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTI is suitable for use in microprocessor application systems where high speed, low power battery backup are required, and wide operating temperature.

The TC554161FTI is offered in a 54-pin thin small outline plastic package.

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 8μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC554161FTI	
	-85	-10
Access Time	85ns	100ns
$\overline{CE}$ Access Time	85ns	100ns
$\overline{OE}$ Access Time	45ns	50ns

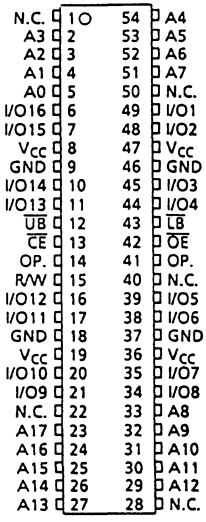
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC554161FTI : TSOP54-P-400
- Wide temperature operation: -40 ~ 85°C

Pin Names

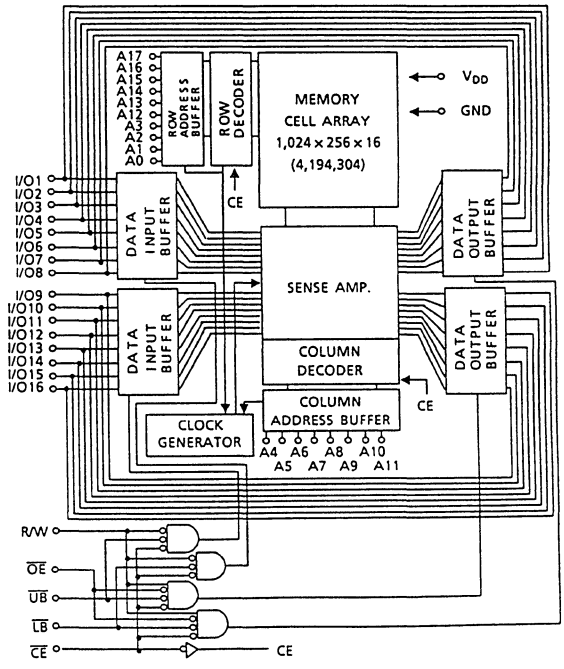
A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP.*	Option

* OP. pin must be connected to GND or open.

Pin Connection (Top View)



Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 30ns Max.

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V with a pulse width of 30ns

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	110	mA
				85ns, 10ns	–	–	100	
				1μs	–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	100	
				85ns, 10ns	–	–	90	
				1μs	–	10	–	
I_{DDS1} I_{DDS2}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C		–	–	140	μA
			Ta = 25°C		–	4	8	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	CE Access Time	–	85	–	100	
t_{OE}	OE Access Time	–	45	–	50	
t_{BA}	UB, LB Access Time	–	45	–	50	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	5	–	5	–	
t_{OEE}	Output Enable Time from OE	0	–	0	–	
t_{BE}	Output Enable Time from UB, LB	0	–	0	–	
t_{OD}	Output Disable Time from CE	–	35	–	40	
t_{ODO}	Output Disable Time from OE	–	35	–	40	
t_{BD}	Output Disable Time from UB, LB	–	35	–	40	

Write Cycle

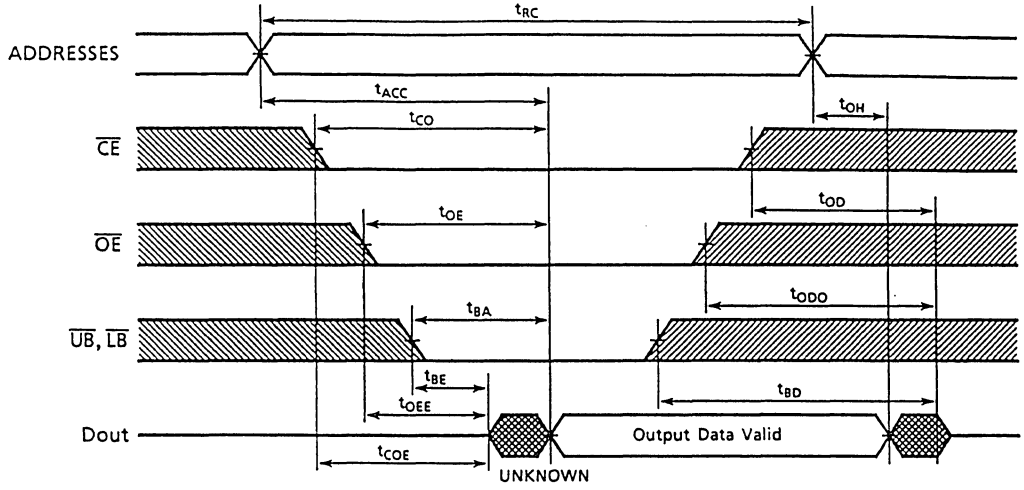
SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85L		-10L		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	
t_{CW}	Chip Enable to End of Write	70	–	80	–	
t_{BW}	UB, LB Enable to End of Write	55	–	60	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	0	–	
t_{ODW}	Output Disable Time from R/W	–	35	–	40	

AC Test Conditions

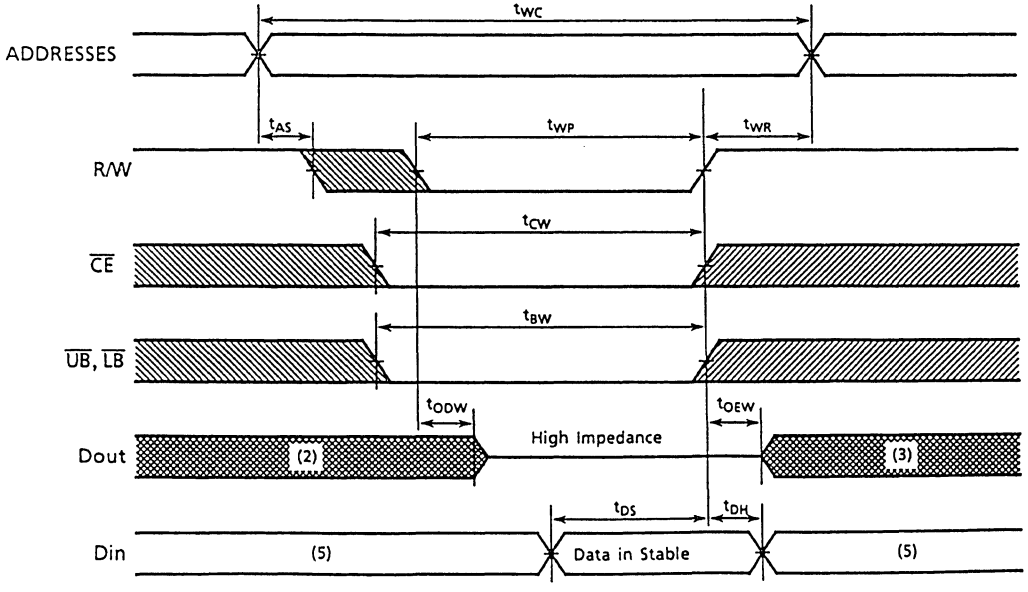
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

Timing Waveforms

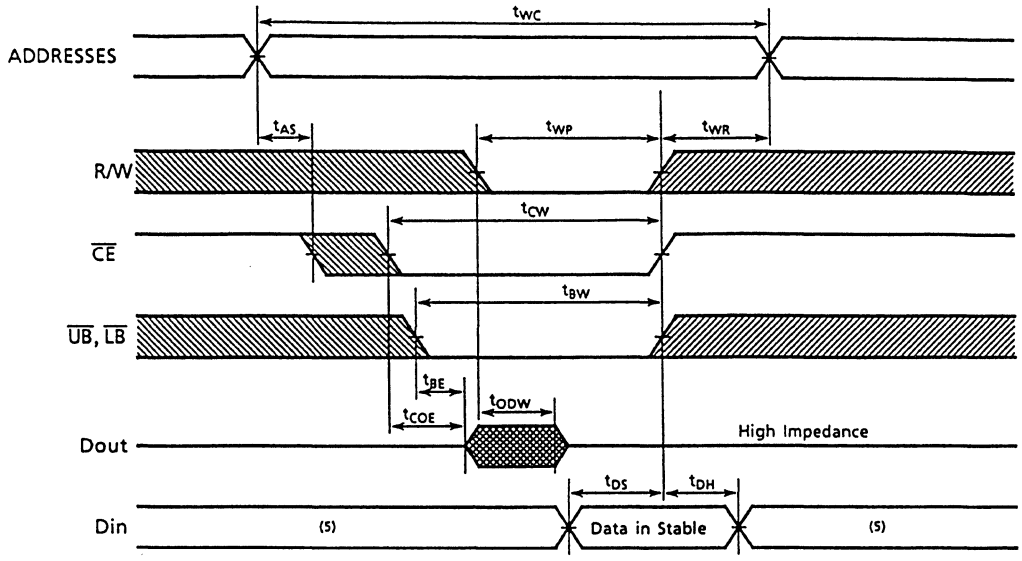
Read Cycle (1)



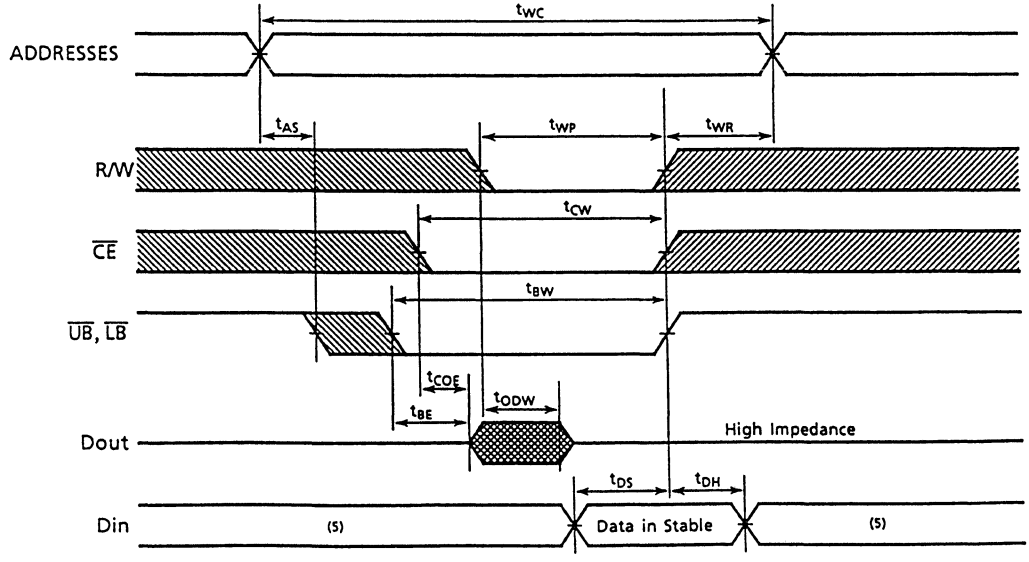
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Write Cycle 3 [4] ($\overline{UB}$, $\overline{LB}$ Controlled Write)



Notes:

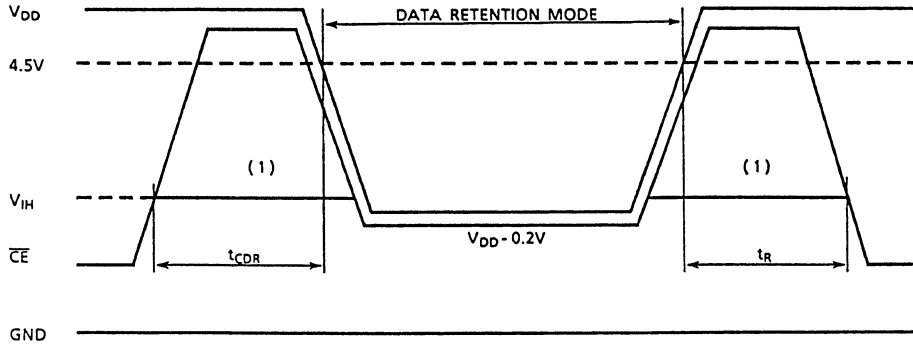
1. R/W is high for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a Write Cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	70*	μA
		V_{DH} = 5.5V	–	–	140	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*6μA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode



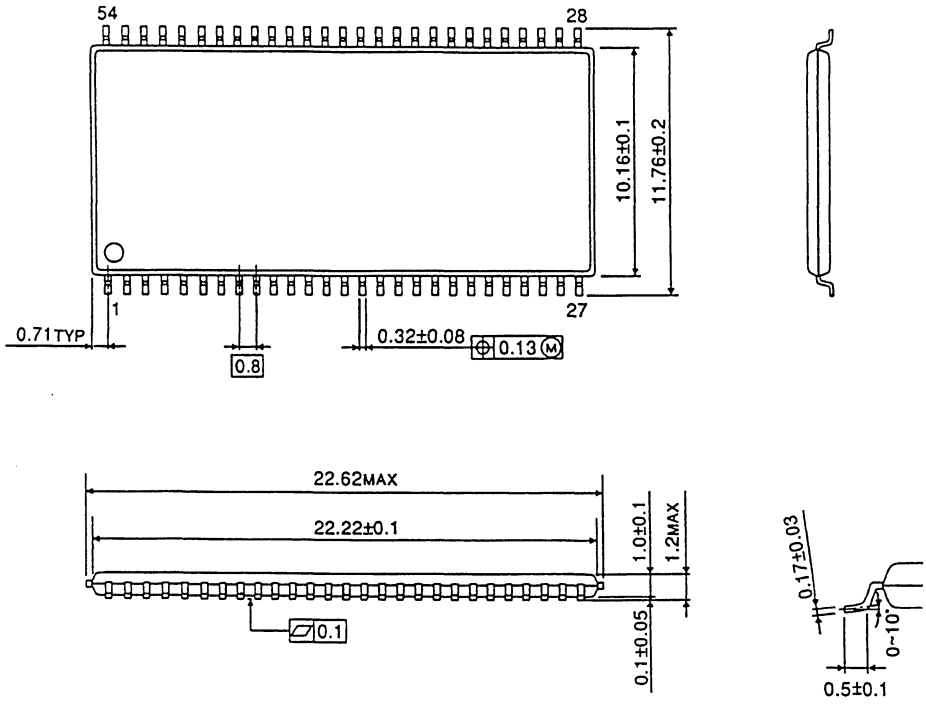
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



Notes

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TC554161FTI-85V/10V

PRELIMINARY

SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTI is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits using CMOS technology, and operated from a single 3.0 ~ 5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 60μA (max.). The TC554161FTI has two control inputs.

A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTI is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC554161FTI is offered in a 54-pin thin small outline plastic package.

Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 8μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	5V±10%		3.0V ~ 5.5V
	-85V	-10V	-85V/-10V
Access Time	85ns	100ns	150ns
$\overline{CE}$ Access Time	85ns	100ns	150ns
$\overline{OE}$ Access Time	45ns	50ns	75ns

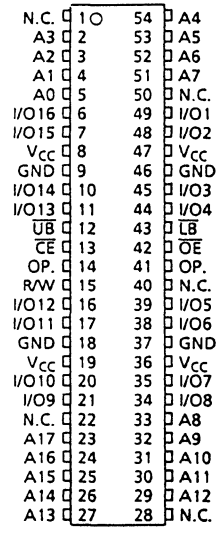
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC554161FTI : TSOP54-P-400
- Wide temperature operation: -40 ~ 85°C

Pin Names

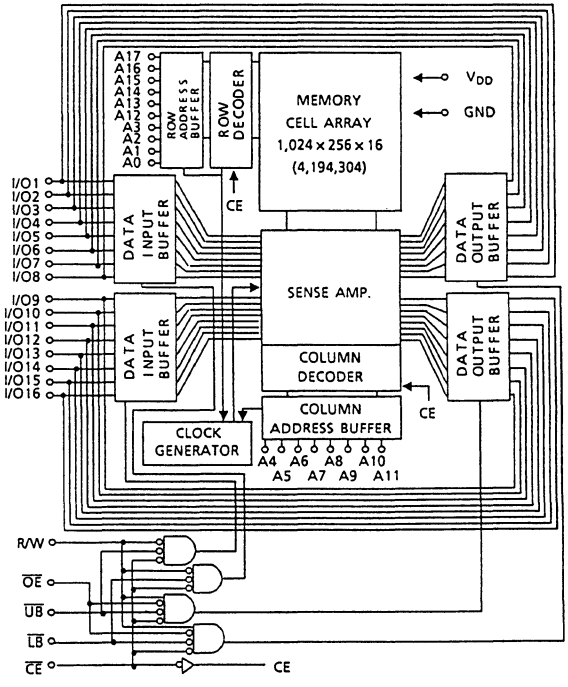
A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP.*	Option

* OP. pin must be connected to GND or ope.

Pin Connection (Top View)



Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V with a pulse width of 30ns

DC Recommended Operating Conditions (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	5V±10%			30% ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	3.0	–	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 0.3	V_{DD} - 0.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V with a pulse width of 30ns

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	100	mA
				1μs	–	15	–	
I_{DDO2}		$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	Min.	–	–	90	
				1μs	–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 2.0V ~ 5.5V	Ta = -40 ~ 85°C	–	–	140	μA
				Ta = 25°C	–	4	8	
			V_{DD} = 3.0V	Ta = -40 ~ 85°C	–	–	70	
				Ta = -40 ~ 40°C	–	–	6	
				Ta = 25°C	–	2	–	

DC and Operating Characteristics (Ta = -40 ~ 85°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	MIN.	–	–	35	mA
				1μs	–	5	–	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 3.3V ± 0.3V	Ta = -40 ~ 85°C	–	–	90	μA
				Ta = 25°C	–	2	4	
			V_{DD} = 3.3V	Ta = -40 ~ 85°C	–	–	80	
				Ta = -40 ~ 40°C	–	–	8	
				Ta = 25°C	–	2	–	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	CE Access Time	–	85	–	100	
t_{OE}	OE Access Time	–	45	–	50	
t_{BA}	UB, LB Access Time	–	45	–	50	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	5	–	5	–	
t_{OEE}	Output Enable Time from OE	0	–	0	–	
t_{BE}	Output Enable Time from UB, LB	0	–	0	–	
t_{OD}	Output Disable Time from CE	–	35	–	40	
t_{ODO}	Output Disable Time from OE	–	35	–	40	
t_{BD}	Output Disable Time from UB, LB	–	35	–	40	

Write Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85V		-10V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	
t_{CW}	Chip Enable to End of Write	70	–	80	–	
t_{BW}	UB, LB Enable to End of Write	55	–	60	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	0	–	
t_{ODW}	Output Disable Time from R/W	–	35	–	40	

AC Test Conditions

Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 3.0V ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO}	CE Access Time	–	150	
t_{OE}	OE Access Time	–	75	
t_{BA}	UB, LB Access Time	–	75	
t_{OH}	Output Data Hold Time from Address Change	10	–	
t_{COE}	Output Enable Time from CE	5	–	
t_{OEE}	Output Enable Time from OE	0	–	
t_{BE}	Output Enable Time from UB, LB	0	–	
t_{OD}	Output Disable Time from CE	–	50	
t_{ODO}	Output Disable Time from OE	–	50	
t_{BD}	Output Disable Time from UB, LB	–	50	

Write Cycle

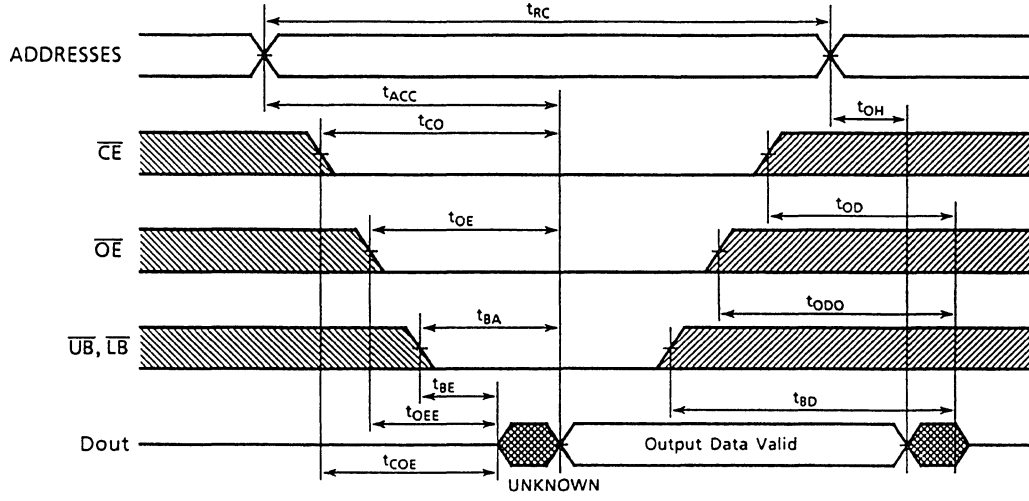
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Enable to End of Write	120	–	
t_{BW}	UB, LB Enable to End of Write	100	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	
t_{OEW}	Output Enable Time from R/W	0	–	
t_{ODW}	Output Disable Time from R/W	–	50	

AC Test Conditions

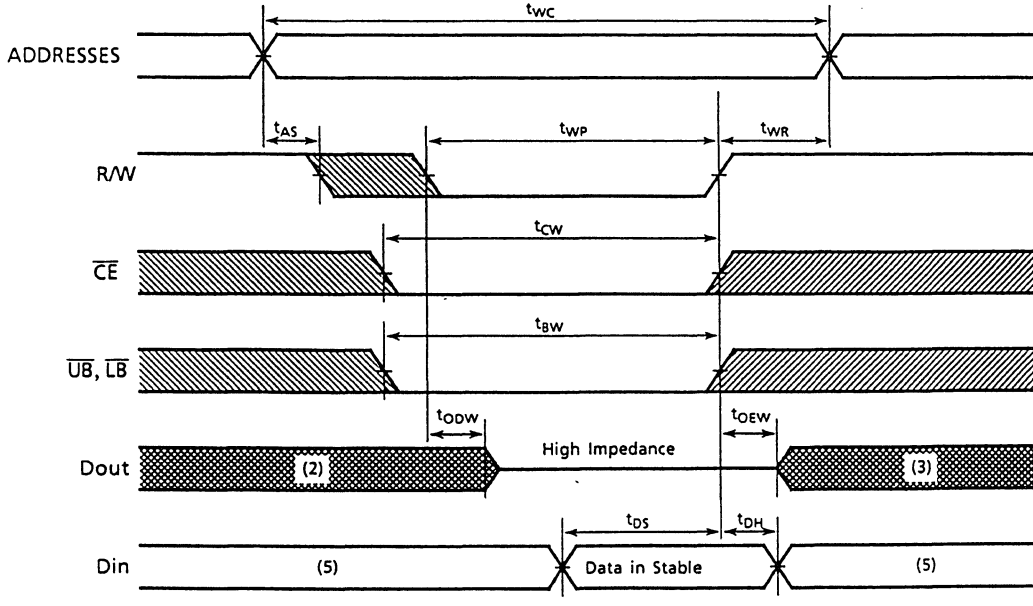
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	100pF (Include Jig)

Timing Waveforms

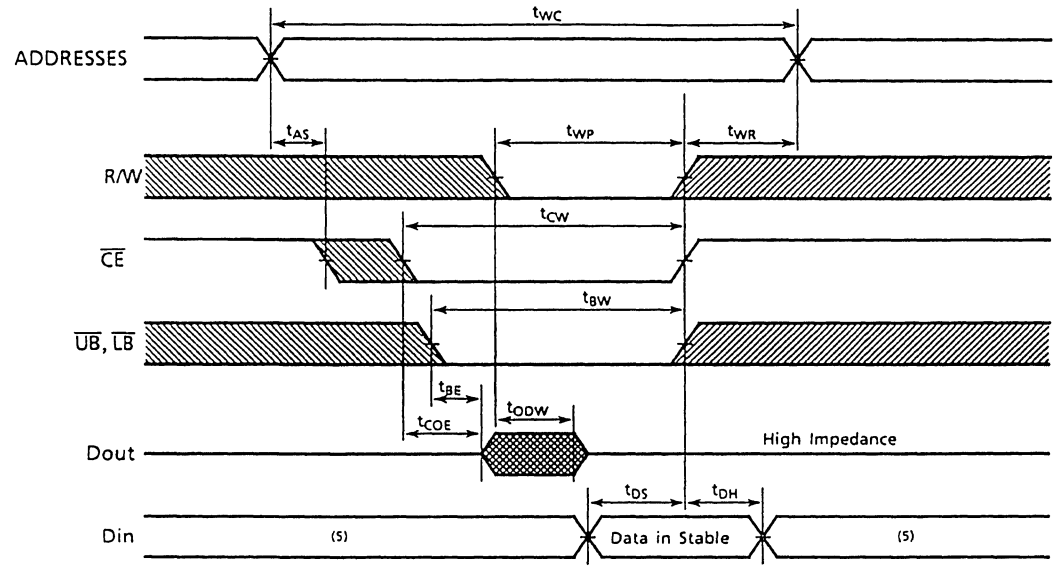
Read Cycle (1)



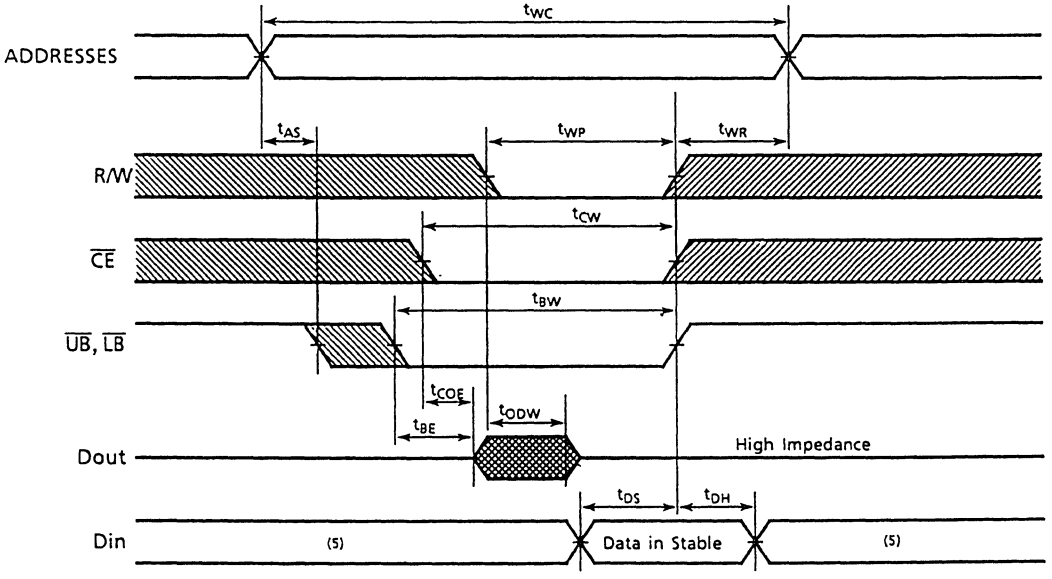
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Write Cycle 3 [4] ($\overline{UB}$, $\overline{LB}$ Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a write cycle, the Outputs are in a high impedance state during this period.

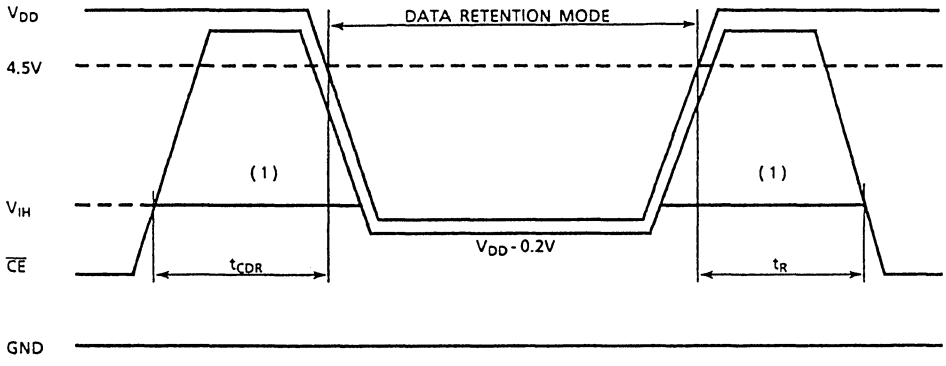
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.3V	–	–	80*	μA
		V_{DH} = 5.5V	–	–	140	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*8μA (max.) Ta = -40 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode



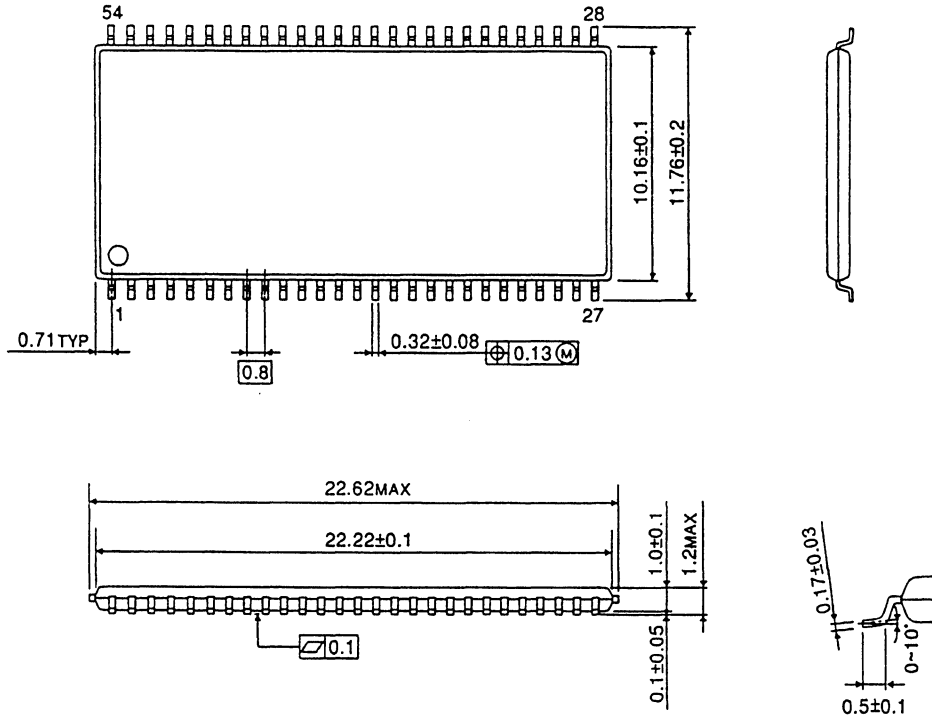
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



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SILICON GATE CMOS

262,144 WORD x 16 BIT STATIC RAM

Description

The TC554161FTL is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits a using CMOS technology, and operated from a single 3.0 ~ 5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (typ.) and a minimum cycle time of 70ns. When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 4μA (max.). The TC554161FTL has two control inputs.

A Chip Enable input ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC554161FTL is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The TC554161FTL is offered in a 54-pin thin small outline plastic package.

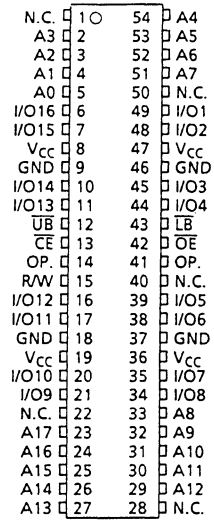
Features

- Low power dissipation: 55mW/MHz (typ.)
- Standby current: 8μA (max.) at Ta = 25°C
- Single power supply: 3.0 ~ 5.5V
- Access time (max.)

	5V±10%		3.0V ~ 5.5V
	-70V	-85V	-70V/-85V
Access Time	70ns	85ns	150ns
$\overline{CE}$ Access Time	70ns	85ns	150ns
$\overline{OE}$ Access Time	35ns	45ns	75ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package TC554161FTL : TSOP54-P-400

Pin Connection (Top View)

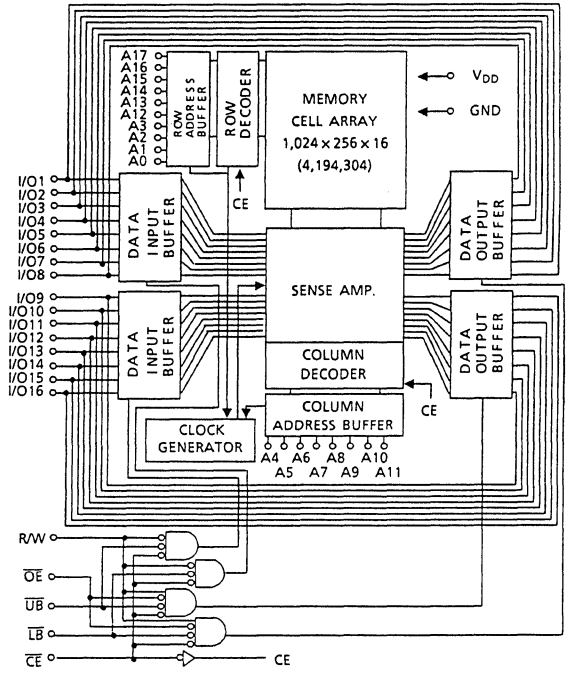


Pin Names

A0 ~ A17	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
OP. *	Option

* OP. pin must be connected to GND or open.

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O8	I/O9 ~ I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Deselect	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width of 30ns Max.

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	5V ±10%			3.0 ~ 5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	3.0	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V_{DD} - 2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	-0.3*	–	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	2.0	–	5.5	

* -3.0V at pulse width 30ns Max.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	110	mA
				85ns	–	–	100	
				1µs	–	15	–	
I_{DDO2}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Inputs = V_{IH}/V_{IL}	t_{cycle}	70ns	–	–	100	mA
				85ns	–	–	90	
				1µs	–	10	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}			–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} - 0.2V ~ 5.5V	Ta = 0 ~ 70°C	–	–	60	µA
				Ta = 25°C	–	4	8	
			V_{DD} - 3.0V	Ta = 0 ~ 70°C	–	–	30	
				Ta = 0 ~ 40°C	–	–	6	
				Ta = 25°C	–	2	–	

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}			–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2V, V_{DD} - 0.2V, I_{OUT} = 0mA Other Inputs = V_{DD} - 0.2V/0.2V	t_{cycle}	MIN.	–	–	35	mA
				1µs	–	5	–	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} - 0.2V	V_{DD} = 3.3V ±0.3V	Ta = 0 ~ 70°C	–	–	40	µA
				Ta = 25°C	–	2	4	
			V_{DD} = 3.3V	Ta = 0 ~ 70°C	–	–	35	
				Ta = 0 ~ 40°C	–	–	8	
				Ta = 25°C	–	2	–	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	85	–	ns
t_{ACC}	Address Access Time	–	70	–	85	
t_{CO}	CE Access Time	–	70	–	85	
t_{OE}	OE Access Time	–	35	–	45	
t_{BA}	UB, LB Access Time	–	35	–	45	
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	
t_{COE}	Output Enable Time from CE	10	–	10	–	
t_{OEE}	Output Enable Time from OE	5	–	5	–	
t_{BE}	Output Enable Time from UB, LB	5	–	5	–	
t_{OD}	Output Disable Time from CE	–	25	–	30	
t_{ODO}	Output Disable Time from OE	–	25	–	30	
t_{BD}	Output Disable Time from UB, LB	–	25	–	30	

Write Cycle

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-70V		-85V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	ns
t_{WP}	Write Pulse Width	50	–	55	–	
t_{CW}	Chip Enable to End of Write	60	–	70	–	
t_{BW}	UB, LB Enable to End of Write	50	–	55	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	30	–	35	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from R/W	5	–	5	–	
t_{ODW}	Output Disable Time from R/W	–	25	–	30	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 100pF

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.0 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO}	CE Access Time	–	150	
t_{OE}	OE Access Time	–	75	
t_{BA}	UB, LB Access Time	–	75	
t_{OH}	Output Data Hold Time from Address Change	10	–	
t_{COE}	Output Enable Time from CE	10	–	
t_{OEE}	Output Enable Time from OE	5	–	
t_{BE}	Output Enable Time from UB, LB	5	–	
t_{OD}	Output Disable Time from CE	–	50	
t_{ODO}	Output Disable Time from OE	–	50	
t_{BD}	Output Disable Time from UB, LB	–	50	

Write Cycle

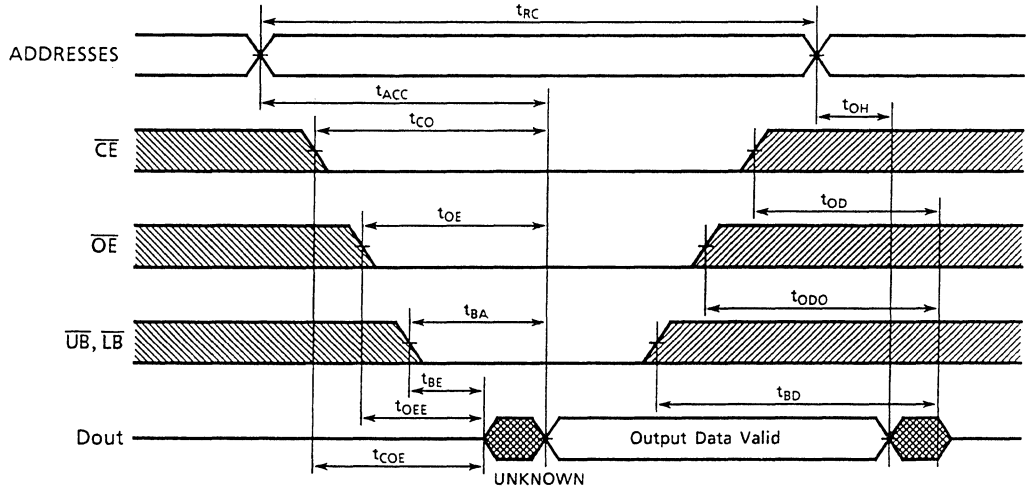
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Enable to End of Write	120	–	
t_{BW}	UB, LB Enable to End of Write	100	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	
t_{OEW}	Output Enable Time from R/W	5	–	
t_{ODW}	Output Disable Time from R/W	–	50	

AC Test Conditions

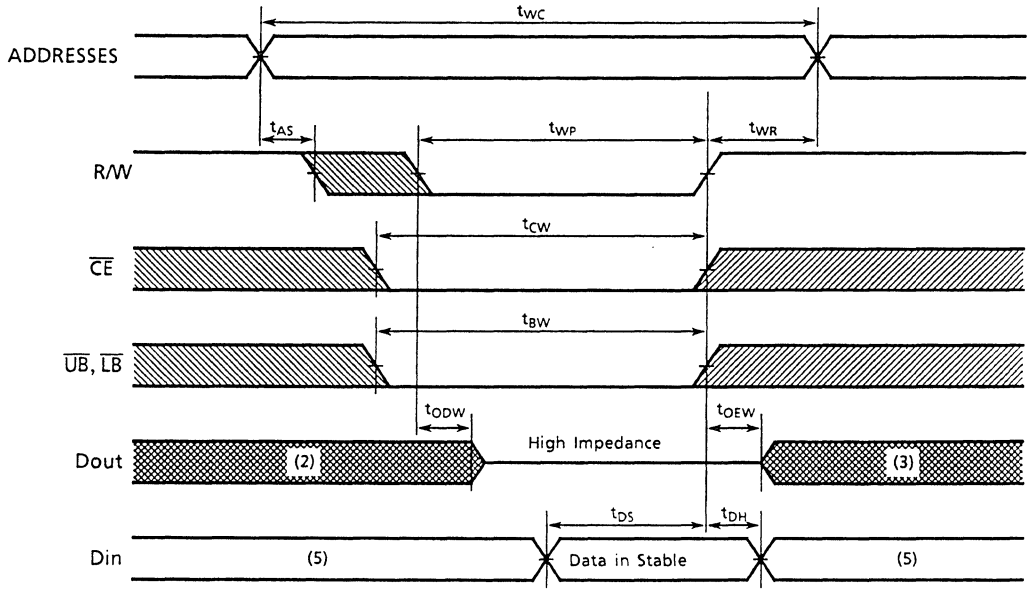
Input Pulse Levels	V_{DD} - 0.2V/0.2V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	100pF (Include Jig)

Timing Waveforms

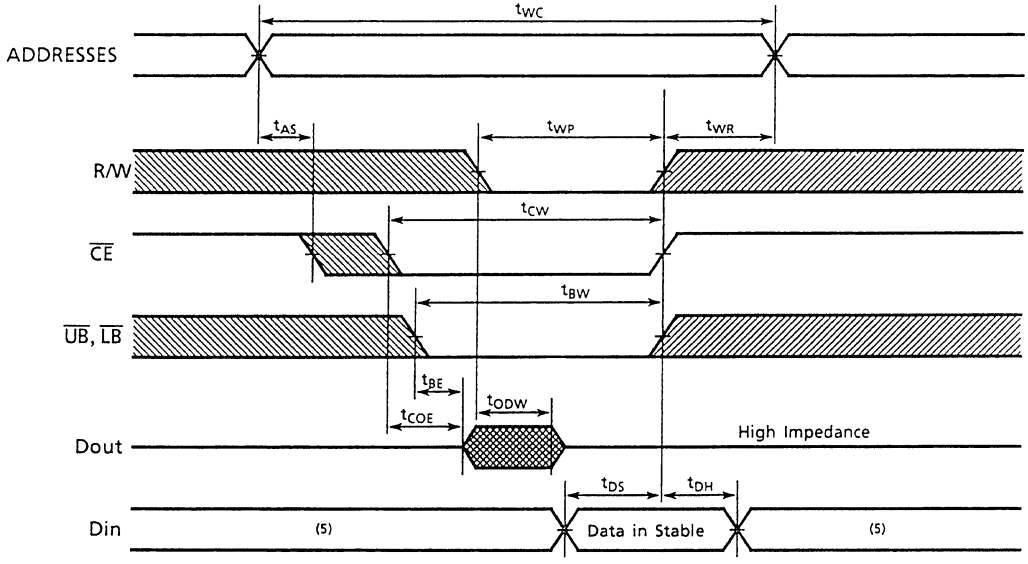
Read Cycle (1)



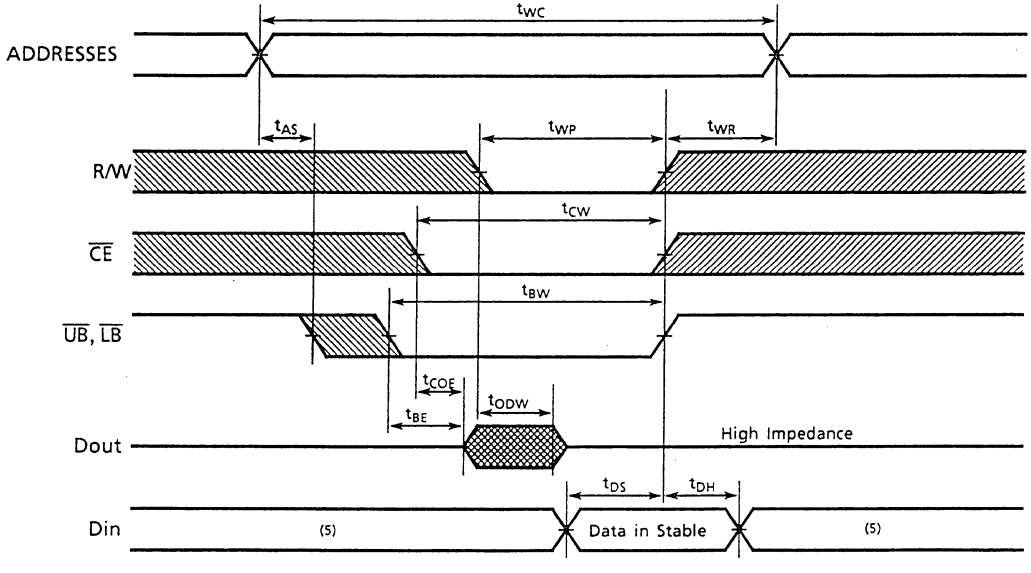
Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Write Cycle 3 (4) ($\overline{UB}$, $\overline{LB}$ Controlled Write)



Notes:

1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, Outputs are in a high impedance state during this period.

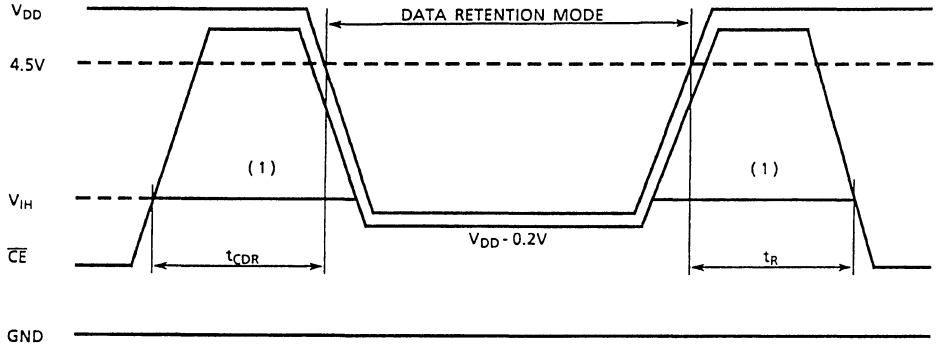
5. The I/O may be in the output state during this time, input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.3V	–	–	35*	µA
		V_{DD} = 5.5V	–	–	60	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		5	–	–	ms

*8µA (max.) Ta = 0 ~ 40°C

$\overline{CE}$ Controlled Data Retention Mode



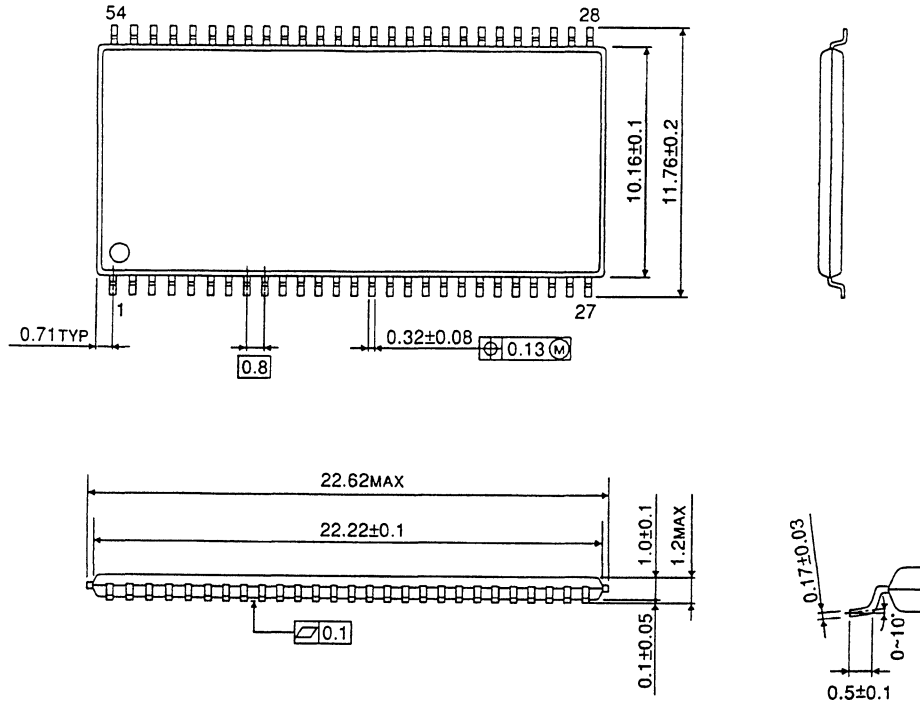
Note:

1. If the V_{IH} of $\overline{CE}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

Outline Drawing

TSOP54-P-400

Unit in mm



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High Speed SRAM

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS STATIC RAM

Description

The TC55V328AJ is a 262,144 bits high speed static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 3.3-volt supply. Toshiba's CMOS technology and advanced circuit form provide low voltage operation and high speed feature.

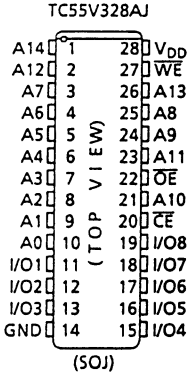
The TC55V328AJ has low power feature with device control using Chip Enable ($\overline{CE}$) and has an Output Enable Input ($\overline{OE}$) for fast memory access. The TC55V328AJ is suitable for use in cache memory where high speed is required, and high speed storage. All inputs and outputs are LVTTL compatible.

The TC55V328AJ is packaged in a 28-pin standard SOJ with 300mil width for high density surface assembly.

Features

- Fast access time
  - TC55V328AJ-15 15ns (max.)
  - TC55V328AJ-17 17ns (max.)
  - TC55V328AJ-20 20ns (max.)
- Low power dissipation
  - Operation:
  - TC55V328AJ-15 100mA (max.)
  - TC55V328AJ-17 100mA (max.)
  - TC55V328AJ-20 90mA (max.)
  - Standby: 300μA (max.)
- Fully static operation
- 3.3V single power supply: 3.3V ±0.3V
- Output buffer control: $\overline{OE}$
- All inputs and outputs:
  - LVTTL compatible
- Package:
  - TC55V328AJ: SOJ28-P-300A

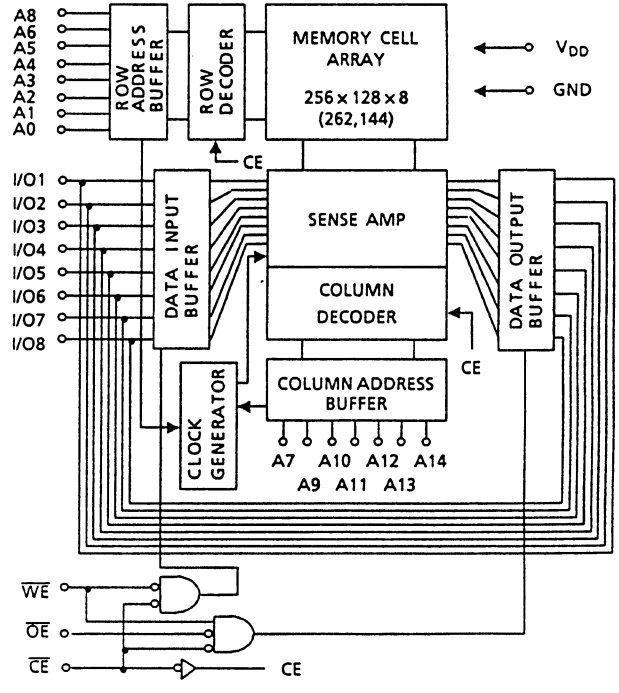
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+3.3V)
GND	Ground

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 ~ I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* High or Low

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V_{IN}	Input Voltage	-0.5* ~ 4.6	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5**	V
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -2.0V with a pulse width of 10ns
**V_{DD} + 1.5V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage	-0.3*	–	0.8	V

* -1.5V with a pulse width of 10ns
**V_{DD} + 1.0V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0 ~ V_{DD}		–	–	±1	μA
V_{OH}	Output High Voltage	I_{OH} = -2mA		2.4	–	–	V
		I_{OH} = -100μA		V_{DD} - 0.2	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		–	–	0.4	V
		I_{OL} = 100μA		–	–	0.2	V
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, I_{OUT} = 0 mA	-15	–	–	100	mA
			-17	–	–	100	
			-20	–	–	90	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min cycle		–	–	20	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	300	μA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

Read Cycle

SYMBOL	PARAMETER	TC55V328AJ-15		TC55V328AJ-17		TC55V328AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	17	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	17	–	20	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	17	–	20	
t_{OE}	$\overline{OE}$ Access Time	–	7	–	7	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC55V328AJ-15		TC55V328AJ-17		TC55V328AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	17	–	20	–	ns
t_{WP}	Write Pulse Width	10	–	10	–	13	–	
t_{AW}	Address Valid to End of Write	10	–	10	–	13	–	
t_{CW}	Chip Enable to End of Write	11	–	11	–	13	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Setup Time	8	–	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

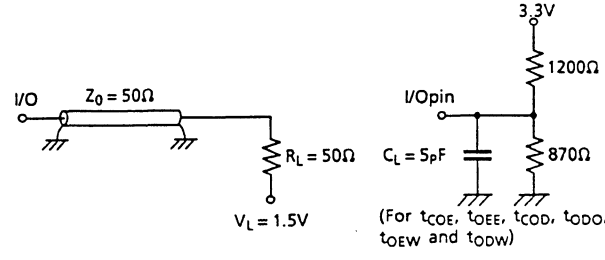
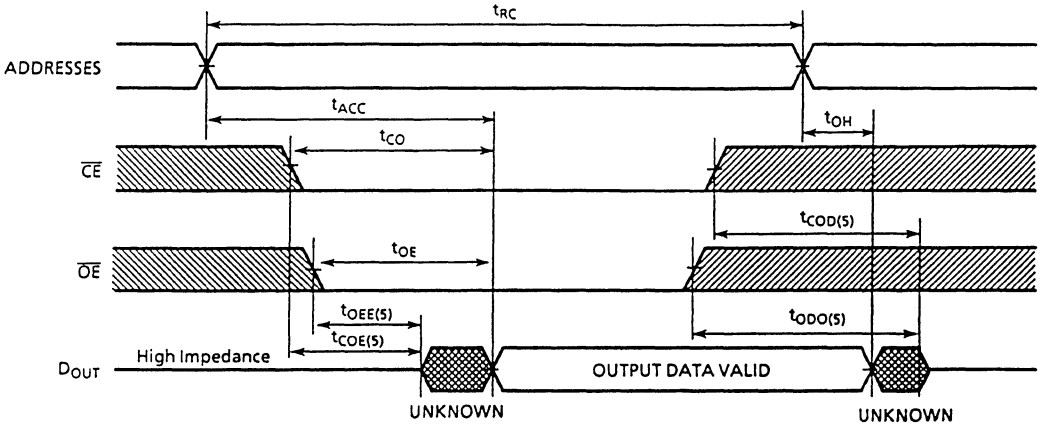


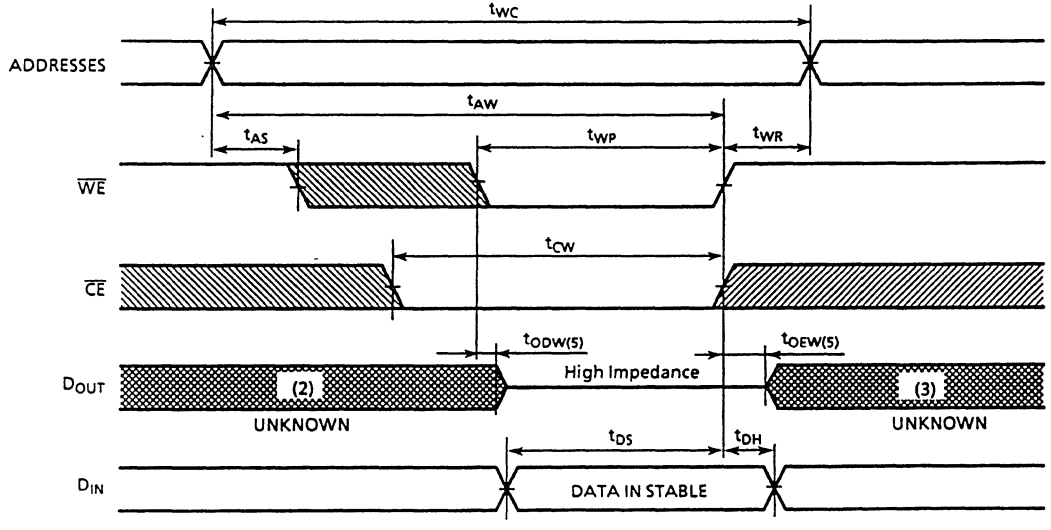
Figure 1.

Timing Waveforms

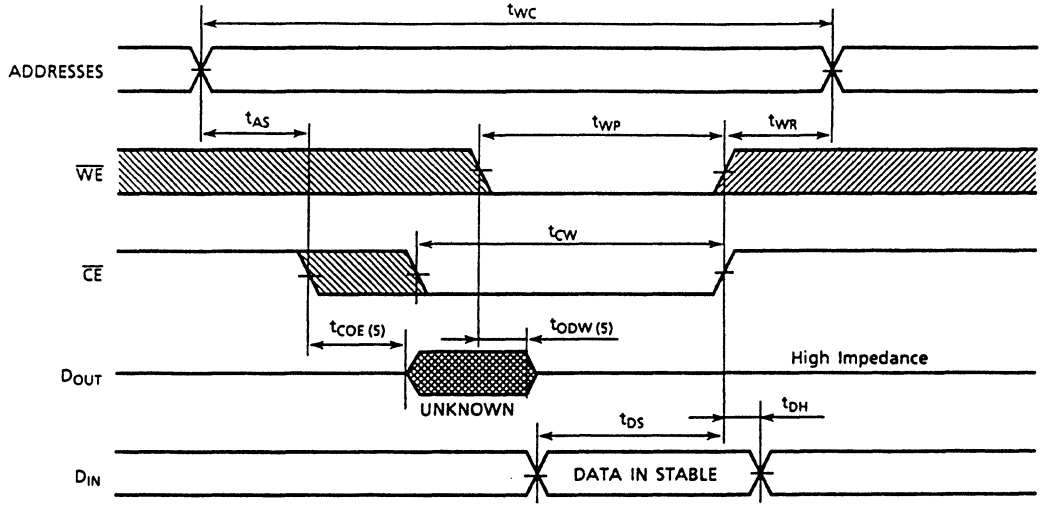
Read Cycle (1)



Write Cycle 1 (4) ($\overline{WE}$ Controlled Write)



Write Cycle 2 (4) ($\overline{CE}$ Controlled Write)



Notes:

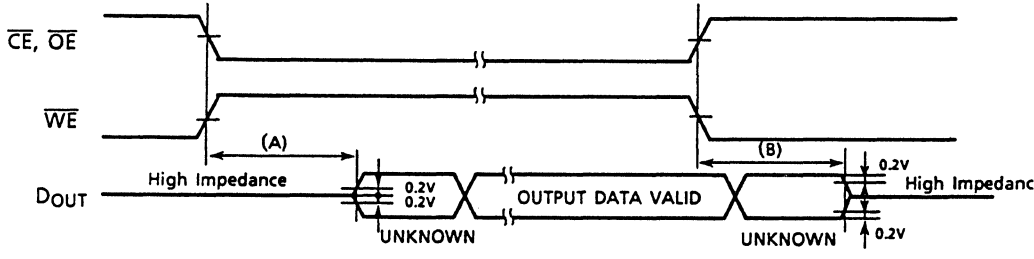
1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

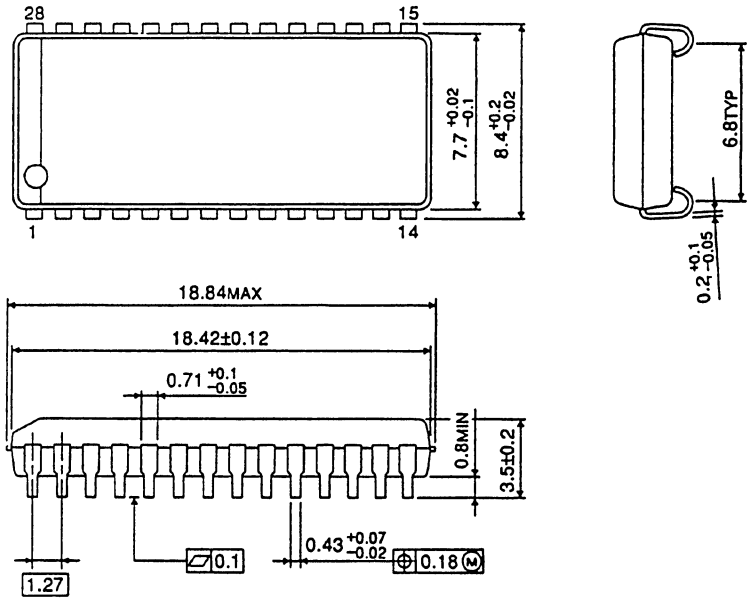
4. Assuming that $\overline{OE}$ is High for a Write Cycle, the Outputs are in a high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings **Unit in mm**

Plastic SOJ (SOJ28-P-300A)



Weight: 083g (Typ.)

Notes

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TC558128AJ-15/20

PRELIMINARY

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS STATIC RAM

Description

The TC558128AJ is a 1,048,576 bits high speed static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature. The TC558128AJ has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable input ($\overline{OE}$) for fast memory access.

The TC558128AJ is suitable for use in cache memory where high speed is required and high speed storage. All Inputs and Outputs are TTL compatible.

The TC558128AJ is packaged in a 32-pin plastic SOJ with 400mil width for high density surface assembly.

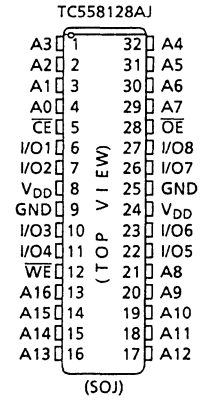
Features

- Fast access time
  - TC558128AJ-15 15ns (max.)
  - TC558128AJ-20 20ns (max.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (max.)	170	140	130	120	100	mA

  - Standby: 1mA (max.)
- 5V single power supply: 5V±10%
- Fully static operation
- All nputs and outputs: TTL compatible
- Output buffer control: $\overline{OE}$
- Package:
  - TC558128AJ: SOJ32-P-400A

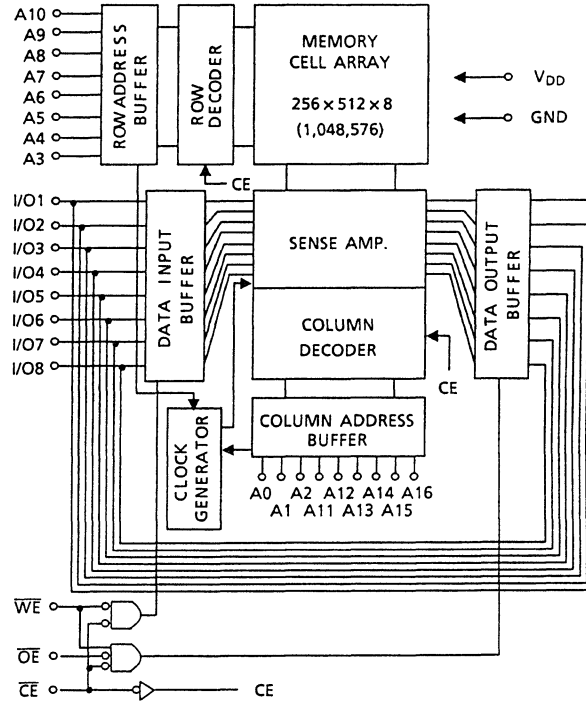
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disabled	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.1	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	t_{cycle} = 15ns	–	–	170	mA
			t_{cycle} = 20ns	–	–	140	
			t_{cycle} = 25ns	–	–	130	
			t_{cycle} = 30ns	–	–	120	
			t_{cycle} = 50ns	–	–	100	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V, Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C(1), V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC558128AJ-15		TC558128AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	20	
t_{CO}	Chip Enable Access Time	–	15	–	20	
t_{OE}	Output Enable Access Time	–	8	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC558128AJ-15		TC558128AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	
t_{AW}	Address Valid to End of Write	12	–	13	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

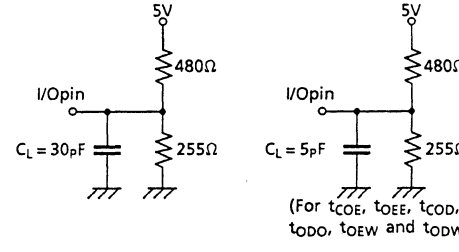
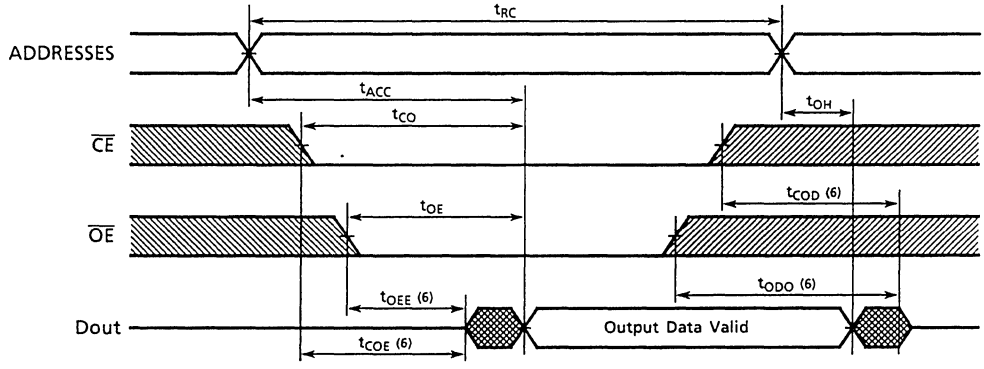


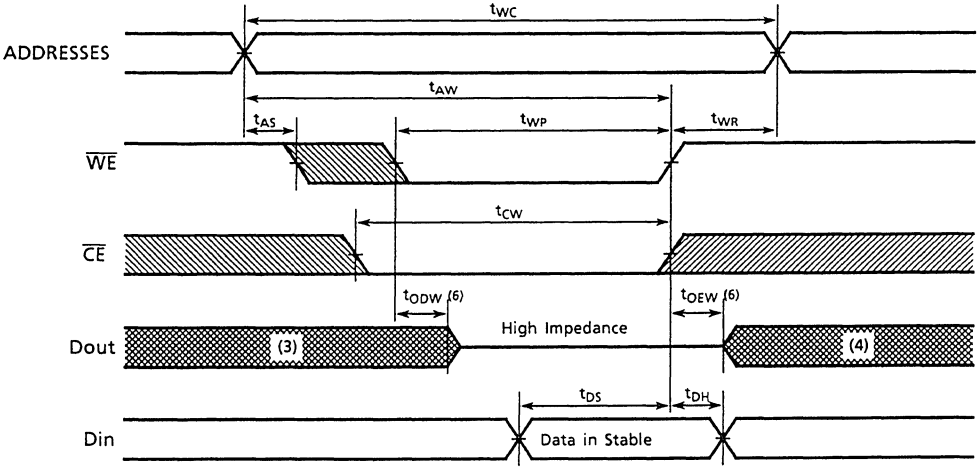
Figure 1.

Timing Waveforms

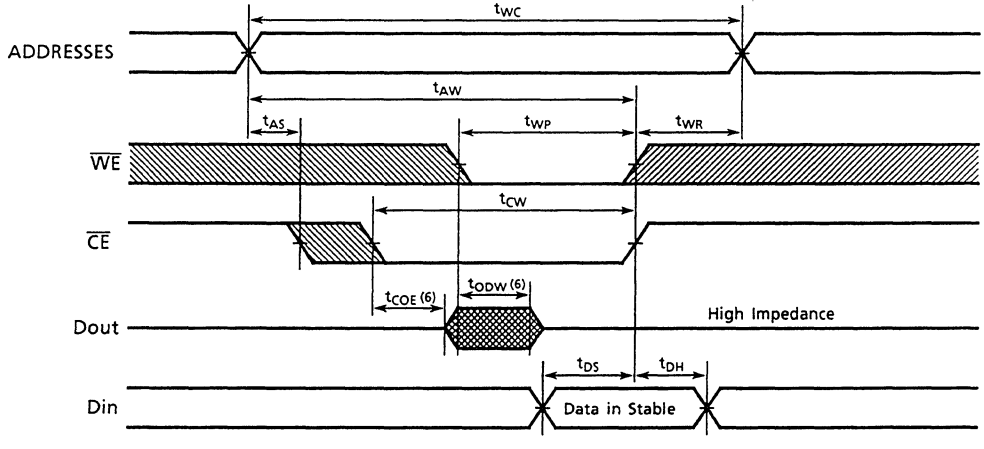
Read Cycle (2)



Write Cycle 1 (5) ($\overline{WE}$ Controlled)



Write Cycle 2 (5) ($\overline{CE}$ Controlled)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

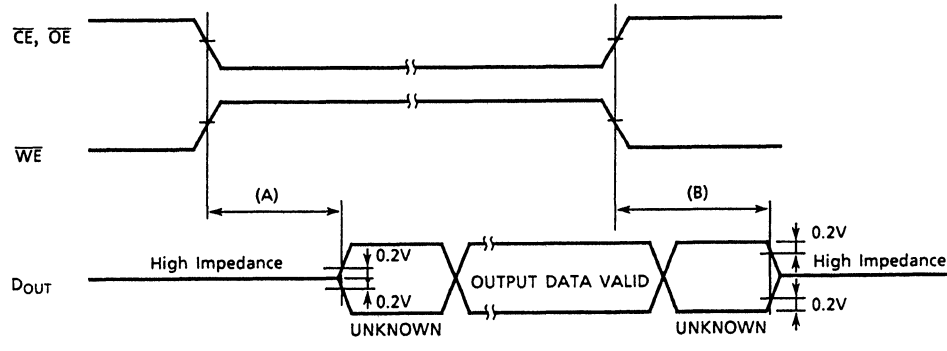
2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

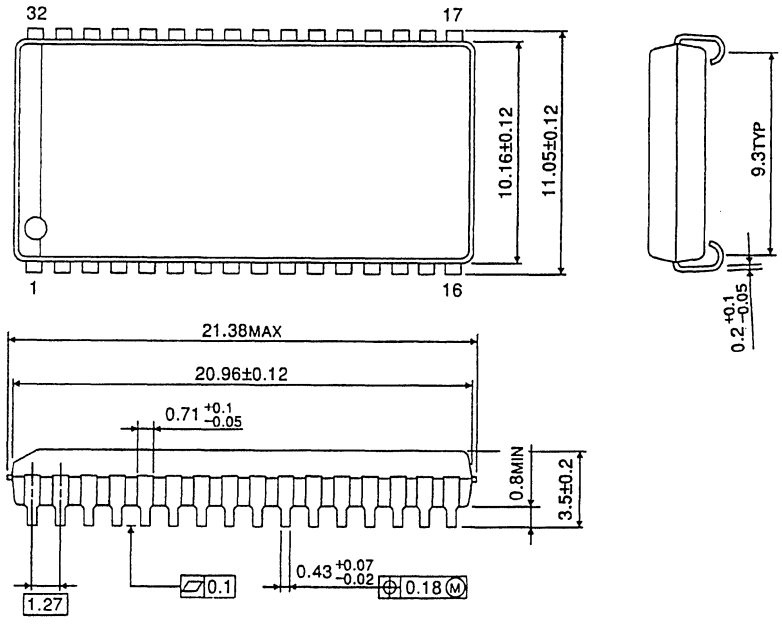
5. Assuming that $\overline{OE}$ is High during a Write Cycle, the Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings **Unit in mm**

Plastic SOJ (SOJ32-P-400A)



Weight : 1.22g (Typ.)

Notes

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TC559128AJ-15/20

PRELIMINARY

SILICON GATE CMOS

131,072 WORD x 9 BIT CMOS STATIC RAM

Description

The TC559128AJ is a 1,179,648 bits high speed static random access memory organized as 131,072 words by 9 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature. The TC559128AJ has low power feature with device control using Chip Enable ($\overline{CE}$), and has an Output Enable input ($\overline{OE}$) for fast memory access.

The TC559128AJ is suitable for use in cache memory where high speed is required and high speed storage. All inputs and outputs are TTL compatible.

The TC559128AJ is packaged in a 36-pin plastic SOJ with 400mil width for high density surface assembly.

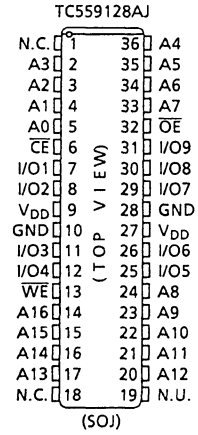
Features

- Fast access time
  - TC559128AJ-15 15ns (max.)
  - TC559128AJ-20 20ns (max.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (max.)	170	140	130	120	100	mA

- 5V single power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Package:
  - TC559128AJ: SOJ36-P-400

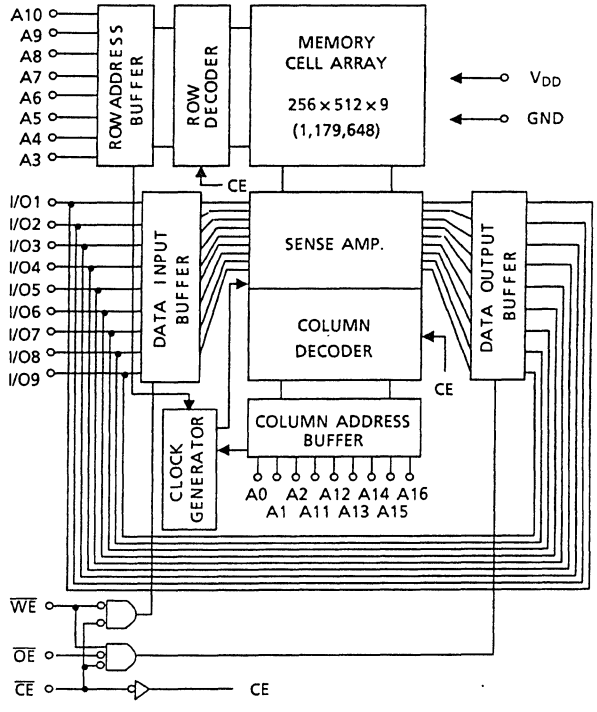
Pin Connection (Top View)



Pin Names

A0 ~ A16	Address Inputs
I/O1 ~ I/O9	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
N.U.	Not Usable (Input)

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 ~ I/O9	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disabled	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

*H or L

Note: N.U. pin must be kept open electrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.1	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (Except N.U. pin)	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
$I_{I\ (N.U.)}$	Input Current (N.U. pin)	V_{IN} = 0 ~ 0.8V		-1	–	20	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	t_{cycle} = 15ns	–	–	170	mA
			t_{cycle} = 20ns	–	–	140	
			t_{cycle} = 25ns	–	–	130	
			t_{cycle} = 30ns	–	–	120	
			t_{cycle} = 50ns	–	–	100	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V, Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC559128AJ-15		TC559128AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	20	
t_{CO}	Chip Enable Access Time	–	15	–	20	
t_{OE}	Output Enable Access Time	–	8	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC559128AJ-15		TC559128AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	
t_{AW}	Address Valid to End of Write	13	–	13	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Leve	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

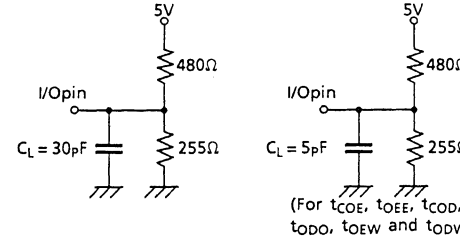
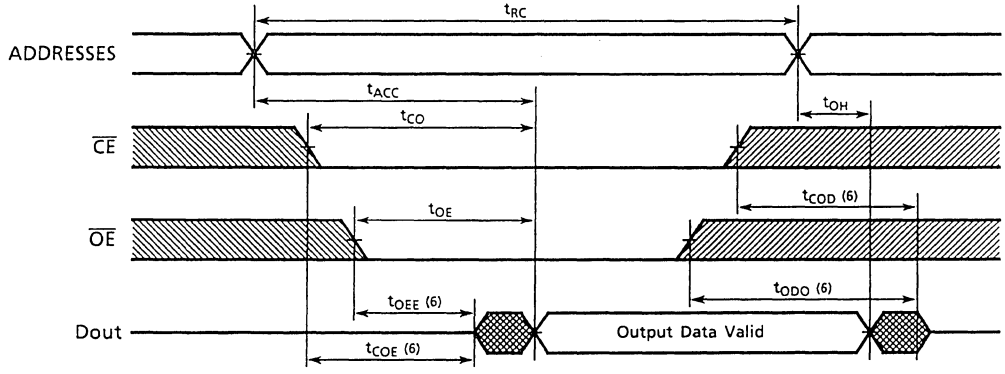


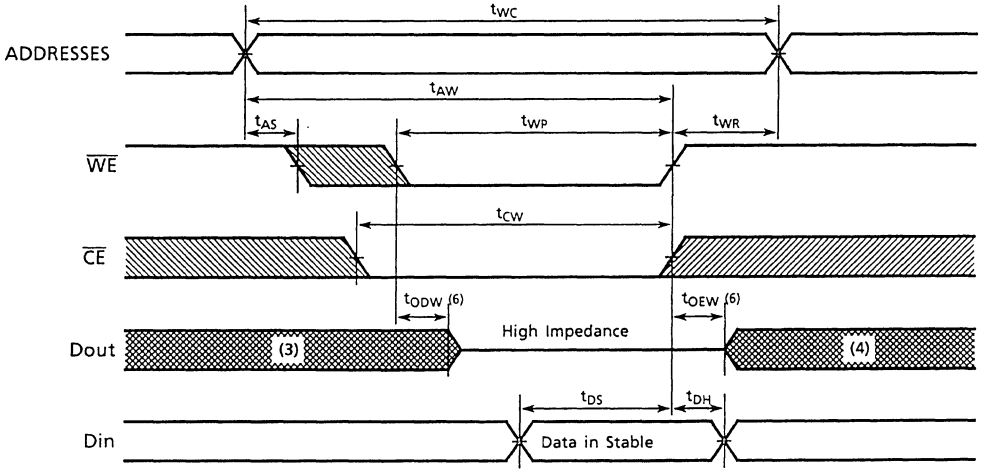
Figure 1.

Timing Waveforms

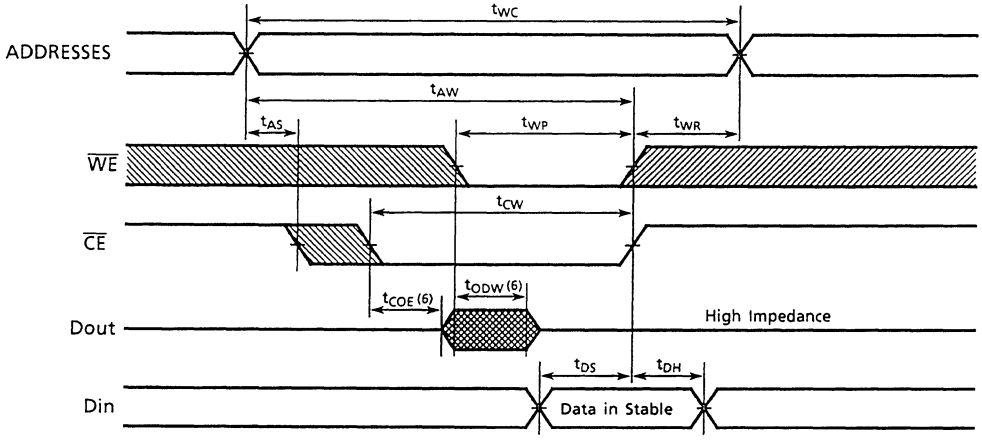
Read Cycle (2)



Write Cycle 1 (5) (WE Controlled)



Write Cycle 2 (5) (CE Controlled)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

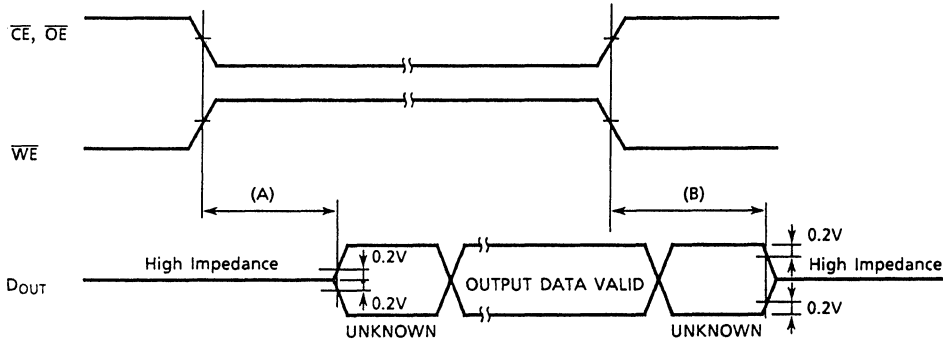
2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, the Outputs are in a high impedance state during this period.

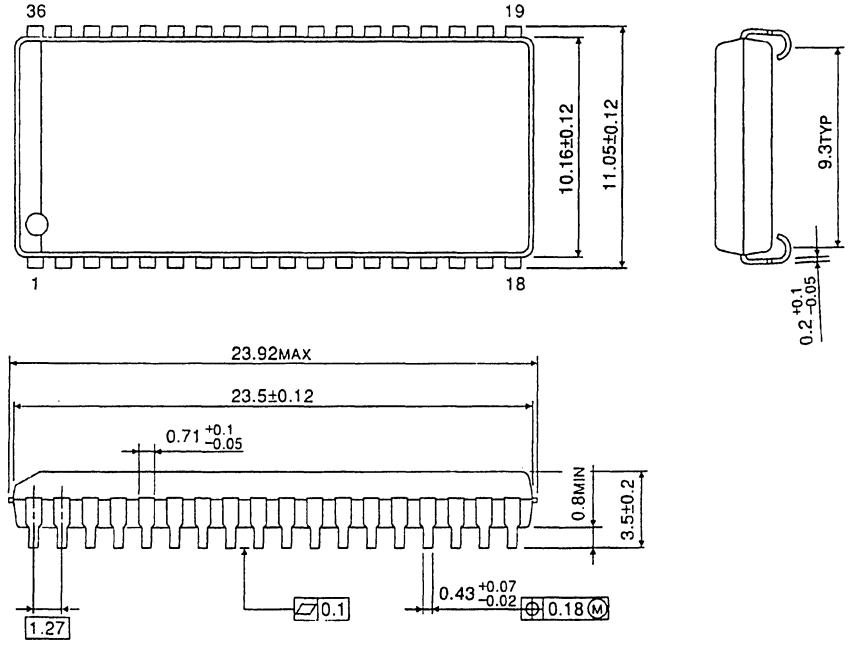
6. These parameters are specified and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings

Unit in mm

Plastic SOJ (SOJ36-P-400)



Weight : 1.35g (Typ.)

Notes

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SILICON GATE CMOS

65,536 WORD x 16 BIT CMOS STATIC RAM

Description

The TC551664AJ is a 1,048,576 bits high speed static random access memory organized as 65,536 words by 16 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551664AJ has low power feature with device control using Chip Enable ($\overline{CE}$), and has Output Enable input ($\overline{OE}$) for fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC551664AJ is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC551664AJ is packaged in a 44-pin SOJ with 400mil width for high density surface assembly.

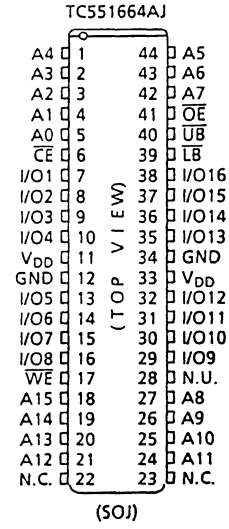
Features

- Fast access time
  - TC551664AJ -15 15ns (max.)
  - TC551664AJ -20 20ns (max.)
- Low power dissipation

Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

  - Standby: 1mA (max.)
- 5V single power supply: 5V±10%
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Data byte controls: $\overline{LB}$ (I/O1 ~ I/O8), $\overline{UB}$ (I/O9 ~ I/O16)
- Package: SOJ44-P-400

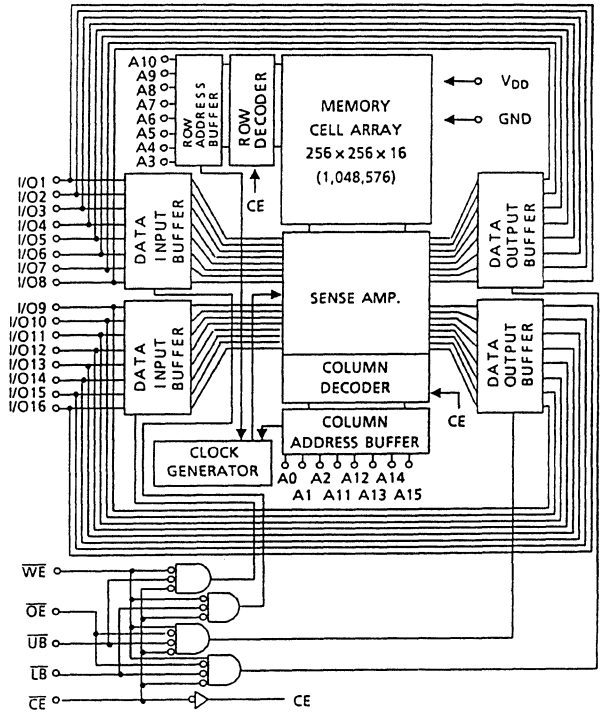
Pin Connection (Top View)



Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection
N.U.	Not Usable Input

Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/01 ~ I/08	I/09 ~ I/016	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			I_{DDO}
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Note: N.U. pin must be kept open elctrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

* -3V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (Except N.U. pin)	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
$I_{I(N.U.)}$	Input Current (N.U. pin)	V_{IN} = 0 ~ 0.8V		-1	–	20	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	t_{cycle} = 15ns	–	–	260	mA
			t_{cycle} = 20ns	–	–	220	
			t_{cycle} = 25ns	–	–	200	
			t_{cycle} = 30ns	–	–	180	
			t_{cycle} = 50ns	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V, Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551664AJ -15		TC551664AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	20	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	20	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC551664AJ -15		TC551664AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	12	–	12	–	
t_{AW}	Address Valid to End of Write	12	–	12	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

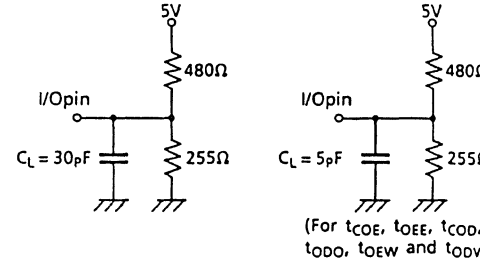
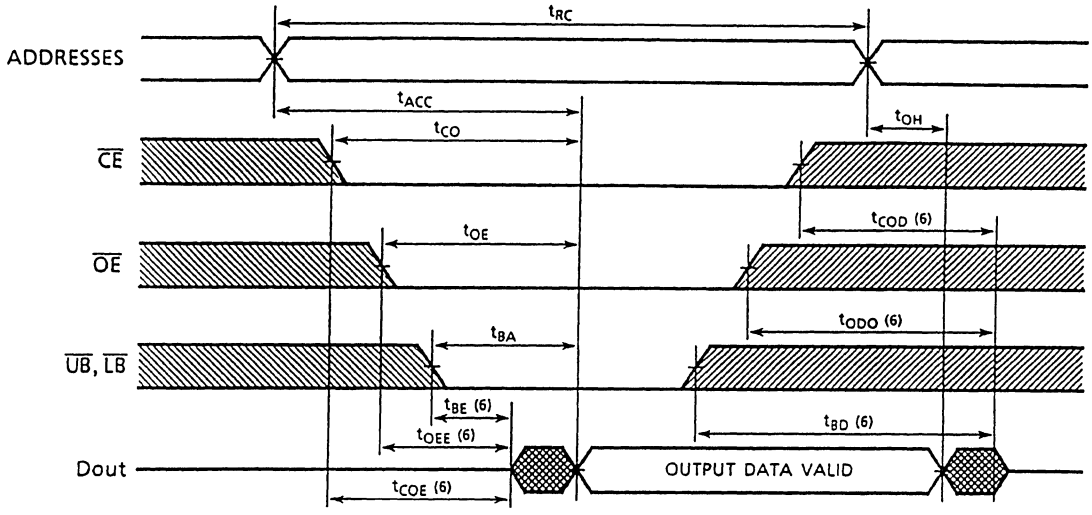


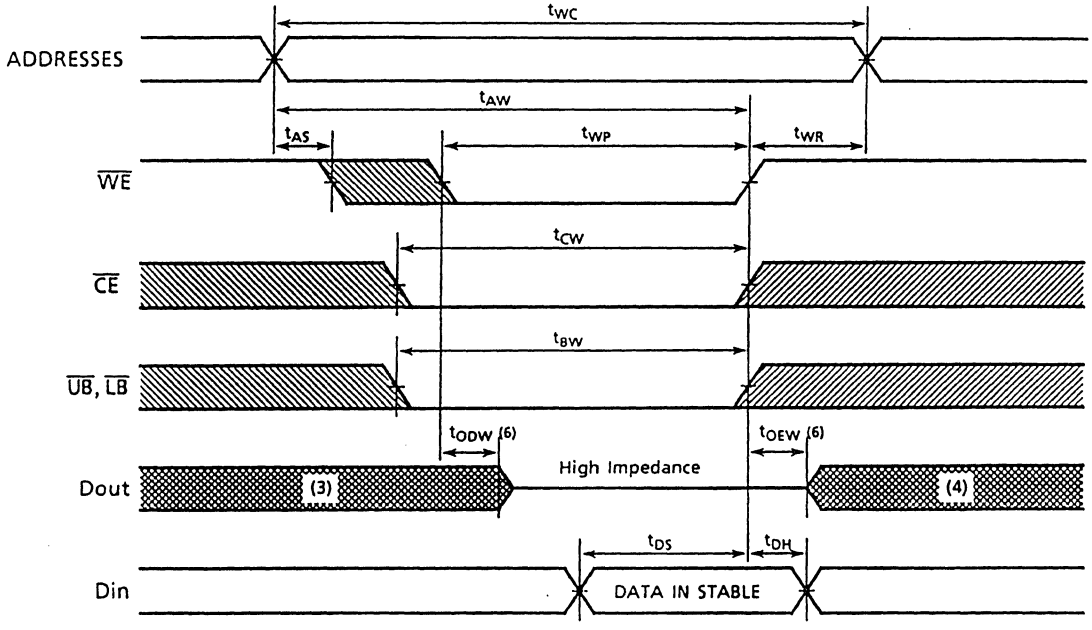
Figure 1.

Timing Waveforms

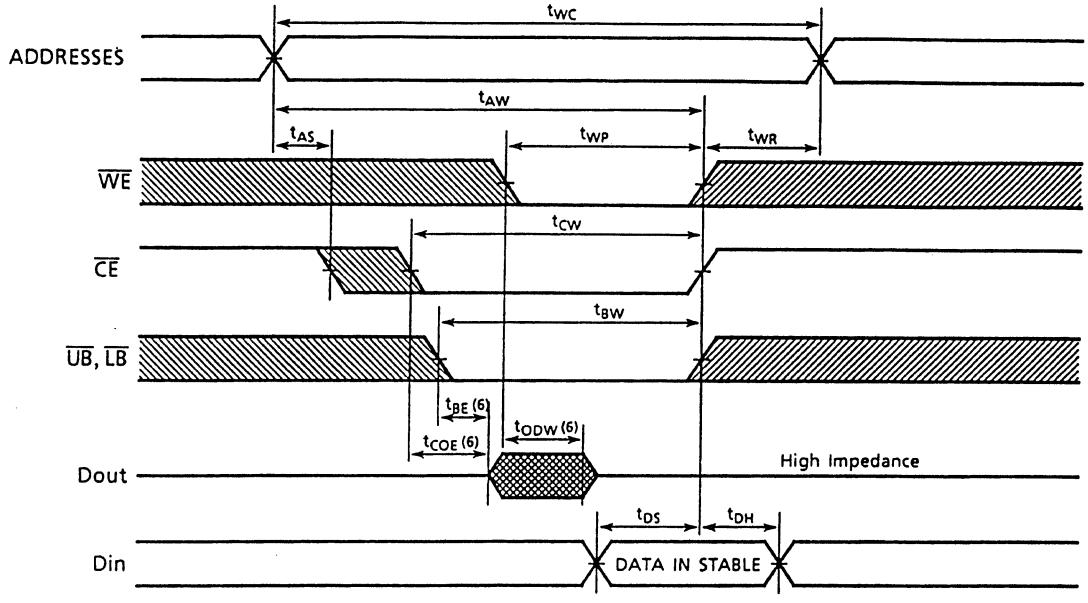
Read Cycle (2)



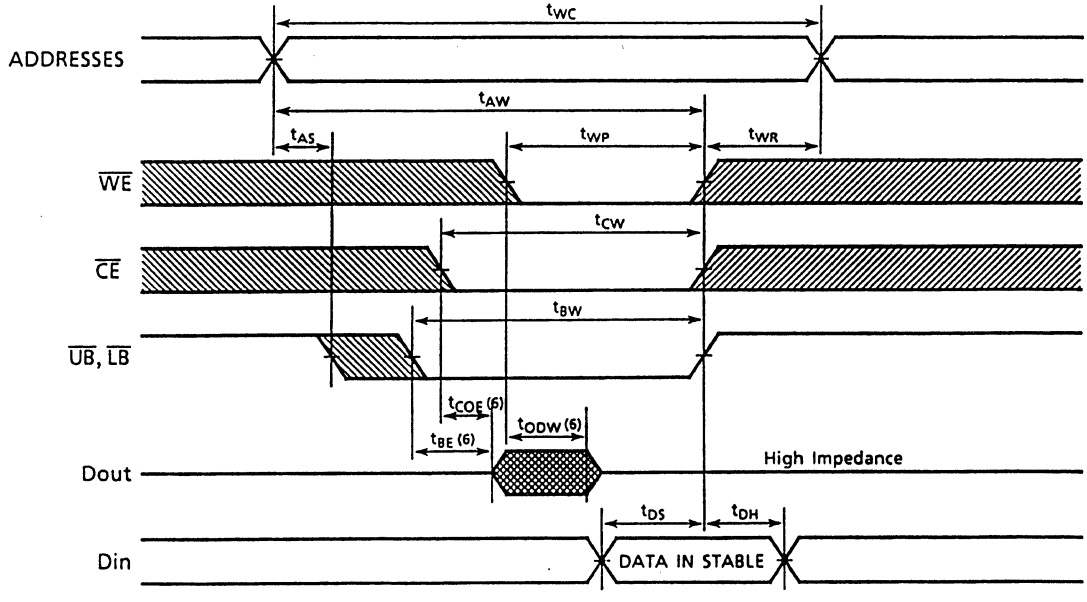
Write Cycle 1 (5) ($\overline{WE}$ Controlled)



Write Cycle 2 [5] ($\overline{CE}$ Controlled)



Write Cycle 3 [5] ($\overline{UB}$, $\overline{LB}$ Controlled)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

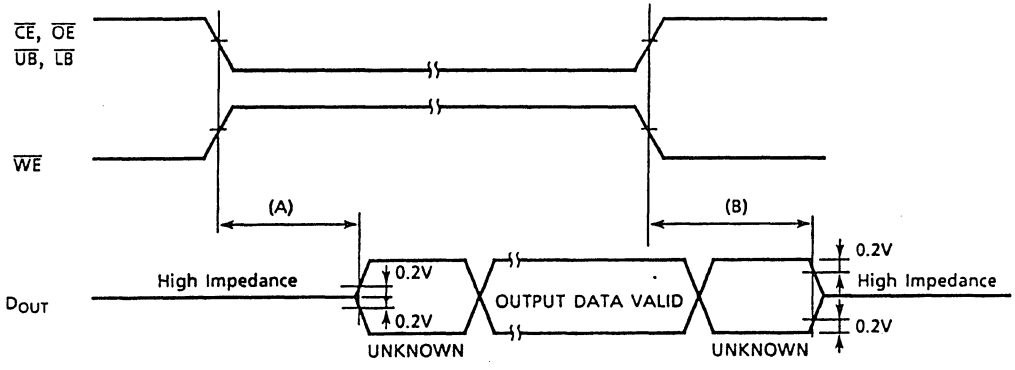
2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, the Outputs are in a high impedance state during this period.

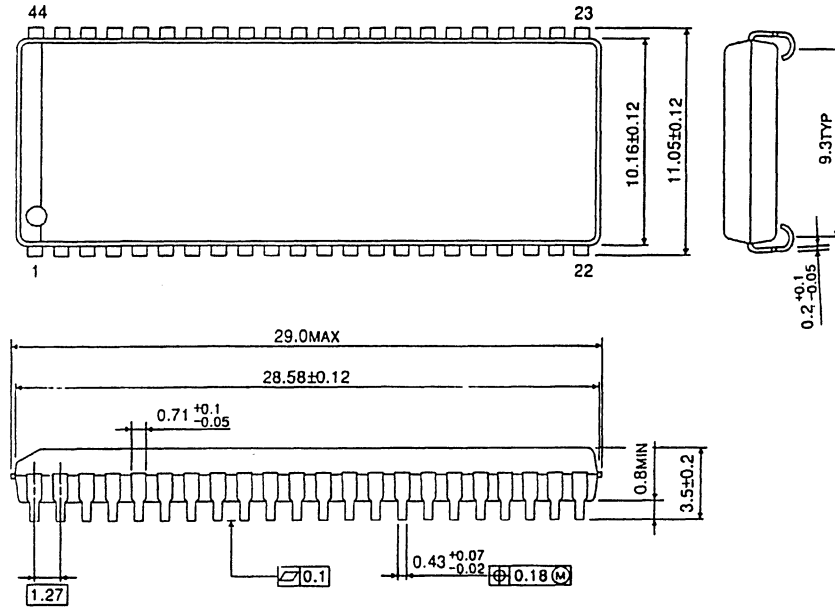
6. These parameters are specified and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings

Unit in mm

Plastic SOJ (SOJ44-P-400)



Weight : 1.64g (Typ.)

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TC551864AJ-15/20

PRELIMINARY

SILICON GATE CMOS

65,536 WORD x 18 BIT CMOS STATIC RAM

Description

The TC551864AJ is a 1,179,648 bits high speed static random access memory organized as 65,536 words by 18 bits using CMOS technology and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provide high speed feature.

The TC551864AJ has a low power feature with device control using Chip Enable ($\overline{CE}$), and has an Output Enable input ($\overline{OE}$) for fast memory access. Also, it allows that lower and upper byte access by Data Byte Control ($\overline{LB}$, $\overline{UB}$). The TC551864AJ is suitable for use in various application systems where high speed is required such as cache memory, high speed storage, and so on. All inputs and outputs are directly TTL compatible.

The TC551864AJ is packaged in a 44-pin plastic SOJ with 400mil width for high density surface assembly.

Features

- Fast access time
  - TC551864AJ -15 15ns (max.)
  - TC551864AJ -20 20ns (max.)
- Low power dissipation

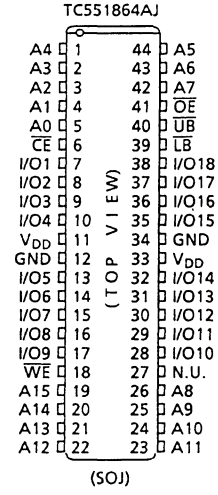
Cycle Time	15	20	25	30	50	ns
Operation (max.)	260	220	200	180	150	mA

  - Standby: 1mA (max.)
- 5V single power supply: 5V±10%
- Fully static operation
- All inputs and outputs TTL compatible
- Output buffer control: $\overline{OE}$
- Data byte controls: $\overline{LB}$, (I/O1 ~ I/O9), $\overline{UB}$ (I/O10 ~ I/O18)
- Package
  - TC551864AJ: SOJ44-P-400

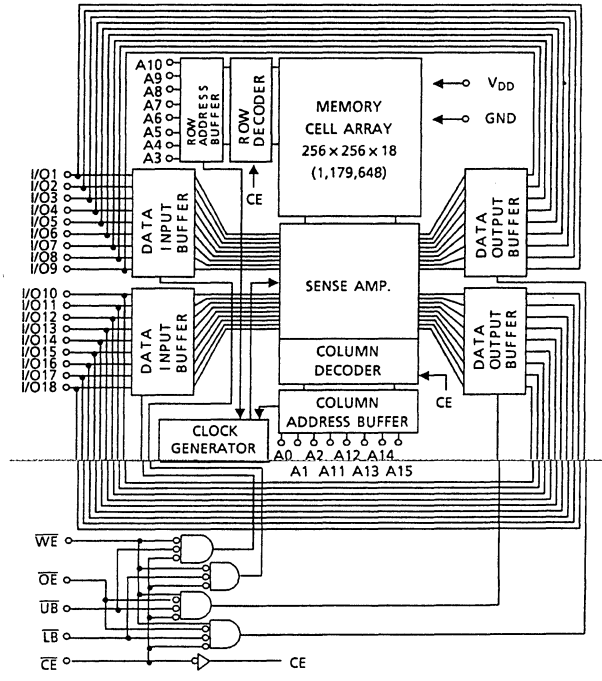
Pin Names

A0 ~ A15	Address Inputs
I/O1 ~ I/O18	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+5V)
GND	Ground
N.U.	Not Usable (Input)

Pin Connection (Top View)



Block Diagram



Operating Mode

OPERATING MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 ~ I/O9	I/O10 ~ I/O18	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	*	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Output Disable	L	H	H	*	*	High Impedance	High Impedance	I_{DDO}
	L	*	*	H	H			I_{DDO}
Standby	H	*	*	*	*	High Impedance	High Impedance	I_{DDS}

*H or L

Note: N.U. pin must be kept open elctrically or pulled down to GND level or less than 0.8V. Applying a voltage more than 0.8V to N.U. pin is prohibited.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

*-3V with a pulse width of 10ns

DC and Operationg Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (Except N.U. Pin)	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±10	μA
$I_{I(N.U.)}$	Input Current (N.U. Pin)	V_{IN} = 0 ~ 0.8V		-1	–	20	μA
I_{OH}	Output High Voltage	V_{OH} = 2.4V		-4	–	–	mA
I_{OL}	Output Low Voltage	V_{OL} = 0.4V		8	–	–	mA
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	t_{cycle} = 15ns	–	–	260	mA
			t_{cycle} = 20ns	–	–	220	
			t_{cycle} = 25ns	–	–	200	
			t_{cycle} = 30ns	–	–	180	
			t_{cycle} = 50ns	–	–	150	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	1	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551864AJ -15		TC551864AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	20	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	12	
t_{OE}	$\overline{OE}$ Access Time	–	8	–	10	
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	–	8	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{BE}	Output Enable Time from $\overline{UB}$, $\overline{LB}$	1	–	1	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	
t_{BD}	Output Disable Time from $\overline{UB}$, $\overline{LB}$	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC551864AJ -15		TC551864AJ -20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	ns
t_{WP}	Write Pulse Width	9	–	10	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	
t_{BW}	$\overline{UB}$, $\overline{LB}$ Enable to End of Write	12	–	13	–	
t_{AW}	Address Valid to End of Write	12	–	13	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

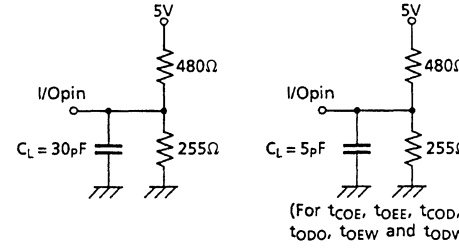
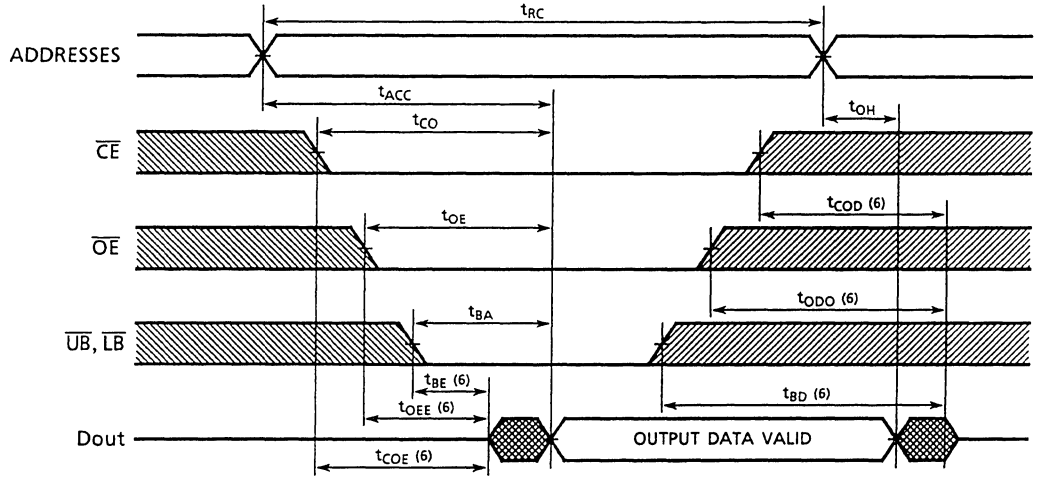


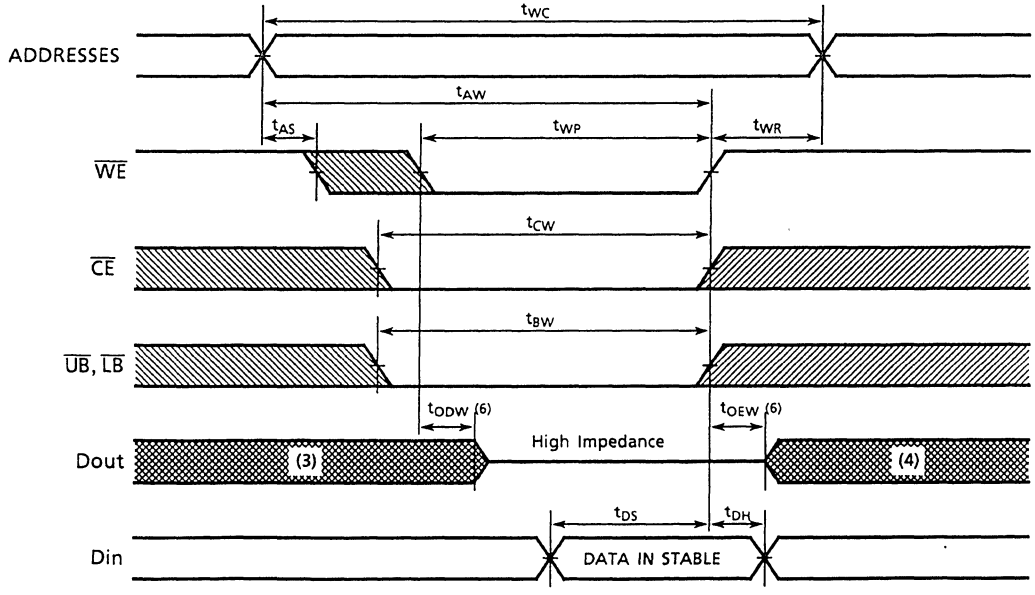
Figure 1.

Timing Waveforms

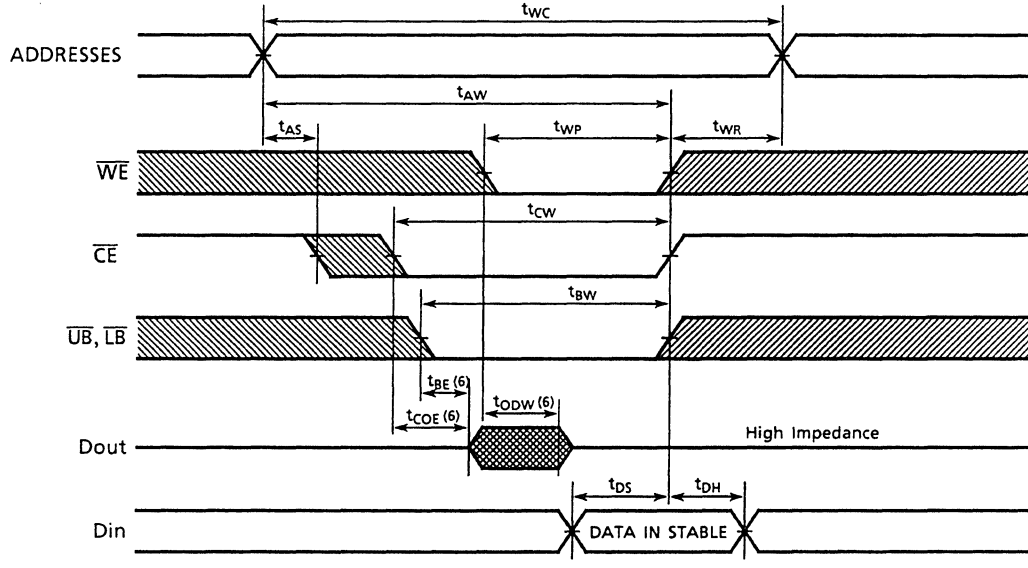
Read Cycle (2)



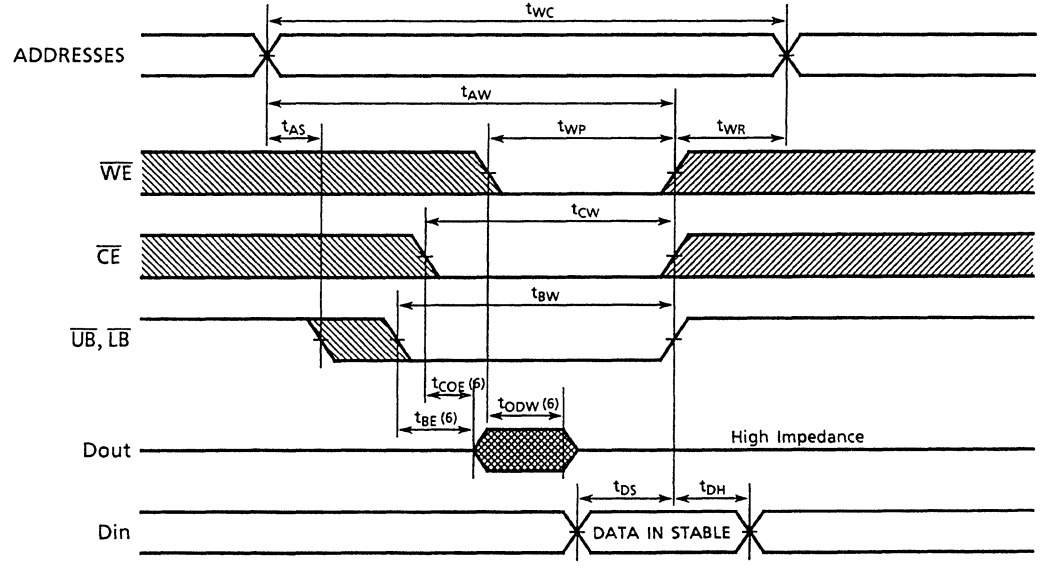
Write Cycle 1 (5) (WE Controlled)



Write Cycle 2 [5] ($\overline{CE}$ Controlled)



Write Cycle 3 [5] ($\overline{UB}$, $\overline{LB}$ Controlled)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

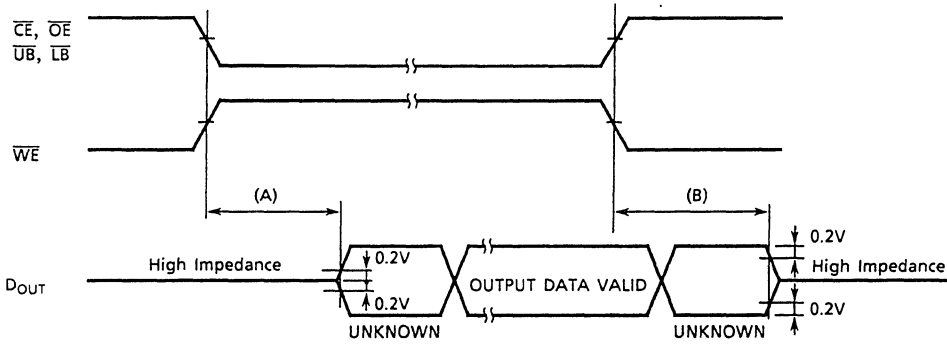
2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, the Outputs are in a high impedance state during this period.

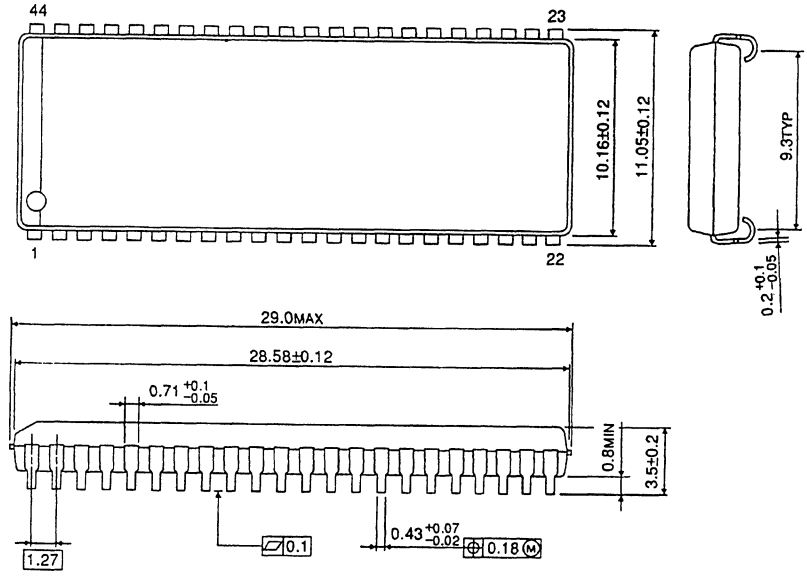
6. These parameters are specified as follows and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings

Unit in mm

Plastic SOJ (SOJ44-P-400)



Weight: 1.64g (typ.)

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TC551402J-25

PRELIMINARY

SILICON GATE CMOS

4,194,304 WORD x 1 BIT/1,048,576 WORD x 4 BIT CMOS STATIC RAM

Description

The TC551402J is a 4,194,304 bits high speed static random access memory, it is possible to change the organization between 4,194,304 words by 1 bit and 1,048,576 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's CMOS technology and advanced circuit form provides high speed feature.

The TC551402J has a low power feature with device control using Chip Enable ($\overline{CE}$), and has an Output Enable input ($\overline{OE}$) for fast memory access.

The TC551402J is suitable for use in various application systems where high speed is required such as cache memory, high speed storage, main memory, and so on. All inputs and outputs are directly TTL compatible and separation.

The TC551402J is packaged in a 32-pin SOJ with 400mil width for high density surface assembly.

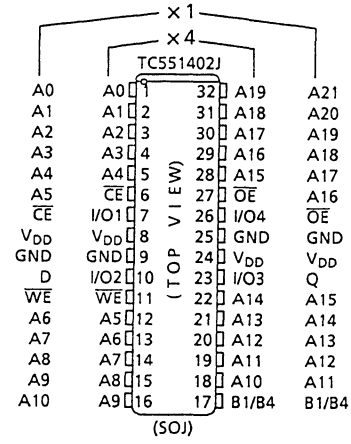
Features

- Fast access time
  - TC551402J -25 25ns (max.)
- Low power dissipation
  - TC551402J -25 160mA (max.)
  - Standby: 10mA (max.)
- 5V single power supply: 5V±10%
- Fully static operation
- All inputs and outputs TTL compatible
- I/O separation (x1 Mode), I/O common (x4 Mode)
- Output buffer control: $\overline{OE}$
- Package:
  - TC551402J: SOJ32-P-400A

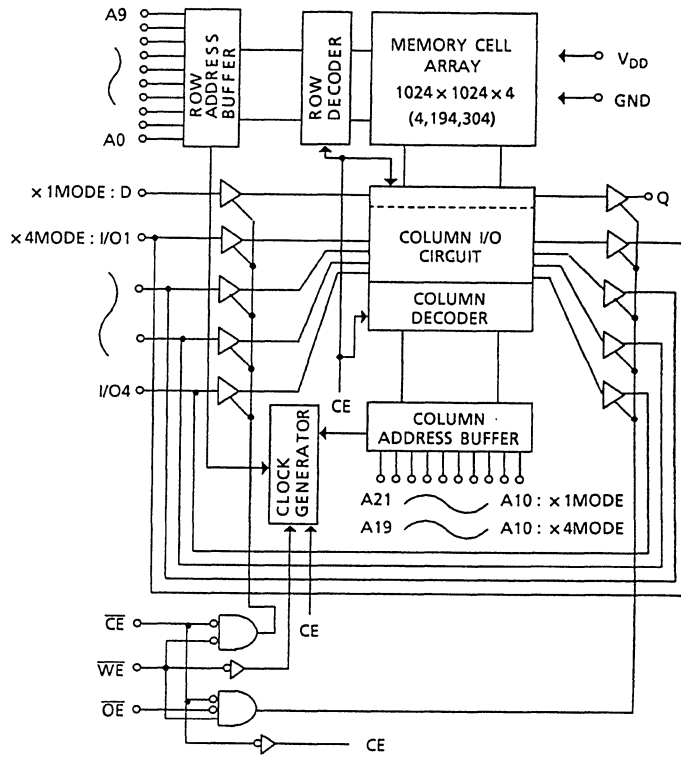
Pin Names

A0 ~ A21	Address Inputs
D	Data Input
Q	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
B1/B4	Bit Function

Pin Connection (Top View)



Block Diagram



Truth Table

TC551402J is possible to change the organization of bit mode between 4M words by one bit and 1M words by four bits with input level of pin condition B1/B4.

"4M x 1 Mode" is performed on when pin pin B1/B4 is held on "V_{IH} level". On the other hand "1M x 4 Mode" requires B1/B4 to be connected to "V_{IL} level".

Input level of B1/B4 condition must be set at the same time of power on. Any chnage of input level B1/B4, high or low, is prohibited after power on.

MODE		B1/B4	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	POWER
x1 Mode	Read	H	L	L	H	D_{OUT}	I_{DDO}
	Write	H	L	*	L	D_{IN}	I_{DDO}
	Output Disable	H	L	H	H	High-Z	I_{DDO}
	Standby	H	H	*	*	High-Z	I_{DDS}
x4 Mode	Read	L	L	L	H	D_{OUT}	I_{DDO}
	Write	L	L	*	L	D_{IN}	I_{DDO}
	Output Disable	L	L	H	H	High-Z	I_{DDO}
	Standby	L	H	*	*	High-Z	I_{DDS}

*:H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~ 7.0	V
V_{OUT}	Output Terminal Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*-3V with a pulse width of 10ns

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.5*	–	0.8	V

*-3V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	µA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	–	–	
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}	–	–	±10	µA
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, Other Inputs = V_{IH}/V_{IL}	–	–	160	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}	–	–	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	–	–	10	

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C[1], V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551402J -25		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	25	–	ns
t_{ACC}	Address Access Time	–	25	
t_{CO}	Chip Enable Access Time	–	25	
t_{OE}	Output Enable Access Time	–	12	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	10	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	
t_{PU}	Chip Selection to Power Up Time	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	25	

Write Cycle

SYMBOL	PARAMETER	TC551402J -25		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	25	–	ns
t_{WP}	Write Pulse Width	13	–	
t_{AW}	Address Valid to End of Write	20	–	
t_{CW}	Chip Enable to End of Write	20	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	10	
t_{DS}	Data Setup Time	12	–	
t_{DH}	Data Hold Time	0	–	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

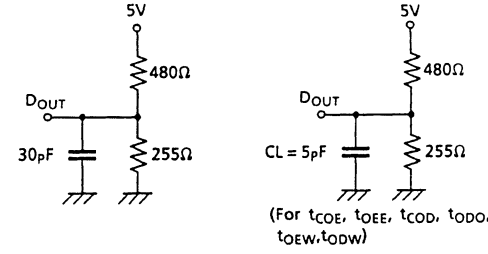
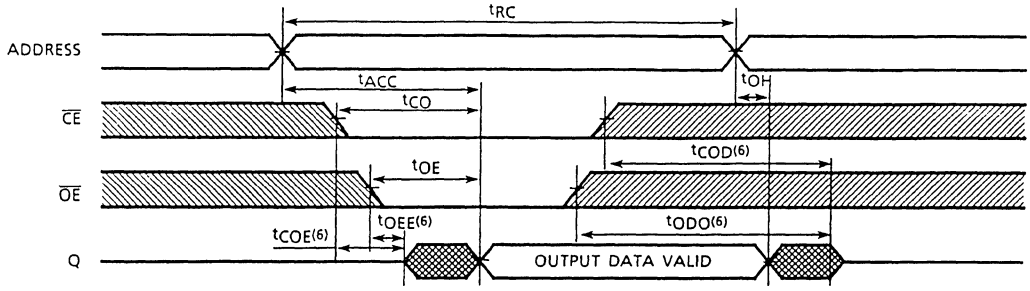


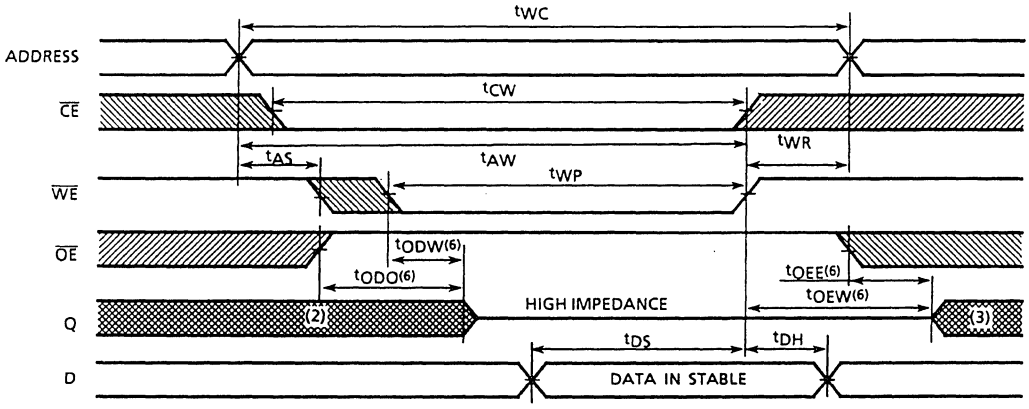
Figure 1.

Timing Waveforms

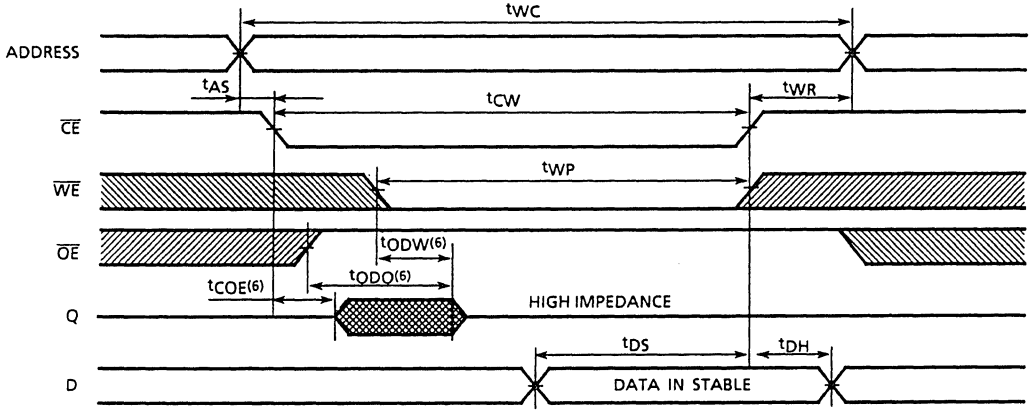
Read Cycle (1)



Write Cycle 1 (5) ($\overline{WE}$ Controlled Write)



Write Cycle 2 (5) ($\overline{CE}$ Controlled Write)



Notes:

1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

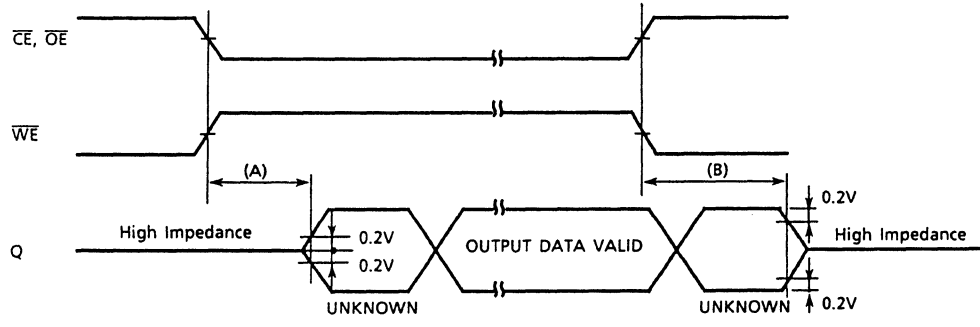
2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

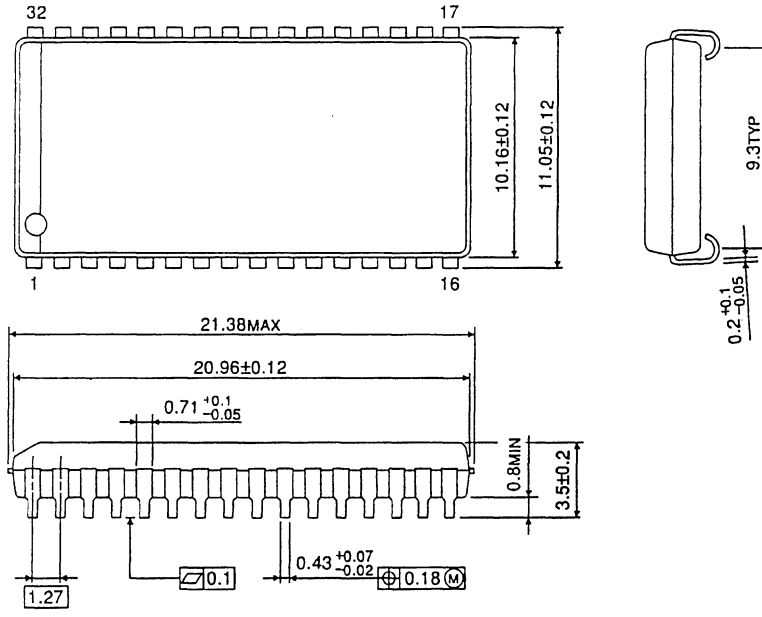
5. Assuming that $\overline{OE}$ is High for Write Cycle, the Outputs are in a high impedance state during this period.

6. These parameters are specified and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings **Unit in mm**

Plastic SOJ (SOJ32-P-400A)



Weight : 1.22g (Typ.)

Notes

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High Speed Synchronous SRAM

65,536 WORD x 16 BIT SYNCHRONOUS PIPELINE BURST SRAM

Description

The TC55V1165FF is a 1,048,576 bit synchronously pipelined burst SRAM that is organized as 65,536 words by 16 bits and designed for use in a secondary cache to support MPUs which have burst functions.

The TC55V1165FF integrates a 2-bit burst address counter and control logic with a 64K x 16 static RAM. All inputs, except the output enable ($\overline{OE}$) input, are synchronous with either the rising edge of the clock (CLK) input.

The read operation can be initiated with either the address status processor ($\overline{ADSP}$) input or the address status controller ($\overline{ADSC}$) input. Subsequent burst addresses can be generated internally and are controlled by the address advance ($\overline{ADV}$) input.

The write operation is internally self-timed and is initiated by the rising edge of the clock (CLK) input. Byte Write Enables ($\overline{BW1}$ - $\overline{BW2}$) allow a one to two byte write operation according to their logic states.

The TC55V1165FF operates from a single 3.3V power supply, and is packaged in a low profile 100-pin plastic QFP (LQFP).

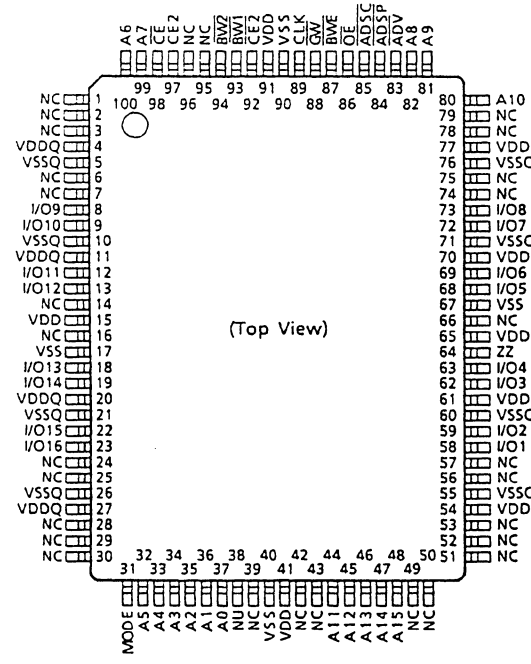
Features

- Organization: 64K words x 16 bits
- Fast cycle time: 15ns min. (66.7MHz)
- Fast access time: 8ns (max.) (Clock to data output)
- Pipelined burst operation
- 2-bit burst address counter (Interleaved Burst or Linear Burst Sequences)
- Synchronous self-timed write (Global Write and Byte Write)
- LVTTL compatible interface
- Package:
  - 100-pin LQFP (0.65mm pitch, 1.6mm height typ.): LQFP100-P-1420 (Weight: 0.56g typ.)

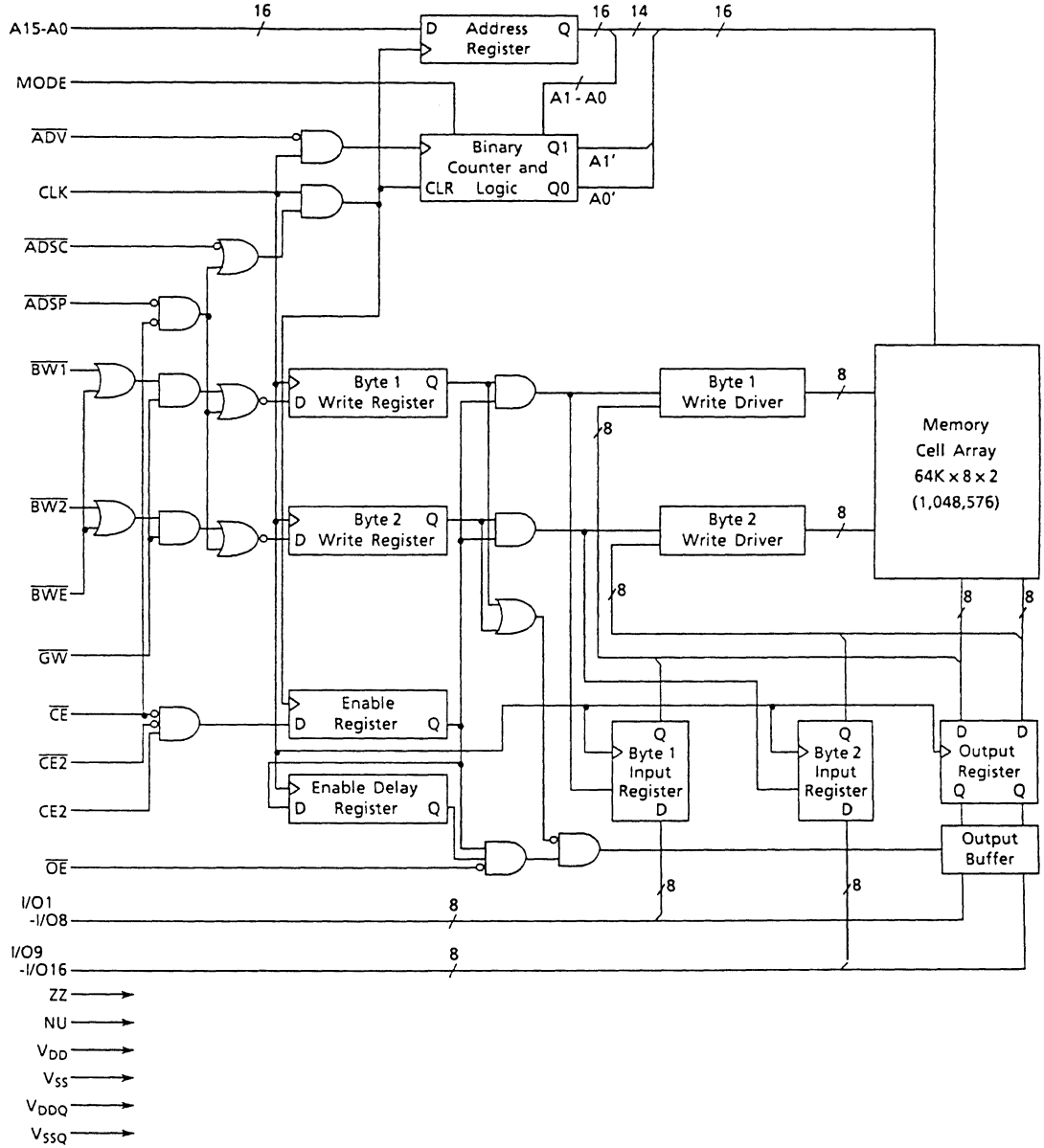
Pin Names

$\overline{A0}$ ~ $\overline{A15}$	Address Inputs
$\overline{I/O1}$ ~ $\overline{I/O16}$	Data Inputs /Outputs
$\overline{CLK}$	Clock Input
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable Inputs
$\overline{ADSP}$	Address Status Processor Input
$\overline{ADSC}$	Address Status Controller Input
$\overline{ADV}$	Address Advance Input
$\overline{GW}$	Global Write Enable Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{BW1}$ ~ $\overline{BW2}$	Byte Write Enable Inputs
$\overline{OE}$	Output Enable Input
$\overline{MODE}$	Mode Select Input
$\overline{ZZ}$	Snooze Input
$\overline{NU}$	Not Usable Input
$\overline{V_{DD}}$, $\overline{V_{DDQ}}$	Power
$\overline{V_{SS}}$, $\overline{V_{SSQ}}$	Ground

Pin Connection (Top View)



Block Diagram



Pin Descriptions

Pin Number	Symbol	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0 - A15	Input (Synchronous)	Synchronous Address Inputs. These address inputs are registered on the rising edges of CLK. All address inputs must meet the setup and hold times for all rising edges of CLK when the chip is enabled.
93, 94	$\overline{BW1}$, $\overline{BW2}$	Input (Synchronous)	Synchronous Byte Write Enables. These inputs are active low and control byte write operations when $\overline{BWE}$ is low. $\overline{BW1}$ controls I/O1 - 8. $\overline{BW2}$ controls I/O9 - 16. For byte write operations, if either of two inputs are low, all outputs are in high impedance.
87	$\overline{BWE}$	Input (Synchronous)	Synchronous Byte Write Enable. This input is active low and controls byte write operations.
88	$\overline{GW}$	Input (Synchronous)	Synchronous Global Write. This input is active low and controls a 16bit write operation independent of the $\overline{BWE}$ and $\overline{BW1}$, $\overline{BW2}$ inputs.
89	CLK	Input	Reference Clock. All synchronous input signals are registered on all rising edges of CLK. All synchronous signal timings are measured from the rising edges of CLK. All synchronous input signals must meet the setup time and hold times referenced to the rising edges of CLK.
83	$\overline{ADV}$	Input (Synchronous)	Synchronous Burst Advance. This signal is active low and controls the internal burst address counter after the external address is loaded. When the signal is low, the internal burst address is not advanced. If a write operation initiated by $\overline{ADSP}$ is desired, this signal must be high to write the loaded address at the rising edge of the first clock after an assertion of $\overline{ADSP}$.
84	$\overline{ADSP}$	Input (Synchronous)	Synchronous Address Status Processor. The signal is active low. This signal controls the burst start by registering the new external address. The write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$) are ignored at the assertion of $\overline{ADSP}$ and a read operation is initiated. A subsequent operation is dependent on the write enables at the rising edge of the first clock after an assertion of $\overline{ADSP}$. This signal is ignored if $\overline{CE}$ is high.
85	$\overline{ADSC}$	Input (Synchronous)	Synchronous Address Status Controller. This signal is active low. This signal initiates a burst read or write depending on the write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$) by registering the new external address.
98	$\overline{CE}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable) and the internal use of ADSP. This signal is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.
97	CE2	Input (Synchronous)	Synchronous Chip Enable. This signal is active high. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.

86	$\overline{OE}$	Input (Asynchronous)	Asynchronous Output Enable. This signal is active low and controls all 16bit I/O buffers. This signal must be high for the time write data is driven prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$) following a read operation.
Pin Number	**Symbol**	**Type**	**Description**
58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	I/O1 - I/O16	Input /Output (Synchronous)	Synchronous Data Inputs/Outputs. Byte1 is I/O1 - I/O8, Byte2 is I/O9 - I/O16.
31	$\overline{MODE}$	Input (Asynchronous)	Mode Select. This signal is used to select the burst sequence. If this signal is high or not connected, the burst sequence is Interleaved Burst. If this signal is low, the burst sequence is Linear Burst. This input is internally pulled up. Altering the input state while the device is operating is prohibited.
64	$\overline{ZZ}$	Input (Asynchronous)	Snooze. This signal is active high and is used to place the device into sleep mode, which is a low power standby mode. If this signal is low or not connected, the device is in an active state. If this signal is high, the device is in a sleep state, and the memory data is retained. The device wakes up when a read or write operation is initiated by ADSP or ADSC after deasserting this signal. This input must be connected to V_{SS} when ZZ mode is not used.
38	NU	Input (Asynchronous)	Not Usable. This signal is used only by the manufacturer. This signal must be low or not connected. This input is internally pulled down.
1, 2, 3, 6, 7, 14, 16, 24, 25, 28, 29, 30, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 74, 75, 78, 79	NC	–	No Connection. These inputs are not internally connected. Pin numbers 49 and 50 are reserved for future device expansion.
15, 41, 65, 91	V_{DD}	Supply	Power Supply.
17, 40, 67, 90	V_{SS}	Ground	Ground.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	Output Buffer Power Supply.
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Ground	Output Buffer Ground.

Operation Mode

(1) Synchronous Input Truth Table →

Operation	CLK	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$ [4]	ZZ [4]	ADDRESS USED	I/O [5]	CURRENT [2]
$\overline{\text{Begin Burst Read}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{L}$	$\overline{\text{External Address}}$	$\overline{\text{Dout (n)}}$	$\overline{I_{DDO1}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{H}$	$\overline{L}$			
$\overline{\text{Continue Burst Read}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{\text{Next Burst Address}}$	$\overline{\text{Dout (n)}}$	$\overline{I_{DDO1}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$ [6]	$\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{L}$			
$\overline{\text{Suspend Burst Read}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{\text{Current Burst Address}}$	$\overline{\text{Dout (n)}}$	$\overline{I_{DDO2}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$ [6]	$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{L}$			
$\overline{\text{Begin Burst Write}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{L}$	$\overline{L}$	$\overline{\text{External Address}}$	$\overline{\text{Din (p)}}$	$\overline{\text{N/A}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{\text{Current Burst Address}}$		$\overline{\text{N/A}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$ [6]	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$			
$\overline{\text{Continue Burst Write}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{L}$	$\overline{\text{Next Burst Address}}$	$\overline{\text{Din (p)}}$	$\overline{\text{N/A}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$ [6]	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{L}$			
$\overline{\text{Suspend Burst Write}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{\text{Current Burst Address}}$	$\overline{\text{Din (p)}}$	$\overline{\text{N/A}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$ [6]	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$			
$\overline{\text{Deselected}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{L}$	$\overline{\text{None}}$	$\overline{\text{Hi - Z (p)}}$	$\overline{I_{DDS2}}$
	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{x}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{L}$			
	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{L}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{L}$			
	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{x}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{L}$			
	$\overline{L}\rightarrow\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{L}$			
$\overline{\text{Snooze}}$	$\overline{L}\rightarrow\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{\text{None}}$	$\overline{\text{Hi - Z (p)}}$	$\overline{I_{DDS3}}$

Note:
1. ZZ input is asynchronous, but is included in this table.
2. Consumption current does not include output buffer current.
3. H is logical High and L is logical Low. X is High or Low.
4. $\overline{WRITE}$ = L means any one or two byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.
5. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is present cycle.
6. When $\overline{CE}$ = H, $\overline{ADSP}$ is disabled ($\overline{ADSP}$ = X). $\overline{ADSP}$ = L to avoid redundancy with the previous truth table entry when $\overline{CE}$ = H and $\overline{ADSP}$ = H.

(2) Partial Truth Table for Write Enables (Synchronous Input)

Operation	CLK	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	I/O1 - I/O8	I/O9 - I/O16
$\overline{Read}$	$\overline{L} \rightarrow \overline{H}$	$\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{Dout\ (n)}$	$\overline{Dout\ (n)}$
	$\overline{L} \rightarrow \overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{H}$	$\overline{Dout\ (n)}$	$\overline{Dout\ (n)}$
$\overline{Write}$	$\overline{L} \rightarrow \overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{Din\ (p)}$	$\overline{Din\ (p)}$
	$\overline{L} \rightarrow \overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{L}$	$\overline{Din\ (p)}$	$\overline{Din\ (p)}$
	$\overline{L} \rightarrow \overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{Din\ (p)}$	$\overline{Hi - Z\ (p)}$
	$\overline{L} \rightarrow \overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{Hi - Z\ (p)}$	$\overline{Din\ (p)}$

Note: 1. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is present cycle.

(3) Asynchronous Truth Table

Operation	$\overline{OE}$	ZZ	I/O1 - I/O32
$\overline{Read}$	$\overline{L}$	$\overline{L}$	$\overline{Dout}$
	$\overline{H}$	$\overline{L}$	$\overline{Hi - Z}$
$\overline{Write}$	$\overline{x}$	$\overline{L}$	$\overline{Din, Hi - Z}$
$\overline{Deselected}$	$\overline{x}$	$\overline{L}$	$\overline{Hi - Z}$
$\overline{Snooze}$	$\overline{x}$	$\overline{H}$	$\overline{Hi - Z}$

(4) Write Pass-through Truth Table

Previous Cycle				Present Cycle											Next Cycle
Operation	Addr.	$\overline{WRITE}$	I/O	Operation	Addr.	$\overline{WRITE}$	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	I/O	I/O
$\overline{Write\ Cycle}$	$\overline{Ak}$	$\overline{L}$	$\overline{Dn\ (Ak)}$	$\overline{ADSP\ Initiated\ Read\ Cycle}$	$\overline{Am}$	$\overline{x}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{x}$	$\overline{L}$	$\overline{Qn\ (Ak)}$	$\overline{Q1\ (Am)}$
				$\overline{ADSC\ Initiated\ Read\ Cycle}$	$\overline{Am}$	$\overline{H}$	$\overline{L}$	$\overline{L}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{x}$	$\overline{L}$		
				$\overline{Con\text{-}tinue\ Read\ Cycle}$	$\overline{x}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{L}$	$\overline{L}$		$\overline{Qn + 1\ (Ak)}$
					$\overline{x}$	$\overline{H}$	$\overline{H}$	$\overline{x}$	$\overline{x}$	$\overline{L}$	$\overline{H}$	$\overline{L}$	$\overline{L}$		

Note: 1. Dn (Ak) represents input data for the n-th burst address starting from address Ak.
2. Qn (Ak) represents output data from the n-th burst address starting from address Ak.
3. n = 1, 2, 3, or 4.
4. $\overline{WRITE}$ = L means any one or two byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.

(5) Interleaved Burst Sequence (MODE input = NC or V_{DD})

Bit Order: A_{15} A_{14}..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
xx..... xx00	xx..... xx01	xx..... xx10	xx..... xx11
xx..... xx01	xx..... xx00	xx..... xx11	xx..... xx10
xx..... xx10	xx..... xx11	xx..... xx00	xx..... xx01
xx..... xx11	xx..... xx10	xx..... xx01	xx..... xx00

The burst address wraps around to its initial state.

(6) Linear Burst Sequence (MODE input = V_{SS})

Bit Order: A_{15} A_{14}..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
xx..... xx00	xx..... xx01	xx..... xx10	xx..... xx11
xx..... xx01	xx..... xx10	xx..... xx11	xx..... xx00
xx..... xx10	xx..... xx11	xx..... xx00	xx..... xx01
xx..... xx11	xx..... xx00	xx..... xx01	xx..... xx10

The burst address wraps around to its initial state.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	-0.5 ~ V_{DD}	V
V_{IN}	Input Terminal Voltage	-0.5* ~ 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DDQ} + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*: -1.5V with a pulse width of 20% • t_{KC} min (4ns max)
**: V_{DDQ} + 1.5V with a pulse width of 20% • t_{KC} min (4ns max)

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.1	3.3	3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	3.1	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3**	V
V_{IH1}	Input High Voltage for MODE pin	V_{DD} - 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3*	–	0.8	V
V_{IL1}	Input Low Voltage for MODE and NU pins	-0.5	0.0	0.3	V

* : -1.0V with a pulse width of 20% • t_{KC} min (4ns max)
** : V_{DD} + 1.0V with a pulse width of 20% • t_{KC} min (4ns max)
Note: NU pin must be low or not connected.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.1V ~ 3.6V)

SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (Except MODE, ZZ, NU pins)		V_{IN} = 0 ~ V_{DD}	–	–	±1	μA
I_{LO}	Output Leakage Current		Device Deselected or Output Deselected, V_{OUT} = 0 ~ V_{DD}	–	–	±1	μA
I_I	Input Current	MODE pin	V_{IN} = V_{DD} ~ V_{DD} - 0.3V	-1	–	1	μA
			V_{IN} = 0 ~ 0.3V	-100	–	1	
		ZZ pin	V_{IN} = V_{DD} ~ 2.0V	-1	–	100	
			V_{IN} = 0 ~ 0.8V	-1	–	20	
			V_{IN} = 0 ~ 0.3V	-1	–	1	
		NU pin	V_{IN} = 0 ~ 0.3V	-1	–	1	
V_{OH}	Output High Voltage		I_{OH} = -8mA	2.4	–	–	V
			I_{OH} = -100μA	V_{DD} - 0.2	–	–	
V_{OL}	Output Low Voltage		I_{OL} = 8mA	–	–	0.4	
			I_{OL} = 100μA	–	–	0.2	
I_{DDO1}	Operating Current		Device Selected, I_{OUT} = 0 mA, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	180	mA
I_{DDO2}	Operating Current (Idle)		Device Selected, I_{OUT} = 0 mA, ADSC, ADSP, ADV ≥ V_{IH}, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	150	mA
I_{DDS1}	Standby Current (CLK running)		Device Selected, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	35	mA
I_{DDS2}	Standby Current		Device Selected, All inputs = V_{DD} - 0.2V or 0.2V, CLK frequency = 0Hz	–	–	2	mA
I_{DDS3}	Snooze Current		ZZ = V_{DD} - 0.2V, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{RC} min.	–	–	2	mA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
	Input Capacitance for MODE, ZZ, NU pin	V_{IN} = GND	8	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = GND	7	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.1V ~ 3.6V)

SYMBOL	PARAMETER	TC55V1165FF-8		TC55V1165FF-10		TC55V1165FF-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{KC}	CLK Cycle Time	15	–	16	–	20	–	ns
t_{KH}	CLK High Pulse Width	5	–	5	–	6	–	
t_{KL}	CLK Low Pulse Width	5	–	5	–	6	–	
t_{KQV}	Access Time from CLK	–	8	–	10	–	12	
t_{KQX}	Output Hold Time from CLK	2	–	2	–	2	–	
t_{KQLZ}	Output Enable Time from CLK	5	–	5	–	5	–	
t_{KQHZ}	Output Disable Time from CLK	2	5	2	5	2	6	
t_{GQV}	Access Time from OE	–	6	–	6	–	7	
t_{GQLZ}	Output Enable Time from OE	0	–	0	–	0	–	
t_{GQHZ}	Output Disable Time from OE	2	5	2	5	2	6	
t_{AS}	Address Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{AH}	Address Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ADSS}	ADSP, ADSC Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{ADSH}	ADSP, ADSC Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{VS}	ADV Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{VH}	ADV Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{WS}	GW, BWE, BW1, BW2 Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{WH}	GW, BWE, BW1, BW2 Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CES}	CE, CE2, CE2 Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{CEH}	CE, CE2, CE2 Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{DS}	Data Setup Time CLK	2.5	–	2.5	–	3.0	–	
t_{DH}	Data Hold Time CLK	0.5	–	0.5	–	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	5	–	6	–	
t_{ZR}	ZZ Recovery Time	8	–	10	–	12	–	
t_{ZHZ}	Output Disable Time ZZ	0	12	0	12	0	14	

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

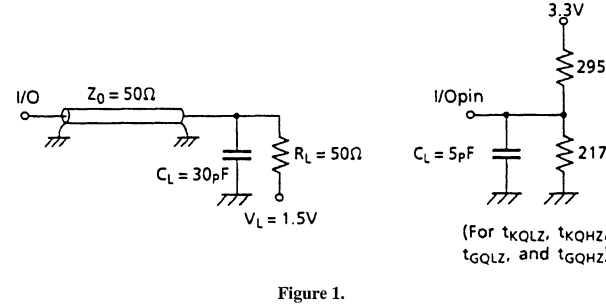
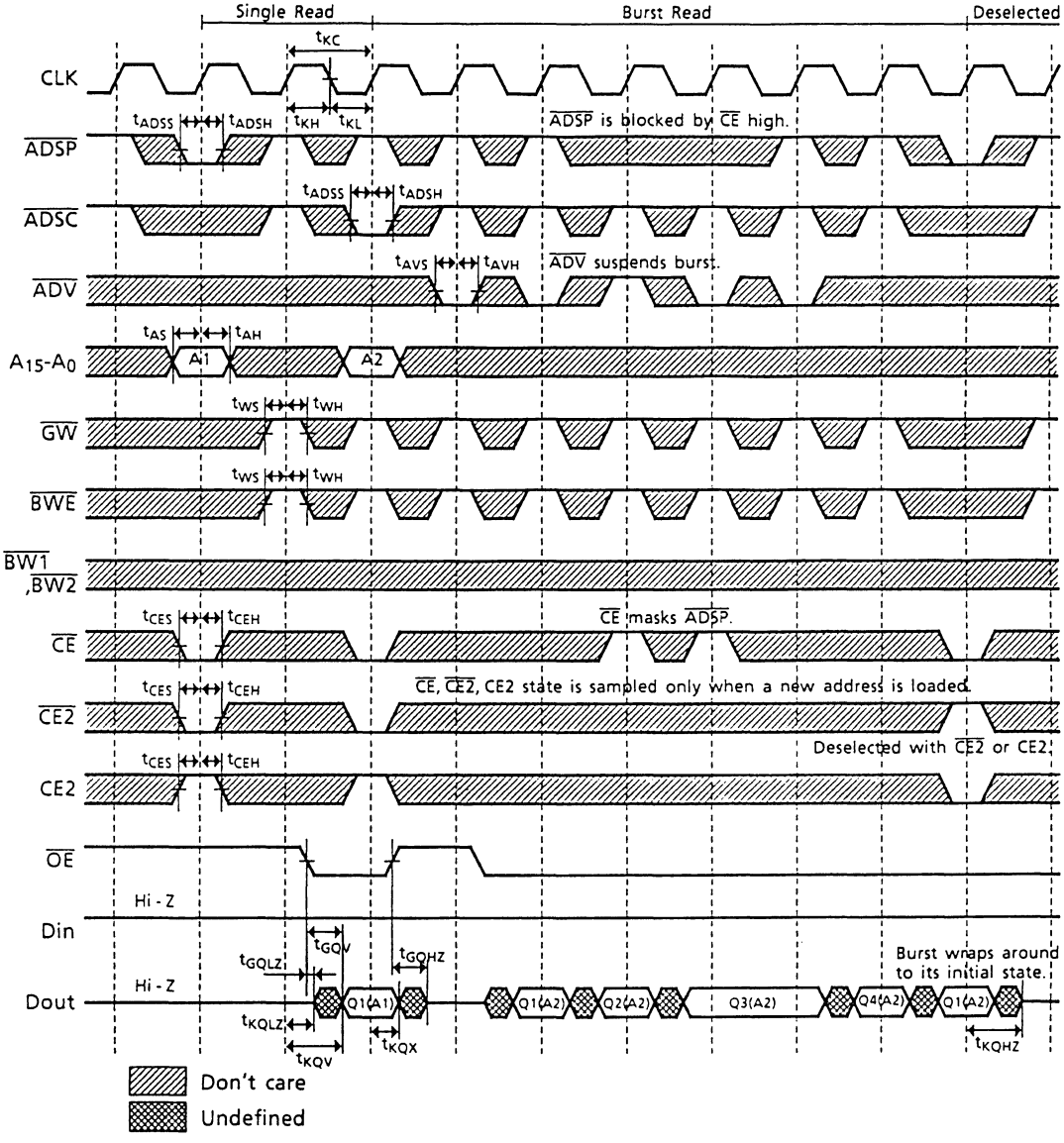


Figure 1.

Timing Waveforms

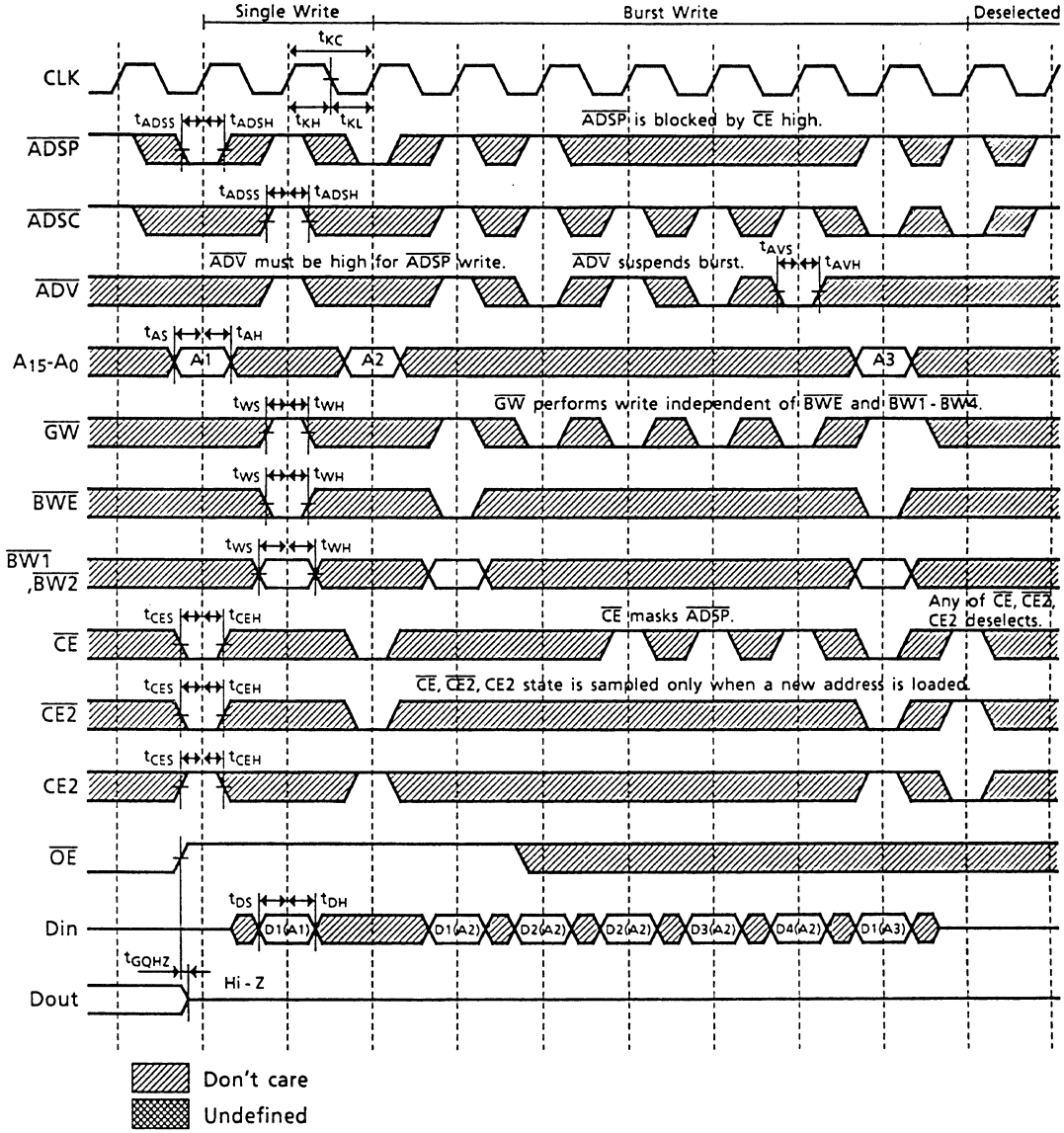
Read Cycle



Note

1. Q1(A2) represents output data from 1st burst address starting from address A2. Q2(A2) represents output data from 2nd burst address starting from address A2.
2. ZZ is Low.

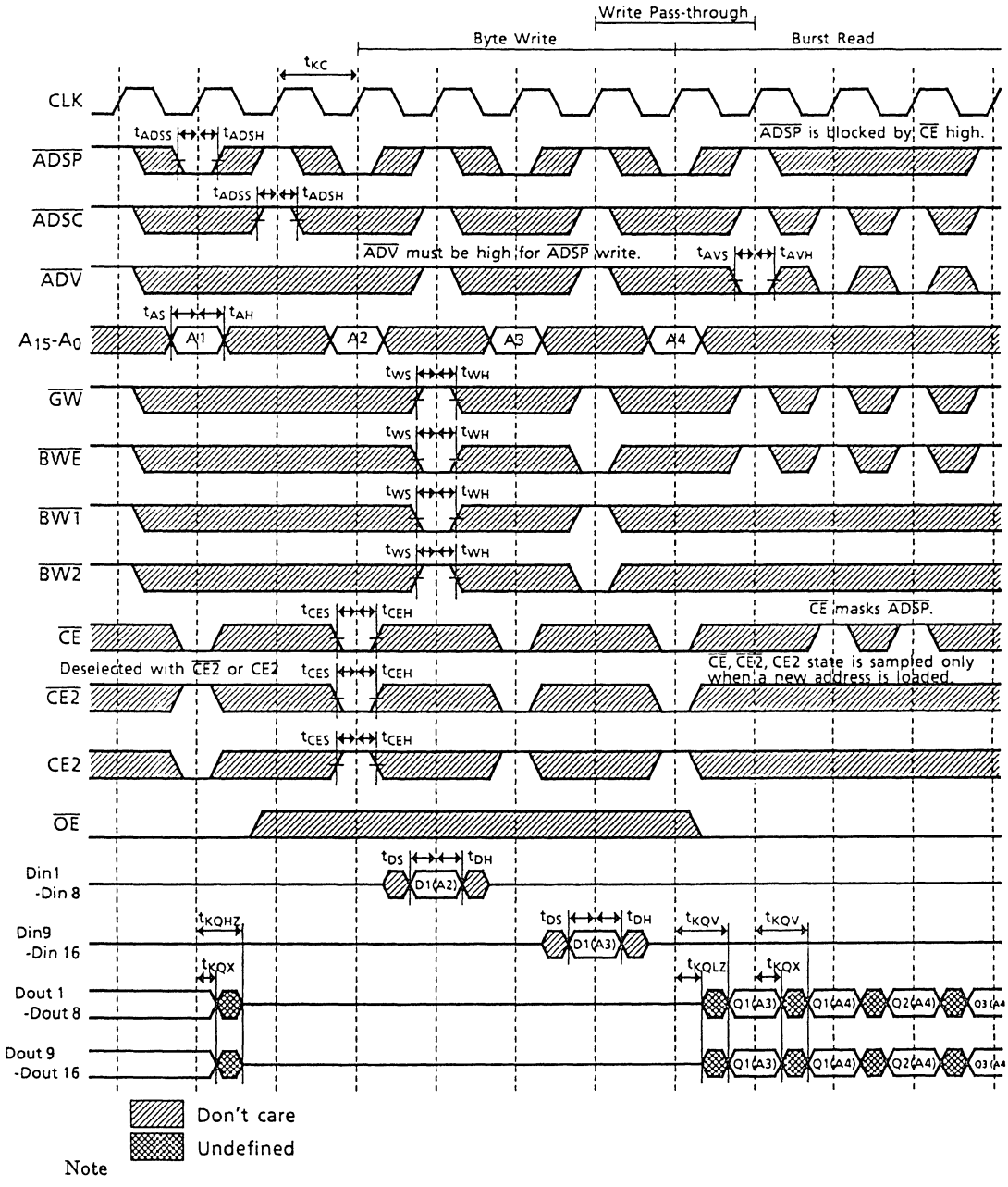
Write Cycle



Note

1. D1(A2) represents input data for 1st burst address starting from address A2. D2(A2) represents input data for 2nd burst address starting from address A2.
2. ZZ is Low.

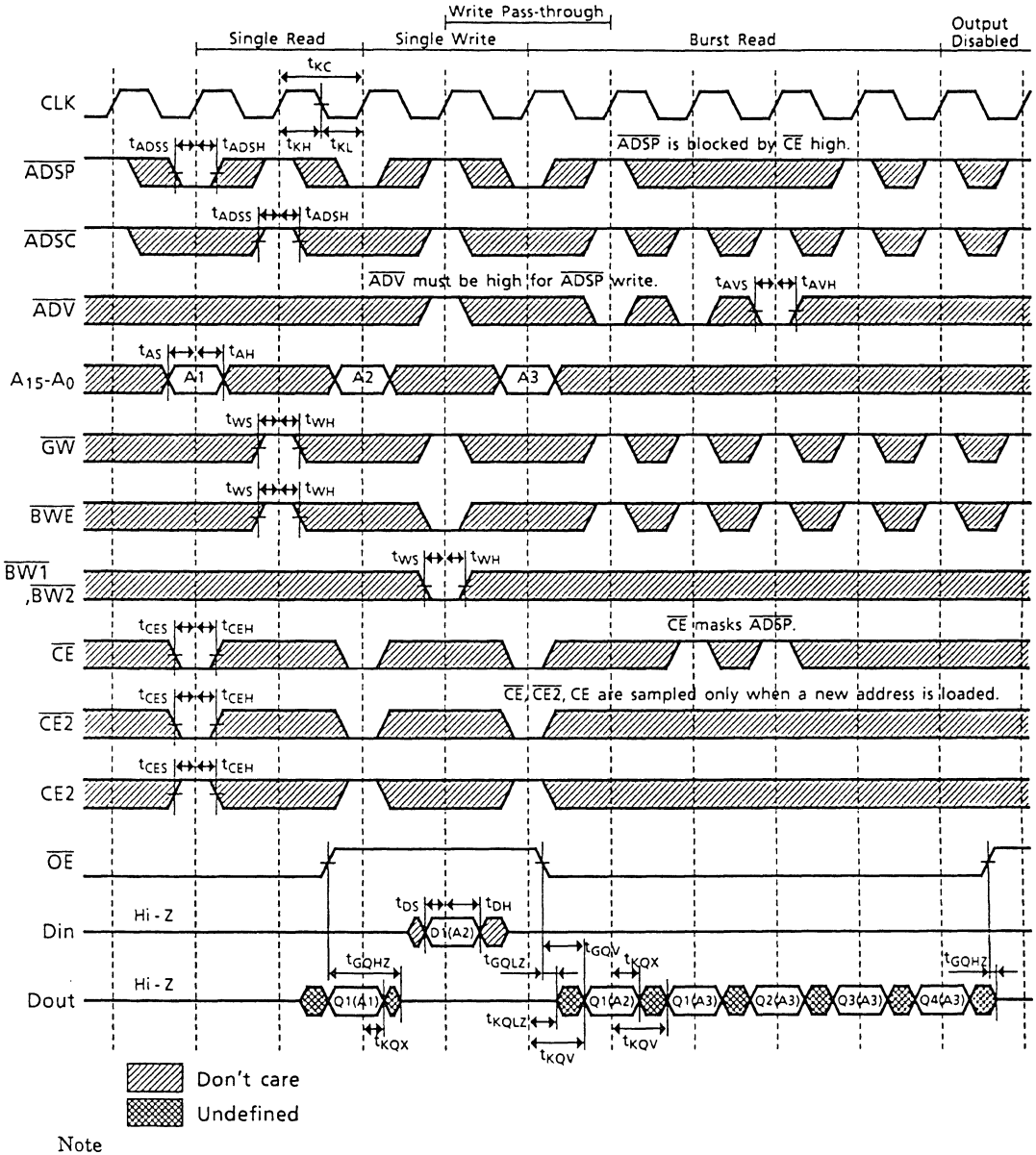
Write Cycle (Byte Write Timing)



Note

1. ZZ is Low.

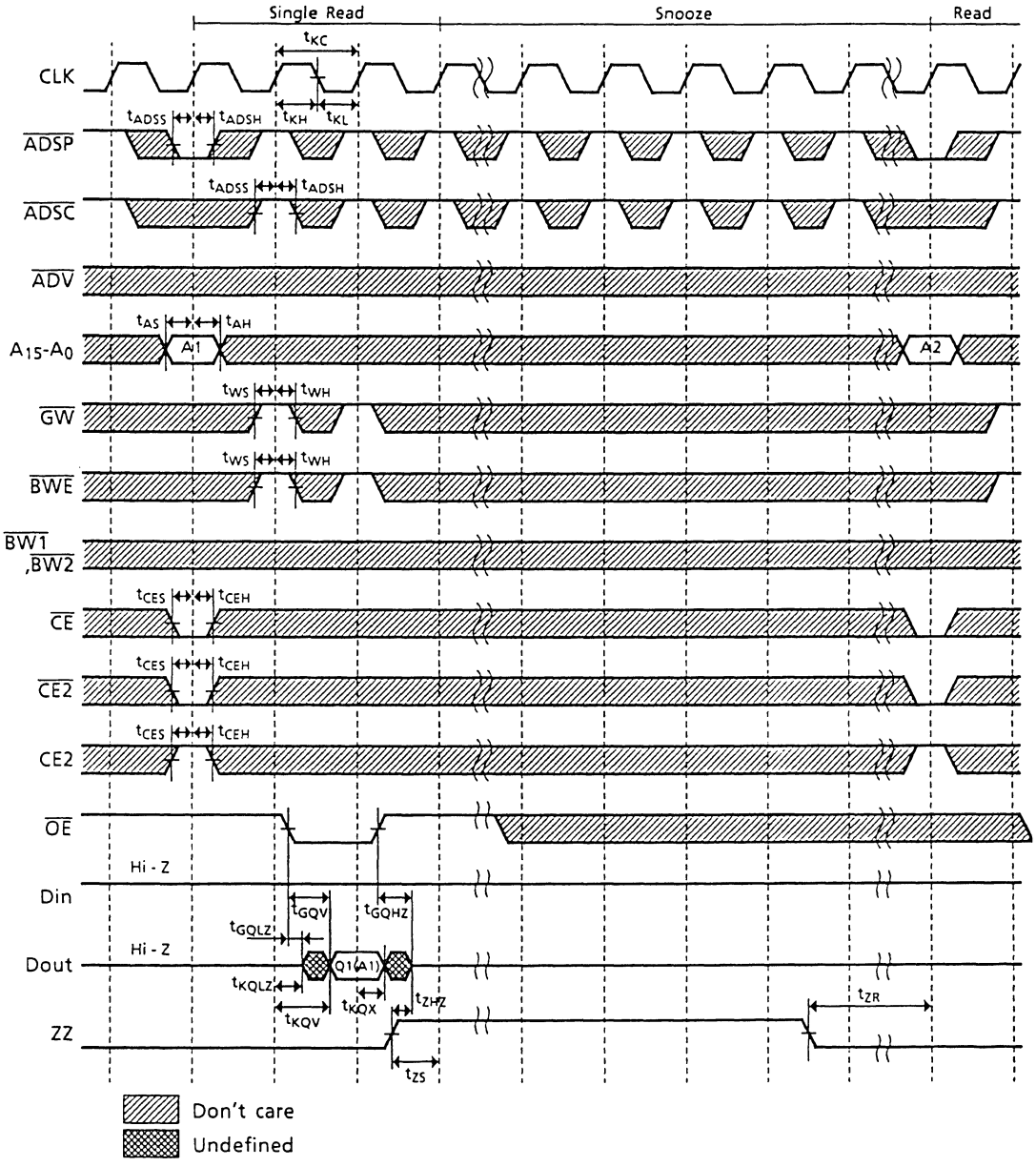
Read/Write Cycle



Note

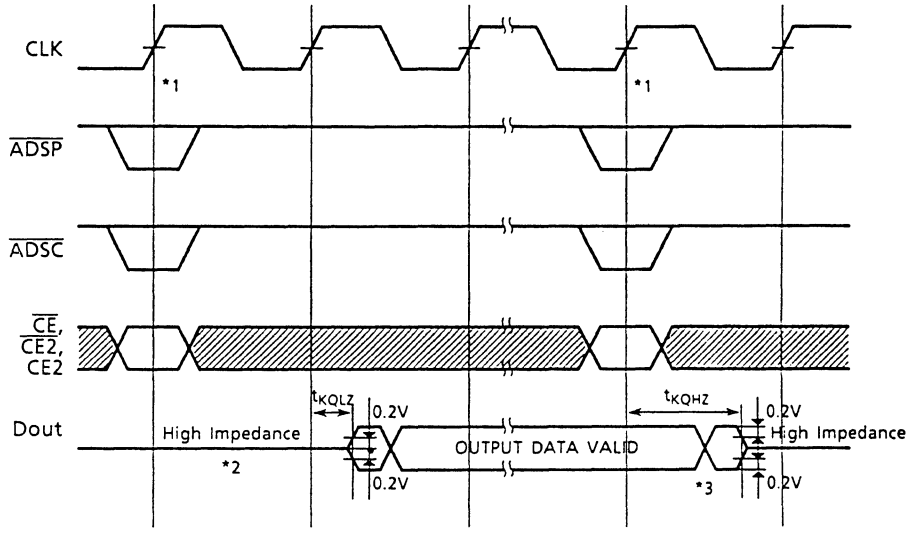
1. When a write operation follows a read operation, $\overline{OE}$ must be driven high prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$) and before input data is applied to avoid data bus contention.
2. ZZ is Low.

Snooze Cycle



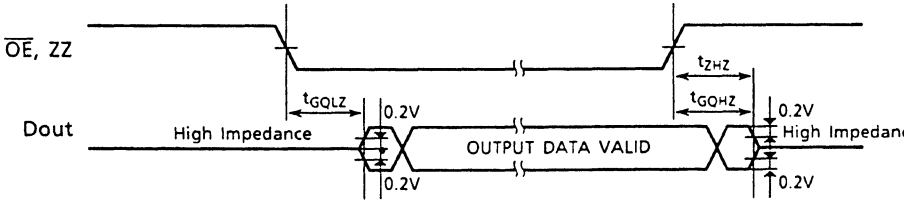
NOTE: 1. Don't apply opposite phase data to the I/O pins when they are in the output state.
2. Output enable and output disable times are specified as follows with the output load shown in Figure 1.

(a) t_{KQLZ}, t_{KQHZ}



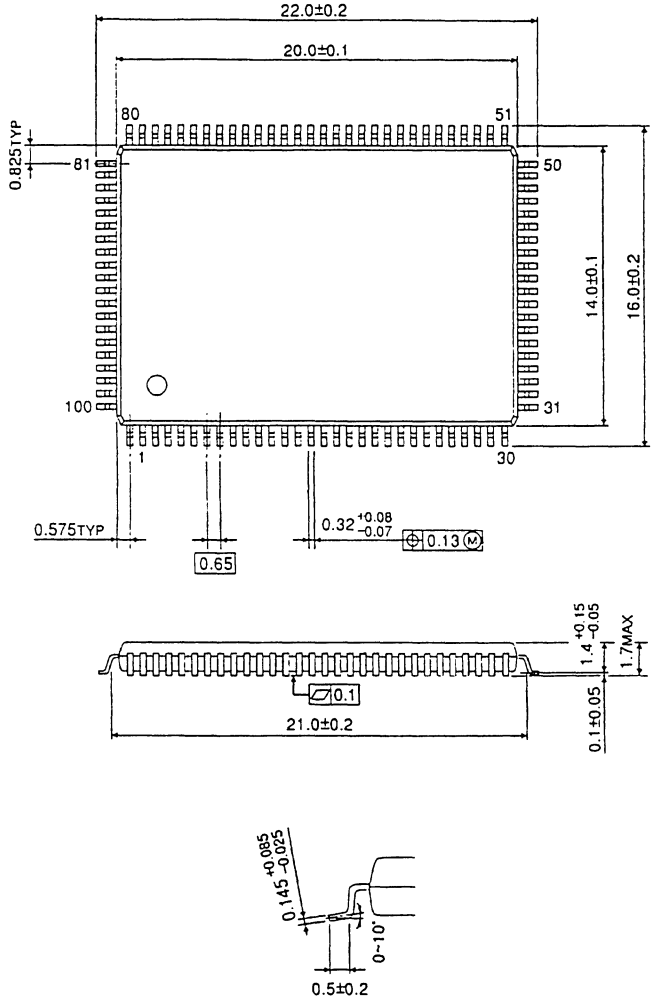
*1: The input states are defined in the Synchronous Input Truth Table.
*2: If the device was previously deselected, when the device is selected, the output remains in a high impedance state in the present clock cycle regardless of $\overline{OE}$ because of the output enable delay register. Valid data appears in the second clock cycle when $\overline{OE}$ is low.
*3: When the device is deselected, the output goes into a high impedance state in the present clock cycle regardless of $\overline{OE}$.

(b) t_{GQLZ}, t_{GQHZ}, t_{ZHZ}



Outline Drawings **Unit in mm**

Plastic LQFP (LQFP100-P-1420)



Weight : 0.56g (Typ.)

Notes

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32,768 WORD x 32 BIT SYNCHRONOUS PIPELINE BURST SRAM

Description

The TC55V1325FF is a 1,048,576 bit synchronously pipelined burst SRAM that is organized as 32,768 words by 32 bits and designed for use in a secondary cache to support MPUs which have burst functions.

The TC55V1325FF integrates a 2-bit burst address counter and control logic with a 32K x 32 static RAM. All inputs, except the Output Enable ($\overline{OE}$) input, are synchronous with either the rising edge of the clock (CLK) input.

The read operation can be initiated with either the address status processor ($\overline{ADSP}$) input or the address status controller ($\overline{ADSC}$) input. Subsequent burst addresses can be generated internally and are controlled by the address advance ($\overline{ADV}$) input.

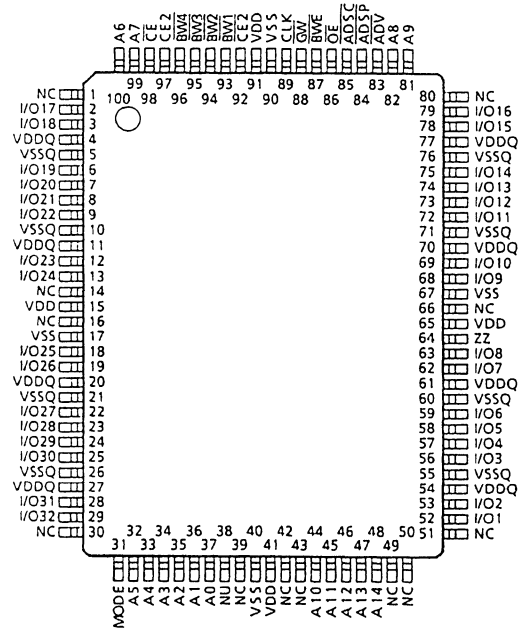
The write operation is internally self-timed and is initiated by the rising edge of the clock (CLK) input. Byte Write Enables ($\overline{BW1}$ - $\overline{BW4}$) allow a one to four byte write operation according to their logic states.

The TC55V1325FF operates from a single 3.3V power supply, and is packaged in a low profile 100-pin plastic QFP (LQFP).

Features

- Organization: 32K words x 32 bits
- Fast cycle time: 15ns min. (66.7MHz)
- Fast access time: 8ns (max.) (Clock to data output)
- Pipelined burst operation
- 2-bit burst address counter (Interleaved Burst or Linear Burst Sequences)
- Synchronous self-timed write (Global Write and Byte Write)
- LVTTL compatible interface
- Package:
  - 100-pin LQFP (0.65mm pitch, 1.6mm height typ.): LQFP100-P-1420 (Weight: 0.56g typ.)

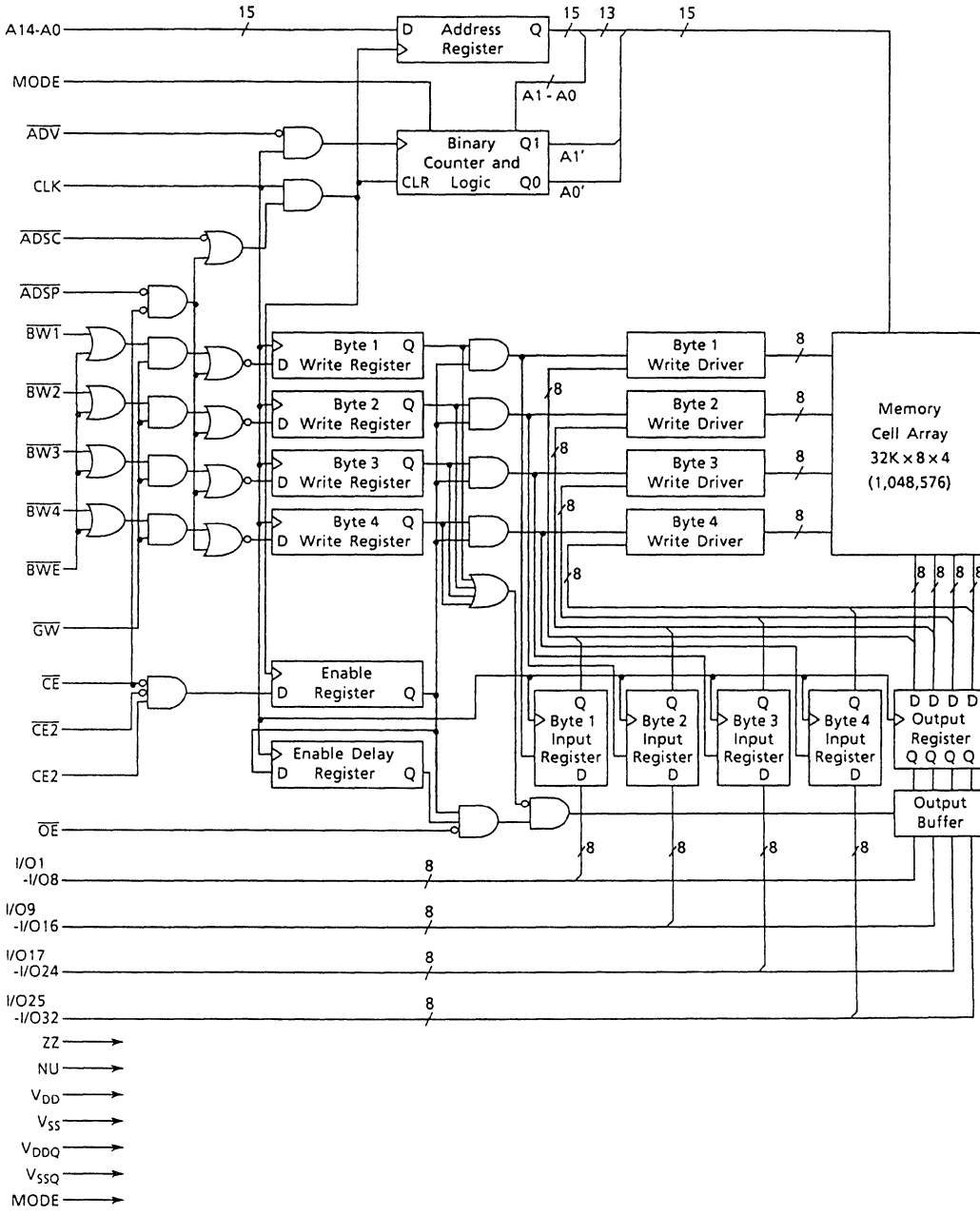
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O32	Data Inputs /Outputs
CLK	Clock Input
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable Inputs
$\overline{ADSP}$	Address Status Processor Input
$\overline{ADSC}$	Address Status Controller Input
$\overline{ADV}$	Address Advance Input
$\overline{GW}$	Global Write Enable Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{BW1}$ ~ $\overline{BW4}$	Byte Write Enable Inputs
$\overline{OE}$	Output Enable Input
MODE	Mode Select Input
ZZ	Snooze Input
NU	Not Usable Input
V_{DD}, V_{DDQ}	Power
V_{SS}, V_{SSQ}	Ground

Block Diagram



Pin Descriptions

Pin Number	Symbol	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0 - A14	Input (Synchronous)	Synchronous Address Inputs. These address inputs are registered on the rising edges of CLK. All address inputs must meet the setup and hold times for all rising edges of CLK when the chip is enabled.
93, 94, 95, 96	BW1, BW2, BW3, BW4	Input (Synchronous)	Synchronous Byte Write Enables. These inputs are active low and control byte write operations when BWE is low. BW1 controls I/O1 - 8. BW2 controls I/O9 - 16. BW3 controls I/O17 - 24. BW4 controls I/O25 - 32. For byte write operations, if any of these four inputs are low, all outputs are in high impedance.
87	$\overline{BWE}$	Input (Synchronous)	Synchronous Byte Write Enable. This input is active low and controls byte write operations.
88	$\overline{GW}$	Input (Synchronous)	Synchronous Global Write. This input is active low and controls a 32bit write operation independent of the BWE and BW1 - BW4 inputs.
89	CLK	Input	Reference Clock. All synchronous input signals are registered on all rising edges of CLK. All synchronous signal timings are measured from the rising edges of CLK. All synchronous input signals must meet the setup time and hold times referenced to the rising edges of CLK.
83	$\overline{ADV}$	Input (Synchronous)	Synchronous Burst Advance. This signal is active low and controls the internal burst address counter after the external address is loaded. When the signal is low, the internal burst address is not advanced. If a write operation initiated by ADSP is desired, this signal must be high to write the loaded address at the rising edge of the first clock after an assertion of ADSP.
84	$\overline{ADSP}$	Input (Synchronous)	Synchronous Address Status Processor. The signal is active low. This signal controls the burst start by registering the new external address. The write enables (GW, BWE, BW1 - BW4) are ignored at the assertion of ADSP and a read operation is initiated. A subsequent operation is dependent on the write enables at the rising edge of the first clock after an assertion of ADSP. This signal is ignored if CE is high.
85	$\overline{ADSC}$	Input (Synchronous)	Synchronous Address Status Controller. This signal is active low. This signal initiates a burst read or write depending on the write enables (GW, BWE, BW1 - BW4) by registering the new external address.
98	$\overline{CE}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable) and the internal use of $\overline{ADSP}$. This signal is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (Synchronous)	Synchronous Chip Enable. This signal is active low. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.
97	CE2	Input (Synchronous)	Synchronous Chip Enable. This signal is active high. This signal controls the chip status (enable or disable). This signal is sampled only when a new external address is loaded. This input can be used for memory address depth expansion.
86	$\overline{OE}$	Input (Asynchronous)	Asynchronous Output Enable. This signal is active low and controls all 32bit I/O buffers. This signal must be high for the time write data is driven prior to the assertion of the byte write enables (GW, BWE, BW1 - BW4) following a read operation.

Pin Number	Symbol	Type	Description
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	I/O1 - I/O32	Input /Output (Synchronous)	Synchronous Data Inputs/Outputs. Byte1 is I/O1 - I/O8, Byte2 is I/O9 - I/O16, Byte3 is I/O7 - I/O24, Byte4 is I/O25 - I/O32
31	MODE	Input (Asynchronous)	Mode Select. This signal is used to select the burst sequence. If this signal is high or not connected, the burst sequence is Interleaved Burst. If this signal is low, the burst sequence is Linear Burst. This input is internally pulled up. Altering the input state while the device is operating is prohibited.
64	ZZ	Input (Asynchronous)	Snooze. This signal is active high and is used to place the device into sleep mode, which is a low power standby mode. If this signal is low or not connected, the device is in an active state. If this signal is high, the device is in a sleep state, and the memory data is retained. The device wakes up when a read or write operation is initiated by $\overline{ADSP}$ or $\overline{ADSC}$ after deasserting this signal. This input must be connected to V_{SS} when ZZ mode is not used.
38	NU	Input (Asynchronous)	Not Usable. This signal is used only by the manufacturer. This signal must be low or not connected. This input is internally pulled down.
1, 14, 16, 30, 39, 42, 43, 49, 50, 51, 66, 80	NC	–	No Connection. These inputs are not internally connected. Pin numbers 49 and 50 are reserved for future device expansion.
15, 41, 65, 91	V_{DD}	Supply	Power Supply.
17, 40, 67, 90	V_{SS}	Ground	Ground.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	Output Buffer Power Supply.
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Ground	Output Buffer Ground.

Operation Mode

(1) Synchronous Input Truth Table

Operation	CLK	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$ [4]	ZZ [4]	ADDRESS USED	I/O [5]	CURRENT [2]
Begin Burst Read	L → H	L	L	H	L	x	x	x	L	External Address	Dout (n)	I_{DDO1}
	L → H	L	L	H	H	L	x	H	L			
Continue Burst Read	L → H	x	x	x	H	H	L	H	L	Next Burst Address	Dout (n)	I_{DDO1}
	L → H	H	x	x	L [6]	H	L	H	L			
Suspend Burst Read	L → H	x	x	x	H	H	H	H	L	Current Burst Address	Dout (n)	I_{DDO2}
	L → H	H	x	x	L [6]	H	H	H	L			
Begin Burst Write	L → H	L	L	H	H	L	x	L	L	External Address	Din (p)	N/A
	L → H	x	x	x	H	H	H	L	L	Current Burst Address		N/A
	L → H	H	x	x	L [6]	H	H	L	L			
Continue Burst Write	L → H	x	x	x	H	H	L	L	L	Next Burst Address	Din (p)	N/A
	L → H	H	x	x	L [6]	H	L	L	L			
Suspend Burst Write	L → H	x	x	x	H	H	H	L	L	Current Burst Address	Din (p)	N/A
	L → H	H	x	x	L [6]	H	H	L	L			
Deselected	L → H	H	x	x	x	L	x	x	L	None	Hi - Z (p)	I_{DDS2}
	L → H	L	H	x	L	x	x	x	L			
	L → H	L	x	L	L	x	x	x	L			
	L → H	L	H	x	H	L	x	x	L			
	L → H	L	x	L	H	L	x	x	L			
Snooze	L → H	x	x	x	x	x	x	x	H	None	Hi - Z (p)	I_{DDS3}

Note:
1. ZZ input is asynchronous, but is included in this table.
2. Consumption current does not include output buffer current.
3. H is logical High and L is logical Low. X is High or Low.
4. $\overline{WRITE}$ = L means any one or more byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.
5. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is present cycle.
6. When $\overline{CE}$ = H, $\overline{ADSP}$ is disabled ($\overline{ADSP}$ = X). $\overline{ADSP}$ = L to avoid redundancy with the previous truth table entry when $\overline{CE}$ = H and $\overline{ADSP}$ = H.

(2) Partial Truth Table for Write Enables (Synchronous Input)

Operation	CLK	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	I/O1 - I/O8	I/O9 - I/O16	I/O17 - I/O24	I/O25 - I/O32
Read	L → H	H	H	x	x	x	x	Dout (n)	Dout (n)	Dout (n)	Dout (n)
	L → H	H	L	H	H	H	H	Dout (n)	Dout (n)	Dout (n)	Dout (n)
Write	L → H	L	x	x	x	x	x	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	L	L	L	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	H	H	H	Din (p)	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)
				H	L	H	H	Hi - Z (p)	Din (p)	Hi - Z (p)	Hi - Z (p)
				H	H	L	H	Hi - Z (p)	Hi - Z (p)	Din (p)	Hi - Z (p)
				H	H	H	L	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)	Din (p)
				The other 11 combinations of BW1 to BW4 are also effective. BW1 controls I/O1 - I/O8. BW2 controls I/O9 - I/O16. BW3 controls I/O17 - I/O24. BW4 controls I/O25 - I/O32.						

Note: 1. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is present cycle.

(3) Asynchronous Truth Table

Operation	$\overline{OE}$	ZZ	I/O1 - I/O32
Read	L	L	Dout
	H	L	Hi - Z
Write	x	L	Din, Hi - Z
Deselected	x	L	Hi - Z
Snooze	x	H	Hi - Z

(4) Write Pass-through Truth Table

Previous Cycle				Present Cycle											Next Cycle
Operation	Addr.	$\overline{WRITE}$	I/O	Operation	Addr.	$\overline{WRITE}$	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	I/O	I/O
Write Cycle	Ak	L	Dn (Ak)	ADSP Initiated Read Cycle	Am	x	L	L	H	L	x	x	L	Qn (Ak)	Q1 (Am)
				ADSC Initiated Read Cycle	Am	H	L	L	H	H	L	x	L		
				Continue Read Cycle	x	H	x	x	x	H	H	L	L		Qn + 1 (Ak)
					x	H	H	x	x	L	H	L	L		

Note: 1. Dn (Ak) represents input data for the n-th burst address starting from address Ak.
2. Qn (Ak) represents output data from the n-th burst address starting from address Ak.
3. n = 1, 2, 3, or 4.
4. $\overline{WRITE}$ = L means any one or more byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low or $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.

(5) Interleaved Burst Sequence (MODE input = NC or V_{DD})

Bit Order: A_{14} A_{13}..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
xx..... xx00	xx..... xx01	xx..... xx10	xx..... xx11
xx..... xx01	xx..... xx00	xx..... xx11	xx..... xx10
xx..... xx10	xx..... xx11	xx..... xx00	xx..... xx01
xx..... xx11	xx..... xx10	xx..... xx01	xx..... xx00

The burst address wraps around to its initial state.

(6) Linear Burst Sequence (MODE input = V_{SS})

Bit Order: A_{14} A_{13}..... A_3 A_2 A_1 A_0
Lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
xx..... xx00	xx..... xx01	xx..... xx10	xx..... xx11
xx..... xx01	xx..... xx10	xx..... xx11	xx..... xx00
xx..... xx10	xx..... xx11	xx..... xx00	xx..... xx01
xx..... xx11	xx..... xx00	xx..... xx01	xx..... xx10

The burst address wraps around to its initial state.

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	-0.5 ~ V_{DD}	V
V_{IN}	Input Terminal Voltage	-0.5* ~ 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5* ~ V_{DDQ} + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

*: -1.5V with a pulse width of 20% • t_{KC} min (4ns max)
**: V_{DDQ} + 1.5V with a pulse width of 20% • t_{KC} min (4ns max)

DC Recommended Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.1	3.3	3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	3.1	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3**	V
V_{IH1}	Input High Voltage for MODE pin	V_{DD} - 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3*	–	0.8	V
V_{IL1}	Input Low Voltage for MODE and NU pins	-0.5	0.0	0.3	V

* : -1.0V with a pulse width of 20% • t_{KC} min (4ns max)
** : V_{DD} + 1.0V with a pulse width of 20% • t_{KC} min (4ns max)
Note: NU pin must be low or not connected.

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.1V ~ 3.6V)

SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current (Except MODE, ZZ, NU pins)		V_{IN} = 0 ~ V_{DD}	–	–	±1	μA
I_{LO}	Output Leakage Current		Device Deselected or Output Deselected, V_{OUT} = 0 ~ V_{DD}	–	–	±1	μA
I_I	Input Current	MODE pin	V_{IN} = V_{DD} ~ V_{DD} ~ 0.3V	-1	–	1	μA
			V_{IN} = 0 ~ 0.3V	-100	–	1	
		ZZ pin	V_{IN} = V_{DD} ~ 2.0V	-1	–	100	
			V_{IN} = 0 ~ 0.8V	-1	–	20	
			V_{IN} = 0 ~ 0.3V	-1	–	1	
		NU pin	V_{IN} = 0 ~ 0.3V	-1	–	1	
V_{OH}	Output High Voltage		I_{OH} = -8mA	2.4	–	–	V
			I_{OH} = -100μA	V_{DD} - 0.2	–	–	
V_{OL}	Output Low Voltage		I_{OL} = 8mA	–	–	0.4	
			I_{OL} = 100μA	–	–	0.2	
I_{DDO1}	Operating Current		Device Selected, I_{OUT} = 0 mA, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	220	mA
I_{DDO2}	Operating Current (Idle)		Device Selected, I_{OUT} = 0 mA, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	190	mA
I_{DDS1}	Standby Current (CLK running)		Device Selected, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{KC} min.	–	–	35	mA
I_{DDS2}	Standby Current		Device Selected, All inputs = V_{DD} - 0.2V or 0.2V, CLK frequency = 0Hz	–	–	2	mA
I_{DDS3}	Snooze Current		ZZ = V_{DD} - 0.2V, All inputs = V_{IH}/V_{IL}, CLK ≥ t_{RC} min.	–	–	2	mA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
	Input Capacitance for MODE, ZZ, NU pin	V_{IN} = GND	8	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = GND	7	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.1V ~ 3.6V)

SYMBOL	PARAMETER	TC55V1325FF-8		TC55V1325FF-10		TC55V1325FF-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{KC}	CLK Cycle Time	15	–	16	–	20	–	ns
t_{KH}	CLK High Pulse Width	5	–	5	–	6	–	
t_{KL}	CLK Low Pulse Width	5	–	5	–	6	–	
t_{KQV}	Access Time from CLK	–	8	–	10	–	12	
t_{KQX}	Output Hold Time from CLK	2	–	2	–	2	–	
t_{KQLZ}	Output Enable Time from CLK	5	–	5	–	5	–	
t_{KQHZ}	Output Disable Time from CLK	2	5	2	5	2	6	
t_{GQV}	Access Time from $\overline{OE}$	–	6	–	6	–	7	
t_{GQLZ}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	
t_{GQHZ}	Output Disable Time from $\overline{OE}$	2	5	2	5	2	6	
t_{AS}	Address Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{AH}	Address Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{ADSS}	$\overline{ADSP}$, $\overline{ADSC}$ Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{AAH}	$\overline{ADV}$ Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{AAS}	$\overline{ADV}$ Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{WS}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{WH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{CES}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Setup Time from CLK	2.5	–	2.5	–	3.0	–	
t_{CEH}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Hold Time from CLK	0.5	–	0.5	–	0.5	–	
t_{DS}	Data Setup Time CLK	2.5	–	2.5	–	3.0	–	
t_{DH}	Data Hold Time CLK	0.5	–	0.5	–	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	5	–	6	–	
t_{ZR}	ZZ Recovery Time	8	–	10	–	12	–	
t_{ZHZ}	Output Disable Time ZZ	0	12	0	12	0	14	

AC Test Conditions

Input Pulse Levels	3.0/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

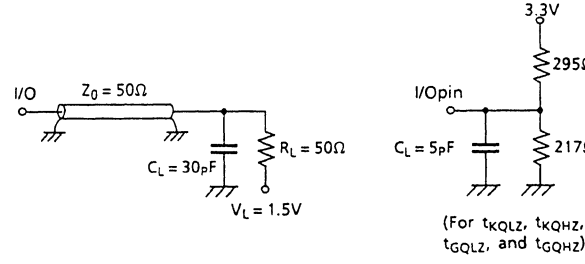
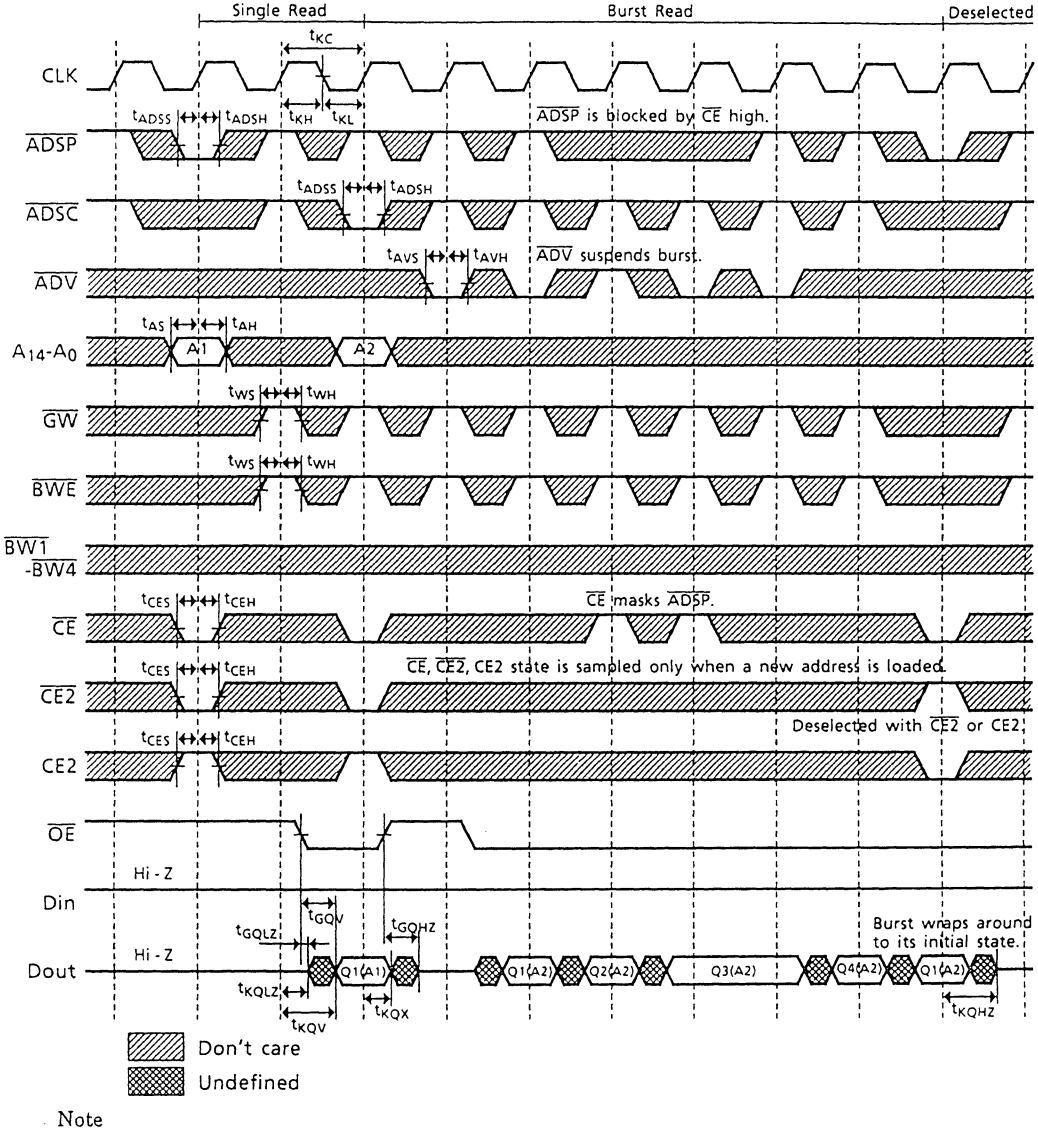


Figure 1.

Timing Waveforms

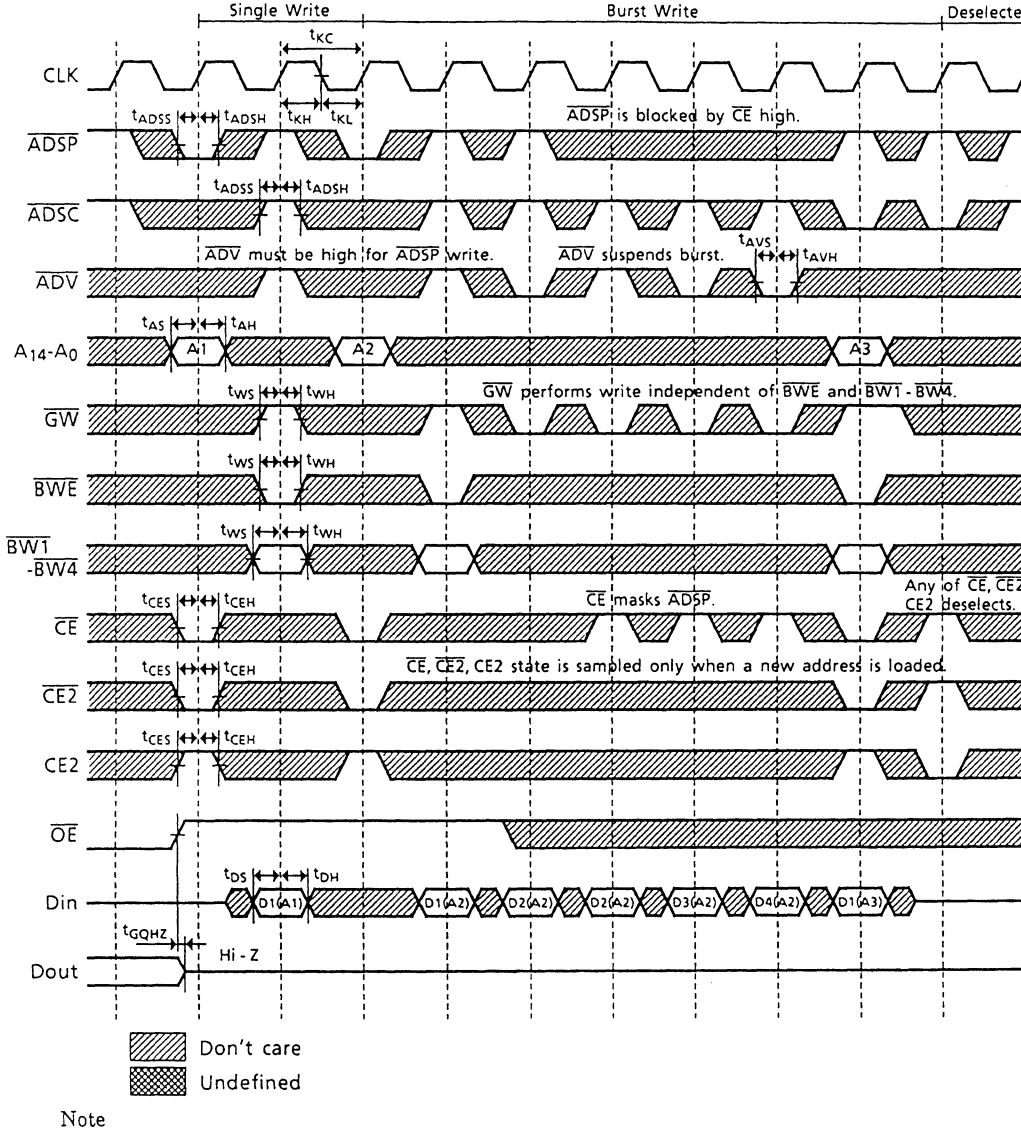
Read Cycle



Note

1. Q1(A2) represents output data from 1st burst address starting from address A2. Q2(A2) represents output data from 2nd burst address starting from address A2.
2. ZZ is Low.

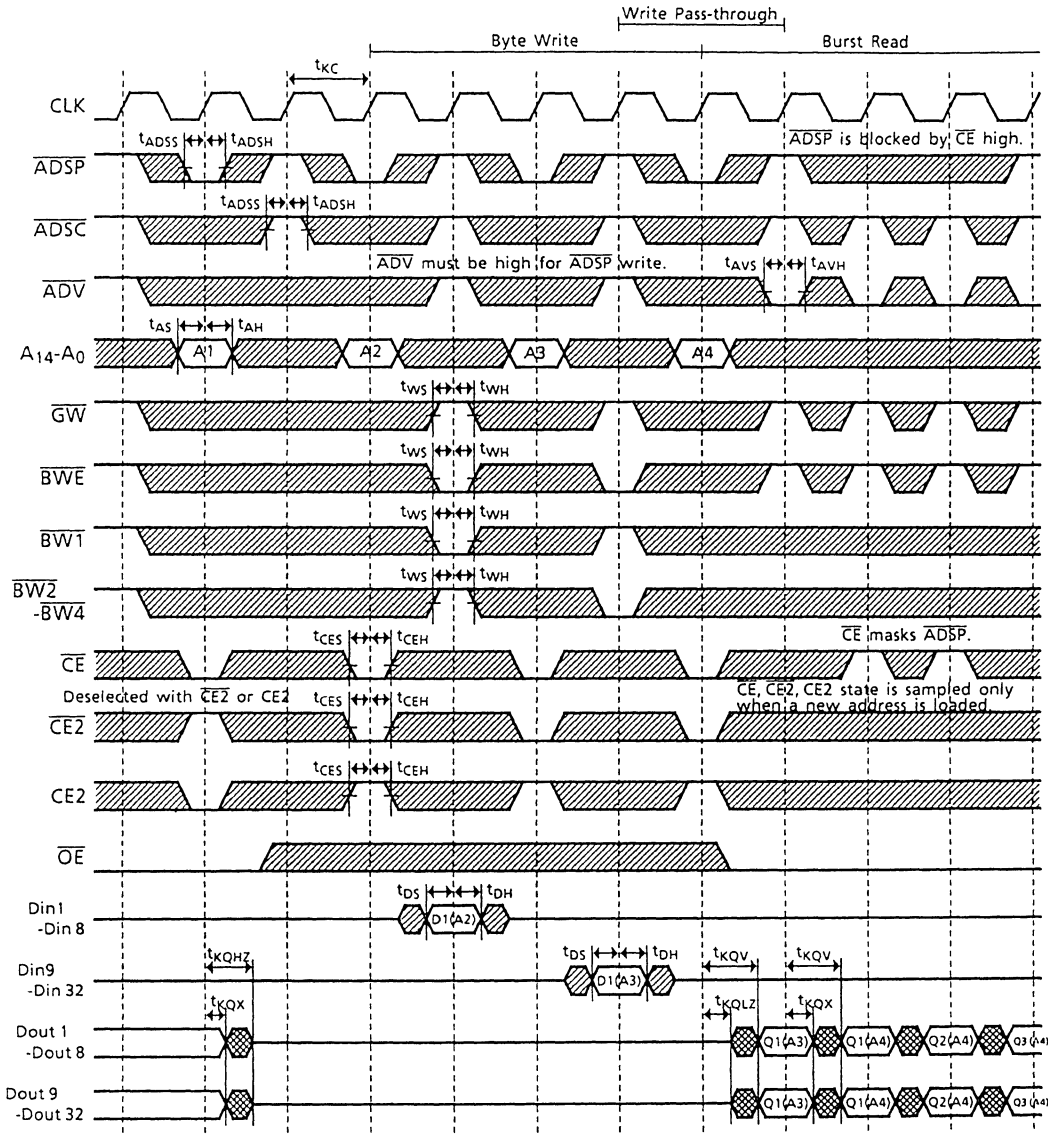
Write Cycle



Note

1. D1(A2) represents input data for 1st burst address starting from address A2. D2(A2) represents input data for 2nd burst address starting from address A2.
2. ZZ is Low.

Write Cycle (Byte Write Timing)

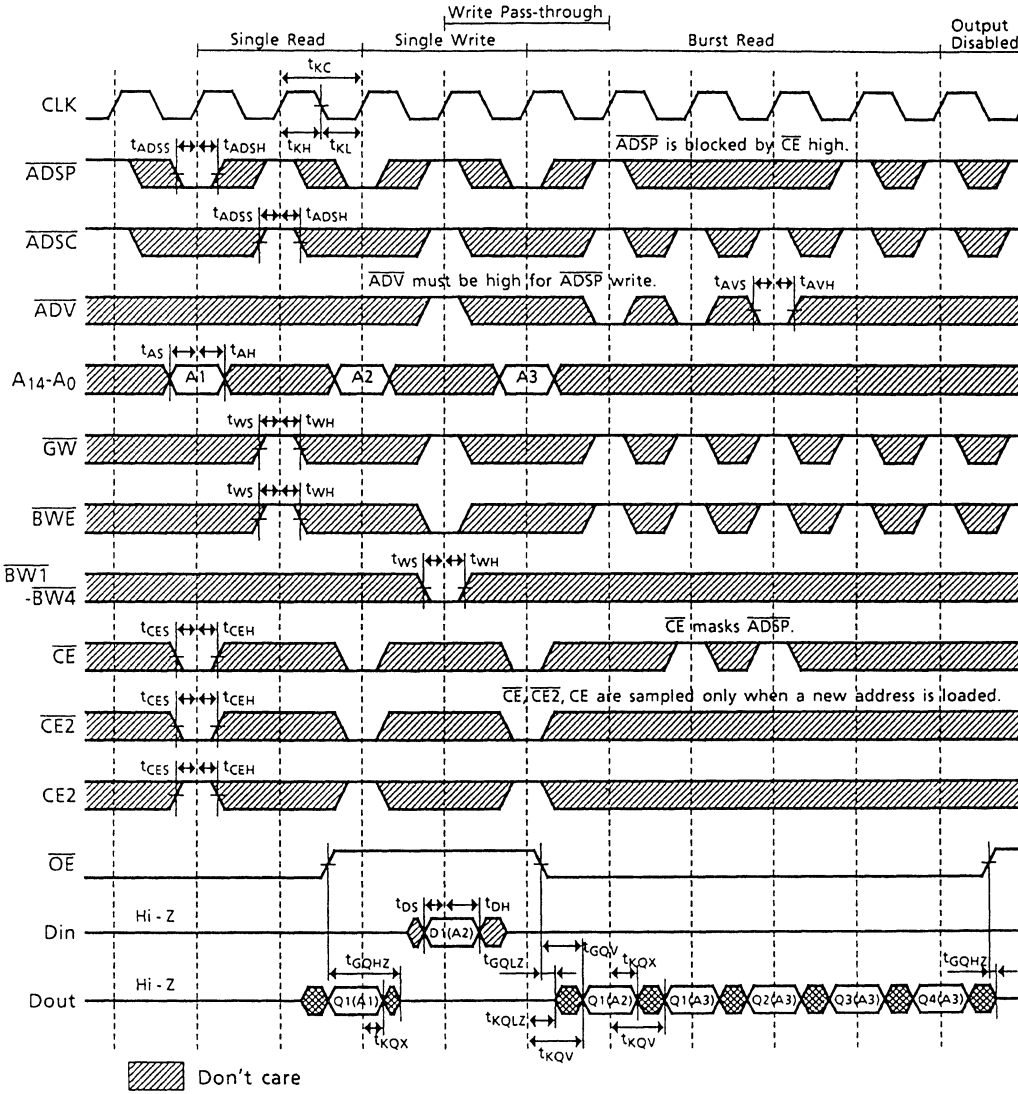


Note

1. ZZ is Low.

C. High Speed Synchronous RAM

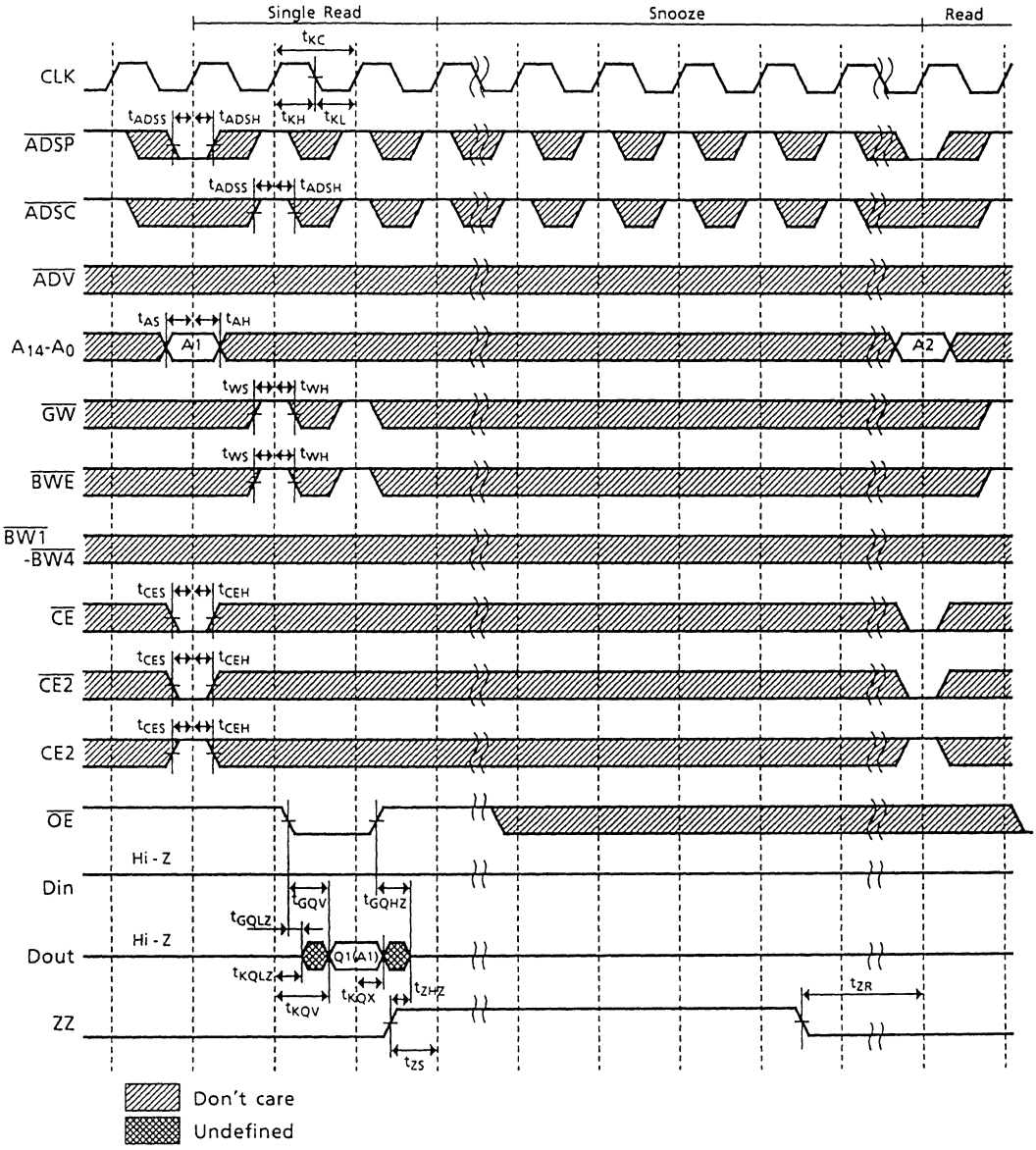
Read/Write Cycle



Note

1. When a write operation follows a read operation, $\overline{OE}$ must be driven high prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$) and before input data is applied to avoid data bus contention.
2. ZZ is Low.

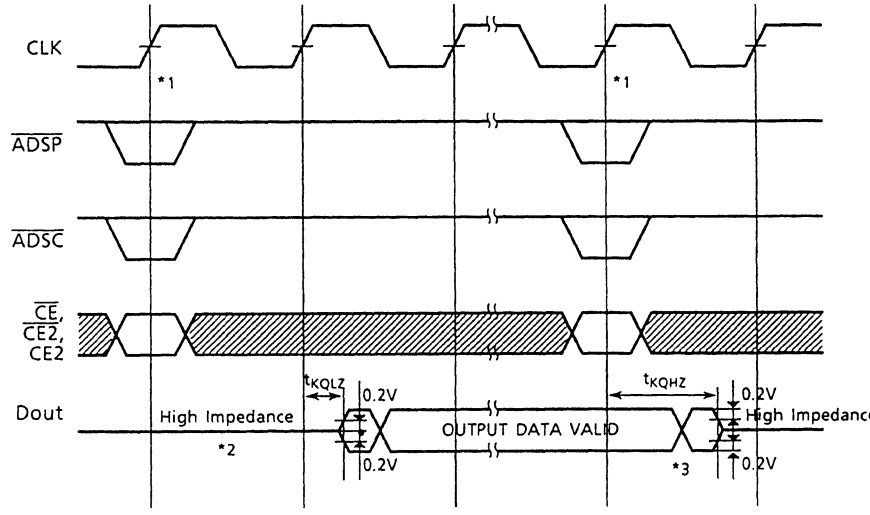
Snooze Cycle



C. High Speed Synchronous RAM

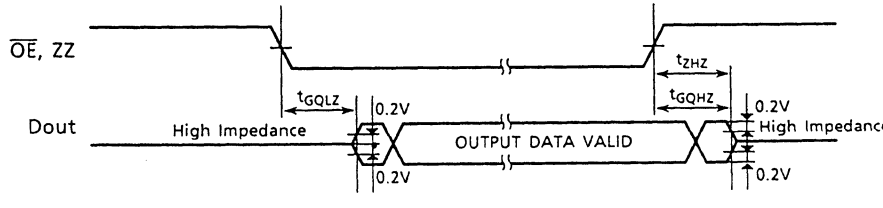
NOTE: 1. Don't apply opposite phase data to the I/O pins when they are in the output state.
2. Output enable and output disable times are specified as follows with the output load shown in Figure 1.

(a) t_{KQLZ}, t_{KQHZ}



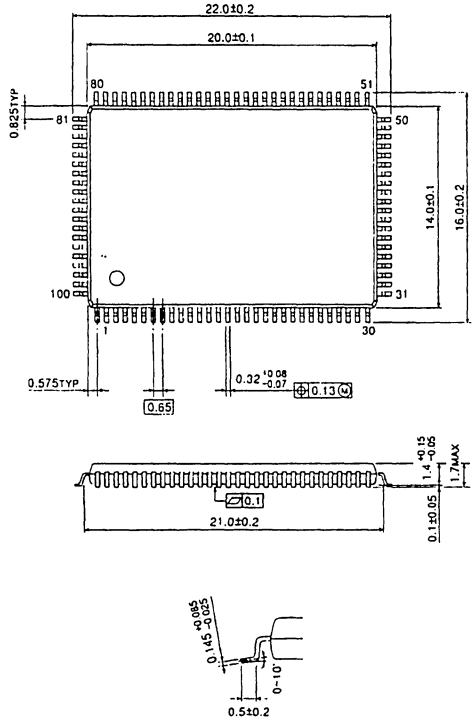
*1: The input states are defined in the Synchronous Input Truth Table.
*2: If the device was previously deselected, when the device is selected, the output remains in a high impedance state in the present clock cycle regardless of $\overline{OE}$ because of the output enable delay register. Valid data appears in the second clock cycle when $\overline{OE}$ is low.
*3: When the device is deselected, the output goes into a high impedance state in the present clock cycle regardless of $\overline{OE}$.

(b) t_{GQLZ}, t_{GQHZ}, t_{ZHZ}



Outline Drawings **Unit in mm**

Plastic LQFP (LQFP100-P-1420)



Weight : 0.56g (Typ.)

Notes

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Non-Volatile

TC58A040F

PRELIMINARY

4Mbit (4M x 1 BIT) CMOS AUDIO NAND EEPROM

Description

The TC58A040 is a single 5 volt 4M bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 256 bits x 128 pages x 128 blocks.

The device has a 256 bit static register which allows program and read data to be transferred between the register and the memory cell array in 256 bit increments. The erase operation is implemented in a single block unit (4k bytes).

The TC58A040 is suitable for digital recording systems such as digital answering machines and personal digital recorders.

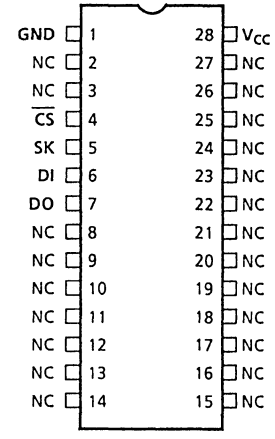
Features

- Organization
  - Memory cell array : 4M x 1
  - Page Buffer : 256 bits
  - Page size : 256 bits
  - Block size : 4k bytes
- Mode : Read, Auto program, Auto block erase, Status read
- Mode control : Serial input/output Command control
- Package : TC58A040F SOP28-P-450 (Weight: 0.81g Typ.)
- Power supply : V_{CC} = 5V±10%
- Access time
  - Cell array - Register : 25µs
  - Serial Read Cycle : 250ns
- Operating current
  - Read (500ns cycle) : 5mA typ.
  - Write : 15mA typ.
  - Erase : 10mA typ.
  - Standby : 50µA

Pin Names

DO	Serial Data Output
DI	Serial Data Input
SK	Serial Clock
$\overline{CS}$	Chip Select
NC	No Connection
V_{CC}/V_{SS}	Power Supply

Pin Connection (Top View)



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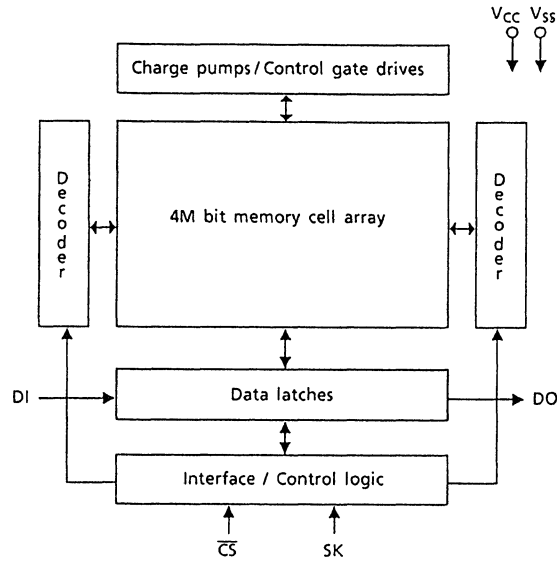
Block Diagram



Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power Supply	-0.6 ~ 7.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6V ~ V_{CC} + 0.5V (≤ 7V)	
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STG}	Storage Temperature	-55 ~ 150	
T_{OPR}	Operating Temperature	0 ~ 70	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	5	10	

*This parameter is periodically sampled and is not 100% tested.

Valid Blocks (1)

The number of valid blocks in the range Block 0 ~ Block 126 (2) is:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$N_{VP\,1}$	Number of Valid Blocks	117	TBD	127	Block

(1) The TC58A040 includes unusable blocks. Refer to notification (8) toward the end of this document.
(2) Block 127 is guaranteed to be good.

DC Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IH}	High Level Input Voltage	2.2	–	V_{CC} + 0.5	
V_{IL}	Low Level Input Voltage	-0.3*	–	0.8	

* -2V (pulse width ≤ 20ns).

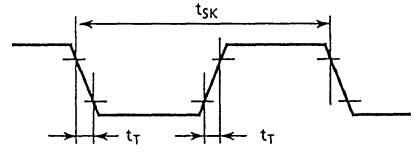
DC Operating Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{CC}	–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}	–	–	±10	
I_{CCO1}	Operating Current (Read Cycle)	t_{cycle} = 250ns	–	5	20	mA
I_{CCO2}	Operating Current (Read Cycle)	t_{cycle} = 1μs	–	–	10	
I_{CCO3}	Operating Current (Program)	–	–	15	60	
I_{CCO4}	Operating Current (Erase)	–	–	10	40	
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	–	500	μA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2V	–	–	50	
V_{OH}	High Level Output Voltage	I_{OH} = - 400μA	2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA	–	–	0.4	

AC Electrical Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{SK}	Serial Clock Cycle Time		250*	–	ns
t_{SKH}	SK High Time		120	–	
t_{SKL}	SK Low Time		120	–	
t_{CS}	$\overline{CS}$ High Time		250	–	
t_{CSS}	$\overline{CS}$ Setup Time	Relative to SK Rising edge	100	–	
t_{DIS}	DI Setup Time	Relative to SK Rising edge	50	–	
t_{CSH1}	$\overline{CS}$ Hold Time	t_{CSH1}: Relative to DO Rising edge	0	–	
t_{CSH2}	$\overline{CS}$ Hold Time	t_{CSH2}: Relative to SK Falling edge	20	–	
t_{DIH}	DI Hold Time	Relative to SK Rising edge	20	–	
t_{DF}	$\overline{CS}$ to DO in High Z		–	100	
t_{DH}	DO Hold Time	Relative to SK Falling edge	0	–	
t_{PD}	Output Delay	Relative to SK Falling edge	–	100	
t_{SADD}	Set Address Time		–	200	µs
t_R	Page Read Transfer Time		–	25	
t_{SKB}	SK to DO (Busy)	Relative to SK Falling edge	–	200	ns

*t_T (transition time) = 5ns



Programming and Erasing Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PROG}	Programming time	–	300 ~ 1000	2000	µs
t_{BERASE}	Block erasing time	–	7	100	ms
$N_{W/E}$	Number of write/erase cycles	10^5	–	–	Cycles
N_{PP}*	Number of programming cycles on same master page	–	–	50	Cycles

* Refer to the partial page write operation.

Pin Description

Serial Data Input: DI

The DI pin is used for transferring in commands and data. Commands and data are latched on the rising edge of SK.

Serial Data Output: DO

The DO pin is used for transferring out status and data. Data is available t_{PD} after the falling edge of SK. DO indicates the internal state except during data output. A low level indicates that the device is busy. A high level indicates that the device is ready.

Chip Select: $\overline{CS}$

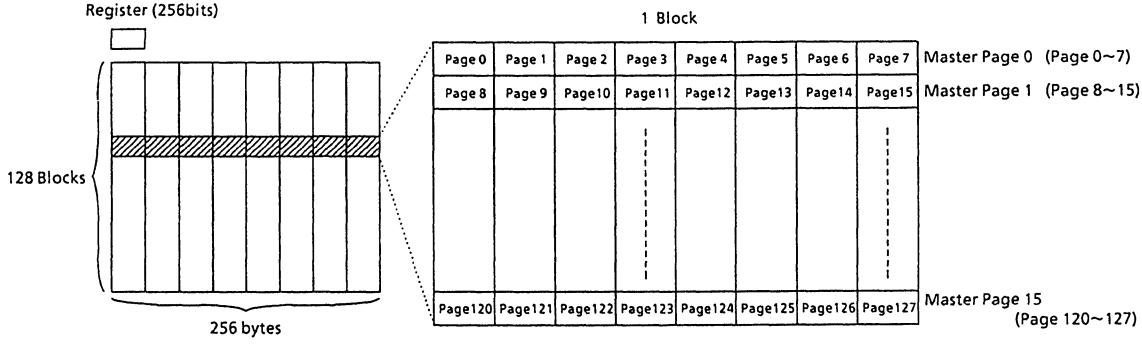
This signal enables the device. When this signal is high, the device ignores SK. This signal can be tied to ground when there is only one Audio-NAND device. The $\overline{CS}$ pin may be pulled high to reset the device.

Serial Clock: SK

This signal controls serial data input and output. Commands and data are latched on the rising edge of SK. Data is output on the falling edge of SK.

Organization

The TC58A040F is a 4M bit device organized as 128 blocks of 16 master pages. A master page is further segmented into 8 pages as shown in the following figure. The write and read operations are executed on a page basis and the erase is executed on a block basis.



1 page = 256 bits

1 master page = 8 pages = 256 bytes

1 block = 16 master pages = 128 pages = 4096 bytes

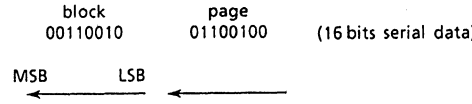
A page is the unit of reading and programming.
A block is the unit of erasure.
A master page is divided into 8 pages. These 8 pages are controlled by a common word line.

Address Assignment

The address is acquired through the DI pin using 16 consecutive clock cycles. The first 8 bits are the block address. The last 8 bits are the page address.

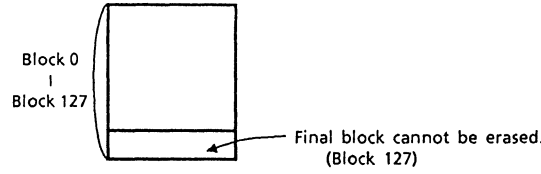
	Decimal	Binary
Block address	0 ~ 126	00000000 ~ 01111110
Set Address	0 ~ 127	00000000 ~ 01111111

Example: Page 100 in block 50



Write Once Block

The TC58A040F has 128 blocks (block 0 ~ 127). The final block (block 127) has been set aside as a read only block. Once data is written, this block cannot be erased. This block needs a special command for reading and writing. Block 127 may be used for storing system configuration information that cannot be lost.



Command Table

There are 12 commands in the TC58A040. All operations are controlled by these commands, shown in the following table.

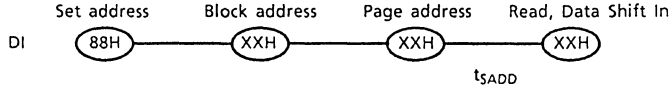
Instruction	Start Bit	Opcode	Reserved	Hex Command
Get Status	1	0000	000	80H
Set Address	1	0001	000	88H
Increment	1	0010	000	90H
Read	1	0011	000	98H
Write	1	0100	000	A0H
Erase	1	0101	000	A8H
Data Shift In	1	0110	000	B0H
Data Shift Out	1	0111	000	B8H
Write Enable	1	1100	000	E0H
Write Disable	1	1101	000	E8H
Write Last Block	1	1110	000	F0H
Read Last Block	1	1010	000	D0H

Commands

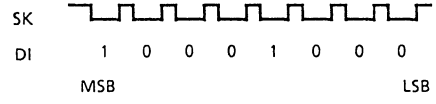
Set Address

The set address command defines which block and page of the memory is affected by an operation. The set address command is followed by two bytes, the first indicating the block number and the second indicating the page number. The set address command is usually followed by a read or a data shift in command. Between the page address byte and the next command there is a delay of t_{SADD}.

The address that is selected remains the active address until a new set address or increment command is given.



Example: If the 88H command is input, the MSB must be input first.



Increment

The increment command automatically increments the page address. When the last page in a block is selected, if the increment command is input, the address is set to 00H (Page 0) in the next block. However, if the last page in the last block (Block 126) is selected, the increment command will set the address to 00H (Page 0) in the same block (Block 126).

Read

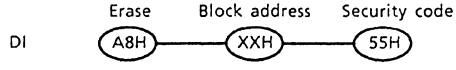
The read command transfers data from the selected page of the memory array into the on-chip buffer (256 bit shift register). The read command is usually followed by a data shift out command. There is a delay of t_R between the read command and the data shift out command as the data is transferred from the memory array to the on chip buffer.

Write

The write command programs data from the on-chip buffer into the selected page of the memory array. A security code (55H) follows the write command to ensure against accidental writes. Get status may be used to ensure that the operation was successful. The write command will be ignored if write disable has been set.

Erase

The erase command erases a selected block. The erase command is followed by the block address. A security code (55H) follows the block address to ensure against accidental erase. The get status command may be used to verify that the operation was successful. The erase command will be ignored if write disable has been set.



Get Status

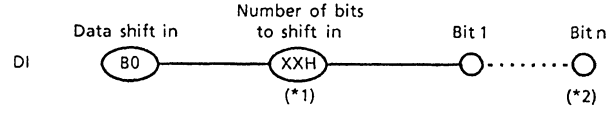
The get status command is used to output the status of the TC58A040. The eight status bits are defined as follows.

Bit	Status	Output
0 (LSB)	Ready/Busy	Ready "1" Busy "0"
1	Pass/Fail	Pass "1" Fail "0"
2	Write enable/Write disable	Write enable: "1" Write disable: "0"
3	Not used	Unknown "1" or "0"
4	Not used	Unknown "1" or "0"
5	Not used	Unknown "1" or "0"
6	Not used	Unknown "1" or "0"
7 (MSB)	Not used	Unknown "1" or "0"

The status is output LSB first.

Data Shift In

The data shift in command is used to shift data into the on chip buffer. The number of bits sent into the buffer is determined by an 8-bit argument following the command. The data shift in command is usually used prior to the write command.

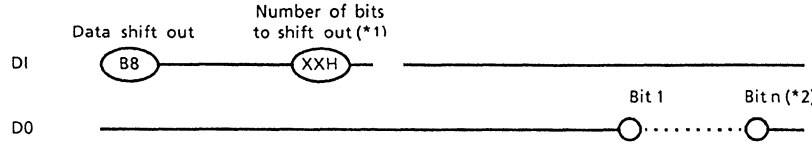


The value of (*1) is 1 less than the actual number of bits to be shifted in (*2).
Example:

Number of bits (*2)	n = 256	n = 128	n = 1
Number of bits argument (*1)	FFH = 11111111	7FH = 01111111	00H = 00000000

Data Shift Out

The data shift out command is used to shift data out of the on chip buffer. The number of bits sent out of the buffer is determined by an 8-bit argument following the command. The data shift out command is usually used after the read command.



The value of (*1) is 1 less than the actual number of bits to be shifted out (*2).
Example:

Number of bits (*2)	n = 256	n = 128	n = 1
Number of bits argument (*1)	FFH = 11111111	7FH = 01111111	00H = 00000000

Write Disable

The write disable command is used to prevent inadvertent writes or erases. Once this command is executed, all subsequent write or erase commands will not be accepted. The status read operation (get status command) can be used to determine whether the device is in the write enable or disable state.

Write Enable

The write enable command is used to cancel the write disable mode.

Read Last Block

The read last block command is used to read the contents in the final block (Block 127). The set address command and 2 address bytes are required to set the page address. The block address is automatically set to 127, so the first address byte is ignored.

Write Last Block

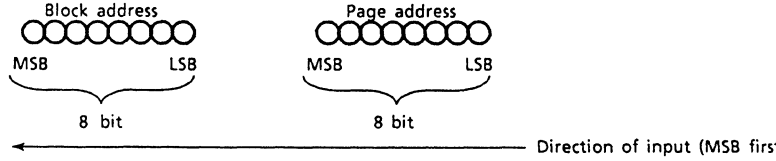
The write last block command is used to program into the selected page in the final block (Block 127). Once data is written into the last block, it cannot be erased. A security code (55H) follows the write last block command to ensure against accidental writes.

Device Operation

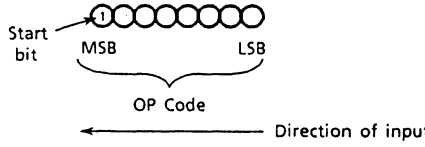
Input/Output Operation

The TC58A040 has separate input and output pins. Address, command and input data are input as serial data through DI. Status data and output data are output as serial data through DO. Input and output operations are as follows.

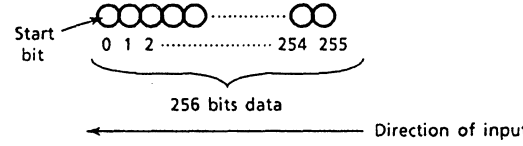
(1) Address input



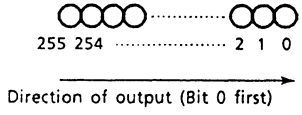
(2) Command input



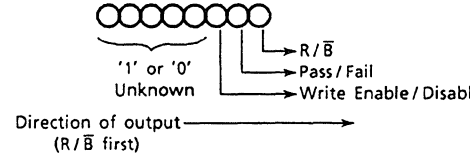
(3) Data input



(4) Data output

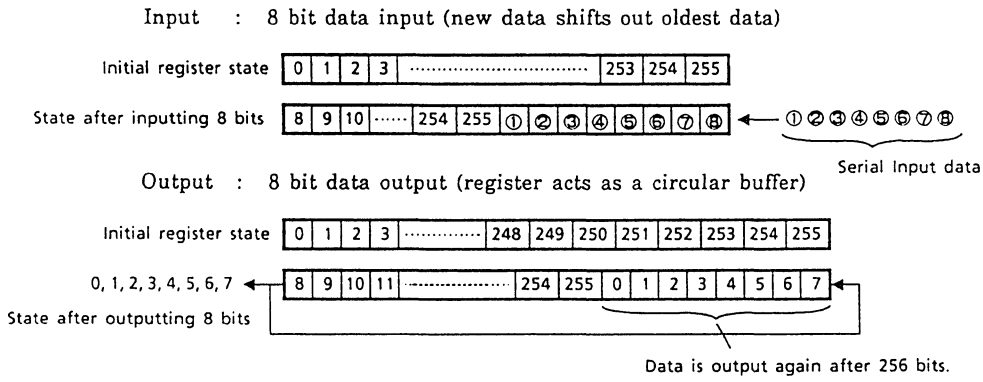


(5) Status data output



Register Operation

The TC58A040 has a 256 bit shift register on the chip. This register is used to transfer data to and from the memory cell array. The register operation is as follows:



Read Operation

The read operation transfers data to the register from the memory cell array and outputs data synchronized to SK. This operation is shown in Figure 1.

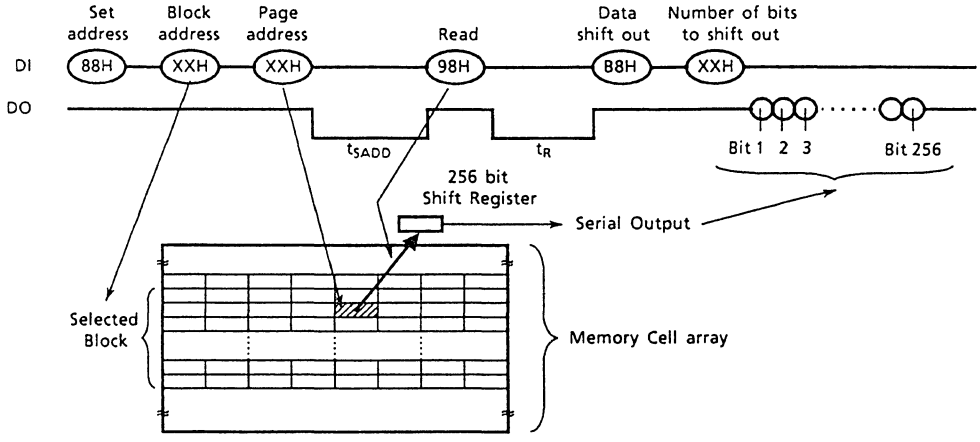
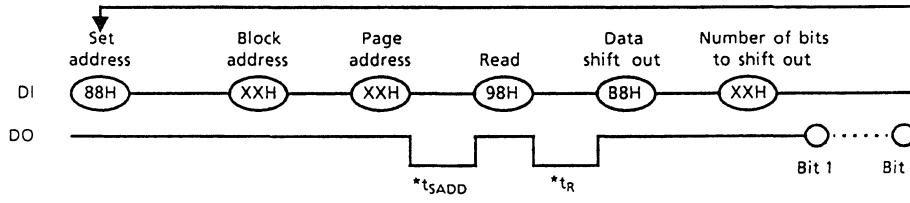


Figure 1. Read operation diagram

The read operation is executed page by page. When reading from two or more consecutive pages, two methods are possible:

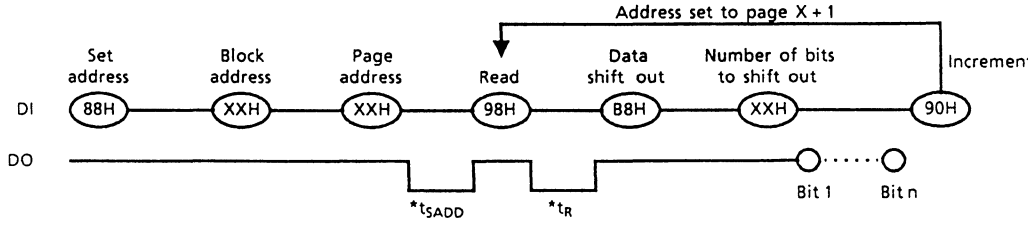
Read Mode (1)

The set address command is input for every page read cycle.



Read Mode (2)

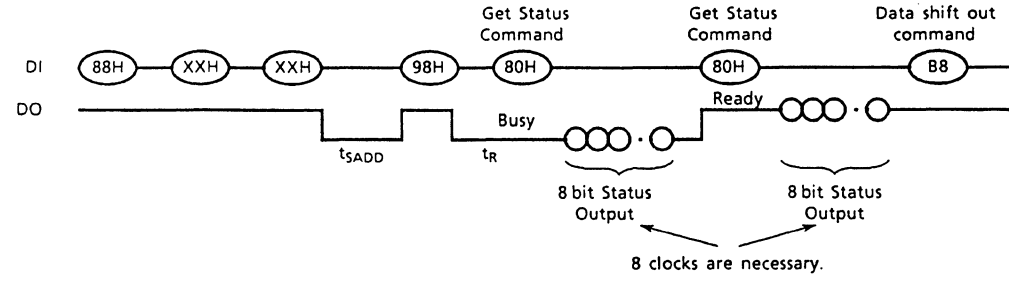
The increment command is used instead of applying the set address command.



* D0 becomes low and is held at low level during the busy state.
The device state (busy or ready) can be output by executing the status read operation.

Status Read

This operation outputs the devices's internal state by using the get status command.



Write Operation

The write operation inputs data into the on-chip data register, and transfers the data from the register into the selected page in the memory array. This operation is shown in figure 2.

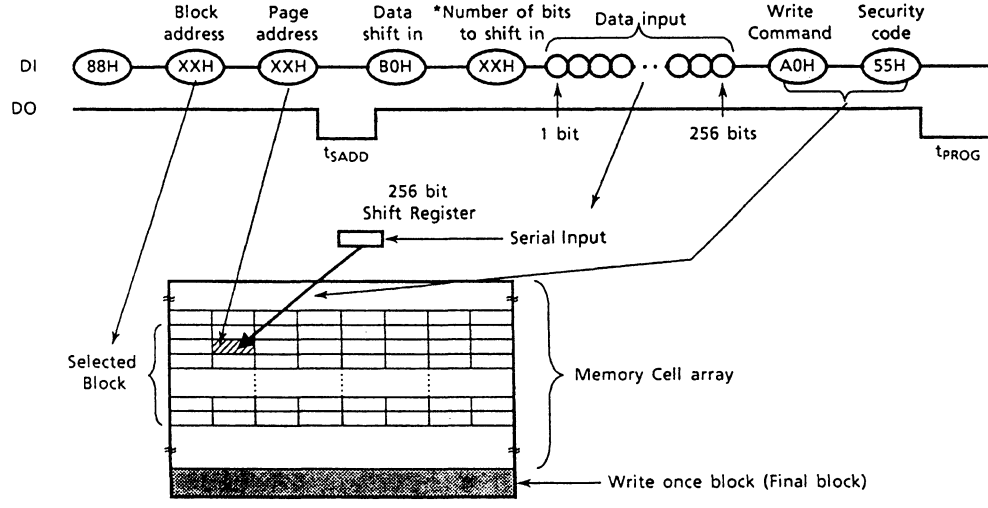
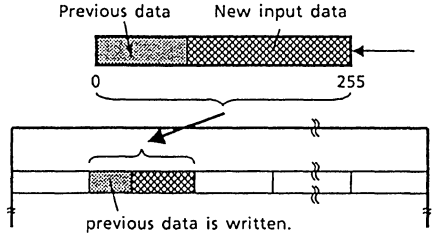


Figure 2. Write operation diagram

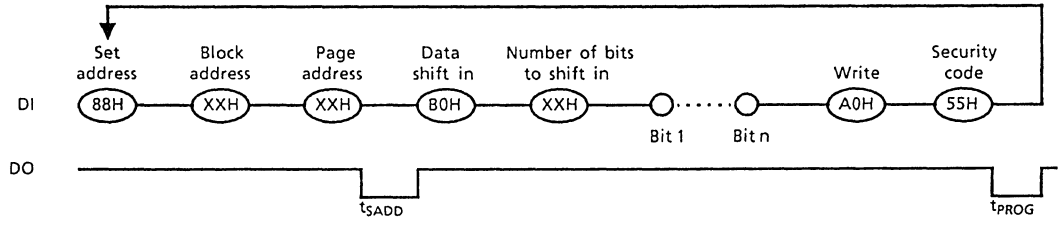
* Number of bits to shift in: 256 (#FFh) should be input.
If the number of bits to shift in is less than 256 (#FFh), previous data will be written into the memory array.



The write operation is executed page by page. When writing two or more consecutive pages, two methods are possible:

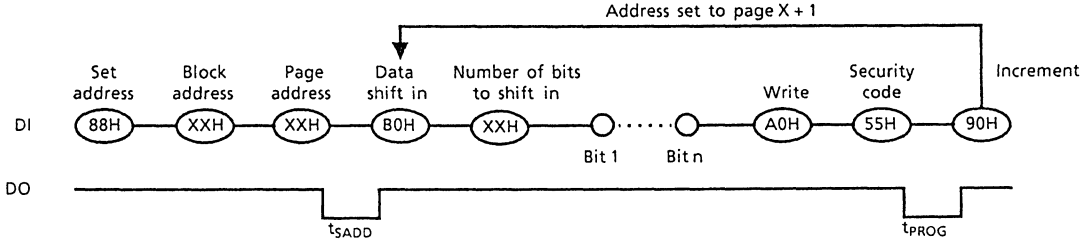
Write Mode (1)

The set address command is input for every page write operation.



Write Mode (2)

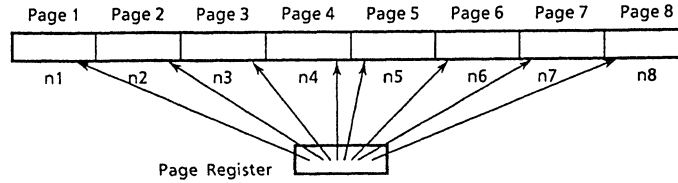
The increment command is used instead of applying the set address command.



D. Non-Volatile

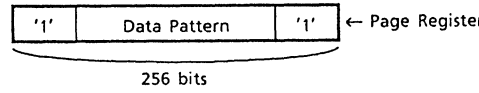
Partial Page Write Operation

The TC58A040 allows a master page to be divided into a maximum of 50 segments with each page segment written individually as follows:



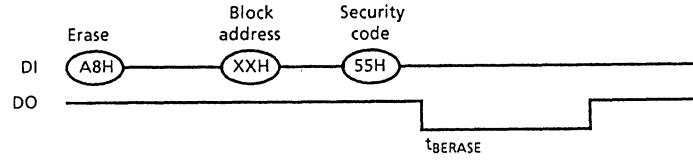
Npp = n1 + n2 + n3 + n4 + n5 + n6 + n7 + n8 = 50
* n1 - n8 : Number of partial programs in a page
* Npp : Number of partial programs in a master page

The input data for unprogrammed or previously programmed page segments must be "1".
Example:



Erase Operation

The erase operation is executed block by block. The erase operation sequence is shown below.

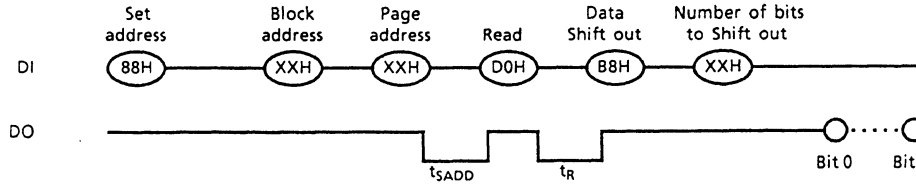


Read and Write Operation for the Final Block (Write Once Block)

The final block (Block 127) has been set aside as a read only block. The final block needs special commands for the read and write operations.

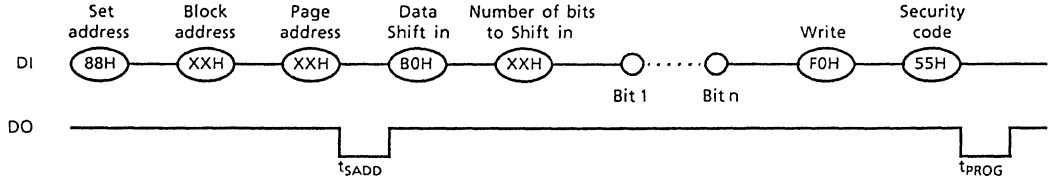
Read Last Block

The block address is ignored.



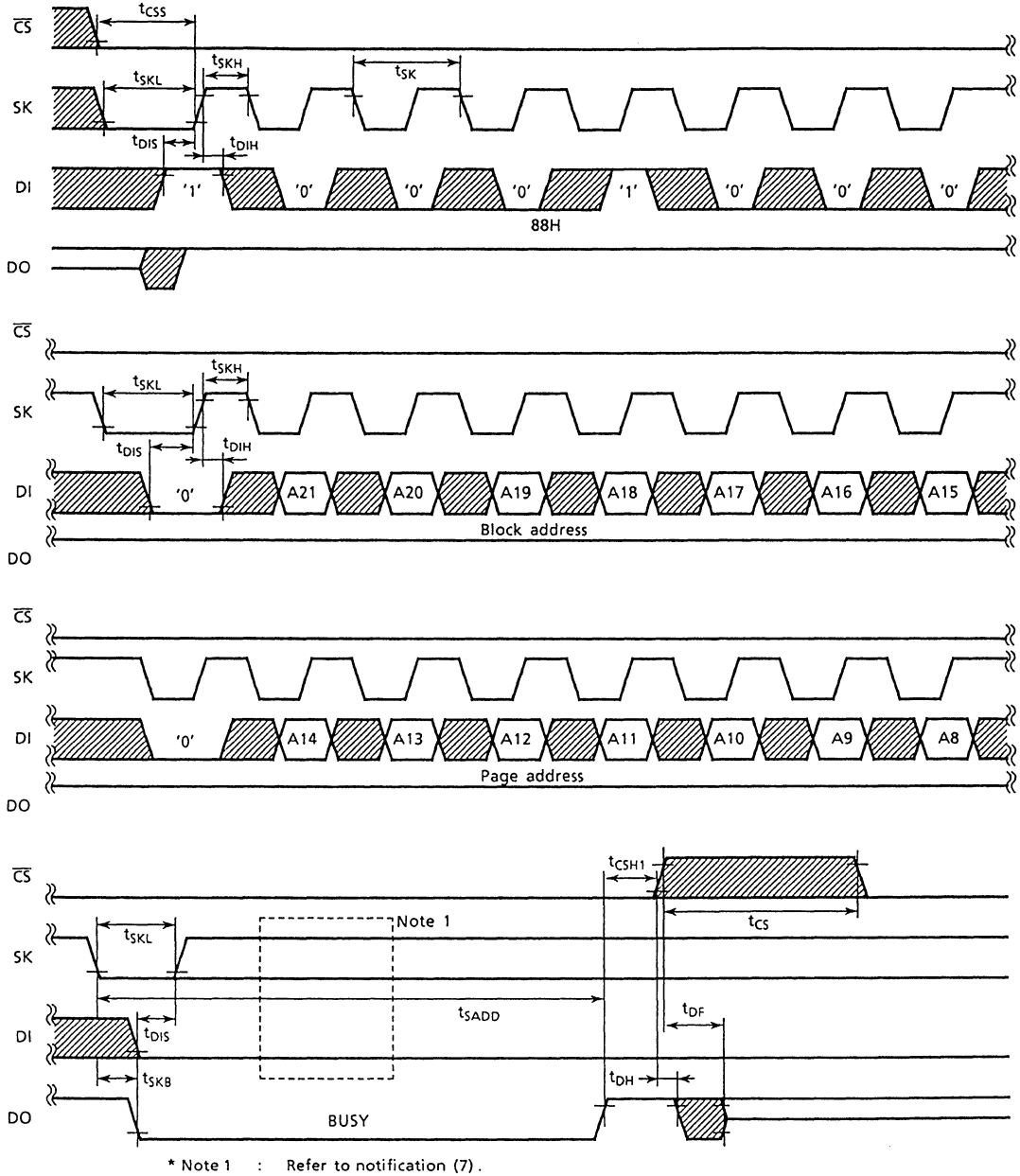
Write Last Block

The block address is ignored.



Timing Diagrams

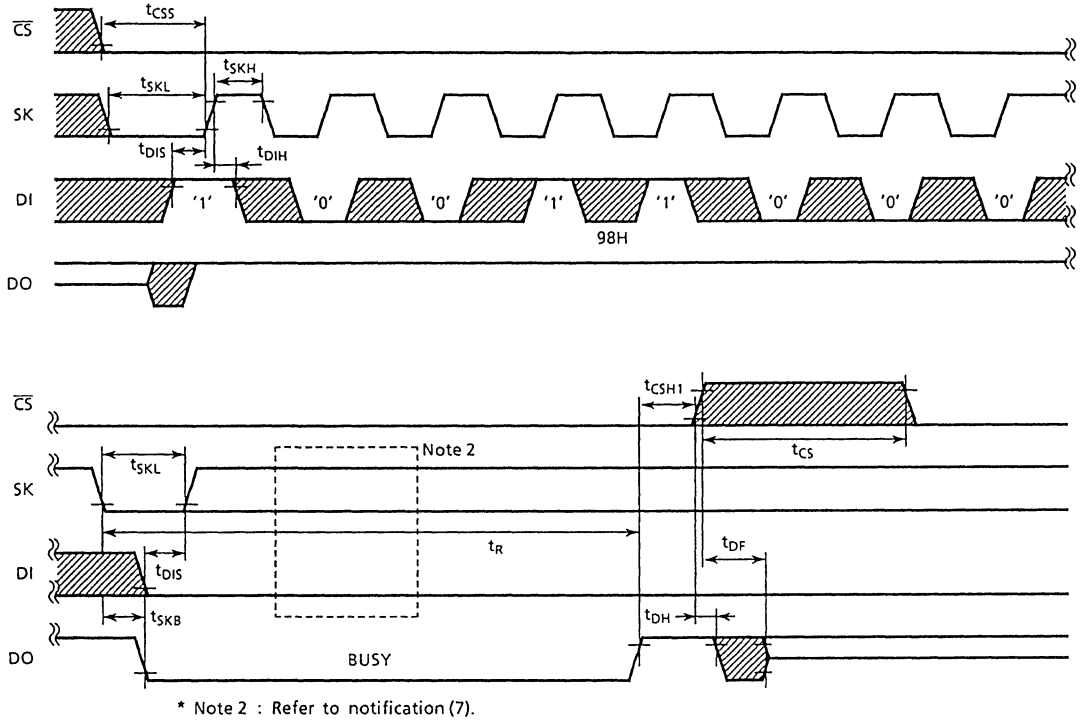
Set Address



* Note 1 : Refer to notification (7).

Note : The above 4 timing diagrams are contiguous.

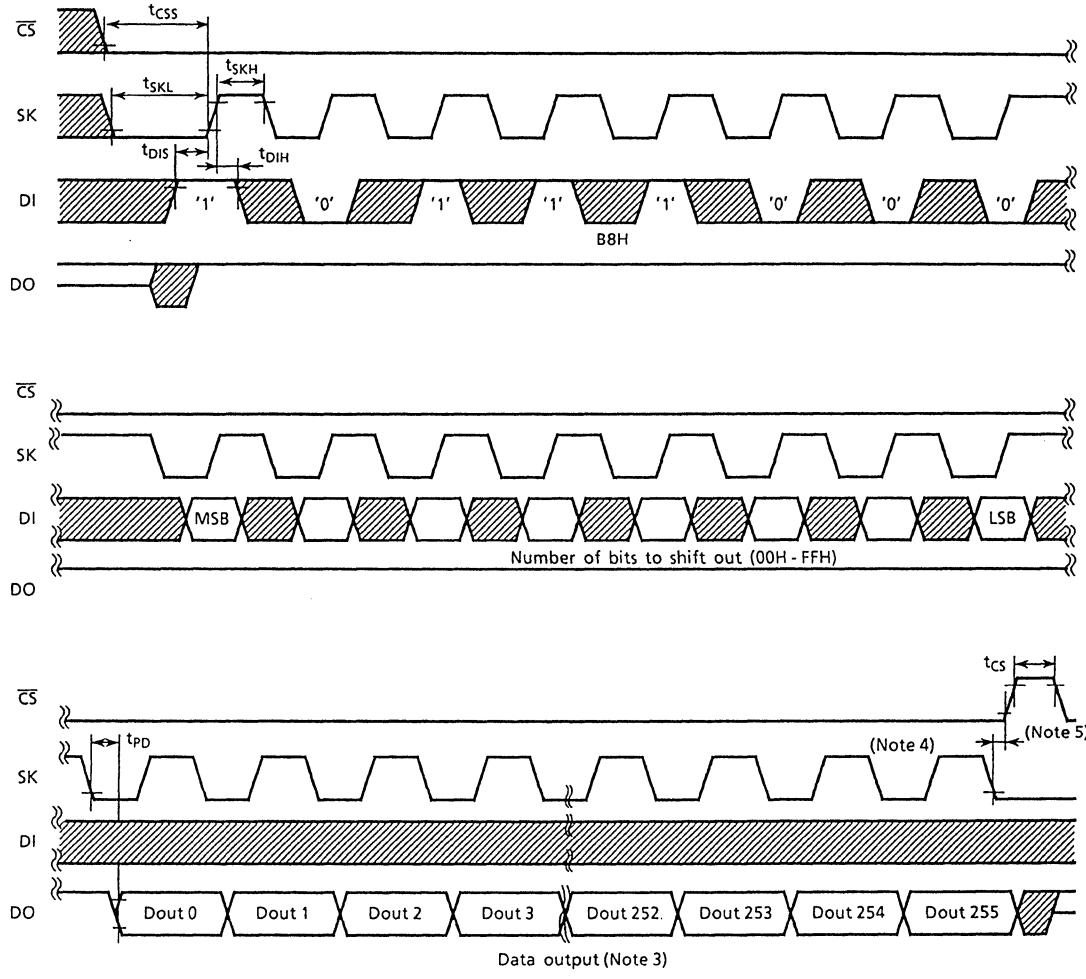
Read



* Note 2 : Refer to notification (7).

Note : The above 2 timing diagrams are contiguous.

Data Shift Out



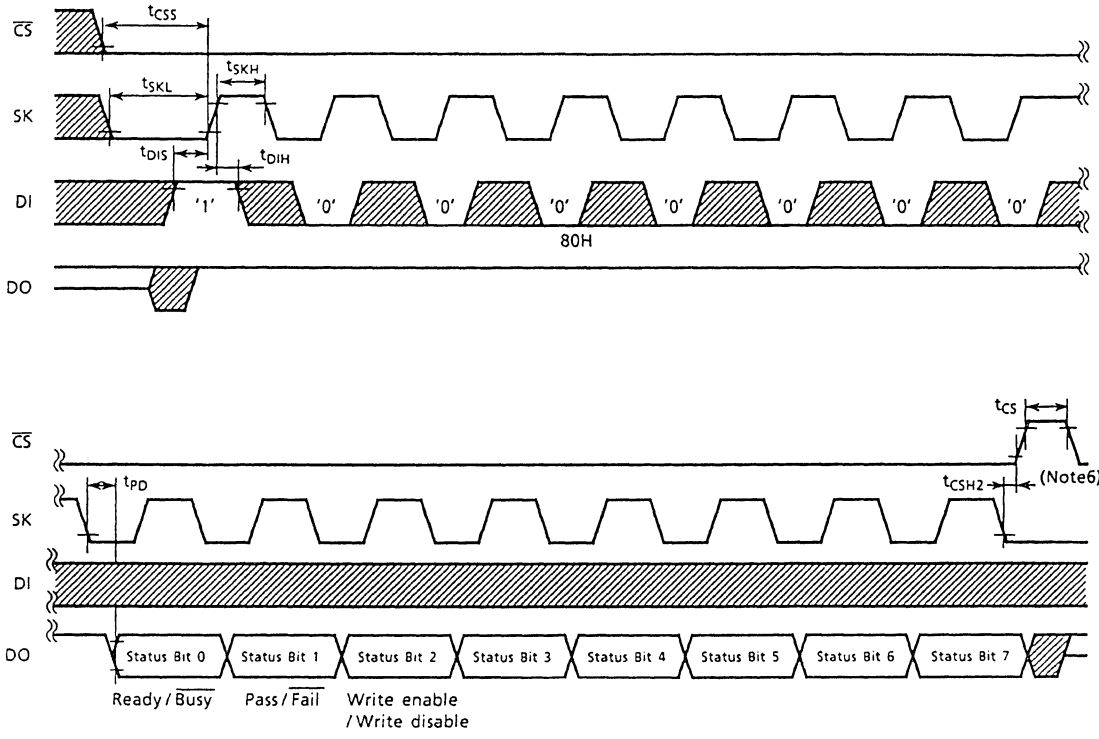
Note 3 : FFH input as the number of bits to shift out.

Note 4 : Refer to notification (6).

Note 5 : Refer to notification (9).

Note : The above 3 timing diagrams are contiguous.

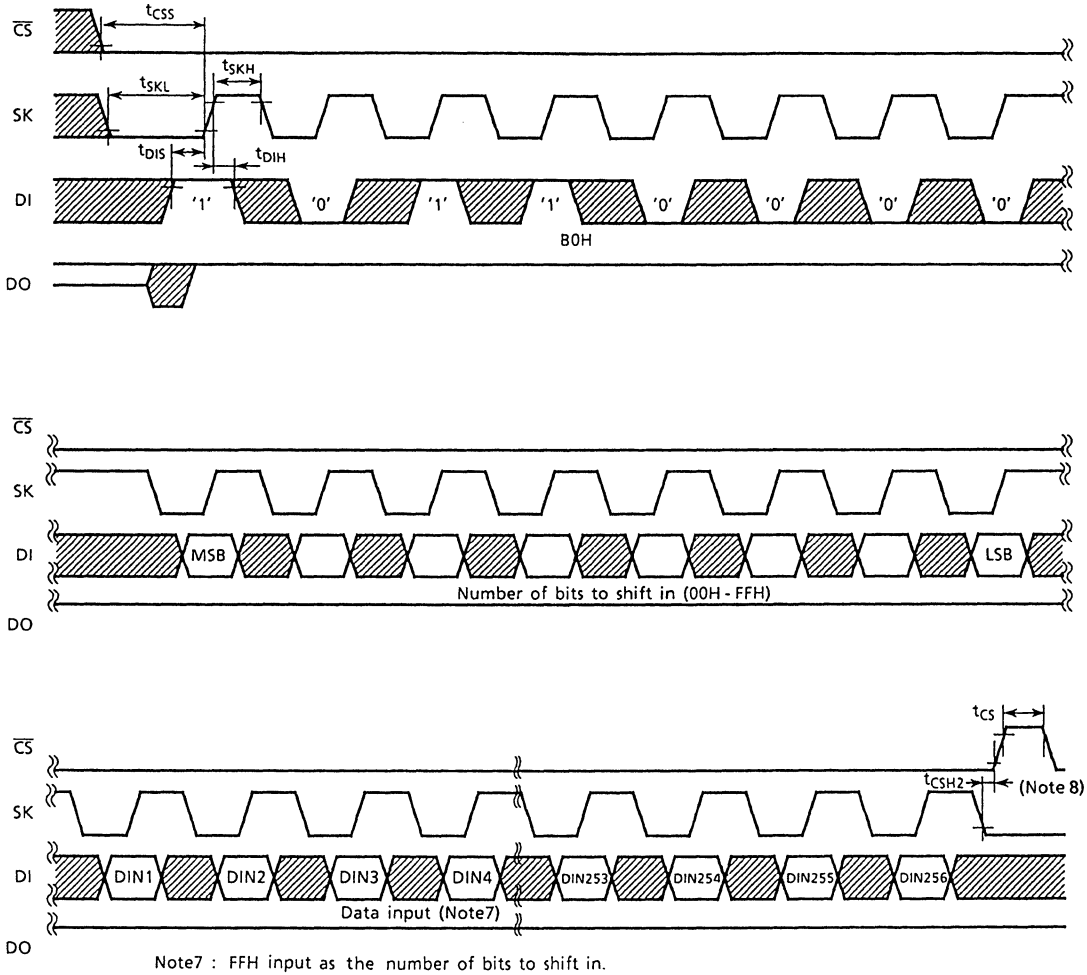
Status Read



Note 6 : Refer to notification (9).

Note : The above 2 timing diagrams are contiguous.

Data Shift In

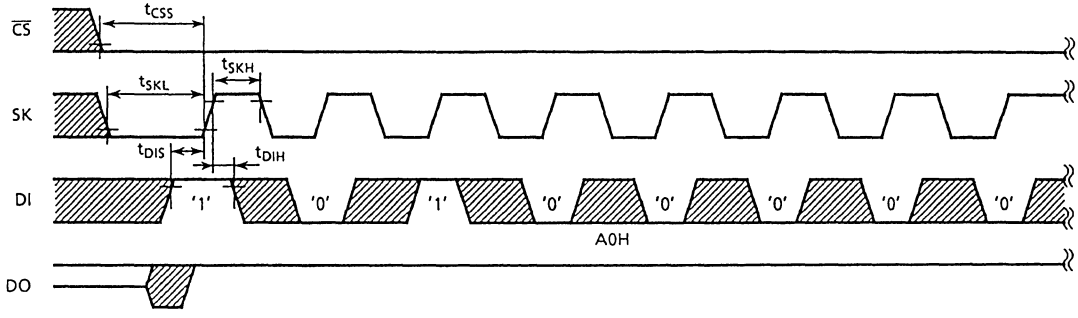


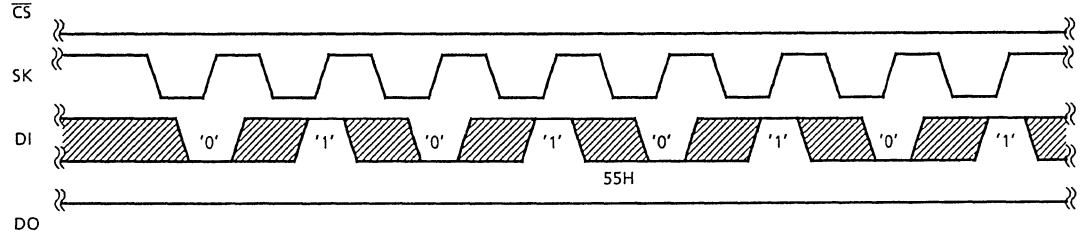
Note7 : FFH input as the number of bits to shift in.

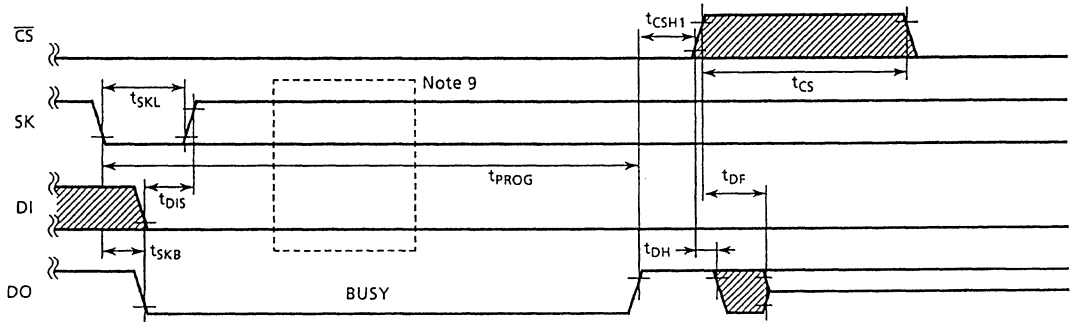
Note 8 : Refer to notification (9).

Note : The above 3 timing diagrams are contiguous.

Write



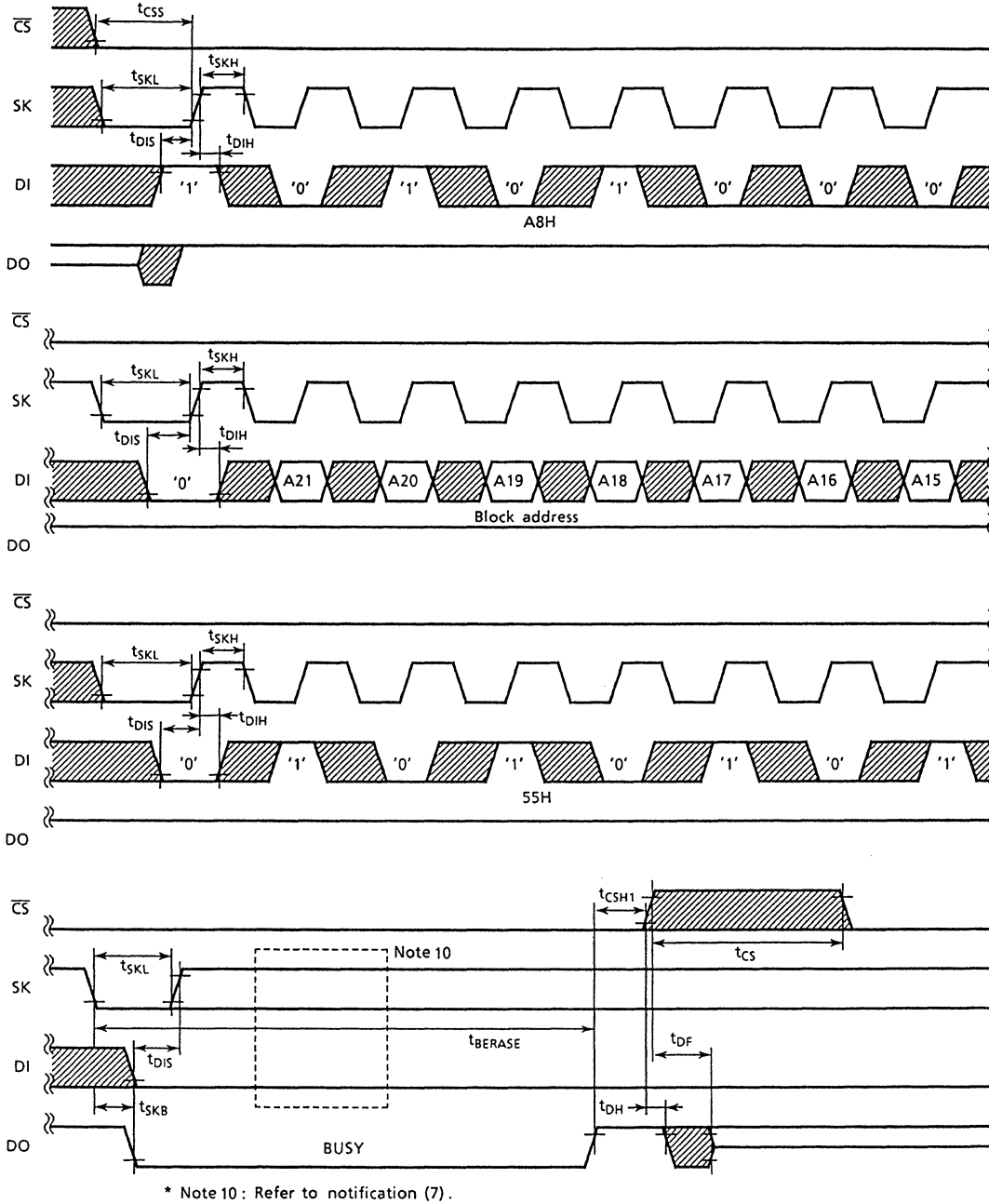




* Note 9 : Refer to notification (7).

Note : The above 3 timing diagrams are contiguous.

Erase



* Note 10 : Refer to notification (7).

Note : The above 4 timing diagrams are contiguous.

Notifications

(1) Prohibition of unspecified commands
The 12 operation commands are listed in the command table. Commands other than these specified commands are prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

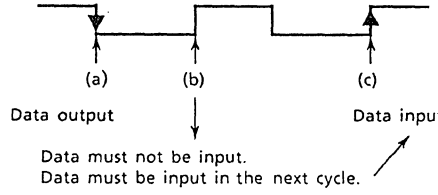
(2) Interruption by $\overline{CS}$ going high
During the period when the TC58A040 is reading a page from the array (t_R), writing a page to the array (t_{PROG}), or erasing a block (t_{BERASE}), the operation will complete regardless of the state of $\overline{CS}$. The CS pin may go high during these operations. The DO pin will reflect the state of the operation by staying low while the operation is being executed. When the operation is completed, DO will go high to reflect the ready state.

(3) Device reset
The TC58A040 is reset whenever $\overline{CS}$ changes from low to high. The command register will be cleared at this point. The data register will continue to hold whatever data is in the register. To clear the data register, 32 bytes of "00H" data must be input. $\overline{CS}$ does not affect operations as described in notification (2) above.

(4) Write disable at power-up
On power-up, the TC58A040 is set in the write disabled mode. This prevents any spurious writes to the device. To enable write operations, the Write Enable (E0H) command must be given.

(5) Prohibition of extra clocks
If an unexpected clock is induced on the SK terminal by noise, the device may malfunction. Also, the device has no reset command. Therefore, noise must be controlled.

(6) Prohibition of data output and data input in the same cycle
Input and output operations in one cycle is prohibited. The following shows an example.



(7) Notification during busy
When the device is in a busy state (when the TC58A040 reads a page from the array (t_R), writes a page to the array (t_{PROG}), erases a block (t_{BERASE}), or decodes an address (t_{SADD}), the DO pin outputs a low level (busy status). During this period, operations, except for status read, are prohibited. If SK is clocked during this period, except for the status read operation, the DI pin must be kept low. If SK is held at a high or low level, the DI pin is don't care.

(8) Identification of Bad Blocks

The TC58A040 may contain unusable blocks. Bad blocks must be identified by user software during initial operation. The figure below describes how to identify bad blocks.

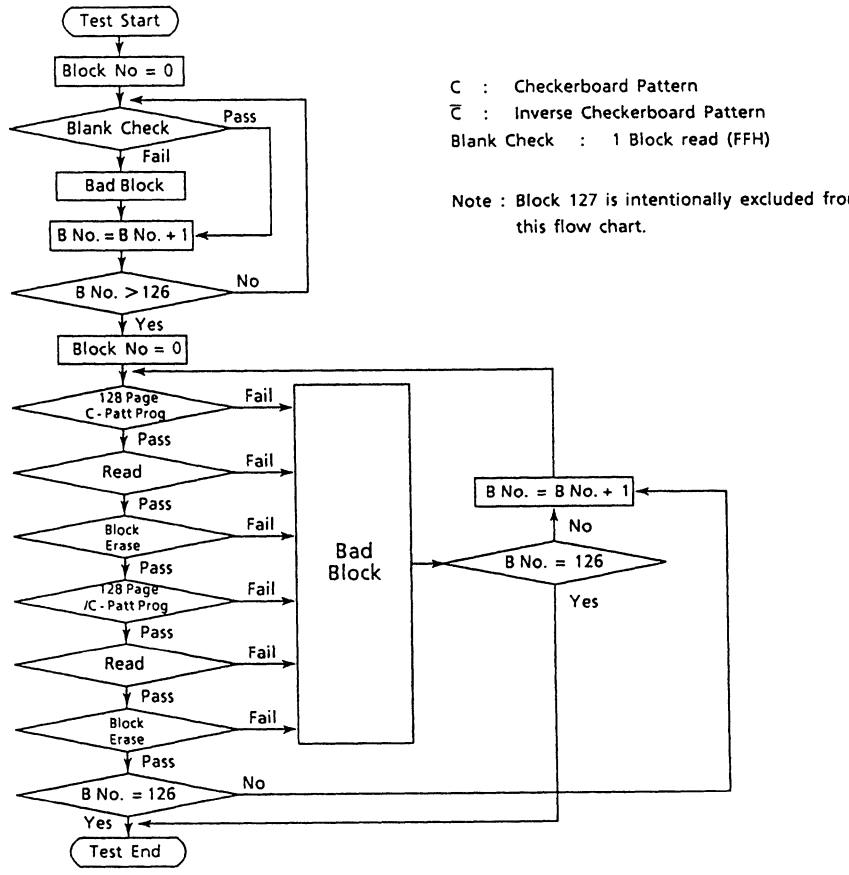
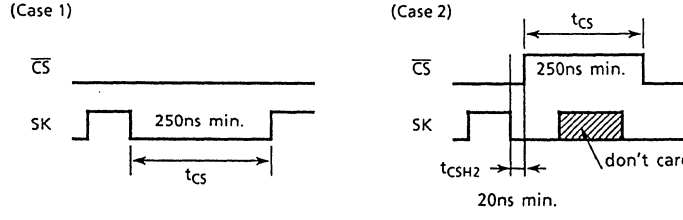


Figure 3

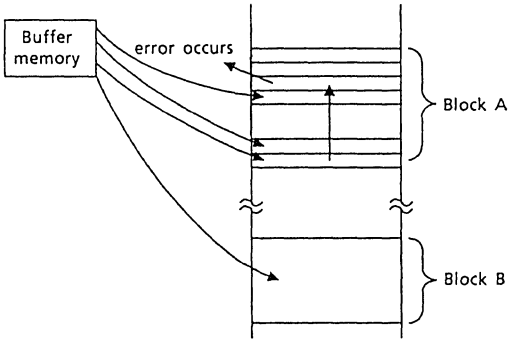
(9) Notification of when an operation finishes

When the data shift out, data shift in, or status read operation finishes, the $\overline{CS}$ pin must go to a high level or SK must stay low for at least 250ns. This must occur before inputting subsequent commands such as increment, write enable, or write disable.



(10) Error in program or erase operation (Fail at status read)
The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs:

Program



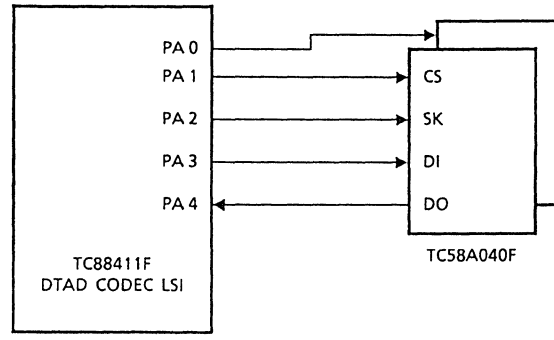
When an error happens in Block A, try to reprogram the data into another block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a 'bad block' table or other appropriate scheme.)

Erase

When the error occurs after an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)

System Concepts

The TC58A040 is a 4M bit NAND EEPROM designed to provide the most cost effective solution for digital audio recording applications. For digital audio storage, the TC58A040 has been matched with DTAD CODEC LSI TC88411F. Applications that can benefit from this combination include digital answering machines and personal digital recorders. Customers can quickly bring to market systems capable of recording up to 15 minutes of audio on a single 4M bit device. Multiple TC58A040 can be used to extend the recording time.



Data Transfer Rate

The data transfer rate of the TC58A040 is as follows.

	Data Transfer Rate		Total Time	
	Page	Block	Page	Block
Read	0.85M bits/s	2.60M bits/s	301μs	12.6ms
Write (t_{PROG}: 400μs)	377.6k bits/s	538.3k bits/s	678μs	60.9μs
Erase (t_{ERASE}: 7.0ms)	–	–	–	7.0ms

Device Physics

Program Operation

Figure 4 shows the NAND memory cell level details of the programming mechanism. The program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example program operation to program "0" data in TR1 and "1" data in TR2 is as follows:

(1) A high level is applied to select line 1 and a low level is applied to select line 2 so that the device is connected to the bit line and disconnected from the ground line.
(2) V_{PP} (~20V) is applied to the selected word line and an inhibit voltage of VPI (≈10V) is applied to the unselected word lines.
(3) The bit line tied to cell transistor TR1 is biased to 0V and the bit line tied to TR2 is biased to the inhibit voltage of VDP1 (≈10V).
(4) V_{PP} is applied between the control gate and the channel in TR1, as shown in Figure 4, which causes electrons to be injected from the channel to the floating gate by tunneling.
(5) The injected electrons are captured in the floating gate (surrounded by an oxide layer) and will remain, even after power is cut off, until they are removed by an erase operation.
(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10V because the voltage of the channel is 10V. Therefore, tunneling does not take place. (i.e. electrons are not injected into the floating gate.)
(7) Tunneling does not take place in the unselected pages because of the 10V (VPI) being applied to the unselected word lines which again makes the voltage difference between control gate and channel only 10 volts. Thus, the floating gate of the "0" cell is charged to "Minus" and that of the "1" cell is charged to "Plus".

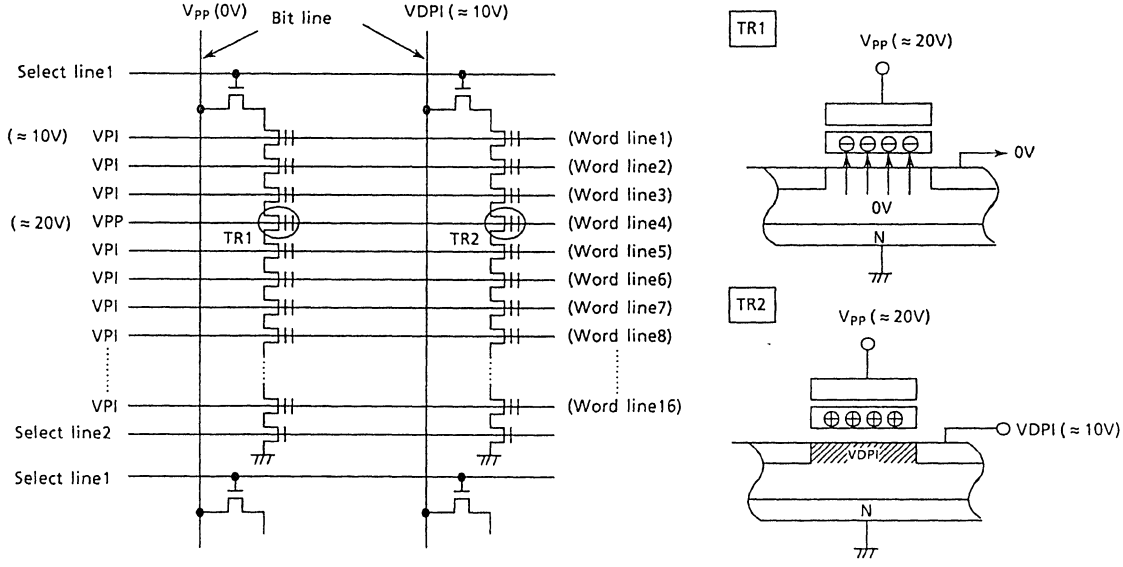


Figure 4. TC58A040 Program Device Physics

Erase Operation

Figure 5 shows the NAND memory cell level details of the erase mechanism. The erase operation is used to turn the "0" (programmed) cells back to "1" in a block. The captured electrons are pulled out from the floating gate to the substrate by tunneling. Zero volts is applied to the control gate and V_{PP} (~20V) is applied to the substrate so that a 20 volt potential is created and the electrons in the floating gate are pulled out through tunneling.

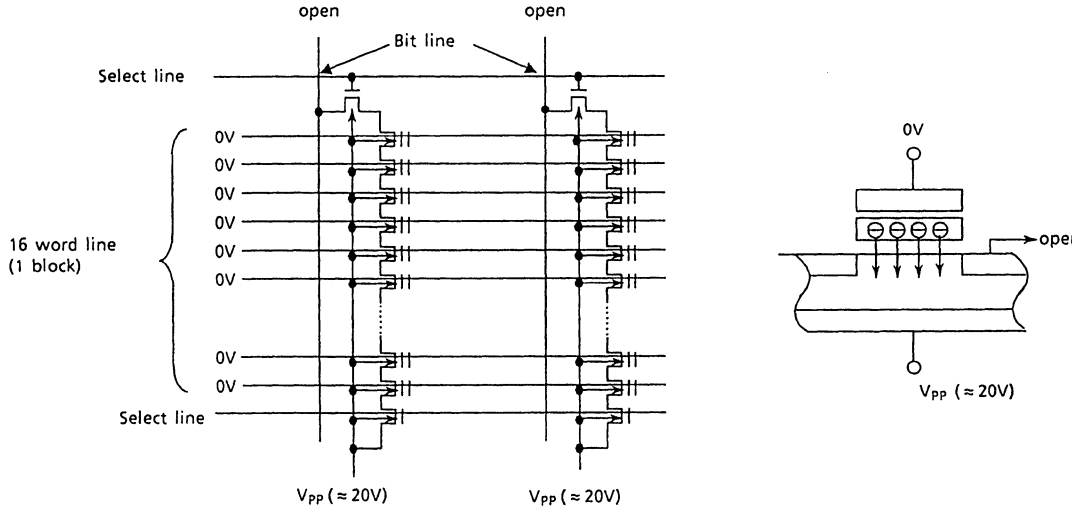


Figure 5. TC58A040 Erase Device Physics

Read Operation

The state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate) after programming. Each state is indicated by a "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 6. The threshold voltage of a transistor with data "0" distributes in the "plus" region while data "1" distributes in the "minus". The distribution band depends on transistor fluctuations.

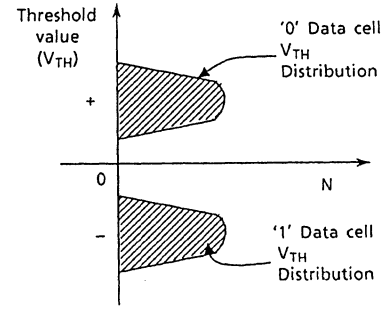


Figure 6. V_{TH} Distribution for "0" and "1" data cell

Figure 7 shows the memory cell level details of the read operation:

(1) Select lines 1 and 2 in the block, including the selected page, are biased at a high level so that the 16 NAND memory cells are connected to the bit line and ground.

(2) Zero volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 7, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground while the precharged bit line tied to TR1 remains at a high level because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

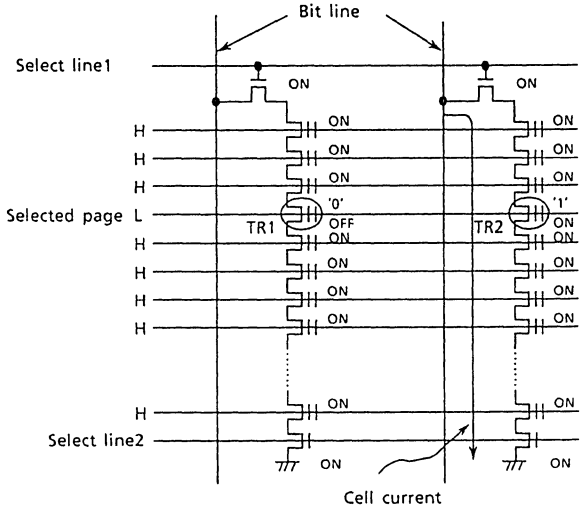
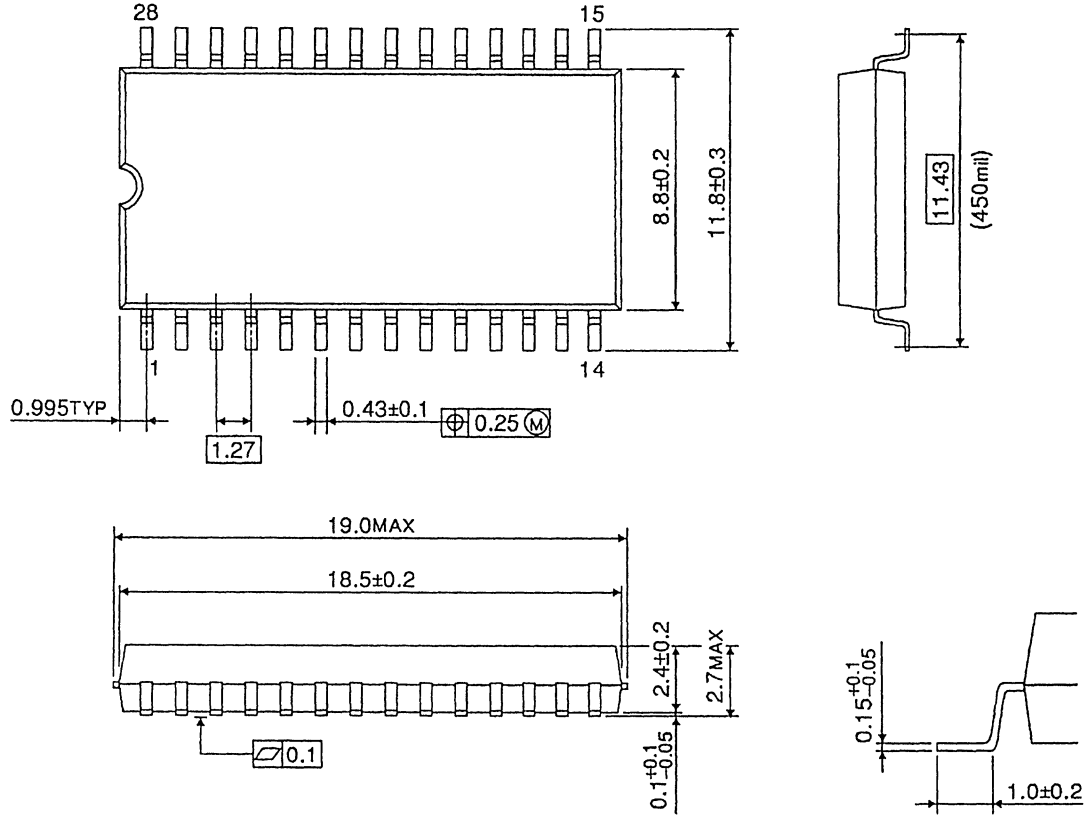


Figure 7. TC58A040 Read Device Physics

Outline Drawings

Plastic SOP: SOP28-P-450 Unit: mm



TC5816AFT

PRELIMINARY

16Mbit (2M x 8 BIT) CMOS NAND EEPROM

Description

The TC5816 is a 5 volt 16M bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) with a spare 64k x 8 bits. This device is organized as 264 bytes x 16 pages x 512 blocks. The device has a 264 byte static register which allows program and read data to be transferred between the register and the memory cell array in 264 byte increments. The erase operation is implemented in a single block unit (4k bytes + 128 bytes: 264 bytes x 16 pages).

The TC5816 is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for still cameras, and other systems which require high density, non-volatile memory data storage.

Features

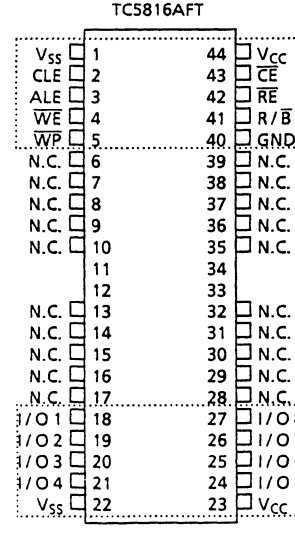
- Organization
  - Memory cell array : 264 x 8K x 8
  - Register : 264 x 8
  - Page size : 264 bytes
  - Block size : (4k + 128) bytes
- Modes : Read, Reset, Auto page program, Auto block erase, Suspend/ Resume, Status read
- Mode control : Serial input/output Command control
- Package 400mil TSOP Type II
  - TC5816AFT : TSOP44-P-400B
- Power supply : V_{CC} = 5V±10%
- Access time
  - Cell array - Register : 25μs max.
  - Serial access : 80ns min.
- Operating current
  - Read (80ns cycle) : 15mA typ.
  - Program (ave.) : 40mA typ.
  - Erase (ave.) : 20mA typ.
  - Standby : 100μA
- Operating temperature : 0 ~ 70°C

Pin Names

$I/O_{1\sim8}$	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
$R/\overline{B}$	Ready/Busy
GND	Ground Input
V_{CC}/V_{SS}	Power Supply/Ground (5V/GND)

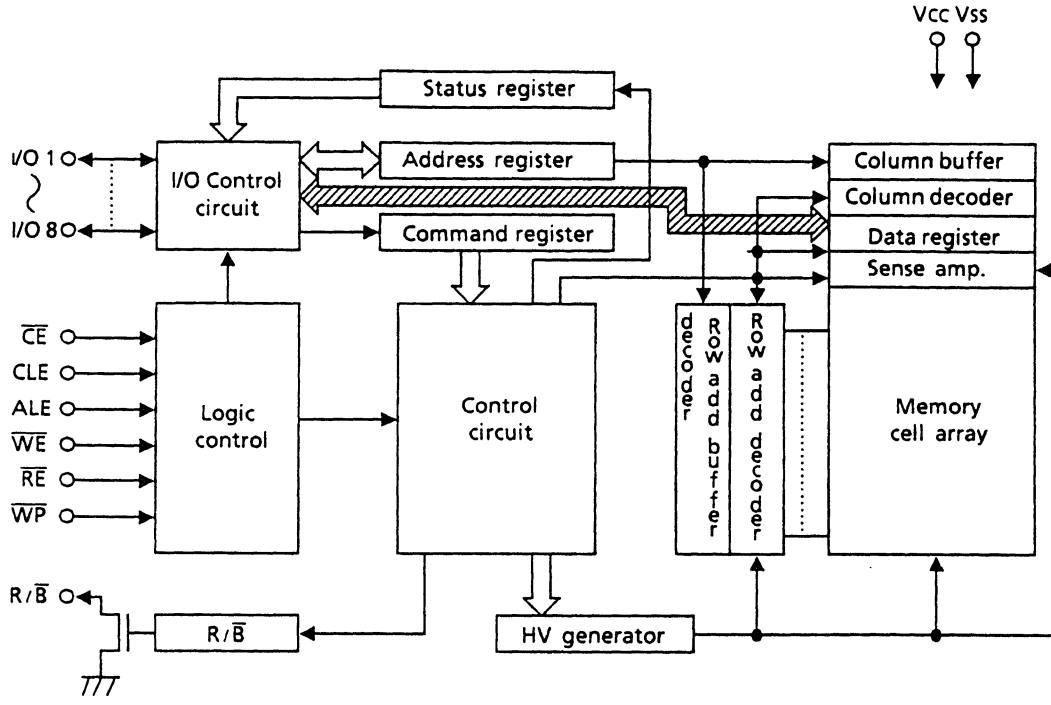
Pin Connection (Top View)

TC5816AFT



D. Non-Volatile

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6V ~ V_{CC} + 0.5V (≤ 7V)	
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STG}	Storage Temperature	-55 ~ 150	
T_{OPR}	Operating Temperature	0 ~ 70	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	5	10	

*This parameter is periodically sampled and is not 100% tested.

Valid Blocks (1)

SYMBOL	PARAMETER	TC5816FT			UNIT
		MIN.	TYP.	MAX.	
N_{VB}	Valid block number	502	508	512	Blocks

(1) The TC5816AFT includes unusable blocks. Refer to notification (17) toward the end of this document.

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.5	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	

* -2V (pulse width ≤ 20ns)

DC Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{DD}		–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{DD}		–	–	±10	
I_{DDO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}	t_{cycle} = 80ns	–	15	30	mA
I_{DDO2}	Operating Current (Serial Read)	I_{OUT} = 0mA	t_{cycle} = 1μs	–	–	5	
I_{DDO3}	Operating Current (Command Input)	t_{cycle} = 80ns		–	15	30	
I_{DDO4}	Operating Current (Data Input)	t_{cycle} = 80ns		–	50	70	
I_{DDO5}	Operating Current (Address Input)	t_{cycle} = 80ns		–	15	30	
I_{DDO6}	Operating Current (Register Read)	t_{cycle} = 80ns		–	15	30	
I_{DDO7}	Program Current	–		–	40	60	
I_{DDO8}	Erasing Current	–		–	20	40	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2V		–	–	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = - 400μA		2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		–	–	0.4	
$I_{OL}(R/\overline{B})$	Output Current of (R/$\overline{B}$) pin	V_{OL} = 0.4V		–	10	–	mA

AC Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%) (1)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{CLS}	CLE Setup Time	20	–	ns	
t_{CLH}	CLE Hold Time	40	–	ns	
t_{CS}	$\overline{CE}$ Setup Time	20	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	40	–	ns	
t_{WP}	Write Pulse Width	40	–	ns	
t_{ALS}	ALE Setup Time	20	–	ns	
t_{ALH}	ALE Hold Time	40	–	ns	
t_{DS}	Data Setup Time	30	–	ns	
t_{DH}	Data Hold Time	20	–	ns	
t_{WC}	Write Cycle Time	80	–	ns	(2)
t_{WH}	$\overline{WE}$ High Hold Time	20	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Falling Edge	100	–	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	–	ns	
t_{RC}	Read Cycle Time	80	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	45	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in the Serial Read Cycle	250	–	ns	(4)
t_{READ}	$\overline{RE}$ Access Time (ID Read)	–	90	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	5	20	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	–	30	ns	
t_{REH}	$\overline{RE}$ High Hold Time	20	–	ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	45	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	55	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low (Status Read)	50	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)	50	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_{R}	Memory Cell Array to Starting Address	–	25	µs	
t_{WB}	$\overline{WE}$ High to Busy	–	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (read cycle)	150	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (Sequential Read)	–	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of Interception by $\overline{CE}$ during Read Mode)	–	100 + tr ($R/\overline{B}$)	ns	(3)
t_{RST}	Device reset time (Read/Program/Erase/after suspend)	–	10/20/1500/10	µs	

AC Test Conditions

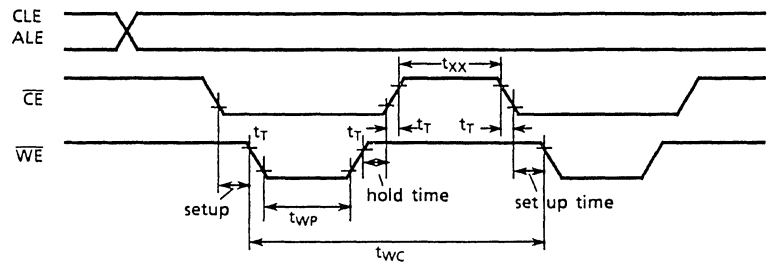
Input Level	2.4V/0.6V
Input Timing Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1 TTL and C_L (100 pF) -

(1) Transition time (t_T) = 5ns.

(2) In the case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 80ns.

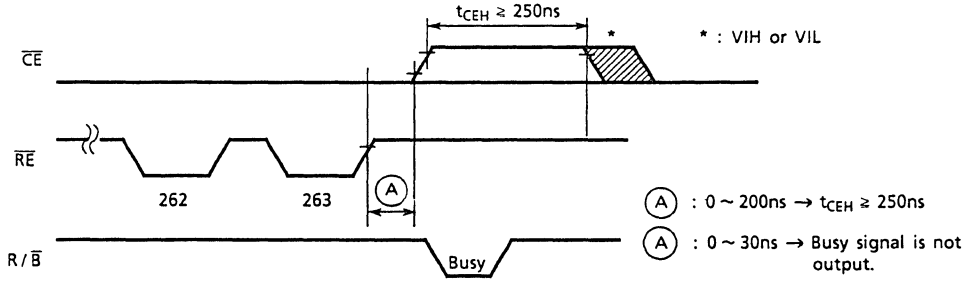
$$\underset{20ns}{\text{set - up time}} + \underset{40ns}{\text{hold time}} + \underset{40ns}{t_{WP}} + \underset{20ns}{t_{XX}} + \underset{20ns}{4t_T}$$

(ex.)



(3) The $\overline{CE}$ high to Ready time depends on the pull up resistor tied to the R/$\overline{B}$ pin. (Refer to notification (10) toward the end of this document.)

(4) If $\overline{CE}$ returns to a high level after accessing the last address (263) in read mode (1) or (2), $\overline{CE}$ high time must keep equal to or greater than 250ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200ns as shown below. In the second case, the device will not turn to a "Busy" state when the $\overline{CE}$ delay time is less than 30ns.



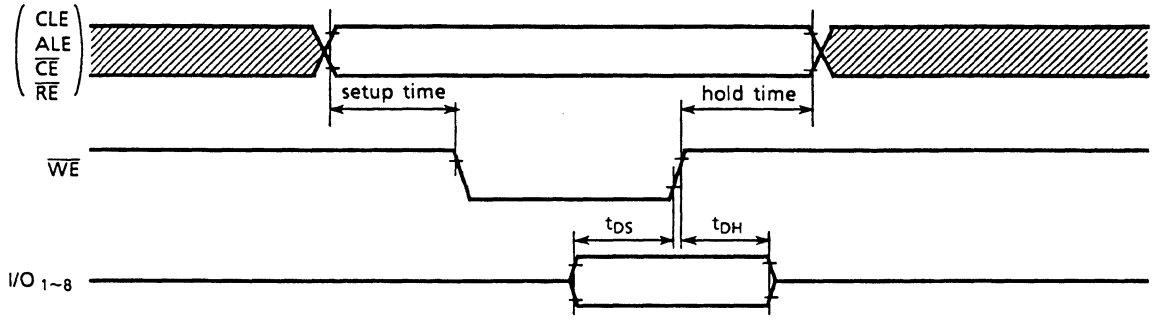
Programming and Erasing Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
t_{PROG}	Average Programming Time		300 ~ 1000	5000	μs	
N	Divided Number on Same Page			10		(1)
t_{BERASE}	Block Erasing Time	6	6	100	ms	
t_{SR}	Suspend Input to Ready			1.5	ms	
$N_{W/E}$	Number of Write/Erase Cycles	2.5×10^5			cycles	

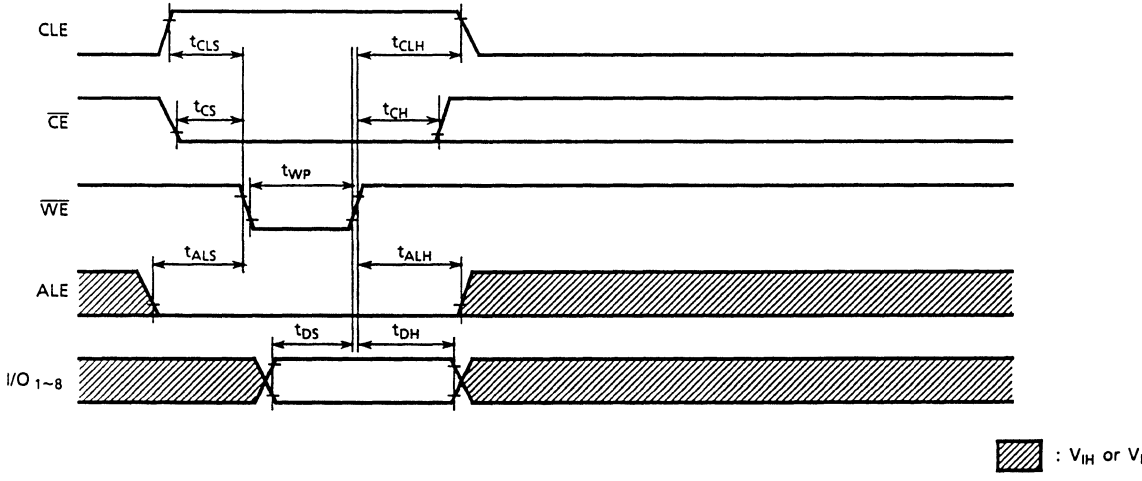
(1) Refer to notification (15) toward the end of this document.

Timing Charts

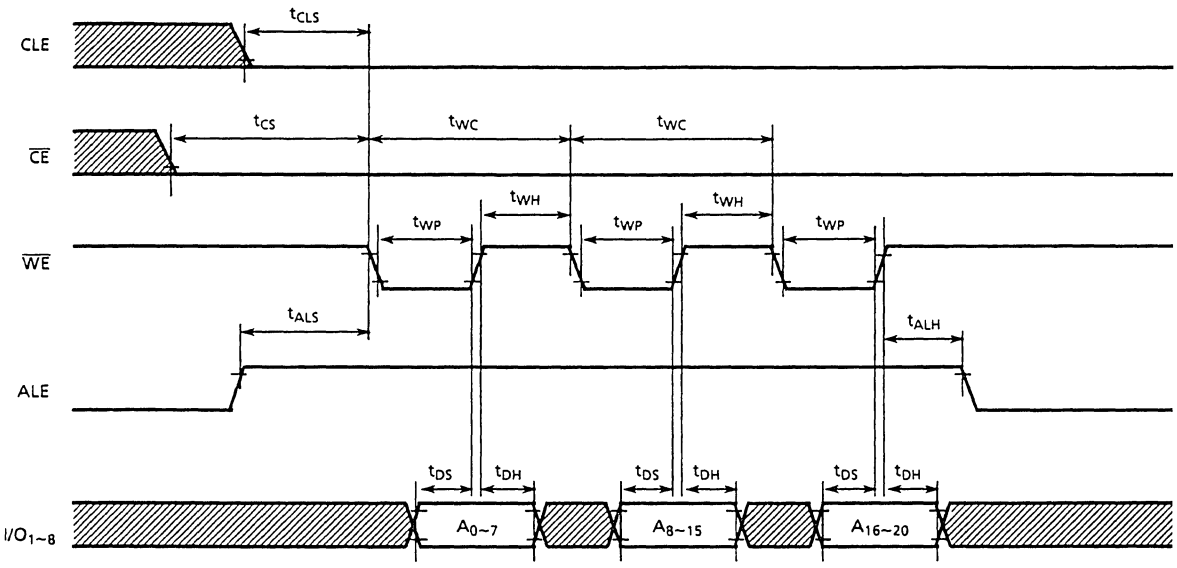
Latch Timing Chart for Command/Address/Data



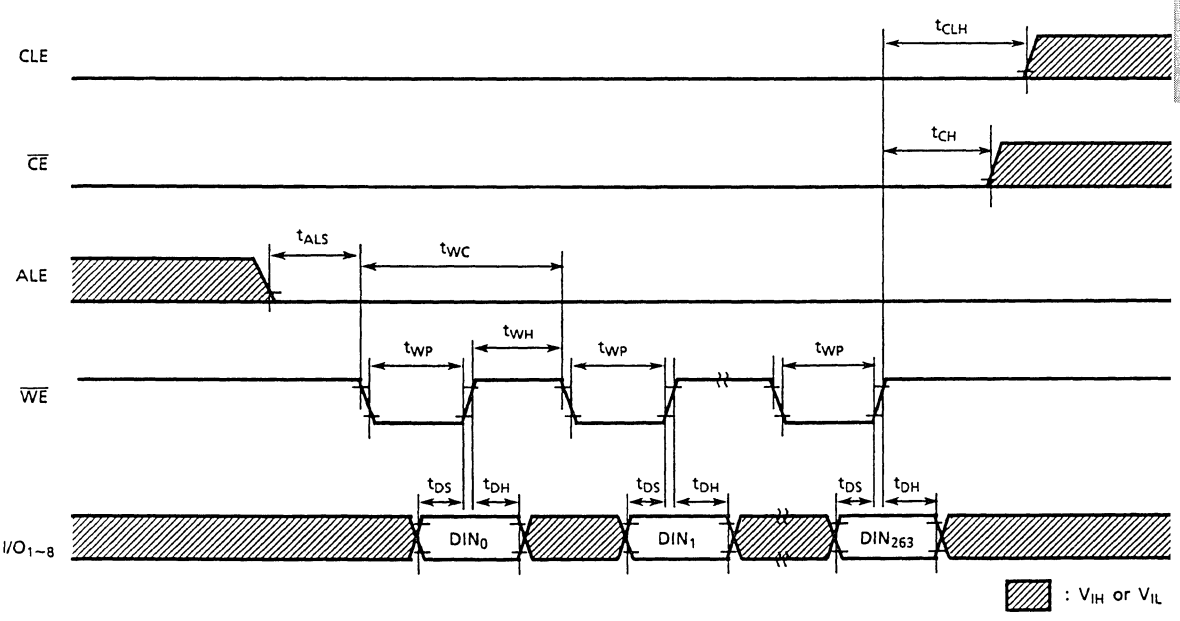
Command Input Cycle



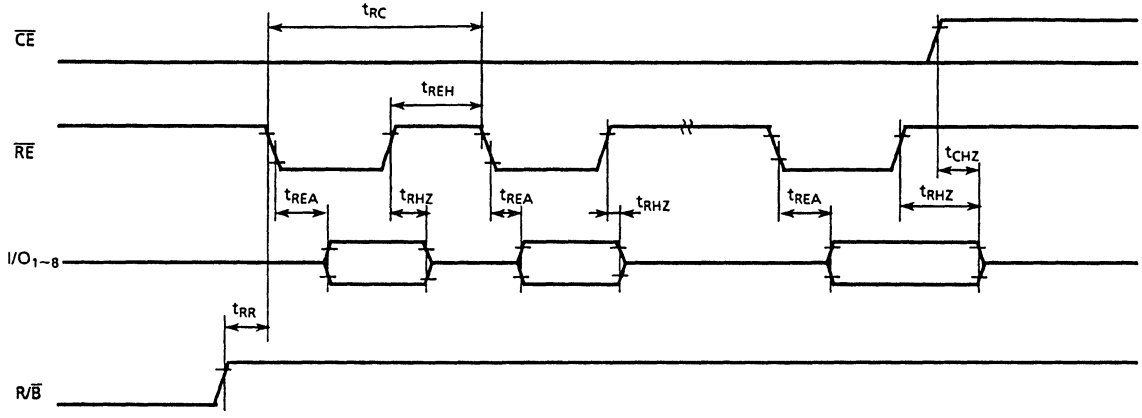
Address Input Cycle



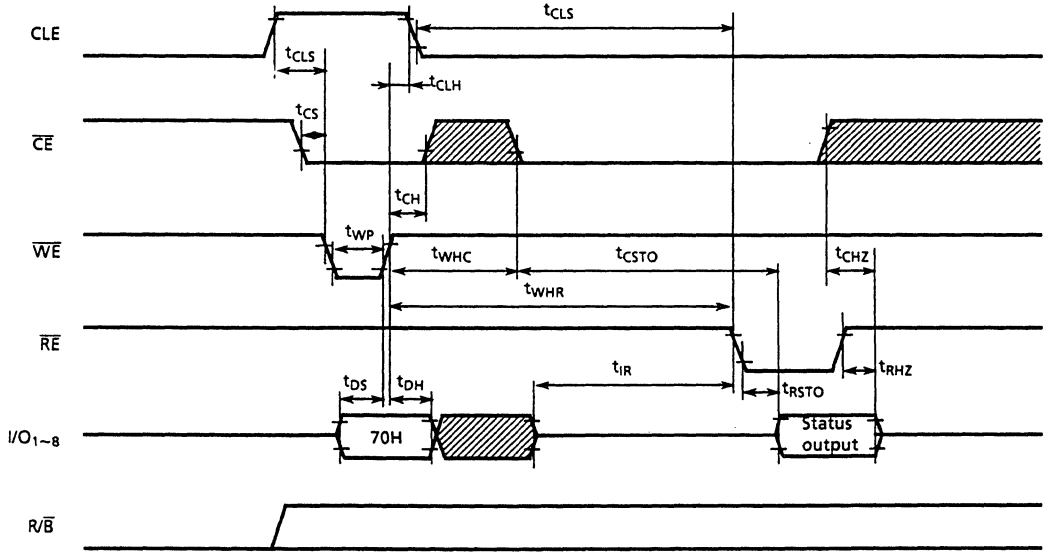
Data Input Cycle



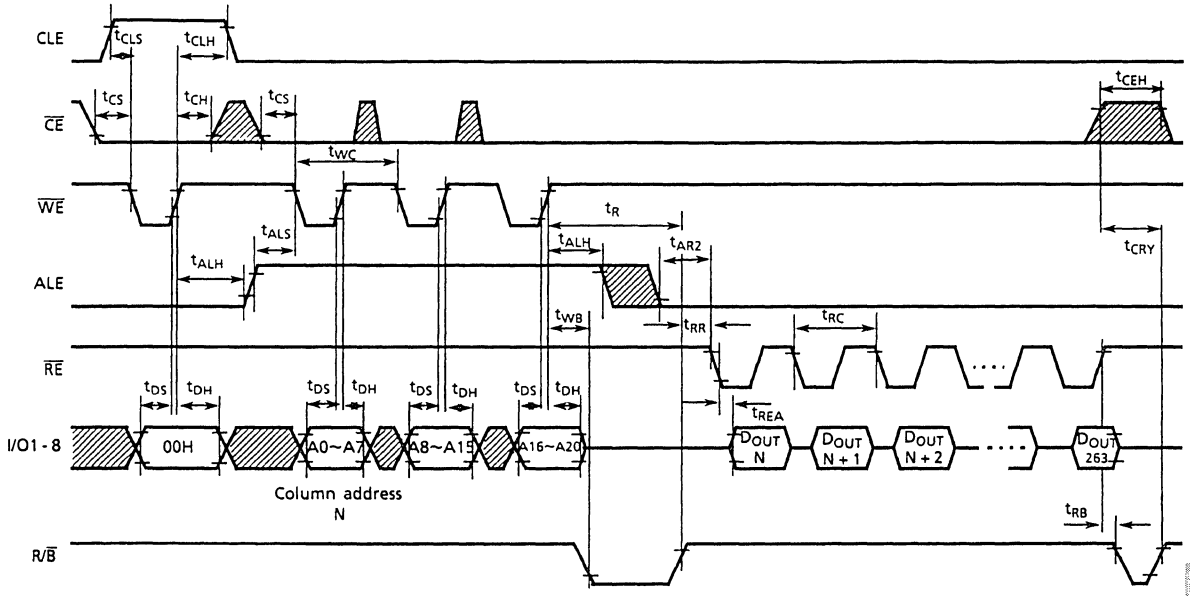
Serial Read Cycle



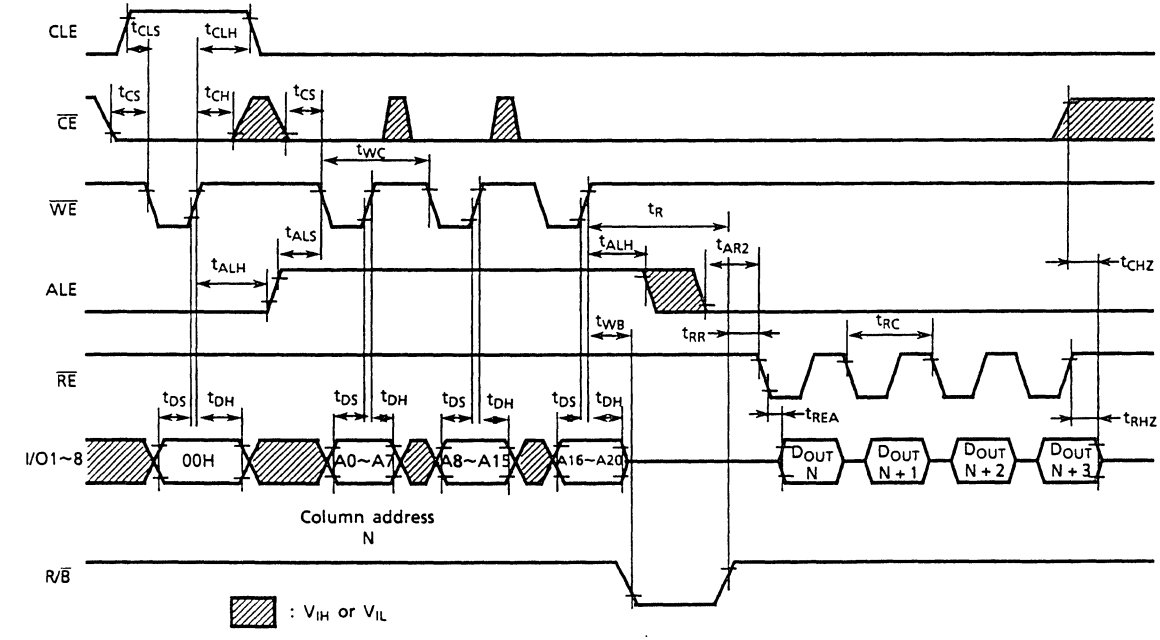
Status Read Cycle



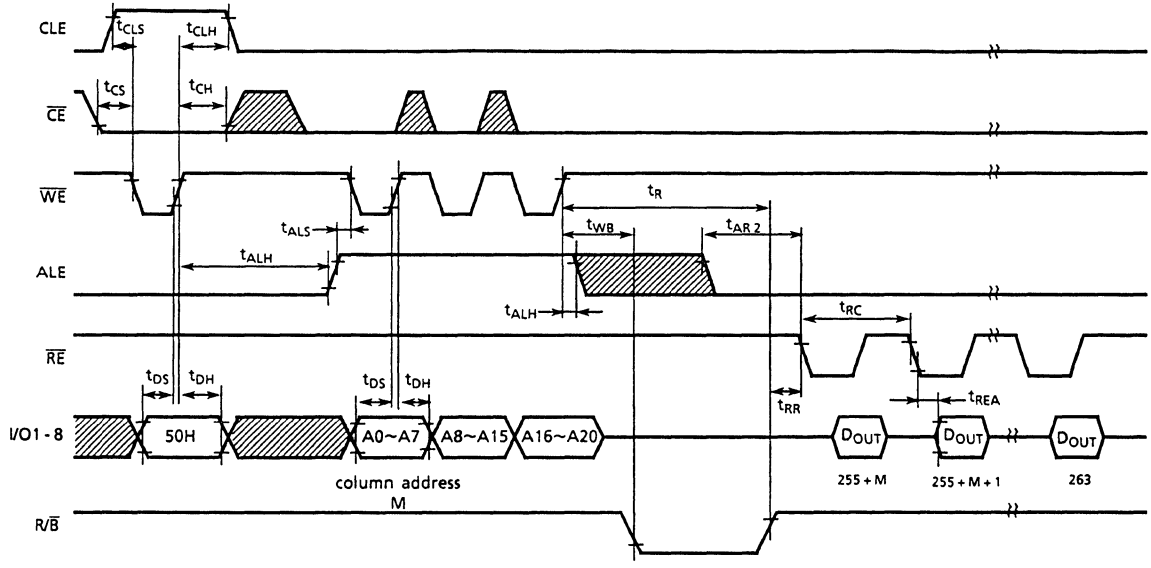
Read Cycle (1)



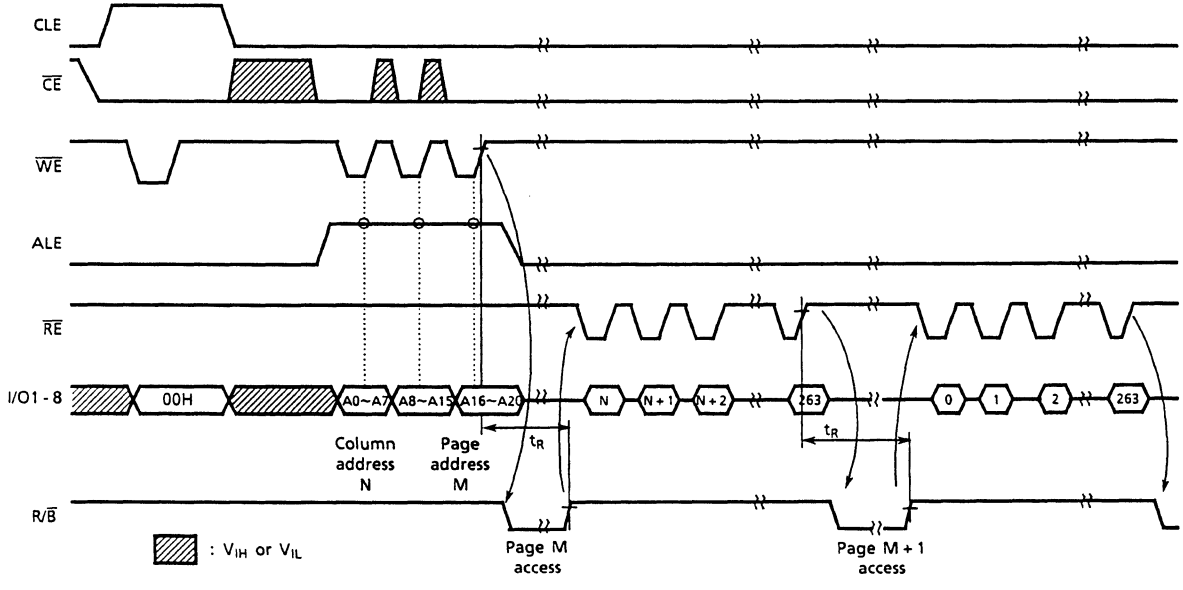
Read Cycle (1): Interception by $\overline{CE}$



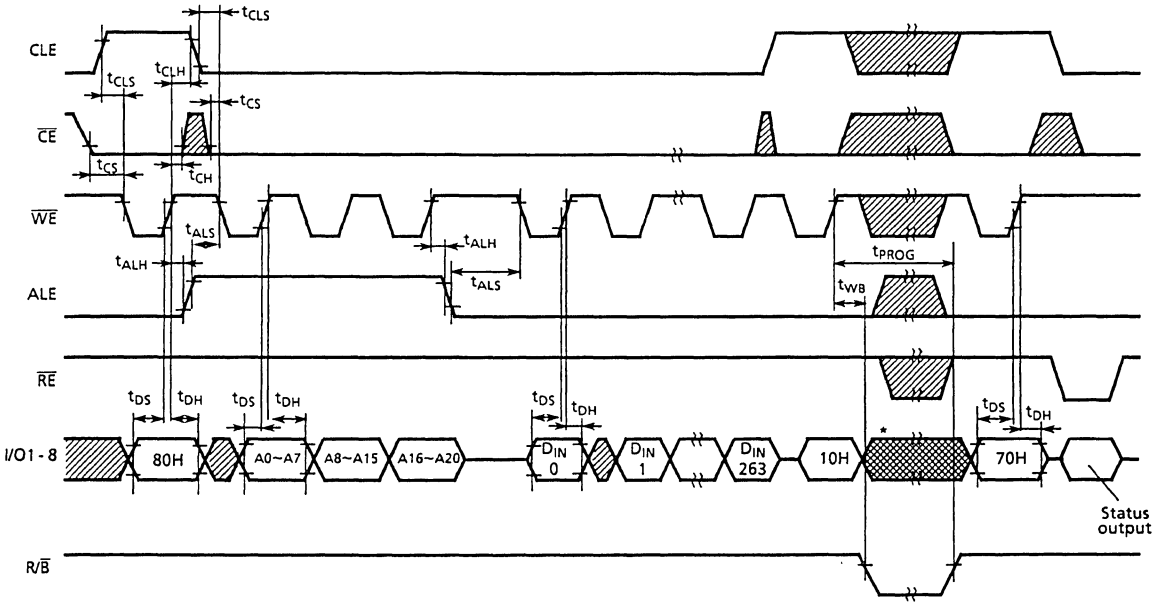
Read Cycle (2)



Sequential Read Timing



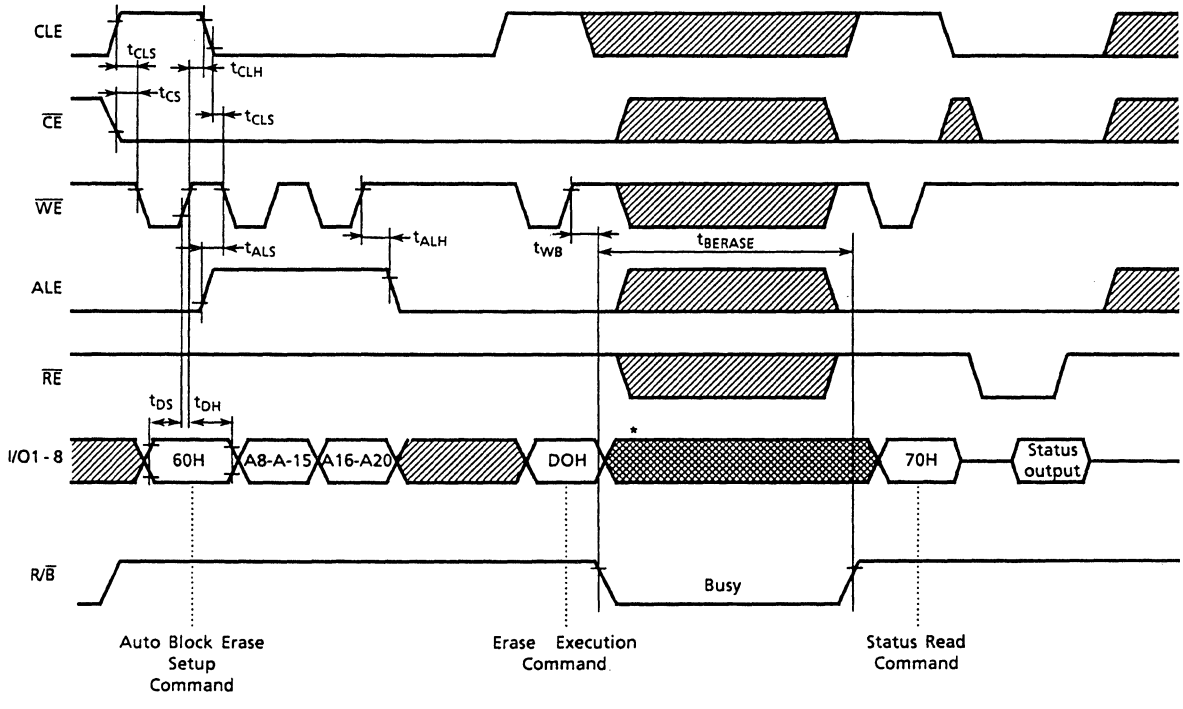
Auto Program Operation Timing Chart



: V_{IH} or V_{IL}

* : Do not collide data input with data output

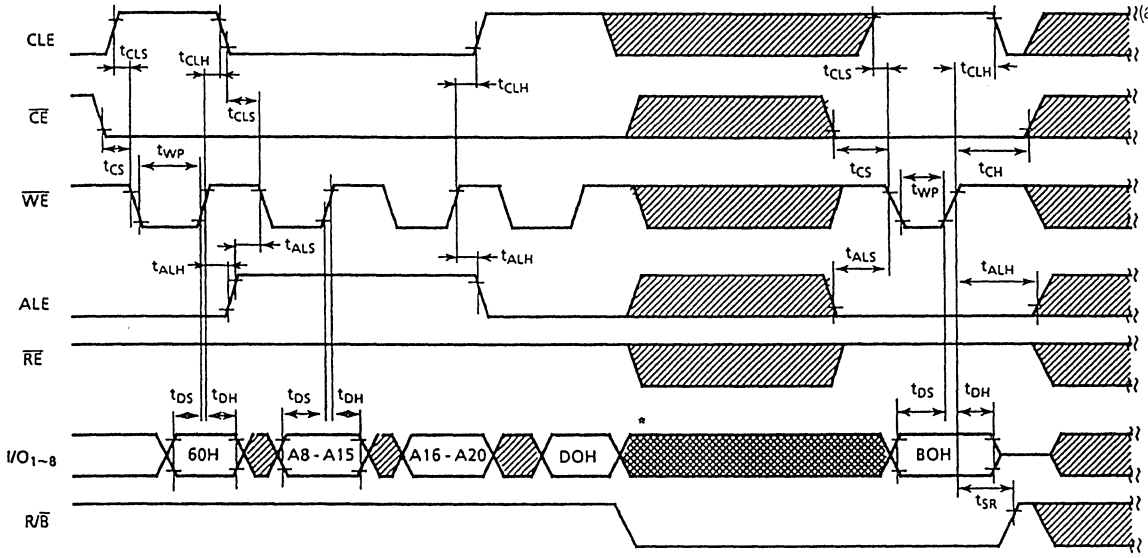
Auto Block Erase Timing

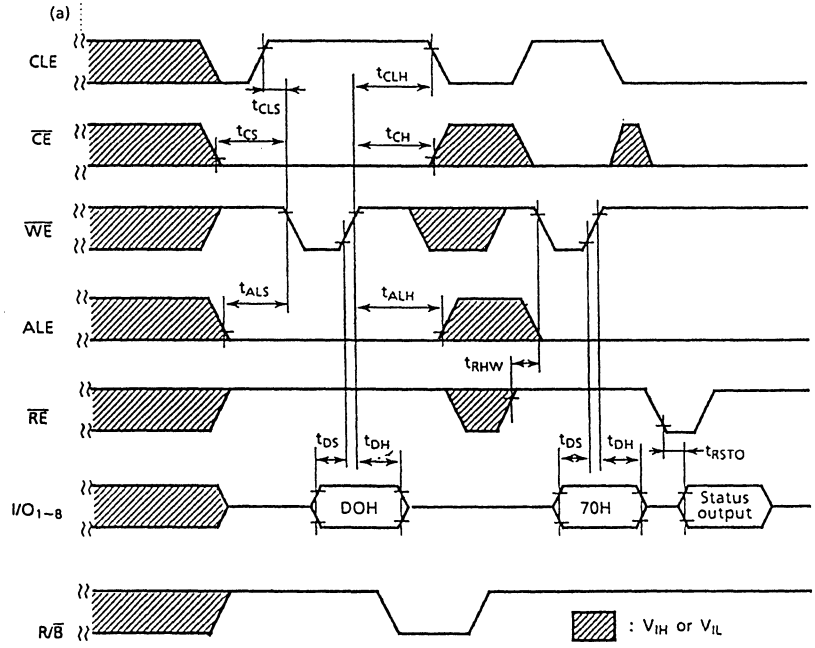


: V_{IH} or V_{IL}

* : Do not collide data input with data output

Suspend/Resume on Block Erase Operation

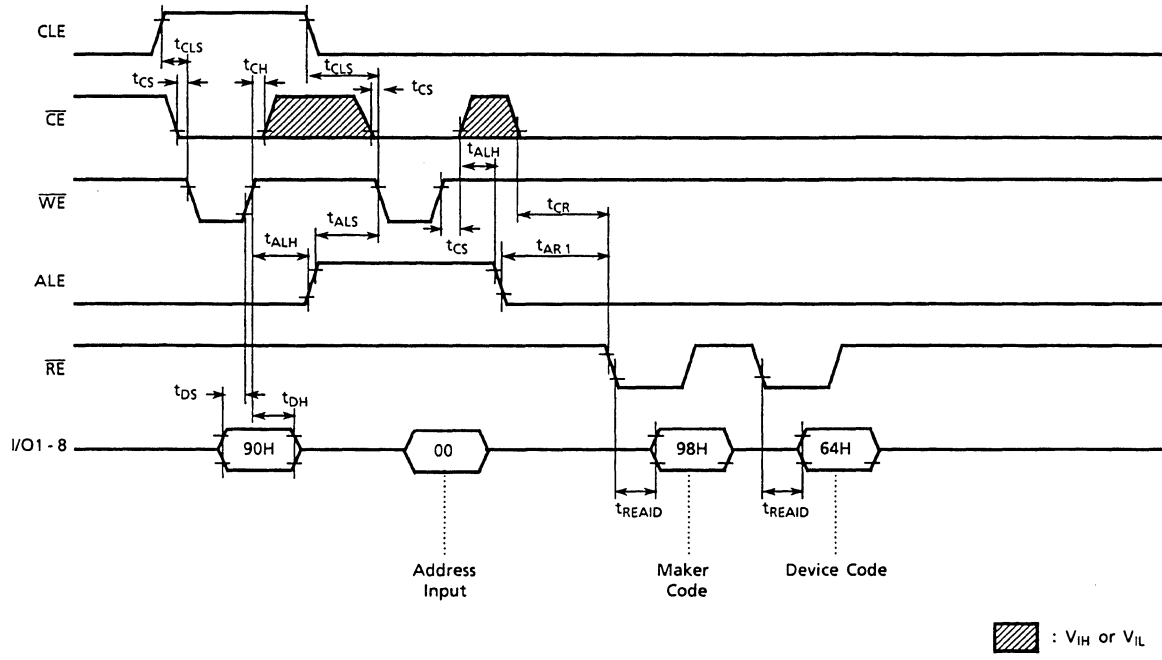




(a) : Continued

* : Do not collide data input with data output

ID Read Operation



Pin Function

The TC5816AFT is a serial access memory in which address and data information is multiplexed. The device pinout is shown in Figure 1.

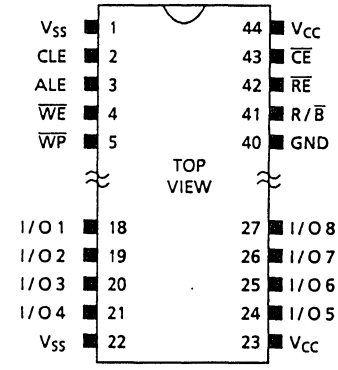


Figure 1. TC5816 Pinout

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$

The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the busy state ($R/\overline{B}$ = L) such as during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input. The $\overline{CE}$ signal must stay low during the read mode busy state.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls the serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O1 ~ 8

The I/O 1 ~ 8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect: $\overline{WP}$

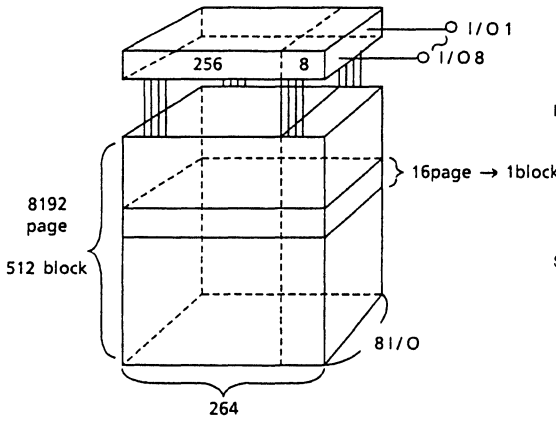
The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: $R/\overline{B}$

The $R/\overline{B}$ output signal is used to indicate the state of the device. The $R/\overline{B}$ signal indicates a busy state ($R/\overline{B}$ = L) during program, erase, or read operations and will return to a ready state ($R/\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

Schematic Cell Layout and Address Assignment

The program operation is implemented in a page unit while the erase operation is carried out in block units.



A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 Page = 264 bytes;

1 Block = 264 bytes x 16 pages = (4K + 128) bytes

Total device density = 264 bytes x 16 pages x 512 blocks
= 16.5M bits (2.0625M bytes)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Figure 3.

Figure 2. TC5816 Schematic Cell Layout

	I/01	I/02	I/03	I/04	I/05	I/06	I/07	I/08
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third cycle	A16	A17	A18	A19	A20	*L	*L	*L

A0 ~ A7 : column address
A8 ~ A20 : page address
(A12 ~ A20: block address
A8 ~ A11 : NAND address in block)

* I/O 6 ~ 8 during the third cycle must be set to low level

Figure 3. Addressing

Operation Mode: Logic and Command Tables

The operation modes such as program, erase, read, erase suspend, and reset are controlled by the ten different command operations shown in Table 2. The address, command input, and data input /output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, and $\overline{WP}$ signals as shown in Table 1.

Table 1. Logic Table

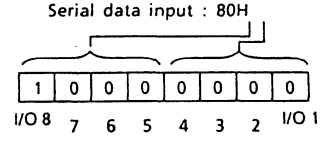
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command input	H	L	L	⌐‾_	H	*
Data input	L	L	L	⌐‾_	H	*
Address input	L	H	L	⌐‾_	H	*
Serial data output	L	L	L	H	_‾⌐	*
During programming (Busy)	*	*	*	*	*	H
During erasing (Busy)	*	*	*	*	*	H
Program, Erase inhibit	*	*	*	*	*	L

$H = V_{IH}$, $L = V_{IL}$, $* = V_{IH}$ or V_{IL}

Table 2. Command Table (HEX data)

	FIRST CYCLE	SECOND CYCLE	ACCEPTABLE COMMAND DURING BUSY
Serial data input	80	–	
Read mode (1)	00	–	
Read mode (2)	50	–	
Reset	FF	–	√
Auto program	10	–	
Auto block erase	60	D0	
Suspend in erasing	B0	–	√
Resume	D0	–	
Status read	70	–	√
ID read	90	–	

Bit assignment of HEX data (Example)



Once the device is set into the read mode by the "00H" or "50H" command, additional read commands are not needed for sequential page read operations. Table 3 shows the operation mode for reads.

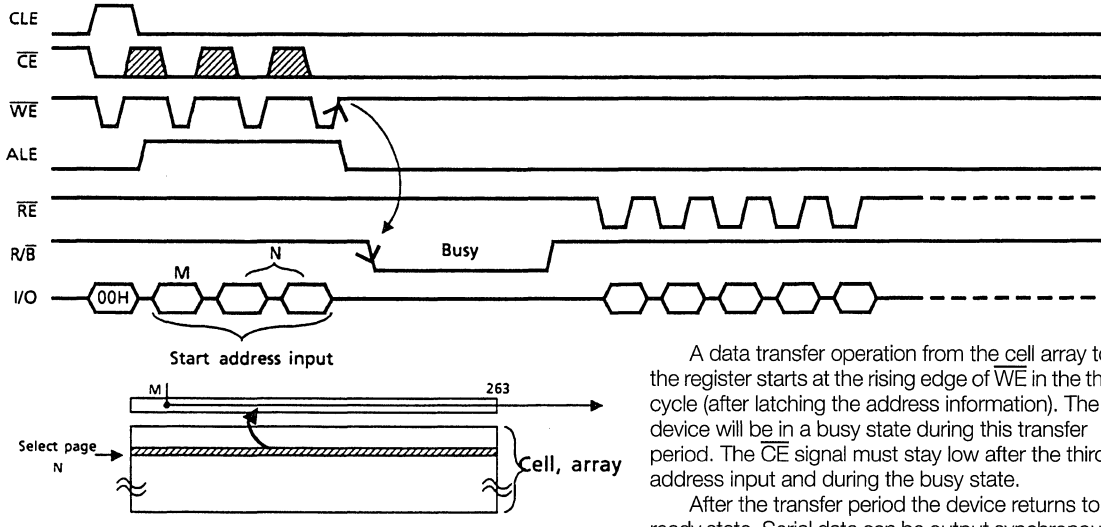
Table 3. Operation mode for reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/01 ~ I/08	POWER
Read mode	L	L	L	H	L	Data output	Active
Output deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

Device Operation

Read Mode (1)

Read mode (1) is set by issuing a "00H" command to the command register. Refer to Figure 4 below for timing details and block diagram.



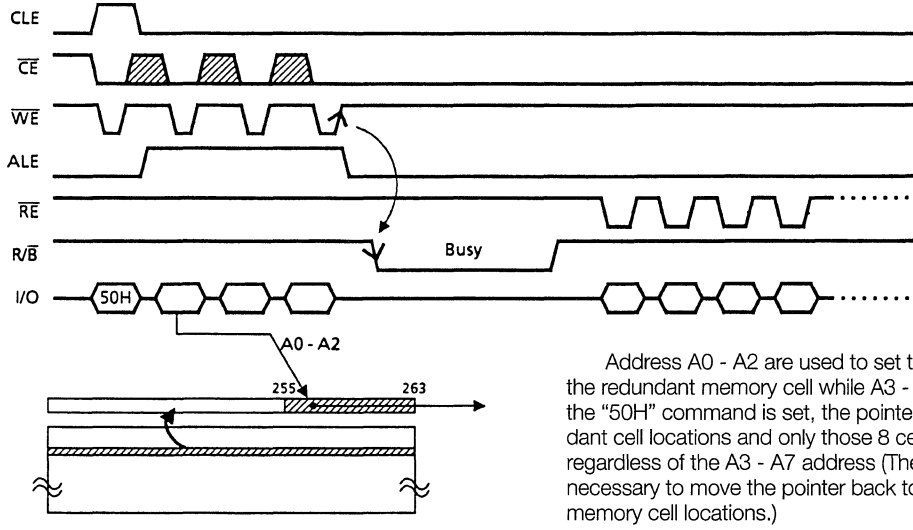
A data transfer operation from the cell array to the register starts at the rising edge of WE in the third cycle (after latching the address information). The device will be in a busy state during this transfer period. The CE signal must stay low after the third address input and during the busy state.

After the transfer period the device returns to a ready state. Serial data can be output synchronously with the RE clock from the designated starting pointer indicated during the address input cycle.

Figure 4. Read mode (1) operation

Read Mode (2)

Read mode (2) has the same timing as read mode (1) but it is used to access information in the extra 8 byte redundancy area of the page. The starting pointer is therefore assigned between byte 256 and 263.



Address A0 - A2 are used to set the starting pointer for the redundant memory cell while A3 - A7 are ignored. Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed regardless of the A3 - A7 address (The "00H" command is necessary to move the pointer back to the 0 - 255, main memory cell locations.)

Figure 5. Read mode (2) operation

Sequential Read (1)(2)

This mode allows sequential reads without additional address input.

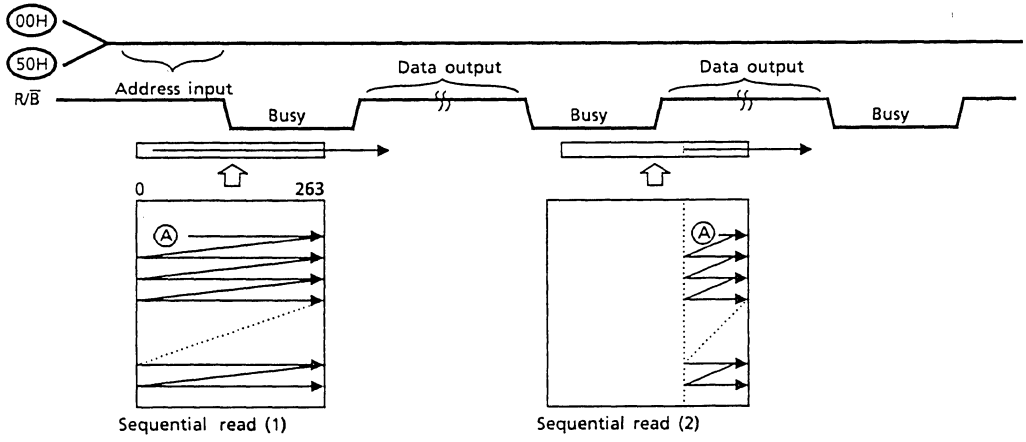


Figure 6. Sequential read

Sequential read mode (1) outputs data from addresses 0 to 263 while sequential read mode (2) outputs data from the 8-byte redundant area only. When the pointer reaches the last address, the device continues to output data from the last address with each $\overline{RE}$ clock signal.

Status Read

The TC5816 automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the ready/busy status of the device, determines the pass /fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 4.

Table 4. Status output table

	STATUS	OUTPUT	
I/O 1	Pass/Fail	Pass: "0"	Fail: "1"
I/O 2	Not used	"0"	
I/O 3	Not used	"0"	
I/O 4	Not used	"0"	
I/O 5	Not used	"0"	
I/O 6	Suspend	Suspended: "1"	Not Suspended: "0"
I/O 7	Ready/Busy	Ready: "1"	Busy: "0"
I/O 8	Write protect	Protect: "0"	Not Protect: "1"

The Pass/Fail status on I/O 1 is only valid when the device is in the ready state. The device will always indicate a pass status while in the busy state.

An application example with multiple devices is shown in Figure 7.

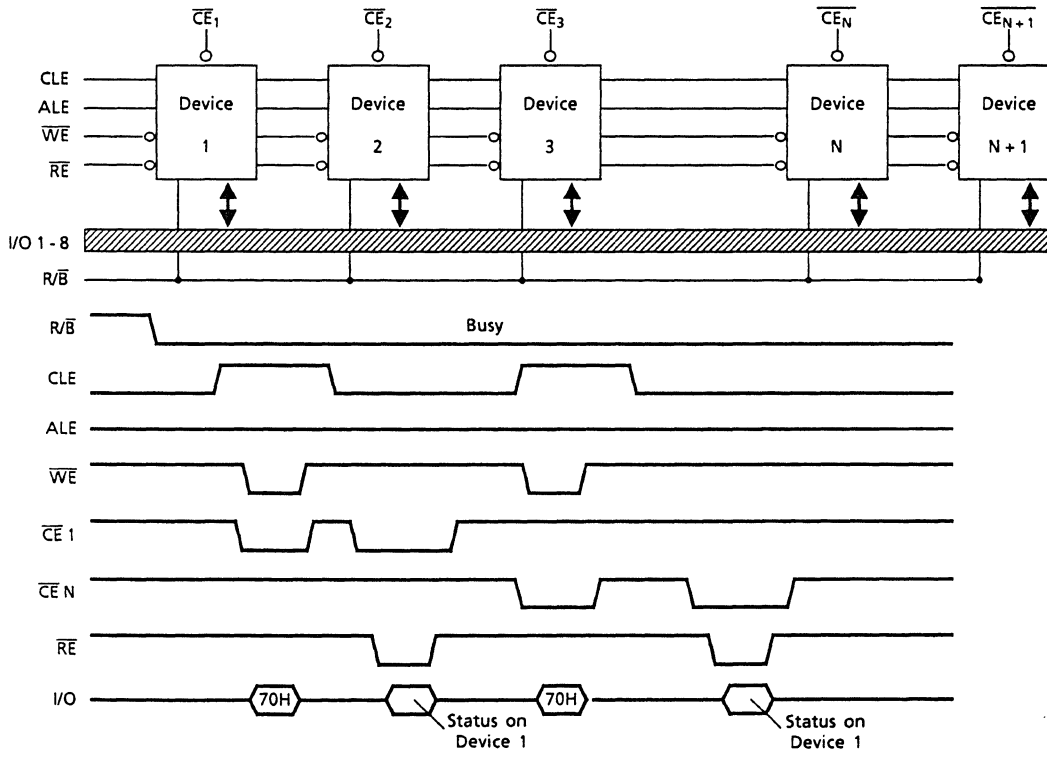
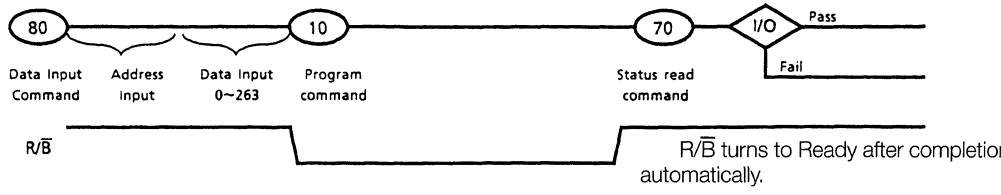


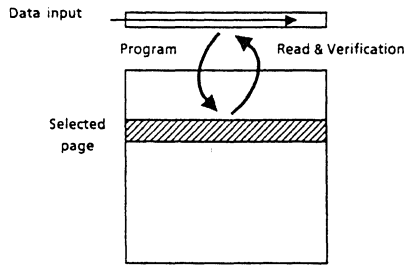
Figure 7. Status read timing application example

SYSTEM DESIGN NOTE: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status read function can be used to determine the status of each individually selected device.

Auto Page Program

The TC5816 implements the automatic page program operation after receiving a "10H" program command after the address and data have been input. The sequence of command, address, and data input is shown below. (Refer to the detail timing chart.)





The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the "10H" command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

Figure 8. Auto Page Program

Auto Block Erase

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command "D0H" (which follows the erase setup command "60H"). This two cycle process for erase operations acts as an extra layer of protection from accidental erasure of data due to possible external noise. The device automatically executes the erase and verify operations.

Auto Block Erase

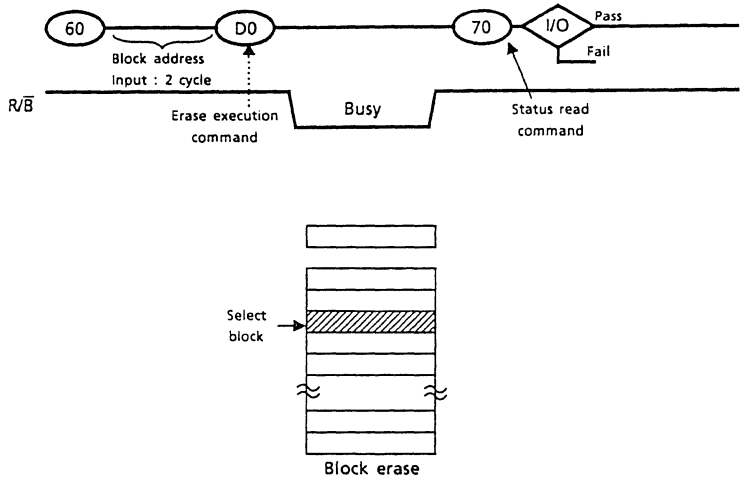


Figure 9. Auto Block Erase Operation

Suspend/Resume

Because a block erase operation can keep the device in a busy state for an extended period of time, the TC5816 has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence for this operation are shown below. (Refer to the detail timing chart)

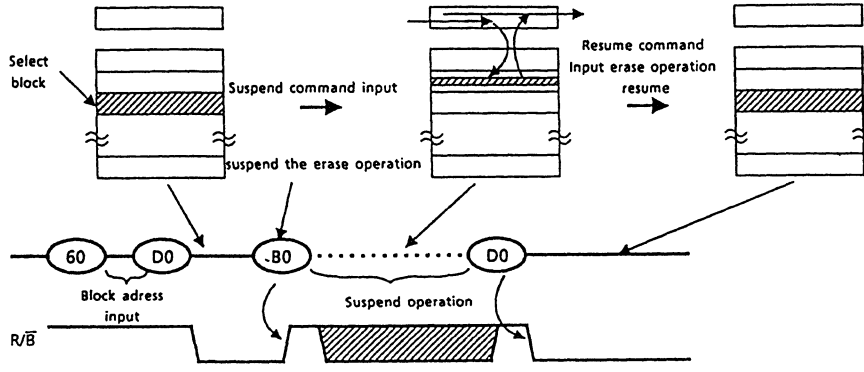


Figure 10. Suspend /Resume Operation

The B0 ····· D0 suspend/resume cycle can be repeated up to 20 times during a block erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

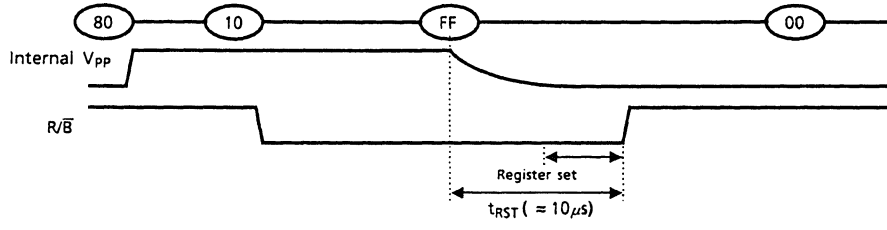
Reset

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go into a wait state. The address and data register are set after a reset as follows:

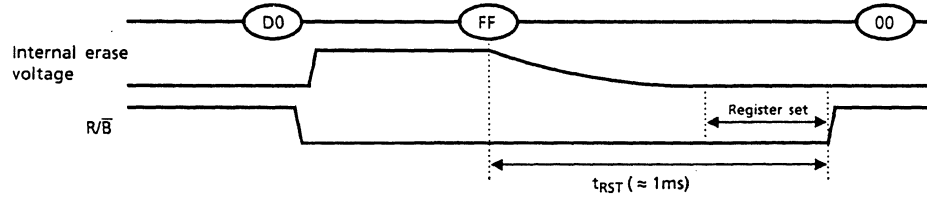
- Address Register : All "0"
- Data Register : All "1"
- Operation Mode : Wait State

The response after a "FFH" reset command input is as follows:

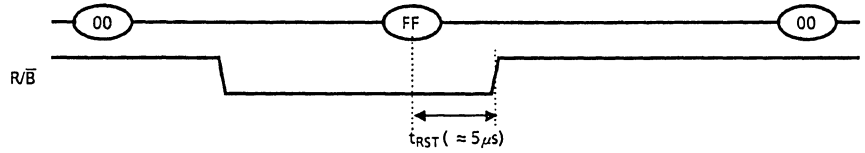
- If the reset (FFH) command is input during programming: Figure 11



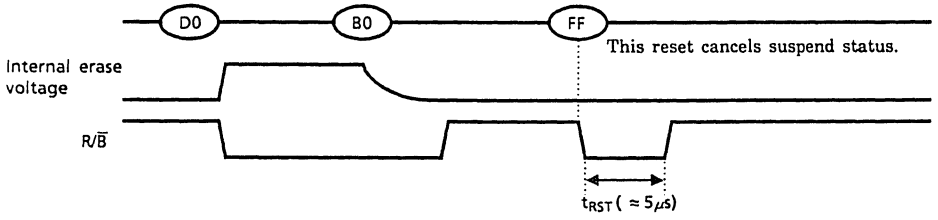
- If the reset (FFH) command is input during erasing: Figure 12



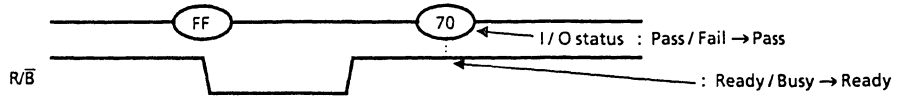
• If the reset (FFH) command is input during the read operation: Figure 13



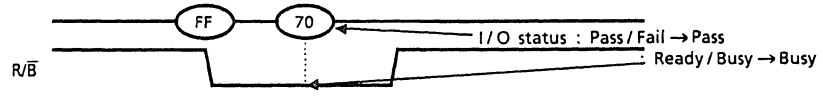
• If the reset (FFH) command is input after suspend: Figure 14



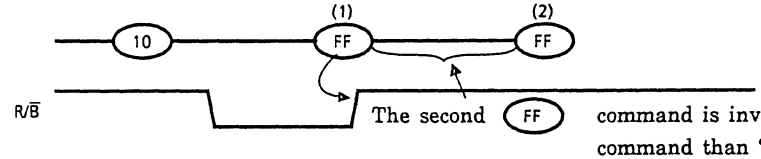
• If the status read command (70H) is input after reset: Figure 15



However, the following operation is prohibited. If the following operation is executed, set up for the address and data register cannot be guaranteed.



• If the reset command is input in succession: Figure 16



ID Read

The TC5816 contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

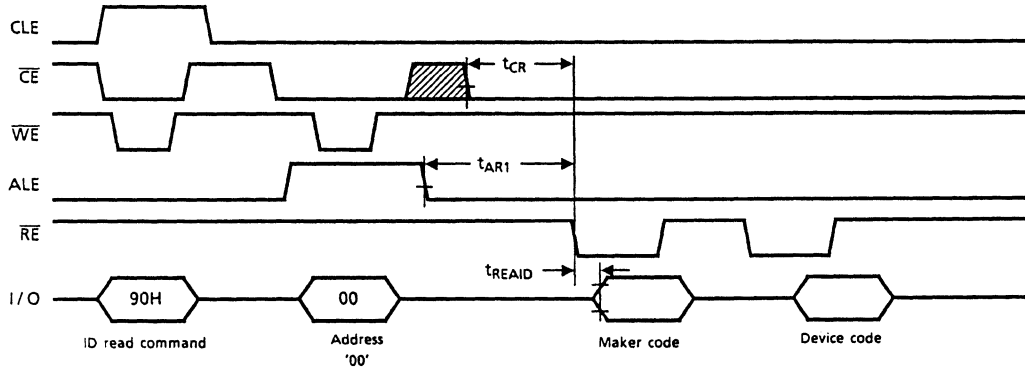


Figure 17. ID read timing

Table 5. Code table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	HEX data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	0	0	1	0	0	64H

Refer to AC characteristics for t_{REAID}, t_{CR}, t_{AR1} (Refer to the specification).

Device Physics

Program Operation

Figure 18 shows the NAND memory cell and details of the programming mechanism. The program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example showing the operations necessary to program '0' data in TR1 and "1" data in TR2 follows:

(1) The select lines are activated so that the transistor array is connected to the bit line and disconnected from the ground line.
(2) V_{PP} (~20V) is applied to the selected word line and an inhibit voltage of VPI (≈10V) is applied to the unselected word lines.
(3) The bit line tied to cell transistor TR1 is biased to 0V and the bit line tied to TR2 is biased to the inhibit voltage of VDPI (≈10V).
(4) V_{PP} is applied between the control gate and the channel in TR1, as shown in Figure 18, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.
(5) The injected electrons are captured in the floating gate (which is surrounded by an oxide layer) and will remain, even after power is cut off, until they are removed by an erase operation.
(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10V because the voltage of the channel is 10V. Therefore, tunneling does not take place. (i.e. electrons are not injected into the floating gate.)
(7) Tunneling does not take place in the unselected pages because of the 10V (VPI) being applied to the unselected word lines which again makes the voltage difference between control gate and channel only 10 volts. Thus, the floating gate of the "0" cell is charged to "minus" and that of the "1" cell is charged to "plus".

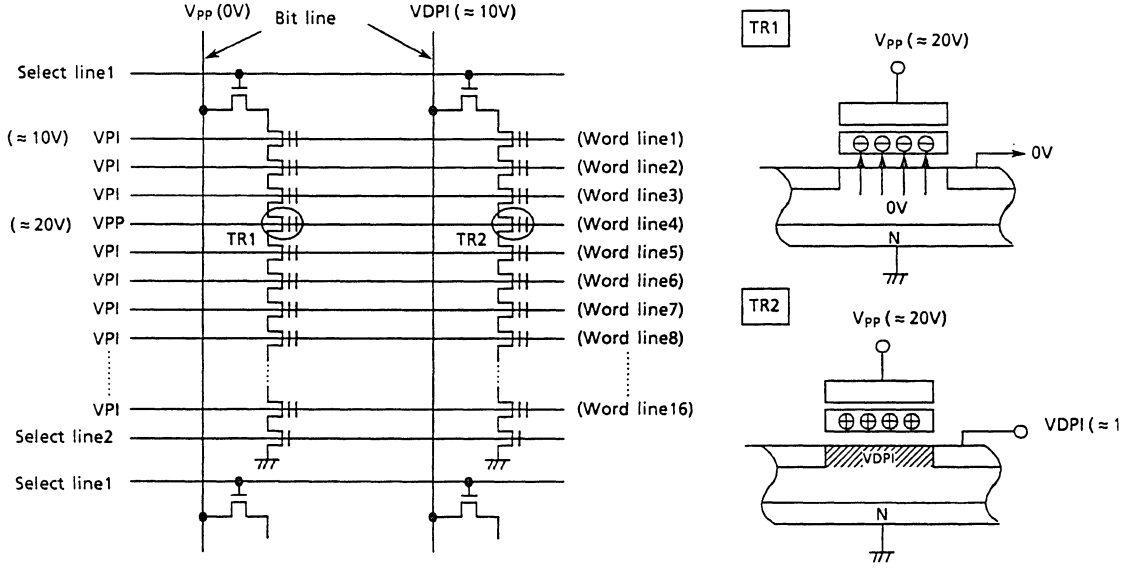


Figure 18. TC5816 Program Device Physics

Erase Operation

Figure 19 shows the NAND memory cell and details of the erase mechanism. The erase operation is used to turn the "0" (programmed) cells back to "1" in a block. Zero volts is applied to the control gate and V_{PP} (~20V) is applied to the substrate so that a 20 volt potential is created and the electrons in the floating gate are pulled out through tunneling.

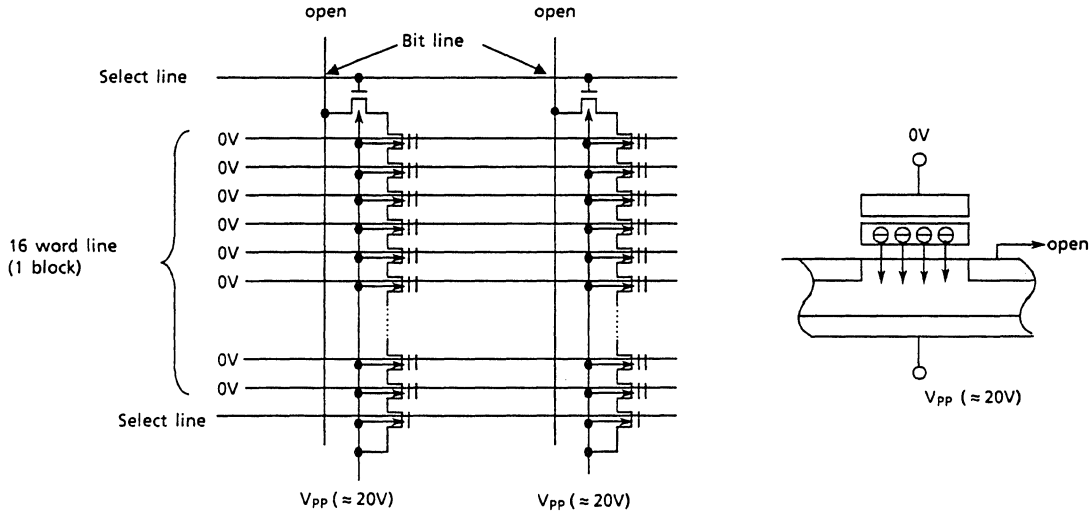


Figure 19. TC5816 Erase Device Physics

Read Operation

The state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate) after programming. Each state is indicated as the "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 20. The threshold voltage of a transistor with "0" data falls within the "plus" distribution while the threshold voltage of a transistor with "1" data falls within the "minus" distribution. The distribution band depends on transistor fluctuations.

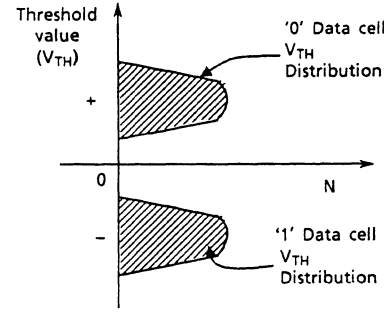


Figure 20. V_{TH} Distribution for "0" and "1" data cell

Figure 21 shows the memory cell and details of the read operation:

(1) Select lines 1 and 2 in the block including the selected page are biased at a high level so that the 16 NAND memory cell array is connected to the bit line and ground.

(2) Zero volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 21, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground while the precharged bit line tied to TR1 remains at a high level because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

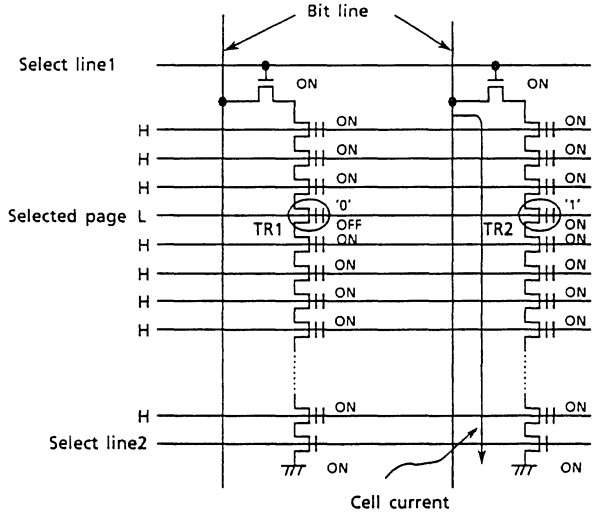


Figure 21. TC5816 Read Device Physics

Application Notes and Comments

(1) Prohibition of unspecified commands

The operation commands are listed in Table 1. Data input as a command other than the specified commands in Table 1 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer control for "00H", "50H"

The TC5816AFT has two read modes which set the destination of the pointer to either the main memory area of a page or the redundancy area. The pointer can point to any location from 0 to 255 in read mode (1) and from 256 to 263 in read mode (2). Figure 22 shows the block diagram of their operations.

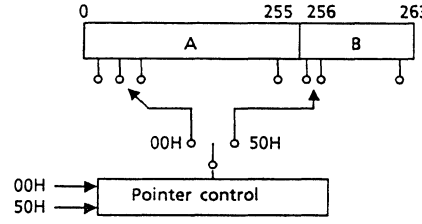


Figure 22. Pointer control

The pointer is set to region "A" by the "00H" command and to region "B" by the "50H" command.

(Example)
The "00H" command needs to be input to set the pointer back to region "A" when the pointer control points to region "B".

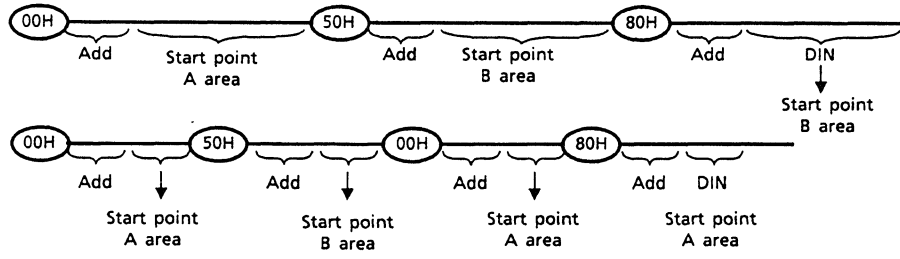
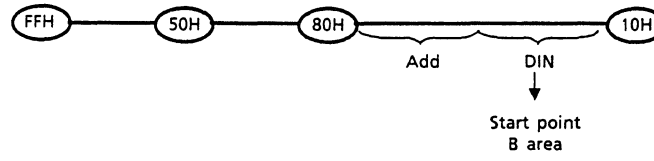


Figure 23. Example for Pointer Set

For programming into region B only, first reset the contents of the data register to "1"s by inputting the FFH (reset) command.



(3) Acceptable commands after the serial input command "80H"

Once the serial input command ("80H") is input, do not input any command other than the program execution command ("10H") or the reset command ("FFH") during programming.

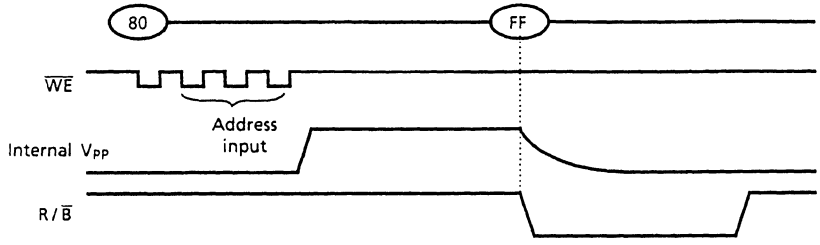
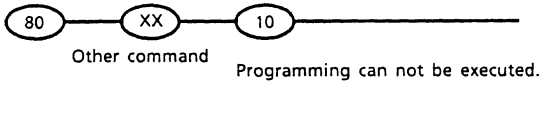


Figure 24

If a command other than "10H" or "FFH" is input, the program operation is not performed.



In this case, the reset command (FFH) command is needed.

(4) Status read during read operation

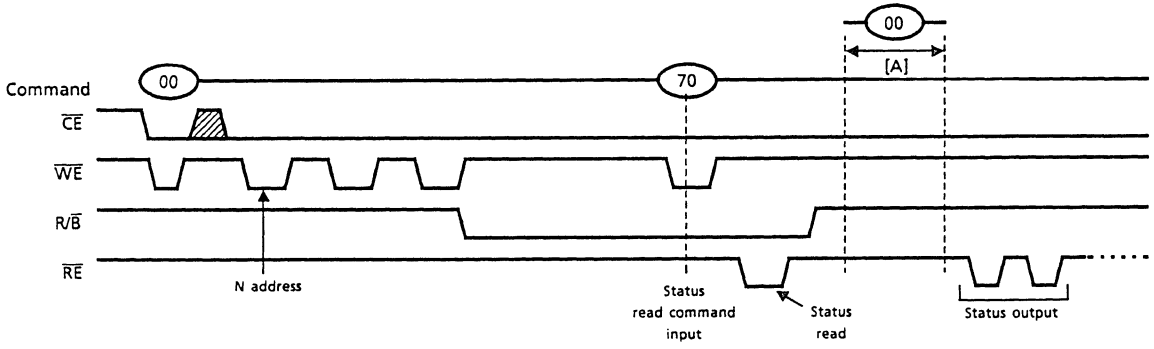


Figure 25

The device status can be read out by inputting the status read command "70H" during the read mode. Once the device is set to the status read mode after a "70H" command input, the device does not return to the read mode.

Therefore, status read during the read operation is prohibited.

However, when the read command "00H" is input during [A], the status mode is reset, and the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) Suspend command "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.

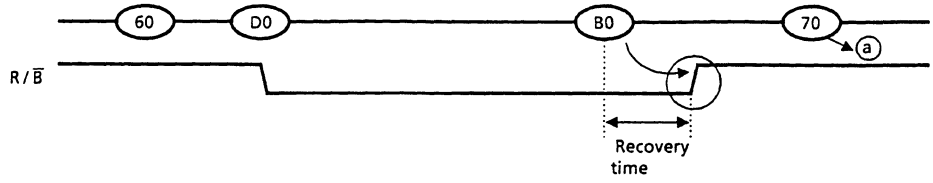


Figure 26

Although the device status changes from busy to ready after "B0H" is input, the following two cases cannot be distinguished.

-After a "B0H" command input, Busy→Ready

-After an erase operation is finished with "D0H", Busy→Ready

Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to ready.

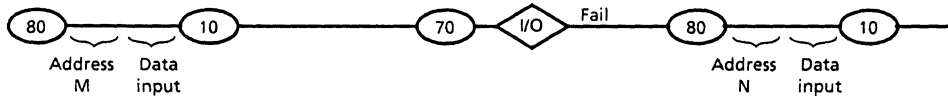
The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

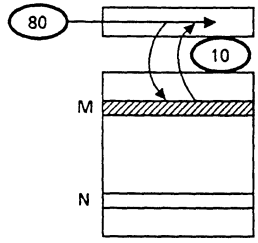
-"B0H" has been accepted: Erase operation is executed. (The device is busy.)

-"B0H" has not been accepted. (Erase operation has been completed): "D0H" command cannot be accepted. (The device is ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) Program fail





When the programming result for the page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

Figure 27

(7) Data transfer

The data in page address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e. "1" data will become "0" and "0" will become "1").

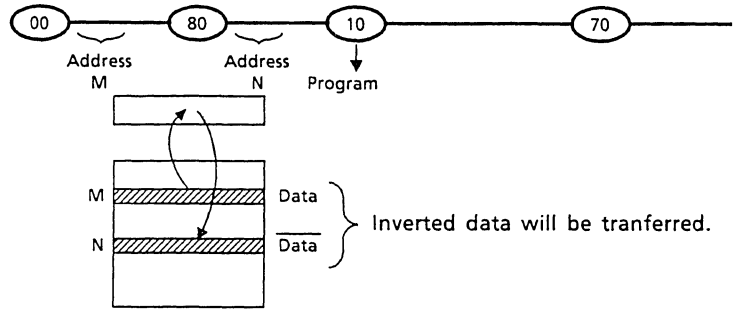
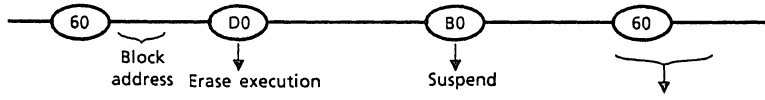


Figure 28

(8) Block erase after suspend command "B0H"

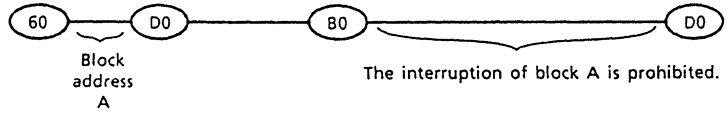


A block erase command is prohibited when the device has been suspended by inputting "B0H" during a block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

D. Non-Volatile

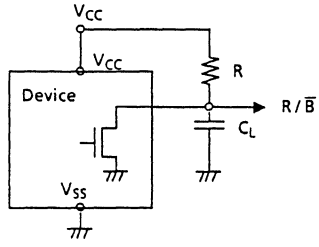
(9) Interruption of an erasing block

After a "B0H" command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



(10) R/$\overline{B}$: Termination for the Ready/Busy pin (R/$\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.



This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.

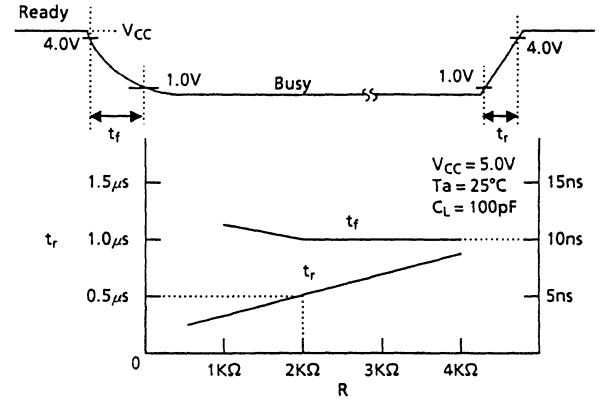


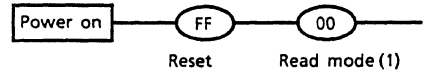
Figure 29

(11) Status After Power On

Although the device is set to read mode after power-up, the following sequence is needed because each input signal may not be stable at power on.

- Operation mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminate
- High voltage generation circuit : Off state

Power on sequence



(12) Power On/Off Sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:

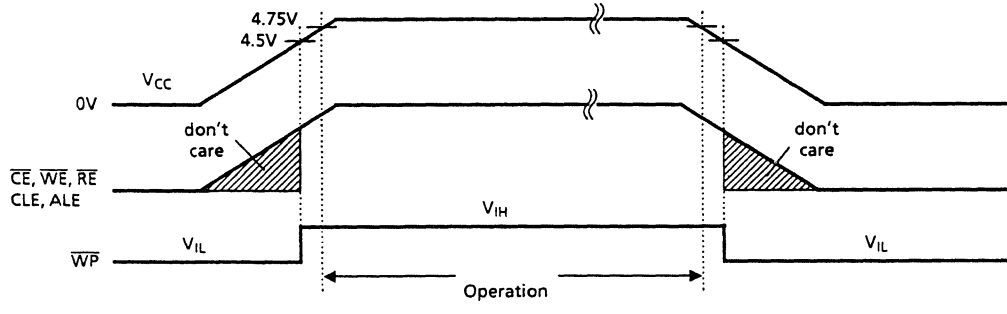


Figure 30. TC5816 Power On/Off Sequence

(13) Setup for $\overline{WP}$ Signal

The erase and program operations are compulsively reset when $\overline{WP}$ goes low. The $\overline{WP}$ signal must be kept at a high level before the 80H/60H command input for the program and erase operations.

If $\overline{WP}$ goes high after the 80H/60H command input for a program/erase operation, the program and erase operations cannot be guaranteed.

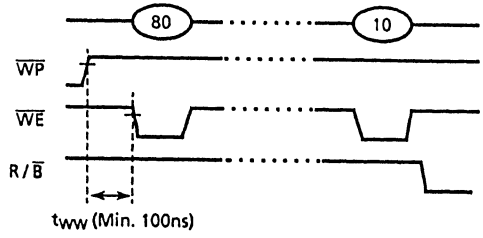


Figure 31. $\overline{WP}$ Setup before Programming

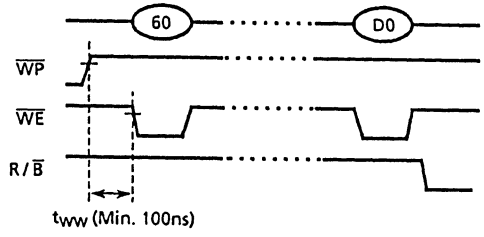


Figure 32. $\overline{WP}$ Setup before Erasing

(14) In the case that 4 address cycles are input

Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation:

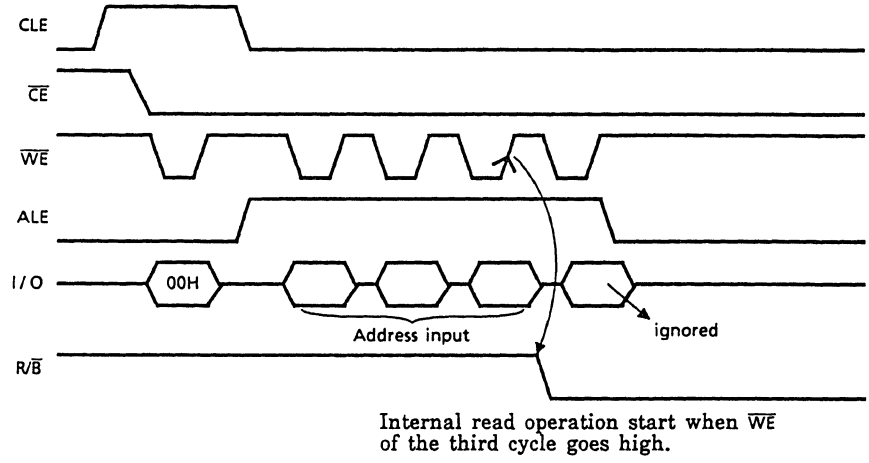


Figure 33

Program operation:

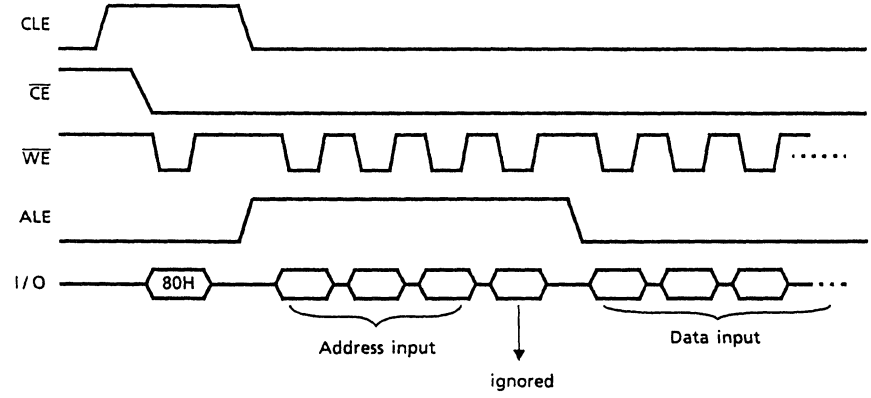


Figure 34

(15) Divided program in the same page (Partial page program)

The device allows a page to be divided into 10 segments (typically) with each page segment programmed individually as follows:

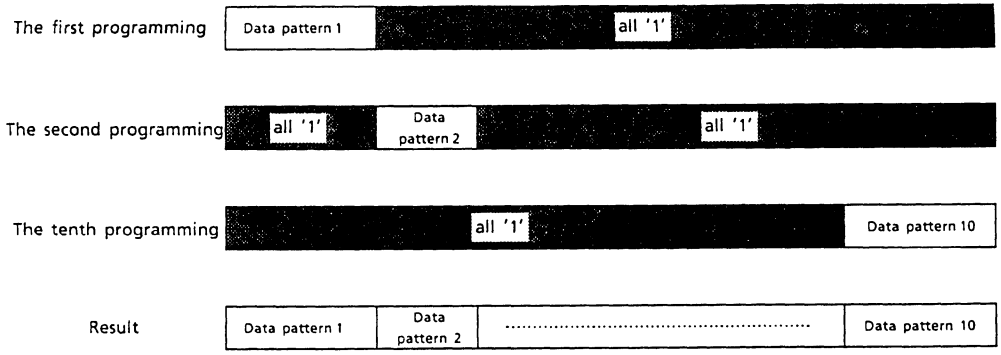


Figure 35

Note: The input data for unprogrammed or previously programmed page segments must be "1" (i.e. Mask all page bytes outside the segment to be programmed with "1" data.).

(16) $\overline{RE}$ Signal During Read

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in the read mode. Therefore, once the device is set into the read mode by the "00H" or "50H" command, the internal column address counter can be incremented by the $\overline{RE}$ clock before or after the address input. Assuming that $\overline{RE}$ clocks before the address input and the pointer reaches the last column address, an internal read operation (array→register) will occur and the device will be in a busy state. (See Figure 36)

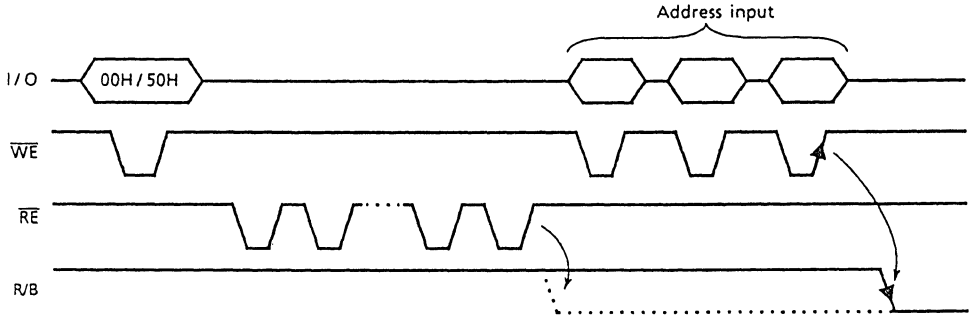
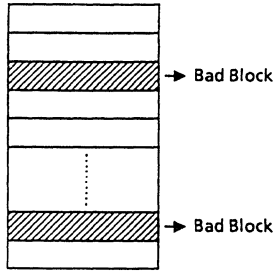


Figure 36

Therefore, $\overline{RE}$ clocking must occur after the address input.

(17) Invalid block (bad block)

The TC5816 device contains unusable blocks. Therefore, the following issues must be recognized:



Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate. The number of valid blocks is as follows:

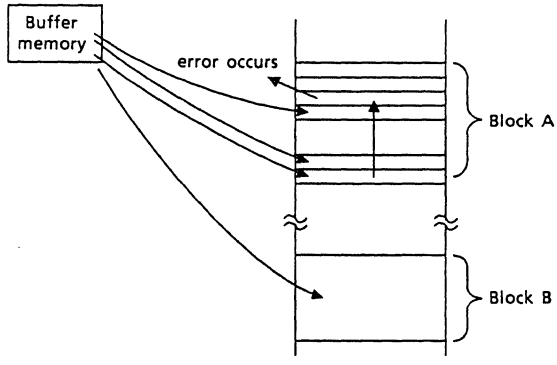
	MIN.	TYP.	MAX.	UNIT
Valid (Good) Block Number	502	508	512	Blocks

Figure 37 shows the bad block test flow.

(18) Error in program or erase operation (Fail at status read)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs.

Program

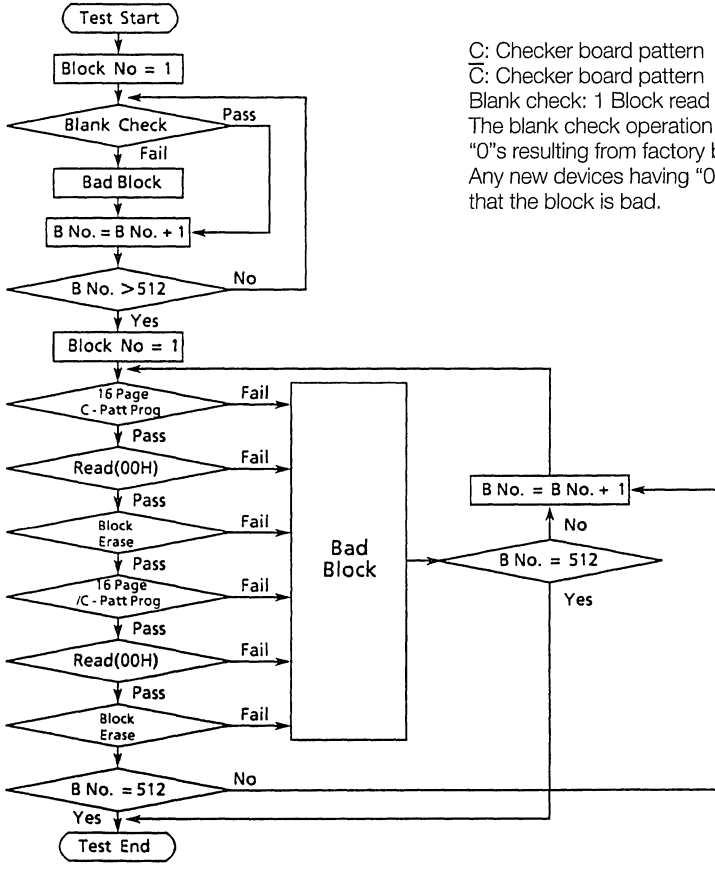


When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad blocks" table or another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)

Bad Block Test Flow

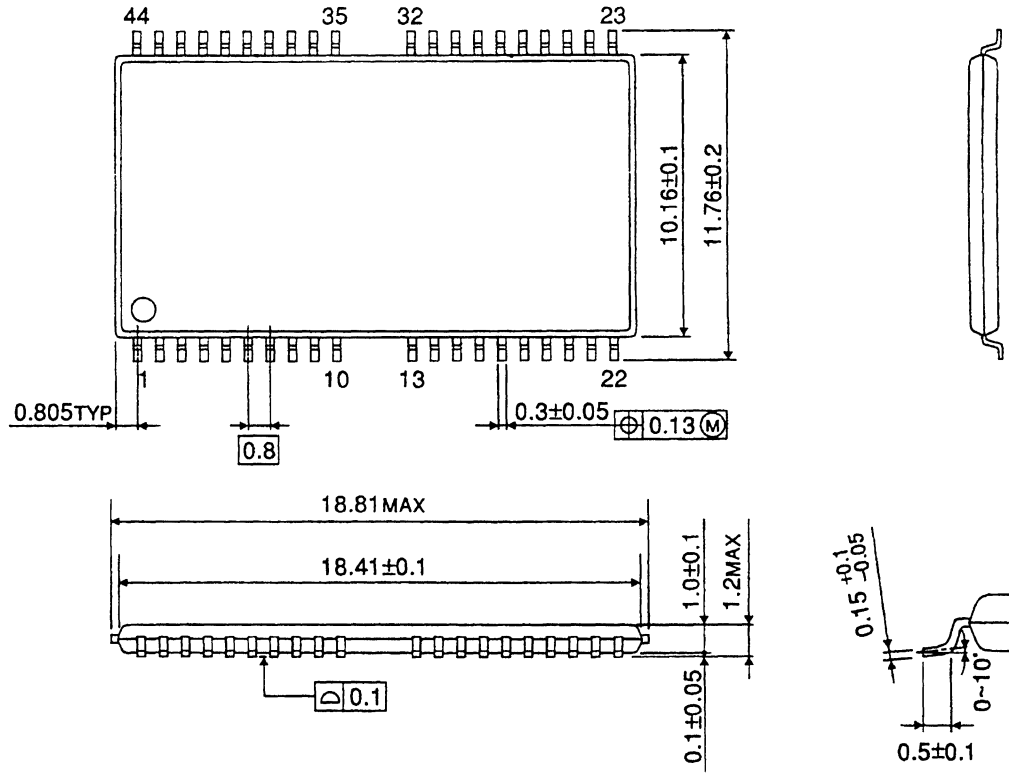


C: Checker board pattern
$\overline{C}$: Checker board pattern
Blank check: 1 Block read (FFH)
The blank check operation detects "0"s resulting from factory block testing.
Any new devices having "0"s in a block indicates that the block is bad.

Figure 37. Bad Block Test Flow

Outline Drawings

Plastic TSOP TSOP44-P-400B Unit: mm



Weight: 0.48g (typ.)

TC5816ADC

16Mbit (2M x 8 BIT) CMOS NAND EEPROM

PRELIMINARY

Description

The TC5816 is a 5 volt 16M bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) with a spare 64k x 8 bits. This device is organized as 264 bytes x 16 pages x 512 blocks. The device has a 264 byte static register which allows program and read data to be transferred between the register and the memory cell array in 264 byte increments. The erase operation is implemented in a single block unit (4k bytes + 128 bytes: 264 bytes x 16 pages).

The TC5816 is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for still cameras, and other systems which require high density, non-volatile memory data storage.

Actual Size

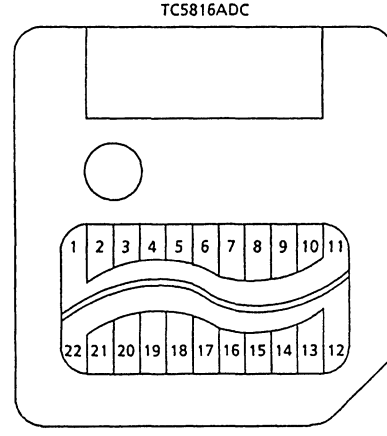
Features

- Organization
  - Memory cell array : 264 x 8K x 8
  - Register : 264 x 8
  - Page size : 264 bytes
  - Block size : (4k + 128) bytes
- Modes : Read, Reset, Auto page program, Auto block erase, Suspend/ Resume, Status read
- Mode control : Serial input/output Command control
- Package
  - TC5816ADC : FDC-22 (Weight: 1.8g typ.)
- Power supply : V_{CC} = 5V±10%
- Access time
  - Cell array - Register : 25μs max.
  - Serial access : 80ns min.
- Operating current
  - Read (80ns cycle) : 15mA typ.
  - Program (ave.) : 40mA typ.
  - Erase (ave.) : 20mA typ.
  - Standby : 100μA
- Operating temperature : 0 ~ 55°C

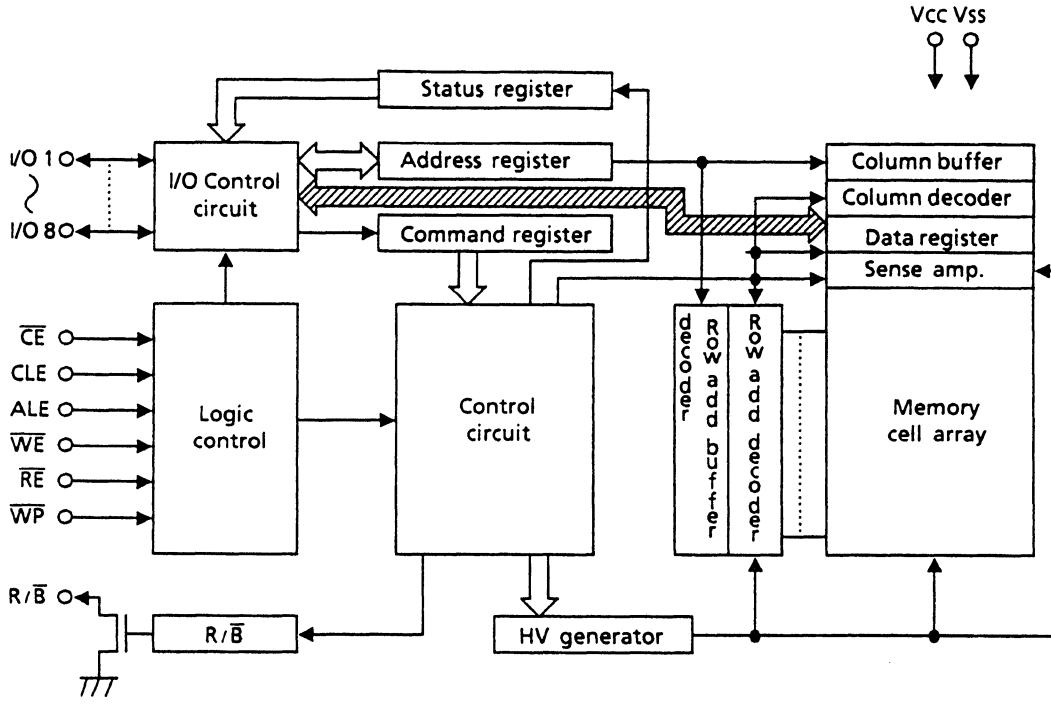
Pin Assignment

1, 10, 11	V_{SS}	Ground
2	CLE	Command Latch Enable
3	ALE	Address Latch Enable
4	$\overline{WE}$	Write Enable
5	$\overline{WP}$	Write Protect
6 ~ 9	$I/O_{1 \sim 4}$	I/O Port
13 ~ 16	$I/O_{5 \sim 8}$	I/O Port
17	NC	No Connection
18	GND	Ground Input
19	R/$\overline{B}$	Ready/Busy
20	$\overline{RE}$	Read Enable
21	$\overline{CE}$	Chip Enable
22, 12	V_{CC}	Power Supply (5V)

Pin Connection (Top View)



Block Diagram



Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6V ~ V_{CC} + 0.5V (≤ 7V)	
P_D	Power Dissipation	0.5	W
T_{STG}	Storage Temperature	-20 ~ 65	°C
T_{OPR}	Operating Temperature	0 ~ 55	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	

*This parameter is periodically sampled and is not 100% tested.

Valid Blocks (1)

SYMBOL	PARAMETER	TC5816			UNIT
		MIN.	TYP.	MAX.	
N_{VB}	Valid block number	502	508	512	Blocks

(1) The TC5816 includes unusable blocks. Refer to notification (17) toward the end of this document.

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{CC} + 0.5	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	

* -2V (pulse width ≤ 20ns)

DC Characteristics (Ta = 0 ~ 55°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{CC}		–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}		–	–	±10	
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	t_{cycle} = 80ns	–	15	30	mA
I_{CCO2}	Operating Current (Serial Read)		t_{cycle} = 1µs	–	–	5	
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 80ns		–	15	30	
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 80ns		–	50	70	
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 80ns		–	15	30	
I_{CCO6}	Operating Current (Register Read)	t_{cycle} = 80ns		–	15	30	
I_{CCO7}	Program Current	–		–	40	60	
I_{CCO8}	Erasing Current	–		–	20	40	
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2V		–	–	100	µA
V_{OH}	High Level Output Voltage	I_{OH} = - 400µA		2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		–	–	0.4	
$I_{OL}(R/\overline{B})$	Output Current of (R/$\overline{B}$) pin	V_{OL} = 0.4V		–	10	–	mA

AC Characteristics (Ta = 0 ~ 55°C, V_{CC} = 5V±10%) (1)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{CLS}	CLE Setup Time	20	–	ns	
t_{CLH}	CLE Hold Time	40	–	ns	
t_{CS}	$\overline{CE}$ Setup Time	20	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	40	–	ns	
t_{WP}	Write Pulse Width	40	–	ns	
t_{ALS}	ALE Setup Time	20	–	ns	
t_{ALH}	ALE Hold Time	40	–	ns	
t_{DS}	Data Setup Time	30	–	ns	
t_{DH}	Data Hold Time	20	–	ns	
t_{WC}	Write Cycle Time	80	–	ns	(2)
t_{WH}	$\overline{WE}$ High Hold Time	20	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Falling Edge	100	–	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	–	ns	
t_{RC}	Read Cycle Time	80	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	45	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in the Serial Read Cycle	250	–	ns	(4)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	–	90	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	5	20	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	–	30	ns	
t_{REH}	$\overline{RE}$ High Hold Time	20	–	ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	45	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	55	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low (Status Read)	50	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low (Status Read)	50	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	200	–	ns	
t_{R}	Memory Cell Array to Starting Address	–	25	µs	
t_{WB}	$\overline{WE}$ High to Busy	–	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (read cycle)	150	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (Sequential Read)	–	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of Interception by $\overline{CE}$ during Read Mode)	–	100 + tr ($R/\overline{B}$)	ns	(3)
t_{RST}	Device reset time (Read/Program/Erase/after suspend)	–	10/20/1500/10	µs	

AC Test Conditions

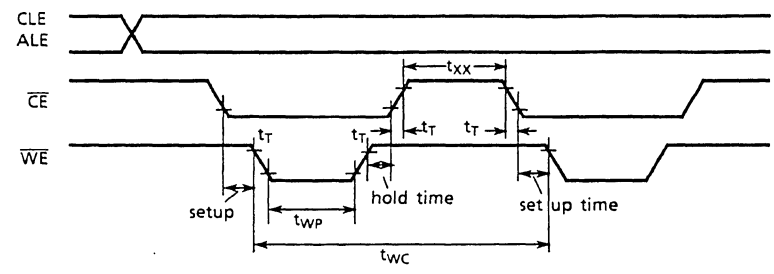
Input Level	2.4V/0.6V
Input Timing Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1 TTL and C_L (100 pF)

(1) Transition time (t_T) = 5ns.

(2) In the case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 80ns.

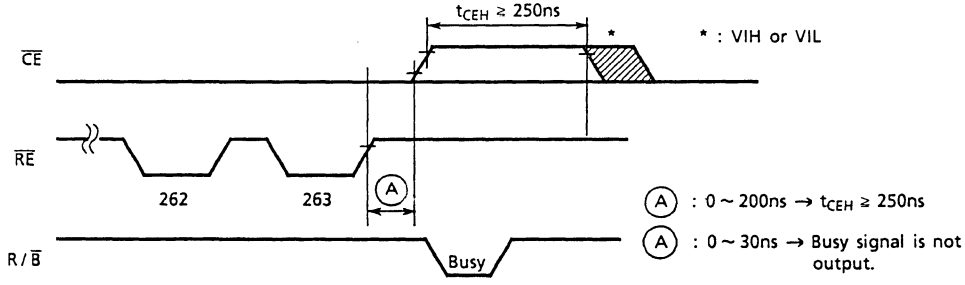
$$\underset{20ns}{\text{set - up time}} + \underset{40ns}{\text{hold time}} + \underset{40ns}{t_{WP}} + \underset{20ns}{t_{XX}} + 4t_T$$

(ex.)



(3) The $\overline{CE}$ high to Ready time depends on the pull up resistor tied to the R/$\overline{B}$ pin. (Refer to notification (10) toward the end of this document.)

(4) If $\overline{CE}$ returns to a high level after accessing the last address (263) in read mode (1) or (2), $\overline{CE}$ high time must keep equal to or greater than 250ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200ns as shown below. In the second case, the device will not turn to a "Busy" state when the $\overline{CE}$ delay time is less than 30ns.



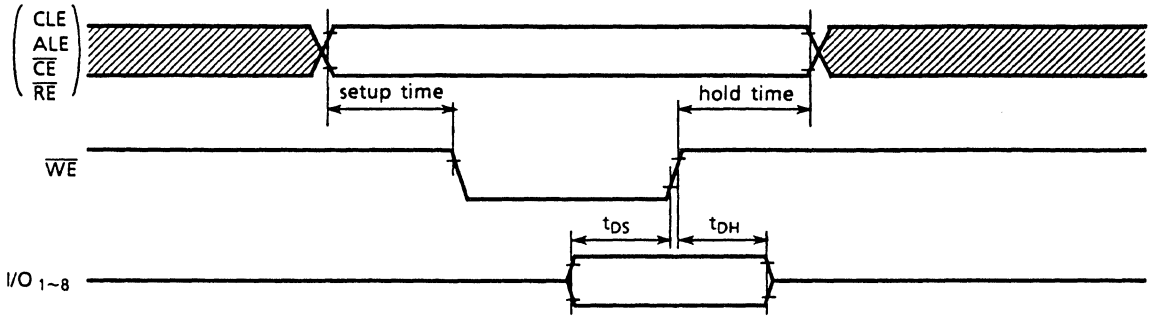
Programming and Erasing Characteristics (Ta = 0 ~ 55°C, V_{CC} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
t_{PROG}	Average Programming Time		300 ~ 1000	5000	μs	
N	Divided Number on Same Page			10		(1)
t_{BERASE}	Block Erasing Time	6	6	100	ms	
t_{SR}	Suspend Input to Ready			1.5	ms	
$N_{W/E}$	Number of Write/Erase Cycles	2.5×10^5			cycles	

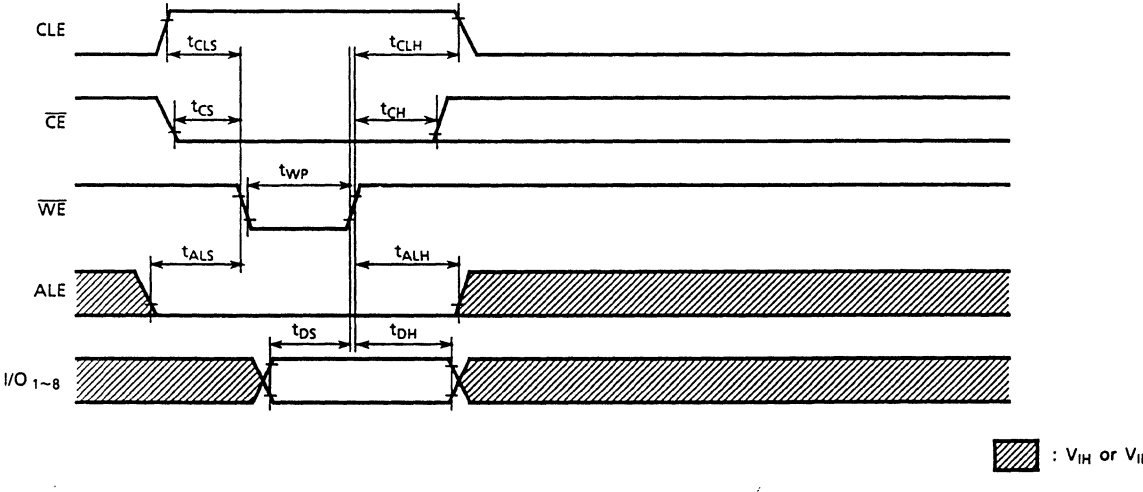
(1) Refer to notification (15) toward the end of this document.

Timing Charts

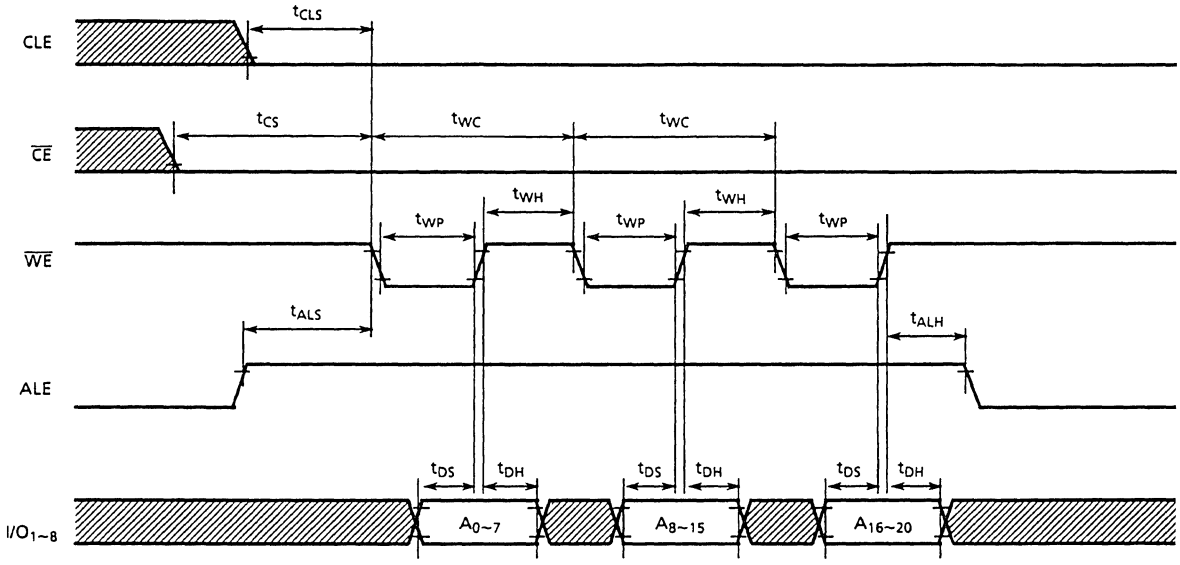
Latch Timing Chart for Command/Address/Data



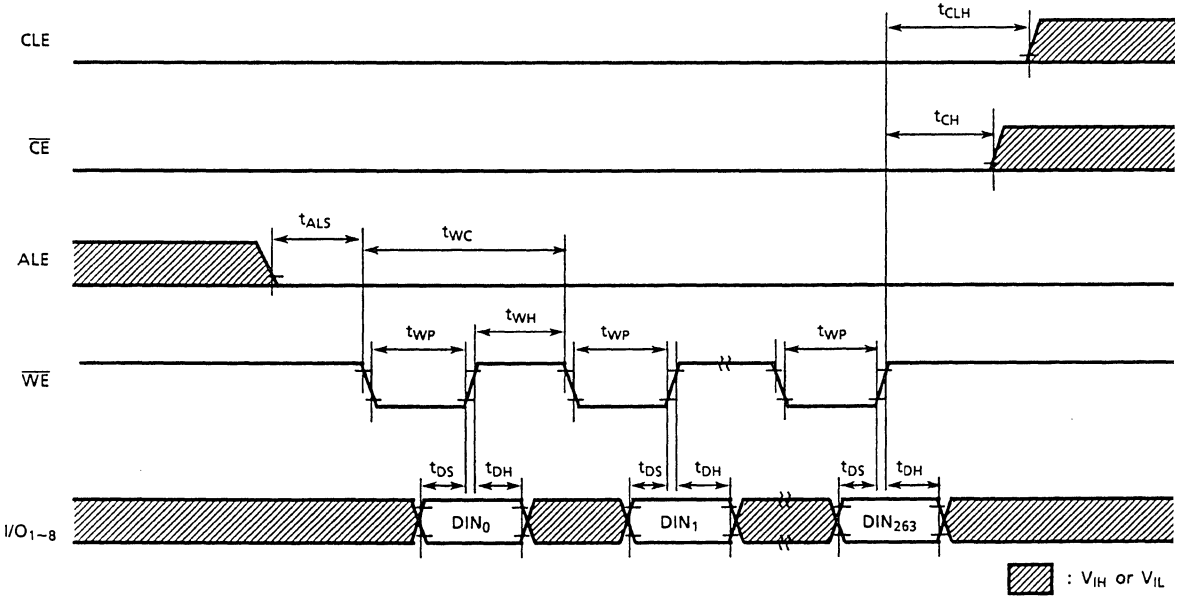
Command Input Cycle



Address Input Cycle

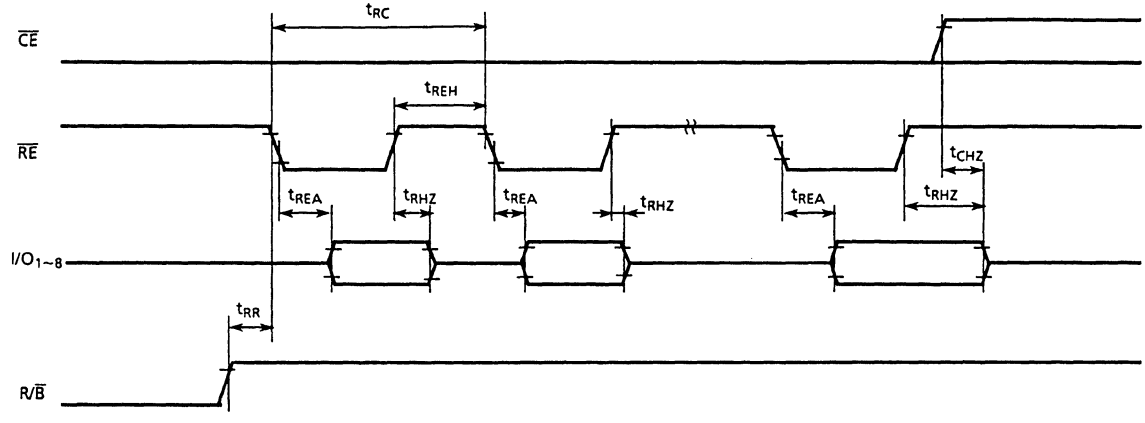


Data Input Cycle

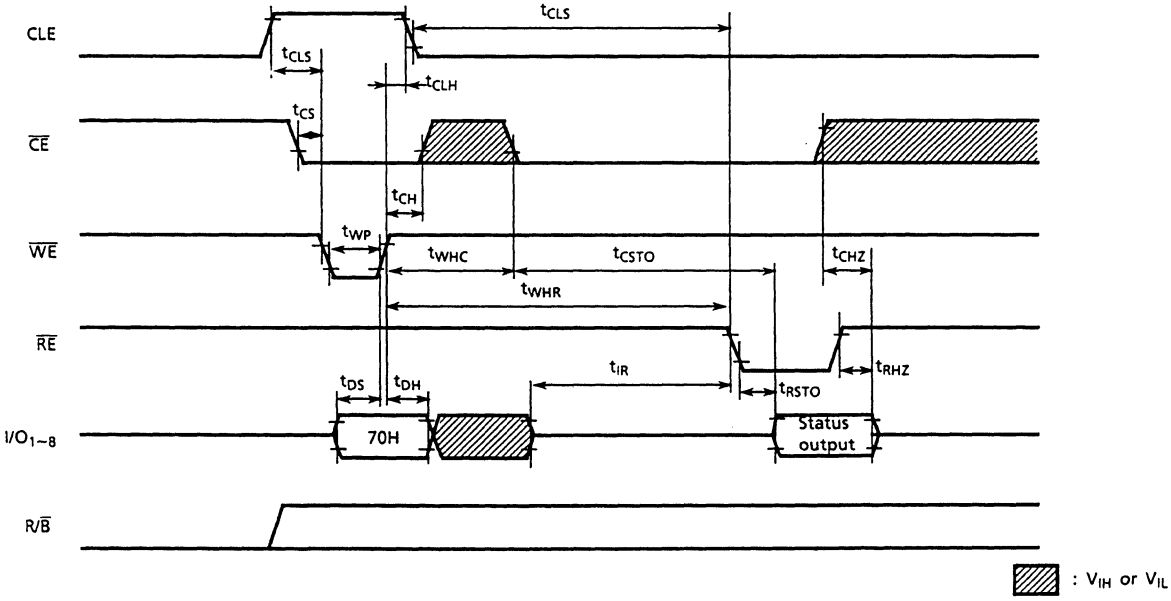


D. Non-Volatile

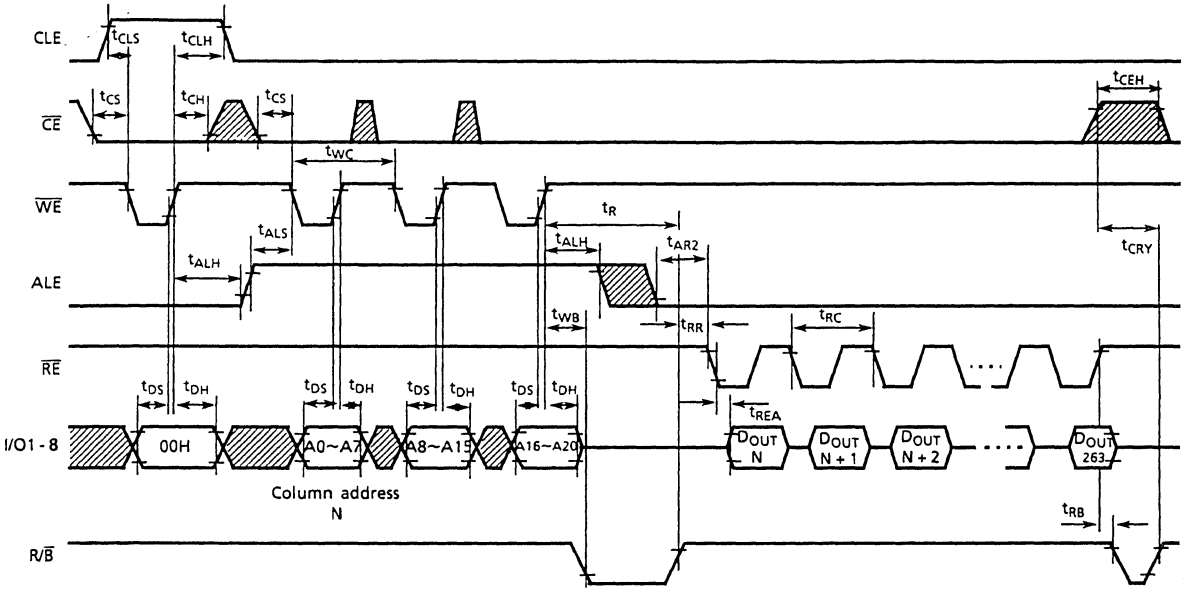
Serial Read Cycle



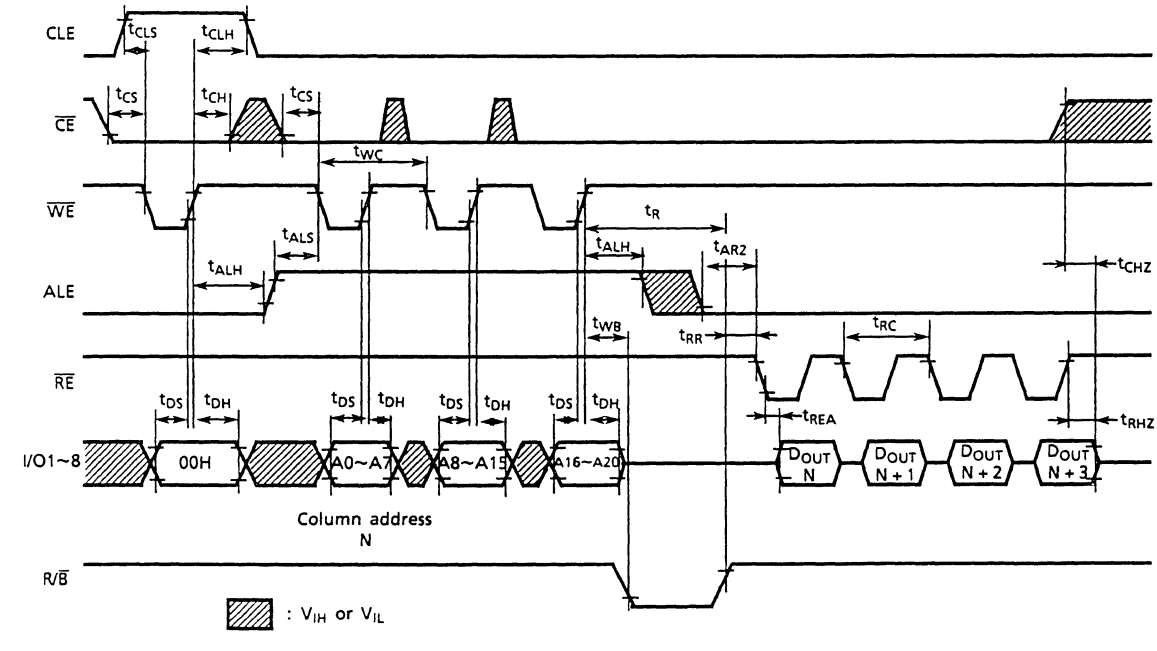
Status Read Cycle



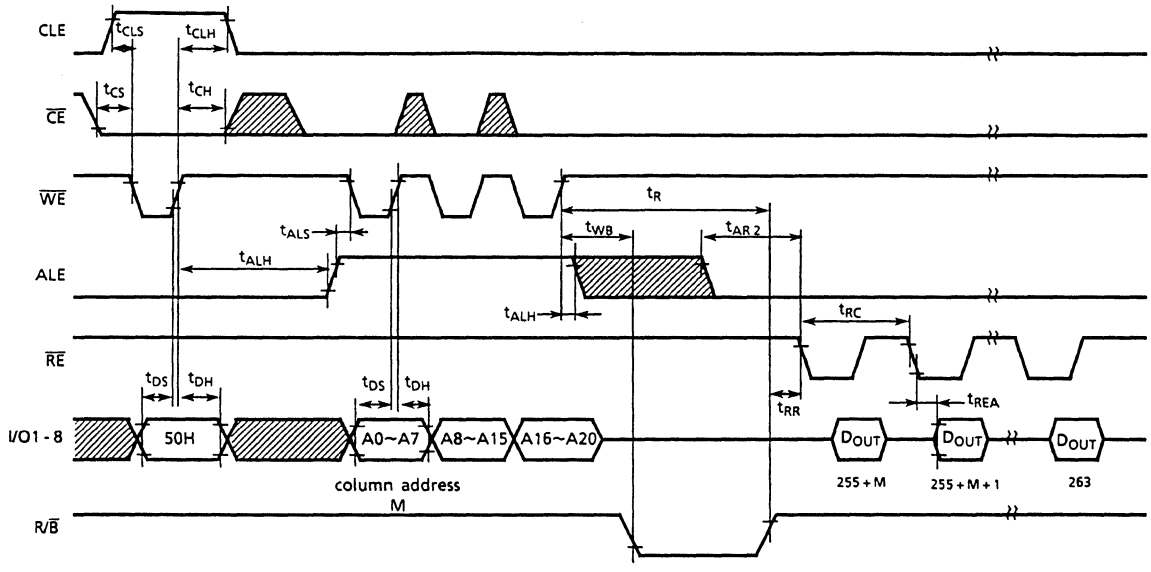
Read Cycle (1)



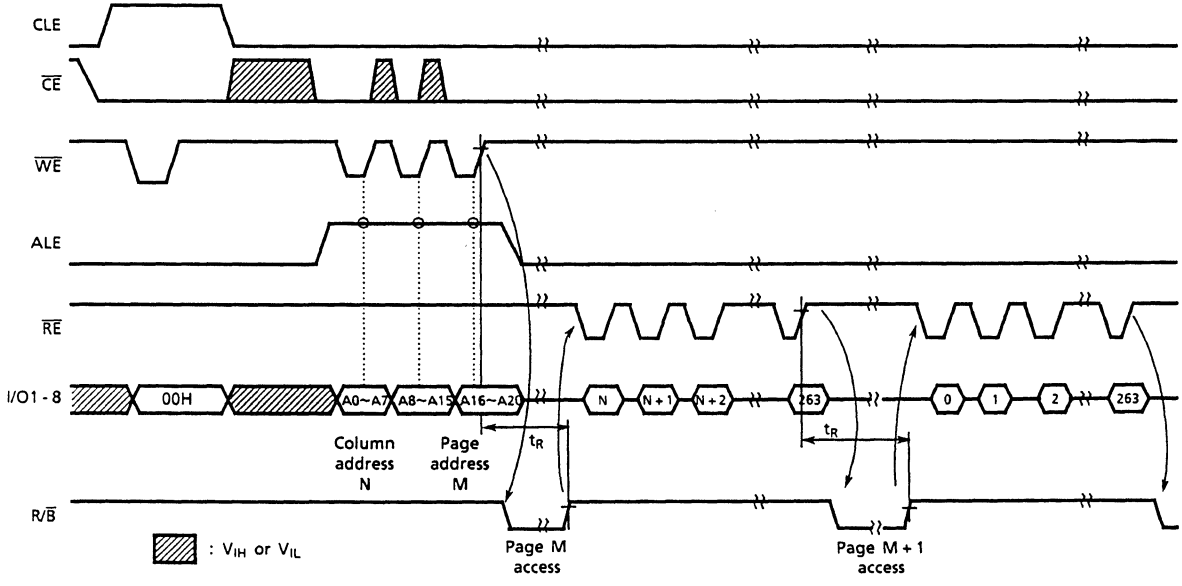
Read Cycle (1): Interception by $\overline{CE}$



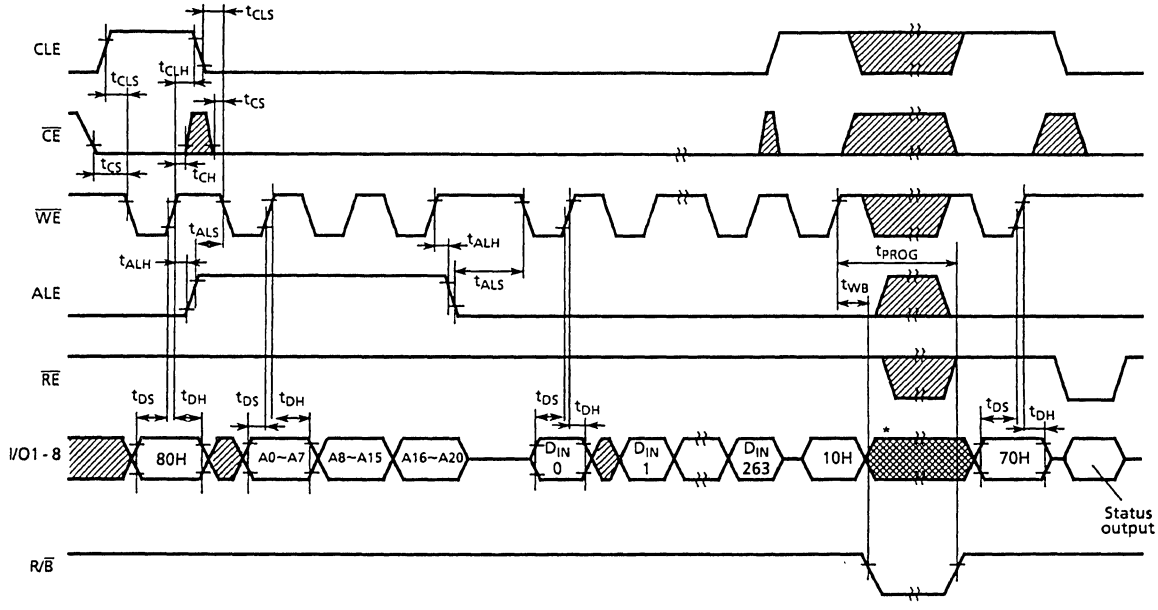
Read Cycle (2)



Sequential Read Timing



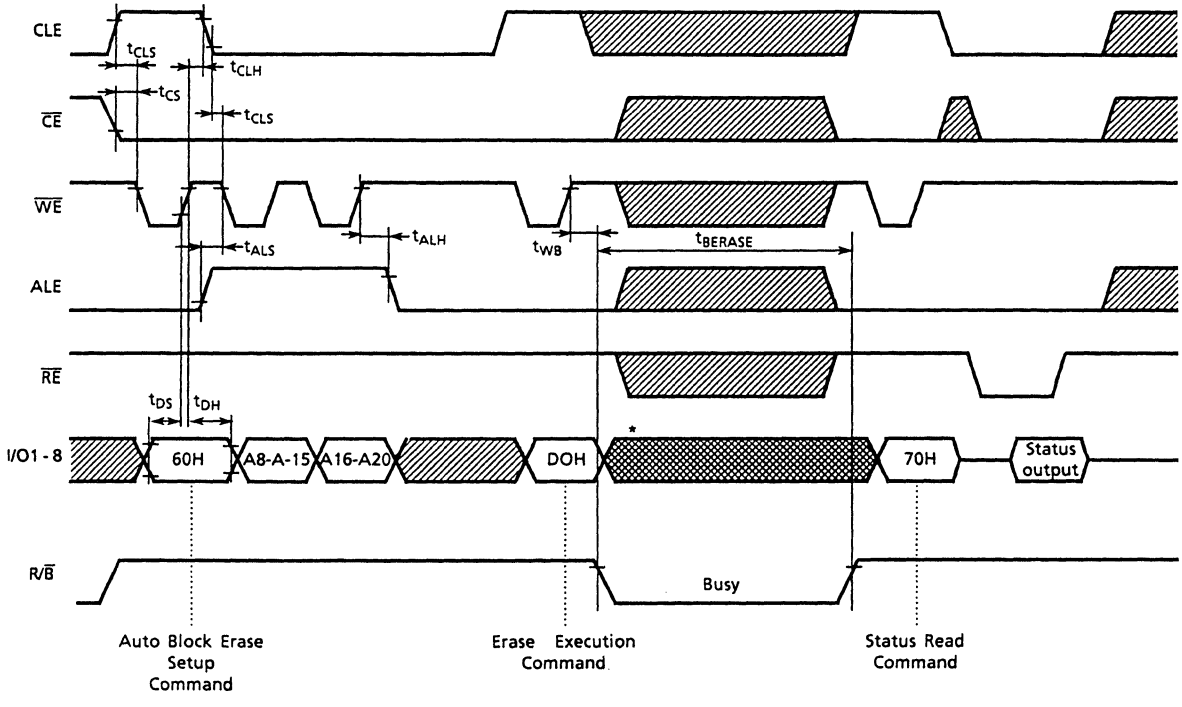
Auto Program Operation Timing Chart



: V_{IH} or V_{IL}

* : Do not collide data input with data output

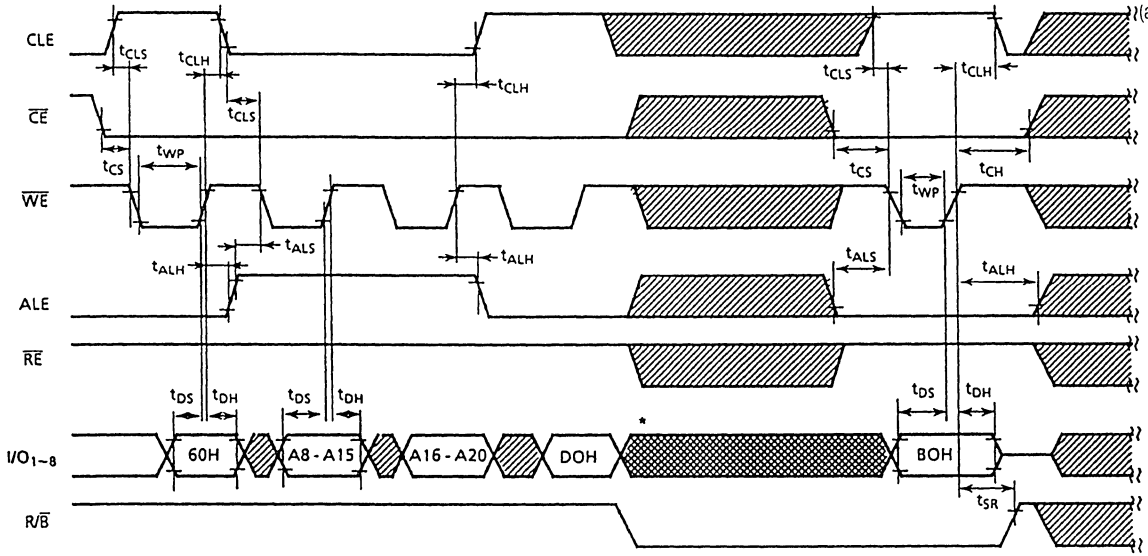
Auto Block Erase Timing

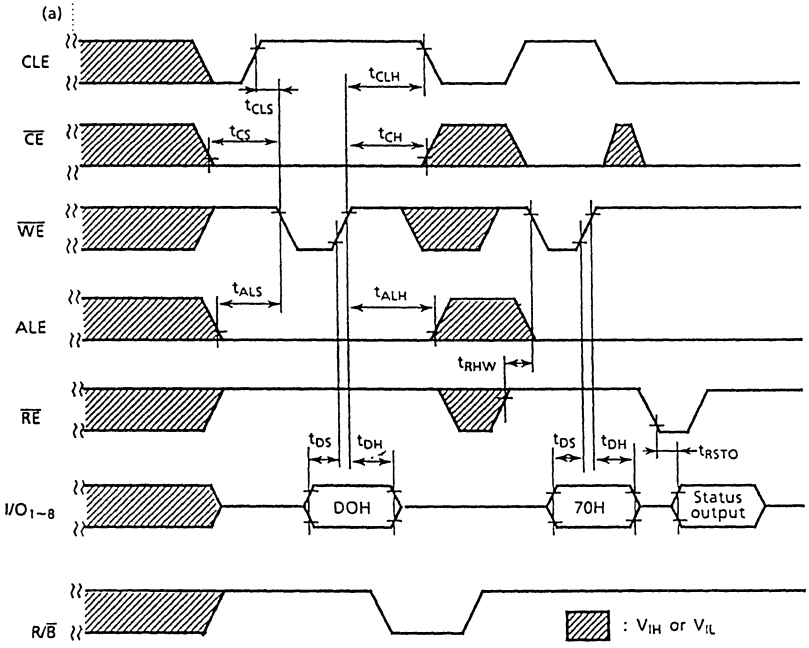


: V_{IH} or V_{IL}

* : Do not collide data input with data output

Suspend/Resume on Block Erase Operation



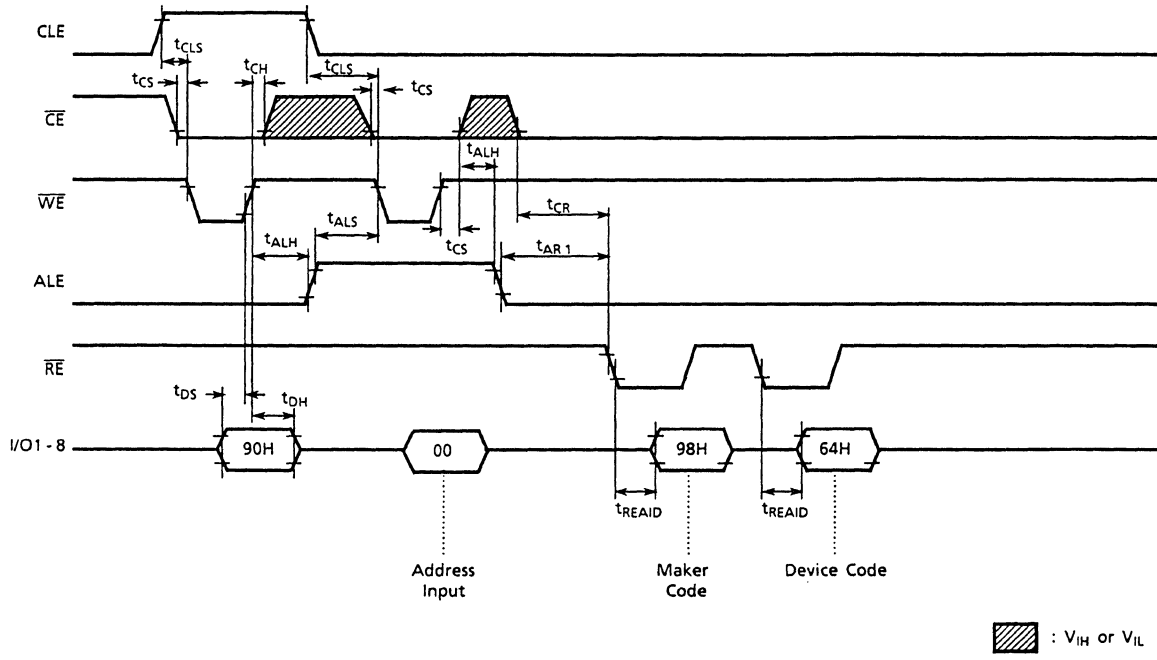


: V_{IH} or V_{IL}

(a) : Continued

* : Do not collide data input with data output

ID Read Operation



Pin Function

The TC5816 is a serial access memory in which address and data information is multiplexed. The device pinout is shown in Figure 1.

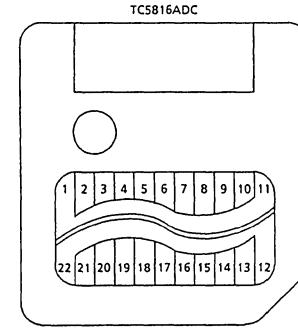


Figure 1. TC5816 Pinout

Command Latch Enable: CLE (Fig. 1, Pin 2)

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE (Fig. 1, Pin 3)

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$ (Fig. 1, Pin 21)

The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the busy state ($R/\overline{B}$ = L) such as during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input. The $\overline{CE}$ signal must stay low during the read mode busy state.

Write Enable: $\overline{WE}$ (Fig. 1, Pin 4)

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$ (Fig. 1, Pin 20)

The $\overline{RE}$ signal controls the serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O1 ~ 8 (Fig. 1, Pin 6 ~ 9, 13 ~ 16)

The I/O 1 ~ 8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect: $\overline{WP}$ (Fig. 1, Pin 5)

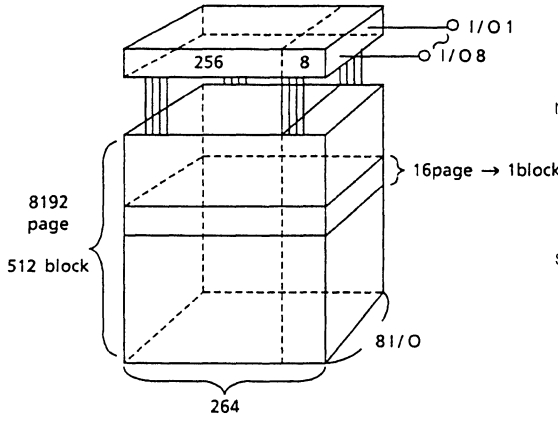
The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: $R/\overline{B}$ (Fig. 1, Pin 19)

The $R/\overline{B}$ output signal is used to indicate the state of the device. The $R/\overline{B}$ signal indicates a busy state ($R/\overline{B}$ = L) during program, erase, or read operations and will return to a ready state ($R/\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

Schematic Cell Layout and Address Assignment

The program operation is implemented in a page unit while the erase operation is carried out in block units.



A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 Page = 264 bytes;
1 Block = 264 bytes x 16 pages = (4K + 128) bytes
Total device density = 264 bytes x 16 pages x 512 blocks
= 16.5M bits (2.0625M bytes)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Figure 3.

Figure 2. TC5816 Schematic Cell Layout

	I/01	I/02	I/03	I/04	I/05	I/06	I/07	I/08
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third cycle	A16	A17	A18	A19	A20	*L	*L	*L

A0 ~ A7 : column address
A8 ~ A20 : page address
(A12 ~ A20: block address
A8 ~ A11 : NAND address in block)

* I/O 6 ~ 8 during the third cycle must be set to low level

Figure 3. Addressing

Operation Mode: Logic and Command Tables

The operation modes such as program, erase, read, erase suspend, and reset are controlled by the ten different command operations shown in Table 2. The address, command input, and data input /output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, and $\overline{WP}$ signals as shown in Table 1.

Table 1. Logic Table

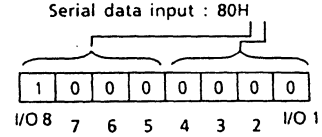
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command input	H	L	L	⌐‾↗	H	*
Data input	L	L	L	⌐‾↗	H	*
Address input	L	H	L	⌐‾↗	H	*
Serial data output	L	L	L	H	↘_⌐	*
During programming (Busy)	*	*	*	*	*	H
During erasing (Busy)	*	*	*	*	*	H
Program, Erase inhibit	*	*	*	*	*	L

H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Table 2. Command Table (HEX data)

	FIRST CYCLE	SECOND CYCLE	ACCEPTABLE COMMAND DURING BUSY
Serial data input	80	–	
Read mode (1)	00	–	
Read mode (2)	50	–	
Reset	FF	–	√
Auto program	10	–	
Auto block erase	60	D0	
Suspend in erasing	B0	–	√
Resume	D0	–	
Status read	70	–	√
ID read	90	–	

Bit assignment of HEX data (Example)



Once the device is set into the read mode by the "00H" or "50H" command, additional read commands are not needed for sequential page read operations. Table 3 shows the operation mode for reads.

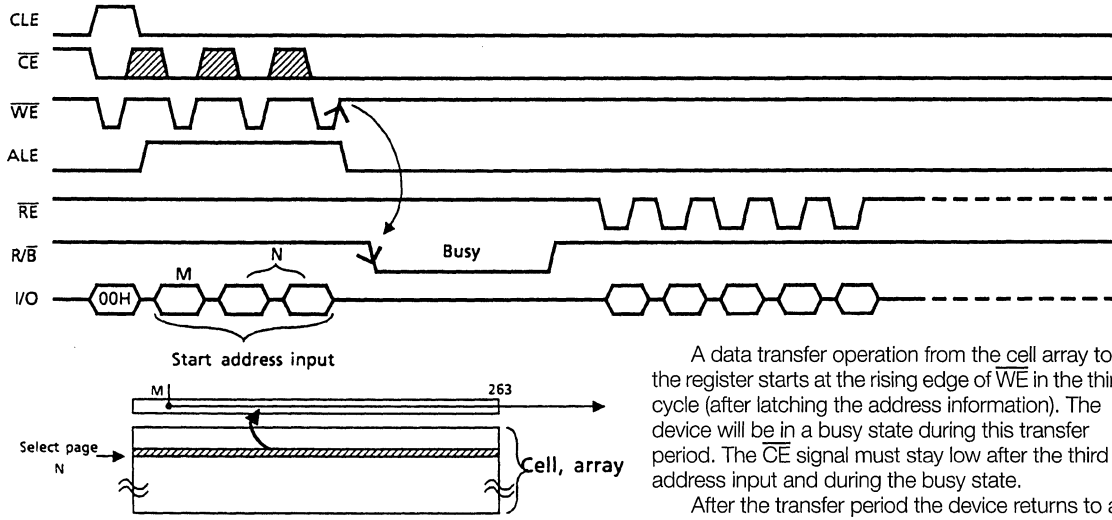
Table 3. Operation mode for reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 ~ I/O8	POWER
Read mode	L	L	L	H	L	Data output	Active
Output deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

Device Operation

Read Mode (1)

Read mode (1) is set by issuing a "00H" command to the command register. Refer to Figure 4 below for timing details and block diagram.



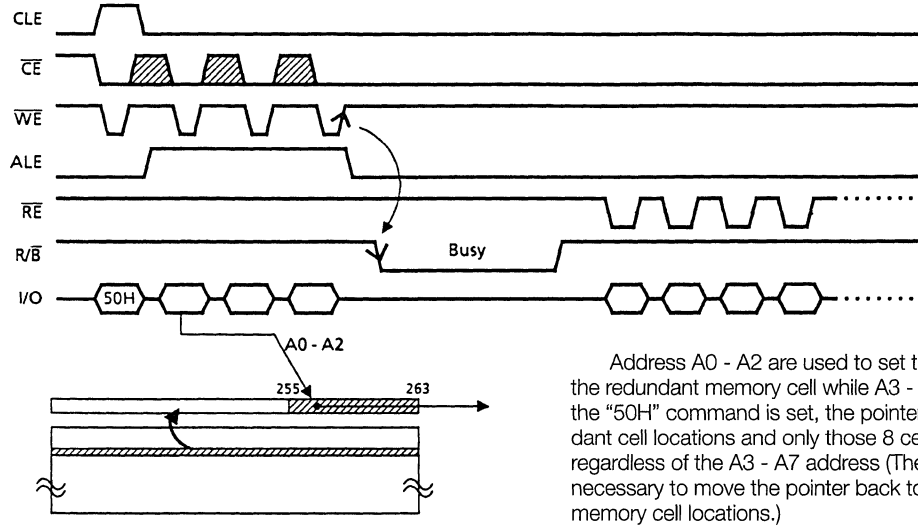
A data transfer operation from the cell array to the register starts at the rising edge of $\overline{WE}$ in the third cycle (after latching the address information). The device will be in a busy state during this transfer period. The $\overline{CE}$ signal must stay low after the third address input and during the busy state.

After the transfer period the device returns to a ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the designated starting pointer indicated during the address input cycle.

Figure 4. Read mode (1) operation

Read Mode (2)

Read mode (2) has the same timing as read mode (1) but it is used to access information in the extra 8 byte redundancy area of the page. The starting pointer is therefore assigned between byte 256 and 263.



Address A0 - A2 are used to set the starting pointer for the redundant memory cell while A3 - A7 are ignored. Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed regardless of the A3 - A7 address (The "00H" command is necessary to move the pointer back to the 0 - 255, main memory cell locations.)

Figure 5. Read mode (2) operation

Sequential Read (1)(2)

This mode allows sequential reads without additional address input.

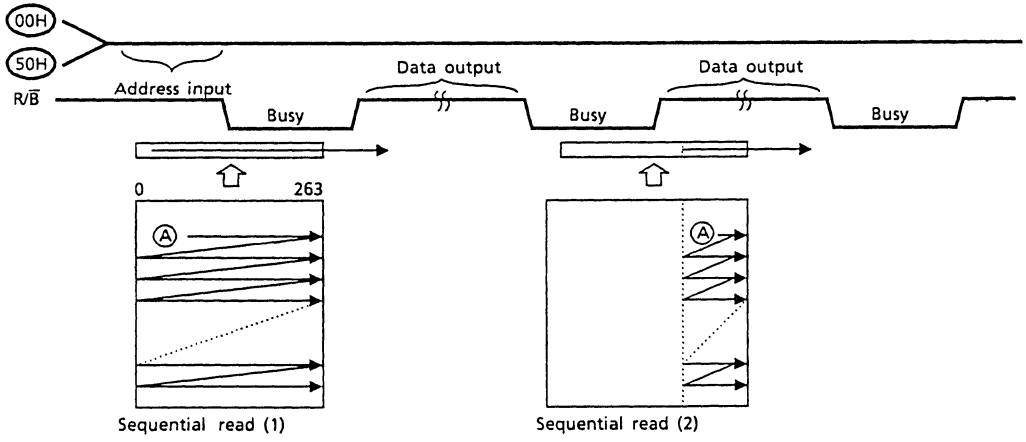


Figure 6. Sequential read

Sequential read mode (1) outputs data from addresses 0 to 263 while sequential read mode (2) outputs data from the 8-byte redundant area only. When the pointer reaches the last address, the device continues to output data from the last address with each $\overline{RE}$ clock signal.

Status Read

The TC5816 automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the ready/busy status of the device, determines the pass /fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 4.

Table 4. Status output table

	STATUS	OUTPUT	
I/O 1	Pass/Fail	Pass: "0"	Fail: "1"
I/O 2	Not used	"0"	
I/O 3	Not used	"0"	
I/O 4	Not used	"0"	
I/O 5	Not used	"0"	
I/O 6	Suspend	Suspended: "1"	Not Suspended: "0"
I/O 7	Ready/Busy	Ready: "1"	Busy: "0"
I/O 8	Write protect	Protect: "0"	Not Protect: "1"

The Pass/Fail status on I/O 1 is only valid when the device is in the ready state. The device will always indicate a pass status while in the busy state.

An application example with multiple devices is shown in Figure 7.

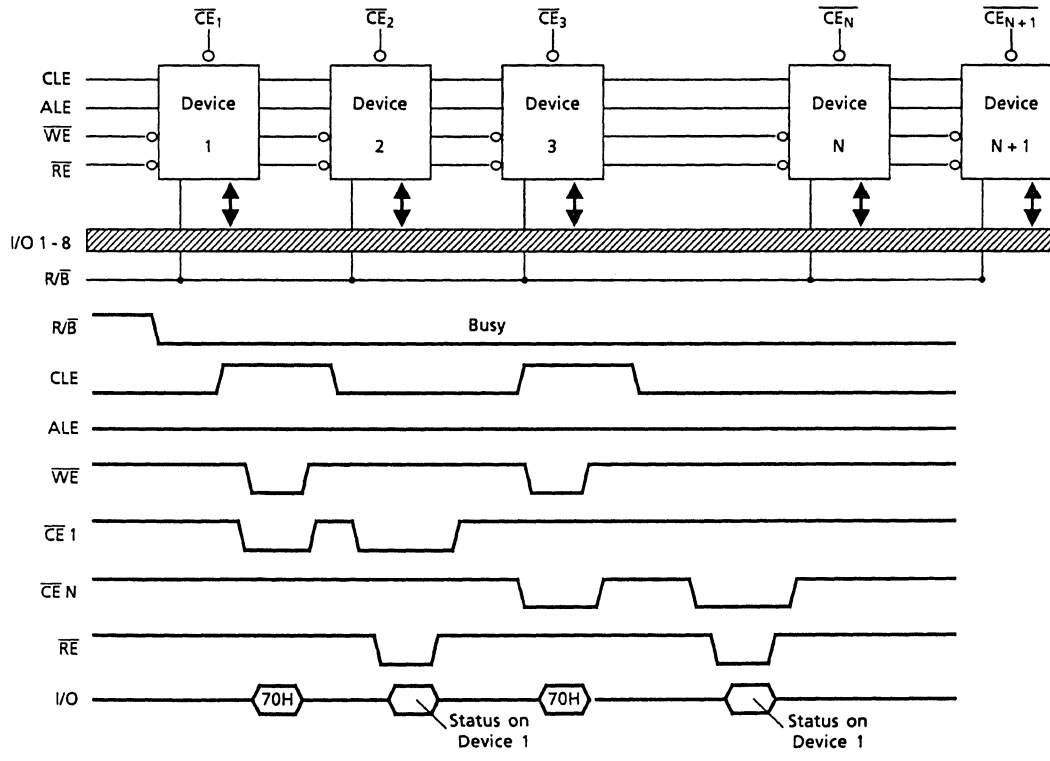
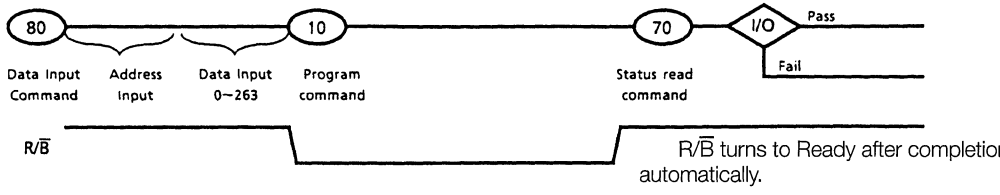


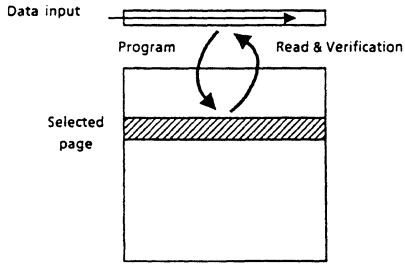
Figure 7. Status read timing application example

SYSTEM DESIGN NOTE: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status read function can be used to determine the status of each individually selected device.

Auto Page Program

The TC5816 implements the automatic page program operation after receiving a "10H" program command after the address and data have been input. The sequence of command, address, and data input is shown below. (Refer to the detail timing chart.)





The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the "10H" command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

Figure 8. Auto Page Program

Auto Block Erase

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command "D0H" (which follows the erase setup command "60H"). This two cycle process for erase operations acts as an extra layer of protection from accidental erasure of data due to possible external noise. The device automatically executes the erase and verify operations.

Auto Block Erase

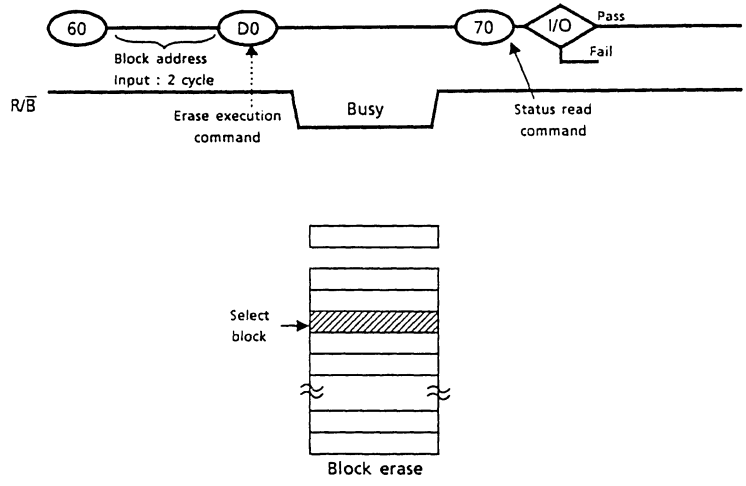


Figure 9. Auto Block Erase Operation

Suspend/Resume

Because a block erase operation can keep the device in a busy state for an extended period of time, the TC5816 has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence for this operation are shown below. (Refer to the detail timing chart)

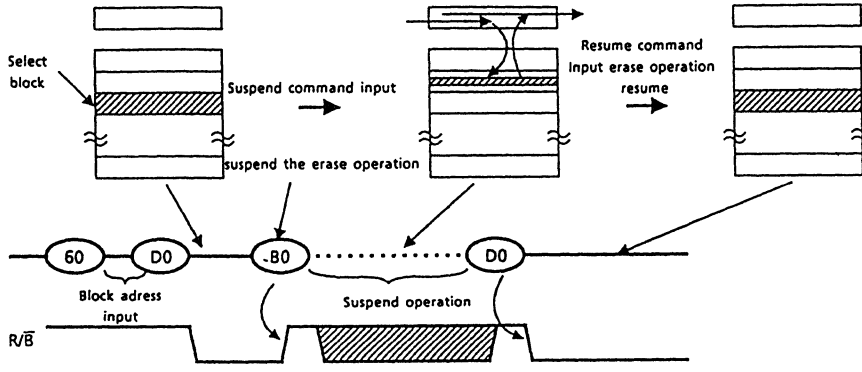


Figure 10. Suspend /Resume Operation

The (80)····(D0) suspend/resume cycle can be repeated up to 20 times during a block erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

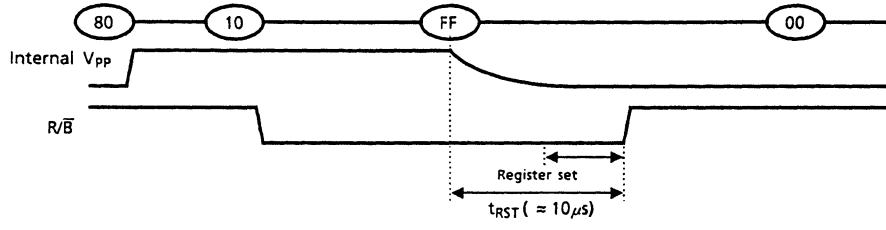
Reset

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go into a wait state. The address and data register are set after a reset as follows:

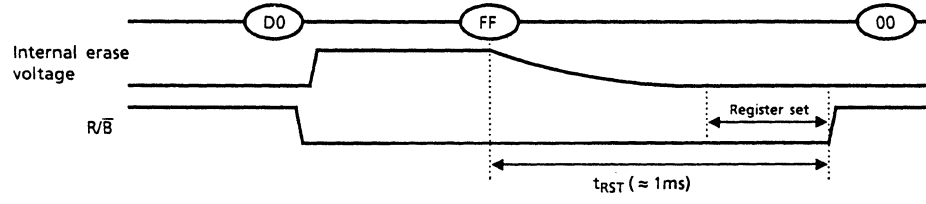
- Address Register : All "0"
- Data Register : All "1"
- Operation Mode : Wait State

The response after a "FFH" reset command input is as follows:

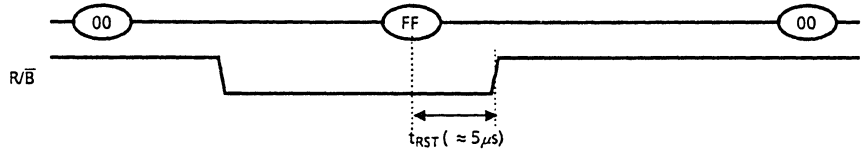
- If the reset (FFH) command is input during programming: Figure 11



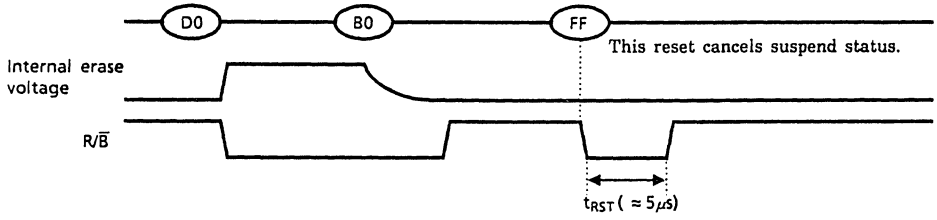
- If the reset (FFH) command is input during erasing: Figure 12



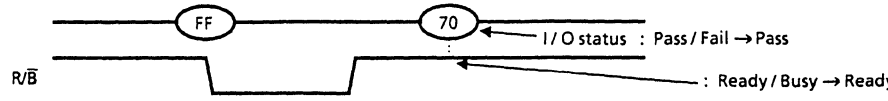
- If the reset (FFH) command is input during the read operation: Figure 13



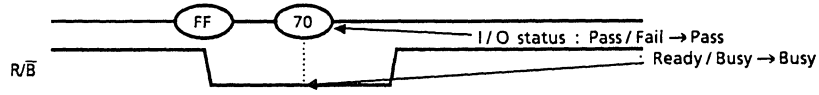
- If the reset (FFH) command is input after suspend: Figure 14



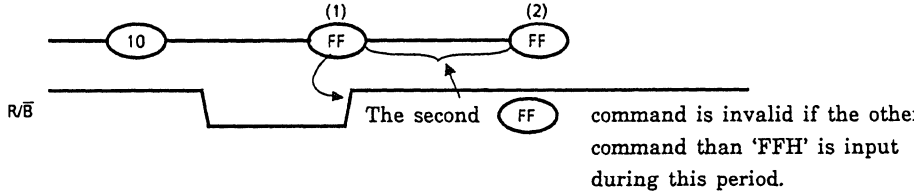
- If the status read command (70H) is input after reset: Figure 15



However, the following operation is prohibited. If the following operation is executed, set up for the address and data register cannot be guaranteed.



- If the reset command is input in succession: Figure 16



ID Read

The TC5816 contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

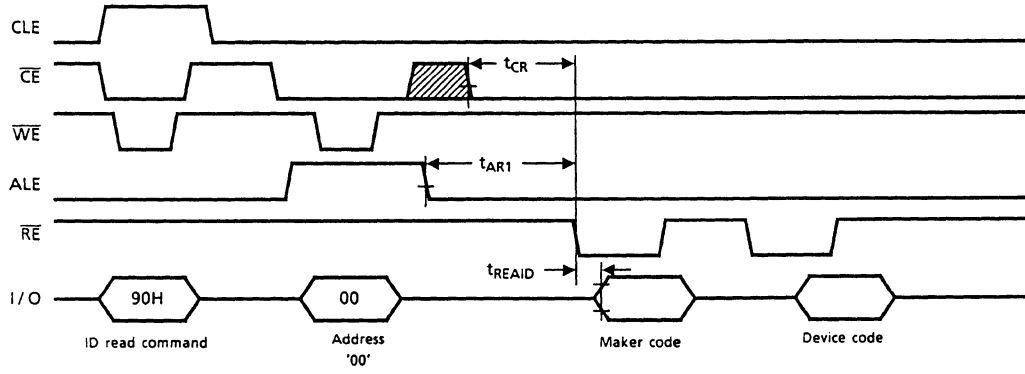


Figure 17. ID read timing

Table 5. Code table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	HEX data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	0	0	1	0	0	64H

Refer to AC characteristics for t_{READID}, t_{CR}, t_{AR1} (Refer to the specification).

Device Physics

Program Operation

Figure 18 shows the NAND memory cell and details of the programming mechanism. The program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example showing the operations necessary to program '0' data in TR1 and "1" data in TR2 follows:

(1) The select lines are activated so that the transistor array is connected to the bit line and disconnected from the ground line.
(2) V_{PP} (~20V) is applied to the selected word line and an inhibit voltage of VPI (≈10V) is applied to the unselected word lines.
(3) The bit line tied to cell transistor TR1 is biased to 0V and the bit line tied to TR2 is biased to the inhibit voltage of VDPI (≈10V).
(4) V_{PP} is applied between the control gate and the channel in TR1, as shown in Figure 18, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.
(5) The injected electrons are captured in the floating gate (which is surrounded by an oxide layer) and will remain, even after power is cut off, until they are removed by an erase operation.
(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10V because the voltage of the channel is 10V. Therefore, tunneling does not take place. (i.e. electrons are not injected into the floating gate.)
(7) Tunneling does not take place in the unselected pages because of the 10V (VPI) being applied to the unselected word lines which again makes the voltage difference between control gate and channel only 10 volts. Thus, the floating gate of the "0" cell is charged to "minus" and that of the "1" cell is charged to "plus".

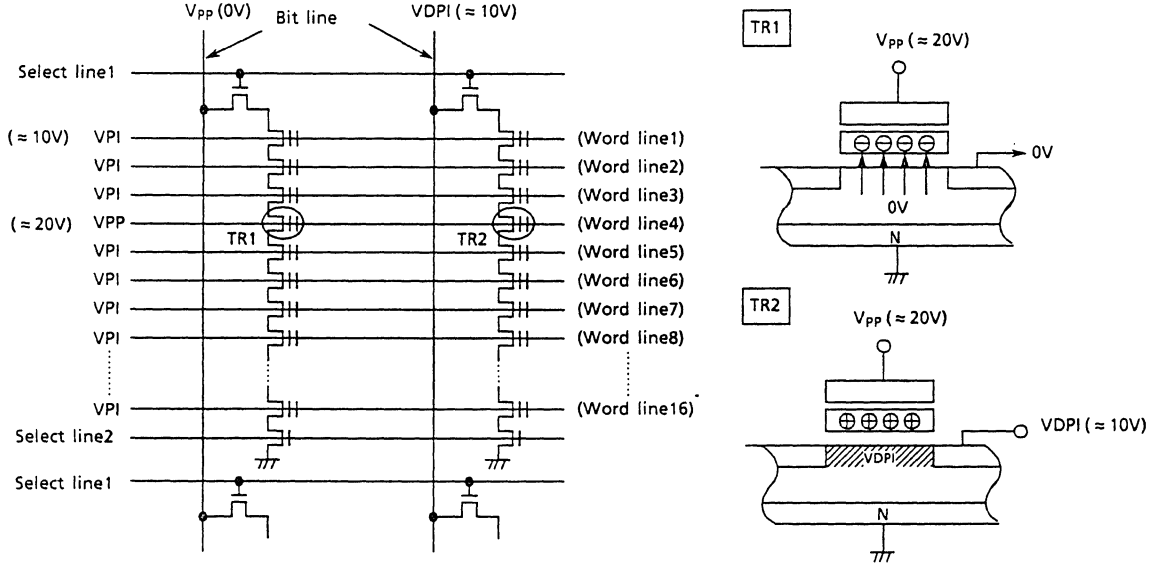


Figure 18. TC5816 Program Device Physics

Erase Operation

Figure 19 shows the NAND memory cell and details of the erase mechanism. The erase operation is used to turn the "0" (programmed) cells back to "1" in a block. Zero volts is applied to the control gate and V_{PP} (~20V) is applied to the substrate so that a 20 volt potential is created and the electrons in the floating gate are pulled out through tunneling.

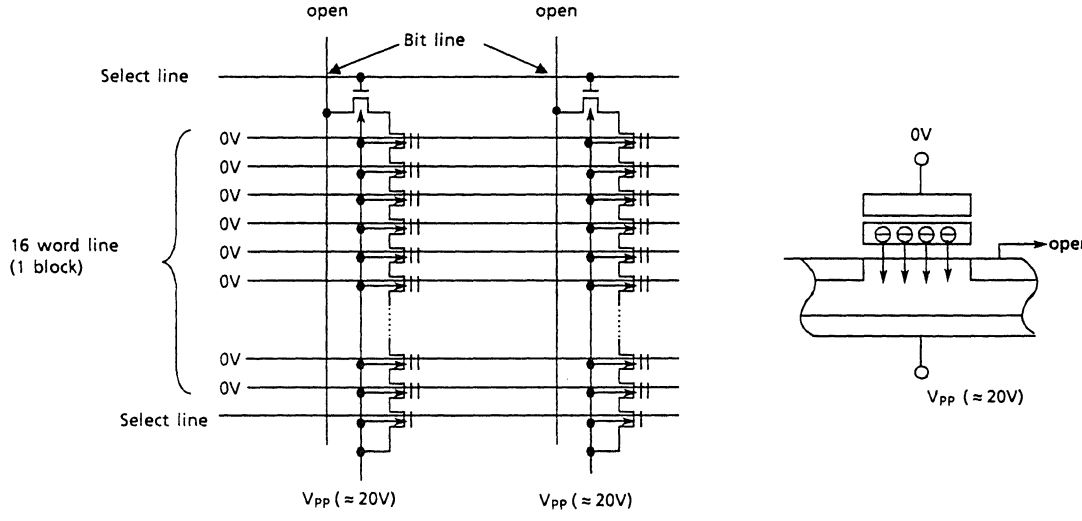


Figure 19. TC5816 Erase Device Physics

Read Operation

The state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate) after programming. Each state is indicated as the "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 20. The threshold voltage of a transistor with "0" data falls within the "plus" distribution while the threshold voltage of a transistor with "1" data falls within the "minus" distribution. The distribution band depends on transistor fluctuations.

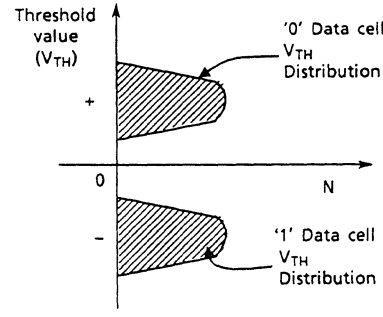


Figure 20. V_{TH} Distribution for "0" and "1" data cell

Figure 21 shows the memory cell and details of the read operation:

(1) Select lines 1 and 2 in the block including the selected page are biased at a high level so that the 16 NAND memory cell array is connected to the bit line and ground.

(2) Zero volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 21, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground while the precharged bit line tied to TR1 remains at a high level because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

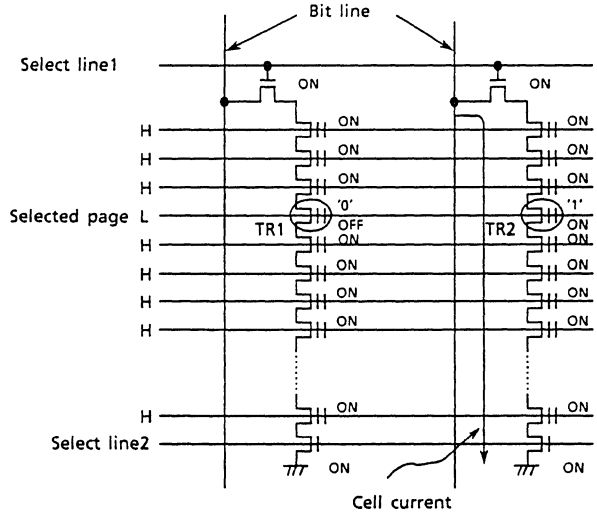


Figure 21. TC5816 Read Device Physics

Application Notes and Comments

(1) Prohibition of unspecified commands

The operation commands are listed in Table 1. Data input as a command other than the specified commands in Table 1 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer control for "00H", "50H"

The TC5816AFT has two read modes which set the destination of the pointer to either the main memory area of a page or the redundancy area. The pointer can point to any location from 0 to 255 in read mode (1) and from 256 to 263 in read mode (2). Figure 22 shows the block diagram of their operations.

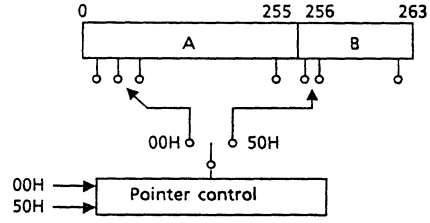


Figure 22. Pointer control

The pointer is set to region "A" by the "00H" command and to region "B" by the "50H" command.

(Example)
The "00H" command needs to be input to set the pointer back to region "A" when the pointer control points to region "B".

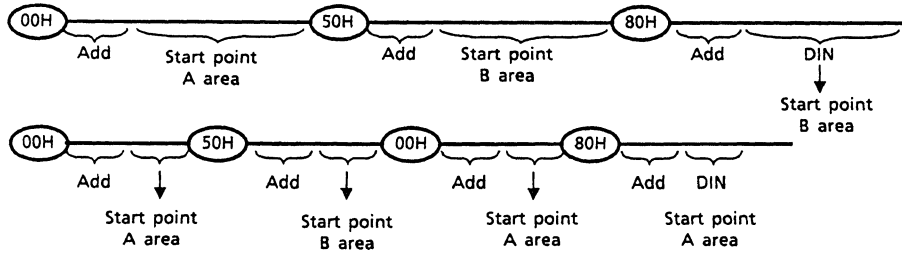
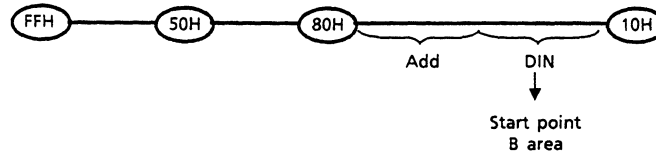


Figure 23. Example for Pointer Set

For programming into region B only, first reset the contents of the data register to "1"s by inputting the FFH (reset) command.



(3) Acceptable commands after the serial input command "80H"

Once the serial input command ("80H") is input, do not input any command other than the program execution command ("10H") or the reset command ("FFH") during programming.

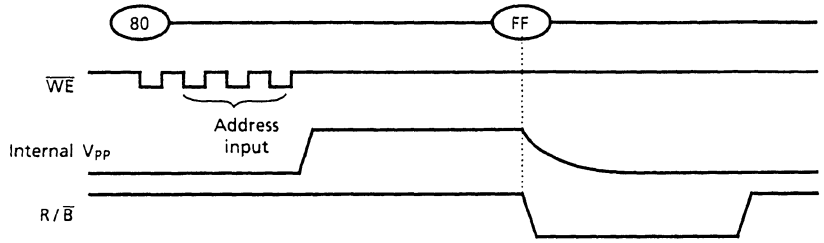
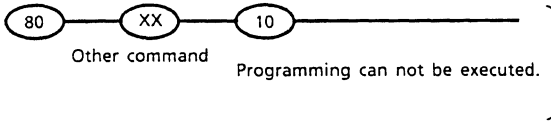


Figure 24

If a command other than "10H" or "FFH" is input, the program operation is not performed.



In this case, the reset command (FFH) command is needed.

(4) Status read during read operation

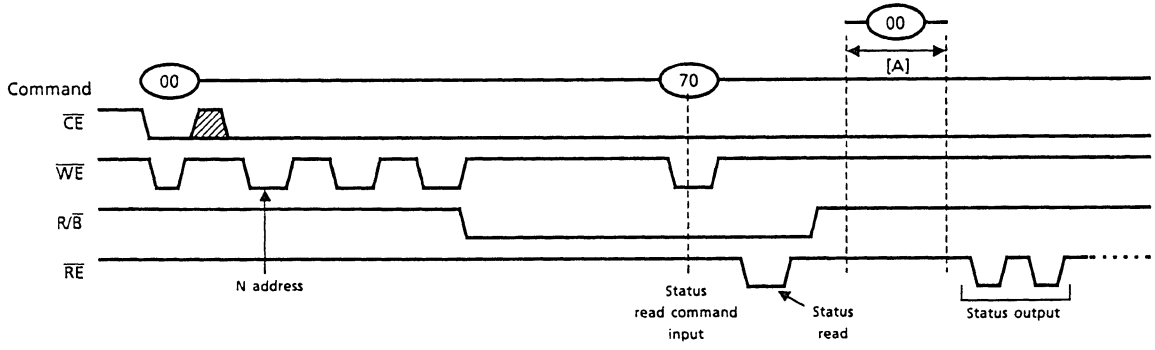


Figure 25

The device status can be read out by inputting the status read command "70H" during the read mode. Once the device is set to the status read mode after a "70H" command input, the device does not return to the read mode.

Therefore, status read during the read operation is prohibited.

However, when the read command "00H" is input during [A], the status mode is reset, and the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) Suspend command "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.

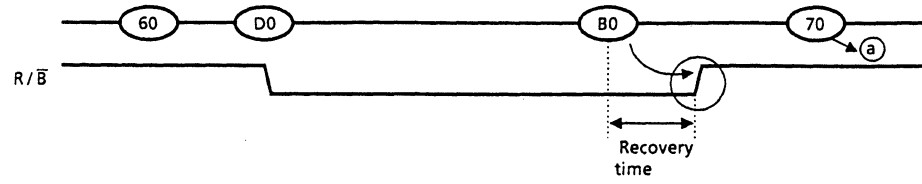


Figure 26

Although the device status changes from busy to ready after "B0H" is input, the following two cases cannot be distinguished.

-After a "B0H" command input, Busy→Ready

-After an erase operation is finished with "D0H", Busy→Ready

Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to ready.

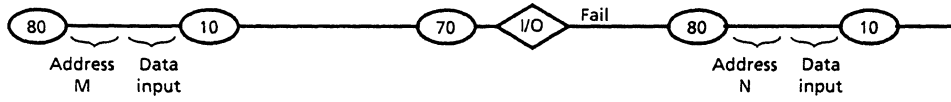
The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

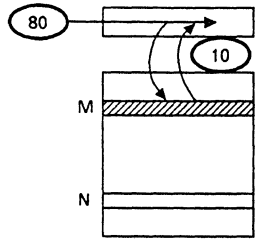
-"B0H" has been accepted: Erase operation is executed. (The device is busy.)

-"B0H" has not been accepted. (Erase operation has been completed): "D0H" command cannot be accepted. (The device is ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) Program fail





When the programming result for the page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

Figure 27

(7) Data transfer

The data in page address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e. "1" data will become "0" and "0" will become "1").

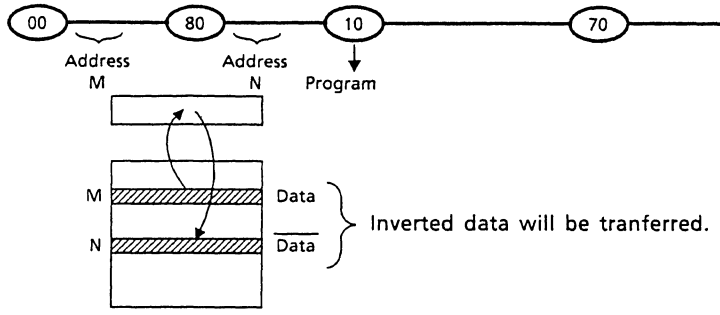
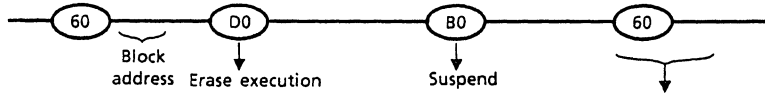


Figure 28

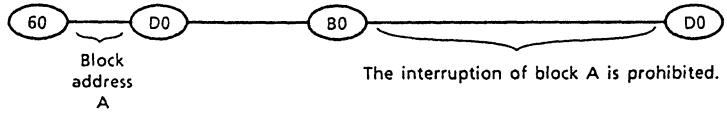
(8) Block erase after suspend command "B0H"



A block erase command is prohibited when the device has been suspended by inputting "B0H" during a block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

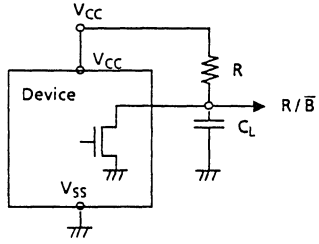
(9) Interruption of an erasing block

After a "B0H" command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



(10) R/$\overline{B}$: Termination for the Ready/Busy pin (R/$\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.



This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.

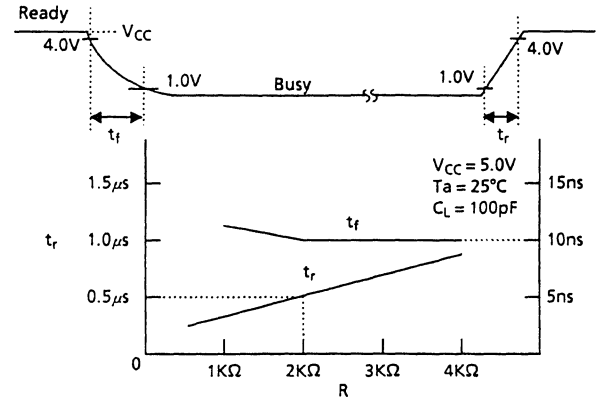


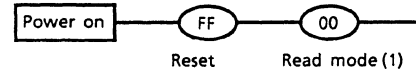
Figure 29

(11) Status After Power On

Although the device is set to read mode after power-up, the following sequence is needed because each input signal may not be stable at power on.

- Operation mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminate
- High voltage generation circuit : Off state

Power on sequence



(12) Power On/Off Sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:

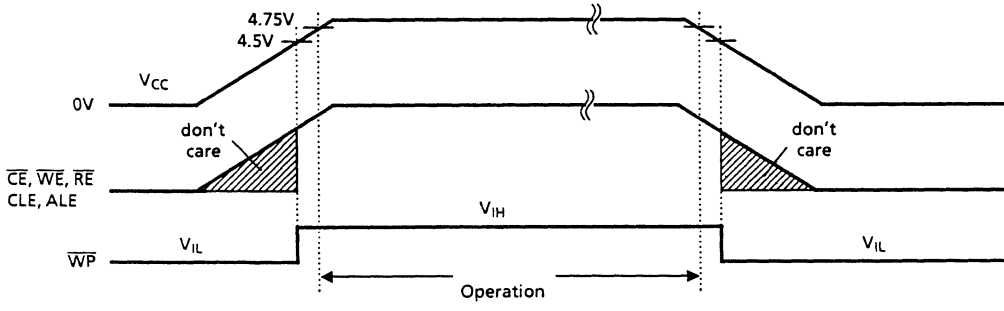


Figure 30. TC5816 Power On/Off Sequence

(13) Setup for $\overline{WP}$ Signal

The erase and program operations are compulsively reset when $\overline{WP}$ goes low. The $\overline{WP}$ signal must be kept at a high level before the 80H/60H command input for the program and erase operations.

If $\overline{WP}$ goes high after the 80H/60H command input for a program/erase operation, the program and erase operations cannot be guaranteed.

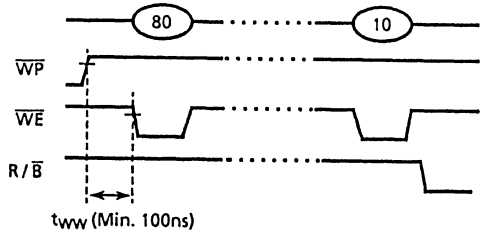


Figure 31. $\overline{WP}$ Setup before Programming

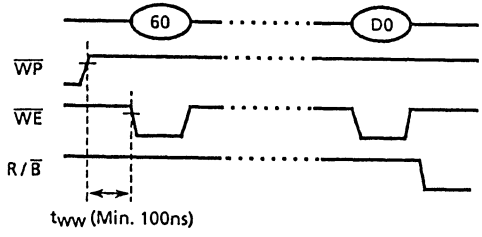


Figure 32. $\overline{WP}$ Setup before Erasing

(14) In the case that 4 address cycles are input

Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation:

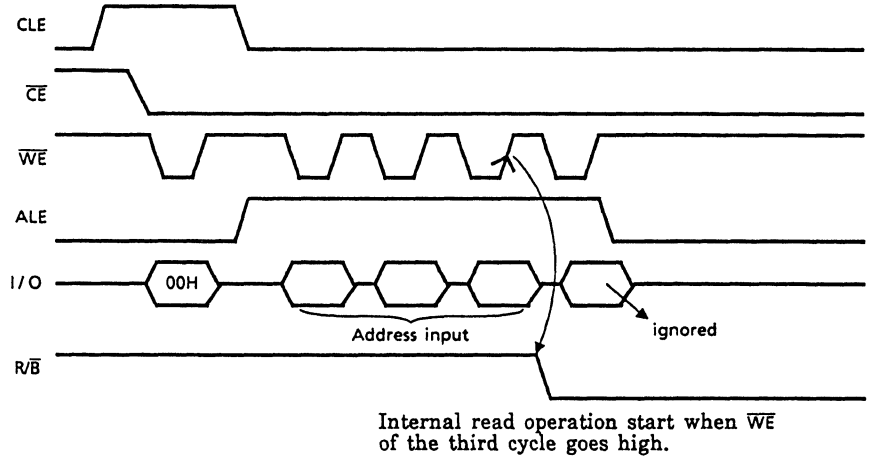


Figure 33

Program operation:

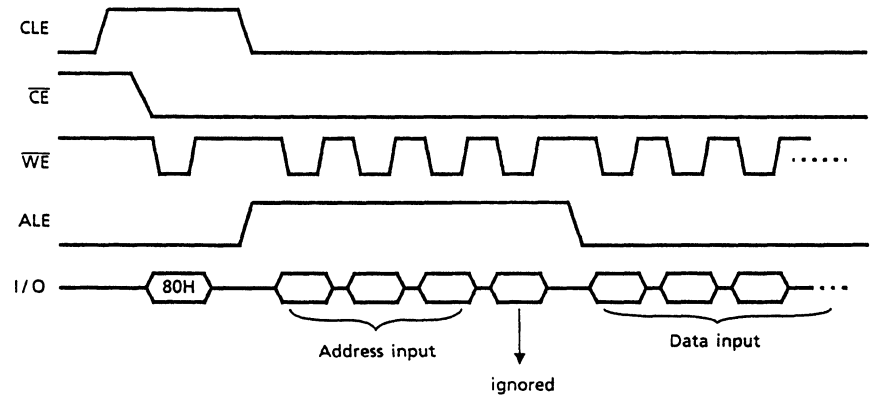


Figure 34

(15) Divided program in the same page (Partial page program)

The device allows a page to be divided into 10 segments (typically) with each page segment programmed individually as follows:

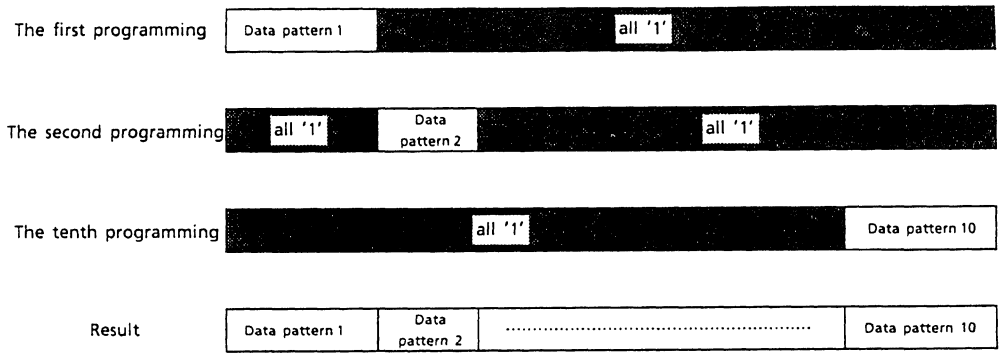


Figure 35

Note: The input data for unprogrammed or previously programmed page segments must be "1" (i.e. Mask all page bytes outside the segment to be programmed with "1" data.).

(16) $\overline{RE}$ Signal During Read

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in the read mode. Therefore, once the device is set into the read mode by the "00H" or "50H" command, the internal column address counter can be incremented by the $\overline{RE}$ clock before or after the address input. Assuming that $\overline{RE}$ clocks before the address input and the pointer reaches the last column address, an internal read operation (array→register) will occur and the device will be in a busy state. (See Figure 36)

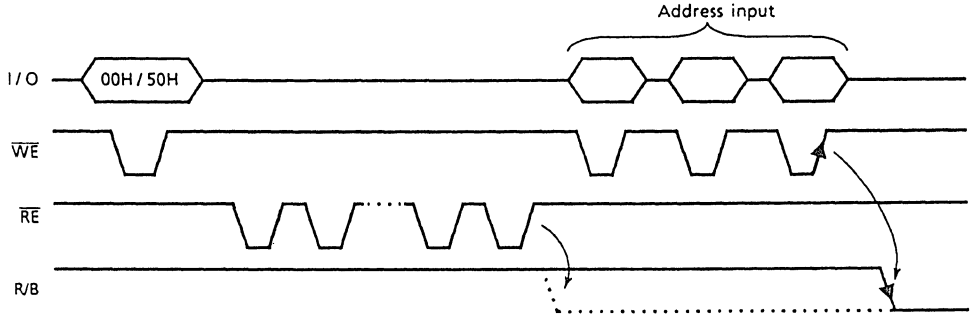
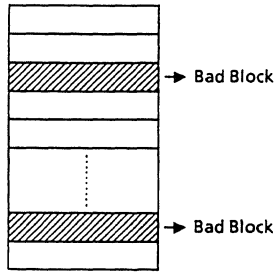


Figure 36

Therefore, $\overline{RE}$ clocking must occur after the address input.

(17) Invalid block (bad block)

The TC5816 device contains unusable blocks. Therefore, the following issues must be recognized:



Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate. The number of valid blocks is as follows:

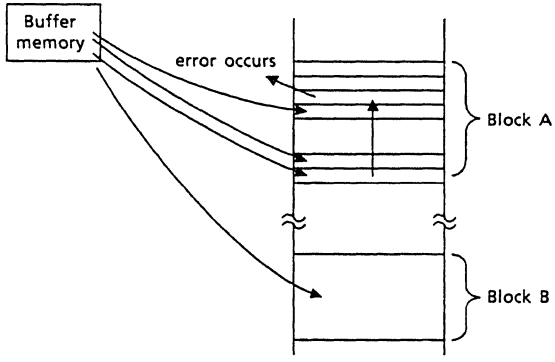
	MIN.	TYP.	MAX.	UNIT
Valid (Good) Block Number	502	508	512	Blocks

Figure 37 shows the bad block test flow.

(18) Error in program or erase operation (Fail at status read)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs.

Program

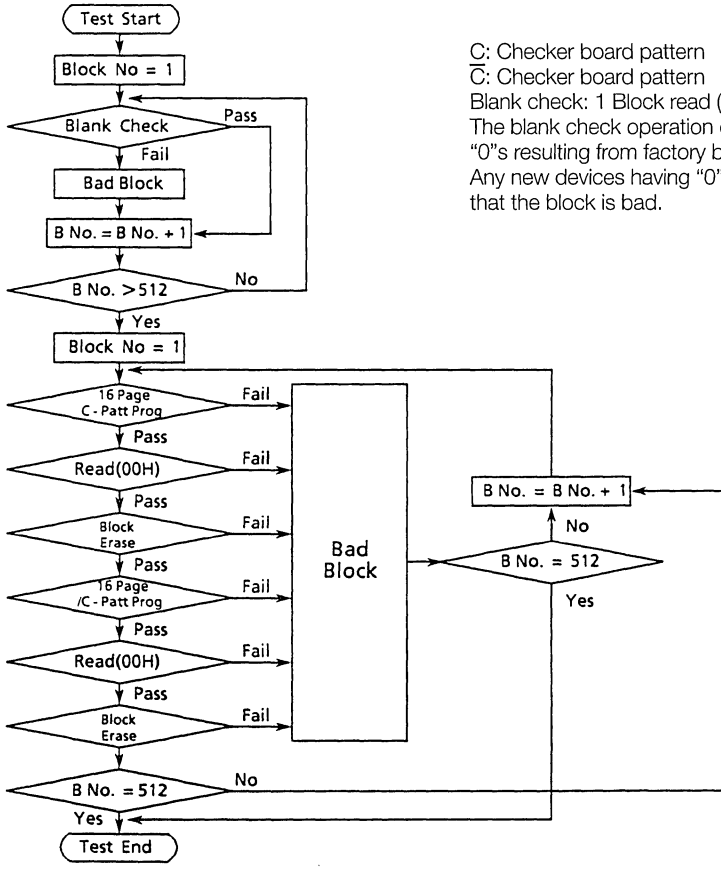


When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad blocks" table or another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)

Bad Block Test Flow



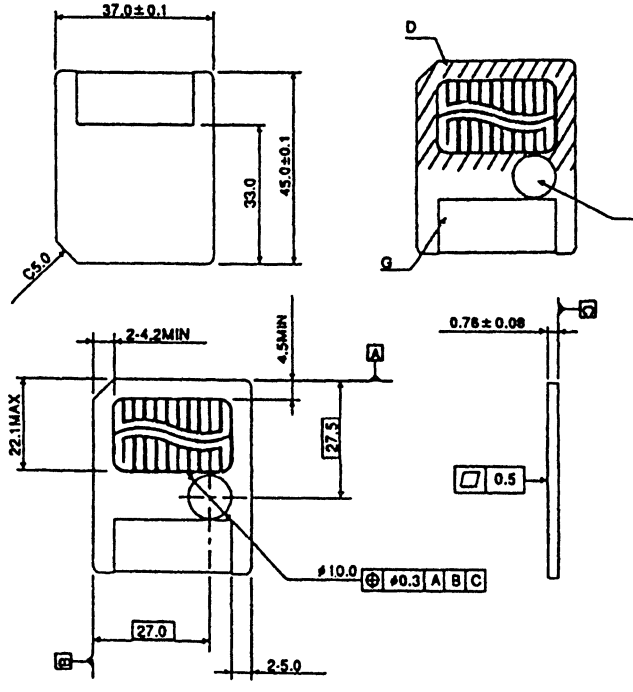
C: Checker board pattern
$\overline{C}$: Checker board pattern
Blank check: 1 Block read (FFH)
The blank check operation detects
"0"s resulting from factory block testing.
Any new devices having "0"s in a block indicates
that the block is bad.

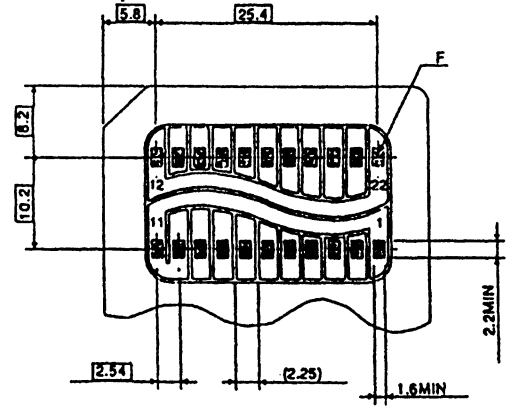
Figure 37. Bad Block Test Flow

Outline Drawings

FDC-22

Unit: mm





Contact area (2 : 1)

E: Write protect area
F: The distance between the surface of D and all contact area is less than 0.1mm.
G: Index area

Weight: 0.48g (typ.)

Attention

(1) Avoid bending or subjecting the card to sudden impact.
(2) Avoid touching the connectors to protect against damage from static electricity.
This card should be kept in the antistatic film case when not in use.
(3) Toshiba cannot accept and hereby disclaims liability for any damage to the card including data corruption that may occur because of mishandling.

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TC5832FT

PRELIMINARY

32Mbit (4M x 8 BIT) CMOS NAND EEPROM (5V)

Description

The TC5832FT is a 5 volt 34M (34,603,008) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 528 bytes x 16 pages x 512 blocks. The device has a 528 byte static register which allows program and read data to be transferred between the register and the memory cell array in 528 byte increments. The erase operation is implemented in a single block unit (8k bytes + 256 bytes: 528 bytes x 16 pages).

The TC5832FT is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for still cameras, and other systems which require high density, non-volatile memory data storage.

Features

- Organization
  - Memory cell array : 528 x 8K x 8
  - Register : 528 x 8
  - Page size : 528 bytes
  - Block size : (8k + 256) bytes
- Mode : Read, Reset, Auto page program, Auto block erase, Suspend/ Resume, Status read
- Mode control : Serial input/output Command control
- Package :400mil TSOP Type II
  - TC5832FT : TSOP44-P-400B (0.48g typ.)
- Power supply : V_{CC} = 5.0V±0.5V
- Access time
  - Cell array - Register : 10µs max.
  - Serial Read Cycle : 50ns max.
- Operating current
  - Read (50ns cycle) : 15mA typ.
  - Program (ave.) : 40mA typ.
  - Erase (ave.) : 20mA typ.
  - Standby : 100µA
- Operating temperature : 0 ~ 70°C

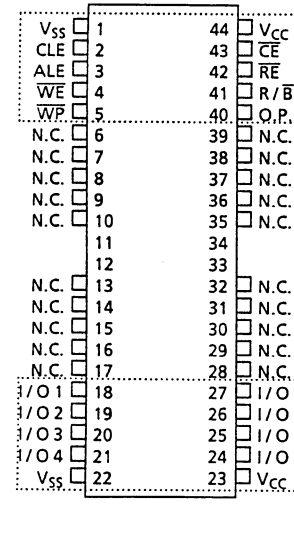
Pin Names

$I/O_{1\sim8}$	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready/Busy
OP	Option Pin
V_{CC}	Power Supply
V_{SS}	Ground

OP: GND Input: 528 Byte/Page Operation
V_{CC} Input: 512 Byte/Page Operation

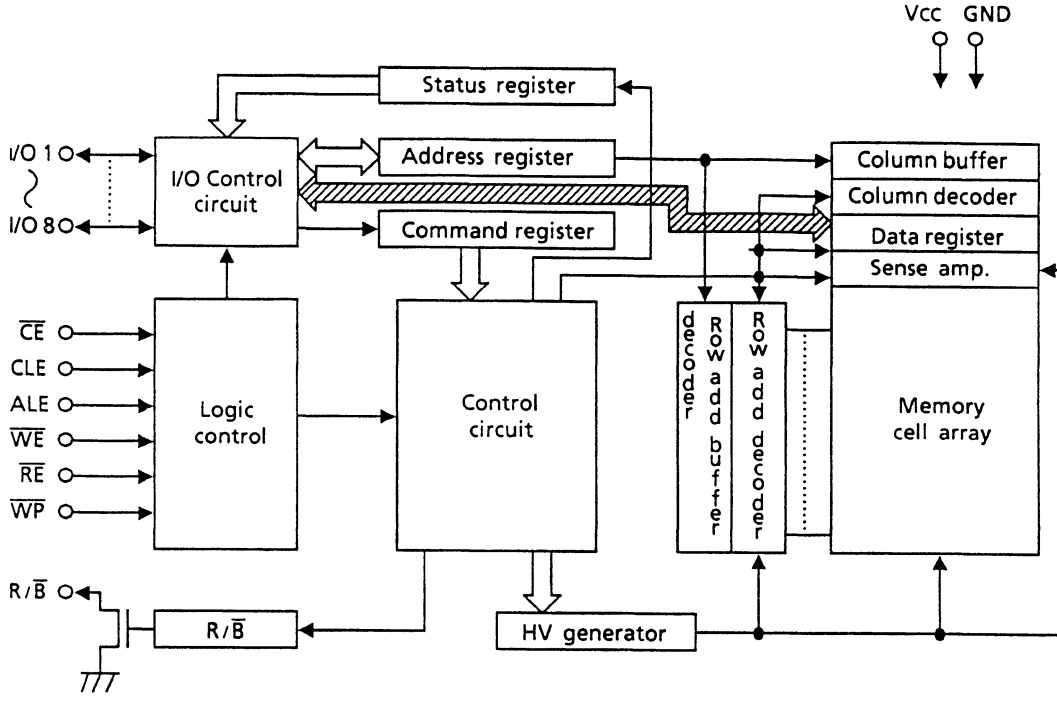
Pin Connection (Top View)

TC5832FT



D. Non-Volatile

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply	-0.6 ~ 7.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	
$V_{I/O}$	Input/Output Voltage	-0.6V ~ V_{CC} + 0.5V (≤ 7.0V)	
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STG}	Storage Temperature	-55 ~ 150	
T_{OPR}	Operating Temperature	0 ~ 70	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	5	10	

*This parameter is periodically sampled and is not 100% tested.

Valid Blocks (1)

SYMBOL	PARAMETER	TC5832FT			UNIT
		MIN.	TYP.	MAX.	
N_{VB}	Valid block number	502	508	512	Blocks

(1) The TC5832FT includes unusable blocks. Refer to notification (17) toward the end of this document.

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.5	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	

* -2V (pulse width ≤ 20ns)

DC Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5.0V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0V ~ V_{CC}		–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}		–	–	±10	
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL} I_{OUT} = 0mA	t_{cycle} = 50ns	–	15	30	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 50ns		–	15	30	
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 50ns		–	40	60	
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 50ns		–	15	30	
I_{CCO7}	Program Current	–		–	40	60	
I_{CCO8}	Erasing Current	–		–	20	40	
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2V		–	–	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = - 400μA		2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		–	–	0.4	
$I_{OL}(R/\overline{B})$	Output Current of ($R/\overline{B}$) pin	V_{OL} = 0.4V		–	8	–	mA

D. Non-Volatile

AC Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5.0V±0.5V) (1)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	–	ns	
t_{CLH}	CLE Hold Time	10	–	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	–	ns	
t_{WP}	Write Pulse Width	25	–	ns	
t_{ALS}	ALE Setup Time	0	–	ns	
t_{ALH}	ALE Hold Time	10	–	ns	
t_{DS}	Data Setup Time	20	–	ns	
t_{DH}	Data Hold Time	10	–	ns	
t_{WC}	Write Cycle Time	50	–	ns	(2)
t_{WH}	$\overline{WE}$ High Hold Time	15	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	–	ns	
t_{RP}	Read Pulse Width	25	–	ns	
t_{RC}	Read Cycle Time	50	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	35	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in the Serial Read Cycle	100	–	ns	(4)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	–	35	ns	
t_{OH}	Data Output Hold Time	10	–	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	–	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	–	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	–	ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_{R}	Memory Cell Array to Starting Address	–	10	µs	
t_{WB}	$\overline{WE}$ High to Busy	–	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (read cycle)	50	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (Sequential Read)	–	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of Interception by $\overline{CE}$ in Read Mode)	–	600	ns	(3)
t_{RST}	Device Resetting Time (Read/Program/Erase/after Suspend Command)	–	6/10/ 500/5	µs	

AC Test Conditions

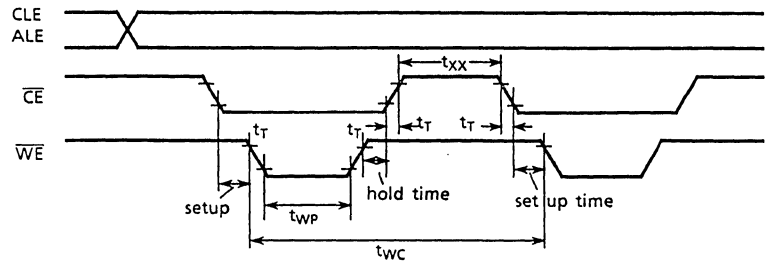
Input Level	2.4V/0.6V
Input Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1 TTL and C_L (100 pF)

(1) Transition time (t_T) = 5ns.

(2) In the case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 50ns.

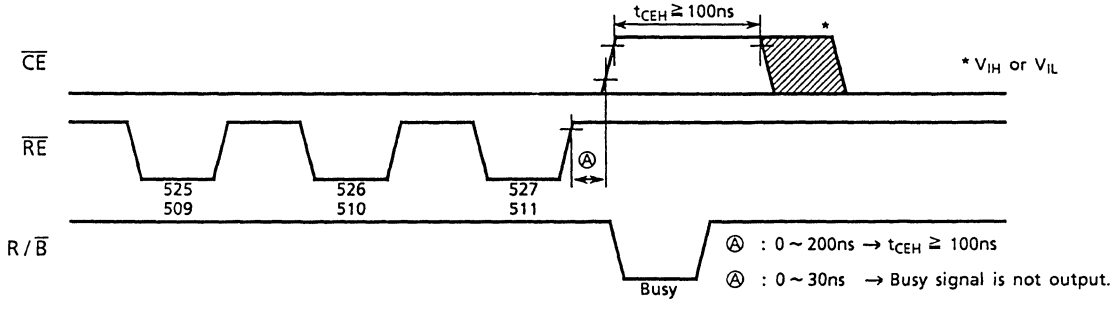
$$\underset{0ns}{\text{set - up time}} + \underset{10ns}{\text{hold time}} + \underset{25ns}{t_{WP}} + \underset{20ns}{t_{XX}} + 4t_T$$

(ex.)



(3) $\overline{CE}$ high to Ready time depends on the pullup resistor tied to the R/$\overline{B}$ pin. (Refer to notification (10) toward the end of this document.).

(4) If $\overline{CE}$ returns to a high level after accessing the last address (527) in read modes (1), (2) or (3), the $\overline{CE}$ high time must keep equal to or greater than 100ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200ns as shown below. In the second case, the device will not turn to a "Busy" state when the $\overline{CE}$ delay time is less than 30ns.



D. Non-Volatile

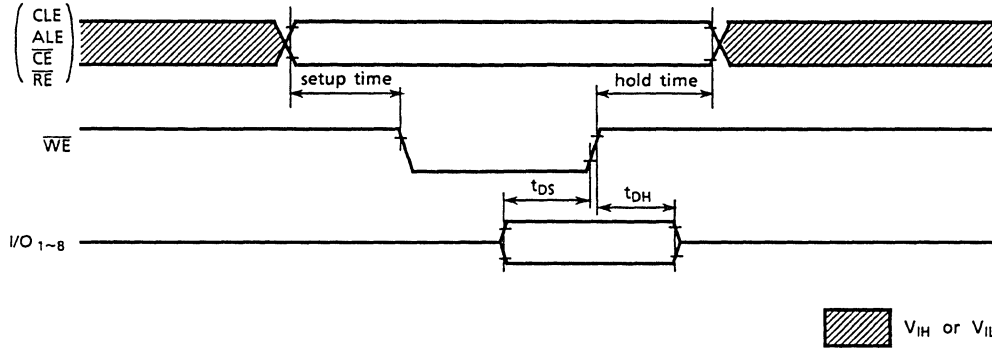
Programming and Erasing Characteristics (Ta = 0 ~ 70°C, V_{CC} = 5.0V±0.5V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
t_{PROG}	Average Programming Time		300	1500	µs	
N	Divided Number on Same Page			3		(1)
t_{BERASE}	Block Erasing Time		6	50	ms	
t_{SR}	Suspend Input to Ready			0.5	ms	
t_{EV}	Erase verify time			6	µs	
$N_{P/E}$	Number of Program/Erase Cycles	250K	1 x 10^6			

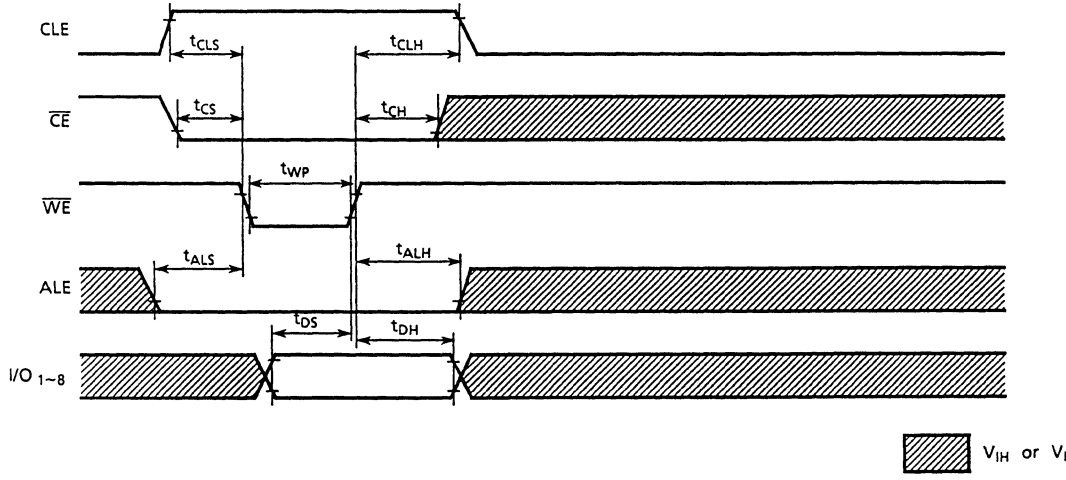
(1) Refer to notification (15) toward the end of this document.

Timing Charts

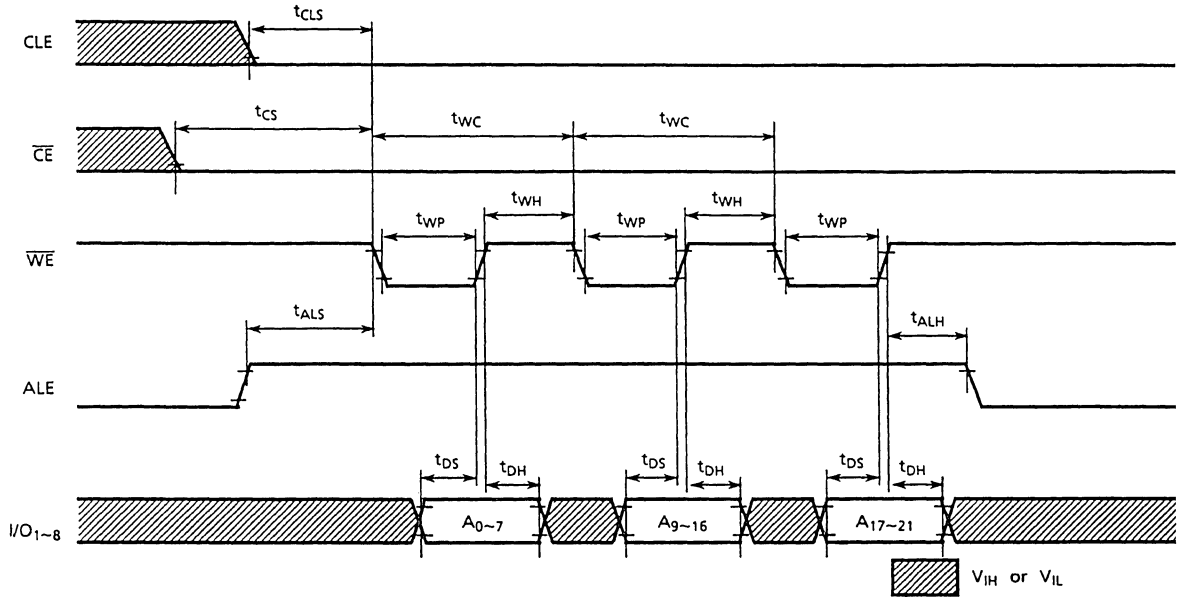
Latch Timing Chart for Command/Address/Data



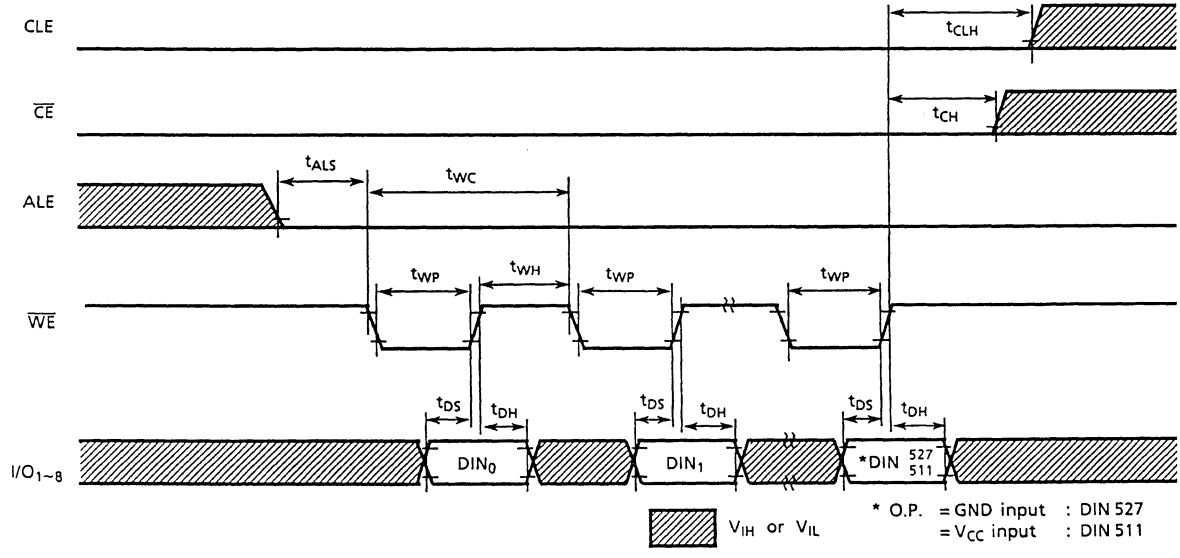
Command Input Cycle



Address Input Cycle

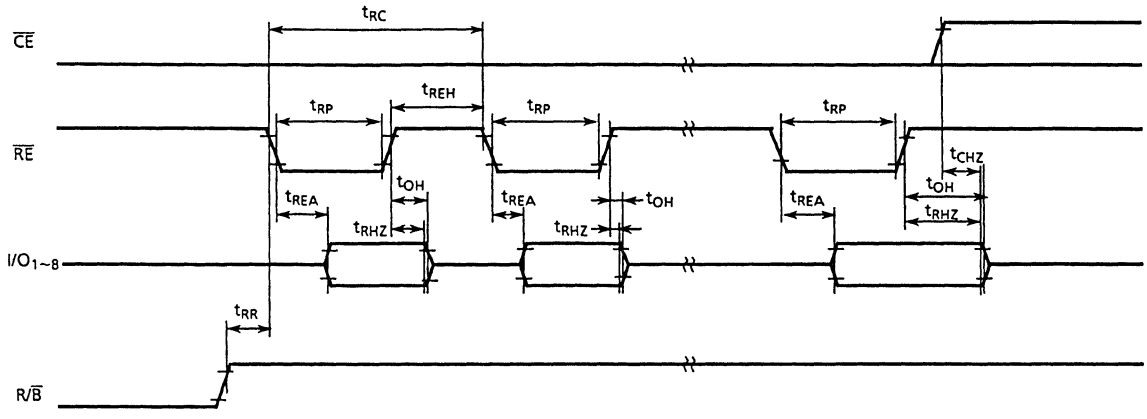


Data Input Cycle

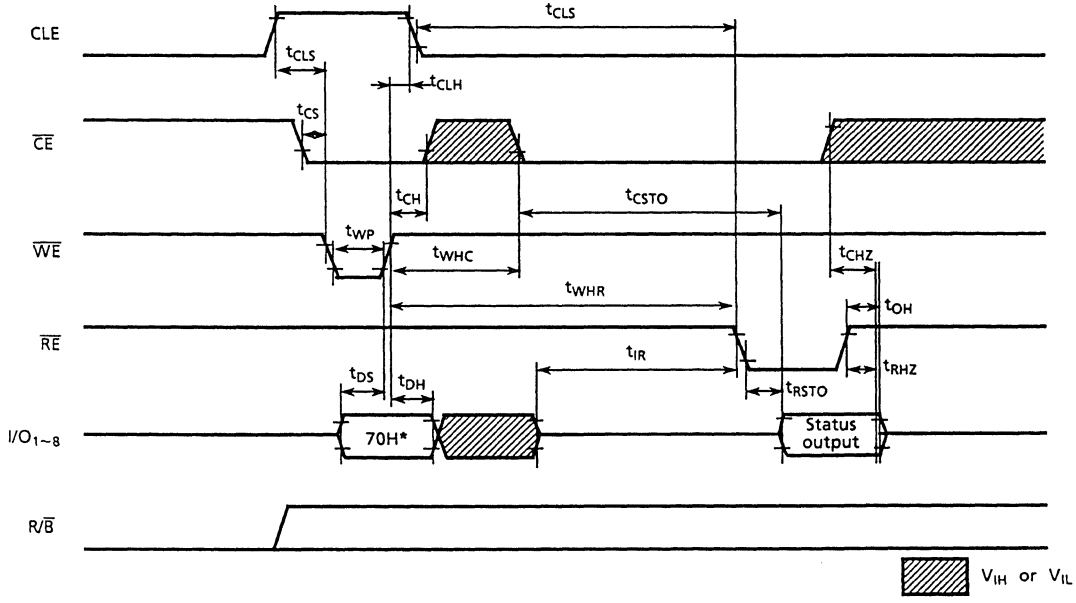


D. Non-Volatile

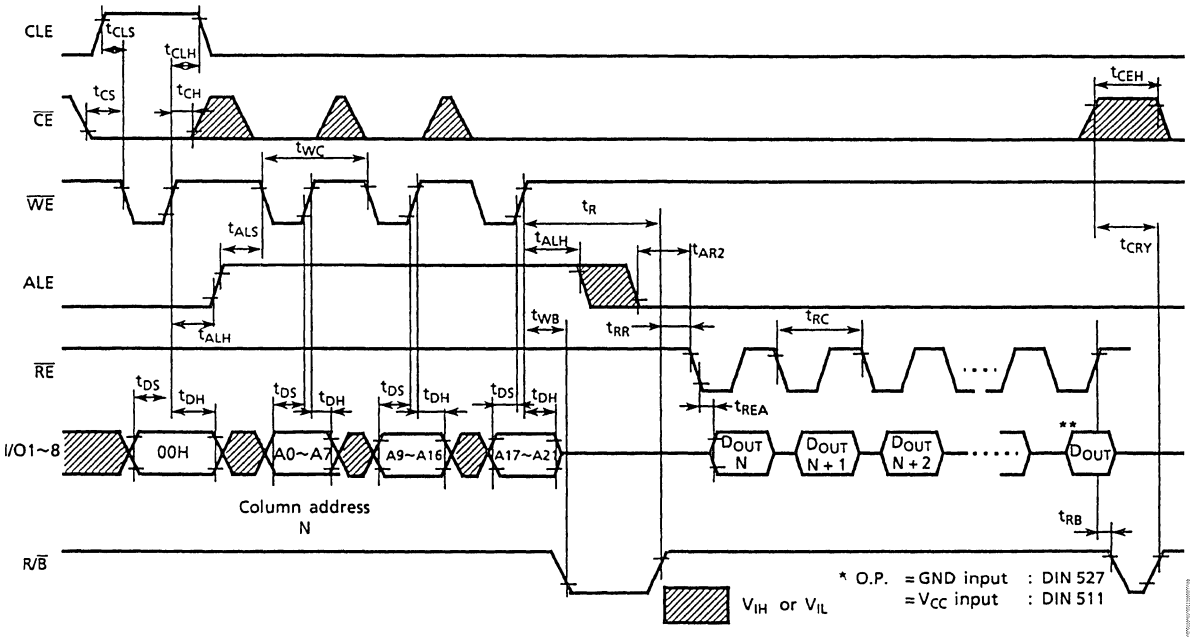
Serial Read Cycle



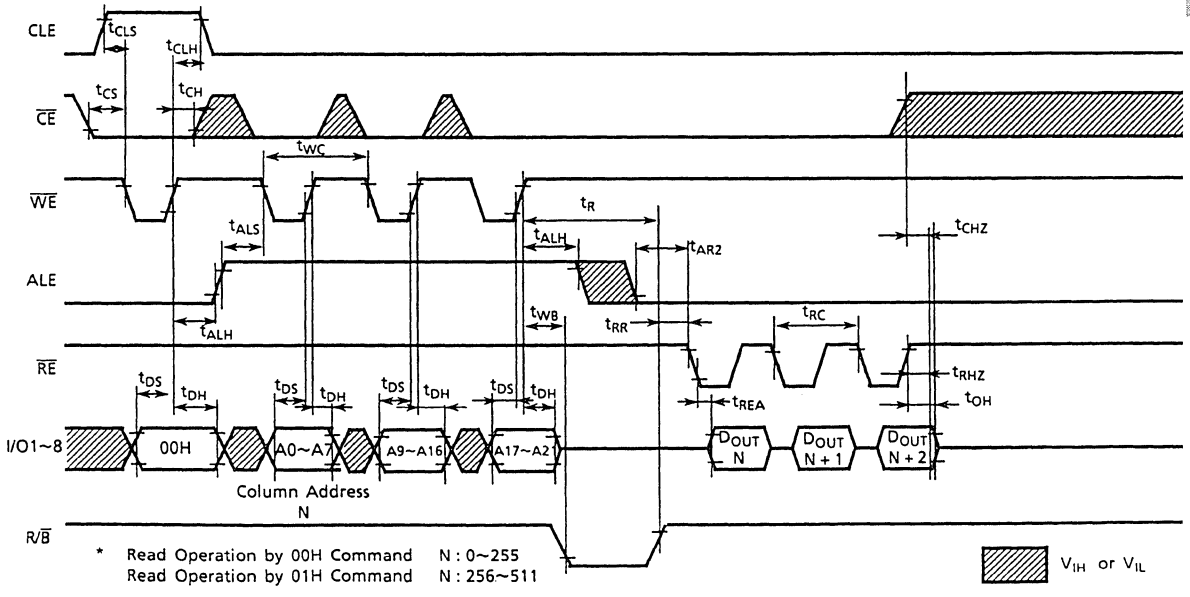
Status Read Cycle



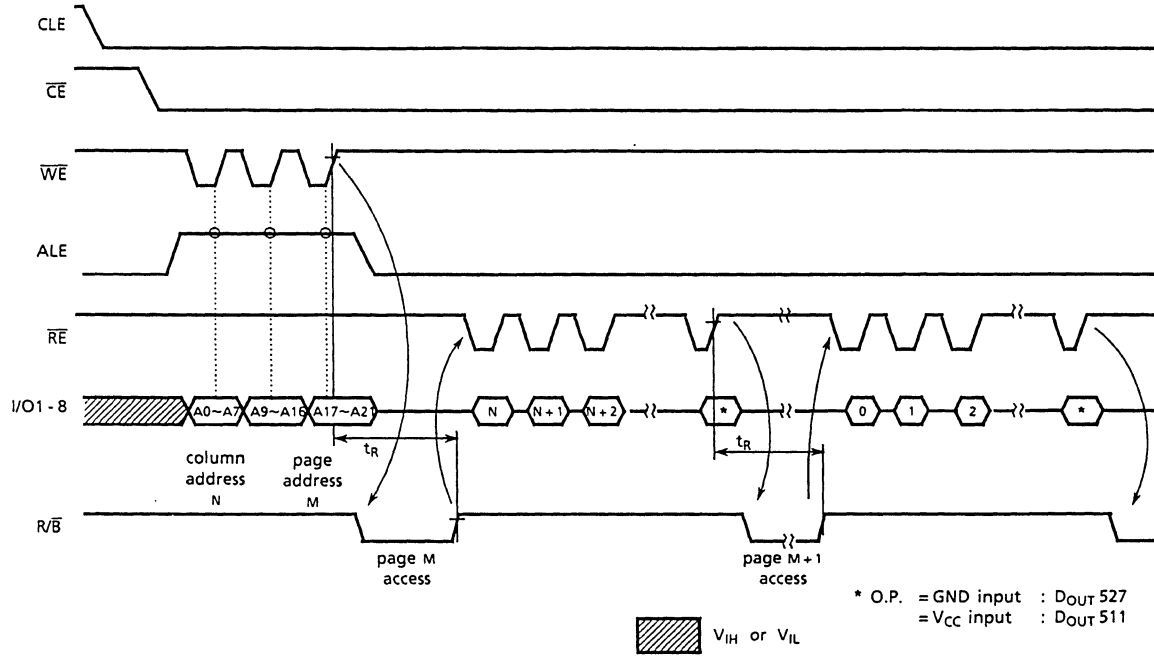
Read Cycle (1)



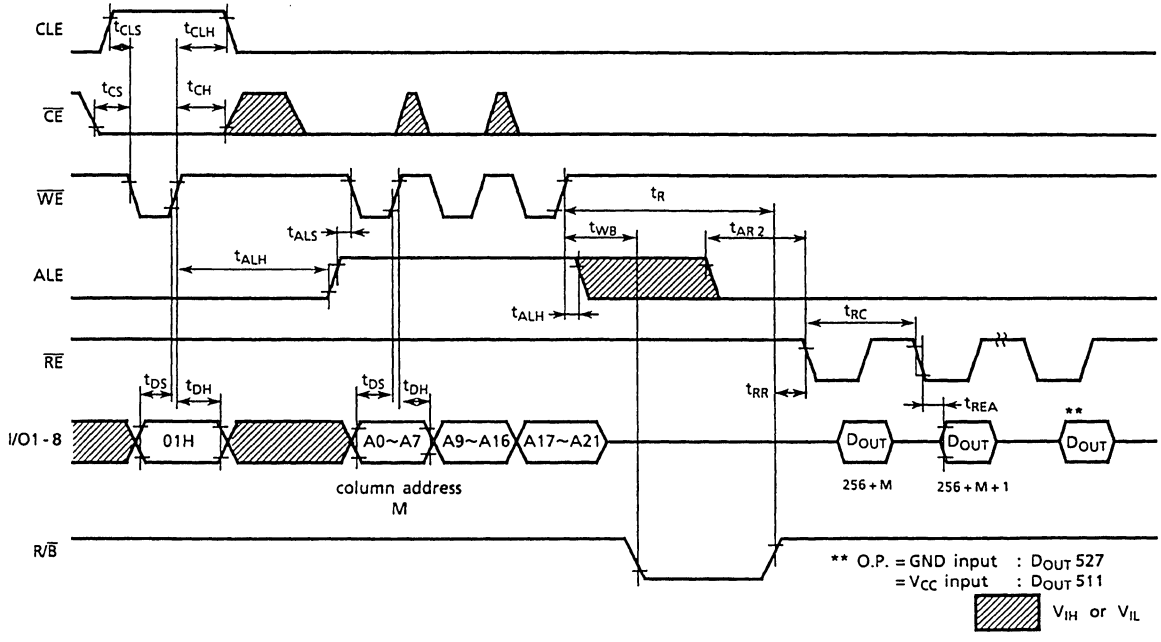
Read Cycle (1): Interception by $\overline{CE}$



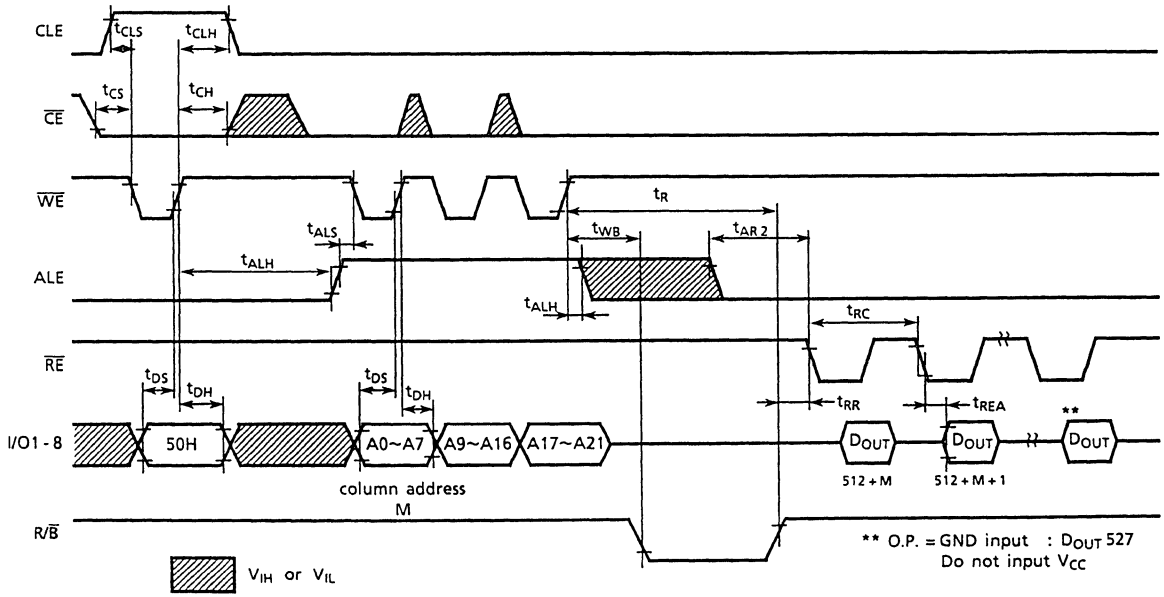
Sequential Read Timing



Read Cycle (2)

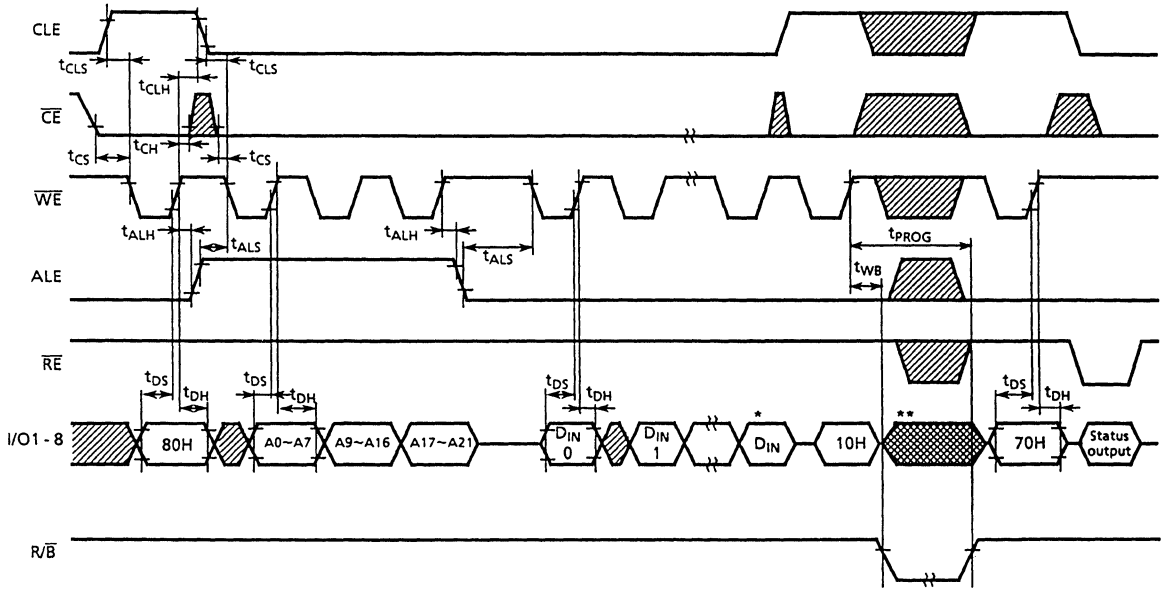


Read Cycle (3)

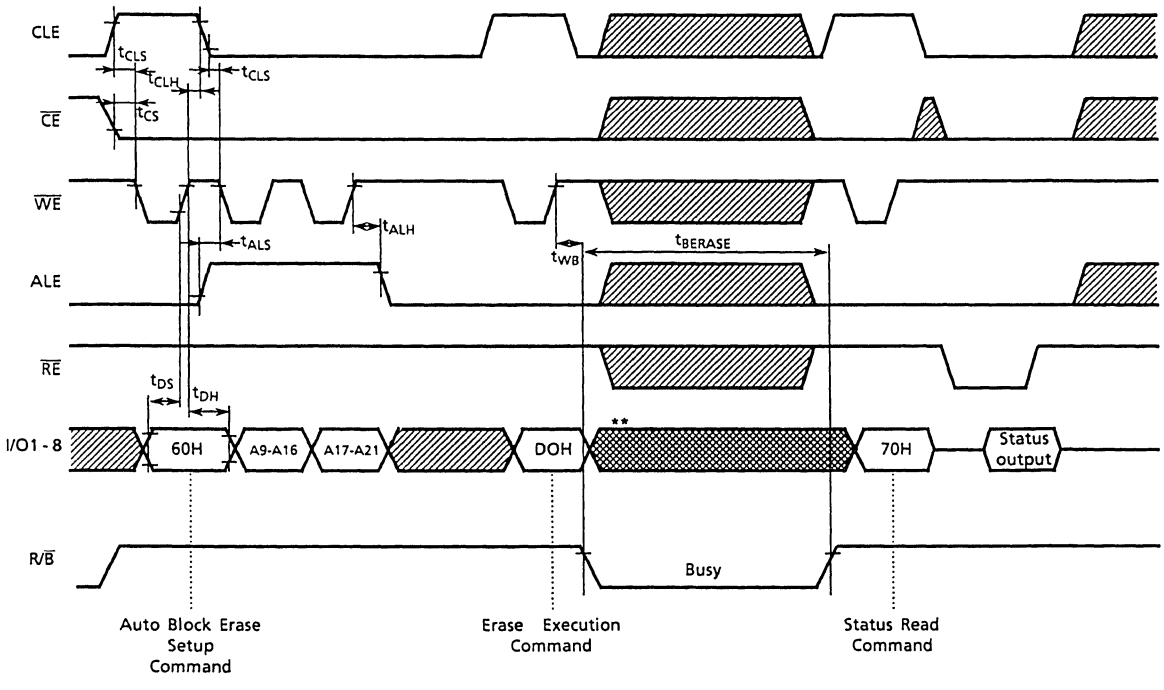


D. Non-Volatile

Auto Program Operation Timing Chart



Auto Block Erase Timing

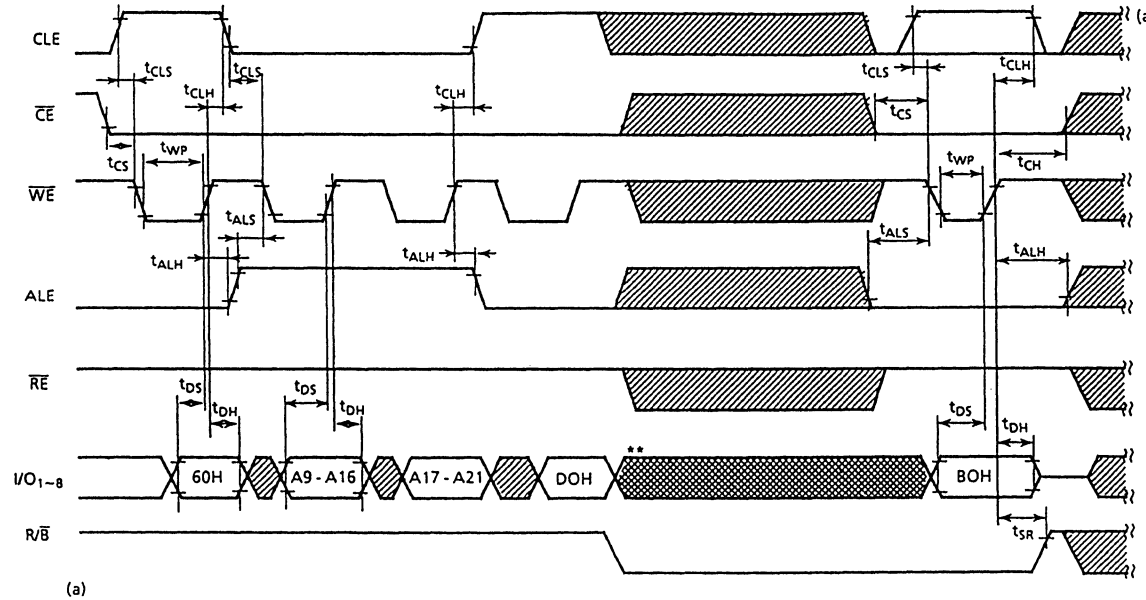


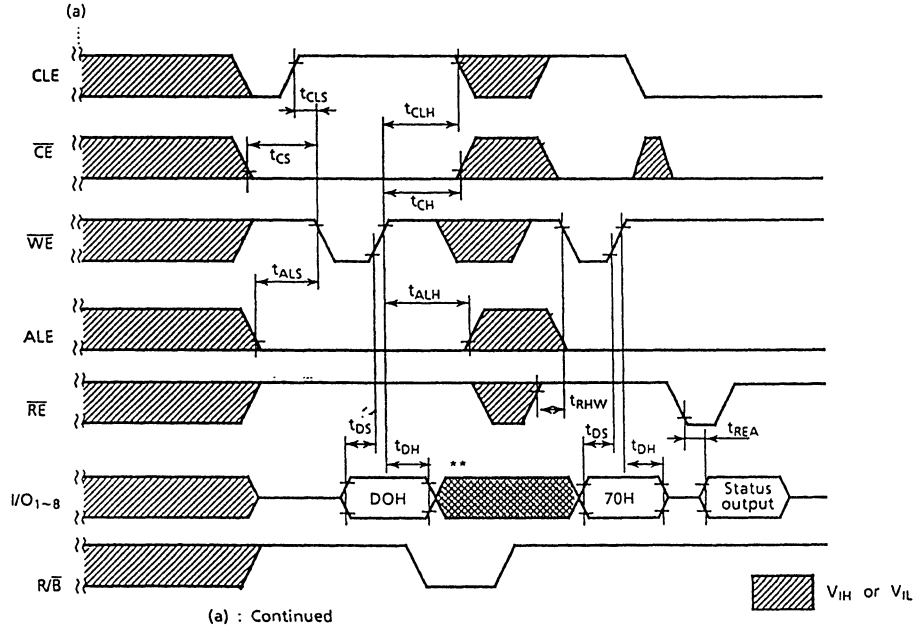
** Do not collide data input with data output.

V_{IH} or V_{IL}

D. Non-Volatile

Suspend/Resume on Block Erase Operation

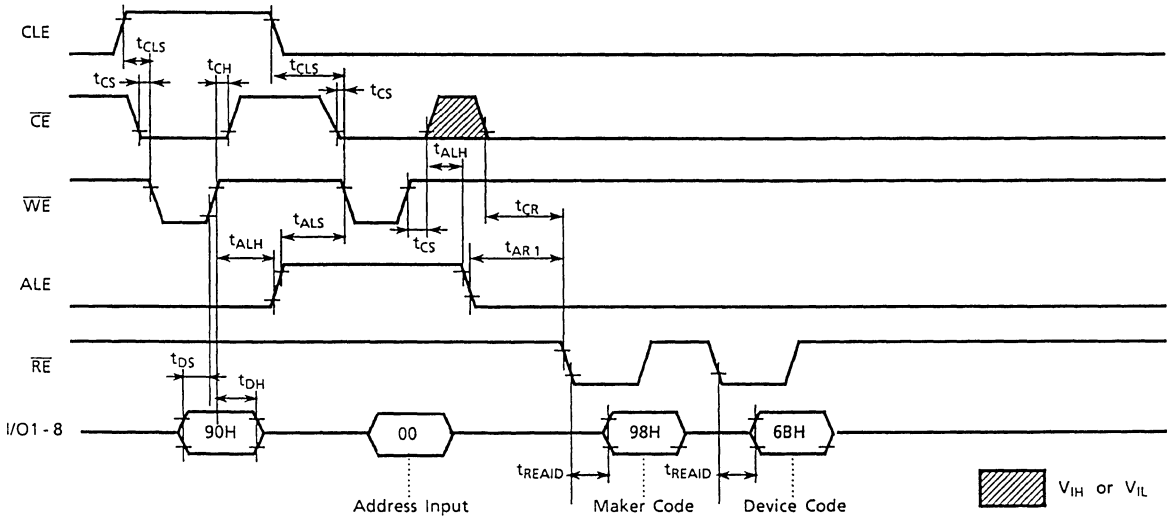




(a) : Continued

** Do not collide data input with data

ID Read Operation



Pin Function

The TC5832FT is a serial access memory in which address and data information is multiplexed. The device pinout is shown in Figure 1.

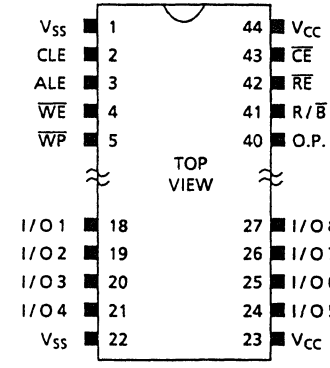


Figure 1. TC5832FT Pinout

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$

The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the busy state ($R/\overline{B}$ = L) during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input. The $\overline{CE}$ signal must stay low during the read mode busy state to ensure that the memory array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls the serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O1 ~ 8

The I/O 1 ~ 8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: $R/\overline{B}$

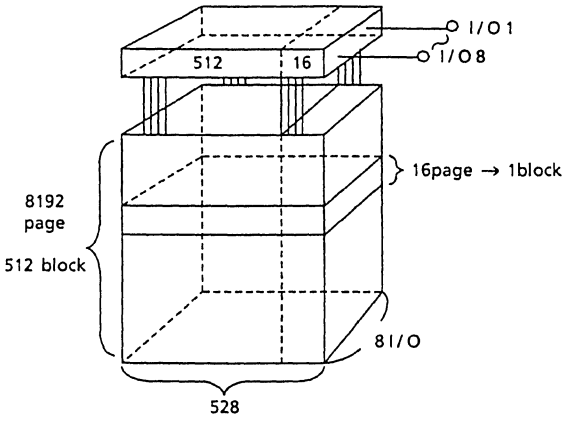
The $R/\overline{B}$ output signal is used to indicate the state of the device. The $R/\overline{B}$ signal indicates a busy state ($R/\overline{B}$ = L) during program, erase, or read operations and will return to a ready state ($R/\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

Option Pin: OP

The OP signal is used to change the page size. The device is in the 528 byte/page mode when OP = GND, and 512 byte/page mode when OP = V_{CC}.

Schematic Cell Layout and Address Assignment

The program operation is implemented in a page unit while the erase operation is carried out in block units.



A page consists of 528 bytes in which 512 bytes are for main memory and 16 bytes are for redundancy or other uses.

1 Page = 528 bytes;
1 Block = 528 bytes x 16 pages = (8K + 256) bytes
Total device density = 528 bytes x 16 pages
x 512 blocks
≈ 34M bits (4.325M bytes)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Figure 3.

Figure 2. TC5832 Schematic Cell Layout

	I/01	I/02	I/03	I/04	I/05	I/06	I/07	I/08
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A9	A10	A11	A12	A13	A14	A15	A16
Third cycle	A17	A18	A19	A20	A21	*L	*L	*L

A0 ~ A7 : column address
A9 ~ A21 : page address
A13 ~ A21: block address
A9 ~ A12 : NAND address in block

* A8 is initially set to "Low" or "High" by "00H" Command or "01H" Command.
* I/O 6 ~ 8 during the third cycle must be set to low level

Figure 3. Addressing

Operation Mode: Logic and Command Tables

The operation modes such as program, erase, read, erase suspend, and reset are controlled by the eleven different command operations shown in Table 2. The address, command input, and data input /output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, and $\overline{WP}$ signals as shown in Table 1.

D. Non-Volatile

Table 1. Logic Table

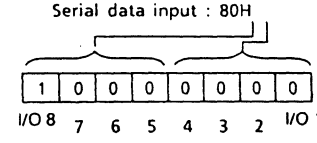
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command input	H	L	L	⌐↓	H	*
Data input	L	L	L	⌐↓	H	*
Address input	L	H	L	⌐↓	H	*
Serial data output	L	L	L	H	↓⌐	*
During programming (Busy)	*	*	*	*	*	H
During erasing (Busy)	*	*	*	*	*	H
Program, Erase inhibit	*	*	*	*	*	L

H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Table 2. Command Table (HEX data)

	FIRST CYCLE	SECOND CYCLE	ACCEPTABLE COMMAND DURING BUSY
Serial data input	80	–	
Read mode (1)	00	–	
Read mode (2)	01	–	
Read mode (3)	50	–	
Reset	FF	–	√
Auto program	10	–	
Auto block erase	60	D0	
Suspend in erasing	B0	–	√
Resume	D0	–	
Status read	70	–	√
ID read	90	–	

Bit assignment of HEX data (Example)



Once the device is set into the read mode by the "00H", "01H" or "50H" command, additional read commands are not needed for sequential page read operations. Table 3 shows the operation mode for reads.

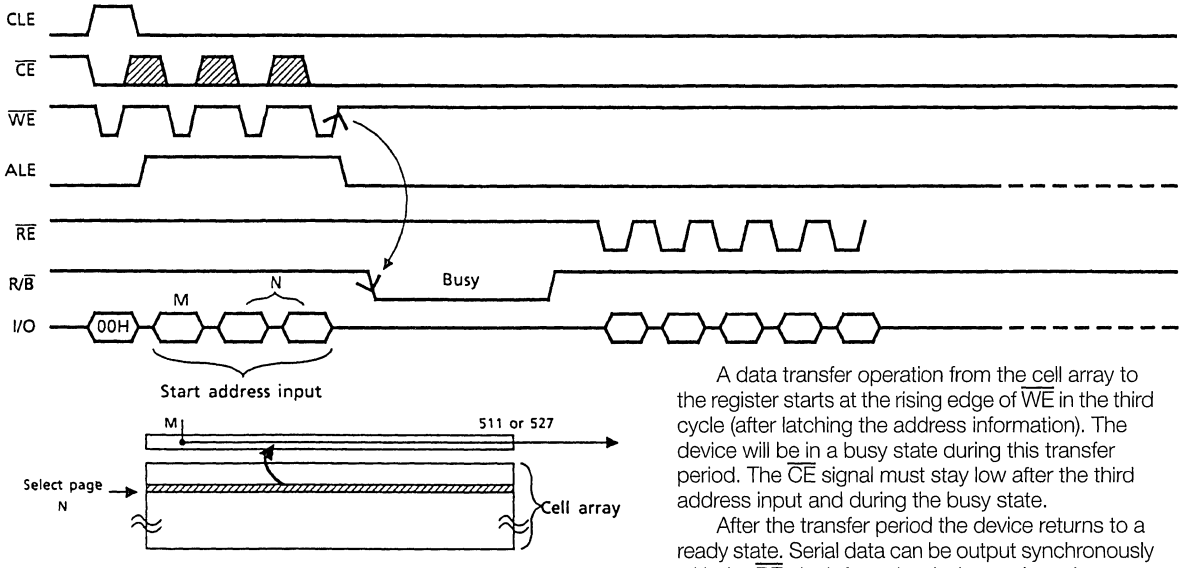
Table 3. Operation mode for reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 ~ I/O8	POWER
Read mode	L	L	L	H	L	Data output	Active
Output deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

Device Operation

Read Mode (1)

Read mode (1) is set by issuing a "00H" command to the command register. Refer to Figure 4 below for timing details and block diagram.

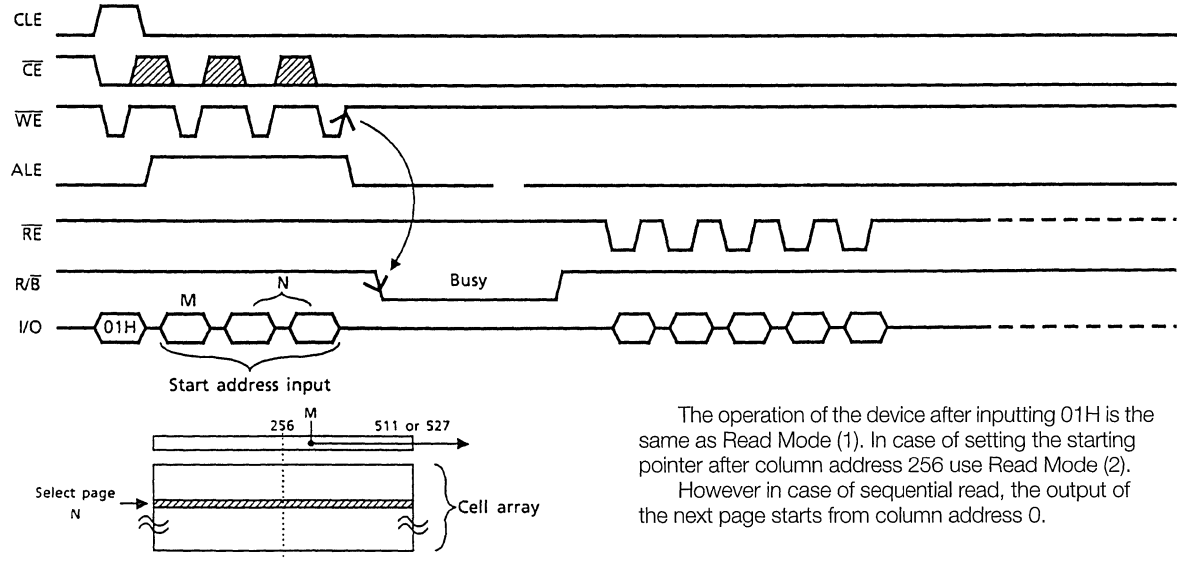


A data transfer operation from the cell array to the register starts at the rising edge of $\overline{WE}$ in the third cycle (after latching the address information). The device will be in a busy state during this transfer period. The $\overline{CE}$ signal must stay low after the third address input and during the busy state.

After the transfer period the device returns to a ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the designated starting pointer indicated during the address input cycle.

Figure 4. Read mode (1) operation

Read Mode (2)



The operation of the device after inputting 01H is the same as Read Mode (1). In case of setting the starting pointer after column address 256 use Read Mode (2).

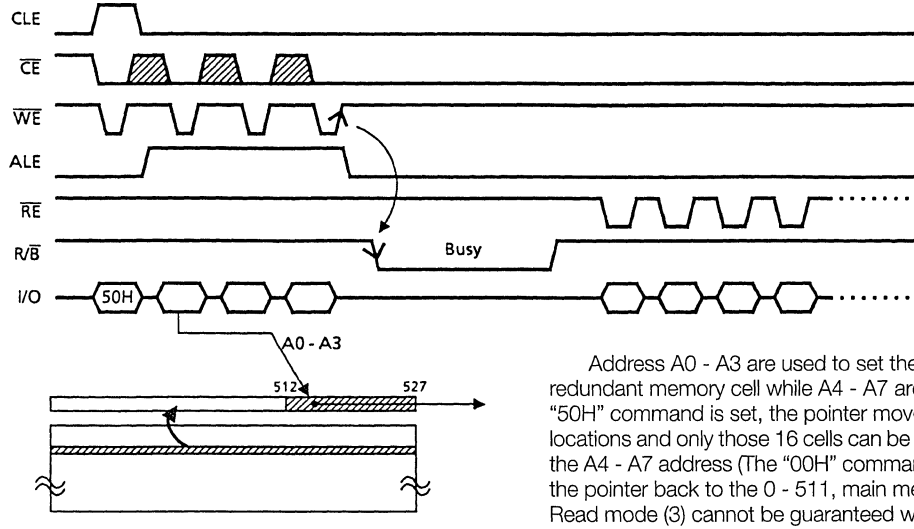
However in case of sequential read, the output of the next page starts from column address 0.

Figure 5. Read mode (2) operation

D. Non-Volatile

Read Mode (3)

Read mode (3) has the same timing as read mode (1) and (2) but it is used to access information in the extra 16 byte redundancy area of the page. The starting pointer is therefore assigned between byte 512 and 527.

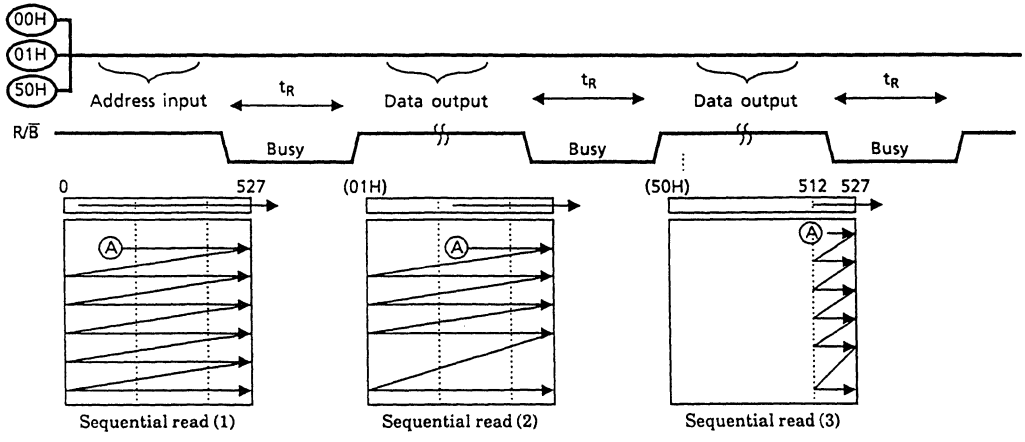


Address A0 - A3 are used to set the starting pointer for the redundant memory cell while A4 - A7 are ignored. Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 16 cells can be addressed regardless of the A4 - A7 address (The "00H" command is necessary to move the pointer back to the 0 - 511, main memory cell locations.) Read mode (3) cannot be guaranteed when OP is V_{CC}.

Figure 6. Read mode (3) operation

Sequential Read (1)(2)(3)

This mode allows sequential reads without additional address input.



Sequential read mode (1) and (2) outputs addresses 0 to 527 as shown above while sequential read mode (3) outputs the redundant address locations only. When the pointer reaches the last address, the device continues to output the last data ** with each $\overline{RE}$ clock signal.

** OP = GND input: column address 527.
V_{CC} input: column address 511.

Status Read

The TC5832FT automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the ready/busy status of the device, determines the pass /fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 4.

Table 4. Status output table

	STATUS	OUTPUT	
I/O 1	Pass/Fail	Pass: "0"	Fail: "1"
I/O 2	Not used	"0"	
I/O 3	Not used	"0"	
I/O 4	Not used	"0"	
I/O 5	Not used	"0"	
I/O 6	Suspend	Suspended: "1"	Not Suspended: "0"
I/O 7	Ready/Busy	Ready: "1"	Busy: "0"
I/O 8	Write protect	Protect: "0"	Not Protect: "1"

The Pass/Fail status on I/O 1 is only valid when the device is in the ready state. The device will always indicate a pass status while in the busy state.

An application example with multiple devices is shown in Figure 7.

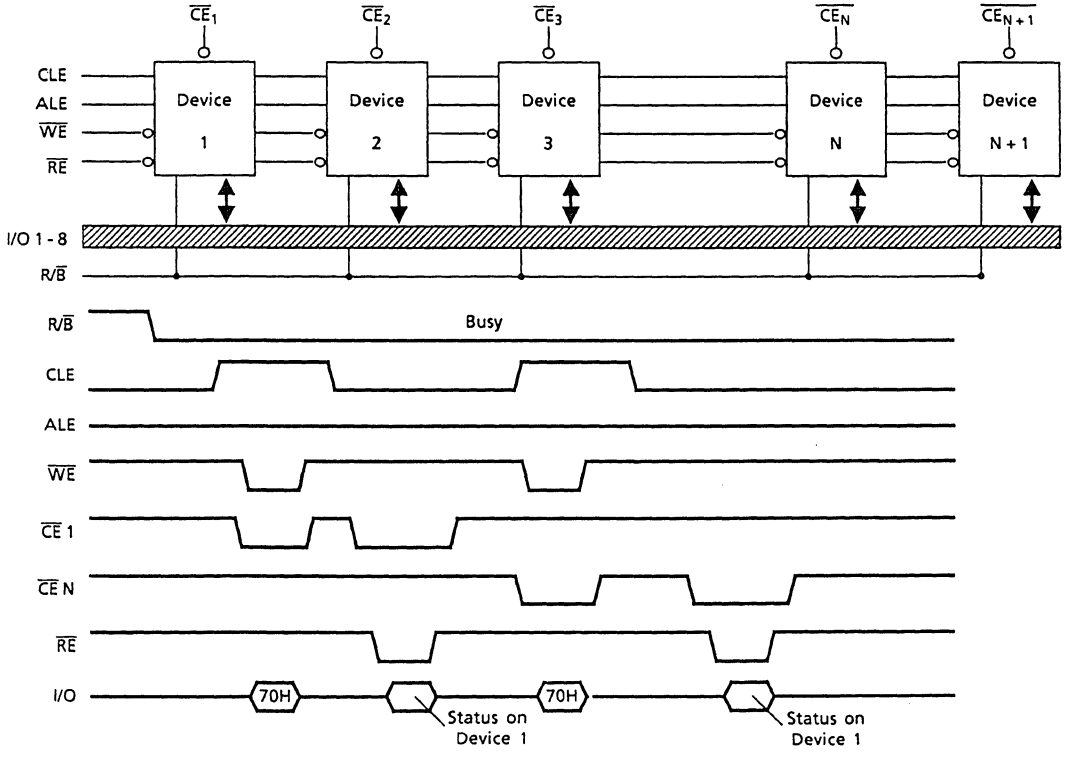
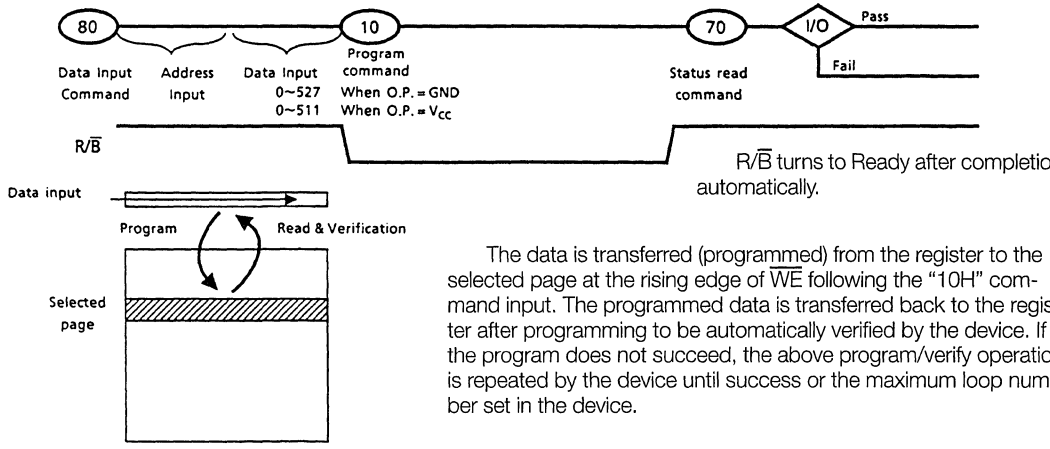


Figure 7. Status read timing application example

SYSTEM DESIGN NOTE: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status read function can be used to determine the status of each individually selected device.

Auto Page Program

The TC5832FT implements the automatic page program operation after receiving a "10H" program command after the address and data have been input. The sequence of command, address, and data input is shown below. (Refer to the detail timing chart.)



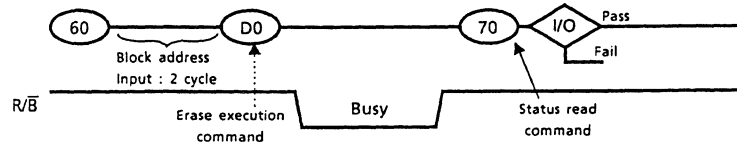
The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the "10H" command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

Figure 8. Auto page program

Auto Block Erase

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command "D0H" (which follows the erase setup command "60H"). This two cycle process for erase operations acts as an extra layer of protection from accidental erasure of data due to possible external noise. The device automatically executes the erase and verify operations.

Auto Block Erase



Suspend/Resume

The TC5832FT has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence for this operation are shown below. (Refer to the detail timing chart)

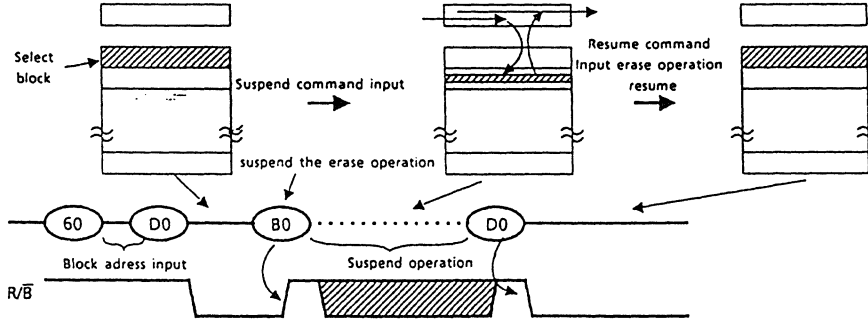


Figure 9. Suspend /Resume Operation

The (B0)·····(D0) suspend/resume cycle can be repeated up to 20 times during a block erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

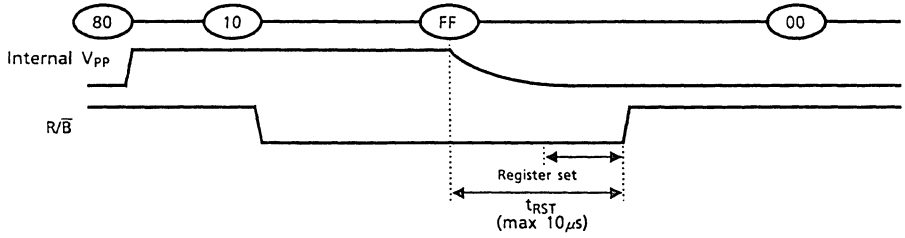
Reset

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go into a wait state. The address and data register are set after a reset as follows:

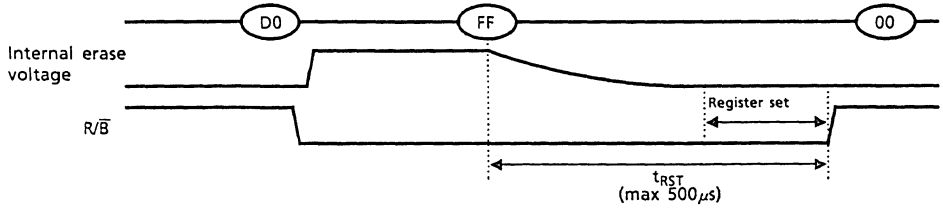
- Address Register : All "0"
- Data Register : All "1"
- Operation Mode : Wait State

The response after a "FFH" reset command input is as follows:

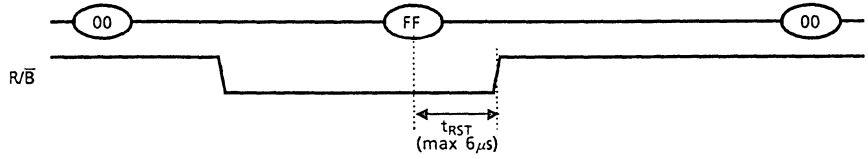
- If the reset (FFH) command is input during programming: Figure 10



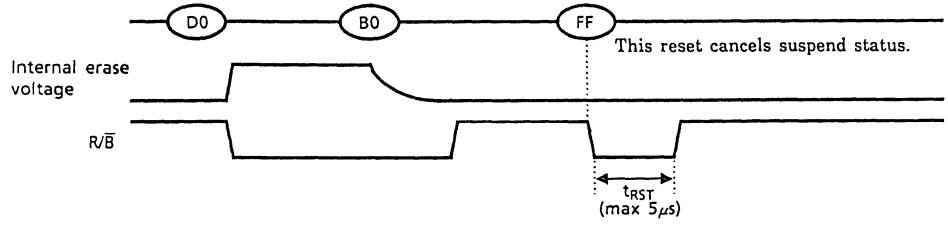
- If the reset (FFH) command is input during erasing: Figure 11



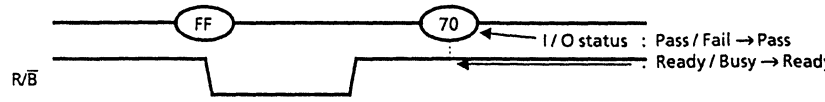
- If the reset (FFH) command is input during the read operation: Figure 12



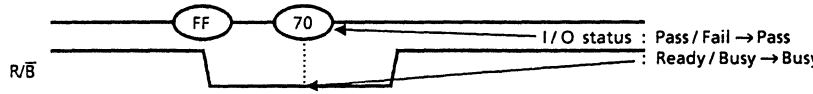
- If the reset (FFH) command is input after suspend: Figure 13



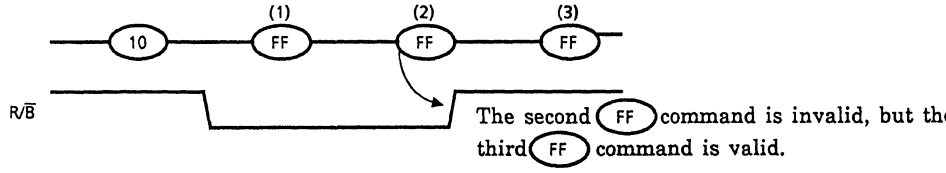
•If the status read command (70H) is input after reset: Figure 14



However, the following operation is prohibited. If the following operation is executed, set up for the address and data register cannot be guaranteed.



If the reset command is input in succession: Figure 15



ID Read

The TC5832FT contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

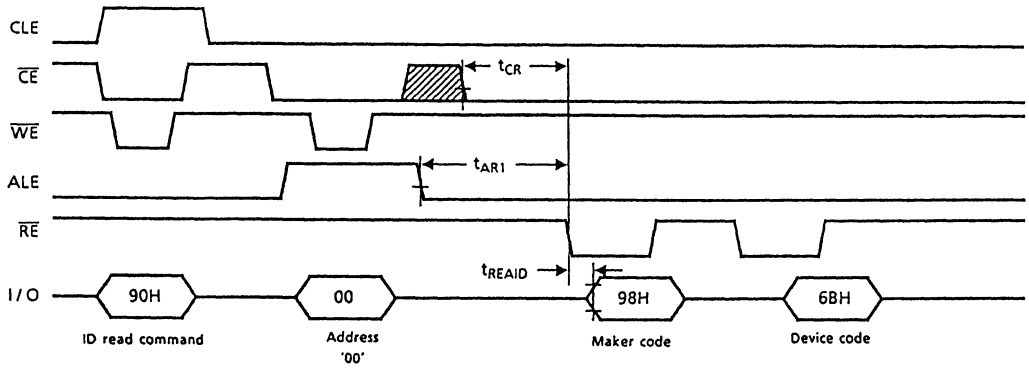


Figure 16. ID read timing

Table 5. Code table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	HEX data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	0	1	0	1	1	6BH

Refer to AC characteristics for t_{READ}, t_{CR}, t_{AR1}.

Device Physics

Program Operation

Figure 17 shows the NAND memory cell and details of the programming mechanism. The program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example showing the operations necessary to program '0' data in TR1 and "1" data in TR2 follows:

(1) The select lines are activated so that the transistor array is connected to the bit line and disconnected from the ground line.
(2) V_{PP} (~20V) is applied to the selected word line and an inhibit voltage of VPI (≈10V) is applied to the unselected word lines.
(3) The bit line tied to cell transistor TR1 is biased to 0V and the bit line tied to TR2 is biased to the inhibit voltage of VDPI (≈10V).
(4) V_{PP} is applied between the control gate and the channel in TR1, as shown in Figure 17, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.
(5) The injected electrons are captured in the floating gate (which is surrounded by an oxide layer) and will remain, even after power is cut off, until they are removed by an erase operation.
(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10V because the voltage of the channel is 10V. Therefore, tunneling does not take place. (i.e. electrons are not injected into the floating gate.)
(7) Tunneling does not take place in the unselected pages because of the 10V (VPI) being applied to the unselected word lines which again makes the voltage difference between control gate and channel only 10 volts. Thus, the floating gate of the "0" cell is charged to "minus" and that of the "1" cell is charged to "plus".

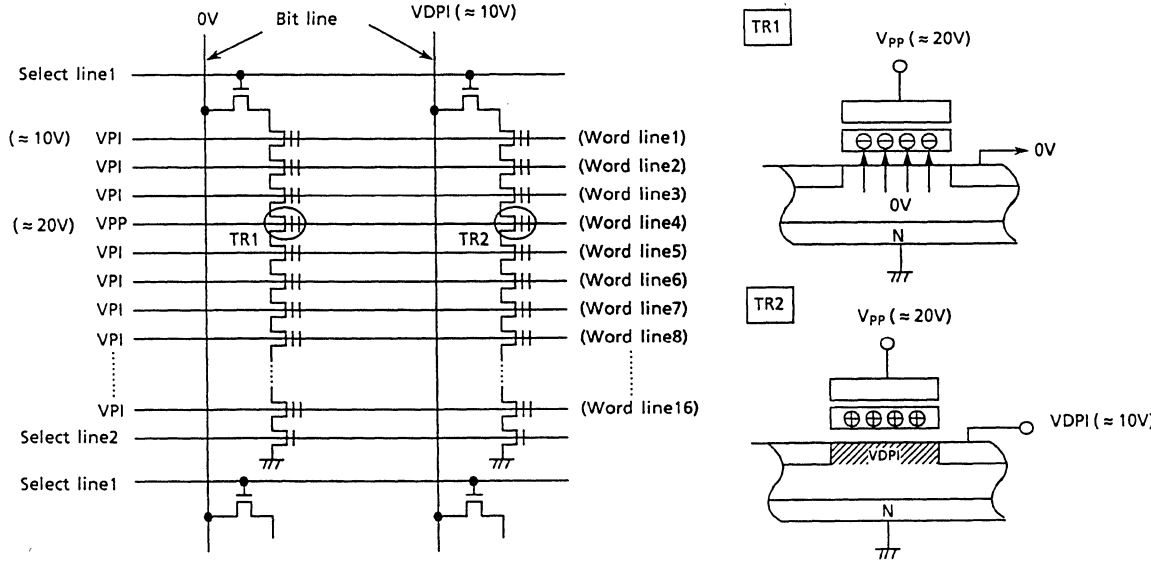


Figure 17. TC5832FT Program Device Physics

Erase Operation

Figure 18 shows the NAND memory cell and details of the erase mechanism. The erase operation is used to turn the "0" (programmed) cells back to "1" in a block. Zero volts is applied to the control gate and V_{PP} (~20V) is applied to the substrate so that a 20 volt potential is created and the electrons in the floating gate are pulled out through tunneling.

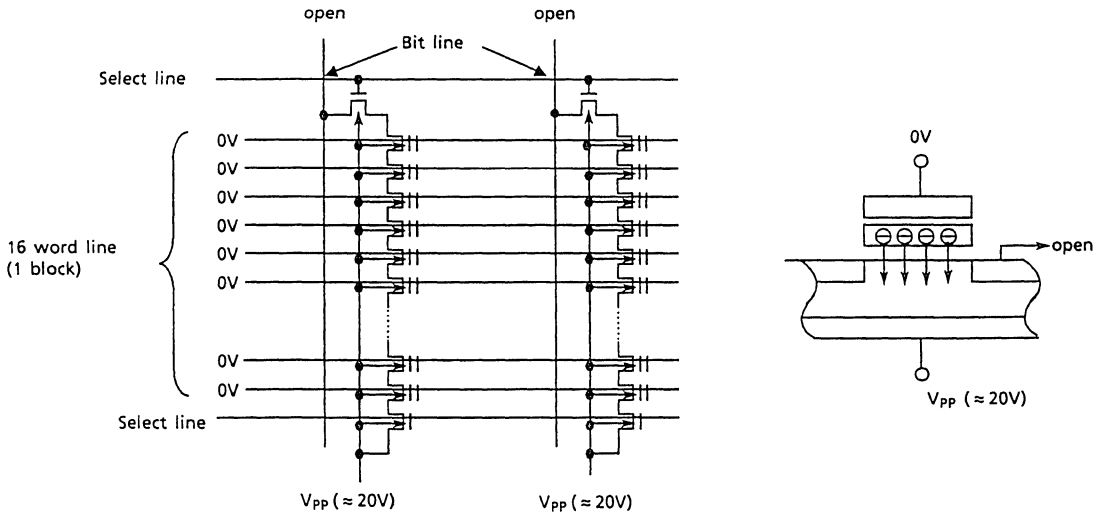


Figure 18. TC5832 Erase Device Physics

Read Operation

The state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate) after programming. Each state is indicated as the "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 19. The threshold voltage of a transistor with "0" data falls within the "plus" distribution while the threshold voltage of a transistor with "1" data falls within the "minus". The distribution band depends on the fluctuation of the transistor.

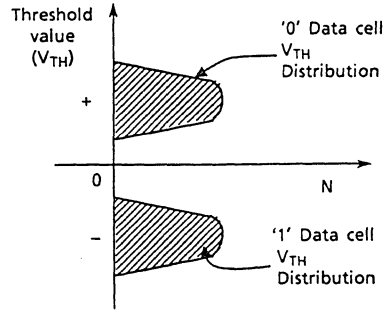


Figure 19. V_{TH} Distribution for "0" and "1" data cell

Figure 20 shows the memory cell and details of the read operation:

(1) Select lines 1 and 2 in the block including the selected page are biased at a high level so that the 16 NAND memory cell array is connected to the bit line and ground.

(2) Zero volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 20, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground while the precharged bit line tied to TR1 remains at a high level because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

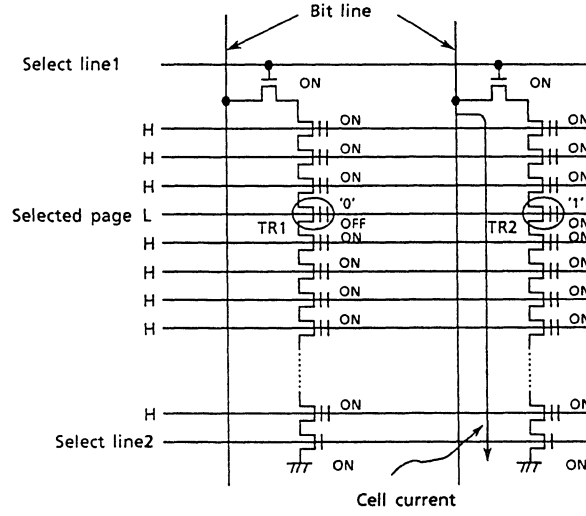


Figure 20. TC5832FT Read Device Physics

Application Notes and Comments

(1) Prohibition of unspecified commands

The operation commands are listed in Table 2. Data input as a command other than the specified commands in Table 2 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer control for "00H", "01H", "50H"

The TC5832FT has three read modes which set the destination of the pointer. Table 6 shows the destination of the pointer, and Figure 21 shows the block diagram of their operations.

Table 6. Pointer Destination

Read mode	Command	Pointer
(1)	00H	0 ~ 255
(2)	01H	256 ~ 511
(3)	50H	512 ~ 527

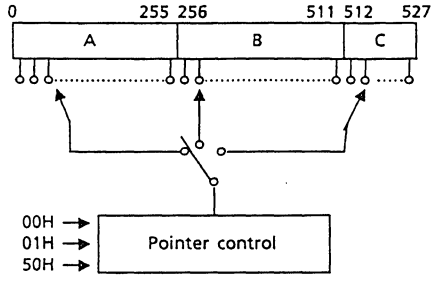
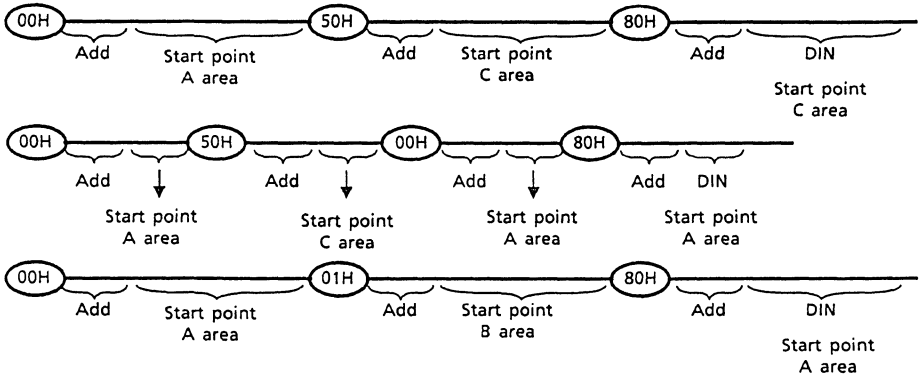


Figure 21. Pointer control

The pointer is set to region "A" by the "00H" command, to region "B" by the "01" command, and to region "C" by the "50H" command.

(Example)

The "00H" command needs to be input to set the pointer back to region "A" when the pointer control points to region "C".



For programming into region "C" only, set the start point to region "C" with the "50H" command. (To program into region C or if OP = V_{CC}, it is necessary to reset the contents of the data register to "1" by issuing the "FFH" command in advance.

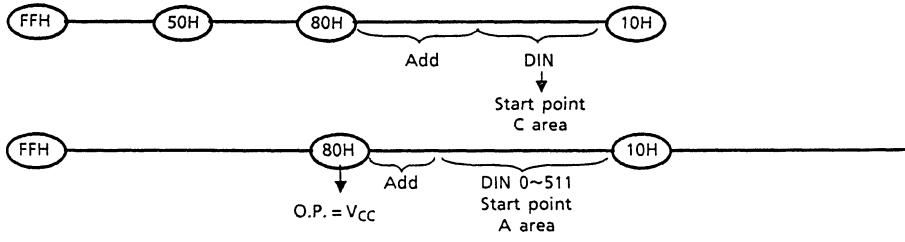


Figure 22. Example for Pointer Set

D. Non-Volatile

(3) Acceptable commands after the serial input command "80H"

Once the serial input command ("80H") is input, do not input any command other than the program execution command ("10H") or the reset command ("FFH") during programming.

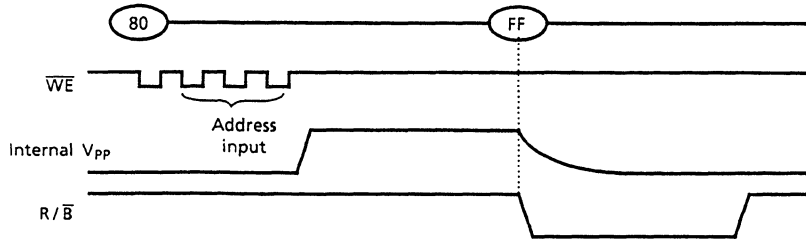
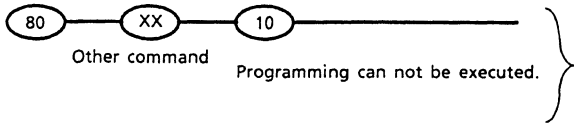


Figure 23

If a command other than "10H" or "FFH" is input, the program operation is not performed.



In this case, the reset command (FFH) command is needed.

(4) Status read during read operation

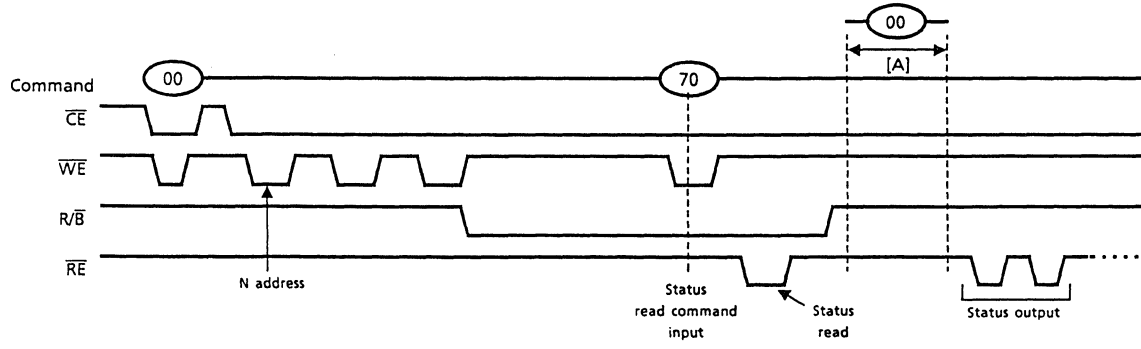


Figure 24

The device status can be read out by inputting the status read command "70H" during the read mode. Once the device is set to the status read mode after a "70H" command input, the device does not return to the read mode.

Therefore, status read during the read operation is prohibited.

However, when the read command "00H" is input during [A], the status mode is reset, and the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) Suspend command "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.

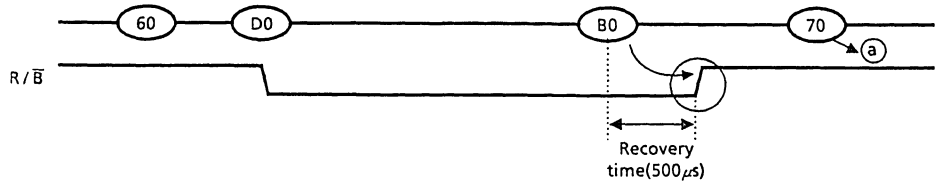


Figure 25

Although the device status changes from busy to ready after "B0H" is input, the following two cases cannot be distinguished.

-After a "B0H" command input, Busy→Ready

-After an erase operation is finished with "D0H", Busy→Ready

Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to ready.

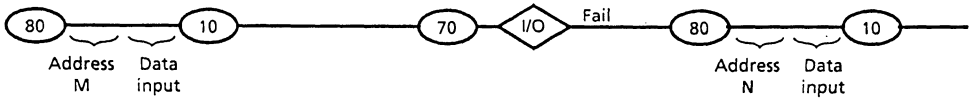
The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

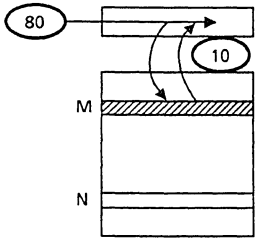
-"B0H" has been accepted: Erase operation is executed. (The device is busy.)

-"B0H" has not been accepted. (Erase operation has been completed): "D0H" command cannot be accepted. (The device is ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) Program fail





When the programming result for the page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

Figure 26

(7) Data transfer

The data in page address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e. "1" data will become "0" and "0" will be "1").

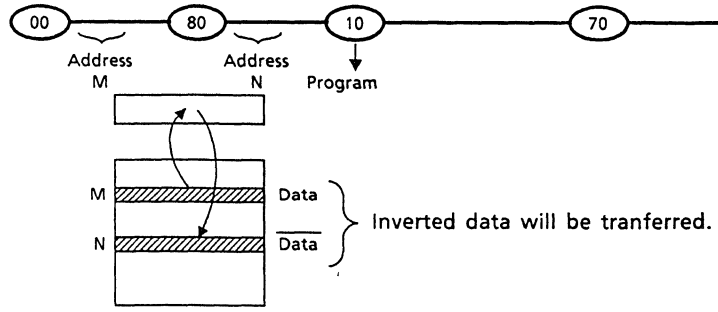
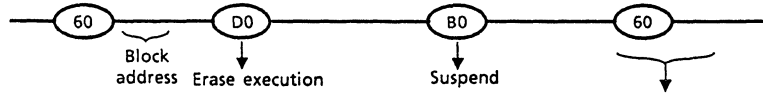


Figure 27

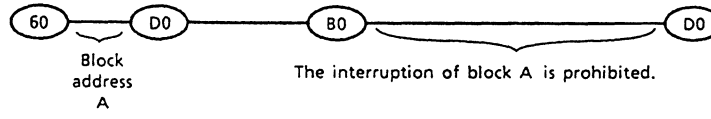
(8) Block erase after suspend command "B0H"



A block erase command is prohibited when the device has been suspended by inputting "B0H" during a block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

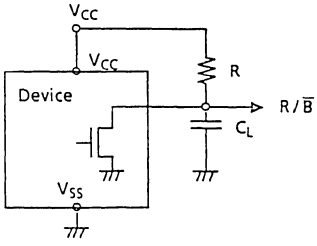
(9) Interruption of an erasing block

After a "B0H" command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



(10) R/$\overline{B}$: Termination for the Ready/Busy pin (R/$\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.



This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.

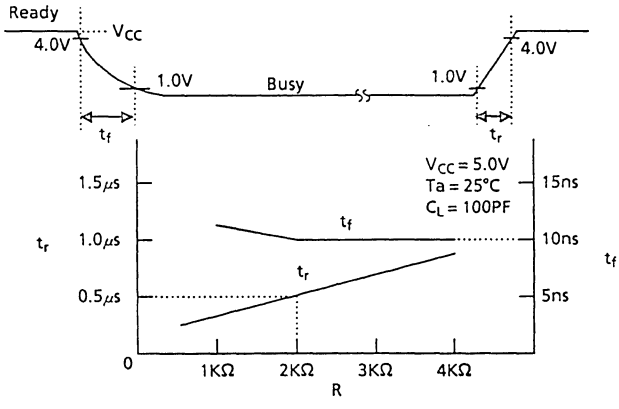


Figure 28

(11) Status After Power On

Although the device is set to read mode after power-up, the following sequence is needed because each input signal may not be stable at power on.

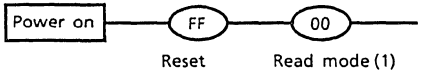


Figure 29

(12) Power On/Off Sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is necessary:

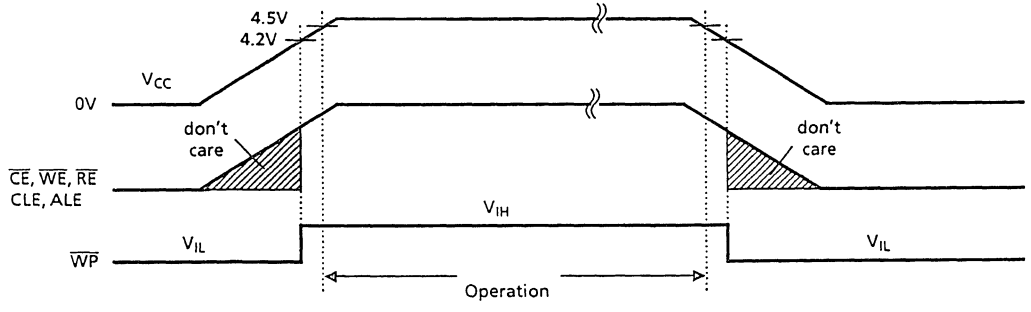


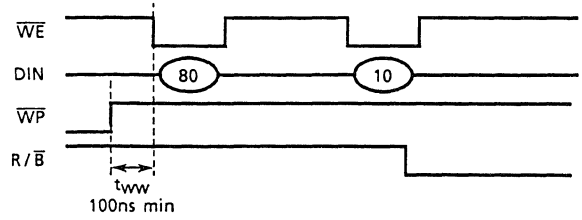
Figure 30. TC5832FT Power On/Off Sequence

D. Non-Volatile

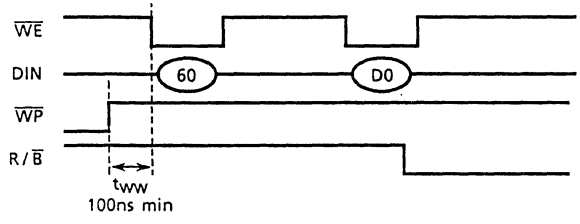
(13) Setup of $\overline{WP}$ Signal

The erase and program operations are compulsively reset when $\overline{WP}$ goes low. The following conditions must be met:

Program



Erase



(14) In the case that 4 address cycles are input

Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation:

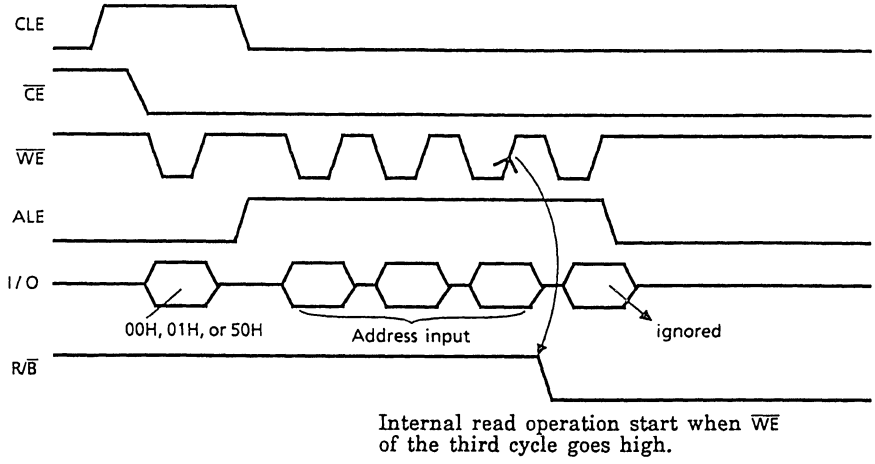


Figure 31

Program operation:

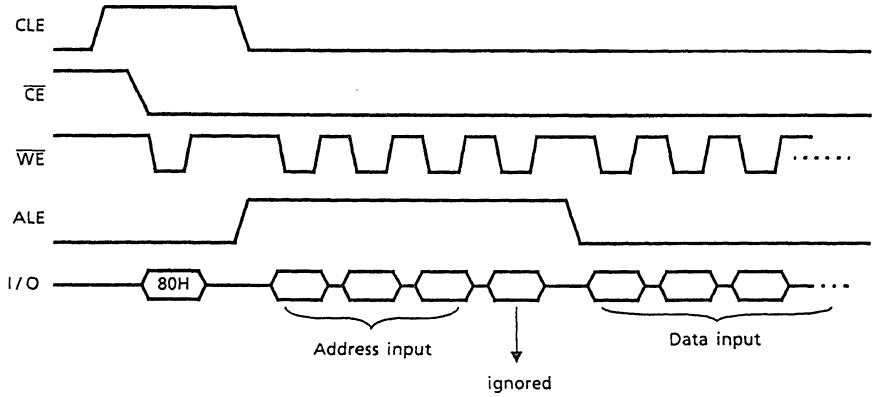


Figure 32

(15) Divided program in the same page (Partial page program)

The device allows a page to be divided into 3 segments (typically) with each page segment programmed individually as follows:

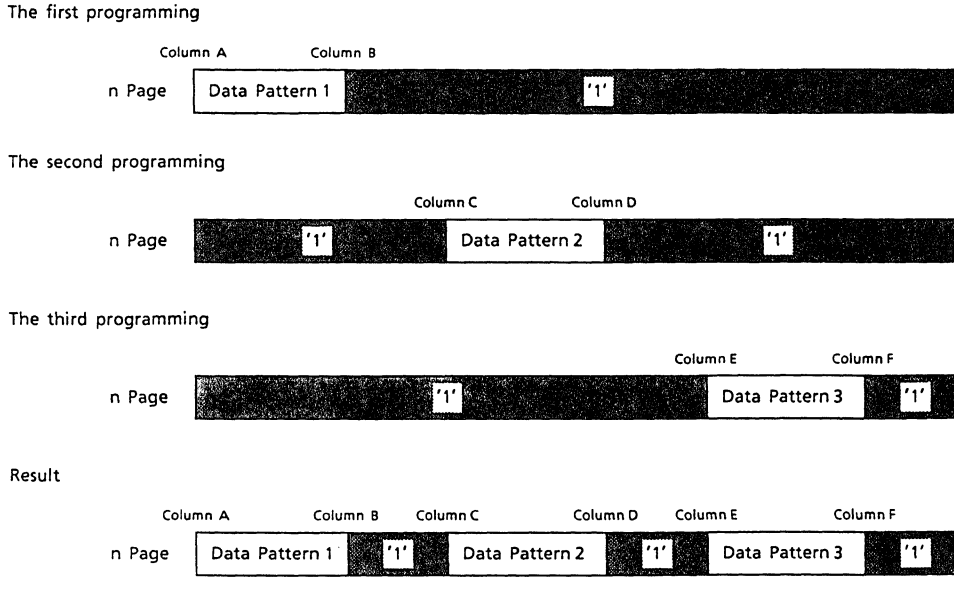
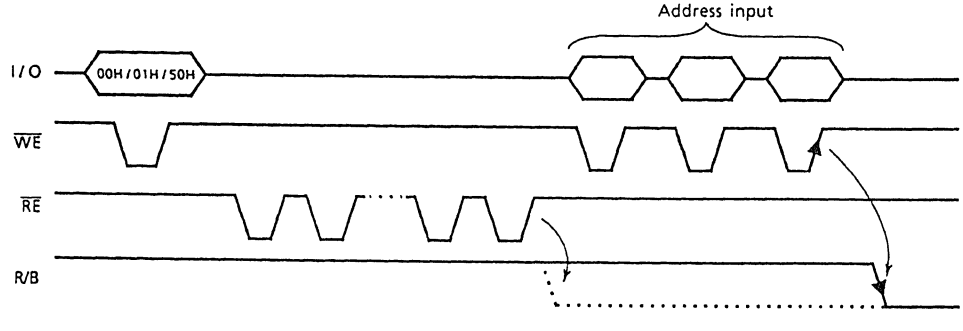


Figure 33

Note: The input data for unprogrammed or previously programmed page segments must be "1". (i.e. Mask all page bytes outside the segment to be programmed with "1" data.)

(16) $\overline{RE}$ Signal During Read

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in the read mode. Therefore, once the device is set into the read mode by the "00H", 01H" or "50H" command, the internal column address counter can be incremented by the $\overline{RE}$ clock before or after the address input. Assume that $\overline{RE}$ clocks before the address input and the pointer reaches the last column address, an internal read operation (array→register) will occur and the device will be in a busy state. (See Figure 34)



Therefore, $\overline{RE}$ clocking must occur after the address input.

Figure 34

(17) Invalid block (bad block)

The TC5832FT device contains unusable blocks. Therefore, the following issues must be recognized:

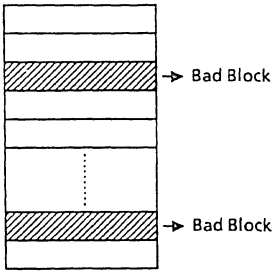


Figure 35

Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate. The number of valid blocks is as follows:

	MIN.	TYP.	MAX.	UNIT
Valid (Good) Block Number	502	508	512	Blocks

Figure 37 shows the bad block test flow.

(18) Error in program or erase operation (Fail at status read)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs.

Program

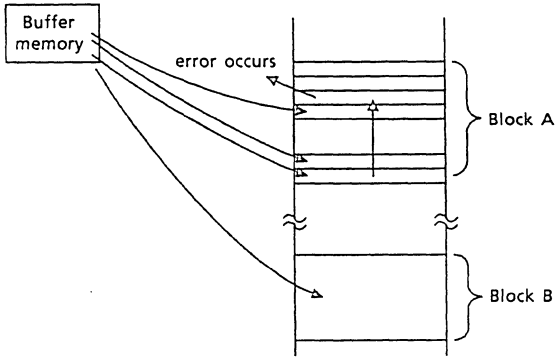


Figure 36

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad blocks" table or another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)

Bad Block Test Flow

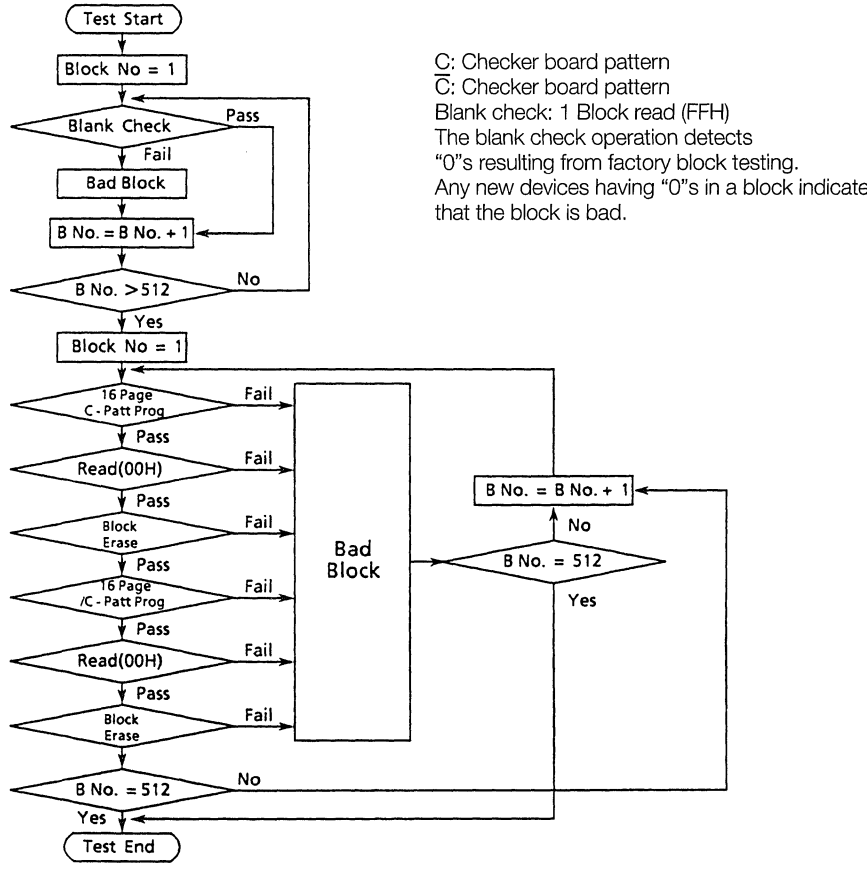
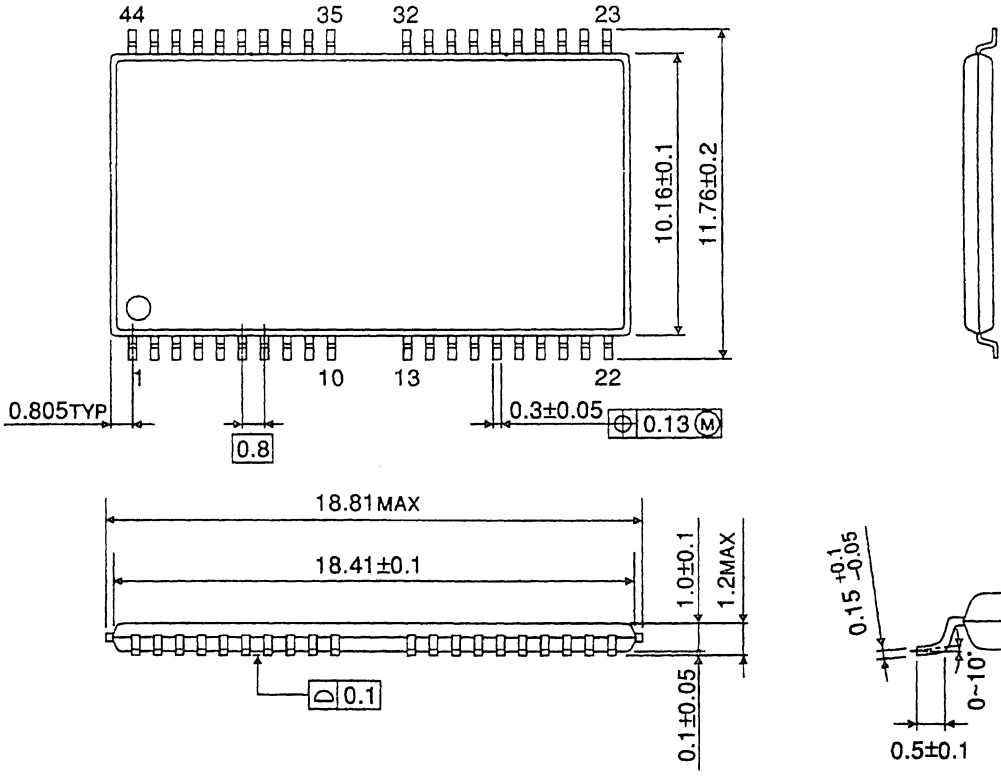


Figure 37. Bad Block Test Flow

Outline Drawings

Plastic TSOP TSOP44-P-400B Unit: mm



Weight: 0.48g (typ.)

D. Non-Volatile

Notes

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