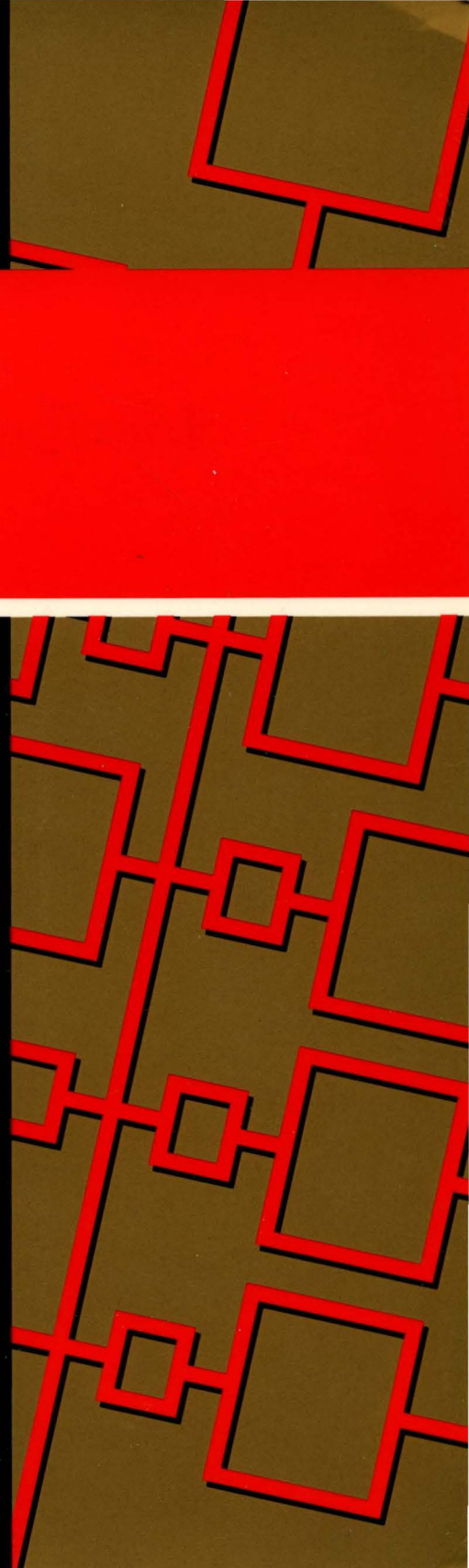
1553

1553

PRODUCT HANDBOOK



UNITED TECHNOLOGIES MICROELECTRONICS CENTER

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

1553 Product Handbook

United Technologies Microelectronics Center, Inc.
1575 Garden of the Gods Road
Colorado Springs, CO 80907

The price of this product handbook is $5.00 but it is available free of charge to qualified individuals.

Preface

Overview

At United Technologies Microelectronics Center (UTMC), we are dedicated to supplying high-reliability VLSI integrated circuits for the aerospace and defense markets. In 1986, our 280,000-square-foot manufacturing facility earned full MIL-STD-976 certification from the Defense Electronic Supply Center (DESC). This DESC certification covers all phases of our manufacturing process including circuit design and simulation, wafer fabrication, research and development, assembly, and testing to Class B military requirements.

UTMC also offers comprehensive quality assurance and reliability programs, radiation-hardened and Level S products, and foundry services specifically for military and aerospace customers.

In addition to the military-standard products discussed below, UTMC produces semicustom 1.5- and 1.2-micron CMOS gate arrays. Our UTD and rad-hard UTD-R gate array families (1.5-micron) use a patented continuous-column architecture that reduces the number of wasted transistors in the array. The 1.2-micron UTE-R family can handle up to 50,000 usable gates and has IEEE Standard 1149.1 (JTAG) boundary-scan test capability.

UTMC also offers high-reliability foundry services for its bulk CMOS processes. Our customers have a choice of either 3.0-, 1.5-, or 1.2-micron double metal CMOS technologies. The fabrication facility is DESC certified, and complete processing and testing to MIL-STD-883 Level B and Level S are available.

Demonstrating our dedication to the military and aerospace marketplace, UTMC also now offers RAD-SPEC℠ products -- "off-the-shelf" products guaranteed to meet radiation-hardness assurance levels M, D, R, and H of MIL-M-38510.

Military-Standard Products

UTMC supplies a broad range of military-standard products supporting MIL-STD-1553, 1750, 1760, DSP, and memory applications. All military products meet specifications over the full -55°C to +125°C temperature range and are screened according to specific test methods of MIL-STD-883. We also offer many devices as Standard Military Drawings.

We have the widest selection of monolithic Avionic System Division/ENASC-validated (formerly SEAFAC -- Systems Engineering Avionics Facility) MIL-STD-1553 products in the industry. The 1553B BCRT (Bus Controller/Remote Terminal) features advanced memory structures and powerful message handling. Variations of the BCRT -- the BCRTM (Monitor) and BCRTMP (Multi-Protocol) -- readily adapt to a variety of 1553 bus applications. The bus protocol family also includes the Remote Terminal Multi-Protocol (RTMP), the Remote Terminal with RAM (RTR), the 1760A Remote Terminal for Stores (RTS), the first available JAN-qualified RTI (Remote Terminal Interface), and a line of monolithic 1553A/B Transceivers which are fit- and functionally-compatible to industry-standard 631xx series transceivers.

MIL-STD-1750 products include the RISC Microprocessor, which can operate in 1750 protocol or in its native RISC mode, and its associated software tools including interactive simulator, assembler, and linker.

On the cutting edge of DSP technology, UTMC also offers the IQMAC™ (In-phase Quadrature Multiplier/Accumulator), a 32-bit, 75 MFLOP pipelined vector processor. This part uses five floating-point elements -- two multipliers and three ALUs -- to perform rapid vector calculations. The versatile IQMAC efficiently performs matrix and polynomial operations, DSP and graphics functions, and can be used for math accelerators and digital filters.

Our expanding line of military-standard products also includes a radiation-hardened memory family. The family presently includes a 8K x 8 SRAM with two levels of SEU immunity and mask-programmable 8K x 8 ROM.

RAD-SPEC Products

RAD-SPEC is UTMC's radiation-hardness specification program guaranteeing the hardness assurance levels specified in MIL-M-38510. UTMC offers RAD-SPEC semicustom and military-standard products with "off-the-shelf" pricing and delivery to simplify compliance and procurement.

Our rigorous testing and qualification guarantee the cost-effective, rad-hard products needed to consistently meet MIL-M-38510 tactical levels M and D and strategic levels R and H. Hardness levels M and D have total dose levels of 3E3 and 1E4 rads(Si) respectively and neutron fluence of 2E12 n/cm2. Levels R and H require total dose limits of 1E5 and 1E6 rads(Si) respectively and the same neutron fluence. UTMC guarantees to meet the customer's specified radiation-hardness level across the full military temperature range at cost-effective prices.

Table of Contents

UTMC recognizes the assistance in developing Section 1 provided by Al Crossgrove, Chris deLong, and Ray Turner.

Table of Contents

PREFACE

Section 1 has four parts. Part 1 presents network and communication terms the way MIL-STD-1553 uses them and describes how a 1553 network compares to other networks. Part 1 also presents the history of 1553 since its inception in 1970 and discusses its acceptance and use today. Part 2 summarizes the Standard's requirements and relates them to systems use. Parts 3 and 4 are for system, hardware, or software designers. Part 3 describes how system integration should occur, and part 4 presents guidelines and good design practices when MIL-STD-1553 is the communication means.

1.0 GENERAL DATA BUS CONCEPTS

1.1 Introduction to Data Buses

A data bus is the communication means to connect two or more users. Data refers to computer words, and the term "bus" is borrowed from the electrical power system term referring to a common connection for several circuits. A physical data bus - usually electrical conductors - is the transmission medium. A user can be either a sender or receiver of data, or both.

Parallel data buses use one physical connection for each binary bit so that all bits in a word are transmitted simultaneously. An example of a parallel data bus is the data path in a personal computer board which connects the processor chip and the memory.

In contrast, serial data buses use one physical connection to sequentially transmit bits. Therefore, serial data buses must use a decoding and timing scheme to distinguish logical ones and zeros. Serial data buses also use a control mechanism to synchronize the receiver with the sender. Synchronous means a mutually sensed clock pulse controls transmission and reception. The clock pulse may be on an additional control line dedicated to synchronizing the communication link, or the data may contain the control information. A master clock reference available to all users on a data bus is an example of a synchronous data bus. Receivers use the master clock to know when each bit begins, while senders use it to time transmissions.

Serial buses may be operated asynchronously when the transmitter and receiver use crystal-controlled clocks and start and stop information within each word of the message so the receiver knows when each word begins. Self-clocking by the receiver to its independent clock occurs word by word as the words are received. An example of a serial data bus is the telephone wire connecting two computers through modems. With one telephone connection, the connection operates asynchronously.

Manchester encoding allows the timing and data to be combined in each data bit by changing the polarity of the signal depending on whether the bit to be transmitted is a zero or a one. The receiver decodes the received signal by using its matched clock for timing bits in a word.

Electrical characteristics of the data bus include bit encoding and timing, data bus transmission rate (bits per second), and transmission waveform. Messages are multiplexed when the data bus is used for messages for multiple users. Control of a multiplexed bus is more complex because priorities for the use of the bus must exist, the address of the receiver must be added to the message, and the receiver must be able to decode and use only the messages addressed to it.

Data buses may be designed so that either each word or each message is acknowledged. Acknowledging each word has the advantage that the receiver does not need to know how many words are to be received, and the disadvantage is that the receiver cannot detect message errors. For example, the printer connected to a desktop computer uses word by word acknowledgment. Two methods are used to determine message length or completion. In the first method, transmission of a special sequence of bits different from any data indicates the start and the end of each message. In the second method, the sender includes the word count in the message and the receiver acknowledges correct receipt of the message. MIL-STD-1553 uses the latter method.

Data buses detect errors which occur during message transmission and reception so the sender can retransmit messages and the receiver can discard messages with errors. Word parity is an example of an error detection technique. Since data buses transmit messages with words of the equal length, adding a word parity bit will enable the receiver to verify the word by independently recalculating parity and comparing the result with the transmission.

The data bus protocol defines all of the actions of both receiver and sender including what to do when messages have bit and word errors. Protocol also includes: (1) message and word formats including destination address and message identification; (2) method of message acknowledgement; and (3) special messages that are related only to managing the data bus, such as which users have authority to transmit messages and which users are ready to receive.

MIL-STD-1553 defines a serial asynchronous data bus on which the messages are multiplexed among users. The transmission medium is a twisted wire cable. The Standard specifies all of the electrical characteristics of the receivers, transmitters, and cable. It also defines the complete protocol but makes the use of many parts optional. To initiate all messages, the Standard requires a centralized control bus (as opposed to either a distributed or autonomous controlled bus). Figure 1 shows an example of a MIL-STD-1553 data bus system.

The U.S. Department of Defense (DoD) requires the use of this standard multiplexed data bus on all military airplanes and helicopters. It is also used on ships and land vehicles.

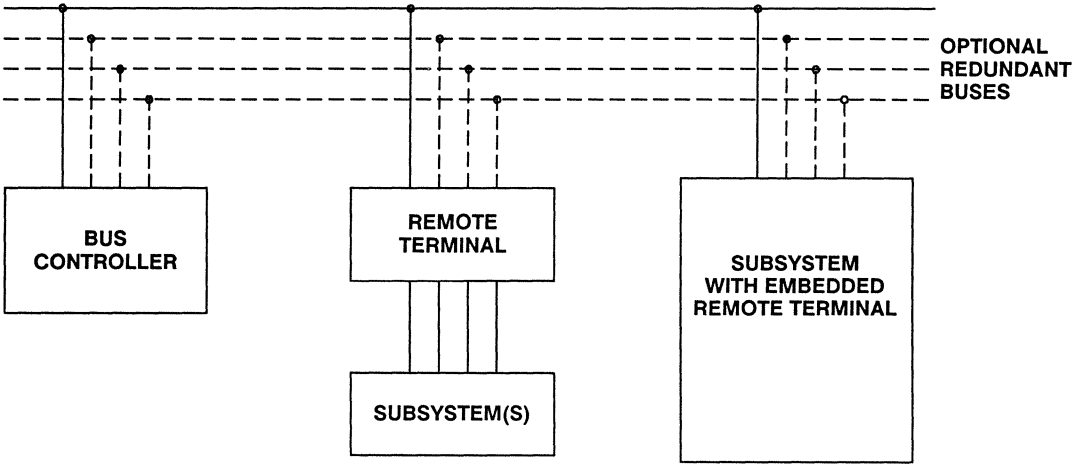


Figure 1. MIL-STD-1553 Data Bus System Architecture

1.2 Historical Need for a Bus

From about 1965 to 1970, airplane designers incorporated digital computers and multi-wire digital links to supplement or replace analog systems in airplanes. Three well-known programs provided the motivation for development of a data bus.

In late 1969, the U.S Air Force (USAF) released its procurement request for the B-1A airplane. The request included a requirement for a crew capsule which could be separated from the aircraft during an aircraft emergency. Reducing the number of electrical connections between the capsule and the aircraft body gave great impetus to designing a serial data link. For B-1A, this link was a twisted pair of wires, operating at a clock rate of one million bits per second, with a maximum message length of 512 words.

From 1970 to 1972, designers of the space shuttle avionics also created a serial data bus to interconnect flight-critical computers and subsystems using multiple buses primarily to facilitate redundant communication.

The F-15, which became operational in 1975, used a synchronous serial link to connect avionics subsystems to the mission computer to provide an extension of the computer input/output interface to remote electronics. This design used a one million cycles per second (1 MHz) separate clock line, and a maximum message length of 15 words.

In summary, the advantages of using multiplexed data buses as viewed in 1970-1975 included performance improvements made possible by the distribution of data from dissimilar sources, weight saving, ease of achieving communication redundancy, and flexibility of integration. Many engineers in industry recognized these advantages and developed prototype systems, but the USAF and the U.S. Navy (USN) took the lead in encouraging investigation to determine the best design for aircraft.

1.3 Development of MIL-STD-1553 Data Bus as a Standard

In 1968, the Society of Automotive Engineers (SAE) Aerospace Branch in cooperation with the USN formed a task group to generate a military standard which would specify a data bus system to control electrical power (Control Group, Electrical Power, General Specification for, MIL-P-81883). The task group consisted of industry and military designers. Common features were specified and areas of disagreement were delegated to "slash sheets," which, when completed, constituted a complete standard. Because of the interest in multiplexing on the F-15, B-1A, and space shuttle, each with unique designs, the industry looked for a common approach. Through this effort, the USAF developed and published MIL-STD-1553 in 1973 for use on the F-16 program.

During the next two years, industry, the USAF, and the USN reviewed many drafts of potential revisions to the Standard. In 1975, by direction of the DoD and with the support of industry, the USN, the USAF, and the Army published a coordinated revision A to the Standard. Because of problems and difficulties with revision A, industry and the military formed another SAE task group in 1976 to propose further changes.

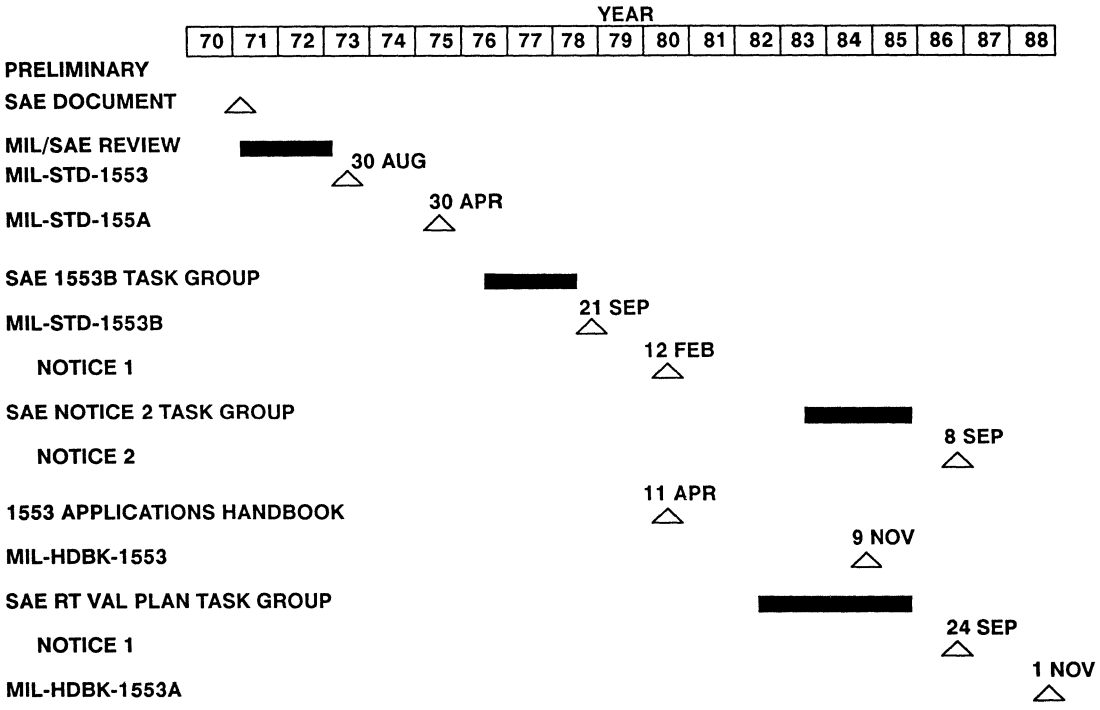


Figure 2. History of MIL-STD-1553

After a complete rewrite of the "A" document, the SAE task group worked with the USAF, USN, and Army to produce the DoD-released MIL-STD-1553B in September 1978. The USAF further limited MIL-STD-1553 by creating USAF Notice 1 for the Standard in February 1980. After several years, the SAE again worked with the DoD tri-service group to generate the most recent 1553B Notice 2 for DoD usage. International standards incorporate or reference MIL-STD-1553B without notices. Figure 2 illustrates the key MIL-STD-1553 historical events.

1.4 The Impact of MIL-STD-1553B

All three DoD services require MIL-STD-1553B as the Standard for inter- and intra-subsystem communication. The USAF established a "Form-Fit-Function" concept for avionic equipment common to more than one airplane beginning with the standard inertial navigation system. The signal interface is MIL-STD-1553. Currently, many such boxes including radios and air data computers use MIL-STD-1553 interfaces. Avionic upgrades to existing airplanes with analog systems always include the addition of MIL-STD-1553 data buses to incorporate the many existing subsystems with MIL-STD-1553 interfaces. MIL-STD-1553 is the main communication link between aircraft and weapons, as required by MIL-STD-1760. Today's expendable stores and captive-carry pods such as infrared sensors and electronic warfare components that conform to MIL-STD-1760 will have at least one MIL-STD-1553 interface. Complex air-to-ground and air-to-air missiles also have their internal avionics interconnected with MIL-STD-1553. The Army uses MIL-STD-1553 in helicopters and tanks. The USN uses MIL-STD-1553 in surface ships and submarines.

Originally used only in mission avionics, MIL-STD-1553 is now used in flight critical avionics (such a terrain following subsystems), flight control, weapons, electrical power control, and propulsion control.

MIL-STD-1553 is commonly used outside the U.S. The United Kingdom (U.K.) Ministry of Defence and NATO have adopted MIL-STD-1553 as a standard. The NATO alliance countries as well as others (e.g., Israel) produce subsystems and weapons with MIL-STD-1553 interfaces.

MIL-STD-1553 has become easier for the designer to use. Twenty years ago, a MIL-STD-1553 bus interface unit (BIU) required significant design and production effort. Now, MIL-STD-1553 use resembles

microcomputer interfacing. Minicomputers and desktop personal computers used in ground laboratories also use MIL-STD-1553 interfaces produced by many companies in the U.S., U.K., and Europe.

MIL-STD-1553 is the most successful and most widely used standard of its type. International standardization is achieved by MIL-STD-1553B (without Notices) as part of or referenced by NATO STANAG 3838, ASCC Standard 50/2 and UK DEF STAN 00-18 (Part 2)/Issue 1.

2.0 Understanding MIL-STD-1553

MIL-STD-1553 is designed for high integrity data exchanges between unattended equipment in military airplanes, ships, and land vehicles. The messages are highly repetitive, and their content and periodicity are all preplanned. Computers or digital logic control message execution include what action takes place when errors occur. Each piece of equipment contains a MIL-STD-1553 communication terminal operating from power within the equipment and providing the equipment data interface. The Standard calls the communication terminals Bus Controller (BC), Remote Terminal (RT), and Monitor (M).

The Standard specifies the terminal's exact electrical characteristics. The terminal hardware must operate exactly the way the Standard has defined it.

The Standard defines all of the message protocols that may be used. Unlike the electrical requirements, the system designer may choose to use any message protocol, as long as it is a complete protocol. The Standard does not define the many ways BCs, RTs, and Ms can be interconnected, except that: (a) the number of RTs on a single data bus cannot exceed the maximum number of addresses, and (b) the BC is the single controller of all messages on the bus.

2.1 Functions of Bus Controllers, Remote Terminals, and Monitors

This section provides an introduction to the most common uses of 1553 terminals in systems today. It provides a frame of reference for the discussion of the 1553 protocol that follows.

All messages and their transmission rates are pre-established during system design. Since the BC is the only controller, the BC only needs to follow instructions stored in memory to control communication and to monitor and service message requests. The BC also contains error analysis and decision logic to deal with all errors that can occur in the communication system. Thus, the BC's operation is well ordered, pre-established at design, and specific for each step necessary to achieve data communication and control. These operations are unique for their application. BC hardware design should have sufficient flexibility to allow BC use in many applications.

In contrast to the BC, the RT usually has specific functions and will use the data bus (under control of the BC) for bidirectional communications with other RTs or the BC as it supports system operation. For example, an inertial navigation system is an RT that provides position and acceleration data to the flight control computer and to crew instruments. The RT's primary roles are to be an interface for the equipment function within it and to communicate with other equipment connected to the same data bus.

The M is the only other electronic device used in MIL-STD-1553, and it has a limited application. The M has the features of both an RT and BC, except that it cannot transmit information on the bus. It can receive and store every message addressed to every terminal. Because this capability is usually impractical, the designer specifies which messages addressed to specific terminals the M will store. The design may include the ability to use loadable programmed data to establish the selection of the M's capability at power-on. The M's most common use is flight test instrumentation to verify data bus system performance.

2.2 MIL-STD-1553 Message Formats

The Standard defines two types of message formats: non-broadcast or "information transfer formats" and broadcast or "broadcast information transfer formats." Figures 3 and 4 show these formats, which are reproduced from figures 6 and 7 respectively of the Standard. Both information transfer formats are divided into data communication messages and communication management messages. Each message uses only standardized word types that are described in later sections.

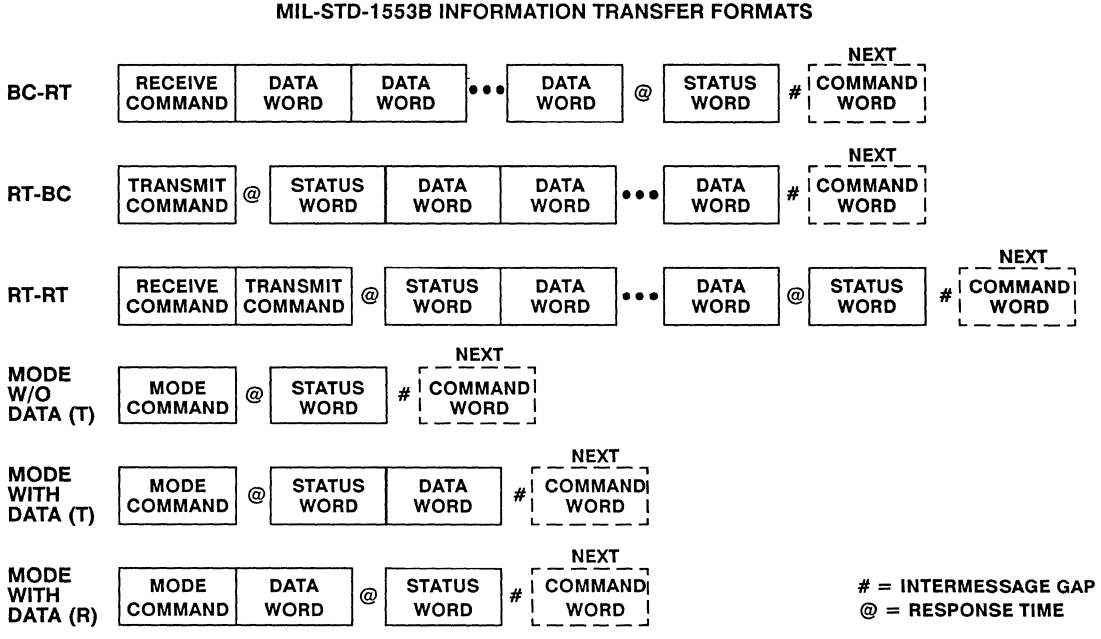


Figure 3. Information Transfer Formats

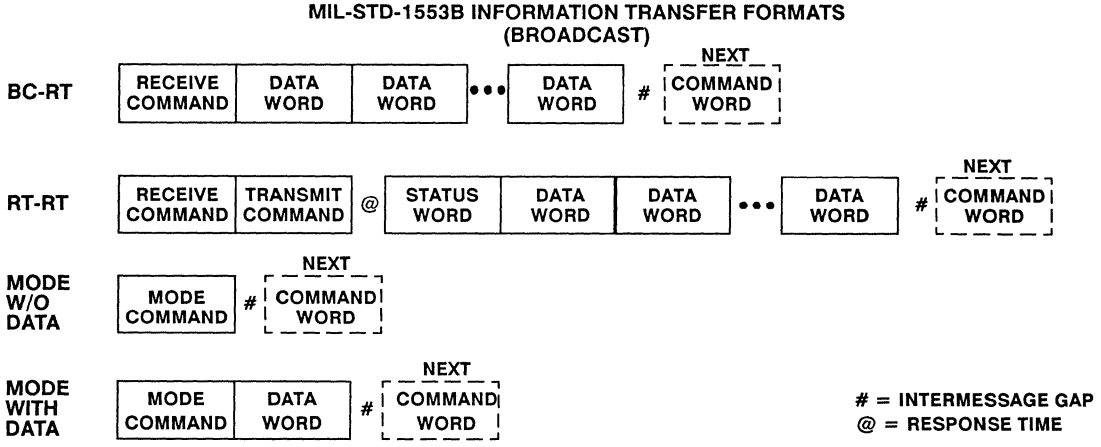


Figure 4. Broadcast Information Transfer Formats

Figures 3 and 4 show that all message formats begin with one or two command words that contain the RT's address number, message identification field number (subaddress), word count, and a one-bit field to indicate whether the data words are to be transmitted or received. RTs acknowledge message reception by transmitting a status word if they received an error free non-broadcasted message. Since RTs must respond within the response time the Standard allows, the response time is part of the message format. The status word contains the RT's address and additional information conveyed by setting the status word bits from logic zero to logic one.

The Standard also defines communication management messages that are identified by a specific message identification number in the message identification field. The communication management message number is the word count number field. The Standard calls these mode commands. The Standard defines mode commands for both non-broadcast and broadcast formats. (Section 2.6 describes all mode codes and their uses in a typical system.)

The Standard defines only three types of words: command word, status word, and data word. Figures 3 and 4 show the order of these words in messages. The non-broadcast message formats are used only for communication between two terminals. In contrast, broadcast message formats allow either a BC or an RT to transmit to all other terminals under the BC's direction. One of the terminal addresses is reserved for use as the broadcast address for all terminals.

As shown in both figures 3 and 4, each message must be separated in time from the next by a minimum intermessage gap of at least two microseconds. This delay allows the analog bus to "quiet" prior to next message transmission. Typical intermessage gaps on computer-based BCs range from 30 to 60 microseconds.

2.2.1 Non-Broadcast Message Formats

In non-broadcast formats, only six message types are allowed, and the use of any or all of them is optional. Three of these messages are for normal data communication, and three are for communication management. For normal non-broadcast communication management, the BC issues commands to: (a) require an RT to transmit a message to the BC (RT-to-BC); (b) originate a message to an RT (BC-to-RT); (c) require one RT to transmit a message, while directing another RT to receive it (RT-to-RT). For non-broadcast communication management, the BC issues mode commands to: (a) command one RT to perform the operation the mode indicates and to transmit its status word and a single data word (RT-to-BC with data word); (b) command one RT to transmit only its status word (RT-to-BC without data word) and perform the mode operation; and (c) command one RT to receive one data word, transmit its status word, and perform the mode operation.

Each message format requires the RT to transmit its status word so the BC can validate that the RT received the message. The message formats are basically "closed loop" because the BC receives confirmation that the message was received when the BC receives the RT status word. The RT status word bits provide additional information on the general maintenance condition of the RT and its subsystem and allow the RT to request service to transmit pre-planned aperiodic data.

The Standard defines word and message validation criteria. If the terminal hardware detects either an invalid word or a transmission discontinuity, it considers the word and message invalid. This requirement applies to all terminals. The Standard requires the RT to suppress the status word if the message validation criteria is not met or if the number of words received does not match the word count in the command word. In both of these cases, the RT sets but does not transmit the Message Error bit in the status word. The BC easily detects the message failure if, after waiting the maximum RT response time, it does not receive the status word. Although the Standard does not impose any error handling requirements, the BC should be programmed to handle such error occurrences. The system designer must decide what error response the system will perform for each pre-programmed message.

2.2.1.1 BC-to-RT Receive Message

The BC-to-RT receive message occurs when the BC transmits a command word with a unique RT address followed by 1 to 32 contiguous data words as specified by the command word. The RT recognizes the command word, its own unique address, and the word count, and starts receiving data words for validation and use. After the RT receives a complete message and the response time elapses, the RT will transmit its status word and indicate that it received a valid message. The BC examines the returning status word and bases its actions on the RT's status bits. Since the RT is returning the status word, the BC is assured of message reception validation. If a valid complete message was not received, the RT will suppress the transmission of its status word, and the BC will wait only the specified response time before originating another message. The next message may be the error handling message to resolve the problem or a retry of the original message. See figure 3.

2.2.1.2 BC-to-RT Transmit Message

The BC performs the BC-to-RT transmit message when it desires data from a unique RT. After the response time, the unique RT selects the data requested based on the command word subaddress and transmits its status word followed by the number of data words the BC specified in the command word. The BC receives the unique RT's status word, bases its actions on the RT's status bits, and stores the incoming data words. Message validation is accomplished by examining the RT's status word, performing the message validation the Standard requires, and verifying that the number of data words received agrees with the word count in the command word. See figure 3.

2.2.1.3 RT-to-RT Message
The BC can direct one RT to transmit data and another RT to receive the data. The receive command comes first and prepares the receiving RT for data words. The next command word, a transmit command, causes another RT (based on address) to transmit. As in the BC-to-RT transmit command, the transmitting RT sends its status word followed by the commanded number of contiguous data words. The receiving RT validates message correctness prior to transmitting its status word. The BC then must review and act accordingly on both the transmitting and the receiving status words to complete the message. The receipt of both status words results in the verification of individual message completion. See figure 3.

2.2.1.4 Non-Broadcast Mode Command Messages
The BC can use three different mode command message formats to manage unique RT problems. The first format commands a unique RT to accomplish the action specified and transmit its status word after the appropriate response time. The second and third formats allow the BC to request the RT to transmit its status word and a data word or to receive a command word and one contiguous data word prior to the RT transmitting its status word. A description of the BC's use of the mode codes to manage the system and resolve problems with RTs follows the message and word descriptions in section 2.6.

2.2.2 Broadcast Message Formats
The broadcast messages allow a single terminal to transmit a message to all terminals. The Standard defines four broadcast messages: BC to all RTs, single RT to all RTs, BC mode command to all RTs, and BC mode command with data word to all RTs.

2.2.2.1 BC Broadcast to RTs
The BC-to-RTs message is a transmission from the BC to all RTs which have the ability to receive a broadcast message. (The Standard does not require RTs to have the capability to receive a broadcast message.) The command word contains the reserved address for broadcast. Following the command word are from 1 to 32 data words as specified in the command word data count field. The data words tell the RTs the type of message being transmitted and the length of message. If the message is validated, the RTs will use the broadcasted data. With broadcast messages, transmission of the status word to the BC is not permitted thereby avoiding status word collisions and unreadable communication on the bus. If the BC must verify message reception to one or all RTs, it may transmit a non-broadcast mode command message to any RT individually to determine the status of the previous message reception.

2.2.2.2 RT Broadcast to RTs
The BC uses two contiguous command words to command a single RT-to-all-RTs message. The first command word contains the broadcast address to receive a message. The second command word contains the address of a unique RT. The BC uses the second command word to direct the unique RT to transmit a message to all receiving RTs. The message states the required number of data words. Note that the receiving RTs are waiting for data words.

The unique RT prepares the commanded message during a response time. When the response time ends, the unique RT transmits a status word followed by the commanded number of data words to all receiving RTs. Because the status word contains the address of the transmitting RT, the receiving RTs ignore it. The receiving RTs do accept the data words that follow the status word. They decode the data words and use the data if it is error free. The receiving RTs set their status words to indicate broadcast reception (message completion) but do not automatically transmit their status words. To verify message completion, the BC requests each RT to transmit its status word using a mode command. The BC examines the transmitting RT's status word and waits for message completion before beginning the next message. See figure 4.

2.2.2.3 Broadcast Mode Command Messages
The BC uses two broadcast mode code command message formats to manage RT problems. The BC can transmit seven broadcast mode commands without a data word to all RTs: Synchronize, Initiate Self-Test, Transmitter Shutdown, Override Transmitter Shutdown, Inhibit Terminal Flag, and Override Inhibit Terminal Flag. (See section 2.6 for a description of the meaning of mode codes.) Three additional broadcast mode command formats are transmitted with a data word: Synchronize With Data Word, Selected Transmitter Shutdown, and Override Selected Transmitter Shutdown. The data word contains information RTs need to execute these commands. The designer, not the Standard, defines these data words.

The RT receives the mode command and performs the required function if it is designed to support broadcast messages and has implemented the optional mode commands as part of its design. If the RT does not have the broadcast design capability, it will not accept the RT address and will continue to operate as if the command was to another RT.

2.3 Note on MIL-STD-1553B Notice 2
This note distinguishes the BC and RT capability dictated by Notice 2 from optional use and prohibited use. (Notice 2 completely replaces Notice 1.)

Since MIL-STD-1553 allows optional use of all the message formats and mode commands, many early BC and RT designs did not include the capability to decode some or all of the mode codes or to respond to some of the message formats. Many early RT designs did not have the capability to implement the RT-to-RT message. For these designs, the designer selected the message formats and mode commands required only for the specific application.

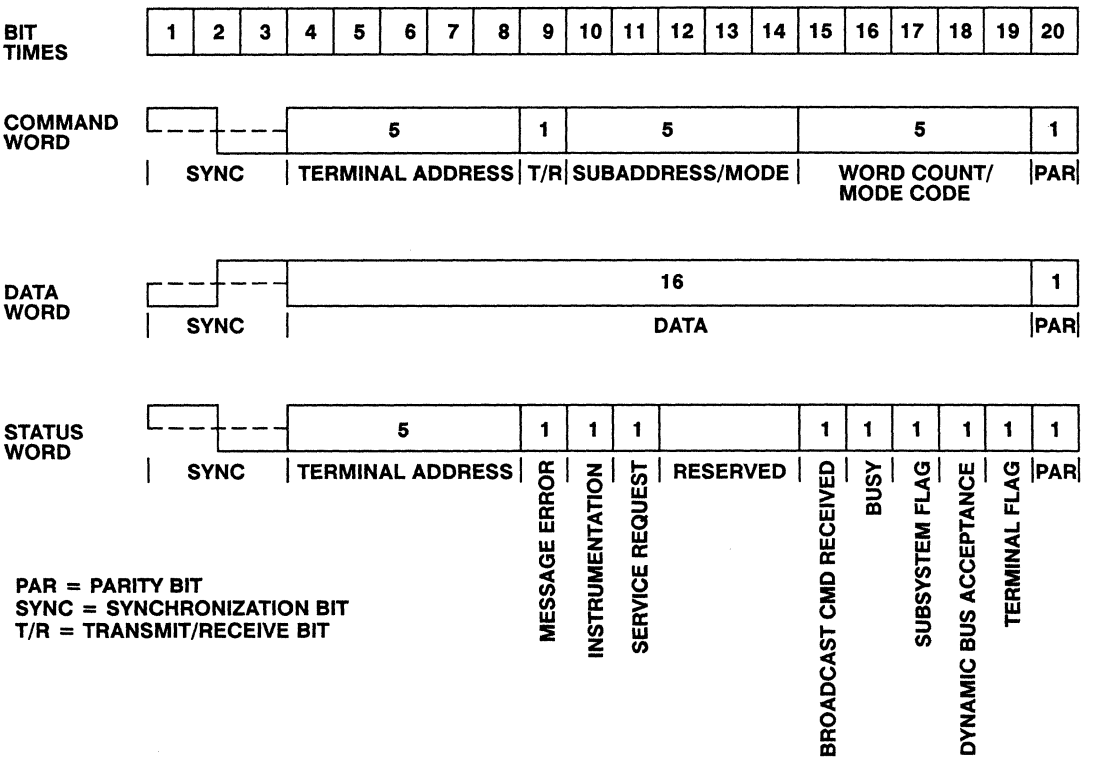


Figure 5. MIL-STD-1553B Word Formats

Notice 2 clarified that BCs and RTs must have all non-broadcast message formats. RTs, however, are not required to implement non-broadcast mode commands with data words if such mode commands are not part of the RT's design requirements. Notice 2 also defined a required minimum set of mode codes that the RT's design must include. The RT may or may not use all of the mode codes. In Notice 2, the USAF also mandated that some of the optional capabilities of MIL-STD-1553B never be used in airplanes.

2.4 Command, Status, and Data Words

All bus data is transmitted as 20-bit words, as figure 5 shows. The Standard identifies and specifies only three types of words: command, status, and data.

The time interval of three bits serves as a combination of word identification and synchronization (sync). The sync pattern, defined by the Standard, is unique and is not the same as the waveform of data bits. The two parts of the sync are each 1.5 times a one-bit time, transmitted either as a positive voltage waveform followed by negative voltage waveform or vice-versa. The sync order identifies the words: the command and status words have the positive waveform first while the data word has negative waveform first. Word parity is also part of the word. The 20 bits are, in order: 3 bit times for the sync, 16 bit times for data, and 1 bit time for parity.

2.4.1 Command Word

The Standard uses these terms for the command word fields:

Bit Times	Number of Bits	1553 Name
1-3	3	Sync
4-8	5	RT address
9	1	T/R bit
10-14	5	Subaddress/Mode
15-19	5	Data word count/Mode
20	1	Parity

The command and status words use the same sync pattern. The data word uses the inverse of the command and status pattern. However, since the BC always issues commands to RTs, the BC knows which RT it has commanded. The BC compares the RT address in its command word to the address in the RT's status word to validate that the commanded RT is transmitting its status

word. This address comparison is always unambiguous because the BC does not have a commanded address.

RTs use the sync pattern to determine if the word is a command. If it is, the RT will examine the address for its own unique address number or the broadcast address. Status words transmitted on the bus will always have the address of the transmitting RT. Therefore, the RT can always determine if a word with a command/status sync is a command word to which it must respond. The RT can always separate command and status words from each other and from data words.

If the command word is addressed to a particular RT and the RT determines that it is being commanded, it decodes the T/R bit. A logic one indicates the RT will transmit data while logic zero indicates it will receive data.

Finally, the RT decodes the subaddress/mode field. First the RT determines if a mode command is being transmitted and if it is, the RT interprets the word count/mode field as a mode code. If it is not a mode command, the RT interprets the subaddress/mode field as the message identification and the word count/mode field as the number of words to be received or transmitted, depending on the T/R bit.

The last bit in the command word is the parity bit. All 1553 words end with the parity bit set to "odd." Odd parity means there is an odd number of logic ones in the word (16 data bits plus the parity bit). Odd parity is accomplished by counting the logic ones in the word and setting the parity bit to one or zero to achieve an "odd" number of ones.

2.4.2 Note on Subaddress Assignment

The Standard reserves two subaddresses for mode command identification. A maximum of 30 transmit and 30 receive messages can be assigned to subaddresses. Each RT must be designed to store its assigned receive messages and construct its required transmit messages. The receive and transmit messages are assigned to the receiving and transmitting subaddresses, respectively. If more than 30 subaddresses are needed, mode code messages can be used to switch from one set of 30 transmit/receive subaddresses to another set.

MIL-STD-1553 does not define or restrict the subaddress-to-message assignment. The only exception is Notice 2 requires a receive and transmit subaddress be dedicated to a wrap-around message equal in length to the longest message the RT receives or transmits. The Notice suggests, but does not mandate, that this dedicated subaddress be 30. The wrap-around message would be received from the BC, unaltered by the RT, and transmitted upon BC command.

2.4.3 Status Word

The Standard uses these terms for the status word fields:

Bit Times	Number of Bits	1553 Name
1-3	3	Sync
4-8	5	RT address
9	1	Message error
10	1	Instrumentation
11	1	Service request
12-14	3	Reserved
15	1	Broadcast command received
16	1	Busy
17	1	Subsystem flag
18	1	Dynamic bus control acceptance
19	1	Terminal flag
20	1	Parity

The RT transmits a status word after receiving a command with or without a data word (or words) from the BC unless the address in the command word is the broadcast address. The status word sync is identical to the command word sync and precedes the RT address. Each RT has a unique address and may also have a broadcast address which is never transmitted in the status word. Notice 2 requires that an address change be possible by external connector without physical modification of the RT and that the RT validate its address at power-on as a minimum. Notice 2 also requires that no single failure cause an RT to validate a false address. This requirement is usually accomplished by adding a sixth interface, which is parity on the five address lines and itself and is part of the wire bundle just like the address lines. Even though this is a Notice 2 requirement, it has general application to all MIL-STD-1553B RTs and is a de facto method of defining an RT's address. The remainder of the status word, excluding the common approach for parity, contains specific status bits. Each bit has a single application and is used to convey information that generally solicits standard responses from the BC.

The paragraphs below describe how a typical system uses status bits and BC responses. Many of the BC responses are associated with the mode commands described in section 2.6.

The Message Error bit is set in an RT when the incoming message has failed the Standard's word or message validation requirements. Since the status word is not transmitted for message errors or broadcast messages, the BC can only observe a message error when the mode code Transmit Status

or Transmit Last Command is sent to the RT. The only exception to this operation occurs with an RT that has been designed with the illegal command monitor option. If this type of RT receives a command that it is not designed to receive, the RT will respond with a status word with the Message Error bit set.

The Instrumentation bit is always set to zero to allow the same bit in the command word to be set to one, thus allowing a Monitor to determine status versus command words. If the one is used in the command word, mode codes are identified by all ones and subaddresses are limited to 15. If the one is not used in the command word, mode commands are usually all zeros, and 30 receive and transmit subaddresses are available.

The Service Request bit is set in the status word when the RT wants to transmit an aperiodic message. As described in section 2.6, the BC uses the Transmit Vector mode command to determine the desired transmission.

The Broadcast Command Receive bit is set when the RT has received a valid broadcast message. Since the RT is required to suppress (not transmit) the status word on broadcast messages, the BC can validate message reception using the Transmit Status or Transmit Last Command mode code.

The Busy bit indicates to the BC that the RT is unable to receive or transmit valid data with its subsystem interface. If the BC commands the RT to receive data when it is in a busy condition, the RT cannot use the received data. If the BC commands the RT to transmit when it is busy, the RT will transmit its status word only with the Busy bit set. RTs should be designed to minimize the time when they are busy. During initialization, however, an RT is often busy until it completes power-up. Busy operation at other times is usually unnecessary.

The Subsystem Flag alerts the BC of a subsystem problem. Subsystem error handling software is required to manage this problem. Thus, the BC will pass this information to application software to deal with the aspects of a failed subsystem on the bus.

The Dynamic Bus Acceptance bit is discussed in section 2.6. It is associated with the Dynamic Bus Control mode command. The new BC sets this bit to tell the existing BC to stop operating in the BC mode and revert to an RT or Monitor mode.

The Terminal Flag bit indicates an RT hardware failure. This failure may not prevent the RT from continuing to operate due to its redundancy. Several mode codes such as Initiate Self-Test and/or Transmit BIT can analyze the problem's severity. Once failure analysis is complete, the BC can use the Inhibit Terminal Flag mode code to suppress future reporting. Then, with subsequent communications, the BC can continue to use a non-fatal failure in an RT without re-examining the failure.

2.4.4 Data Word

The data word contains the three-bit inverse sync pattern of the command and status words, followed by 16 bits of user-defined data, ending in an "odd" parity bit. MIL-STD-1553 requires the most significant bit be transmitted first. It does not require that a logic one or zero represent any specific meaning, such as "on" or "off."

2.5 Note on Probability of Undetected Errors

MIL-STD-1553's noise rejection capability has been satisfactory for almost any application. Table II of MIL-STD-1553B indicates that an RT can have only one error after receiving 52 million words. This translates to approximately one error every 33 minutes for BC-to-RT messages of 10 words transmitted at 1667 messages per second. Ten-word messages transmitted at this rate use approximately one-half the capacity of the data bus.

If the system uses non-broadcast messages or verifies broadcast messages using a mode command, the system will detect one error per 33 minutes and will activate the system error correction to resolve the message error. Therefore, the chance of an error going undetected is approximately 10E21 bits/error, yielding more than a lifetime before an undetected error can occur. If data integrity requirements exceed this number, then the designer can add error correction encoding techniques to each message. Since the designer controls all data definition methods, the complexity of data encoding is user dependent.

2.6 Meaning of the Command Word Mode Codes

The following table defines all of the mode codes in MIL-STD-1553B. The first 16 codes are not transmitted with a data word, but the last 16 are transmitted with a data word. It is inappropriate to broadcast mode codes requiring RT data word responses because multiple RT transmissions cause bus crashes. Dynamic Bus Control broadcast is also inappropriate. For mode codes 17 to 31,

the T/R bit is important because it defines whether the BC or the RT transmits the associated data word.

T/R Bit	Mode Code	Function	Data Word	Broad-cast?
1	0	Dynamic bus control	No	No
1	1	Synchronize	No	Yes
1	2	Transmit status word	No	No
1	3	Initiate self-test	No	Yes
1	4	Transmitter shutdown	No	Yes
1	5	Override transmitter shutdown	No	Yes
1	6	Inhibit terminal flag bit	No	Yes
1	7	Override inhibit terminal flag bit	No	Yes
1	8	Reset remote terminal	No	Yes
1	9-16	Reserved	No	TBD
1	17	Transmit vector word	Yes	No
1	18	Synchronize	Yes	Yes
0	19	Transmit last command	Yes	No
1	20	Transmit BIT word	Yes	No
1	21	Selected transmitter shutdown	Yes	Yes
0	22	Override selected transmitter shutdown	Yes	Yes
1 or 0	23-31	Reserved	Yes	TBD

0 Dynamic Bus Control

The active BC uses this mode code to pass control to another BC. The transfer allows the other BC(s) time to control subsystems on the same data bus. Once the BC has passed control, the former BC must assume the role of an RT or M. This approach provides considerable autonomy from BC to BC at the overhead expense of time-sharing the bus and the risk of no BC or more than one BC being in control at any one time. This method should never be used to pass control from the primary BC to the back-up BC when performance problems with the primary BC occur because the failing unit seldom operates as planned.

1 Synchronize without Associated Data Word

18 Synchronize with Associated Data Word

These BC-transmitted mode codes can be used to synchronize one or all RTs if used with a broadcast address number in the command word. Since no additional data is provided with the first mode command, the receiving RT(s) must be designed so that a predefined action occurs. The same is true for the Synchronize with Data Word mode. In this mode command the user may define specific synchronization information. These mode commands have been used to initialize RTs, set clocks to a preset value, release or set internal RT buffers, define frame changes, select subaddress blocks, and perform many other user-designed functions. Each designer has chosen different applications for these mode commands. Therefore, the designer should examine system impact when using off-the-shelf RTs.

2 Transmit Status Word

This is one of the most common mode codes used to obtain a status word from a specific RT. Since this mode code does not update the information bits in the status word when the RT receives it, the BC can interrogate an RT concerning the previous message. This mode code can also be issued to troubleshoot an RT that fails to transmit a status word to determine if the previous message was received with or without error. This mode code provides one method to determine if a unique RT received a previous message that was a broadcast message. (See Transmit Last Command mode code for a second method.)

19 Transmit Last Command Word

The BC can use this mode code to determine if an RT received a previous message (broadcast or non-broadcast). The command will not change the status word, therefore the status word will reflect the previous command's information. If the BC is capable of storing and evaluating both the data word (the 16 bits from the previous command word), and the status word, this command can provide the same information as the Transmit Status mode command. Often systems are not designed to store both the status word and the data word, thus two separate mode commands are required (i.e., Transmit Status and Transmit Last Command). This mode command is used to verify order of message reception where order is critical to system performance. However, the system designer should minimize the use of messages requiring specific order, if possible, or use unique subaddress mapping to ensure multiple message order in the receiving RT, thus requiring no specific verification.

3 Initiate Self-Test

This mode code allows the BC to command an RT to initiate self-test. The test results can be collected after the RT has conducted its self-test via the Transmit BIT mode command. Generally, RTs require time to accomplish this task, therefore the transmission of this mode command and its associated reporting mode command must be properly timed to achieve the most recent self-test results.

4 Transmitter Shutdown

5 Override Transmitter Shutdown

8 Reset Remote Terminal

21 Selected Transmitter Shutdown

22 Override Selected Transmitter Shutdown

These mode commands are used to shutdown or initialize transmitters or to reset the RT to a power-on state. With dual-redundant standby systems, mode commands 04 and 05 are usually used. Mode commands 04 and 05 always refer to the transmitter on the other bus, not the transmitter associated with the bus receiving the command. Mode commands 21 and 22 are used in systems where the number of redundant data buses exceeds two. The data word indicates which bus to shutdown. Once again it will not be the transmitter of the receiving bus. Mode commands 21 and 22 are used only when the BC cannot communicate with an RT on a bus because the RT's transmitter is active. Generally this condition is due to a failure. Another method, the Reset mode command, causes the RT to re-initialize completely by going through a power-down and power-up sequence. These methods should be required only if the RT's watchdog timer associated with the length of a transmission fails. Reset may also be used to initiate one or all RTs to a power-on condition for start-up. This action will clear internal information to create an orderly start-up.

6 Inhibit Terminal Flag Bit

7 Override Inhibit Terminal Flag Bit

These mode codes allow the BC to control operation of the Terminal Flag bit in the status word. When a single RT interfaces to more than one bus, a method of monitoring for the first failure is required. After analysis of the fault, the BC can remove the fault reporting to prevent unnecessary analysis by the BC as the RT continues to perform using its redundant circuitry. Since most systems have a minimum dual-standby redundancy capability, the elimination of fault reporting after a single failure causes no hardship. If greater than dual redundancy is used, other methods such as Transmit BIT word should be used to monitor performance after the first failure. Thus, the inhibit mode code prevents needless error analysis after every message transmitted or received by the RT because the status word's Terminal Flag bit is set.

17 Transmit Vector Word

This mode command is used to determine the subaddress of the aperiodic message that the RT has requested using the Service Request bit in the status word. Although user defined, the data word usually contains the information that allows the BC to enter its aperiodic message table and command the appropriate message transmission. The RT design may require the subsystem to queue several aperiodic requests prior to transmitting the Service Request bit in the status word.

2.7 1553 Electrical Interface Requirements

The Standard defines interface characteristics that achieve electrically compatible terminals capable of bus communication. It specifies transmitter and receiver interface parameters compatible with bus cable and bus coupler parameters. These are analog design parameters which allow the system designer to build multiple systems using terminal electronics regardless of subsystem function.

The Standard has word and message validation requirements for terminals and requirements for the data bus cable and bus termination resistors. The Standard allows a designer to connect a terminal to the bus in two ways. The direct method allows a connection of the RT to the main bus with no electrical components. The transformer-coupled method uses an isolation transformer and resistors between the RT and the main bus. The cable from the main bus to the RT, if it is used, is called a stub.

2.8 Note on the Historical Rationale for MIL-STD-1553 Characteristics

Technical papers and conference handouts during the early 1970s explain the rationale for the technical decisions that lead to the MIL-STD-1553 data bus. Several commercial airplane multi-wire serial link designs and RS-232 existed, but no available design met the data rate and integrity needed for serial multiplexing of automatic subsystems. Therefore, a new design had to be selected. The existing B-1A, F-15A, and space shuttle designs provided a design foundation. Designers had to select modulation, method of synchronization, link control and data protocol, and physical media.

Baseband modulation was chosen instead of carrier modulation because of hardware complexity and the lower bandwidth required by baseband modulation. The link would be asynchronous (independent clocks in terminals) and self-clocking (synchronization information contained in message words). Studies of the trade-off of the number of overhead bits required versus noise immunity pointed to the unique three-bit word synchronization that MIL-STD-1553 uses.

Bus control methods studied included both central and distributed control. Time slot control by a central timing mechanism was discarded as inflexible. Contention methods for obtaining bus control were discarded because of lack of positive control of the bus within a predictable time. Message failure detection has always been an outstanding feature of MIL-STD-1553. Concerns of the high overhead to assure message completion on a contention bus, as well as the non-deterministic latency, contributed to the rejection of contention. The choice of a single bus controller was left, but the protocol made it possible to pass bus control to any capable unit. Dynamic bus control is a rarely used feature.

With only one active bus controller, message formats with minimum overhead were desirable. Controller-to-terminal and terminal-to-controller messages were obvious choices. The USAF and USN, however, never agreed on broadcast message utility or desirability. Broadcast messages were nevertheless included. The overhead consisted of the command word (16 bits), a delay less than one word time for the terminal to respond with a status word, a status word (16 bits), and parity and sync for each word.

Multiple cables were rejected in favor of the single cable because 1 MHz (1 Mbps) bandwidth was adequate for control and data. At that time, 30 terminals on one cable were adequate. The decision to transformer couple the cable influenced the signal encoding. Manchester biphase level encoding was chosen from among candidates that included polar and bipolar NRZ (non-return to zero voltage waveform), polar RZ (return to zero voltage waveform), and unipolar level NRZ. Tests showed that a twisted, shielded pair was adequate for the 1 MHz transmission rate, making coaxial or triaxial lines unnecessary. The greatest noise and fault immunity was gained by choosing an impedance-matched and loaded data bus for the bus connections (the impedance into a terminal is much greater than the characteristic impedance of the line). Common mode rejection was attained by using balanced differential transmitter/receivers.

3.0 MIL-STD-1553 AND SYSTEMS INTEGRATION

3.1 Range of Bus Topologies and Applications

Figure 6 presents three 1553 data bus schematics, or "topologies," to show that the relative position of the BCs, back-up BCs (BBCs), and RTs on the bus is not significant, but that the level of control is important. The three topologies represent typical bus configurations in use and illustrate how the system designer may use MIL-STD-1553. Only dual-standby-redundant buses are illustrated, but any of the topologies could have additional buses operating either in standby or active redundancy.

Equipment with MIL-STD-1553 interfaces need not be restricted to either a BC, RT, or M. BC redundancy is essential because the data bus cannot operate without a BC. Therefore, most designs include BBCs. The equipment will usually contain both a BC and an RT capability that may share common functions within the same chip. The BC/RT capable interface provides an effective BBC.

The Single Level bus is the most widely used, usually with one BC, one BBC, and multiple RTs. Note that the BC and BBC can also function as RTs. As a BBC/RT, a unit may receive special update or coordination messages which keep it ready to assume the BBC role if the BC fails. The Single Level bus reliability has been well established for all but flight-critical applications.

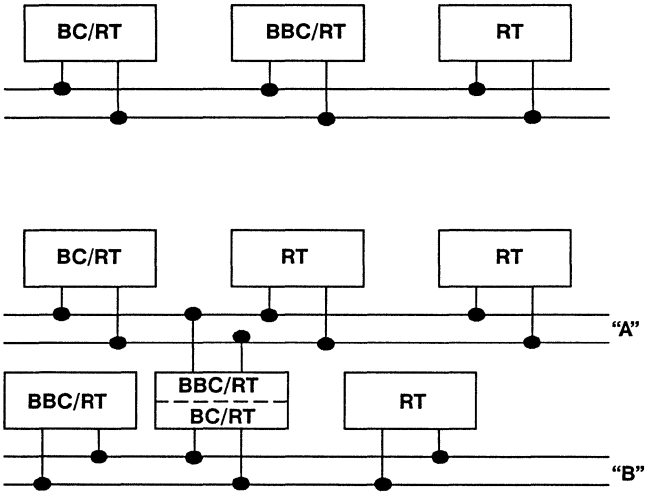
The Multiple Level example illustrates a single unit on buses A and B that serves as the BBC on one bus and the BC on the other bus. When the BBC is not functioning as a BC, it is an RT. Multiple level bus topologies allow more RTs to be integrated into a system or the system to be divided into subsystem buses with dedicated databus functions.

The Hierarchical Level illustrates indirect control of a bus through a unit which receives data on bus A and transmits the data on either bus W1 or W2. The command word, which the BC transmits on W1 or W2, may be one of the words in the message received on bus A, or it may contain its own bus controller table like any other BC. Hierarchical Level bus topologies allow more RTs to be integrated into a system while maintaining greater centralized control at the main bus level.

When compared to the BC, a BBC may be an identical, a functionally equivalent, or a functionally less capable unit. Of these three unit types, the identical BBC requires the least development but may not be economical if an expensive unit contains the BC. If one unit connects to several buses, it may be the BBC for all of them, in which case it is probably functionally less capable than any of the BCs it backs up. The BC to BBC switch-over is automatic. The switch-over must be designed so that no single-point failure will prevent the switch-over and the successful operation of the back-up. Therefore multiple mechanisms must be used: timers to detect lack of updates; discretes to assert control; bus activity detectors to note lack of bus activity; self-test to verify readiness to assume control; and storing of physical or logical address. Frequently, the switch-over will be logically similar to start-up because the readiness to control the bus is usually tested at start-up.

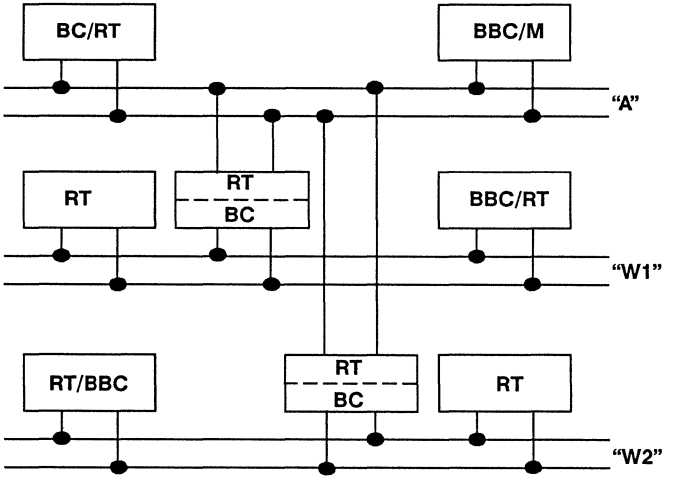
Multiple Level and Hierarchical Level topologies can usually be designed from an existing Single Level design. In retrofit situations, this frequently occurs and requires the designer to accommodate RTs with varying capabilities and possibly to include units designed to various versions of 1553.

Each of these topologies presents successively more difficult MIL-STD-1553 system control issues that the designer must solve. The main ones are: (a) successful initialization at start-up and ability to switch over to BBC; (b) operation after RT failures; (c) message handling and processing capacity of the BBC/BC after failure of the BC in the Multiple Level; (d) and ability to sustain operational capability if a BC on W1 or W2 has failed in the Hierarchical Level when there is no BBC.



SINGLE LEVEL
BCs/BBCs and RTs connected to one dual redundant bus. The BC/RT (or the BBC/RT) are contained in one physical unit.

MULTIPLE LEVEL
A BC on bus "B" is the BBC on bus "A." The BBC/RT on bus "A" and the BBC/RT on bus "B" are contained in one physical unit.



HIERARCHICAL
Special purpose units pass data between two dual redundant data buses. Each unit is an RT on bus "A" and a BC on either "W1" or "W2."

Figure 6. Data Bus Topology

3.2 Data Required to Specify the BC, RT, or M

The data bus topology, control scheme, and data transfer requirements provide the data required to define the MIL-STD-1553 interfaces. The application's functional capability will determine the requirements of the BC, RTs, and M. Since MIL-STD-1553 does not dictate the topology and gives the designer the option to use only part of the protocol, the following information offers a way to organize the decisions required to select among the options. The result should be the bus topology and the control scheme that will provide the basis for unit hardware specifications and for software needed to work with the MIL-STD-1553 equipment. The iterative steps are: define the source and destination of all data; establish the bus topology; choose the level and detail of the control of messages; choose the mode codes to be used to assist in control of messages; choose the design options for the BC and RT.

First, the designer determines the source and destination of each data item. To complete this step, the designer must know what processing and computations will be performed with the data. The designer must define each individual data transfer, which may be a message, several messages, or part of a message. The definition includes: the function performed that creates the source; the function performed by the using process (only data transmitted on the bus is discussed here); the data definition in 16-bit words; the iteration rate if it is periodic data; the conditional events if it is aperiodic data; the allowable latency; the conditional events related to transmission of the data (such as mission modes or demands); and the error handling, if it affects transmission of data.

When choosing a topology, the designer's main considerations usually include the redundancy and isolation requirements, required use of existing equipment (usually RTs), and cost. Within cost constraints, bus loading should be less than 50 percent with less than 15 physical units on one bus. The lessons learned during the establishment of bus topology for previous MIL-STD-1553 systems can be a valuable information resource.

RTs and BCs on a 1553 bus are the sources and users of data transmitted on the bus. RTs that are not BBCs may be primarily data sources (such as a primary sensor) or primarily data users (such as a display). A MIL-STD-1553 system will always use either RT-to-BC messages or RT-to-RT messages to transmit RT data from source to user. Since it controls the messages, the BC, as a computational unit, is almost always key to data use. If another RT, not the BC, uses data, the RT-to-RT message is more efficient. Finally, the broadcast message should be considered if a system requires BC coordination among several RTs or if more than one RT uses the same data. Designers will establish message lists that BCs will use to supply the data needs of the system.

The Standard permits a multiplex topology and control design without mode codes. Few existing systems use no mode codes because mode codes increase bus loading efficiency.

The following table shows some common mode code uses. Some RTs in a system are incapable of responding to some mode codes. The designer can specify not to send mode commands to an RT that is incapable of responding to them.

USE	MODE CODES
Time synchronization of RTs	Synchronize Synchronize with data word
Polling RTs to determine status	Transmit Status word
No Status word received from an RT	Transmit Status word
Busy bit set in Status word	Transmit last command
No response on a bus from an RT	Transmit Status word Initiate self-test Reset remote terminal

Some MIL-STD-1553 requirements may only be implemented in hardware due to the timing requirements (for example, the maximum no response time-out that a BC may wait for an RT status word). Additional hardware features in some manufacturer's terminal hardware assist the message designer, simplify the software, and decrease the number of times a BC processor is interrupted to handle an exception. An example is the capability to set the number of retries and automatically retry a message on the same bus or redundant bus if a time-out occurs. Therefore the designer must also know the special capabilities of the 1553 hardware used.

MIL-STD-1553 system documentation is completed when each bit of each word in each message is documented. MIL-HDBK-1553A, Section 80 gives formats for all of the commonly used data (e.g., acceleration, angular measurement, angular acceleration, velocity, voltage). Section 80 gives format recommendations for message documentation including the source, destination, message type, and word count. Because this type of information requires great detail, it is contained in a separate document controlled by configuration management. This information is usually called an Interface Control Document (ICD) or it is part of an Interface Specification. Buyer's specifications or statements of work frequently reference these documents.

3.3 Typical System Product Qualification Referenced to MIL-STD-1553

MIL-STD-1553 systems are typically installed in production vehicles by large aerospace companies or the DoD. The vehicles frequently use units with MIL-STD-1553 interfaces acquired from companies that specialize in units such as sensors, displays, and mission computers. Such companies usually supply the units, particularly RTs, with all software or firmware included. To comply with a buyer's request for equipment with a MIL-STD-1553 interface, the designer must have access to the interface specification or control document. The designer also needs additional data bus systems information. The designer of a unit with a MIL-STD-1553 interface must understand the user's requirements before selecting the interface hardware and the subsystem-to-interface design and establishing the software requirements.

MIL-STD-1553 system testing usually includes component tests, integration tests in a system integration laboratory, and system tests in the vehicle. Suppliers of units with MIL-STD-1553 interfaces will conduct three complete test cycles: in their own laboratory; in the system engineering laboratory; and in vehicle test. In addition to conducting these tests and demonstrations, the subsystem designer should be able to verify that the unit with the MIL-STD-1553 interface satisfies the test requirements in the RT Validation Test Plan.

3.4 RT Validation Test Plan and Other Test Plans

MIL-HDBK-1553A documents the comprehensive RT Validation Test Plan. The plan says "a remote terminal is considered to have failed ...if (it) fails any test...(of) this test plan." The plan is therefore the only correct interpretation of any optional or mandatory MIL-STD-1553B requirement. The plan covers 1553B, 1553B Notice 1, and 1553B Notice 2. It describes the test procedure, the measurements to be made, the number of test iterations (repetitions of a single test), and the acceptable responses. The plan includes many combinations of valid MIL-STD-1553 conditions, such as measurement of the message gap over a 30-second period for each of 12 messages.

At the USAF's request, the SAE prepared the RT Validation Test Plan. The SAE has published RT production test plans; validation and production plans; M test plans; coupler, terminator, and cable test plans; and 1553 data bus systems test plans. These and additional 1553-related publications are available from the SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

4.0 Design Considerations for MIL-STD-1553 Interfaces

The designer may choose LSI, VLSI, or hybrid MIL-STD-1553 components from several manufacturers. This section deals with the design issues and considerations the designer must consider prior to selecting these components. The most common components are transceivers, transformers, encoder-decoders, and protocol devices. Although many of the MIL-STD-1553 components available today incorporate all of the Standard's options, the correct use of these components remains a significant design effort.

4.1 Systems Requirements

The first goal of any design involves understanding and meeting the system requirements. The 1553 interface designer must know the following: (a) what versions and notices of MIL-STD-1553 are included in the system requirements; (b) what options in those versions and notices have been selected for use; and (c) how to ensure that the selected options are implemented in the design.

New designs should conform to MIL-STD-1553B, Notice 2, the latest released version of the Standard. Notice 2 defines a minimum set of requirements that all terminals must implement and specifies how to implement some options, such as status word bits and mode codes. Since Notice 2 defines only a minimum set of options, designers should consider all the options in the Standard.

4.2.Terminal Definition

The MIL-STD-1553 text defines the terminal as "the electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus."

A typical terminal consists of the following elements: a transceiver, an encoder/decoder, protocol logic, data buffer(s) or memory, and a subsystem interface. Figure 7 shows a block diagram of a typical terminal. The terminal is the only electronics necessary to transfer data between the data user and the data bus. In figure 7, the dashed line defines the "terminal." Any processor that has other duties besides controlling the MIL-STD-1553 interface electronics would also be considered part of the subsystem.

4.3 Terminal Functions

Some companies manufacture a single MIL-STD-1553 interface circuit that can perform all terminal functions. In this case, the subsystem interface has features which allow the selection of the terminal function. A multi-function terminal will often reduce the number of components.

If the terminal being designed must be capable of performing as the BC, the designer must know if the terminal must also operate as a BBC. When functioning as the active BBC, it can obtain data from the terminals in the data bus system by performing as an RT, receiving data from the BC; or it can act as an M, collecting data from selected messages "listened to" on the bus; or it can be idle, performing no function until it becomes the active controller. Provision for these capabilities, if required, must be part of the design.

The designer must know the protocol to which the terminal is interfacing and whether the design must accommodate multiple versions of the Standard. Some early aircraft data bus designs do not conform to any version of the Standard, further complicating the design. The designer may solve the electrical differences between the versions by correctly selecting the analog devices (e.g., transceiver and transformer). The protocol differences, however, may require specialized designs. Some available components implement the protocol of only a single version of the Standard, while others implement the protocols of all versions and notices of the Standard. Table 1 compares 1553A, 1553B, Notice 1, and Notice 2.

The designer must also know the subsystem interface to the terminal. For RTs, the interface may be hardware registers; a direct memory access (DMA) into private, local, or global memory; a dual or multi-port memory; or a memory register (e.g., a first-in first-out (FIFO) memory). For BCs and Ms, the interface is usually a microprocessor or a large memory system.

The designer must also consider both the software requirements and the physical hardware design in MIL-STD-1553 terminals, specifically the BC. System control considerations are derived from requirements allocated to software to support the missions, transfer data, control the data bus, handle errors and failures, and manage the data bus hardware and software interface. System control includes the data bus system hardware and software as well as the interface to the application software.

4.4 Terminal Design Issues

The following paragraphs present options from the Standard that the designer should consider in the terminal design.

4.4.1 Mode Commands

Most protocol logic components available today handle all of the mode commands. The designer needs to know which mode commands to implement. Notice 2 to the Standard requires that a minimum of four mode commands be implemented: Transmit Status Word, Transmitter Shutdown, Override Transmitter Shutdown, and Reset Remote Terminal.

Mode command transactions are automatic and are usually transparent to the subsystem. For example, there is no need for the subsystem to know that the Transmit Status Word Mode Command was received (although most components allow an interrupt to the subsystem host to be generated upon receipt of any mode command). However, for mode commands which have data associated with them, such as Synchronize with Data Word or Transmit Vector Word, the subsystem should be informed immediately. The subsystem processor should also be informed upon receipt of the Reset Remote Terminal and Initiate Self-Test mode commands. Notice 2 to the Standard imposes timing constraints upon these two mode commands; the subsystem processor (or logic) may be required to assist in their implementation.

4.4.2 Status Word Bits

Like the mode commands, most protocol components available automatically handle the status word bits and the response of the status word. In most cases, the subsystem can examine the status word by reading a register (a BC-unique requirement). The design must address the Notice 2 to the Standard restrictions on the use of the Busy bit (an RT-unique requirement). The hardware and software design issues usually determine the method used to set the status word bits. For example, the designer may use a hardware timer, reset periodically by applications software, to set the subsystem flag if the timer expires.

4.4.3 Terminal Address Selection

The Standard allows the terminal address to be set either from inputs hardwired directly to the encoder/decoder or by changeable software via a register read by the encoder/decoder. Notice 2 to the Standard requires that the address is programmed external to the terminal (usually by cable wiring). Notice 2 also requires a validity test (usually a parity test), on the terminal address.

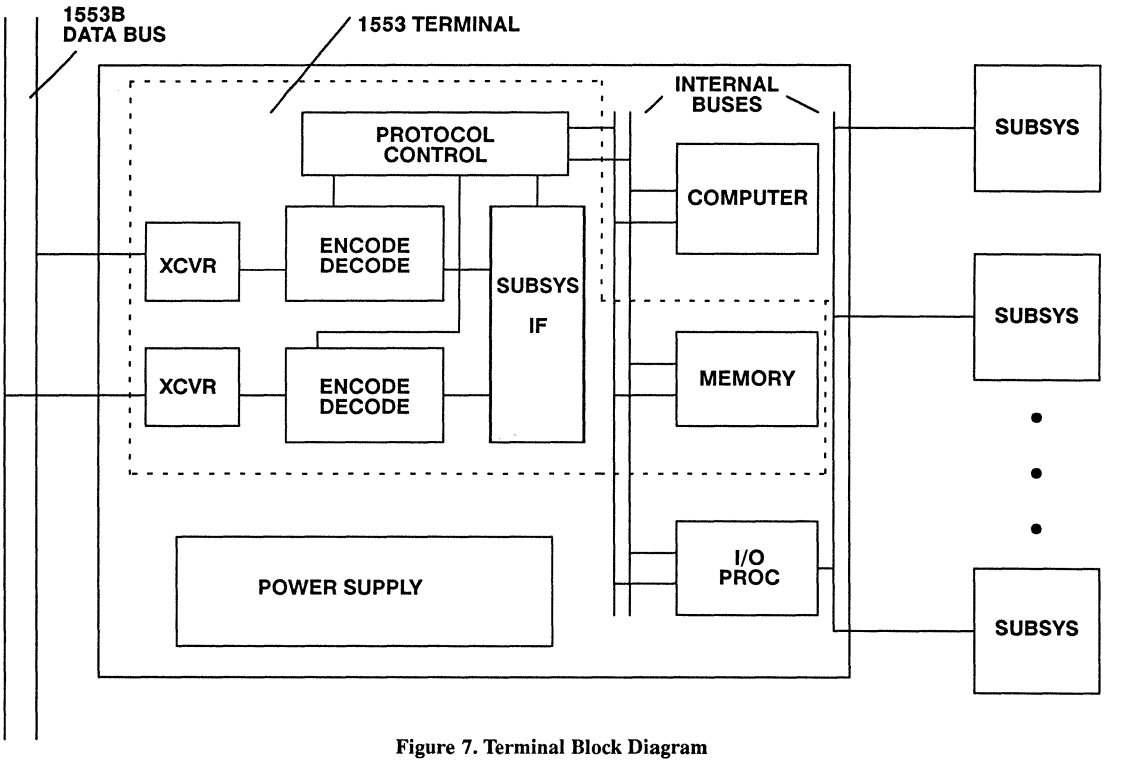


Figure 7. Terminal Block Diagram

4.4.4 Extended Subaddressing
RT subaddresses map data to specific memory locations. Subaddresses within an RT are limited to 30 transmit and 30 receive messages. The 32 data words per message limit means only 960 unique data words may be transferred in each direction (transmitted and received). In complex subsystems and for BBCs operating as RTs, this restriction usually provides insufficient data transfer space. Therefore the subaddress range must be extended to accommodate more data. Changing an address pointer to allow the addressing of multiple sets of subaddresses in memory will extend the subaddress range.

Two methods can implement this concept. The first dedicates one of the existing subaddresses for subaddress location change. The second, the preferred method, uses the data word associated with the Synchronize with Data Word mode command. The receipt of a Synchronize Mode Command with data word interrupts the subsystem processor. The data word contents determine a value for the memory area that the terminal addresses for data transfer. The design requirements include the "glue logic" and software/firmware implementation. During the early design stages, the designer must define the subaddress mapping to determine if the data storage is adequate or if the design requires additional subaddressing.

4.4.5 Subaddress Restrictions
For the most part, the designer defines the use of subaddresses (SA). Notice 2 to the Standard suggests that SA30 be reserved for "data wrap-around" testing. If the Instrumentation bit in the status word is used, the designer can only use the upper sixteen subaddresses (SA16-SA30). This implementation, however, limits the amount of data that can be transferred without an extended subaddress scheme. Designers who implement terminals for MIL-STD-1760 will also find that the Standard imposes further restrictions upon subaddress uses.

4.4.6 Illegal Command Detection
If implemented, illegal command detection should at least be provided for each subaddress. Additional features could monitor unused, reserved, and undefined mode commands.

4.4.7 Broadcast Mode Commands
Notice 2 to the Standard restricts broadcast mode commands. The designer must carefully examine requirements to determine which broadcast mode commands to allow (e.g., a Broadcast Reset Remote Terminal could have disastrous effects if issued in a flight-critical situation).

4.4.8 Data Validity and Status Word Bits
MIL-STD-1553's protocol and electrical requirements provide strict conditions and control for message and data word validation. However, cases where bad data passes all validity tests may occur (e.g., when the data received has the associated terminal's status word with the Subsystem Flag bit set). The RT's interface circuitry does not examine and analyze data; it merely moves it across the data bus. When the RT receives a valid message, the data should be passed to the subsystem and applications software. The terminal should also save the status word bits associated with the data so the software can determine if the data should be used. The protocol component should store each received status word in memory locations that the applications software can access and that are separate from the data message.

4.5 Bus Controller Issues
A terminal that functions as the BC should attempt to "off load" the subsystem host processor by reducing processor interrupts that service the terminal. This operation implies that the terminal possess its own logic and data bus system software for handling frequently occurring tasks. A good BC should provide the following functions: multiple message processing, multiple protocol processing, automatic polling of status words, automatic retries on errors, and programmable interrupts. The requirement for the BC to have some autonomous intelligence often requires a unique BC protocol logic design. For this reason, various companies offer devices specifically for the BC function.

4.5.1 Message Processing
Multiple message processing is the ability to chain messages without interrupting the host application software. A BC protocol component should offer multiple message processing with as many message scenarios as possible. The scenarios include periodic and aperiodic message lists, and functional message lists such as initialization, operational modes, and failure handling. A powerful BC can also interrupt a message list chain (at the completion of a message only) and modify the list for special situations such as response to a vector word received from an RT or for time-critical message transmission. The designer should also provide message sequences for error recovery or system reconfiguration resulting from an error. A powerful BC will accommodate top-level software task managers or error handlers within the subsystem to change the bus communications by changing only a pointer to a new message list. Less powerful BCs may do the same thing by changing multiple message pointers in the current message sequence or changing bits in each message control word to indicate a "skip."

4.5.2 Automatic Retry
The protocol component design should allow the automatic retry of a message before the next message is sent. A powerful BC component allows a control word to define the message chaining and retries for each message. Retries should be programmable based upon either a no-response or the setting of the Message Error or Busy bit in the status word. Retries should be programmable on a message-by-message basis. A powerful BC can usually perform two retries on the same or redundant data bus. However, a single retry on the opposite data bus is usually sufficient.

4.5.3 Error Processing
Application software handles nearly all of the error processing functions. The BC's amount or level of error processing often determines its power. The protocol component should have the intelligence and capability to detect problems and either to handle them itself (e.g., auto retry) or to report them to the subsystem host processor via an interrupt. The ability to switch message lists easily allows the designer to "dynamically reconfigure" the data bus system by inserting or removing messages.

4.5.4 Mode Commands
The Standard provides mode commands to help the BC control and manage the data bus system. The commands provide the ability to turn terminals on or off, reset them to a known state, test them and determine the results of those tests, "poll" them to determine particular needs or status, and synchronize them to each other or to some unit of measure (e.g., time or frame count). The designer should use these mode commands to help manage the data bus system. For example, a single Synchronize with Data Word mode command can reset all clocks or timers in all terminals to the same value.

A good design includes the capability to determine which mode commands have been implemented. If a wide range of commands is used (as is typical for terminals designed prior to Notice 2), then the designer has two options. First, to simplify the bus control logic, the designer can use the minimum set of commands used by all terminals. This option, however, may result in no or few mode commands available for use. Second, the designer may track mode command implementation on a terminal by terminal basis. Although this option maximizes bus control flexibility, it requires complex bus control logic to determine which commands each terminal implements. The designer must evaluate the need for maximum bus control versus the cost of the bus control complexity.

4.5.5 Status Word Bits
The BC uses the terminal's status word to determine the RT's condition and data validity. Certain status bits are solely for use by the BC, while others are important to the applications software. The application software uses the Subsystem Flag, Service Request, and Busy bits.

4.5.6. Multiple Protocols
Each version of the Standard has a different protocol. Consequently, existing and new systems may include "mixed protocols." For example, an avionics upgrade to an aircraft may require both MIL-STD-1553B and MIL-STD-1553A RTs. Upon error detection, a MIL-STD-1553A RT always responds with its status word but a MIL-STD-1553B RT always suppresses its status word. The BC logic must decode the status word address so it can respond to the messages and status words

accordingly. Today certain MIL-STD-1553 components provide the capability to handle mixed protocols.

4.5.7 Backup Bus Controllers
While the primary BC must receive information on the configuration and status of the data bus system, the BBC must receive information on the system status. The designer can use numerous methods to transfer this data to the BBC. The BBC can operate as an RT with the BC periodically sending it data; as an M, collecting the data it needs; and as an RT with all data transfers being RT-RT and with the BBC as the sending or receiving terminal (depending on the direction of data flow). Any of these methods can be used as long as the BBC receives the data necessary to allow a smooth transition to occur. The designer must provide the BBC with the hardware and software to manage this incoming data.

4.6 Monitor Issues
The Standard only allows two cases for the M: as a "data collector," or as a BBC. For the data collector, the Standard states that "all information obtained while acting as a bus Monitor shall be strictly used for off-line applications (e.g., flight test recording, maintenance recording or mission analysis)." When functioning as an M, the BBC may collect data as necessary to determine system status. The protocol component should be selectively programmed to monitor messages on a terminal-by-terminal basis and to store that information sequentially.

4.6.1 Amount of Data
For the data collector applications, the M designer must first address the subsystem host processor's ability to move the data to a bulk storage device. Very large amounts of data can be collected. The system control data collected is later correlated to the data in messages. This information includes data pointers, command words, status words, and control words that provide error and bus information regarding the collected message. The designer must also ensure that the subsystem (i.e., the interface to the bulk storage device) can transfer the data without losing any of the data being monitored.

4.6.2 Error Codes
The system should also store the command words and status words for each message. In addition, for post-analysis, the system should store the flags that indicate on which bus the message occurred and if an error occurred. Stored information should also include a time tag so messages can be reconstructed.

4.6.3 Backup Bus Controller
For terminals functioning as a BBC and collecting data as an M, data collection is not as critical. Typically, the BBC/M needs to retain data to determine the system status. Only the most current messages and the status of the RT's health are important so that the subsystem need not move large amounts of data. A terminal operating as an M does not need the BC's error handling capability until it begins to function as a BBC.

4.7 Transceiver Issues
In addition to selecting the proper encoder/decoder and protocol logic, the designer must select a transceiver to provide the analog interface to the data bus. Typical concerns regarding the transceiver are listed below.

4.7.1 Idle State
Different transceivers require and provide different logic levels on the transmit and receive TTL input and output lines for the Manchester idle state. For this Manchester encoding state, the idle level should be two "high" or two "low" states. Therefore, the designer must ensure that the requirements of the selected encoder/decoder chip match those of the selected transceiver. These lines typically impact the transceiver turn-on and shut-off.

4.7.2 Power Supply Loading and Power Dissipation
As with all electronic components, the designer must define the power supply loading and power dissipation needs. The system must provide proper decoupling of the power lines close to the transceiver and adequate heat sinking. Most transceiver power characteristics have a duty cycle rating of 25%. The power supply and heat sinking should sustain this value. However, the system may require RTs in BCs and BBCs to output data at a much higher duty cycle. Designers should evaluate the system data transmission requirements to establish the duty cycle.

4.7.3 Voltage Drive Versus Current Drive
Two types of transceiver drive circuits exist: voltage drive and current drive. Both are available and used in existing terminal designs. Arguments can be made for either type. MIL-STD-1760 stores management applications should use the voltage drive transceiver. The designer must determine which is better suited for the design.

4.7.4 Circuit Layout
Data bus characteristics contain requirements which include the terminal interface. These characteristics affect the transceiver and the encoder/decoder design. The Standard carefully defines the requirements for cabling and termination. The circuit layout must prevent any imbalances of this impedance. The transceiver should be located in an area that allows equal length and width of traces to the transformer and to the encoder/decoder chip. Ground plane geometry and layout are important in reducing stray capacitance due to signal delays or rise and fall time skewing and in avoiding crosstalk or coupling from other signal traces.

4.7.5 Coupling Methodology
The Standard provides two ways to connect the terminal to the data bus: direct and transformer coupling. Notice 2 to the Standard requires that USAF and Army applications use only transformer coupling and that USN applications use both methods. The designer must be certain that the terminal provides proper voltages for the methods used. Also, use of both methods requires careful attention to stub isolation and termination design.

4.8 Subsystem Interface Issues

The designer must define the subsystem interface at the onset of the design. Some components available today provide the maximum flexibility in subsystem interface design. The interface may be private or global memory accessed via a DMA scheme, a FIFO memory buffer, multi-port access to private memory, or direct connections to some I/O register or port. Even though the Standard imposes no requirements on the subsystem itself, MIL-STD-1553 requirements set the amount of time it takes to transfer data to and from the subsystem.

4.8.1 Memory/Data Timing

A terminal must be able to pass data either to or from its subsystem so it is ready to process the next command on the bus. This requirement applies only to RTs and Ms, since the BC controls the bus and may operate at any speed necessary to interface with its subsystem. For a receive command, the terminal has approximately 56 μs to either pass the data to the subsystem or to buffer the data in memory. For a transmit command, the terminal must be able to retrieve the desired data (at least the first word) within approximately 28 μs.

4.8.2 Sample Consistency

When transmitting data, the terminal software must ensure that all data transmitted within the same message is from the sample set. A good protocol logic design will provide double buffering of transmitted data to help ensure sample consistency. Many systems also use double buffering for receive messages.

4.8.3 Host Processor Interface

The protocol chip selected should provide the maximum amount of intelligence to the terminal electronics and thereby allow the maximum off-loading of the subsystem host processor. The designer should use this intelligence to establish interrupt criteria. Unnecessary interrupts should be eliminated.

4.9 Gateways

Gateways are special terminals, usually composed of two RTs or one RT and one BC, that provide a data path between two independent data bus systems. Figure 8 is an example of such a gateway. The data (or portions of it) received in a message on one of the data bus systems is transferred to a area of shared memory.

4.9.1 Data Formats

When data is transferred between terminals, differences in data word formats must be recognized. For example, the meaning of bit "4" in word "6" must be the same for both terminals. If the meanings are different, the data must be scaled or reformatted. The BC usually performs this task. However, for gateway applications, the subsystem within the gateway may be required to manipulate the data. The designer must examine the data word formats for each word transferred between buses to ensure that no reformatting is necessary.

4.9.2 Data Latency

Use of gateways can cause concern due to data latency incurred by moving the data between buses. Data latency occurs because when the subsystem processor moves the data or changes data location pointers, the two data buses operate asynchronously. If data latency is a concern, two easy solutions exist. The first solution synchronizes the two buses so that the receive and transmit commands from the two BCs are established. The second solution time-tags the data. Transferring a time-tag with the data (assuming that the gateway added the time-tag and not the originator), reduces the number of data words the gateway can output.

4.9.3 MIL-STD-1760 Gateways

MIL-STD-1760 limits the gateways used as BCs for stores management buses to the transfer of 30 data words on the stores bus. (Note that MIL-STD-1553 allows 32 data words.) MIL-STD-1760 provides a two-data-word overhead to handle the transfer of messages between the higher-level BC (1553 bus) and the lower-level BC on the stores bus.

4.10 MIL-STD-1760 Design Issues

Designers dealing with MIL-STD-1760 have additional restrictions and limitations placed on the terminal design. These include restrictions on data word count, restrictions on subaddress utilization, and differences in the transceiver output voltages. The subystem host processor can handle the first two of these restrictions. The transceiver must meet MIL-STD-1760 voltage requirements. MIL-STD-1760 terminal designers should pay close attention to the 1760 Standard "logic" section which provides the message sequencing, timing, and data definitions.

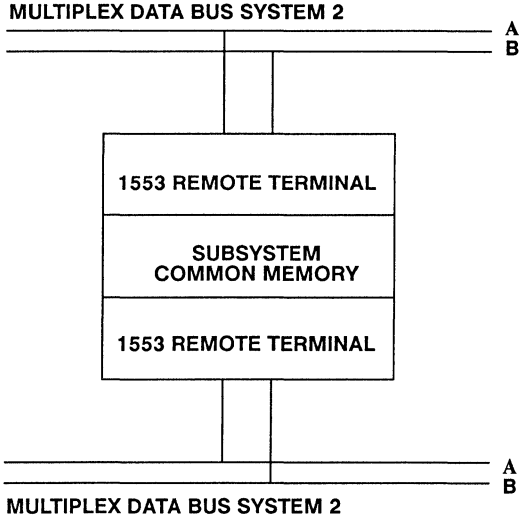


Figure 8. Gateway

4.11 Overview of MIL-STD-1553 Versions and Notices
The first Standard was issued in August 1973 for the USAF only. In April 1975, DoD released a coordinated tri-service revision (1553A) to provide wider application and standardization. Table 1 uses the tri-service Standard (1553A) as the basis to track 1553B (September 1978), Notice 1 to 1553B (February 1980), and Notice 2 to 1553B (September 1986). Today the DoD Standard is MIL-STD-1553B as modified by Notice 2. Because Notice 2 completely replaces Notice 1, only the additional requirements of Notice 2 supersede 1553B if Notice 2 is a requirement.

Table 1 is divided into three parts, each starting with 1553A as a baseline and showing changes to arrive at 1553B, 1553B Notice 1, and 1553B Notice 2. Table 1 - Part 1 tabulates and condenses many of the design parameters into a quick reference table. The designer who must consider systems using terminals of different vintage or the designer who must design to multiple standard versions can compare requirements using this table. The table is separated into a protocol section including message format, command word, status word, and data word and into a message validation list of requirements. Table 1 - Part 2 is divided into parameters for a terminal operating in a system with transformer coupled stubs versus direct coupled stubs. Table 1 - Part 3 is a collection of general requirements. This series of tables summarizes differences and does not represent a complete set of requirements. Designers should consult the appropriate MIL-STD-1553 version or notice for complete requirement descriptions.

4.12 Summary
This section covered the important design concerns the systems designer must address prior to selection of 1553 design components and implementation of the requirements of a MIL-STD-1553 or MIL-STD-1760 terminal. Manufacturers will provide the actual technique to use to interface selected 1553 components to particular subsystems.

MIL-HDBK-1553A contains additional information regarding issues discussed in this section.

The Validation Test Plans provide the ultimate asessment of a terminal's design integrity. Consult these Test Plans whenever a question regarding the interpretation of the Standard arises. In this respect, by providing the designer with the test methods, the Test Plans establish detailed terminal design requirements.

Table 1. Standards Comparison - Part 1

REQUIREMENTS	1553A	1553B	NOTICE 1	NOTICE 2
Message Formats, Non-Broadcast:				
RT-to-BC	Optional	Optional		Required
BC-to-RT	Optional	Optional		Required
RT-to-RT	Optional	Optional		Required
Mode Code without Data Word	Dynamic Bus Only	Optional	Restricted	Restricted
Mode Code with Data	Not Defined	Optional		
Message Formats, Broadcast:				
BC-to-RTs	Not Defined	Optional		
RT-to RTs	Not Defined	Optional		
Mode Code without Data Word	Not Defined	Optional		
Mode Code with Data Word	Not Defined	Optional		
Mode Code Indicator (replaces subaddress)	00000	00000 or 11111 NOTE 1		
T/R Bit if Mode Code	Not Specified	If no Data = 1 If Data 1 = xmit, 0 = receive		
Assigned Mode Codes:				
00000	Dynamic Bus Allocation	Dynamic Bus Control NOTE 2	Not allowed for USAF	Not allowed for DoD
00001	Not Specified	Synchronize without Data Word		
00010	Not Specified	Transmit Status Word		Required NOTE 3
00011	Not Specified	Initiate Self-Test		100 ms
00100	Not Specified	Transmitter Shutdown		Required
00101	Not Specified	Override Transmitter Shutdown		Required
00110	Not Specified	Inhibit Terminal Flag	Not Allowed for USAF	
00111	Not Specified	Override Inhibit Terminal Flag	Not Allowed for USAF	
01000	Not Specified	Reset Remote Terminal		5 ms
01001 - 01111	Not Specified	Reserved		
10000	Not Specified	Transmit Vector Word		
10001	Not Specified	Synchronize with Data Word		
10010	Not Specified	Transmit Last Command Word		
10011	Not Specified	Transmit BIT Word		
10100	Not Specified	Selected Transmitter Shutdown		Not Defined for Dual Redundancy

10101	Not Specified	Override Selected Transmitter Shutdown		Not Defined for Dual Redun-dancy
10110 - 11111	Not Specified	Reserved		Status Word Bit
Definitions:				
Bit 9	Message Error	Message Error	Required	Required
Bit 10	User Defined NOTE 4	Instrumentation	Zero	Zero
Bit 11	User Defined NOTE 4	Service Request		Optional
Bit 12	User Defined NOTE 4	Reserved	Zero	Zero
Bit 13	User Defined NOTE 4	Reserved	Zero	Zero
Bit 14	User Defined NOTE 4	Reserved	Zero	Zero
Bit 15	User Defined NOTE 4	Broadcast Command Received		If Broad-cast is used
Bit 16	User Defined NOTE 4	Busy		Restricted
Bit 17	User Defined NOTE 4	Subsystem Flag		If BIT
Bit 18	User Defined NOTE 4	Dynamic Bus Control Acceptance		Not allowed for USAF
Bit 19	Terminal Flag	Terminal Flag		If Self-Test

Notes:

1. 11111 Used with Instrumentation bit in status word.
2. In 1553B, implementation and/or use is optional.
3. Means it is a required capability of the hardware.
4. Impact upon BC design due to different RTs having different requirements.
5. Status word requirement change from 1553A in status word bit settings and status word transmission.

Table 1. Standard Comparison - Part 2

REQUIREMENTS	1553A	1553B	NOTICE 1	NOTICE 2
RTs - Transformer Coupled Stubs				
Stub Length	20 ft.	20 ft. (suggested)		
Stub Input Voltage	Not Specified	1.0-14.0 V		
Isolation Resistor	0.75 Zo + 5%	0.75 Zo +/- 2%		
Transfmr Open Ckt Impedance	Not Specified	3 Kohms (75 KHz-1 MHz)		
Cable Coupling	Shielded Coupler Box	Min 75%	Min 90 %	360° Min 75%
Transfmr Turns Ratio	Not Specified	1:1.41 +/- 3%		
Transfmr Waveform Integrity				
Droop	Not Specified	20%		
Overshoot and Ringing	Not Specified	1.0 V peak		
Common Mode Rejection	Not Specified	45 dB at 1 MHz		
Output Waveform Requirements	Trapezoid	Trapezoid		
Output Voltage Level	6.0-20.0 Vpp l-l	18.0-27.0 Vpp l-l		
Output Level with fault	1.0-20.0 Vpp l-l	1.0-14.0 Vpp l-l		
Max Zero-Crossing Deviation	25 ns	25 ns		
Rise/Fall Time	100 ns or greater	100-300 ns		
Max Distortion	Not Specified	+/- 900 mVp l-l		
Output Noise	10 mVpp	14 mV rms		+/- 250 mVp l-l NOTE 6
Output Symmetry	Not Specified	+/- 250 mVpp l-l		
Input Waveform Requirements	Square to Sinewave	Square to Sinewave		
Input Signal Level	1.0-20.0 Vpp l-l	0.86-14.0 Vpp l-l		
Common Mode Rejection @ RT	Not Specified	10.0 V l-g (dc-2 MHz)		
Max Zero-Crossing Deviation	Not Specified	150 ns		
Common Mode Rejection @ Bus	10.0 V l-g (dc-2 MHz)	Not Specified		
No Response Input Level	Not Specified	0.0-0.2 Vpp l-l		
Input Impedance	2000 ohms	1000 ohms		
Noise Rejection	1 Error in 10E12 bits	1 Error in 10E7 words		
Message Rejection	1 Error in 10E6 Mgs	Not Specified		
Electrical Isolation between Data Buses	Not Specified	435 dB		
RTs - Direct Coupled Stubs				
Stub Length	1 ft.	Max 1 ft.		
Stub Input Voltage	1.0-20.0 Vpp	1.4-20.0 Vpp		
Isolation Resistors	0.75 Zo +/- 5%	55 + 2%		
Cable Coupling	Shielded Coupler Box	Min 75%		
Output Waveform Requirements	Trapezoid	Trapezoid		
Output Voltage Level	6.0-20.0 Vpp l-l	6.0-9.0 Vpp l-l		
Output Level with RT Fault	1.0-20.0 Vpp l-l	1.4-20.0 Vpp l-l		

Max Zero-Crossing Deviation	25 ns	25 ns		
Rise/Fall Time	100 ns or greater	100-300 ns		
Max Distortion	Not Specified	300 mV peak l-l		
Output Noise	10 mV p-p	5 mV rms		+/- 90 mVp l-l NOTE 6
Output Symmetry	Not Specified	+/- 90 mVp l-l		
Input Waveform	Square to Sinewave	Square to Sinewave		
Input Voltage Level	1.0-20.0 Vpp l-l	1.2-20.0 Vpp l-l		
Common Mode Rejection	+/- 10 V l-g (dc-2 MHz)	+/- 10 V l-g (dc-2 MHz)		
Max Zero-Crossing Deviation	Not Specified	+/- 150 ns		
No Response Input Level	Not Specified	0.0-0.28 Vpp l-l		
Input Impedance	2000 ohms	2000 ohms		
Noise Rejection	1 Error in 10E12 bits	1 Error in 10E7 words		
Message Rejection	1 Error in 10E6 Msg	Not Specified		
Electrical Isolation between Data Buses	Not Specified	45 dB		

Note:

6. Power On/Off noise.

Table 1. Standard Comparison - Part 3

REQUIREMENTS	1553A	1553B	NOTICE 1	NOTICE 2
Transmission Bit Ratepled Stubs	1 Mbit/sec	1 Mbit/sec		
Short Term Stability	0.001%	0.01%	0.001 or 0.01%	
Long Term Stability	0.01%	0.1%	0.01 or 0.1%	
Transmission Continuity	Required			
Transmission Fail Safe (cutoff)	660 µs	800 us		
Superseding Valid Command	Required	Required		
Invalid Data Rejection	Required	Required		
Parity	Odd	Odd		
Cable, twisted, shielded, jacketed	Required	Required		
Twists	12/ft.	4/ft.		
Shield Coverage	80%	75%	90% Min	90% Min
Characteristic Impedance Zo	70 +/- 10 % (1 MHz)	70-85 (1 MHz)	70-85 (1 MHz)	70-85 (1 MHz)
Attenuation	1 dB/100 ft. (1 MHz)	1.5 dB/100 ft. (1 MHz)		
Length	300 ft.	Not Specified		
Capacitance	30 pF/ft.	30 pF/ft.		
Stub Failure Bus Impedance	1.5 Zo	1.5 Zo		
Termination	Characteristic Impedance	Characteristic Impedance		
Connector	Specified	Not Specified		
Connector Polarity	Not Specified	Not Specified	Not Specified	Required NOTE 7
Redundant Data Buses	Not Specified	Optional	Required	Required
Unique Address for RT (external to RT)	Not Specified	Not Specified	Not Specified	Required
Data Wrap-around	Not Specified	Not Specified	Not Specified	Required
RT-RT Validation Timing	Not Specified	Not Specified	Not Specified	57 +/- 3 µs
Referenced Documents	MIL-STD-442 MIL-STD-461 MIL-STD-462 MIL-E-6051	MIL-E-6051		

Note:

7. Positive (high) - center pin; negative (low) - inner ring.

Table of Contents

INTRODUCTION

The following section discusses the individual hardware architectures used to implement UTMC's family of BCRT products (i.e., BCRT, BCRTM, and BCRTMP). Examined in this section are the bus controller (BC), remote terminal (RT), and monitor terminal (M) functions of these devices. The intent of this section is to give the reader an understanding of the various modes of operation.

Architecture descriptions include register usage, interrupt structures, message processing, error recording, DMA activity, and timing diagrams. For detailed timing, pin-outs, or bit descriptions reference the applicable data sheet.

1.0 REMOTE TERMINAL ARCHITECTURE

A similar architecture implements the RT mode of operation for the BCRT, BCRTM, and BCRTMP. The RT is an interface device linking a serial bus and a host microprocessor/subsystem. The serial bus for the BCRT or BCRTM is MIL-STD-1553B. The BCRTMP allows interface to a number of serial buses (reference the data sheet for more detail). The interface includes the following logic blocks: encoder/decoder, error and command recognition (RT-protocol), bus transfer, built-in test, register file, DMA control, interrupt handler, timers, and clock reset.

The UTMC RT family provides all protocol, data handling, message error checking, and memory control functions. Discussed in this section are the following features and functions of the RT:

- 64K x 16 of external address space
- Two-level interrupt structure
- Built-in self test
- Message buffering
- Message time-tagging
- Mode codes
- Illegal command decoding
- Error detection and message status reporting
- Illegal command decoding
- Flexible system interface

2

1.1 Register File

The RT is a register-based architecture configured for operation via a series of register writes. Not all of the internal registers are applicable for RT-mode operation. The RT register file consists of the following registers and decode bits. For all registers bit 15 is the most significant bit, bit 0 the least significant bit.

Register Name	Register Decode BCRT/BCRTMP A(3:0)	Register Decode BCRTM A(4:0)
Control	0000	00000
Status	0001	00001
Descriptor Address	0010	00010
BIT Word	0100	00100
Current Command	0101	00101
Interrupt Log List Pointer	0110	00110
High-Priority Interrupt Enable	0111	00111
High-Priority Interrupt Status/Reset	1000	01000
Standard Interrupt Enable	1001	01001
Remote Terminal Address	1010	01010
BIT Start Command	1011	01011
Reset Command	1100	01100
RT Timer Reset Command	1101	01101
Bus Monitor Control	N/A	01110
Activity Status/Operational Mode	1110 (1)	N/A
Programmable Status/Last Status Word	1111 (1)	N/A

Note:
1. BCRTMP only.

1.1.1 Control Register

In the RT mode operation use the following Control Register bits to enable the device for operation.

Bit Number	Name	Read	Write	Programmed Reset
0	Start Enable	No	Yes	0
7	Channel A Enable	Yes	Yes	U (3)
8	Channel B Enable	Yes	Yes	U
10	BC or RT Select	No	Yes	U
11	Enable External Override	Yes	Yes	U
12	Remote Terminal Time Out (1, 2)	Yes	Yes	U
13	Subaddress 31 (2)	Yes	Yes	U
14	RT-Address 31 (2)	Yes	Yes	U

Notes:
1. Applicable to BCRTMP only.
2. Applicable to BCRTM only.
3. U = unaffected by programmed reset.

1.1.2 Status Register

This read-only register reflects RT status and configuration. All bits are applicable in the RT mode of operation.

Bit Number	Name	Read	Write	Programmed Reset
0	Remote Terminal Active	Yes	No	0
4-1	Reserved	--	--	--
5	Subsystem Fail Indicator	Yes	No	U
6	Channel A/$\overline{B}$	Yes	No	1
7	BC or $\overline{RT}$/$\overline{MT}$ Mode (1)	Yes	No	A (2)
8	Reset Active	Yes	No	0
9	BIT Active	Yes	No	0
10	BUSY Active	Yes	No	0
11	Service Request Active	Yes	No	0
12	Terminal Flag Active	Yes	No	0
13	Dynamic Bus Acceptance	Yes	No	0
14	Remote Terminal or Monitor Active (1)	Yes	No	0
15	Memory Window	Yes	No	1

Notes:
1. Applicable to BCRTM only.
2. A = affected by reset, logic state is determined by other conditions.

1.1.3 Descriptor Address Register

This register contains the data pointer used to link the RT with a descriptor table that resides in the external 64K x 16 memory space. All bits are applicable in the RT-mode operation.

Bit Number	Name	Read	Write	Programmed Reset
15-0	RT Descriptor Block Address	Yes	Yes	U

1.1.4 Built-in Test (BIT) Word Register

This register reports the results of a BIT. The user defines the least significant fourteen bits. Contents of the register are transmitted on receipt of a Transmit BIT Word Mode Code. All bits are read and write.

Bit Number	Name	Read	Write	Programmed Reset
13-0	BIT Word	Yes	Yes	U
14	Channel A Failure	Yes	Yes	U
15	Channel B Failure	Yes	Yes	U

1.1.5 Current Command Register

This register contains the last command the RT received. Since status words and command words have the same sync-field, status words other RTs transmit on the bus are also stored in this register. All bits are applicable, read-only register.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Command Word	Yes	No	U

1.1.6 Interrupt Log List Pointer Register

This register contains the data pointer used to link the RT with the top of the interrupt log list upon initialization. Logging of interrupts results in the RT updating register contents. List resides in the external 64K x 16 memory space. All bits are applicable in RT mode operation.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Interrupt Log List Address	Yes	Yes	U

1.1.7 High-Priority Interrupt Enable Register

Use this register to enable the generation of a High-Priority Interrupt, $\overline{\text{HPINT}}$, upon the occurrence of specified event (e.g., message error or BIT fail). All bits are read and write.

Enable the standard-priority level output pin ($\overline{\text{STDINTL}}$) via bit 0. If a Standard-Priority Interrupt occurs and is enabled, and bit 0 equals logic zero, only the Standard-Priority Interrupt pulse ($\overline{\text{STDINTP}}$) is generated. If bit 0 equals a logic one, both the pulse and the level interrupt signals are generated.

Bit Number	Name	Read	Write	Programmed Reset
0	Standard Interrupt (1)	Yes	Yes	U
1	Message Error (2)	Yes	Yes	U
3	BIT Fail	Yes	Yes	U
4	BIT Complete	Yes	Yes	U
5	Subsystem Fail	Yes	Yes	U
6	Dynamic Bus Control Acceptance	Yes	Yes	U
8	Data Overrun Enable	Yes	Yes	U

Notes:

1. Setting this bit enables the $\overline{\text{STINTL}}$ output pin in addition to $\overline{\text{STINTP}}$ output pin.
2. RT will halt operation if this interrupt is enabled and message error occurs. To restart, clear interrupt in High-Priority Status/Reset Register (bit 1) before the next 1553 command arrives.

1.1.8 High-Priority Interrupt Status/Reset Register

Upon the occurrence of an event that generates a High-Priority Interrupt the appropriate bit in this register is set to a logic one and the $\overline{\text{HPINT}}$ pin is asserted. Once the interrupt is serviced, clear the $\overline{\text{HPINT}}$ pin by writing a logic one to the appropriate bit of this register. Writing a logic one also resets the bit in the register. A logic one written to a bit location containing zero will not result in the generation of an interrupt. All bits are read and write.

Bit Number	Name	Read	Write	Programmed Reset
0	Standard Interrupt	Yes	Yes	0
1	Message Error	Yes	Yes	0
3	BIT Fail	Yes	Yes	0
4	BIT Complete	Yes	Yes	0
5	Subsystem Fail (1)	Yes	Yes	0
6	Dynamic Bus Control Acceptance	Yes	Yes	0
8	Data Overrun Enable	Yes	Yes	0

Note:
1. Generated on the assertion of external pin SSYSF.

1.1.9 Standard-Priority Interrupt Enable Register

Use this register to enable the generation of a Standard-Priority Interrupt, $\overline{\text{STDINTL}}$ or $\overline{\text{STDINTP}}$, upon the occurrence of specified event (e.g., message error or illegal command). All bits are read and write.

Bit Number	Name	Read	Write	Programmed Reset
1	Message Error	Yes	Yes	U
4	Illegal Command	Yes	Yes	U
5	Illegal Broadcast Command	Yes	Yes	U

1.1.10 Remote Terminal Address Register

The Remote Terminal Address Register is used to control bits in the RT's status word response, along with defining the mode of operation and the RT's terminal address.

Bit Number	Name	Read	Write	Programmed Reset
0	Remote Terminal Address Bit 0	(1)	(1)	U
1	Remote Terminal Address Bit 1	(1)	(1)	U
2	Remote Terminal Address Bit 2	(1)	(1)	U
3	Remote Terminal Address Bit 3	(1)	(1)	U
4	Remote Terminal Address Bit 4	(1)	(1)	U
5	Remote Terminal Address Parity Bit	(1)	(1)	U
6	Remote Terminal Address Parity Error	Yes	No	U
7	LOCK Indicator	Yes	No	U
8	BC or RT Select	Yes	No	U
9	Busy Mode Enable (2)	Yes	Yes	U
10	Service Request	Yes	Yes	U
11	Terminal Flag	Yes	Yes	U
12	Dynamic Bus Control Acceptance	Yes	Yes	U
13	Subsystem Fail	Yes	Yes	U
14	Busy	Yes	Yes	U
15	Instrumentation	Yes	Yes	U

Notes:

1. If the LOCK input pin is a logic one, this bit is read-only. Bit reflects status of the corresponding external Remote Terminal Address Bus bit or Parity bit. If LOCK equals logic zero, this bit is read and write.
2. The Status Word bit is not set/reset until the part actually enters/exits the busy mode. The RT does not enter or exit the busy mode until current command processing is complete (i.e., remote terminal inactive). This Register bit is written to at any time, but it will not reflect being set/reset until the RT enters/exits busy mode.

1.1.11 BIT Start Register

Writing any data pattern to this 16-bit register invokes the built-in self-test routine. Self-test takes 100 µs. The results of the test are recorded in the BIT Word Register. For a detailed description of BIT see 16.0, Built-In-Test of this section. The register is write only.

Bit Number	Name	Read	Write	Programmed Reset
15-0	BIT Start	No	Yes	N/A

1.1.12 Programmed Reset Register

Writing any data to this 16-bit register invokes a programmed reset of the RT. Reset takes 1 µs. Programmed reset stops operation of the RT. The register is write only.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Programmed Reset	No	Yes	N/A

1.1.13 RT Time-Tag Reset Register

Writing any data pattern to this 16-bit register resets the 8-bit time-tag counter to zero. The register is write only.

Bit Number	Name	Read	Write	Programmed Reset
15-0	RT Time-Tag Reset	No	Yes	N/A

1.1.14 Bus Monitor Register (BCRTM Only)

Bit 15 selects the monitor mode of operation. For RT operation set bit 15 equal to logic zero. When read, this bit reflects the current mode of operation of BCRTM, read to verify the BCRTM is in the RT mode. The bit is read and write.

Bit Number	Name	Read	Write	Programmed Reset
12-0	Reserved			U
13	Monitor Mode only	N/A	N/A	N/A
14	Monitor Mode only	N/A	N/A	N/A
15	Bus Monitor Control Register	Yes	Yes	U

1.1.15 Activity Status/Operational Mode Register (BCRTMP Only)

This register augments the BCRTMP Control Register; bits implemented in this register control special features, protocol, and status.

Bit Number	Name	Read	Write	Programmed Reset
0	MD0	(1)	(1)	U
1	MD1	(1)	(1)	U
2	MD2	(1)	(1)	U
3	MD3	(1)	(1)	U
4	MD4	(1)	(1)	U
5	MD5	(1)	(1)	U
6	MD6	(1)	(1)	U
7	$\overline{\text{WRAPEN}}$	(1)	(1)	U
8	$\overline{\text{ALTWRAP}}$	(1)	(1)	U
9	WRAPF	Yes	Yes	U
10	Bus A	Yes	Yes	U
11	Bus B	Yes	Yes	U
12	Stop Enable	Yes	Yes	U
13	Ignore T/R	Yes	Yes	U
15-14	Reserved	--	--	--

Note:
1. If the LOCK pin is a logic 1 the bit is read only. If the LOCK pin is a logic one the bit is read and write.

1.1.16 Programmable Status/Last Status Word Register (BCRTMP Only)

This dual-mode register controls the outgoing status word and reads the last transmitted status word. The register bits also control special functions used to implement multiple protocols. All bits are read and write.

Bit Number	Name	Read	Write	Programmed Reset
0	Terminal Flag	Yes	Yes	U
1	Programmable Status Bit 18 Last Status Word Bit 18	Yes	Yes	U
2	Programmable Status Bit 17 Last Status Word Bit 17	Yes	Yes	U
3	Programmable Status Bit 16 Last Status Word Bit 16	Yes	Yes	U
4	Programmable Status Bit 15 Last Status Word Bit 15	Yes	Yes	U
5	Programmable Status Bit 14 Last Status Word Bit 14	Yes	Yes	U
6	Programmable Status Bit 13 Last Status Word Bit 13	Yes	Yes	U
7	Programmable Status Bit 12 Last Status Word Bit 12	Yes	Yes	U
8	Programmable Status Bit 11 Last Status Word Bit 11	Yes	Yes	U
9	Programmable Status Bit 10 Last Status Word Bit 10	Yes	Yes	U
10	Message Error	Yes	Yes	U
11	Forced Busy	Yes	Yes	U
12	Automatic Data Ready	Yes	Yes	U
13	Automatic Terminal Flag Bit Enable Option 2	Yes	Yes	U
14	Automatic Terminal Flag Bit Enable Option 1	Yes	Yes	U
15	Immediate Clear Mode Enable	Yes	Yes	U

2.0 Descriptor Block

To process messages the RT uses data supplied in the internal registers along with data stored in external memory. The RT accesses three words stored in external memory called a Descriptor Block. The Descriptor Block is accessed at the beginning and end of command processing. Sequentially entered into memory, multiple Descriptor Blocks form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host for the RT allocates 320 consecutive memory spaces for the subaddress and mode code descriptor table. For proper operation locate the top of the descriptor table on an I x 512 address boundary, where I is an integer value (I can equal zero).

Defined and entered into memory by the host, the RT is linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a control word, Message Status Pointer, and Data List Pointer. A fourth word is allocated in each Descriptor Block but is not accessed by the RT. Each subaddress is assigned a descriptor block for receive and transmit commands. Mode codes with data and without data share a common Descriptor Block.

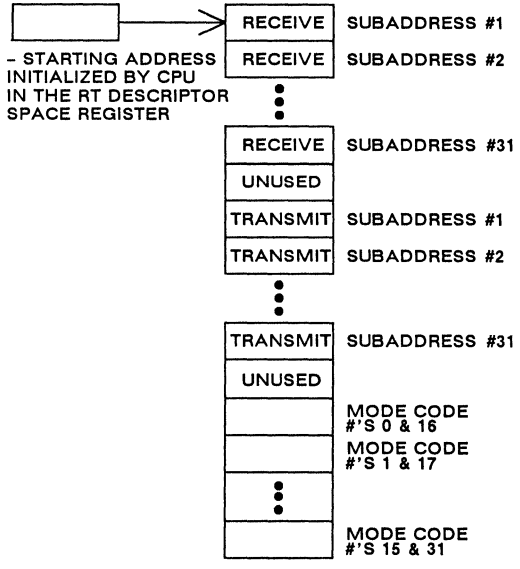
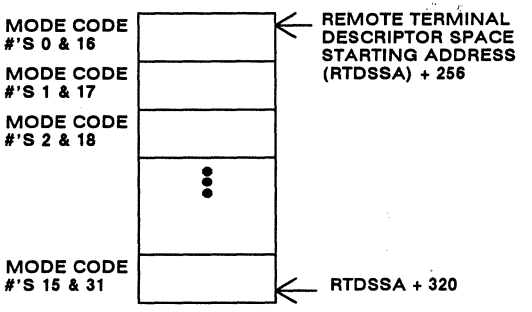


Figure 5a. Descriptor Space



Note:
Mode code descriptor blocks are also provided for reserved mode codes but have no associated predefined BCRTM operation.

Figure 5b. (RT) Mode Code Descriptor Space

Control word information allows the RT to illegalize commands, generate interrupts, and buffer messages on a subaddress basis. To enable an interrupt or illegalize a subaddress, set the appropriate bit in the control word. The Message Status Pointer links the RT to a Message Status Word list. Information contained in the Message Status Word pertains to each message the RT processes. Information includes word count, time-tag value, broadcast flag, message error, and status of subsystem flag during message transaction (i.e., outgoing status word). The Data List Pointer links the RT to data for message processing. For a receive command the Data List Pointer is read to determine the top of the data buffer. The RT stores data words sequentially from the top of data buffer (e.g., 0100, 0101, 0102, 0103, etc.). When processing a transmit command, the Data List Pointer is read to determine where data words are retrieved. The RT retrieves data words sequentially from the address the Data List Pointer designates. Within the Descriptor Block the control word is entered first, followed by the Message Data List Pointer, and the Data List Pointer; the fourth entry is allocated but not used.

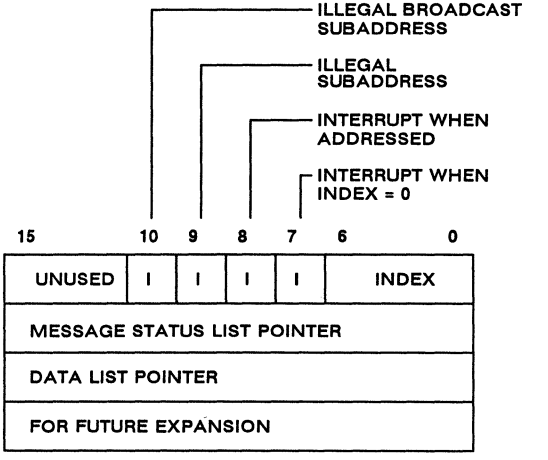


Figure 6a. Remote Terminal (RT) Subaddress Descriptor

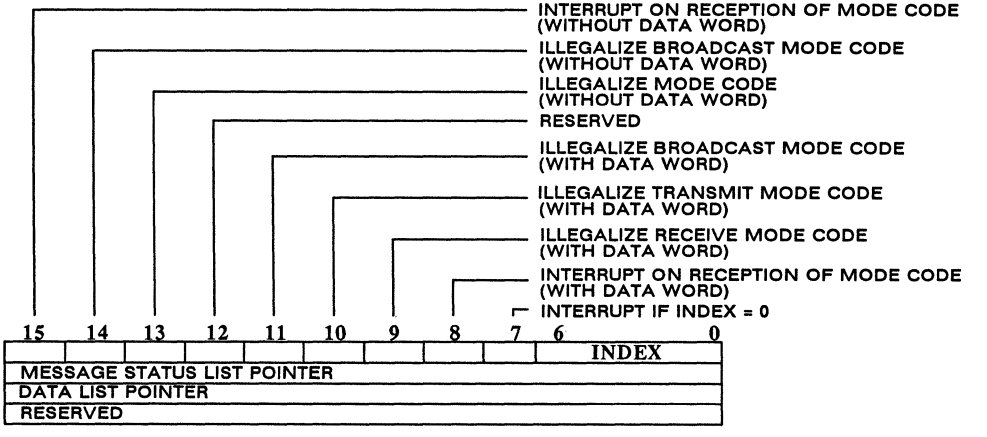


Figure 6b. (RT) Mode Code Descriptor

3.0 DMA Activity

Once given ownership of the local bus (i.e., DMAG asserted) the RT will perform either a single access or multiple accesses (BURST). The following section discusses what types of accesses occur during message processing. For a graphical description of DMA activity please reference 15.0 of this section (Typical Timing Diagrams) or the applicable data sheet.

When performing multiple memory accesses the RT asserts $\overline{\text{DMACK}}$ and BURST output signals. After asserting the BURST signal the RT performs either 2, 3, or 4 memory acceses. The number of memory accesses is dependent on the operation the RT is performing. Three different burst memory accesses ocurr in RT mode operation: Descriptor Block read, Interrupt Log, and Descriptor Block update.

To begin message processing the RT performs a Descriptor Block read. A Descriptor Block read requires three memory accesses to fetch the control word, Message Status List Pointer, and Data List Pointer. Upon completion of any burst accesses the RT surrenders the local bus by negating the $\overline{\text{DMACK}}$ output.

The second burst scenario corresponds to the RT entering an interrupt event into the interrupt log list (i.e., Interrupt Log). An interrupt log requires three memory accesses to memory. The first access is a memory write of the Interrupt Status Word. Contained in the Interrupt Status Word is information pertaining to the event that resulted in the interrrupt (e.g. message error, illegal command, etc.). Following the Interrupt Status Word write is a Descriptor Pointer write. The Descriptor Pointer is stored in the interrupt log list to allow the host to calculate which subaddress or mode code generated the interrupt. The third memory access is a fetch of the Tail Pointer; the RT updates the Interrupt Log List Pointer to contain the contents of this memory location.

A Descriptor Block update is the third type of burst access. Containing up to four memory accesses, the Descriptor Block update writes the Message Status Word, Data List Pointer, Message Status List Pointer, and control word. If message indexing is not invoked, the Data List Pointer, Message Status List Pointer, and control word are not updated. Message indexing is not invoked when the control word's seven least significant bits equal zero.

The RT performs single memory accesses to read or write data words from memory. In the case of no message indexing, the Message Status Word is entered into memory during a single memory access.

4.0 Command Illegalization

The host controls command illegalization via the descriptor control word. The control word instructs the RT to illegalize commands on a subaddress or mode code basis. In response to an illegal command the RT transmits a status word with the Message Error bit set to a logic one. For a transmit command no data is sent with the outgoing status word. If the illegal command is to receive data, the associated data is not stored. The following is a list of conditions that the RT can illegalize:

Subaddress Descriptor Control Word:

- Illegal Broadcast Command (1)
- Illegal Receive Subaddress
- Illegal Transmit Command

Mode Code Descriptor Control Word:

- Illegal Broadcast Mode Code (with data word)
- Illegal Broadcast Mode Code (no data word)
- Illegal Mode Code (with data word)
- Illegal Mode Code (no data word)
- Illegal Transmit Mode Code (with data)
- Illegal Receive Mode Code (with data)

Note:

1. Although the transmit subaddress control word has the ability to illegalize a broadcast transmit command, MIL-STD-1553B does not support the command and the RT automatically illegalizes this command.

5.0 Remote Terminal Address

Definition of the remote terminal address is controlled by either hardware or software. For a hardware assignment, the terminal address is entered into the RT from RTA(4:0). Asserting $\overline{\text{MRST}}$ latches the RT's terminal address from pins RTA(4:0) and Parity bit RTPTY. The terminal address parity is odd; input RTPTY is set to a logic state to satisfy this requirement. A logic one on Remote Terminal Address Register bit 6 indicates incorrect terminal address parity. Operation of the RT does not begin until the parity error is cleared.

To assign the terminal address via software the host writes to the Remote Terminal Address Register six least significant bits. The new terminal address is loaded on the completion of the write cycle (i.e., $\overline{\text{WR}}$ negated). Software programming the remote terminal address is allowed only when the LOCK pin is negated (i.e., LOCK equal logic zero). Assertion of the LOCK pin allows programming the terminal address through hardware only.

The system locks the BCRTM device into the RT mode either by hardware or software. A software lock disables the remote terminal from entering the monitor mode due to a software data error. The hardware lock is through the LOCK input pin. A software lock is invoked by clearing the Bus Monitor Control Register followed by a write to the Control Register. Please note that a programmed reset disables the software lock between the remote terminal mode and monitor mode of operation.

6.0 RT-RT Transfer Compare (Receive Mode)

Internal RT-to-RT terminal address compare logic checks that the incoming status word's terminal address matches the terminal address of the transmitting RT specified in the transmit command word. An incorrect match results in setting the Message Error bit and suppressing transmission of the status word (RT-to-RT transfer time-out = 56 μs).

7.0 Receive Message Processing

After receipt of valid receive command the BCRT performs a Descriptor Block read for the designated subaddress or mode code. The RT fetches the control word, Message Status List Pointer, and Data List Pointer during a burst DMA cycle. The Descriptor Block contains information that the RT uses and creates during message processing (i.e., Data List Pointer, Message Status Word). The RT stores all three descriptor words internally.

The control word instructs the RT how to process the incoming message (i.e., interrupt generation, command illegalization, and message indexing). The Data List Pointer designates where in the 64K x 16 memory space that receive data is stored. During the Descriptor Block read, the RT loads the contents of the Data List Pointer location into an internal register. The internal register contents are then used, as an address, to store data words being received. The internal register is incremented, by one, as data words are received.

Upon receipt and storage of all data words the RT generates a Message Status Word. The Message Status Word is stored at the memory address the Descriptor Block Message Status List Pointer defines. If message indexing is invoked the RT rewrites (updates) the Data List Pointer and Message Status List Pointer. The Data List Pointer is updated with the final incremented value after all data words are received. The Message Status List Pointer is incremented by one and written back into the Descriptor Block. The Control Word index field (bits 6 through 0) is decremented by one and rewritten into the Descriptor Block memory. The RT does not update the Message Status List Pointer, Data List Pointer, and control word if message indexing is not invoked. However, the Message Status Word is always generated and written. Consider the preceding sequence of events and memory accesses a Descriptor Block update. At this point message processing is completed.

Please note that the Data List Pointer is not decremented if a message error condition is observed during message processing. The index field of the control word is decremented for messages that contain message errors. Also note that mode codes without data do not involve a descriptor block update.

7.1 Receive Message Indexing

The RT has the ability to index up to 128 messages at a subaddress or mode code. The index buffer size is defined by the value assigned in the descriptor control word. The control word index is decremented each time a message is processed. The RT buffers messages until the index field is decremented to zero. To signal a need for host servicing, the RT can generate an interrupt when the specified message length is reached (i.e., index decremented to zero).

The RT generates a Message Status Word for each message transaction to aid the host in processing messages from the buffer. The Message Status List Pointer, read from the Descriptor Block, defines the storage location for the Message Status Word. Due to the increment of the Message Status List Pointer, at the end of message processing the RT stores the Message Status Word sequentially in memory (Message Status Word Log). For example, if the RT indexes 5 messages (i.e., Control Word Index Field equal 0000100) and the Message Status List Pointer is initially 100 (hex); Message Status Words are stored at memory locations, 100 (hex), 101 (hex), 102 (hex), 103 (hex), and 104 (hex). If enabled, an interrupt is generated on the transition of the control word index field from logic one to logic zero. Once the index is decremented to zero the Message Status List Pointer is not updated. Messages processed after the index is zero result in an over-write of the last Message Status Word entered in the Message Status Word Log.

The Data List Pointer is used similarly to the Message Status List Pointer during message processing. As the RT validates and stores incoming data words the Data List Pointer is incremented internally. Upon receipt of the correct number of data words the Data List Pointer is updated in the Descriptor Block (i.e., Descriptor Block update). The RT continues to update the Data List Pointer, after message completion, until the index is decremented to zero. Once the index has reached zero the buffer is considered full and the Data List Pointer is not updated. Messages processed after the index is zero result in an over-write of the last data words entered into the buffer. See the Application Note section of this handbook for examples of receive command message indexing.

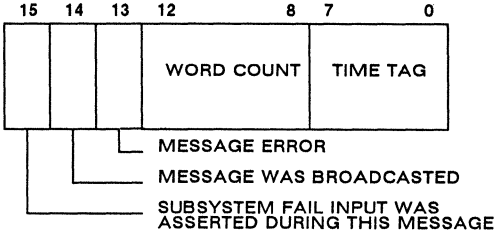


Figure 7. Message Status Word

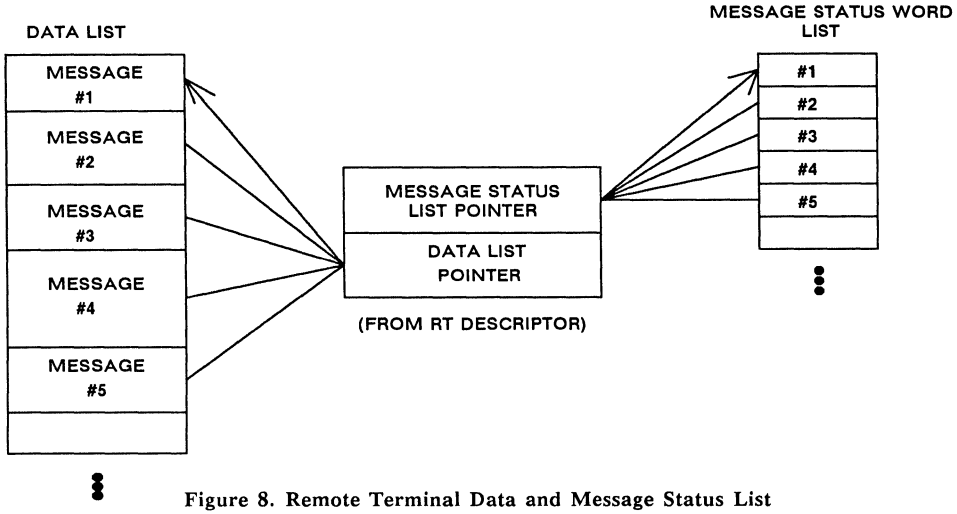


Figure 8. Remote Terminal Data and Message Status List

8.0 Transmit Message Processing

After receipt of a valid transmit command the BCRT performs a Descriptor Block read for the designated subaddress or mode code. The RT fetches the control word, Message Status List Pointer, and Data List Pointer during a burst DMA cycle. The Descriptor Block information is used in the same manner as for a receive command.

The RT begins message processing by transmitting a status word. The RT then uses the Data List Pointer, as an address, to retrieve the first data word. The Data List Pointer is incremented after each memory access, therefore when processing multiple word commands, data is retrieved sequentially from memory. It is the responsibility of the host or subsystem to enter data words, for transmission, in the correct memory locations.

Upon transmission of all data words the RT generates a Message Status Word and performs a Descriptor Block update. Reference section 7.0 for details of the Descriptor Block update.

8.1 Transmit Message Indexing

The message indexing mechanics for transmit commands work the same as for receive commands. The Control Word index field determines the number of messages that the RT will transmit without service from the host. Once the prescribed number of messages is transmitted, the RT can generate an interrupt requesting service. In order to implement transmit message indexing the RT must know the number of data words in each transmit command it plans to process.

When configuring the RT memory to transmit multiple commands the host or subsystem places data packets sequentially in memory. The data packet contains "N" data words for each transmit command the RT is expecting to process. The Data List Pointer accesses consecutive data words in the data packet for transmission. Data List Pointer and Message Status List Pointer updating is performed as described for receive command (section 7.1). See Application Note section of this handbook for examples of transmit command indexing.

9.0 Interrupt Architecture

The RT can generate two levels of interrupts--Standard-Priority and High-Priority Interrupts. Use these interrupts to signal the host that a user-selected event has taken place. Selectable events include: index equals zero, illegal command, message error, etc. The host interfaces to the RT interrupt architecture via the interrupt enable, status/reset registers, and outputs $\overline{\text{STDINTL}}$, $\overline{\text{STDINTP}}$, and $\overline{\text{HPINTP}}$.

During initialization of the RT the Interrupt Log List Register is loaded. The contents of the register define the start of the Interrupt Log List. On the occurrence of each standard-priority interrupt the RT stores two words into the list and retrieves a third word. The burst of three DMAs (read, read, write) is defined as an interrupt log. The first word written into memory is the Interrupt Status Word; this 16-bit word contains information on the interrupt event. The second 16-bit word stored in memory defines which subaddress or mode code generated the interrupt. The third word is loaded into the Interrupt Log List Register and is used as an address to store the next interrupt log entry. After the interrupt log is completed the standard-priority pulse or level ($\overline{\text{STDINTL}}$ or $\overline{\text{STDINTP}}$) is asserted. Output $\overline{\text{STDINTL}}$ is asserted until High-Priority Interrupt Status/Reset

Register bit 0 is cleared. The interrupt log occurs after the last data word is retrieved or stored into memory. If the interrupt is due to a message error, the interrupt is logged after the message error is observed.

Interrupt Status Word Applicable Bits:

Bit #	Description
1	Message error condition occured during message processing.
4	Command received was illegalized in descriptor control word.
5	Broadcast command received was illegalized in descriptor control word.
6	Mode code without data word was received.
7	Mode code with data was received or a subaddress event occurred. Subaddess events include interrupt when addressed or index equals zero.
8	Indicates the ME bit of transmitted status word was set to a logic one. Message error or illegal command condition exists.
15	Bit always set to a logic one by the RT. Bit indicates that the RT has accessed this particular memory location.

The RT does not log High-Priority Interrupts into the Interrupt Log List. High-Priority Interrupts are logged into the High-Priority Interrupt Status/Reset Register. To signal the occurrence of a High-Priority event output $\overline{\text{HPINT}}$ is asserted immediately after the event is observed. $\overline{\text{HPINT}}$ stays asserted until the host clears the applicable bit the High-Priority Interrupt Status/Reset Register.

Enabling High-Priority Interrupts for message errors immediately halts the RT from processing messages. To restart the RT, clear the appropriate bit in the High-Priority Interrupt Status/Reset Register (i.e., bit that reflects interrupt occurred).

10.0 RT Error Detection

In accordance with MIL-STD-1553B, the remote terminal can detect various Message Error conditions. Error checking occurs on Manchester waveforms and word formats. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

11.0 Status Signals

The RT has eight input/output signals that provide the host with RT status information. The following is a description of each signal:

Signal Name	Type	Description
$\overline{\text{HPINT}}$	Output	Signals the occurrence of a High-Priority Interrupt event (active low).
$\overline{\text{STDINTL}}$	Output	Asserted on the occurrence of Standard-Priority Interrrupt event (active low).
$\overline{\text{STDINTP}}$	Output	333 ns pulse indicating a priority interrupt event (active low).
$\overline{\text{COMSTR}}$	Output	Asserted upon the recognition and validation of a command to the RT (active low).
$\overline{\text{TIMERON}}$	Output	Signal used to implement MIL-STD-1553B fail-safe timer (760 μs pulse).
CHA/$\overline{\text{B}}$	Output	Asserted upon validation of a command; indicates on which channel the command was received.
BCRTF	Output	Output indicates that the RT has failed internal self-test (active high). Examine BIT Word Register to further evaluate results of tests.
SSYSF	Input	Direct link to the subsystem flag of the MIL-STD-1553 status word. When asserted by the subsystem or host the outgoing status word bit has the subsystem flag bit set (active high).

12.0 Encoder And Decoder

The RT interfaces directly to a bus transmitter/receiver (i.e., transceiver) via the RT Manchester II encoder/decoder. Interface to the bus transceiver requires a zero idle state. The RT receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse, Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RT processes each incoming data word for correct format and checks the control logic for correct word count and contiguous data. If invalid data is detected, the Message Error bit or interrupt is asserted, the RT ceases processing the remainder (if any) of the message, and the status word is suppressed from transmission. Upon command recognition and validation, the external status outputs become valid. Reception of illegal commands does not suppress status word transmission, but sets the ME bit in the response.

13.0 Busy Mode

Enter the BUSY mode of operation by asserting Remote Terminal Address Register bit 9 (logic one). Once in the BUSY mode the RT inhibits the storage and retrieval of data from the subsystem. Upon reception of all valid commands the RT responds with a status word only (no data). The BUSY bit in the outgoing status word is automatically set to a logic one indicating the RT is BUSY.

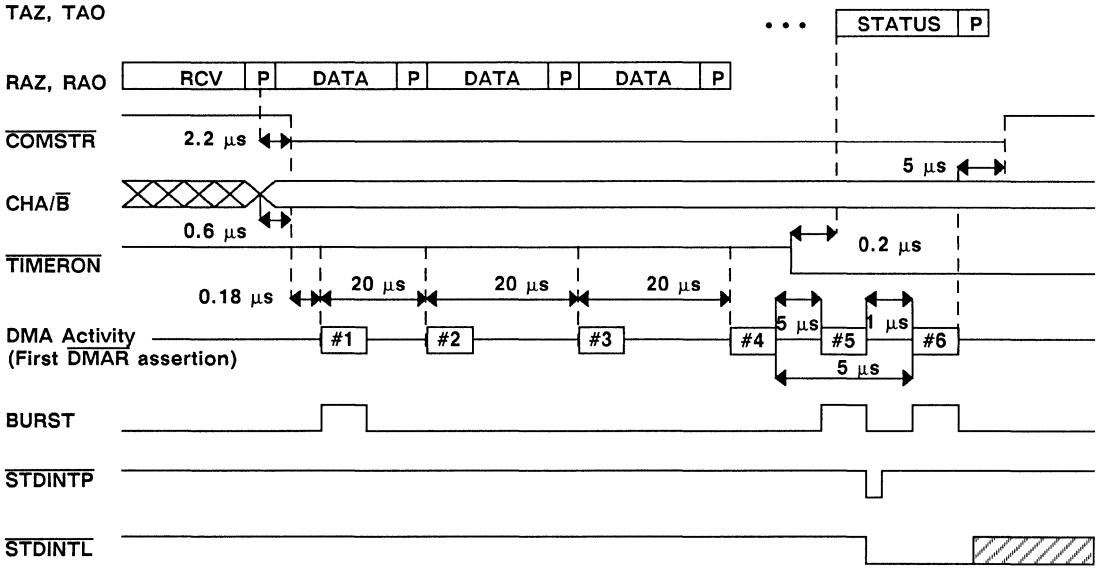
The RT exits the BUSY mode when Remote Terminal Address Register bit 9 is cleared (logic zero). The RT asserts the status word BUSY bit until a receive, transmit, or mode code command is received. Neither Transmit Last Command or Transmit Status word clears the BUSY bit of the status word.

14.0 Status Word Control

Use the Remote Terminal Address Register to control various bits in the outgoing status word: Instrumentation, Busy, Subsystem Fail, Dynamic Bus Control Acceptance, Terminal Flag, and Service Request. The Subsystem Fail bit is also asserted by hardware input SSYSF. The RT protocol logic controls the Message Error bit in the status word.

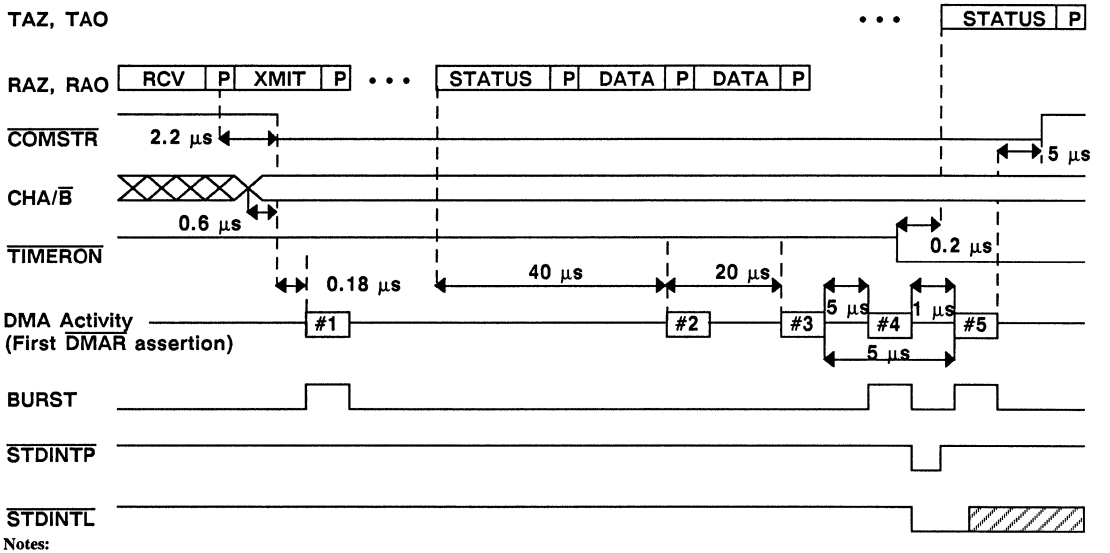
15.0 Typical Timing Diagrams

The following timing diagrams show DMA activity and status signals during message processing.



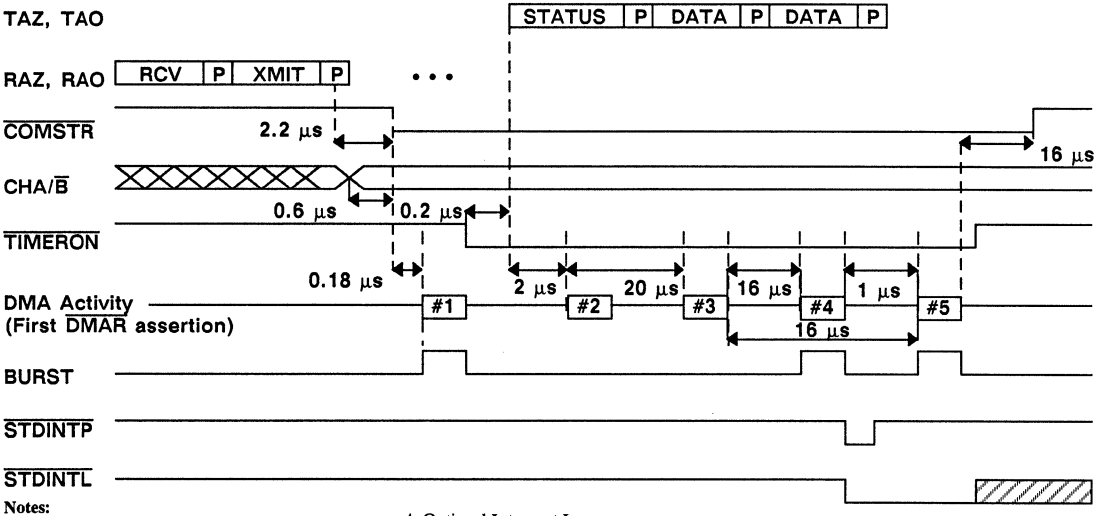
Notes:
1. Descriptor read.
2. Data word write.
3. Data word write.
4. Data word write.
5. Optional Interrupt Log.
6. Descriptor update.

Figure 9. Typical Receive Command (RT Mode)



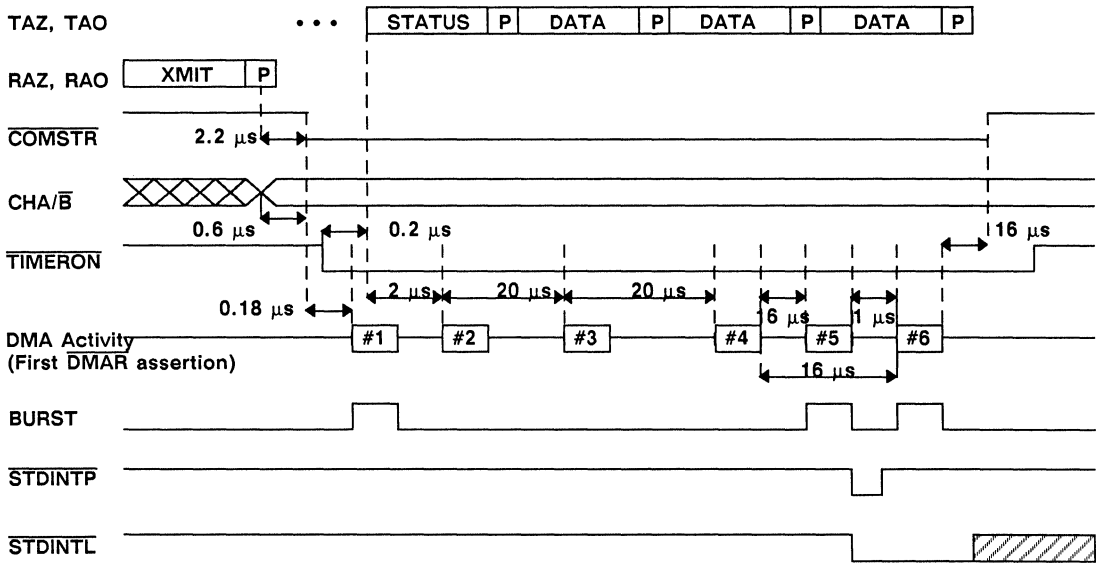
Notes:
1. Descriptor read.
2. Data word write.
3. Data word write.
4. Optional interrupt log.
5. Descriptor update.
6. 9 µs pulse aligned with second command word and status word.

Figure 10. Typical Timing for RT-RT Transfer (receive) (RT Mode)



Notes:
1. Descriptor read.
2. Data word read.
3. Data word read.
4. Optional Interrupt Log.
5. Descriptor update.

Figure 11. Typical Timing for RT-RT Transfer (transmit) (RT Mode)



Notes:
1. Descriptor read.
2. Data Word read.
3. Data Word read.
4. Data Word read.
5. Optional Interrupt Log.
6. Descriptor update.

Figure 12. Typical Timing for Transmit Command (RT Mode)

16.0 Built-In-Test

Built-in self-test of the BCRTM exercises the encoders, decoders, parallel-to-serial, and serial-to-parallel conversion circuits. Initiate self-test by writing to the BIT Start Register (BC, MT modes) or on receipt of initiate self-test mode code. The test duration is 100 µs, and covers aproximately 25% of the device.

When initiating self-test via the BIT Start Register, stop the BC, RT, or MT before starting the test. The device is stopped via a programmed reset. After completion of BIT issue a start enable (Control Register bit 0) to resume operation. A mode code initiated BIT does not require a programmed reset before BIT or re-start upon completion.

The BCRTM's self-test performs an internal wrap-around test between its Manchester encoder and its two Manchester decoders. This test consists of having the BCRTM's Manchester encoder transmit a pattern of alternating ones and zeros (5555 hex) to the Manchester decoder under test. After the Manchester decoder receives the pattern, the BCRTM does a simple comparison of the received word versus the transmitted word. If there is a match, the test is successful. Any mismatch in the bit patterns results in the BCRTM flagging an error condition in the BIT Word Register.

The BCRTM then swaps ones and zeroes in the test pattern and wraps this word (AAAA hex) from the Manchester decoder under test. Once again, after the BCRTM receives this word, it compares the received word versus the transmitted word. The test result is logged into the BIT Word Register. The same two tests are then performed on the alternate Manchester decoder.

The BCRTM can signal the end of built-in-test by asserting a high-priority interrupt. The host monitors BIT in progress via the Status Register.

17.0 RT Design Example

17.1 Introduction

The following paragraphs outline the configuration of a UT1553B BCRTM by a UT1750AR microprocessor. The UT1750AR is operating in the RISC mode: the BCRTM is configured for operation as a remote terminal (RT). Examples show register initialization, descriptor setup, memory map, and message buffering. For more detailed information on the BCRTM or UT1750AR please reference the applicable data sheet or application note.

17.2 Memory Map

The Remote Terminal Descriptor Space is located on an I x 512 boundary in memory. For this example I is equal to zero: the first Descriptor Block resides at 0000 (hex). The next 320 (decimal) sequential locations contain descriptor information to assist the RT in processing MIL-STD-1553 (1553) commands. RT internal registers (18) follow the Descriptor Space sequentially in memory. To perform message recovery when indexing is invoked, the initial Data List Pointer and Message Status List Pointer value for each Descriptor Block is stored in memory, reserve 156 sequential locations for this task. See UTMC's application notes for examples of message recovery with message indexing.

0000 (hex) to 013F (hex)	Remote Terminal Descriptor (320)
0140 (hex) to 0152 (hex)	RT Internal Registers (18)
0153 (hex) to 01EE (hex)	Receive Data List Pointers (31) Transmit Data List Pointer (31) Receive Message Status List Pointer (31) Transmit Message Status List Pointer (31) Mode Code Data List Pointer (16) Mode Code Message Status List Pointer (16)
01EF (hex) to 01FF (hex)	Scratch Pad

Data List Pointers contained in the Descriptor Space link the RT to the memory map. For this example each receive subaddress is allowed 256 (decimal) memory locations. These memory locations allow the subaddress to buffer a maximum of 8 messages of 32 words each. Data List Pointers contained in Descriptor Blocks begin at 0200, 0300, 0400, 0500, etc. Message Status List Pointers begin at 24E0, 24E8, 24EF, etc. For 31 subaddresses, reserve 7.9K memory locations. Reserve 32 memory locations for each subaddress (31) for transmit command processing (31 x 32 = 992). Mode codes with data require allocation of one memory location for each mode code. The RT supports 16 mode codes with data.

0200 (hex) to 20FF (hex)	Receive Subaddress Data Space (31 x 256)
2100 (hex) to 24CF (hex)	Transmit Subaddress Data Space (31 x 32)
24D0 (hex) to 24DF (hex)	Mode Code Data Space (16 x 1)

Assign 8 memory locations, per subaddress, for Receive Message Status Words. Transmit subaddresses and mode codes require allocation of 1 location since indexing is not used.

24E0 (hex) to 25D7 (hex)	Receive Subaddress Message Status Space (31 x 8)
25D8 (hex) to 25F6 (hex)	Transmit Subaddress Message Status Space (31 x 1)
25F7 (hex) to 2606 (hex)	Mode Code Message Status Space (16 x 1)
2607 (hex) to 26FF (hex)	Scratch Pad
2700 (hex) to 27FF (hex)	Interrupt Log List

A circular buffer starting at 2700 (hex) is reserved to store interrupt log list information.

17.3 Descriptor Control Word

The 16-bit subaddress control word contains a 7-bit index field, 4-bit illegalization and interrupt field, and 5 reserve bits. The next section describes use of index field and interrupt when index equals zero (i.e., bits 0 to 7). Bits 9 and 10 allow the subsystem to illegalize subaddresses and broadcast commands associated with a subaddress. Bit 8 allows the subsystem to generate an interrupt when the subaddress is addressed in the command word. Program unused bits 11 through 15 to logic one or zero. For more detailed description on the use of these bits, reference the BCRTM data sheet.

A mode code descriptor control word is similiar to the subaddress control word with the following exceptions. Bits 7 through 15 designate various interrupt and illegalization criteria. Note that mode codes with and without data share Descriptor Blocks (i.e., control word, Data List Pointer, and Message Status List Pointer). Therefore the control word has provisions to illegalize or interrupt mode codes with or without data as well as interrupt when addressed. Mode codes without data do not use the data list pointer or update a message status word.

17.4 Message Buffering

Each subaddress can index/buffer a maximum 128 individual messages via the control word index field (7-bit field). Memory space is then allocated to insure that the maximum number of data words does not exceed the buffer size. The data space (i.e., buffer) for receive messages was sized to hold 256 data words. Eight messages of 32 words each will fill the data space, therefore the index field of the descriptor control word is set to 0000111. The index field for mode codes and transmit commands was set to zero (i.e., 0000000) therefore disabling indexing.

Bit 7 of the Descriptor Block control word enables an interrupt to signal the subsystem or microprocessor that a subaddress has processed "N" messaages. Standard priority interrupt outputs STDINTL and STDINTP assert when the index count goes from 0000001 to 000000 (i.e., seventh message completed).

Example Descriptor Block

An example of the Descriptor Block for receive subaddress 1 and 2 follows:

0000 (hex)	0087
0001 (hex)	0200
0002 (hex)	24E0
0003 (hex)	0000
0004 (hex)	0087
0005 (hex)	0300
0006 (hex)	24E8
0007 (hex)	0000

An example of the descriptor block for transmit subaddress 1 and 2 follows:

0080 (hex)	0100 (hex)
0081 (hex)	2100 (hex)
0082 (hex)	25D8 (hex)
0083 (hex)	0000 (hex)
0084 (hex)	0100 (hex)
0085 (hex)	2120 (hex)
0086 (hex)	25D9 (hex)
0087 (hex)	0000 (hex)

An example of the descriptor block for the first and second mode code follows:

0100 (hex)	0100 (hex)
0101 (hex)	24D0 (hex)
0102 (hex)	25F7 (hex)
0103 (hex)	0000 (hex)
0104 (hex)	0100 (hex)
0105 (hex)	24D1 (hex)
0106 (hex)	25F8 (hex)
0107 (hex)	0000 (hex)

17.5 Register Initialization

The BCRTM has 18 internal registers that control message processing. This section reviews the initialization of registers required to begin command processing. For more detailed bit descriptions, reference the BCRTM data sheet.

Example RT Setup (1):

#0 Control Register

0110 0001 1000 0000 6180 (hex)

#2 Remote Terminal Descriptor Space Address Register

0000 0000 0000 0000 0000 (hex)

#6 Interrupt Log List Register

0200 0111 0000 0000 2700 (hex)

#7 High Priority Interrupt Enable Register

0000 0000 0000 0000 0000 (hex)

#8 High Priority Interrupt Status/Reset Register

0000 0000 0000 0000 0000 (hex)

#9 Standard Priority Enable Register

0000 0000 0000 0000 0000 (hex)

#10 Remote Terminal Address Register (2)

0000 0000 0000 0000 0000 (hex)

#14 Bus Monitor Control Register

0000 0000 0000 0000 0000 (hex)

Notes:

1. Initializing the RT as shown above is a minimum configuration.
2. Assumes that the remote terminal address is loaded via external address bus RTA(4:0).

RISC Subroutines

The following UT1750AR RISC machine code shows examples of subroutines that configure the RT for operation. The RISC port (1M x 16) of the UT1750AR allows accesses to non-volatile memory for configuration. Information read from the non-volatile memory is stored in the RT internal registers and RAM locations residing on the UT1750AR data port (64K x 16).

```
DESCR_INT:                  ; Descriptor Space
                              Initialization
            mov R2, 0000    ; Top of RAM desrciptor
                              space
            mov R0, 0010    ; Top of ROM

LOOP1:      lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in RAM
            addu R0, 0001   ; increment ROM counter
            addu R2, 0001   ; increment RAM
            cmp R2, 013F
            jc NE, LOOP1
            nop

REG_INT:                    ; Register Initialization
            mov R2, 0140    ; RT internal registers
            mov R0, 0150    ; Initialization information

LOOP2:      lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #0
            addu R0, 0001   ; increment ROM counter
            addu R2, 0002   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #2
            addu R0, 0001   ; increment ROM counter
            addu R2, 0004   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #6
            addu R0, 0001   ; increment ROM counter
            addu R2, 0001   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #7
            addu R0, 0001   ; increment ROM counter
            addu R2, 0001   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #8
            addu R0, 0001   ; increment ROM counter
            addu R2, 0001   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #9
            addu R0, 0001   ; increment ROM counter
            addu R2, 0001   ; increment RAM counter
            nop

            lri R1, R0      ; fetch data from ROM
            str R1, R2      ; store data in Register #A
```

```
                addu R0, 0001   ; increment ROM counter
                addu R2, 0004   ; increment RAM counter
                nop

                lri R1, R0      ; fetch data from ROM
                str R1, R2      ; store data in Register #E
                nop

DATA_LIST:                      ; Data and Message
                                  Status List Pointer

                mov R2, 0153    ; Top of RAM storage
                                  buffer
                mov R0, 0163    ; Top of ROM storage
                                  buffer


LOOP3:          lri R1, R0      ; fetch data from ROM
                str R1, R2      ; store data in RAM
                addu R0, 0001   ; increment ROM counter
                addu R2, 0001   ; increment RAM counter
                cmp R2, 01EE
                jc NE, LOOP3
                nop
```

Execution of these subroutines configures the RT for operation. The Control Register was configured for operation via the data field of 6180 (hex). RT operation does not begin until the least significant bit of the Control Register is set to a logic one. To begin operation write the value 6181 (hex) to the Control Register.

1.0 Bus Controller Architecture

The preceding section discussed the RT architecture and how to use the UTMC BCRTM device to effectively handle the Remote Terminal (RT) protocol. The following section describes the BCRTM's Bus Controller (BC) architecture. Please note that the UT1553B BCRT and UT1553 BCRTMP Bus Controller architectures are the same as the BCRTM, so this BC description will also be applicable to both of those devices.

The UTMC BC family of products provide all protocol, data handling, message error checking, and memory control functions. Discussed in this section are the following BC features and functions:

- Multiple Message Processing
- Linked-List Architecture
- Built-In Self-Test
- Message Scheduling
- Two-level Interrupt Structure
- Polling Compare
- Memory Management

1.1 Register File

To initialize the BCRTM to be a Bus Controller, the engineer must understand the internal registers. These registers offer many programmable functions and allow host access to extensive information. For a complete description of each register bit, review the data sheet section of this product handbook. Each register associated with the Bus Controller mode of operation is individually described below.

Register Name	Register Decode BCRT/BCRTMP A(3:0)	Register Decode BCRTM A(4:0)
Control	0000	00000
Status	0001	00001
Current Command Block	0010	00010
Polling Compare	0011	00011
BIT Word	0100	00100
Current Command	0101	00101
Interrupt Log List Pointer	0110	00110
High-Priority Interrupt Enable	0111	00111
High-Priority Interrupt Status/Reset	1000	01000
Standard Interrupt Enable	1001	01001
BIT Start	1011	01011
Programmed Reset	1100	01100
Activity Status/Operational Mode(1)	1110	N/A

Note:
1. BCRTMP only.

1.1.1 Control Register

This register is used to place the BCRTM device into the required mode of operation, whether that be a BC, RT, or MT. To operate the BCRTM as a Bus Controller, use the following bits.

Bit Number	Name	Read	Write	Programmed Reset
14	RT-Address 31 (1)	Yes	Yes	U (3)
13	Subaddress 31 (1)	Yes	Yes	U
12	BC Time-Out (2)	Yes	Yes	U
11	Enable External Override	Yes	Yes	U
10	BC or RT Select	No	Yes	U
9	Retry on Alternate Bus	Yes	Yes	U
7	Channel Select A/$\overline{B}$	Yes	Yes	U
6	Retry Count	Yes	Yes	U
5	Retry Count	Yes	Yes	U
4	Retry on BC Message Error	Yes	Yes	U
3	Retry on Time-Out	Yes	Yes	U
2	Retry on Message Error	Yes	Yes	U
1	Retry on Busy	Yes	Yes	U
0	Start Enable	No	Yes	0

Notes:
1. Applicable to BCRTM only.
2. Applicable to BCRTM and BCRTMP.
3. U = unaffected by programmed reset.

1.1.2 Status Register

The Status Register is a read-only register that contains the current status associated with the BC operation. The following bits are used to differentiate between the modes.

Bit Number	Name	Read	Write	Programmed Reset
9	BIT Active	Yes	No	0
8	Reset Active	Yes	No	0
7	BC or $\overline{RT}/\overline{M}$(1) Mode	Yes	No	A (1)
6	Channel A/$\overline{B}$	Yes	No	1
0	Command Block Execution	Yes	No	0

Note:
1. Applicable to BCRTM only.
2. A = affected by reset; logic state is determined by other conditions.

1.1.3 Current Command Block Register

This host-initialized Register must point to the head pointer of the first Command Block in a linked list and thereafter will automatically be updated on the execution of each command.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Current Command Block	Yes	Yes	U

1.1.4 Polling Compare Register

This register contains the host-defined 1553 status word bits that the BC is to interrupt if the register bits match the RT response.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Polling Compare Date	Yes	Yes	U

1.1.5 Built-in Self-test (BIT) Word Register

In the BC mode, the upper two bits can be used to determine the failure after completion of BIT. This register's fourteen least significant bits are user defined and the upper two bits show the result of BIT.

Bit Number	Name	Read	Write	Programmed Reset
15	Channel B Failure	Yes	Yes(1)	0
14	Channel A Failure	Yes	Yes(1)	0

Note:
1. Writing a logic one to this location will induce a BIT failure. This may be useful for testing a fail operation.

1.1.6 Current Command Register

This register contains the most current BC command transmitted on the 1553 bus and will automatically be updated on the execution of each command.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Current Command	Yes	No	U

1.1.7 Interrupt Log List Pointer Register

This host-initialized register contains the location to start the Interrupt Log List associated with each Command Block. After execution begins, this register is automatically updated with the address of the next entry.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Interrupt Log List Address	Yes	Yes	U

1.1.8 High-Priority Interrupt Enable Register

This register's bits, when enabled (set to a logic one), will generate high-priority interrupts caused by certain events. Enable the standard-priority level output pin ($\overline{\text{STDINTL}}$) by setting bit 0. If not enabled and a standard-priority interrupt occurs, only the Standard-Priority Interrupt pulse ($\overline{\text{STDINTP}}$) is asserted. Note: the Standard Interrupt Enable bit listed below has nothing to do with the High-Priority Interrupt even though the bit is contained in this register.

Bit Number	Name	Read	Write	Programmed Reset
8	Data Overrun Enable	Yes	Yes	U
7	Illogical Command Error Enable	Yes	Yes	U
6	Dynamic Bus Control Acceptance	Yes	Yes	U
5	Subsystem Fail Enable	Yes	Yes	U
4	End of BIT Enable	Yes	Yes	U
3	BIT Word Fail Enable	Yes	Yes	U
2	End of Command Block Enable	Yes	Yes	U
1	Message Error Enable	Yes	Yes	U
0	Standard Interrupt Enable	Yes	Yes	U

1.1.9 High-Priority Interrupt Status/Reset Register

When an enabled High-Priority Interrupt occurs, the corresponding bit in this register is set and the $\overline{\text{HPINT}}$ pin is asserted. Once the interrupt is serviced, the $\overline{\text{HPINT}}$ pin and the bit in this register may be reset by writing a logic one to the corresponding bit in this register. If a condition is met such that a standard interrupt is generated, a High-Priority Interrupt will not be asserted even if the standard interrupt is enabled in the High-Priority Register.

Bit Number	Name	Read	Write	Programmed Reset
8	Data Overrun	Yes	Yes	0
7	Illogical Command	Yes	Yes	0
6	Dynamic Bus Control	Yes	Yes	0
5	Subsystem Fail	Yes	Yes	0
4	End of BIT	Yes	Yes	0
3	BIT Word Fail	Yes	Yes	0
2	End of Command Block	Yes	Yes	0
1	Message Error	Yes	Yes	0
0	Standard Interrupt	Yes	Yes	0

1.1.10 Standard-Priority Interrupt Enable Register

This register's bits, when enabled (set to a logic one), will generate standard-priority interrupts caused by certain events. For each interrupt, the standard interrupt pulse will be asserted. If the standard interrupt is enabled in the High-Priority Interrupt enable register, then both the standard-priority level output pin ($\overline{\text{STDINTL}}$) and the Standard-Priority Interrupt pulse ($\overline{\text{STDINTP}}$) always will be asserted.

Bit Number	Name	Read	Write	Programmed Reset
3	Polling Comparison Match	Yes	Yes	U
2	Retry Fail	Yes	Yes	U
1	Message Error	Yes	Yes	U
0	Command Block Interrupt/Continue	Yes	Yes	U

1.1.11 BIT Start Register

This register is used to invoke the built-in self-test. To start the BIT, the BCRT/M/MP must be inactive and idle. To take the device out of the active BC mode, a write to the Programmed Reset Register must precede a write to this register. Writing any data pattern to this register will place the device into BIT. The routine takes 100 μs to complete and the results are logged into the BIT Word Register as previously described.

Bit Number	Name	Read	Write	Programmed Reset
15-0	BIT Start	No	Yes	N/A

1.1.12 Programmed Reset Register

This register is used to invoke the Programmed Reset. Writing any data pattern to this register will take the device out of the BC mode and perform a device reset. The self-test routine takes 1 μs to complete and no other activity should occur while the BCRTM self-test is in progress. During this programmed reset, none of the registers are affected except for the Status Register which will be updated with the latest status information.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Programmed Reset	No	Yes	N/A

2.0 THE BCRTM'S LINKED-LIST ARCHITECTURE

As previously defined, the BC initiates all 1553 communications. To meet the MIL-STD-1553B Bus Controller requirements, the BCRTM uses a Command Block architecture that takes advantage of both internal registers and external memory. Each command word transmitted over the bus must be associated with a Command Block. The Command Block, which is located in external contiguous memory, contains eight distinct parameters associated with each message. These parameters are a head pointer, the control word, two command word locations, a Data List Pointer, two status word locations, and a Tail Pointer.

The host must initialize each of the locations associated with each Command Block (the exception is for the two status locations which will be updated as command words are transmitted and corresponding status words are received). Figure 1 shows the Command Block followed by a brief description of each location associated with the Command Block.

HEAD POINTER
CONTROL WORD
COMMAND WORD 1
COMMAND WORD 2 (RT-RT ONLY)
DATA LIST POINTER
STATUS WORD 1
STATUS WORD 2 (RT-RT ONLY)
TAIL POINTER

Figure 1. Command Block

Head Pointer - The first memory location of each Command Block contains the Head Pointer. The Head Pointer may be used by the host to traverse up the list. This location is merely a starting point for the Command Block and the BCRTM does not use it.

Control Word - Immediately following the Head Pointer is the control word, which contains message options for the BC. For the BC mode of operation, the control word has 16 bits for selectable options (see figure 2). Each of these bits is defined below.

Bit 15 — This bit is set by the BCRTM when an invalid RT response is detected.

Bit 14 — This bit, when set, instructs the BC to skip execution of the current Command Block and jump to the next. If a time delay is programmed into the device (bits 7-0 below), the BCRTM will delay that set time before jumping to the next Command Block.

Bit 13 — This bit, when set, instructs the BC to assert a standard interrupt and continue operation. This is one method to synchronize the host with the BCRTM.

Bit 12 — This bit, when set, enables the polling feature of the BCRTM. For information on the polling operation, see the data sheet or section 6.0 of this text.

Bit 11 — This bit, when set, enables the auto retry function for this message. The Control Register determines the bus and the number of retries that will occur.

Bit 10 — This bit, when set, enables the End Of List function in the BC mode of operation. This bit allows the BC to halt execution and assert a high-priority interrupt after completing the current message. The interrupt must be enabled in the High-Priority Interrupt Enable Register.

Bit 9 — This bit, when set, instructs the BC that the current Command Block is an RT-to-RT transfer.

Bit 8 — This bit, when set, instructs the BC to store the message beginning at the data pointer location for RT-RT messages.

Bit 7-0 — These bits determine a specified time delay between message starts. This operation causes the BC to delay that specified time between Command Blocks. See the following section for specific notes associated with this feature.

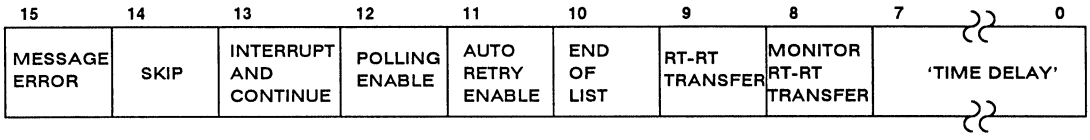


Figure 2. Control Word

Command Word 1 & 2 - The next two locations are for command words; the second command word only needs to be initialized for RT-to-RT transfers.

Data List Pointer - The fifth location in the Command Block is the Data List Pointer. It points to the first memory location to store or fetch the data words associated with the message for this Command Block. While the Data List Pointer actually points to the first memory location, it should be noted that the data associated with each individual message must be stored contiguously. This data structure allows the BCRTM to store or fetch the exact specified number of data words, thus saving memory space and providing efficient space allocation. One common application for the Data List Pointer is when the BC needs to send the same data words to several RTs. Here, each Command Block associated with those messages would contain the same Data List Pointer value, thus fetching and transmitting the same data to each of the RTs.

Status Word 1 & 2 - The next two locations in the Command Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. The second status word is recorded only in RT-to-RT transfers.

Tail Pointer - The last location in the command block is the Tail Pointer that points to the Head Pointer of the next Command Block.

3.0 Command Block Chaining

The host determines the first Command Block by setting the initial start address in the current Command Block Register. The Tail Pointer of the first Command Block will point to the Head Pointer of the second Command Block, and so on. Several Command Blocks may be linked together to form a chain of commands. Several Command Blocks may be linked together in a linked-list architecture to build minor frames.

4.0 Message Delay Programming

As defined in bits 7-0 of the control word, the Time Delay feature allows for sophisticated message scheduling. When using the Time Delay feature in the BC mode of operation, it is important to note that the BCRTM will provide at least the 4 μs intermessage gap as defined in MIL-STD-1553B. The timer resolution of 16 μs allows the BC to meet system requirements for message delay programming. Also, the time delay may be initialized differently for each Command Block. This initialization will allow different delays between messages or allow the designer to complete minor frames in specified times. If all ones (11111111) are written to these bits, the maximum gap time will be (255 x 16 μs) 4.08 ms. This time corresponds to a 4.08 ms gap time from the start of one command to the start of the next command.

As an example, let's say that requirements call for a 124 μs message gap on the first message and a 200 μs message gap on the second message. Based on those specifications, 00001000 (8 x 16 μs = 128 μs) must be written to the time delay field of the control word in the first Command Block and 00001101 (13 x 16 μs = 208 μs) must be written to the time delay field of the control word in the second Command Block.

5.0 Interrupt Levels And Handling

The BCRTM uses the same type of architecture on interrupts as on the linked-list Command Block structure. The interrupt consists of the internal registers previously discussed, control bits in the BC data structure, and an Interrupt Log List. This List allows flexible memory definition and allows the host to view the interrupts as they occur. The BCRTM has two levels of interrupts (High- or Standard-Priority) and three output signals ($\overline{\text{HPINT}}$, $\overline{\text{STDINTL}}$, and $\overline{\text{STDINTP}}$) to indicate the occurrence of an interrupt. Each of the output pins is defined below.

$\overline{\text{STDINTL}}$ - Standard Interrupt Level - This signal is asserted when any of the events enabled in the Standard Interrupt Enable Register occurs, provided it is enabled in Register 8. Clear the level by writing a logic one to bit 0 of the High-Priority Interrupt Status/Reset Register.

$\overline{\text{STDINTP}}$ - Standard Interrupt Pulse - This signal goes low for 320 ns for any enabled bit in the Standard Interrupt Enable Register or in the BC control word.

$\overline{\text{HPINT}}$ - High-Priority Interrupt - This signal is asserted for any of the events enabled in the High-Priority Interrupt/Enable Register. Clear the level by writing a logic one to the corresponding bit in the High-Priority Interrupt Status/Reset Register.

Based on the interrupt scheme, the BC generates the Interrupt Log List to allow the host to review all interrupts in chronological order. Only one interrupt log will occur per message, except on retry failures. When an

interrupt condition occurs, the BC performs two memory writes and one memory read to the Interrupt Log List Pointer Register. Definitions of all three words follow:

Interrupt Status Word - BCRTM written, this word will show the type of standard interrupt that occurred, if the interrupt is enabled. Active high bits indicate which of the interrupts were generated. Each bit in the Interrupt Status Word that is associated with the BC mode of operation is defined below.

Bit 15 This bit is always set during the DMA write of the Interrupt status word. Here, the host can reset this bit after reading the word to help determine which of the entries have been acknowledged.

Bit 14 No Response Time-Out - Under message error conditions, this bit is set to indicate that a message error time-out has occurred.

Bit 3 Polling Comparison Match - This bit is set when a polling comparison interrupt occurred.

Bit 2 Retry Fail - This bit is set when all the programmed retries have failed.

Bit 1 Message Error - This bit is set when a message error associated with the device's protocol logic has occurred.

Bit 0 Interrupt and Continue - This bit is set when the Command Block was addressed.

High-Priority Interrupt Status Register - BCRTM written, this register will show the type of high-priority interrupt that occurred, if the interrupt is enabled. Active high bits indicate which of the interrupts were generated. Each bit in the High-Priority Interrupt Status Register that is associated with the BC mode of operation is defined below.

Bit 8 Data Overrun Enable - This bit, when set, indicates the BCRTM did not receive a $\overline{\text{DMAG}}$ within the allotted time to successfully perform a write to memory. If this condition occurs, the BCRTM stops execution and waits for the $\overline{\text{DMAG}}$ signal.

Bit 7 Illogical Command Error - This bit, when set, indicates the occurrence of an Illogical Command, which may include incorrectly formatted RT-RT Command Blocks.

Bit 2 End of Command Block List - This bit is set when all the Command Blocks have been executed.

Bit 1 Message Error - This bit is set at the occurrence of a message error.

If a High-Priority Interrupt occurs due to an illogical command, end of list, or a message error, the BCRTM will halt operation and stop execution until the user services the interrupt. Here the user must read the High-Priority Interrupt Status/Reset Register to pinpoint what caused the interrupt. Once the interrupt has been cleared, the device will automatically restart if the interrupt was due to a message error condition. However, once the interrupt has been cleared and the interrupt was due to an illogical command or End Of List, the user must restart the BCRTM by writing a logic one to bit 0 of the Control Register.

6.0 Polling Function

In the BC mode, the system may require the Bus Controller to periodically interrogate each RT for subsystem status. If required, the BCRTM can use the Polling feature to accomplish this task. Here the BC not only gets each RT to respond with its status word but may also compare each bit with a known response to determine if additional tests must be performed on the particular RT.

As previously discussed, the Polling Compare Register contains the host-defined data which the BC is to interrupt. For example, if the Service Request bit is set in the RT response, an interrupt may be generated to allow the host to decide what action to take. To use the Polling Compare Register, the host must initialize the register to contain logic ones in each status bit the host wants to try and detect during polling. Once each of the RT status words are received, it is compared to the register contents. Interrupts, if enabled, will occur if the corresponding bits in the register and status bits are both logic high.

Use of the polling function varies between applications. One common use is to allow the BC to alert the host processor, in real time, of certain types of RT responses. Another application for polling may be the general use of mode codes such as Transmit Last Status Word. This mode code allows the BC to "poll" each individual RT as to its last status word to see if additional servicing is required.

7.0 Memory Architecture

After reviewing the BCRTM's internal registers, a look at the external memory requirements and how the host sets up memory in order to make the BCRTM a bus controller may be advantageous. The intent of this memory section is to show that memory configurations are almost unlimited. Below are just two configurations used to allocate memory. Each configuration is discussed separately.

The first configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 3 shows that the first block of memory is allocated for the Command Blocks. Notice that Register 2 initially points to the Head Pointer of the first Command Block. After completing execution of that first Command Block, Register 2 will automatically be updated to show the address associated with the next Command Block. Also the Head Pointer of the second Command Block may be located directly after the preceding Command Block's Tail Pointer.

Following the Command Block locations is the memory required for all the data words. In BC applications, the

number of data words for each Command Block is known. In figure 3 for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List. The third block of memory is allocated for this Log List. Notice that Register 6 points to the top of the initial Log List. After execution of that first Command Block, Register 6 will automatically be updated. Notice the Tail Pointer of the first may be followed directly with the start of the second Log List.

A second memory configuration may wish to place all the Command Blocks, data, and interrupts associated with each message transfer together as figure 4 shows.

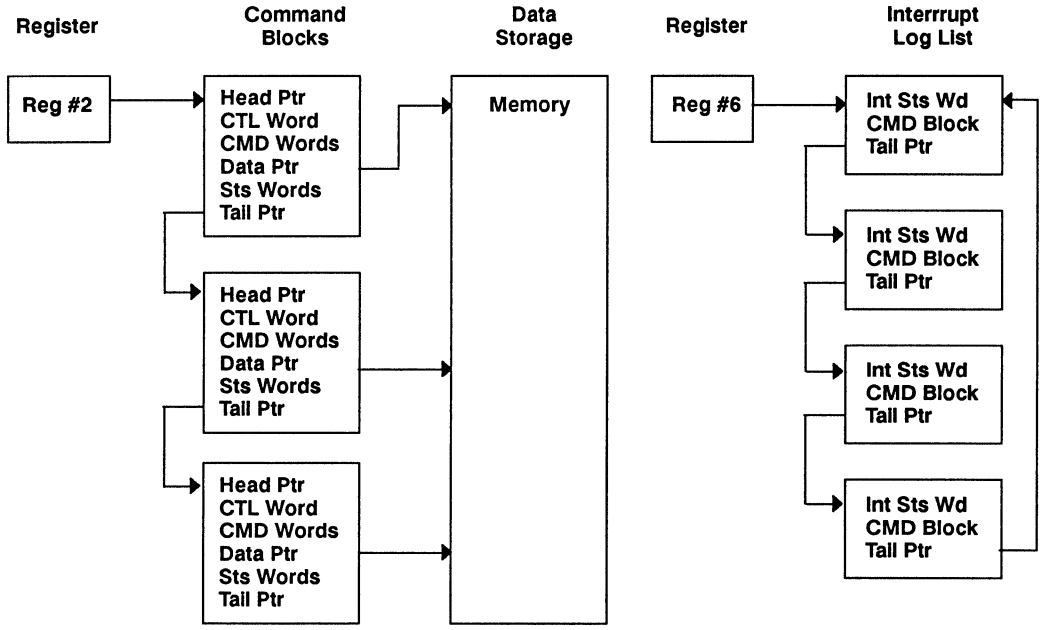


Figure 3. Memory Architecture For BC Mode

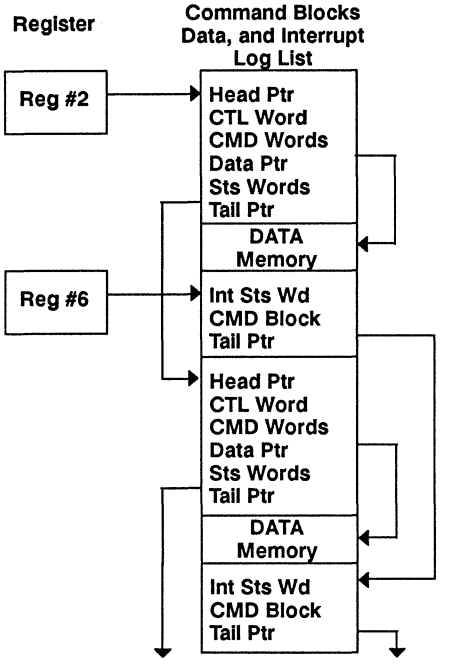
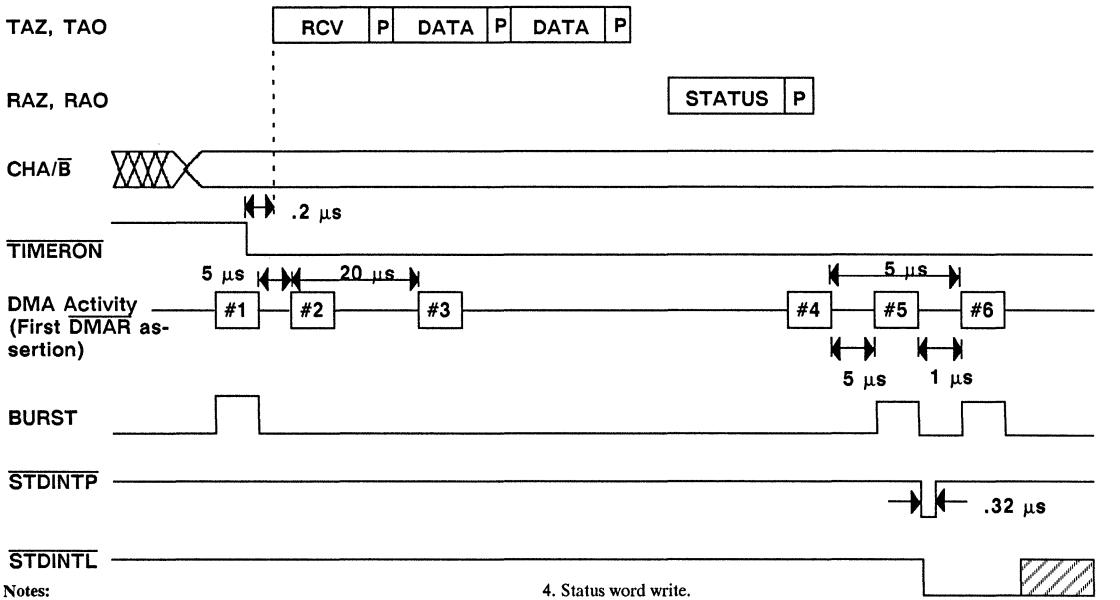


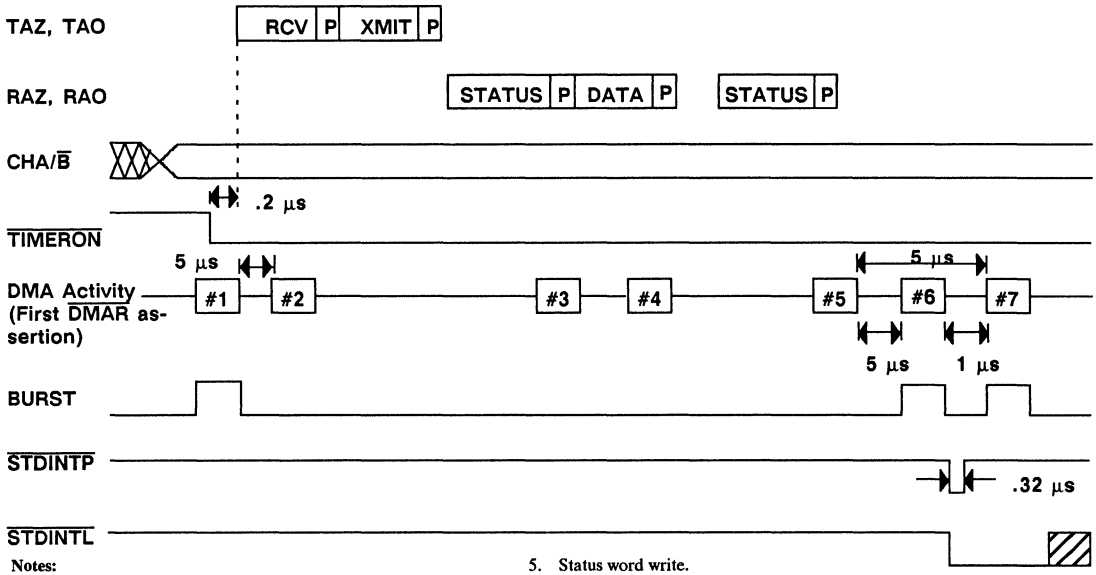
Figure 4. Memory Architecture For BC Mode

After reviewing the past several pages, it should be obvious that the designer has complete control over the BC memory mapping architecture. Each system may require slightly different memory requirements and the BCRTM's flexibility allows the user to "fill in the blanks." This flexibility allows designers to generate the correct memory map that meets their specific applications. This mapping allows the definition of all Command Blocks, identifies where the data for each Command Block is stored, and clearly shows how much memory is required.



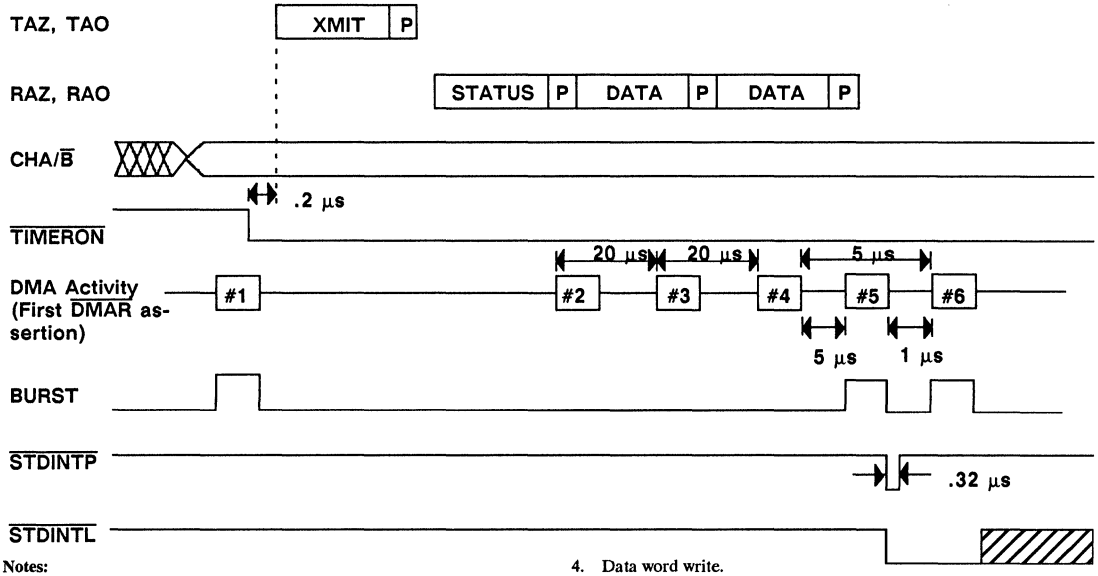
Notes:
1. Command Block read, control word read, command word write, data pointer read.
2. Data word read.
3. Data word read.
4. Status word write.
5. Optional Interrupt Log.
6. Command Block update, control word write, read tail pointer, read next Command Block.

Figure 5. Typical Receive Command (BC Mode)



Notes:
1. Command Block read, Control word read, command word write, Data pointer read.
2. Command word #2 read.
3. Status word write.
4. Data word write (Optional if monitoring RT-RT).
5. Status word write.
6. Optional Interrupt Log.
7. Command Block update, Control word write, read tail pointer, read next Command block.

Figure 6. Typical RT-RT Command (BC Mode)



Notes:
1. Command Block read, Control word read, Command word write, Data pointer read.
2. Status word write.
3. Data word write.
4. Data word write.
5. Optional Interrupt Log.
6. Command Block update, Control word write, Read tail pointer, read next Command block.

Figure 7. Typical Transmit Command (BC Mode)

8.0 BC Design Example

This final BC section will offer an example to clearly define, initialize, and operate the BCRTM as a Bus Controller. The user will learn how to set up the registers, set up memory, and determine when DMA transactions will occur.

The following baseline specifications will apply to our sample BC design.

1. Operate the BCRTM as a Bus Controller.
2. Have the BC transmit 3 messages to 2 different RTs with an intermessage gap of 150 μs (RT addresses = 2 and 23).
3. Set Bus A as the primary bus.
4. Retry messages on time-outs and/or RT message errors only.
5. Retry up to 4 times on the alternate bus (Bus B).
6. Generate an interrupt if all retries fail.
7. Start the Command Blocks at location 0000H.
8. Interrupt and stop execution at the end of the Command Block chain.
9. Start the data words at location 1000H.
10. Start the Interrupt Log List at location 2000H.

8.1 Register Files

To effectively meet all the above requirements, a review of the registers is useful. The following discussion will review each register that is affected and show why the register was initialized to the stated value.

Control Register - Register 0

The Control Register will help the designer meet specifications 1, 3, 4, and 5 listed above. By writing 06ECH to this register, the BCRTM will function as a Bus Controller, retry on the alternate channel (Bus B), enable Channel A as the primary bus, retry up to four consecutive times, and retry for time-outs and/or RT message errors. To verify this value (06ECH), take a moment and review each bit in the Control Register.

Current Command Block Register - Register 2

This register may be initiated to meet specification 7. To have the Command Block Register start at location 0000H, simply have the host write that value (0000H) into Register 2 and make sure that the memory locations 0000H - 0008H contain the first Command Block. Again, depending on your memory structure and availability, the tail pointer of that first Command Block may point to 0009H (if following the setup in figure 3) or to just about any other location (as shown in figure 4).

Interrupt Log List Pointer Register - Register 6

This register may be used to meet the 10 specification listed above. To have the Interrupt Log List Pointer start at location 2000H, simply have the host write that value (2000H) into Register 6 and make sure that memory locations 2000H - 2002H are set aside for the three words, previously discussed, defined by the Log List.

High-Priority Interrupt Enable Register - Register 7

To meet specification 8 above and to make sure that the BC interrupts the host and stops executing the Command Blocks once it has completed the chain, the host must initialize this register to 0004H. This value (0004H) will enable the End of Command Block List High-Priority Interrupt. The BCRTM will automatically stop once the last Command Block has been executed and the interrupt will tell the host of the occurrence. The interrupt will be a pulse only unless bit 0 in the High-Priority Interrupt Register is set. Note that the control word in the last Command Block must have the End Of List bit set.

Standard Interrupt Enable Register - Register 9

To meet specification 6 above and have the BC generate an interrupt if all programmed retries fail, the host must initialize this register to 0004H. This value (0004H) will not only enable the BCRTM to generate a standard-priority interrupt on the occurrence but will allow the BC to log the interrupt into the Interrupt Log List for future evaluations.

The final two specifications can be handled while setting up the BC's Command Blocks. From previous discussion, each message on the 1553 bus must have a corresponding Command Block. With one of the specifications calling for the transmission of three messages, three separate Command Blocks must be initialized (with the first Command Block starting at memory location 0000H). Below are the contents of the three Command Blocks that must be written into memory.

MEMORY LOCATION	CONTENTS (hex)	COMMENTS CMD = Command Block
0000	XXXX	Head Pointer for CMD #1.
0001	080A	Control Word for CMD #1; Auto Retry enabled and 150 μs time delay.
0002	1041	Command Word #1 for CMD #1; notice this is a receive message of one word to RT #2, subaddress #2.
0003	XXXX	Command Word #2 for CMD #1; since this is not an RT-RT transfer, the contents are not read.
0004	1000	Data List Pointer for CMD #1; to meet #9 specification above, all data is to start at location 1000H.
0005	XXXX	Status Word #1 for CMD #1; will be updated after the RT responds.
0006	XXXX	Status Word #2 for CMD #1; won't be used since this is not an RT-RT transfer.
0007	0008	Tail Pointer for CMD #1; should point to the start of the next Command Block.
0008	XXXX	Head Pointer for CMD #2.
0009	080A	Control Word for CMD #2; Auto Retry enabled and 150 μs time delay.
000A	B982	Command Word #1 for CMD #2; notice this is a receive message of two words to RT #23, subaddress #12.
000B	XXXX	Command Word #2 for CMD #2; since this is not an RT-RT transfer, the contents are not read.
000C	1001	Data List Pointer for CMD #2; with the previous Command Block receiving one data word, it will be safe to allocate only one memory location for that Command Block.
000D	XXXX	Status Word #1 for CMD #2; will be updated after the RT responds.
000E	XXXX	Status Word #2 for CMD #2; won't be used since this is not an RT-RT transfer.
000F	0010	Tail Pointer for CMD #2; should point to the start of the next Command Block.
0010	XXXX	Head Pointer for CMD #3.
0011	0C0A	Control Word for CMD #3; Auto Retry and End Of List enabled and 150 μs time delay.
0012	13A3	Command Word #1 for CMD #3; notice this is a receive message of three words to RT #2, subaddress #29.
0013	XXXX	Command Word #2 for CMD #3; since this is not an RT-RT transfer, the contents are not read.
0014	1003	Data List Pointer for CMD #3; with the previous Command Block receiving two data words, it will be safe to allocate two memory locations for that Command Block.
0015	XXXX	Status Word #1 for CMD #3; will be updated after the RT responds.
0016	XXXX	Status Word #2 for CMD #3; won't be used since this is not an RT-RT transfer.
0017	0000	Tail Pointer for CMD #3; should point to the start of the next Command Block.

Now that the BCRTM is set up to meet the specifications given, the device must be started and processing will begin. To start the device as a BC, a rewrite to the Control Register (Register 0) must occur to toggle the Start Enable (bit 0). Notice that in the initialization section 06EC was written to the Control Register. This value initialized the register but did not start the device. Now, if the value of 06ED is written to the Control Register, it will not only maintain the same setup configuration, but will also start the device.

While the above example only deals with BC to RT messages, it is easily changed to handle different sequences. To transmit data from the RT to the BC,

simply change the T/R bit in each command word in the Command Blocks. To perform an RT-to-RT transfer, initialize the Control Word (bit 9) and both command words associated with the Command Block.

8.2 DMA Activity

In the BC mode, the BCRTM must access external memory in order to function properly. To gain access to the local bus, the BCRTM must arbitrate for that bus. Once $\overline{\text{DMAG}}$ is asserted, the BC may proceed with either a single memory access or multiple accesses (BURST). The following section describes what types of memory accesses are performed and when these occur. Please refer to figures 5-7 of this text or the applicable data sheet for a graphical representation.

After the external memory and internal BC registers are initialized, the host starts the BC operation by writing a "1" to Register 0, bit 0. Immediately after doing so, the BCRTM performs a burst of memory accesses. The device performs three accesses to read in the control word, the first command word, and the Data List Pointer for the first Command Block. Upon completion of this or any burst accesses, the BC surrenders the local bus by negating the $\overline{\text{DMACK}}$ output.

For BC to RT Command Blocks, as shown in our previous example, the BC transmits the command word to the RT. Now, as in the example, a data word is involved in the transaction and the BCRTM must access memory and read in the data word. The DMA for this data word occurs while the status word is transmitted. If more than one data word is involved in the message, the DMAs (single) and data word transmissions will continue until the message is complete.

For RT to BC Command Blocks, the BC transmits the command word to the RT. As soon as the BC receives the RT status word it immediately writes that value into the sixth location of the Command Block. Once again, if data words are involved in the message, the data word writes to memory will continue until all the data words are received.

While the Command Block DMA is the first burst mode the BCRTM uses, there are several other burst conditions. The second burst occurs if an interrupt condition is met during a message transfer. If a standard interrupt condition is met, the BC writes the Interrupt Status Word, writes the Command Block Pointer, reads the Tail Pointer, pulses the $\overline{\text{STDINTP}}$ signal, and asserts the $\overline{\text{STDINTL}}$ (if enabled).

The third burst mode is used when a retry condition occurs (if retries are enabled). The BC will read the control word, read the first command word, and read the Data List Pointer. Notice this DMA activity is the exact same as the Command Block DMA, since the BC needs to retransmit the same message.

The fourth burst mode occurs when the BC detects a message error while processing the current Command Block. The BC writes the control word, reads the Command Block Tail Pointer of the last command, holds the bus to determine the next Command Block, reads the new control word, reads the first command word associated with the new Command Block, and reads the Data List Pointer associated with the new Command Block. However, if the End Of List (EOL) bit is enabled, the BC only writes the control word.

The last burst mode is used during normal execution when no message errors occur during the current Command Block. However, if the EOL bit is enabled, the BC simply stops execution and waits for further instruction. If not enabled, the BC proceeds to the next Command Block and a burst occurs. Here the BC reads the Command Block Tail Pointer, holds the bus to determine the next Command Block, reads the new control word, reads the first command word associated with the new Command Block, and reads the new data list pointer.

1.0 Monitor Terminal Architecture

The preceding section has discussed the BC architecture and how to use the UTMC BCRTM device to effectively handle the Bus Controller protocol. The following section describes the BCRTM's monitor terminal (MT) architecture and the three additional registers used in the Monitor mode of operation. Note that the UT1553B BCRT and UT1553 BCRTMP have no bus monitor capabilities, so this MT description will not apply to those devices. For clarity all registers and bits associated with the MT mode are discussed below.

The UTMC BCRTM provides for data handling, message error checking, and memory control functions. Discussed in this section are the following features and functions of the Monitor Terminal:

- Command History List
- Interrupt History List
- Monitor Selected Terminal Addresses
- Selectable/Sequential Data Storage
- Variable Memory Allocation
- Programmable Interrupt Structure

2

1.1.1 Initializing The Registers

To initialize the BCRTM to be a Monitor, the user must have a complete understanding of the internal registers. These registers offer many programmable functions and allow host access to extensive information. For a complete description of each register bit, review the BCRTM data sheet. Each register associated with the Monitor mode of operation is described below.

Register Name	Register Decode BCRTM A(4:0)
Control	00000
Status	00001
Current Command Block	00010
Current Command	00101
Interrupt Log List Pointer	00110
High-Priority Interrupt Enable	00111
High-Priority Interrupt Status/Reset	01000
Standard Interrupt Enable	01001
Remote Terminal Address	01010
BIT Start	01011
Programmed Reset	01100
RT Timer Reset	01101
Bus Monitor Control	01110
Monitor Selected RT Addresses (0-15)	10000
Monitor Selected RT Addresses (16-31)	10001

1.1.2 Control Register

This register is used to place the BCRTM device into the required mode of operation, whether that be a BC, RT, or MT. To place the BCRTM in the Monitor mode use the following bits.

Bit Number	Name	Read	Write	Programmed Reset
12	BC Time Out	Yes	Yes	U (1)
11	Enable External Override	Yes	Yes	U
10	BC or RT Select	No	Yes	U
8	Channel B Enable	Yes	Yes	U
7	Channel A Enable	Yes	Yes	U
0	Start Enable	No	Yes	0

Note:
1. U = unaffected by programmed reset

1.1.3 Status Register

The Status Register is a Read-Only register that contains the current status associated with the MT operation. The following bits are used to differentiate between the modes.

Bit Number	Name	Read	Write	Programmed Reset
14	Monitor Active	Yes	No	0
9	BIT Active	Yes	No	0
8	Reset Active	Yes	No	0
7	BC or $\overline{RT}/\overline{M}$ Mode	Yes	No	A (1)
6	Channel A/$\overline{B}$	Yes	No	1
5	Subsystem Fail Indicator	Yes	No	U

Note:
1. A = affected by reset, logic state is determined by other conditions.

1.1.4 Current Command Block Register

Initially this register contains the address of the control/status word of the current Command Block and thereafter will automatically be updated on the execution of each command.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Current Command Block	Yes	Yes	U

1.1.5 Current Command Register

This register contains the most current command transmitted on the 1553 bus and will automatically be updated on the execution of each command.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Current Command	Yes	No	U

1.1.6 Interrupt Log List Pointer Register

This register contains the location to start the Interrupt Log List associated with each Command Block. After execution begins, this register is automatically updated with the address of the next entry.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Interrupt Log List Address	Yes	Yes	U

1.1.7 High-Priority Interrupt Enable Register

This register's bits, when enabled, will generate High-Priority Interrupts caused by certain events. Enable the standard-priority level output pin ($\overline{STDINTL}$) by setting bit 0. If not enabled and a Standard-Priority Interrupt occurs, only the Standard-Priority Interrupt pulse ($\overline{STDINTP}$) is outputted. Note: the Standard Interrupt Enable bit listed below has nothing to do with the High-Priority Interrupt even though the bit is contained in this register.

Bit Number	Name	Read	Write	Programmed Reset
8	Data Overrun Enable	Yes	Yes	U
5	Subsystem Fail Enable	Yes	Yes	U
4	End of BIT Enable	Yes	Yes	U
3	BIT Word Fail Enable	Yes	Yes	U
1	Message Error Enable	Yes	Yes	U
0	Standard Interrupt Enable	Yes	Yes	U

1.1.8 High-Priority Interrupt Status/Reset Register

When a High-Priority Interrupt occurs, the corresponding bit in this register is set and the $\overline{\text{HPINT}}$ pin is asserted. Once the interrupt is serviced, the $\overline{\text{HPINT}}$ pin and the bit in this register may be reset by writing a logic one to that corresponding bit. If a condition is met such that a standard interrupt is generated, a High-Priority Interrupt will not be asserted even if the standard interrupt is enabled in the High-Priority Register.

Bit Number	Name	Read	Write	Programmed Reset
8	Data Overrun	Yes	Yes	0
5	Subsystem Fail	Yes	Yes	0
4	End of BIT	Yes	Yes	0
3	BIT Word Fail	Yes	Yes	0
1	Message Error	Yes	Yes	0
0	Standard Interrupt	Yes	Yes	0

1.1.9 Standard-Priority Interrupt Enable Register

This register's bits, when enabled, will generate Standard-Priority Interrupts caused by certain events. If enabled, both the standard-priority level output pin ($\overline{\text{STDINTL}}$) and the Standard-Priority Interrupt pulse ($\overline{\text{STDINTP}}$) will be outputted.

Bit Number	Name	Read	Write	Programmed Reset
1	Message Error	Yes	Yes	U
0	Command Block Interrupt/Continue	Yes	Yes	U

1.1.10 Remote Terminal Address Register

This register is used to control several bits in the RT's status word response and to monitor the state of operation in the MT mode.

Bit Number	Name	Read	Write	Programmed Reset
8	Mode Select	Yes	No	U
7	LOCK Pin Indicator	Yes	No	U

1.1.11 Bit Start Register

This register is used to invoke the built-in self-test. Writing any data pattern, except 0000H, will place the device into BIT. The routine takes 100 μs to complete and the results are logged into the BIT Word Register previously described.

Bit Number	Name	Read	Write	Programmed Reset
15-0	BIT Start	No	Yes	N/A

1.1.12 Programmed Reset Register

This register is used to invoke the Programmed Reset. Writing any data pattern, except 0000H, will perform a device reset. The self-test routine takes 1 μs to complete and no other activity should occur while the BCRTM self-test is in progress.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Programmed Reset	No	Yes	N/A

1.1.13 Bus Monitor Control Register

This register is used to place the BCRTM device into the Monitor mode of operation. Before writing a logic zero to bit 10 of Register 0, the host should write a logic one to bit 15 of this register. This places the BCRTM into the Monitor mode of operation. If the LOCK pin is externally tied high, the user may write once to the Control Register before the terminal is locked into one particular mode. Once the LOCK is set externally and software has written to Register 0, the BCRTM cannot change between modes without a programmed reset.

Bit Number	Name	Read	Write	Programmed Reset
15	Bus Monitor Select	Yes	Yes	U
14	Monitor All Terminals	Yes	Yes	U
13	Monitor Selected Terminals	Yes	Yes	U

1.1.14 Monitor Selected Remote Terminal Addresses 15-0

This register is used to select which specific Remote Terminals (RT 0 - RT 15) to monitor. For example, if the MT is to monitor remote terminals 0 - 5, the first six bits should contain a logic one. The host should write to this register after initializing the Control Register and the Bus Monitor Control Register to place the BCRTM in the Monitor mode of operation. Note: The BCRTM must already be configured as a Monitor (i.e., a write to the Bus Monitor Control Register) before initializing this register.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Selected Remote Terminals	Yes	Yes	0

1.1.15 Monitor Selected Remote Terminal Addresses 31-16

This register is used to select which specific Remote Terminals (RT 16 - RT 31) to monitor. For example, if the MT is to monitor remote terminal 21, the sixth bit should contain a logic one (i.e., 0020H should be written into this register). The host should write to this register after initializing the Control Register and the Bus Monitor Control Register to place the BCRTM in the Monitor mode of operation. Note: The BCRTM must already be enabled (i.e. a write to the Bus Monitor Control Register) before initializing this register.

Bit Number	Name	Read	Write	Programmed Reset
15-0	Selected Remote Terminals	Yes	Yes	0

2.0 The BCRTM's Linked-List Architecture

As previously defined, the MT should have the capability of monitoring any or all 1553 communications. To meet the MIL-STD-1553B monitor terminal requirements, the BCRTM uses a Command Block architecture that uses both internal registers and external memory. Two of the internal registers allow the designer the flexibility to monitor selected remote terminals. For example, if the system requires the monitoring of RT register's 1, 2, 6, 8, 10, 14, 17, 20, 25, and 29 only, the BCRTM may be initialized accordingly. Simply write 4546H to Register 16 and 2212H to Register 17 and the above selected remote terminal will be monitored.

Just as in the BC mode, each message received over the bus must be associated with a Command Block. The Command Block, much like the BC architecture, is located in external memory. However, unlike the BC architecture, this Command Block contains seven distinct functions associated with each message. These functions are a Monitor control/status word, two command word locations, a Data List Pointer, two status word locations, and a Tail Pointer.

The host must initialize each of the locations associated with each Command Block (the exception is for the two status locations which will be updated as command words are transmitted). The Command Block in shown in figure 1, followed by a brief description of each location associated with the Command Block.

MONITOR CONTROL/STATUS
1553 COMMAND WORD 1
1553 COMMAND WORD 2
DATA LIST POINTER
1553 STATUS WORD 1
1553 STATUS WORD 2
TAIL POINTER

Figure 1. BCRTM Bus Monitor Command Block

Control/Status Word - The first location in the Monitor Command Block is the control/status word. This location contains message options for each of the Monitor messages. The control/status word has sixteen bits for selectable options. Each of these bits is defined below.

Bit 15	This bit is set when the BCRTM has accessed this Command Block.
Bit 14	This bit is set when a message error occurred while receiving this message.
Bit 13	The BCRTM issues a Standard-Priority Interrupt and sets this bit when this Command Block has been accessed, if enabled in the Standard Interrupt Enable Register.
Bit 12	This bit defines the bus upon which the message was received. If set, the message was received on Bus A and if not set, the message was received on Bus B.
Bit 11-8	Not used.
Bit 7-0	These bits record a specified time tag between message starts. The time-tag feature has a 64 μs resolution and may be different for each of the Command Blocks.

Command Word 1 & 2 - The next two locations are for command words; the second command word will only contain information on RT-to-RT transfers.

Data List Pointer - The fourth location in the Monitor Command Block is the Data List Pointer. It points to the first memory location to store the data words associated with the message for this Command Block. While the Data List Pointer actually points to the first memory location, note that the data associated with each individual message must be stored contiguously.

Status Word 1 & 2 - The next two locations in the Command Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. The second status word is recorded only in RT to RT transfers.

Tail Pointer - The last location in the command block is the Tail Pointer that points to the next Monitor Command Block.

3.0 Command Block Chaining

The host determines where to start the first Command Block by setting the initial start address in the current Command Block Register. The Tail Pointer of the first Command Block will point to the control/status word of the second Command Block, and so on. This architecture allows the Command Blocks to be linked together to store multiple 1553 messages. This list may be as short or

as long as the system requires. Figure 2 shows several Command Blocks linked together to form a chain.

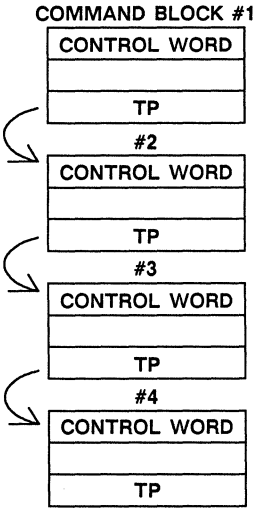


Figure 2. Monitor Command Block Tail Pointers

4.0 Interrupt Levels And Handling

The BCRTM uses the same type of architecture on interrupts as on the linked-list Command Block structure. The interrupt consists of the internal registers previously discussed, control bits in the MT data structure, and an Interrupt Log List. This List allows flexible memory definition and allows the host to view the interrupts as they occur. The BCRTM has two levels of interrupts and three output signals, as previously discussed, to indicate the occurrence of an interrupt. Each of the output pins is defined below.

$\overline{\text{STDINTL}}$ - Standard Interrupt Level - This signal is asserted when any of the events enabled in the Standard Interrupt Enable Register occurs. Clear the level by writing a logic one to bit 0 of the High-Priority Interrupt Status/Reset Register.

$\overline{\text{STDINTP}}$ - Standard Interrupt Pulse - This signal is asserted for 320 ns for any enabled bit in the Standard Interrupt Enable Register or in the MT control word.

$\overline{\text{HPINT}}$ - High-Priority Interrupt - This signal is asserted for any of the events enabled in the High-Priority Interrupt/Enable Register. Clear the level by writing a logic one to the corresponding bit in the High-Priority Interrupt Status/Reset Register.

Based on the interrupt scheme, the MT generates the Interrupt Log List to allow the host to review all interrupts in chronological order. Only one interrupt log will occur per message, except on retry failures. When an interrupt condition occurs, the MT performs two memory writes and one memory read to the Interrupt Log List Pointer Register. Definitions of all three words follow.

Interrupt Status Word - BCRTM written, this word will show the type of standard interrupt that occurred, if the interrupt is enabled. Active high bits indicate which of the interrupts were generated. Each bit in the Interrupt Status Word that is associated with the MT mode of operation is defined below:

Bit 15 This bit is always set during the DMA write of the Interrupt status word. Here, the host can reset this bit after reading the word to help determine which of the entries have been acknowledged.

Bit 14 No Response Time-Out - Under message error conditions, this bit is set to indicate that a message error time-out has occurred.

Bit 1 Message Error - This bit is set when a message error associated with the device's protocol logic has occurred.

Bit 0 Interrupt and Continue - This bit is set when the Command Block was addressed.

High-Priority Interrupt Status Register - BCRTM written, this register will show the type of High-Priority Interrupt that occurred, if the interrupt is enabled. Active high bits indicate which of the interrupts were generated. Each bit in the Interrupt Status Register that is associated with the MT mode of operation is defined below.

Bit 8 Data Overrun Enable - This bit, when set, indicates the BCRTM did not receive a $\overline{\text{DMAG}}$ within the allotted time to successfully perform a memory data transfer.

Bit 7 Illogical Command Error - This bit, when set, indicates the occurrence of an Illogical Command, which may include incorrectly formatted RT-RT Command Blocks.

Bit 1 Message Error - This bit is set at the occurrence of a message error.

If a High-Priority Interrupt occurs due to an illogical command, end of list, or a message error, the BCRTM will halt operation and stop execution until the user services the interrupt. Here the user must read the High-Priority Interrupt Status/Reset Register to pinpoint what caused the interrupt. Once the interrupt has been cleared, the device will automatically restart if the interrupt was due to a message error condition. However, once the interrupt has been cleared and the interrupt was due to an illogical command or End Of List, the user must restart the BCRTM by writing a logic one to bit 0 of the Control Register.

In the MT mode of operation if an interrupt condition occurs, the monitor performs the two writes and read listed above and then generates the interrupt pulse and level (if enabled).

5.0 Memory Architecture

After reviewing the BCRTM's internal registers, a look at the external memory requirements and how the host sets up memory in order to make the BCRTM a monitor may be advantageous. The intent of this memory section is to show that memory configurations are almost unlimited. Below are just two configurations used to allocate memory. Each configuration is discussed separately.

The first configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities, as figure 3 shows. The first block of memory is allocated for the Command Blocks. Notice that Register 2 initially points to the control/status word of the first Command Block. After completing execution of that first Command Block, Register 2 will automatically be updated to show the address associated with the next Command Block. Also the control/status word of the second Command Block may be located directly after the preceding Command Block's Tail Pointer.

Following all the Command Block locations is the memory required for all the data words. In some applications, the number of data words for each Command Block is known. However, if the number of data words is not known or undetermined, 32 memory locations must be set aside to meet the maximum data transfer for MIL-STD-1553B. In figure 3 for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. If the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List. The third block of memory is allocated for this Log List. Notice that Register 6 points to the top of the initial Log List. After execution of that first Command Block, Register 6 will automatically be updated. Notice the Tail Pointer of the first may be followed directly with the start of the second Log List.

A second memory configuration may wish to place all the Command Blocks, data, and interrupts associated with each message received together as figure 4 shows.

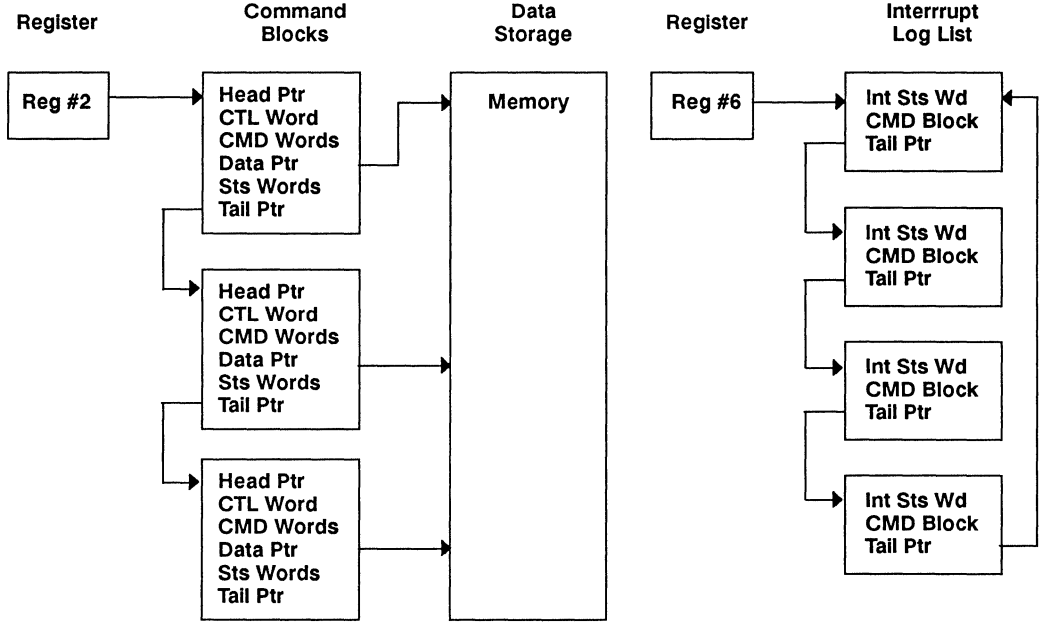


Figure 3. Memory Architecture For Monitor Mode

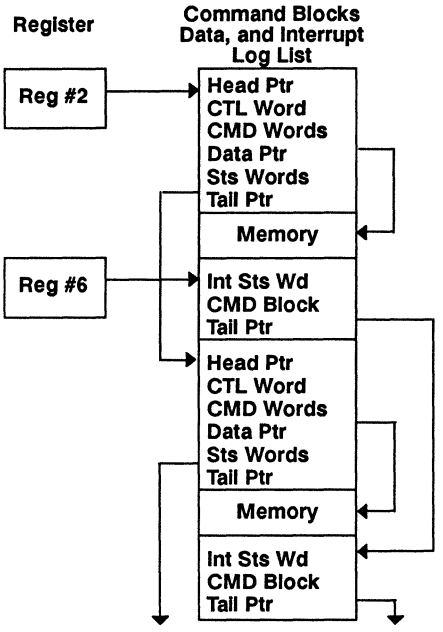
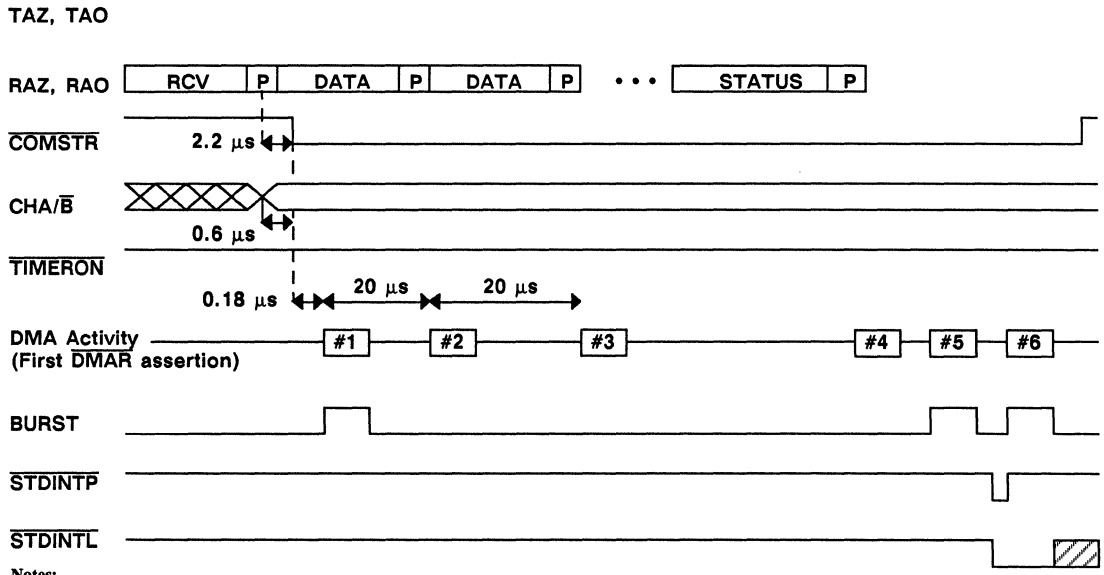


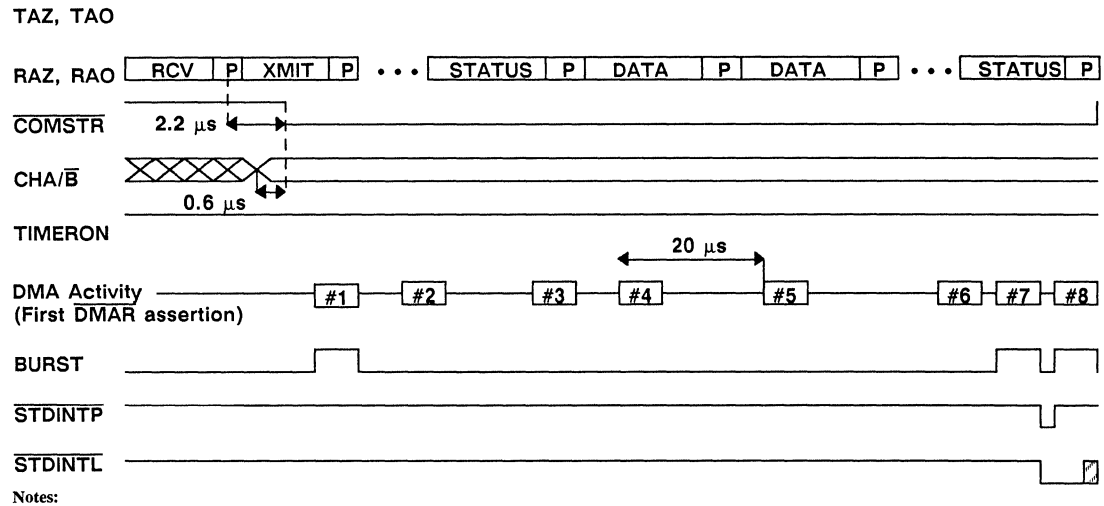
Figure 4. Memory Architecture For Monitor Mode

After reviewing the past several pages, it should be obvious that the designer has complete control over the MT memory mapping architecture. Each system may require slightly different memory requirements and the BCRTM's flexibility allows the user to "fill in the blanks." This flexibility allows designers to generate the correct memory map that meets their specific application. This mapping allows the definition of all Command Blocks, identifies where the data for each Command Block is stored, and clearly shows how much memory is required.



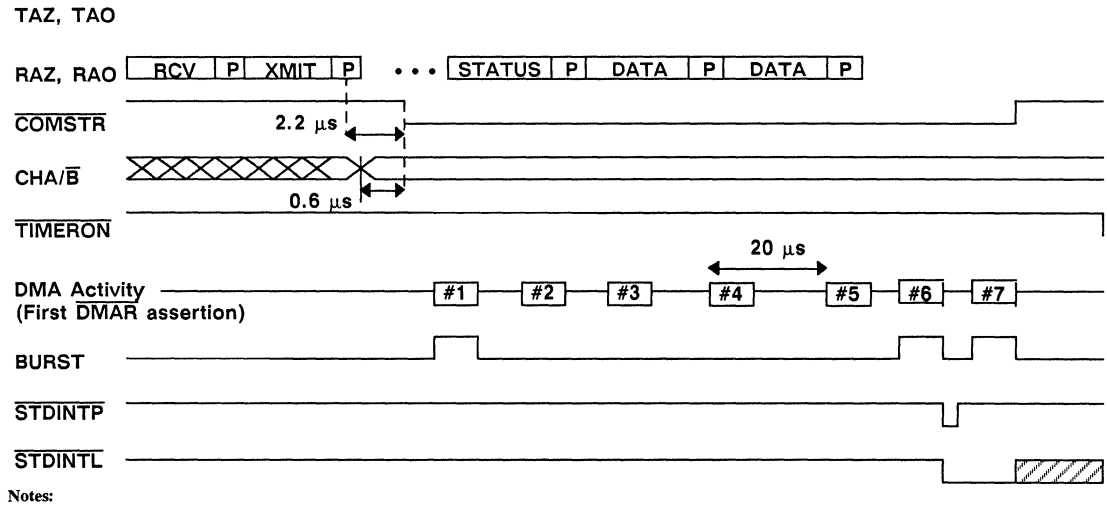
Notes:
1. Command Block read, Control word read, Command word write, Data pointer read.
2. Data word write.
3. Data word write.
4. Status word write.
5. Optional Interrupt Log.
6. Command Block update, Control word write, Read tail pointer.

Figure 5. Typical Receive Command (MT Mode)



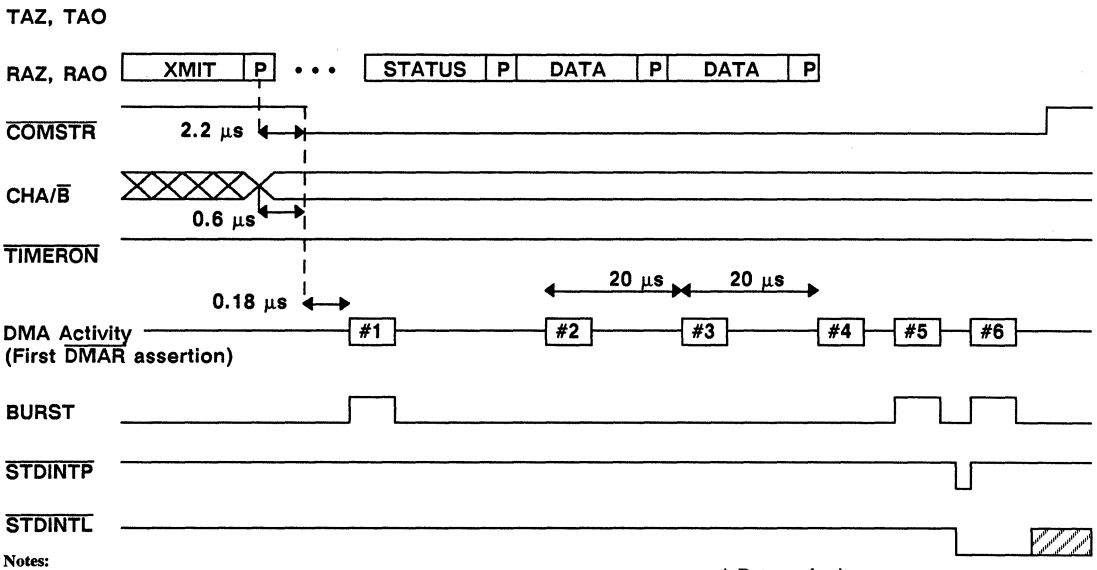
Notes:
1. Command Block read, Control word read, Command word write, Data pointer read.
2. Command word write.
3. Status word write.
4. Data word write.
5. Data word write.
6. Status word write.
7. Optional Interrupt Log.
8. Command Block update, Control word write, Read tail pointer.

Figure 6. Typical Timing for RT-RT Transfer (receive) (MT Mode)



Notes:
1. Command Block read, Control word read, Command word write, Data pointer read.
2. Command word write.
3. Status word write.
4. Data word write.
5. Data word write.
6. Optional Interrupt Log.
7. Command Block update, Control word write, Read tail pointer.

Figure 7. Typical Timing for RT-RT Transfer (transmit) (MT Mode)



Notes:
1. Command Block read, Control word read, Command word write, Data pointer read.
2. Write status word.
3. Write data word.
4. Data word write.
5. Optional Interrupt Log.
6. Command Block update, Control word write, Read tail pointer.

Figure 8. Typical Timing Transmit Command (MT Mode)

6.0 Programmed Design Example

This final MT section will offer an example to clearly define, initialize, and operate the BCRTM as a bus Monitor. The user will learn how to set up the registers, set up memory, and determine when the DMA transactions will occur.

For simplicity, the following baseline specifications will apply to our MT design. The specifications follow.

1. Operate the BCRTM as a bus Monitor.
2. Have the MT monitor RT addresses 2 and 23 only.
3. Enable Bus A and Bus B.
4. Start the Command Blocks at location 0000H.
5. Start the data words at location 1000H.
6. Start the Interrupt Log List at location 2000H.
7. Generate a standard-priority interrupt on message errors and when the Command Block is addressed.

6.1 Register Files

To effectively meet all the above requirements, a review of the registers is a must. The following discussion will review each register that is affected and show why the register was initialized to the stated value.

Control Register - Register 0

The Control Register will help the designer meet specifications 1 and 3 listed above. By writing 0180H to this register, the BCRTM will function as a bus Monitor (also need to initialize the Monitor Control Register) and enable both Bus A and Bus B. To verify this value (0180H), take a moment and review each bit in the Control Register.

Current Command Block Register - Register 2

This register may be initiated to meet specification 4. To have the Command Block Register start at location 0000H, simply have the host write that value (0000H) into Register 2 and make sure that the memory locations 0000H - 0007H contain the first Command Block. Again, depending on your memory structure and availability, the tail pointer of that first Command Block may point to 0008H (if following the setup in figure 3) or to just about any other location (as shown in figure 4).

Interrupt Log List Pointer Register - Register 6

This register may be used to meet 6 specification listed above. To have the Interrupt Log List Pointer start at location 2000H, simply have the host write that value (2000H) into Register 6 and make sure that memory locations 2002H are set aside for the three words previously defined by the Log List.

Standard Interrupt Enable Register - Register 9

To meet specification 7 above and have the MT generate an interrupt on message errors or if the Command Block is addressed, the host must initialize this register to 0003H. This value (0003H) will not only enable the BCRTM to generate a Standard-Priority Interrupt on the

occurrence but will allow the MT to log the interrupt into the Interrupt Log List for future evaluations.

Bus Monitor Control Register - Register 14

To meet specifications 1 and 2 above, the host must initialize this register to A000H. This value (A000H) will not only enable the Monitor function of the BCRTM but will also allow the MT to monitor specific remote terminals as specified by Registers 16 and 17.

Monitor Selected RT Addresses 15-0 - Register 16

To meet the final step of specification 2, the Monitor needs to monitor only RT 2 and 23. To select RT 2, the host must initialize this register to 0004H. This value (0004H) will enable the BCRTM to monitor RT 2 and store all data transactions to and from that RT.

Monitor Selected RT Addresses 31-16 - Register 17

To meet the final step of specification 2, the Monitor needs to monitor only RT 2 and 23. To select RT 23, the host must initialize this register to 0080H. This value (0080H) will enable the BCRTM to monitor RT 23 and store all data transactions to and from that RT. From previous discussion, each message on the 1553 bus must have a corresponding Command Block. The final specification can be handled while setting up the MT's Command Blocks. The last specification calls for the data list pointer to start at location 1000H. Refer to the following data to see this initialization.

MEMORY LOCATION	CONTENTS	COMMENTS CMD = Command Block
0000	0600	Control Word for CMD #1; message error and Interrupt When Addressed enabled.
0001	XXXX	Command Word #1 for CMD #1; to be updated as messages are received for RT #2 or #23.
0002	XXXX	Command Word #2 for CMD #1; this is to contain data for an RT-RT transfer.
0003	1000	Data List Pointer for CMD #1; to meet #5 specification above, all data is to start at location 1000H.
0004	XXXX	Status Word #1 for CMD #1; will be updated after the RT responds.
0005	XXXX	Status Word #2 for CMD #1; won't be used if not an RT-RT transfer.
0006	0007	Tail Pointer for CMD #1; should point to the start of the next Command Block.
0007	0600	Control Word for CMD #2; message error and Interrupt When Addressed enabled.
0008	XXXX	Command Word #1 for CMD #2; to be updated as messages are received for RT #2 or #23.
0009	XXXX	Command Word #2 for CMD #2; this is to contain data for an RT-RT transfer.
000A	1031	Data List Pointer for CMD #2; since the number of data words associated with the command is not known, the designer must leave 32 locations (maximum number of data words).
000B	XXXX	Status Word #1 for CMD #2; will be updated after the RT responds.
000C	XXXX	Status Word #2 for CMD #2; won't be used if not an RT-RT transfer.
000D	000E	Tail Pointer for CMD #2; should point to the start of the next Command Block.
000F	0600	Control Word for CMD #3; message error and Interrupt When Addressed enabled.
0010	XXXX	Command Word #1 for CMD #3; to be updated as messages are received for RT #2 or #23.
0011	XXXX	Command Word #2 for CMD #3; this is to contain data for an RT-RT transfer.
0012	1062	Data List Pointer for CMD #3; since the number of data words associated with the command is not known, the designer must leave 32 locations (maximum number of data words).
0013	XXXX	Status Word #1 for CMD #3; will be updated after the RT responds.
0014	XXXX	Status Word #2 for CMD #3; won't be used if not an RT-RT transfer.
0015	0000	Tail Pointer for CMD #3; should point to the start of the next Command Block.

Now that the BCRTM is set up to meet the specifications given, the device must be started and processing will begin. To start the device as a MT, a rewrite to the Control Register (Register 0) must occur to toggle the Start Enable (bit 0). Notice that in the initialization section 0600 was written to the Control Register. This value initialized the register but did not start the device. Now, if the value of 0601 is written to the Control Register, it will not only maintain the same setup configuration, but will also start the device.

6.2 DMA Activity

The MT mode of operation requires the BCRTM to access external memory in order to function properly. To gain access to the local bus, the BCRTM must arbitrate for that bus. Once $\overline{\text{DMAG}}$ is asserted, the MT may proceed with either a single memory access or multiple accesses (BURST). The following section describes what types of memory accesses are performed and when these occur. Figures 5-8 of this text or the applicable data sheet provides graphical representation of this DMA timing.

The MT operation is started by writing a "1" to Register 0, bit 0, after the external memory and internal registers are initialized. For BC to RT Commands, after a valid message is received, the MT performs a burst of three accesses. The MT reads the control word, writes the command word, and reads the Data List Pointer. If several data words are involved in the message, the DMAs (single) will continue until the message is completely received. Upon completion of this or any burst accesses, the BC surrenders the local bus by negating the $\overline{\text{DMACK}}$ output.

For RT to BC Command Blocks, the MT handles the message in the same fashion. As soon as the MT receives the RT status word, it immediately writes that value into the fifth location of the Command Block. Once again, if data words are involved in the message, the data word writes to memory will continue until all the data words are received.

While the Command Block DMA is the first burst mode the BCRTM uses, there are several other burst conditions. The second burst (burst of three) occurs when an interrupt condition is met during a message transfer. If a standard interrupt condition is met, the MT writes the Interrupt status word, writes the Monitor Command Block Pointer, reads the Tail Pointer, pulses the $\overline{\text{STDINTP}}$ signal, and asserts the $\overline{\text{STDINTL}}$ (if enabled).

The third burst mode occurs when used during normal execution with no message errors during the current Command Block. Here the MT executes on two words by writing the control/status word and reading the Command Block Tail Pointer. By doing so, the BCRTM is ready to monitor the next Command Block.

Table of Contents

UT1553B BCRT

FEATURES

- ☐ Comprehensive MIL-STD-1553B dual-redundant Bus Controller (BC) and Remote Terminal (RT) functions
- ☐ Multiple message processing capability in BC and RT modes
- ☐ Automatic polling and intermessage delay in BC mode
- ☐ Programmable interrupt scheme and internally generated interrupt history list
- ☐ Register-oriented architecture to enhance programmability
- ☐ DMA or pseudo-dual-port memory interface with 64K addressability
- ☐ Internal wraparound self-test
- ☐ Time tagging and message logging in RT mode
- ☐ Packaged in 84-pin pingrid array, 84-lead flatpack, or 84-pad LCC
- ☐ Low-power CMOS technology
- ☐ Full military operating temperature range, −55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B

3

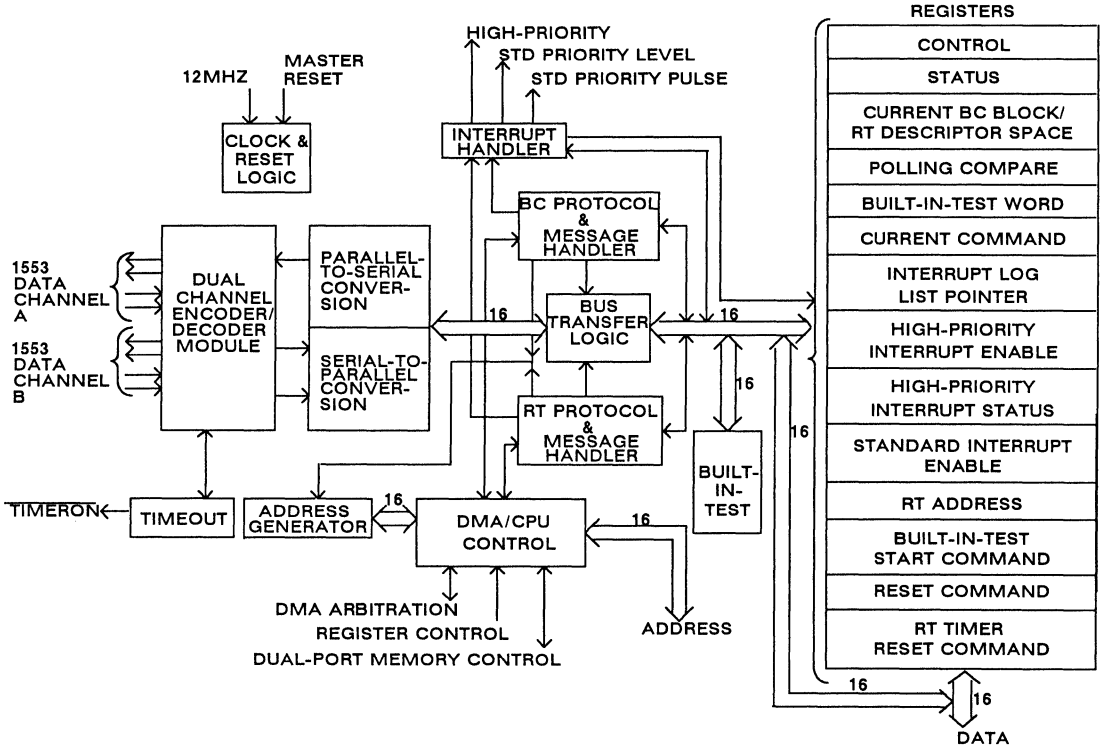


Figure 1. BCRT Block Diagram

Table of Contents

1.0 INTRODUCTION

The monolithic CMOS UT1553B BCRT provides the system designer with an intelligent solution to MIL-STD-1553B multiplexed serial data bus design problems. The UT1553B BCRT is a single-chip device that implements two of the defined MIL-STD-1553B functions - Bus Controller and Remote Terminal. Designed to reduce host CPU overhead, the BCRT's powerful state machines automatically execute message transfers, provide interrupts, and generate status information. Multiple registers offer many programmable functions as well as extensive information for host use. In the BC mode, the BCRT uses a linked-list message scheme to provide the host with message chaining capability. The BCRT enhances memory use by supporting variable-size, relocatable data blocks. In the RT mode, the BCRT implements time-tagging and message history functions. It also supports multiple (up to 128) message buffering and variable length messages to any subaddress.

The UT1553B BCRT is an intelligent, versatile, and easy to implement device -- a powerful asset to system designers.

1.1 Features - Remote Terminal (RT) Mode

Indexing
The BCRT is programmable to index or buffer messages on a subaddress-by-subaddress basis. The BCRT, which can index as many as 128 messages, can also assert an interrupt when either the selected number of messages is reached or every time a specified subaddress is accessed.

Variable Space Allocation
The BCRT can use as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRT provides flexible data placement and convenient access.

Sequential Data Storage
The BCRT stores/retrieves, by subaddress, all messages in the order in which they are transacted.

Sequential Message Status Information
The BCRT provides message validity, time-tag, and word-count information, and stores it sequentially in a separate, cross-referenced list.

Illegalizing Mode Codes and Subaddresses
The host can declare mode codes and subaddresses illegal by setting the appropriate bit(s) in memory.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRT provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

1.2 Features - Bus Controller (BC) Mode

Multiple Message Processing
The BCRT autonomously processes any number of messages or lists of messages that may be stored in a 64K memory space.

Automatic Intermessage Delay
When programmed by the host, the BCRT can delay a host-specified time before executing the next message in sequence.

Automatic Polling
When polling, the BCRT interrogates the remote terminals and then compares their status word responses to the contents of the Polling Compare Register. The BCRT can interrupt the host CPU if an erroneous remote terminal status word response occurs.

Automatic Retry
The BCRT can automatically retry a message on busy, message error, and/or response time-out conditions. The BCRT can retry up to four times on the same or on the alternate bus.

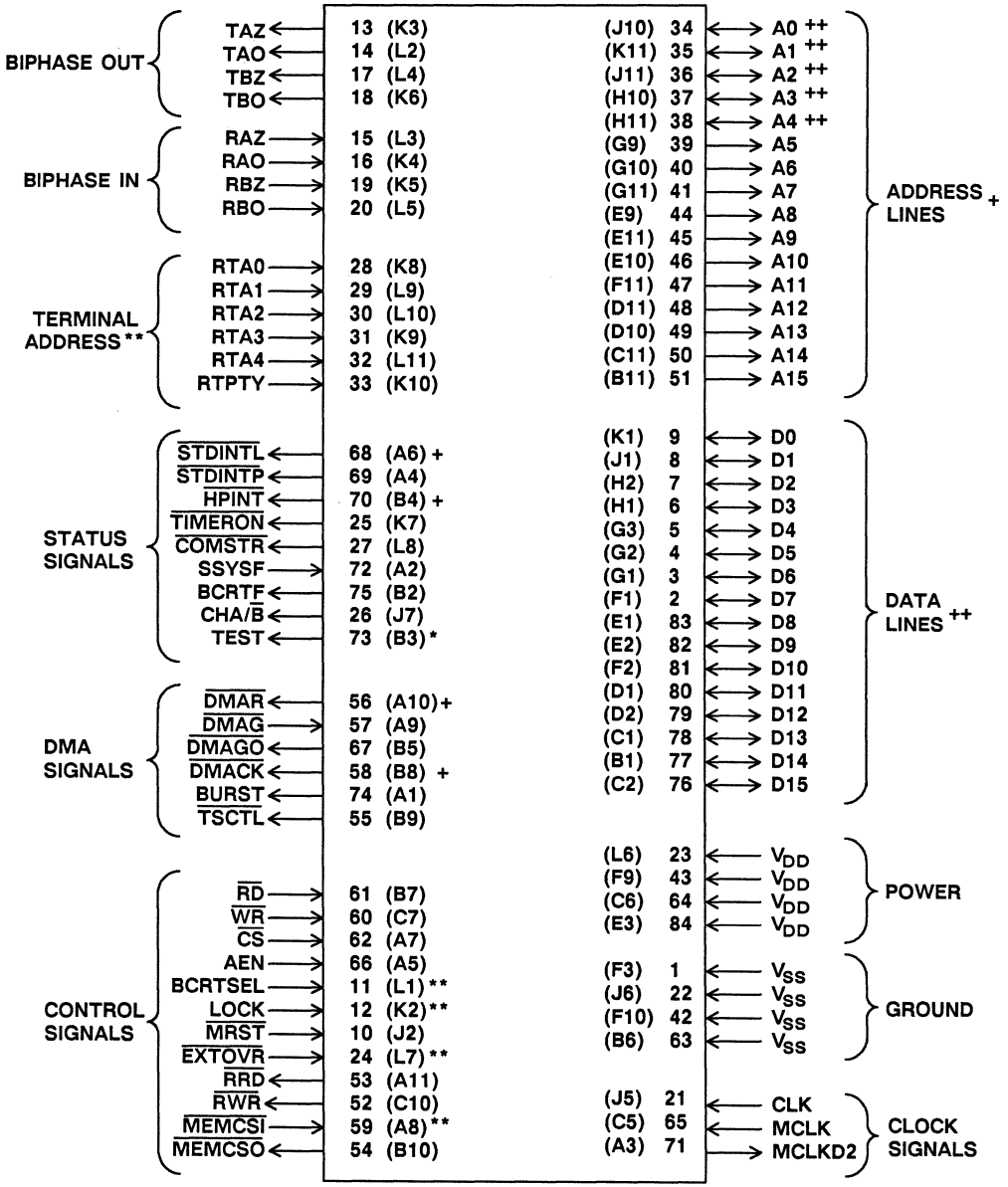
Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRT provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

Variable Space Allocation
The BCRT uses as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRT provides flexible data placement and convenient access.

2.0 Pin Identification And Description



** Pin internally pulled up.

+ Pin at high impedance when not asseted

++ Bidirectional pin.

• Formerly $\overline{\text{MEMWIN}}$.

( ) Pingrid array lead identification in parentheses.
LCC, flatpack pin number not in parentheses.

Figure 2. BCRT Functional Pin Description

Legend for TYPE and ACTIVE fields:

TUI = TTL Input (pull-up)
AL = Active low
AH = Active high
ZL = Active low - inactive state is high impedance
TI = TTL input
TO = TTL output
TTO = Three-state TTL output
TTB = Bidirectional

Notes:
1. Address and data buses are in the high-impedance state when idle.
2. Flatpack pin numbers are same as LCC.

ADDRESS BUS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
A0	34	J10	TTB	--	Bit 0 (LSB) of the Address bus
A1	35	K11	TTB	--	Bit 1 of the Address bus
A2	36	J11	TTB	--	Bit 2 of the Address bus
A3	37	H10	TTB	--	Bit 3 of the Address bus
A4	38	H11	TTO	--	Bit 4 of the Address bus
A5	39	G9	TTO	--	Bit 5 of the Address bus
A6	40	G10	TTO	--	Bit 6 of the Address bus
A7	41	G11	TTO	--	Bit 7 of the Address bus
A8	44	E9	TTO	--	Bit 8 of the Address bus
A9	45	E11	TTO	--	Bit 9 of the Address bus
A10	46	E10	TTO	--	Bit 10 of the Address bus
A11	47	F11	TTO	--	Bit 11 of the Address bus
A12	48	D11	TTO	--	Bit 12 of the Address bus
A13	49	D10	TTO	--	Bit 13 of the Address bus
A14	50	C11	TTO	--	Bit 14 of the Address bus
A15	51	B11	TTO	--	Bit 15 (MSB) of the Address bus

DATA BUS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
D0	9	K1	TTB	--	Bit 0 (LSB) of the Data bus
D1	8	J1	TTB	--	Bit 1 of the Data bus
D2	7	H2	TTB	--	Bit 2 of the Data bus
D3	6	H1	TTB	--	Bit 3 of the Data bus
D4	5	G3	TTB	--	Bit 4 of the Data bus
D5	4	G2	TTB	--	Bit 5 of the Data bus
D6	3	G1	TTB	--	Bit 6 of the Data bus
D7	2	F1	TTB	--	Bit 7 of the Data bus
D8	83	E1	TTB	--	Bit 8 of the Data bus
D9	82	E2	TTB	--	Bit 9 of the Data bus
D10	81	F2	TTB	--	Bit 10 of the Data bus
D11	80	D1	TTB	--	Bit 11 of the Data bus
D12	79	D2	TTB	--	Bit 12 of the Data bus
D13	78	C1	TTB	--	Bit 13 of the Data bus
D14	77	B1	TTB	--	Bit 14 of the Data bus
D15	76	C2	TTB	--	Bit 15 (MSB) of the Data bus

TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
RTA0	28	K8	TUI	--	Remote Terminal Address Bit 0 (LSB). The entire RT address is strobed in at Master Reset. Verify it by reading the Remote Terminal Address Register. All the Remote Terminal Address bits are internally pulled up.
RTA1	29	L9	TUI	--	Remote Terminal Address Bit 1. This is bit 1 of the Remote Terminal Address.
RTA2	30	L10	TUI	--	Remote Terminal Address Bit 2. This is bit 2 of the Remote Terminal Address.
RTA3	31	K9	TUI	--	Remote Terminal Address Bit 3. This is bit 3 of the Remote Terminal Address.
RTA4	32	L11	TUI	--	Remote Terminal Address Bit 4. This is bit 4 (MSB) of the Remote Terminal Address.
RTPTY	33	K10	TUI	--	Remote Terminal (Address) Parity. This is an odd parity input for the Remote Terminal Address.

CONTROL SIGNALS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{RD}$	61	B7	TI	AL	Read. The host uses this in conjunction with $\overline{CS}$ to read an internal BCRT register.
$\overline{WR}$	60	C7	TI	AL	Write. The host uses this in conjunction with $\overline{CS}$ to write to an internal BCRT register.
$\overline{CS}$	62	A7	TI	AL	Chip Select. This selects the BCRT when accessing the BCRT's internal register.
AEN	66	A5	TI	AH	Address Enable. The host CPU uses AEN to indicate to the BCRT that the BCRT's address lines can be asserted; this is a precautionary signal provided to avoid address bus crash. If not used, it must be tied high.
BCRTSEL	11	L1	TUI	--	BC/$\overline{RT}$ Select. This selects between either the Bus Controller or Remote Terminal mode. The BC/RT Mode Select bit in the Control Register overrides this input if the LOCK pin is not high. This pin is internally pulled high.
LOCK	12	K2	TUI	AH	Lock. When set, this pin prevents internal changes to both the RT address and BC/$\overline{RT}$ mode select functions. This pin is internally pulled high.
$\overline{EXTOVR}$	24	L7	TUI	AL	External Override. Use this in multi-redundant applications. Upon receipt, the BCRT aborts all current activity. EXTOVR should be connected to $\overline{COMSTR}$ output of the adjacent BCRT when used. This pin is internally pulled high.
$\overline{MRST}$	10	J2	TI	AL	Master Reset. This resets all internal state machines, encoders, decoders, and registers. The minimum pulse width for a successful Master Reset is 500ns.
$\overline{MEMCSO}$	54	B10	TO	AL	Memory Chip Select Out. This is the regenerated MEMCSI input for external RAM during the pseudo-dual-port RAM mode. The BCRT also uses it to select external memory during memory accesses.
$\overline{MEMCSI}$	59	A8	TUI	AL	Memory Chip Select In. Used in the pseudo-dual-port RAM mode only, $\overline{MEMCSI}$ is received from the host and is propagated through to $\overline{MEMCSO}$.
$\overline{RRD}$	53	A11	TO	AL	RAM Read. In the pseudo-dual-port RAM mode, the host uses this signal in conjunction with $\overline{MEMCSO}$ to read from external RAM through the BCRT. It is also the signal the BCRT uses to read from memory. It is asserted following receipt of $\overline{DMAG}$. When the BCRT performs multiple reads, this signal is pulsed.
$\overline{RWR}$	52	C10	TO	AL	RAM Write. In the pseudo-dual-port RAM mode, the CPU and BCRT use this to write to external RAM. This signal is asserted following receipt of $\overline{DMAG}$. For multiple writes, this signal is pulsed.

STATUS SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{STDINTL}}$	68	A6	TTO	ZL	Standard Interrupt Level. This is a level interrupt. It is asserted when one or more events enabled in either the Standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur. Resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register clears the interrupt.
$\overline{\text{STDINTP}}$	69	A4	TO	AL	Standard Interrupt Pulse. $\overline{\text{STDINTP}}$ pulses when an interrupt is logged.
$\overline{\text{HPINT}}$	70	B4	TTO	ZL	High-Priority Interrupt. The High-Priority Interrupt level is asserted upon occurence of events enabled in the High-Priority Interrupt Enable Register. The corresponding bit(s) in the High-Priority Interrupt Status/Reset Register reset $\overline{\text{HPINT}}$.
$\overline{\text{TIMERON}}$	25	K7	TO	AL	(RT) Timer On. This is a 760-microsecond fail-safe transmitter enable timer. Started at the beginning of a transmission, $\overline{\text{TIMERON}}$ goes inactive 760 microseconds later or is reset automatically with the receipt of a new command. Use it in conjunction with CHA/$\overline{\text{B}}$ output to provide a fail-safe timer for Channels A and B transmitters.
$\overline{\text{COMSTR}}$	27	L8	TO	AL	(RT) Command Strobe. The BCRT asserts this signal after receiving a valid command. The BCRT deactivates it after servicing the command.
SSYSF	72	A2	TI	AH	Subsystem Fail. Upon receipt, this signal propagates directly to the RT 1553 status word and the BCRT Status Register.
BCRTF	75	B2	TO	AH	BCRT Fail. This indicates a Built-In-Test (BIT) failure. In the RT mode, the Terminal Flag bit in 1553 status word is also set.
CHA/$\overline{\text{B}}$	26	J7	TO	--	Channel A/$\overline{\text{B}}$. This indicates the active or last active channel.
TEST	73	B3	TO	AL	Test. This pin is used as a factory test pin. (Formerly $\overline{\text{MEMWIN}}$.)

BIPHASE INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
RAO	16	K4	TI	--	Receive Channel A One. This is the Manchester-encoded true signal input from Channel A of the bus receiver.
RAZ	15	L3	TI	--	Receive Channel A Zero. This is the Manchester-encoded complementary signal input from Channel A of the bus receiver.
RBO	20	L5	TI	--	Receive Channel B One. This is the Manchester-encoded true signal input from Channel B of the bus receiver.
RBZ	19	K5	TI	--	Receive Channel B Zero. This is the Manchester-encoded complementary signal input from Channel B of the bus receiver.

BIPHASE OUTPUTS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
TAO	14	L2	TO	--	Transmit Channel A One. This is the Manchester-encoded true output to be connected to the Channel A bus transmitter input. This signal is idle low.
TAZ	13	K3	TO	--	Transmit Channel A Zero. This is the Manchester-encoded complementary output to be connected to the Channel A bus transmitter input. This signal is idle low.
TBO	18	K6	TO	--	Transmit Channel B One. This is the Manchester-encoded true output to be connected to the Channel B bus transmitter input. This signal is idle low.
TBZ	17	L4	TO	--	Transmit Channel B Zero. This is the Manchester-encoded complementary output to be connected to the Channel B bus transmitter input. This signal is idle low.

DMA SIGNALS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{DMAR}}$	56	A10	TTO	ZL	DMA Request. The BCRT issues this signal when access to RAM is required. It goes inactive after receiving a $\overline{\text{DMAG}}$ signal.
$\overline{\text{DMAG}}$	57	A9	TI	AL	DMA Grant. This input to the BCRT allows the BCRT to access RAM. It is recognized 45 ns before the rising edge of MCLKD2.
$\overline{\text{DMAGO}}$	67	B5	TO	AL	DMA Grant Out. If $\overline{\text{DMAG}}$ is received but not needed, it passes through to this output.
$\overline{\text{DMACK}}$	58	B8	TTO	ZL	DMA Acknowledge. The $\overline{\text{BCRTM}}$ asserts this signal to confirm receipt of $\overline{\text{DMAG}}$; it stays low until memory access is complete.
BURST	74	A1	TO	AH	Burst (DMA Cycle). This indicates that the current DMA cycle transfers at least two words; worst case is five words plus a "dummy" word.
$\overline{\text{TSCTL}}$	55	B9	TO	AL	Three-State Control. This signal indicates when the BCRT is actually accessing memory. The host subsystem's address and data lines must be in the high-impedance state when the signal is active. This signal assists in placing the external data and address buffers into the high-impedance state.

CLOCK SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
CLK	21	J5	TI	--	Clock. The 12 MHz input clock requires a 50% +/-10% duty cycle with an accuracy of +/-0.01%. The accuracy is required in order to meet the Manchester encoding/decoding requirements of MIL-STD-1553B.
MCLK	65	C5	TI	--	Memory Clock. This is the input clock frequency the BCRT uses for memory accesses. The memory cycle time is equal to two MCLK cycles. Therefore, RAM access time is dependent upon the chosen MCLK frequency (6 MHz minimum, 12 MHz maximum). Please see the BCRT DMA timing diagrams in this data sheet.
MCLKD2	71	A3	TO	--	Memory Clock Divided by Two. This signal is the Memory Clock input divided by two. It assists the host subsystem in synchronizing DMA events.

POWER AND GROUND

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
V_{DD}	23	L6	PWR	--	+5V
V_{DD}	43	F9	PWR	--	+5V
V_{DD}	64	C6	PWR	--	+5V
V_{DD}	84	E3	PWR	--	+5V
V_{SS}	1	F3	GND	--	Ground
V_{SS}	22	J6	GND	--	Ground
V_{SS}	42	F10	GND	--	Ground
V_{SS}	63	B6	GND	--	Ground

3.0 INTERNAL REGISTERS

The BCRT's internal registers (see table 1 on pages 16-17) enable the CPU to control the actions of the BCRT while maintaining low DMA overhead by the BCRT. All functions are active high and ignored when low unless stated otherwise. Functions and parameters are used in both RT and BC modes except where indicated. Registers are addressed by the binary equivalent of their decimal number. For example, Register 1 is addressed as 0001B. Register usage is defined as follows:

#0 Control Register

Bit Number	Description
BIT 15-12	Reserved.
BIT 11	Enable External Override. For use in multi-redundant systems. This bit enables the $\overline{\text{EXTOVR}}$ pin.
BIT 10	BC/$\overline{\text{RT}}$ Select. This function selects between the Bus Controller and Remote Terminal operation modes. It overrides the external BCRTSEL input setting if the Change Lock-Out function is not used. A reset operation must be performed when changing between BC and RT modes. This bit is write-only.
BIT 9	(BC) Retry on Alternate Bus. This bit enables an automatic retry to operate on alternate buses. For example, if on bus A, with two automatic retries programmed, the automatic retries occur on bus B.
BIT 8	(RT) Channel B Enable. When set, this bit enables Channel B operation. (BC) No significance.
BIT 7	(RT) Channel A Enable. When set, this bit enables Channel A operation. (BC) Channel Select A/$\overline{\text{B}}$. When set, this bit selects Channel A.
BITs 6-5	(BC) Retry Count. These bits program the number (1-4) of retries to attempt. (00 = 1 retry, 11 = 4 retries)
BIT 4	(BC) Retry on Bus Controller Message Error. This bit enables automatic retries on an error the Bus Controller detects (see the Bus Controller Architecture section, page 27).
BIT 3	(BC) Retry on Time-Out. This bit enables an automatic retry on a response time-out condition.
BIT 2	(BC) Retry on Message Error. This bit enables an automatic retry when the Message Error bit is set in the RT's status word response.
BIT 1	(BC) Retry on Busy. This bit enables automatic retry on a received Busy bit in an RT status word response.
BIT 0	Start Enable. In the BC mode, this bit starts/restarts Command Block execution. In the RT mode, it enables the BCRT to receive a valid command. RT operation does not start until a valid command is received. When using this function: • Restart the BCRT after each Master Reset or programmed reset. • This bit is not readable; verify operation by reading bit 0 of the BCRT's Status Register.

#1 Status Register (Read Only)
These bits indicate the BCRT's current status.

Bit Number	Description
BIT 15	TEST. This bit reflects the inverse of the TEST output. It changes state simultaneously with the TEST output.
BIT 14	(RT) Remote Terminal Active. Indicates that the BCRT, in the Remote Terminal mode, is presently servicing a command. This bit reflects the inverse of the $\overline{\text{COMSTR}}$ pin.
BIT 13	(RT) Dynamic Bus Control Acceptance. This bit reflects the state of the Dynamic Bus Control Acceptance bit in the RT status word (see Register 10 on page 15).
BIT 12	(RT) Terminal Flag bit is set in RT status word. This bit reflects the result of writing to Register 10, bit 11.
BIT 11	(RT) Service Request bit is set in RT status word. This bit reflects the result of writing to Register 10, bit 10.
BIT 10	(RT) Busy bit is set in RT status word. This bit reflects the result of writing to Register 10, bits 9 or 14.
BIT 9	BIT is in progress.
BIT 8	Reset is in progress. This bit indicates that either a write to Register 12 has just occurred or the BCRT has just received a Reset Remote Terminal (#01000) Mode Code. This bit remains set less than one microsecond.
BIT 7	BC/$\overline{\text{RT}}$ Mode. Indicates the current mode of operation. A reset operation must be performed when changing between BC and RT modes.
BIT 6	Channel A/$\overline{\text{B}}$. Indicates either the channel presently in use or the last channel used.
BIT 5	Subsystem Fail Indicator. Indicates receiving a subsystem fail signal from the host subsystem on the SSYSF input.
BITs 4-1	Reserved.
BIT 0	(BC) Command Block Execution is in progress. (RT) Remote Terminal is in operation. This bit reflects bit 0 of Register 0.

#2 Current Command Block Register (BC)/Remote Terminal Descriptor Space Address Register (RT)
(BC) This register contains the address of the head pointer of the Command Block being executed. Accessing a new Command Block updates it.

(RT) The host CPU initializes this register to indicate the starting location of the RT Descriptor Space. The host must allocate 320 sequential locations following this starting address. For proper operation, this location must start on an I x 512 decimal address boundary, where I is an integer multiple. (I = 0 is valid boundary condition.)

#3 Polling Compare Register
In the polling mode, the CPU sets the Polling Compare Register to indicate the RT response word on which the BCRT should interrupt. This register is 11 bits wide, corresponding to bit times 9 through 19 of the RT's 1553 status word response. The sync, Remote Terminal Address, and parity bits are not included (see the section on Polling, page 30).

#4 BIT (Built-In-Test) Word Register
The BCRT uses the contents of this register when it responds to the Transmit BIT Word Mode Code (#10011). In addition, the BCRT writes to the two most significant bits of the BIT Word Register in response to either an Initiate Self-Test Mode Code (RT mode) or a write to Register 11 (BIT Start Command). If the BIT Word needs to be modified, it can be read out, modified, then rewritten to this register. Note that if the processor writes a "1" to either bit 14 or 15 of this register, it effectively induces a BIT failure.

Bit Number	Description
BIT 15	Channel B. Failure.
BIT 14	Channel A. Failure.
BITs 13-0	BIT Word. The least significant fourteen bits of the BIT Word are user programmable.

#5 Current Command Register (Read Only)
In the RT mode, this register contains the command currently being processed. When not processing a command, the BCRT stores the last command or status word transmitted on the 1553B bus. This register is updated only when bit 0 of Register 0 is set. In the BC mode, this register contains the most current command sent out on the 1553B bus.

#6 Interrupt Log List Pointer Register
Initialized by the CPU, the Interrupt Log List Pointer Register indicates the start of the Interrupt Log List. After each list entry, the BCRT updates this register with the address of the next entry in the list. (See page 33.)

#7 High-Priority Interrupt Enable Register (R/W)
Setting the bits in this register causes a High-Priority Interrupt when the enabled event occurs. To service the High-Priority Interrupt, the user reads Register 8 to determine the cause of the interrupt, then writes to Register 8 to clear the appropriate bits. The BCRT also provides a Standard Priority Interrupt Scheme that does not require host intervention. If High-Priority Interrupt service is not possible in a given application, it is advisable to use the Standard Priority features.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun Enable. When set, this bit enables an interrupt when $\overline{\text{DMAG}}$ was not received by the BCRT within the allotted time needed for a successful data transfer to memory.
BIT 7	(BC) Illogical Command Error Enable. This bit enables a High-Priority Interrupt to be asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formated RT-RT Command Blocks.
BIT 6	(RT) Dynamic Bus Control Mode Code Interrupt Enable. When set, the BCRT asserts an interrupt when the Dynamic Bus Control Mode Code is received.
BIT 5	Subsystem Fail Enable. When set, a High-Priority Interrupt is asserted after receiving a Subsystem Fail (SSYSF) input pin.
BIT 4	End of BIT Enable. This bit indicates the end of the internal BIT routine.
BIT 3	BIT Word Fail Enable. This bit enables an interrupt indicating that the BCRT detected a BIT failure.
BIT 2	(BC) End of Command Block List Enable (see Command Block Control Word, page 29.) This interrupt can be superseded by other high-priority interrupts.
BIT 1	Message Error Enable. If enabled, a High-Priority Interrupt is asserted at the occurrence of a message error. If a High-Priority Interrupt condition occurs, as the result of an enabled message error, the device will halt operation until the user clears the interrupt by writing a "1" to bit 1 of the High-Priority Interrupt Status/Reset Register (Reg. #8). If this interrupt is not cleared, the BCRT remains in the HALTED state (appearing to be "locked-up"), even if it receives a valid message. This High-Priority Interrupt scheme is necessary in order to maintain the BCRT's state of operation so that the host CPU has this information available at the time of interrupt service.
BIT 0	Standard Interrupt Enable. Setting this bit enables the $\overline{\text{STDINTL}}$ pin, but does not cause a high-priority interrupt. If low, only the $\overline{\text{STDINTP}}$ pin is asserted when a Standard Interrupt occurs.

#8 High-Priority Interrupt Status/Reset Register

When a High-Priority Interrupt is asserted, this register indicates the event that caused it. To clear the interrupt signal and reset the bit, write a "1" to the appropriate bit. See the corresponding bit definitions of Register 7, High-Priority Interrupt Enable Register.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun.
BIT 7	Illogical Command.
BIT 6	Dynamic Bus Control Mode Code Received.
BIT 5	Subsystem Fail.
BIT 4	End of BIT.
BIT 3	BIT Word Fail.
BIT 2	End of Command Block.
BIT 1	Message Error.
BIT 0	Standard Interrupt. The BCRT sets this bit when any Standard Interrupt occurs, providing bit 0 of Register 7 is enabled. (Reset $\overline{\text{STDINTL}}$ output.)

#9 Standard Interrupt Enable Register

This register enables Standard Interrupt logging for any of the following enabled events (Standard Interrupt logging can also occur for events enabled in the BC Command Block or RT Subaddress/Mode Code Descriptor):

Bit Number	Description
BITs 15-6	Reserved.
BIT 5	(RT) Illegal Broadcast Command. When set, this bit enables an interrupt indicating that an Illegal Broadcast Command has been received.
BIT 4	(RT) Illegal Command. When set, this bit enables an interrupt indicating that an illegal command has been received.
BIT 3	(BC) Polling Comparison Match. This enables an interrupt indicating that a polling event has occurred. The user must also set bit 12 in the BC Command Block Control Word for this interrupt to occur.
BIT 2	(BC) Retry Fail. This bit enables an interrupt indicating that all the programmed number of retries have failed.
BIT 1	(BC,RT) Message Error Event. This bit enables a standard interrupt for message errors.
BIT 0	(BC) Command Block Interrupt and Continue. This bit enables an interrupt indicating that a Command Block, with the Interrupt and Continue Function enabled, has been executed.

#10 Remote Terminal Address Register
This register sets the Remote Terminal Address via software. The Change Lock-Out Enable feature, when set, prevents the Remote Terminal Address or the BCRT Mode Selection from changing.

Bit Number	Description
BIT 15	(RT) Instrumentation. Setting this bit sets the RT status word Instrumentation bit.
BIT 14	(RT) Busy. Setting this bit sets the RT status word Busy bit. It does not inhibit data transfers to the subsystem.
BIT 13	(RT) Subsystem Fail. Setting this bit sets the RT status word Subsystem Flag bit. In the RT mode, the Subsystem Fail is also logged into the Message Status Word.
BIT 12	(RT) Dynamic Bus Control Acceptance. Setting this bit sets the RT status word Dynamic Bus Control Acceptance bit when the BCRT receives the Dynamic Bus Control Mode Code from the currently active Bus Controller. Host intervention is required for the BCRT to take over as the active Bus Controller.
BIT 11	(RT) Terminal Flag. Setting this bit sets the RT status word Terminal Flag bit; the Terminal Flag bit in the RT status word is also internally set if the BIT fails.
BIT 10	(RT) Service Request. Setting this bit sets the RT status word Service Request bit.
BIT 9	(RT) Busy Mode Enable. Setting this bit sets the RT status word Busy bit and inhibits all data transfers to the subsystem.
BIT 8	BC/$\overline{RT}$ Mode Select. This bit's state reflects the external pin BCRTSEL. It does not necessarily reflect the state of the chip, since the BC/$\overline{RT}$ Mode Select is software-programmable via bit 10 of Register 0. This bit is read-only.
BIT 7	Change Lock-Out. This bit's state reflects the external pin LOCK. When set, this bit indicates that changes to the RT address or the BC/$\overline{RT}$ Mode Select are not allowed using internal registers. This bit is read-only.
BIT 6	Remote Terminal Address Parity Error. This bit indicates a Remote Terminal Address Parity error. It appears after the Remote Terminal Address is latched if a parity error exists.
BIT 5	Remote Terminal Address Parity. This is an odd parity input bit used with the Remote Terminal Address. It ensures accurate recognition of the Remote Terminal Address.
BITs 4-0	Remote Terminal Address (Bit 0 is the LSB). This reflects the RTA4-0 inputs at Master Reset. Modify the Remote Terminal Address by writing to these bits.

#11 BIT Start Register (Write Only)
Any write (i.e., data = don't care) to this register's address location initiates the internal BIT routine, which lasts 100 μs. Verify using the BIT-in-progress bit in the Status Register. A programmed reset (write to Register 12) must precede a write to this register to initiate the internal BIT. A failure of the BIT will be indicated in Register 4 and the BCRTF pin.

The BCRT's self-test performs an internal wrap around test between its Manchester encoder and its two Manchester decoders. If the BCRT detects a failure on either the primary or the secondary channel, it flags this failure by setting bit 14 of Register 4 (BIT Word Register) for Channel A and/or bit 15 for Channel B. When in the Remote Terminal mode, while the BCRT is performing its self-test, it ignores any commands on the 1553 bus until it has completed the self-test.

#12 Programmed Reset Register (Write Only)
Any write (i.e., data = don't care) to this register's address location initiates a reset sequence of the encoder/decoder and protocol sections of the BCRT which lasts less than 1 microsecond. This is identical to the reset used for the Reset Remote Terminal Mode Code except that command processing halts. For a total reset (i.e., including registers), see the $\overline{MRST}$ signal description.

#13 RT Timer Reset Register (Write Only)
Any write (i.e., data = don't care) to this register's address location resets the RT Time Tag timer to zero. The BCRT's Remote Terminal Timer time-tags message transactions. The time tag is generated from a free-running eight-bit timer of 64 microseconds resolution. This timer can be reset to zero simply by writing to Register 13. When the timer is reset, it immediately starts running.

#0 BC/RT CONTROL REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	EXTOVR	BC/RT	RTYALTB	BUSBEN
7	6	5	4	3	2	1	0
CHNSEL BUSAEN	RTYCNT		RTYBCME	RTYTO	RTYME	RTYBSY	STEN

#1 BC/RT STATUS REGISTER

15	14	13	12	11	10	9	8
TEST	RTACT	DYNBUS	RT FLAG	SRQ	BUSY	BIT	RESET
7	6	5	4	3	2	1	0
BC/RT	BUSA/B	SSFAIL	UNUSED	UNUSED	UNUSED	UNUSED	CMBKPG

#2 (BC) CURRENT COMMAND BLOCK REGISTER
(RT) REMOTE TERMINAL DESCRIPTOR SPACE ADDRESS REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#3 POLLING COMPARE REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	MSGERR	INSTR	SRQ
7	6	5	4	3	2	1	0
SWBT12	SWBT13	SWBT14	BRDCST	BUSY	SS FLAG	DBC	RT FLAG

#4 BIT WORD REGISTER

15	14	13	12	11	10	9	8
CHBFAIL	CHAFAIL	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#5 CURRENT COMMAND REGISTER

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#6 INTERRUPT LOG LIST POINTER REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#7 BCRT HIGH-PRIORITY INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DMAERR
7	6	5	4	3	2	1	0
CMDERR	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

#8 BCRT HIGH-PRIORITY INTERRUPT STATUS/RESET REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

Table 1. BCRT Registers

#9 STANDARD INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
7	6	5	4	3	2	1	0
UNUSED	UNUSED	ILLBCMD	ILLCMD	POLFAIL	RTYFAIL	MSGERR	CMDBLK

#10 REMOTE TERMINAL ADDRESS REGISTER

15	14	13	12	11	10	9	8
INSTR	BUSY2	SS FLAG	DBC	RT FLAG	SRQ	BUSY1	BC/RT
7	6	5	4	3	2	1	0
LOCK	PARERR	RTAPAR	RTA4	RTA3	RTA2	RTA1	RTA0

#11 BUILT-IN-TEST START REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#12 PROGRAMMED RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#13 REMOTE TERMINAL TIMER RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

X= DON'T CARE

Table 1. BCRT Registers (continued from page 16)

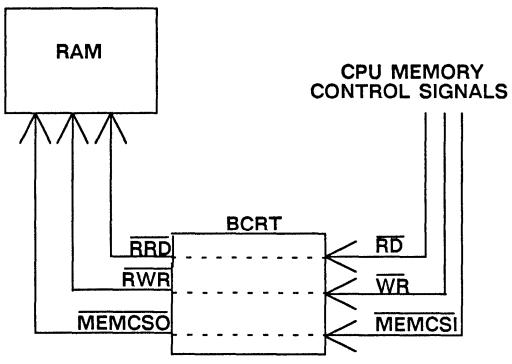


Figure 3a. Pseudo Dual-Port RAM Control Signals

4.0 System Overview

The BCRT can be configured for a variety of processor and memory environments. The host processor and the BCRT communicate via a flexible, programmable interrupt structure, internal registers, and a user-definable shared memory area. The shared memory area (up to 64K) is completely user-programmable and communicates BCRT control information -- message data, and status/error information.

Built-in memory management functions designed specifically for MIL-STD-1553B applications aid processor off-loading. The host needs only to establish the parameters within memory so the BCRT can access this information as required. For example, in the RT mode, the BCRT can store data associated with individual subaddresses anywhere within its 64K address space. The BCRT then can automatically buffer up to 128 incoming messages of the same subaddress, thus preventing the previous messages

from being overwritten by subsequent messages. This buffering also extends the intervals required by the host processor to service the data. Selecting an appropriate MCLK frequency to meet system memory access time requirements controls the memory access rate. The completion of a user-defined task or the occurrence of a user-selected event is indicated by using the extensive set of interrupts provided.

In the BC mode, the BCRT can process multiple messages, assist in scheduling message lists, and provide host-programmable functions such as auto retry. The BCRT is incorporated in systems with a variety of interrupt latencies by using the Interrupt History List feature (see Exception Handling and Interrupt Logging, page 33). The Interrupt History List sequentially stores the events that caused the interrupt in memory without losing information if a host processor does not respond immediately to an interrupt.

5.0 System Interface

5.1 DMA Transfers

The BCRT initiates DMA transfers whenever it executes command blocks (BC mode) or services commands (RT mode). $\overline{\text{DMAR}}$ initiates the transfer and is terminated by the inactive edge of $\overline{\text{DMACK}}$. The Address Enable (AEN) input enables the BCRT to output an address onto the Address bus.

The BCRT requests transfer cycles by asserting the $\overline{\text{DMAR}}$ output, and initiates them when a $\overline{\text{DMAG}}$ input is received. A $\overline{\text{DMACK}}$ output indicates that the BCRT has control of the Data and Address buses. The $\overline{\text{TSCTL}}$ output is asserted when the BCRT is actually asserting the Address and Data buses.

To support using multiple bus masters in a system, the BCRT outputs the $\overline{\text{DMAGO}}$ signal that results from the $\overline{\text{DMAG}}$ signal passing through the chip when a BCRT bus request was not generated ($\overline{\text{DMAR}}$ inactive). You can use $\overline{\text{DMAGO}}$ in daisy-chained multimaster systems.

5.2 Hardware Interface

The BCRT provides a simple subsystem interface and facilitates DMA arbitration. The user can configure the BCRT to operate in a variety of memory-processor environments including the pseudo-dual-port RAM and standard DMA configurations.

For complete circuit description, such as arbitration logic and I/O, please refer to the appropriate application note.

5.3 CPU Interconnection

Pseudo-Dual-Port RAM Configuration

The BCRT's Address and Data buses connect directly to RAM, with buffers isolating the BCRT's buses from those of the host CPU (figures 3a and 3b). The CPU's memory control signals ($\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{MEMCSI}}$) pass through the BCRT and connect to memory as $\overline{\text{RRD}}$, $\overline{\text{RWR}}$ and $\overline{\text{MEMCSO}}$.

Standard DMA Configuration

The BCRT's and CPU's data, address, and control signals are connected to each other as shown in figures 3c and 3d. The $\overline{\text{RWR}}$, $\overline{\text{RRD}}$, and $\overline{\text{MEMCSO}}$ are activated after $\overline{\text{DMAG}}$ is asserted.

In either case, the BCRT's Address and Data buses remain in a high-impedance state unless the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are active, indicating a host register access; or $\overline{\text{TSCTL}}$ is asserted, indicating a memory access by the BCRT. CPU attempts to access BCRT registers are ignored during BCRT memory access. Inhibit DMA transfers by using the Busy function in the Remote Terminal Address Register while operating in the Remote Terminal mode.

The designer can use $\overline{\text{TSCTL}}$ to indicate when the BCRT is accessing memory. AEN is also available (use is optional), giving the CPU control over the BCRT's Address bus. A DMA Burst (BURST) signal indicates multiple DMA accesses.

Register Access

Registers 0 through 13 are accessed with the decode of the four LSBs of the Address bus (A0-A3) and asserting $\overline{\text{CS}}$. Pulse either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ for multiple register accesses.

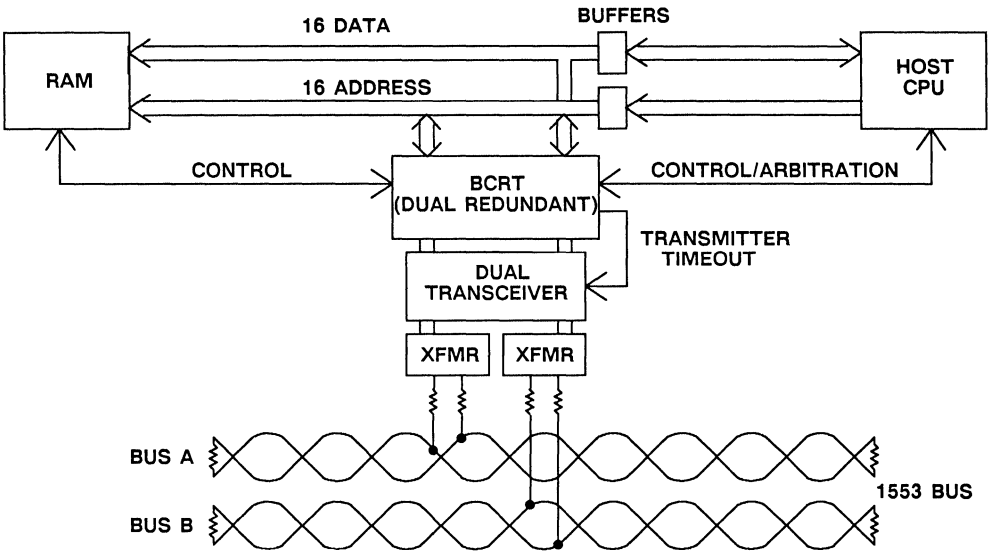


Figure 3b. CPU/BCRT Interface -- Pseudo-Dual-Post RAM Configuration

5.4 RAM Interface

The BCRT's $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ signals serve as read and write controls during BCRT memory accesses. The host subsystem signals $\overline{RD}$, $\overline{WR}$, and $\overline{MEMCSI}$ propagate through the BCRT to become $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ outputs to support a pseudo-dual-port. During BCRT-RAM data transfers, the host subsystem's memory signals are ignored until the BCRT access is complete.

5.5 Transmitter/Receiver Interface

The BCRT's Manchester II encoder/decoder interfaces directly with the 1553 bus transceiver, using the TAO-TAZ and RAZ-RAO signals for Channel A, and TBO-TBZ and RBZ-RBO signals for Channel B.

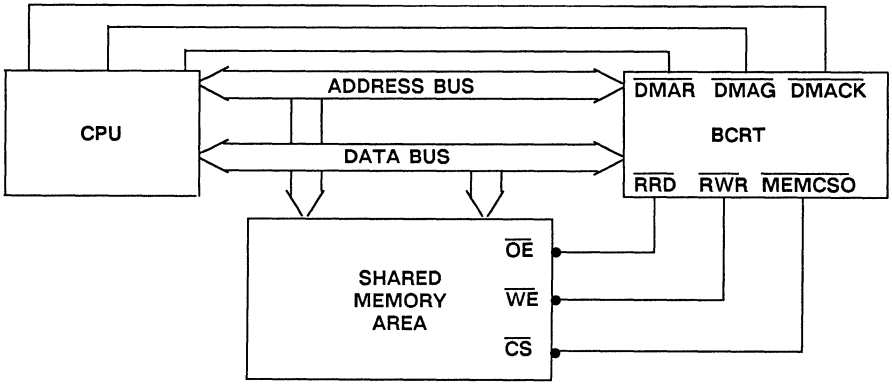


Figure 3c. DMA Signals

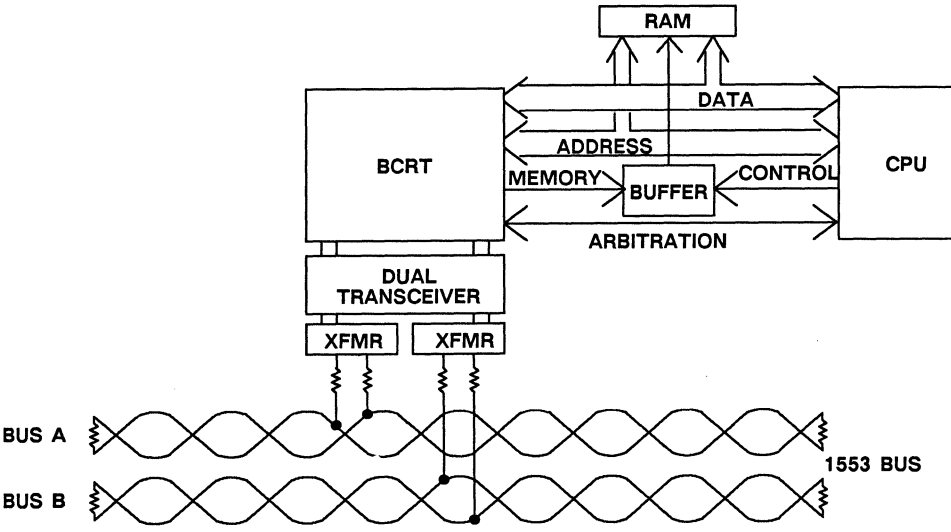


Figure 3d. CPU/BCRT Interface -- DMA Configuration

The BCRT also provides a $\overline{\text{TIMERON}}$ signal output and an active channel output indicator (CHA/$\overline{\text{B}}$) to assist in meeting the MIL-STD-1553B fail-safe timer requirements (see figure 4).

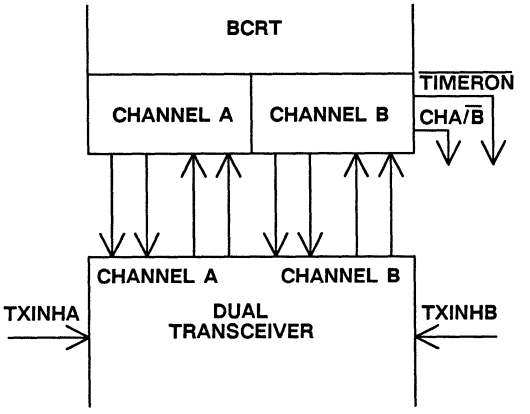


Figure 4. Dual-Channel Transceiver

6.0 Remote Terminal Architecture

The Remote Terminal architecture is a descriptor-based configuration of relevant parameters. It is composed of an RT Descriptor Space (see figure 5) and internal, host-programmable registers. The Descriptor Space contains only descriptors.

Descriptors contain programmable subaddress parameters relating to handling message transfers. Each descriptor consists of four words: (1) a Control Word, (2) a Message Status List Pointer, (3) a Data List Pointer, and (4) an unused fourth word (see figure 6.) These words indicate how to perform the data transfers associated with the designated subaddress.

A receive descriptor and a transmit descriptor are associated with each subaddress. The descriptors reside in memory and are listed sequentially by subaddress. By using the index within the descriptor, the BCRT can buffer incoming and outgoing messages, which reduces host CPU overhead. This message buffering also reduces the risk of incoming messages being overwritten by subsequent incoming messages.

Each descriptor contains a programmable interrupt structure for subsystem notification of user-selected message transfers and indicates when the message buffers are full. Illegalizing subaddresses, in normal and broadcast modes, is accomplished by using programmable bits within the descriptor (see the RT Functional Operation section on next page).

Message Status information -- including word count, an internally generated time tag, and broadcast and message validity information -- is provided for each message. The Message Status Words are stored in a separate Message Status Word list according to subaddress. The list's starting locations are programmable within the descriptor.

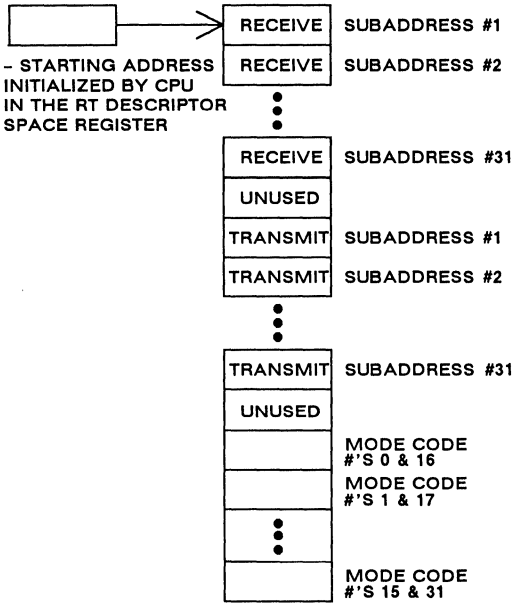


Figure 5. Descriptor Space

Message data, received or transmitted, is also stored in lists. The message capacity of the lists and the lists' locations are user selectable within the descriptor.

6.1 RT Functional Operation

The RT off-loads the host computer of all routine data transfers involved with message transfers over the 1553B bus by providing a wide range of user-programmable functions. These functions make the BCRT's operation flexible for a variety of applications. The following paragraphs give each function's operational descriptions.

6.1.1 RT Subaddress Descriptor Definition

The host sets words within the descriptor. The BCRT then reads the descriptor words when servicing a command corresponding to the specified descriptor. All bit-selectable functions are active high and inhibited when low.

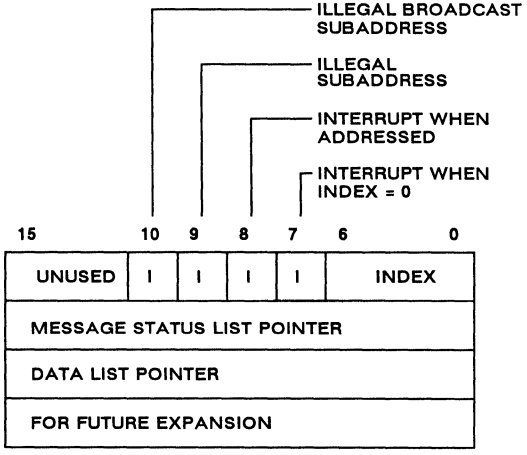


Figure 6. Remote Terminal Subaddress Descriptor

A. Control Word. The first word in the descriptor, the Control Word, selects or disables message transfers and selects an index.

Bit Number	Description
BITs 15-11	Reserved.
BIT 10	Illegal Broadcast Subaddress. Indicates to the BCRT not to access this subaddress using broadcast commands. The Message Error bit in the status word is set if the illegal broadcast subaddress is addressed. Since transmit commands do not apply to broadcast, this bit applies only to receive commands.
BIT 9	Illegal Subaddress. Set by the host CPU, it indicates to the BCRT that a command with this subaddress is illegal. If a command uses an illegal subaddress the Message Error bit in the 1553 status word is set. The Illegal Command Interrupt is also asserted if enabled.
BIT 8	Interrupt Upon Valid Command Received. Indicates that the BCRT is to assert an interrupt every time a command addresses this descriptor. The interrupt occurs just prior to post-command descriptor updating.
BIT 7	Interrupt When Index = 0. Indicates that the BCRT initiates an interrupt when the index is decremented to zero.
BITs 6-0	Index. These bits are for indexed message buffering. Indexing means transacting a pre-specified number of messages before notifying the host CPU. After each message transaction, the BCRT decrements the index by one until index = 0. Note that the index is decremented for messages that contain message errors.

B. Message Status List Pointer. The host sets the Message Status List Pointer, the second word within the descriptor, and the BCRT uses it as a starting address for the Message Status List. It is incremented by one with each Message status word write. If the Control Word Index is already equal to zero, the Message Status List Pointer is not incremented and the previous Message status word is overwritten.
Note: A Message Status Word is also written and the pointer is incremented when the BCRT detects a message error.

C. Data List Pointer. The Data List Pointer is the third word within the descriptor. The BCRT stores data in RAM beginning at the address indicated by the Data List Pointer. The Data List Pointer is updated at the end of each successful message with the next message's starting address with the following exceptions:

- If the message is erroneous, the Data List Pointer is not updated. The next message overwrites any data corresponding to the erroneous message.
- Upon receiving a message, if the index is already equal to zero, the Data List Pointer is not incremented and data from the previous message is overwritten.

D. Reserved. The fourth descriptor word is reserved for future use.

6.1.2 Message Status Word

Each message the BCRT transacts has a corresponding Message Status Word, which is pointed to by the Message Status List Pointer of the Descriptor. This word allows the host CPU to evaluate the message's validity, determine the word count, and calculate the approximate time frame in which the message was transacted (figures 7 and 8).

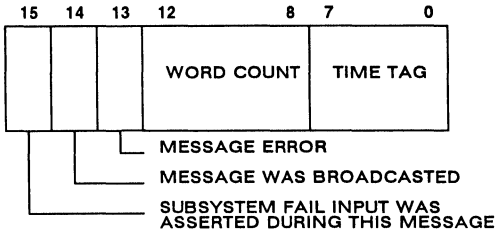


Figure 7. Message Status Word

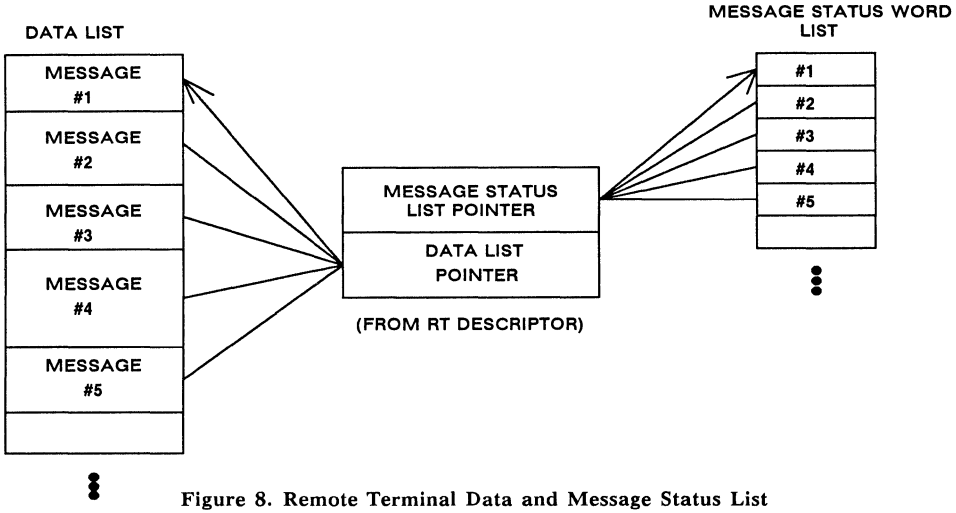


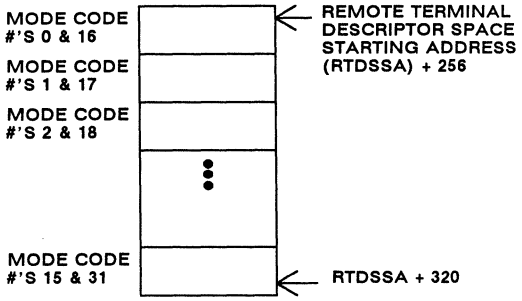
Figure 8. Remote Terminal Data and Message Status List

Message Status Word Definition

Bit Number	Description
BIT 15	Subsystem Failed. Indicates SSYSF was asserted before the Message Status Word transfer to memory. This bit is also set when the user sets bit 13 of Register 10.
BIT 14	Broadcast Message. Indicates that the corresponding message was received in the broadcast mode.
BIT 13	Message Error. Indicates a message is invalid due to improper synchronization, bit count, word count, Manchester error.
BITs 12-8	Word Count. Indicates the number of words in the message and reflects the Word Count field in the command word. Should the message contain a different number of words than the Word Count field, the Message Error flag is triggered. If there are too many words, they are withheld from RAM. If the actual word count is less than or grater than it should be, the Message Error bit in the 1553 status word is set.
BITs 7-0	Time Tag. The BCRT writes the internally generated Time Tag to this location after message completion. The resolution is 64 microseconds. (See Register 13). If the timer reads 2, it indicates the message was completed 128 to 191 microseconds after the timer started.

6.1.3 Mode Code Descriptor Definition

Mode codes are handled similarly to subaddress transactions. Both use the four-word descriptors residing in the RT descriptor space to allow the host to program their operational mode. Corresponding to each mode code is a descriptor (see figure 9a). Of the 32 address combinations for mode codes in MIL-STD-1553B, some are clearly defined functions while others are reserved for future use. Sixteen descriptors are used for mode code operations with each descriptor handling two mode codes: one mode code with an associated data word and one mode code without an associated data word. All mode codes are handled in accordance with MIL-STD-1553B. The function of the first word of the Mode Code Descriptor is similar to that of the Subaddress Descriptor and is defined below. The remaining three words serve the same purpose as in the Subaddress Descriptor.



Note:
Mode code descriptor blocks are also provided for reserved mode codes but have no associated predefined BCRTM operation.

Figure 9a. (RT) Mode Code Descriptor Space

Control Word

Bit Number	Description
BIT 15	Interrupt on Reception of Mode Code (without Data Word).
BIT 14	Illegalize Broadcast Mode Code (without Data Word).
BIT 13	Illegalize Mode Code (without Data Word).
BIT 12	Reserved.
BIT 11	Illegalize Broadcast Mode Code (with Data Word).
BIT 10	Illegalize Transmit Mode Code (with Data Word).
BIT 9	Illegalize Receive Mode Code (with Data Word).
BIT 8	Interrupt on Reception of Mode Code (with Data Word).
BIT 7	Interrupt if Index = 0.
BITs 6-0	Index. Functionally equivalent to the index described in the Subaddress Descriptor. It applies to mode codes with data words only.

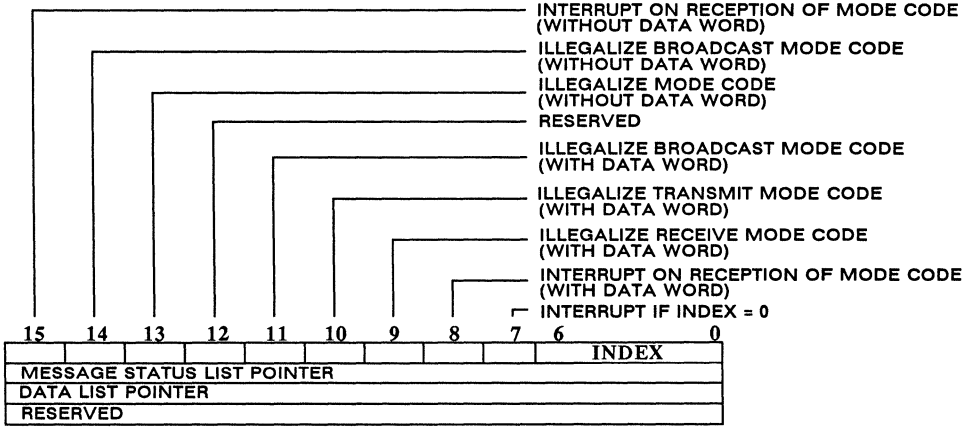


Figure 9b. (RT) Mode Code Descriptor

The descriptors, numbered sequentially from 0 to 15, correspond to mode codes 0 to 15 without data words and mode codes 16 to 31 with data words. For example, mode codes 0 and 16 correspond to descriptor 0 and mode codes 1 and 17 correspond to descriptor 1. The Mode Code Descriptor Space is appended to the Subaddress Descriptor Space starting at 0100H (256D) of the 320-word RT Descriptor Space (see figure 5).

The BCRT autonomously supports all mode codes without data words by executing the specific function and transmitting the 1553 status word. The subsystem provides the data word for mode codes with data words (see the Data List Pointer section). For all mode codes, an interrupt can be asserted upon successful completion of the mode command by setting the appropriate bit in the control word (see figure 9b).

Dynamic Bus Control #00000
This mode code is accepted automatically if the Dynamic Bus Control Enable bit in the Remote Terminal Address Register is set. Setting the Dynamic Bus Control Acceptance bit in the 1553 status word and BCRT Status Register confirms the mode code acceptance. A High-Priority Interrupt is also asserted if enabled. If the Dynamic Bus Control Enable bit is not set, the BCRT does not accept Dynamic Bus Control.

Synchronize (Without Data Word) #00001
If enabled in the Mode Code #00001 Descriptor Control Word, the BCRT asserts an interrupt when this mode code is received.

Transmit Status Word #00010
The BCRT automatically transmits the 1553 status word corresponding to the last message transacted.

Initiate Self-Test #00011
The BCRT automatically starts its BIT routine. An interrupt, if enabled, is asserted when the test is completed. The BIT Word Register and external pin BCRTF are updated when the test is completed. A failure in BIT will also set the TF status word bit.

Transmitter Shutdown #00100
The BCRT disables the channel opposite the channel on which the command was received.

Override Transmitter Shutdown #00101
The BCRT enables the channel previously disabled.

Inhibit Terminal Flag Bit #00110
The BCRT inhibits the Terminal Flag from being set in the status word.

Override Inhibit Terminal Flag Bit #00111
The BCRT disables the Terminal Flag inhibit.

Reset Remote Terminal #01000
The BCRT automatically resets the encoder, decoders, and protocol logic.

Transmit Vector Word #10000
The BCRT transmits the vector word from the location addressed by the Data List Pointer in the Mode Code Descriptor Block.

Synchronize (with Data Word) #10001
On receiving this mode code, the BCRT simply stores the associated data word.

Transmit Last Command #10010
The BCRT transmits the last command executed and the corresponding 1553 status word.

Transmit BIT Word #10011
The BCRT transmits BIT information from the BIT Register.

Selected Transmitter Shutdown #10100
On receiving this mode code, the BCRT simply stores the associated data word.

Override Selected Transmitter Shutdown #10101
On receiving this mode code, the BCRT simply stores the associated data word.

Mode codes 9-15 and 22-31 are reserved for future expansion of MIL-STD-1553B.

6.2 RT Error Detection

In accordance with MIL-STD-1553B, the remote terminal handles superseding commands on the same or opposite bus. When receiving, the remote terminal performs a response time-out function of 56 microseconds for RT-RT transfers. If the response time-out condition occurs, a Message Error bit is set in the 1553 status word and in the Message Status Word. Error checking occurs on both of the Manchester logic and the word formats. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

6.3 RT Operational Sequence

The following is a general description of the typical behavior of the BCRT as it processes a message in the RT mode. It is assumed that the user has already written a "1" to Register 0, bit 0, enabling RT operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active

- DMA Descriptor Read. After receiving a valid command, the BCRT initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read
  Message Status List Pointer read
  Data List Pointer read

Data Transmitted/Received.

- Data Word DMA.

  If the BCRT needs to transmit data from memory, it initiates a DMA cycle for each Data Word shortly before the Data Word is needed on the 1553B bus:

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

  If the BCRT receives data, it writes each Data Word to memory after the Data Word is received:

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Status Word Transmission.

The BCRT automatically transmits the Status Word as defined in MIL-STD-1553B. The Message Error and Broadcast Command Received bits are generated internally. Writing to Register 10 enables the other predefined bits. For illegalized commands, the BCRT sets the Message Error Bit in the 1553 Status Word.

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRT is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
RT Descriptor Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

- Descriptor Write.

  After the BCRT processes the message, a final DMA burst occurs to update the descriptor block, if necessary:

  DMA arbitration (BURST)
  Message Status Word write
  Data List Pointer write
  (incremented by word count)
  Message Status List Pointer write
  (incremented by 1)
  Control Word write (index decremented)

  Note the following exceptions:

  Mode codes without data require no descriptor update.

  Predefined mode codes (18 and 19) which do not require access to memory for the data word, do not involve updating the Data List Pointer.

  Messages with errors prevent updates to the Data List Pointer.

  If the message index was zero, neither the Message Status List Pointer nor the Data List Pointer is updated.

7.0 Bus Controller Architecture

The BCRT's bus controller architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553B bus has an associated Command Block, which the CPU sets up (see figures 10 and 11). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts. This memory interface system is flexible due to a doubly-linked list data structure.

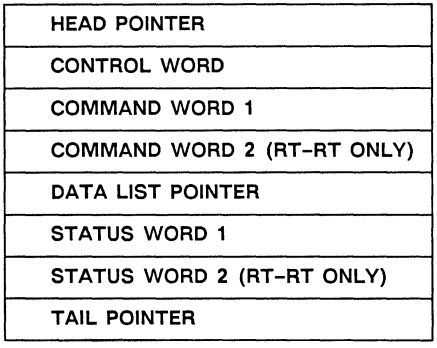


Figure 10. Command Block

In a doubly-linked Command Block structure, pointers delimit each Command Block to the previous and successive blocks (see figure 12). The linking feature eases multiple message processing tasks and supports message scheduling because of its ability to loop through a series of transfers at a predetermined cycle time. A data pointer in the command allows efficient space allocation because data blocks only have to be configured to the exact word count used in the message. Data pointers also provide flexibility in data-bank switching.

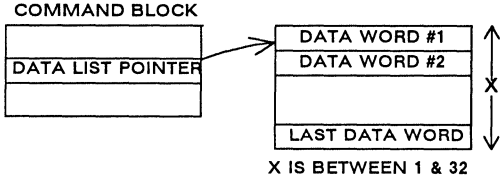


Figure 11. Data Placement

A control word with bit-programmable functions and a Message Error bit are in each Command Block. This allows selecting individual functions for each message and provides message validity information. The BCRT's register set provides additional global parameters and address pointers.

A programmable auto retry function is selectable from the control word and Control Register.

The auto retry can be activated when any of the following occurs:

- Busy bit set in the status word
- Message Error (indicated by the RT status response)
- Response Time-Out
- Message Error detected by the Bus Controller

One to four retries are programmable on the same or opposite bus.

The Bus Controller also has a programmable intermessage delay timer that facilitates message transfer scheduling (see figures 13 and 14). This timer, programmed in the control word, automatically delays between the start of two successive commands.

A polling function is also provided. The Bus Controller, when programmed, compares incoming status words to a host-specified status word and generates an interrupt if the comparison indicates any matching bits. An Interrupt and Continue function facilitates the host subsystem's synchronization by generating an interrupt when the specified Command Block's message is executed.

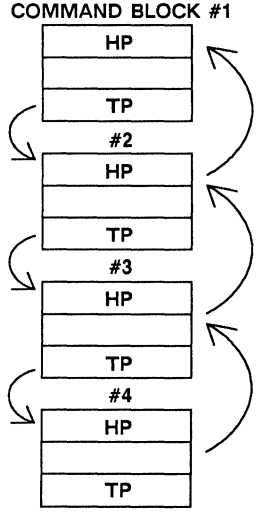


Figure 12. Command Block Chaining

7.1 BC Functional Operation

The Bus Controller off-loads the host computer of many functions needed to coordinate 1553B bus data transfers. Special architectural features provide message-by-message flexibility. In addition, a programmable interrupt scheme, programmable intermessage timing delays, and internal registers enhance the BCRT's operation.

The host determines the first Command Block by setting the initial starting address in the current Command Block Register. Once set, the BCRT updates the current Command Block register with the next Command Block Address. The BCRT then executes the sequential Command Blocks and counts out message delays (where programmed) until it encounters the last Command Block listed (indicated by the End of List bit in the control word). Interrupts are asserted when enabled events occur (see the Exception Handling and Interrupt Logging section, page 33).

The functions and their programming instructions are described below. The registers also contain many programmable functions and function parameters.

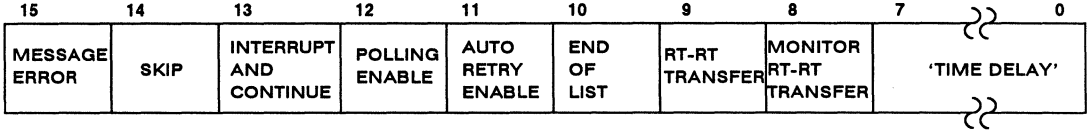


Figure 13. Control Word

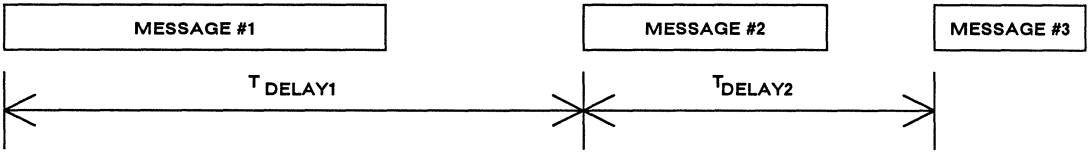


Figure 14. BC Timing Delays

BC Command Block Definition
Each Command Block contains (see figure 10):

A. Head Pointer. Host-written, this location can contain the address of the previous Command Block's Head Pointer. The BCRT does not access this location.

B. Control Word. Host-written, the Control Word contains bit-selectable options and a Message Error bit the BCRT provides (see figure 13). The bit definitions follow.

Bit Number	Description
BIT 15	Message Error. The BCRT sets this bit when it detects an invalid RT response as defined in MIL-STD-1553B.
BIT 14	Skip. When set, this bit instructs the BCRT to skip this Command Block and execute the next.
BIT 13	Interrupt and Continue. If set, a Standard Interrupt is asserted when this block is addressed; operation, however, continues. Note that this interrupt must also be enabled by setting bit 0 of Register 9.
BIT 12	Polling Enable. Enables the BCRT's polling operation.
BIT 11	Auto Retry Enable. When set, the Auto Retry function, governed by the global parameters in the Control Register, is enabled for this message.
BIT 10	End of List. Set by the CPU, this bit indicates that the BCRTP, upon completion of the current message, will halt and assert a High-Priority Interrupt. The interrupt must also be enabled in the High-Priority Interrupt Enable Register.
BIT 9	RT-RT. Set by the CPU, this indicates that this Command Block transacts an RT-RT transfer.
BIT 8	Monitor RT-RT Transfer. Set by the CPU, this function indicates that the BCRT should receive and store the message beginning at the location indicated by the data pointer.
BITs 7-0	Time Delay. The CPU sets this field, which causes the BCRT to delay the specified time between sequential message starts (see figures 13 and 14). Regardless of the value in the Time Delay field (including zero), the BCRT will at least meet the minimum 4 μs intermessage gap time as specified in MIL-STD-1553B. The timer is enabled by having a non-zero value in this bit field. When using this function, please note: • Timer resolution is 16 microseconds. As an example, if a given message requires 116 us to complete (including the minimum 4 us intermessage gap time) the value in the Time Delay field must be at least 00001000 (8 x 16 μs = 128 μs) to provide an intermessage gap greater than the 4 μs minimum requirement. • If the timer is enabled and the Skip bit is set, the timer provides the programmed delay before proceeding. • If the message duration exceeds the timer delay, the message is completed just as if the timer were not enabled. • If SKIP = 1 and EOL = 1, the $\overline{\text{HPINT}}$ is generated if enabled. • If SKIP = 1 and Interrupt and Continue = 1, the $\overline{\text{STDINT}}$ is generated if enabled.

C. Command Word One. Initialized by the CPU, this location contains the first command word corresponding to the Command Block's message transfer.

D. Command Word Two. Initialized by the CPU, this location is for the second (transmit) command word in RT-RT transfers. In messages involving only one RT, the location is unused.

E. Data Pointer. Initialized by the CPU, this location contains the starting location in RAM for the Command Block's message (see figure 15).

F. Status Word One. Stored by the BCRT, this location contains the entire Remote Terminal status response.

G. Status Word Two. Stored by the BCRT, this location contains the receiving Remote Terminal status word. For transfers involving one Remote Terminal, the location is unused.

H. Tail Pointer. Initialized by the host CPU, the Tail Pointer contains the next Command Block's starting address.

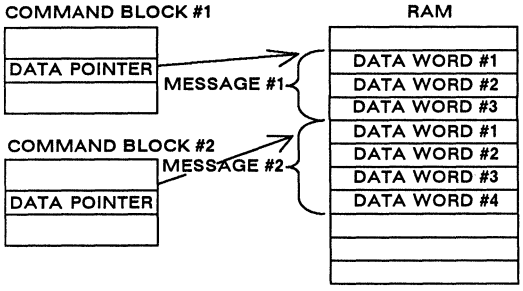


Figure 15. Contiguous Data Storage

7.2 Polling

During a typical polling scenario (see figure 16) the Bus Controller interrogates remote terminals by requesting them to transmit their status words. This feature can also alert the host if a bit is set in any RT status word response during normal message transactions. The BCRT enables the host to initialize a chain of Command Blocks with the command word's Polling Enable bit. A programmable Polling Compare Register (PCR) is provided. In the polling mode, the Remote Terminal response is compared to the Polling Compare Register contents. Program the PCR by setting the PCR bits corresponding to the RT's 1553 status word bits to be compared. If they match (i.e., two 1's in the same bit position) then, if enabled in both the BC Command Block Control Word and in the Standard Interrupt Enable Register (Register 9), a polling comparison interrupt is generated.

Example 1. No bit match is present

PCR	00000000001
RT's 1553 Status Word response	00000100010
Result	No Polling Comparison Interrupt

Example 2. Bit match is present

PCR	00100100000
RT's 1553 Status Word response	00000100000
Result	Polling Comparison Interrupt

7.3 BC Error Detection

The Bus Controller checks for errors (see the Exception Handling and Interrupt Logging and the RT Error Detection sections, pages 33 and 26) on each message transaction. In addition, the BC compares the RT command word addresses to the incoming status word addresses. The BC monitors for response time-out and checks data and control words for proper format according to MIL-STD-1553B. Illogical commands include incorrectly formatted RT-RT Command Blocks.

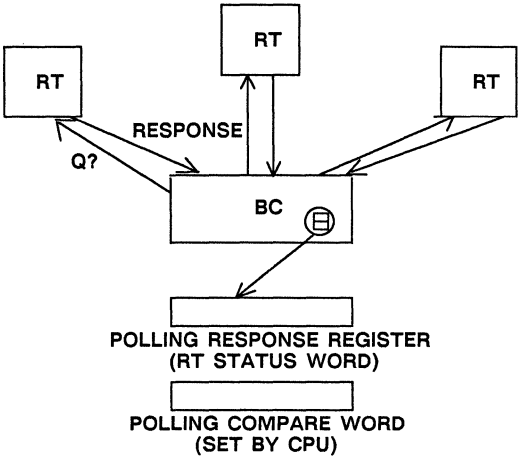


Figure 16. Polling Operation

7.4 Bus Controller Operational Sequence

The following is a general description of the typical behavior of the BCRT as it processes a message in the BC mode.

The user starts BC operation by writing a "1" to Register 0, Bit 0.

- Command Block DMA - the following occurs immediately after Bus Controller startup:

  DMA arbitration (BURST)
  Control Word read
  Command Word 1 read (from third location of Command Block)
  Data List Pointer read

A. For BC-to-RT Command Blocks:

The BCRT transmits the Command Word.

- Data Word DMA

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

The BCRT transmits the Data Word. Data Word DMAs and transmissions continue until all Data Words are transmitted.

- Status Word DMA

The BCRT receives the RT Status Word.

DMA arbitration
Status Word write (to sixth location of Command Block)

B. For RT-to-BC Command Blocks:

The BCRT transmits the Command Word.

- Status Word DMA

The BCRT receives the RT Status Word.

DMA arbitration
Status Word write (to sixth location of Command Block)

The BCRT receives the first Data Word.

- Data Word DMA

DMA arbitration
Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

C. For RT(B)-to-RT(A) Command Blocks:

The BCRT transmits Command Word 1 to RT(B).

- Command Word 2 DMA

DMA arbitration
Command Word 2 read (from fourth location of Command Block)

The BCRT transmits Command Word 2 to RT(A).

The BCRT receives the RT Status Word from RT(A).

- Status Word DMA for RT(A) Status Word

DMA arbitration
Status Word write (to sixth location of Command Block)

The BCRT receives the first Data Word

- Data Word DMA (only if the BCRT is enabled to monitor the RT-to-RT message).

DMA arbitration
Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

The BCRT receives the RT Status Word from RT(B).

- Status Word DMA for RT(B) Status Word

DMA arbitration
Status Word write (to seventh location of Command Block)

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRT is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
Command Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

If Retries are enabled and a Retry condition occurs, the following DMA occurs:

DMA arbitration (BURST)
Control Word read
Command Word 1 read (from third location of Command Block)
Data List Pointer read

The BCRT proceeds from the current Command Block to the next successive Command Block.

- If no Message Error has occurred during the current Command Block, the following occurs:

DMA arbitration (BURST)
Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
DMA hold cycle
Control Word read (next Command Block)
Command Word 1 read (next Command Block)
Data List Pointer read

- If the BCRT detects a Message Error while processing the current Command Block, the following occurs:

DMA arbitration (BURST)
Control Word write
Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
DMA hold cycle
Control Word read (next Command Block)
Command Word 1 read (next Command Block)
Data List Pointer read

The BCRT proceeds again from point A, B, or C as shown above.

7.5 BC Operational Example (see figure 18 on page 35)

The BCRT is programmed initially to accomplish the following:

The first Command Block is for a four-word RT-RT transfer with the BCRT monitoring the transfer and storing the data.

- Auto-retry is enabled on the opposite bus using only one retry attempt, if the incoming Status Word is received with the Message Error bit set.
- Wait for a time delay of 400 microseconds before proceeding to the next Command Block.
- The Data List Pointer contains the address 0400H.

The second Command Block is for a BC-RT transfer of two words.

- The End of List bit is set in its Control Word.
- The Data List Pointer contains the address 0404H.
- The Polling Enable bit is set and the Polling Compare Register contains a one in the Subsystem Fail position (bit 2).

Then:

A. The CPU initializes all the appropriate registers and Command Blocks, and issues a Start Enable by writing a "1" to Register 0, bit 0.

B. The BCRT, through executing a DMA cycle, reads the control word, command words, and the Data List Pointer. The delay timer starts and message execution begins by transmitting the receive and transmit commands stored in the Command Blocks. The BCRT then waits to receive the status word back from the transmitting RT.

C. The BCRT receives the RT status word with all status bits low from the transmitting RT and stores the status word in Command Block 1. The incoming data words from the transmitting RT follow. The BCRT stores them in memory locations 0400H - 0403H.

   If the status word indicates that the message cannot be transmitted (Message Error), the response time-out clock counts to zero and the allotted message time runs out. An auto-retry can be initiated if programmed to do so. Nevertheless, the ME bit in the control word is set.

D. The BCRT receives the status word response from the receiving RT. The ME bit in the status word is set, indicating the message is invalid. The BCRT initiates the auto retry function, (as programmed) on the alternate bus, re-transmits the command words, receives the correct status word, and stores the data again in locations 0400H - 0403H. This time the status word response from the receiving RT indicates the message transfer is successful.

E. The timer delay between the two successive transactions counts down another 135 microseconds before proceeding. This is determined as follows:

   The message transaction time is approximately 130 microseconds (the only approximation is due to the range in status response and intermessage gap times specified by MIL-STD-1553B). Approximating that with the retry, the total duration for the two attempts is 265 microseconds.

F. The BCRT reads the Tail Pointer of Command Block 1 and places it in the Current Command Register. It also reads the control word, command word, and Data List Pointer, and the first data word in the second Command Block.

G. Since this is a BC-RT transfer, the BCRT transmits the receive command followed by two data words from locations 0404H - 0405H in memory. The BCRT reads the second data word from memory while transmitting the first.

H. The BCRT receives the status response from the RT. In this case, the status word indicates, by the ME bit being low, that the message is valid. The status word also has the Subsystem Fail bit set.

I. The status word is stored in the Command Block. The BCRT, having encountered the end of the list, halts message transactions and waits for another start signal.

J. The BCRT asserts a High-Priority Interrupt indicating the end of the command list. Due to the polling comparison match, the BCRT also asserts a Standard Priority Interrupt and logs the event in the Interrupt Log List.

8.0 Exception Handling and Interrupt Logging

The exception handling scheme the BCRT uses is based on an interrupt structure and provides a high degree of flexibility in:

- defining the events that cause an interrupt,
- selecting between High-Priority and Standard interrupts, and
- selecting the amount of interrupt history retained.

The interrupt structure consists of internal registers that enable interrupt generation, control bits in the RT and BC data structures (see the Remote Terminal Descriptor Definition section, page 24, and the Bus Controller Command Block definition, page 27), and an Interrupt Log List that sequentially stores an interrupt events record in system memory.

The BCRT generates the Interrupt Log List (see figure 17) to allow the host CPU to view the Standard Interrupt occurrences in chronological order. Each Interrupt Log List entry contains three words. The first, the Interrupt Status Word, indicates the type of interrupt (entries are only for interrupts enabled). In the BC mode, the second word is a Command Block Pointer that refers to the corresponding Command Block. In the RT mode, the second word is a Descriptor Pointer that refers to the corresponding subaddress descriptor. The CPU-initialized third word, a Tail Pointer, is read by the BCRT to determine the next Interrupt Log List address. The list length can be as long or as short as required. The configuration of the Tail Pointers determines the list length.

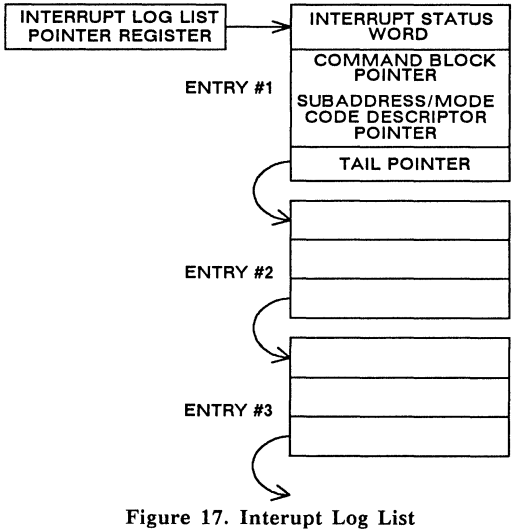


Figure 17. Interupt Log List

The host CPU initializes the list by setting the tail pointers. This gives flexibility in the list capacity and the ability to link the list around noncontiguous blocks of memory. The host CPU sets the list's starting address using the Interrupt Log List Register. The BCRT then updates this register with the address of the next list entry.

The internal High-Priority Interrupt Status/Reset Register indicates the cause of a High-Priority Interrupt. The High-Priority Interrupt signal is reset by writing a "1" to the set bits in this register.

The interrupt structure also uses three BCRT-driven output signals to indicate when an interrupt event occurs:

$\overline{\text{STDINTL}}$ Standard Interrupt Level. This signal is asserted when one or more of the events enabled in the Standard Interrupt Enable Register occurs. Clear the signal by resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register.

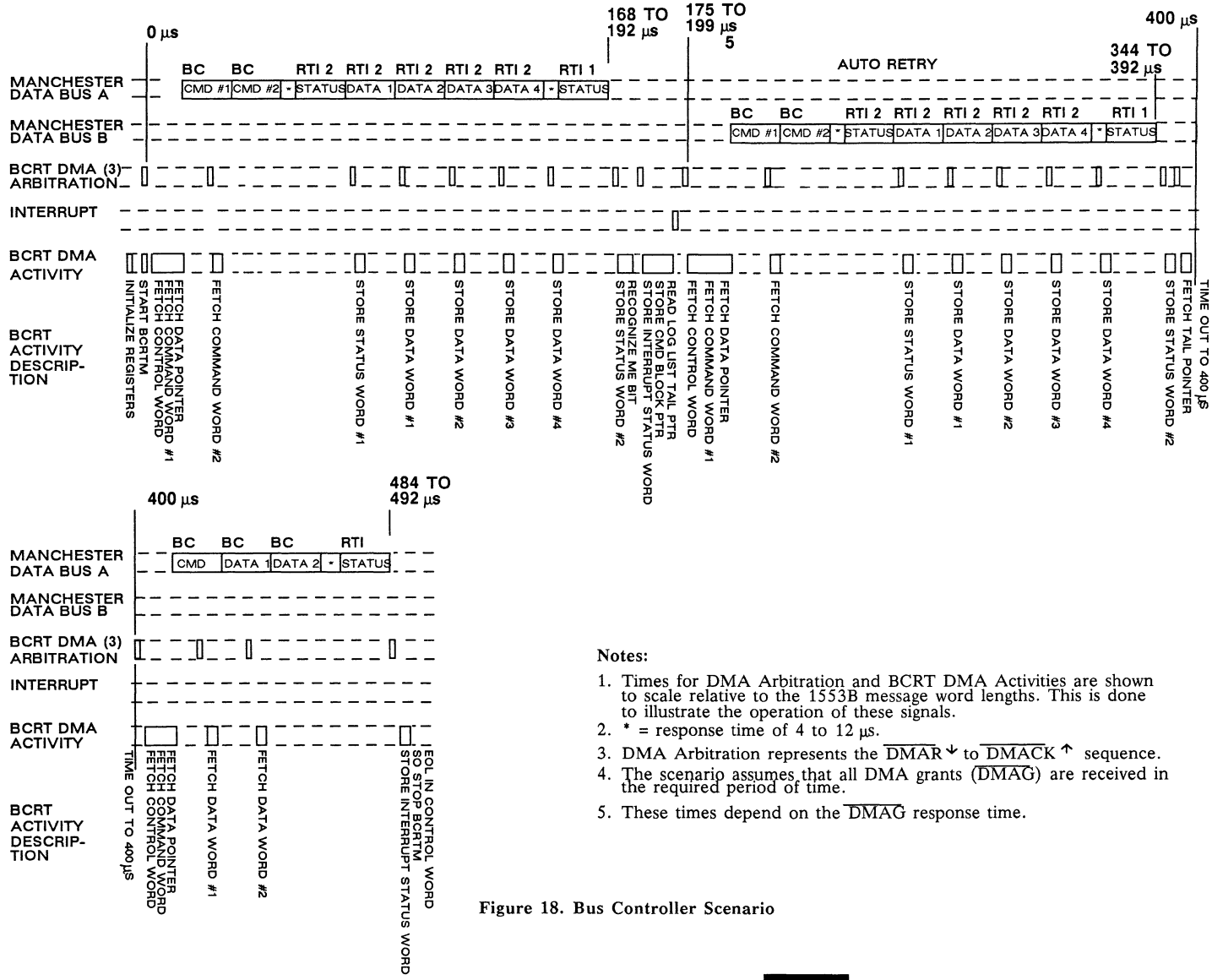
$\overline{\text{STDINTP}}$ Standard Interrupt Pulse. This signal is pulsed for each occurrence of an event enabled in the Standard Interrupt Enable Register.

$\overline{\text{HPINT}}$ High-Priority Interrupt. This signal is asserted for each occurrence of an event enabled in the High-Priority Interrupt/Enable Register. Writing to the corresponding bit in the High-Priority Status/Reset Register resets it.

Interrupt Status Word Definition

All bits in the Interrupt Status Word are active high and have the following functions:

Bit Number	Description
BIT 15	Interrupt Status Word Accessed. The BCRT always sets this bit during the DMA Write of the Interrupt Status Word. If the CPU resets this bit after reading the Interrupt Status Word, the bit can help the CPU determine which entries have been acknowledged.
BIT 14	No Response Time-Out (Message Error condition). Further defines the Message Error condition to indicate that a Response Time-Out condition has occurred.
BIT 13	(RT) Message Error (ME). Indicates the ME bit was set in the 1553 status word response.
BITs 12-8	Reserved.
BIT 7	(RT) Subaddress Event or Mode Code with Data Word Interrupt. Indicates a descriptor control word has been accessed with either an Interrupt Upon Valid Command Received bit set or an Interrupt when Index=0 bit set (and the Index is decremented to 0).
BIT 6	(RT) Mode Code without Data Word Interrupt. Indicates a mode code has occurred with an Interrupt When Addressed interrupt enabled.
BIT 5	(RT) Illegal Broadcast Command. Applies to receive commands only. This bit indicates that a received command, due to an illegal mode code or subaddress field, has been received in the broadcast mode. This does not include invalid commands.
BIT 4	(RT) Illegal Command. This indicates that an illegal command has occurred due to an illegal mode code or subaddress and T/R field. This does not include invalid commands.
BIT 3	(BC) Polling Comparison Match. Indicates a polling comparison interrupt.
BIT 2	(BC) Retry Fail. Indicates all the programmed retries have failed.
BIT 1	(BC,RT) Message Error. Indicates a Message Error has occurred.
BIT 0	(BC) Interrupt and Continue. This corresponds to the interrupt and continue function described in the Command Block.



Notes:

1. Times for DMA Arbitration and BCRT DMA Activities are shown to scale relative to the 1553B message word lengths. This is done to illustrate the operation of these signals.
2. * = response time of 4 to 12 µs.
3. DMA Arbitration represents the $\overline{\text{DMAR}}$ ↓ to $\overline{\text{DMACK}}$ ↑ sequence.
4. The scenario assumes that all DMA grants ($\overline{\text{DMAG}}$) are received in the required period of time.
5. These times depend on the $\overline{\text{DMAG}}$ response time.

Figure 18. Bus Controller Scenario

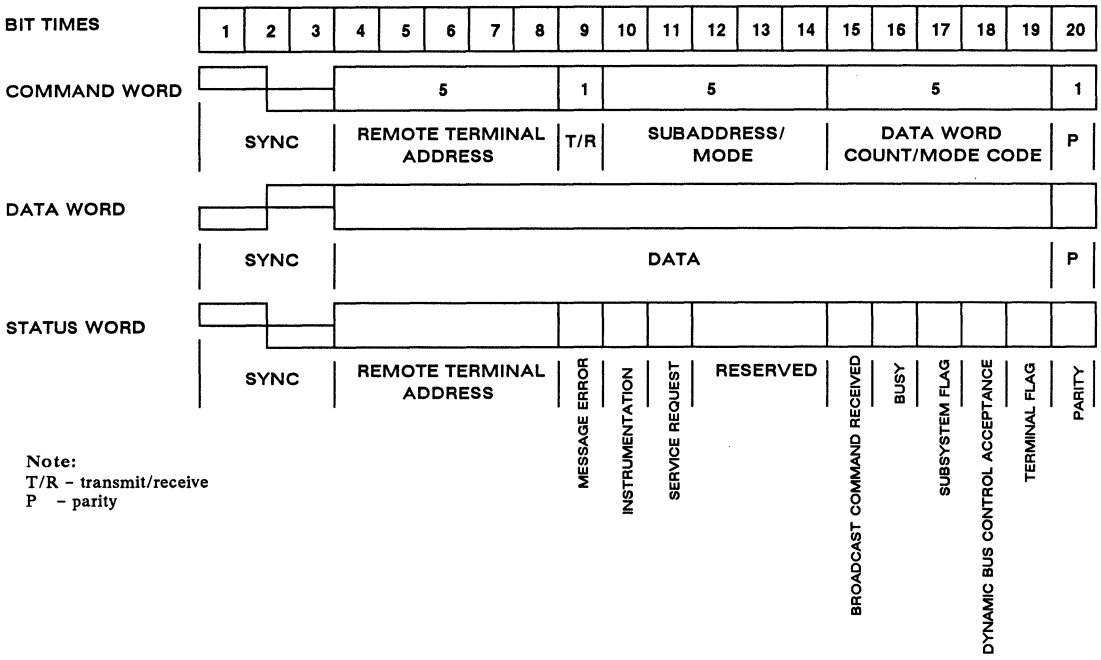


Figure 19. MIL-STD-1553B Word Formats

9.0 Operating Conditions*

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_{JMAX}	Maximum junction temperature	+175	°C
P_D	Average power dissipation (1)	300	mW
Θ_{JC}	Thermal resistance, junction-to-case	10	°C/W

Notes:
1. Does not reflect the added PD due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ±.01%	MHz

10.0 DC Electrical Characteristics

(V_{DD} - 5.0 V ± 10%; -55°C < T_C < + 125°C)

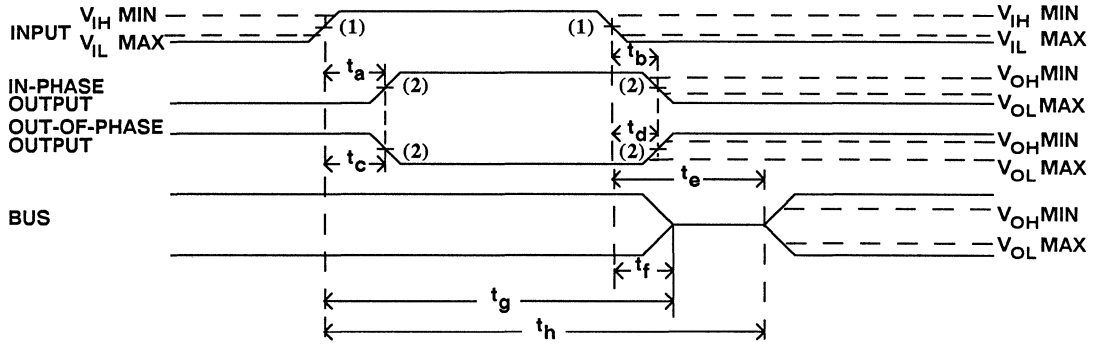
SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH} Non-RAD	High-level input voltage TTL inputs		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-up resistors Inputs with pull-up resistors	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	-1 -1 -550	1 1 -80	µA µA µA
V_{IH} RAD-HARD	High-level input voltage (6) TTL inputs (7) CMOS inputs		2.2 .7 V_{DD}		V V
I_{IN} RAD-HARD	Input leakage current TTL (7), CMOS inputs Inputs with pull-up resistors Inputs with pull-up resistors	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	-10 +150 -900	10 +900 -150	µA µA µA
V_{OL}	Low-level output voltage TTL outputs CMOS outputs	I_{OL} = 3.2 mA I_{OL} = 50 µA		0.4 V ss +.1	V V
V_{OH}	High-level output voltage TTL outputs CMOS outputs	I_{OH} = -400 µA I_{OH} = 50 µA	2.4 VDD -.1		V V
I_{OZ}	Three-state output leakage current TTL outputs	V_O = V_{DD} or V_{SS}	-10	10	µA
I_{OS}	Short-circuit output current (1,2)	V_{DD} = 5.5 V, V_O = V_{DD} V_{DD} = 5.5 V, V_O = 0 V	-100	100	mA mA
C_{IN}	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		20	pF
I_{DD}	Average operating current (1,4)	F = 12 MHz, C_L = 50 pF		50	mA
QI_{DD}	Quiescent current	See Note 5		3	mA

Notes:

1. Supplied as a design limit, but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes which may affect input/output capacitance.
4. Includes current through input pull-up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
5. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.
6. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) +20%, -0%; V_{IL} = V_{IL}(max) +0%, -50%, as specified herein, for TTL - compatible inputs. Devices may be tested using input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL} (max).
7. To 1 x 10^6 total dose; above this level CMOS I/Os required.

11.0 AC Electrical Characteristics

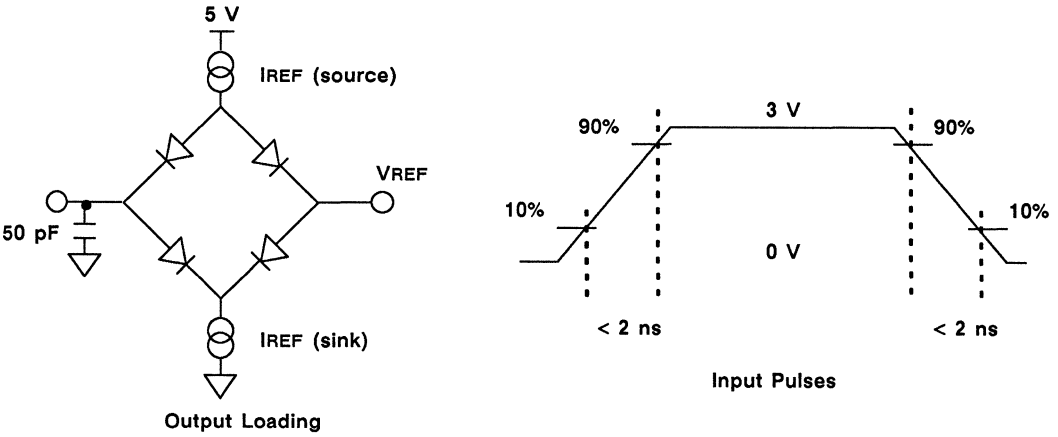
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

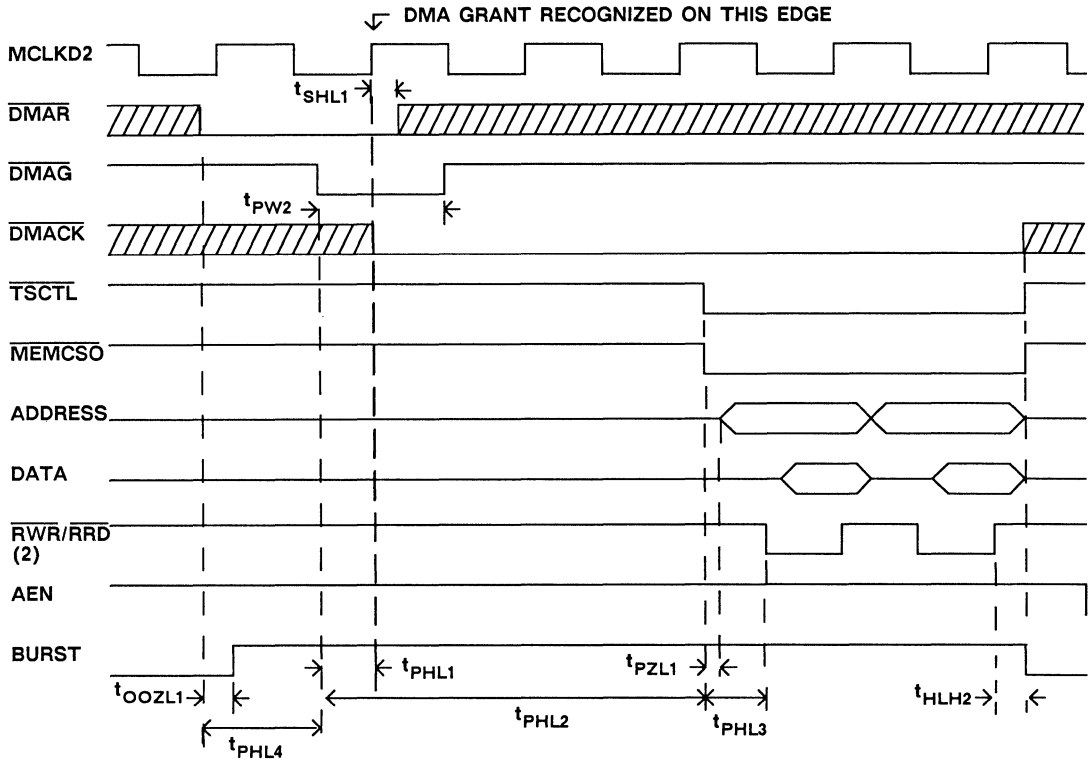
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 20. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

Figure 21. AC Test Loads and Input Waveforms

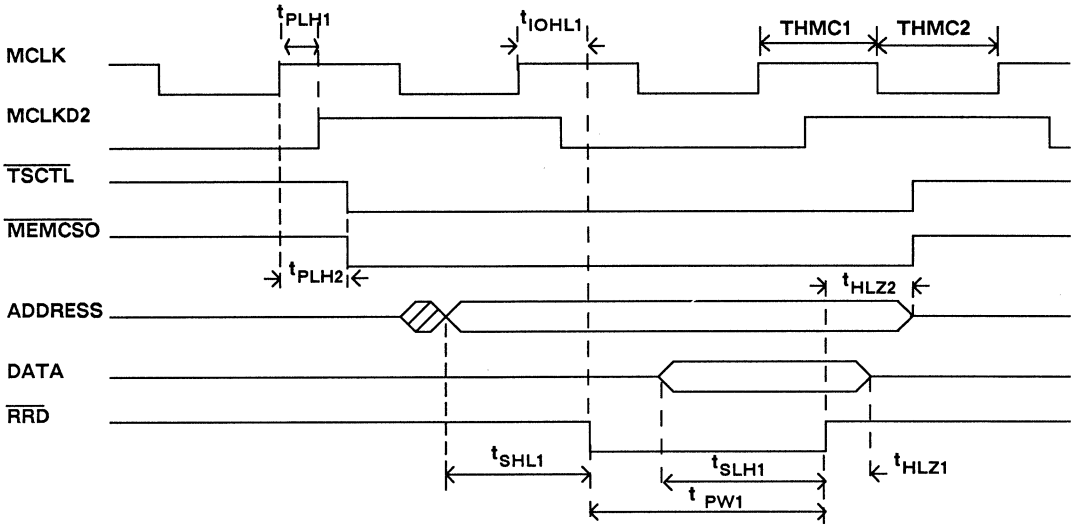


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	$\overline{DMACK}\downarrow$ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PHL1} (1)	$\overline{DMAG}\downarrow$ to $\overline{DMACK}\downarrow$ See note 3	0	45	ns
t_{PHL2}	$\overline{DMAG}\downarrow$ to $\overline{TSCTL}\downarrow$	2xMCLK	4xMCLK	ns
t_{PZL1}	$\overline{TSCTL}\downarrow$ to ADDRESS valid	0	40	ns
t_{HLH2}	$\overline{RWR/RRD}\uparrow$ to $\overline{DMACK}\uparrow$	THMC1-10	THMC1+10	ns
t_{PHL3}	$\overline{TSCTL}\downarrow$ to $\overline{RWR/RRD}\downarrow$	MCLK-20	MCLK+20	ns
t_{PW2}	$\overline{DMAG}\downarrow$ to $\overline{DMAG}\uparrow$	MCLK	6xMCLK	ns
t_{OOZL1}	$\overline{DMAR}\downarrow$ to BURST $\uparrow$	0	10	ns
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See note 4	0	3.5 (1.9)	µs
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See note 5	0	1.9 (0.8)	µs

Notes:
1. Guaranteed by test.
2. See figure 23 & 24 for detailed DMA read and write timing.
3. $\overline{DMAG}$ must be asserted at least 45 ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If $\overline{DMAG}$ is not asserted at least 45 ns prior to the rising edge of MCLKD2, $\overline{DMAG}$ is not recognized until the following MCLKD2 cycle.
4. Provided MCLK = 12 MHz. Number in parentheses indicates the longest $\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.
5. Provided MCLK = 6 MHz. Number in parentheses indicates the longest $\overline{DMAR}\downarrow$ $\overline{DMAG}\downarrow$ allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.

MCLK = period of thememory clock cycle.
BURST signal is for multiple-word DMA accesses.
THMC1 is equivalent to the positive phase of MCLK (see figure 23).

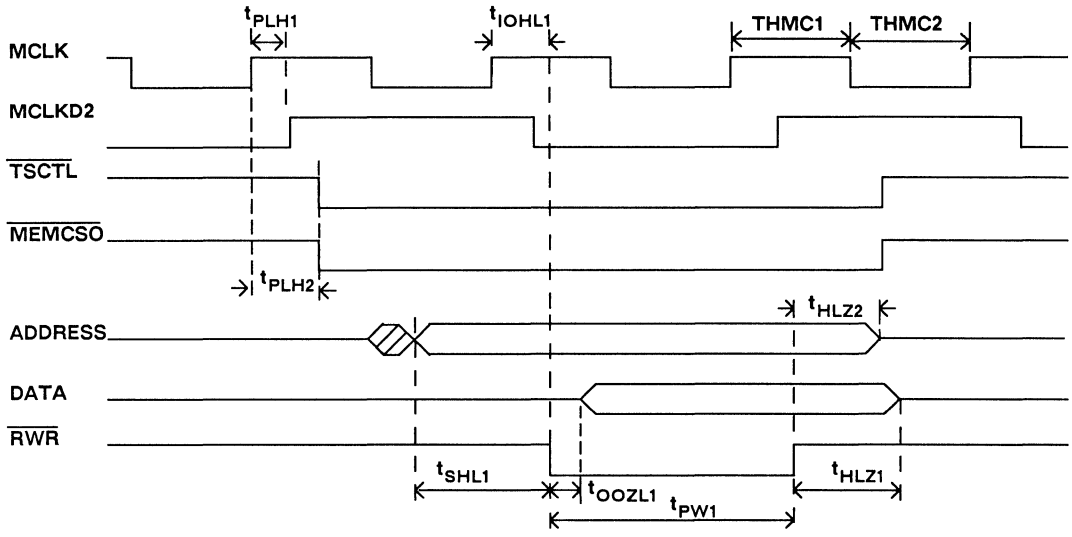
Figure 22. BURST DMA Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RRD}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{PW1}	$\overline{RRD}$ ↓ to $\overline{RRD}$ ↑	MCLK-5	MCLK+5	ns
t_{HLZ2}	$\overline{RRD}$ ↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-10	THMC1	ns
t_{HLZ1}	$\overline{RRD}$ ↑ to DATA High Impedance (DATA hold)	5	–	ns
t_{SLH1}	DATA valid to $\overline{RRD}$ ↑ (DATA setup)	40	–	ns
t_{PLH1} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑ to $\overline{TSCTL/MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑ to $\overline{RRD}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

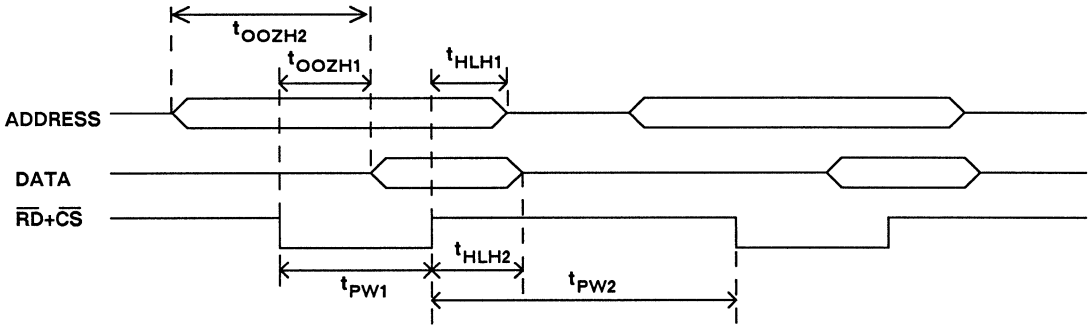
Figure 23. BCRT DMA Read Timing (One-Word Read)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RWR}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{OOZL1}(1)	$\overline{RWR}$↓ to DATA valid	0	30	ns
t_{HLZ1}	$\overline{RWR}$↑ to DATA High Impedance (DATA hold)	THMC1-20	THMC1	ns
t_{HLZ2}	$\overline{RWR}$↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-20	THMC1	ns
t_{PW1}	$\overline{RWR}$ ↓to $\overline{RWR}$ ↑	MCLK-5	MCLK+5	ns
t_{PLH1} (1)	MCLK ↑to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑to $\overline{TSCTL}$/$\overline{MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑to $\overline{RWR}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

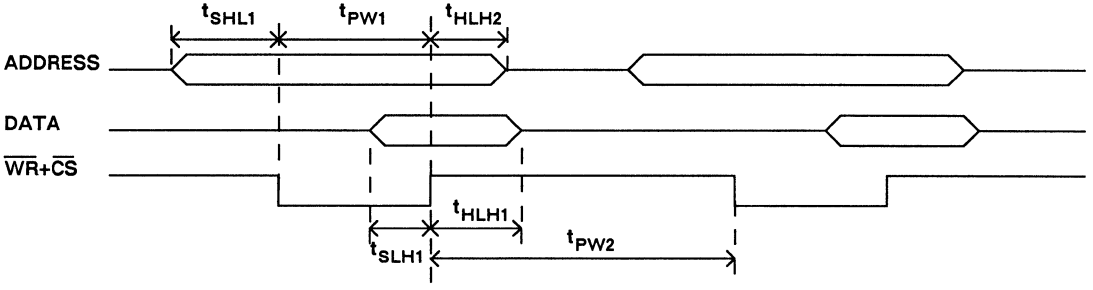
Figure 24. BCRT DMA Write Timing (One-Word Write)



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{OOZH2}	ADDRESS valid to DATA valid		-	80	ns
t_{HLH2}	$\overline{RD}+\overline{CS}$ ↑to DATA High Impedance	(DATA hold)	5	50	ns
t_{OOZH1} (1)	$\overline{RD}+\overline{CS}$ ↓to DATA valid	(DATA access)	-	60	ns
t_{HLH1}	$\overline{RD}+\overline{CS}$ ↑to ADDRESS High Impedance	(ADDRESS hold)	5	-	ns
t_{PW1}	$\overline{RD}+\overline{CS}$ ↓to $\overline{RD}+\overline{CS}$ ↑		60	-	ns
t_{PW2}	$\overline{RD}+\overline{CS}$ ↑to $\overline{RD}+\overline{CS}$ ↓		80	-	ns

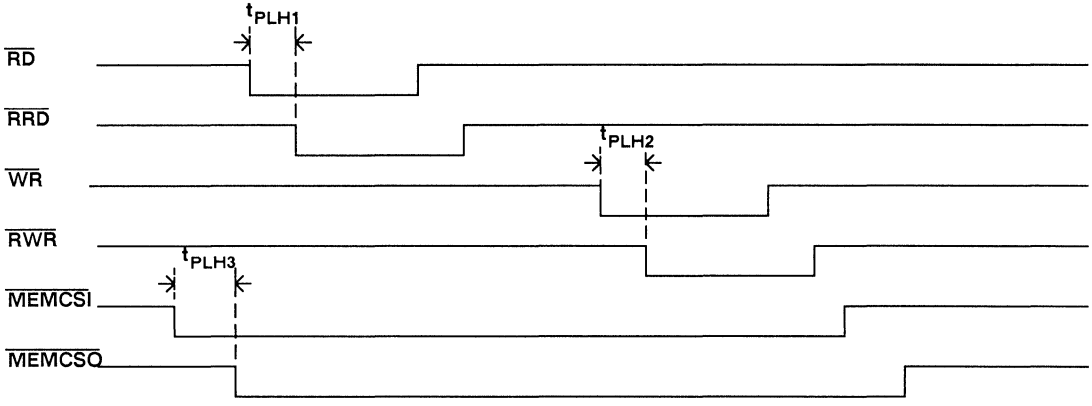
Notes:
1. Guaranteed by test.
2. User must adhere to both tOOZH1 and tOOZH2 timing constraints to ensure valid data.

Figure 25. BCRT Register Read Timing



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{WR}+\overline{CS}$ ↓	(ADDRESS setup)	60	-	ns
t_{SLH1}	DATA valid to $\overline{WR}+\overline{CS}$ ↑	(DATA setup)	60	-	ns
t_{PW1}	$\overline{WR}+\overline{CS}$↓ to $\overline{WR}+\overline{CS}$ ↑		60	-	ns
t_{HLH1}	$\overline{WR}+\overline{CS}$↑ to DATA High Impedance	(DATA hold)	10	-	ns
t_{HLH2}	$\overline{WR}+\overline{CS}$↑ to ADDRESS High Impedance	(ADDRESS hold)	10	-	ns
t_{PW2}	$\overline{WR}+\overline{CS}$↑ to $\overline{WR}+\overline{CS}$ ↓		80	-	ns

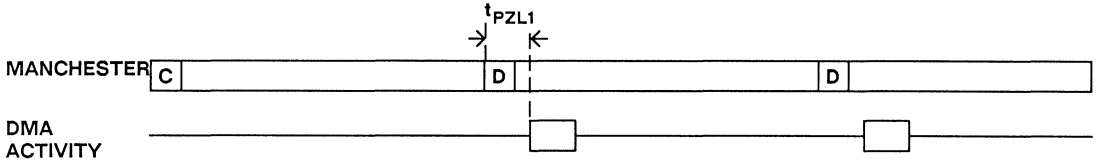
Figure 26. BCRT Register Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PLH1} (1)	$\overline{RD}$ ↓to $\overline{RRD}$ ↓	0	30	ns
t_{PLH2} (1)	$\overline{WR}$↓ to $\overline{RWR}$ ↓	0	30	ns
t_{PLH3} (1)	$\overline{MEMCSI}$ ↓to $\overline{MEMCSO}$ ↓	0	30	ns

Note:
1. Guaranteed by test.

Figure 27. BCRT Dual-Port Interface Timing Delays

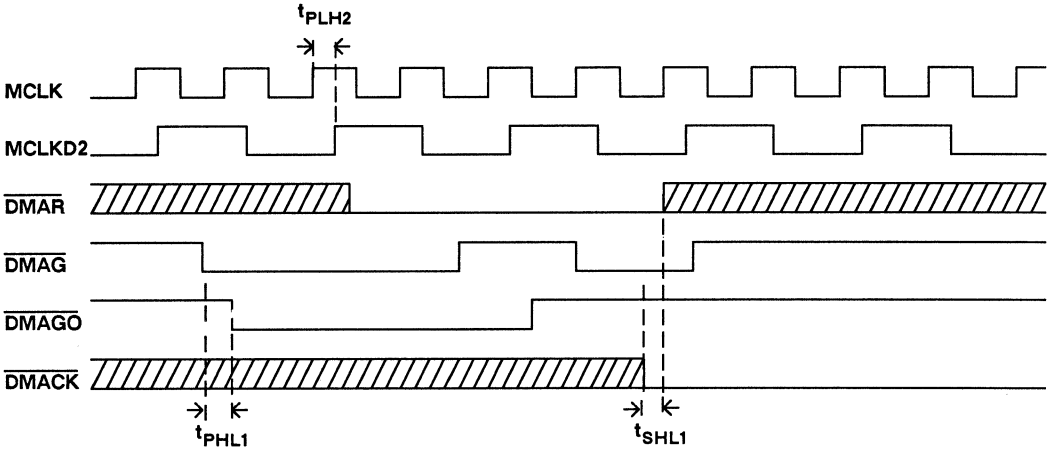


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PZL1}	Data word to DMA activity	0	4	μs

This diagram indicates the relationship between the incoming Manchester code and DMA activity (i.e., $\overline{DMAR}$↓ to $\overline{DMACK}$↑).

Note:
The pulsewidth = (11 μs -t_{DMA} -t_{PZL1}) where t_{DMA} is the time to complete DMA activity (i.e., $\overline{DMAR}$↓ to $\overline{DMACK}$ ↑).

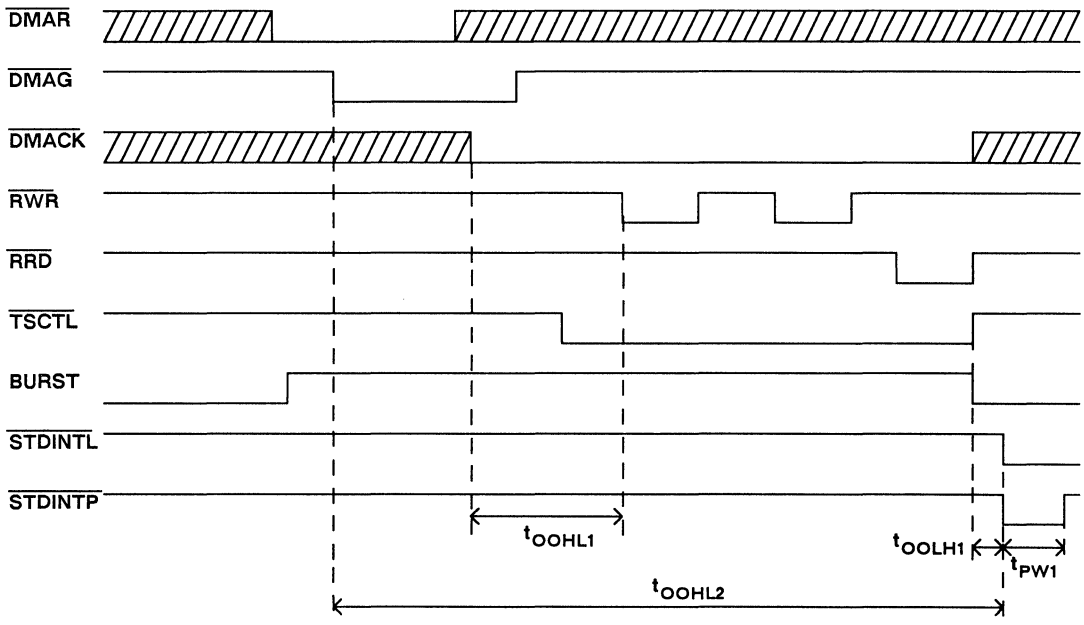
Figure 28. DMA Activity (RT Mode)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PHL1}	$\overline{DMAG}$ ↓ to $\overline{DMAGO}$ ↓	0	30	ns
t_{SHL1}	$\overline{DMACK}$ ↓ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PLH2} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns

Notes:
1. Guaranteed by test.
2. When $\overline{DMAG}$ is asserted before $\overline{DMAR}$, the $\overline{DMAG}$ signal passes through the BCRT as $\overline{DMAGO}$.

Figure 29. BCRT Arbitration when $\overline{DMAG}$ is Asserted before Arbitration



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{OOLH1}	$\overline{TSCTL}\uparrow$ to $\overline{STDINTP}/\overline{STDINTL}\downarrow$	-	1	µs
t_{PW1}	$\overline{STDINTP}\downarrow$ to $\overline{STDINTP}\uparrow$	320	340	ns
t_{OOHL1}	$\overline{DMACK}\downarrow$ to $\overline{RWR}\downarrow$	3xMCLK-10	5xMCLK	ns
t_{OOHL2}	$\overline{DMAG}\downarrow$ to $\overline{STDINTL}\downarrow$	8xMCLK+0.5	10xMCLK+1	ns

Note:
Address and data bus relationships (not shown) are identical to figure 22.

Figure 30. BCRT Interrupt Log List Entry Operation Timing

12.0 Package Outline Drawings

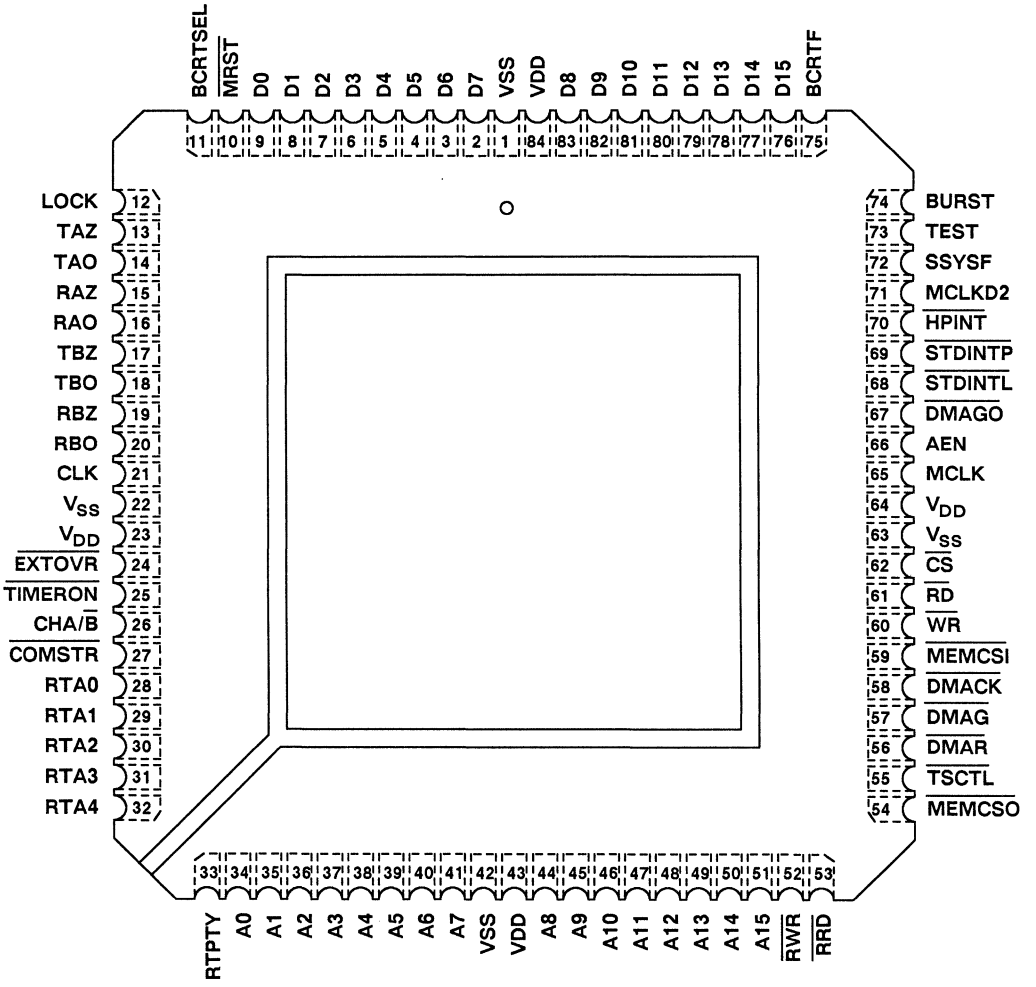


Figure 31a. BCRT Flatpack and LCC Pin Identification (Top View)
(Flatpack Leads Omitted for Clarity)

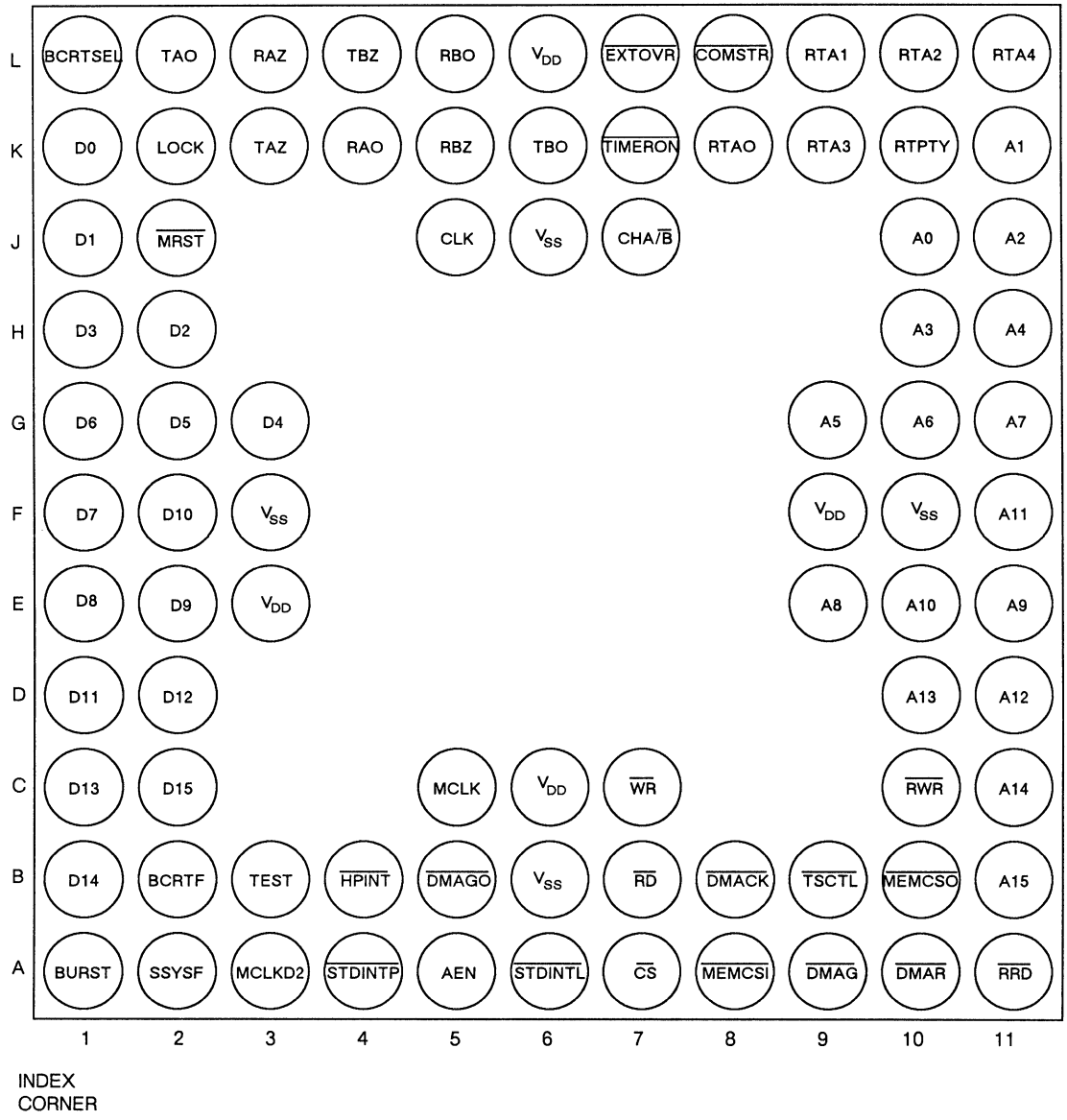


Figure 31b. BCRT Pingrid Array Pin Indentification (Bottom View)

UT1553B BCRTM

FEATURES

- ☐ Comprehensive MIL-STD-1553B dual-redundant Bus Controller (BC) and Remote Terminal (RT) and Monitor (M) functions
- ☐ Multiple message processing capability in BC, RT, and M modes
- ☐ Automatic polling and intermessage delay in BC mode
- ☐ Programmable interrupt scheme and internally generated interrupt history list
- ☐ Register-oriented architecture to enhance programmability
- ☐ DMA or pseudo-dual-port memory interface with 64K addressability
- ☐ Internal wraparound self-test
- ☐ Time tagging and message logging in RT and M modes
- ☐ Packaged in 84-pin pingrid array, 84-lead flatpack, or 84-pad LCC
- ☐ Low-power CMOS technology
- ☐ Full military operating temperature range, −55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ☐ Architecturally and pin-compatible with UTMC's UT1553B BCRT

3

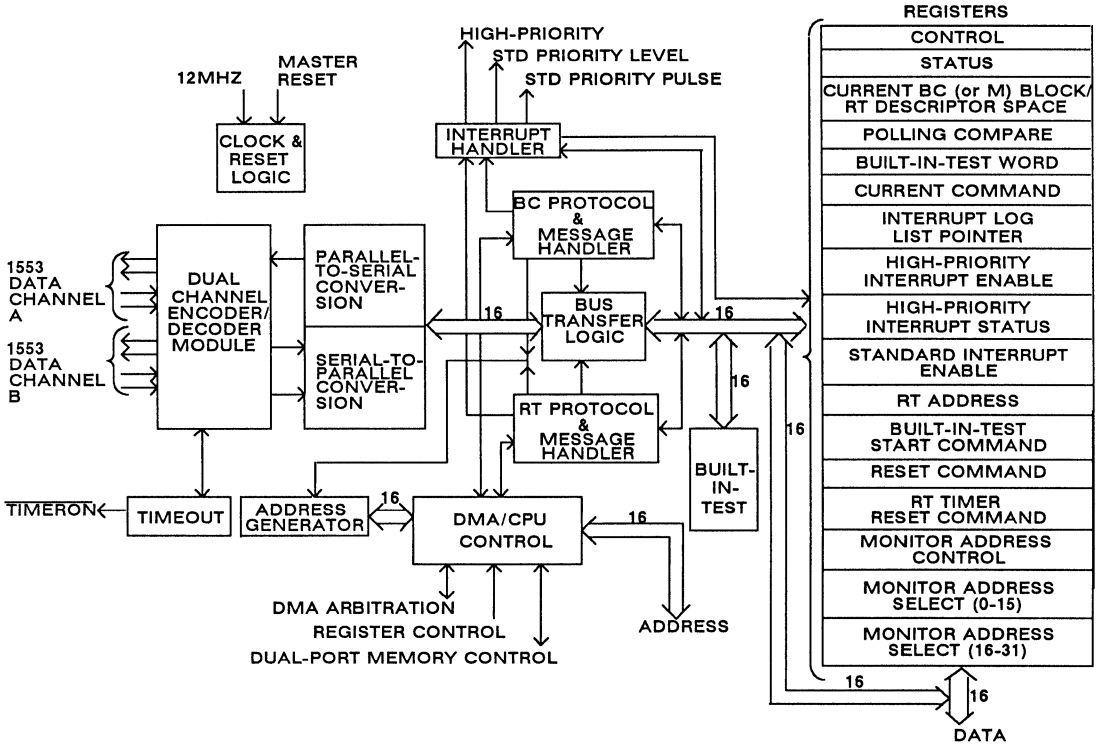


Figure 1. BCRTM Block Diagram

Table of Contents

1.0 INTRODUCTION

The monolithic CMOS UT1553B BCRTM provides the system designer with an intelligent solution to MIL-STD-1553B multiplexed serial data bus design problems. The UT1553B BCRTM is a single-chip device that implements all three of the defined MIL-STD-1553B functions - Bus Controller, Remote Terminal, and Monitor. Designed to reduce host CPU overhead, the BCRTM's powerful state machines automatically execute message transfers, provide interrupts, and generate status information. Multiple registers offer many programmable functions as well as extensive information for host use. In the BC mode, the BCRTM uses a linked-list message scheme to provide the host with message chaining capability. The BCRTM enhances memory use by supporting variable-size, relocatable data blocks. In the RT mode, the BCRTM implements time-tagging and message history functions. It also supports multiple (up to 128) message buffering and variable length messages to any subaddress. In the Monitor (M) mode, the BCRTM's powerful linked list command block structure allows it to process a series of monitored 1553 messages without the intervention of the host. The BCRTM can store as much bus traffic as can be contained in its 64K memory space. In addition, the host has the capability of instructing the BCRTM to monitor and store data for only selected remote terminals.

The UT1553B BCRTM is an intelligent, versatile, and easy to implement device -- a powerful asset to system designers.

1.1 Features - Remote Terminal (RT) Mode

Indexing
The BCRTM is programmable to index or buffer messages on a subaddress-by-subaddress basis. The BCRTM, which can index as many as 128 messages, can also assert an interrupt when either the selected number of messages is reached or every time a specified subaddress is accessed.

Variable Space Allocation
The BCRTM can use as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

Sequential Data Storage
The BCRTM stores/retrieves, by subaddress, all messages in the order in which they are transacted.

Sequential Message Status Information
The BCRTM provides message validity, time-tag, and word-count information, and stores it sequentially in a separate, cross-referenced list.

Illegalizing Mode Codes and Subaddresses
The host can declare mode codes and subaddresses illegal by setting the appropriate bit(s) in memory.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTM provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

1.2 Features - Bus Controller (BC) Mode

Multiple Message Processing
The BCRTM autonomously processes any number of messages or lists of messages that may be stored in a 64K memory space.

Automatic Intermessage Delay
When programmed by the host, the BCRTM can delay a host-specified time before executing the next message in sequence.

Automatic Polling
When polling, the BCRTM interrogates the remote terminals and then compares their status word responses to the contents of the Polling Compare Register. The BCRTM can interrupt the host CPU if an erroneous remote terminal status word response occurs.

Automatic Retry
The BCRTM can automatically retry a message on busy, message error, and/or response time-out conditions. The BCRTM can retry up to four times on the same or on the alternate bus.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTM provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

Variable Space Allocation
The BCRTM uses as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

1.3 Features - Monitor (M) Mode

Command History List
The BCRTM's linked list command block structure permits the BCRTM to process a series of monitored messages without host intervention.

Monitor Selected Terminal Addresses
The host can select the remote terminals to be monitored by programming the proper bits in the Terminal Address Select registers (Registers 16 and 17). The BCRTM can monitor any or all remote terminals.

Variable Space Allocation
The BCRTM can use as little or as much memory (up to 64K) as needed.

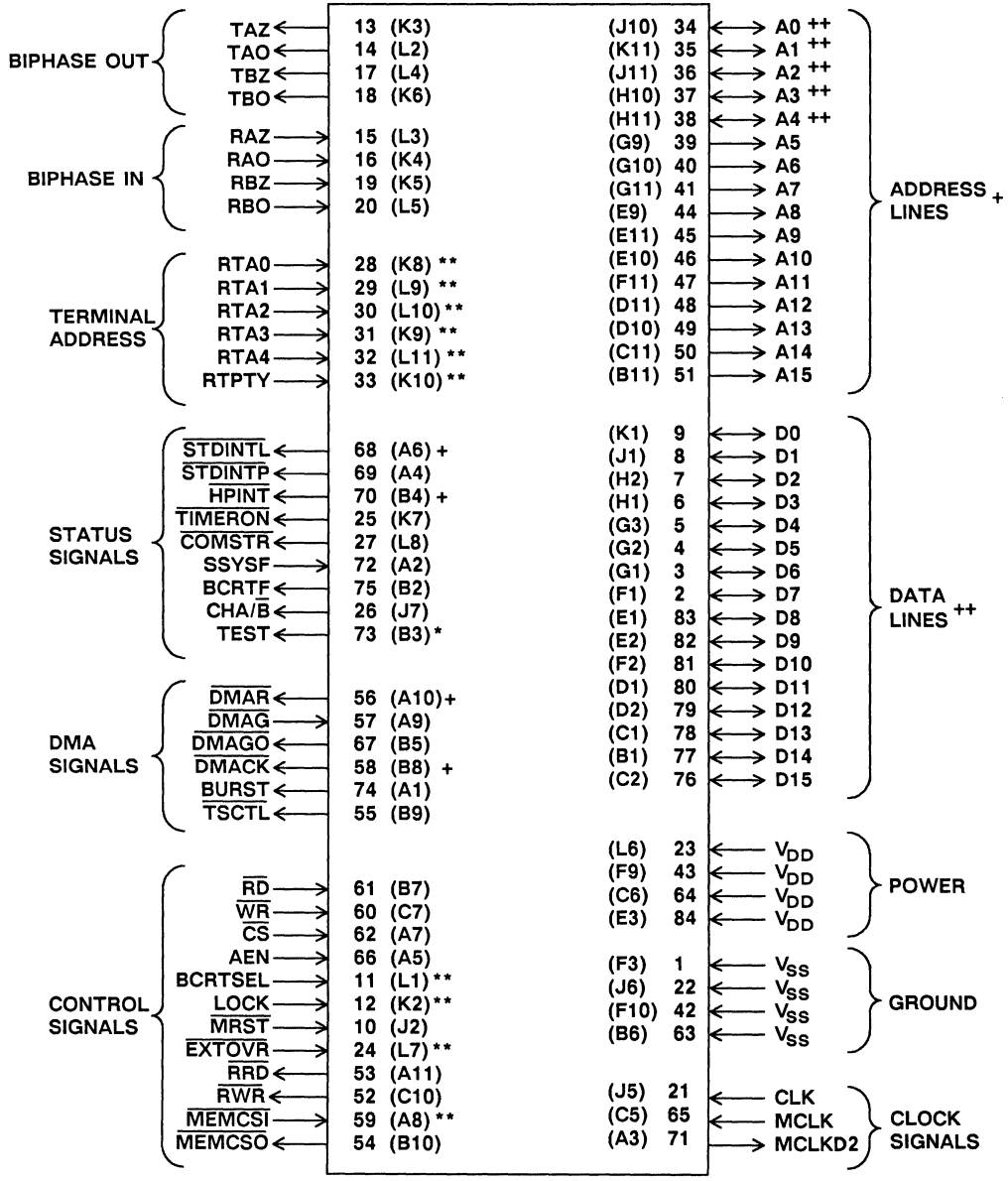
Selectable Data Storage
Address programmability within the BCRTM provides flexible data placement and convenient access.

Sequential Data Storage
The BCRTM stores, by Terminal Address, all 1553 messages in the order in which they are transacted.

Programmable Interrupt Selection
The host can select a wide variety of events that may cause an interrupting event.

Interrupt History List
The BCRTM stores, chronologically in memory, an Interrupt History List of each event that caused an interrupt.

2.0 Pin Identification And Description



** Pin internally pulled up.
+ Pin at high impedance when not asserted.
++ Bidirectional pin.
* Formerly $\overline{\text{MEMWIN}}$

( ) Pingrid array pin identification in parentheses.
LCC, flatpack pin number not in parentheses.

Figure 2. BCRTM Functional Pin Description

Legend for TYPE and ACTIVE fields:

TUI = TTL input (pull-up)
AL = Active low
AH = Active high
ZL = Active low - inactive state is high impedance
TI = TTL input
TO = TTL output
TTO = Three-state TTL output
TTB = Bidirectional

Notes:
1. Address and data buses are in the high-impedance state when idle.
2. Flatpack pin numbers are same as LCC.

ADDRESS BUS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
A0	34	J10	TTB	--	Bit 0 (LSB) of the Address bus.
A1	35	K11	TTB	--	Bit 1 of the Address bus.
A2	36	J11	TTB	--	Bit 2 of the Address bus.
A3	37	H10	TTB	--	Bit 3 of the Address bus.
A4	38	H11	TTB	--	Bit 4 of the Address bus.
A5	39	G9	TTO	--	Bit 5 of the Address bus.
A6	40	G10	TTO	--	Bit 6 of the Address bus.
A7	41	G11	TTO	--	Bit 7 of the Address bus.
A8	44	E9	TTO	--	Bit 8 of the Address bus.
A9	45	E11	TTO	--	Bit 9 of the Address bus.
A10	46	E10	TTO	--	Bit 10 of the Address bus.
A11	47	F11	TTO	--	Bit 11 of the Address bus.
A12	48	D11	TTO	--	Bit 12 of the Address bus.
A13	49	D10	TTO	--	Bit 13 of the Address bus.
A14	50	C11	TTO	--	Bit 14 of the Address bus.
A15	51	B11	TTO	--	Bit 15 (MSB) of the Address bus.

DATA BUS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
D0	9	K1	TTB	--	Bit 0 (LSB) of the Data bus.
D1	8	J1	TTB	--	Bit 1 of the Data bus.
D2	7	H2	TTB	--	Bit 2 of the Data bus.
D3	6	H1	TTB	--	Bit 3 of the Data bus.
D4	5	G3	TTB	--	Bit 4 of the Data bus.
D5	4	G2	TTB	--	Bit 5 of the Data bus.
D6	3	G1	TTB	--	Bit 6 of the Data bus.
D7	2	F1	TTB	--	Bit 7 of the Data bus.
D8	83	E1	TTB	--	Bit 8 of the Data bus.
D9	82	E2	TTB	--	Bit 9 of the Data bus.
D10	81	F2	TTB	--	Bit 10 of the Data bus.
D11	80	D1	TTB	--	Bit 11 of the Data bus.
D12	79	D2	TTB	--	Bit 12 of the Data bus.
D13	78	C1	TTB	--	Bit 13 of the Data bus.
D14	77	B1	TTB	--	Bit 14 of the Data bus.
D15	76	C2	TTB	--	Bit 15 (MSB) of the Data bus.

TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
RTA0	28	K8	TUI	--	Remote Terminal Address Bit 0 (LSB). The entire RT address is strobed in at Master Reset. Verify it by reading the Remote Terminal Address Register. All the Remote Terminal Address bits are internally pulled up.
RTA1	29	L9	TUI	--	Remote Terminal Address Bit 1. This is bit 1 of the Remote Terminal Address.
RTA2	30	L10	TUI	--	Remote Terminal Address Bit 2. This is bit 2 of the Remote Terminal Address.
RTA3	31	K9	TUI	--	Remote Terminal Address Bit 3. This is bit 3 of the Remote Terminal Address.
RTA4	32	L11	TUI	--	Remote Terminal Address Bit 4. This is bit 4 (MSB) of the Remote Terminal Address.
RTPTY	33	K10	TUI	--	Remote Terminal (Address) Parity. This is an odd parity input for the Remote Terminal Address.

CONTROL SIGNALS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{RD}$	61	B7	TI	AL	Read. The host uses this in conjunction with $\overline{CS}$ to read an internal BCRTM register.
$\overline{WR}$	60	C7	TI	AL	Write. The host uses this in conjunction with $\overline{CS}$ to write to an internal BCRTM register.
$\overline{CS}$	62	A7	TI	AL	Chip Select. This selects the BCRTM when accessing the BCRTM's internal register.
AEN	66	A5	TI	AH	Address Enable. The host CPU uses AEN to indicate to the BCRTM that the BCRTM's address lines can be asserted; this is a precautionary signal provided to avoid address bus crash. If not used, it must be tied high.
BCRTSEL	11	L1	TUI	--	BC/$\overline{RT}$ Select. This selects between either the Bus Controller or Remote Terminal mode. The BC/$\overline{RT}$ Mode Select bit in the Control Register overrides this input if the LOCK pin is not high. To operate in Monitor mode, the pin should be held low. This pin is internally pulled high.
LOCK	12	K2	TUI	AH	Lock. When set, this pin prevents internal changes to both the RT address and BC/$\overline{RT}$ mode select functions. This pin is internally pulled high.
$\overline{EXTOVR}$	24	L7	TUI	AL	External Override. Use this in multi-redundant applications. Upon receipt, the BCRTM aborts all current activity. $\overline{EXTOVR}$ should be connected to $\overline{COMSTR}$ output of the adjacent BCRTM when used. This pin is internally pulled high.
$\overline{MRST}$	10	J2	TI	AL	Master Reset. This resets all internal state machines, encoders, decoders, and registers. The minimum pulse width for a successful Master Reset is 500 ns.
$\overline{MEMCSO}$	54	B10	TO	AL	Memory Chip Select Out. This is the regenerated MEMCSI input for external RAM during the pseudo-dual-port RAM mode. The BCRTM also uses it to select external memory during memory accesses.
$\overline{MEMCSI}$	59	A8	TI	AL	Memory Chip Select In. Used in the pseudo-dual-port RAM mode only, $\overline{MEMCSI}$ is received from the host and is propagated through to $\overline{MEMCSO}$.
$\overline{RRD}$	53	A11	TO	AL	RAM Read. In the pseudo-dual-port RAM mode, the host uses this signal in conjunction with $\overline{MEMSCO}$ to read from external RAM through the BCRTM. It is also the signal the BCRTM uses to read from memory. It is asserted following receipt of $\overline{DMAG}$. When the BCRTM performs multiple reads, this signal is pulsed.
$\overline{RWR}$	52	C10	TO	AL	RAM Write. In the pseudo-dual-port RAM mode, the CPU and BCRTM use this to write to external RAM. This signal is asserted following receipt of $\overline{DMAG}$. For multiple writes, this signal is pulsed.

STATUS SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{STDINTL}}$	68	A6	TTO	ZL	Standard Interrupt Level. This is a level interrupt. It is asserted when one or more events enabled in either the Standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur. Resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register clears the interrupt.
$\overline{\text{STDINTP}}$	69	A4	TO	AL	Standard Interrupt Pulse. $\overline{\text{STDINTP}}$ pulses when an interrupt is logged.
$\overline{\text{HPINT}}$	70	B4	TTO	ZL	High-Priority Interrupt. The High-Priority Interrupt level is asserted upon occurence of events enabled in the High-Priority Interrupt Enable Register. The corresponding bit(s) in the High-Priority Interrupt Status/Reset Register reset $\overline{\text{HPINT}}$.
$\overline{\text{TIMERON}}$	25	K7	TO	AL	(RT) Timer On. This is a 760-microsecond fail-safe transmitter enable timer. Started at the beginning of a transmission, $\overline{\text{TIMERON}}$ goes inactive 760 microseconds later or is reset automatically with the receipt of a new command. Use it in conjunction with CHA/$\overline{\text{B}}$ output to provide a fail-safe timer for channel A and B transmitters.
$\overline{\text{COMSTR}}$	27	L8	TO	AL	(RT) Command Strobe. The BCRTM asserts this signal after receiving a valid command. The BCRTM deactivates it after servicing the command.
SSYSF	72	A2	TI	AH	Subsystem Fail. Upon receipt, this signal propagates directly to the RT 1553 status word and the BCRTM Status Register.
BCRTF	75	B2	TO	AH	BCRT Fail. This indicates a Built-In-Test (BIT) failure. In the RT mode, the Terminal Flag bit in 1553 status word is also set.
CHA/$\overline{\text{B}}$	26	J7	TO	--	Channel A/$\overline{\text{B}}$. This indicates the active or last active channel.
TEST	73	B3	TO	AL	TEST. This pin is used as a factory test pin. (Formerly $\overline{\text{MEMWIN}}$.)

BIPHASE INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
RAO	16	K4	TI	--	Receive Channel A One. This is the Manchester-encoded true signal input from Channel A of the bus receiver.
RAZ	15	L3	TI	--	Receive Channel A Zero. This is the Manchester-encoded complementary signal input from Channel A of the bus receiver.
RBO	20	L5	TI	--	Receive Channel B One. This is the Manchester-encoded true signal input from Channel B of the bus receiver.
RBZ	19	K5	TI	--	Receive Channel B Zero. This is the Manchester-encoded complementary signal input from Channel B of the bus receiver.

BIPHASE OUTPUTS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
TAO	14	L2	TO	--	Transmit Channel A One. This is the Manchester-encoded true output to be connected to the Channel A bus transmitter input. This signal is idle low.
TAZ	13	K3	TO	--	Transmit Channel A Zero. This is the Manchester-encoded complementary output to be connected to the Channel A bus transmitter input. This signal is idle low.
TBO	18	K6	TO	--	Transmit Channel B One. This is the Manchester-encoded true output to be connected to the Channel B bus transmitter input. This signal is idle low.
TBZ	17	L4	TO	--	Transmit Channel B Zero. This is the Manchester-encoded complementary output to be connected to the Channel B bus transmitter input. This signal is idle low.

DMA SIGNALS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{DMAR}}$	56	A10	TTO	ZL	DMA Request. The BCRTM issues this signal when access to RAM is required. It goes inactive after receiving a $\overline{\text{DMAG}}$ signal.
$\overline{\text{DMAG}}$	57	A9	TI	AL	DMA Grant. This input to the BCRTM allows the BCRT to access RAM. It is recognized 45 ns before the rising edge of MCLKD2.
$\overline{\text{DMAGO}}$	67	B5	TO	AL	DMA Grant Out. If $\overline{\text{DMAG}}$ is received but not needed, it passes through to this output.
$\overline{\text{DMACK}}$	58	B8	TTO	ZL	DMA Acknowledge. The BCRTM asserts this signal to confirm receipt of $\overline{\text{DMAG}}$; it stays low until memory access is complete.
BURST	74	A1	TO	AH	Burst (DMA Cycle). This indicates that the current DMA cycle transfers at least two words; worst case is five words plus a "dummy" word.
$\overline{\text{TSCTL}}$	55	B9	TO	AL	Three-State Control. This signal indicates when the BCRTM is actually accessing memory. The host subsystem's address and data lines must be in the high-impedance state when the signal is active. This signal assists in placing the external data and address buffers into the high-impedance state.

CLOCK SIGNALS

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
CLK	21	J5	TI	--	Clock. The 12 MHz input clock requires a 50% +/-10% duty cycle with an accuracy of +/-0.01%. The accuracy is required in order to meet the Manchester encoding/decoding requirements of MIL-STD-1553B.
MCLK	65	C5	TI	--	Memory Clock. This is the input clock frequency the BCRTM uses for memory accesses. The memory cycle time is equal to two MCLK cycles. Therefore, RAM access time is dependent upon the chosen MCLK frequency (6 MHz minimum, 12 MHz maximum). Please see the BCRTM DMA timing diagrams in this data sheet.
MCLKD2	71	A3	TO	--	Memory Clock Divided by Two. This signal is the Memory Clock input divided by two. It assists the host subsystem in synchronizing DMA events.

POWER AND GROUND

NAME	PIN NUMBER LCC	PGA	TYPE	ACTIVE	DESCRIPTION
V_{DD}	23	L6	PWR	--	+5V
V_{DD}	43	F9	PWR	--	+5V
V_{DD}	64	C6	PWR	--	+5V
V_{DD}	84	E3	PWR	--	+5V
V_{SS}	1	F3	GND	--	Ground
V_{SS}	22	J6	GND	--	Ground
V_{SS}	42	F10	GND	--	Ground
V_{SS}	63	B6	GND	--	Ground

3.0 Internal Registers

The BCRTM's internal registers (see table 1 on pages 18-19) enable the CPU to control the actions of the BCRTM while maintaining low DMA overhead by the BCRTM. All functions are active high and ignored when low unless stated otherwise. Functions and parameters are used in both RT and BC modes except where indicated. Registers are addressed by the binary equivalent of their decimal number. For example, Register 1 is addressed as 0001B. Register usage is defined as follows:

#0 Control Register

Bit Number	Description
BIT 15	Reserved.
BIT 14	RT Address 31. When RT31 = 0, the BCRTM recognizes RT Address 31 as a Broadcast command. When RT31 = 1, the BCRTM treats RT Address 31 as a normal terminal address.
BIT 13	Subaddress 31. When SA31 = 0, the BCRTM recognizes a command word with either subaddress 0 or 31 as being a valid mode code. When SA31 = 1, the BCRTM only recognizes a command word with a subaddress of 0 as a valid mode code.
BIT 12	Bus Controller Time-Out. When the BCRTM is a BC and BCTO = 0, the BCRTM allows an RT up to 16 μs to respond with a status word before it declares a bus time-out. If BCTO = 1, the BCRTM allows an RT up to 32 μs to respond with a status word before it declares a bus time-out.
BIT 11	Enable External Override. For use in multi-redundant systems. This bit enables the $\overline{\text{EXTOVR}}$ pin.
BIT 10	BC/$\overline{\text{RT}}$ Select. This function selects between the Bus Controller and Remote Terminal/Monitor operation modes. It overrides the external BCRTSEL input setting if the Change Lock-Out function is not used. A reset operation must be performed when changing between BC and RT/M modes. For Monitor operation this bit must be "0". This bit is write-only.
BIT 9	(BC) Retry on Alternate Bus. This bit enables an automatic retry to operate on alternate buses. For example, if on bus A, with two automatic retries programmed, the automatic retries occur on bus B.
BIT 8	(RT,M) Channel B Enable. When set, this bit enables Channel B operation. (BC) No significance.
BIT 7	(RT,M) Channel A Enable. When set, this bit enables Channel A operation. (BC) Channel Select A/$\overline{\text{B}}$. When set, this bit selects Channel A.
BITs 6-5	(BC) Retry Count. These bits program the number (1-4) of retries to attempt. (00 = 1 retry, 11 = 4 retries)
BIT 4	(BC) Retry on Bus Controller Message Error. This bit enables automatic retries on an error the Bus Controller detects (see the Bus Controller Architecture section, page 29).
BIT 3	(BC) Retry on Time-out. This bit enables an automatic retry on a response time-out condition.
BIT 2	(BC) Retry on Message Error. This bit enables an automatic retry when the Message Error bit is set in the RT's status word response.
BIT 1	(BC) Retry on Busy. This bit enables automatic retry on a received Busy bit in an RT status word response.
BIT 0	Start Enable. In the BC mode, this bit starts/restarts Command Block execution. In the RT or M mode, it enables the BCRTM to receive a valid command. RT or M operation does not start until a valid command is received. When using this function: • Restart the BCRTM after each Master Reset or programmed reset. • This bit is not readable; verify operation by reading bit 0 of the BCRTM's Status Register.

#1 Status Register (Read Only)
These bits indicate the BCRTM's current status.

Bit Number	Description
BIT 15	TEST. This bit reflects the inverse of the TEST output. It changes state simultaneously with the TEST output.
BIT 14	(RT,M) Remote Terminal (or Monitor) Active. Indicates that the BCRTM, in the Remote Terminal (or Monitor) mode, is presently servicing a command. This bit reflects the inverse of the $\overline{\text{COMSTR}}$ pin.
BIT 13	(RT) Dynamic Bus Control Acceptance. This bit reflects the state of the Dynamic Bus Control Acceptance bit in the RT status word (see Register 10 on page 16).
BIT 12	(RT) Terminal Flag bit is set in RT status word. This bit reflects the result of writing to Register 10, bit 11.
BIT 11	(RT) Service Request bit is set in RT status word. This bit reflects the result of writing to Register 10, bit 10.
BIT 10	(RT) Busy bit is set in RT status word. This bit reflects the result of writing to Register 10, bits 9 or 14.
BIT 9	BIT is in progress.
BIT 8	Reset is in progress. This bit indicates that either a write to Register 12 has just occurred or the BCRTM has just received a Reset Remote Terminal (#01000) Mode Code. This bit remains set less than one microsecond.
BIT 7	BC/($\overline{\text{RT}}$ or $\overline{\text{M}}$) Mode. Indicates the current mode of operation. A reset operation must be performed when changing between BC and RT modes.
BIT 6	Channel A/$\overline{\text{B}}$. Indicates either the channel presently in use or the last channel used.
BIT 5	Subsystem Fail Indicator. Indicates receiving a subsystem fail signal from the host subsystem on the SSYSF input.
BITs 4-1	Reserved.
BIT 0	(BC) Command Block Execution is in progress. (RT) Remote Terminal is in operation. (M) Monitor is in operation. This bit reflects bit 0 of Register 0.

#2 Current Command Block Register (BC,M)/Remote Terminal Descriptor Space Address Register (RT)
(BC) This register contains the address of the head pointer of the Command Block being executed. Accessing a new Command Block updates it.

(RT) The host CPU initializes this register to indicate the starting location of the RT Descriptor Space. The host must allocate 320 sequential locations following this starting address. For proper operation, this location must start on an I x 512 decimal address boundary, where I is an integer multiple. (I = 0 is valid boundary conditions.)

(M) This register contains the address of the control/status word of the current Monitor Command Block. Accessing a new Command Block updates it.

#3 Polling Compare Register
In the polling mode, the CPU sets the Polling Compare Register to indicate the RT response word on which the BCRTM should interrupt. This register is 11 bits wide, corresponding to bit times 9 through 19 of the RT's 1553 status word response. The sync, Remote Terminal Address, and parity bits are not included (see the section on Polling, page 32).

#4 BIT (Built-In-Test) Word Register
The BCRTM uses the contents of this register when it responds to the Transmit BIT Word Mode Code (#10011). In addition, the BCRTM writes to the two most significant bits of the BIT Word Register in response to either an Initiate Self-Test Mode Code (RT mode) or a write to Register 11 (BIT Start Command). If the BIT Word needs to be modified, it can be read out, modified, then rewritten to this register. Note that if the processor writes a "1" to either bit 14 or 15 of this register, it effectively induces a BIT failure.

Bit Number	Description
BIT 15	Channel B failure.
BIT 14	Channel A failure.
BITs 13-0	BIT Word. The least significant fourteen bits of the BIT Word are user programmable.

#5 Current Command Register (Read Only)
In the RT or Monitor mode, this register contains the command currently being processed. When not processing a command, the BCRTM stores the last command or status word transmitted on the 1553B bus. This register is updated only when bit 0 of Register 0 is set. In the BC mode, this register contains the most current command sent out on the 1553B bus.

#6 Interrupt Log List Pointer Register
Initialized by the CPU, the Interrupt Log List Pointer Register indicates the start of the Interrupt Log List. After each list entry, the BCRTM updates this register with the address of the next entry in the list. (See page 37.)

#7 High-Priority Interrupt Enable Register (Read/Write)
Setting the bits in this register causes a High-Priority Interrupt when the enabled event occurs. To service the High-Priority Interrupt, the user reads Register 8 to determine the cause of the interrupt, then writes to Register 8 to clear the appropriate bits. The BCRTM also provides a Standard Priority Interrupt Scheme that does not require host intervention. If High-Priority Interrupt service is not possible in a given application, it is advisable to use the Standard Priority features.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun Enable. When set, this bit enables an interrupt when $\overline{\text{DMAG}}$ was not received by the BCRTM within the allotted time needed for a successful data transfer to memory.
BIT 7	(BC) Illogical Command Error Enable. This bit enables a High-Priority Interrupt to be asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formated RT-RT Command Blocks.
BIT 6	(RT) Dynamic Bus Control Mode Code Interrupt Enable. When set, the BCRTM asserts an interrupt when the Dynamic Bus Control Mode Code is received.
BIT 5	Subsystem Fail Enable. When set, a High-Priority Interrupt is asserted after receiving a Subsystem Fail (SSYSF) input pin.
BIT 4	End of BIT Enable. This bit indicates the end of the internal BIT routine.
BIT 3	BIT Word Fail Enable. This bit enables an interrupt indicating that the BCRTM detected a BIT failure.
BIT 2	(BC) End of Command Block List Enable (see Command Block Control Word, page 31.) This interrupt can be superseded by other high-priority interrupts.
BIT 1	Message Error Enable. If enabled, a High-Priority Interrupt is asserted at the occurrence of a message error. If a High-Priority Interrupt condition occurs, as the result of an enabled message error, the device will halt operation until the user clears the interrupt by writing a "1" to Bit 1 of the High-Priority Interrupt Status/Reset Register (Reg. #8). If this interrupt is not cleared, the BCRTM remains in the HALTED state (appearing to be "locked-up"), even if it receives a valid message. This High-Priority Interrupt scheme is necessary in order to maintain the BCRTM's state of operation so that the host CPU has this information available at the time of interrupt service.
BIT 0	Standard Interrupt Enable. Setting this bit enables the $\overline{\text{STDINTL}}$ pin, but does not cause a high-priority interrupt. If low, only the $\overline{\text{STDINTP}}$ pin is asserted when a Standard Interrupt occurs.

#8 High-Priority Interrupt Status/Reset Register

When a High-Priority Interrupt is asserted, this register indicates the event that caused it. To clear the interrupt signal and reset the bit, write a "1" to the appropriate bit. See the corresponding bit definitions of Register 7, High-Priority Interrupt Enable Register.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun.
BIT 7	Illogical Command.
BIT 6	Dynamic Bus Control Mode Code Received.
BIT 5	Subsystem Fail.
BIT 4	End of BIT.
BIT 3	BIT Word Fail.
BIT 2	End of Command Block.
BIT 1	Message Error.
BIT 0	Standard Interrupt. The BCRTM sets this bit when any Standard Interrupt occurs, providing bit 0 of Register 7 is enabled. (Reset $\overline{\text{STDINTL}}$ output.)

#9 Standard Interrupt Enable Register

This register enables Standard Interrupt logging for any of the following enabled events (Standard Interrupt logging can also occur for events enabled in the BC Command Block or RT Subaddress/Mode Code Descriptor):

Bit Number	Description
BITs 15-6	Reserved.
BIT 5	(RT) Illegal Broadcast Command. When set, this bit enables an interrupt indicating that an Illegal Broadcast Command has been received.
BIT 4	(RT) Illegal Command. When set, this bit enables an interrupt indicating that an illegal command has been received.
BIT 3	(BC) Polling Comparison Match. This enables an interrupt indicating that a polling event has occurred. The user must also set bit 12 in the BC Command Block Control Word for this interrupt to occur.
BIT 2	(BC) Retry Fail. This bit enables an interrupt indicating that all the programmed number of retries have failed.
BIT 1	(BC,RT,M) Message Error Event. This bit enables a standard interrupt for message errors.
BIT 0	(BC,M) Command Block Interrupt and Continue. This bit enables an interrupt indicating that a Command Block, with the Interrupt and Continue Function enabled, has been executed.

#10 Remote Terminal Address Register
This register sets the Remote Terminal Address via software. The Change Lock-Out Enable feature, when set, prevents the Remote Terminal Address or the BCRTM Mode Selection from changing.

Bit Number	Description
BIT 15	(RT) Instrumentation. Setting this bit sets the RT status word Instrumentation bit.
BIT 14	(RT) Busy. Setting this bit sets the RT status word Busy bit. It does not inhibit data transfers to the subsystem.
BIT 13	(RT) Subsystem Fail. Setting this bit sets the RT status word Subsystem Flag bit. In the RT mode, the Subsystem Fail is also logged into the Message Status Word.
BIT 12	(RT) Dynamic Bus Control Acceptance. Setting this bit sets the RT status word Dynamic Bus Control Acceptance bit when the BCRTM receives the Dynamic Bus Control Mode Code from the currently active Bus Controller. Host intervention is required for the BCRTM to take over as the active Bus Controller.
BIT 11	(RT) Terminal Flag. Setting this bit sets the RT status word Terminal Flag bit; the Terminal Flag bit in the RT status word is also internally set if the BIT fails.
BIT 10	(RT) Service Request. Setting this bit sets the RT status word Service Request bit.
BIT 9	(RT) Busy Mode Enable. Setting this bit sets the RT status word Busy bit and inhibits all data transfers to the subsystem.
BIT 8	BC/$\overline{RT}$ Mode Select. This bit's state reflects the external pin BCRTSEL. It does not necessarily reflect the state of the chip, since the BC/$\overline{RT}$ Mode Select is software-programmable via bit 10 of Register 0. This bit is read-only.
BIT 7	Change Lock-Out. This bit's state reflects the external pin LOCK. When set, this bit indicates that changes to the RT address or the BC/$\overline{RT}$ Mode Select are not allowed using internal registers. This bit is read-only.
BIT 6	Remote Terminal Address Parity Error. This bit indicates a Remote Terminal Address Parity error. It appears after the Remote Terminal Address is latched if a parity error exists.
BIT 5	Remote Terminal Address Parity. This is an odd parity input bit used with the Remote Terminal Address. It ensures accurate recognition of the Remote Terminal Address.
BITs 4-0	Remote Terminal Address (Bit 0 is the LSB). This reflects the RTA4-0 inputs at Master Reset. Modify the Remote Terminal Address by writing to these bits.

#11 BIT Start Register (Write Only)
Any write (i.e., data = don't care) to this register's address location initiates the internal BIT routine, which lasts 100 μs. Verify using the BIT-in-Progress bit in the Status Register. A programmed reset (write to Register 12) must precede a write to this register to initiate the internal BIT. A failure of the BIT will be indicated in Register 4 and the BCRTF pin.

The BCRTM's self-test performs an internal wrap around test between its Manchester encoder and its two Manchester decoders. If the BCRTM detects a failure on either the primary or the secondary channel, it flags this failure by setting bit 14 of Register 4 (BIT Word Register) for Channel A and/or bit 15 for Channel B. When in the Remote Terminal mode, while the BCRTM is performing its self-test, it ignores any commands on the 1553 bus until it has completed the self–test.

#12 Programmed Reset Register (Write Only)
Any write (i.e., data = don't care) to this register's address location initiates a reset sequence of the encoder/decoder and protocol sections of the BCRTM which lasts less than 1 microsecond. This is identical to the reset used for the Reset Remote Terminal Mode Code except that command processing halts. For a total reset (i.e., including registers), see the $\overline{MRST}$ signal description.

#13 RT Timer Reset Register (Write Only)

Any write (i.e., data = don't care) to this register's address location resets the RT Time Tag timer to zero.

The BCRTM's Remote Terminal Timer time-tags message transactions. The time tag is generated from a free-running eight-bit timer of 64 microseconds resolution. This timer can be reset to zero simply by writing to Register 13. When the timer is reset, it immediately starts running.

#14 Bus Monitor Control Register

BIT 15 Bus Monitor Select. This bit should be cleared for RT mode operation. The host sets this bit to enable the BCRTM's Monitor mode of operation. Bit 10 of Register 0 must also be "0" to enable the Monitor mode.

BIT 14 Monitor All Terminals. When this bit is set, the BCRTM monitors all remote terminal bus activity. If this bit is not set, then bit 13 must be set. This bit should be cleared for RT mode operation.

BIT 13 Monitor Declared Terminals. When this bit is set, the BCRTM monitors only the remote terminals that are selected in Registers 16 and 17. If this bit is not set, then bit 14 must be set. This bit should be cleared for RT Mode operation.

BITs 12-0 Reserved.

#15 Reserved Register

This register is reserved for BCRTM use only and the host should not access it.

#16 Monitor Selected Remote Terminal Addresses 15 - 0

BITs 15-0 Monitor Selected Remote Terminal Addresses 15-0. By setting the appropriate bit in this register, the host can determine which of the remote terminals, from RT 0 through RT 15, the BCRTM will monitor. For example, by setting bit 5 in this register, the host instructs the BCRTM to only monitor the bus activity for remote terminal number 5. These bits are not mutually exclusive, therefore, the host can monitor any number of different remote terminals by selecting the proper combination of bits.

#17 Monitor Selected Remote Terminal Addresses 31 - 16

BITs 15-0 Monitor Selected Remote Terminal Addresses 31-16. By setting the appropriate bit in this register, the host can determine which of the remote terminals, from RT 16 through RT 31, the BCRTM will monitor. For example, by setting bit 5 in this register, the host instructs the BCRTM to only monitor the bus activity for remote terminal number 21. These bits are not mutually exclusive, therefore, the host can monitor any number of different remote terminals by selecting the proper combination of bits on this register and Register 16.

#0 BC/RT CONTROL REGISTER

15	14	13	12	11	10	9	8
UNUSED	RT31	SA31	BCTO	EXTOVR	BC/RT	RTYALTB	BUSBEN
7	6	5	4	3	2	1	0
CHNSEL BUSAEN	RTYCNT		RTYBCME	RTYTO	RTYME	RTYBSY	STEN

#1 BC/RT STATUS REGISTER

15	14	13	12	11	10	9	8
TEST	RTACT	DYNBUS	RT FLAG	SRQ	BUSY	BIT	RESET
7	6	5	4	3	2	1	0
BC/RT	BUSA/B	SSFAIL	UNUSED	UNUSED	UNUSED	UNUSED	CMBKPG

#2 (BC) CURRENT COMMAND BLOCK REGISTER
(RT) REMOTE TERMINAL DESCRIPTOR SPACE ADDRESS REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#3 POLLING COMPARE REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	MSGERR	INSTR	SRQ
7	6	5	4	3	2	1	0
SWBT12	SWBT13	SWBT14	BRDCST	BUSY	SS FLAG	DBC	TF

#4 BIT WORD REGISTER

15	14	13	12	11	10	9	8
CHBFAIL	CHAFAIL	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#5 CURRENT COMMAND REGISTER

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#6 INTERRUPT LOG LIST POINTER REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#7 BCRTM HIGH-PRIORITY INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

#8 BCRTM HIGH-PRIORITY INTERRUPT STATUS/RESET REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

Table 1. BCRTM Registers (continued)

#9 STANDARD INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
7	6	5	4	3	2	1	0
UNUSED	UNUSED	ILLBCMD	ILLCMD	POLMTCH	RTYFAIL	MSGERR	CMDBLK

#10 REMOTE TERMINAL ADDRESS REGISTER

15	14	13	12	11	10	9	8
INSTR	BUSY2	SS FLAG	DBC	RT FLAG	SRQ	BUSY1	BC/RT
7	6	5	4	3	2	1	0
LOCK	PARERR	RTAPAR	RTA4	RTA3	RTA2	RTA1	RTA0

#11 BUILT-IN-TEST START REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#12 PROGRAMMED RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#13 REMOTE TERMINAL TIMER RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#14 BUS MONITOR CONTROL REGISTER

15	14	13	12	11	10	9	8
BMS	MAT	MDT	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#15 RESERVED REGISTER (Host CPU Should Not Access)

#16 MONITOR SELECTED REMOTE TERMINAL ADDRESSES 0 - 15

15	14	13	12	11	10	9	8
TA15	TA14	TA13	TA12	TA11	TA10	TA9	TA8
7	6	5	4	3	2	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

#17 MONITOR SELECTED REMOTE TERMINAL ADDRESSES 16 - 31

15	14	13	12	11	10	9	8
TA31	TA30	TA29	TA28	TA27	TA26	TA25	TA24
7	6	5	4	3	2	1	0
TA23	TA22	TA21	TA20	TA19	TA18	TA17	TA16

X= DON'T CARE

Table 1. BCRTM Registers (continued from page 18)

4.0 System Overview

The BCRTM can be configured for a variety of processor and memory environments. The host processor and the BCRTM communicate via a flexible, programmable interrupt structure, internal registers, and a user-definable shared memory area. The shared memory area (up to 64K) is completely user-programmable and communicates BCRTM control information -- message data, and status/error information.

Built-in memory management functions designed specifically for MIL-STD-1553B applications aid processor off-loading. The host needs only to establish the parameters within memory so the BCRTM can access this information as required. For example, in the RT mode, the BCRTM can store data associated with individual subaddresses anywhere within its 64K address space. The BCRTM then can automatically buffer up to 128 incoming messages of the same subaddress, thus preventing the previous messages from being overwritten by subsequent messages. This buffering also extends the intervals required by the host processor to service the data. Selecting an appropriate MCLK frequency to meet system memory access time requirements controls the memory access rate. The completion of a user-defined task or the occurrence of a user-selected event is indicated by using the extensive set of interrupts provided.

In the BC mode, the BCRTM can process multiple messages, assist in scheduling message lists, and provide host-programmable functions such as auto retry. The BCRTM is incorporated in systems with a variety of interrupt latencies by using the Interrupt History List feature (see Exception Handling and Interrupt Logging, page 37). The Interrupt History List sequentially stores the events that caused the interrupt in memory without losing information if a host processor does not respond immediately to an interrupt.

In the Monitor (M) mode, the BCRTM's powerful linked list command block structure allows it to process a series of monitored 1553 messages without the intervention of the host. The BCRTM can store as much bus traffic as can be contained in its 64K memory space. In addition, the host has the capability of instructing the BCRTM to monitor and store data for only selected remote terminals. The host system is responsible for initializing an area in memory that tells the BCRTM where to store command word information and data for each command that the BCRTM receives on the 1553 bus. This area of memory consists of "Bus Monitor Command Blocks." An M Command Block is very similar to the BC Command Block in the BCRTM. The only real differences are the direction of information flow, and that there is no Head Pointer in the M Command Block.

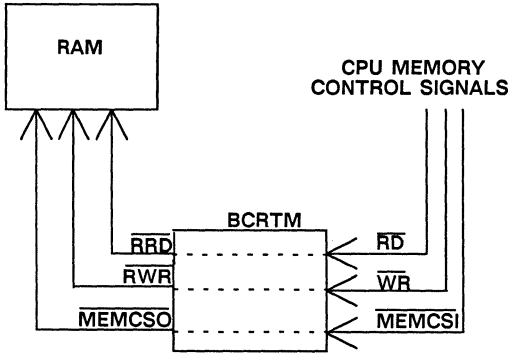


Figure 3a. Pseudo-Dual-Port RAM Control Signals

5.0 System Interface

5.1 DMA Transfers

The BCRTM initiates DMA transfers whenever it executes command blocks (BC mode) or services commands (RT mode). $\overline{\text{DMAR}}$ initiates the transfer and is terminated by the inactive edge of $\overline{\text{DMACK}}$. The Address Enable (AEN) input enables the BCRTM to output an address onto the Address bus.

The BCRTM requests transfer cycles by asserting the $\overline{\text{DMAR}}$ output, and initiates them when a $\overline{\text{DMAG}}$ input is received. A $\overline{\text{DMACK}}$ output indicates that the BCRTM has control of the Data and Address buses. The $\overline{\text{TSCTL}}$ output is asserted when the BCRTM is actually asserting the Address and Data buses.

To support using multiple bus masters in a system, the BCRTM outputs the $\overline{\text{DMAGO}}$ signal that results from the $\overline{\text{DMAG}}$ signal passing through the chip when a BCRTM bus request was not generated ($\overline{\text{DMAR}}$ inactive). You can use $\overline{\text{DMAGO}}$ in daisy-chained multimaster systems.

5.2 Hardware Interface

The BCRTM provides a simple subsystem interface and facilitates DMA arbitration. The user can configure the BCRTM to operate in a variety of memory-processor environments including pseudo-dual-port RAM and standard DMA configurations.

For complete circuit description, such as arbitration logic and I/O, please refer to the appropriate application note.

5.3 CPU Interconnection

Pseudo-Dual-Port RAM Configuration

The BCRTM's Address and Data buses connect directly to RAM, with buffers isolating the BCRTM's buses from those of the host CPU (figures 3a and 3b). The CPU's memory control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{MEMCSI}$) pass through the BCRTM and connect to memory as $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$.

Standard DMA Configuration

The BCRTM's and CPU's data, address, and control signals are connected to each other as shown in figures 3c and 3d. The $\overline{RWR}$, $\overline{RRD}$, and $\overline{MEMCSO}$ are activated after $\overline{DMAG}$ is asserted.

In either case, the BCRTM's Address and Data busses remain in a high-impedance state unless the $\overline{CS}$ and $\overline{RD}$ signals are active, indicating a host register access; or $\overline{TSCTL}$ is asserted, indicating a memory access by the BCRTM. CPU attempts to access BCRTM registers are ignored during BCRTM memory access. Inhibit DMA transfers by using the Busy function in the Remote Terminal Address Register while operating in the Remote Terminal mode.

The designer can use $\overline{TSCTL}$ to indicate when the BCRTM is accessing memory or when the CPU can access memory. AEN is also available (use is optional), giving the CPU control over the BCRTM's Address bus. A DMA Burst (BURST) signal indicates multiple DMA accesses.

Register Access

Registers 0 through 13 are accessed with the decode of the four LSBs of the Address bus (A0-A3) and asserting $\overline{CS}$. Pulse either $\overline{RD}$ or $\overline{WR}$ for multiple register accesses.

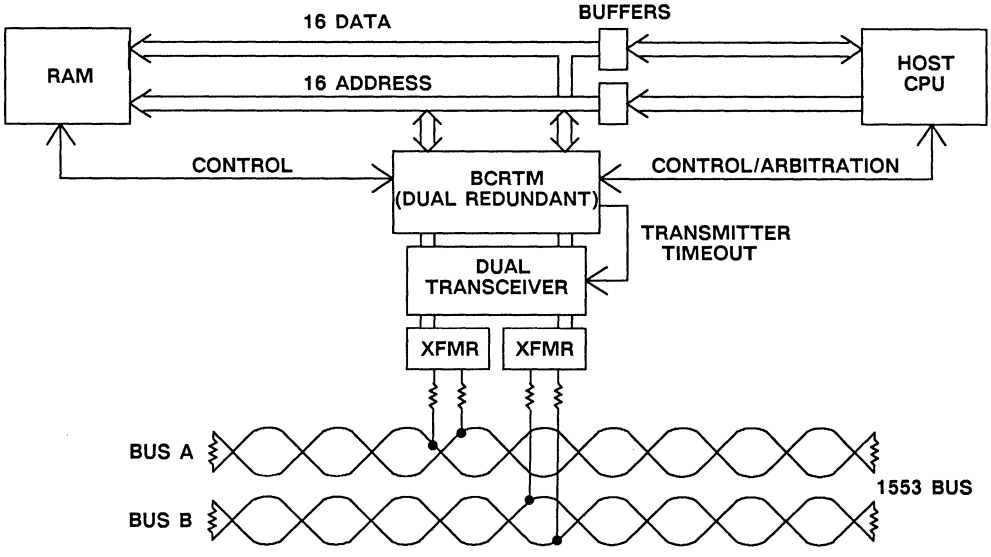


Figure 3b. CPU/BCRTM Interface -- Pseudo-Dual-Post RAM Configuration

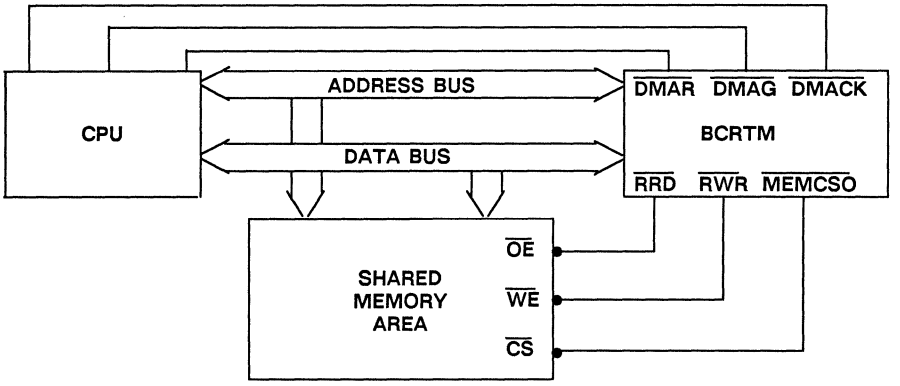


Figure 3c. DMA Signals

5.4 RAM Interface

The BCRTM's $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ signals serve as read and write controls during BCRTM memory accesses. The host subsystem signals $\overline{RD}$, $\overline{WR}$, and $\overline{MEMCSI}$ propagate through the BCRTM to become $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ outputs to support a pseudo-dual-port. During BCRTM-RAM data transfers, the host subsystem's memory signals are ignored until the BCRTM access is complete.

5.5 Transmitter/Receiver Interface

The BCRTM's Manchester II encoder/decoder interfaces directly with the 1553 bus transceiver, using the TAO-TAZ and RAZ-RAO signals for Channel A, and TBO-TBZ and RBZ-RBO signals for Channel B.

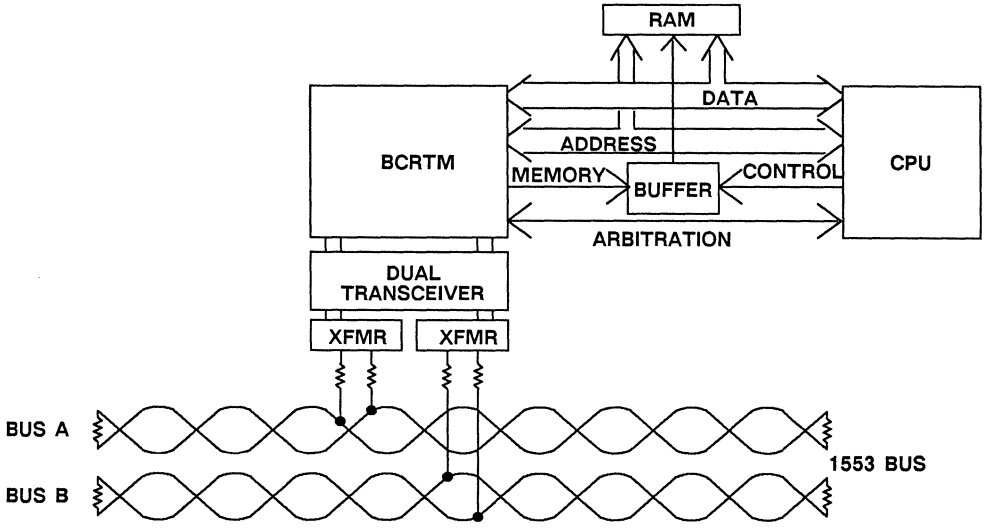


Figure 3d. CPU/BCRTM Interface -- DMA Configuration

The BCRTM also provides a $\overline{\text{TIMERON}}$ signal output and an active channel output indicator (CHA/$\overline{\text{B}}$) to assist in meeting the MIL-STD-1553B fail-safe timer requirements (see figure 4).

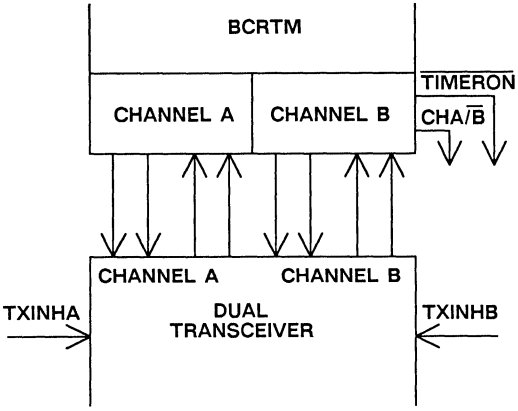


Figure 4. Dual-Channel Transceiver

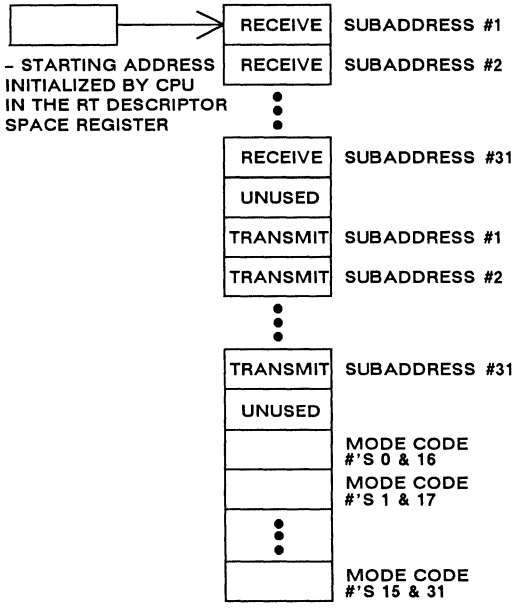


Figure 5. Descriptor Space

6.0 Remote Terminal Architecture

The Remote Terminal architecture is a descriptor-based configuration of relevant parameters. It is composed of an RT Descriptor Space (see figure 5) and internal, host-programmable registers. The Descriptor Space contains only descriptors. Descriptors contain programmable subaddress parameters relating to handling message transfers. Each descriptor consists of four words: (1) a Control Word, (2) a Message Status List Pointer, (3) a Data List Pointer, and (4) an unused fourth word (see figure 6.) These words indicate how to perform the data transfers associated with the designated subaddress.

A receive descriptor and a transmit descriptor are associated with each subaddress. The descriptors reside in memory and are listed sequentially by subaddress. By using the index within the descriptor, the BCRTM can buffer incoming and outgoing messages, which reduces host CPU overhead. This message buffering also reduces the risk of incoming messages being overwritten by subsequent incoming messages.

Each descriptor contains a programmable interrupt structure for subsystem notification of user-selected message transfers and indicates when the message buffers are full. Illegalizing subaddresses, in normal and broadcast modes, is accomplished by using programmable bits within the descriptor (see the RT Functional Operation section on next page).

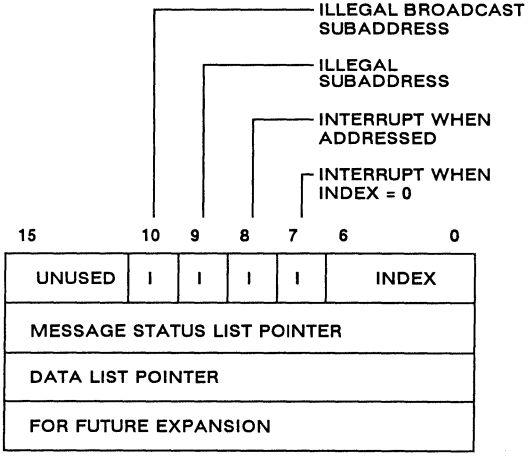


Figure 6. Remote Terminal Subaddress Descriptor

Message Status information -- including word count, an internally generated time tag, and broadcast and message validity information -- is provided for each message. The Message Status Words are stored in a separate Message Status Word list according to subaddress. The list's starting locations are programmable within the descriptor.

Message data, received or transmitted, is also stored in lists. The message capacity of the lists and the lists' locations are user selectable within the descriptor.

6.1 RT Functional Operation

The RT off-loads the host computer of all routine data transfers involved with message transfers over the 1553B bus by providing a wide range of user-programmable functions. These functions make the BCRTM's operation flexible for a variety of applications. The following paragraphs give each function's operational descriptions.

6.1.1 RT Subaddress Descriptor Definition

The host sets words within the descriptor (see figure 6, page 23). The BCRTM then reads the descriptor words when servicing a command corresponding to the specified descriptor. All bit-selectable functions are active high and inhibited when low.

A. Control Word. The first word in the descriptor, the Control Word, selects or disables message transfers and selects an index.

Bit Number	Description
BITs 15-11	Reserved.
BIT 10	Illegal Broadcast Subaddress. Indicates to the BCRTM not to access this subaddress using broadcast commands. The Message Error bit in the status word is set if the illegal broadcast subaddress is addressed. Since transmit commands do not apply to broadcast, this bit applies only to receive commands.
BIT 9	Illegal Subaddress. Set by the host CPU, it indicates to the BCRTM that a command with this subaddress is illegal. If a command uses an illegal subaddress the Message Error bit in the 1553 status word is set. The Illegal Command Interrupt is also asserted if enabled.
BIT 8	Interrupt Upon Valid Command Received. Indicates that the BCRTM is to assert an interrupt every time a command addresses this descriptor. The interrupt occurs just prior to post-command descriptor updating.
BIT 7	Interrupt When Index = 0. Indicates that the BCRTM initiates an interrupt when the index is decremented to zero.
BITs 6-0	Index. These bits are for indexed message buffering. Indexing means transacting a pre-specified number of messages before notifying the host CPU. After each message transaction, the BCRTM decrements the index by one until index = 0. Note that the index is decremented for messages that contain message errors.

B. Message Status List Pointer. The host sets the Message Status List Pointer, the second word within the descriptor, and the BCRTM uses it as a starting address for the Message Status List. It is incremented by one with each Message Status Word write. If the Control Word Index is already equal to zero, the Message Status List Pointer is not incremented and the previous Message Status Word is overwritten.
Note: A Message Status Word is also written and the pointer is incremented when the BCRTM detects a message error.

C. Data List Pointer. The Data List Pointer is the third word within the descriptor. The BCRTM stores data in RAM beginning at the address indicated by the Data List Pointer. The Data List Pointer is updated at the end of each successful message with the next message's starting address with the following exceptions:

- If the message is erroneous, the Data List Pointer is not updated. The next message overwrites any data corresponding to the erroneous message.
- Upon receiving a message, if the index is already equal to zero, the Data List Pointer is not incremented and data from the previous message is overwritten.

D. Reserved. The fourth descriptor word is reserved for future use.

6.1.2 Message Status Word

Each message the BCRTM transacts has a corresponding Message Status Word, which is pointed to by the Message Status List Pointer of the Descriptor. This word allows the host CPU to evaluate the message's validity, determine the word count, and calculate the approximate time frame in which the message was transacted (figures 7 and 8).

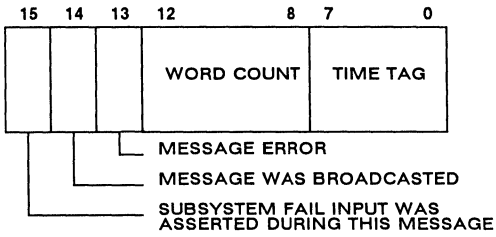


Figure 7. Message Status Word

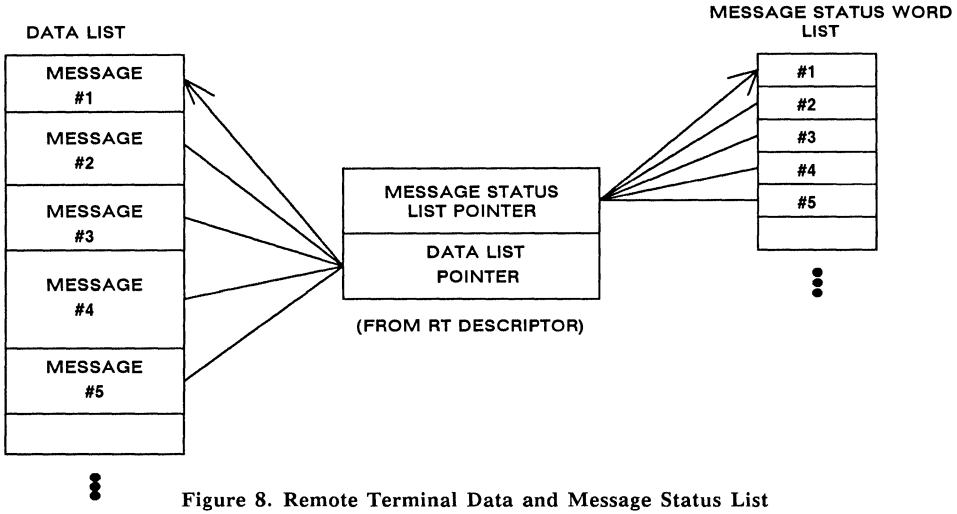


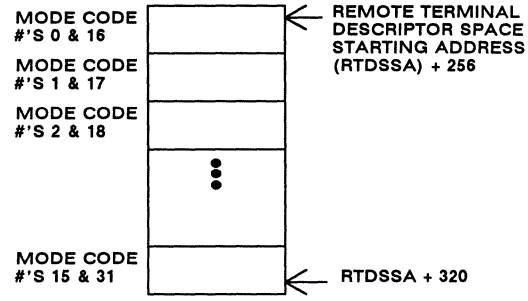
Figure 8. Remote Terminal Data and Message Status List

Message Status Word Definition

Bit Number	Description
BIT 15	Subsystem Failed. Indicates SSYSF was asserted before the Message Status Word transfer to memory. This bit is also set when the user sets bit 13 of Register 10.
BIT 14	Broadcast Message. Indicates that the corresponding message was received in the broadcast mode.
BIT 13	Message Error. Indicates a message is invalid due to improper synchronization, bit count, word count, Manchester error.
BITs 12-8	Word Count. Indicates the number of words in the message and reflects the Word Count field in the command word. Should the message contain a different number of words than the Word Count field, the Message Error flag is triggered. If there are too many words, they are withheld from RAM. If the actual word count is less than or grater than it should be, the Message Error bit in the 1553 status word is set.
BITs 7-0	Time Tag. The BCRTM writes the internally generated Time Tag to this location after message completion. The resolution is 64 microseconds. (See Register 13). If the timer reads 2, it indicates the message was completed 128 to 191 microseconds after the timer started.

6.1.3 Mode Code Descriptor Definition

Mode codes are handled similarly to subaddress transactions. Both use the four-word descriptors residing in the RT descriptor space to allow the host to program their operational mode. Corresponding to each mode code is a descriptor (see figure 9a). Of the 32 address combinations for mode codes in MIL-STD-1553B, some are clearly defined functions while others are reserved for future use. Sixteen descriptors are used for mode code operations with each descriptor handling two mode codes: one mode code with an associated data word and one mode code without an associated data word. All mode codes are handled in accordance with MIL-STD-1553B. The function of the first word of the Mode Code Descriptor is similar to that of the Subaddress Descriptor and is defined below. The remaining three words serve the same purpose as in the Subaddress Descriptor.



Note:
Mode code descriptor blocks are also provided for reserved mode codes but have no associated predefined BCRTM operation.

Figure 9a. (RT) Mode Code Descriptor Space

Control Word

Bit Number	Description
BIT 15	Interrupt on Reception of Mode Code (without Data Word).
BIT 14	Illegalize Broadcast Mode Code (without Data Word).
BIT 13	Illegalize Mode Code (without Data Word).
BIT 12	Reserved.
BIT 11	Illegalize Broadcast Mode Code (with Data Word).
BIT 10	Illegalize Transmit Mode Code (with Data Word).
BIT 9	Illegalize Receive Mode Code (with Data Word).
BIT 8	Interrupt on Reception of Mode Code (with Data Word).
BIT 7	Interrupt if Index = 0.
BITs 6-0	Index. Functionally equivalent to the index described in the Subaddress Descriptor. It applies to mode codes with data words only.

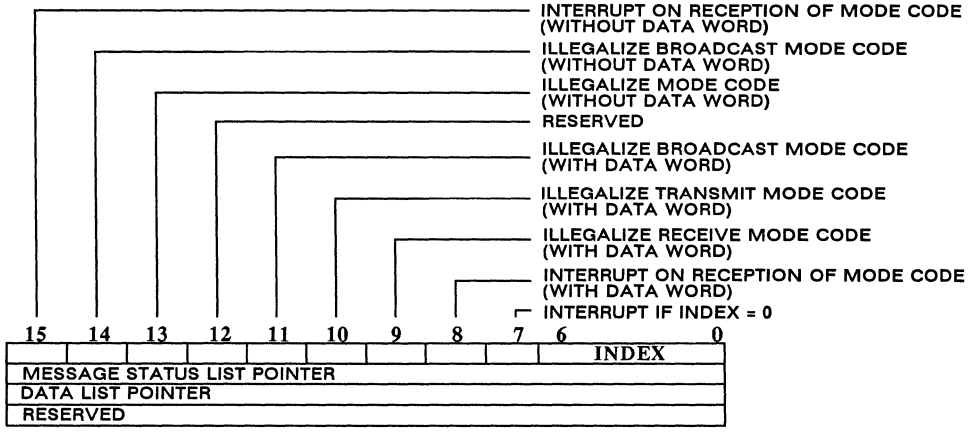


Figure 9b. (RT) Mode Code Descriptor

The descriptors, numbered sequentially from 0 to 15, correspond to mode codes 0 to 15 without data words and mode codes 16 to 31 with data words. For example, mode codes 0 and 16 correspond to descriptor 0 and mode codes 1 and 17 correspond to descriptor 1. The Mode Code Descriptor Space is appended to the Subaddress Descriptor Space starting at 0100H (256D) of the 320-word RT Descriptor Space (see figure 5).

The BCRTM autonomously supports all mode codes without data words by executing the specific function and transmitting the 1553 status word. The subsystem provides the data word for mode codes with data words (see the Data List Pointer section). For all mode codes, an interrupt can be asserted upon successful completion of the mode command by setting the appropriate bit in the control word (see figure 9b).

Dynamic Bus Control #00000
This mode code is accepted automatically if the Dynamic Bus Control Enable bit in the Remote Terminal Address Register is set. Setting the Dynamic Bus Control Acceptance bit in the 1553 status word and BCRTM Status Register confirms the mode code acceptance. A High-Priority Interrupt is also asserted if enabled. If the Dynamic Bus Control Enable bit is not set, the BCRTM does not accept Dynamic Bus Control.

Synchronize (Without Data Word) #00001
If enabled in the Mode Code #00001 Descriptor Control Word, the BCRTM asserts an interrupt when this mode code is received.

Transmit Status Word #00010
The BCRTM automatically transmits the 1553 status word corresponding to the last message transacted.

Initiate Self-Test #00011
The BCRTM automatically starts its BIT routine. An interrupt, if enabled, is asserted when the test is completed. The BIT Word Register and external pin BCRTF are updated when the test is completed. A failure in BIT will also set the TF status word bit.

Transmitter Shutdown #00100
The BCRTM disables the channel opposite the channel on which the command was received.

Override Transmitter Shutdown #00101
The BCRTM enables the channel previously disabled.

Inhibit Terminal Flag Bit #00110
The BCRTM inhibits the Terminal Flag from being set in the status word.

Override Inhibit Terminal Flag Bit #00111
The BCRTM disables the Terminal Flag inhibit.

Reset Remote Terminal #01000
The BCRTM automatically resets the encoder, decoders, and protocol logic.

Transmit Vector Word #10000
The BCRTM transmits the vector word from the location addressed by the Data List Pointer in the Mode Code Descriptor Block.

Synchronize (with Data Word) #10001
On receiving this mode code, the BCRTM simply stores the associated data word.

Transmit Last Command #10010
The BCRTM transmits the last command executed and the corresponding 1553 status word.

Transmit BIT Word #10011
The BCRTM transmits BIT information from the BIT Register.

Selected Transmitter Shutdown #10100
On receiving this mode code, the BCRTM simply stores the associated data word.

Override Selected Transmitter Shutdown #10101
On receiving this mode code, the BCRTM simply stores the associated data word.

Mode codes 9-15 and 22-31 are reserved for future expansion of MIL-STD-1553B.

6.2 RT Error Detection

In accordance with MIL-STD-1553B, the remote terminal handles superseding commands on the same or opposite bus. When receiving, the remote terminal performs a response time-out function of 56 microseconds for RT-RT transfers. If the response time-out condition occurs, a Message Error bit is set in the 1553 status word and in the Message Status Word. Error checking occurs on both of the Manchester logic and the word formats. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

6.3 RT Operational Sequence

The following is a general description of the typical behavior of the BCRTM as it processes a message in the RT mode. It is assumed that the user has already written a "1" to Register 0, bit 0, enabling RT operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active

- DMA Descriptor Read. After receiving a valid command, the BCRTM initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read
  Message Status List Pointer read
  Data List Pointer read

Data Transmitted/Received.

- Data Word DMA.

  If the BCRTM needs to transmit data from memory, it initiates a DMA cycle for each Data Word shortly before the Data Word is needed on the 1553B bus:

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

  If the BCRTM receives data, it writes each Data Word to memory after the Data Word is received:

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Status Word Transmission.

The BCRTM automatically transmits the Status Word as defined in MIL-STD-1553B. The Message Error and Broadcast Command Received bits are generated internally. Writing to Register 10 enables the other predefined bits. For illegalized commands, the BCRTM sets the Message Error Bit in the 1553 Status Word.

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
RT Descriptor Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

- Descriptor Write.

After the BCRTM processes the message, a final DMA burst occurs to update the descriptor block, if necessary:

DMA arbitration (BURST)
Message Status Word write
Data List Pointer write
(incremented by word count)
Message Status List Pointer write
(incremented by 1)
Control Word write (index decremented)

Note the following exceptions:

Mode codes without data require no descriptor update.

Predefined mode codes (18 and 19) which do not require access to memory for the data word, do not involve updating the Data List Pointer.

Messages with errors prevent updates to the Data List Pointer.

If the message index was zero, neither the Message Status List Pointer nor the Data List Pointer is updated.

7.0 Bus Controller Architecture

The BCRTM's bus controller architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553B bus has an associated Command Block, which the CPU sets up (see figures 10 and 11). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts. This memory interface system is flexible due to a doubly-linked list data structure.

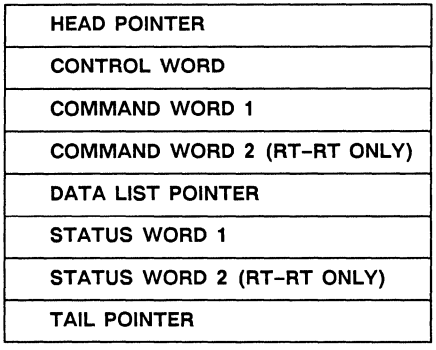


Figure 10. Command Block

In a doubly-linked Command Block structure, pointers delimit each Command Block to the previous and successive blocks (see figure 12). The linking feature eases multiple message processing tasks and supports message scheduling because of its ability to loop through a series of transfers at a predetermined cycle time. A data pointer in the command allows efficient space allocation because data blocks only have to be configured to the exact word count used in the message. Data pointers also provide flexibility in data-bank switching.

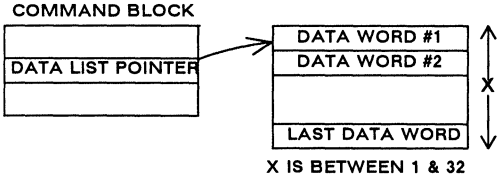


Figure 11. Data Placement

A control word with bit-programmable functions and a Message Error bit are in each Command Block. This allows selecting individual functions for each message and provides message validity information. The BCRTM's register set provides additional global parameters and address pointers.

A programmable auto retry function is selectable from the control word and Control Register.

The auto retry can be activated when any of the following occurs:

- Busy Bit set in the status word
- Message Error (indicated by the RT status response)
- Response Time-Out
- Message Error detected by the Bus Controller

One to four retries are programmable on the same or opposite bus.

The Bus Controller also has a programmable intermessage delay timer that facilitates message transfer scheduling (see figures 13 and 14). This timer, programmed in the control word, automatically delays between the start of two successive commands.

A polling function is also provided. The Bus Controller, when programmed, compares incoming status words to a host-specified status word and generates an interrupt if the comparison indicates any matching bits. An Interrupt and Continue function facilitates the host subsystem's synchronization by generating an interrupt when the specified Command Block's message is executed.

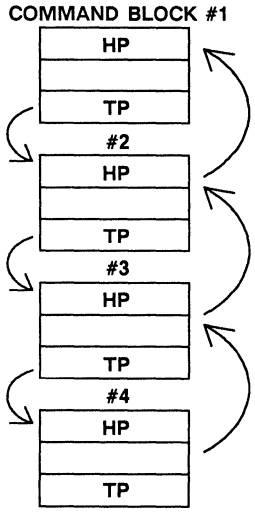


Figure 12. Command Block Chaining

7.1 BC Functional Operation

The Bus Controller off-loads the host computer of many functions needed to coordinate 1553B bus data transfers. Special architectural features provide message-by-message flexibility. In addition, a programmable interrupt scheme, programmable intermessage timing delays, and internal registers enhance the BCRTM's operation.

The host determines the first Command Block by setting the initial starting address in the current Command Block Register. Once set, the BCRTM updates the current Command Block register with the next Command Block Address. The BCRTM then executes the sequential Command Blocks and counts out message delays (where programmed) until it encounters the last Command Block listed (indicated by the End of List bit in the control word). Interrupts are asserted when enabled events occur (see the Exception Handling and Interrupt Logging section, page 37).

The functions and their programming instructions are described below. The registers also contain many programmable functions and function parameters.

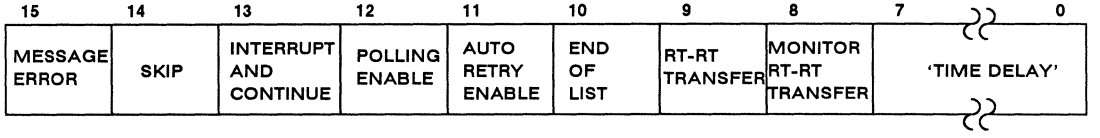


Figure 13. Control Word

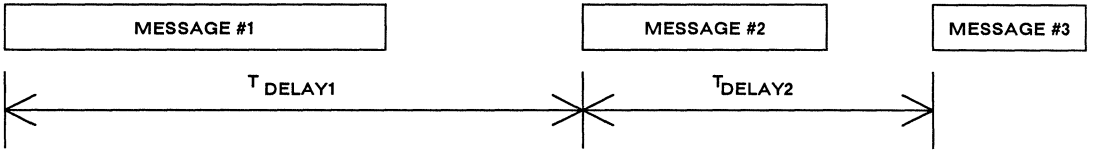


Figure 14. BC Timing Delays

BC Command Block Definition
Each Command Block contains (see figure 10):

A. Head Pointer. Host-written, this location can contain the address of the previous Command Block's Head Pointer. The BCRTM does not access this location.

B. Control Word. Host-written, the Control Word contains bit-selectable options and a Message Error bit the BCRTM provides (see figure 13). The bit definitions follow.

Bit Number	Description
BIT 15	Message Error. The BCRTM sets this bit when it detects an invalid RT response as defined in MIL-STD-1553B.
BIT 14	Skip. When set, this bit instructs the BCRTM to skip this Command Block and execute the next.
BIT 13	Interrupt and Continue. If set, a Standard Interrupt is asserted when this block is addressed; operation, however, continues. Note that this interrupt must also be enabled by setting bit 0 of Register 9.
BIT 12	Polling Enable. Enables the BCRTM's polling operation.
BIT 11	Auto Retry Enable. When set, the Auto Retry function, governed by the global parameters in the Control Register, is enabled for this message.
BIT 10	End of List. Set by the CPU, this bit indicates that the BCRTMP, upon completion of the current message, will halt and assert a High-Priority Interrupt. The interrupt must also be enabled in the High-Priority Interrupt Enable Register.
BIT 9	RT-RT. Set by the CPU, this indicates that this Command Block transacts an RT-RT transfer.
BIT 8	Monitor RT-RT Transfer. Set by the CPU, this function indicates that the BCRTM should receive and store the message beginning at the location indicated by the data pointer.
BITs 7-0	Time Delay. The CPU sets this field, which causes the BCRTM to delay the specified time between sequential message starts (see figures 13 and 14). Regardless of the value in the Time Delay field (including zero), the BCRTM will at least meet the minimum 4 μs intermessage gap time as specified in MIL-STD-1553B. The timer is enabled by having a non-zero value in this bit field. When using this function, please note: • Timer resolution is 16 microseconds. As an example, if a given message requires 116 μs to complete (including the minimum 4 μs intermessage gap time) the value in the Time Delay field must be at least 00001000 (8 x 16 μs = 128 μs) to provide an intermessage gap greater than the 4 μs minimum requirement. • If the timer is enabled and the Skip bit is set, the timer provides the programmed delay before proceeding. • If the message duration exceeds the timer delay, the message is completed just as if the timer were not enabled. • If SKIP = 1 and EOL = 1, the $\overline{\text{HPINT}}$ is generated if enabled. • If SKIP = 1 and Interrupt and Continue = 1, the $\overline{\text{STDINT}}$ is generated if enabled.

C. Command Word One. Initialized by the CPU, this location contains the first command word corresponding to the Command Block's message transfer.

D. Command Word Two. Initialized by the CPU, this location is for the second (transmit) command word in RT-RT transfers. In messages involving only one RT, the location is unused.

E. Data Pointer. Initialized by the CPU, this location contains the starting location in RAM for the command block's message (see figure 15).

F. Status Word One. Stored by the BCRTM, this location contains the entire Remote Terminal status response.

G. Status Word Two. Stored by the BCRTM, this location contains the receiving Remote Terminal status word. For transfers involving one Remote Terminal, the location is unused.

H. Tail Pointer. Initialized by the host CPU, the Tail Pointer contains the next Command Block's starting address.

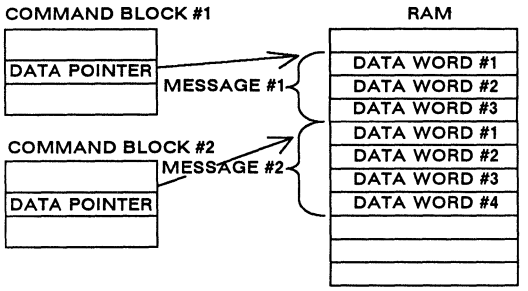


Figure 15. Contiguous Data Storage

7.2 Polling

During a typical polling scenario (see figure 16) the Bus Controller interrogates remote terminals by requesting them to transmit their status words. This feature can also alert the host if a bit is set in any RT status word response during normal message transactions. The BCRTM enables the host to initialize a chain of Command Blocks with the command word's Polling Enable bit. A programmable Polling Compare Register (PCR) is provided. In the polling mode, the Remote Terminal response is compared to the Polling Compare Register contents. Program the PCR by setting the PCR bits corresponding to the RT's 1553 status word bits to be compared. If they match (i.e., two 1's in the same bit position) then, if enabled in both the BC Command Block Control Word and in the Standard Interrupt Enable Register (Register 9), a polling comparison interrupt is generated.

Example 1. No bit match is present

PCR	00000000001
RT's 1553 status word response	00000100010
Result	No Polling Comparison Interrupt

Example 2. Bit match is present

PCR	00100100000
RT's 1553 status word response	00000100000
Result	Polling Comparison Interrupt

7.3 BC Error Detection

The Bus Controller checks for errors (see the Exception Handling and Interrupt Logging and the RT Error Detection sections, pages 37 and 28) on each message transaction. In addition, the BC compares the RT command word addresses to the incoming status word addresses. The BC monitors for response time-out and checks data and control words for proper format according to MIL-STD-1553B. Illogical commands include incorrectly formatted RT-RT Command Blocks.

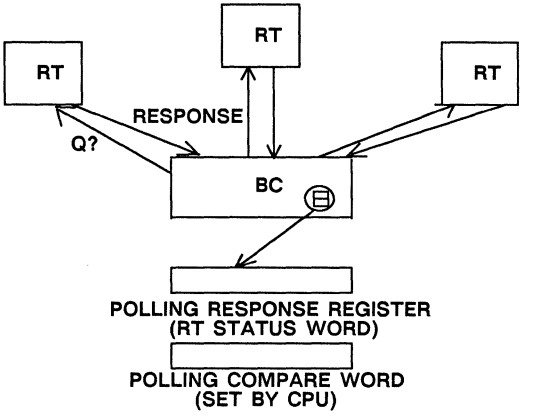


Figure 16. Polling Operation

7.4 Bus Controller Operational Sequence

The following is a general description of the typical behavior of the BCRTM as it processes a message in the BC mode.

The user starts BC operation by writing a "1" to Register 0, Bit 0.

- Command Block DMA - the following occurs immediately after Bus Controller startup:

  DMA arbitration (BURST)
  Control Word read
  Command Word 1 read (from third location of Command Block)
  Data List Pointer read

A. For BC-to-RT Command Blocks:

The BCRTM transmits the Command Word.

- Data Word DMA

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

The BCRTM transmits the Data Word. Data Word DMAs and transmissions continue until all Data Words are transmitted.

- Status Word DMA

The BCRTM receives the RT Status Word.

DMA arbitration
Status Word write (to sixth location of Command Block)

B. For RT-to-BC Command Blocks:

The BCRTM transmits the Command Word.

- Status Word DMA

The BCRTM receives the RT Status Word.

DMA arbitration
Status Word write (to sixth location of Command Block)

The BCRTM receives the first Data Word.

- Data Word DMA

DMA arbitration
Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

C. For RT(B)-to-RT(A) Command Blocks:

The BCRTM transmits Command Word 1 to RT(B).

- Command Word 2 DMA

DMA arbitration
Command Word 2 read (from fourth location of Command Block)

The BCRTM transmits Command Word 2 to RT(A).

The BCRTM receives the RT Status Word from RT(A).

- Status Word DMA for RT(A) Status Word

DMA arbitration
Status Word write (to sixth location of Command Block)

The BCRTM receives the first Data Word

- Data Word DMA (only if the BCRTM is enabled to monitor the RT-to-RT message).

DMA arbitration
Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

The BCRTM receives the RT Status Word from RT(B).

- Status Word DMA for RT(B) Status Word

DMA arbitration
Status Word write (to seventh location of Command Block)

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
Command Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

If Retries are enabled and a Retry condition occurs, the following DMA occurs:

DMA arbitration (BURST)
Control Word read
Command Word 1 read (from third location of Command Block)
Data List Pointer read

The BCRTM proceeds from the current Command Block to the next successive Command Block.

- If no Message Error has occurred during the current Command Block, the following occurs:

DMA arbitration (BURST)
Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
DMA hold cycle
Control Word read (next Command Block)
Command Word 1 read (next Command Block)
Data List Pointer read

- If the BCRTM detects a Message Error while processing the current Command Block, the following occurs:

DMA arbitration (BURST)
Control Word write
Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
DMA hold cycle
Control Word read (next Command Block)
Command Word 1 read (next Command Block)
Data List Pointer read

The BCRTM proceeds again from point A, B, or C as shown above.

7.5 BC Operational Example (see figure 22 on page 39)
The BCRTM is programmed initially to accomplish the following:

The first Command Block is for a four-word RT-RT transfer with the BCRTM monitoring the transfer and storing the data.

- Auto-retry is enabled on the opposite bus using only one retry attempt, if the incoming Status Word is received with the Message Error bit set.
- Wait for a time delay of 400 microseconds before proceeding to the next Command Block.
- The Data List Pointer contains the address 0400H.

The second Command Block is for a BC-RT transfer of two words.

- The End of List bit is set in its Control Word.
- The Data List Pointer contains the address 0404H.
- The Polling Enable bit is set and the Polling Compare Register contains a one in the Subsystem Fail position (Bit 2).

Then:

A. The CPU initializes all the appropriate registers and Command Blocks, and issues a Start Enable by writing a "1" to Register 0, Bit 0.

B. The BCRTM, through executing a DMA cycle, reads the Control Word, Command Words, and the Data List Pointer. The delay timer starts and message execution begins by transmitting the receive and transmit commands stored in the Command Blocks. The BCRTM then waits to receive the Status Word back from the transmitting RT.

C. The BCRTM receives the RT Status Word with all status bits low from the transmitting RT and stores the Status Word in Command Block 1. The incoming data words from the transmitting RT follow. The BCRTM stores them in memory locations 0400H - 0403H.

   If the Status Word indicates that the message cannot be transmitted (Message Error), the response time-out clock counts to zero and the allotted message time runs out. An auto-retry can be initiated if programmed to do so. Nevertheless, the ME bit in the Control Word is set.

D. The BCRTM receives the Status Word response from the receiving RT. The ME bit in the Status Word is set, indicating the message is invalid. The BCRTM initiates the auto retry function, (as programmed) on the alternate bus, re-transmits the Command Words, receives the correct Status Word, and stores the data again in locations 0400H - 0403H. This time the Status Word response from the receiving RT indicates the message transfer is successful.

E. The timer delay between the two successive transactions counts down another 135 microseconds before proceeding. This is determined as follows:

   The message transaction time is approximately 130 microseconds (the only approximation is due to the range in status response and intermessage gap times specified by MIL-STD-1553B). Approximating that with the retry, the total duration for the two attempts is 265 microseconds.

F. The BCRTM reads the Tail Pointer of Command Block 1 and places it in the Current Command Register. It also reads the Control Word, Command Word, and Data List Pointer, and the first data word in the second Command Block.

G. Since this is a BC-RT transfer, the BCRTM transmits the receive command followed by two data words from locations 0404H - 0405H in memory. The BCRTM reads the second data word from memory while transmitting the first.

H. The BCRTM receives the status response from the RT. In this case, the Status Word indicates, by the ME bit being low, that the message is valid. The Status Word also has the Subsystem Fail bit set.

I. The Status Word is stored in the Command Block. The BCRTM, having encountered the end of the list, halts message transactions and waits for another start signal.

J. The BCRTM asserts a High-Priority Interrupt indicating the end of the command list. Due to the polling comparison match, the BCRTM also asserts a Standard Priority Interrupt and logs the event in the Interrupt Log List.

8.0 Bus Monitor Architecture

The BCRTM's bus monitor architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553B bus (for a monitored RT address) has an associated Command Block, which the CPU sets up (see figures 17 and 18). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts.

MONITOR CONTROL/STATUS
1553 COMMAND WORD 1
1553 COMMAND WORD 2
DATA LIST POINTER
1553 STATUS WORD 1
1553 STATUS WORD 2
TAIL POINTER

Figure 17. BCRTM Bus Monitor Command Block

In a linked list Command Block structure, pointers delimit each Command Block to the successive block (see figure 19). A data pointer in the Command Block allows efficient space allocation because data blocks do not have to be placed contiguously in memory.

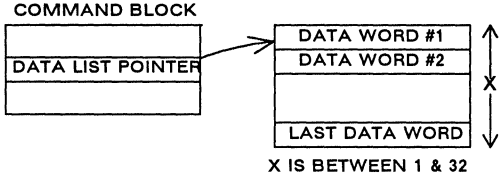


Figure 18. Data Placement

A Monitor control/status word with an eight-bit Time Tag, an Interrupt When Addressed bit, a Message Error bit, and a Command Block Activated bit are in each Monitor Command Block. The user can access these control/status words to determine which Monitor Command Block was last utilized. Also, by selecting the Interrupt When Addressed feature that is available for each Command Block, the host can determine when particular remote terminal activity has occurred.

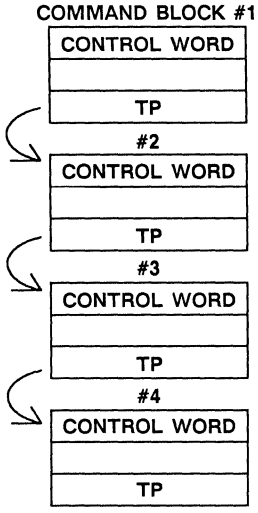


Figure 19. Monitor Command Block Tail Pointers

8.1 Monitor Functional Operation

The Bus Monitor function is a register-selectable mode of operation. The host uses Registers 14, 16, and 17 in conjunction with Register 0 to program the BCRTM to monitor any combination of remote terminals or all of the remote terminals.

The BCRTM's memory management scheme gives the host a great deal of flexibility for processing 1553 bus data and is compatible with many bus monitoring applications. The host CPU is responsible for initializing the Monitor control/status word, the Data Pointer, and the Tail Pointer in each of the Monitor Control Blocks. The Monitor structure is analogous to the Bus Controller Command Block scheme. The only real difference is the direction of information flow.

The number of Monitor Control Blocks that the host initializes depends on the data latency requirements for post-processing of 1553 commands. The linked list of Command Blocks could be connected in a loop fashion, with the BCRTM accessing the loop at one point and the host CPU processing the message behind that point. The bit positions of the BM control/status word are defined as shown in figure 20.

15	14	13	12	11	10	9	8
CBA	ME	IOA	BA/B	X	X	X	X
7	6	5	4	3	2	1	0
TT7	TT6	TT5	TT4	TT3	TT2	TT1	TT0

B0 - B7 Time Tag (64 μs resolution)
B8 - B11 Not used
B12 - Bus A/B: Defines which of the dual redundant 1553 buses on which the BCRTM received this message.
B13 - IWA: Interrupt When Addressed. The BCRTM issues a standard priority interrupt when the host accesses this Bus Monitor Command Block.
B14 - ME: Message Error. The BCRTM sets this bit if a 1553 message error oc curred while receiving this message.
B15 - CBA: Command Block Activated. The BCRTM sets this bit when this Bus Monitor Command Block is accessed by the BCRTM.

Figure 20. Bus Monitor Control/Status Word

8.2 Monitor Error Detection

In the Monitor mode, the BCRTM checks all monitored messages for errors. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

Due to the nature of the 1553 protocol, it can be very difficult for any monitoring device to interpret some types of errors on the 1553 bus. For example, suppose an RT (whose RT Address the BCRTM is monitoring) incorrectly responds to a Broadcast command. The BCRTM, which is not receiving or transmitting the message, cannot distinguish between the erroneous status word and a new command sent from the Bus Controller, since the status sync is identical to the command sync. In this case, the BCRTM will put the extra status word in a new Monitor Command Block, and then report a Message Error due to the incorrect protocol on the erroneously interpreted status word the RT transmitted.

8.3 Monitor Operational Sequence

The following is a general description of the operation of the BCRTM as it processes a monitored BC-to-RT message in the Monitor mode. DMA operations will vary slightly depending on the type of message (i.e., RT-to-BC, RT-to-RT, etc.). It is assumed that the user has already written a "1" to Register 0, bit 0, and all other registers are in the appropriate state to enable Monitor operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active.

- DMA Monitor Command Block Read. After receiving a valid command, the BCRTM initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read
  Command Word write
  Data List Pointer read

Data Received.

- Data Word DMA

  The BCRTM initiates a DMA cycle for each Data Word to store the data in memory, whether the command was a transmit or receive command to any valid monitored RT Address.

  DMA arbitration
  Data Word write (starting at the Data List Pointer address, incremented for each successive word)

Status Word Received.

- Status Word DMA

  DMA Arbitration
  Status Word write

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTM is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
Monitor Command Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

Message Completion.

Upon completion of the message, the BCRTM initiates a DMA cycle to update the status word and fetch the address of the next Monitor Command Block:

DMA Arbitration (BURST)
Control/Status Word Write
Tail Pointer Read

9.0 Exception Handling and Interrupt Logging

The exception handling scheme the BCRTM uses is based on an interrupt structure and provides a high degree of flexibility in:

- defining the events that cause an interrupt,
- selecting between High-Priority and Standard interrupts, and
- selecting the amount of interrupt history retained.

The interrupt structure consists of internal registers that enable interrupt generation, control bits in the RT and BC data structures (see the Remote Terminal Descriptor Definition section, page 23, and the Bus Controller Command Block definition, page 31), and an Interrupt Log List that sequentially stores an interrupt events record in system memory.

The BCRTM generates the Interrupt Log List (see figure 21) to allow the host CPU to view the Standard Interrupt occurrences in chronological order. Each Interrupt Log List entry contains three words. The first, the Interrupt Status Word, indicates the type of interrupt (entries are only for interrupts enabled). In the BC mode, the second word is a Command Block Pointer that refers to the corresponding Command Block. In the RT mode, the second word is a Descriptor Pointer that refers to the corresponding subaddress descriptor. The CPU-initialized third word, a Tail Pointer, is read by the BCRTM to determine the next Interrupt Log List address. The list length can be as long or as short as required. The configuration of the Tail Pointers determines the list length.

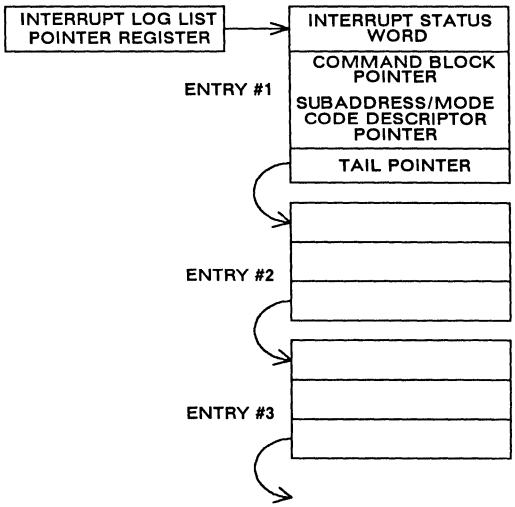


Figure 21. Interrupt Log List

The host CPU initializes the list by setting the tail pointers. This gives flexibility in the list capacity and the ability to link the list around noncontiguous blocks of memory. The host CPU sets the list's starting address using the Interrupt Log List Register. The BCRTM then updates this register with the address of the next list entry.

The internal High-Priority Interrupt Status/Reset Register indicates the cause of a High-Priority Interrupt. The High-Priority Interrupt signal is reset by writing a "1" to the set bits in this register.

The interrupt structure also uses three BCRTM-driven output signals to indicate when an interrupt event occurs:

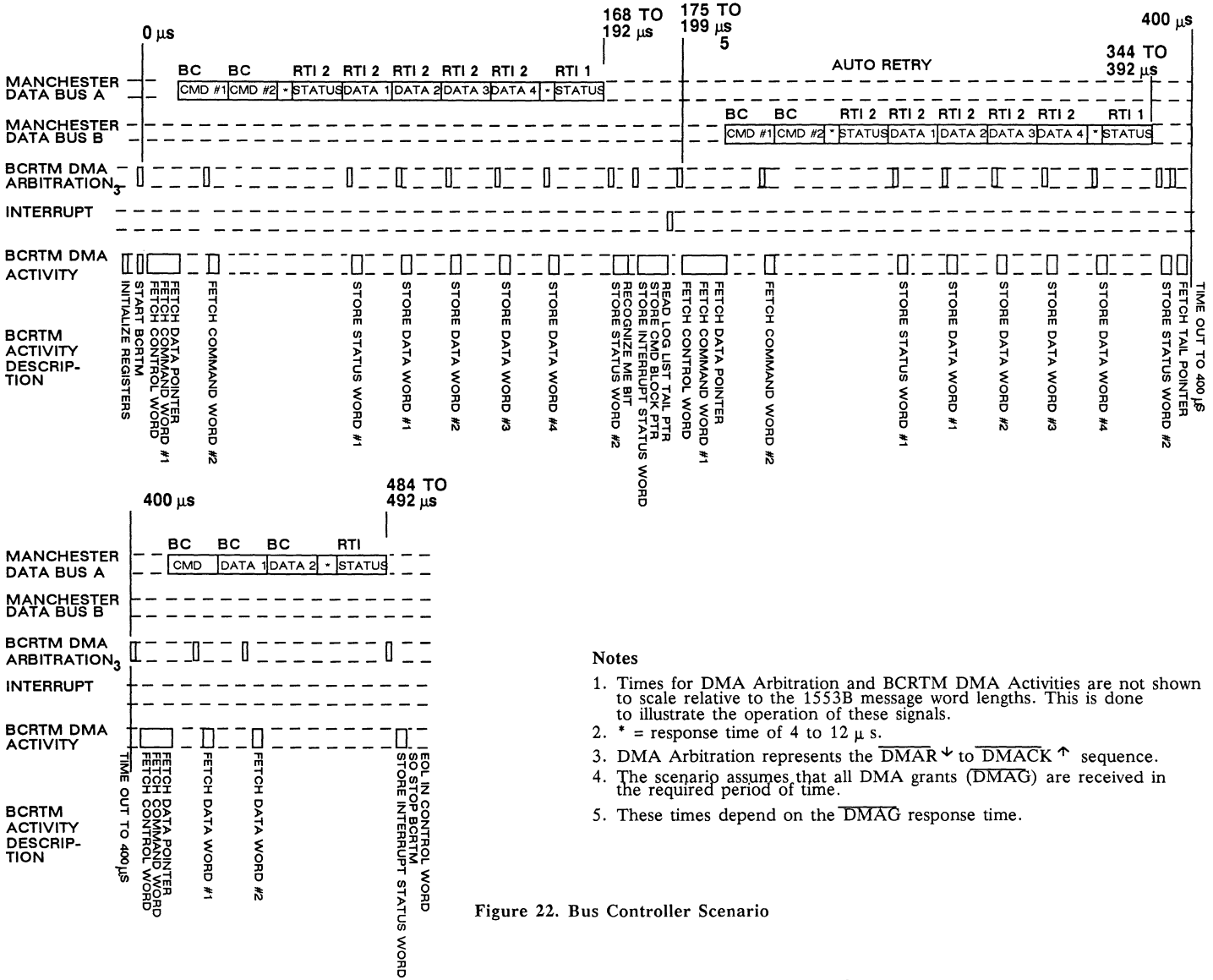
$\overline{\text{STDINTL}}$ Standard Interrupt Level. This signal is asserted when one or more of the events enabled in the Standard Interrupt Enable Register occurs. Clear the signal by resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register.

$\overline{\text{STDINTP}}$ Standard Interrupt Pulse. This signal is pulsed for each occurrence of an event enabled in the Standard Interrupt Enable Register.

$\overline{\text{HPINT}}$ High-Priority Interrupt. This signal is asserted for each occurrence of an event enabled in the High-Priority Interrupt/Enable Register. Writing to the corresponding bit in the High-Priority Status/Reset Register resets it.

Interrupt Status Word Definition
All bits in the Interrupt Status Word are active high and have the following functions:

Bit Number	Description
BIT 15	Interrupt Status Word Accessed. The BCRTM always sets this bit during the DMA Write of the Interrupt Status Word. If the CPU resets this bit after reading the Interrupt Status Word, the bit can help the CPU determine which entries have been acknowledged.
BIT 14	No Response Time-Out (Message Error condition). Further defines the Message Error condition to indicate that a Response Time-Out condition has occurred.
BIT 13	(RT) Message Error (ME). Indicates the ME bit was set in the 1553 status word response.
BITs 12-8	Reserved.
BIT 7	(RT) Subaddress Event or Mode Code with Data Word Interrupt. Indicates a descriptor control word has been accessed with either an Interrupt Upon Valid Command Received bit set or an Interrupt when Index=0 bit set (and the Index is decremented to 0).
BIT 6	(RT) Mode Code without Data Word Interrupt. Indicates a mode code has occurred with an Interrupt When Addressed interrupt enabled.
BIT 5	(RT) Illegal Broadcast Command. Applies to receive commands only. This bit indicates that a received command, due to an illegal mode code or subaddress field, has been received in the broadcast mode. This does not include invalid commands.
BIT 4	(RT) Illegal Command. This indicates that an illegal command has occurred due to an illegal mode code or subaddress and T/R field. This does not include invalid commands.
BIT 3	(BC) Polling Comparison Match. Indicates a polling comparison interrupt.
BIT 2	(BC) Retry Fail. Indicates all the programmed retries have failed.
BIT 1	(BC,RT) Message Error. Indicates a Message Error has occurred.
BIT 0	(BC) Interrupt and Continue. This corresponds to the interrupt and continue function described in the Command Block.



Notes

1. Times for DMA Arbitration and BCRTM DMA Activities are not shown to scale relative to the 1553B message word lengths. This is done to illustrate the operation of these signals.
2. * = response time of 4 to 12 µ s.
3. DMA Arbitration represents the $\overline{\text{DMAR}}\downarrow$ to $\overline{\text{DMACK}}\uparrow$ sequence.
4. The scenario assumes that all DMA grants ($\overline{\text{DMAG}}$) are received in the required period of time.
5. These times depend on the $\overline{\text{DMAG}}$ response time.

Figure 22. Bus Controller Scenario

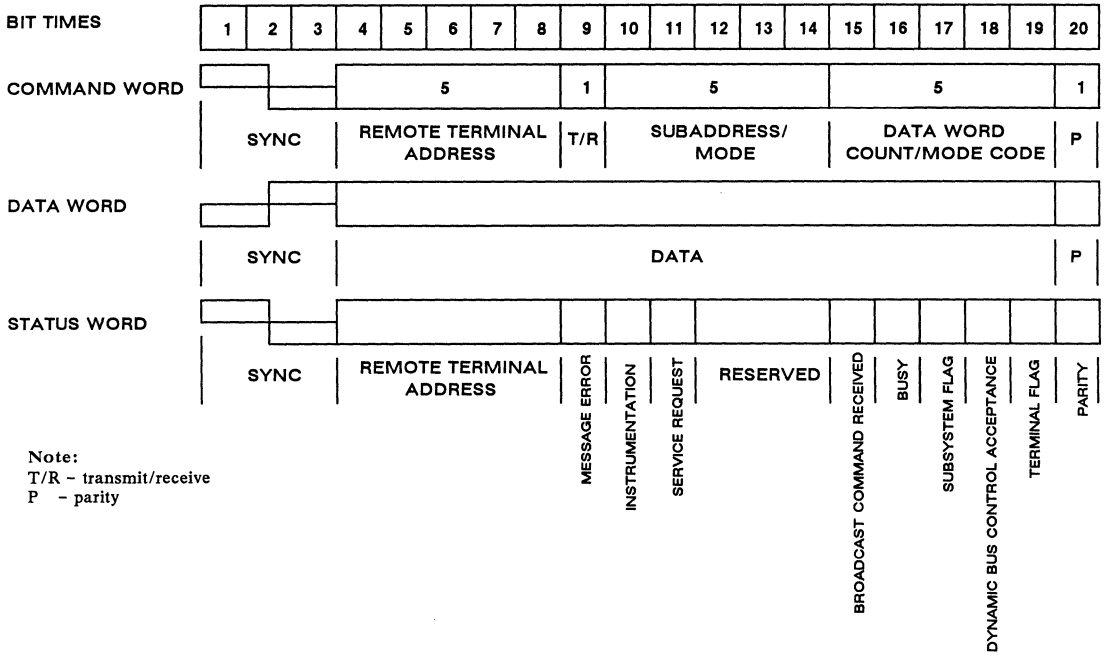


Figure 23. MIL-STD-1553B Word Formats

10.0 Operating Conditions*

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_{JMAX}	Maximum junction temperature	+175	°C
P_D	Average power dissipation (1)	300	mW
Θ_{JC}	Thermal resistance, junction-to-case	10	°C/W

Note:
1. Does not reflect the added PD due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ±.01%	MHz

11.0 DC Electrical Characteristics

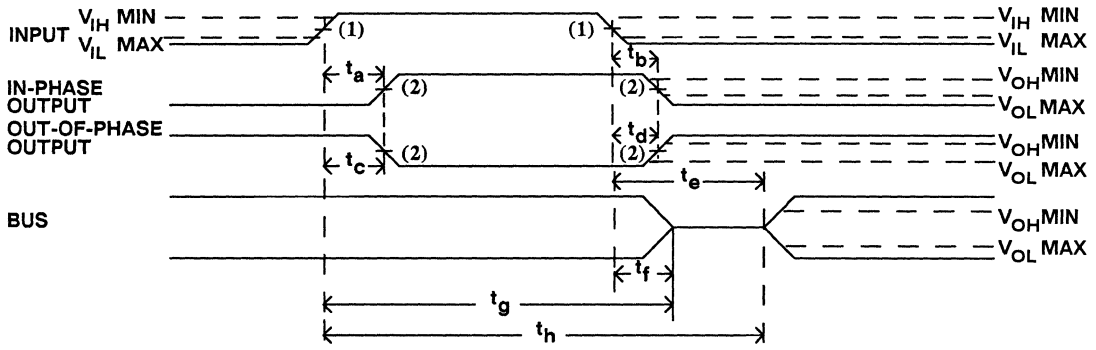
(V_{DD} = 5.0 V ± 10%; -55°C < T_C < + 125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH} Non-RAD	High-level input voltage TTL inputs		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-up resistors Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -1 -1 -550	 1 1 -80	 µA µA µA
V_{IH} RAD-HARD	High-level input voltage (6) TTL inputs (7) CMOS inputs		 2.2 .7 V_{DD}		 V V
I_{IN} RAD-HARD	Input leakage current TTL (7), CMOS inputs Inputs with pull-up resistors Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -10 +150 -900	 10 +900 -150	 µA µA µA
V_{OL}	Low-level output voltage TTL outputs CMOS outputs	 I_{OL} = 3.2 mA I_{OL} = 50 µA		 0.4 V SS +.1	 V V
V_{OH}	High-level output voltage TTL outputs CMOS outputs	 I_{OH} = -400 µA I_{OH} = 50 µA	 2.4 VDD -.1		 V V
I_{OZ}	Three-state output leakage current TTL outputs	 $V_O = V_{DD}$ or V_{SS}	 -10	 10	 µA
I_{OS}	Short-circuit output current (1,2)	V_{DD} = 5.5 V, $V_O = V_{DD}$ V_{DD} = 5.5 V, V_O = 0 V	 -100	100	mA mA
C_{IN}	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		20	pF
I_{DD}	Average operating current (1,4)	F = 12 MHz, C_L = 50 pF		50	mA
QI_{DD}	Quiescent current	See Note 5		3	mA

Notes:
1. Supplied as a design limit, but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes which may affect input/output capacitance.
4. Includes current through input pull-up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
5. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.
6. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) +20%, -0%; $V_{IL} = V_{IL}$(max) +0%, -50%, as specified herein, for TTL - compatible inputs. Devices may be tested using input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
7. To 1 x 10^6 total dose; above this level CMOS I/Os required.

12.0 AC Electrical Characteristics

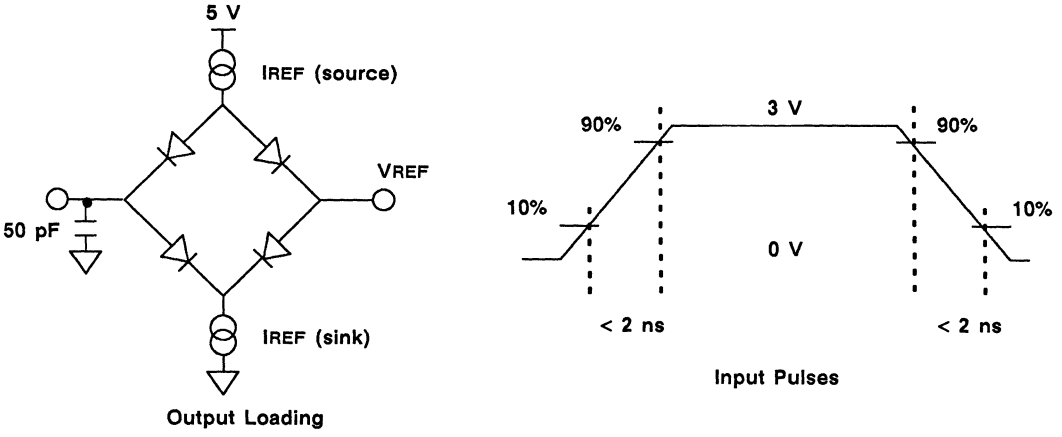
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

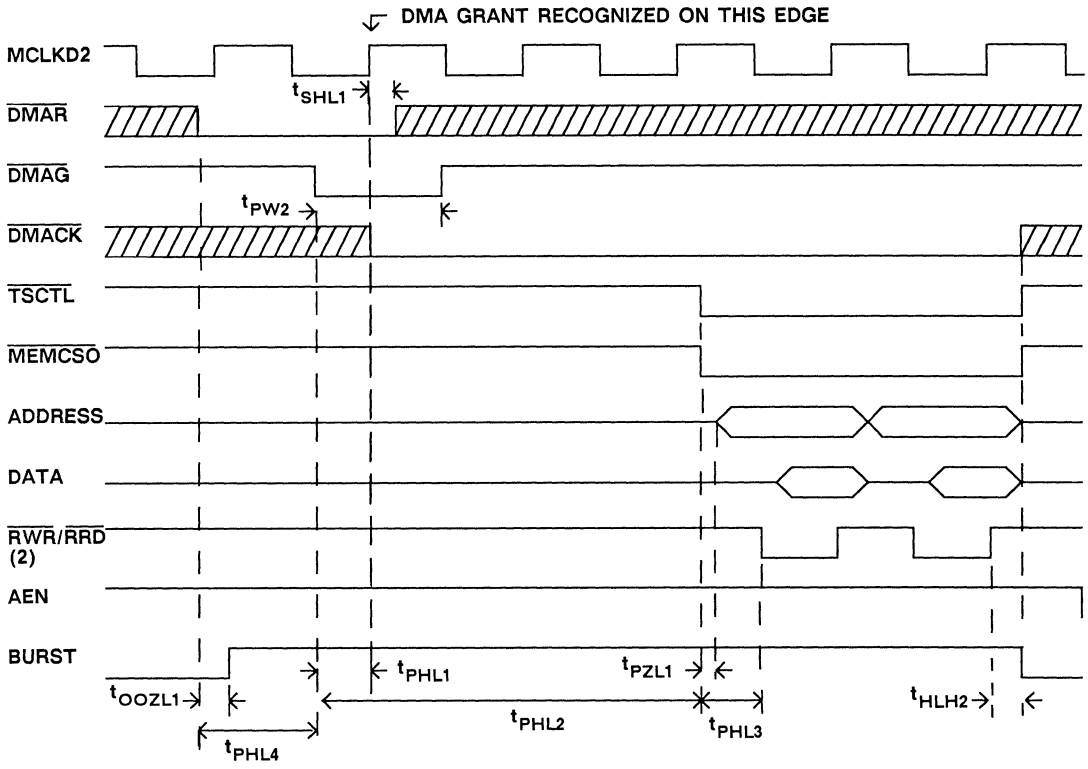
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 24. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

Figure 25. AC Test Loads and Input Waveforms

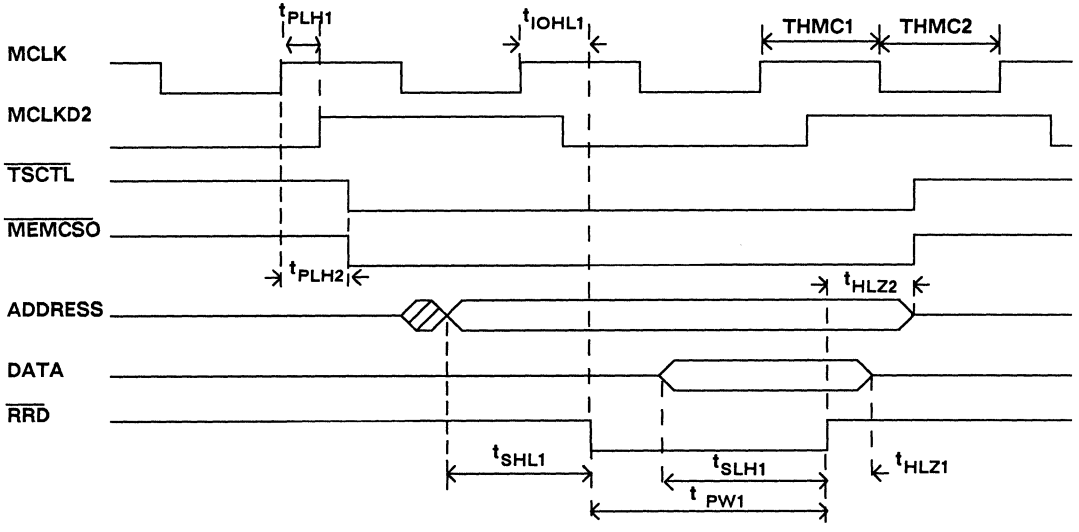


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	$\overline{DMACK}\downarrow$ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PHL1} (1)	$\overline{DMAG}\downarrow$ to $\overline{DMACK}\downarrow$ See note 3	0	45	ns
t_{PHL2}	$\overline{DMAG}\downarrow$ to $\overline{TSCTL}\downarrow$	2xMCLK	4xMCLK	ns
t_{PZL1}	$\overline{TSCTL}\downarrow$ to ADDRESS valid	0	40	ns
t_{HLH2}	$\overline{RWR/RRD}\uparrow$ to $\overline{DMACK}\uparrow$	THMC1-10	THMC1+10	ns
t_{PHL3}	$\overline{TSCTL}\downarrow$ to $\overline{RWR/RRD}\downarrow$	MCLK-20	MCLK+20	ns
t_{PW2}	$\overline{DMAG}\downarrow$ to $\overline{DMAG}\uparrow$	MCLK	6xMCLK	ns
t_{OOZL1}	$\overline{DMAR}\downarrow$ to BURST $\uparrow$	0	10	ns
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See note 4	0	3.5 (1.9)	µs
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See note 5	0	1.9 (0.8)	µs

Notes:
1. Guaranteed by test.
2. See figures 27 & 28 for detailed DMA read and write timing.
3. $\overline{DMAG}$ must be asserted at least 45 ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If $\overline{DMAG}$ is not asserted at least 45 ns prior to the rising edge of MCLKD2, $\overline{DMAG}$ is not recognized until the following MCLKD2 cycle.
4. Provided MCLK = 12 MHz. Number in parentheses indicates the longest $\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ alllowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.
5. Provided MCLK = 6 MHz. Number in parentheses indicates the longest $\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.

MCLK = period of the memory clock cycle.
BURST signal is for multiple-word DMA accesses.
THMC1 is equivalent to the positive phase of MCLK (see figure 27).

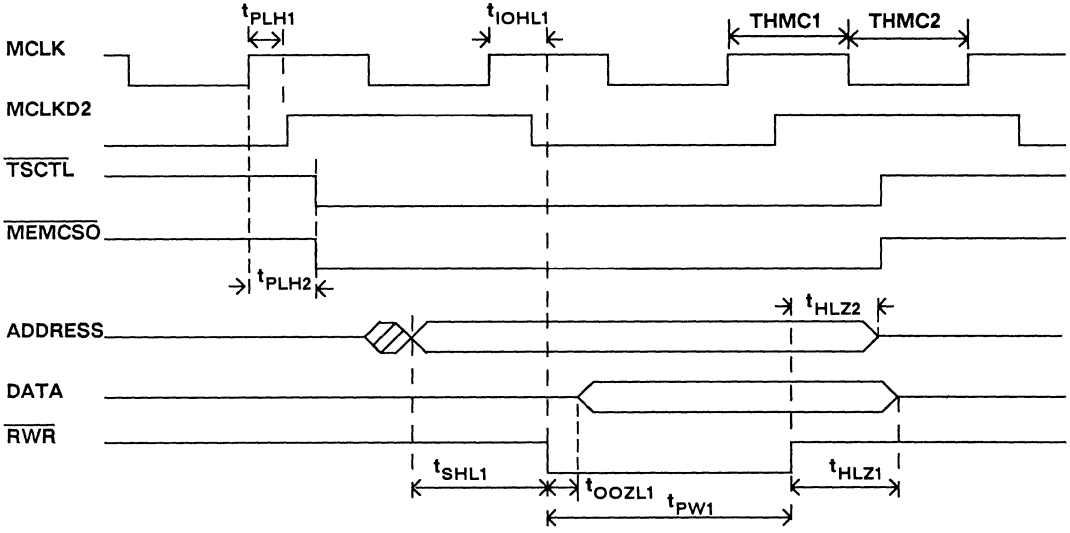
Figure 26. BURST DMA Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RRD}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{PW1}	$\overline{RRD}$ ↓ to $\overline{RRD}$ ↑	MCLK-5	MCLK+5	ns
t_{HLZ2}	$\overline{RRD}$ ↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-10	THMC1	ns
t_{HLZ1}	$\overline{RRD}$ ↑ to DATA High Impedance (DATA hold)	5	-	ns
t_{SLH1}	DATA valid to $\overline{RRD}$ ↑ (DATA setup)	40	-	ns
t_{PLH1} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑ to $\overline{TSCTL/MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑ to $\overline{RRD}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

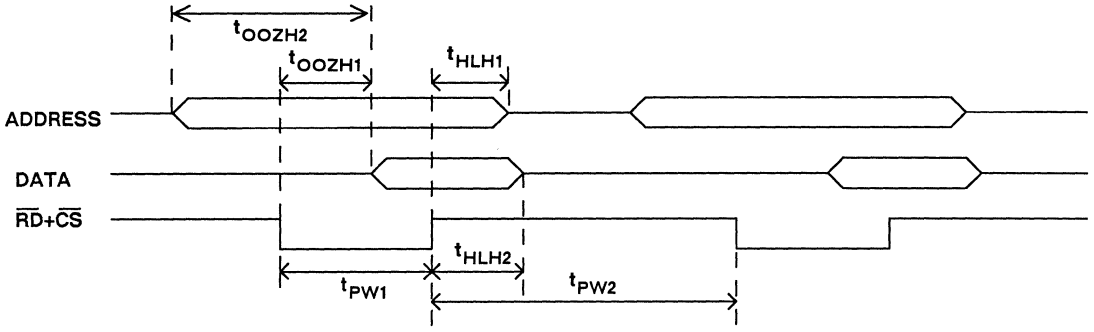
Figure 27. BCRTM DMA Read Timing (One-Word Read)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RWR}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{OOZL1}(1)	$\overline{RWR}$↓ to DATA valid	0	30	ns
t_{HLZ1}	$\overline{RWR}$↑ to DATA High Impedance (DATA hold)	THMC1-20	THMC1	ns
t_{HLZ2}	$\overline{RWR}$↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-20	THMC1	ns
t_{PW1}	$\overline{RWR}$ ↓ to $\overline{RWR}$ ↑	MCLK-5	MCLK+5	ns
t_{PLH1} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑ to $\overline{TSCTL}$/$\overline{MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑ to $\overline{RWR}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

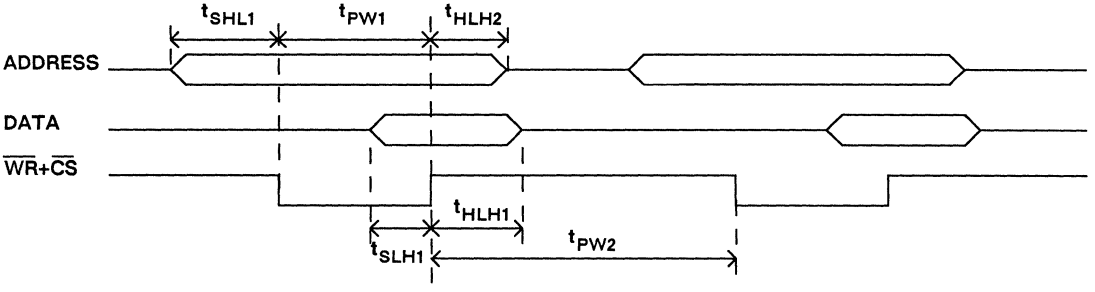
Figure 28. BCRTM DMA Write Timing (One-Word Write)



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{OOZH2}	ADDRESS valid to DATA valid		-	80	ns
t_{HLH2}	$\overline{RD}+\overline{CS}$ ↑to DATA High Impedance	(DATA hold)	5	50	ns
t_{OOZH1} (1)	$\overline{RD}+\overline{CS}$ ↓to DATA valid	(DATA access)	-	60	ns
t_{HLH1}	$\overline{RD}+\overline{CS}$ ↑to ADDRESS High Impedance	(ADDRESS hold)	5	-	ns
t_{PW1}	$\overline{RD}+\overline{CS}$ ↓to $\overline{RD}+\overline{CS}$ ↑		60	-	ns
t_{PW2}	$\overline{RD}+\overline{CS}$ ↑to $\overline{RD}+\overline{CS}$ ↓		80	-	ns

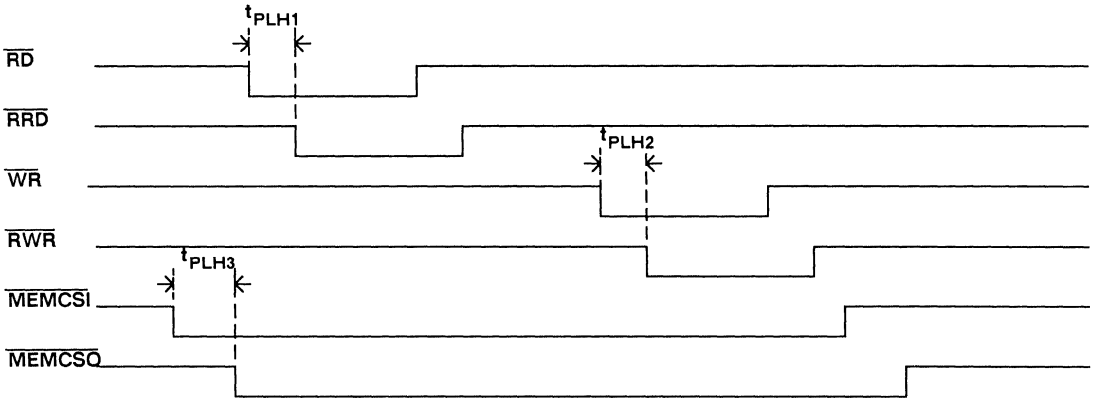
Notes:
1. Guaranteed by test.
2. User must adhere to both tOOZH1 and tOOZH2 timing constraints to ensure valid data.

Figure 29. BCRTM Register Read Timing



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{WR}+\overline{CS}$ ↓	(ADDRESS setup)	60	-	ns
t_{SLH1}	DATA valid to $\overline{WR}+\overline{CS}$ ↑	(DATA setup)	60	-	ns
t_{PW1}	$\overline{WR}+\overline{CS}$↓ to $\overline{WR}+\overline{CS}$ ↑		60	-	ns
t_{HLH1}	$\overline{WR}+\overline{CS}$↑ to DATA High Impedance	(DATA hold)	10	-	ns
t_{HLH2}	$\overline{WR}+\overline{CS}$↑ to ADDRESS High Impedance	(ADDRESS hold)	10	-	ns
t_{PW2}	$\overline{WR}+\overline{CS}$↑ to $\overline{WR}+\overline{CS}$ ↓		80	-	ns

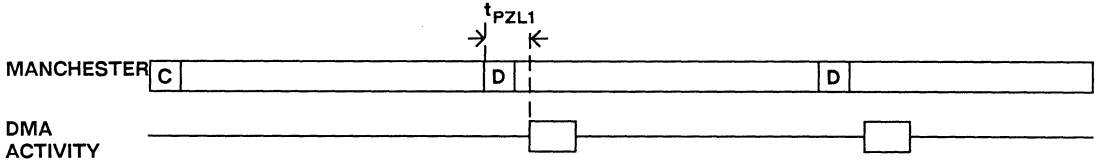
Figure 30. BCRTM Register Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PLH1} (1)	$\overline{RD}$ ↓to $\overline{RRD}$ ↓	0	30	ns
t_{PLH2} (1)	$\overline{WR}$↓ to $\overline{RWR}$ ↓	0	30	ns
t_{PLH3} (1)	$\overline{MEMCSI}$ ↓to $\overline{MEMCSO}$ ↓	0	30	ns

Note:
1. Guaranteed by test.

Figure 31. BCRTM Dual-Port Interface Timing Delays

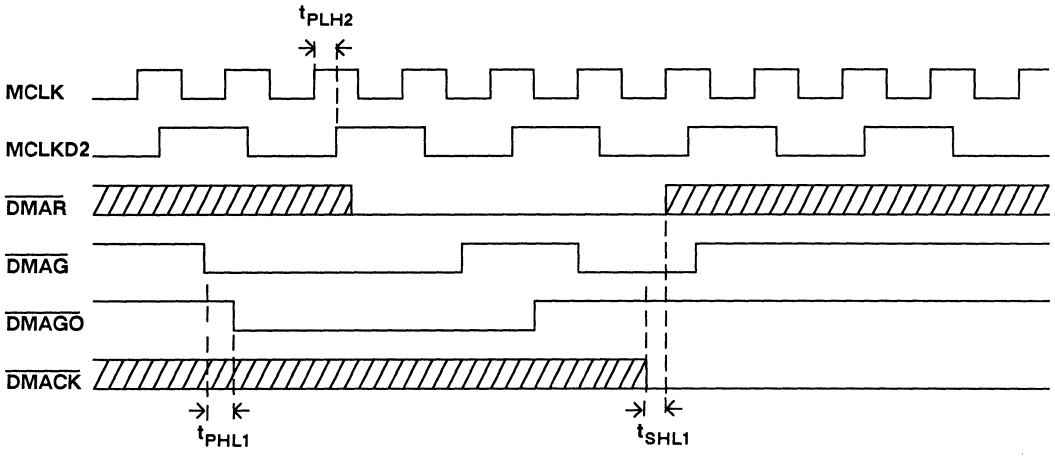


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PZL1}	Data word to DMA activity	0	4	µs

This diagram indicates the relationship between the incoming Manchester code and DMA activity (i.e., $\overline{DMAR}$ ↓ to $\overline{DMACK}$ ↑).

Note:
The pulsewidth = (11 µs -t_{DMA} -t_{PZL1}) where t_{DMA} is the time to complete DMA activity (i.e., $\overline{DMAR}$↓ to $\overline{DMACK}$ ↑).

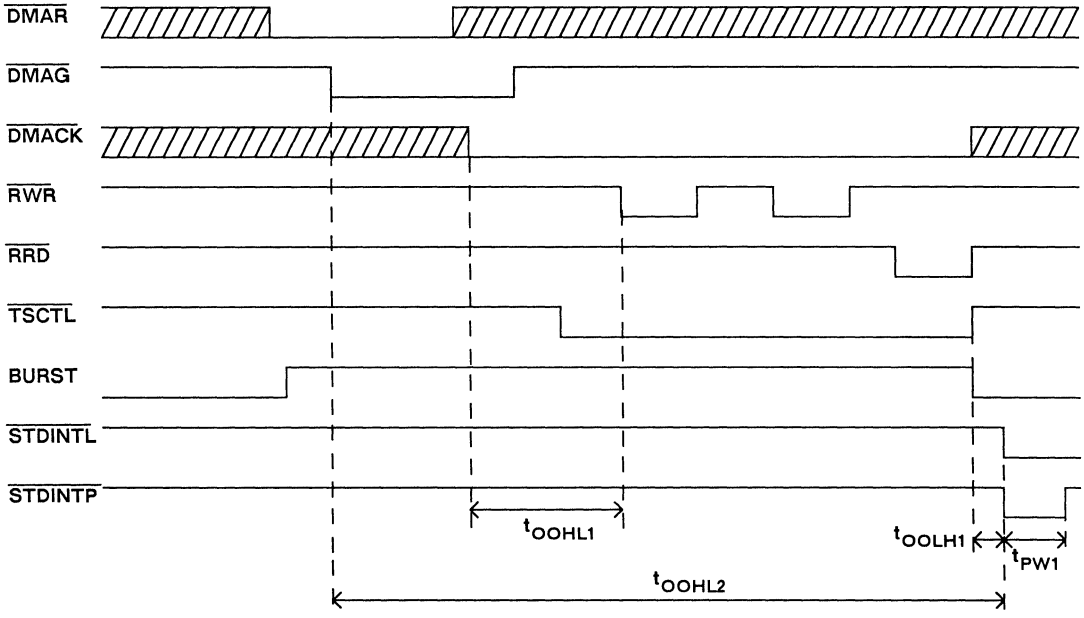
Figure 32. DMA Activity (RT Mode)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PHL1}	$\overline{DMAG}$ ↓ to $\overline{DMAGO}$ ↓	0	30	ns
t_{SHL1}	$\overline{DMACK}$ ↓ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PLH2} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns

Notes:
1. Guaranteed by test.
2. When $\overline{DMAG}$ is asserted before $\overline{DMAR}$, the $\overline{DMAG}$ signal passes through the BCRTM as $\overline{DMAGO}$.

Figure 33. BCRTM Arbitration when $\overline{DMAG}$ is Asserted before Arbitration



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{OOLH1}	$\overline{TSCTL}$ ↑ to $\overline{STDINTP}$/$\overline{STDINTL}$ ↓	-	1	µs
t_{PW1}	$\overline{STDINTP}$ ↓to $\overline{STDINTP}$ ↑	320	340	ns
t_{OOHL1}	$\overline{DMACK}$ ↓to $\overline{RWR}$ ↓	3xMCLK-10	5xMCLK	ns
t_{OOHL2}	$\overline{DMAG}$ ↓to $\overline{STDINTL}$ ↓	8xMCLK+0.5	10xMCLK+1	ns

Note:
Address and data bus relationships (not shown) are identical to figure 26.

Figure 34. BCRTM Interrupt Log List Entry Operation Timing

13.0 Package Outline Drawings

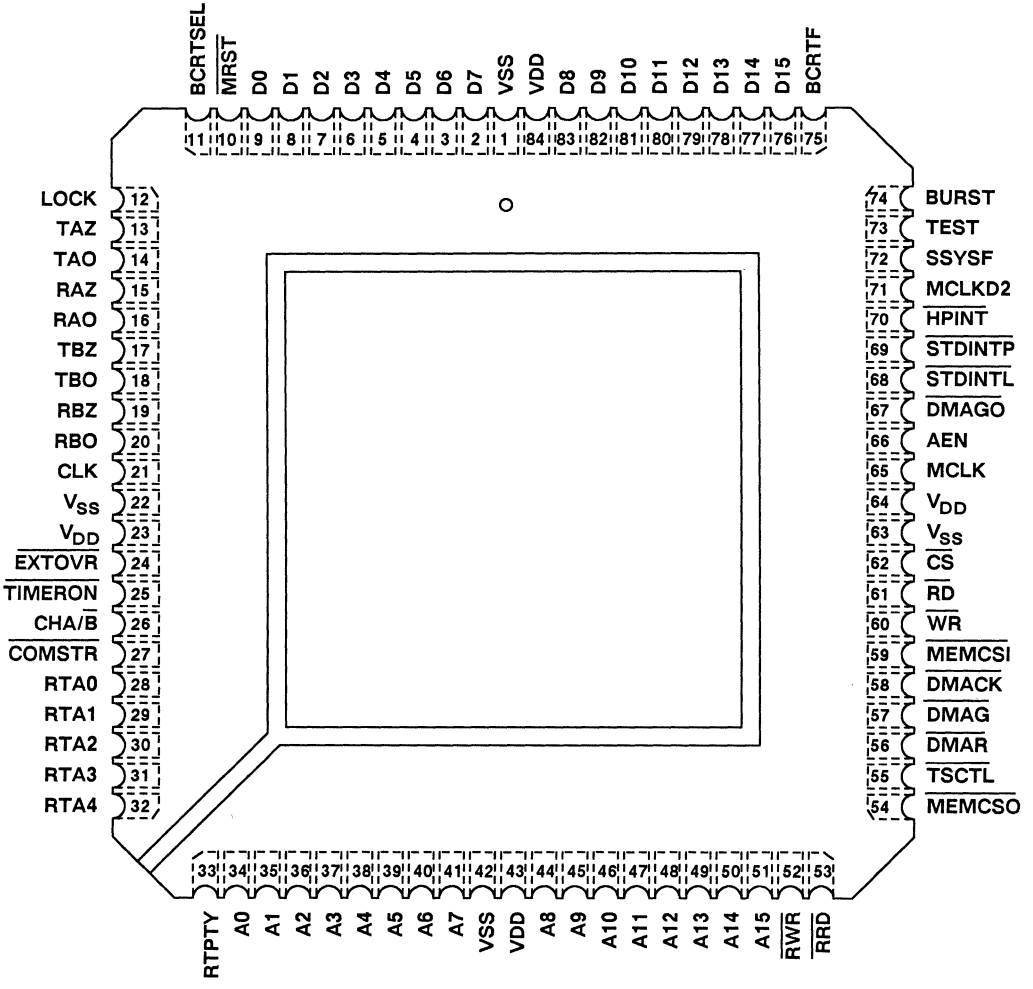


Figure 35a. BCRTM Flatpack and LCC Pin Identification (Top View)
(Flatpack Leads Omitted for Clarity)

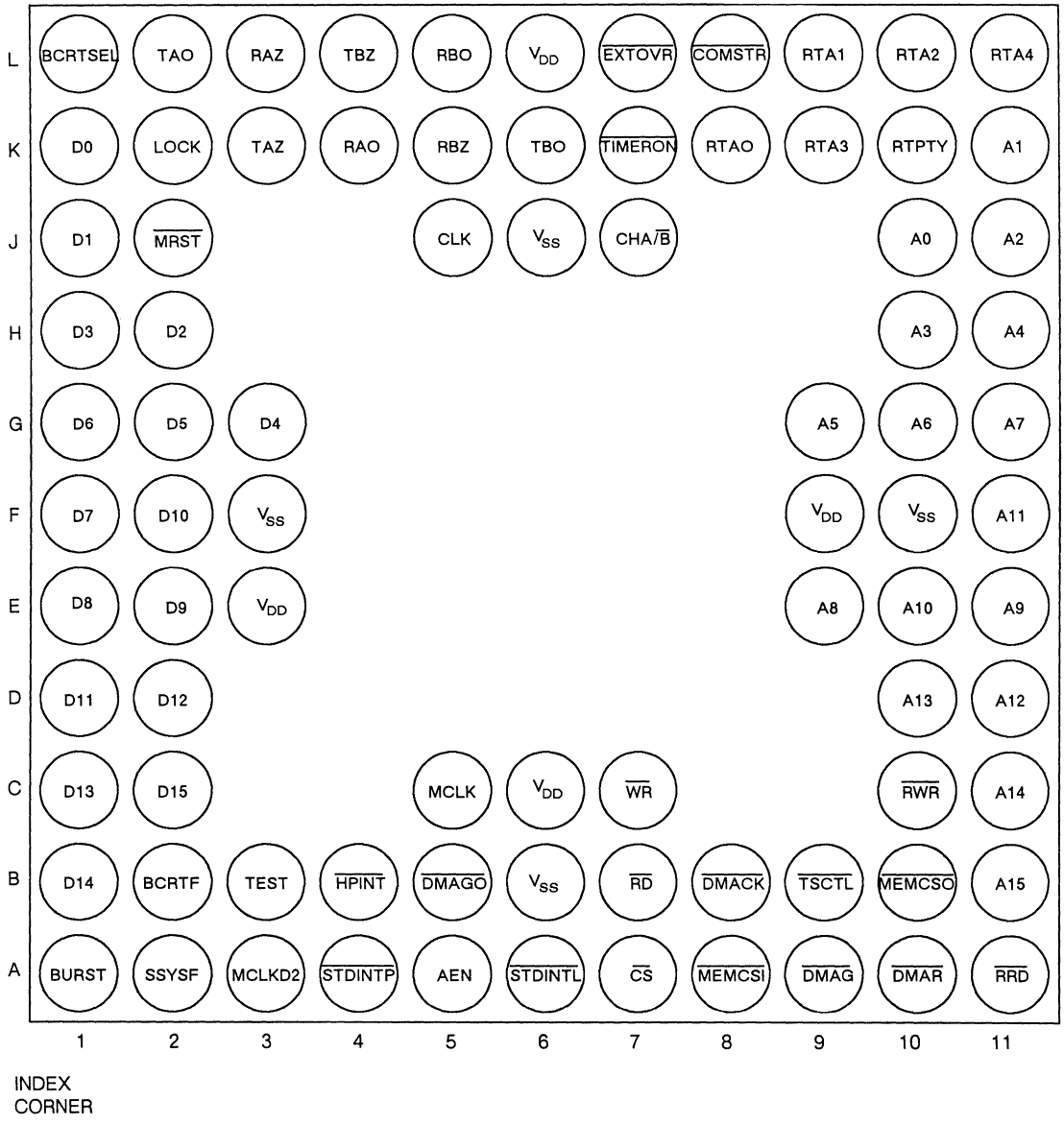


Figure 35b. BCRTM Pingrid Array Pin Identification (Bottom View)

UT1553 BCRTMP

FEATURES

- ☐ Comprehensive MIL-STD-1553 dual-redundant Bus Controller (BC) and Remote Terminal (RT) functions
- ☐ Multiple message processing capability in BC and RT modes
- ☐ Automatic polling and intermessage delay in BC mode
- ☐ Programmable interrupt scheme and internally generated interrupt history list
- ☐ Register-oriented architecture to enhance programmability
- ☐ DMA or pseudo-dual-port memory interface with 64K addressability
- ☐ Time tagging and message logging in RT mode
- ☐ Packaged in 144-pin pingrid array, 132-lead flatpack
- ☐ Low-power CMOS technology
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ☐ Eight mode select inputs configure the device for a wide variety of 1553 protocols: MIL-STD-1553A, MIL-STD-1553B, McDonnell Douglas A3818, A5232, A5690, Grumman Aerospace SP-G-151A
- ☐ Comprehensive Built-In-Test (BIT) includes: Continuous on-line wrap-around test, off-line BIT, special system wrap-around test

3

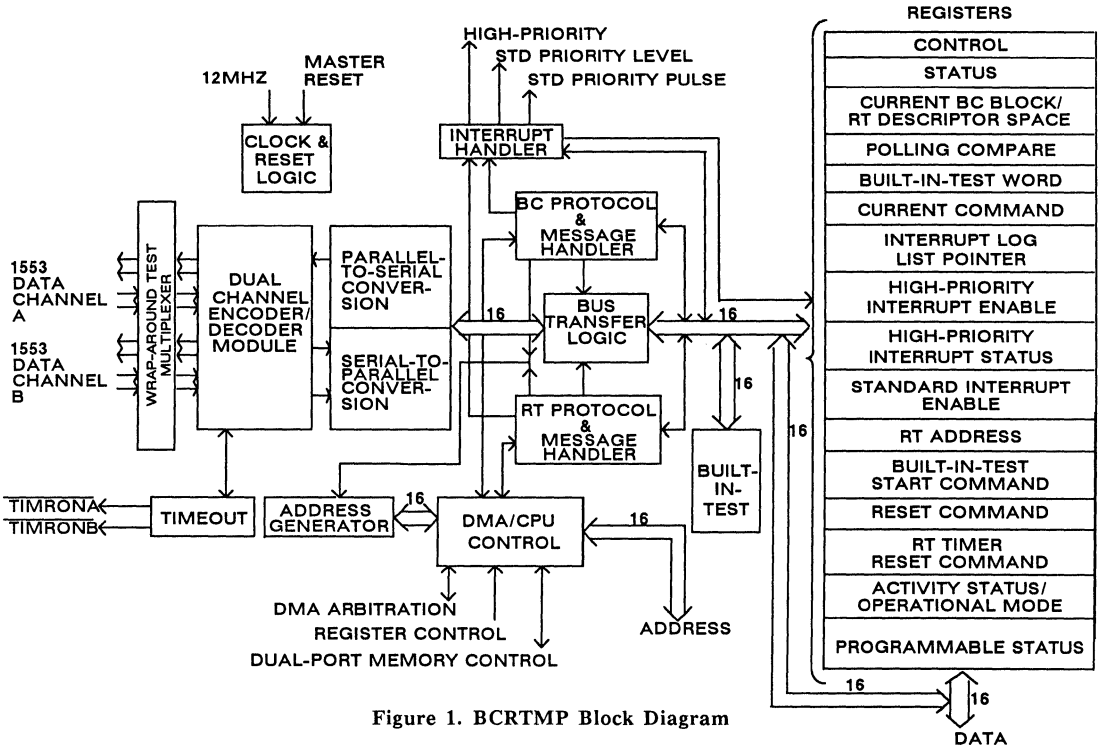


Figure 1. BCRTMP Block Diagram

Table of Contents

1.0 INTRODUCTION

The monolithic CMOS UT1553 BCRTMP provides the system designer with an intelligent solution to MIL-STD-1553 multiplexed serial data bus design problems. The UT1553 BCRTMP is a single-chip device that implements two of the three defined MIL-STD-1553 functions - Bus Controller and Remote Terminal - and is flexible enough to conform to many of the MIL-STD-1553 "industry standards" created between and including releases of MIL-STD-1553A and MIL-STD-1553B. Designed to reduce host CPU overhead, the BCRTMP's powerful state machines automatically execute message transfers, provide interrupts, and generate status information. The BCRTMP's register-based architecture allows it to conform to the many protocol options regarding status words, mode codes, use of Broadcast, Message Error, and RT Response Time as specified in the various "1553 standards." Multiple registers offer many programmable functions as well as extensive information for host use. In the BC mode, the BCRTMP uses a linked-list message scheme to provide the host with message chaining capability. The BCRTMP enhances memory use by supporting variable-size, relocatable data blocks. In the RT mode, the BCRTMP implements time-tagging and message history functions. It also supports multiple (up to 128) message buffering and variable length messages to any subaddress.

The UT1553 BCRTMP is an intelligent, versatile, and easy to implement device -- a powerful asset to system designers.

1.1 Features - Remote Terminal (RT) Mode

Indexing
The BCRTMP is programmable to index or buffer messages on a subaddress-by-subaddress basis. The BCRTMP, which can index as many as 128 messages, can also assert an interrupt when either the selected number of messages is reached or every time a specified subaddress is accessed.

Variable Space Allocation
The BCRTMP can use as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTMP provides flexible data placement and convenient access.

Sequential Data Storage
The BCRTMP stores/retrieves, by subaddress, all messages in the order in which they are transacted.

Sequential Message Status Information
The BCRTMP provides message validity, time-tag, and word-count information, and stores it sequentially in a separate, cross-referenced list.

Illegalizing Mode Codes and Subaddresses
The host can declare mode codes and subaddresses illegal by setting the appropriate bit(s) in memory.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTMP provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

1.2 Features - Bus Controller (BC) Mode

Multiple Message Processing
The BCRTMP autonomously processes any number of messages or lists of messages that may be stored in a 64K memory space.

Automatic Intermessage Delay
When programmed by the host, the BCRTMP can delay a host-specified time before executing the next message in sequence.

Automatic Polling
When polling, the BCRTMP interrogates the remote terminals and then compares their status word responses to the contents of the Polling Compare Register. The BCRTMP can interrupt the host CPU if an erroneous remote terminal status word response occurs.

Automatic Retry
The BCRTMP can automatically retry a message on busy, message error, and/or response time-out conditions. The BCRTMP can retry up to four times on the same or on the alternate bus.

Programmable Interrupt Selection
The host CPU can select various events to cause an interrupt with provision for high and standard priority interrupts.

Interrupt History List
The BCRTMP provides an Interrupt History List that records, in the order of occurrence, the events that caused the interrupts. The list length is programmable.

Variable Space Allocation
The BCRTMP uses as little or as much memory (up to 64K) as needed.

Selectable Data Storage
Address programmability within the BCRTMP provides flexible data placement and convenient access.

1.3 Features - Multiple Protocol

Since the inception of the loosely defined MIL-STD-1553A in 1973, various "1553 standards" have developed, all with their own peculiarities. The UT1553 BCRTMP addresses MIL-STD-1553A, MIL-STD-1553B, McDonnell Douglas A3818, McDonnell Douglas A5232, McDonnell Douglas A5690, and Grumman Aerospace SP-G-151A. While the part was designed with these "standards" specifically in mind, the BCRTMP's flexibility permits conformance to nearly any conceivable "1553-like standard." The basic differences among the various "standards" fall into five categories:

1) Status Word Definition
2) Mode Code Definition
3) Use of Broadcast
4) Message Error Handling
5) Remote Terminal (RT) Response Time

Status Word Definition
The BCRTMP can operate in a mode where the status word is defined in strict conformance with MIL-STD-1553B, or it can operate in a more flexible mode. In this flexible status word mode, the user can program the individual status word bits using internal registers.

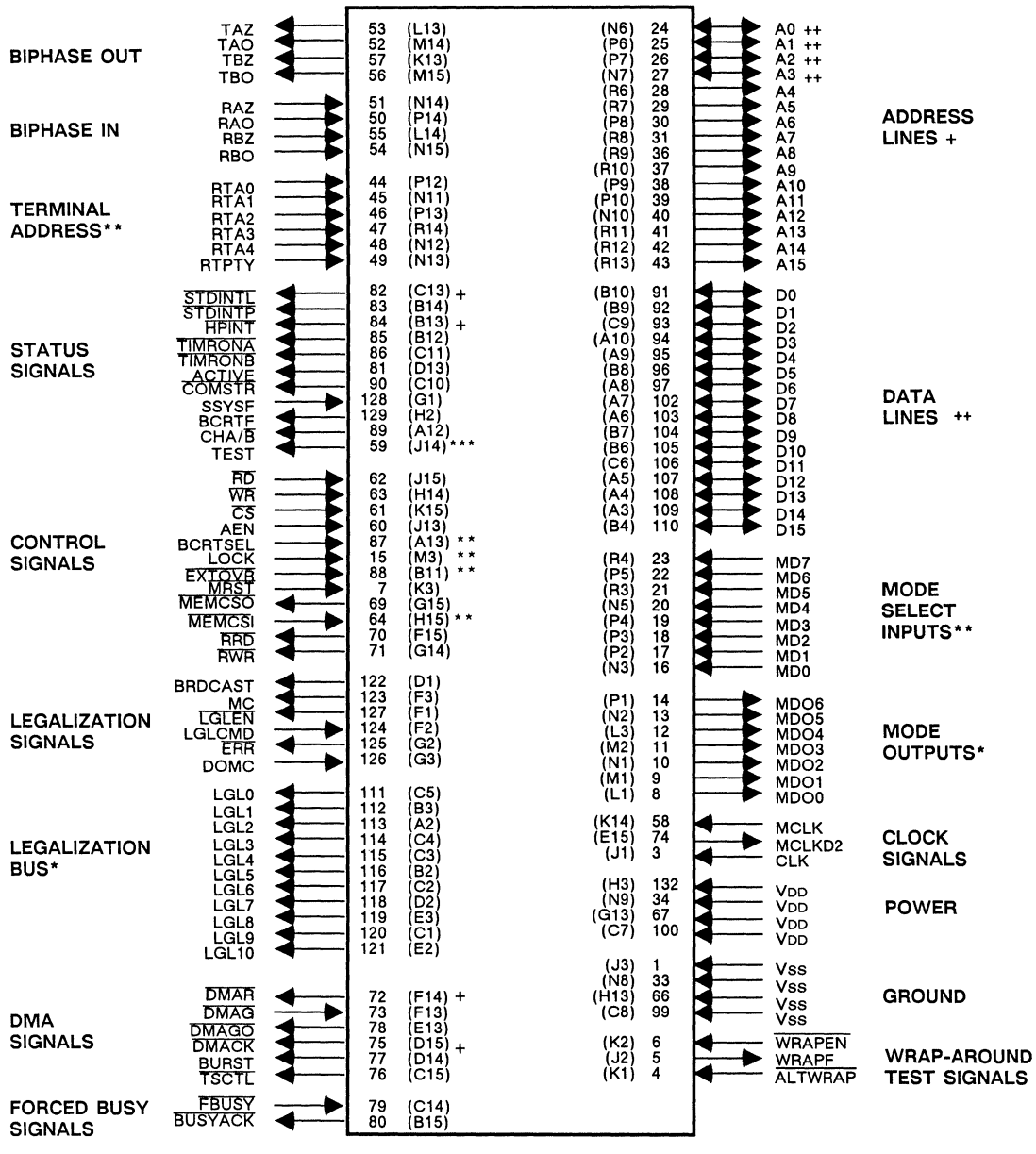
Mode Code Definition
The designer can place the BCRTMP in an operational mode so that the device performs in strict conformance with the mode code definitions for MIL-STD-1553B. The designer may also opt not to automatically execute mode codes, providing flexibility in mode code definition and illegalization.

Use of Broadcast
The BCRTMP has a programmable mode option that allows the user to determine whether to allow broadcast commands in a system.

Message Error Handling
Some 1553 protocols (e. g., MIL-STD-1553B) consider any message error reason to discard the entire message and suppress status word transmission, while others (e. g., McDonnell Douglas A3818) define the required activity according to message error severity. The BCRTMP can be programmed to conform to either requirement.

Remote Terminal (RT) Response Time
The BCRTMP offers two methods of legalization (Bus Legalization and DMA Legalization), which the designer selects depending on the required RT response time.

2.0 Pin Identification And Description



* Pin at high impedance when $\overline{MRST}$ is low.
** Pin internally pulled up.
\+ Pin at high impedance when not asserted.
++ Bidirectional pin.
*** Formerly $\overline{MEMWIN}$.

( ) Pingrid array pin identification in parentheses.
Flatpack pin numbers not in parentheses.

Figure 2. BCRTMP Functional Pin Description

Legend for TYPE and ACTIVE fields:

TUI = TTL input (pull-up)
AL = Active low
AH = Active high
ZL = Active low - inactive state is high impedance
TI = TTL input
TO = TTL output
TTO = Three-state TTL output
TTB = Bidirectional

Notes:
1. Address and data buses are in the high-impedance state when idle.
2. Flatpack pin numbers are same as LCC.

ADDRESS BUS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
A0	24	N6	TTB	--	Bit 0 (LSB) of the Address bus
A1	25	P6	TTB	--	Bit 1 of the Address bus
A2	26	P7	TTB	--	Bit 2 of the Address bus
A3	27	N7	TTB	--	Bit 3 of the Address bus
A4	28	R6	TTO	--	Bit 4 of the Address bus
A5	29	R7	TTO	--	Bit 5 of the Address bus
A6	30	P8	TTO	--	Bit 6 of the Address bus
A7	31	R8	TTO	--	Bit 7 of the Address bus
A8	36	R9	TTO	--	Bit 8 of the Address bus
A9	37	R10	TTO	--	Bit 9 of the Address bus
A10	38	P9	TTO	--	Bit 10 of the Address bus
A11	39	P10	TTO	--	Bit 11 of the Address bus
A12	40	N10	TTO	--	Bit 12 of the Address bus
A13	41	R11	TTO	--	Bit 13 of the Address bus
A14	42	R12	TTO	--	Bit 14 of the Address bus
A15	43	R13	TTO	--	Bit 15 (MSB) of the Address bus

DATA BUS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
D0	91	B10	TTB	--	Bit 0 (LSB) of the Data bus
D1	92	B9	TTB	--	Bit 1 of the Data bus
D2	93	C9	TTB	--	Bit 2 of the Data bus
D3	94	A10	TTB	--	Bit 3 of the Data bus
D4	95	A9	TTB	--	Bit 4 of the Data bus
D5	96	B8	TTB	--	Bit 5 of the Data bus
D6	97	A8	TTB	--	Bit 6 of the Data bus
D7	102	A7	TTB	--	Bit 7 of the Data bus
D8	103	A6	TTB	--	Bit 8 of the Data bus
D9	104	B7	TTB	--	Bit 9 of the Data bus
D10	105	B6	TTB	--	Bit 10 of the Data bus
D11	106	C6	TTB	--	Bit 11 of the Data bus
D12	107	A5	TTB	--	Bit 12 of the Data bus
D13	108	A4	TTB	--	Bit 13 of the Data bus
D14	109	A3	TTB	--	Bit 14 of the Data bus
D15	110	B4	TTB	--	Bit 15 (MSB) of the Data bus

TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
RTA0	44	P12	TUI	--	Remote Terminal Address Bit 0 (LSB). The entire RT address is strobed in at Master Reset. Verify it by reading the Remote Terminal Address Register. All the Remote Terminal Address bits are internally pulled up.
RTA1	45	N11	TUI	--	Remote Terminal Address Bit 1. This is bit 1 of the Remote Terminal Address.
RTA2	46	P13	TUI	--	Remote Terminal Address Bit 2. This is bit 2 of the Remote Terminal Address.
RTA3	47	R14	TUI	--	Remote Terminal Address Bit 3. This is bit 3 of the Remote Terminal Address.
RTA4	48	N12	TUI	--	Remote Terminal Address Bit 4. This is bit 4 (MSB) of the Remote Terminal Address.
RTPTY	49	N13	TUI	--	Remote Terminal (Address) Parity. This is an odd parity input for the Remote Terminal Address.

CONTROL SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{RD}$	62	J15	TI	AL	Read. The host uses this in conjunction with $\overline{CS}$ to read an internal BCRTMP register.
$\overline{WR}$	63	H14	TI	AL	Write. The host uses this in conjunction with $\overline{CS}$ to write to an internal BCRTMP register.
$\overline{CS}$	61	K15	TI	AL	Chip Select. This selects the BCRTMP when accessing the BCRTMP's internal register.
AEN	60	J13	TI	AH	Address Enable. The host CPU uses AEN to indicate to the BCRTMP that the BCRTMP's address lines can be asserted; this is a precautionary signal provided to avoid address bus crash. If not used, it must be tied high.
BCRTSEL	87	A13	TUI	--	BC/$\overline{RT}$ Select. This selects between either the Bus Controller or Remote Terminal mode. The BC/$\overline{RT}$ Mode Select bit in the Control Register overrides this input if the LOCK pin is not high. This pin is internally pulled high.
LOCK	15	M3	TUI	AH	Lock. When set, this pin prevents internal changes to the RT address and BC/$\overline{RT}$ mode select functions as well as the Operation Mode select (MD7-MD0) functions. This pin is internally pulled high.
$\overline{EXTOVR}$	88	B11	TUI	AL	External Override. Use this in multi-redundant applications. Upon receipt, the BCRTMP aborts all current activity. $\overline{EXTOVR}$ should be connected to $\overline{COMSTR}$ output of the adjacent BCRTMP when used. This pin is internally pulled high.
$\overline{MRST}$	7	K3	TI	AL	Master Reset. This resets all internal state machines, encoders, decoders, and registers. The minimum pulse width for a successful Master Reset is 500 ns.
$\overline{MEMCSO}$	69	G15	TO	AL	Memory Chip Select Out. This is the regenerated $\overline{MEMCSI}$ input for external RAM during the pseudo-dual-port RAM mode. The BCRTMP also uses it to select external memory during memory accesses.
$\overline{MEMCSI}$	64	H15	TUI	AL	Memory Chip Select In. Used in the pseudo-dual-port RAM mode only, $\overline{MEMCSI}$ is received from the host and is propagated through to $\overline{MEMCSO}$. This pin internally pulled high.
$\overline{RRD}$	70	F15	TO	AL	RAM Read. In the pseudo-dual-port RAM mode, the host uses this signal in conjunction with $\overline{MEMCSO}$ to read from external RAM through the BCRTMP. It is also the signal the BCRTMP uses to read from memory. It is asserted following receipt of $\overline{DMAG}$. When the BCRTMP performs multiple reads, this signal is pulsed.
$\overline{RWR}$	71	G14	TO	AL	RAM Write. In the pseudo-dual-port RAM mode, the CPU and BCRTMP use this to write to external RAM. This signal is asserted following receipt of $\overline{DMAG}$. For multiple writes, this signal is pulsed.

STATUS SIGNALS

NAME	PIN NUMBER F/P	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{STDINTL}}$	82	C13	TTO	ZL	Standard Interrupt Level. This is a level interrupt. It is asserted when one or more events enabled in either the Standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur. Resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register clears the interrupt.
$\overline{\text{STDINTP}}$	83	B14	TO	AL	Standard Interrupt Pulse. $\overline{\text{STDINTP}}$ pulses when an interrupt is logged.
$\overline{\text{HPINT}}$	84	B13	TTO	ZL	High-Priority Interrupt. The High-Priority Interrupt level is asserted upon occurence of events enabled in the High-Priority Interrupt Enable Register. The corresponding bit(s) in the High-Priority Interrupt Status/Reset Register reset $\overline{\text{HPINT}}$.
$\overline{\text{TIMRONA}}$	85	B12	TO	AL	Timer On - Channel A. When low, this pin indicates that the BCRTMP is transmitting data. This output remains active until the data transmission is complete or until the internal fail-safe timer times out (at 660 µs), indicating that the transceiver should be disabled.
$\overline{\text{TIMRONB}}$	86	C11	TO	AL	Timer On - Channel B. See $\overline{\text{TIMRONA}}$ description.
ACTIVE	81	D13	TO	AH	Activity on 1553 Bus. When high, this pin indicates that the BCRTMP has detected a valid command to any remote terminal address on the bus.
$\overline{\text{COMSTR}}$	90	C10	TO	AL	(RT) Command Strobe. The BCRTMP asserts this signal after receiving a valid command. The BCRTMP deactivates it after servicing the command.
SSYSF	128	G1	TI	AH	Subsystem Fail. Upon receipt, this signal propagates directly to the RT 1553 status word and the BCRTMP Status Register.
BCRTF	129	H2	TO	AH	BCRT Fail. This indicates a Built-In-Test (BIT) failure. In the RT mode, the Terminal Flag bit in 1553 status word is also set.
CHA/$\overline{\text{B}}$	89	A12	TO	--	Channel A/$\overline{\text{B}}$. This indicates the active or last active channel.
TEST	59	J14	TO	AL	TEST. This pin is used as a factory test pin. (Formerly $\overline{\text{MEMWIN}}$.)

BIPHASE INPUTS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
RAO	50	P14	TI	--	Receive Channel A One. This is the Manchester-encoded true signal input from Channel A of the bus receiver.
RAZ	51	N14	TI	--	Receive Channel A Zero. This is the Manchester-encoded complementary signal input from Channel A of the bus receiver.
RBO	54	N15	TI	--	Receive Channel B One. This is the Manchester-encoded true signal input from Channel B of the bus receiver.
RBZ	55	L14	TI	--	Receive Channel B Zero. This is the Manchester-encoded complementary signal input from Channel B of the bus receiver.

BIPHASE OUTPUTS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
TAO	52	M14	TO	--	Transmit Channel A One. This is the Manchester-encoded true output to be connected to the Channel A bus transmitter input. This signal is idle low.
TAZ	53	L13	TO	--	Transmit Channel A Zero. This is the Manchester-encoded complementary output to be connected to the Channel A bus transmitter input. This signal is idle low.
TBO	56	M15	TO	--	Transmit Channel B One. This is the Manchester-encoded true output to be connected to the Channel B bus transmitter input. This signal is idle low.
TBZ	57	K13	TO	--	Transmit Channel B Zero. This is the Manchester-encoded complementary output to be connected to the Channel B bus transmitter input. This signal is idle low.

DMA SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{DMAR}}$	72	F14	TTO	ZL	DMA Request. The BCRTMP issues this signal when access to RAM is required. It goes inactive after receiving a $\overline{\text{DMAG}}$ signal.
$\overline{\text{DMAG}}$	73	F13	TI	AL	DMA Grant. This input to the BCRTMP allows the BCRTMP to access RAM. It is recognized 45 ns before the rising edge of MCLKD2.
$\overline{\text{DMAGO}}$	78	E13	TTO	AL	DMA Grant Out. If $\overline{\text{DMAG}}$ is received but not needed, it passes through to this output.
$\overline{\text{DMACK}}$	75	D15	TO	ZL	DMA Acknowledge. The BCRTMP asserts this signal to confirm receipt of $\overline{\text{DMAG}}$; it stays low until memory access is complete.
BURST	77	D14	TO	AH	Burst (DMA Cycle). This indicates that the current DMA cycle transfers at least two words; worst case is five words plus a "dummy" word.
$\overline{\text{TSCTL}}$	76	C15	TO	AL	Three-State Control. This signal indicates when the BCRTMP is actually accessing memory. The host subsystem's address and data lines must be in the high-impedance state when the signal is active. This signal assists in placing the external data and address buffers into the high-impedance state.

MODE SELECT INPUTS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
MD7	23	R4	TUI	--	Mode 7. This input selects between two Remote Terminal Time Out (RTO) options. When this signal is high, the selected RTO is 16 μs. When this signal is low, the selected RTO is 32 μs.
MD6	22	P5	TUI	--	Mode 6. This input selects whether mode codes with data are allowed in the selected 1553 protocol. When this signal is high, the protocol does allow mode codes with data. When this signal is low, the protocol does not allow mode codes with data.
MD5	21	R3	TUI	--	Mode 5. This input selects the message error handling technique. When this signal is high, the message error handling technique is as defined in MIL-STD-1553B. When this signal is low, the message error handling technique is as defined in MACAIR A3818.
MD4	20	N5	TUI	--	Mode 4. This input selects between MIL-STD-1553A and MIL-STD-1553B status word protocol. When this signal is high, the selected status word protocol is the "B" option. When this signal is low, the selected status word protocol is the "A" option.
MD3	19	P4	TUI	--	Mode 3. This input selects between MIL-STD-1553A and MIL-STD-1553B mode code protocol. When this signal is high, the selected mode code protocol is the "B" option. When this signal is low, the selected mode code protocol is the "A" option.
MD2	18	P3	TUI	--	Mode 2. This input selects between MIL-STD-1553A and MIL-STD-1553B RT Response Time protocol. When this signal is high, the selected response time protocol is the "B" option. When this signal is low, the selected response time protocol is the "A" option.
MD1	17	P2	TUI	--	Mode 1. This input selects whether broadcast is allowed. When this signal is high, broadcast is allowed. When this signal is low, broadcast is not allowed. When MD1 is low, RT address 11111 is treated like RT addresses 00000-11110.
MD0	16	N3	TUI	--	Mode 0. This input selects the legalization method. When this signal is high, the DMA method of legalization is used. When this signal is low, the legalization bus is used.

MODE OUTPUTS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
MDO6	14	P1	TTO	--	Mode 6 Out. This output signal reflects the internal state of Mode 6 (MD6).
MDO5	13	N2	TTO	--	Mode 5 Out. This output signal reflects the internal state of Mode 5 (MD5).
MDO4	12	L3	TTO	--	Mode 4 Out. This output signal reflects the internal state of Mode 4 (MD4).
MDO3	11	M2	TTO	--	Mode 3 Out. This output signal reflects the internal state of Mode 3 (MD3).
MDO2	10	N1	TTO	--	Mode 2 Out. This output signal reflects the internal state of Mode 2 (MD2).
MDO1	9	M1	TTO	--	Mode 1 Out. This output signal reflects the internal state of Mode 1 (MD1).
MDO0	8	L1	TTO	--	Mode 0 Out. This output signal reflects the internal state of Mode 0 (MD0).

FORCED BUSY SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{FBUSY}}$	79	C14	TUI	AL	Forced Busy. This signal places the RT in a mode where it will automatically respond to a command with the Busy bit set in the RT status word. No DMA memory bus accesses are necessary, and the memory buses remain in the high-impedance state until the busy mode is exited. If the RT is involved in a 1553 message transaction, then entry into the busy state is held off until completion of the last DMA associated with that message. Upon entry into the busy state, the BCRTMP asserts the $\overline{\text{BUSYACK}}$ signal.
$\overline{\text{BUSYACK}}$	80	B15	TO	AL	Busy Acknowledge. This signal indicates that the BCRTMP has entered the Forced Busy state.

WRAP-AROUND TEST SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{WRAPEN}}$	6	K2	TUI	AL	Wrap-Around Enable. When this signal is low, the continuous wrap-around feature is enabled.
WRAPF	5	J2	TO	AH	Wrap Fail. When high, this pin indicates that the continuous wrap-around circuitry has detected a failure.
$\overline{\text{ALTWRAP}}$	4	K1	TUI	AL	Alternate Wrap-Around. This signal, when used in conjunction with $\overline{\text{WRAPEN}}$, places the BCRTMP in a special system diagnostic mode, where the two 1553 buses are connected by a stub, and commands transmitted over one bus are received through the continuous wrap circuitry on the other bus. This permits off-line testing of both channels and the associated 1553 interface components.

LEGALIZATION BUS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
LGL10	121	E2	TTO	--	Legalization bus bit 10. The Legalization bus bits 0-10 reflect bit times 19-9 of the current command (i.e., LGL10 = Current Command bit time 9 and LGL0 = Current Command bit time 19. This bus is used to determine whether or not the command is legal. This bus can also be used to selectively determine if auto-execution of a particular mode code is allowed.
LGL9	120	C1	TTO	--	Legalization bus bit 9.
LGL8	119	E3	TTO	--	Legalization bus bit 8.
LGL7	118	D2	TTO	--	Legalization bus bit 7.
LGL6	117	C2	TTO	--	Legalization bus bit 6.
LGL5	116	B2	TTO	--	Legalization bus bit 5.
LGL4	115	C3	TTO	--	Legalization bus bit 4. When the MACAIR A3818 method of error logging is selected, Legalization bus bits 4-0 reflect the word count for the defective data word.
LGL3	114	C4	TTO	--	Legalization bus bit 3.
LGL2	113	A2	TTO	--	Legalization bus bit 2.
LGL1	112	B3	TTO	--	Legalization bus bit 1.
LGL0	111	C5	TTO	--	Legalization bus bit 0.

LEGALIZATION SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{BRDCAST}}$	122	D1	TTO	AH	Broadcast. When high, this pin indicates that the current command is a broadcast command.
MC	123	F3	TTO	AH	Mode Code. When high, this pin indicates that the current command is a mode command.
LGLEN	127	F1	TTO	AL	Legalization Bus Enable. When low, this pin enables the user-supplied legalization logic (if the Legalization bus is used).
LGLCMD	124	F2	TUI	AH	Legal Command. A high on this input signal indicates to the BCRTMP that the current command is legal.
$\overline{\text{ERR}}$	125	G2	TO	AL	Error. When low, this pin indicates that a data word parity error or a Manchester error occurred in the current command. When this signal is asserted, the Legalization bus bits 4-0 contain the word count for the defective data word.
DOMC	126	G3	TUI	AH	Do Mode Code. When high, this signal enables the automatic execution of mode codes. When low, this signal disables auto-execution.

CLOCK SIGNALS

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
CLK	3	J1	TI	--	Clock. The 12 MHz input clock requires a 50% +/-10% duty cycle with an accuracy of +/-0.01%. The accuracy is required in order to meet the Manchester encoding/decoding requirements of MIL-STD-1553.
MCLK	58	K14	TI	--	Memory Clock. This is the input clock frequency the BCRTMP uses for memory accesses. The memory cycle time is equal to two MCLK cycles. Therefore, RAM access time is dependent upon the chosen MCLK frequency (6 MHz minimum, 12 MHz maximum). Please see the BCRTMP DMA timing diagrams in this data sheet.
MCLKD2	74	E15	TO	--	Memory Clock Divided by Two. This signal is the Memory Clock input divided by two. It assists the host subsystem in synchronizing DMA events.

POWER AND GROUND

NAME	PIN NUMBER F/P	PGA	TYPE	ACTIVE	DESCRIPTION
V_{DD}	132	H3	PWR	--	+5V
V_{DD}	34	N9	PWR	--	+5V
V_{DD}	67	G13	PWR	--	+5V
V_{DD}	100	C7	PWR	--	+5V
V_{SS}	1	J3	GND	--	Ground
V_{SS}	33	N8	GND	--	Ground
V_{SS}	66	H13	GND	--	Ground
V_{SS}	99	C8	GND	--	Ground

3.0 Internal Registers

The BCRTMP's internal registers (see table 1 on pages 23-24) enable the CPU to control the actions of the BCRTMP while maintaining low DMA overhead by the BCRTMP. All functions are active high and ignored when low unless stated otherwise. Functions and parameters are used in both RT and BC modes except where indicated. Registers are addressed by the binary equivalent of their decimal number. For example, Register 1 is addressed as 0001B. Register usage is defined as follows:

#0 Control Register

Bit Number	Description
BITs 15-13	Reserved.
BIT 12	(BC,RT) MD7 (Mode 7). Remote Terminal Time-Out Option Select. When high, this bit selects a Remote Terminal Time-Out that is nominally 32 µs. When low, this bit selects a Remote Terminal Time-Out that is nominally 16 µs.
BIT 11	Enable External Override. For use in multi-redundant systems. This bit enables the $\overline{\text{EXTOVR}}$ pin.
BIT 10	BC/$\overline{\text{RT}}$ Select. This function selects between the Bus Controller and Remote Terminal operation modes. It overrides the external BCRTSEL input setting if the Change Lock-Out function is not used. A reset operation must be performed when changing between BC and RT modes. This bit is write-only.
BIT 9	(BC) Retry on Alternate Bus. This bit enables an automatic retry to operate on alternate buses. For example, if on bus A, with two automatic retries programmed, the automatic retries occur on bus B.
BIT 8	(RT) Channel B Enable. When set, this bit enables Channel B operation. (BC) No significance.
BIT 7	(RT) Channel A Enable. When set, this bit enables Channel A operation. (BC) Channel Select A/$\overline{\text{B}}$. When set, this bit selects Channel A.
BITs 6-5	(BC) Retry Count. These bits program the number (1-4) of retries to attempt. (00 = 1 retry, 11 = 4 retries)
BIT 4	(BC) Retry on Bus Controller Message Error. This bit enables automatic retries on an error the bus controller detects (see the Bus Controller Architecture section, page 35).
BIT 3	(BC) Retry on Time-Out. This bit enables an automatic retry on a response time-Out condition.
BIT 2	(BC) Retry on Message Error. This bit enables an automatic retry when the Message Error bit is set in the RT's status word response.
BIT 1	(BC) Retry on Busy. This bit enables automatic retry on a received Busy bit in an RT status word response.
BIT 0	Start Enable. In the BC mode, this bit starts/restarts Command Block execution. In the RT mode, it enables the BCRTMP to receive a valid command. RT operation does not start until a valid command is received. When using this function: • Restart the BCRTMP after each Master Reset or programmed reset. • This bit is not readable; verify operation by reading bit 0 of the BCRTMP's Status Register.

#1 Status Register (Read Only)
These bits indicate the BCRTMP's current status.

Bit Number	Description
BIT 15	TEST. This bit reflects the inverse of the TEST output. It changes state simultaneously with the TEST output.
BIT 14	(RT) Remote Terminal Active. Indicates that the BCRTMP, in the Remote Terminal mode, is presently servicing a command. This bit reflects the inverse of the $\overline{\text{COMSTR}}$ pin.
BIT 13	(RT) Dynamic Bus Control Acceptance. This bit reflects the state of the Dynamic Bus Control Acceptance bit in the RT status word (see Register 10 on page 20).
BIT 12	(RT) Terminal Flag bit is set in RT status word. See also section 8.2.8.10.
BIT 11	(RT) Service Request bit is set in RT status word. See also section 8.2.8.4.
BIT 10	(RT) Busy bit is set in RT status word. See also section 8.2.8.7.
BIT 9	BIT is in progress.
BIT 8	Reset is in progress. This bit indicates that either a write to Register 12 has just occurred or the BCRTMP has just received a Reset Remote Terminal (#01000) Mode Code. This bit remains set less than one microsecond.
BIT 7	BC/($\overline{\text{RT}}$) Mode. Indicates the current mode of operation. A reset operation must be performed when changing between BC and RT modes.
BIT 6	Channel A/$\overline{\text{B}}$. Indicates either the channel presently in use or the last channel used.
BIT 5	Subsystem Fail Indicator. Indicates receiving a subsystem fail signal from the host subsystem on the SSYSF input.
BITs 4-1	Reserved.
BIT 0	(BC) Command Block Execution is in progress. (RT) Remote Terminal is in operation. This bit reflects bit 0 of Register 0.

#2 Current Command Block Register (BC)/Remote Terminal Descriptor Space Address Register (RT)
(BC) This register contains the address of the head pointer of the Command Block being executed. Accessing a new Command Block updates it.

(RT) The host CPU initializes this register to indicate the starting location of the RT Descriptor Space. The host must allocate 320 sequential locations following this starting address. For proper operation, this location must start on an I x 512 decimal address boundary, where I is an integer multiple.

#3 Polling Compare Register
In the polling mode, the CPU sets the Polling Compare Register to indicate the RT response word on which the BCRTMP should interrupt. This register is 11 bits wide, corresponding to bit times 9 through 19 of the RT's 1553 status word response. The sync, Remote Terminal Address, and parity bits are not included (see the section on Polling, page 38).

#4 BIT (Built-In-Test) Word Register
The BCRTMP uses the contents of this register when it responds to the Transmit BIT Word Mode Code (#10011). In addition, the BCRTMP writes to the two most significant bits of the BIT Word Register in response to either an Initiate Self-Test Mode Code (RT mode) or a write to Register 11 (BIT Start Command) to indicate a BIT failure. If the BIT Word needs to be modified, it can be read out, modified, then rewritten to this register. Note that if the processor writes a "1" to either bit 14 or 15 of this register, it effectively induces a BIT failure. Also note that during normal RT operation, bits 10 through 13 of this register indicate specific types of message errors, as shown below.

Bit Number	Description
BIT 15	Channel B failure.
BIT 14	Channel A failure.
BIT 13	Word Count Error.
BIT 12	Parity Error.
BIT 11	Manchester Error.
BIT 10	Remote Terminal Time-Out.
BITs 9-0	BIT Word. The least significant ten bits of the BIT Word are user programmable.

#5 Current Command Register (Read Only)
In the RT, this register contains the command currently being processed. When not processing a command, the BCRTMP stores the last command/status word transmitted on the 1553 bus in this register. This register is updated only when bit 0 of Register 0 is set. In the BC mode, this register contains the most current command sent out on the 1553 bus.

#6 Interrupt Log List Pointer Register
Initialized by the CPU, the Interrupt Log List Pointer Register indicates the start of the Interrupt Log List. After each list entry, the BCRTMP updates this register with the address of the next entry in the list. (See page 45-46.)

#7 High-Priority Interrupt Enable Register (Read/Write)
Setting the bits in this register causes a High-Priority Interrupt when the enabled event occurs. If enabled in Register 14, setting these bits also determines which events trigger the Stop Enable feature. To service the High-Priority Interrupt, the user reads Register 8 to determine the cause of the interrupt, then writes to Register 8 to clear the appropriate bits. The BCRTMP also provides a Standard Priority Interrupt Scheme that does not require host intervention. If High-Priority Interrupt service is not possible in a given application, it is advisable to use the Standard Priority features.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun Enable. When set, this bit enables an interrupt when $\overline{\text{DMAG}}$ was not received by the BCRTMP within the allotted time needed for a successful data transfer to memory.
BIT 7	(BC) Illogical Command Error Enable. This bit enables a High-Priority Interrupt to be asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formatted RT-RT Command Blocks.
BIT 6	(RT) Dynamic Bus Control Mode Code Interrupt Enable. When set, an interrupt is asserted when the Dynamic Bus Control Mode Code is received, provided the T/R bit is "1," the command is legal, and DOMC is active.
BIT 5	Subsystem Fail Enable. When set, a High-Priority Interrupt is asserted after receiving a Subsystem Fail (SSYSF) input pin.
BIT 4	End of BIT Enable. This bit indicates the end of the internal BIT routine.
BIT 3	BIT Word Fail Enable. This bit enables an interrupt indicating that the BCRTMP detected a BIT failure.
BIT 2	(BC) End of Command Block List Enable (see Command Block Control Word, page 37.) This interrupt can be superseded by other high-priority interrupts.
BIT 1	Message Error Enable. If enabled, a High-Priority Interrupt is asserted at the occurrence of a message error. If a High-Priority Interrupt condition occurs, as the result of an enabled message error, the device will halt operation until the user clears the interrupt by writing a "1" to bit 1 of the High-Priority Interrupt Status/Reset Register (Reg. #8). If this interrupt is not cleared, the BCRTMP remains in the HALTED state (appearing to be "locked-up"), even if it receives a valid message. This High-Priority Interrupt scheme is necessary in order to maintain the BCRTMP's state of operation so that the host CPU has this information available at the time of interrupt service.
BIT 0	Standard Interrupt Enable. Setting this bit enables the $\overline{\text{STDINTL}}$ pin, but does not cause a high-priority interrupt. If the user wants the Stop Enable feature activated for Standard Interrupts, this bit must be set. If low, only the $\overline{\text{STDINTL}}$ pin is asserted when a Standard Interrupt occurs.

#8 High-Priority Interrupt Status/Reset Register
When a High-Priority Interrupt is asserted, this register indicates the event that caused it. To clear the interrupt signal and reset the bit, write a "1" to the appropriate bit. See the corresponding bit definitions of Register 7, High-Priority Interrupt Enable Register.

Bit Number	Description
BITs 15-9	Reserved.
BIT 8	Data Overrun.
BIT 7	Illogical Command.
BIT 6	Dynamic Bus Control Accepted.
BIT 5	Subsystem Fail.

BIT 4	End of BIT.
BIT 3	BIT Word Fail.
BIT 2	End of Command Block.
BIT 1	Message Error.
BIT 0	Standard Interrupt. The BCRTMP sets this bit when any Standard Interrupt occurs, providing bit 0 of Register 7 is enabled.

#9 Standard Interrupt Enable Register

This register enables Standard Interrupt logging for any of the following enabled events (Standard Interrupt logging can also occur for events enabled in the BC Command Block or RT Subaddress/Mode Code Descriptor):

Bit Number	Description
BITs 15-6	Reserved.
BIT 5	(RT) Illegal Broadcast Command. When set, this bit enables an interrupt indicating that an Illegal Broadcast Command has been received.
BIT 4	(RT) Illegal Command. When set, this bit enables an interrupt indicating that an illegal command has been received.
BIT 3	(BC) Polling Comparison Match. This enables an interrupt indicating that a polling event has occurred. The user must also set bit 12 in the BC Command Block Control Word for this interrupt to occur.
BIT 2	(BC) Retry Fail. This bit enables an interrupt indicating that all the programmed number of retries have failed.
BIT 1	(BC,RT) Message Error Event. This bit enables a standard interrupt for message errors.
BIT 0	(BC) Command Block Interrupt and Continue. This bit enables an interrupt indicating that a Command Block, with the Interrupt and Continue Function enabled, has been executed.

#10 Remote Terminal Address Register

This register sets the Remote Terminal Address via software. The Change Lock-Out Enable feature, when set, prevents the Remote Terminal Address or the BCRTMP Mode Selection from changing. Note that MD4 also controls the effect of BITs 9-15 on status word generation. See section 8.2.8.

Bit Number	Description
BIT 15	(RT) Instrumentation. Setting this bit sets the RT status word Instrumentation bit.
BIT 14	(RT) Busy. Setting this bit sets the RT status word Busy bit. It does not inhibit data transfers to the subsystem.
BIT 13	(RT) Subsystem Fail. Setting this bit sets the RT status word Subsystem Flag bit. In the RT mode, the Subsystem Fail is also logged into the Message Status Word.
BIT 12	(RT) Dynamic Bus Control Acceptance. Setting this bit sets the RT status word Dynamic Bus Control Acceptance bit when the BCRTMP receives the Dynamic Bus Control Mode Code from the currently active Bus Controller. Host intervention is required for the BCRTMP to take over as the active Bus Controller.
BIT 11	(RT) Terminal Flag. Setting this bit sets the RT status word Terminal Flag bit; the Terminal Flag bit in the RT status word is also internally set if the BIT fails.
BIT 10	(RT) Service Request. Setting this bit sets the RT status word Service Request bit.
BIT 9	(RT) Busy Mode Enable. Setting this bit sets the RT status word Busy bit and inhibits all data transfers to the subsystem. (See Forced Busy Mode, section 8.2.4.)
BIT 8	BC/$\overline{RT}$ Mode Select. This bit's state reflects the external pin BCRTSEL. It does not necessarily reflect the state of the chip, since the BC/$\overline{RT}$ Mode Select is software-programmable via bit 10 of Register 0. This bit is read-only.
BIT 7	Change Lock-Out. This bit's state reflects the external pin LOCK. When set, this bit indicates that changes to the RT address or the BC/$\overline{RT}$ Mode Select are not allowed using internal registers. This bit is read-only.
BIT 6	Remote Terminal Address Parity Error. This bit indicates a Remote Terminal Address Parity error. It appears after the Remote Terminal Address is latched if a parity error exists.

BIT 5 Remote Terminal Address Parity. This is an odd parity input bit used with the Remote Terminal Address. It ensures accurate recognition of the Remote Terminal Address.

BITs 4-0 Remote Terminal Address (Bit 0 is the LSB). This reflects the RTA4-0 inputs at Master Reset. Modify the Remote Terminal Address by writing to these bits.

#11 BIT Start Register (Write Only)

Any write (i.e., data = don't care) to this register's address location initiates the internal BIT routine, which lasts 100 µs. Verify using the BIT-in-Progress bit in the Status Register. If the BCRTMP is online (Bit 0 of Register 1 is high), a programmed reset (write to Register 12) must precede a write to this register to initiate the internal BIT.

The BCRTMP's self-test performs an internal wrap-around test between its Manchester encoder and its two Manchester decoders. If the BCRTMP detects a failure on either the primary or the secondary channel, it flags this failure by setting bit 14 of Register 4 (BIT Word Register) for Channel A and/or bit 15 for Channel B. When in the Remote Terminal mode, while the BCRTMP is performing its self-test, it ignores any commands on the 1553 bus until it has completed the self-test.

#12 Programmed Reset Register (Write Only)

Any write (i.e., data = don't care) to this register's address location initiates a reset sequence of the encoder/decoder and protocol sections of the BCRTMP which lasts less than 1 microsecond. This is identical to the reset used for the Reset Remote Terminal Mode Code except that command processing halts. For a total reset (i.e., including registers), see the $\overline{\text{MRST}}$ signal description.

#13 RT Timer Reset Register (Write Only)

Any write (i.e., data = don't care) to this register's address location resets the RT Time Tag timer to zero. The BCRTMP's Remote Terminal Timer time-tags message transactions. The time tag is generated from a free-running eight-bit timer of 64 microseconds resolution. This timer can be reset to zero simply by writing to Register 13. When the timer is reset, it immediately starts running.

#14 Activity Status/Operational Mode Register

BITs 15-14 Reserved.

BIT 13 Ignore T/R bit in Mode Command. When high, this bit causes the BCRTMP to ignore the value of the T/R bit in 1553 Mode Commands 0-15 (mode codes without data) and prevents automatic execution of modes 18-19. This feature is used in conjunction with Operational Mode 6 (input pin MD6).

BIT 12 Stop Enable. When the BCRTMP is in the RT mode, this bit enables a feature that places the BCRTMP into the Forced Busy Mode when an interrupt (either Standard or High-Priority) occurs. When the BCRTMP enters the Forced Busy Mode, the device responds with the Busy bit set in the 1553 status word any time a valid 1553 command is received. When the interrupt is cleared, the BCRTMP exits the Forced Busy Mode.

For BC operation, setting the Stop Enable bit causes the BCRTMP to halt Command Block execution when an enabled interrupt (either Standard or High-Priority) occurs. Command Block execution resumes when the user clears the interrupt by writing a "1" to the appropriate bit in Register 8.

BIT 11 Bus B Active. This bit goes high when the BCRTMP, acting as a Remote Terminal, receives a valid 1553 command on the secondary bus.

BIT 10 Bus A Active. This bit goes high when the BCRTMP, acting as a Remote Terminal, receives a valid 1553 command on the primary bus.

BIT 9 WRAPF Wrap-Around Test Fail. This bit reflects the state of the WRAPF output signal.

BIT 8 $\overline{\text{ALTWRAP}}$ Alternate Channel Wrap-Around Test Enable. After Master Reset, this bit reflects the complement of the state of the $\overline{\text{ALTWRAP}}$ input signal. This bit can be software-modified if the LOCK pin is low. Thus, to enable the $\overline{\text{ALTWRAP}}$ feature, write a one to this bit location.

BIT 7 $\overline{\text{WRAPEN}}$ Wrap-Around Test Enable. After Master Reset, this bit reflects the complement of the state of the $\overline{\text{WRAPEN}}$ input signal. This bit can be software-modified if the LOCK pin is low. Thus, to enable the $\overline{\text{WRAPEN}}$ feature, write a one to this bit location.

BIT 6 MD6 Operational Mode 6. After Master Reset, this bit reflects the state of the corresponding input pin (MD6). See section 8.1.7 for a summary of Operational Mode 6. This bit can be software-modified if the LOCK pin is low.

BIT 5 MD5 Operational Mode 5. After Master Reset, this bit reflects the state of the corresponding input pin (MD5). See section 8.1.6 for a summary of Operational Mode 5. This bit can be software-modified if the LOCK pin is low.

BIT 4 MD4 Operational Mode 4. After Master Reset, this bit reflects the state of the corresponding input pin (MD4). See section 8.1.5 for a summary of Operational Mode 4. This bit can be software-modified if the LOCK pin is low.

BIT 3 MD3 Operational Mode 3. After Master Reset, this bit reflects the state of the corresponding input pin (MD3). See section 8.1.4 for a summary of Operational Mode 3. This bit can be software-modified if the LOCK pin is low.

BIT 2 MD2 Operational Mode 2. After Master Reset, this bit reflects the state of the corresponding input pin (MD2). See section 8.1.3 for a summary of Operational Mode 2. This bit can be software-modified if the LOCK pin is low.

BIT 1 MD1 Operational Mode 1. After Master Reset, this bit reflects the state of the corresponding input pin (MD1). See section 8.1.2 for a summary of Operational Mode . This bit can be software-modified if the LOCK pin is low.

BIT 0 MD0 Operational Mode 0. After Master Reset, this bit reflects the state of the corresponding input pin (MD0). See section 8.1.1 for a summary of Operational Mode 0. This bit can be software-modified if the LOCK pin is low.

#15 Programmable Status/Last Status Word Register (RT)

This register provides control of and access to the RT Status Word. Bits 15-12 (read/write) allow for special operations on some or all of the Status Word bits. Writing to bit 11 places the BCRTMP into the Forced Busy mode. Reading this bit will verify that the BCRTMP has entered the Forced Busy mode (see section 8.2.4). Writing to the remaining bits (bits 10-0) of this register allows control of the RT Status Word (see section 8.2.8). When reading from this register, bits 10-0 indicate the last Status Word sent by the BCRTMP.

BIT 15 Immediate Clear Mode Enable. When set, this bit will cause the BCRTMP to automatically clear all programmable status bits (bits 10-0 of this register and bits 15-9 of Register 10) after the BCRTMP transmits the RT Status Word. When this bit is set, the first Status Word sent out contains the Status Word created from the programmable status bits in this register, Register 10, and from internally generated conditions (see section 8.2.8). After Status Word transmission, the BCRTMP clears bits 10-0 of this register and bits 15-9 of Register 10. There is one exception to this automatic status bit clearing. When the next command received is the Transmit Status Word or Transmit Last Command mode code, the BCRTMP will respond with the appropriate Status Word from the previous valid command. This feature applies to all operational modes. Note that inhibition of the Terminal Flag bit (receipt of Mode Code 6) is also cleared by this bit.

BIT 14 Automatic Terminal Flag Bit Enable, Option 1. When set, this bit will cause the Terminal Flag to be automatically set when any of the Status Word field bits are set (Status Word bit times 9 through 18).

BIT 13 Automatic Terminal Flag Bit Enable, Option 2. When set, this bit will cause the Terminal Flag to be automatically set when the Busy or Subsystem Flag Status Word bits are set. If both bits 14 and 13 of this register are set, neither option is selected, and the Busy bit will not be set by the Forced Busy mode. These automatic Terminal Flag bit options apply for all operational modes.

BIT 12 Automatic Data Ready. This bit, when set, causes the BCRTMP to place the complement of the Busy Bit in the Data Ready Bit (bit 8). Therefore, when the BCRTMP transmits the Status Word, bit 8 = NOT bit 3.

BIT 11 Forced Busy.

BIT 10 ME Message Error (Bit Time 9)/Last Status Word Message Error Bit.

BIT 9 PSBT10 Programmable Status Bit Time 10/Last Status Word Bit Time 10.

BIT 8 PSBT11 Programmable Status Bit Time 11/Last Status Word Bit Time 11.

BIT 7 PSBT12 Programmable Status Bit Time 12/Last Status Word Bit Time 12.

BIT 6 PSBT13 Programmable Status Bit Time 13/Last Status Word Bit Time 13.

BIT 5 PSBT14 Programmable Status Bit Time 14/Last Status Word Bit Time 14.

BIT 4 PSBT15 Programmable Status Bit Time 15/Last Status Word Bit Time 15.

BIT 3 PSBT16 Programmable Status Bit Time 16/Last Status Word Bit Time 16.

BIT 2 PSBT17 Programmable Status Bit Time 17/Last Status Word Bit Time 17.

BIT 1 PSBT18 Programmable Status Bit Time 18/Last Status Word Bit Time 18.

BIT 0 TF Terminal Flag (Bit Time 19)/Last Status Word Terminal Flag Bit.

#0 BC/RT CONTROL REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	RTO	EXTOVR	BC/RT	RTYALTB	BUSBEN
7	6	5	4	3	2	1	0
CHNSEL BUSAEN	RTYCNT		RTYBCME	RTYTO	RTYME	RTYBSY	STEN

#1 BC/RT STATUS REGISTER

15	14	13	12	11	10	9	8
TEST	RTACT	DYNBUS	RT FLAG	SRQ	BUSY	BIT	RESET
7	6	5	4	3	2	1	0
BC/RT	BUSA/B	SSFAIL	UNUSED	UNUSED	UNUSED	UNUSED	CMBKPG

#2 (BC) CURRENT COMMAND BLOCK REGISTER
(RT) REMOTE TERMINAL DESCRIPTOR SPACE ADDRESS REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#3 POLLING COMPARE REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	MSGERR	SWBT10	SWBT11
7	6	5	4	3	2	1	0
SWBT12	SWBT13	SWBT14	SWBT15	SWBT16	SWBT17	SWBT18	TF

#4 BIT WORD REGISTER

15	14	13	12	11	10	9	8
CHBFAIL	CHAFAIL	WCERR	PARERR	MANERR	RTTO	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#5 CURRENT COMMAND REGISTER

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

#6 INTERRUPT LOG LIST POINTER REGISTER

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

#7 BCRTMP HIGH-PRIORITY INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

Table 1. BCRTMP Registers (continued)

#8 BCRTMP HIGH-PRIORITY INTERRUPT STATUS/RESET REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	DATOVR
7	6	5	4	3	2	1	0
ILLCMD	DYNBUS	SSFAIL	ENDBIT	BITFAIL	EOL	MSGERR	STDINT

#9 STANDARD INTERRUPT ENABLE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
7	6	5	4	3	2	1	0
UNUSED	UNUSED	ILLBCMD	ILLCMD	POLMTCH	RTYFAIL	MSGERR	CMDBLK

#10 REMOTE TERMINAL ADDRESS REGISTER

15	14	13	12	11	10	9	8
INSTR	BUSY2	SS FLAG	DBC	RT FLAG	SRQ	BUSY1	BC/RT
7	6	5	4	3	2	1	0
LOCK	PARERR	RTAPAR	RTA4	RTA3	RTA2	RTA1	RTA0

#11 BUILT-IN-TEST START REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#12 PROGRAMMED RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#13 REMOTE TERMINAL TIMER RESET REGISTER

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

#14 ACTIVITY STATUS/OPERATIONAL MODE REGISTER

15	14	13	12	11	10	9	8
UNUSED	UNUSED	IGNORTR	STPEN	B ACT	A ACT	WRAPF	ALTWRAP
7	6	5	4	3	2	1	0
WRPEN	MD6	MD5	MD4	MD3	MD2	MD1	MD0

#15 PROGRAMMABLE STATUS REGISTER

15	14	13	12	11	10	9	8
IMM CLR	TF OPT1	TF OPT2	PS8=NB	FBUSY	ME	PSBT10	PSBT11
7	6	5	4	3	2	1	0
PSBT12	PSBT13	PSBT14	PSBT15	PSBT16	PSBT17	PSBT18	TF

X= DON'T CARE

Table 1. BCRTMP Registers (continued from page 23)

4.0 System Overview

The BCRTMP can be configured for a variety of processor and memory environments. The host processor and the BCRTMP communicate via a flexible, programmable interrupt structure, internal registers, and a user-definable shared memory area. The shared memory area (up to 64K) is completely user-programmable and communicates BCRTMP control information -- message data, and status/error information.

Built-in memory management functions designed specifically for MIL-STD-1553 applications aid processor off-loading. The host needs only to establish the parameters within memory so the BCRTMP can access this information as required. For example, in the RT mode, the BCRTMP can store data associated with individual subaddresses anywhere within its 64K address space. The BCRTMP then can automatically buffer up to 128 incoming messages of the same subaddress, thus preventing the previous messages from being overwritten by subsequent messages. This buffering also extends the intervals required by the host processor to service the data. Selecting an appropriate MCLK frequency to meet system memory access time requirements controls the memory access rate. The completion of a user-defined task or the occurrence of a user-selected event is indicated by using the extensive set of interrupts provided.

In the BC mode, the BCRTMP can process multiple messages, assist in scheduling message lists, and provide host-programmable functions such as auto retry. The BCRTMP is incorporated in systems with a variety of interrupt latencies by using the Interrupt History List feature (see Exception Handling and Interrupt Logging, page 45). The Interrupt History List sequentially stores the events that caused the interrupt in memory without losing information if a host processor does not respond immediately to an interrupt.

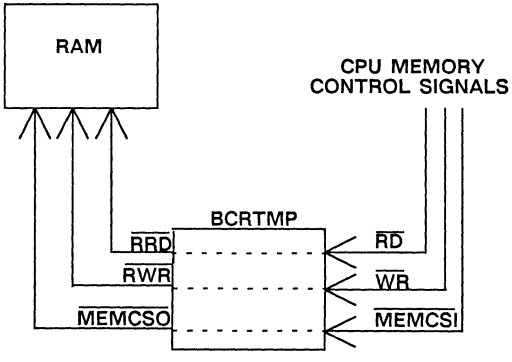


Figure 3a. Pseudo-Dual-Port RAM Control Signals

5.0 System Interface

5.1 DMA Transfers

The BCRTMP initiates DMA transfers whenever it executes command blocks (BC mode) or services commands (RT mode). $\overline{\text{DMAR}}$ initiates the transfer and is terminated by the inactive edge of $\overline{\text{DMACK}}$. The Address Enable (AEN) input enables the BCRTMP to output an address onto the Address bus.

The BCRTMP requests transfer cycles by asserting the $\overline{\text{DMAR}}$ output, and initiates them when a $\overline{\text{DMAG}}$ input is received. A $\overline{\text{DMACK}}$ output indicates that the BCRTMP has control of the Data and Address buses. The $\overline{\text{TSCTL}}$ output is asserted when the BCRTMP is actually asserting the Address and Data buses.

To support using multiple bus masters in a system, the BCRTMP outputs the $\overline{\text{DMAGO}}$ signal that results from the $\overline{\text{DMAG}}$ signal passing through the chip when a BCRTMP bus request was not generated ($\overline{\text{DMAR}}$ inactive). You can use $\overline{\text{DMAGO}}$ in daisy-chained multimaster systems.

5.2 Hardware Interface

The BCRTMP provides a simple subsystem interface and facilitates DMA arbitration. The user can configure the BCRTMP to operate in a variety of memory-processor environments including pseudo-dual-port RAM and standard DMA configurations.

For complete circuit description, such as arbitration logic and I/O, please refer to the appropriate application note.

5.3 CPU Interconnection

Pseudo-Dual-Port RAM Configuration

The BCRTMP's Address and Data buses connect directly to RAM, with buffers isolating the BCRTMP's buses from those of the host CPU (figures 3a and 3b). The CPU's memory control signals ($\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{MEMCSI}}$) pass through the BCRTMP and connect to memory as $\overline{\text{RRD}}$, $\overline{\text{RWR}}$, and $\overline{\text{MEMCSO}}$.

Standard DMA Configuration

The BCRTMP's and CPU's data, address, and control signals are connected to each other as shown in figures 3c and 3d. The $\overline{\text{RWR}}$, $\overline{\text{RRD}}$, and $\overline{\text{MEMCSO}}$ are activated after $\overline{\text{DMAG}}$ is asserted.

In either case, the BCRTMP's Address and Data buses remain in a high-impedance state unless the $\overline{\text{CS}}$ and $\overline{\text{RD}}$

signals are active, indicating a host register access; or $\overline{\text{TSCTL}}$ is asserted, indicating a memory access by the BCRTMP. CPU attempts to access BCRTMP registers are ignored during BCRTMP memory access. Inhibit DMA transfers by using the Busy function in the Remote Terminal Address Register while operating in the Remote Terminal mode.

The designer can use $\overline{\text{TSCTL}}$ to indicate when the BCRTMP is accessing memory. AEN is also available (use is optional), giving the CPU control over the BCRTMP's Address bus. A DMA Burst (BURST) signal indicates multiple DMA accesses.

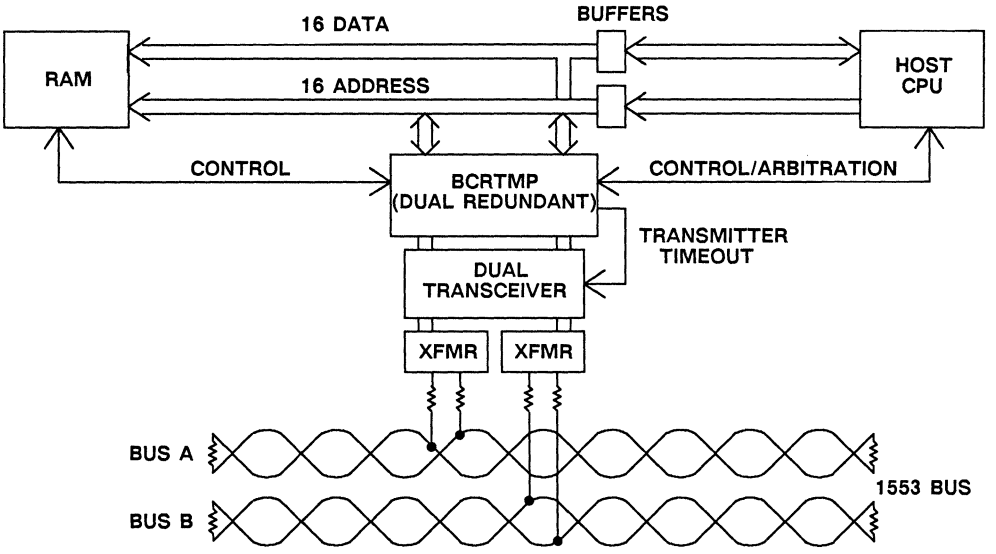


Figure 3b. CPU/BCRTMP Interface -- Pseudo-Dual-Port RAM Configuration

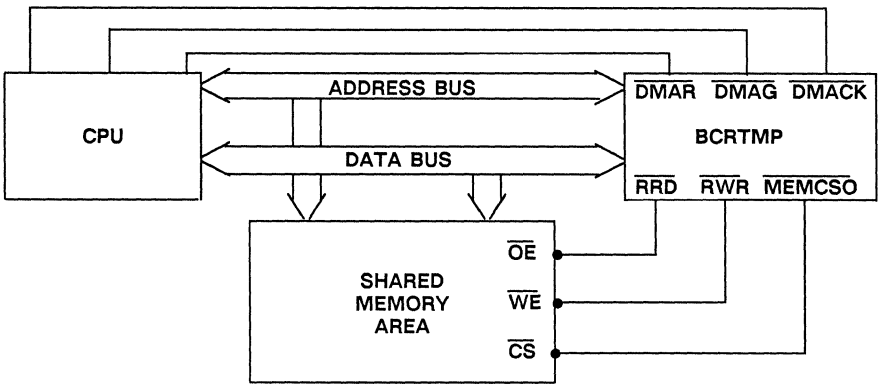


Figure 3c. DMA Signals

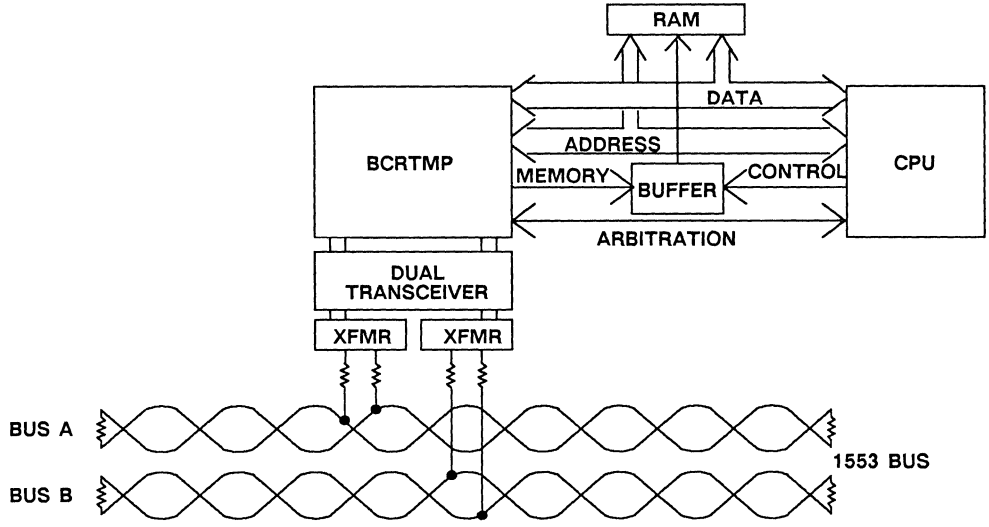


Figure 3d. CPU/BCRTMP Interface -- DMA Configuration

Register Access
Registers 0 through 15 are accessed with the decode of the four LSBs of the Address bus (A0-A3) and asserting $\overline{CS}$. Pulse either $\overline{RD}$ or $\overline{WR}$ for multiple register accesses.

5.4 RAM Interface
The BCRTMP's $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ signals serve as read and write controls during BCRTMP memory accesses. The host subsystem signals $\overline{RD}$, $\overline{WR}$, and $\overline{MEMCSI}$ propagate through the BCRTMP to become $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$ outputs to support a pseudo-dual-port. During BCRTMP-RAM data transfers, the host subsystem's memory signals are ignored until the BCRTMP access is complete.

5.5 Legalization Bus
In the RT mode, when the UT1553 BCRTMP receives a command on the 1553 bus, it must determine whether that command is legal. The BCRTMP provides two methods for the designer to accomplish this task. With the first method, called DMA Legalization, the BCRTMP automatically accesses a specific Descriptor Block when it receives a command to a given subaddress (or mode code). This Descriptor Block (see figure 4a) contains information that the BCRTMP uses to determine if the command is legal or illegal. With the second method, called Bus Legalization, the 1553 Command Word, minus the RT Address, is routed to the Legalization bus outputs of the BCRTMP (see figure 4b). The BCRTMP uses this information, for example, as a PROM address. The single-bit output from the PROM then feeds the LGLCMD input signal of the BCRTMP (see figure 4c). If the command is legal, the PROM output is high; if the command is illegal, the PROM output is low. Figure 31 shows the required timing for the BCRTMP Legalization bus.

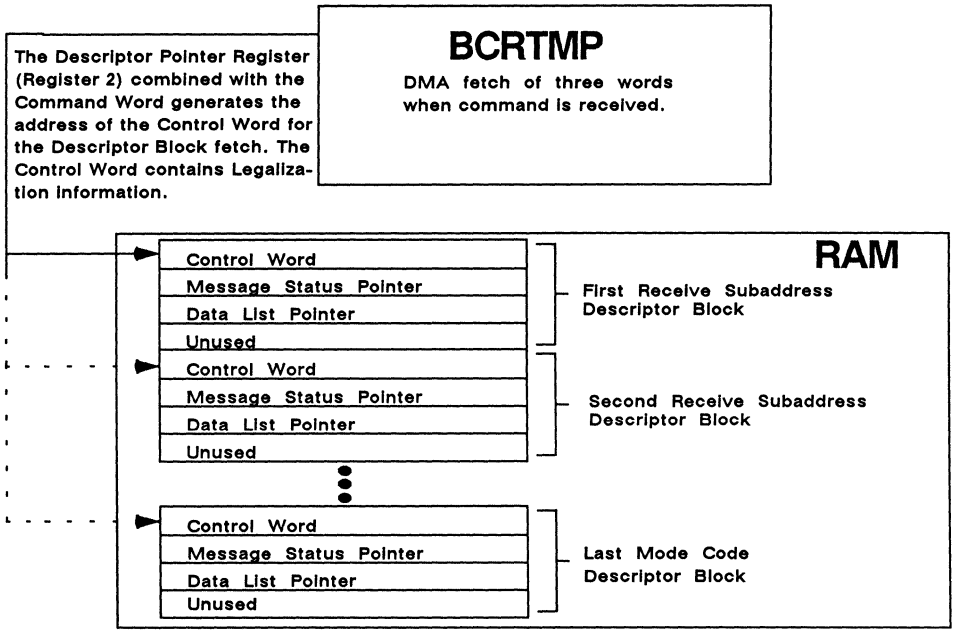


Figure 4a. BCRTMP Descriptor Block Legalization

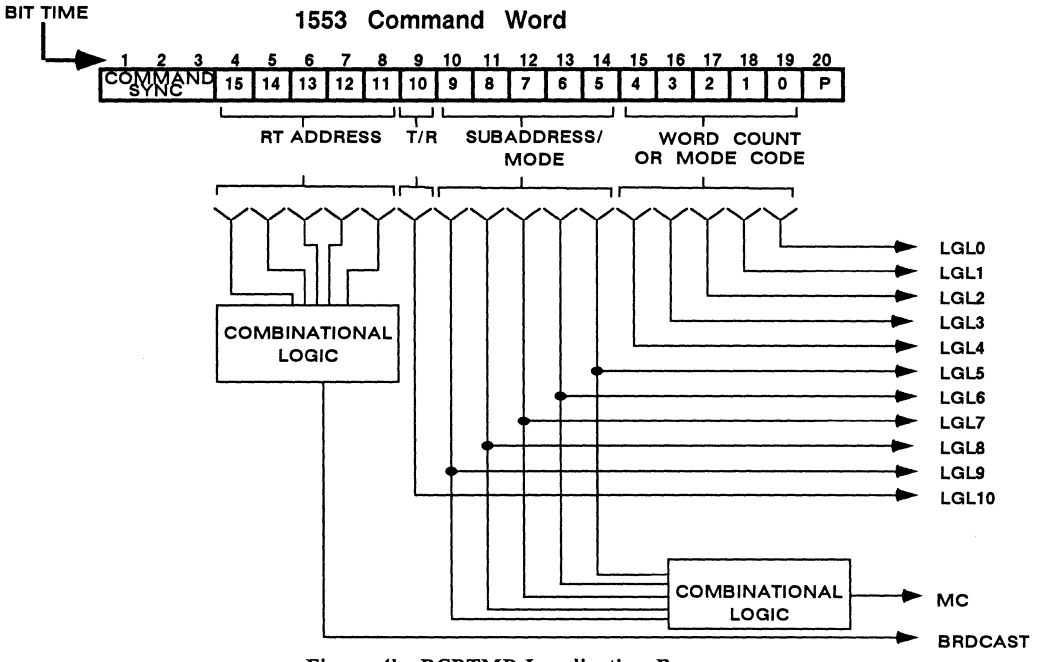


Figure 4b. BCRTMP Legalization Bus

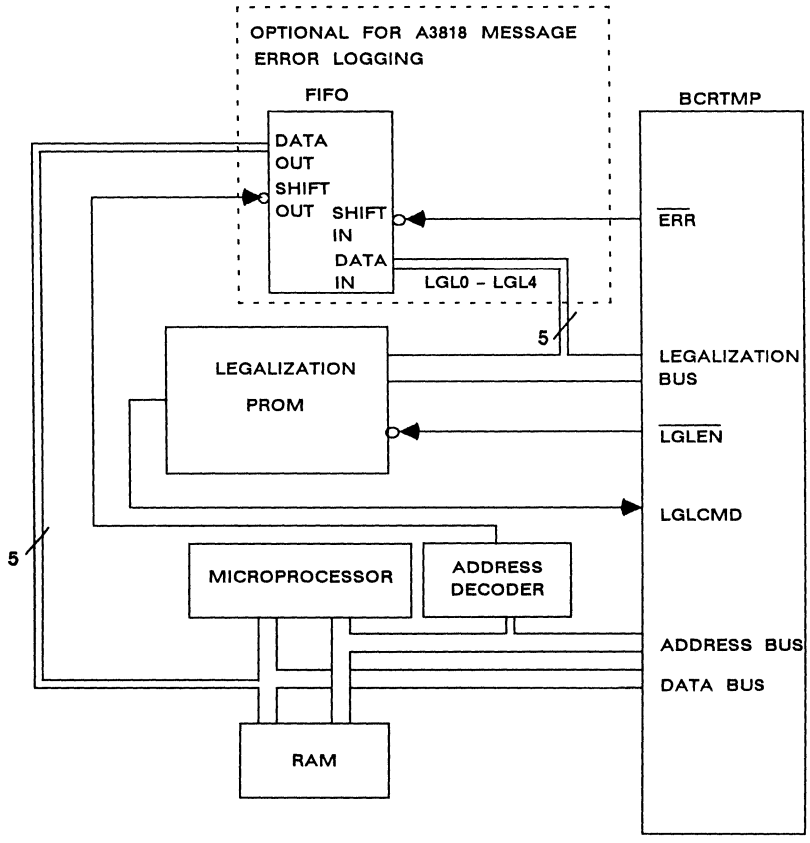


Figure 4c. BCRTMP Bus Legalization Example

To facilitate on-board programming of the 5-volt EEPROMs on the host board, the BCRTMP places the Legalization bus into the high-impedance state when the user asserts the $\overline{\text{MRST}}$ signal.

5.6 Transmitter/Receiver Interface

The BCRTMP's Manchester II encoder/decoder interfaces directly with the 1553 bus transceiver, using the TAO-TAZ and RAZ-RAO signals for Channel A, and TBO-TBZ and RBZ-RBO signals for Channel B.

The BCRTMP also provides $\overline{\text{TIMRONA}}$ and $\overline{\text{TIMRONB}}$ signal outputs and an active channel output indicator (CHA/$\overline{\text{B}}$) to assist in meeting the MIL-STD-1553B fail-safe timer requirements (see figure 5).

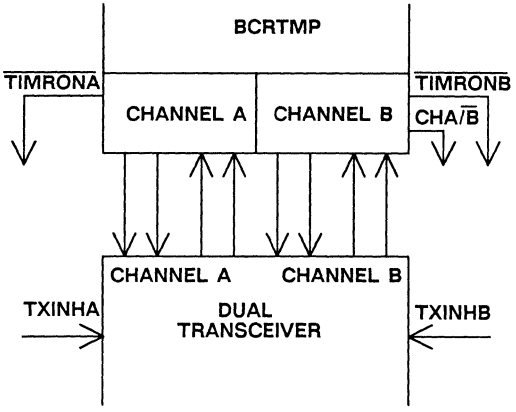


Figure 5. Dual-Channel Transceiver

6.0 Remote Terminal Architecture

The Remote Terminal architecture is a descriptor-based configuration of relevant parameters. It is composed of an RT Descriptor Space (see figure 6) and internal, host-programmable registers. The Descriptor Space contains only descriptors. Descriptors contain programmable subaddress parameters relating to handling message transfers. Each descriptor consists of four words: (1) a Control Word, (2) a Message Status List Pointer, (3) a Data List Pointer, and (4) an unused fourth word (see figure 7.) These words indicate how to perform the data transfers associated with the designated subaddress.

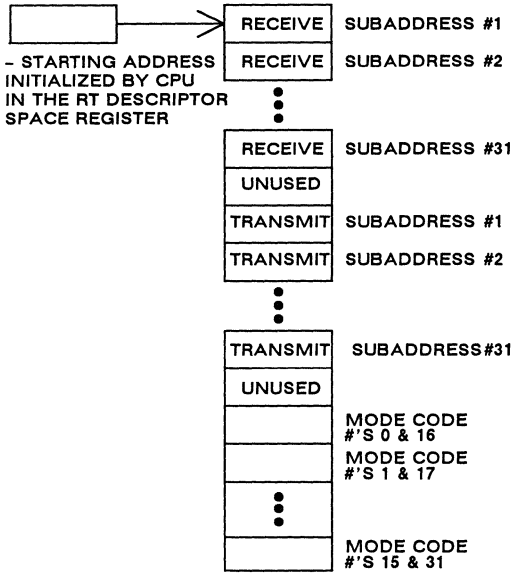


Figure 6. Descriptor Space

A receive descriptor and a transmit descriptor are associated with each subaddress. The descriptors reside in memory and are listed sequentially by subaddress. By using the index within the descriptor, the BCRTMP can buffer incoming and outgoing messages, which reduces host CPU overhead. This message buffering also reduces the risk of incoming messages being overwritten by subsequent incoming messages.

Each descriptor contains a programmable interrupt structure for subsystem notification of user-selected message transfers and indicates when the message buffers are full. Illegalizing subaddresses, in normal and broadcast modes, is accomplished by using programmable bits within the descriptor (see the RT Functional Operation section below).

Message Status information -- including word count, an internally generated time tag, and broadcast and message validity information -- is provided for each message. The Message Status Words are stored in a separate Message Status Word list according to subaddress. The list's starting locations are programmable within the descriptor.

Message data, received or transmitted, is also stored in lists. The message capacity of the lists and the lists' locations are user selectable within the descriptor.

6.1 RT Functional Operation

The RT off-loads the host computer of all routine data transfers involved with message transfers over the 1553 bus by providing a wide range of user-programmable functions. These functions make the BCRTMP's operation flexible for a variety of applications. The following paragraphs give each function's operational descriptions.

6.1.1 RT Subaddress Descriptor Definition

The host sets words within the descriptor. The BCRTMP then reads the descriptor words when servicing a command corresponding to the specified descriptor. All bit-selectable functions are active high and inhibited when low.

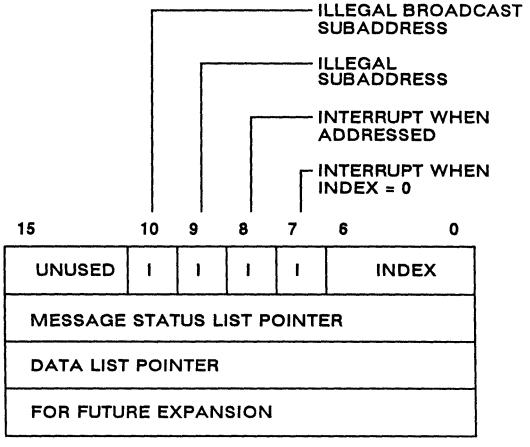


Figure 7. Remote Terminal Subaddress Descriptor

A. Control Word. The first word in the descriptor, the Control Word, selects or disables message transfers and selects an index.

Bit Number	Description
BITs 15-11	Reserved.
BIT 10	Illegal Broadcast Subaddress. Indicates to the BCRTMP not to access this subaddress using broadcast commands. The Message Error bit in the status word is set if the illegal broadcast subaddress is addressed. Since transmit commands do not apply to broadcast, this bit applies only to receive commands.
BIT 9	Illegal Subaddress. Set by the host CPU, it indicates to the BCRTMP that a command with this subaddress is illegal. If a command uses an illegal subaddress the Message Error bit in the 1553 status word is set. The Illegal Command Interrupt is also asserted if enabled.
BIT 8	Interrupt Upon Valid Command Received. Indicates that the BCRTMP is to assert an interrupt every time a command addresses this descriptor. The interrupt occurs just prior to post-command descriptor updating.
BIT 7	Interrupt When Index = 0. Indicates that the BCRTMP initiates an interrupt when the index is decremented to zero.
BITs 6-0	Index. These bits are for indexed message buffering. Indexing means transacting a pre-specified number of messages before notifying the host CPU. After each message transaction, the BCRTMP decrements the index by one until index = 0. Note that the index is decremented for messages that contain message errors.

B. Message Status List Pointer. The host sets the Message Status List Pointer, the second word within the descriptor, and the BCRTMP uses it as a starting address for the Message Status List. It is incremented by one with each Message Status Word write. If the Control Word Index is already equal to zero, the Message Status List Pointer is not incremented and the previous Message Status Word is overwritten.
Note: A Message Status Word is written and the pointer is incremented when the BCRTMP detects a message error.

C. Data List Pointer. The Data List Pointer is the third word within the descriptor. The BCRTMP stores data in RAM beginning at the address indicated by the Data List Pointer. The Data List Pointer is updated at the end of each successful message with the next message's starting address with the following exceptions:

- If the message is erroneous, the Data List Pointer is not updated. The next message overwrites any data corresponding to the erroneous message.
- Upon receiving a message, if the index is already equal to zero, the Data List Pointer is not incremented and data from the previous message is overwritten.

D. Reserved. The fourth descriptor word is reserved for future use.

6.1.2 Message Status Word

Each message the BCRTMP transacts has a corresponding Message Status Word, which is pointed to by the Message Status List Pointer of the Descriptor. This word allows the host CPU to evaluate the message's validity, determine the word count, and calculate the approximate time frame in which the message was transacted (figures 8 and 9).

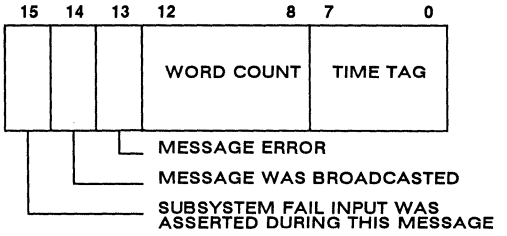


Figure 8. Message Status Word

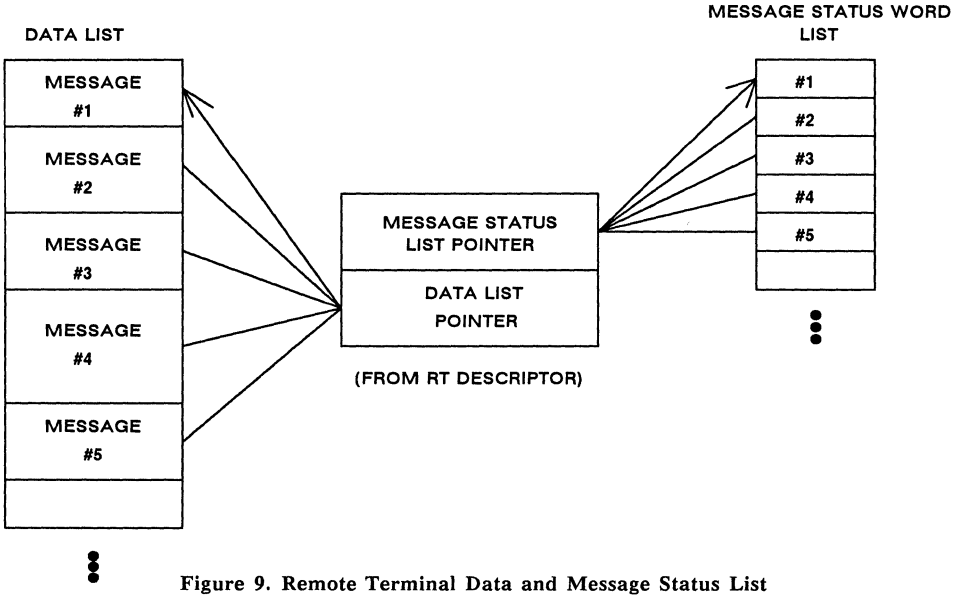


Figure 9. Remote Terminal Data and Message Status List

Message Status Word Definition

BIT 15 Subsystem Failed. Indicates SSYSF was asserted before the Message Status Word transfer to memory. This bit is also set when the user sets bit 13 of Register 10.

BIT 14 Broadcast Message. Indicates that the corresponding message was received in the broadcast mode.

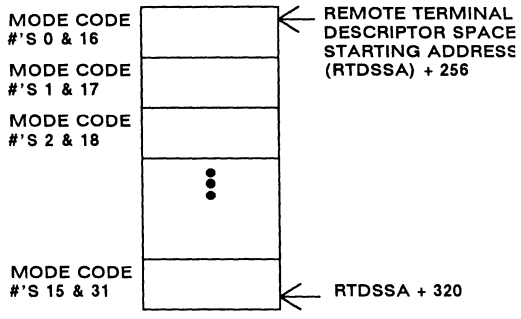
BIT 13 Message Error. Indicates a message is invalid due to improper synchronization, bit count, word count, or Manchester error.

BITs 12-8 Word Count. Indicates the number of words in the message and reflects the Word Count field in the command word. Should the message contain a different number of words than the Word Count field, the Message Error flag is triggered. If there are too many words, they are withheld from RAM. If the actual word count is less than it should be, the Message Error bit in the 1553 status word is set.

BITs 7-0 Time Tag. The BCRTMP writes the internally generated Time Tag to this location after message completion. The resolution is 64 microseconds. (See Register 13). If the timer reads 2, it indicates the message was completed 128 to 191 microseconds after the timer started.

6.1.3 Mode Code Descriptor Definition

Mode codes are handled similarly to subaddress transactions. Both use the four-word descriptors residing in the RT descriptor space to allow the host to program their operational mode. Corresponding to each mode code is a descriptor (see figure 10a). Of the 32 address combinations for mode codes in MIL-STD-1553, some are clearly defined functions while others are reserved for future use. Sixteen descriptors are used for mode code operations with each descriptor handling two mode codes: one mode code with an associated data word and one mode code without an associated data word. All mode codes can be handled in accordance with MIL-STD-1553B. The function of the first word of the Mode Code Descriptor is similar to that of the Subaddress Descriptor and is defined below. The remaining three words serve the same purpose as in the Subaddress Descriptor.



Note:
Mode code descriptor blocks are also provided for reserved mode codes but have no associated predefined BCRTMP operation.

Figure 10a. (RT) Mode Code Descriptor Space

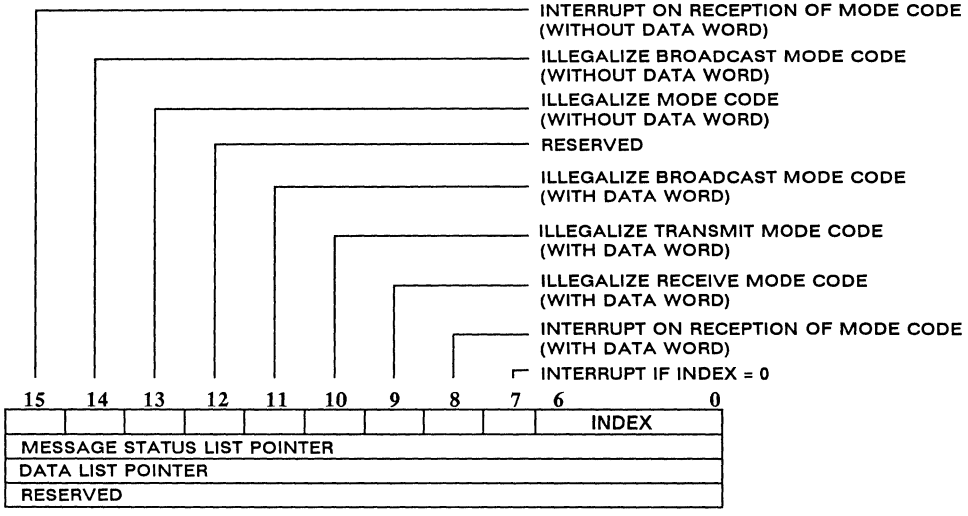


Figure 10b. (RT) Mode Code Descriptor

Control Word

BIT 15 Interrupt on Reception of Mode Code (without Data Word).

BIT 14 Illegalize Broadcast Mode Code (without Data Word).

BIT 13 Illegalize Mode Code (without Data Word).

BIT 12 Reserved.

BIT 11 Illegalize Broadcast Mode Code (with Data Word).

BIT 10 Illegalize Transmit Mode Code (with Data Word).

BIT 9 Illegalize Receive Mode Code (with Data Word).

BIT 8 Interrupt on Reception of Mode Code (with Data Word).

BIT 7 Interrupt if Index = 0.

BITs 6-0 Index. Functionally equivalent to the index described in the Subaddress Descriptor. It applies to mode codes with data words only.

The descriptors, numbered sequentially from 0 to 15, correspond to mode codes 0 to 15 without data words and mode codes 16 to 31 with data words. For example, mode codes 0 and 16 correspond to descriptor 0 and mode codes 1 and 17 correspond to descriptor 1. The Mode Code Descriptor Space is appended to the Subaddress Descriptor Space starting at 0100H (256D) of the 320-word RT Descriptor Space (see figure 6).

The BCRTMP can autonomously support all mode codes without data words by executing the specific function and transmitting the 1553 status word. The subsystem provides the data word for mode codes with data words (see the Data List Pointer section). For all mode codes, an interrupt can be asserted by setting the appropriate bit in the control word upon successful completion of the mode command (see figure 10b).

Dynamic Bus Control #00000
This mode code is accepted automatically if the Dynamic Bus Control Enable bit in the Remote Terminal Address Register is set. Setting the Dynamic Bus Control Acceptance bit in the 1553 status word and BCRTMP Status Register confirms the mode code acceptance. A High-Priority Interrupt is also asserted if enabled. If the Dynamic Bus Control Enable bit is not set, the BCRTMP does not accept Dynamic Bus Control.

Synchronize (Without Data Word) #00001
If enabled in the Mode Code #00001 Descriptor Control Word, the BCRTMP asserts an interrupt when this mode code is received.

Transmit Status Word #00010
The BCRTMP automatically transmits the 1553 status word corresponding to the last message transacted.

Initiate Self-Test #00011
The BCRTMP automatically starts its BIT routine. An interrupt, if enabled, is asserted when the test is completed. The BIT Word Register and external pin BCRTF are updated when the test is completed. A failure in BIT will also set the TF status word bit.

Transmitter Shutdown #00100
The BCRTMP disables the channel opposite the channel on which the command was received.

Override Transmitter Shutdown #00101
The BCRTMP enables the channel previously disabled.

Inhibit Terminal Flag Bit #00110
The BCRTMP inhibits the Terminal Flag from being set in the status word.

Override Inhibit Terminal Flag Bit #00111
The BCRTMP disables the Terminal Flag inhibit.

Reset Remote Terminal #01000
The BCRTMP automatically resets the encoder, decoders, and protocol logic.

Transmit Vector Word #10000
The BCRTMP transmits the vector word from the location addressed by the Data List Pointer in the Mode Code Descriptor Block.

Synchronize (with Data Word) #10001
On receiving this mode code, the BCRTMP simply stores the associated data word.

Transmit Last Command #10010
The BCRTMP transmits the last command executed and the corresponding 1553 status word.

Transmit BIT Word #10011
The BCRTMP transmits BIT information from the BIT Register.

Selected Transmitter Shutdown #10100
On receiving this mode code, the BCRTMP simply stores the associated data word.

Override Selected Transmitter Shutdown #10101
On receiving this mode code, the BCRTMP simply stores the associated data word.

Mode codes 9-15 and 22-31 are reserved for future expansion of MIL-STD-1553.

6.2 RT Error Detection

In accordance with MIL-STD-1553, the remote terminal handles superseding commands on the same or opposite bus. When receiving, the Remote Terminal performs a response time-out function of 56 microseconds for RT-RT transfers. If the response time-out condition occurs, a Message Error bit can be set in the 1553 status word and in the Message Status Word. Error checking occurs on both of the Manchester logic and the word formats. Detectable errors include word count errors, long words, short words, Manchester errors (including zero crossing deviation), parity errors, and data contiguity.

6.3 RT Operational Sequence

The following is a general description of the typical behavior of the BCRTMP as it processes a message in the RT mode. It is assumed that the user has already written a "1" to Register 0, bit 0, enabling RT operation.

Valid Command Received.

$\overline{\text{COMSTR}}$ goes active
Bus Legalization occurs (if selected)

- DMA Descriptor Read. (If Bus Legalization is used, the BCRTMP ignores the legalization information in the Control Word). After receiving a valid command, the BCRTMP initiates a burst DMA:

  DMA arbitration (BURST)
  Control Word read

Message Status List Pointer read
Data List Pointer read

Data Transmitted/Received.

- Data Word DMA.

  If the BCRTMP needs to transmit data from memory, it initiates a DMA cycle for each Data Word shortly before the Data Word is needed on the 1553B bus:

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

  If the BCRTMP receives data, it writes each Data Word to memory after the Data Word is received:

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for eachsuccessive word)

Status Word Transmission.

The BCRTMP automatically transmits the Status Word as described in section 8.2.8. For illegalized commands, the BCRTMP also sets the Message Error Bit in the 1553 Status Word.

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTMP is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
RT Descriptor Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

- Descriptor Write.

  After the BCRTMP processes the message, a final DMA burst occurs to update the descriptor block, if necessary:

  DMA arbitration (BURST)
  Message Status Word write
  Data List Pointer write (incremented by word count)
  Message Status List Pointer write (incremented by 1)
  Control Word write (index decremented)

Note the following exceptions:

Mode codes without data require no descriptor update.

Illegalized commands require no description updates (or data word accesses).

Predefined mode codes (18 and 19) which do not require access to memory for the data word, do not involve updating the Data List Pointer.

Messages with errors prevent updates to the Data List Pointer.

If the message index was zero, neither the Message Status List Pointer nor the Data List Pointer is updated.

7.0 Bus Controller Architecture

The BCRTMP's bus controller architecture is based on a Command Block structure and internal, host-programmable registers. Each message transacted over the MIL-STD-1553 bus has an associated Command Block, which the CPU sets up (see figures 11 and 12). The Command Block contains all the relevant message and RT status information as well as programmable function bits that allow the user to select functions and interrupts. This memory interface system is flexible due to a doubly-linked list data structure.

HEAD POINTER
CONTROL WORD
COMMAND WORD 1
COMMAND WORD 2 (RT-RT ONLY)
DATA LIST POINTER
STATUS WORD 1
STATUS WORD 2 (RT-RT ONLY)
TAIL POINTER

Figure 11. Command Block

In a doubly-linked Command Block structure, pointers delimit each Command Block to the previous and successive blocks (see figure 13). The linking feature eases multiple message processing tasks and supports message scheduling because of its ability to loop through a series of transfers at a predetermined cycle time. A data pointer in the command allows efficient space allocation because data blocks only have to be configured to the exact word count used in the message. Data pointers also provide flexibility in data-bank switching.

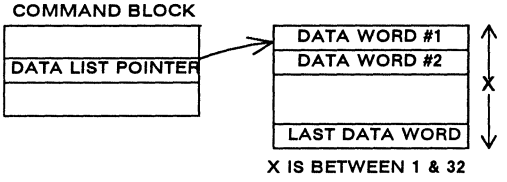


Figure 12. Data Placement

A control word with bit-programmable functions and a Message Error bit are in each Command Block. This allows selecting individual functions for each message and provides message validity information. The BCRTMP's register set provides additional global parameters and address pointers.

A programmable auto retry function is selectable from the control word and Control Register.

The auto retry can be activated when any of the following occurs:

- Busy bit set in the status word
- Message Error (indicated by the RT status response)
- Response Time-Out
- Message Error detected by the Bus Controller

One to four retries are programmable on the same or opposite bus.

The Bus Controller also has a programmable intermessage delay timer that facilitates message transfer scheduling (see figures 14 and 15). This timer, programmed in the control word, automatically delays between the start of two successive commands.

A polling function is also provided. The Bus Controller, when programmed, compares incoming status words to a host-specified status word and generates an interrupt if the comparison indicates any matching bits. An Interrupt and Continue function facilitates the host subsystem's synchronization by generating an interrupt when the specified Command Block's message is executed.

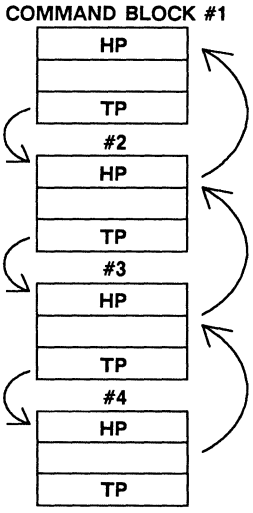


Figure 13. Command Block Chaining

7.1 BC Functional Operation

The Bus Controller off-loads the host computer of many functions needed to coordinate 1553 bus data transfers. Special architectural features provide message-by-message flexibility. In addition, a programmable interrupt scheme, programmable intermessage timing delays, and internal registers enhance the BCRTMP's operation.

The host determines the first Command Block by setting the initial starting address in the current Command Block Register. Once set, the BCRTMP updates the current Command Block register with the next Command Block Address. The BCRTMP then executes the sequential Command Blocks and counts out message delays (where programmed) until it encounters the last Command Block listed (indicated by the End of List bit in the control word). Interrupts are asserted when enabled events occur (see the Exception Handling and Interrupt Logging section, page 45).

The functions and their programming instructions are described below. The registers also contain many programmable functions and function parameters.

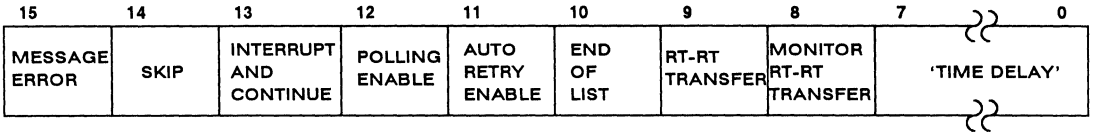


Figure 14. Command Word

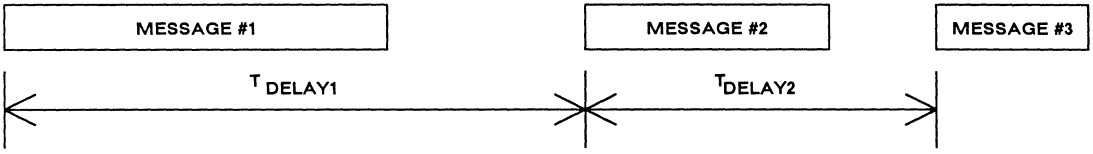


Figure 15. BC Timing Delays

BC Command Block Definition
Each Command Block contains (see figure 11):

A. Head Pointer. Host-written, this location can contain the address of the previous Command Block's Head Pointer. The BCRTMP does not access this location.

B. Control Word. Host-written, the Control Word contains bit-selectable options and a Message Error bit the BCRTMP provides (see figure 14). The bit definitions follow.

BIT 15 Message Error. The BCRTMP sets this bit when it detects an invalid RT response as defined in MIL-STD-1553B.

BIT 14 Skip. When set, this bit instructs the BCRTMP to skip this Command Block and execute the next.

BIT 13 Interrupt and Continue. If set, a Standard Interrupt is asserted when this block is addressed; operation, however, continues. Note that this interrupt must also be enabled by setting bit 0 of Register 9.

BIT 12 Polling Enable. Enables the BCRTMP's polling operation.

BIT 11 Auto Retry Enable. When set, the Auto Retry function, governed by the global parameters in the Control Register, is enabled for this message.

BIT 10 End of List. Set by the CPU, this bit indicates that the BCRTMP, upon completion of the current message, will halt (Register 1, bit 0 goes inactive) and assert a High-Priority Interrupt. The interrupt must also be enabled in the High-Priority Interrupt Enable Register.

BIT 9 RT-RT. Set by the CPU, this indicates that this Command Block transacts an RT-RT transfer.

BIT 8 Monitor RT-RT Transfer. Set by the CPU, this function indicates that the BCRTMP should receive and store the message beginning at the location indicated by the data pointer.

BITs 7-0 Time Delay. The CPU sets this field, which causes the BCRTMP to delay the specified time between sequential message starts (see figures 14 and 15). Regardless of the value in the Time Delay field (including zero), the BCRTMP will at least meet the minimum 4 μs intermessage gap time as specified in MIL-STD-1553B. The timer is enabled by having a non-zero value in this bit field. When using this function, please note:

- Timer resolution is 16 microseconds. As an example, if a given message requires 116 μs to complete (including the minimum 4 μs intermessage gap time) the value in the Time Delay field must be at least 00001000 (8 x 16 μs = 128 μs) to provide an intermessage gap greater than the 4 μs minimum requirement.
- If the timer is enabled and the Skip bit is set, the timer provides the programmed delay before proceeding.

- If the message duration exceeds the timer delay, the message is completed just as if the timer were not enabled.

C. **Command Word One.** Initialized by the CPU, this location contains the first command word corresponding to the Command Block's message transfer.

D. **Command Word Two.** Initialized by the CPU, this location is for the second (transmit) command word in RT-RT transfers. In messages involving only one RT, the location is unused.

E. **Data Pointer.** Initialized by the CPU, this location contains the starting location in RAM for the Command Block's message (see figure 16).

F. **Status Word One.** Stored by the BCRTMP, this location contains the entire Remote Terminal status response.

G. **Status Word Two.** Stored by the BCRTMP, this location contains the receiving Remote Terminal status word. For transfers involving one Remote Terminal, the location is unused.

H. **Tail Pointer.** Initialized by the host CPU, the Tail Pointer contains the next Command Block's starting address.

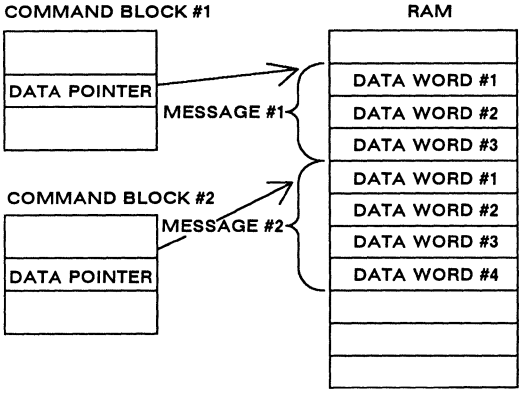


Figure 16. Contiguous Data Storage

7.2 Polling

During a typical polling scenario (see figure 17) the Bus Controller interrogates remote terminals by requesting them to transmit their status words. This feature can also alert the host if a bit is set in any RT status word response during normal message transactions. The BCRTMP enables the host to initialize a chain of Command Blocks with the command word's Polling Enable bit. A programmable Polling Compare Register (PCR) is provided. In the polling mode, the Remote Terminal response is compared to the Polling Compare Register contents. Program the PCR by setting the PCR bits corresponding to the RT's 1553 status word bits to be compared. If they match (i.e., two 1's in the same bit position) then, if enabled in both the BC Command Block Control Word and in the Standard Interrupt Enable Register (Register 9), a polling comparison interrupt is generated.

Example 1. No bit match is present

PCR	00000000001
RT's 1553 Status Word response	00000100010
Result	No Polling Comparison Interrupt

Example 2. Bit match is present

PCR	00100100000
RT's 1553 Status Word response	00000100000
Result	Polling Comparison Interrupt

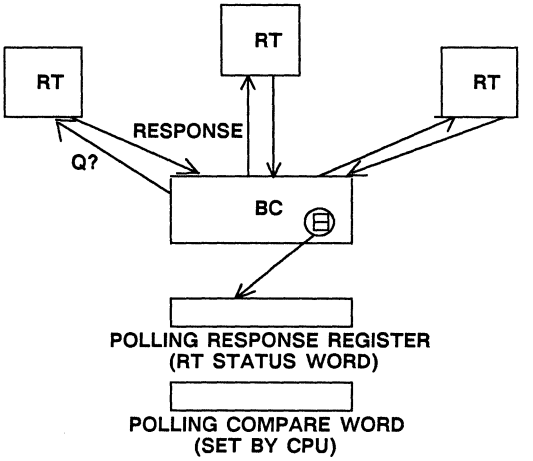


Figure 17. Polling Operation

7.3 BC Error Detection

The Bus Controller checks for errors (see the Exception Handling and Interrupt Logging and the RT Error Detection sections, pages 45 and 37) on each message transaction. In addition, the BC compares the RT command word addresses to the incoming status word addresses. The BC monitors for response time-out and checks data and control words for proper format according to MIL-STD-1553. Illogical commands include incorrectly formatted RT-RT Command Blocks.

7.4 Bus Controller Operational Sequence

The following is a general description of the typical behavior of the BCRTMP as it processes a message in the BC mode.

The user starts BC operation by writing a "1" to Register 0, Bit 0.

- Command Block DMA - the following occurs immediately after Bus Controller startup:

  DMA arbitration (BURST)
  Control Word read
  Command Word 1 read (from third location of Command Block)
  Data List Pointer read

A. For BC-to-RT Command Blocks:

The BCRTMP transmits the Command Word.

- Data Word DMA

  DMA arbitration
  Data Word read (starting at Data List Pointer address, incremented for each successive word)

The BCRTMP transmits the Data Word. Data Word DMAs and transmissions continue until all Data Words are transmitted.

- Status Word DMA

The BCRTMP receives the RT Status Word.

  DMA arbitration
  Status Word write (to sixth location of Command Block)

B. For RT-to-BC Command Blocks:

The BCRTMP transmits the Command Word.

- Status Word DMA

The BCRTMP receives the RT Status Word.

  DMA arbitration
  Status Word write (to sixth location of Command Block)

The BCRTMP receives the first Data Word.

- Data Word DMA

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

C. For RT(A)-to-RT(B) Command Blocks:

The BCRTMP transmits Command Word 1 to RT(B).

- Command Word 2 DMA

  DMA arbitration
  Command Word 2 read (from fourth location of Command Block)

The BCRTMP transmits Command Word 2 to RT(A).

The BCRTMP receives the RT Status Word from RT(A).

- Status Word DMA for RT(A) Status Word

  DMA arbitration
  Status Word write (to sixth location of Command Block)

The BCRTMP receives the first Data Word

- Data Word DMA (only if the BCRTMP is enabled to monitor the RT-to-RT message).

  DMA arbitration
  Data Word write (starting at Data List Pointer address, incremented for each successive word)

Data Word receptions and DMAs continue until all Data Words are received.

The BCRTMP receives the RT Status Word from RT(B).

- Status Word DMA for RT(B) Status Word

  DMA arbitration
  Status Word write (to seventh location of Command Block)

Exception Handling.

If an interrupting condition occurs during the message, the following occurs:

For High-Priority Interrupts:

$\overline{\text{HPINT}}$ is asserted (if enabled in Register 7). For message errors, the BCRTMP is put in a hold state until the interrupt is acknowledged (by writing a "1" to the appropriate bit in Register 8).

For Standard Interrupts:

DMA arbitration (BURST)
Interrupt Status Word write
Command Block Pointer write
Tail Pointer read (into Register 6)
$\overline{\text{STDINTP}}$ pulses low
$\overline{\text{STDINTL}}$ asserted (if enabled)
Processing continues

If Retries are enabled and a Retry condition occurs, the following DMA occurs:

DMA arbitration (BURST)
Control Word read
Command Word 1 read (from third location of Command Block)
Data List Pointer read

The BCRTMP proceeds from the current Command Block to the next successive Command Block.

- If no Message Error has occurred during the current Command Block, the following occurs:

  DMA arbitration (BURST)
  Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry).
  DMA hold cycle
  Control Word read (next Command Block)
  Command Word 1 read (next Command Block)
  Data List Pointer read

- If the BCRTMP detects a Message Error while processing the current Command Block, the following occurs:

  DMA arbitration (BURST)
  Control Word write
  Command Block Tail Pointer read (to determine location of next Command Block. Note that this occurs only if no Retry.)
  DMA hold cycle
  Control Word read (next Command Block)
  Command Word 1 read (next Command Block)
  Data List Pointer read

The BCRTMP proceeds again from point A, B, or C as shown above.

7.5 BC Operational Example (figure 19 on page 48)
The BCRTMP is programmed initially to accomplish the following:

The first Command Block is for a four-word RT-RT transfer with the BCRTMP monitoring the transfer and storing the data.

- Auto-retry is enabled on the opposite bus using only one retry attempt, if the incoming Status Word is received with the Message Error bit set.
- Wait for a time delay of 400 microseconds before proceeding to the next Command Block.
- The Data List Pointer contains the address 0400H.

The second Command Block is for a BC-RT transfer of two words.

- The End of List bit is set in its Control Word.
- The Data List Pointer contains the address 0404H.
- The Polling Enable bit is set and the Polling Compare Register contains 0004H (check for Subsystem Fail bit.

Then:

A. The CPU initializes all the appropriate registers and Command Blocks, and issues a Start Enable by writing a "1" to Register 0, bit 0.

B. The BCRTMP, through executing a DMA cycle, reads the Control Word, Command Words, and the Data List Pointer. The delay timer starts and message execution begins by transmitting the receive and transmit commands stored in the Command Blocks. The BCRTMP then waits to receive the Status Word back from the transmitting RT.

C. The BCRTMP receives the RT Status Word with all status bits low from the transmitting RT and stores the Status Word in Command Block 1. The incoming data words from the transmitting RT follow. The BCRTMP stores them in memory locations 0400H - 0403H.

   If the Status Word indicates that the message cannot be transmitted (Message Error), the response time-out clock counts to zero and the allotted message time runs out. An auto-retry can be initiated if programmed to do so. Nevertheless, the ME bit in the Control Word is set.

D. The BCRTMP receives the Status Word response from the receiving RT. The ME bit in the Status Word is set, indicating the message is invalid. The BCRTMP initiates the auto retry function, (as programmed) on the alternate bus, re-transmits the Command Words, receives the correct Status Word, and stores the data again in locations 0400H - 0403H. This time the Status Word response from the receiving RT indicates the message transfer is successful.

E. The timer delay between the two successive transactions counts down another 135 microseconds before proceeding. This is determined as follows:

   The message transaction time is approximately 130 microseconds (the only approximation is due to the range in status response and intermessage gap times specified by MIL-STD-1553B). Approximating that with the retry, the total duration for the two attempts is 265 microseconds.

F. The BCRTMP reads the Tail Pointer of Command Block 1 and places it in the Current Command Register. It also reads the Control Word, Command Word, and Data List Pointer, and the first data word in the second Command Block.

G. Since this is a BC-RT transfer, the BCRTMP transmits the receive command followed by two data words from locations 0404H - 0405H in memory. The BCRTMP reads the second data word from memory while transmitting the first.

H. The BCRTMP receives the status response from the RT. In this case, the Status Word indicates, by the ME bit being low, that the message is valid. The Status Word also has the Subsystem Fail bit set.

I. The Status Word is stored in the Command Block. The BCRTMP, having encountered the end of the list, halts message transactions and waits for another start signal.

J. The BCRTMP asserts a High-Priority Interrupt indicating the end of the command list. Due to the polling comparison failure, the BCRTMP also asserts a Standard Priority Interrupt and logs the event in the Interrupt Log List.

8.0 Multiple Protocol Options

The UT1553 BCRTMP was developed from the industry's first monolithic MIL-STD-1553B Bus Controller and Remote Terminal chip, the UT1553B BCRT. Many additional features were added to the BCRT to create the UT1553 BCRTMP, which conforms to the requirements of the many different "1553 standards" which developed between releases of MIL-STD-1553A and MIL-STD-1553B.

User-configurable Operational Mode selections allow the BCRTMP to interface to a wide variety of 1553 protocols. Protocols for which the user can configure the UT1553 BCRTMP include: MIL-STD-1553A, MIL-STD-1553B, McDonnell Douglas A3818, A5232, and A5690, and Grumman Aerospace SP-G-151A. The user need only to determine which Operational Mode settings are necessary to conform to the application's needs.

8.1 Operational Modes

The user can program the BCRTMP to conform to many of the currently used MIL-STD-1553 variations in protocol by simply selecting different operating modes. The BCRTMP provides seven Mode Select input pins and/or register bits to select the different operating modes. If all mode bits are high, the BCRTMP operates in accordance with MIL-STD-1553B.

8.1.1 MD0 (Mode 0)

Legalization Select (RT)

The MD0 input pin or bit 0 of Register 14 selects the method of command legalization the BCRTMP uses. Before issuing the appropriate RT response to a command, the BCRTMP must determine whether the command is legal. The BCRTMP accomplishes command legalization by one of two methods -- DMA, by fetching the appropriate Descriptor Block (MD0 = 1); or by using the Legalization bus (MD0 = 0). The Legalization bus is the faster of the two methods and must be selected in order to meet the RT Response Time requirements of MIL-STD-1553A. Since the BCRTMP cannot meet the "A" response time unless it uses the Legalization bus for command legalization, it forces Mode 0 low internally if the "A" response time is selected (MD2 = 0). See also section 5.5, Legalization bus.

8.1.2 MD1 (Mode 1)

Broadcast Option Select (BC, RT)

The MD1 input pin or bit 1 of Register 14 selects the Broadcast option the BCRTMP uses. The use of Broadcast varies with differences in the 1553 protocols. For protocols that support the Broadcast option (MD1 = 1), the RT address 11111 is reserved to indicate a Broadcast command. When the Bus Controller transmits a Broadcast command, all RTs must receive the message, but no RT is to respond with a status word. For protocols that do not support the Broadcast option (MD1 = 0), RT address 11111 is treated as a normal RT address.

8.1.3 MD2 (Mode 2)

RT Response Time Select (RT)

The MD2 input pin or bit 2 of Register 14 selects the RT Response Time the BCRTMP uses in the RT mode to respond to 1553 commands. Before an RT can respond to a command, it must determine whether that command is legal. As stated is section 8.1.1 above, the BCRTMP accomplishes Command Legalization by using either DMA Descriptor Block fetching or by using the Legalization bus.

The RT Response Time differs among the 1553 protocols. The RT Response Time is measured from the zero crossing of the parity bit of the receive command's last data word (or the zero crossing of the parity bit of the transmit command word) to the status word sync's zero crossing. The maximum response time allowed for an RT is either 7.0 μs ("A" response time, MD2 = 0) or 12.0 μs ("B" response time, MD2 = 1), depending on the specification.

8.1.4 MD3 (Mode 3)

Mode Code Option Select (BC,RT)

The MD3 input pin or bit 3 of Register 14 selects the mode code option the BCRTMP uses. Differences in mode code definitions among the 1553 protocols concern the number of defined mode codes and whether mode codes with data are defined. MIL-STD-1553B's definition is formal, but the other specifications define the possible mode codes to varying degrees, and may not use mode codes with data.

The BCRTMP uses this selection to determine which bit patterns in the subaddress field of the command word indicate that the word count field contains a mode code. When MD3 is high, either 00000 or 11111 in the subaddress field indicates a mode code. When MD3 is low, only 00000 indicates a mode code. The BCRTMP provides additional control over mode code definition with the MD6 selection (see section 8.1.7). Also, the user can program bit 13 of Register 14 to provide additional mode code control.

8.1.5 MD4 (Mode 4)

Status Word Option Select (RT)

The MD4 input pin or bit 4 of Register 14 selects the method the BCRTMP uses to generate the RT status word. Most, if not all, 1553 protocols define the Terminal Address, Message Error (ME), and Terminal Flag (TF) status word bits in the same manner. The remaining bits are defined in a variety of ways, not only dependent on the 1553 protocol, but also on the individual procurement specification. MIL-STD-1553B is quite formal in defining the status word bits, while the other specifications either define or leave undefined the other bits to varying degrees for procurement-specific options. When MD4 is high, the BCRTMP generates the status word in accordance with MIL-STD-1553B, using the contents of Register 10 for many of the status bits. When MD4 is

low, the BCRTMP generates the status word using the Programmable status register (Register 15). See section 8.2.8 for more information regarding status word generation.

8.1.6 MD5 (Mode 5)
Message Error Technique Select (RT)
The MD5 input pin or bit 5 of Register 14 selects the method the BCRTMP uses for handling message errors. Some 1553 protocols (e. g., MIL-STD-1553B) consider any message error reason to discard the entire message and suppress status word transmission, while others (e. g., McDonnell Douglas A3818) define the required activity according to message error severity.

When MD5 is high, message error handling is as described in MIL-STD-1553B. The MIL-STD-1553B definition states that on the occurrence of any Message Error condition, the RT sets the message error bit in the status word and suppresses status word transmission. Message error conditions are defined as any of the following: parity errors, word count errors, or Manchester errors.

When MD5 is low, message error handling is as described in McDonnell Douglas A3818. In this method, a less severe error (either a Manchester error or a parity error in a data word, for example) requires special attention. The RT must mark the individual defective data word and respond with the message error bit set in the status word. When the BCRTMP detects this type of Message Error, the BCRTMP asserts the $\overline{\text{ERR}}$ output and places the word count for the defective data word on the least significant five bits of the Legalization bus. Due to the BCRTMP's internal detection circuitry, errors in the first two data bits will force the BCRTMP to ignore the word and cause a word count error. Word count errors cause the RT to suppress the status word and set the Message Error bit.

8.1.7 MD6 (Mode 6)
Mode Code with Data Select (BC,RT)
The MD6 input pin or bit 6 of Register 14 selects whether mode codes with data are allowed. When MD6 is high, the mode codes defined in MIL-STD-1553B as mode codes with data have an associated data word. When MD6 is low, the BCRTMP treats all mode codes as mode codes without data.

8.1.8 MD7 (Mode 7)
Remote Terminal Time Out Option Select (BC,RT)
The MD7 input pin or bit 12 of Register 0 selects the Remote Terminal Time-Out option. When MD7 is high, the Remote Terminal Time-Out (RTO) is nominally 16 μs. When MD7 is low, the Remote Terminal Time-Out (RTO) is nominally 32 μs.

8.2 Additional UT1553 BCRTMP Features
8.2.1 DOMC Do Mode Code Control Signal (RT)
The BCRTMP provides additional mode code flexibility through use of the DOMC input. This input (internally pulled high) can be pulled low when the BCRTMP receives a mode code to prevent the BCRTMP from automatically executing the mode code. This input can be used to disable automatic execution of mode codes at any time; however, the individual selection of mode code execution applies only when using the Legalization bus for command legalization (i.e., MD0 is low), since the timing for mode code execution decision-making corresponds with mode code legalization using the Legalization bus method only. If the user desires automatic execution of the mode code as defined in MIL-STD-1553B, then the user asserts the DOMC signal high after the BCRTMP receives the mode code. If the user desires to suppress automatic execution of the Mode Code, then the user asserts the DOMC signal low after the BCRTMP receives the mode code. The timing for the DOMC input follows, identically, the timing for the LGLCMD of the Legalization bus. See Table 2 for the actions the BCRTMP takes when receiving specific mode codes.

8.2.2 Continuous Wrap-Around Circuitry (BC,RT)
The Continuous Wrap-Around Test feature is available for both Bus Controller and Remote Terminal operation. This feature permits continuous monitoring of the correct operation of the BCRTMP.

The user either asserts the $\overline{\text{WRAPEN}}$ input low or writes a "one" to bit 7 of Register 14 to enable the Continuous Wrap-Around feature. This feature permits the BCRTMP to compare everything it transmits with a "reflected-back" version of the transmitted data. The data is reflected back by the 1553 transceiver and serially received into the BCRTMP's decoder circuitry. If a mismatch is found between the transmitted data and the reflected data, then the BCRTMP asserts the WRAPF output.

Asserting the $\overline{\text{WRAPEN}}$ and the $\overline{\text{ALTWRAP}}$ inputs places the BCRTMP in a special off-line system diagnostics mode to allow the system to test both 1553 buses and the associated transceivers, transformers, connectors, etc.

Typical use of this feature would involve connecting a bus stub between the Channel A and B connectors. The user could then place the BCRTMP in a Bus Controller mode of operation and execute a list of commands. With the $\overline{\text{ALTWRAP}}$ and $\overline{\text{WRAPEN}}$ signals asserted, each transmission on the selected bus would be received through the wrap-around circuitry on the opposite bus. Any assertion of the WRAPF output would indicate that either the BCRTMP or some part of the bus or interface network has failed. Note that if no RT is present in the system, then the BCRTMP will naturally detect a no-response error. This can be avoided by using Broadcast commands, in which case no RT is expected to respond on the bus.

8.2.3 Stop Enable (BC,RT)

The user implements this feature by setting bit 12 of Register 14 high. In the Bus Controller mode, when this bit is high, the occurrence of any enabled interrupt (either Standard or High-Priority) causes the BCRTMP to automatically halt Bus Controller message processing. The BCRTMP resumes message processing when the user clears the interrupt by writing a "one" to the appropriate bit in Register 8.

In the Remote Terminal mode, when this bit is high, the occurrence of any enabled interrupt (either Standard or High-Priority) causes the BCRTMP to automatically enter the Forced Busy mode of operation (see section 8.2.4). The BCRTMP exits the Forced Busy mode when the user clears the interrupt.

8.2.4 Forced Busy (RT)

The user places the BCRTMP into the Forced Busy mode (RT only) by either pulling the $\overline{\text{FBUSY}}$ input low or by writing a "one" to bit 11 of Register 15 or bit 9 of Register 10. As discussed in Section 8.2.3, the BCRTMP can also automatically enter the Forced Busy mode with the occurrence of enabled interrupts. While in the Forced Busy mode, all interrupts are disabled, the Busy bit is set in the status word response, and no DMA transactions will occur. The $\overline{\text{BUSYACK}}$ output acknowledges that the BCRTMP is in the Forced Busy mode.

8.2.5 ACTIVE Signal (RT)

The ACTIVE output provides a means for the user to place the BCRTMP on the 1553 bus, enabled as an RT, and determines if it should assume bus mastership. The BCRTMP asserts the ACTIVE signal when it detects a valid command on the bus to any RT address. The host determines which bus is active by examining bits 10 and 11 of Register 14. To disable bus activity detection, the host writes a "one" to bit 10 of Register 14 to disable Channel A (or bit 11 of Register 14 for Channel B). The ACTIVE output remains deasserted until one or both of the channels is enabled. The user writes a "zero" to the appropriate bit location(s) to enable the desired channel(s). Performing a programmed or hardware reset also enables both activity monitors.

8.2.6 Transmitter Inhibit Signals (BC,RT)

The UT1553 BCRTMP contains two transmitter inhibit signals (one for Channel A and one for Channel B) that provide fail-safe timing for the 1553 buses. The signals are active ($\overline{\text{TIMRONA}}$ for Channel A or $\overline{\text{TIMRONB}}$ for Channel B) when the BCRTMP begins transmitting and time out, or go inactive, 660 μs later, if the BCRTMP has not completed its transmission.

8.2.7 Immediate Clear Mode

The user sets bit 15 of Register 15 to enter the Immediate Clear Mode. When set, this bit will cause the BCRTMP to automatically clear all programmable status bits after the BCRTMP transmits the RT status word. When this bit is set, the first status word sent out contains the programmable status bits as programmed by either the Programmable Status Register ("A" protocol, MD4 = 0) or the RT Address Register ("B" protocol, MD4 = 1). After status word transmission, all programmable status bits are cleared automatically. The exception to this occurs when the next command received is the Transmit Status Word or Transmit Last Command mode code. When either of these mode codes is received, the BCRTMP will respond with the appropriate status word from the previous valid command. This feature applies to all operational modes.

8.2.8 Status Word Generation

As a result of the differing requirements for status words in the various 1553 protocols, the BCRTMP must be capable of generating the RT status word in a variety of ways. It is appropriate to discuss the separate status word bits individually in order to understand how the BCRTMP generates these bits. The three status word bits defined as "reserved" in MIL-STD-1553B are handled identically by the BCRTMP, as shown below. The action taken to generate all other status word bits varies, depending on the mode in which the BCRTMP is operating. In most cases, the BCRTMP generates the status word bits in different ways depending on the internal state of Operational Mode 4.

8.2.8.1 The Terminal Address Field

The Terminal Address field in the status word is always provided in the same manner. The BCRTMP uses pins RTA4 to RTA0 (or bits 4-0 of the Remote Terminal Address Register) to generate the Remote Terminal Address bits of the status word.

8.2.8.2 The Message Error Bit

If MD4 = 1, then the Message Error bit in the status word is set if any 1553 Message Error condition (or Illegal Command) occurs.

If MD4 = 0, then the Message Error bit in the status word is set when any 1553 Message Error condition (or Illegal Command) occurs or if bit 10 of Register 15 is set.

8.2.8.3 The Instrumentation Bit

If MD4 = 1, then the BCRTMP uses bit 15 of Register 10 to set the Instrumentation bit in the status word.

If MD4 = 0, then the BCRTMP uses bit 9 of Register 15 (the Programmable Status Register) to set the Instrumentation bit in the status word.

8.2.8.4 The Service Request Bit

If MD4 = 1, then the BCRTMP uses bit 10 of Register 10 to set the Service Request bit in the status word.

If MD4 = 0, then the BCRTMP uses bit 8 of Register 15 (the Programmable Status Register) to set the Service Request bit in the status word.

Also, the Service Request bit can be forced to reflect the complement of the status word Busy bit (independent of the internal state of MD4) if the user sets bit 12 of Register 15 high.

8.2.8.5 The MIL-STD-1553B "Reserved" Status Word Bits

The BCRTMP always provides the MIL-STD-1553B "Reserved" status word bit field (bit Times 12-14) in the status word in the same manner. The BCRTMP uses bits 5-7 of the Register 15 to generate these bits (independent of the internal state of MD4).

8.2.8.6 The Broadcast Command Received Bit

If MD4 = 1, then the Broadcast Command Received bit in the status word is set when a Broadcast command is received, if Broadcast is enabled.

If MD4 = 0, then the Broadcast Command Received bit in the status word is set if bit 4 of the Programmable Status Register is set high.

8.2.8.7 The Busy Bit

If MD4 = 1, then the Busy bit in the status word is set if either bit 14 of Register 10 is set high or if the BCRTMP is in the Forced Busy mode (see section 8.2.4 for a discussion on entry to the Forced Busy mode). The assertion of the Busy bit while in the Forced Busy mode can be disabled if both bits 13 and 14 of Register 15 are set high. Note that the Forced Busy mode is independent of the internal state of MD4.

If MD4 = 0, then the Busy bit in the Status Word is set if either bit 14 of Register 10 or bit 3 of the Programmable Status Register is set high, or if the BCRTMP is in the Forced Busy mode.

8.2.8.8 The Subsystem Flag Bit

If MD4 = 1, then the Subsystem Flag bit in the status word is set either if the user sets bit 13 of Register 10 or asserts the SSYSF input of the BCRTMP, or if a BIT failure has occurred.

If MD4 = 0, then the Subsystem Flag bit in the status word is set if the user sets bit 2 of the Programmable Status Register.

8.2.8.9 The Dynamic Bus Control Acceptance Bit

If MD4 = 1, the Dynamic Bus Control Acceptance bit in the status word will be set when the BCRTMP receives a Dynamic Bus Control Mode Code that is not a Broadcast command, if the user has not illegalized that command and has set bit 12 of Register 10 high.

8.2.8.10 The Terminal Flag Bit

If MD4 = 1, setting bit 11 of Register 10 or the occurrence of a BIT failure will always set the Terminal Flag bit in the status word.

If MD4 = 0, setting bit 0 of the Programmable Status Register will always set the Terminal Flag bit in the status word.

Independent of the internal state of MD4, the following conditions will also set the Terminal Flag bit in the status word.

1) If bit 13 of Register 15 is "1", and bit 14 of Register 15 is "0", then the Terminal Flag bit in the status word is also set if the Busy bit or the Subsystem Flag bit is set in the status word.

2) If bit 13 of Register 15 is "0" and bit 14 of Register 15 is "1", then the Terminal Flag bit in the status word is also set if any of the status word bits are set.

Note that if the Terminal Flag bit has been inhibited by Mode Code 6, this bit will not be set by any of the above methods.

9.0 Exception Handling and Interrupt Logging

The exception handling scheme the BCRTMP uses is based on an interrupt structure and provides a high degree of flexibility in:

- defining the events that cause an interrupt,
- selecting between High-Priority and Standard interrupts, and
- selecting the amount of interrupt history retained.

The interrupt structure consists of internal registers that enable interrupt generation, control bits in the RT and BC data structures (see the Remote Terminal Descriptor Definition section, page 30, and the Bus Controller Command Block definition, page 35), and an Interrupt Log List that sequentially stores an interrupt events record in system memory.

The BCRTMP generates the Interrupt Log List (see figure 18) to allow the host CPU to view the Standard Interrupt occurrences in chronological order. Each Interrupt Log List entry contains three words. The first, the Interrupt Status Word, indicates the type of interrupt (entries are only for interrupts enabled). In the BC mode, the second word is a Command Block Pointer that refers to the corresponding Command Block. In the RT mode, the second word is a Descriptor Pointer that refers to the corresponding subaddress descriptor. The CPU-initialized third word, a Tail Pointer, is read by the BCRTMP to determine the next Interrupt Log List address. The list length can be as long or as short as required. The configuration of the Tail Pointers determines the list length.

The host CPU initializes the list by setting the tail pointers. This gives flexibility in the list capacity and the ability to link the list around noncontiguous blocks of memory. The host CPU sets the list's starting address using the Interrupt Log List Register. The BCRTMP then updates this register with the address of the next list entry.

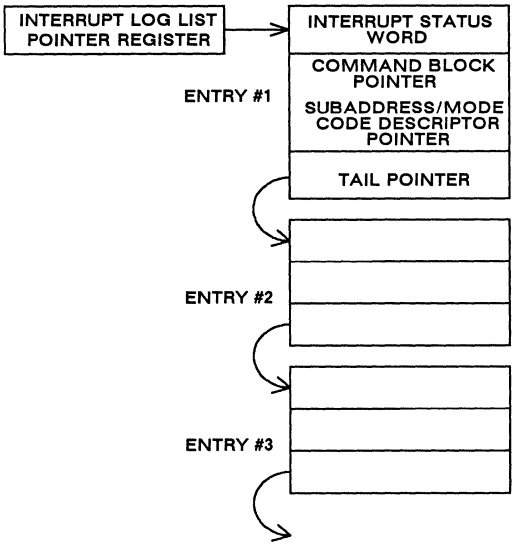


Figure 18. Interrupt Log List

The internal High-Priority Interrupt Status/Reset Register indicates the cause of a High-Priority Interrupt. The High-Priority Interrupt signal is reset by writing a "1" to the set bits in this register.

The interrupt structure also uses three BCRTMP-driven output signals to indicate when an interrupt event occurs:

$\overline{\text{STDINTL}}$ Standard Interrupt Level. This signal is asserted when one or more of the events enabled in the Standard Interrupt Enable Register occurs. Clear the signal by resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register.

$\overline{\text{STDINTP}}$ Standard Interrupt Pulse. This signal is pulsed for each occurrence of an event enabled in the Standard Interrupt Enable Register.

$\overline{\text{HPINT}}$ High-Priority Interrupt. This signal is asserted for each occurrence of an event enabled in the High-Priority Interrupt/Enable Register. Writing to the corresponding bit in the High-Priority Status/Reset Register resets it.

Interrupt Status Word Definition

All bits in the Interrupt Status Word are active high and have the following functions:

BIT 15 Interrupt Status Word Accessed. The BCRTMP always sets this bit during the DMA Write of the Interrupt Status Word. If the CPU resets this bit after reading the Interrupt Status Word, the bit can help the CPU determine which entries have been acknowledged.

BIT 14 No Response Time-Out (Message Error condition). Further defines the Message Error condition to indicate that a Response Time-Out condition has occurred.

BIT 13 (RT) Message Error (ME). Indicates the ME bit was set in the 1553 status word response.

BITs 12-8 Reserved.

BIT 7 (RT) Subaddress Event or Mode Code with Data Word Interrupt. Indicates a descriptor control word has been accessed with either an Interrupt Upon Valid Command Received bit set or an Interrupt when Index=0 bit set (and the Index is decremented to 0).

BIT 6 (RT) Mode Code Interrupt. Indicates a mode code has occurred with an Interrupt When Addressed interrupt enabled.

BIT 5 (RT) Illegal Broadcast Command. Applies to receive commands only. This bit indicates that a received command, due to an illegal mode code or subaddress field, has been received in the broadcast mode. This does not include invalid commands.

BIT 4 (RT) Illegal Command. This indicates that an illegal command has occurred due to an illegal mode code or subaddress and T/R field. This does not include invalid commands.

BIT 3 (BC) Polling Comparison Match. Indicates a polling comparison interrupt.

BIT 2 (BC) Retry Fail. Indicates all the programmed retries have failed.

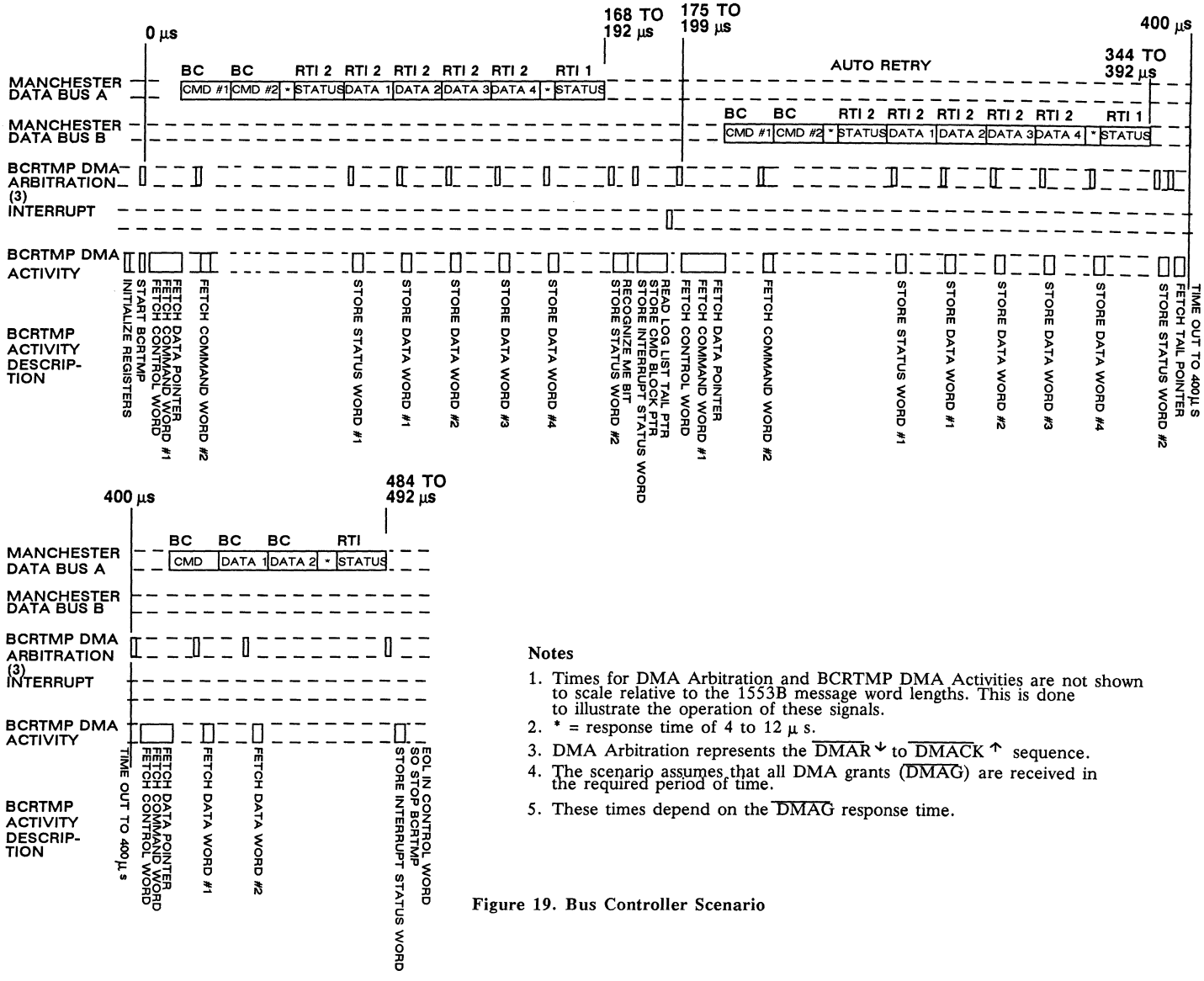
BIT 1 (BC,RT) Message Error. Indicates a Message Error has occurred.

BIT 0 (BC) Interrupt and Continue. This corresponds to the interrupt and continue function described in the Command Block.

Table 2. BCRTMP Automatic Mode Code Execution

T/R Bit	Mode Code	Function	Automatic Execution
1	00000	Dynamic Bus Control	No, Note 1
1	00001	Synchronize (without Data Word)	No, Note 2
1	00010	Transmit Status Word	Yes
1	00011	Initiate Self-Test	Yes
1	00100	Transmitter Shutdown	Yes
1	00101	Override Transmitter Shutdown	Yes
1	00110	Inhibit Terminal Flag Bit	Yes
1	00111	Override Inhibit Terminal Flag Bit	Yes
1	01000	Reset Remote Terminal	Yes
1	01001	Reserved	Note 3
1	01010	Reserved	Note 3
1	01011	Reserved	Note 3
1	01100	Reserved	Note 3
1	01101	Reserved	Note 3
1	01110	Reserved	Note 3
1	01111	Reserved	Note 3
1	10000	Transmit Vector Word	Yes, Note 5
0	10001	Synchronize (with Data Word)	No, Note 2
1	10010	Transmit Last Command	Yes
1	10011	Transmit BIT Word	Yes
0	10100	Selected Transmitter Shutdown	No, Note 4
0	10101	Override Selected Transmitter Shutdown	No, Note 4
0 or 1	10110	Reserved	Note 3
0 or 1	10111	Reserved	Note 3
0 or 1	11000	Reserved	Note 3
0 or 1	11001	Reserved	Note 3
0 or 1	11010	Reserved	Note 3
0 or 1	11011	Reserved	Note 3
0 or 1	11100	Reserved	Note 3
0 or 1	11101	Reserved	Note 3
0 or 1	11110	Reserved	Note 3
0 or 1	11111	Reserved	Note 3

Notes:
1. If the Dynamic Bus Control Enable bit in the RT Address Register (bit 12 of Register 10) is set, then a high priority interrupt can occur (if enabled in Register 7) and the Dynamic Bus Control Acceptance bit is set in the status word.
2. As with any subaddress or mode code, an interrupt can be caused and used for synchronization purposes.
3. These mode codes can be used, but the BCRTMP will not automatically execute them. The designer can enable an interrupt to occur on the reception of the mode code.
4. The host CPU is responsible for shutting down a bus in a more than dual-redundant system.
5. For the Transmit Vector Word Mode Code, the BCRTMP must access memory for the Vector Word, as with other mode codes with data (except mode codes 18 and 19).



Notes

1. Times for DMA Arbitration and BCRTMP DMA Activities are not shown to scale relative to the 1553B message word lengths. This is done to illustrate the operation of these signals.
2. * = response time of 4 to 12 µ s.
3. DMA Arbitration represents the $\overline{\text{DMAR}}\downarrow$ to $\overline{\text{DMACK}}\uparrow$ sequence.
4. The scenario assumes that all DMA grants ($\overline{\text{DMAG}}$) are received in the required period of time.
5. These times depend on the $\overline{\text{DMAG}}$ response time.

Figure 19. Bus Controller Scenario

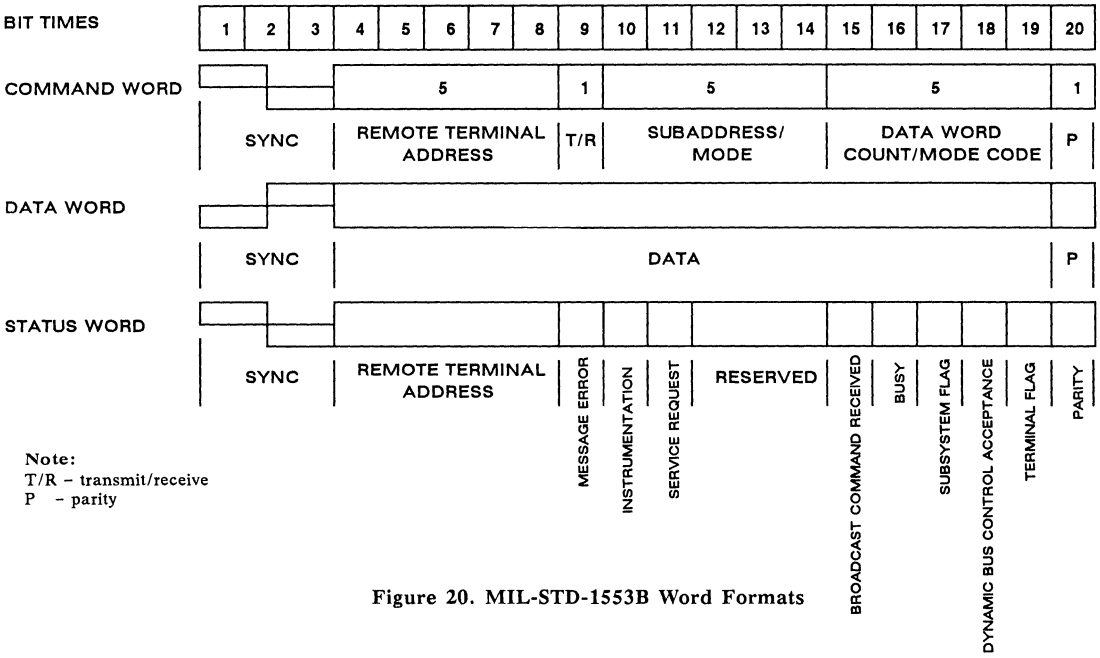


Figure 20. MIL-STD-1553B Word Formats

10.0 Operating Conditions*

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
T_{JMAX}	Maximum junction temperature	+175	°C
P_D	Average power dissipation (1)	300	mW
Θ_{JC}	Thermal resistance, junction-to-case	12	°C/Watt

Notes:
1. Does not reflect the added PD due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ±.01%	MHz

11.0 DC ELECTRICAL CHARACTERISTICS

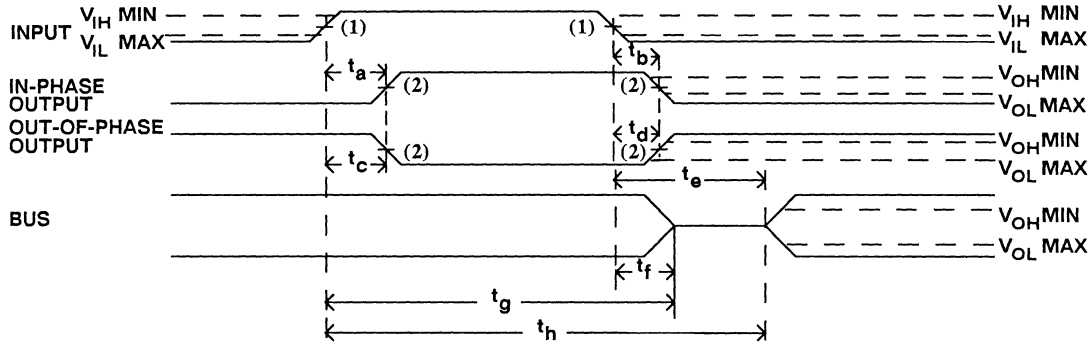
(V_{DD} - 5.0 V +/-10%; -55°C < T_C < + 125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH}	High-level input voltage TTL inputs		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-up resistors Inputs with pull-up resistors	 V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	 -1 -1 -550	 1 1 -80	 µA µA µA
V_{OL}	Low-level output voltage TTL outputs CMOS outputs	 I_{OL} = 3.2 mA I_{OL} = 50 µA		 0.4 V SS +.1	 V V
V_{OH}	High-level output voltage TTL outputs CMOS outputs	 I_{OH} = -400 µA I_{OH} = 50 µA	 2.4 VDD -.1		 V V
I_{OZ}	Three-state output leakage current TTL outputs	 V_O = V_{DD} or V_{SS}	 -10	 10	 µA
I_{OS}	Short-circuit output current (1,2)	V_{DD} = 5.5 V, V_O = V_{DD} V_{DD} = 5.5 V, V_O = 0 V	 -100	100	mA mA
C_{IN}	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		20	pF
I_{DD}	Average operating current (1,4)	F = 12 MHz, C_L = 50 pF		50	mA
QI_{DD}	Quiescent current	See Note 5		3	mA

Notes:
1. Supplied as a design limit, but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes which may affect input/output capacitance.
4. Includes current through input pull-up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
5. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

12.0 AC Electrical Characteristics

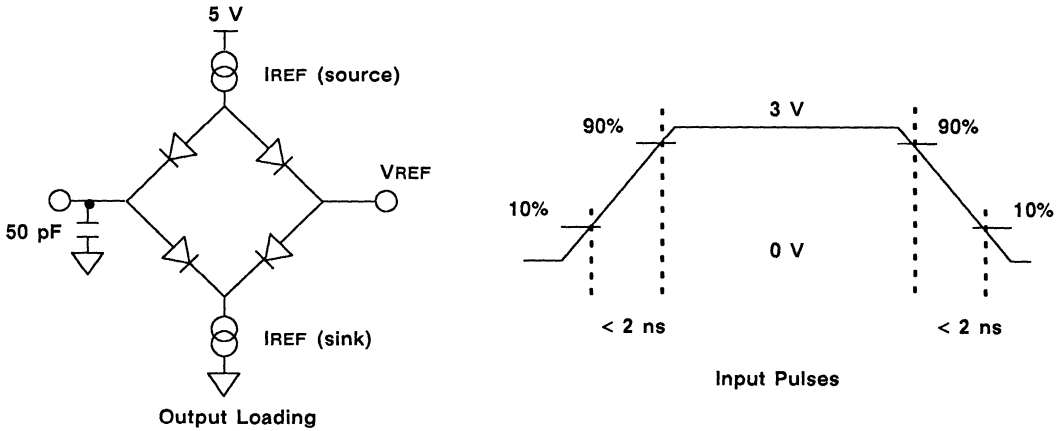
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

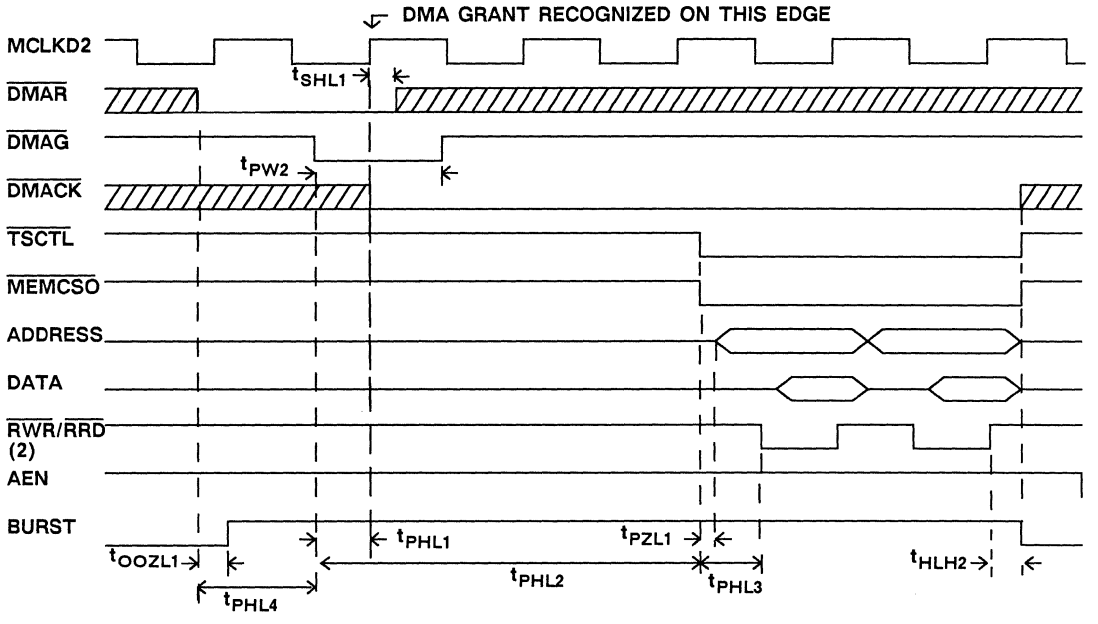
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 21. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

Figure 22. AC Test Loads and Input Waveforms

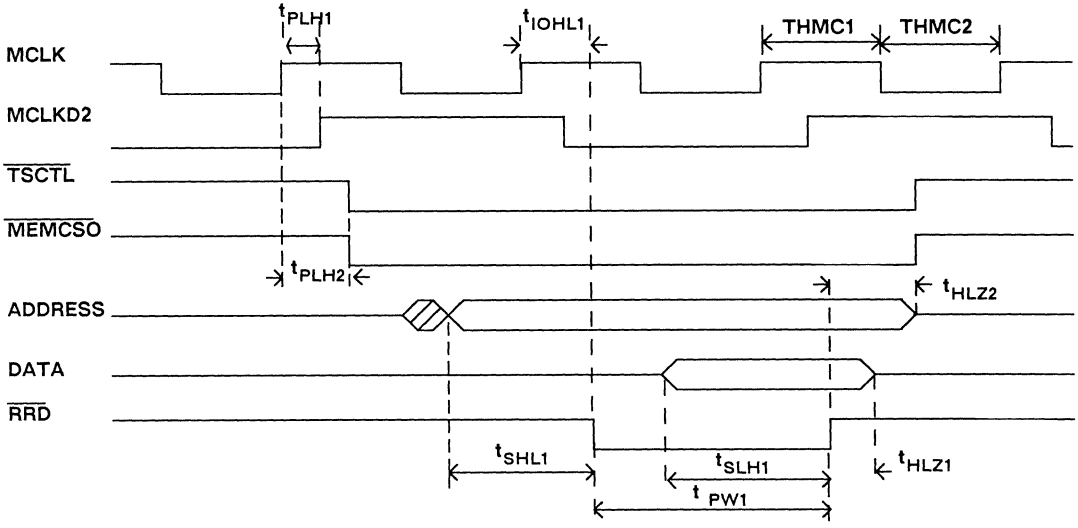


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	$\overline{DMACK}\downarrow$ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PHL1} (1)	$\overline{DMAG}\downarrow$ to $\overline{DMACK}\downarrow$ See note 3	0	45	ns
t_{PHL2}	$\overline{DMAG}\downarrow$ to $\overline{TSCTL}\downarrow$	2xMCLK	4xMCLK	ns
t_{PZL1}	$\overline{TSCTL}\downarrow$ to ADDRESS valid	0	40	ns
t_{HLH2}	$\overline{RWR/RRD}\uparrow$ to $\overline{DMACK}$ High Impedance	THMC1-10	THMC1+10	ns
t_{PHL3}	$\overline{TSCTL}\downarrow$ to $\overline{RWR/RRD}\downarrow$	MCLK-20	MCLK+20	ns
t_{PW2}	$\overline{DMAG}\downarrow$ to $\overline{DMAG}\uparrow$	MCLK	6xMCLK	ns
t_{OOZL1}	$\overline{DMAR}\downarrow$ to BURST $\uparrow$	0	10	ns
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See notes 4, 6	0	3.5 (1.9)	µs
t_{PHL4}	$\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ See notes 5, 6	0	1.9 (0.8)	µs

Notes:
1. Guaranteed by test.
2. See figures 24 and 25 for detailed DMA read and write timing.
3. $\overline{DMAG}$ must be asserted at least 45 ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If $\overline{DMAG}$ is not asserted at least 45 ns prior to the rising edge of MCLKD2, $\overline{DMAG}$ is not recognized until the following MCLKD2 cycle.
4. Provided MCLK = 12 MHz. Number in parentheses indicates the longes $\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.
5. Provided MCLK = 6 MHz. Number in parentheses indicates the longest $\overline{DMAR}\downarrow$ to $\overline{DMAG}\downarrow$ allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT Response Time. The number not in parentheses applies to all other circumstances.
6. The maximum limit for this specification applies only when using DMA Legalization (MD0=1).

MCLK = period of the memory clock cycle.
BURST signal is for multiple-word DMA accesses.
THMC1 is equivalent to the positive phase of MCLK (see figure 24).

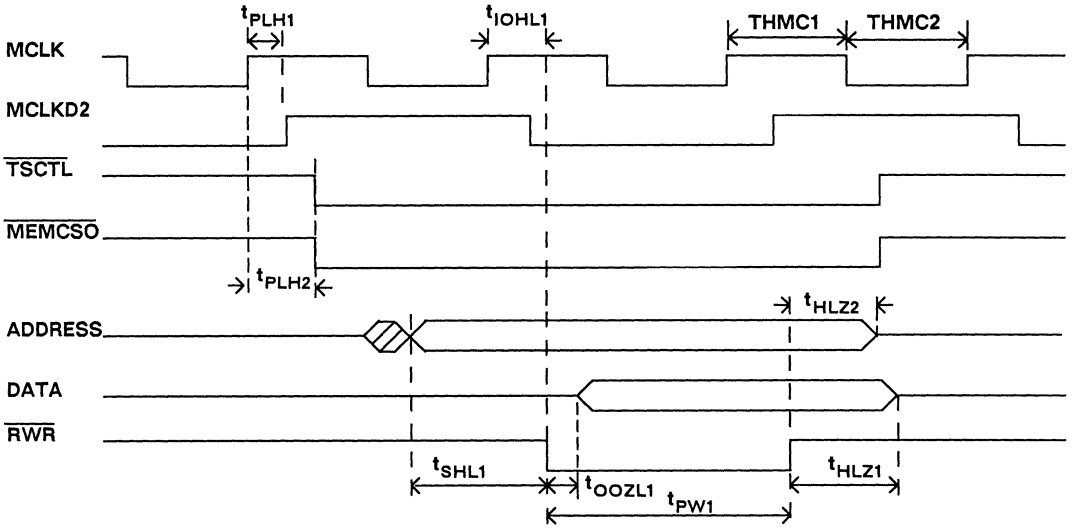
Figure 23. BURST DMA Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RRD}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{PW1}	$\overline{RRD}$ ↓ to $\overline{RRD}$ ↑	MCLK-5	MCLK+5	ns
t_{HLZ2}	$\overline{RRD}$ ↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-10	THMC1	ns
t_{HLZ1}	$\overline{RRD}$ ↑ to DATA High Impedance (DATA hold)	5	-	ns
t_{SLH1}	DATA valid to $\overline{RRD}$ ↑ (DATA setup)	40	-	ns
t_{PLH1} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑ to $\overline{TSCTL/MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑ to $\overline{RRD}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

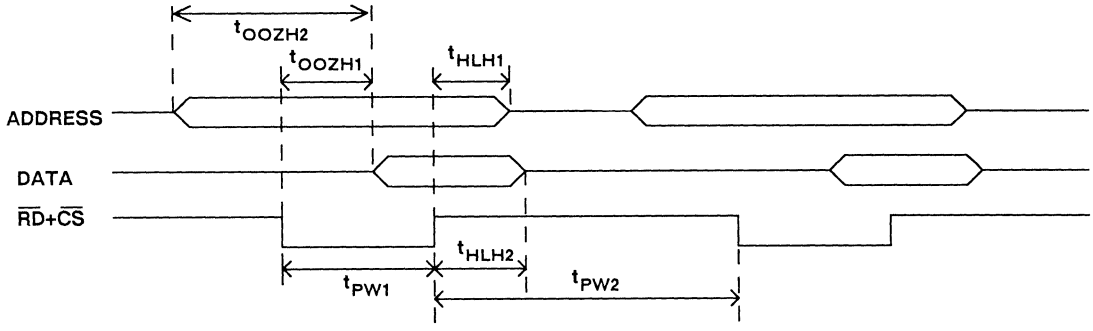
Figure 24. BCRTMP DMA Read Timing (One-Word Read)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{RWR}$ ↓ (ADDRESS setup)	THMC2-20	THMC2	ns
t_{OOZL1} (1)	$\overline{RWR}$↓ to DATA valid	0	30	ns
t_{HLZ1}	$\overline{RWR}$↑ to DATA High Impedance (DATA hold)	THMC1-20	THMC1	ns
t_{HLZ2}	$\overline{RWR}$↑ to ADDRESS High Impedance (ADDRESS hold)	THMC1-20	THMC1	ns
t_{PW1}	$\overline{RWR}$ ↓to $\overline{RWR}$ ↑	MCLK-5	MCLK+5	ns
t_{PLH1} (1)	MCLK ↑to MCLKD2 ↑	0	40	ns
t_{PLH2}	MCLK ↑to $\overline{TSCTL/MEMCSO}$ ↓	0	40	ns
t_{IOHL1} (1)	MCLK ↑to $\overline{RWR}$ ↓	0	60	ns

Note:
1. Guaranteed by test.

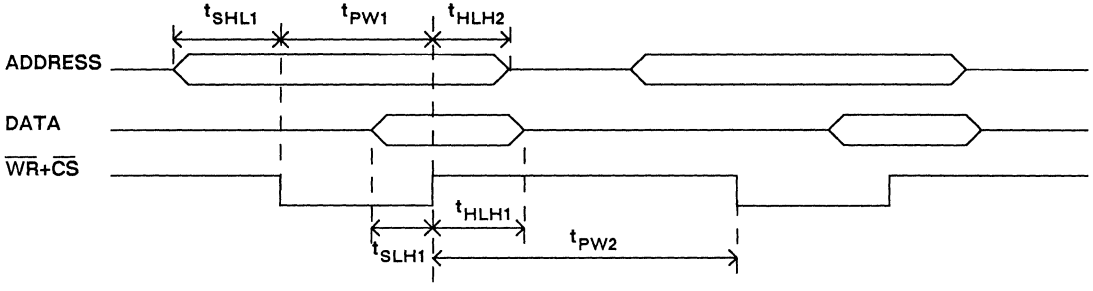
Figure 25. BCRTMP DMA Write Timing (One-Word Write)



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{OOZH2}	ADDRESS valid to DATA valid		–	80	ns
t_{HLH2}	$\overline{RD}+\overline{CS}$ ↑to DATA High Impedance	(DATA hold)	5	50	ns
t_{OOZH1} (1)	$\overline{RD}+\overline{CS}$ ↓to DATA valid	(DATA access)	–	60	ns
t_{HLH1}	$\overline{RD}+\overline{CS}$ ↑to ADDRESS High Impedance	(ADDRESS hold)	5	–	ns
t_{PW1}	$\overline{RD}+\overline{CS}$ ↓to $\overline{RD}+\overline{CS}$ ↑		60	–	ns
t_{PW2}	$\overline{RD}+\overline{CS}$ ↑to $\overline{RD}+\overline{CS}$ ↓		80	–	ns

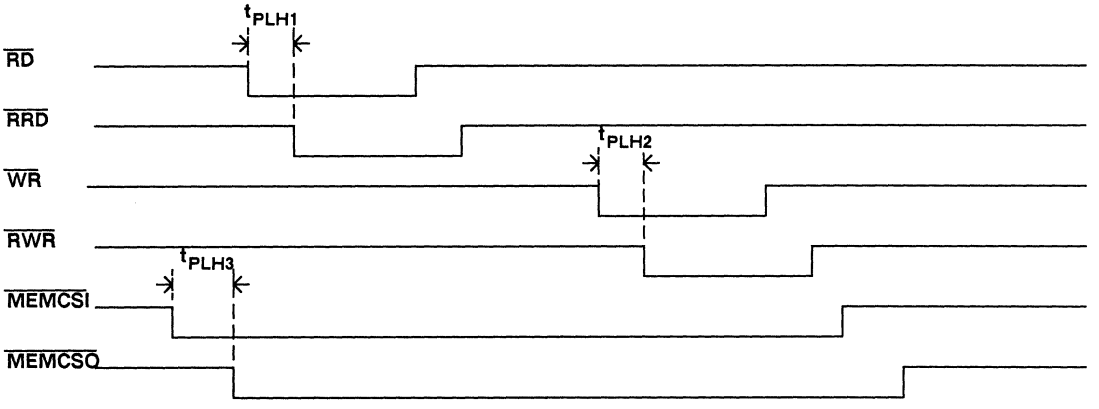
Notes:
1. Guaranteed by test.
2. User must adhere to both tOOZH1 and tOOZH2 timing constraints to ensure valid data.

Figure 26. BCRTMP Register Read Timing



SYMBOL	PARAMETER		MIN	MAX	UNITS
t_{SHL1}	ADDRESS valid to $\overline{WR}+\overline{CS}$ ↓	(ADDRESS setup)	60	–	ns
t_{SLH1}	DATA valid to $\overline{WR}+\overline{CS}$ ↑	(DATA setup)	60	–	ns
t_{PW1}	$\overline{WR}+\overline{CS}$↓ to $\overline{WR}+\overline{CS}$ ↑		60	–	ns
t_{HLH1}	$\overline{WR}+\overline{CS}$↑ to DATA High Impedance	(DATA hold)	10	–	ns
t_{HLH2}	$\overline{WR}+\overline{CS}$↑ to ADDRESS High Impedance	(ADDRESS hold)	10	–	ns
t_{PW2}	$\overline{WR}+\overline{CS}$↑ to $\overline{WR}+\overline{CS}$ ↓		80	–	ns

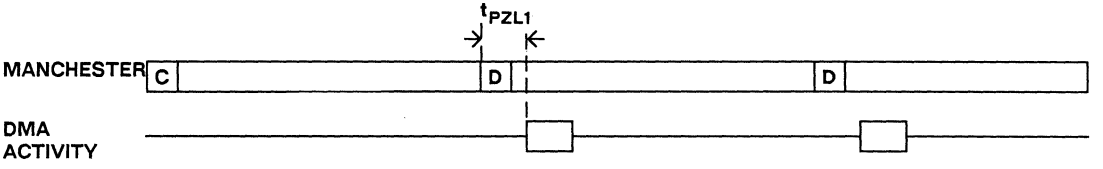
Figure 27. BCRTMP Register Write Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PLH1} (1)	$\overline{RD}$ ↓to $\overline{RRD}$ ↓	0	30	ns
t_{PLH2} (1)	$\overline{WR}$↓ to $\overline{RWR}$ ↓	0	30	ns
t_{PLH3} (1)	$\overline{MEMCSI}$ ↓to $\overline{MEMCSO}$ ↓	0	30	ns

Note:
1. Guaranteed by test.

Figure 28. BCRTMP Dual-Port Interface Timing Delays

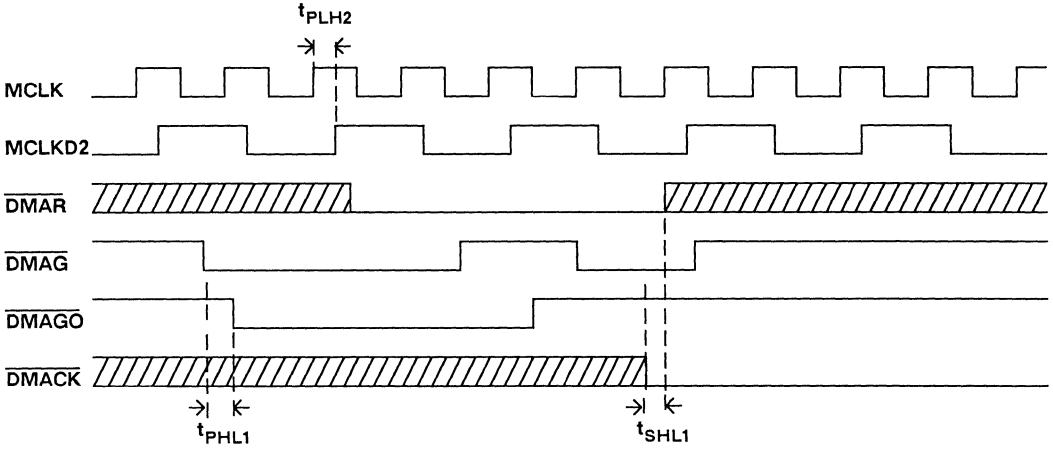


SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PZL1}	Data word to DMA activity	0	4	µs

This diagram indicates the relationship between the incoming Manchester code and DMA activity (i.e., $\overline{DMAR}$ ↓ to $\overline{DMACK}$↑).

Note:
The pulsewidth = (11 µs -t_{DMA} -t_{PZL1}) where t_{DMA} is the time to complete DMA activity (i.e., $\overline{DMAR}$↓ to $\overline{DMACK}$↑).

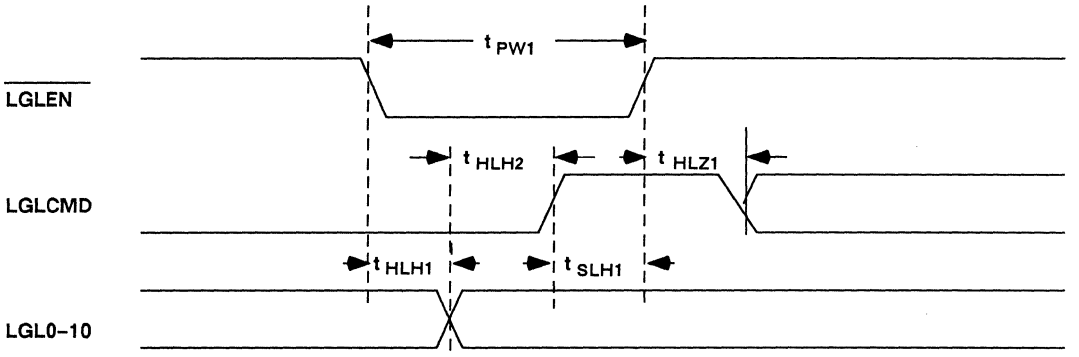
Figure 29. DMA Activity (RT Mode)



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PHL1}	$\overline{DMAG}$ ↓ to $\overline{DMAGO}$ ↓	0	30	ns
t_{SHL1}	$\overline{DMACK}$ ↓ to $\overline{DMAR}$ High Impedance	0	10	ns
t_{PLH2} (1)	MCLK ↑ to MCLKD2 ↑	0	40	ns

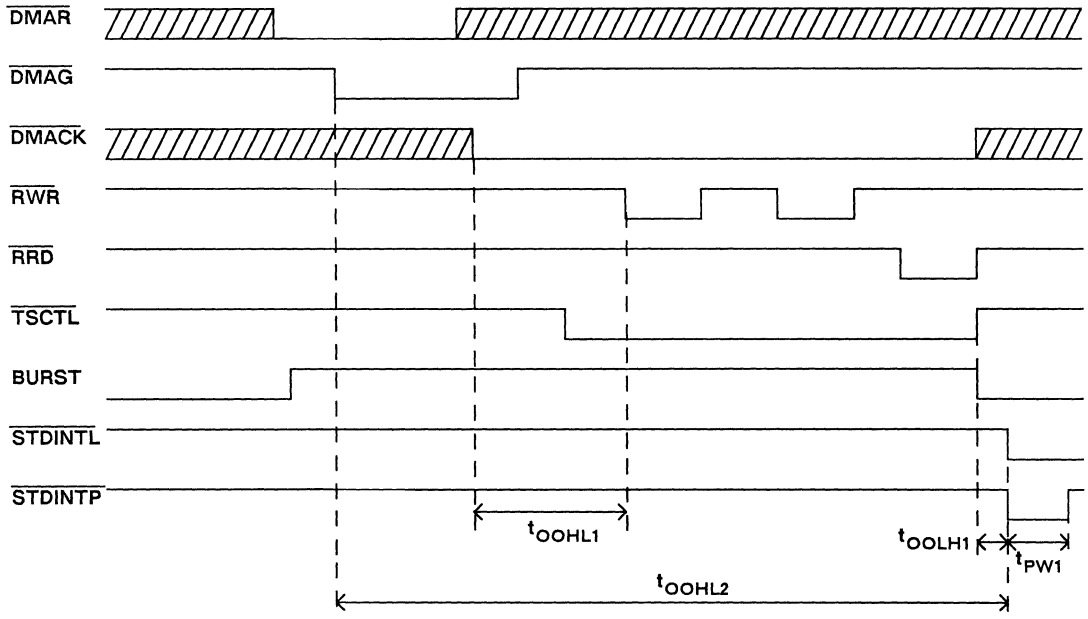
Notes:
1. Guaranteed by test.
2. When $\overline{DMAG}$ is asserted before $\overline{DMAR}$, the $\overline{DMAG}$ signal passes through the BCRTMP as $\overline{DMAGO}$.

Figure 30. BCRTMP Arbitration when $\overline{DMAG}$ is Asserted before Arbitration



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{PW1}	$\overline{\text{LGLEN}}$ ↓ to $\overline{\text{LGLEN}}$ ↑ (Pulse width)	750	—	ns
t_{HLH1}	$\overline{\text{LGLEN}}$ ↓ to Legalization Bus Valid	—	200	ns
t_{SLH1}	LGLCMD ↑ to $\overline{\text{LGLEN}}$ ↑ (Setup Time)	—	100	ns
t_{HLZ1}	$\overline{\text{LGLEN}}$ ↑ to LGLCMD Invalid (Hold Time)	0	—	ns
t_{HLH2}	Legalization Bus Valid to LGLCMD ↑ (Setup Time)	—	450	ns

Figure 31. BCRTMP Legalization Bus Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{OOLH1}	$\overline{TSCTL}$ ↑ to $\overline{STDINTP}$/$\overline{STDINTL}$ ↓	–	1	µs
t_{PW1}	$\overline{STDINTP}$ ↓ to $\overline{STDINTP}$ ↑	320	340	ns
t_{OOHL1}	$\overline{DMACK}$ ↓ to $\overline{RWR}$ ↓	3xMCLK–10	5xMCLK	ns
t_{OOHL2}	$\overline{DMAG}$ ↓ to $\overline{STDINTL}$ ↓	8xMCLK+0.5	10xMCLK+1	ns

Note:
Address and data bus relationships (not shown) are identical to figure 23.

Figure 32. BCRTMP Interrupt Log List Entry Operation Timing

13.0 Package Outline Drawings

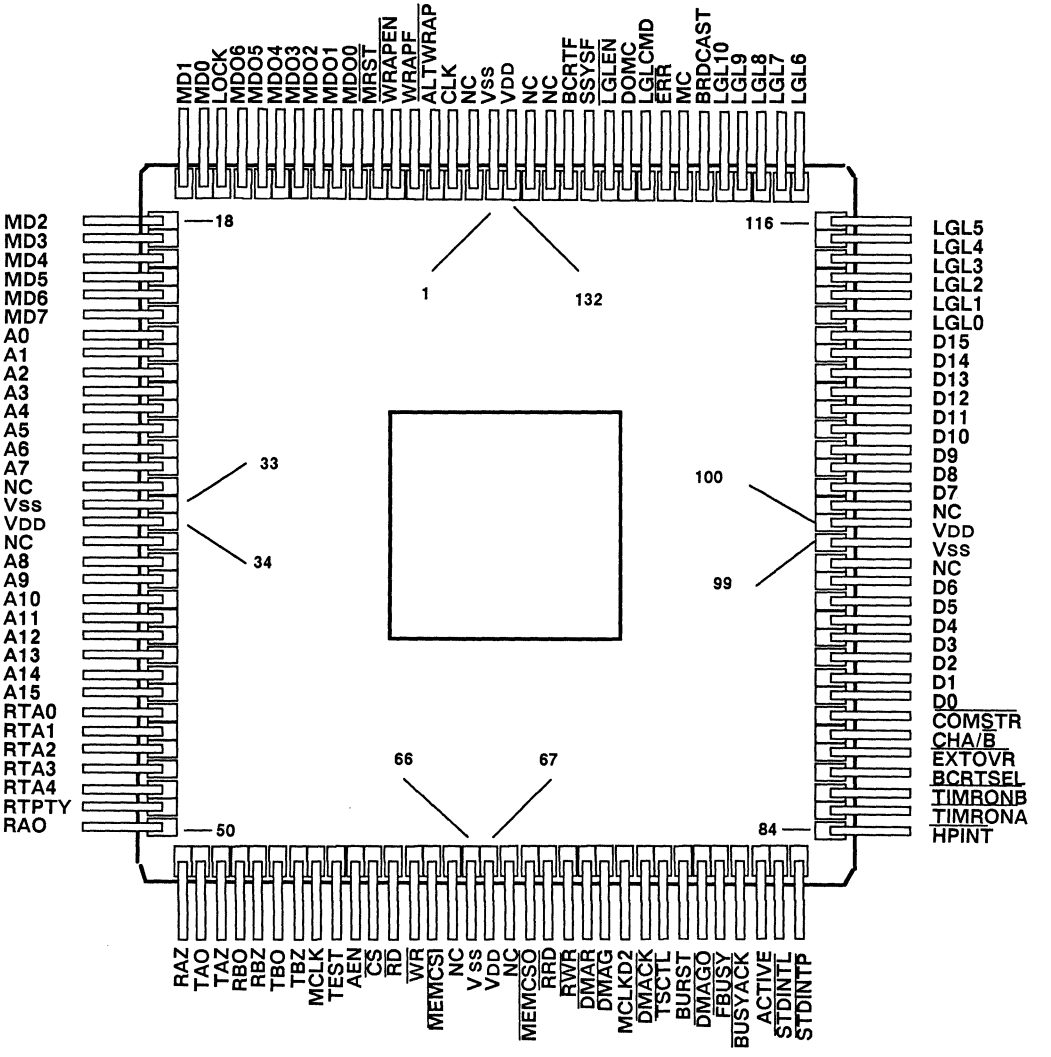
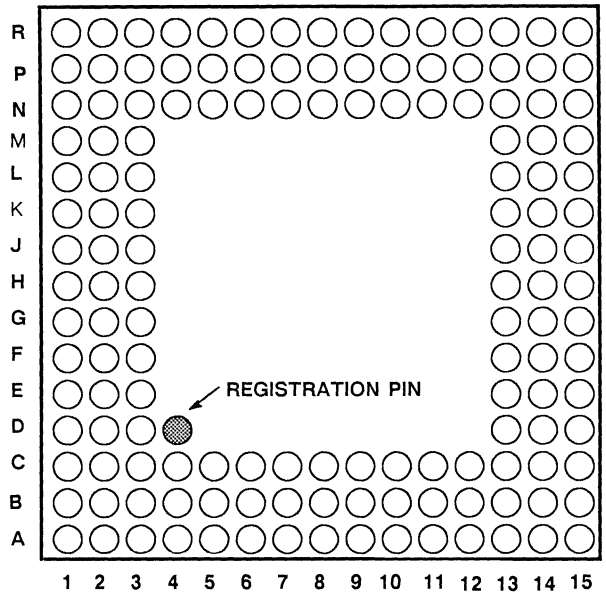


Figure 33a. BCRTMP Flatpack Identification (Top View)



A1 - NC	B1 - NC	C1 - LGL9	N1 - MDO2	P1 - MDO6	R1 - NC	D1 - BRDCAST	
A2 - LGL2	B2 - LGL5	C2 - LGL6	N2 - MDO5	P2 - MD1	R2 - NC	D2 - LGL7	
A3 - D14	B3 - LGL1	C3 - LGL4	N3 - MD0	P3 - MD2	R3 - MD5	D3 - NC	
A4 - D13	B4 - D15	C4 - LGL3	N4 - NC	P4 - MD3	R4 - MD7	D4 - NC	
A5 - D12	B5 - NC	C5 - LGL0	N5 - MD4	P5 - MD6	R5 - NC	D13 - ACTIVE	
A6 - D8	B6 - D10	C6 - D11	N6 - A0	P6 - A1	R6 - A4	D14 - $\overline{\text{BURST}}$	
A7 - D7	B7 - D9	C7 - VDD	N7 - A3	P7 - A2	R7 - A5	D15 - $\overline{\text{DMACK}}$	
A8 - D6	B8 - D5	C8 - Vss	N8 - Vss	P8 - A6	R8 - A7	E1 - NC	
A9 - D4	B9 - D1	C9 - $\overline{\text{D2}}$	N9 - VDD	P9 - A10	R9 - A8	E2 - LGL10	
A10 - D3	B10 - $\overline{\text{D0}}$	C10 - $\overline{\text{COMSTR}}$	N10 - A12	P10 - A11	R10 - A9	E3 - $\overline{\text{LGL8}}$	
A11 - NC	B11 - $\overline{\text{EXTOVR}}$	C11 - TIMRONB	N11 - RTA1	P11 - NC	R11 - A13	E13 - DMAGO	
A12 - CHA/$\overline{\text{B}}$	B12 - $\overline{\text{TIMRONA}}$	C12 - NC	N12 - RTA4	P12 - RTA0	R12 - A14	E14 - NC	
A13 - BCRTSEL	B13 - $\overline{\text{HPINT}}$	C13 - $\overline{\text{STDINTL}}$	N13 - RTPTY	P13 - RTA2	R13 - A15	E15 - MCLKD2	
A14 - NC	B14 - $\overline{\text{STDINTP}}$	C14 - $\overline{\text{FBUSY}}$	N14 - RAZ	P14 - RAO	R14 - RTA3		
A15 - NC	B15 - $\overline{\text{BUSYACK}}$	C15 - $\overline{\text{TSCTL}}$	N15 - RBO	P15 - NC	R15 - NC		

F1 - $\overline{\text{LGLEN}}$	G1 - SSYSF	H1 - NC	J1 - CLK	K1 - $\overline{\text{ALTWRAP}}$	L1 - MDO0	M1 - MDO1	
F2 - LGLCMD	G2 - $\overline{\text{ERR}}$	H2 - BCRTF	J2 - WRAPF	K2 - $\overline{\text{WRAPEN}}$	L2 - NC	M2 - MDO3	
F3 - $\overline{\text{MC}}$	G3 - DOMC	H3 - VDD	J3 - Vss	K3 - $\overline{\text{MRST}}$	L3 - MDO4	M3 - LOCK	
F13 - $\overline{\text{DMAG}}$	G13 - $\overline{\text{VDD}}$	H13 - $\overline{\text{Vss}}$	J13 - AEN	K13 - TBZ	L13 - TAZ	M13 - NC	
F14 - $\overline{\text{DMAR}}$	G14 - $\overline{\text{RWR}}$	H14 - $\overline{\text{WR}}$	J14 - TEST	K14 - MCLK	L14 - RBZ	M14 - TAO	
F15 - $\overline{\text{RRD}}$	G15 - $\overline{\text{MEMCSO}}$	H15 - $\overline{\text{MEMCSI}}$	J15 - $\overline{\text{RD}}$	K15 - $\overline{\text{CS}}$	L15 - NC	M15 - TBO	

Figure 33b. BCRTMP Pingrid Array Pin Identification (Bottom View)

UT1553B RTR Remote Terminal with RAM

Features

- ☐ Complete MIL-STD-1553B remote terminal interface
- ☐ 1K x 16 of on-chip static RAM for message data, completely accessible to host
- ☐ Self-test capability, including continuous loop-back compare
- ☐ Programmable memory mapping via pointers for efficient use of internal memory, including buffering multiple messages per subaddress
- ☐ RT-RT Terminal Address Compare
- ☐ Command word stored with incoming data for enhanced data management
- ☐ User selectable RAM Busy (RBUSY) signal for slow or fast processor interfacing
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B, also Standard Military Drawing available
- ☐ Available in 68-pin pingrid array, and 68-lead leadless chip carrier packages

Introduction

The UT1553B RTR is a monolithic CMOS VLSI solution to the requirements of the dual-redundant MIL-STD-1553B interface. Designed to reduce cost and space, the RTR integrates the remote terminal logic with a user-configured 1K x 16 static RAM. In addition, the RTR has a flexible subsystem interface to permit use with most processors or controllers.

The RTR provides all protocol, data handling, error checking, and memory control functions, as well as comprehensive self-test capabilities. The RTR's memory meets all of MIL-STD-1553B message storage needs through user-defined memory mapping. This memory-mapped architecture allows multiple message buffering at each subaddress.

3

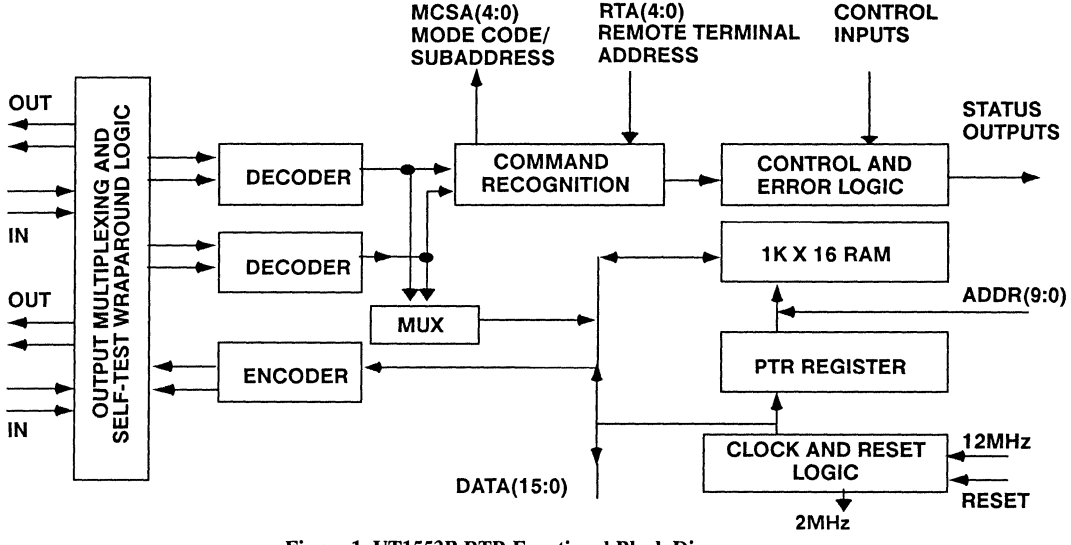


Figure 1. UT1553B RTR Functional Block Diagram

Table of Contents

1.0 Architecture And Operation

The UT1553B RTR is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system. The RTR's MIL-STD-1553B interface includes encoding/decoding logic, error detection, command recognition, 1K x 16 of SRAM, pointer registers, clock, and reset circuits.

1.1 Memory Map and Host Memory Interface

The host can access the 1K x 16 RAM memory like a standard RAM device through the 10-bit address and 16-bit data buses. The host uses the Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) signals to control data transfer to and from memory. When the RTR requires access to its own internal RAM, it asserts the RBUSY signal to alert the host. The RBUSY signal is programmable via the internal Control Register to be asserted either 5.7 µs or 2.7 µs prior to the RTR needing access to its internal RAM.

The RTR stores MIL-STD-1553B messages in 1K x 16 of on-chip RAM. For efficient use of the 1K x 16 memory on the RTR, the host programs a set of pointers to map where the 1553B message is stored. The RTR uses the upper 64 words (address 3C0 (hex) through 3FF (hex)) as pointers. The RTR provides pointers for all 30 receive subaddresses, all 30 transmit subaddresses, and four mode code commands with associated data words as defined in MIL-STD-1553B. The remaining 960 words of memory contain receive, transmit, and mode code data in a host-defined structure.

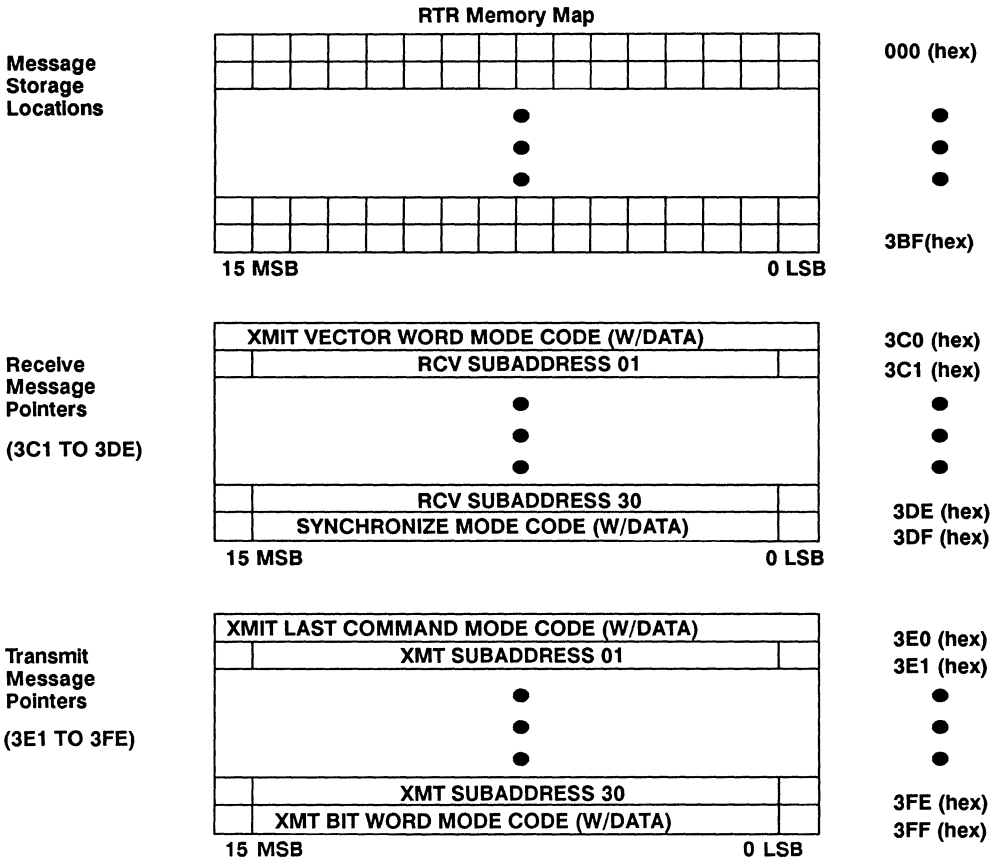


Figure 2. RTR Memory Map

1.2 RTR RAM Pointer Structure

The RAM 16-bit pointers have a 6-bit index field and a 10-bit address field. The 6-bit index field allows for the storage of up to 64 messages per subaddress. A message consists of the 1553 command word and its associated data words.

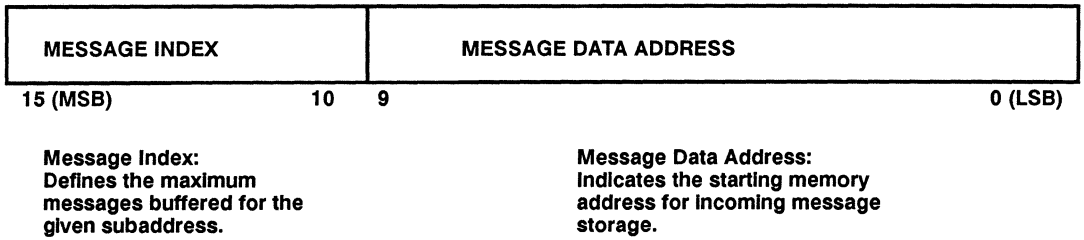


Figure 3. Message Pointer Structure

The 16-bit pointer for Transmit Last Command Mode Code is located at memory location 3E0 (hex). The Transmit Last Command Mode Code pointer buffers up to 63 command words. An example of command word storage follows:

Example:

3E0 (hex) Contents = FC00 (hex)

11 1111 00 0000 0000

Address Field = 000 (hex)
Index Field = 3F (hex)

First command word storage location (3E0=F801):

Address Field = 001 (hex)
Index Field = 3E (hex)

Sixty-third command word storage location (3E0=003F):

Address Field = 03F (hex)
Index Field = 00 (hex)

Sixty-fourth command word storage location (3E0=003F) (previous command word overwritten):

Address Field = 03F (hex)
Index Field = 00 (hex)

The Transmit Last Command Mode Code has Address Field boundary conditions for the location of command word buffers. The host can allocate a maximum 63 sequential locations following the Address Field starting address. For proper operation, the Address Field must start on an I x 40 (hex) address boundary, where I is greater than or equal to zero and less than or equal to 14. A list of valid Index and Address Fields follows:

I	Valid Index Fields	Valid Address Fields
0	3F (hex) to 00 (hex)	000 (hex) to 03F (hex)
1	3F (hex) to 00 (hex)	040 (hex) to 07F (hex)
2	3F (hex) to 00 (hex)	080 (hex) to 0BF (hex)
3	3F (hex) to 00 (hex)	0C0 (hex) to 0FF (hex)
4	3F (hex) to 00 (hex)	100 (hex) to 13F (hex)
5	3F (hex) to 00 (hex)	140 (hex) to 17F (hex)
6	3F (hex) to 00 (hex)	180 (hex) to 1BF (hex)
7	3F (hex) to 00 (hex)	1C0 (hex) to 1FF (hex)
8	3F (hex) to 00 (hex)	200 (hex) to 23F (hex)
9	3F (hex) to 00 (hex)	240 (hex) to 27F (hex)
10	3F (hex) to 00 (hex)	280 (hex) to 2BF (hex)
11	3F (hex) to 00 (hex)	2C0 (hex) to 2FF (hex)
12	3F (hex) to 00 (hex)	300 (hex) to 33F (hex)
13	3F (hex) to 00 (hex)	340 (hex) to 37F (hex)
14	3F (hex) to 00 (hex)	380 (hex) to 3BF (hex)

Subaddress/Mode Code		RAM Location	Subaddress/Mode Code		RAM Location
Transmit Vector Word Mode Code		3C0 (hex)	Transmit Last Command Mode Code		3E0 (hex)
Receive Subaddress	01	3C1 (hex)	Transmit Subaddress	01	3E1 (hex)
Receive Subaddress	02	3C2 (hex)	Transmit Subaddress	02	3E2 (hex)
Receive Subaddress	03	3C3 (hex)	Transmit Subaddress	03	3E3 (hex)
Receive Subaddress	04	3C4 (hex)	Transmit Subaddress	04	3E4 (hex)
Receive Subaddress	05	3C5 (hex)	Transmit Subaddress	05	3E5 (hex)
Receive Subaddress	06	3C6 (hex)	Transmit Subaddress	06	3E6 (hex)
Receive Subaddress	07	3C7 (hex)	Transmit Subaddress	07	3E7 (hex)
Receive Subaddress	08	3C8 (hex)	Transmit Subaddress	08	3E8 (hex)
Receive Subaddress	09	3C9 (hex)	Transmit Subaddress	09	3E9 (hex)
Receive Subaddress	10	3CA (hex)	Transmit Subaddress	10	3EA (hex)
Receive Subaddress	11	3CB (hex)	Transmit Subaddress	11	3EB (hex)
Receive Subaddress	12	3CC (hex)	Transmit Subaddress	12	3EC (hex)
Receive Subaddress	13	3CD (hex)	Transmit Subaddress	13	3ED (hex)
Receive Subaddress	14	3CE (hex)	Transmit Subaddress	14	3EE (hex)
Receive Subaddress	15	3CF (hex)	Transmit Subaddress	15	3EF (hex)
Receive Subaddress	16	3D0 (hex)	Transmit Subaddress	16	3F0 (hex)
Receive Subaddress	17	3D1 (hex)	Transmit Subaddress	17	3F1 (hex)
Receive Subaddress	18	3D2 (hex)	Transmit Subaddress	18	3F2 (hex)
Receive Subaddress	19	3D3 (hex)	Transmit Subaddress	19	3F3 (hex)
Receive Subaddress	20	3D4 (hex)	Transmit Subaddress	20	3F4 (hex)
Receive Subaddress	21	3D5 (hex)	Transmit Subaddress	21	3F5 (hex)
Receive Subaddress	22	3D6 (hex)	Transmit Subaddress	22	3F6 (hex)
Receive Subaddress	23	3D7 (hex)	Transmit Subaddress	23	3F7 (hex)
Receive Subaddress	24	3D8 (hex)	Transmit Subaddress	24	3F8 (hex)
Receive Subaddress	25	3D9 (hex)	Transmit Subaddress	25	3F9 (hex)
Receive Subaddress	26	3DA (hex)	Transmit Subaddress	26	3FA (hex)
Receive Subaddress	27	3DB (hex)	Transmit Subaddress	27	3FB (hex)
Receive Subaddress	28	3DC (hex)	Transmit Subaddress	28	3FC (hex)
Receive Subaddress	29	3DD (hex)	Transmit Subaddress	29	3FD (hex)
Receive Subaddress	30	3DE (hex)	Transmit Subaddress	30	3FE (hex)
Synchronize w/Data Word Mode Code		3DF (hex)	Transmit Bit Word Mode Code		3FF (hex)

1.3 Internal Registers

The RTR uses two internal registers to allow the host to control the RTR operation and monitor its status. The host uses the Control ($\overline{CTRL}$) signal along with Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) to read the 16-bit Status Register or write to the 11-bit Control Register. No address data is needed to select a register. The Control Register toggles bits in the MIL-STD-1553B status word, enables the biphase inputs, recognizes broadcast commands, determines RAM Busy (RBUSY) timing, selects terminal active flag, and puts the part in self-test mode. The Status Register supplies operational status of the UT1553B RTR to the host. These registers must be initialized before attempting RTR operation. Internal registers can be accessed while RBUSY is active.

Control Register (Write Only)
The 11-bit write-only Control Register manages the operation of the RTR. Write to the Control Register by applying a logic one to $\overline{OE}$, and a logic zero to $\overline{CTRL}$, $\overline{CS}$, and RD/$\overline{WR}$. Data is loaded into the Control Register via I/O pins DATA(12:0). Control register write must occur 50 ns before the rising edge of $\overline{COMSTR}$ to latch data into outgoing status word.

Bit Number	Initial Condition	Description
Bit 0	[1]	Channel A Enable. A logic 1 enables Channel A biphase inputs.
Bit 1	[1]	Channel B Enable. A logic 1 enables Channel B biphase inputs.
Bit 2	[0]	Terminal Flag. A logic 1 sets the Terminal Flag bit of the Status Word.
Bit 3	[1]	System Busy. A logic 1 sets the Busy bit of the Status Word and limits RTR access to the memory. No data words can be retrieved or stored; command words will be stored.
Bit 4	[0]	Subsystem Busy. A logic 1 sets the Subsystem Flag bit of the Status Word.
Bit 5	[0]	Self-Test Channel Select. This bit selects which channel the self-test checks; a logic 1 selects Channel A and a logic 0 selects Channel B.
Bit 6	[0]	Self-Test Enable. A logic 1 places the RTR in the internal self-test mode and inhibits normal operation. Channels A and B should be disabled if self-test is chosen.
Bit 7	[0]	Service Request. A logic 1 sets the Service Request bit of the Status Word.
Bit 8	[0]	Instrumentation. A logic 1 sets the Instrumentation bit of the Status Word.
Bit 9	[1]	Broadcast Enable. A logic 1 enables the RTR to recognize broadcast commands.
Bit 10	[X]	Do not care.
Bit 11	[X]	Do not care.
Bit 12	[1]	RBUSY Time Select. A logic 1 selects a 5.7 μs RBUSY alert; a logic 0 selects a 2.7 μs RBUSY alert.

[] - Values in parentheses indicate the initialized values of these bits.

CONTROL REGISTER (WRITE ONLY):

X	X	X	RBUSY TS	X	X	BCEN	INS	SRQ	ITST	ITCS	SUBS	BUSY	TF	CH B EN	CH A EN
			[1]			[1]	[0]	[0]	[0]	[0]	[0]	[1]	[0]	[1]	[1]

MSB LSB

[ ] defines reset state
X do not care

Figure 4a. Control Register

Status Register (Read Only)

The 16-bit read-only Status Register provides the RTR system status. Read the Status Register by applying a logic 0 to $\overline{CTRL}$, $\overline{CS}$, and $\overline{OE}$, and a logic 1 to RD/$\overline{WR}$. The 16-bit contents of the Status Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
Bit 0	[0]	MCSA0. The LSB of the mode code or subaddress as indicated by the logic state of bit 5.
Bit 1	[0]	MCSA1. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 2	[0]	MCSA2. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 3	[0]	MCSA3. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 4	[0]	MCSA4. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 5	[0]	$\overline{MC}$/SA. A logic 1 indicates that bits 4 through 0 are the subaddress of the last command word, and that the last command word was a normal transmit or receive command. A logic 0 indicates that bits 4 through 0 are a mode code, and that the last command was a mode command.
Bit 6	[1]	Channel A/$\overline{B}$. A logic 1 indicates that the most recent command arrived on Channel A; a logic 0 indicates that it arrived on Channel B.
Bit 7	[1]	Channel B Enabled. A logic 1 indicates that Channel B is available for both reception and transmission.
Bit 8	[1]	Channel A Enabled. A logic 1 indicates that Channel A is available for both reception and transmission.
Bit 9	[1]	Terminal Flag Enabled. A logic 1 indicates that the Bus Controller has not issued an Inhibit Terminal Flag Mode Code. A logic 0 indicates that the Bus Controller, via the above mode code, is overriding the host system's ability to set the Terminal Flag bit of the status word.
Bit 10	[1]	Busy. A logic 1 indicates the Busy bit is set. This bit is reset when the System Busy bit in the Control Register is reset.
Bit 11	[0]	Self-Test. A logic 1 indicates that the chip is in the internal self-test mode. This bit is reset when the self-test is terminated.
Bit 12	[0]	TA Parity Error. A logic 1 indicates the wrong Terminal Address parity; it causes the biphase inputs to be disabled. TA Parity Error results in the Message Error bit being set to a logic one, and Channels A and B become disabled.
Bit 13	[0]	Message Error. A logic 1 indicates that a message error has occurred since the last Status Register read. This bit is not reset until the Status Register has been examined. Message error condition must be removed before reading the Status Register to reset the Message Error bit.
Bit 14	[0]	Valid Message. A logic 1 indicates that a valid message has been received since the last Status Register read. This bit is not reset until the Status Register has been examined.
Bit 15	[0]	Terminal Active. A logic 1 indicates the device is executing a transmit or receive operation. Same as $\overline{TERACT}$ output except active high.

[] - Values in parentheses indicate the initialized values of these bits.

STATUS REGISTER (READ ONLY):

TERM ACTV	VAL MESS	MESS ERR	TAPA ERR	SELF-TEST	BUSY	TFEN	CH A EN	CH B EN	CHNL A/B	$\overline{MC}$/ SA	MCSA 4	MCSA 3	MCSA 2	MCSA 1	MCSA 0
[0] MSB	[0]	[0]	[0]	[0]	[1]	[1]	[1]	[1]	[1]	[0]	[0]	[0]	[0]	[0]	[0] LSB

[ ] defines reset state

Figure 4b. Status Register

1.4 Mode Code and Subaddress

The UT1553B RTR provides subaddress and mode code decoding meeting MIL-STD-1553B. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Upon command word validation and decode, status pins MCSA(4:0) and $\overline{MC}$/SA become valid. Status pin $\overline{MC}$/SA will indicate whether the data on pins MCSA(4:0) is mode code or subaddress information. Status Register bits 0 through 5 contain the same information as pins MCSA(4:0) and $\overline{MC}$/SA.

The system designer can use signals MCSA(4:0), $\overline{MC}$/SA, $\overline{BRDCST}$, RTRT, etc. to illegalize mode codes, subaddresses, and other message formats (broadcast and RT-to-RT) via the Illegal Command (ILLCOM) input to the part (see figure 21 on page 31).

RTR MODE CODE HANDLING PROCEDURE

T/$\overline{R}$	Mode Code	Function	Operation
0	10100	Selected Transmitter Shutdown (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10101	Override Selected Transmitter Shutdown (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10001	Synchronize (w/Data)	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
1	00001	Synchronize (1)	1. Command word stored 2. Status word transmitted
1	00010	Transmit Status Word (3)	1. Command word stored 2. Status word transmitted
1	00011	Initiate Self-Test (1)	1. Command word stored 2. Status word transmitted
1	00100	Transmitter Shutdown	1. Command word stored 2. Alternate bus shutdown 3. Status word transmitted
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Alternate bus enabled 3. Status word transmitted
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit set to zero and disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag	1. Command word stored 2. Terminal Flag bit enabled, but not set to logic one 3. Status word transmitted
1	01000	Reset Remote Terminal (1)	1. Command word stored 2. Status word transmitted
1	10010	Transmit Last Command Word (3)	1. Status word transmitted 2. Last command word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Notes:

1. Further host intersaction required for mode code operation.
2. Reserved mode code; A) MERR pin asserted, B) MESS ERR bit set, C) status word transmitted (ME bit set to logic one).
3. Status Word not affected.
4. Undefined mode codes are treated as reserved mode codes.

1.5 MIL-STD-1553B Subaddress and Mode Code Definitions

Table 1. Subaddress and Mode Code Definitions Per MIL-STD-1553B

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	(1)	(1)	Mode Code Indicator
00001 (01)	User Defined	User Defined	
00010 (02)	User Defined	User Defined	
00011 (03)	User Defined	User Defined	
00100 (04)	User Defined	User Defined	
00101 (05)	User Defined	User Defined	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	User Defined	User Defined	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	User Defined	User Defined	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	User Defined	User Defined	
01111 (15)	User Defined	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	User Defined	User Defined	
10100 (20)	User Defined	User Defined	
10101 (21)	User Defined	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	User Defined	User Defined	
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	(1)	(1)	Mode Code Indicator

Notes:
1. Refer to mode code assignments per MIL-STD-1553B.

1.6 Terminal Address

The Terminal Address of the RTR is programmed via five input pins: RTA(4:0) and RTPTY. Asserting $\overline{MRST}$ latches the RTR's Terminal Address from pins RTA(4:0) and parity bit RTPTY. The address and parity cannot change until the next assertion of the $\overline{MRST}$. The parity of the Terminal Address is odd; input pin RTPTY is set to a logic state to satisfy this requirement. A logic 1 on Status Register bit 12 indicates incorrect Terminal Address parity. An example follows:

RTA(4:0) = 05 (hex) = 00101
RTPTY = 1 (hex) = 1
Sum of 1's = 3 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 0 (hex) = 0
Sum of 1's = 1 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 1 (hex) = 1
Sum of 1's = 2 (even), Status Register bit 12 = 1

The RTR checks the Terminal Address and parity on Master Reset. With Broadcast disabled, RTA (4:0) = 11111 operates as a normal RT address.

1.7 Internal Self-Test

Setting bit 6 of the Control Register to a logic one enables the internal self-test. Disable Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The self-test capability of the RTR is based on the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the encoder is fed back to the decoder, the RTR will recognize the incoming status word as a command word and thus cause the RTR to transmit another status word. After the host invokes self-test, the RTR self-test logic forces a status word transmission even though the RTR has not received a valid command. The status word is sent to decoder A or B depending on the channel the host selected for self-test. The self-test is controlled by the host periodically changing the bit patterns in the status word being transmitted. Writing to the Control Register bits 2, 3, 4, 7, and 8 changes the status word. Monitor the self-test by sampling either the Status Register or the external status pins (i.e. Command Strobe ($\overline{COMSTR}$), Transmit/Receive (T/$\overline{R}$)). For more detailed explanation of internal self-test, consult UTMC publication *RTR/RTS Internal Self-Test Routine.*

1.8 Power-up and Master Reset

After power-up, reset initializes the part with its biphase ports enabled, latches the Terminal Address, and turns on the busy option. The device is ready to accept commands from the MIL-STD-1553B bus. The busy flag is asserted while the host is loading the message pointers and messages. After this task is completed, the host removes the busy condition via a Control Register write to the RTR. On power-up if the terminal address parity (odd) is incorrect, the biphase inputs are disabled and the message error pin (MERR) is asserted. This condition can also be monitored via bit 12 of the Status Register. The MERR pin is negated on reception of first valid command.

1.9 Encoder and Decoder

The RTR interfaces directly to a bus transmitter/ receiver via the RTR Manchester II encoder/decoder. The UT1553B RTR receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RTR processes each incoming data word for correct format and checks the control logic for correct word count and contiguous data. If an invalid message error is detected, the message error pin is asserted, the RTR ceases processing the remainder (if any) of the message, and it then suppresses status word transmission. Upon command validation recognition, the external status outputs are enabled. Reception of illegal commands does not suppress status word transmission.

The RTR automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the transmitter error pin (TXERR) is asserted. In addition to the loop-back compare test, a timer precludes a transmission greater than 760 microseconds by the assertion of Fail-safe Timer ($\overline{TIMERON}$). This timer is reset upon receipt of another command.

1.10 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic makes sure that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the Message Error bit and suppressing transmission of the status word. (RT-to-RT transfer time-out = 54 μs)

1.11 Illegal Command Decoding

The host has the option of asserting the ILLCOM pin to illegalize a received command word. On receipt of an illegal command, the RTR sets the Message Error bit in the status word, sets the message error output, and sets the message error latch in the Status Register.

The following RTR outputs may be used to externally decode an illegal command, Mode Code or Subaddress indicator ($\overline{MC}$/SA), Mode Code or Subaddress bus MCSA(4:0), Command Strobe ($\overline{COMSTR}$), Broadcast ($\overline{BRDCST}$), and Remote Terminal to Remote Terminal transfer (RTRT) (see figure 21 on page 31.).

To illegalize a transmit command, the ILLCOM pin must be asserted within 3.3 µs after VALMSG goes to a logic 1 if the RTR is to respond with the Message Error bit of the status word at a logic 1. If the illegal command is mode code 2, 4, 5, 6, 7, or 18, the ILLCOM pin must be asserted within 664 ns after Command Strobe ($\overline{COMSTR}$) transitions to logic 0. Asserting the ILLCOM pin within the 664 ns inhibits the mode code function. For mode code illegalization, assert the ILLCOM pin until the VALMSG signal is asserted.

For an illegal receive command, the ILLCOM pin is asserted within 18.2 µs after the $\overline{COMSTR}$ transitions to a logic 0 in order to suppress data words from being stored. In addition, the ILLCOM pin must be at a logic 1 throughout the reception of the message until VALMSG is asserted. This does not apply to illegal transmit commands since the status word is transmitted first.

The above timing conditions also apply when the host externally decodes an illegal broadcast command. The host must remove the illegal command condition so that the next command is not falsely decoded as illegal.

2.0 Memory Map Example

Figures 5 and 6 illustrate the UT1553B RTR buffering three receive command messages to Subaddress 4. The receive message pointer for Subaddress 4 is located at 03C4 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03C4 (hex) point to the memory location where the first receive message is stored. The Address Field defined as bits 0 through 9 of address 03C4 (hex) contain address information. The Index Field defined as bits 10 through 15 of address 03C4 (hex) contain the message buffer index (i.e. number of messages buffered).

Figure 5 demonstrates the updating of the message pointer as each message is received and stored. The memory storage of these three messages is shown in figure 6. After receiving the third message for Subaddress 4 (i.e. Index Field equals zero) the Address Field of the message pointer is not incremented. If the host does not update the receive message pointer for Subaddress 4 before the next receive command for Subaddress 4 is accepted, the third message will be overwritten.

Figures 7 and 8 show an example of multiple message retrieval from Subaddress 16 upon reception of a MIL-STD-1553B transmit command. The message pointer for transmit Subaddress 16 is located at 03F0 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03F0 (hex) point to the memory location where the first message data words are stored.

Figure 7 demonstrates the updating of the message pointer as each message is received and stored. The data memory for these three messages is shown in figure 8.

Example:
Remote terminal will receive and buffer three MIL-STD-1553 receive commands of various word lengths to Subaddress 4.

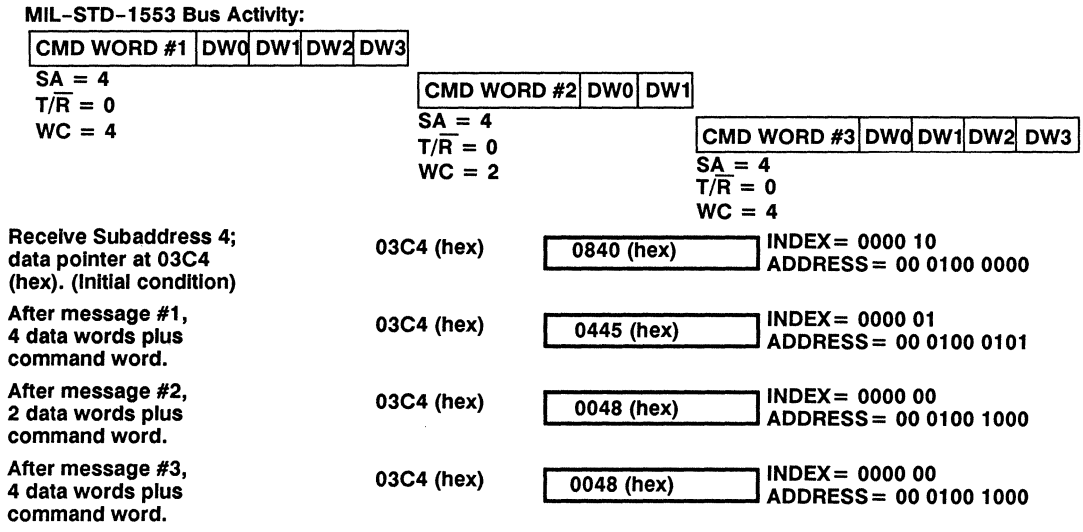


Figure 5. RTR Message Handling

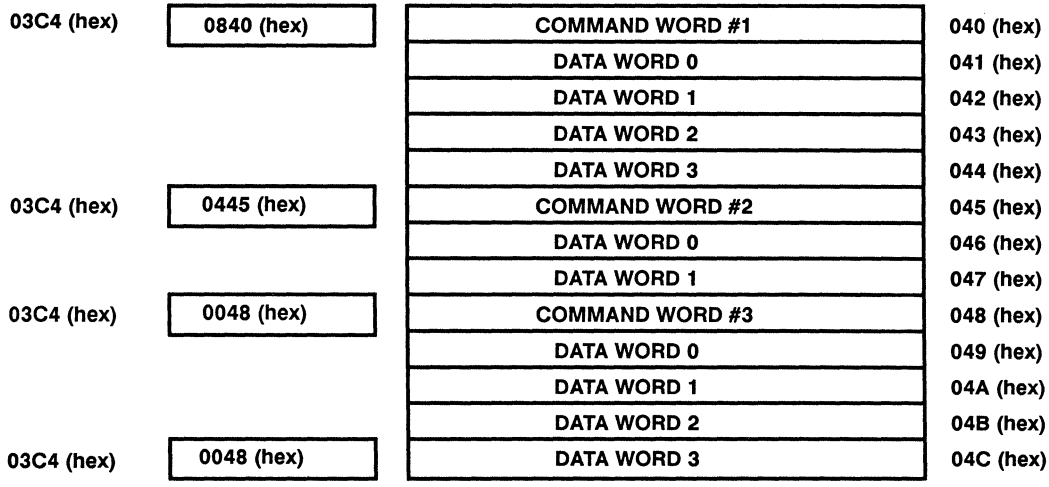


Figure 6. Memory Storage Subaddress 4

Example:
Remote terminal will transmit and buffer three MIL-STD-1553 transmit commands of various word lengths to Subaddress 16.

MIL-STD-1553 Bus Activity:

CMD WORD #1	SW	DW0	DW1	DW2	DW3

SA = 16
T/R = 1
WC = 4

CMD WORD #2	SW	DW0	DW1

SA = 16
T/R = 1
WC = 2

CMD WORD #3	SW	DW0	DW1	DW2	DW3

SA = 16
T/R = 1
WC = 4

Transmit Subaddress 16; data pointer at 03F0 (hex). (Initial condition)	03F0 (hex)	0830 (hex)	INDEX = 0000 10 ADDRESS = 00 0011 0000
After message #1, 4 data words.	03F0 (hex)	0434 (hex)	INDEX = 0000 01 ADDRESS = 00 0011 0100
After message #2, 2 data words.	03F0 (hex)	0036 (hex)	INDEX = 0000 00 ADDRESS = 00 0011 0110
After message #3, 4 data words.	03F0 (hex)	0036 (hex)	INDEX = 0000 00 ADDRESS = 00 0011 0110

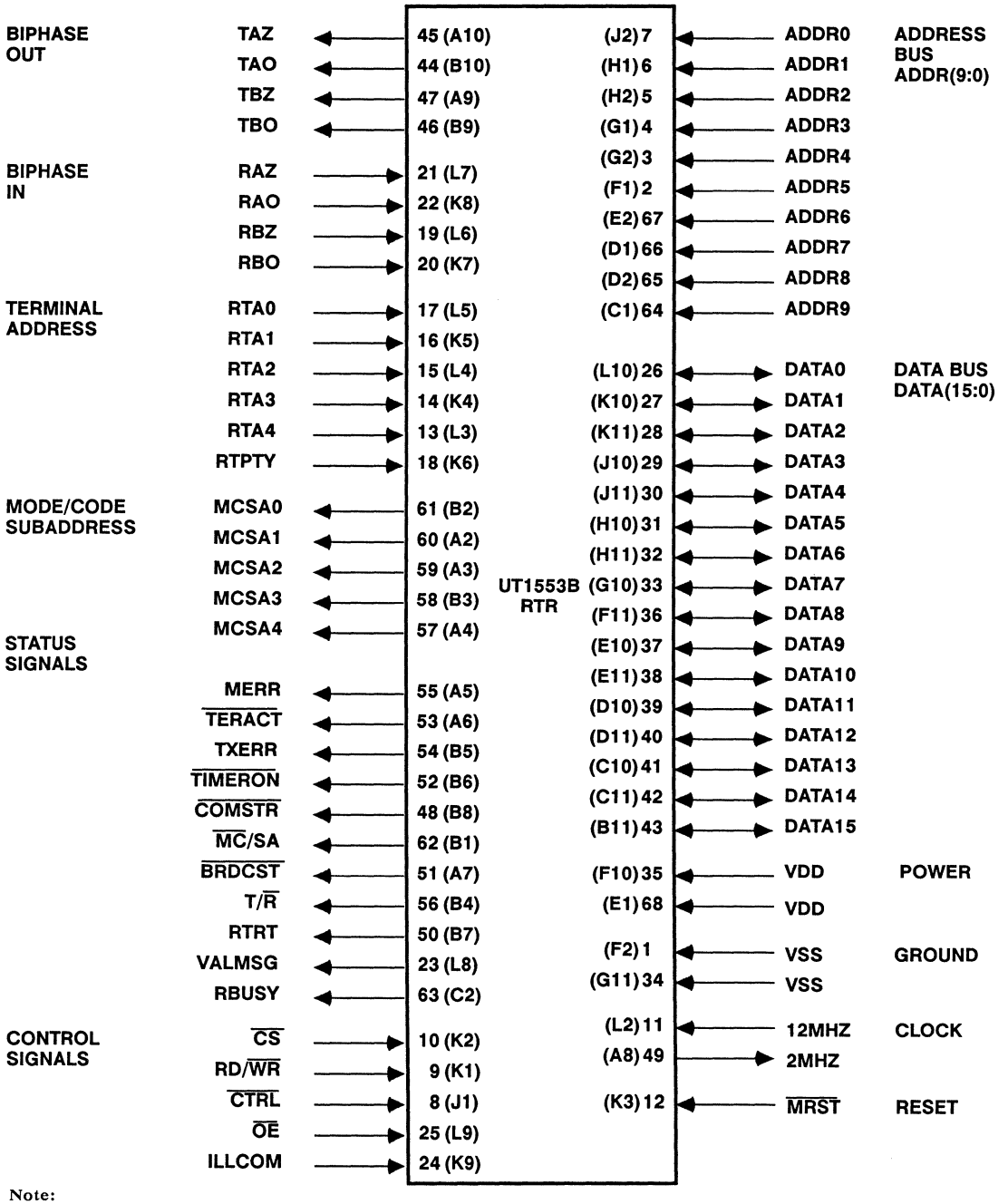
Figure 7. RTR Message Handling

03F0(hex)	0830 (hex)	DATA WORD 0	030 (hex)
		DATA WORD 1	031 (hex)
		DATA WORD 2	032 (hex)
		DATA WORD 3	033 (hex)
03F0 (hex)	0434 (hex)	DATA WORD 0	034 (hex)
		DATA WORD 1	035 (hex)
03F0 (hex)	0036 (hex)	DATA WORD 0	036 (hex)
		DATA WORD 1	037 (hex)
		DATA WORD 2	038 (hex)
03F0 (hex)	0036 (hex)	DATA WORD 3	039 (hex)

Note:
The example is valid only if message structure is known in advance.

Figure 8. Memory Storage Subaddress 16

3.0 Pin Identification And Description



Note:
( ) Pingrid array pin numbers are in parentheses. Leadless chip carrier pin numbers are not in parentheses.

Figure 9. UT1553B RTR Pin Description

Legend for TYPE and ACTIVE fields:

TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TO = TTL output
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional
AL = Active low
AH = Active high
[] - Value in parentheses indicates initial state of pins.

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DATA(15)	43	B11	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
DATA(14)	42	C11	TTB	--	Bit 14 of the bidirectional Data bus.
DATA(13)	41	C10	TTB	--	Bit 13 of the bidirectional Data bus.
DATA(12)	40	D11	TTB	--	Bit 12 of the bidirectional Data bus.
DATA(11)	39	D10	TTB	--	Bit 11 of the bidirectional Data bus.
DATA(10)	38	E11	TTB	--	Bit 10 of the bidirectional Data bus.
DATA(9)	37	E10	TTB	--	Bit 9 of the bidirectional Data bus.
DATA(8)	36	F11	TTB	--	Bit 8 of the bidirectional Data bus.
DATA(7)	33	G10	TTB	--	Bit 7 of the bidirectional Data bus.
DATA(6)	32	H11	TTB	--	Bit 6 of the bidirectional Data bus.
DATA(5)	31	H10	TTB	--	Bit 5 of the bidirectional Data bus.
DATA(4)	30	J11	TTB	--	Bit 4 of the bidirectional Data bus.
DATA(3)	29	J10	TTB	--	Bit 3 of the bidirectional Data bus.
DATA(2)	28	K11	TTB	--	Bit 2 of the bidirectional Data bus.
DATA(1)	27	K10	TTB	--	Bit 1 of the bidirectional Data bus.
DATA(0)	26	L10	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR(9)	64	C1	TI	--	Bit 9 (MSB) of the Address bus.
ADDR(8)	65	D2	TI	--	Bit 8 of the Address bus.
ADDR(7)	66	D1	TI	--	Bit 7 of the Address bus.
ADDR(6)	67	E2	TI	--	Bit 6 of the Address bus.
ADDR(5)	2	F1	TI	--	Bit 5 of the Address bus.
ADDR(4)	3	G2	TI	--	Bit 4 of the Address bus.
ADDR(3)	4	G1	TI	--	Bit 3 of the Address bus.
ADDR(2)	5	H2	TI	--	Bit 2 of the Address bus.
ADDR(1)	6	H1	TI	--	Bit 1 of the Address bus.
ADDR(0)	7	J2	TI	--	Bit 0 (LSB) of the Address bus.

CONTROL INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{CS}$	10	K2	TI	AL	Chip Select. The host processor uses the $\overline{CS}$ signal for RTR Status Register reads, Control Register writes, or host access to the RTR internal RAM.
RD/$\overline{WR}$	9	K1	TI	--	Read/Write. The host processor uses a high level on this input in conjunction with $\overline{CS}$ to read the RTR Status Register or the RTR internal RAM. A low level on this input is used in conjunction with $\overline{CS}$ to write to the RTR Control Register or the RTR internal RAM.
$\overline{CTRL}$	8	J1	TI	AL	Control. The host processor uses the active low $\overline{CTRL}$ input signal in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ to access the RTR registers. A high level on this input means access is to RTR internal RAM only.
$\overline{OE}$	25	L9	TI	AL	Output Enable. The active low $\overline{OE}$ signal is used to control the direction of data flow from the RTR. For $\overline{OE}$ = 1, RTR Data bus is three-state; for $\overline{OE}$ = 0, the RTR Data bus is active.
ILLCOM	24	K9	TDI	AH	Illegal Command. The host processor uses the ILLCOM input to inform the RTR that the present command is illegal.

STATUS OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
MERR [0]	55	A5	TO	AH	Message Error. The active high MERR output signals that the Message Error bit in the Status Register has been set due to receipt of an illegal command, or an error during message sequence. MERR will reset to logic zero on the receipt of next valid command.
TXERR [0]	54	B5	TO	AH	Transmission Error. The active high TXERR output is asserted when the RTR detects an error in the reflected word versus the transmitted word, using the continuous loop-back compare feature. Reset on next $\overline{COMSTR}$ assertion.
$\overline{TIMERON}$ [1]	52	B6	TO	AL	Fail-safe Timer. The $\overline{TIMERON}$ output pulses low for 760 microseconds when the RTR begins transmitting (i.e. rising edge of VALMSG) to provide a fail-safe timer meeting the requirements of MIL-STD-1553B. This pulse is reset when $\overline{COMSTR}$ goes low or during a Master Reset.
$\overline{COMSTR}$ [1]	48	B8	TO	AL	Command Strobe. $\overline{COMSTR}$ is an active low output of 500 ns duration identifying receipt of a valid command.
$\overline{TERACT}$	53	A6	TO	AL	Terminal Active. The active low $\overline{TERACT}$ output is asserted at the beginning of the RTR access to internal RAM for a given command and negated after the last access for that command.

Continued on page 17.

STATUS OUTPUTS

Continued from page 16.

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{BRDCST}}$ [1]	51	A7	TO	AL	Broadcast. $\overline{\text{BRDCST}}$ is an active low output that identifies receipt of a valid broadcast command.
T/$\overline{\text{R}}$ [0]	56	B4	TO	--	Transmit/Receive. A high level on this pin indicates a transmit command message transfer is being or was processed, while a low level indicates a receive command message transfer is being or was processed.
RTRT [0]	50	B7	TO	AH	Remote Terminal to Remote Terminal. RTRT is an active high output indicating that the RTR is processing a remote terminal to remote terminal command.
VALMSG [0]	23	L8	TO	AH	Valid Message. VALMSG is an active high output indicating a valid message (including Broadcast) has been received. VALMSG goes high prior to transmitting the 1553 status word and is reset upon receipt of the next command.
RBUSY [0]	63	C2	TO	AH	RTR Busy. RBUSY is asserted high while the RTR is accessing its own internal RAM either to read or update the pointers or to store or retrieve data words. RBUSY becomes active either 2.7 µs or 5.7 µs before RTR requires RAM access. This timing is controlled by Control Register bit 12; see section 1.3.

MODE CODE/SUBADDRESS OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{MC}}$/SA [0]	62	B1	TO	--	Mode Code/Subaddress Indicator. If $\overline{\text{MC}}$/SA is low, it indicates that the most recent command word is a mode code command. If $\overline{\text{MC}}$/SA is high, it indicates that the most recent command word is for a subaddress. This output indicates whether the mode code/subaddress outputs (i.e. MCSA(4:0)) contain mode code or subaddress information.
MCSA0 [0]	61	B2	TO	--	Mode Code/Subaddress Output 0. If $\overline{\text{MC}}$/SA is low, this pin represents the least significant bit of the most recent command word (the LSB of the mode code). If $\overline{\text{MC}}$/SA is high, this pin represents the LSB of the subaddress.
MCSA1 [0]	60	A2	TO	--	Mode Code/Subaddress Output 1.
MCSA2 [0]	59	A3	TO	--	Mode Code/Subaddress Output 2.
MCSA3 [0]	58	B3	TO	--	Mode Code/Subaddress Output 3.
MCSA4 [0]	57	A4	TO	--	Mode Code/Subaddress Output 4. If $\overline{\text{MC}}$/SA is low, this pin represents the most significant bit of the mode code. If $\overline{\text{MC}}$/SA is high, this pin represents the MSB of the subaddress.

REMOTE TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RTA4	13	L3	TUI	--	Remote Terminal Address bit 4 (MSB).
RTA3	14	K4	TUI	--	Remote Terminal Address bit 3.
RTA2	15	L4	TUI	--	Remote Terminal Address bit 2.
RTA1	16	K5	TUI	--	Remote Terminal Address bit 1.
RTA0	17	L5	TUI	--	Remote Terminal Address bit 0 (LSB).
RTPTY	18	K6	TUI	--	Remote Terminal Address Parity. This input must provide odd parity for the Remote Terminal Address.

BIPHASE INPUTS (1)

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RAZ	21	L7	TI	--	Receiver - Channel A, Zero Input. Idle low Manchester input from the 1553 bus receiver.
RAO	22	K8	TI	--	Receiver - Channel A, One Input. This input is the complement of RAZ.
RBZ	19	L6	TI	--	Receiver - Channel B, Zero Input. Idle low Manchester input from the 1553 bus receiver.
RBO	20	K7	TI	--	Receiver - Channel B, One Input. This input is the complement of RBZ.

Note:
1. For uniphase operation, tie RAZ (or RBZ) to V_{DD} and apply true uniphase input signal to RAO (or RBO).

BIPHASE OUTPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
TAZ [0]	45	A10	TO	--	Transmitter - Channel A, Zero Output. This idle low Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TAO [0]	44	B10	TO	--	Transmitter - Channel A, One Output. This output is the complement of TAZ. The output is idle low.
TBZ [0]	47	A9	TO	--	Transmitter - Channel B, Zero Output. This idle low Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TBO [0]	46	B9	TO	--	Transmitter - Channel B, One Output. This output is the complement of TBZ. The output is idle low.

MASTER RESET AND CLOCK

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{MRST}$	12	K3	TUI	AL	Master Reset. Initializes all internal functions of the RTR. $\overline{MRST}$ must be asserted 500 ns before normal RTR operation. (500 ns minimum) Does not reset RAM.
12MHz	11	L2	TI	--	12 MHz Input Clock. This is the RTR system clock that requires an accuracy greater than 0.01% with a duty cycle of 50% +/-10%.
2MHz	49	A8	TO	--	2 MHz Clock Output. This is a 2 MHz clock output generated by the 12 MHz input clock. This clock is stopped when $\overline{MRST}$ is low.

POWER AND GROUND

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
VDD	35	F10	PWR	--	+5 VDC Power. Power supply must be +5 VDC +/-10%.
	68	E1	PWR	--	
VSS	1	F2	GND	--	Reference ground. Zero VDC logic ground.
	34	G11	GND	--	

4.0 Operating Conditions

ABSOLUTE MAXIMUM RATINGS*
(referenced to VSS)

SYMBOL	PARAMETER	LIMITS	UNIT
VDD	DC supply voltage	-0.3 to +7.0	V
VIO	Voltage on any pin	-0.3 to VDD+0.3	V
II	DC input current	+/-10	mA
TSTG	Storage temperature	-65 to +150	°C
PD	Maximum power dissipation (1)	300	mW
TJ	Maximum junction temperature	+175	°C
ΘJC	Thermal resistance, junction-to-case	20	°C/W

Note:
1. Does not reflect the added P_D due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
VDD	DC supply voltage	4.5 to 5.5	V
VIN	DC input voltage	0 to VDD	V
TC	Temperature range	-55 to +125	°C
FO	Operating frequency	12 +/- .01%	MHz

5.0 DC Electrical Characteristics

(V_{DD} = 5.0 V +/-10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	 V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	 -1 110 -2000	 1 2000 -110	 µA µA µA
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -400 µA	2.4		V
I_{OZ}	Three-state output leakage current	V_O = V_{DD} or V_{SS}	-10	+10	µA
I_{OS}	Short-circuit output current (1,2)	V_{DD} = 5.5 V, V_O = V_{DD} V_{DD} = 5.5 V, V_O = 0 V	 -90	90	mA mA
C_{IN}	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		20	pF
I_{DD}	Average operating current (1,4)	F = 12 MHz, CL = 50 pF		50	mA
QI_{DD}	Quiescent current	Note 5		1.5	mA

Notes:
1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
4. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
5. All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

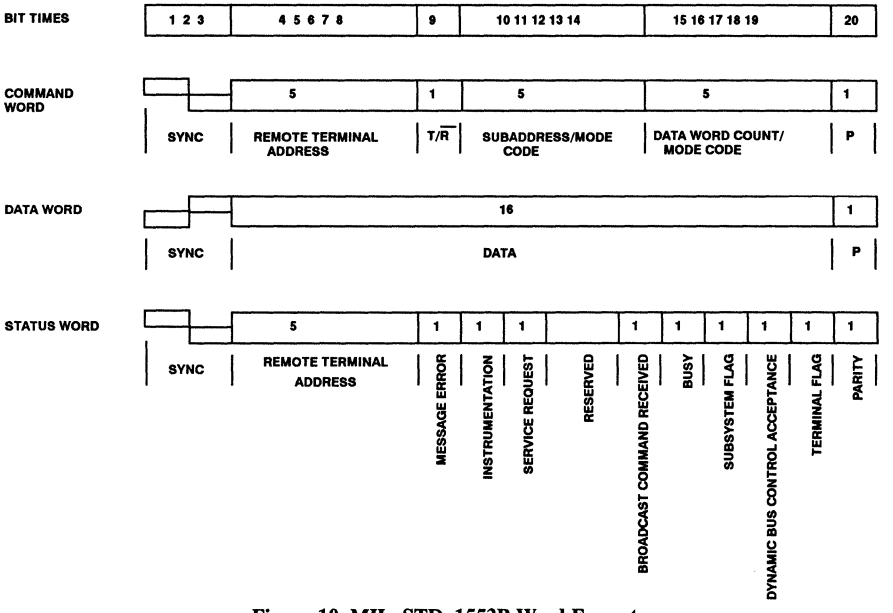
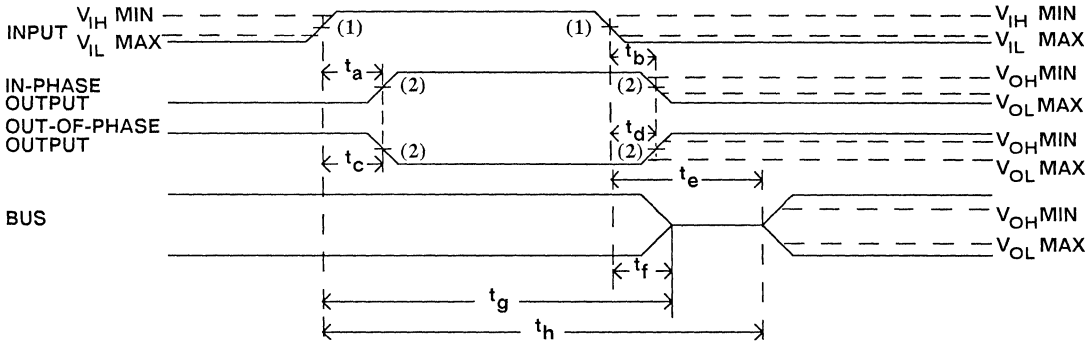


Figure 10. MIL-STD-1553B Word Formats

6.0 AC Electrical Characteristics

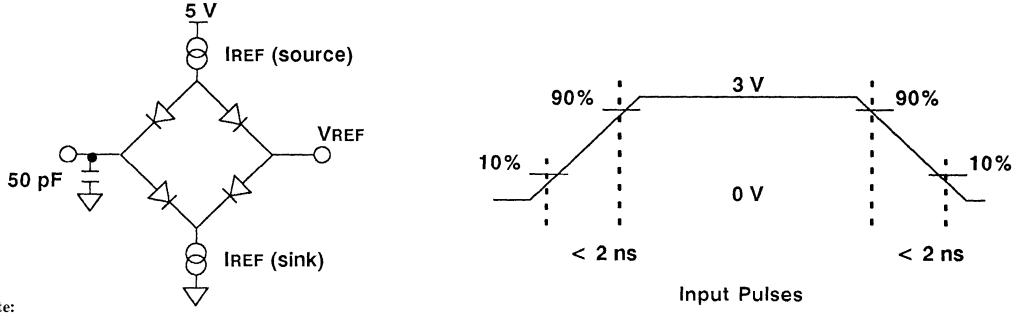
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 11a. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

Figure 11b. AC Test Loads and Input Waveforms

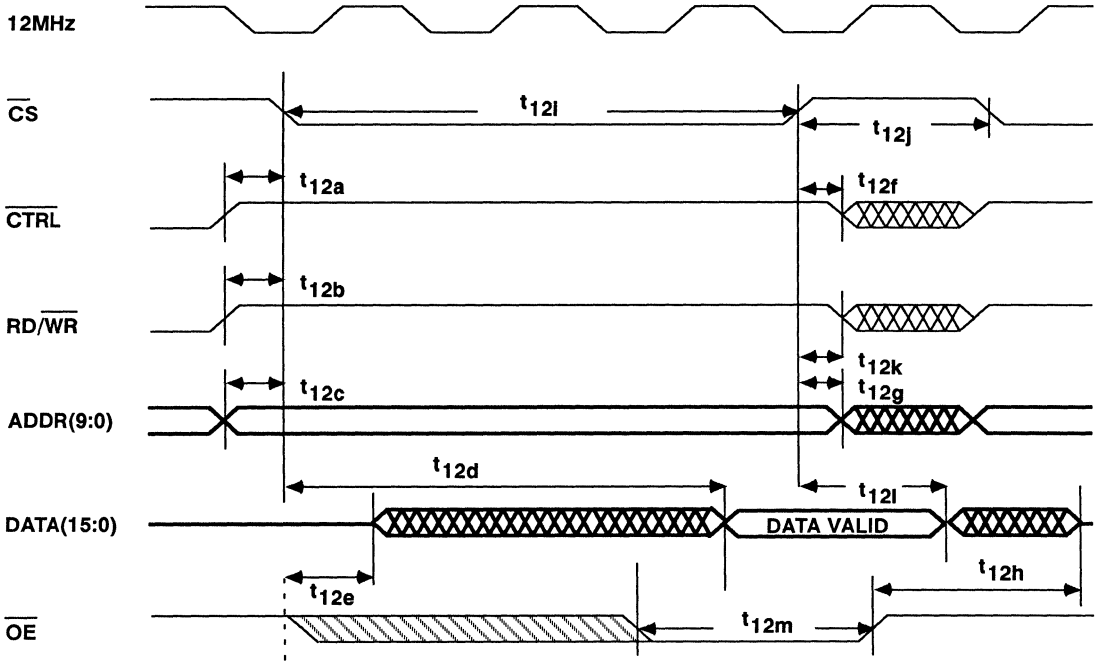


Figure 12. Microprocessor RAM Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t12a	$\overline{CTRL}$ ↑ set up wrt $\overline{CS}$ ↓ (1)	10	--	ns
t12b	RD/$\overline{WR}$ ↑ set up wrt $\overline{CS}$ ↓	10	--	ns
t12c	ADDR(9:0) Valid to $\overline{CS}$ ↓ (Address Set up)	10	--	ns
t12d	$\overline{CS}$ ↓ to DATA(15:0) Valid	--	155	ns
t12e	$\overline{OE}$ ↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t12f	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	0	--	ns
t12g	$\overline{CS}$ ↑ to ADDR(9:0) Don't Care	0	--	ns
t12h	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	--	40	ns
t12i	$\overline{CS}$ ↓ to $\overline{CS}$ ↑ (2)	220	5500	ns
t12j	$\overline{CS}$ ↑ to $\overline{CS}$ ↓	85	--	ns
t12k	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t12l	$\overline{CS}$ ↑ to DATA(15:0) Invalid (3)	25	--	ns
t12m	$\overline{OE}$ ↓ to $\overline{OE}$ ↑	65	--	ns

Notes:
1. "wrt" defined as "with respect to."
2. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.
3. Assumes $\overline{OE}$ is asserted.

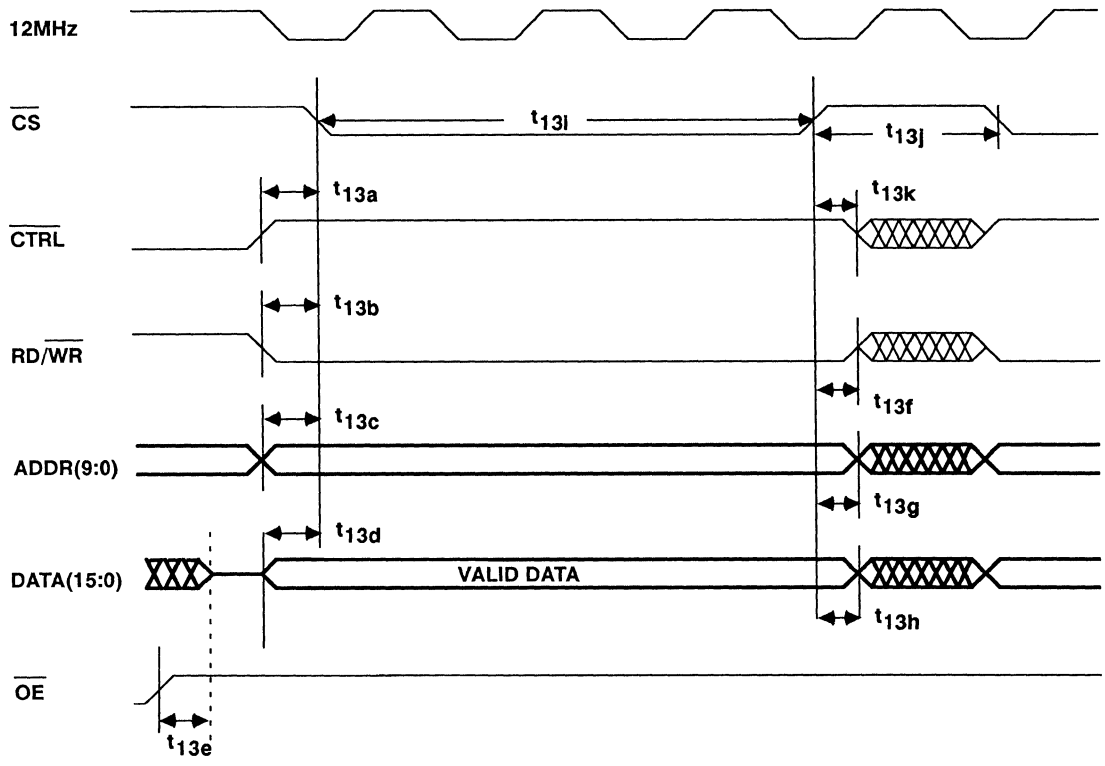


Figure 13. Microprocessor RAM Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t13a	$\overline{CTRL}$ ↑ set up wrt $\overline{CS}$ ↓	10	--	ns
t13b	RD/$\overline{WR}$ ↓ set up wrt $\overline{CS}$ ↓	10	--	ns
t13c	ADDR(9:0) Valid to $\overline{CS}$ ↓ (Address set up)	10	--	ns
t13d	DATA(15:0) Valid to $\overline{CS}$ ↓ (DATA set up)	0	--	ns
t13e	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	40	--	ns
t13f	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t13g	$\overline{CS}$ ↑ to ADDR(9:0) Don't Care	0	--	ns
t13h	$\overline{CS}$ ↑ to DATA(15:0) Don't Care (Hold-time)	20	--	ns
t13i	$\overline{CS}$ ↓ to $\overline{CS}$ ↑(1)	180	5500	ns
t13j	$\overline{CS}$ ↑ to $\overline{CS}$ ↓	85	--	ns
t13k	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	0	--	ns

Note:

1. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

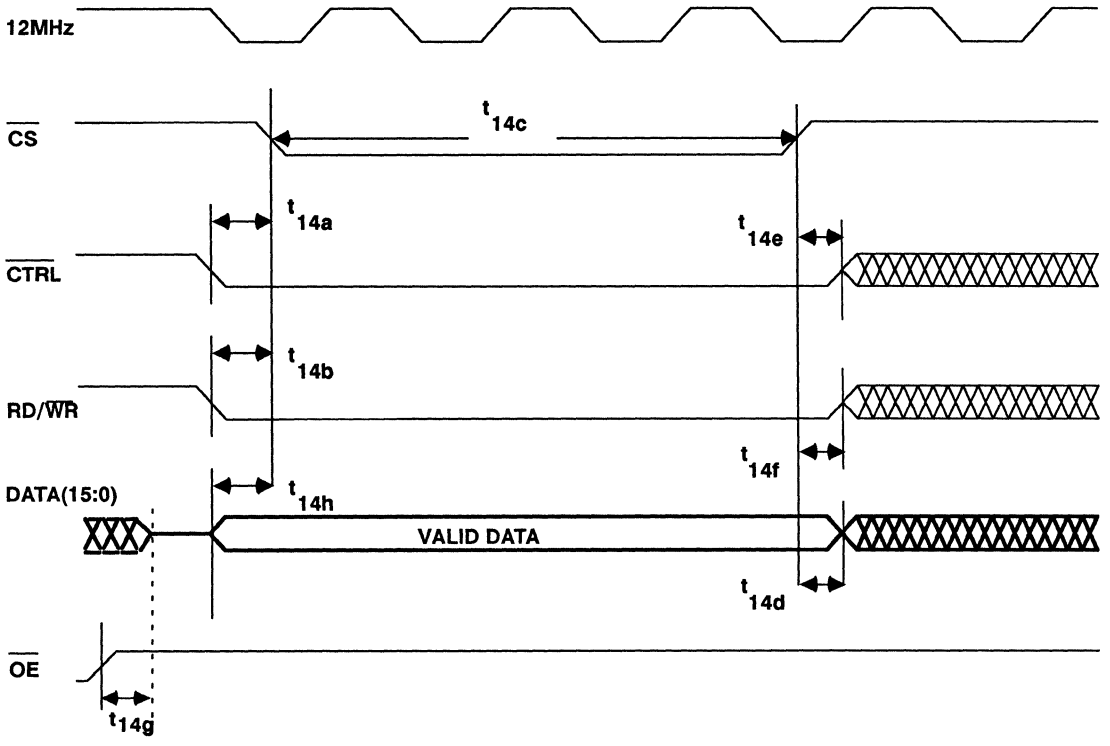


Figure 14. Control Register Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t14a	$\overline{CTRL}$ ↓ set up wrt $\overline{CS}$ ↓	0	--	ns
t14b	RD/$\overline{WR}$ ↓ set up wrt $\overline{CS}$ ↓	0	--	ns
t14c	$\overline{CS}$ ↓ to $\overline{CS}$ ↑(1)	50	5500	ns
t14d	$\overline{CS}$ ↑ to DATA(15:0) Don't Care (Hold-time)	0	--	ns
t14e	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	0	--	ns
t14f	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t14g	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	40	--	ns
t14h	DATA(15:0) Valid to $\overline{CS}$ ↓ (DATA set up)	0	--	ns

Note:

1. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

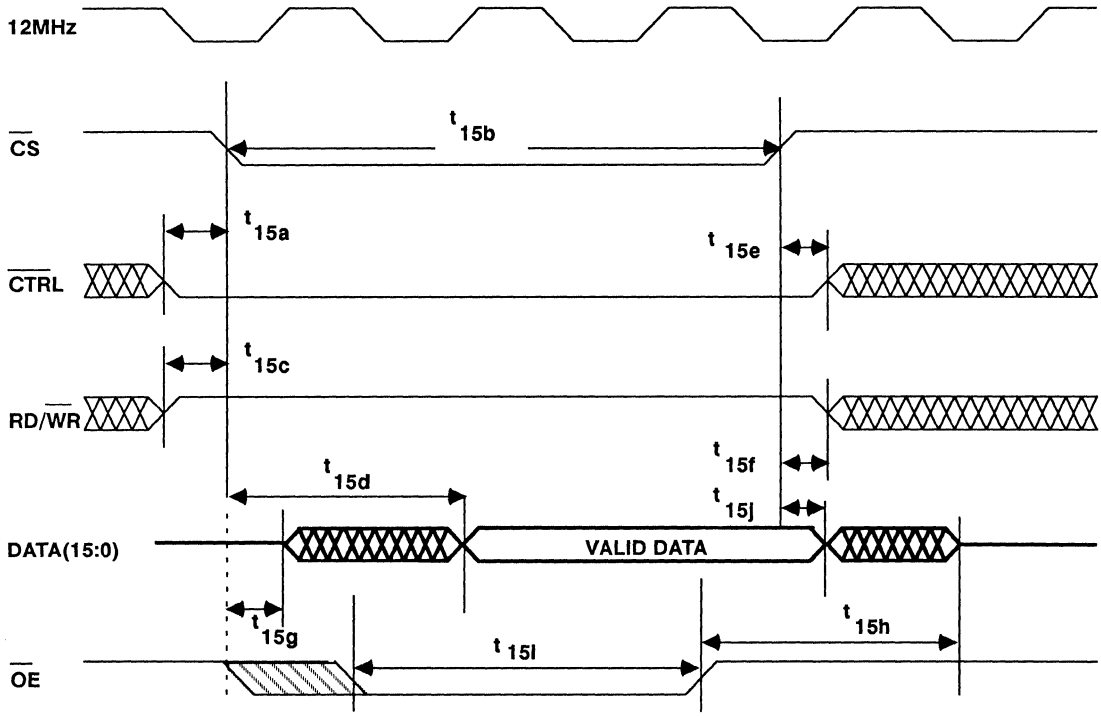


Figure 15. Status Register Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t15a	$\overline{CTRL}$ ↓ set up wrt $\overline{CS}$ ↓	0	--	ns
t15b	$\overline{CS}$ ↓ to $\overline{CS}$ ↑(1)	65	5500	ns
t15c	RD/$\overline{WR}$ ↑ set up wrt $\overline{CS}$ ↓	0	--	ns
t15d	$\overline{CS}$ ↓ to DATA(15:0) Valid	--	65	ns
t15e	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	5	--	ns
t15f	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	5	--	ns
t15g	$\overline{OE}$ ↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t15h	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	--	40	ns
t15i	$\overline{OE}$ ↓ to $\overline{OE}$ ↑	65	--	ns
t15j	$\overline{CS}$ ↓ to DATA(15:0) Don't Care (Active)	25	--	ns

Note:

1. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

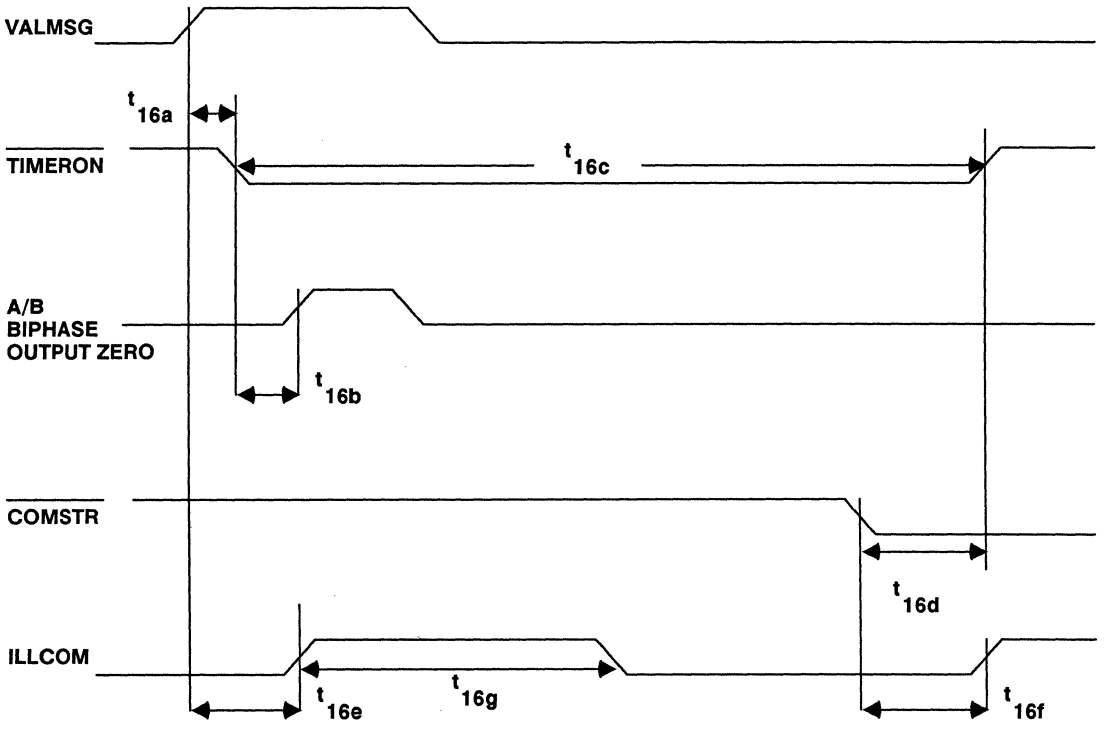
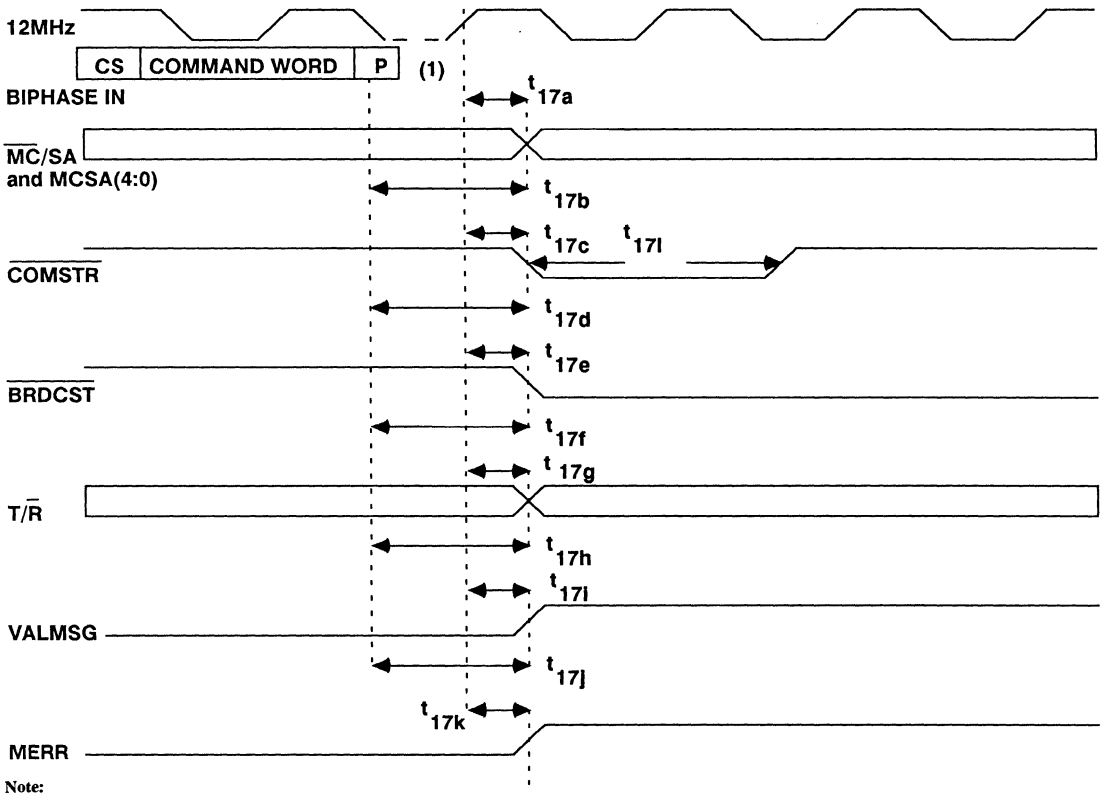


Figure 16. RT Fail-Safe Timer Signal Relationships

SYMBOL	PARAMETER	MIN	MAX	UNITS
t16a	VALMSG ↑ before $\overline{\text{TIMERON}}$ ↓	0	35	ns
t16b	$\overline{\text{TIMERON}}$ ↓ before first BIPHASE OUT O ↑	1.2	--	µs
t16c	$\overline{\text{TIMERON}}$ low pulse width (time-out)	727.3	727.4	µs
t16d	$\overline{\text{COMSTR}}$ ↓ to $\overline{\text{TIMERON}}$ ↑	--	25	ns
t16e	VALMSG ↑ to ILLCOM ↑	--	3.3	µs
t16f	$\overline{\text{COMSTR}}$ ↓ to ILLCOM ↑ (1)	--	664	ns
t16f	$\overline{\text{COMSTR}}$ ↓ to ILLCOM ↑ (2)	--	18.2	µs
t16g	ILLCOM ↑ to ILLCOM ↓ (3)	500	--	ns

Notes:
1. Mode code 2, 4, 5, 6, 7, or 18 received.
2. To suppress data word storage.
3. For transmit command illegalization.

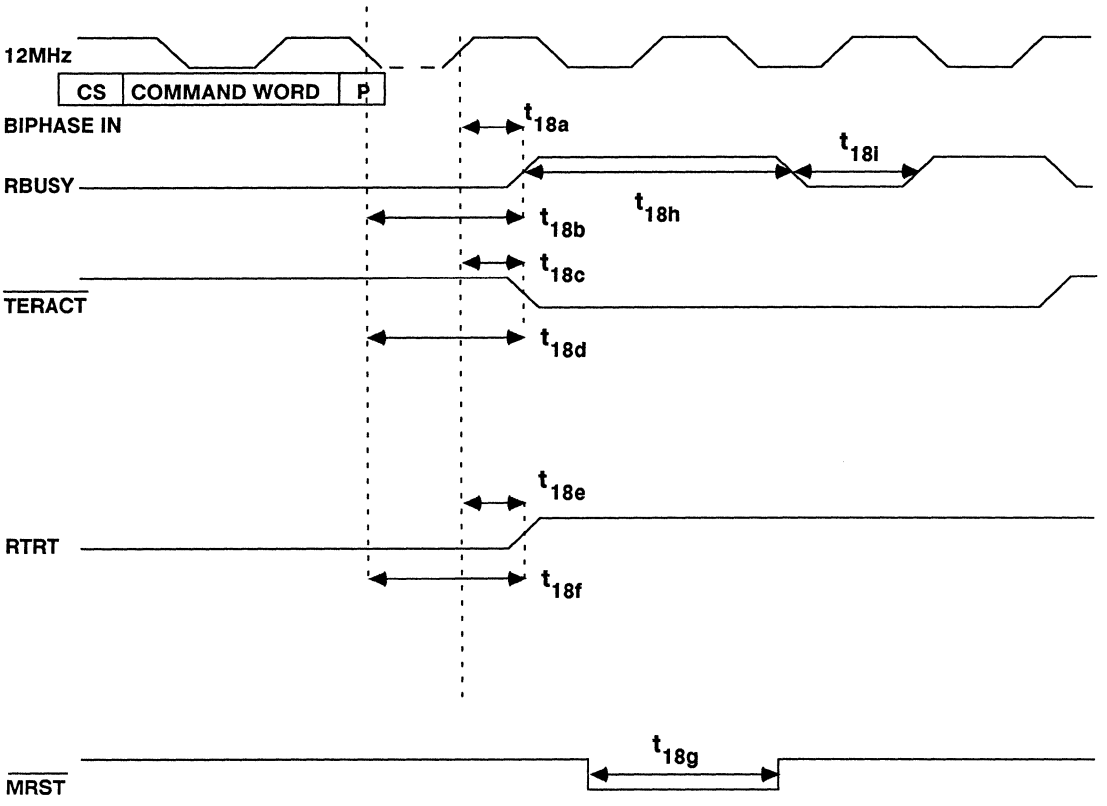


Note:
1. Measured from the mid-bit parity crossing.

Figure 17. Status Output Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t17a (4)	12MHz ↑ to $\overline{MC}$/SA Valid	0	14	ns
t17b	Command Word to $\overline{MC}$/SA Valid (3)	2.1	2.8	µs
t17c (4)	12MHz ↑ to $\overline{COMSTR}$ ↓	0	17	ns
t17d	Command Word to $\overline{COMSTR}$ ↓ (3)	3.2	3.7	µs
t17e (4)	12MHz ↑ to $\overline{BRDCST}$ ↓	0	32	ns
t17f	Command Word to $\overline{BRDCST}$ ↓ (3)	2.6	3.2	µs
t17g (4)	12MHz ↑ to T/$\overline{R}$ Valid	0	57	ns
t17h	Command Word to T/$\overline{R}$ Valid (3)	2.2	2.7	µs
t17i (4)	12MHz ↑ to VALMSG ↑	0	32	ns
t17j	Command Word to VALMSG ↑ (1,2,3)	6.2	6.7	µs
t17k (4)	12MHz ↑ to MERR ↑	0	37	ns
t17l	$\overline{COMSTR}$ ↓ to $\overline{COMSTR}$ ↑	485	500	ns

Notes:
1. Receive last data word to Valid Message active (VALMSG↑).
2. Transmit command word to Valid Message active (VALMSG ↑).
3. Command word measured from mid-bit crossing.
4. Guaranteed by test.

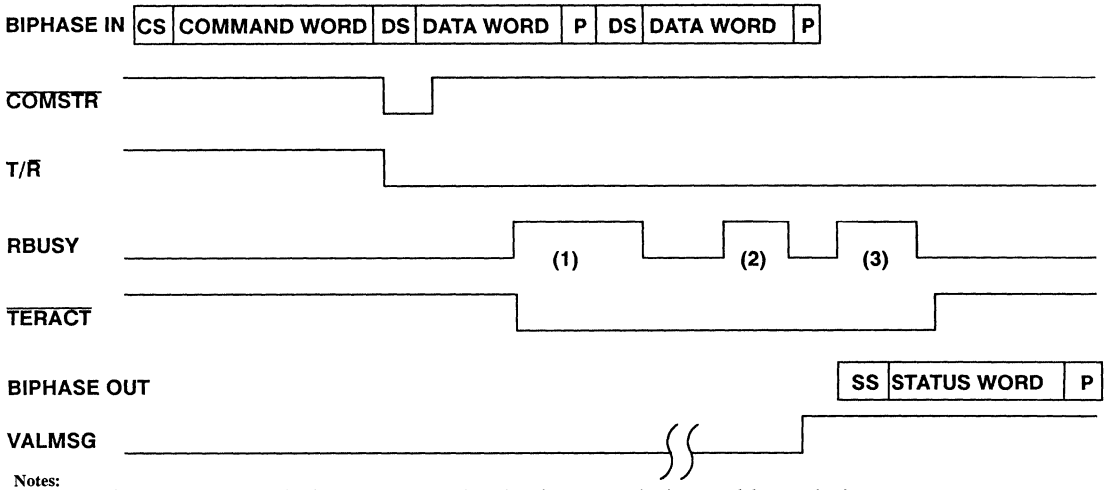


Note:
1. Measured from mid-bit parity crossing.

Figure 18. Status Output Timing

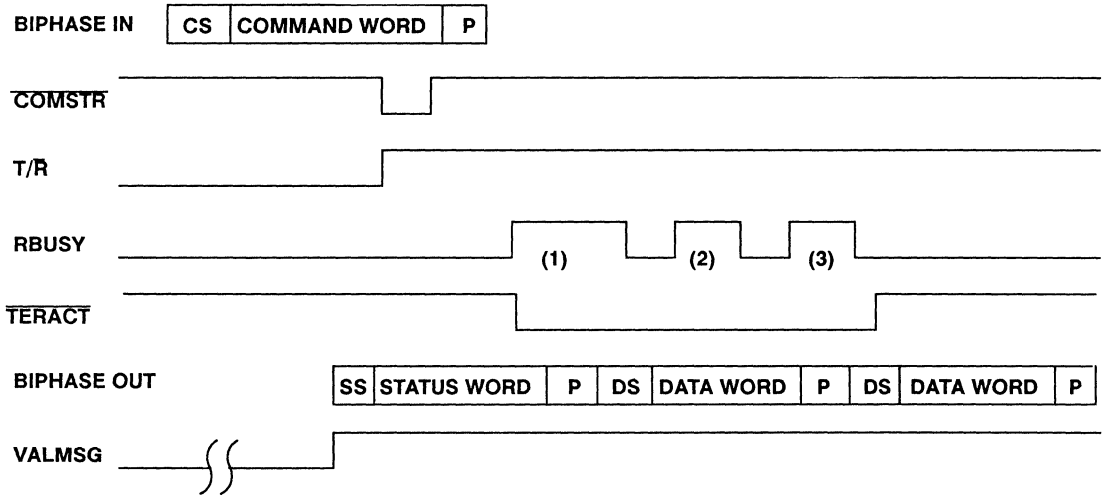
SYMBOL	PARAMETER	MIN	MAX	UNITS
t18a	12MHz ↑ to RBUSY ↑	--	37	ns
t18b	Command Word to RBUSY ↑ (2)	3.2	3.8	µs
t18c (1)	12MHz ↑ to $\overline{\text{TERACT}}$ ↓	0	37	ns
t18d	Command Word to $\overline{\text{TERACT}}$ ↓ (2)	3.1	3.7	µs
t18e (1)	12MHz ↑ to RTRT ↑	0	32	ns
t18f	Command Word to RTRT ↑ (2)	21.0	22.0	µs
t18g	$\overline{\text{MRST}}$ ↓ to $\overline{\text{MRST}}$ ↑	500	--	ns
t18h	RBUSY ↑ to RBUSY ↓ (2.7 µs) (5.7 µs)	-- --	5.5 8.5	µs µs
t18i	RBUSY ↓ to RBUSY ↑ (2.7 µs) (5.7 µs)	3.10 240	-- --	µs ns

Notes:
1. Guaranteed by test.
2. Command word measured from mid-bit crossing.



Notes:
1. Burst of 5 DMAs: read command pointer, store command word, update command pointer, read data word pointer, store command word.
2. Burst of 1 DMA: store data word.
3. Burst of 2 DMAs: store data word, update data word pointer.
4. Approximately 560 ns per DMA access.

Figure 19a. Receive Command with Two Data Words



CS = Command sync
SS = Status sync
DS = Data sync
P = Parity

Notes:
1. Burst of 4 DMAs: read command pointer, store command word, update command pointer, read data word pointer.
2. Burst of 1 DMA: read data word.
3. Burst of 2 DMAs: read data word, update data word pointer.
4. Approximately 560 ns per DMA access.

Figure 19b. Transmit Command with Two Data Words

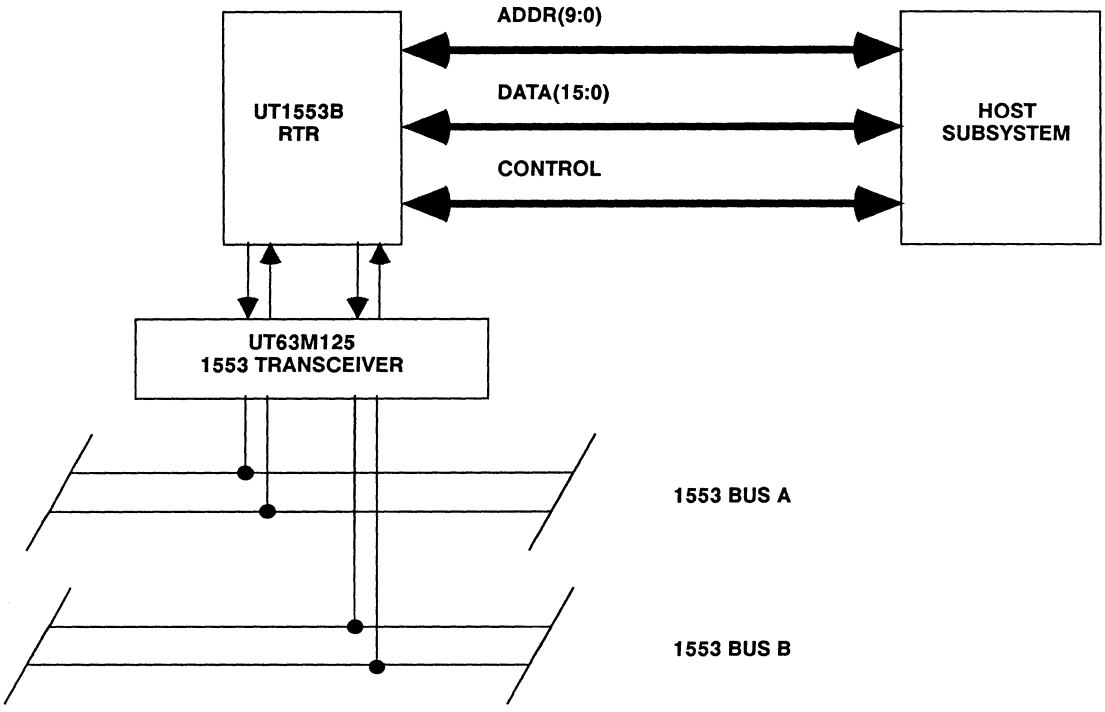


Figure 20a. RTR General System Diagram (Idle low interface)

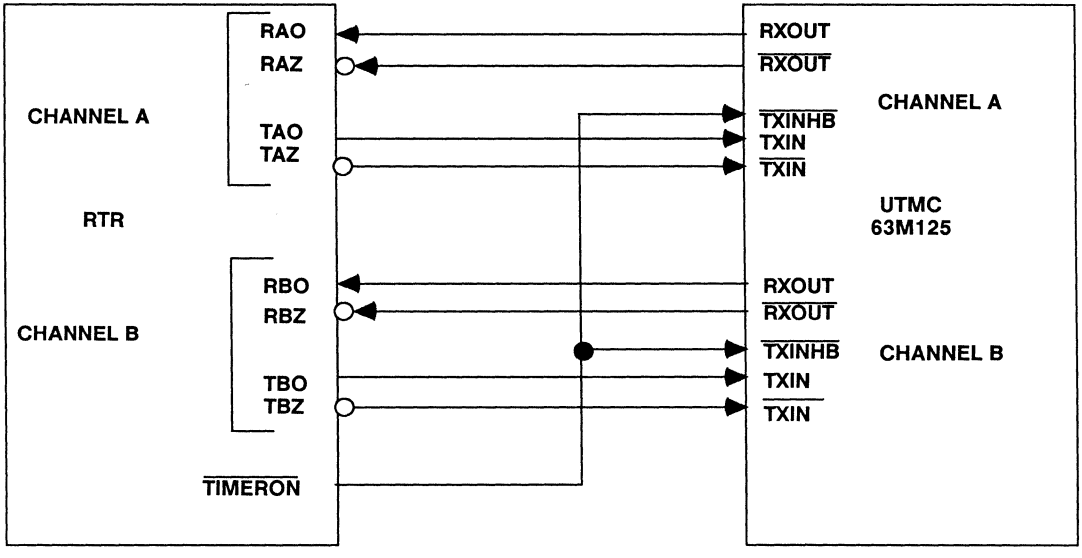


Figure 20b. RTR Transceiver Interface Diagram

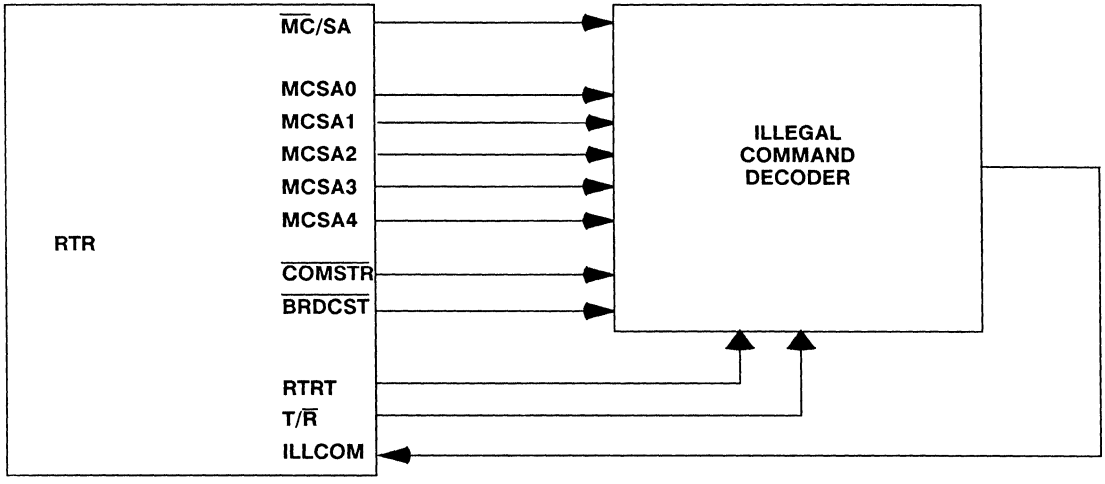
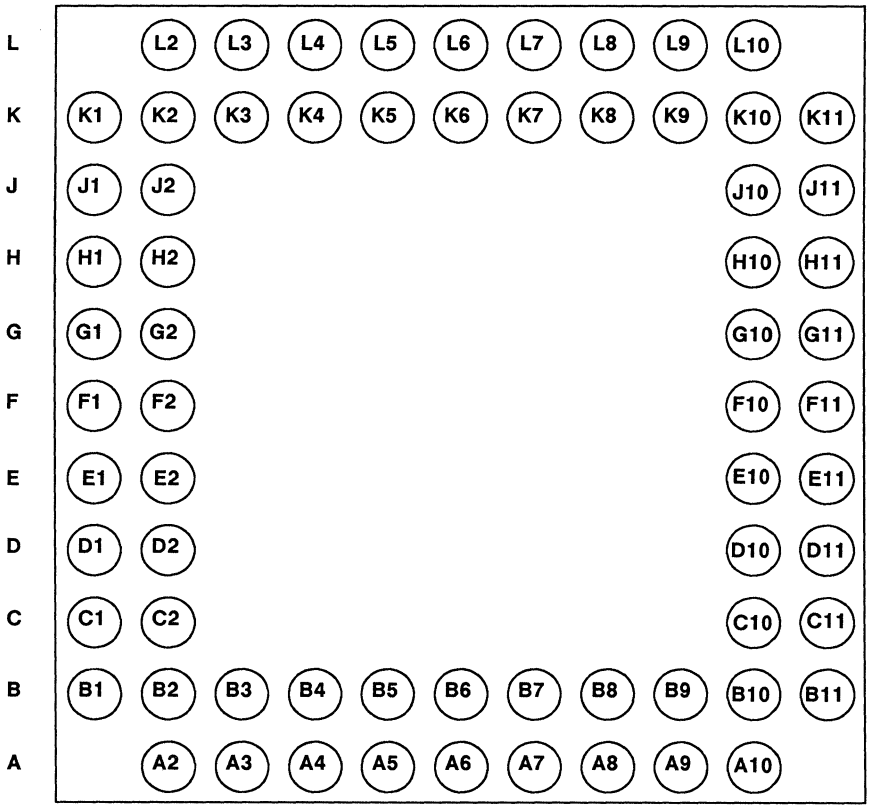


Figure 21. Mode Code/Subaddress Illegalization Circuit

7.0 Package Outline Drawing



A2 MCSA1
A3 MCSA2
A4 MCSA4
A5 MERR
A6 TERACT
A7 BRDCST
A8 2MHz
A9 TBZ
A10 TAZ

B1 MC/SA
B2 MCSA0
B3 MCSA3
B4 T/R
B5 TXERR
B6 TIMERON
B7 RTRT
B8 COMSTR
B9 TBO
B10 TAO
B11 DATA15

C1 ADDR9
C2 RBUSY
C10 DATA13
C11 DATA14

D1 ADDR7
D2 ADDR8
D10 DATA11
D11 DATA12

E1 VDD
E2 ADDR6
E10 DATA9
E11 DATA10

F1 ADDR5
F2 VSS
F10 VDD
F11 DATA8

G1 ADDR3
G2 ADDR4
G10 DATA7
G11 VSS

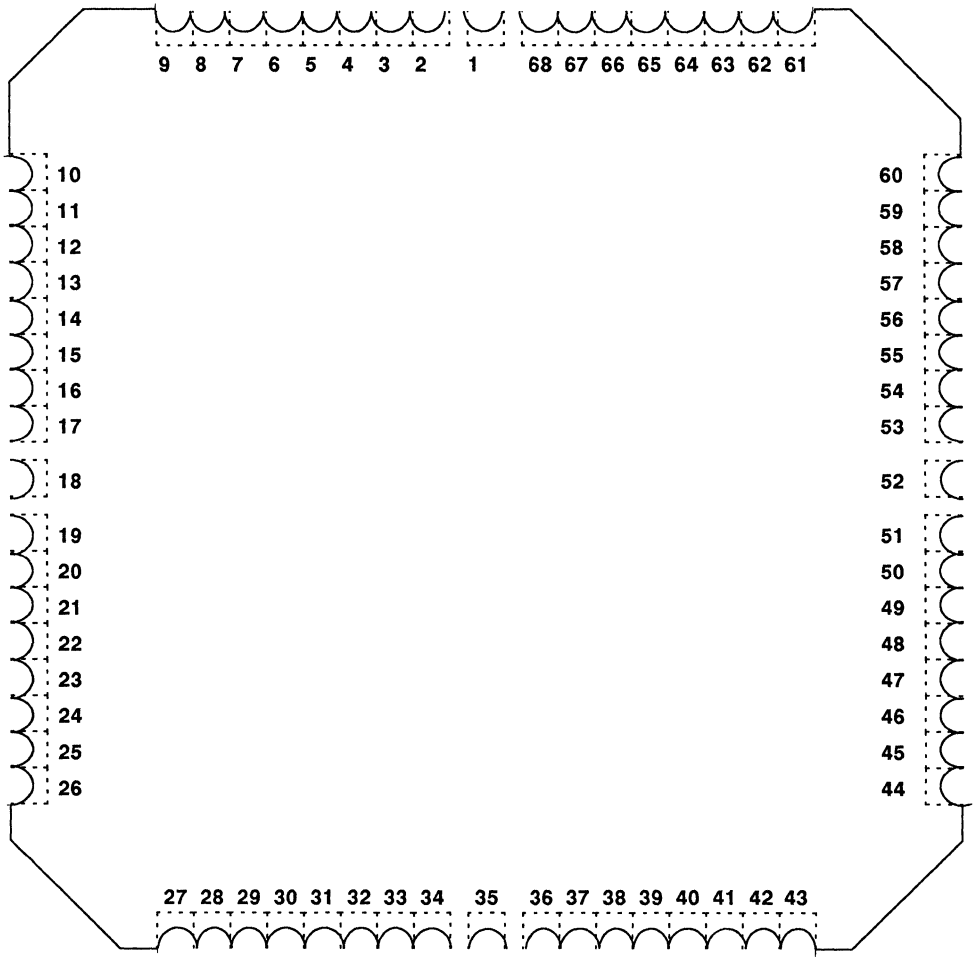
H1 ADDR1
H2 ADDR2
H10 DATA5
H11 DATA6

J1 CTRL
J2 ADDR0
J10 DATA3
J11 DATA4

K1 RD/WR
K2 CS
K3 MRST
K4 RTA3
K5 RTA1
K6 RTPTY
K7 RBO
K8 RAO
K9 ILLCOM
K10 DATA1
K11 DATA2

L2 12MHz
L3 RTA4
L4 RTA2
L5 RTA0
L6 RBZ
L7 RAZ
L8 VALMSG
L9 OE
L10 DATA0

Figure 22a. UT1553B RTR Pingrid Array Configuration (Bottom View)



1	Vss	15	RTA2	29	DATA3	43	DATA15	56	T/$\overline{R}$
2	ADDR5	16	RTA1	30	DATA4	44	TAO	57	MCSA4
3	ADDR4	17	RTA0	31	DATA5	45	TAZ	58	MCSA3
4	ADDR3	18	RTPTY	32	DATA6	46	TBO	59	MCSA2
5	ADDR2	19	RBZ	33	DATA7	47	$\overline{TBZ}$	60	MCSA1
6	ADDR1	20	RBO	34	Vss	48	$\overline{COMSTR}$	61	MCSA0
7	ADDR0	21	RAZ	35	VDD	49	2MHz	62	$\overline{MC}$/SA
8	$\overline{CTRL}$	22	RAO	36	DATA8	50	RTRT	63	RBUSY
9	RD/$\overline{WR}$	23	VALMSG	37	DATA9	51	$\overline{BRDCST}$	64	ADDR9
10	$\overline{CS}$	24	ILLCOM	38	DATA10	52	$\overline{TIMERON}$	65	ADDR8
11	12MHz	25	$\overline{OE}$	39	DATA11	53	$\overline{TERACT}$	66	ADDR7
12	$\overline{MRST}$	26	DATA0	40	DATA12	54	TXERR	67	ADDR6
13	RTA4	27	DATA1	41	DATA13	55	MERR	68	VDD
14	RTA3	28	DATA2	42	DATA14				

Figure 22b. UT1553B RTR Chip Carrier Configuration (Top View)

UT1760A RTS Remote Terminal for Stores

Features

- ☐ Complete MIL-STD-1760A Notice I through III remote terminal interface
- ☐ 1K x 16 of on-chip static RAM for message data, completely accessible to host
- ☐ Self-test capability, including continuous loop-back compare
- ☐ Programmable memory mapping via pointers for efficient use of internal memory, including buffering multiple messages per subaddress
- ☐ RT-RT Terminal Address Compare
- ☐ Command word stored with incoming data for enhanced data management
- ☐ User selectable RAM Busy (RBUSY) signal for slow or fast processor interfacing
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B, also Standard Military Drawing available
- ☐ Available in 68-pin pingrid array, and 68-lead leadless chip carrier packages

Introduction

The UT1760A RTS is a monolithic CMOS VLSI solution to the requirements of the dual-redundant MIL-STD-1553B interface as specified by MIL-STD-1760A. Designed to reduce cost and space in the mission stores interface, the RTS integrates the remote terminal logic with a user-configured 1K x 16 static RAM. In addition, the RTS has a flexible subsystem interface to permit use with most processors or controllers.

The RTS provides all protocol, data handling, error checking, and memory control functions, as well as comprehensive self-test capabilities. The RTS's memory meets all of a mission store's message storage needs through user-defined memory mapping. This memory-mapped architecture allows multiple message buffering at each subaddress.

3

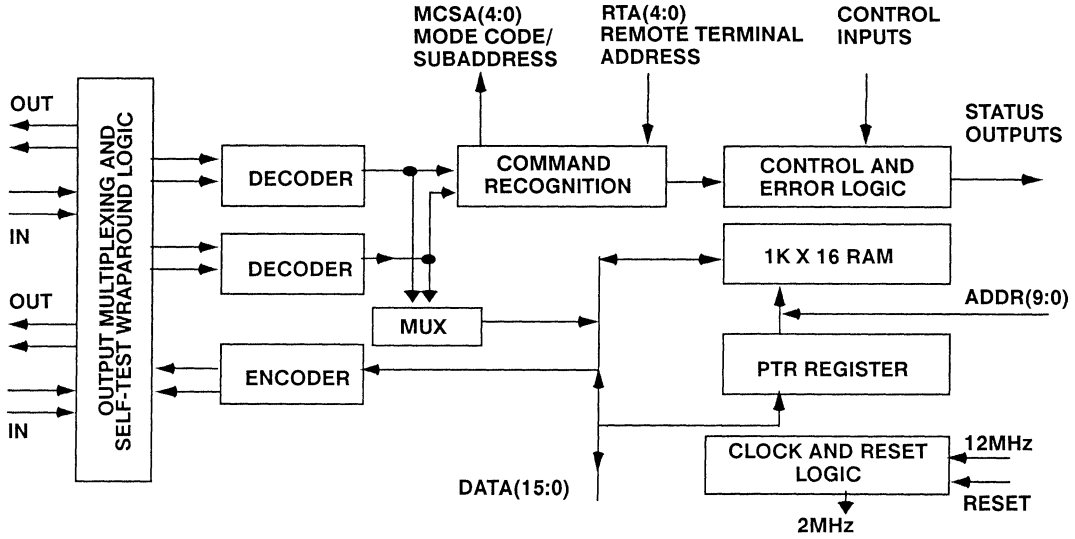


Figure 1. UT1760A RTS Functional Block Diagram

Table of Contents

1.0 Architecture And Operation

The UT1760A RTS is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system. The RTS's MIL-STD-1553B interface includes encoding/decoding logic, error detection, command recognition, 1K x 16 of SRAM, pointer registers, clock, and reset circuits. Illegal subaddress circuitry makes the RTS MIL-STD-1760A-specific.

1.1 Memory Map and Host Memory Interface

The host can access the 1K x 16 RAM memory like a standard RAM device through the 10-bit address and 16-bit data buses. The host uses the Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) signals to control data transfer to and from memory. When the RTS requires access to its own internal RAM, it asserts the RBUSY signal to alert the host. The RBUSY signal is programmable via the internal Control Register to be asserted either 5.7 µs or 2.7 µs prior to the RTS needing access to its internal RAM.

The RTS stores MIL-STD-1760A messages in 1K x 16 of on-chip RAM. For efficient use of the 1K x 16 memory on the RTS, the host programs a set of pointers to map where the 1760A message is stored. The RTS uses the upper 64 words (address 3C0 (hex) through 3FF (hex)) as pointers. The RTS provides pointers for all 30 receive subaddresses, all 30 transmit subaddresses, and four mode code commands with associated data words as defined in MIL-STD-1553B. The remaining 960 words of memory contain receive, transmit, and mode code data in a host-defined structure.

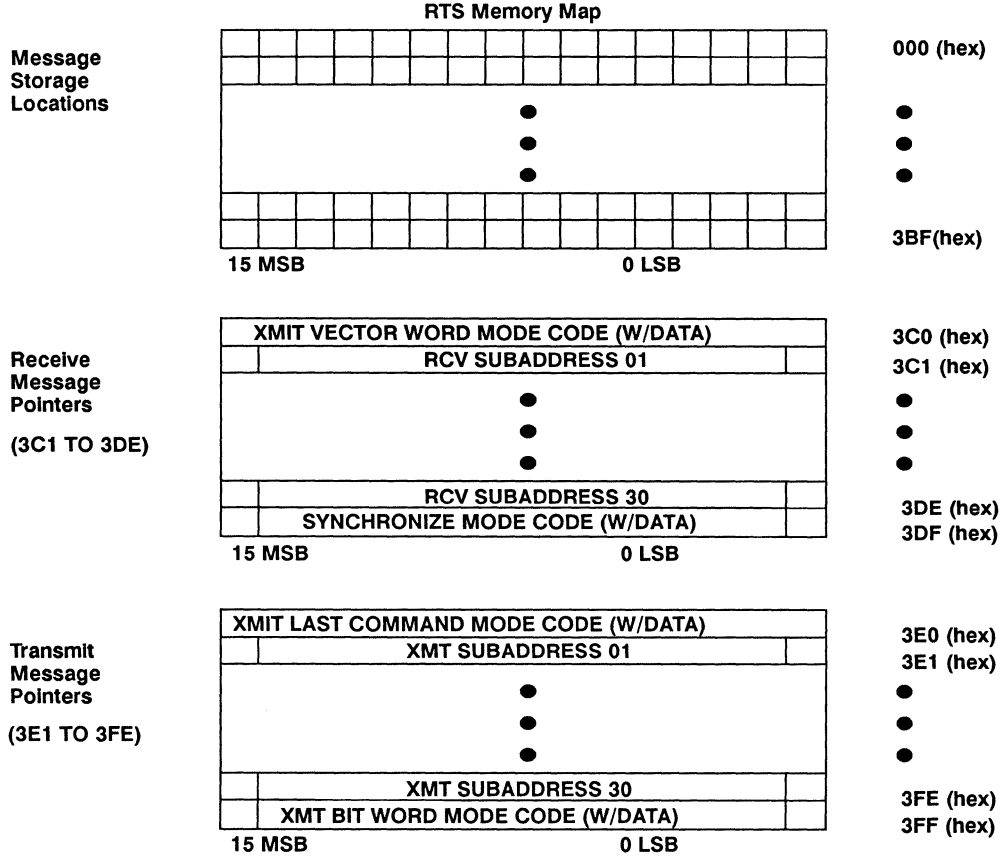


Figure 2. RTS Memory Map

1.2 RTS RAM Pointer Structure

The RAM 16-bit pointers have a 6-bit index field and a 10-bit address field. The 6-bit index field allows for the storage of up to 64 messages per subaddress. A message consists of the 1553 command word and its associated data words.

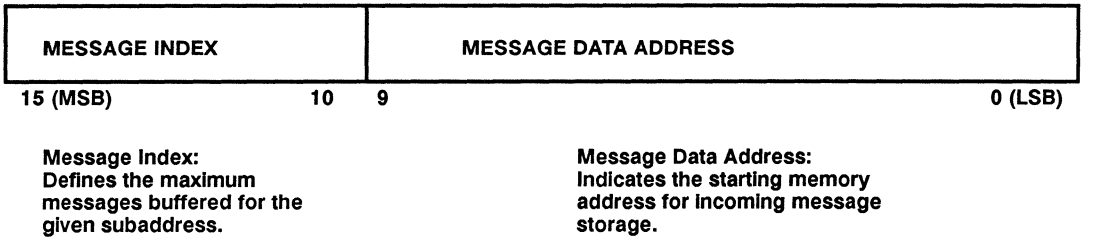


Figure 3. Message Pointer Structure

The 16-bit pointer for Transmit Last Command Mode Code is located at memory location 3E0 (hex). The Transmit Last Command Mode Code pointer buffers up to 63 command words. An example of command word storage follows:

Example:

3E0 (hex) Contents = FC00 (hex)

11 1111 00 0000 0000

Address Field = 000 (hex)
Index Field = 3F (hex)

First command word storage location (3E0 = F801):

Address Field = 001 (hex)
Index Field = 3E (hex)

Sixty-third command word storage location (3E0 = 003F):

Address Field = 03F (hex)
Index Field = 00 (hex)

Sixty-fourth command word storage location (3E0 = 003F) (previous command word overwritten):

Address Field = 03F (hex)
Index Field = 00 (hex)

The Transmit Last Command Mode Code has Address Field boundary conditions for the location of command word buffers. The host can allocate a maximum 63 sequential locations following the Address Field starting address. For proper operation, the Address Field must start on an I x 40 (hex) address boundary, where I is greater than or equal to zero and less than or equal to 14. A list of valid Index and Address Fields follows:

I	Valid Index Fields	Valid Address Fields
0	3F (hex) to 00 (hex)	000 (hex) to 03F (hex)
1	3F (hex) to 00 (hex)	040 (hex) to 07F (hex)
2	3F (hex) to 00 (hex)	080 (hex) to 0BF (hex)
3	3F (hex) to 00 (hex)	0C0 (hex) to 0FF (hex)
4	3F (hex) to 00 (hex)	100 (hex) to 13F (hex)
5	3F (hex) to 00 (hex)	140 (hex) to 17F (hex)
6	3F (hex) to 00 (hex)	180 (hex) to 1BF (hex)
7	3F (hex) to 00 (hex)	1C0 (hex) to 1FF (hex)
8	3F (hex) to 00 (hex)	200 (hex) to 23F (hex)
9	3F (hex) to 00 (hex)	240 (hex) to 27F (hex)
10	3F (hex) to 00 (hex)	280 (hex) to 2BF (hex)
11	3F (hex) to 00 (hex)	2C0 (hex) to 2FF (hex)
12	3F (hex) to 00 (hex)	300 (hex) to 33F (hex)
13	3F (hex) to 00 (hex)	340 (hex) to 37F (hex)
14	3F (hex) to 00 (hex)	380 (hex) to 3BF (hex)

Subaddress/Mode Code		RAM Location	Subaddress/Mode Code		RAM Location
Transmit Vector Word Mode Code		3C0 (hex)	Transmit Last Command Mode Code		3E0 (hex)
Receive Subaddress	01	3C1 (hex)	Transmit Subaddress	01	3E1 (hex)
Receive Subaddress	02	3C2 (hex)	Transmit Subaddress	02	3E2 (hex)
Receive Subaddress	03	3C3 (hex)	Transmit Subaddress	03	3E3 (hex)
Receive Subaddress	04	3C4 (hex)	Transmit Subaddress	04	3E4 (hex)
Receive Subaddress	05	3C5 (hex)	Transmit Subaddress	05	3E5 (hex)
Receive Subaddress	06	3C6 (hex)	Transmit Subaddress	06	3E6 (hex)
Receive Subaddress	07	3C7 (hex)	Transmit Subaddress	07	3E7 (hex)
Receive Subaddress	08	3C8 (hex)	Transmit Subaddress	08	3E8 (hex)
Receive Subaddress	09	3C9 (hex)	Transmit Subaddress	09	3E9 (hex)
Receive Subaddress	10	3CA (hex)	Transmit Subaddress	10	3EA (hex)
Receive Subaddress	11	3CB (hex)	Transmit Subaddress	11	3EB (hex)
Receive Subaddress	12	3CC (hex)	Transmit Subaddress	12	3EC (hex)
Receive Subaddress	13	3CD (hex)	Transmit Subaddress	13	3ED (hex)
Receive Subaddress	14	3CE (hex)	Transmit Subaddress	14	3EE (hex)
Receive Subaddress	15	3CF (hex)	Transmit Subaddress	15	3EF (hex)
Receive Subaddress	16	3D0 (hex)	Transmit Subaddress	16	3F0 (hex)
Receive Subaddress	17	3D1 (hex)	Transmit Subaddress	17	3F1 (hex)
Receive Subaddress	18	3D2 (hex)	Transmit Subaddress	18	3F2 (hex)
Receive Subaddress	19	3D3 (hex)	Transmit Subaddress	19	3F3 (hex)
Receive Subaddress	20	3D4 (hex)	Transmit Subaddress	20	3F4 (hex)
Receive Subaddress	21	3D5 (hex)	Transmit Subaddress	21	3F5 (hex)
Receive Subaddress	22	3D6 (hex)	Transmit Subaddress	22	3F6 (hex)
Receive Subaddress	23	3D7 (hex)	Transmit Subaddress	23	3F7 (hex)
Receive Subaddress	24	3D8 (hex)	Transmit Subaddress	24	3F8 (hex)
Receive Subaddress	25	3D9 (hex)	Transmit Subaddress	25	3F9 (hex)
Receive Subaddress	26	3DA (hex)	Transmit Subaddress	26	3FA (hex)
Receive Subaddress	27	3DB (hex)	Transmit Subaddress	27	3FB (hex)
Receive Subaddress	28	3DC (hex)	Transmit Subaddress	28	3FC (hex)
Receive Subaddress	29	3DD (hex)	Transmit Subaddress	29	3FD (hex)
Receive Subaddress	30	3DE (hex)	Transmit Subaddress	30	3FE (hex)
Synchronize w/Data Word Mode Code		3DF (hex)	Transmit Bit Word Mode Code		3FF (hex)

1.3 Internal Registers

The RTS uses two internal registers to allow the host to control the RTS operation and monitor its status. The host uses the Control ($\overline{CTRL}$) signal along with Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) to read the 16-bit Status Register or write to the 13-bit Control Register. No address data is needed to select a register. The Control Register toggles bits in the MIL-STD-1553B status word, enables the biphase inputs, recognizes broadcast commands, selects Notice I and II or III, determines RAM Busy (RBUSY) timing, selects disconnect or terminal active flag, and puts the part in self-test mode. The Status Register supplies operational status of the UT1760A RTS to the host. These registers must be initialized before attempting RTS operation. Internal registers can be accessed while RBUSY is active.

Control Register (Write Only)
The 13-bit write-only Control Register manages the operation of the RTS. Write to the Control Register by applying a logic one to $\overline{OE}$, and a logic zero to $\overline{CTRL}$, $\overline{CS}$, and RD/$\overline{WR}$. Data is loaded into the Control Register via I/O pins DATA(12:0). Control register write must occur 50 ns before the rising edge of $\overline{COMSTR}$ to latch data into the outgoing status word.

Bit Number	Initial Condition	Description
Bit 0	[1]	Channel A Enable. A logic 1 enables Channel A biphase inputs.
Bit 1	[1]	Channel B Enable. A logic 1 enables Channel B biphase inputs.
Bit 2	[0]	Terminal Flag. A logic 1 sets the Terminal Flag bit of the Status Word.
Bit 3	[1]	System Busy. A logic 1 sets the Busy bit of the Status Word and limits RTS access to the memory. No data word can be retrieved or stored; command words will be stored.
Bit 4	[0]	Subsystem Busy. A logic 1 sets the Subsystem Flag bit of the Status Word.
Bit 5	[0]	Self-Test Channel Select. This bit selects which channel the self-test checks; a logic 1 selects Channel A and a logic 0 selects Channel B.
Bit 6	[0]	Self-Test Enable. A logic 1 places the RTS in the internal self-test mode and inhibits normal operation. Channels A and B should be disabled if self-test is chosen.
Bit 7	[0]	Service Request. A logic 1 sets the Service Request bit of the Status Word.
Bit 8	[0]	Instrumentation. A logic 1 sets the Instrumentation bit of the Status Word.
Bit 9	[1]	Broadcast Enable. A logic 1 enables the RTS to recognize broadcast commands.
Bit 10	[1]	Notice Select. A logic 1 enables Notice III operation; logic 0 enables Notice I or II operation.
Bit 11	[1]	DSCNCT/$\overline{TERACT}$ Pin Select. A logic 1 selects the "Disconnect" function; a logic 0 selects the "Terminal Active" function.
Bit 12	[1]	RBUSY Time Select. A logic 1 selects a 5.7 μs RBUSY alert; a logic 0 selects a 2.7 μs RBUSY alert.

[] - Values in parentheses indicate the initialized values of these bits.

CONTROL REGISTER (WRITE ONLY):

X	X	X	RBUSY TS	PS	NO-TICE	BCEN	INS	SRQ	ITST	ITCS	SUBS	BUSY	TF	CH B EN	CH A EN
			[1]	[1]	[1]	[1]	[0]	[0]	[0]	[0]	[0]	[1]	[0]	[1]	[1]

MSB LSB

[ ] defines reset state

Figure 4a. Control Register

Status Register (Read Only):
The 16-bit read-only Status Register provides the RTS system status. Read the Status Register by applying a logic 0 to $\overline{CTRL}$, $\overline{CS}$, and $\overline{OE}$, and a logic 1 to RD/$\overline{WR}$. The 16-bit contents of the Status Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
Bit 0	[0]	MCSA0. The LSB of the mode code or subaddress as indicated by the logic state of bit 5.
Bit 1	[0]	MCSA1. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 2	[0]	MCSA2. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 3	[0]	MCSA3. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 4	[0]	MCSA4. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 5	[0]	$\overline{MC}$/SA. A logic 1 indicates that bits 4 through 0 are the subaddress of the last command word, and that the last command word was a normal transmit or receive command. A logic 0 indicates that bits 4 through 0 are a mode code, and that the last command was a mode command.
Bit 6	[1]	Channel A/$\overline{B}$. A logic 1 indicates that the most recent command arrived on Channel A; a logic 0 indicates that it arrived on Channel B.
Bit 7	[1]	Channel B Enabled. A logic 1 indicates that Channel B is available for both reception and transmission.
Bit 8	[1]	Channel A Enabled. A logic 1 indicates that Channel A is available for both reception and transmission.
Bit 9	[1]	Terminal Flag Enabled. A logic 1 indicates that the Bus Controller has not issued an Inhibit Terminal Flag Mode Code. A logic 0 indicates that the Bus Controller, via the above mode code, is overriding the host system's ability to set the Terminal Flag bit of the status word.
Bit 10	[1]	Busy. A logic 1 indicates the Busy bit is set. This bit is reset when the System Busy bit in the Control Register is reset.
Bit 11	[0]	Self-Test. A logic 1 indicates that the chip is in the internal self-test mode. This bit is reset when the self-test is terminated.
Bit 12	[0]	TA Parity Error. A logic 1 indicates the wrong Terminal Address parity; it causes the biphase inputs to be disabled. TA Parity Error results in the Message Error bit being set to a logic one, and Channels A and B become disabled.
Bit 13	[0]	Message Error. A logic 1 indicates that a message error has occurred since the last Status Register read. This bit is not reset until the Status Register has been examined. Message error condition must be removed before reading the Status Register to reset the Message Error bit.
Bit 14	[0]	Valid Message. A logic 1 indicates that a valid message has been received since the last Status Register read. This bit is not reset until the Status Register has been examined.
Bit 15	[0]	Terminal Active. A logic 1 indicates the device is executing a transmit or receive operation. Same as $\overline{TERACT}$ output except active high. (Always $\overline{TERACT}$; never DSCNCT.)

[] - Values in parentheses indicate the initialized values of these bits.

STATUS REGISTER (READ ONLY):

TERM ACTV	VAL MESS	MESS ERR	TAPA ERR	SELF-TEST	BUSY	TFEN	CH A EN	CH B EN	CHNL A/B	$\overline{MC}$/ SA	MCSA 4	MCSA 3	MCSA 2	MCSA 1	MCSA 0
[0] MSB	[0]	[0]	[0]	[0]	[1]	[1]	[1]	[1]	[1]	[0]	[0]	[0]	[0]	[0]	[0] LSB

[ ] defines reset state

Figure 4b. Status Register

1.4 Mode Code and Subaddress

The UT1760A RTS provides two modes of illegal subaddress decoding, one meeting MIL-STD-1760A Notices I and II, and the other meeting MIL-STD-1760A Notice III. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. These definitions are extracted from MIL-STD-1760A and reviewed in section 1.5 of this document. Upon command word validation and decode, status pins MCSA(4:0) and $\overline{MC}$/SA become valid. Status pin $\overline{MC}$/SA will indicate whether the data on pins MCSA(4:0) is mode code or subaddress information. Status Register bits 0 through 5 contain the same information as pins MCSA(4:0) and $\overline{MC}$/SA.

The system designer can use signals MCSA(4:0), $\overline{MC}$/SA, $\overline{BRDCST}$, RTRT, etc. to illegalize mode codes, subaddresses, and other message formats (broadcast and RT-to-RT) via the Illegal Command (ILLCOM) input to the part.

RTS MODE CODE HANDLING PROCEDURE

T/$\overline{R}$	Mode Code	Function	Operation
0	10100	Selected Transmitter Shutdown (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10101	Override Selected Transmitter Shutdown (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10001	Synchronize (w/Data)	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control (2)	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
1	00001	Synchronize (1)	1. Command word stored 2. Status word transmitted
1	00010	Transmit Status Word (3)	1. Command word stored 2. Status word transmitted
1	00011	Initiate Self-Test (1)	1. Command word stored 2. Status word transmitted
1	00100	Transmitter Shutdown	1. Command word stored 2. Alternate bus shutdown 3. Status word transmitted
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Alternate bus enabled 3. Status word transmitted
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit set to zero and disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag	1. Command word stored 2. Terminal Flag bit enabled, but not set to logic one 3. Status word transmitted
1	01000	Reset Remote Terminal (1)	1. Command word stored 2. Status word transmitted
1	10010	Transmit Last Command Word (3)	1. Status word transmitted 2. Last command word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Notes:

1. Further host intersaction required for mode code operation.
2. Reserved mode code; A) MERR pin asserted, B) MESS ERR bit set, C) status word transmitted (ME bit set to logic one).
3. Status word not affected.
4. Undefined mode codes are treated as reserved mode codes.

1.5 MIL-STD-1760A Subaddress and Mode Code Definitions

Table 1. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice I

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 (1)	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 (2)	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	Reserved	Reserved	
00100 (04)	User Defined	User Defined	
00101 (05)	Reserved	Reserved	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	Reserved	Reserved	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	Reserved	Reserved	
01111 (15)	Reserved	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	Reserved	Reserved	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	Reserved	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	Reserved	Reserved	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:
1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

Table 2. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice II

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 (1)	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 (2)	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	Reserved	Reserved	
00100 (04)	User Defined	User Defined	
00101 (05)	Reserved	Reserved	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	Reserved	Reserved	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	Reserved	Reserved	
01111 (15)	Reserved	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	Reserved	Reserved	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	Reserved	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	Reserved	Reserved	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:
1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

Table 3. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice III

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 (1)	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 (2)	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	User Defined	User Defined	
00100 (04)	User Defined	User Defined	
00101 (05)	User Defined	User Defined	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	Test Only
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	B.40.2.2.1 (3)	B.40.2.2.1	Mission Store Control/Monitor
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	B.40.1.1.5.8 (4)	B.40.1.5.8	Mass Data Transfer
01111 (15)	User Defined	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	B.40.2.2.4 (5)	B.40.2.2.5 (6)	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	User Defined	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	B.40.2.2.4	B.40.2.2.5	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:
1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Refer to section B.40.2.2.1 of the MIL-STD-1760A specification for definition.
4. Refer to section B.40.1.1.5.8 of the MIL-STD-1760A specification for definition.
5. Refer to section B.40.2.2.4 of the MIL-STD-1760A specification for definition.
6. Refer to section B.40.2.2.5 of the MIL-STD-1760A specification for definition.
7. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

1.6 Terminal Address

The Terminal Address of the RTS is programmed via five input pins: RTA(4:0) and RTPTY. Asserting $\overline{MRST}$ latches the RTS's Terminal Address from pins RTA(4:0) and parity bit RTPTY. The address and parity cannot change until the next assertion of the $\overline{MRST}$. The parity of the Terminal Address is odd; input pin RTPTY is set to a logic state to satisfy this requirement. A logic 1 on Status Register bit 12 indicates incorrect Terminal Address parity. An example follows:

RTA(4:0) = 05 (hex) = 00101
RTPTY = 1 (hex) = 1
Sum of 1's = 3 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 0 (hex) = 0
Sum of 1's = 1 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 1 (hex) = 1
Sum of 1's = 2 (even), Status Register bit 12 = 1

The RTS checks the Terminal Address and parity on Master Reset. The state of the DSCNCT signal indicates the mated status of the store. When all six Terminal Address pins (RTA(4:0), RTPTY) go to a logic one, the DSCNCT pin is asserted. To enable the disconnect function (DSCNCT pin) bit 11 of the Control Register is set to a logic one. With broadcast disabled, RTA (4:0) = 11111 operates as a normal RT address.

1.7 Internal Self-Test

Setting bit 6 of the Control Register to a logic one enables the internal self-test. Disable Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The self-test capability of the RTS is based on the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the encoder is fed back to the decoder, the RTS will recognize the incoming status word as a command word and thus cause the RTS to transmit another status word. After the host invokes self-test, the RTS self-test logic forces a status word transmission even though the RTS has not received a valid command. The status word is sent to decoder A or B depending on the channel the host selected for self-test. The self-test is controlled by the host periodically changing the bit patterns in the status word being transmitted. Writing to the Control Register bits 2, 3, 4, 7, 8, and 10 changes the status word. Monitor the self-test by sampling either the Status Register or the external status pins (i.e. Command Strobe ($\overline{COMSTR}$), Transmit/Receive (T/$\overline{R}$)). For more detailed explanation of internal self-test, consult UTMC publication *RTR/RTS Internal Self-Test Routine.*

1.8 Power-up and Master Reset

After power-up, reset initializes the part with its biphase ports enabled, latches the Terminal Address, selects Notice III subaddress decoding, and turns on the busy option. The device is ready to accept commands from the MIL-STD-1553B bus. The busy flag is asserted while the host is loading the message pointers and messages. After this task is completed, the host removes the busy condition via a Control Register write to the RTS. On power-up if the terminal address parity (odd) is incorrect, the biphase inputs are disabled and the message error pin (MERR) is asserted. This condition can also be monitored via bit 12 of the Status Register. The MERR pin is negated on reception of first valid command.

1.9 Encoder and Decoder

The RTS interfaces directly to a bus transmitter/ receiver via the RTS Manchester II encoder/decoder. The UT1760A RTS receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RTS processes each incoming data word for correct format and checks the control logic for correct word count and contiguous data. If an invalid message error is detected, the message error pin is asserted, the RTS ceases processing the remainder (if any) of the message, and it then suppresses status word transmission. Upon command validation recognition, the external status outputs are enabled. Reception of illegal commands does not suppress status word transmission.

The RTS automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the transmitter error pin (TXERR) is asserted. In addition to the loop-back compare test, a timer precludes a transmission greater than 760 microseconds by the assertion of Fail-safe Timer ($\overline{TIMERON}$). This timer is reset upon receipt of another command. (RT-to-RT transfer time-out = 57 μs).

1.10 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic makes sure that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message error bit and suppressing transmission of the status word.

1.11 Illegal Command Decoding

The host has the option of asserting the ILLCOM pin to illegalize a received command word. On receipt of an illegal command, the RTS sets the Message Error bit in the status word, sets the message error output, and sets the message error latch in the Status Register.

The following RTS outputs may be used to externally decode an illegal command, Mode Code or Subaddress indicator ($\overline{MC}$/SA), Mode Code or Subaddress bus MCSA(4:0), Command Strobe ($\overline{COMSTR}$), Broadcast ($\overline{BRDCST}$), and Remote Terminal to Remote Terminal transfer (RTRT) (see figure 21 on page 33.)

To illegalize a transmit command, the ILLCOM pin must be asserted within 3.3 µs after VALMSG goes to a logic 1 if the RTS is to respond with the Message Error bit of the status word at a logic 1. If the illegal command is mode code 2, 4, 5, 6, 7, or 18, the ILLCOM pin must be asserted within 664 ns after Command Strobe ($\overline{COMSTR}$) transitions to logic 0. Assserting the ILLCOM pin within the 664 ns inhibits the mode code function. For mode code illegalization, assert the ILLCOM pin until the VALMSG signal is asserted.

For an illegal receive command, the ILLCOM pin must be asserted within 18.2 µs after the $\overline{COMSTR}$ transitions to a logic 0 in order to suppress data words from being stored. In addition, the ILLCOM pin must be at a logic 1 throughout the reception of the message until VALMSG is asserted. This does not apply to illegal transmit commands since the status word is transmitted first.

The above timing conditions also apply when the host externally decodes an illegal broadcast command. The host must remove the illegal command condition so that the next command is not falsely decoded as illegal.

2.0 Memory Map Example

Figures 5 and 6 illustrate the UT1760A RTS buffering three receive command messages to Subaddress 4. The receive message pointer for Subaddress 4 is located at 03C4 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03C4 (hex) point to the memory location where the first receive message is stored. The Address Field defined as bits 0 through 9 of address 03C4 (hex) contain address information. The Index Field defined as bits 10 through 15 of address 03C4 (hex) contain the message buffer index (i.e. number of messages buffered).

Figure 5 demonstrates the updating of the message pointer as each message is received and stored. The memory storage of these three messages is shown in figure 6. After receiving the third message for Subaddress 4 (i.e. Index Field equals zero) the Address Field of the message pointer is not incremented. If the host does not update the receive message pointer for Subaddress 4 before the next receive command for Subaddress 4 is accepted, the third message will be overwritten.

Figures 7 and 8 show an example of multiple message retrieval from Subaddress 16 upon reception of a MIL-STD-1553B transmit command. The message pointer for transmit Subaddress 16 is located at 03F0 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03F0 (hex) point to the memory location where the first message data words are stored.

Figure 7 demonstrates the updating of the message pointer as each message is received and stored. The data memory for these three messages is shown in figure 8.

Example:
Remote terminal will receive and buffer three MIL-STD-1553 receive commands of various word lengths to Subaddress 4.

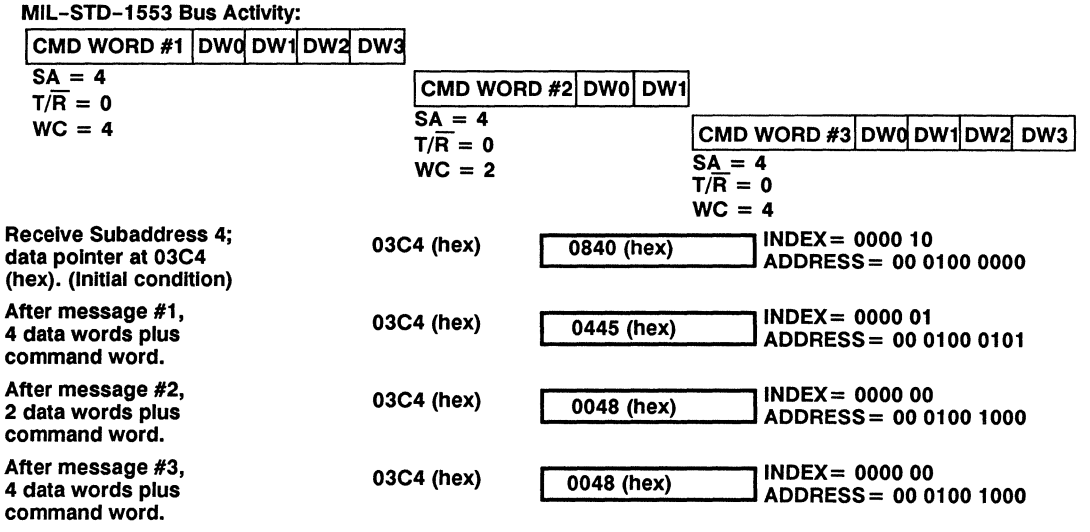


Figure 5. RTS Message Handling

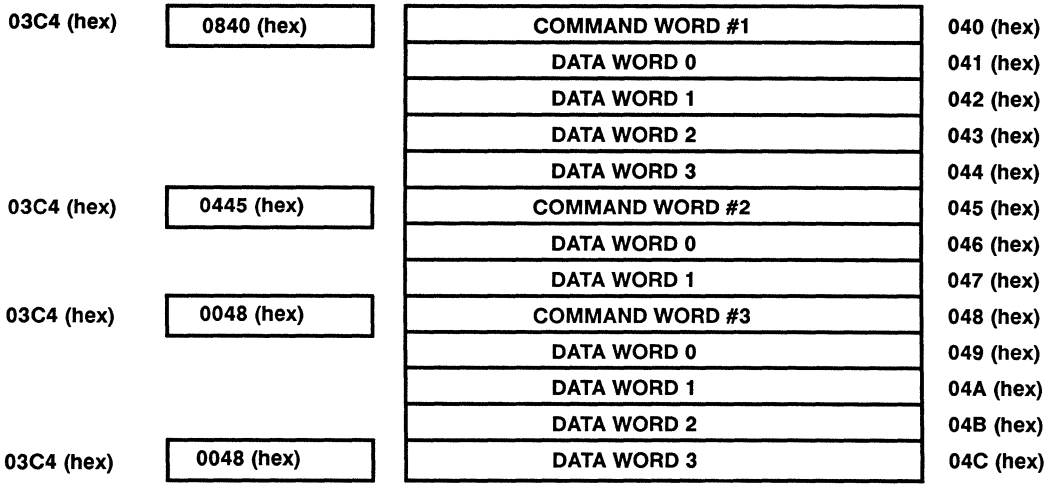


Figure 6. Memory Storage Subaddress 4

Example:
Remote terminal will transmit and buffer three MIL-STD-1553 transmit commands of various word lengths to Subaddress 16.

MIL-STD-1553 Bus Activity:

CMD WORD #1	SW	DW0	DW1	DW2	DW3

SA= 16
T/R= 1
WC= 4

CMD WORD #2	SW	DW0	DW1

SA= 16
T/R= 1
WC= 2

CMD WORD #3	SW	DW0	DW1	DW2	DW3

SA= 16
T/R= 1
WC= 4

Transmit Subaddress 16; data pointer at 03F0 (hex). (Initial condition)	03F0 (hex)	0830 (hex)	INDEX= 0000 10 ADDRESS= 00 0011 0000
After message #1, 4 data words.	03F0 (hex)	0434 (hex)	INDEX= 0000 01 ADDRESS= 00 0011 0100
After message #2, 2 data words.	03F0 (hex)	0036 (hex)	INDEX= 0000 00 ADDRESS= 00 0011 0110
After message #3, 4 data words.	03F0 (hex)	0036 (hex)	INDEX= 0000 00 ADDRESS= 00 0011 0110

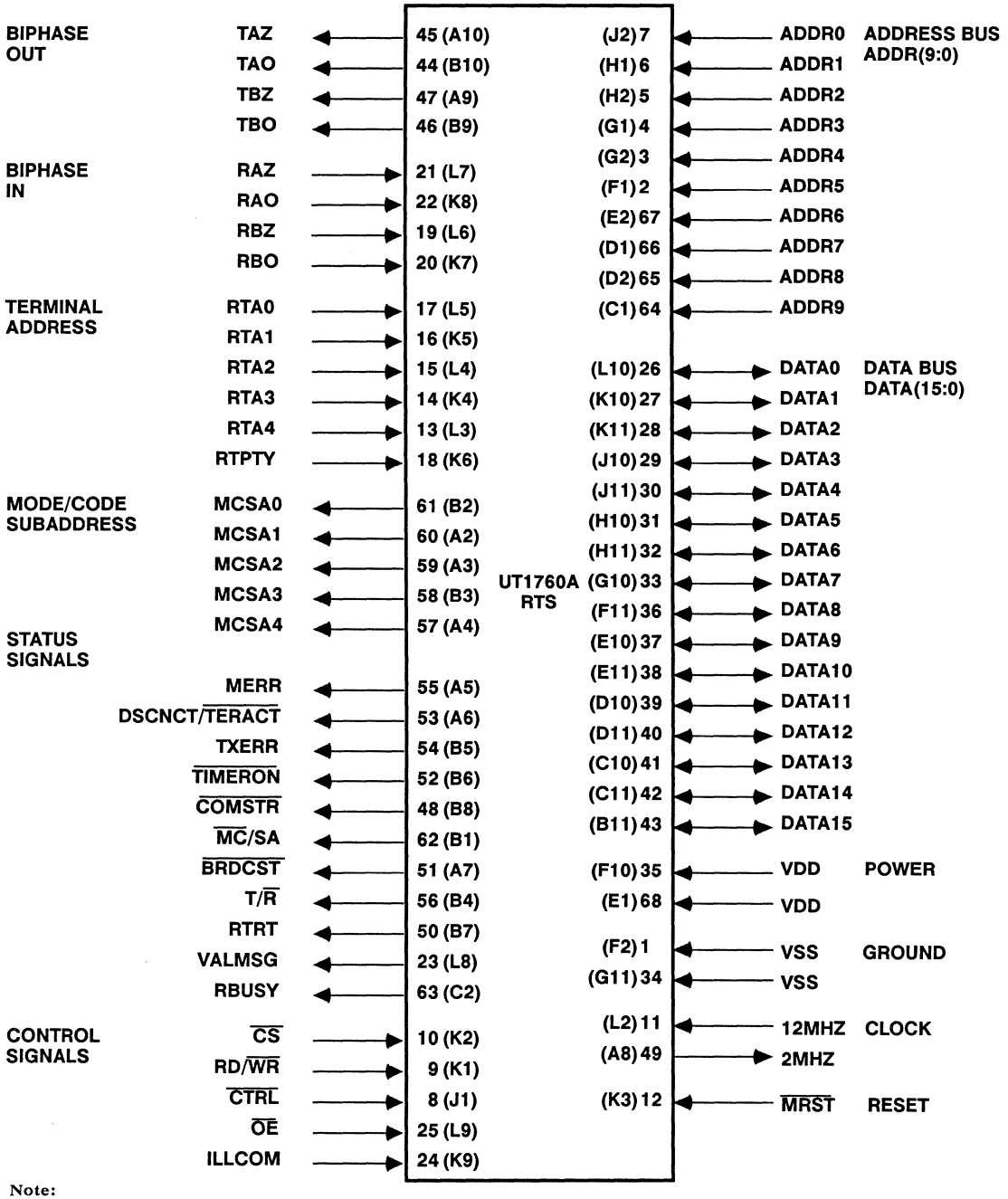
Figure 7. RTS Message Handling

03F0(hex)	0830 (hex)	DATA WORD 0	030 (hex)
		DATA WORD 1	031 (hex)
		DATA WORD 2	032 (hex)
		DATA WORD 3	033 (hex)
03F0 (hex)	0434 (hex)	DATA WORD 0	034 (hex)
		DATA WORD 1	035 (hex)
03F0 (hex)	0036 (hex)	DATA WORD 0	036 (hex)
		DATA WORD 1	037 (hex)
		DATA WORD 2	038 (hex)
03F0 (hex)	0036 (hex)	DATA WORD 3	039 (hex)

Note:
Example is valid only if massage structure is known in advance.

Figure 8. Memory Storage Subaddress 16

3.0 Pin Identification And Description



Note:
( ) Pingrid array pin numbers are in parentheses.
Leadless chip carrier pin numbers are not in parentheses.

Figure 9. UT1760A RTS Pin Description

Legend for TYPE and ACTIVE fields:

TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TO = TTL output
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional
AL = Active low
AH = Active high
[] - Value in parentheses indicates initial state of these pins.

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DATA(15)	43	B11	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
DATA(14)	42	C11	TTB	--	Bit 14 of the bidirectional Data bus.
DATA(13)	41	C10	TTB	--	Bit 13 of the bidirectional Data bus.
DATA(12)	40	D11	TTB	--	Bit 12 of the bidirectional Data bus.
DATA(11)	39	D10	TTB	--	Bit 11 of the bidirectional Data bus.
DATA(10)	38	E11	TTB	--	Bit 10 of the bidirectional Data bus.
DATA(9)	37	E10	TTB	--	Bit 9 of the bidirectional Data bus.
DATA(8)	36	F11	TTB	--	Bit 8 of the bidirectional Data bus.
DATA(7)	33	G10	TTB	--	Bit 7 of the bidirectional Data bus.
DATA(6)	32	H11	TTB	--	Bit 6 of the bidirectional Data bus.
DATA(5)	31	H10	TTB	--	Bit 5 of the bidirectional Data bus.
DATA(4)	30	J11	TTB	--	Bit 4 of the bidirectional Data bus.
DATA(3)	29	J10	TTB	--	Bit 3 of the bidirectional Data bus.
DATA(2)	28	K11	TTB	--	Bit 2 of the bidirectional Data bus.
DATA(1)	27	K10	TTB	--	Bit 1 of the bidirectional Data bus.
DATA(0)	26	L10	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR(9)	64	C1	TI	--	Bit 9 (MSB) of the Address bus.
ADDR(8)	65	D2	TI	--	Bit 8 of the Address bus.
ADDR(7)	66	D1	TI	--	Bit 7 of the Address bus.
ADDR(6)	67	E2	TI	--	Bit 6 of the Address bus.
ADDR(5)	2	F1	TI	--	Bit 5 of the Address bus.
ADDR(4)	3	G2	TI	--	Bit 4 of the Address bus.
ADDR(3)	4	G1	TI	--	Bit 3 of the Address bus.
ADDR(2)	5	H2	TI	--	Bit 2 of the Address bus.
ADDR(1)	6	H1	TI	--	Bit 1 of the Address bus.
ADDR(0)	7	J2	TI	--	Bit 0 (LSB) of the Address bus.

CONTROL INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{CS}$	10	K2	TI	AL	Chip Select. The host processor uses the $\overline{CS}$ signal for RTS Status Register reads, Control Register writes, or host access to the RTS internal RAM.
RD/$\overline{WR}$	9	K1	TI	--	Read/Write. The host processor uses a high level on this input in conjunction with $\overline{CS}$ to read the RTS Status Register or the RTS internal RAM. A low level on this input is used in conjunction with $\overline{CS}$ to write to the RTS Control Register or the RTS internal RAM.
$\overline{CTRL}$	8	J1	TI	AL	Control. The host processor uses the active low $\overline{CTRL}$ input signal in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ to access the RTS registers. A high level on this input means access is to RTS internal RAM only.
$\overline{OE}$	25	L9	TI	AL	Output Enable. The active low $\overline{OE}$ signal is used to control the direction of data flow from the RTS. For $\overline{OE}$ = 1, the RTS Data bus is three-state; for $\overline{OE}$ = 0, the RTS Data bus is active.
ILLCOM	24	K9	TDI	AH	Illegal Command. The host processor uses the ILLCOM input to inform the RTS that the present command is illegal.

STATUS OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
MERR [0]	55	A5	TO	AH	Message Error. The active high MERR output signals that the Message Error bit in the Status Register has been set due to receipt of an illegal command, or an error during message sequence. MERR will reset to logic zero on the receipt of next valid command.
TXERR [0]	54	B5	TO	AH	Transmission Error. The active high TXERR output is asserted when the RTS detects an error in the reflected word versus the transmitted word, using the continuous loop-back compare feature. Reset on next $\overline{COMSTR}$ assertion.
$\overline{TIMERON}$ [1]	52	B6	TO	AL	Fail-safe Timer. The $\overline{TIMERON}$ output pulses low for 760 microseconds when the RTS begins transmitting (i.e. rising edge of VALMSG) to provide a fail-safe timer meeting the requirements of MIL-STD-1553B. This pulse is reset when $\overline{COMSTR}$ goes low or during a Master Reset.
$\overline{COMSTR}$ [1]	48	B8	TO	AL	Command Strobe. $\overline{COMSTR}$ is an active low output of 500 ns duration identifying receipt of a valid command.
$\overline{BRDCST}$ [1]	51	A7	TO	AL	Broadcast. $\overline{BRDCST}$ is an active low output that identifies receipt of a valid broadcast command.
RTRT [0]	50	B7	TO	AH	Remote Terminal to Remote Terminal. RTRT is an active high output indicating that the RTS is processing a remote terminal to remote terminal command.

Continued on page 19.

STATUS OUTPUTS

Continued from page 18.

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
DSCNCT or $\overline{\text{TERACT}}$ [X]	53	A6	TO	--	Disconnect or Terminal Active. Bit 11 of the Control Register selects the mode of this dual-function pin. In the "Disconnect" mode (bit 11 = 1), the active high DSCNCT output is asserted when all six Terminal Address pins (RTA0 - RTA4, RTPTY) go high, indicating a disconnect condition. In the "Terminal Active" mode (bit 11 = 0), the active low $\overline{\text{TERACT}}$ output is asserted at the beginning of the RTS access to internal RAM for a given command and negated after the last access for that command.
VALMSG [0]	23	L8	TO	AH	Valid Message. VALMSG is an active high output indicating a valid message (including Broadcast) has been received. VALMSG goes high prior to transmitting the 1553 status word and is reset upon receipt of the next command.
RBUSY [0]	63	C2	TO	AH	RTS Busy. RBUSY is asserted high while the RTS is accessing its own internal RAM either to read or update the pointers or to store or retrieve data words. RBUSY becomes active either 2.7 µs or 5.7 µs before RTS requires RAM access. This timing is controlled by Control Register bit 12; see section 1.3.
T/$\overline{\text{R}}$ [0]	56	B4	TO	--	Transmit/Receive. A high level on this pin indicates a transmit command message transfer is being or was processed, while a low level indicates a receive command message transfer is being or was processed.

MODE CODE/SUBADDRESS OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{MC}}$/SA [0]	62	B1	TO	--	Mode Code/Subaddress Indicator. If $\overline{\text{MC}}$/SA is low, it indicates that the most recent command word is a mode code command. If $\overline{\text{MC}}$/SA is high, it indicates that the most recent command word is for a subaddress. This output indicates whether the mode code/subaddress outputs (i.e. MCSA(4:0)) contain mode code or subaddress information.
MCSA0 [0]	61	B2	TO	--	Mode Code/Subaddress Output 0. If $\overline{\text{MC}}$/SA is low, this pin represents the least significant bit of the most recent command word (the LSB of the mode code). If $\overline{\text{MC}}$/SA is high, this pin represents the LSB of the subaddress.
MCSA1 [0]	60	A2	TO	--	Mode Code/Subaddress Output 1.
MCSA2 [0]	59	A3	TO	--	Mode Code/Subaddress Output 2.
MCSA3 [0]	58	B3	TO	--	Mode Code/Subaddress Output 3.

Continued on page 20.

MODE CODE/SUBADDRESS OUTPUTS

Continued from page 19.

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
MCSA4 [0]	57	A4	TO	--	Mode Code/Subaddress Output 4. If $\overline{MC}$/SA is low, this pin represents the most significant bit of the mode code. If $\overline{MC}$/SA is high, this pin represents the MSB of the subaddress.

REMOTE TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
RTA4	13	L3	TUI	--	Remote Terminal Address bit 4 (MSB).
RTA3	14	K4	TUI	--	Remote Terminal Address bit 3.
RTA2	15	L4	TUI	--	Remote Terminal Address bit 2.
RTA1	16	K5	TUI	--	Remote Terminal Address bit 1.
RTA0	17	L5	TUI	--	Remote Terminal Address bit 0 (LSB).
RTPTY	18	K6	TUI	--	Remote Terminal Address Parity. This input must provide odd parity for the Remote Terminal Address.

BIPHASE INPUTS (1)

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
RAZ	21	L7	TI	--	Receiver - Channel A, Zero Input. Idle low Manchester input from the 1553 bus receiver.
RAO	22	K8	TI	--	Receiver - Channel A, One Input. This input is the complement of RAZ.
RBZ	19	L6	TI	--	Receiver - Channel B, Zero Input. Idle low Manchester input from the 1553 bus receiver.
RBO	20	K7	TI	--	Receiver - Channel B, One Input. This input is the complement of RBZ.

Note:

1. For uniphase operation, tie RAO (or RBO) to V_{DD} and apply uniphase input signal to RAZ (or RBZ).

BIPHASE OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
TAZ [0]	45	A10	TO	--	Transmitter - Channel A, Zero Output. This Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TAO [0]	44	B10	TO	--	Transmitter - Channel A, One Output. This output is the complement of TAZ. The output is idle low.
TBZ [0]	47	A9	TO	--	Transmitter - Channel B, Zero Output. This Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TBO [0]	46	B9	TO	--	Transmitter - Channel B, One Output. This output is the complement of TBZ. The output is idle low.

MASTER RESET AND CLOCK

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{MRST}$	12	K3	TUI	AL	Master Reset. Initializes all internal functions of the RTS. $\overline{MRST}$ must be asserted 500 ns before normal RTS operation (500 ns minimum). Does not reset RAM.
12MHz	11	L2	TI	--	12 MHz Input Clock. This is the RTS system clock that requires an accuracy greater than 0.01% with a duty cycle of 50% +/- 10%.
2MHz	49	A8	TO	--	2 MHz Clock Output. This is a 2 MHz clock output generated by the 12 MHz input clock. This clock is stopped when $\overline{MRST}$ is low.

POWER AND GROUND

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
VDD	35 68	F10 E1	PWR PWR	-- --	+5 VDC Power. Power supply must be +5 VDC +/-10%.
VSS	1 34	F2 G11	GND GND	-- --	Reference ground. Zero VDC logic ground.

3

4.0 Operating Conditions

ABSOLUTE MAXIMUM RATINGS*
(referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
VDD	DC supply voltage	-0.3 to +7.0	V
VIO	Voltage on any pin	-0.3 to VDD+0.3	V
II	DC input current	+/-10	mA
TSTG	Storage temperature	-65 to +150	°C
PD	Maximum power dissipation (1)	300	mW
TJ	Maximum junction temperature	+175	°C
ΘJC	Thermal resistance, junction-to-case	20	°C/W

Note:
1. Does not reflect the added P_D due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
VDD	DC supply voltage	4.5 to 5.5	V
VIN	DC input voltage	0 to VDD	V
TC	Temperature range	-55 to +125	°C
FO	Operating frequency	12 +/-.01%	MHz

5.0 DC Electrical Characteristics

(V_{DD} = 5.0 V +/-10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
VIL	Low-level input voltage			0.8	V
VIH	High-level input voltage		2.0		V
IIN	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	 VIN = VDD or VSS VIN = VDD VIN = VSS	 -1 110 -2000	 1 2000 -110	 µA µA µA
VOL	Low-level output voltage	IOL = 3.2 mA		0.4	V
VOH	High-level output voltage	IOH = -400 µA	2.4		V
IOZ	Three-state output leakage current	VO = VDD or VSS	-10	+10	µA
IOS	Short-circuit output current (1,2)	VDD = 5.5 V, VO = V_{DD} VDD = 5.5 V, VO = 0 V	 -90	90	mA mA
CIN	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
COUT	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
CIO	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		20	pF
IDD	Average operating current (1,4)	F = 12 MHz, CL = 50 pF		50	mA
QIDD	Quiescent current	Note 5		1.5	mA

Notes:
1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
4. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
5. All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

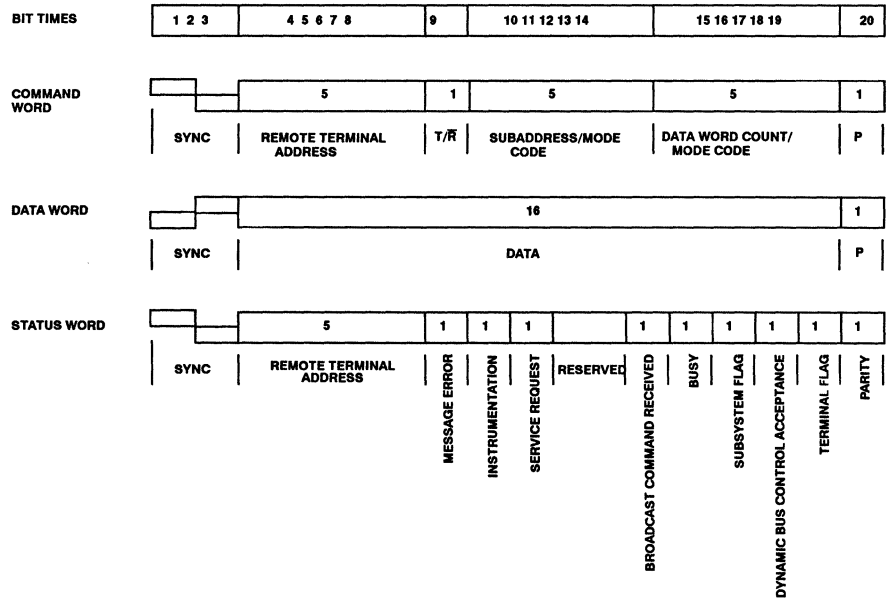
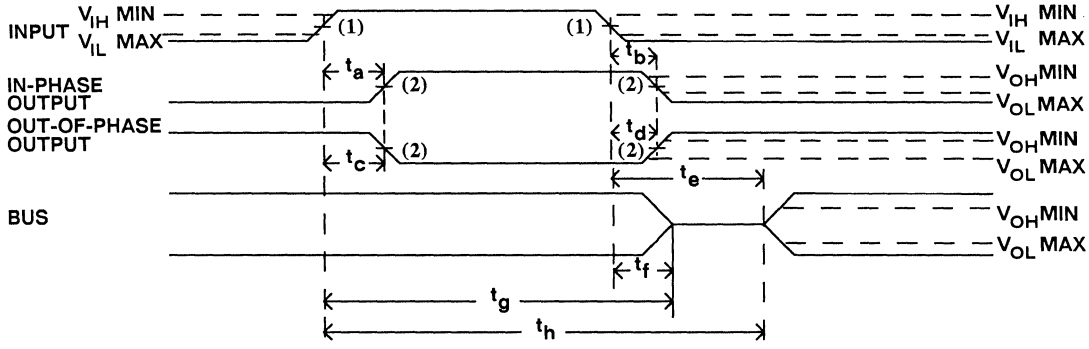


Figure 10. MIL-STD-1553B Word Formats

6.0 AC Electrical Characteristics

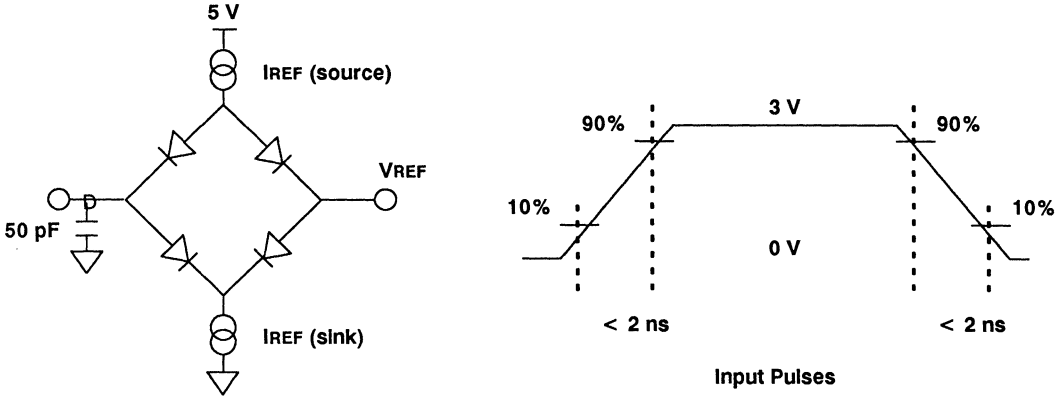
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pf load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 11a. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

Figure 11b. AC Test Loads and Input Waveforms

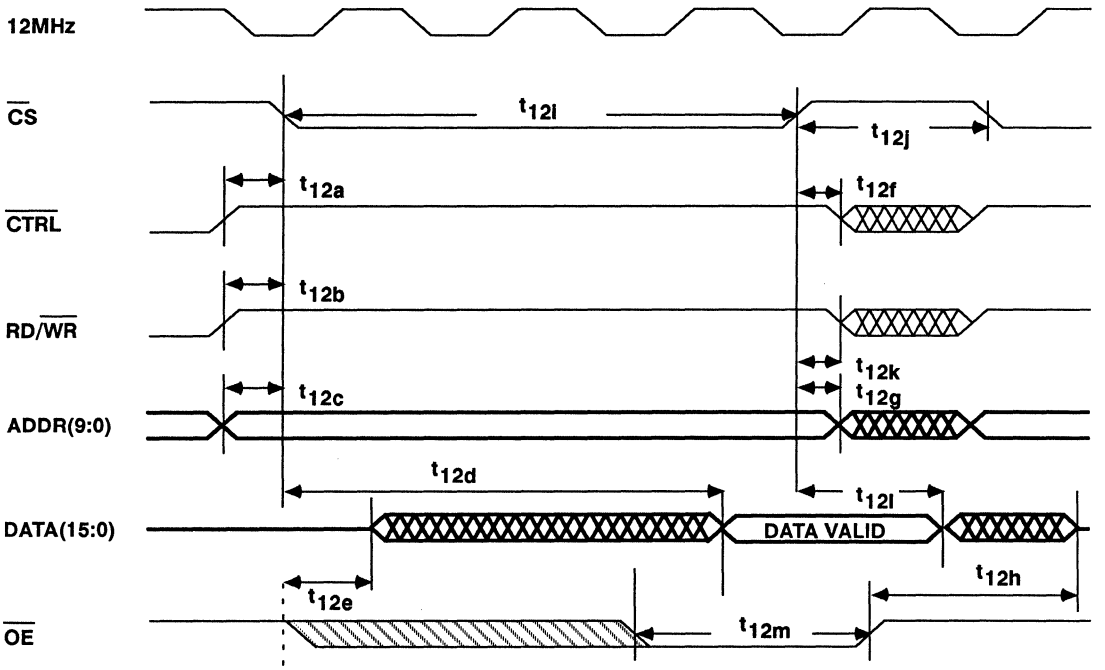


Figure 12. Microprocessor RAM Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t12a	$\overline{CTRL}$ ↑ set up wrt $\overline{CS}$ ↓ (1)	10	--	ns
t12b	RD/$\overline{WR}$ ↑ set up wrt $\overline{CS}$ ↓	10	--	ns
t12c	ADDR(9:0) Valid to $\overline{CS}$ ↓ (Address Set up)	10	--	ns
t12d	$\overline{CS}$ ↓ to DATA(15:0) Valid	--	155	ns
t12e	$\overline{OE}$ ↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t12f	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	0	--	ns
t12g	$\overline{CS}$ ↑ to ADDR(9:0) Don't Care	0	--	ns
t12h	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	--	40	ns
t12i	$\overline{CS}$ ↓ to $\overline{CS}$ ↑ (2)	220	5500	ns
t12j	$\overline{CS}$ ↑ to $\overline{CS}$ ↓	85	--	ns
t12k	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t12l	$\overline{CS}$ ↑ to DATA(15:0) Invalid (3)	25	--	ns
t12m	$\overline{OE}$ ↓ to $\overline{OE}$ ↑	65	--	ns

Notes:
1. "wrt" defined as "with respect to."
2. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.
3. Assumes $\overline{OE}$ is asserted.

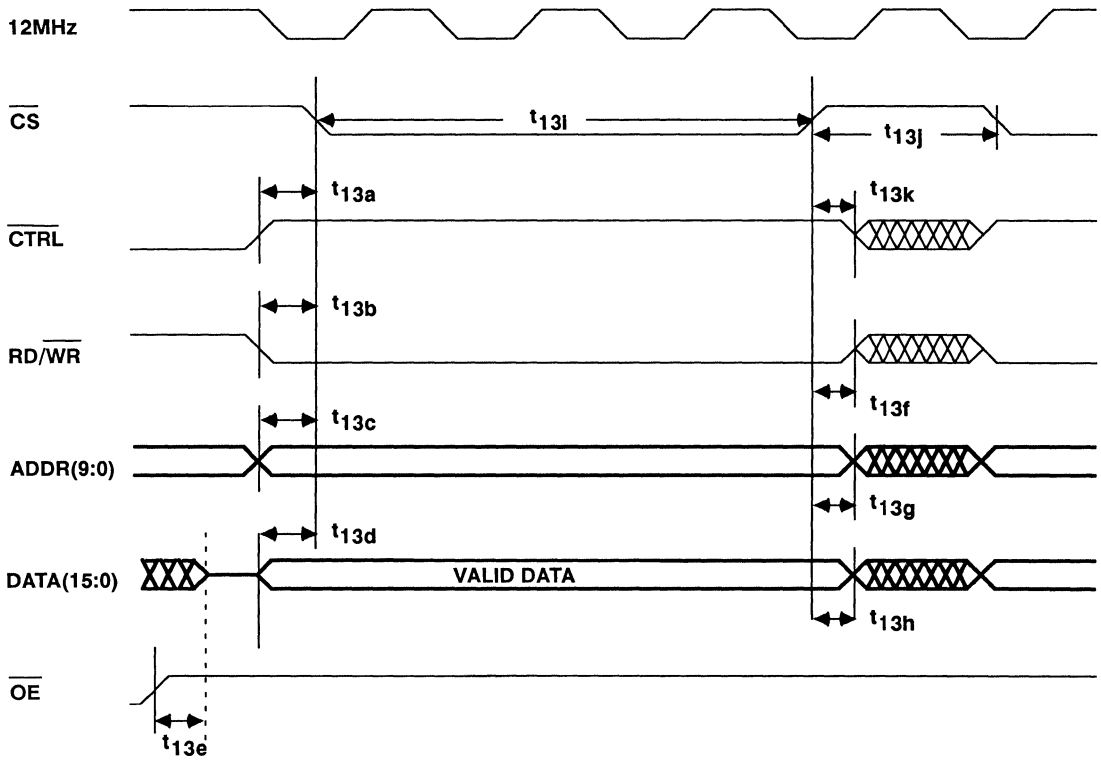


Figure 13. Microprocessor RAM Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t13a	$\overline{CTRL}$ ↑ set up wrt $\overline{CS}$ ↓	10	--	ns
t13b	RD/$\overline{WR}$ ↓ set up wrt $\overline{CS}$ ↓	10	--	ns
t13c	ADDR(9:0) Valid to $\overline{CS}$ ↓ (Address set up)	10	--	ns
t13d	DATA(15:0) Valid to $\overline{CS}$ ↓ (DATA set up)	0	--	ns
t13e	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	40	--	ns
t13f	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t13g	$\overline{CS}$ ↑ to ADDR(9:0) Don't Care	0	--	ns
t13h	$\overline{CS}$ ↑ to DATA(15:0) Don't Care (Hold-time)	20	--	ns
t13i	$\overline{CS}$ ↓ to $\overline{CS}$ ↑(1)	180	5500	ns
t13j	$\overline{CS}$ ↑ to $\overline{CS}$ ↓	85	--	ns
t13k	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	0	--	ns

Note:

1. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

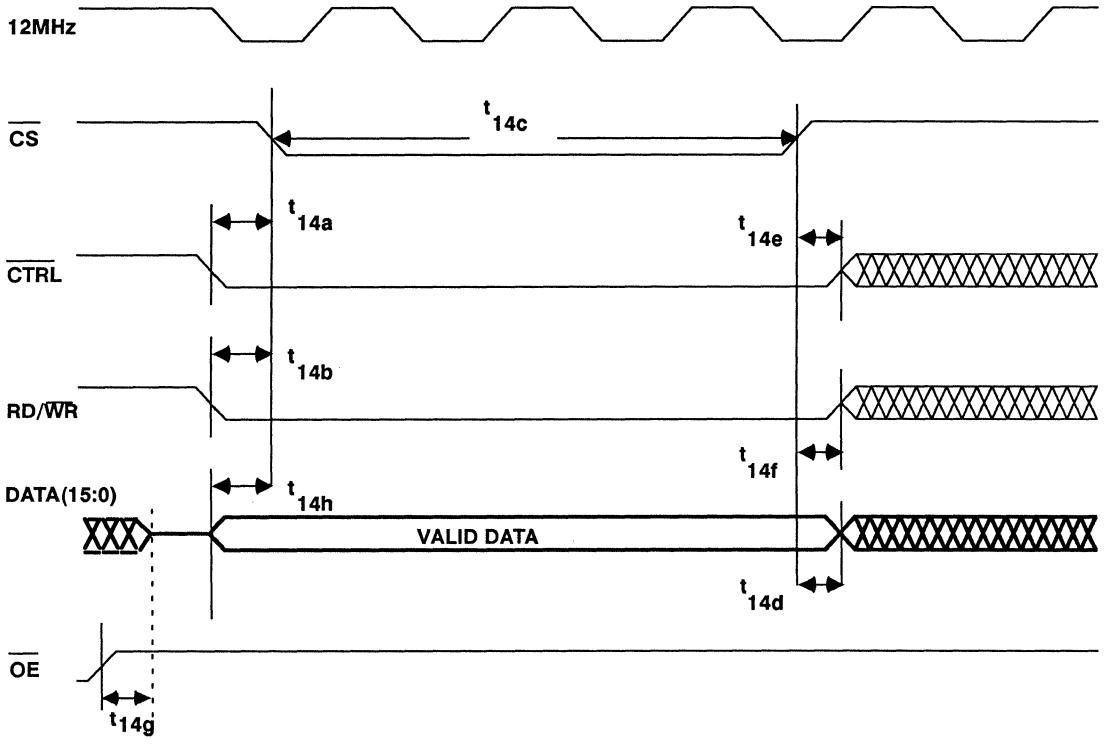


Figure 14. Control Register Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t14a	CTRL ↓ set up wrt CS ↓	0	--	ns
t14b	RD/WR ↓ set up wrt CS ↓	0	--	ns
t14c	CS ↓ to CS ↑(1)	50	5500	ns
t14d	CS ↑ to DATA(15:0) Don't Care (Hold-time)	0	--	ns
t14e	CS ↑ to CTRL Don't Care	0	--	ns
t14f	CS ↑ to RD/WR Don't Care	0	--	ns
t14g	OE ↑ to DATA(15:0) High Impedance	40	--	ns
t14h	DATA(15:0) Valid to CS ↓ (DATA set up)	0	--	ns

Note:

1. The maximum amount of time that CS can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum CS low time is 2500 ns.

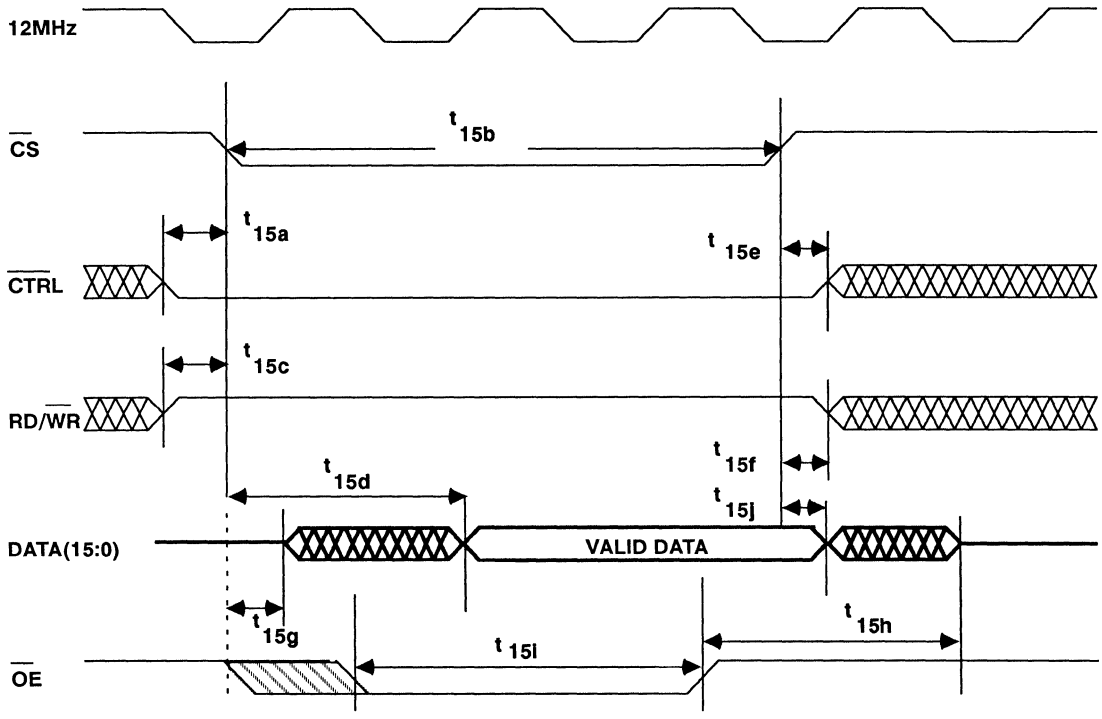


Figure 15. Status Register Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t15a	$\overline{CTRL}$ ↓ set up wrt $\overline{CS}$ ↓	0	--	ns
t15b	$\overline{CS}$ ↓ to $\overline{CS}$ ↑(1)	65	5500	ns
t15c	RD/$\overline{WR}$ ↑ set up wrt $\overline{CS}$ ↓	0	--	ns
t15d	$\overline{CS}$ ↓ to DATA(15:0) Valid	--	65	ns
t15e	$\overline{CS}$ ↑ to $\overline{CTRL}$ Don't Care	5	--	ns
t15f	$\overline{CS}$ ↑ to RD/$\overline{WR}$ Don't Care	5	--	ns
t15g	$\overline{OE}$ ↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t15h	$\overline{OE}$ ↑ to DATA(15:0) High Impedance	--	40	ns
t15i	$\overline{OE}$ ↓ to $\overline{OE}$ ↑	65	--	ns
t15j	$\overline{CS}$ ↓ to DATA(15:0) Don't Care (Active)	25	--	ns

Note:

1. The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

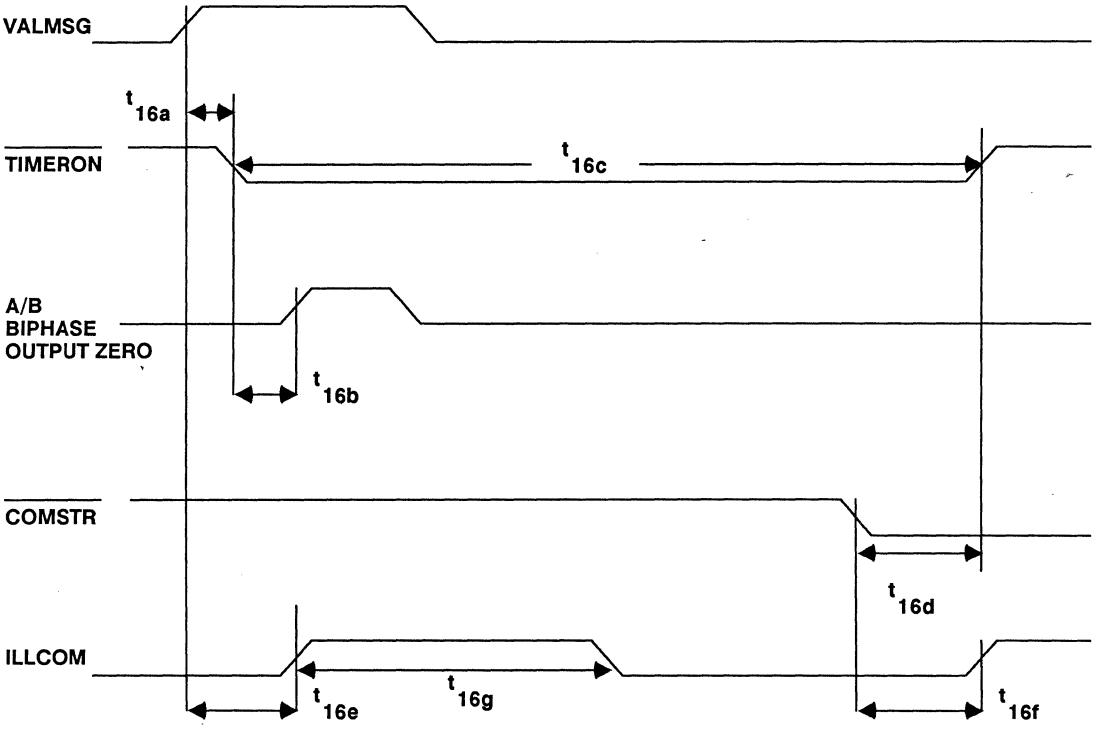
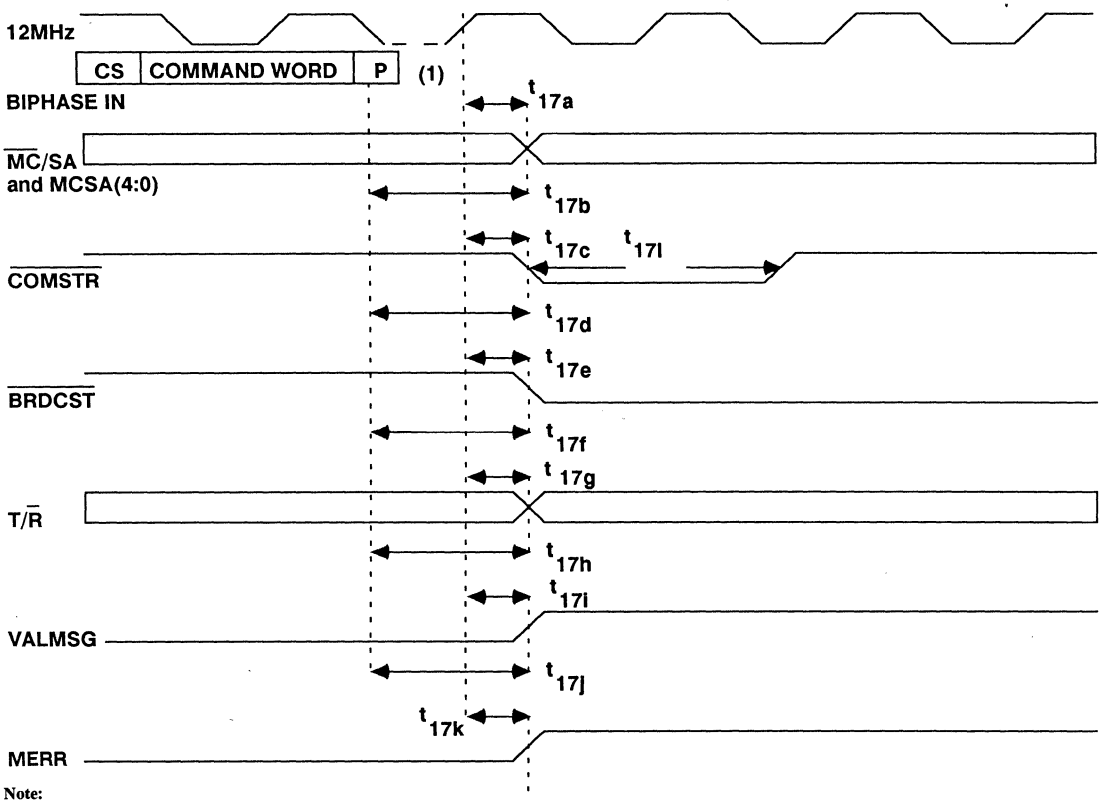


Figure 16. RT Fail-Safe Timer Signal Relationships

SYMBOL	PARAMETER	MIN	MAX	UNITS
t16a	VALMSG ↑ before $\overline{\text{TIMERON}}$ ↓	0	35	ns
t16b	$\overline{\text{TIMERON}}$ ↓ before first BIPHASE OUT O ↑	1.2	--	µs
t16c	$\overline{\text{TIMERON}}$ low pulse width (time-out)	727.3	727.4	µs
t16d	$\overline{\text{COMSTR}}$ ↓ to $\overline{\text{TIMERON}}$ ↑	--	25	ns
t16e	VALMSG ↑ to ILLCOM ↑	--	3.3	µs
t16f	$\overline{\text{COMSTR}}$ ↓ to ILLCOM ↑ (1)	--	664	ns
t16f	$\overline{\text{COMSTR}}$ ↓ to ILLCOM ↑ (2)	--	18.2	µs
t16g	ILLCOM ↑ to ILLCOM ↓ (3)	500	--	ns

Notes:
1. Mode code 2, 4, 5, 6, 7, or 18 received.
2. To suppress data word storage.
3. For transmit command illegalization.

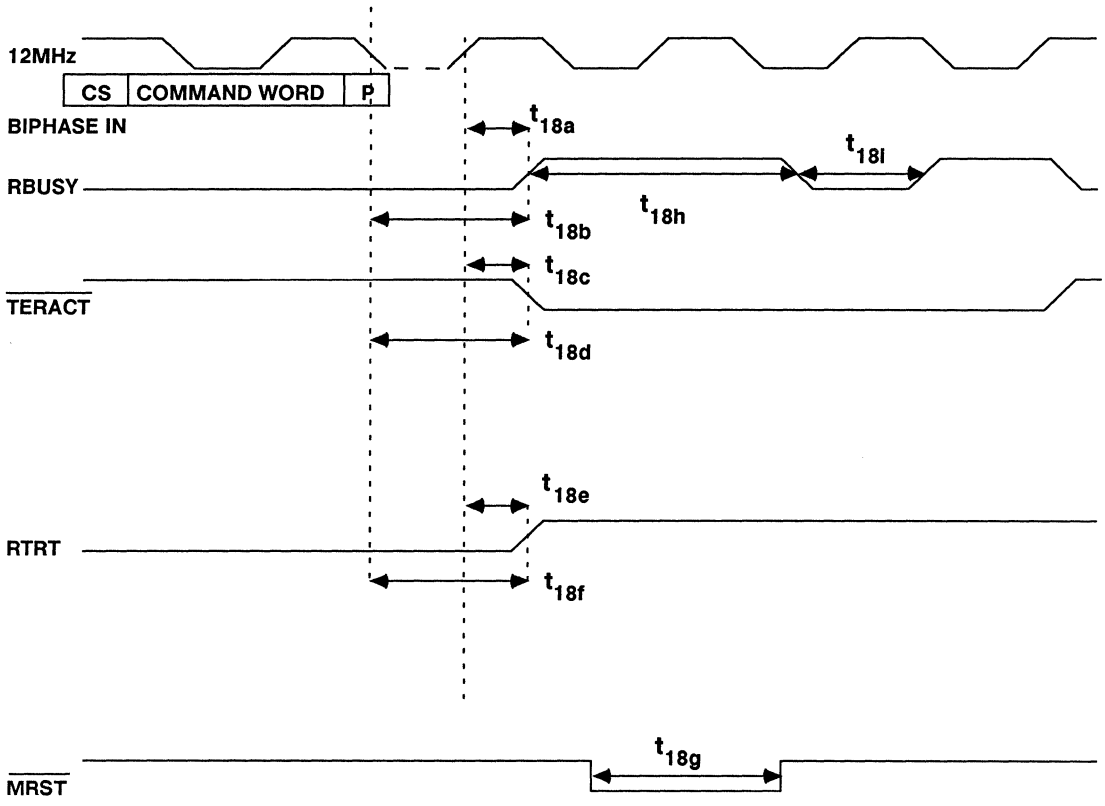


Note:
1. Measured from the mid-bit parity crossing.

Figure 17. Status Output Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t17a (4)	12MHz ↑ to $\overline{MC}$/SA Valid	0	14	ns
t17b	Command Word to $\overline{MC}$/SA Valid (3)	2.1	2.8	µs
t17c (4)	12MHz ↑ to $\overline{COMSTR}$ ↓	0	17	ns
t17d	Command Word to $\overline{COMSTR}$ ↓ (3)	3.2	3.7	µs
t17e (4)	12MHz ↑ to $\overline{BRDCST}$ ↓	0	32	ns
t17f	Command Word to $\overline{BRDCST}$ ↓ (3)	2.6	3.2	µs
t17g (4)	12MHz ↑ to T/$\overline{R}$ Valid	0	57	ns
t17h	Command Word to T/$\overline{R}$ Valid (3)	2.2	2.7	µs
t17l (4)	12MHz ↑ to VALMSG ↑	0	32	ns
t17j	Command Word to VALMSG ↑ (1,2,3)	6.2	6.7	µs
t17k (4)	12MHz ↑ to MERR ↑	0	37	ns
t17l	$\overline{COMSTR}$ ↓ to $\overline{COMSTR}$ ↑	485	500	ns

Notes:
1. Receive last data word to Valid Message active (VALMSG↑).
2. Transmit command word to Valid Message active (VALMSG ↑).
3. Command word measured from mid-bit crossing.
4. Guaranteed by test.

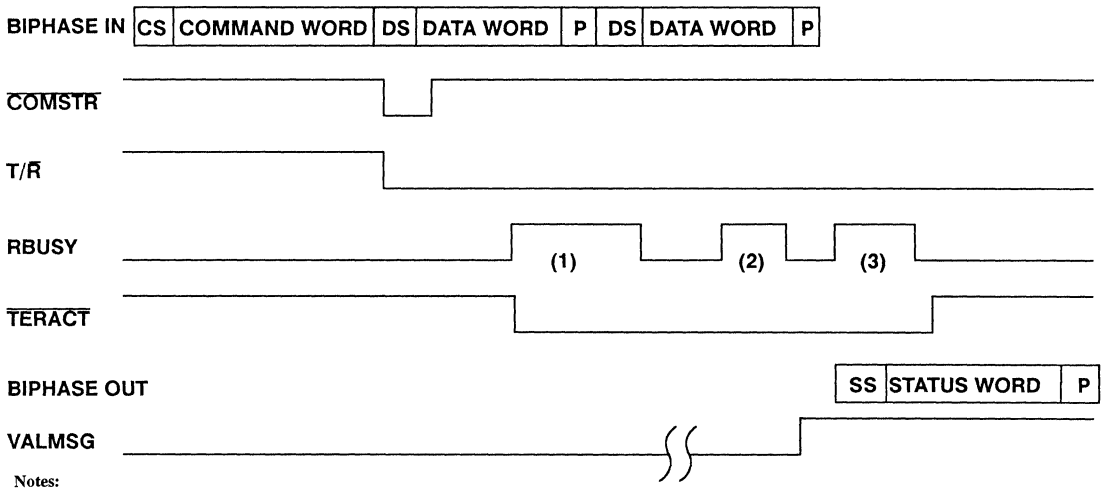


Note:
1. Measured from mid-bit parity crossing.

Figure 18. Status Output Timing

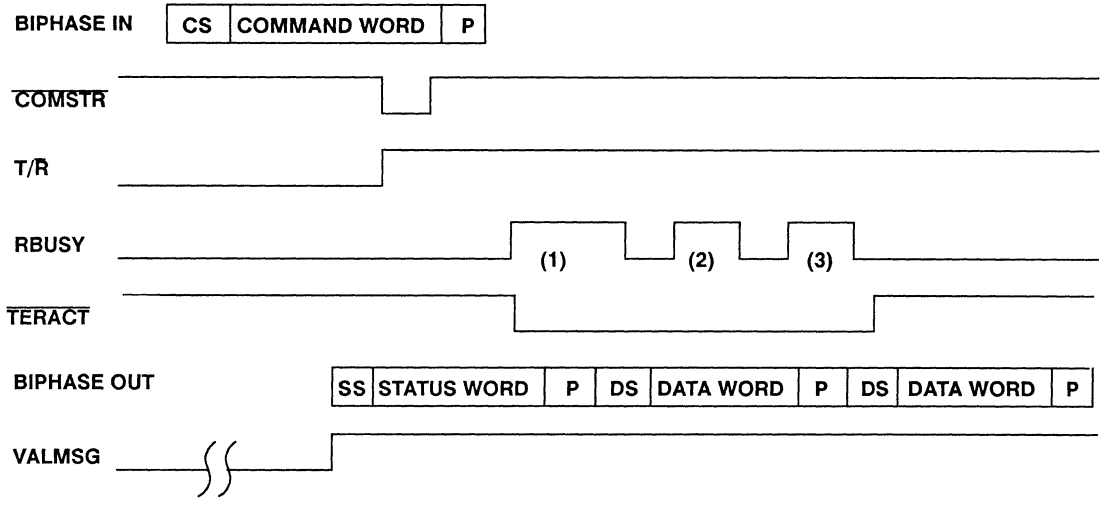
SYMBOL	PARAMETER	MIN	MAX	UNITS
t18a	12MHz ↑ to RBUSY ↑	--	37	ns
t18b	Command Word to RBUSY ↑ (3)	3.2	3.8	µs
t18c (2)	12MHz ↑ to $\overline{\text{TERACT}}$ ↓	0	37	ns
t18d	Command Word to $\overline{\text{TERACT}}$ ↓ (1, 3)	3.1	3.7	µs
t18e (2)	12MHz ↑ to RTRT ↑	0	32	ns
t18f	Command Word to RTRT ↑ (3)	21	22	µs
t18g	$\overline{\text{MRST}}$ ↓ to $\overline{\text{MRST}}$ ↑	500	--	ns
t18h	RBUSY ↑ to RBUSY ↓ (2.7 µs) (5.7 µs)	-- --	5.5 8.5	µs µs
t18i	RBUSY ↓ to RBUSY ↑ (2.7 µs) (5.7 µs)	3.10 240	-- --	µs ns

Notes:
1. $\overline{\text{TERACT}}$ enabled via Control Register.
2. Guaranteed by test.
3. Command word measured from mid-bit crossing.



Notes:
1. Burst of 5 DMAs: read command pointer, store command word, update command pointer, read data word pointer, store command word.
2. Burst of 1 DMA: store data word.
3. Burst of 2 DMAs: store data word, update data word pointer.
4. Approximately 560 ns per DMA access.

Figure 19a. Receive Command with Two Data Words



CS = Command sync
SS = Status sync
DS = Data sync
P = Parity

Notes:
1. Burst of 4 DMAs: read command pointer, store command word, update command pointer, read data word pointer.
2. Burst of 1 DMA: read data word.
3. Burst of 2 DMAs: read data word, update data word pointer.
4. Approximately 560 ns per DMA access.

Figure 19b. Transmit Command with Two Data Words

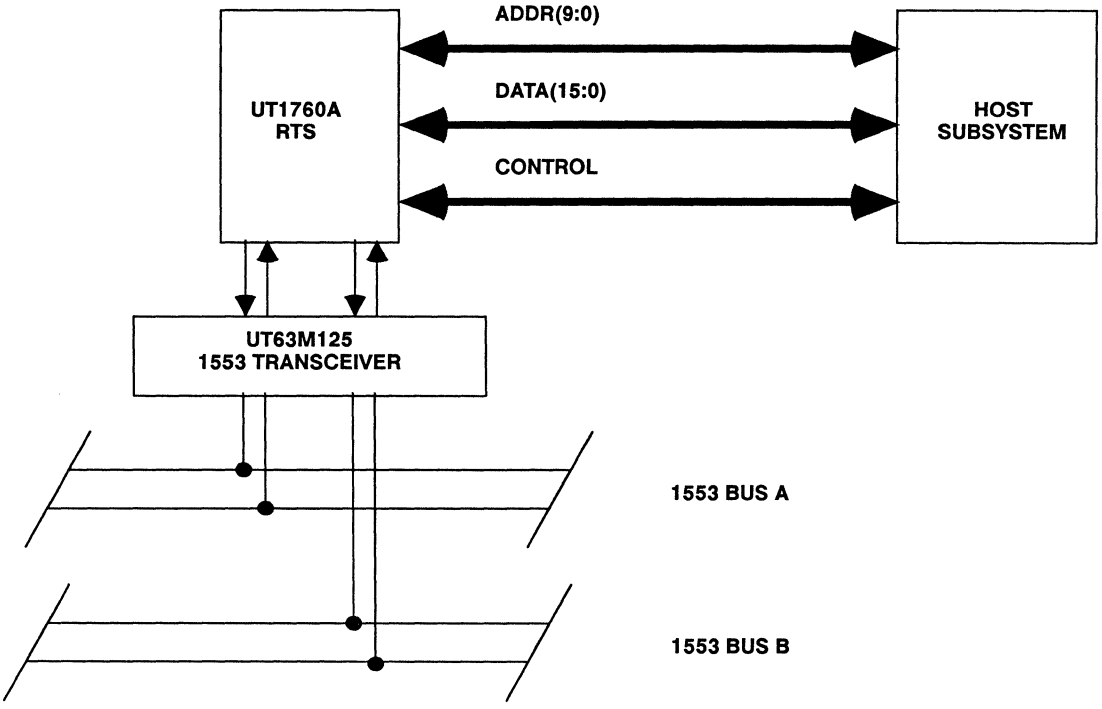


Figure 20a. RTS General System Diagram (Idle low interface)

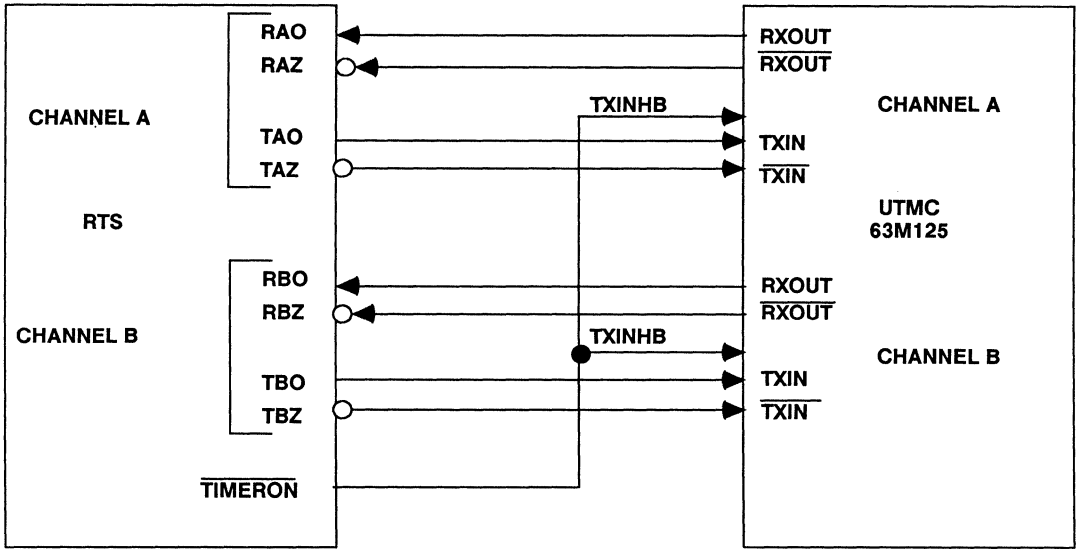
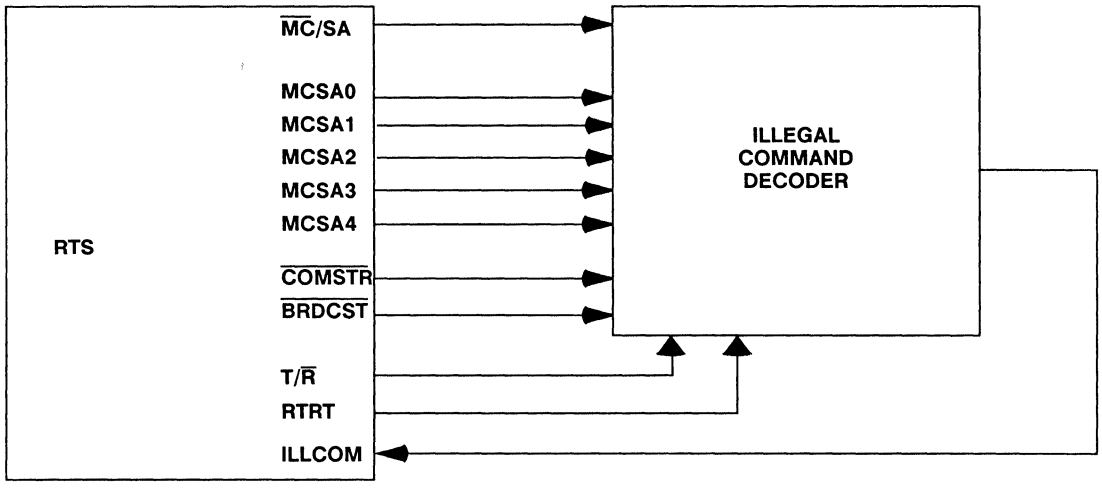


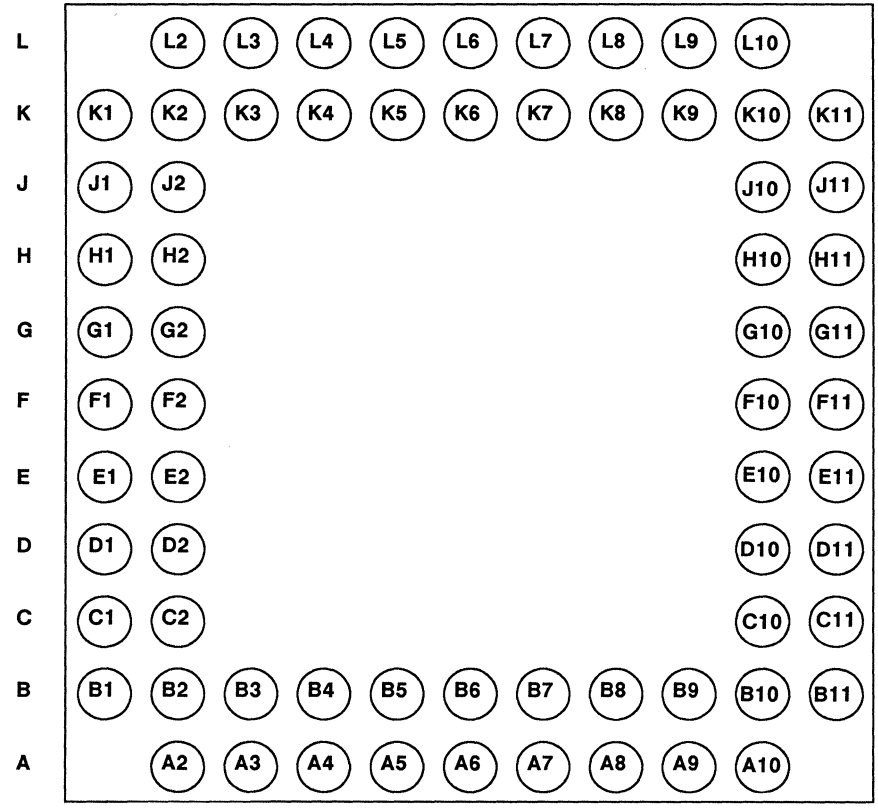
Figure 20b. RTS Transceiver Interface Diagram



3

Figure 21. Mode Code/Subaddress Illegalization Circuit

7.0 Package Outline Drawings



A2 MCSA1
A3 MCSA2
A4 MCSA4
A5 MERR
A6 TERACT or DSCNCT
A7 BRDCST
A8 2MHz
A9 TBZ
A10 TAZ

B1 MC/SA
B2 MCSA0
B3 MCSA3
B4 T/R
B5 TXERR
B6 TIMERON
B7 RTRT
B8 COMSTR
B9 TBO
B10 TAO
B11 DATA15

C1 ADDR9
C2 RBUSY
C10 DATA13
C11 DATA14

D1 ADDR7
D2 ADDR8
D10 DATA11
D11 DATA12

E1 VDD
E2 ADDR6
E10 DATA9
E11 DATA10

F1 ADDR5
F2 VSS
F10 VDD
F11 DATA8

G1 ADDR3
G2 ADDR4
G10 DATA7
G11 VSS

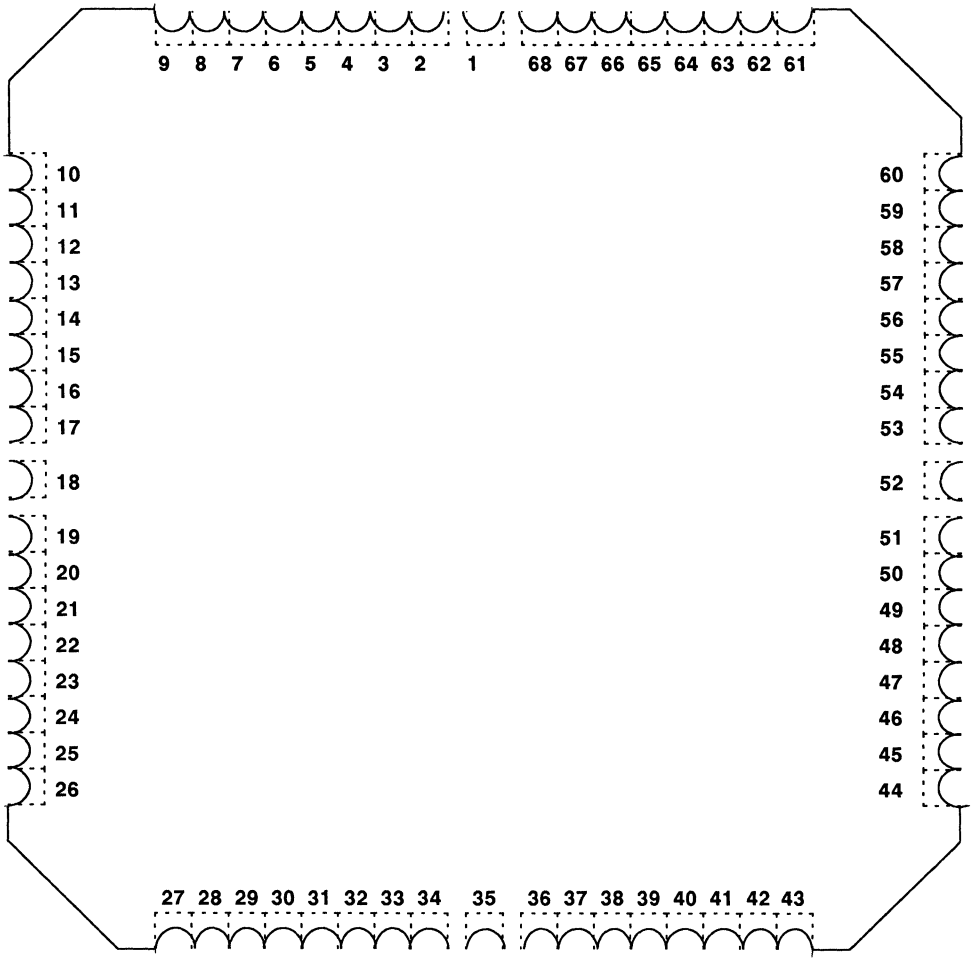
H1 ADDR1
H2 ADDR2
H10 DATA5
H11 DATA6

J1 CTRL
J2 ADDR0
J10 DATA3
J11 DATA4

K1 RD/WR
K2 CS
K3 MRST
K4 RTA3
K5 RTA1
K6 RTPTY
K7 RBO
K8 RAO
K9 ILLCOM
K10 DATA1
K11 DATA2

L2 12MHz
L3 RTA4
L4 RTA2
L5 RTA0
L6 RBZ
L7 RAZ
L8 VALMSG
L9 OE
L10 DATA0

Figure 22a. UT1760A RTS Pingrid Array Configuration (Bottom View)



1	V_{SS}	15	RTA2	29	DATA3	43	DATA15	56	T/$\overline{R}$
2	ADDR5	16	RTA1	30	DATA4	44	TAO	57	MCSA4
3	ADDR4	17	RTA0	31	DATA5	45	TAZ	58	MCSA3
4	ADDR3	18	RTPTY	32	DATA6	46	TBO	59	MCSA2
5	ADDR2	19	RBZ	33	DATA7	47	$\overline{TBZ}$	60	MCSA1
6	ADDR1	20	RBO	34	V_{SS}	48	$\overline{COMSTR}$	61	MCSA0
7	ADDR0	21	RAZ	35	V_{DD}	49	2MHz	62	$\overline{MC}$/SA
8	$\overline{CTRL}$	22	RAO	36	DATA8	50	$\overline{RTRT}$	63	RBUSY
9	RD/$\overline{WR}$	23	VALMSG	37	DATA9	51	$\overline{BRDCST}$	64	ADDR9
10	$\overline{CS}$	24	ILLCOM	38	DATA10	52	$\overline{TIMERON}$	65	ADDR8
11	12MHz	25	$\overline{OE}$	39	DATA11	53	$\overline{TERACT}$ or	66	ADDR7
12	$\overline{MRST}$	26	DATA0	40	DATA12		DSCNCT	67	ADDR6
13	RTA4	27	DATA1	41	DATA13	54	TXERR	68	V_{DD}
14	RTA3	28	DATA2	42	DATA14	55	MERR		

Figure 22b. UT1760A RTS Chip Carrier Configuration (Top View)

UT1553B RTI Remote Terminal Interface

FEATURES

- ☐ Complete MIL-STD-1553B Remote Terminal interface compliance
- ☐ Dual-redundant data bus operation supported
- ☐ Internal illegalization of selected mode code commands
- ☐ External illegal command definition capability
- ☐ Automatic DMA control and address generation
- ☐ Operational status available via dedicated lines or internal status register
- ☐ ASD/ENASC (formerly SEAFAC) tested and approved
- ☐ Available in ceramic 84-lead leadless chip carrier and 84-pin pingrid array
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ☐ JAN-qualified devices available

3

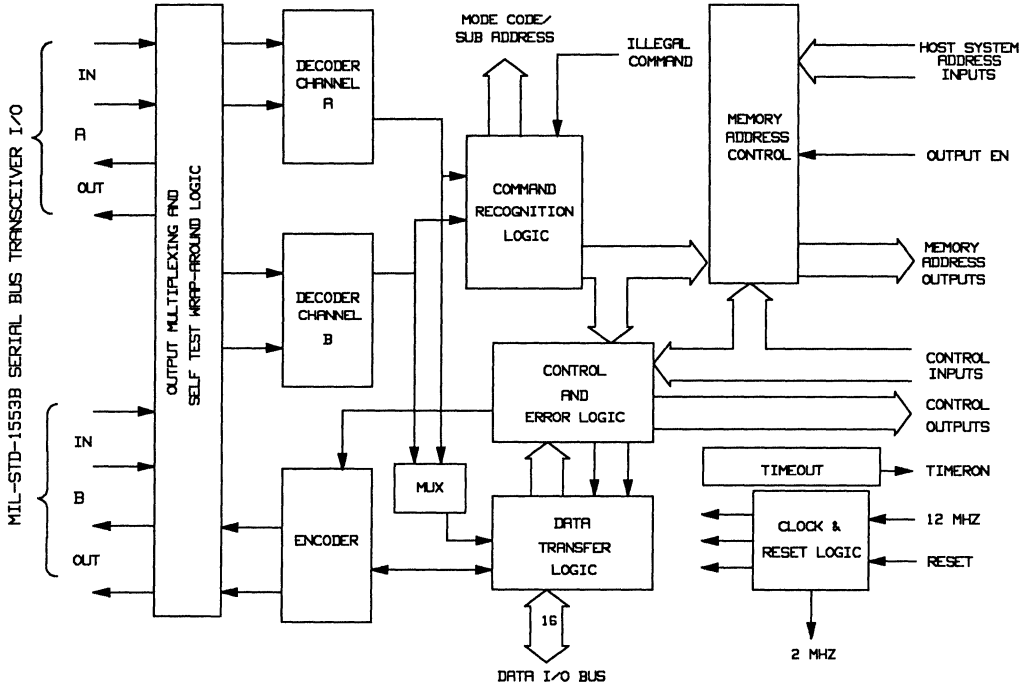


Figure 1. UT1553B RTI Functional Block Diagram

Table of Contents

1.0 Architecture And Operation

The UT1553B RTI is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system. The RTI's MIL-STD-1553B interface includes encoding/decoding logic, error detection, command recognition, memory address control, clock, and reset circuits.

Decoders
The UT1553B RTI contains two separate free-running decoders to insure that all redundancy requirements of MIL-STD-1553B are met. Each decoder receives, decodes, and verifies biphase Manchester II data. Proper frequency and edge skew are also verified.

Command Recognition Logic
The command recognition logic monitors the output of both decoders at all times. Recognition of a valid command causes a reset of present interface activity followed by execution of the command. This procedure meets the requirement for superseding valid commands.

Encoder
The encoder receives serial data from the data transfer logic, converts it to Manchester II form with proper synchronization and parity, and passes it to the output and self-test logic.

Data Transfer Logic
The data transfer logic provides double-buffered 16-bit parallel-to-serial and serial-to-parallel conversion during reception and transmission of data.

Memory Address Control
The memory address control logic controls the output of the three-state address lines during memory access. In DMA system implementations, the memory address control provides RTI-generated addresses. In a pseudo-dual-port memory configuration, the memory address control logic provides either RTI-generated or host system addressing.

Control and Error Logic
The control and error logic performs the following four major functions:

- Interface control for proper processing of MIL-STD-1553B commands
- Error checking of both MIL-STD-1553B data and RTI operation
- Memory control (DMA or pseudo-dual-port) for proper data transfer
- Operational status and control signal generation

Output Multiplexing and Self-Test Logic
This logic directs the output of the encoder to one of four places:

- Channel A outputs
- Channel B outputs
- Channel A decoders during self-test
- Channel B decoders during self-test

Clock and Reset Logic
The UT1553B RTI requires a 12 MHz input clock to operate properly. The RTI provides a 2 MHz output for the system designer to use. The device provides a hardware reset pin as well as software-generated reset.

Timer Logic
The UT1553B RTI has a built-in 730-microsecond timer that is activated when the encoder is about to transmit. The timer is reset upon receipt of a valid command, master reset, or a time-out condition.

3

1.1 HOST INTERFACE

Configure the RTI into the host system for either a direct memory or transparent memory access. The following sections discuss the system configuration for each method of memory management.

1.1.1 Direct Memory Access
In the direct memory access configuration the RTI and host arbitrate for the shared 2K x 16 memory space. To request access to memory the RTI asserts direct memory request output (DMARQ); the system bus arbiter grants the RTI access to memory by asserting the direct memory access grant signal ($\overline{\text{MEMCK}}$). The system arbiter should not assert the $\overline{\text{MEMCK}}$ signal before the RTI has requested access to memory (i.e., DMARQ asserted).

Once granted access to memory, the RTI address out (ADDR OUT(10:0)), RAM chip select ($\overline{\text{RCS}}$), RAM read/write (RRD/$\overline{\text{RWR}}$), and Data bus (DATA I/O(15:0)) provide the interface signals to control the memory access. Figure 2 shows an example of a direct memory access system configuration; for clarity the interface buffers and logic are excluded. The host microprocessor also gains access to memory by arbitration.

Take care to insure that bus contention does not occur between the host and RTI Address buses or memory control signals. To place the RTI Address Out bus in a high impedance state negate the $\overline{\text{ADOEN}}$ input pin. Also note that outputs $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ are not three-state outputs. When the RTI is not writing to memory, bidirectional Data bus DATA I/O(15:0) is an input (i.e., not actively driving the bus).

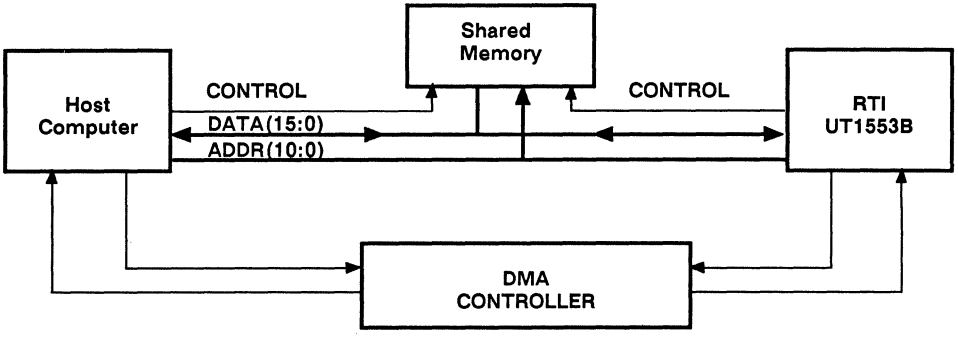


Figure 2. Direct Memory Access Configuration

The host microprocessor gains access to the RTI internal registers by controlling input pins $\overline{CS}$, $\overline{CTRL}$, ADDR IN (10:0), and RD/$\overline{WR}$. During message processing the host microprocessor should limit access to RTI internal registers.

1.1.2 Transparent Memory Access

Configured in the transparent memory mode the host microprocessor accesses shared memory through the RTI. Arbitration for access to the bus is performed as discussed in section 1.1.1 of this document.

When granted access to memory, the RTI asserts memory control signals ADDR OUT(10:0), $\overline{RCS}$, and RRD/$\overline{RWR}$. For host-controlled memory accesses the RAM memory address from the host is propagated from the Address In bus ADDR IN (10:0) to the Address Out bus ADDR OUT (10:0). Memory control signals RD/$\overline{WR}$ and $\overline{CS}$ are also propagated through the RTI as RRD/$\overline{RWR}$ and $\overline{RCS}$. Input $\overline{CTRL}$ is negated during all transparent memory accesses to prevent the RTI from inadvertently performing an internal register access or software reset. While $\overline{CS}$ is asserted, the RTI's bidirectional Data bus DATA I/O (15:0) is an input (i.e., not actively driving bus).

The host microprocessor gains access to the RTI internal registers by controlling input pins $\overline{CS}$, $\overline{CTRL}$, ADDR IN (10:0), and RD/$\overline{WR}$. During message processing the host microprocessor should limit access to RTI internal registers. The host should not assert $\overline{CS}$ while the RTI is performing a memory access.

1.2 Internal Register Description

The RTI uses three internal registers to allow the host to control the RTI operation and monitor its status. The host uses the following inputs Control ($\overline{CTRL}$), Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and ADDR IN (0) to read the 16-bit System Register or write to the 8-bit Control Register. The Control Register toggles bits in the MIL-STD-1553B status word, enables biphase inputs, selects terminal active flag, and puts the part in self-test. The System Register supplies operational status of the UT1553B RTI to the host. The Last Command Register saves the command word for a Transmit Last Command mode code, along with operational status from the System Register.

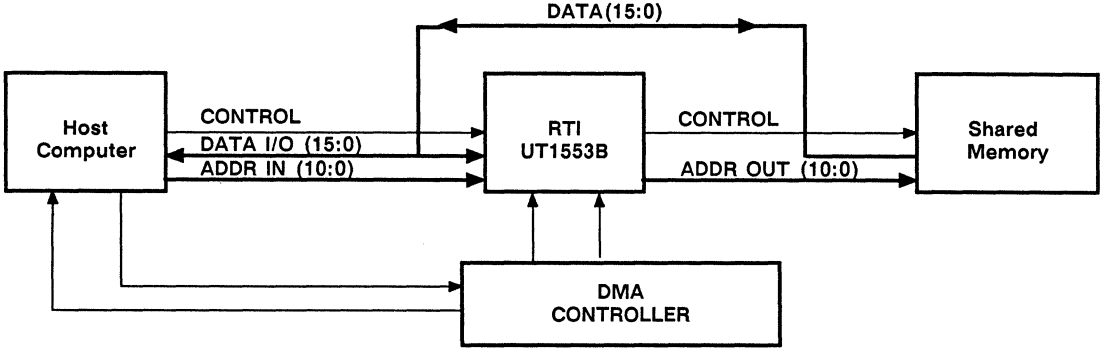


Figure 3. Transparent Memory Access Configuration

Control Register (Write Only)
The 8-bit write-only Control Register manages the operation of the RTI. Write to the Control Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, RD/$\overline{WR}$, and ADDR IN (0); if ADDR IN (0) is a logic one a master reset occurs. Data is loaded into the Control Register via I/O pins DATA(7:0). Control Register writes must occur 50 ns before the rising edge of $\overline{COMSTR}$ to latch data in the outgoing status word.

Bit Number	Initial Condition	Description
0	[0]	Channel A Enable. A logic one enables Channel A biphase inputs.
1	[0]	Channel B Enable. A logic one enables Channel B biphase inputs.
2	[0]	Terminal Flag. A logic one sets the Terminal Flag bit of the Status Register.
3	[0]	System Busy. A logic one sets the Busy bit of the System Register and inhibits RTI access to memory. No data words are retrieved or stored; command word is stored.
4	[0]	Subsystem Busy. A logic one sets the Subsystem Flag bit of the Status Register.
5	[0]	Self-Test Channel Select. This bit selects which channel the internal self-test checks; a logic one selects Channel A and a logic zero selects Channel B.
6	[0]	Self-Test Enable. A logic one sets the RTI in the internal self-test mode and inhibits normal operation. Internal testing is not visible on biphase output channels.
7	[0]	Service Request. A logic one sets the Service Request bit of the Status Register.

CONTROL REGISTER (WRITE ONLY)

X	X	X	X	X	X	X	X	SRV RQ	SELF TEST	SELF CH	SUBS	BUSY	TF	CH B EN	CH A EN
								[0]	[0]	[0]	[0]	[0]	[0]	[0]	[0]

MSB **LSB**
[ ] defines reset state

Figure 4. Control Register

System Register (Read Only)
The 16-bit read-only System Register provides the RTI system status. Read the System Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, ADDR IN (0), and a logic one to RD/$\overline{WR}$. The 16-bit contents of the System Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
0	[0]	MCSA(0). The LSB of the mode code or subaddress as indicated by the logic state of bit 5.
1	[0]	MCSA(1). Mode code or subaddress as indicated by the state of bit 5.
2	[0]	MCSA(2). Mode code or subaddress as indicated by the state of bit 5.
3	[0]	MCSA(3). Mode code or subaddress as indicated by the state of bit 5.
4	[0]	MCSA(4). Mode code or subaddress as indicated by the state of bit 5.
5	[0]	$\overline{MC}$/SA. A logic one indicates that bits 4 through 0 are the subaddress of the last command word, and that the last command word was a normal transmit or receive command. A logic zero indicates that bits 4 through 0 are a mode code, and that the last command was a mode code.
6	[1]	Channel A/$\overline{B}$. A logic one indicates that the most recent command arrived on Channel A; a logic zero indicates that it arrived on Channel B.

7	[0]	Channel B Enabled. A logic one indicates that Channel B is available for both reception and transmission.
8	[0]	Channel A Enabled. A logic one indicates that Channel A is available for both reception and transmission.
9	[1]	Terminal Flag Enabled. A logic one indicates that the Bus Controller has not issued an Inhibit Terminal Flag mode code. A logic zero indicates that the Bus Controller, via the above mode code, is overriding the host system's ability to set the Terminal Flag bit of the status word.
10	[0]	Busy. A logic one indicates the Busy bit is set. This bit is reset when the System Busy bit in the Control Register is reset.
11	[0]	Self-Test. A logic one indicates that the RTI is in the self-test mode. This bit is reset when the self-test is terminated.
12	[0]	TA Parity Error. A logic one indicates the wrong Terminal Address parity; it causes the biphase inputs to be disabled and a message error condition. This bit is reset by reloading the terminal address latch with correct parity.
13	[0]	Message Error. A logic one indicates that a message error has occurred since the last System Register read. This bit is not reset until the System Register has been examined and the message error condition is removed.
14	[0]	Valid Message. A logic one indicates that a valid message has been received since the last System Register read. This bit is not reset until the System Register has been examined.
15	[0]	Terminal Active. A logic one indicates the device is executing a transmit or receive operation. The state of this bit is the logical NAND of the external $\overline{XMIT}$ and $\overline{RCV}$ pins.

SYSTEM REGISTER (READ ONLY)

TERM ACTV	VAL MESS	MESS ERR	TAPA ERR	SELF-TEST	BUSY	TFEN	CH A EN	CH B EN	CHNL A/B	$\overline{MC}$/SA	MCSA 4	MCSA 3	MCSA 2	MCSA 1	MCSA 0
[0]	[0]	[0]	[0]	[0]	[0]	[1]	[0]	[0]	[1]	[0]	[0]	[0]	[0]	[0]	[0]

MSB **LSB**

[ ] defines reset state

Figure 5. System Registers

Last Command Register (Read Only)

The 16-bit read-only Last Command Register provides the host with last command and operational status information. The RTI transmits the lower 11 bits of this register along with terminal address upon receipt of a Transmit Last Command mode code. Read the Last Command Register by applying a logic zero to $\overline{CS}$, $\overline{CTRL}$, and a logic one to RD/$\overline{WR}$ and ADDR IN (0). The 16-bit contents of the Last Command Register are read from data I/O pins DATA(15:0).

Bit Number	Initial Condition	Description
0 through 10	[all 0]	Least significant 11 bits of the last command word.
11	[0]	Busy Bit. System Register bit 10.
12	[0]	Self-test. System Register bit 11.
13	[1]	Terminal Flag Enabled. System Register bit 9.
14	[1]	Channel A/$\overline{B}$. System Register bit 6.
15	[1]	Illegal Command. The RTI illegalized the last command.

1.3 Mode Codes and Subaddresses

The UT1553B RTI provides subaddress and mode code decoding meeting MIL-STD-1553B. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Upon command word validation and decode, status pins MCSA(4:0) and $\overline{MC}$/SA become valid. Status pin $\overline{MC}$/SA will indicate whether the data pins MCSA(4:0) are mode code or subaddress information. Status Register bits 5 through 0 contain the same information as pins MCSA(4:0) and $\overline{MC}$/SA.

The system designer can use signals MCSA(4:0), $\overline{MC}$/SA, $\overline{BRDCST}$, $\overline{XMIT}$, and $\overline{RCV}$ to illegalize mode codes, subaddresses, and other message formats via the Illegal Command (ILL COMM) input (see figure 23 on page 36).

The RTI will internally decode the following mode codes as illegal:

- Dynamic Bus Control
- Selected Transmitter Shutdown
- Override Selected Transmitter Shutdown
- All Reserved Mode Codes

If the RTI receives one of the above mode codes, the RTI responds by transmitting a status word with the Message Error bit set to logic one.

Mode codes which involve data transfer are processed like receive and transmit commands. The RTI will not generate DMA request for Transmit Status Word and Transmit Last Command mode codes since the information is stored internal to the RTI.

The following mode codes require assistance from the host:

- Synchronize
- Initiate Self-Test
- Reset Remote Terminal

For example, the RTI will accept and respond to a Reset Remote Terminal mode code; however it will not perform a reset operation. The host must interpret the mode code and take appropriate action.

The RTI does not define or interpret the following data words associated with mode code commands:

- Transmit Vector Word
- Synchronize With Data Word
- Transmit Bit Word

The RTI will accept and respond to mode code with data; the host must interpret or define the data word. The RTI will store or retrieve the data required for mode code command from block #1 of the receive or transmit page.

RTI MODE CODE HANDLING PROCEDURE

T/$\overline{R}$	Mode Code	Function	Operation
0	10100	Selected Transmitter Shutdown (2)	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
0	10101	Override Selected Transmitter Shutdown (2)	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
0	10001	Synchronize (w/data)	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control (2)	1. Command word stored 2. MES ERR pin asserted 3. Message error latch set in System Register 4. Status word transmitted
1	00001	Synchronize (1)	1. Command word stored 2. Status word transmitted
1	00010	Transmit Status Word (3)	1. Command word stored 2. Status word transmitted
1	00011	Initiate Self-Test (1)	1. Command word stored 2. Status word transmitted
1	00100	Transmitter Shutdown	1. Command word stored 2. Alternate bus shutdown 3. Status word transmitted
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Alternate bus enabled 3. Status word transmitted
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit set to zero and disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit enabled, but not set to logic one 3. Status word transmitted
1	01000	Reset Remote Terminal (1)	1. Command word stored 2. Status word transmitted
1	10010	Transmit Last Command Word (3)	1. Status word transmitted 2. Last command word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Notes:
1. Further host interaction required for mode code operation.
2. Reserved mode code; A) MES ERR pin asserted, B) Message Error bit set, C) status word transmitted (ME bit set to logic one).
3. Status word not affected.

1.4 MIL-STD-1553B Subaddress and Mode Code Definitions

Table 1. Subaddress and Mode Code Definitions Per MIL-STD-1553B

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	(1)	(1)	Mode Code Indicator
00001 (01)	User Defined	User Defined	
00010 (02)	User Defined	User Defined	
00011 (03)	User Defined	User Defined	
00100 (04)	User Defined	User Defined	
00101 (05)	User Defined	User Defined	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	User Defined	User Defined	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	User Defined	User Defined	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	User Defined	User Defined	
01111 (15)	User Defined	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	User Defined	User Defined	
10100 (20)	User Defined	User Defined	
10101 (21)	User Defined	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	User Defined	User Defined	
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	(1)	(1)	Mode Code Indicator

Note:
1. Refer to mode code assignments per MIL-STD-1553B.

1.5 Remote Terminal Address

Assign the RTI remote terminal address by either a software or hardware exercise. The host assigns the RTI remote terminal address by performing a Control Register write; the Terminal Address bus (TA(4:0)) is strobed into the RTI Remote Terminal Address Register upon completion of the Control Register write. To assign the RTI remote terminal address via hardware, use the $\overline{\text{TALEN}}$/PARITY input pin operating in the terminal latch address enable mode. The Terminal Address bus is latched into the RTI while the $\overline{\text{TALEN}}$ is asserted (i.e., logic low). Valid remote terminal addresses (RTA) include decimal 0 through 31 if Broadcast is disabled, 0 through 30 if Broadcast is enabled.

Parity Checker

An address parity check is performed to insure the remote terminal address applied to TA(4:0) was properly latched into the Remote Terminal Address Register. To perform a parity check, enable the RTI parity circuit via EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ input pins. The parity bit is entered through the $\overline{\text{TALEN}}$/PARITY input pin operating in the parity mode. Input pins EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ control dual-function input pin $\overline{\text{TALEN}}$/PARITY; see table 2 for description of operation.

If a parity error exists, the Parity Error bit of the System Register is set to a logic one, biphase Channels A and B are disabled (set to logic zero), the Message Error bit set to logic one, and the message error pin is asserted.

Table 2. Parity Checking

STATE #	EXT TEST	EXT TST CH SEL A/$\overline{B}$	Function of $\overline{TALEN}$/PARITY
0	0	0	Terminal Address Latch Enable. Active low signal used to latch TA(4:0) into RTI. Internal parity checker disabled.
1	0	1	Parity. Internal remote terminal address parity checker enabled. $\overline{TALEN}$/PARITY pin functions as parity bit for TA(4:0) bus. Proper operation requires odd parity.
2	1	0	Terminal Address Latch Enable. Do not assert EXT TST during reset, otherwise self-test is invoked.
3	1	1	Terminal Address Latch Enable. Do not assert EXT TST during reset, otherwise self-test is invoked.

The following are examples of sequences used to enter remote terminal addresses into the RTI.

Example 1. Hardware-Controlled Remote Terminal Address (parity check disabled):

EXT TEST and EXT TST CH SEL A/$\overline{B}$ in
STATE 0, 2, or 3 (i.e., 00, 10, or 11)
$\overline{TALEN}$ - asserted (i.e., logic low)
TA(4:0) - valid RTA

Example 2. Software-Controlled Remote Terminal Address (parity check disabled):

EXT TEST and EXT TST CH SEL A/$\overline{B}$ in
STATE 0, 2, or 3 (i.e., 00, 10, or 11)
$\overline{CTRL}$ - logic zero
$\overline{CS}$ - logic zero
RD/$\overline{WR}$ - logic zero
ADDR IN (0) - logic zero
$\overline{TALEN}$ - logic one
TA(4:0) - valid RTA

Example 3. Software Controlled Remote Terminal Address (parity check enabled):

EXT TEST and EXT TST CH SEL A/$\overline{B}$ in
STATE 1 (i.e., 01)
$\overline{CTRL}$ - logic zero
$\overline{CS}$ - logic zero
RD/$\overline{WR}$ - logic zero
ADDR IN (0) - logic zero
PARITY - input must provide odd parity for the TA(4:0) bus
TA(4:0) - valid RTA

For examples 1 and 2, enabling the parity check circuit (STATE 1) after the remote terminal address is stored results in a parity check of the data loaded into the Remote Terminal Address Register.

1.6 Internal Self-Test

Setting bit 6 of the Control Register to a logic one enables the internal self-test. Disable Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The RTI's self-test capability is based on the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the encoder is fed back to the decoder, the RTI will recognize the incoming status word as a command word and thus cause the RTI to transmit another status word. After the host invokes self-test, the RTI self-test logic forces a status word transmission even though the RTI has not received a command word. The status word is sent to decoder A or B depending on the channel the host selected for self-test. The host controls the self-test by periodically changing the bit patterns in the status word being transmitted. Writing to the Control Register bits 2, 3, 4, and 8 changes the status word. Monitor the self-test by sampling either the System Register or the external status pins (i.e. Command Strobe ($\overline{COMSTR}$), Transmit ($\overline{XMIT}$), Receive ($\overline{RCV}$)). For a more detailed explanation of internal self-test, consult the UTMC publication *RTI Internal Self-Test Routine.*

1.7 Power-up Master Reset

Reset the RTI by invoking either a hardware or software master reset after power-up to place the device in a known state. The master reset clears the decoder and encoder registers, the command recognition logic, the control and error logic (which includes the Status, Control and System Registers), the data transfer logic, and the memory address control logic. After reset, configure the device for operation via a Control Register write.

Perform a hardware reset by asserting the $\overline{MRST}$ input pin for a minimum of 500 ns. During reset negate the EXT TEST pin (i.e., logic low); assertion of the EXT TEST pin forces the RTI to enter the external self-test mode of operation.

Software reset the RTI by simultaneously applying a logic zero to input pins $\overline{CS}$, RD/$\overline{WR}$, and $\overline{CTRL}$ while the least significant bit of the address input bus is a logic one (ADDR IN (0)=0).

1.8 Encoder and Decoder

The RTI interfaces directly to a bus transmitter/receiver via the RTI Manchester II encoder/decoder. The UT1553B RTI receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decode checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RTI processes each incoming data word for correct word count and contiguous data. If an invalid message error is detected, the message error pin is asserted, the RTI ceases processing the remainder (if any) of the message, and it then suppresses status word transmission. Upon command validation recognition, the external status outputs are enabled. Reception of illegal commands does not suppress status word transmission.

A timer precludes transmission greater than 730 microseconds by the assertion of fail-safe timer ($\overline{TIMERON}$). This timer is reset upon receipt of another valid command.

1.9 Illegal Command Decoding

The host has the option of asserting the ILL COMM pin to illegalize a received command word. On receipt of an illegal command, the RTI sets the message error bit in the status word, sets the Message Error output, and sets the message error latch in the System Register.

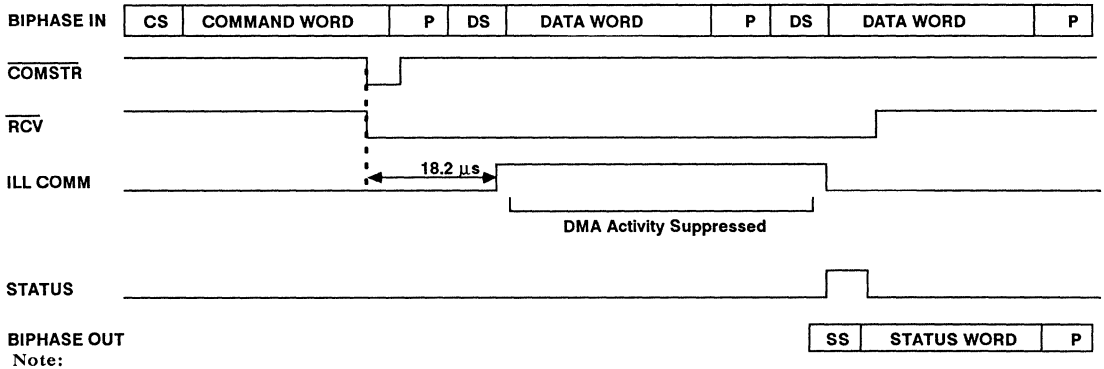
Use the following RTI outputs to externally decode an illegal command, Mode Code or Subaddress indicator ($\overline{MC}$/SA), Mode Code or Subaddress bus MCSA(4:0), Command Strobe ($\overline{COMSTR}$), Broadcast ($\overline{BRDCST}$), etc. (See figure 6 pages 11-12).

To illegalize a transmit command the ILL COMM pin is asserted 3.3 microseconds after STATUS goes to a logic one. Assertion of the ILL COMM pin within 3.3 microseconds allows the RTI to respond with the Message Error bit of the outgoing status word at a logic one.

For an illegal receive command, the ILL COMM pin is asserted within 18.2 microseconds after the $\overline{COMSTR}$ transitions to a logic zero in order to suppress data words from being stored (suppress DMARQ assertions). In addition, the ILL COMM pin must be at a logic one throughout the reception of the message until STATUS is asserted.

If the illegal command is mode code 2, 4, 5, 6, 7, or 18, assert the ILL COMM pin within 664 nanoseconds after Command Strobe ($\overline{COMSTR}$) transitions to logic zero. Asserting the ILL COMM pin within the 664 nanoseconds inhibits the mode code function.

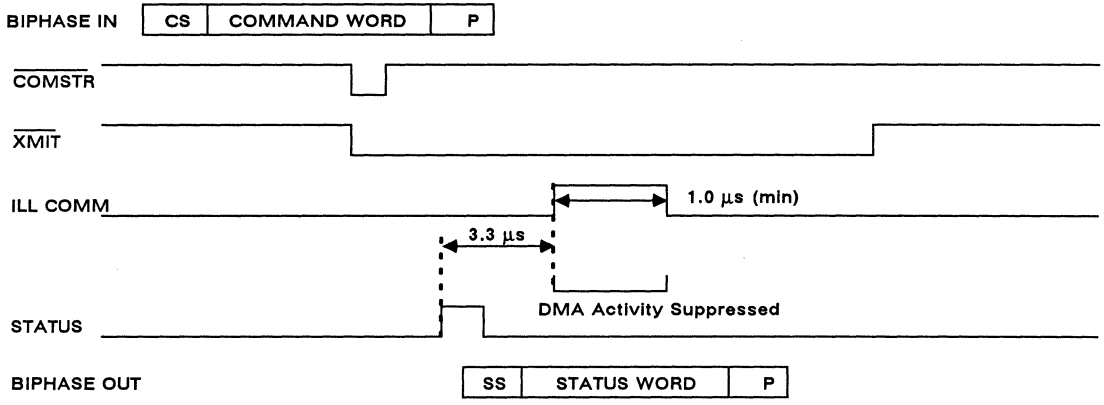
The above timing conditions also apply when the host externally decodes an illegal broadcast command. The host must remove the illegal command condition so that the next command is not falsely decoded as illegal. These requirements are easily met if the $\overline{COMSTR}$ output is used to qualify the ILL COMM input to the RTI.



Note:

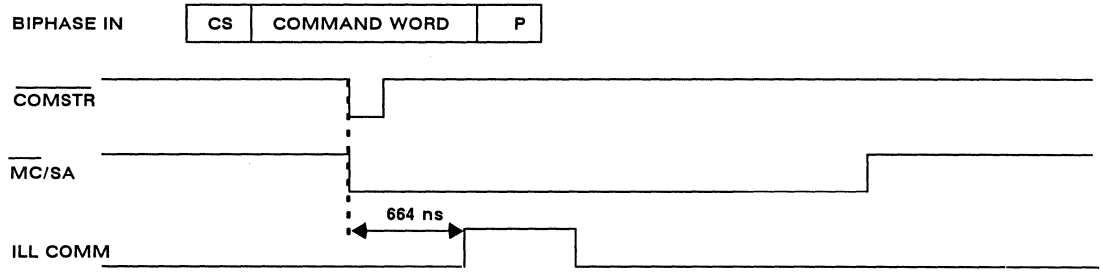
1. Illegal command condition; status word Message Error bit set to logic one, RTI MES ERR pin set to a logic one, RTI Status Register Message Error bit set to logic one.

Figure 6a. Illegal Receive Command Decoding



Note:
1. Illegal command condition; status word Message Error bit set to logic one, RTI MES ERR pin set to a logic one, RTI Status Register Message Error bit set to logic one.

Figure 6b. Illegal Transmit Command Decoding



Note:
1. To illegalize mode codes 2, 4, 5, 6, 7, or 18 assert ILL COMM within 664 ns of $\overline{\text{COMSTR}}$'s transition to logic zero. Asserting the ILL COMM within 664 ns inhibits the mode code function.

Figure 6c. Mode Code Command Decoding

2.0 Memory Map

The RTI is capable of addressing 2048 x 16 of external memory for message storage. The 2K memory space is divided into two 1K pages and subdivided into 32 blocks of 32 x 16:

Page 1 (Receive): 32 blocks for receive messages (32 x 16)

Page 2 (Transmit): 32 blocks for transmit messages (32 x 16)

Address Decode

The RTI derives addresses (i.e. data pointers) for external memory directly from the 11 least significant bits of the command word. The address data pointer corresponds to ADDR OUT (10:0) during RTI memory accesses.

T/$\overline{\text{R}}$ = ADDR OUT (10)
SUBADDRESS/MODE = ADDR OUT (9:5)
WORD COUNT/MODE CODE = ADDR OUT (4:0)

The T/$\overline{\text{R}}$ bit of the command word becomes the most significant bit of the data pointer; the T/$\overline{\text{R}}$ bit serves to divide the RAM into transmit and receive pages of 1K each. The 5-bit subaddress/mode field is used to select 1 of 32 possible message storage blocks within the transmit or receive message page. The 5-bit word count/mode code field acts as a data pointer to select one of 32 locations within the message storage block. Multiple word messages are stored from top to bottom within the message storage block.

For mode commands, the address data pointer always contains 00000 in the $\overline{\text{MC}}$/SA field, regardless of whether 00000 or 11111 was received. Forcing the mode code field to 00000 reserves the first message storage block on both

pages (receive and transmit) for mode code messages that require data. The 5-bit mode code specifies which of the 32 locations within the message storage block to access.

For "wrap-around" applications (transmission of data previously received), force the RTI to store and receive messages on one memory page. To accomplish one-page operation do not use the T/$\overline{R}$ output pin. Eliminating the T/$\overline{R}$ limits the RTI access to only one page and the RTI will not differentiate between receive and transmit pages.

Table 3. RTI Memory Map

1: Receive Memory Map

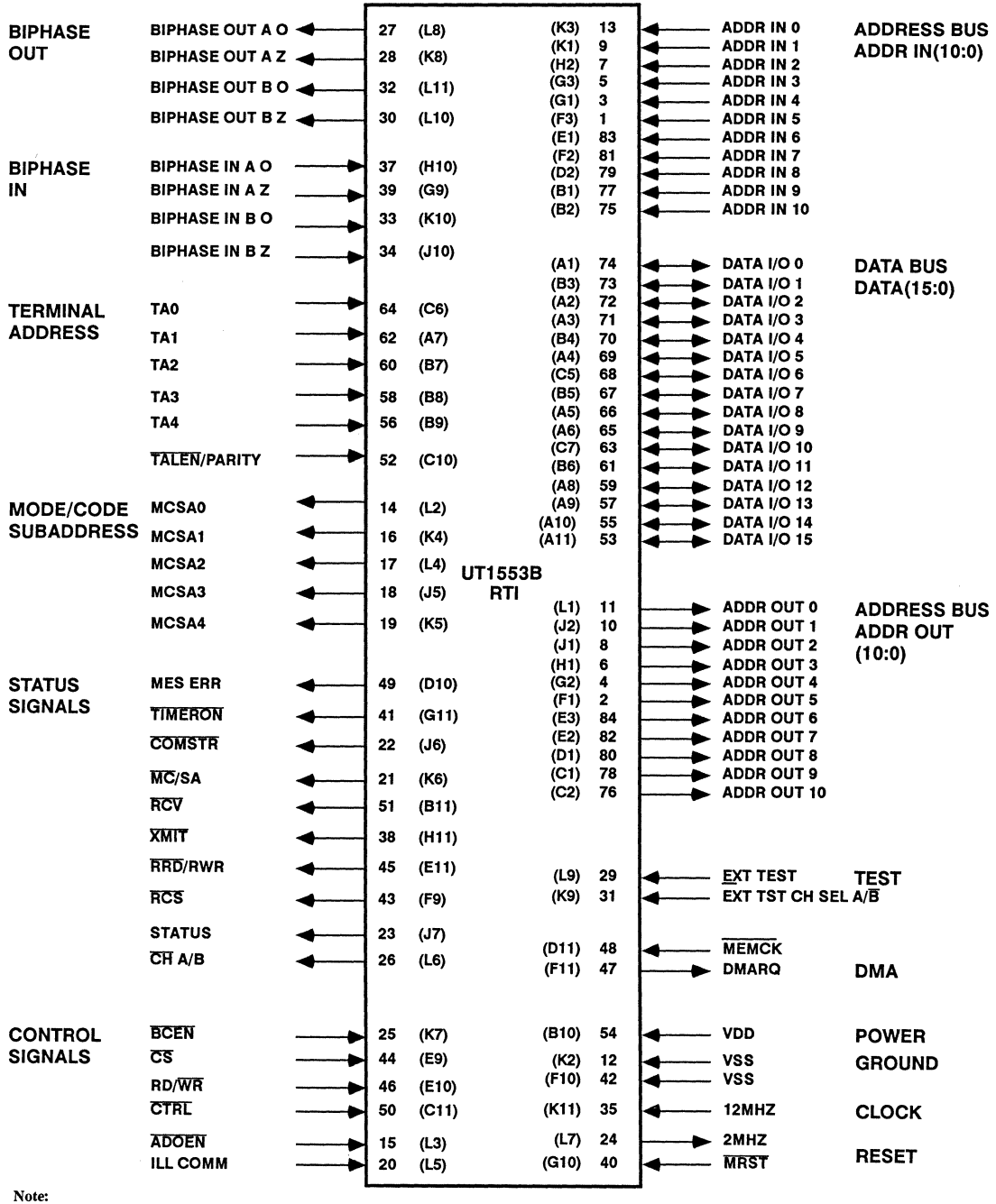
Block #	Operation	Address Field (hex)
1	Mode Code (1)	000 to 01F
2	Subaddress 1	020 to 03F
3	Subaddress 2	040 to 05F
4	Subaddress 3	060 to 07F
5	Subaddress 4	080 to 09F
6	Subaddress 5	0A0 to 0BF
7	Subaddress 6	0C0 to 0DF
8	Subaddress 7	0E0 to 0FF
9	Subaddress 8	100 to 11F
10	Subaddress 9	120 to 13F
11	Subaddress 10	140 to 15F
12	Subaddress 11	160 to 17F
13	Subaddress 12	180 to 19F
14	Subaddress 13	1A0 to 1BF
15	Subaddress 14	1C0 to 1DF
16	Subaddress 15	1E0 to 1FF
17	Subaddress 16	200 to 21F
18	Subaddress 17	220 to 23F
19	Subaddress 18	240 to 25F
20	Subaddress 19	260 to 27F
21	Subaddress 20	280 to 29F
22	Subaddress 21	2A0 to 2BF
23	Subaddress 22	2C0 to 2DF
24	Subaddress 23	2E0 to 2FF
25	Subaddress 24	300 to 31F
26	Subaddress 25	320 to 33F
27	Subaddress 26	340 to 35F
28	Subaddress 27	360 to 37F
29	Subaddress 28	380 to 39F
30	Subaddress 29	3A0 to 3BF
31	Subaddress 30	3C0 to 3DF
32	Unused	3E0 to 3FF

2: Transmit Memory Map

Block #	Operation	Address Field (hex)
1	Mode Code (1)	400 to 41F
2	Subaddress 1	420 to 43F
3	Subaddress 2	440 to 45F
4	Subaddress 3	460 to 47F
5	Subaddress 4	480 to 49F
6	Subaddress 5	4A0 to 4BF
7	Subaddress 6	4C0 to 4DF
8	Subaddress 7	4E0 to 4FF
9	Subaddress 8	500 to 51F
10	Subaddress 9	520 to 53F
11	Subaddress 10	540 to 55F
12	Subaddress 11	560 to 57F
13	Subaddress 12	580 to 59F
14	Subaddress 13	5A0 to 5BF
15	Subaddress 14	5C0 to 5DF
16	Subaddress 15	5E0 to 5FF
17	Subaddress 16	600 to 61F
18	Subaddress 17	620 to 63F
19	Subaddress 18	640 to 65F
20	Subaddress 19	660 to 67F
21	Subaddress 20	680 to 69F
22	Subaddress 21	6A0 to 6BF
23	Subaddress 22	6C0 to 6DF
24	Subaddress 23	6E0 to 6FF
25	Subaddress 24	700 to 71F
26	Subaddress 25	720 to 73F
27	Subaddress 26	740 to 75F
28	Subaddress 27	760 to 77F
29	Subaddress 28	780 to 79F
30	Subaddress 29	7A0 to 7BF
31	Subaddress 30	7C0 to 7DF
32	Unused	7E0 to 7FF

Notes:
1. Receive mode codes with data:
   - Synchronize with data
   - Selected Transmitter Shutdown (Illegal)
   - Override Selected Transmitter Shutdown (Illegal)
2. Transmit mode codes with data:
   - Transmit Vector Word
   - Transmit Bit Word

3.0 Pin Identification And Description



Note:
Pingrid array numbers are in parentheses. LCC pin numbers are not in parentheses.

Figure 7. UT1553B RTI Pin Description

Legend for TYPE and ACTIVE fields:

TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TO = TTL output
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional
[] - Values in parentheses indicate the initialized state of output pin.

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
DATA I/O (15)	53	A11	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
DATA I/O (14)	55	A10	TTB	--	Bit 14 of the bidirectional Data bus.
DATA I/O (13)	57	A9	TTB	--	Bit 13 of the bidirectional Data bus.
DATA I/O (12)	59	A8	TTB	--	Bit 12 of the bidirectional Data bus.
DATA I/O (11)	61	B6	TTB	--	Bit 11 of the bidirectional Data bus.
DATA I/O (10)	63	C7	TTB	--	Bit 10 of the bidirectional Data bus.
DATA I/O (9)	65	A6	TTB	--	Bit 9 of the bidirectional Data bus.
DATA I/O (8)	66	A5	TTB	--	Bit 8 of the bidirectional Data bus.
DATA I/O (7)	67	B5	TTB	--	Bit 7 of the bidirectional Data bus.
DATA I/O (6)	68	C5	TTB	--	Bit 6 of the bidirectional Data bus.
DATA I/O (5)	69	A4	TTB	--	Bit 5 of the bidirectional Data bus.
DATA I/O (4)	70	B4	TTB	--	Bit 4 of the bidirectional Data bus.
DATA I/O (3)	71	A3	TTB	--	Bit 3 of the bidirectional Data bus.
DATA I/O (2)	72	A2	TTB	--	Bit 2 of the bidirectional Data bus.
DATA I/O (1)	73	B3	TTB	--	Bit 1 of the bidirectional Data bus.
DATA I/O (0)	74	A1	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

INPUT ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR IN (10)	75	B2	TI	--	Bit 10 (MSB) of the Address Input bus.
ADDR IN (9)	77	B1	TI	--	Bit 9 of the Address Input bus.
ADDR IN (8)	79	D2	TI	--	Bit 8 of the Address Input bus.
ADDR IN (7)	81	F2	TI	--	Bit 7 of the Address Input bus.
ADDR IN (6)	83	E1	TI	--	Bit 6 of the Address Input bus.
ADDR IN (5)	1	F3	TI	--	Bit 5 of the Address Input bus.
ADDR IN (4)	3	G1	TI	--	Bit 4 of the Address Input bus.
ADDR IN (3)	5	G3	TI	--	Bit 3 of the Address Input bus.
ADDR IN (2)	7	H2	TI	--	Bit 2 of the Address Input bus.
ADDR IN (1)	9	K1	TI	--	Bit 1 of the Address Input bus.
ADDR IN (0)	13	K3	TI	--	Bit 0 (LSB) of the Address Input bus.

OUTPUT ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
ADDR OUT (10)	76	C2	TTO	--	Bit 10 (MSB) of the Address Output bus.
ADDR OUT (9)	78	C1	TTO	--	Bit 9 of the Address Output bus.
ADDR OUT (8)	80	D1	TTO	--	Bit 8 of the Address Output bus.
ADDR OUT (7)	82	E2	TTO	--	Bit 7 of the Address Output bus.
ADDR OUT (6)	84	E3	TTO	--	Bit 6 of the Address Output bus.
ADDR OUT (5)	2	F1	TTO	--	Bit 5 of the Address Output bus.
ADDR OUT (4)	4	G2	TTO	--	Bit 4 of the Address Output bus.
ADDR OUT (3)	6	H1	TTO	--	Bit 3 of the Address Output bus.
ADDR OUT (2)	8	J1	TTO	--	Bit 2 of the Address Output bus.
ADDR OUT (1)	10	J2	TTO	--	Bit 1 of the Address Output bus.
ADDR OUT (0)	11	L1	TTO	--	Bit 0 (LSB) of the Address Output bus.

REMOTE TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
TA4	56	B9	TUI	--	Remote Terminal Address bit 4 (MSB).
TA3	58	B8	TUI	--	Remote Terminal Address bit 3.
TA2	60	B7	TUI	--	Remote Terminal Address bit 2.
TA1	62	A7	TUI	--	Remote Terminal Address bit 1.
TA0	C6	64	TUI	--	Remote Terminal Address bit 0.
$\overline{\text{TALEN}}$/PARITY	52	C10	TUI	--	Remote Terminal Address Latch Enable/Remote Terminal Parity Input. Function of input is defined by the state of pin EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$. For EXT TEST = 0, EXT TST CH SEL A/$\overline{\text{B}}$ = 1, $\overline{\text{TALEN}}$/PARITY must provide odd parity for the Remote Terminal Address. For all other states of EXT TEST and EXT TST CH SEL A/$\overline{\text{B}}$ (i.e., 00, 10, 11) $\overline{\text{TALEN}}$/PARITY functions as an active low address strobe.

MODE CODE/SUBADDRESS OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{MC}$/SA	21	K6	TO	--	Mode Code/Subaddress Indicator. If $\overline{MC}$/SA is low, it indicates that the most recent command word is a mode code command. If $\overline{MC}$/SA is high, it indicates that the most recent command word is for a subaddress. This output indicates whether the mode code/subaddress outputs (i.e., MCSA(4:0)) contain mode code or subaddress information.
MCSA4	19	K5	TO	--	Mode Code/Subaddress 4. If $\overline{MC}$/SA is low, this pin represents the most significant bit of the the most recent command word (the MSB of the mode code). If $\overline{MC}$/SA is high, this pin represents the MSB of the subaddress.
MCSA3	18	J5	TO	--	Mode Code/Subaddress 3.
MCSA2	17	L4	TO	--	Mode Code/Subaddress 2.
MCSA1	16	K4	TO	--	Mode Code/Subaddress 1.
MCSA0	14	L2	TO	--	Mode Code/Subaddress 0. If $\overline{MC}$/SA is low, this pin represents the least significant bit of the the most recent command word. If $\overline{MC}$/SA is high, this pin represents the LSB of the subaddress.

BIPHASE INPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
BIPHASE IN A Z	39	G9	TI	--	Receiver - Channel A, Zero Input. Idle low Manchester input from the 1553 bus transceiver.
BIPHASE IN A O	37	H10	TI	--	Receiver - Channel A, One Input. This input is the complement of BIPHASE IN A Z.
BIPHASE IN B Z	34	J10	TI	--	Receiver - Channel B, Zero Input. Idle low Manchester input from the 1553 bus transceiver.
BIPHASE IN B O	33	K10	TI	--	Receiver - Channel B, One Input. This input is the complement of BIPHASE IN B Z.

BIPHASE OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
BIPHASE OUT A Z	28	K8	TO	--	Transmitter - Channel A, Zero Output. This Manchester-encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
BIPHASE OUT A O	27	L8	TO	--	Transmitter - Channel A, One Output. This output is the complement of BIPHASE OUT A Z. The output is idle low.
BIPHASE OUT B Z	30	L10	TO	--	Transmitter - Channel B, Zero Output. This Manchester-encoded data output is connected to the 1553 bus transmitter. The output is idle low.
BIPHASE OUT B O	32	L11	TO	--	Transmitter - Channel B, One Output. This output is the complement of BIPHASE OUT B Z. The output is idle low.

MASTER RESET AND CLOCK

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{MRST}}$	40	G10	TUI	AL	Master Reset. Initializes all internal functions of the RTI. $\overline{\text{MRST}}$ must be asserted 500 nanoseconds before normal RTI operation. (500 ns minimum).
12MHz	35	K11	TI	--	12 MHz Input Clock. This is the RTI system clock that requires an accuracy greater than 0.01% with a duty cycle from 50% +/-10%.
2MHz	24	L7	TO	--	2 MHz Clock Output. This is a 2 MHz output generated by the 12 MHz input clock. This clock is stopped when $\overline{\text{MRST}}$ is low.

POWER AND GROUND

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
V_{DD}	54	B10	PWR	--	+5 V_{DC}. Power supply must be +5 V_{DC} +/-10%.
V_{SS}	12 42	K2 F10	GND GND	-- --	Ground reference. Zero V_{DC} logic ground.

CONTROL PINS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{CS}$	44	E9	TI	AL	Chip Select. Active low input for host access of transparent memory or the RTI internal registers. In the transparent memory configuration $\overline{CS}$ is propagated through the RTI to the $\overline{RCS}$ output.
$\overline{CTRL}$	50	C11	TI	AL	Control. The host processor uses the active low $\overline{CTRL}$ input signal in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ to access the RTI internal registers. $\overline{CTRL}$ is also used in the software assignment of the terminal address and programmed reset.
$\overline{ADOEN}$	15	L3	TI	AL	Address Output Enable. When $\overline{ADOEN}$ is low the Address Out bus (ADDR OUT (15:0)) is active. If $\overline{ADOEN}$ = 1 the Address Out bus is high impedance.
RD/$\overline{WR}$	46	E10	TI	--	Read/Write. The host processor uses a high level on this input in conjunction with $\overline{CS}$ and $\overline{CTRL}$ to read the RTI internal registers. A low level on this input is used in conjunction with $\overline{CS}$ and $\overline{CTRL}$ to write to internal RTI registers. In the transparent memory configuration RD/$\overline{WR}$ is propagated through the RTI to the RRD/$\overline{RWR}$ output.
$\overline{BCEN}$	25	K7	TUI	AL	Broadcast Enable. Active low input enables broadcast commands.
ILL COMM	20	L5	TDI	AH	Illegal Command. The host processor uses the ILL COMM input to inform the RTI that the present command is illegal. ILL COMM is used in conjunction with MCSA(4:0) and $\overline{MC}$/SA to define system dependent illegal commands.

STATUS OUTPUTS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{RCS}$	43	F9	TO	AL	RAM Chip Select. Active low output used to enable memory for access.
RRD/$\overline{RWR}$	45	E11	TO	--	RAM Read/Write. High output enables memory read, low output enables memory write, used in conjunction with $\overline{RCS}$). Normally high output.
$\overline{COMSTR}$	22	J6	TO	AL	Command Strobe. $\overline{COMSTR}$ is an active low output of 500 nanoseconds duration identifying receipt of a valid command.
$\overline{TIMERON}$	41	G11	TO	AL	Fail-safe Timer. The $\overline{TIMERON}$ output pulses low for 730 microseconds when the RTI begins transmitting (i.e., rising edge of STATUS) to provide a fail-safe timer meeting the requirements of MIL-STD-1553B. This pulse is reset when $\overline{COMSTR}$ goes low or during Master Reset. In the external self-test mode $\overline{TIMERON}$ does not recognize $\overline{COMSTR}$ and resets after 730 microseconds.
MES ERR	49	D10	TO	AH	Message Error. The active high MES ERR output signals that the Message Error bit in the Status Register has been set due to receipt of an invalid command or an error during message sequence. MES ERR will reset to logic zero on receipt of next valid command.
CH A/$\overline{B}$	26	L6	TO	--	Channel A/$\overline{B}$. Output identifying the channel on which the most recent valid command was received. Channel A = 1, Channel B = 0.
$\overline{XMIT}$	38	H11	TO	AL	Transmit. Active low output identifies a transmit command message transfer by the RTI is in progress.
$\overline{RCV}$	51	B11	TO	AL	Receive. Active low output identifies a receive command message transfer by the RTI is in progress.
$\overline{BRDCST}$	36	J11	TO	AL	Broadcast. $\overline{BRDCST}$ is an active low output that identifies receipt of a valid broadcast command.
STATUS	23	J7	TO	AH	Status. Active high output pulse indicating that the RTI is in the process of transmitting a status word.

BUS ARBITRATION

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
DMARQ	47	F11	TO	AH	Direct Memory Access Request. Active high output requesting RTI access to memory.
$\overline{MEMCK}$	48	D11	TI	AL	Memory Clock (DMA Grant). Active low input signaling the RTI that a memory access is granted. Internal to the RTI, receipt of $\overline{MEMCK}$ generates RAM chip select and RAM read/write signals.

BUS ARBITRATION

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
EXT TST	29	L9	TDI	--	External Self-test Enable. Multi-function input pin. In self-test mode forcing this pin high allows the monitoring of self-test activity at the bus stub. When the RTI is not in self-test this pin defines the function of $\overline{\text{TALEN}}$/PARITY.
EXT TST CH SEL	31	K9	TUI	--	External Self-test Channel Select. A/$\overline{\text{B}}$ Multi-function input pin. In self-test mode forcing this pin high selects the channel on which the self-test is performed (Channel A = 1, Channel B = 0). When the RTI is not in self-test this pin defines the function of $\overline{\text{TALEN}}$/PARITY.

4.0 Operating Conditions

ABSOLUTE MAXIMUM RATINGS(1)
(referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
V_{IO}	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	+/-10	mA
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation	300	mW
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance, junction-to-case	20	°C/W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
V_{IN}	DC input voltage	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 +/- .01%	MHz

5.0 DC Electrical Characteristics

(V_{DD} = 5.0V +/-10%; -55°C < Tc < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	 V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	 -1 110 -2750	 1 2750 -110	 µA µA µA
V_{OL}	Low-level output voltage (TTL)	I_{OL} = 4 mA		0.4	V
V_{OH}	High-level output voltage (TTL)	I_{OH} = -400 µA	2.4		V
I_{OZ}	Three-state output leakage current	V_O = V_{DD} or V_{SS}	-10	+ 10	µA
I_{OS}	Short-circuit output current (1,2)	V_{DD} = 5.5 V, V_O = V_{DD} V_{DD} = 5.5 V, V_O = 0 V	 -90	90	mA mA
C_{IN}	Input capacitance (3)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (3)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (3)	F = 1 MHz @ 0 V		25	pF
I_{DD}	Average operating current (1,4)	F = 12 MHz, CL = 50 pF		50	mA
QI_{DD}	Quiescent current	Note 5		1.5	mA

Notes:
1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
4. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
5. All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

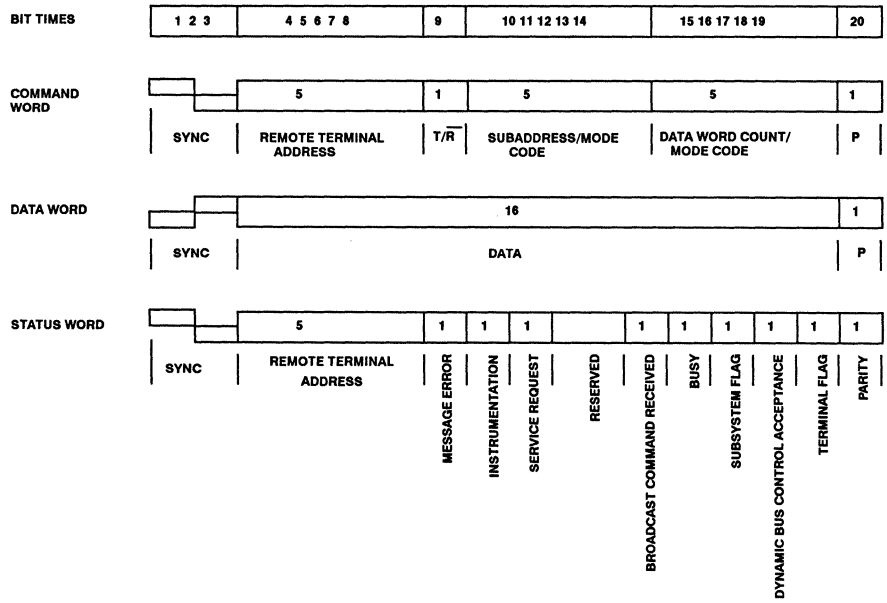
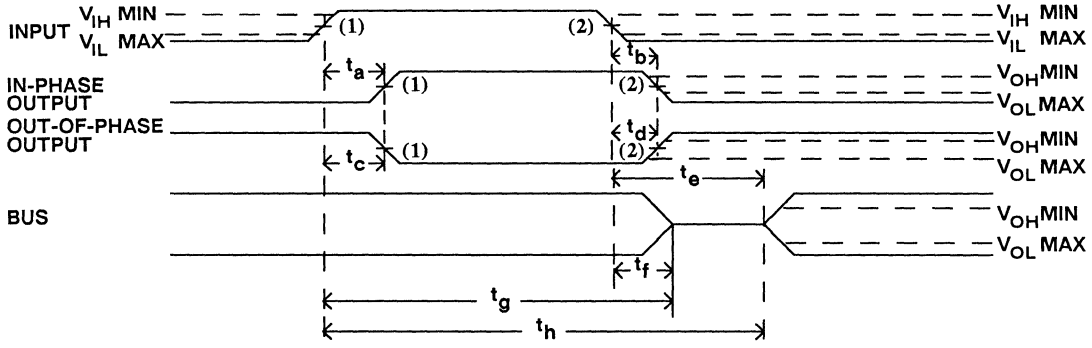


Figure 8. MIL-STD-1553B Word Formats

6.0 AC Electrical Characteristics (3, 4)

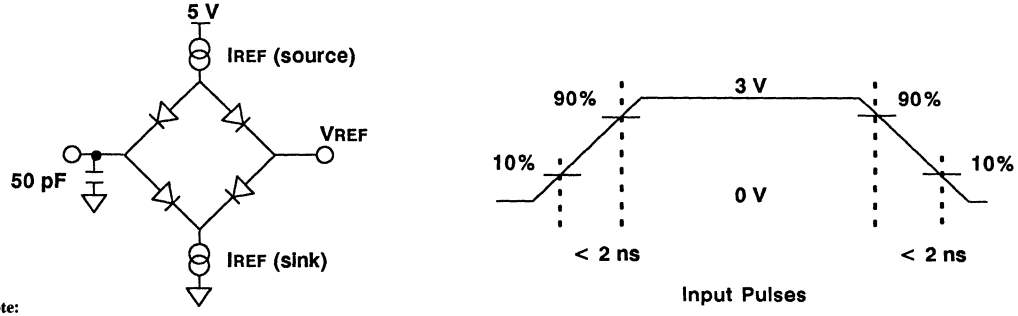
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 9a. Typical Timing Measurements



Note:
30 pF including scope probe and test socket

Figure 9b. AC Test Loads and Input Waveforms

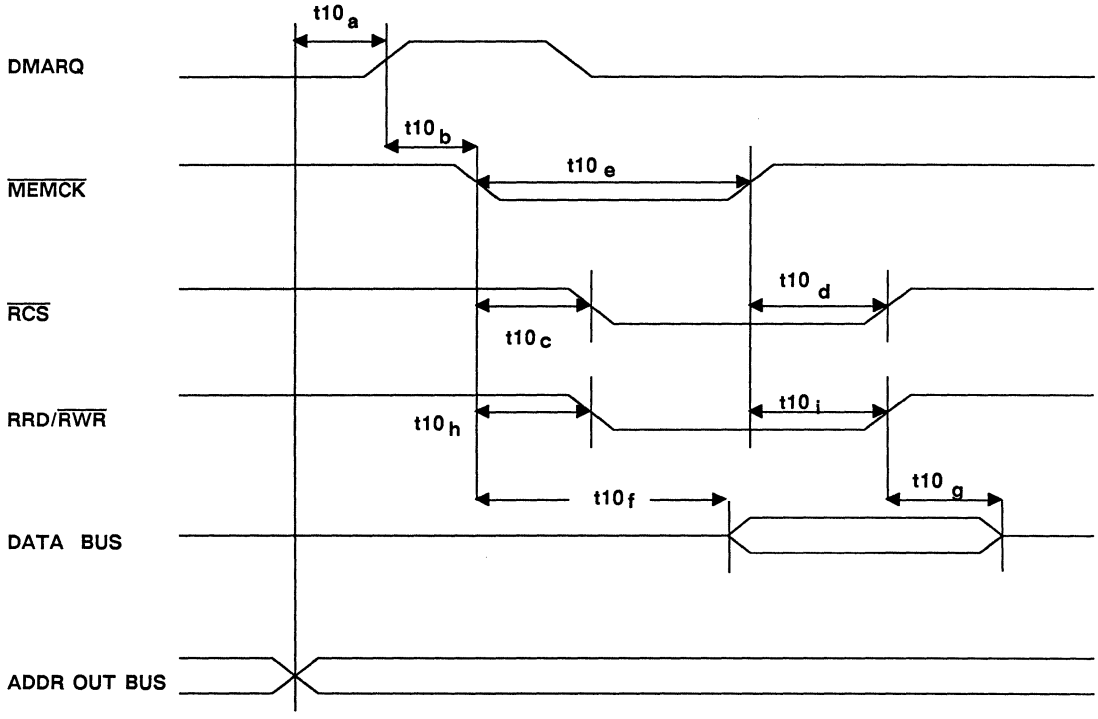


Figure 10. RTI Memory Write

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t10_a$	ADDR OUT valid to DMARQ active (3)	883	992	ns
$t10_b$	DMARQ active to $\overline{\text{MEMCK}}$ active (2, 3)	0	–	ns
$t10_c$	$\overline{\text{MEMCK}}$ active to $\overline{\text{RCS}}$ active (4)	–	67	ns
$t10_d$	$\overline{\text{MEMCK}}$ inactive to $\overline{\text{RCS}}$ inactive (4)	–	61	ns
$t10_e$	$\overline{\text{MEMCK}}$ pulse width (1, 2, 4)	83	–	ns
$t10_f$	$\overline{\text{MEMCK}}$ active to DATA bus valid (4)	–	115	ns
$t10_g$	$\overline{\text{MEMCK}}$ active to DATA bus high impedance (3)	5	101	ns
$t10_h$	$\overline{\text{MEMCK}}$ active to RRD/$\overline{\text{RWR}}$ active	–	61	ns
$t10_i$	$\overline{\text{MEMCK}}$ inactive to RRD/$\overline{\text{RWR}}$ inactive	–	58	ns

Notes:
1. Allows a 20 ns data valid set-up time before $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ go high.
2. The sum $t_b + t_e$ must not exceed 18.8 μs.
3. Supplied as a design limit, but not guaranteed or tested.
4. Guaranteed by test.

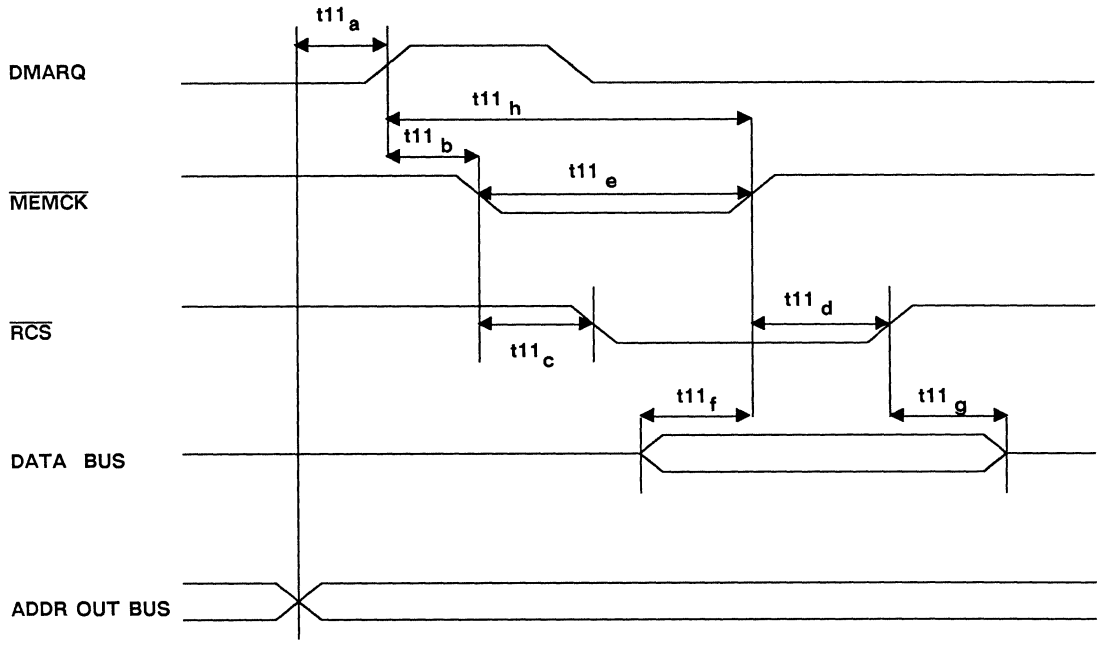


Figure 11. RTI Memory Read

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t11_a$	ADDR OUT valid to DMARQ active (3)	883	992	ns
$t11_b$	DMARQ active to $\overline{\text{MEMCK}}$ active (3)	0	14.9	µs
$t11_c$	$\overline{\text{MEMCK}}$ active to $\overline{\text{RCS}}$ active (4)	–	67	ns
$t11_d$	$\overline{\text{MEMCK}}$ inactive to $\overline{\text{RCS}}$ inactive (4)	–	61	ns
$t11_e$	$\overline{\text{MEMCK}}$ pulse width (1, 2, 4)	50	–	ns
$t11_f$	Input DATA valid to $\overline{\text{MEMCK}}$ inactive (4)	45	–	ns
$t11_g$	Input DATA valid after $\overline{\text{RCS}}$ inactive (4)	5	–	ns
$t11_h$	DMARQ active to $\overline{\text{MEMCK}}$ inactive (4)	–	18.3	µs

Notes:
1. Allows a 20 ns data valid set-up time before $\overline{\text{RCS}}$ and RRD/$\overline{\text{RWR}}$ go high.
2. The sum $t_b + t_e$ must not exceed 18.8 µs.
3. Supplied as a design limit, but not guaranteed or tested.
4. Guaranteed by test.

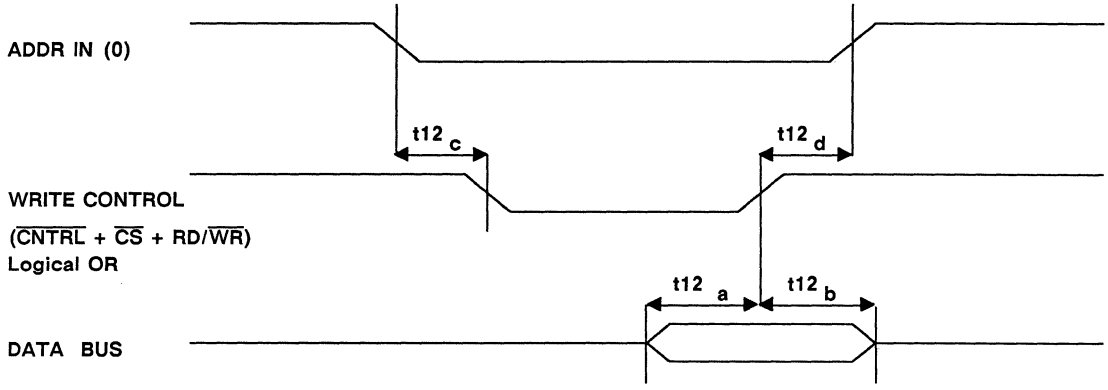


Figure 12. Control Register Write Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t12 a	Input DATA valid before WRITE CONTROL inactive (set-up time) (3)	20	-	ns
t12 b	Input DATA valid after WRITE CONTROL inactive (hold-time) (3)	25	-	ns
t12 c	ADDR IN valid before WRITE CONTROL asserts (1, 3)	20	-	ns
t12 d	ADDR IN valid after WRITE CONTROL negates (2, 3)	20	-	ns

Notes:
1. Set-up time required to prevent inadvertent software reset.
2. Hold-time required to prevent inadvertent software reset.
3. Guaranteed by test.

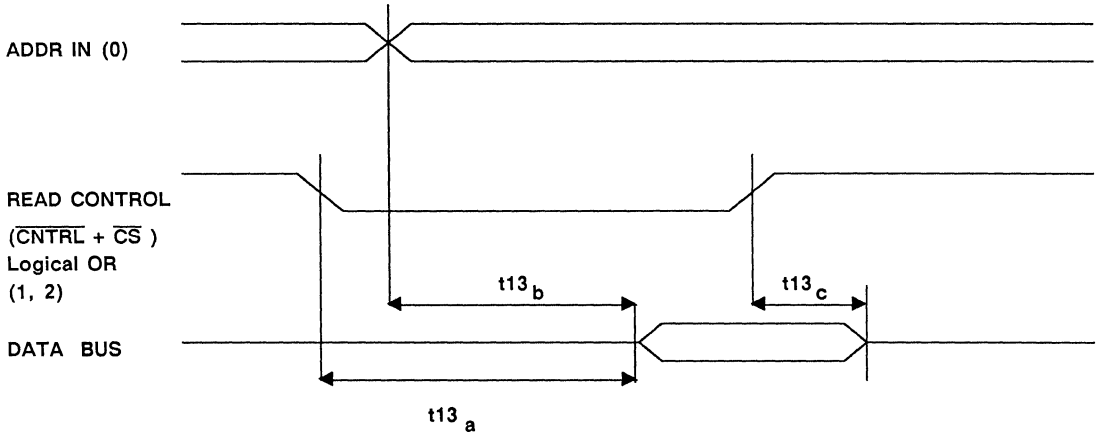


Figure 13. System and Last Command Register Read Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t13_a$	DATA bus valid after READ CONTROL valid while ADDR IN (0) = 0 or 1	-	132	ns
$t13_b$	DATA bus valid after ADDR IN (0) = 0 or 1 while READ CONTROL = 0	-	70	ns
$t13_c$	READ CONTROL negation to DATA bus high impedance (3)	-	101	ns

Notes:
1. ADDR IN (0) = 0 System Register read.
2. ADDR IN (0) = 1 Last Command Register read.
3. Supplied as a design limit but not guaranteed or tested.

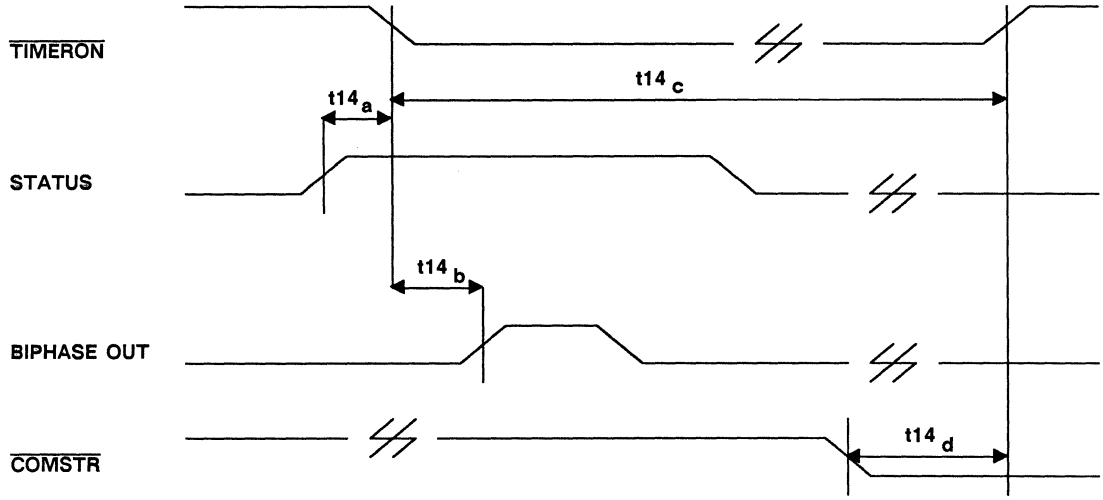


Figure 14. RT Fail-Safe Timer Signal Relationships

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t14_a$	STATUS active to $\overline{\text{TIMERON}}$ active (1)	4	31	ns
$t14_b$	$\overline{\text{TIMERON}}$ active to first BIPHASE OUT transition (1)	1.2	–	µs
$t14_c$	$\overline{\text{TIMERON}}$ low pulse width (1)	–	732	µs
$t14_d$	$\overline{\text{COMSTR}}$ active to $\overline{\text{TIMERON}}$ reset (1)	–	31	ns

Note:
1. Supplied as a design limit, but not guaranteed or tested.

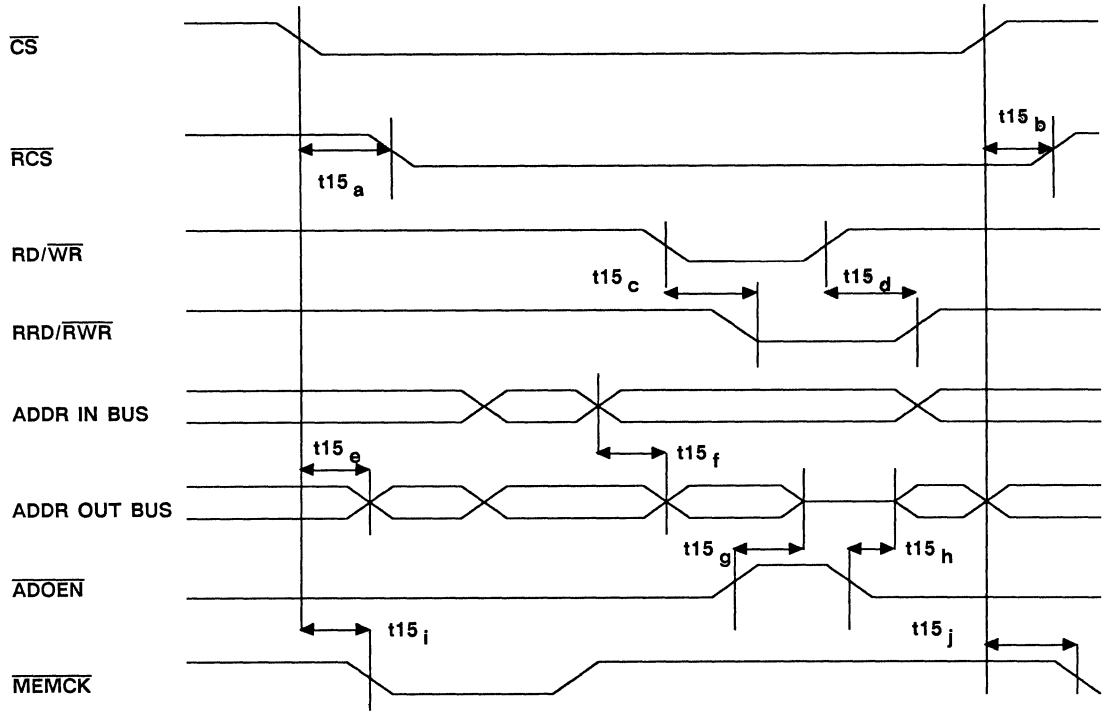


Figure 15. RTI Propagation Delays

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t15_a$	$\overline{CS}$ active to $\overline{RCS}$ active (2)	–	48	ns
$t15_b$	$\overline{CS}$ negation to $\overline{RCS}$ negation (2)	–	40	ns
$t15_c$	RD/$\overline{WR}$ active to RRD/$\overline{RWR}$ active (2)	–	45	ns
$t15_d$	RD/$\overline{WR}$ negation to RRD/$\overline{RWR}$ negation (2)	–	35	ns
$t15_e$	$\overline{CS}$ active to ADDR OUT valid (2)	6	52	ns
$t15_f$	ADDR IN valid to ADDR OUT valid (2)	–	44	ns
$t15_g$	$\overline{ADOEN}$ negation to ADDR OUT high impedance (1)	–	42	ns
$t15_h$	$\overline{ADOEN}$ active to ADDR OUT active (2)	6	50	ns
$t15_i$	$\overline{CS}$ active to $\overline{MEMCK}$ active ($\overline{MEMCK}$ not recognized) (1)	13	–	ns
$t15_j$	$\overline{CS}$ negation to $\overline{MEMCK}$ active ($\overline{MEMCK}$ recognized) (1)	10	–	ns

Note:
1. Supplied as a design limit, but not guaranteed or tested.
2. Guaranteed by test.

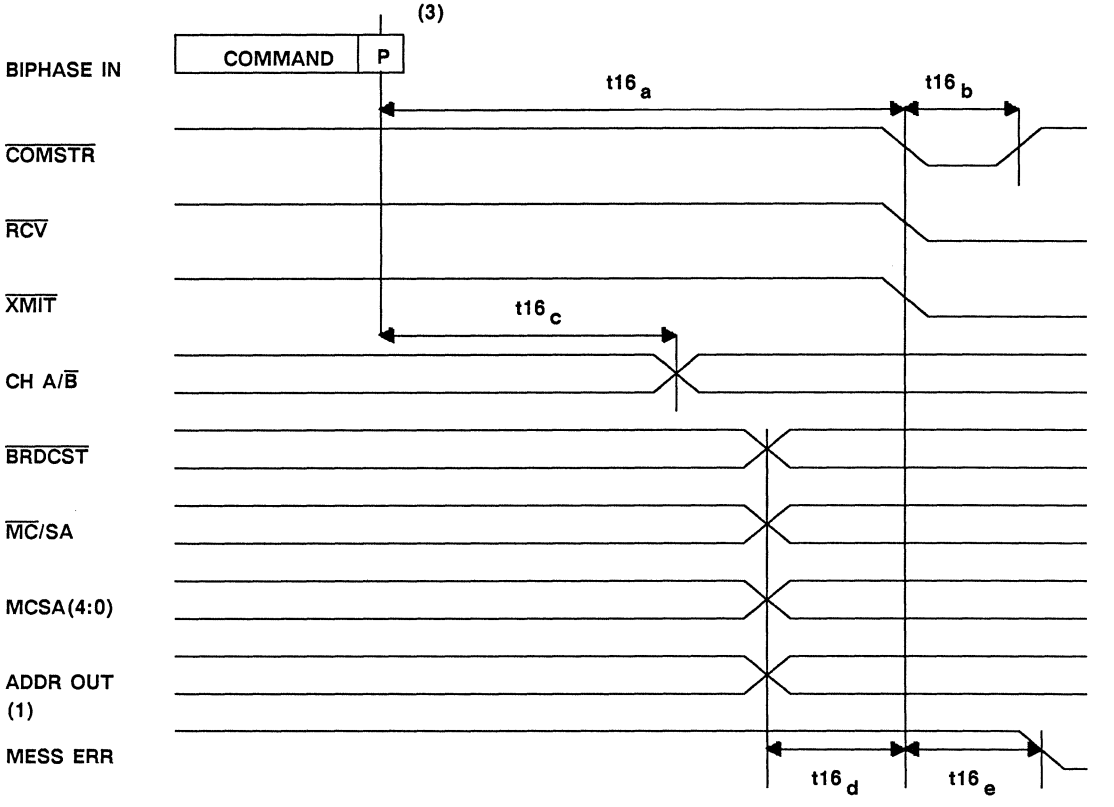


Figure 16. Command Word Validation

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t16_a$	Command word parity to $\overline{\text{COMSTR}}$ and $\overline{\text{RCV}}$ or $\overline{\text{XMIT}}$ active (4)	3.58	3.67	µs
$t16_b$	$\overline{\text{COMSTR}}$ pulse width (4)	499	502	ns
$t16_c$	Command word parity to CH A/$\overline{\text{B}}$ valid (4)	2.58	2.66	µs
$t16_d$	Status output signals valid to $\overline{\text{COMSTR}}$ active (2, 4)	430	–	ns
$t16_e$	MES ERR reset after $\overline{\text{COMSTR}}$ active (4)	745	750	ns

Notes:
1. $\overline{\text{ADOEN}}$ is asserted (i.e., logic low).
2. Status signals include $\overline{\text{BRDCST}}$, $\overline{\text{MC}}$/SA, MCSA(4:0), and ADDR OUT.
3. Measured from mid-bit parity crossing.
4. Supplied as a design limit, but not guaranteed or tested.

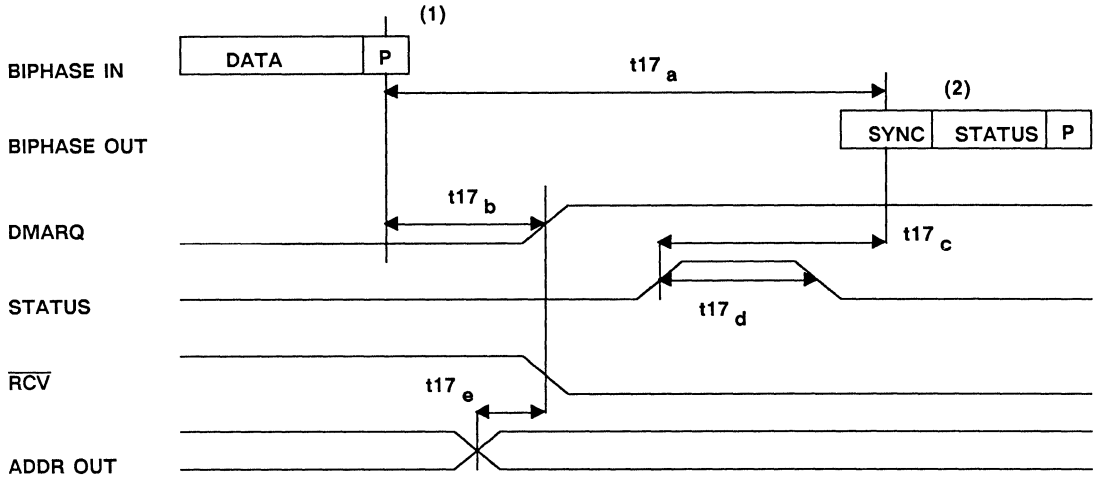


Figure 17. Receive Command Message Processing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
$t17_a$	Data word parity bit to status word response (1, 3)	8.80	9.37	µs
$t17_b$	Data word parity bit to DMARQ active (2, 3)	3.58	3.68	µs
$t17_c$	STATUS active to BIPHASE OUT active (3)	1.24	1.25	µs
$t17_d$	STATUS pulse width (3)	4.48	4.98	µs
$t17_e$	ADDR OUT valid before DMARQ (H) (3)	0.90	–	µs

Notes:
1. Measured from last data word mid-bit parity crossing.
2. Measured from transmitted status word sync field mid-bit crossing.
3. Supplied as a design limit, but not guaranteed or tested.

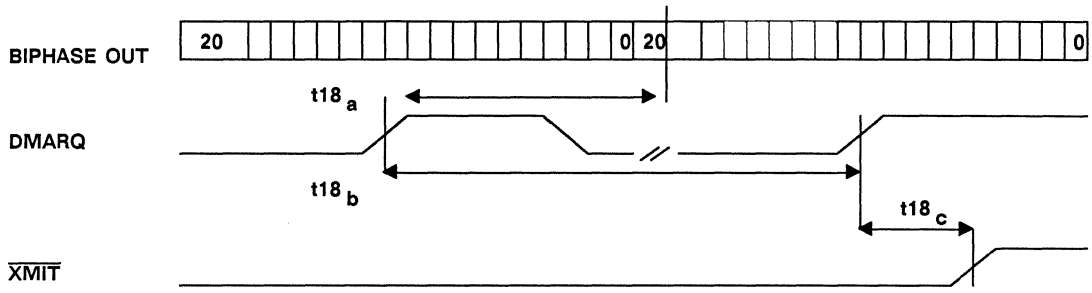


Figure 18. Transmitted Data Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
* t18 a	DMARQ active to sync field of transmitted data word	17.15	17.18	µs
* t18 b	DMARQ active to DMARQ active	–	19.2	µs
* t18 c	XMIT negation after last DMARQ active	460	500	ns

Note:
* Supplied as a design limit but not guaranteed or tested.

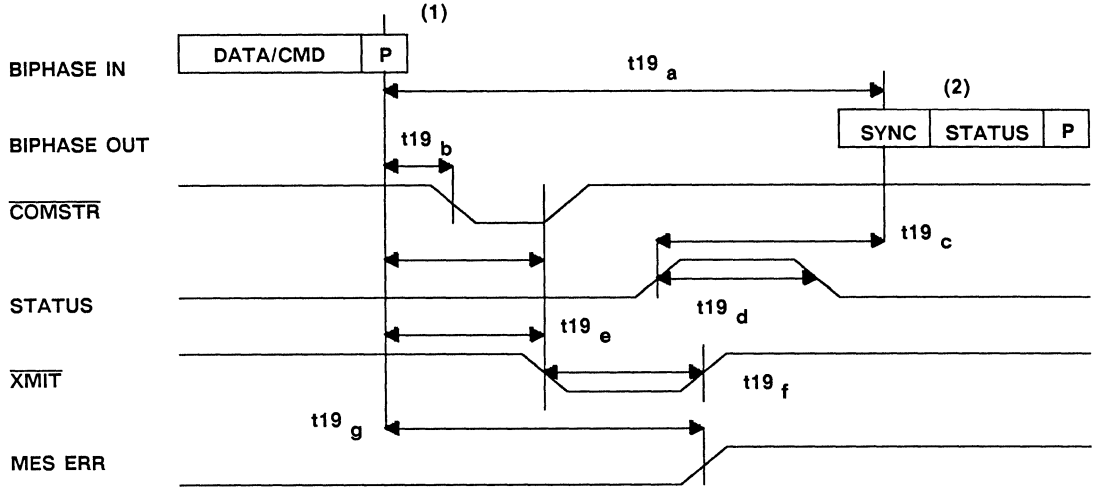


Figure 19. Mode Command Message Processing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
* $t19_a$	Response time BIPHASE IN to BIPHASE OUT (2)	3.58	3.67	µs
* $t19_b$	Command word parity bit to $\overline{\text{COMSTR}}$ assertion (1)	8.80	9.37	µs
* $t19_c$	STATUS active to BIPHASE OUT active	1.24	1.25	µs
* $t19_d$	STATUS pulse width	4.48	4.98	µs
* $t19_e$	Command word parity bit to $\overline{\text{XMIT}}$ assertion	3.58	3.67	µs
* $t19_f$	$\overline{\text{XMIT}}$ pulse width for mode code reception	1.00	–	µs
* $t19_g$	Command word parity bit to MES ERR assertion	6.57	6.68	µs

Notes:
1. Measured from data or command word mid-bit parity crossing.
2. Measured from transmitted status word sync field mid-bit crossing.
* Supplied as a design limit but not guaranteed or tested.

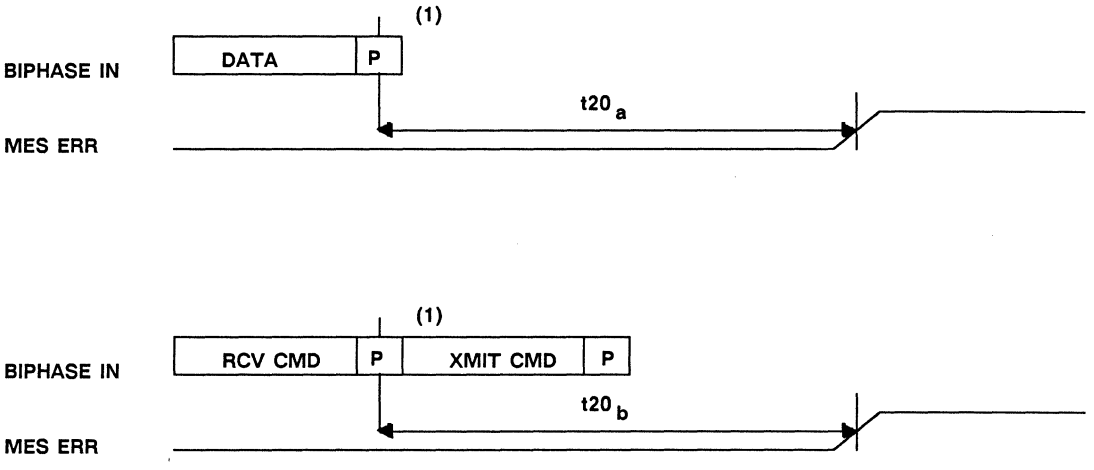


Figure 20. Message Error Timing

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
*t20 a	Data word parity bit to MES ERR assertion (1)	23.50	23.63	µs
*t20 b	Command word parity bit to MES ERR assertion RT to RT transfer (2)	55.4	55.5	µs

Notes:
1. Measured from last data word mid-bit parity crossing.
2. No-response from transmitter.
* Supplied as a design limit but not guaranteed or tested.

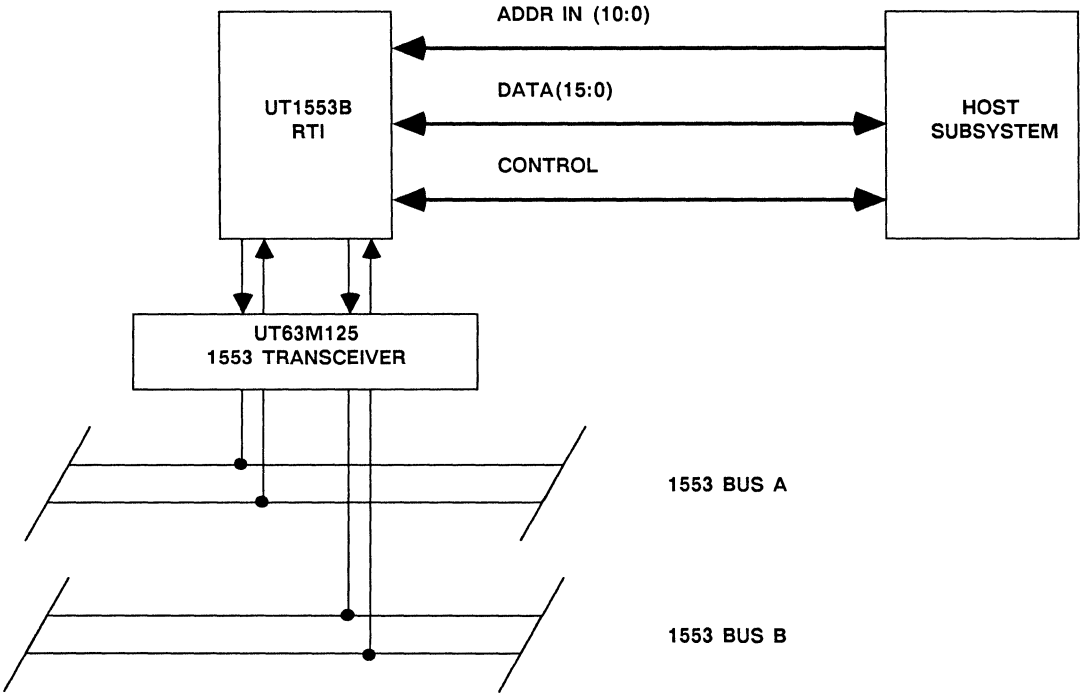


Figure 21. RTI General System Diagram (Idle low interface)

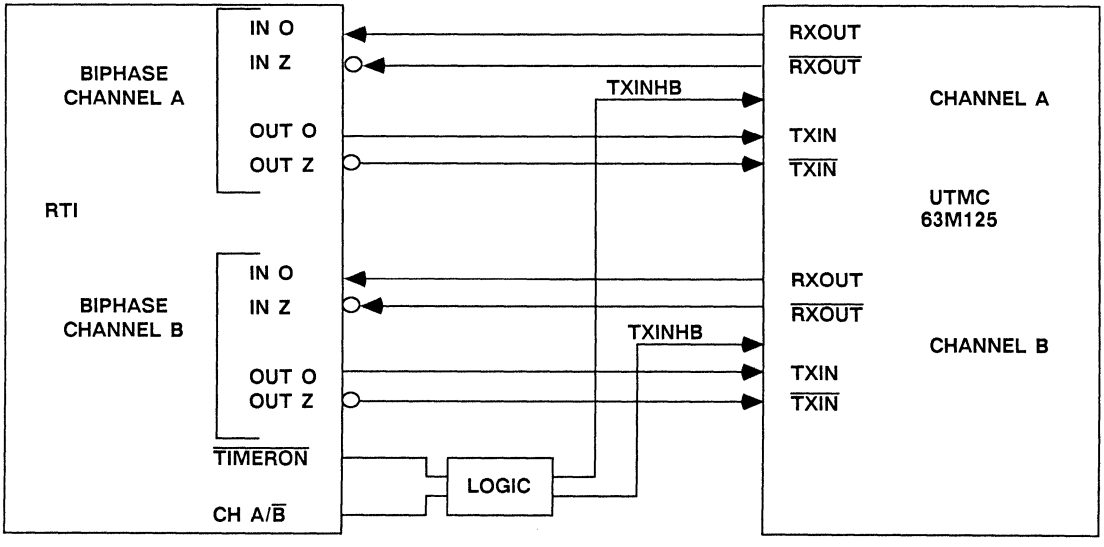


Figure 22. RTI Transceiver Interface Diagram

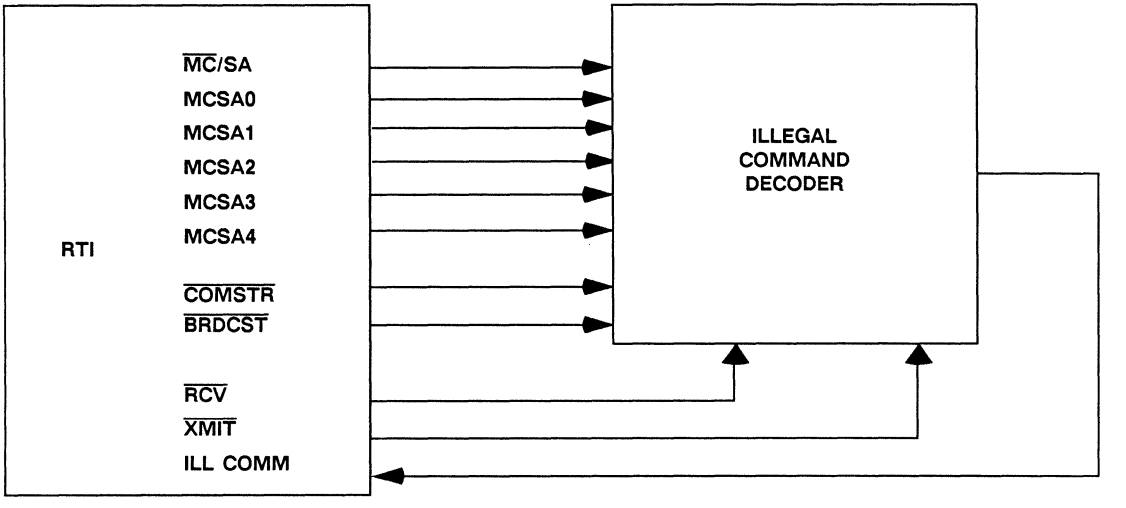


Figure 23. Mode Code/Subaddress Illegalization Circuit

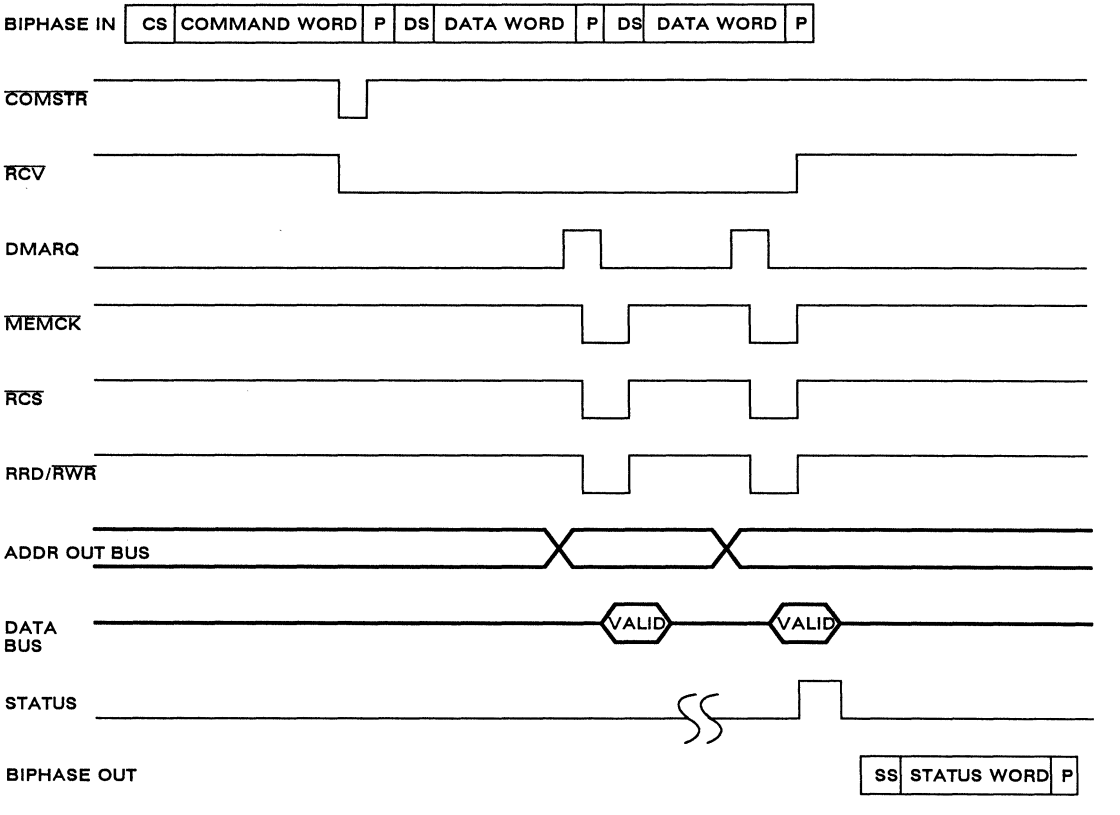


Figure 24. Receive Command with Two Data Words

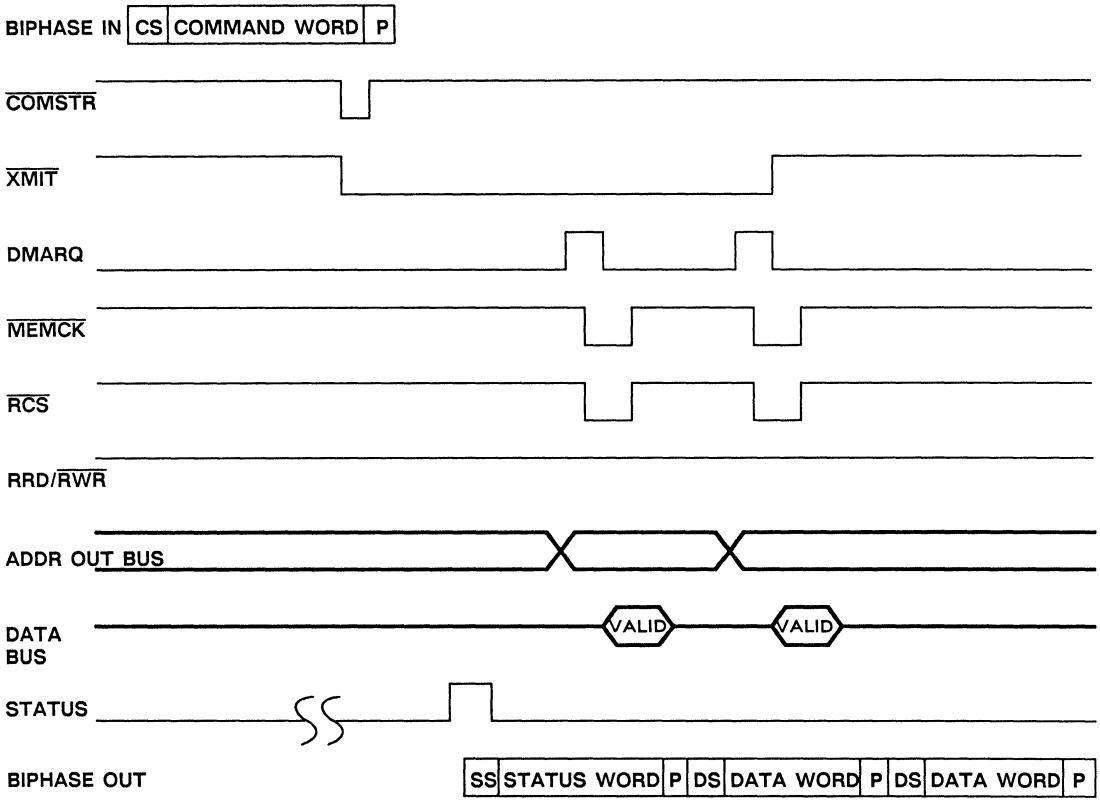
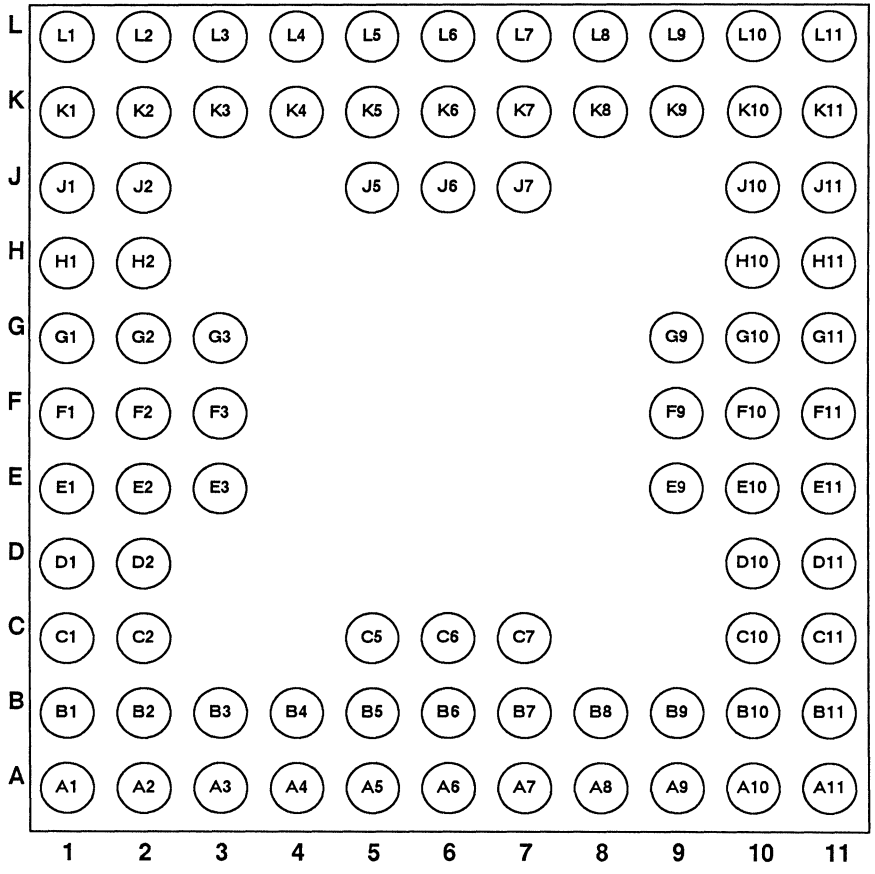
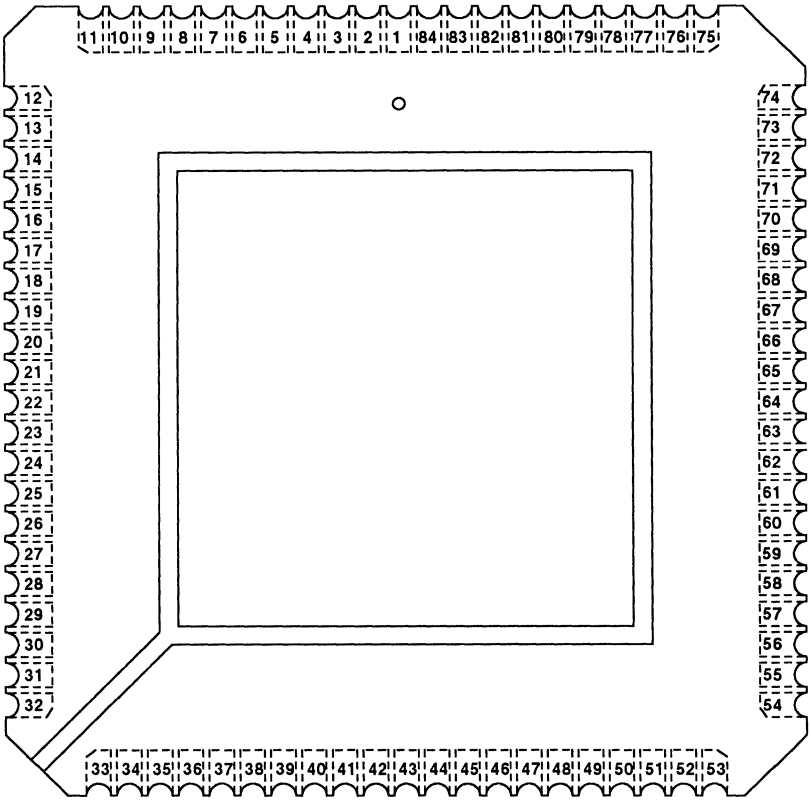


Figure 25. Transmit Command with Two Data Words



A1	DATA I/O 0	C1	ADDR OUT 9	F1	ADDR OUT 5	J1	ADDR OUT 2	L1	ADDR OUT 0
A2	DATA I/O 2	C2	ADDR OUT 10	F2	ADDR IN 7	J2	ADDR OUT 1	L2	MCSA 0
A3	DATA I/O 3	C5	DATA I/O 6	F3	ADDR IN 5	J5	MCSA 3	L3	$\overline{\text{ADOEN}}$
A4	DATA I/O 5	C6	TA 0	F9	$\overline{\text{RCS}}$	J6	$\overline{\text{COMSTR}}$	L4	MCSA 2
A5	DATA I/O 8	C7	DATA I/O 10	F10	VSS	J7	STATUS	L5	ILL COMM
A6	DATA I/O 9	C10	$\overline{\text{TALEN}}$/PARITY	F11	DMARQ	J10	BIPHASE IN B Z	L6	CH A/$\overline{\text{B}}$
A7	TA 1	C11	$\overline{\text{CTRL}}$			J11	$\overline{\text{BRDCST}}$	L7	2MHZ
A8	DATA I/O 12			G1	ADDR IN 4			L8	BIPHASE OUT A
A9	DATA I/O 13	D1	ADDR OUT 8	G2	ADDR OUT 4	K1	ADDR IN 1	L9	EXT TEST
A10	DATA I/O 14	D2	ADDR IN 8	G3	ADDR IN 3	K2	VSS	L10	BIPHASE OUT B
A11	DATA I/O 15	D10	MES ERR	G9	BIPHASE IN A Z	K3	ADDR IN 0	L11	BIPHASE OUT B
		D11	$\overline{\text{MEMCK}}$	G10	$\overline{\text{MRST}}$	K4	MCSA 1		
B1	ADDR IN 9			G11	$\overline{\text{TIMERON}}$	K5	MCSA 4		
B2	ADDR IN 10	E1	ADDR IN 6			K6	$\overline{\text{MC}}$/SA		
B3	DATA I/O 1	E2	ADDR OUT 7	H1	ADDR OUT 3	K7	$\overline{\text{BCEN}}$		
B4	DATA I/O 4	E3	ADDR OUT 6	H2	ADDR IN 2	K8	BIPHASE OUT A Z		
B5	DATA I/O 7	E9	$\overline{\text{CS}}$	H10	BIPHASE IN A O	K9	EXT TST CH SEL	A/B	
B6	DATA I/O 11	E10	RD/$\overline{\text{WR}}$	H11	$\overline{\text{XMIT}}$	K10	BIPHASE IN B O		
B7	TA 2	E11	RRD/$\overline{\text{RWR}}$			K11	12MHZ		
B8	TA 3								
B9	TA 4								
B10	VDD								
B11	$\overline{\text{RCV}}$								

Figure 26a. UT1553B RTI Pingrid Array Configuration (Bottom View)



1	ADDR IN 5	19	MCSA 4	37	BIPHASE IN A O	55	DATA I/O 14	73	DATA I/O 1
2	ADDR OUT 5	20	ILL COMM	38	$\overline{\text{XMIT}}$	56	TA4	74	DATA I/O 0
3	ADDR IN 4	21	MC/SA	39	BIPHASE IN A Z	57	DATA I/O 13	75	ADDR IN 10
4	ADDR OUT 4	22	COMSTR	40	$\overline{\text{MRST}}$	58	TA3	76	ADDR OUT 10
5	ADDR IN 3	23	STATUS	41	$\overline{\text{TIMERON}}$	59	DATA I/O 12	77	ADDR IN 9
6	ADDR OUT 3	24	2MHZ	42	VSS	60	TA2	78	ADDR OUT 9
7	ADDR IN 2	25	BCEN	43	$\overline{\text{RCS}}$	61	DATA I/O 11	79	ADDR IN 8
8	ADDR OUT 2	26	CH A/B	44	$\overline{\text{CS}}$	62	TA1	80	ADDR OUT 8
9	ADDR IN 1	27	BIPHASE OUT A O	45	RRD/$\overline{\text{RWR}}$	63	DATA I/O 10	81	ADDR IN 7
10	ADDR OUT 1	28	BIPHASE OUT A Z	46	RD/$\overline{\text{WR}}$	64	TA0	82	ADDR OUT 7
11	ADDR OUT 0	29	EXT TEST	47	DMARQ	65	DATA I/O 9	83	ADDR IN 6
12	VSS	30	BIPHASE OUT B Z	48	$\overline{\text{MEMCK}}$	66	DATA I/O 8	84	ADDR OUT 6
13	ADDR IN 0	31	EXT TST CH SEL A/B	49	MES ERR	67	DATA I/O 7		
14	MCSA0	32	BIPHASE OUT B O	50	$\overline{\text{CTRL}}$	68	DATA I/O 6		
15	ADOEN	33	BIPHASE IN B O	51	$\overline{\text{RCV}}$	69	DATA I/O 5		
16	MCSA1	34	BIPHASE IN B Z	52	TALEN/PARITY	70	DATA I/O 4		
17	MCSA2	35	12MHZ	53	DATA I/O 15	71	DATA I/O 3		
18	MCSA3	36	$\overline{\text{BRDCST}}$	54	VDD	72	DATA I/O 2		

Figure 26b. UT1553B RTI Chip Carrier Configuration
(Top View)

UT1553 Remote Terminal Multi-Protocol

Features

- ☐ Complete VLSI MIL-STD-1553 Remote Terminal Interface
- ☐ Mode selectable to comply with either MIL-STD-1553A or MIL-STD-1553B bus protocol
- ☐ Remote terminal operation is certified by ASD/ENASC (formerly SEAFAC)
- ☐ Implements all dual-redundant Remote Terminal operational functions
- ☐ Provides handshake control for quad-redundant systems
- ☐ Data pointers permit programmable memory mapping for 1553 data over the entire 64K host memory space
- ☐ Provides all handshaking signals for a DMA (Direct Memory Access) interface
- ☐ Stores 1553 command word and time-tag information with all incoming data for enhanced data management
- ☐ Supports end-of-command activity and data bus error interrupts
- ☐ Low-power CMOS technology with TTL-compatible inputs and outputs
- ☐ Available in 84-pin pingrid array and 84-lead leadless chip carrier packages
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B

Introduction

The UT1553 RTMP (figures 1 and 4) is a monolithic, CMOS, VLSI integrated circuit that meets all requirements for a dual-redundant MIL-STD-1553 Remote Terminal interface. The RTMP's advanced design supports both MIL-STD-1553A and MIL-STD-1553B serial data bus protocols, including differences in the status word response time and bit definitions, providing the system designer a single-chip solution to most Remote Terminal interface requirements.

The UT1553 RTMP provides all requisite 1553 protocol and data handling, 1553 message error checking, DMA handshake and control signals, and comprehensive self-test capabilities. The RTMP's pointer-based, programmable memory-mapping architecture permits the host to map 1553 message data anywhere in the 64K memory space. This advanced memory mapping, along with the RTMP's control and status functions, minimize the host system's 1553 interface overhead.

The UT1553 RTMP is a member of UTMC's complete family of high-reliability monolithic MIL-STD-1553 interface products.

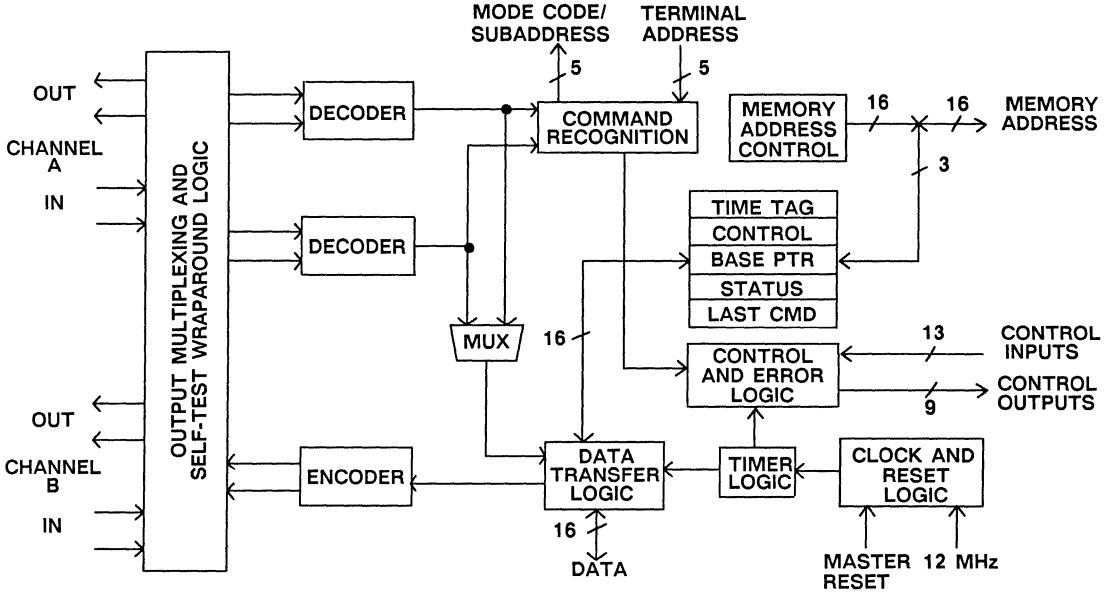


Figure 1. UT1553 RTMP Functional Block Diagram

Table of Contents

1.0 Functional Description

General Description

The RTMP is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system (figure 2). By selecting the correct state of the 1553 protocol select pin (PRA/$\overline{B}$ = 1 for 1553A, 0 for 1553B), the system designer can program the RTMP to comply fully with either MIL-STD-1553A or MIL-STD-1553B.

The link between the 1553 data bus and the RTMP is the shared memory area. All the data the RTMP transmits or receives over the 1553 bus is stored in this shared memory area. The RTMP accesses the shared memory with its DMA signals ($\overline{DMAR}$, $\overline{DMAG}$, and DMAEN), the 16-bit bidirectional data bus (D0-D15), and the 16-bit address bus (A0-A15).

Since the RTMP's architecture is based on a series of data pointers, the 1553 transmit and receive data can be placed anywhere in the 64K memory space, allowing the system designer to optimize memory usage. The system designer can program the RTMP to store the data received over the 1553 bus in one of two ways. The RTMP can store the received data in a single data buffer or in separate buffers. When the RTMP stores the received data in a single buffer, all received data, regardless of subaddress, is stored in contiguous locations in the shared memory. When the RTMP stores the received data in separate buffers, the RTMP stores the data associated with each of the 30 subaddresses in unique locations in memory.

The RTMP has six internal registers that provide the host subsystem with RTMP control and status information. Three of these registers are read/write: Time Tag Data Register (TTD), the Control Register (CTL), and the Base Pointer Data Register (BPD). Two are read only: Operational Status Register (OPS), and the Last Command Register (LCM). The Stop Self-Test Register (SST) is a write-only register. To control the RTMP and the 1553 interface, the host begins by programming the Base Pointer Data Register. By programming the BPD, the system designer tells the RTMP where in the shared memory the 64-word Pointer Block will reside, whether the RTMP will store the 1553 received data in single or separate buffers, and how deep these data buffers will actually be. Figure 3 is a simple representation of the RTMP's memory-mapping architecture.

After the host has programmed the BPD, the 1553 interface is enabled by setting either CHAEN or CHBEN in the RTMP's Control Register. The RTMP now monitors the 1553 data bus for a valid command word or mode code to its particular terminal address. When received, the RTMP looks at the mode bit (single/separate) in the BPD, the 1553 command transmit/receive bit, and the mode code or subaddress portion of the 1553 command to determine which of the address pointers in the 64-word Pointer Block the RTMP will use for this particular memory transaction.

Each memory transaction consists of memory writes for receive command words and memory reads for transmit command words. This process continues until all 1553 data words have been received or transmitted. If the host has enabled any of the RTMP's interrupts, the RTMP asserts them when the memory transaction is complete.

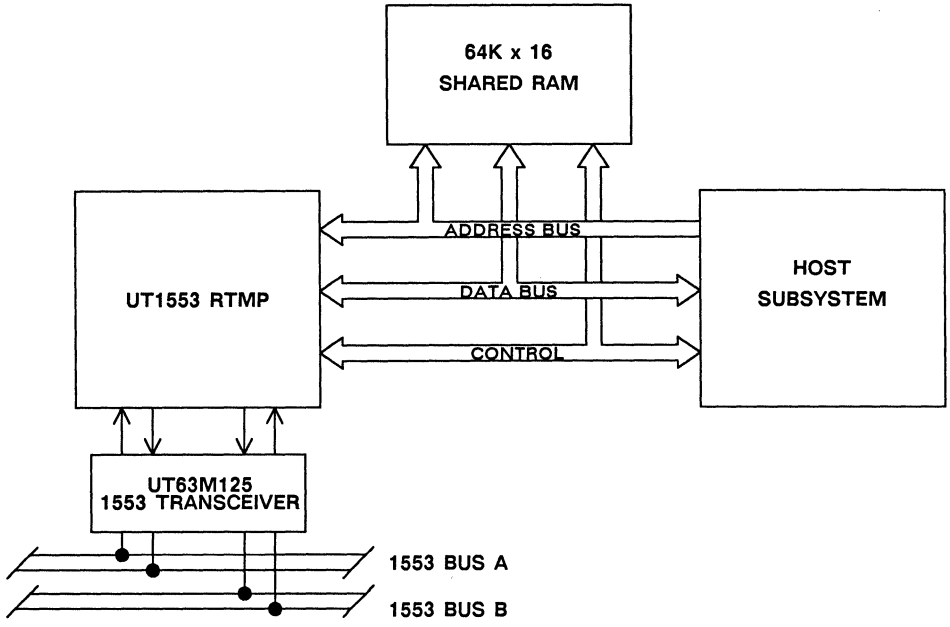


Figure 2. RTMP General System Diagram

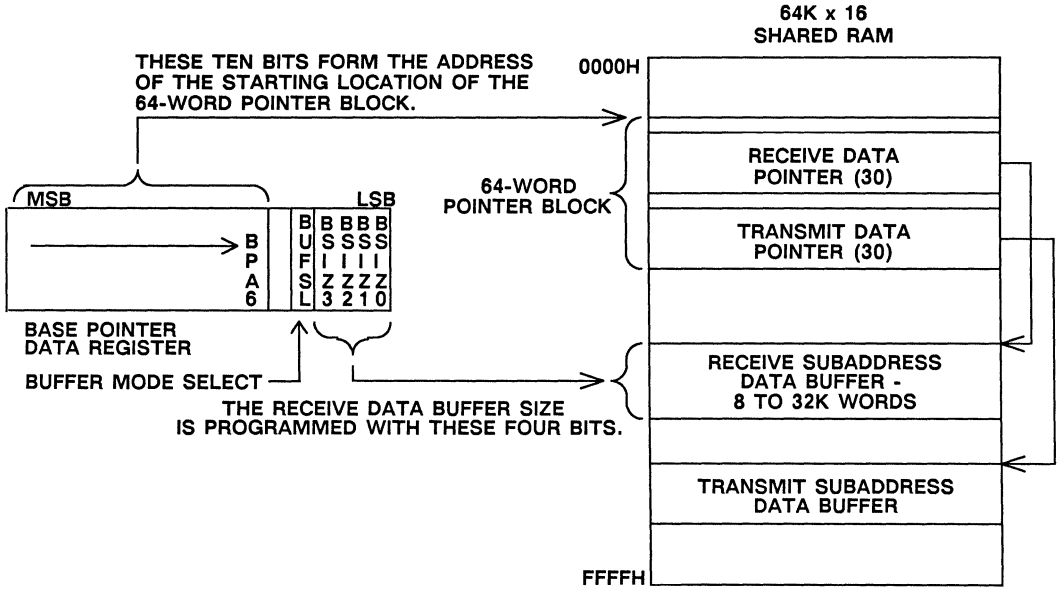
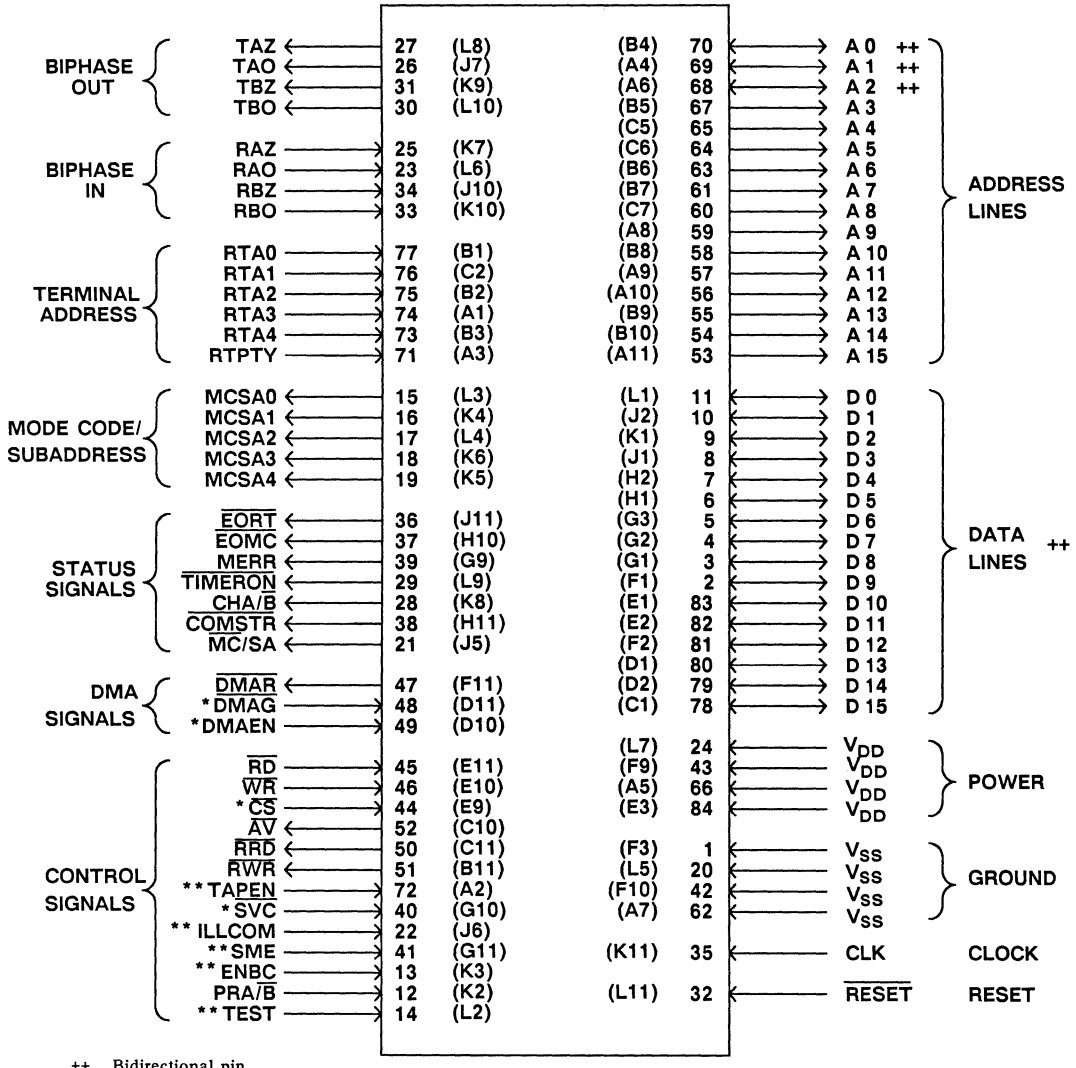


Figure 3. RTMP Receive and Transmit Data Memory Mapping

2.0 Pin Identification And Description



++ Bidirectional pin.
* Pin internally pulled up.
** Pin internally pulled down.

Leadless chip carrier pin numbers are not in parentheses.
( ) Pingrid array pin numbers are in parentheses.

Figure 4. RTMP Functional Pin Description

Legend for TYPE and ACTIVE fields:

TO = TTL output
TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional
AH = Active high
AL = Active low

DATA BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
D15	78	C1	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
D14	79	D2	TTB	--	Bit 14 of the bidirectional Data bus.
D13	80	D1	TTB	--	Bit 13 of the bidirectional Data bus.
D12	81	F2	TTB	--	Bit 12 of the bidirectional Data bus.
D11	82	E2	TTB	--	Bit 11 of the bidirectional Data bus.
D10	83	E1	TTB	--	Bit 10 of the bidirectional Data bus.
D9	2	F1	TTB	--	Bit 9 of the bidirectional Data bus.
D8	3	G1	TTB	--	Bit 8 of the bidirectional Data bus.
D7	4	G2	TTB	--	Bit 7 of the bidirectional Data bus.
D6	5	G3	TTB	--	Bit 6 of the bidirectional Data bus.
D5	6	H1	TTB	--	Bit 5 of the bidirectional Data bus.
D4	7	H2	TTB	--	Bit 4 of the bidirectional Data bus.
D3	8	J1	TTB	--	Bit 3 of the bidirectional Data bus.
D2	9	K1	TTB	--	Bit 2 of the bidirectional Data bus.
D1	10	J2	TTB	--	Bit 1 of the bidirectional Data bus.
D0	11	L1	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

ADDRESS BUS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
A15	53	A11	TTO	--	Bit 15 (MSB) of the Address bus.
A14	54	B10	TTO	--	Bit 14 of the Address bus.
A13	55	B9	TTO	--	Bit 13 of the Address bus.
A12	56	A10	TTO	--	Bit 12 of the Address bus.
A11	57	A9	TTO	--	Bit 11 of the Address bus.
A10	58	B8	TTO	--	Bit 10 of the Address bus.
A9	59	A8	TTO	--	Bit 9 of the Address bus.
A8	60	C7	TTO	--	Bit 8 of the Address bus.
A7	61	B7	TTO	--	Bit 7 of the Address bus.
A6	63	B6	TTO	--	Bit 6 of the Address bus.
A5	64	C6	TTO	--	Bit 5 of the Address bus.
A4	65	C5	TTO	--	Bit 4 of the Address bus.
A3	67	B5	TTO	--	Bit 3 of the Address bus.
A2	68	A6	TTB	--	Bit 2 of the Address bus. Address bits A2 - A0 are bidirectional so the host can select one of the RTMP's internal registers during internal I/O operations.
A1	69	A4	TTB	--	Bit 1 of the Address Bus. (Reference A2)
A0	70	B4	TTB	--	Bit 0 (LSB) of the Address Bus. (Reference A2)

DMA SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{DMAR}}$	47	F11	TO	AL	DMA Request. Indicates the RTMP is requesting use of the Data bus from the current bus master.
$\overline{\text{DMAG}}$	48	D11	TUI	AL	DMA Grant. Gives control of the Data bus to the RTMP. $\overline{\text{DMAG}}$ is recognized only if DMAEN is high. $\overline{\text{DMAG}}$ must remain asserted until $\overline{\text{AV}}$ goes high to ensure that the RTMP completes the current DMA cycle.
DMAEN	49	D10	TUI	AH	DMA Enable. When high, this input allows the RTMP to recognize $\overline{\text{DMAG}}$. When low, DMAEN places all three-state pins in a high-impedance state and disables the RTMP's memory access cycle.

CONTROL SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{CS}$	44	E9	TUI	AL	Chip Select. This input, along with $\overline{RD}$ and $\overline{WR}$, allows the host to access the RTMP's internal data registers.
$\overline{RD}$	45	E11	TI	AL	Read. When used in conjunction with $\overline{CS}$, $\overline{RD}$ allows the RTMP to place data from the selected internal register on the Data bus (D15-D0).
$\overline{WR}$	46	E10	TI	AL	Write. When used in conjunction with $\overline{CS}$, $\overline{WR}$ latches data from the Data bus (D15-D0) into the selected RTMP internal register.
$\overline{AV}$	52	C10	TTO	AL	Address Valid. The RTMP asserts $\overline{AV}$ to indicate that the address (A15-A0) is valid.
$\overline{RRD}$	50	C11	TTO	AL	RAM Read. The RTMP asserts $\overline{RRD}$ during DMA cycles that require data from system RAM.
$\overline{RWR}$	51	B11	TTO	AL	RAM Write. The RTMP asserts $\overline{RWR}$ during DMA cycles to write data to system memory.
$\overline{SVC}$	40	G10	TUI	AL	Superseding Valid Command. The host system uses this input when more than one RT is present in the system; i.e., a quad-redundant system. When asserted, this input causes the RTMP to terminate all present activity and perform an internal reset of encoders/decoders, RT state machine, and DMA state machine. Registers are not affected. Do not assert while $\overline{DMAR}$ is asserted (tpw 250 ns minimum).
SME	41	G11	TDI	AH	Set Message Error. Asserting this input causes the Message Error bit in the status word to be set.
ILLCOM	22	J6	TDI	AH	Illegal Command. This input illegalizes a command word that the RTMP accepts but the system does not support. When set, the RTMP responds with the Message Error bit set in the status word. ILLCOM is used in conjunction with the Mode Code/ Subaddress outputs.
PRA/$\overline{B}$	12	K2	TI	--	Program A/$\overline{B}$. This input is the 1553 mode select input. A high input places the RTMP in the MIL-STD-1553A mode; a low places the RTMP in the MIL-STD-1553B mode.
ENBC	13	K3	TDI	AH	Enable Broadcast. A high on this input, when the RTMP is in the 1553B mode, allows the RTMP to recognize a broadcast command word.
TEST	14	L2	TDI	AH	Test. The TEST input pin allows the user to select between internal (TEST = 0) or external (TEST = 1) self-test. When TEST equals a logic one and DMAEN equals a logic zero, MCSA (4:0) and $\overline{MC}$/SA three-state.

STATUS SIGNALS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{EORT}}$	36	J11	TTO	AL	End of Receive/Transmit. This interrupt is a pulse that is maskable by writing to the Control Register. The user can select $\overline{\text{EORT}}$ to occur at the end of receive command activity, at the end of transmit command activity, under either of these conditions, or disable it completely. The $\overline{\text{EORT}}$ output is designed to simulate an open-collector output and requires a pull-up resistor. (250 ns pulse width). This signal is not generated if a message error condition exists.
$\overline{\text{EOMC}}$	37	H10	TTO	AL	End of Mode Code. This non-maskable interrupt is a pulse that occurs at the end of all memory accesses associated with any mode code command. The $\overline{\text{EOMC}}$ output is designed to simulate an open-collector output and requires a pull-up resistor. $\overline{\text{EOMC}}$ and $\overline{\text{EORT}}$ can be logically ORed together to form a composite interrupt. The 250 ns pulse width is generated after command word is stored. This signal is not generated if a message error condition exists.
$\overline{\text{COMSTR}}$	38	H11	TO	AL	Command Strobe. This low-going pulse identifies receipt of a valid 1553 command word.
MERR	39	G9	TO	AH	Message Error. Active when the RTMP detects an error in the 1553 transmission and sets the Message Error bit in the status word. MERR is reset when the RTMP receives the next valid command word. ($\overline{\text{COMSTR}}$ assertion)
CHA/$\overline{\text{B}}$	28	K8	TO	--	Channel A/$\overline{\text{B}}$. When high, this output indicates the RTMP received the last command on Channel A; when low, the last command was received on Channel B.
$\overline{\text{TIMERON}}$	29	L9	TO	AL	Timer On. Indicates the RTMP is transmitting data. The output remains active until the data transmission is complete or the internal fail-safe timer times out (600 µs for 1553A and 800 µs for 1553B). The RTMP internally disables both transmitters and keeps them disabled until the RTMP receives a valid command word. This signal is asserted approximately 250 ns before beginning of status word transmission.

MODE CODE/SUBADDRESS

NAME	PIN NUMBER LCC	PIN NUMBER PGA	TYPE	ACTIVE	DESCRIPTION
$\overline{\text{MC}}$/SA	21	J5	TTO	AL	Mode Code/Subaddress. $\overline{\text{MC}}$/SA = 0 indicates that the MCSA0-MCSA4 pins contain the Mode Code bits of the most recently received mode code. $\overline{\text{MC}}$/SA = 1 indicates that MCSA0-MCSA4 pins contain the Subaddress bits of the most recently received command word.
MCSA0 MCSA1 MCSA2 MCSA3 MCSA4	15 16 17 18 19	L3 K4 L4 K6 K5	TTO	--	Mode Code/Subaddress. These five bits are used in conjunction with the $\overline{\text{MC}}$/SA output. $\overline{\text{MC}}$/SA = 0 indicates that these five bits are the five least significant bits of the mode code command word. $\overline{\text{MC}}$/SA = 1 indicates these five bits are the 1553 command word subaddress.

REMOTE TERMINAL ADDRESS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RTA4 RTA3 RTA2 RTA1 RTA0	73 74 75 76 77	B3 A1 B2 C2 B1	TI	--	Remote Terminal Address Inputs. The RTMP uses these inputs to select the terminal address for this specific remote terminal.
TAPEN	72	A2	TDI	AH	Terminal Address Parity Enable. Enables the RTMP's Terminal Address parity-checking function.
RTPTY	71	A3	TI	--	Remote Terminal Parity. When the Terminal Address parity-checking function is enabled (TAPEN = 1), RTPTY must provide odd parity for the terminal address input pins (RTA4-RTA0).

MASTER RESET AND CLOCK

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
$\overline{\text{RESET}}$	32	L11	TI	AL	Reset. Initializes all internal functions of the RTMP. $\overline{\text{RESET}}$ must be asserted before normal RTMP operation. 500 ns minimum.
CLK	35	K11	TI	--	Clock. The clock input requires a 50% ±10% duty cycle with an accuracy of 12 MHz ±0.01%

CHANNEL A BIPHASE SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RAO	23	L6	TI	--	Receiver (Channel) A One. Manchester input from the 1553 bus receiver.
RAZ	25	K7	TI	--	Receiver (Channel) A Zero. This input is the complement of RAO.
TAO	26	J7	TO	--	Transmitter (Channel) A One. This Manchester-encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TAZ	27	L8	TO	--	Transmitter (Channel) A Zero. This output is the complement of TAO. The output is idle low.

CHANNEL B BIPHASE SIGNALS

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
RBO	33	K10	TI	--	Receiver (Channel) B One. Manchester data input from the 1553 bus receiver.
RBZ	34	J10	TI	--	Receiver (Channel) B Zero. This input is the complement of RBO.
TBO	30	L10	TO	--	Transmitter (Channel) B One. This Manchester-encoded output is connected to the 1553 bus transmitter input. The output is idle low.
TBZ	31	K9	TO	--	Transmitter (Channel) B Zero. This output is the complement of TBO. The output is idle low.

3

POWER AND GROUND

NAME	PIN NUMBER		TYPE	ACTIVE	DESCRIPTION
	LCC	PGA			
VDD	24 43 66 84	L7 F9 A5 E3	--	--	+5 V_{DC} Power. Power supply input must be +5 ±10%.
VSS	1 20 42 62	F3 L5 F10 A7	--	--	Reference Ground. Zero V_{DC} logic ground.

3.0 Remote Terminal Architecture

3.1 Internal Registers

The RTMP has six internal registers that allow the host to control the RTMP's actions and also to obtain its operational status. The host can read from or write to three of these registers: the Time Tag Data Register (TTD), the Control Register (CTL), and the Base Pointer Data Register (BPD). Two of the registers are read-only: the Operational Status Register (OPS), and the Last Command Register (LCM). The Stop Self-Test Register (SST) is a write-only register.

Six signals allow the host to access the RTMP's internal registers. Three of the six signals are control signals: Chip Select ($\overline{CS}$), Read ($\overline{RD}$), and Write ($\overline{WR}$). The other three signals are the RTMP's bidirectional address lines, A0 - A2. When the $\overline{CS}$ = 0, the three least significant address lines, A0 - A2, become inputs to the RTMP. The RTMP decodes these three address lines, along with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, to determine which of the six internal registers the host is attempting to access. Table 1 shows the addresses for the RTMP's internal registers for read and write operations.

3.2 Read/Write Registers

The RTMP has three internal read/write registers. These three registers are:

- The Time Tag Data Register
- The Control Register
- The Base Pointer Data Register

3.3 Time Tag Data Register (TTD)

The TTD contains a free-running, 16-bit, ripple counter. The Time Tag clock has a resolution of 64 µs. The TTD is initialized to 0000H when the host asserts the $\overline{RESET}$ input. All TTD bits are programmable by performing a write to the TTD with the desired bit pattern.

The RTMP stores the TTD's value in the shared memory area at the end of each 1553 receive message. The host can also directly read the TTD. Since the TTD is a free-running counter, the host may read the TTD while the counter is rippling, resulting in the host reading erroneous data. If this situation presents a problem, the host should read the TTD data twice. Figure 5 represents the TTD. (0000H after Master Reset.)

Table 1. RTMP Internal Register Addresses

1. RTMP Register Write Addresses

$\overline{CS}$	$\overline{WR}$	A2	A1	A0	
0	0	0	0	0	Time Tag Data Register
0	0	0	0	1	Control Register
0	0	0	1	0	Base Pointer Data Register
0	0	0	1	1	Stop Self-Test Register
0	0	1	X	X	Don't Care

2. RTMP Register Read Addresses

$\overline{CS}$	$\overline{RD}$	A2	A1	A0	
0	0	0	0	0	Time Tag Data Register
0	0	0	0	1	Control Register
0	0	0	1	0	Base Pointer Data Register
0	0	0	1	1	Operational Status Register
0	0	1	0	0	Last 1553 Command Register
0	0	1	0	1	Don't Care
0	0	1	1	0	Don't Care
0	0	1	1	1	Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
MSB															LSB

Figure 5. The Time Tag Data Register

3.4 Control Register (CTL)

The CTL provides the host with the ability to control four functions: (1) programming the bits in 1553 status word; (2) masking the End of Receive/Transmit message activity interrupt (output pin $\overline{EORT}$); (3) enabling and selecting the channel for the self-test; and (4) selecting the active 1553 channel. The definition of the 1553 status word bits in the CTL is different when the RTMP is operating in the 1553A mode (PRA/$\overline{B}$ = 1) as opposed to the1553B mode (PRA/$\overline{B}$ = 0). Figure 6 shows the bit definitions in the CTL for the 1553A mode; figure 7 shows the definition for the 1553B mode.

The host determines the CTL functions status by reading the CTL Register.

CTL Bit Definitions - 1553A Mode

Bit 15	CHAEN [0]	Channel A Enable. When CHAEN = 1, the RTMP responds to a 1553 command word or mode code on bus Channel A. CHAEN = 0 disables the RTMP from responding to 1553 command word or mode code on 1553 bus Channel A.
Bit 14	CHBEN [0]	Channel B Enable. When CHBEN = 1, the RTMP responds to a 1553 command word or mode code on bus Channel B. CHBEN = 0 disables the RTMP from responding to 1553 command word or mode code on 1553 bus Channel B. Disable for internal self-test.
Bit 13	STEN [0]	Self-Test Enable. STEN enables the RTMP's internal self-test.
Bit 12	STCS [0]	Self-Test Channel Select. If the host has enabled an RTMP self-test (STEN = 1), STCS selects the RTMP receiver channel to test. STCS = 1 selects Channel A, and STCS = 0 selects Channel B.
Bit 11	IM1 [0]	Interrupt Mask One. If IM1 = 1, the $\overline{EORT}$ interrupt output is active at the end of 1553 receive command memory activity. IM1 = 0 masks this interrupt function.
Bit 10	IM2 [0]	Interrupt Mask Two. If IM2 = 1, the $\overline{EORT}$ interrupt output is active at the end of 1553 transmit command memory activity. IM2 = 0 masks this interrupt function.
Bit 9	SWB10 [0]	Status Word Bit 10. When the host sets this bit, SWB10 = 1, the bit in the RTMP's status word that is transmitted during bit time ten is set (see figure 30 for status word bit time definitions). The bits in the status word are system-defined in MIL-STD-1553A.
Bit 8	SWB11 [0]	Status Word Bit 11. When the host sets this bit (SWB11 = 1), the bit in the RTMP's status word transmitted during bit time 11 is set.
Bit 7	SWB12 [0]	Status Word Bit 12. When the host sets this bit (SWB12 = 1), the bit in the RTMP's status word transmitted during bit time 12 is set.
Bit 6	SWB13 [0]	Status Word Bit 13. When the host sets this bit (SWB13 = 1), the bit in the RTMP's status word transmitted during bit time 13 is set.
Bit 5	SWB14 [0]	Status Word Bit 14. When the host sets this bit (SWB14 = 1), the bit in the RTMP's status word transmitted during bit time 14 is set.
Bit 4	SWB15 [0]	Status Word Bit 15. When the host sets this bit (SWB15 = 1), the bit in the RTMP's status word transmitted during bit time 15 is set.
Bit 3	SWB16 [0]	Status Word Bit 16. When the host sets this bit (SWB16 = 1), the bit in the RTMP's status word transmitted during bit time 16 is set.
Bit 2	SWB17 [0]	Status Word Bit 17. When the host sets this bit (SWB17 = 1), the bit in the RTMP's status word transmitted during bit time 17 is set.
Bit 1	SWB18 [0]	Status Word Bit 18. When the host sets this bit (SWB18 = 1), the bit in the RTMP's status word transmitted during bit time 18 is set.
Bit 0	TFLG	Terminal Flag. TFLG = 1 sets the Terminal Flag bit in the 1553A status word. TFLG = 0 resets the Terminal Flag bit in the 1553A status word.

CTL Bit Definitions - 1553B Mode

Bit 15	CHAEN [0]	Channel A Enable. Same as 1553A mode. Disable for internal self-test.
Bit 14	CHBEN [0]	Channel B Enable. Same as 1533A mode. Disable for internal self-test.
Bit 13	STEN [0]	Self-Test Enable. Same as 1553A mode.
Bit 12	STCS [0]	Self-Test Channel Select. Same as 1553A mode.
Bit 11	IM1 [0]	Interrupt Mask One. Same as 1553A mode.
Bit 10	IM2 [0]	Interrupt Mask Two. Same as 1553A mode.
Bit 9	INSTR [0]	Instrumentation Bit. When INSTR = 1, the RTMP's 1553 status word response has the Instrumentation bit set. This bit remains set until INSTR is set to 0.
Bit 8	SVREQ [0]	Service Request Bit. When SVREQ = 1, the RTMP's 1553 status word response has the Service Request bit set. This bit remains set until SVREQ is set to 0.
Bit 7	N/A	This bit is defined as a reserved bit in MIL-STD-1553B and is not used. Setting this bit has no effect on the status word response.
Bit 6	N/A	Same as bit 7.
Bit 5	N/A	Same as bit 7.
Bit 4	BDCST [0]	Broadcast Bit. When BDCST = 1, the RTMP's 1553 status word response has the Broadcast bit set. Manual override; not cleared by receipt of next command. Broadcast bit in outgoing status word is set to a logical one on the receipt of broadcast command.
Bit 3	BUSY [0]	Busy Bit. When BUSY = 1, the RTMP's 1553 status word response has the Busy bit set. This bit remains set until BUSY is set to 0.
Bit 2	SFLG [0]	Subsystem Flag. When SFLG = 1, the RTMP's 1553 status word response has the Subsystem Flag bit set. This bit remains set until SFLG is set to 0.
Bit 1	N/A	Same as bit 7.
Bit 0	TFLG [0]	Terminal Flag. Same as 1553A mode.

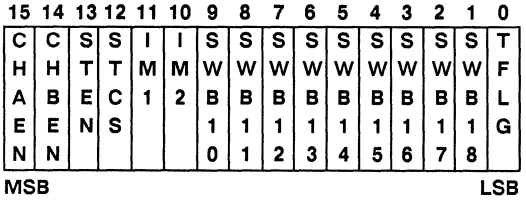


Figure 6. The Control Register in 1553A Mode

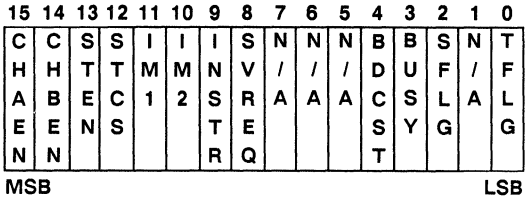


Figure 7. The Control Register in 1553B Mode

3.5 Base Pointer Data Register

The BPD provides three types of information: (1) the location in memory for the 64-word Pointer Block; (2) the receive-data storage-buffer select for either single or separate data buffers; and (3) the size or depth of the single or separate data buffers (figure 8). (0000H after Master Reset.)

BPD Bit Definitions

Bit 15-Bit 6	BPA15-BPA 6	Block Pointer Address. These ten bits provide the RTMP with the ten most significant address lines for the location, within the 64K word addressing range, of the 64-word Pointer Block.
Bit 5	N/A	This bit is not used.
Bit 4	BUFSL	Buffer Select. When BUFSL = 1, the host selects the RTMP's single buffer mode of storing 1553 receive data. If BUFSL = 0, the host selects the separate buffer mode of storing 1553 receive data.
Bit 3-Bit 0	BSIZ3-BSIZ0	Buffer Size Select. These four bits select the size of the receive data buffers and can range from 3 (0011B) to 15 (1111B). The actual size of the data buffer is equal to 2^X where X is the decimal equivalent of BSIZ3-BSIZ0. The size of the data buffers can range from eight (2^3) words to 32K (2^{15}) words. The variable X is not defined for zero through two.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPA15	BPA14	BPA13	BPA12	BPA11	BPA10	BPA9	BPA8	BPA7	BPA6	N/A	BUFSL	BSIZ3	BSIZ2	BSIZ1	BSIZ0

MSB LSB

Figure 8. The Base Pointer Data Register

3.6 Read Only Registers

The RTMP has two internal registers that are read-only. These two registers provide status information on the operation of the RTMP:

- The Operational Status Register
- The Last 1553 Command Register

3.6.1 Operational Status Register (OPS)

The OPS provides the host with the operational status of the RTMP while the RTMP is active. Figure 9 shows the information bits stored in the OPS.

OPS Bit Definitions

Bit 15	MACT [0]	Message Active. MACT = 1 indicates that the RTMP is actively processing a message. The RTMP clears MACT upon completing the message.
Bit 14	VMPRO [0]	Valid Message Processed. VMPRO = 1 indicates that the RTMP has processed a valid 1553 message. The host clears VMPRO bit when the OPS is read.
Bit 13	ME [0]	Message Error. ME = 1 indicates that a 1553 message error has occurred. The host clears ME when the OPS is read *unless* the condition that caused the MERR still persists after the register read.
Bit 12	PE [X]	Parity Error. PE = 0 indicates that the RTMP has detected an error in the Terminal Address parity. This bit can only be active when TAPEN = 1.
Bit 11	STACT [0]	Self-Test Active. STACT = 1 indicates that the RTMP is performing a built-in self-test.
Bit 10	BDCEN [X]	Broadcast Enable. BDCEN = 1 indicates that the RTMP will accept a 1553 broadcast command as a valid command.
Bit 9	TFGEN [1]	Terminal Flag Enable. When the RTMP is in the 1553B mode, TFGEN = 1 indicates that the Terminal Flag option is set. Mode code 00110 (Inhibit Terminal Flag) will clear this bit.
Bit 8	CHAEN [0]	1553 Channel A Enable. CHAEN = 1 indicates that Channel A is enabled and ready to process 1553 bus messages.
Bit 7	CHBEN [0]	1553 Channel B Enable. CHBEN = 1 indicates that Channel B is enabled and ready to process 1553 bus messages.
Bit 6	MSEL [X]	Mode Select. When MSEL = 1, the RTMP is in the 1553A mode of operation. MSEL = 0 indicates the RTMP is in the 1553B mode of operation.
Bit 5	MDRCV [0]	Mode Received. MDRCV = 0 indicates that the last valid 1553 command the RTMP received was a mode command.
Bit 4	XMTAC [0]	Transmitter Active. XMTAC = 1 indicates that the RTMP's transmitter is transmitting data.
Bit 3	ILCMD [X]	Illegal Command. ILCMD = 1 indicates that the last 1553 command the RTMP received was illegal. ILCMD is cleared when the host reads the OPS. In 1553A mode, this bit reflects input pin ILLCOM. In 1553B mode, this bit reflects either input pin ILLCOM or internal hardware. Internal illegalization is reviewed in table 2.
Bit 2	CHA/$\overline{B}$ [0]	Channel A or B. CHA/$\overline{B}$ = 1 indicates that the last valid 1553 command word the RTMP received was on Channel A. CHA/$\overline{B}$ = 0 indicates that the last valid command word was on Channel B.
Bit 1	VCMD [0]	Valid 1553 Command. VCMD = 1 indicates that the last command word the RTMP received was valid. VCMD is reset when the host reads the OPS.
Bit 0	OE [0]	Overrun Error (Framing Error). OE = 1 indicates that the RTMP has detected an overrun error. This bit is reset when the host performs an OPS read *unless* the error condition persists.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACC	VMPRO	ME	PE	STACT	BDCEN	TFGEN	CHAEN	CHBEN	MSEL	MDRCV	XMTAC	ILCMD	CHA/B	VCMD	OE
MSB															LSB

Figure 9. The Operational Status Register

3.6.2 Last 1553 Command Register (LCM)

The RTMP stores the last valid 1553 command word it received in the LCM. The only exception is if the RTMP is in the 1553B mode and it receives a Transmit Last Command Word mode code. Figure 10 shows the configuration of the LCM. (0410H after Master Reset.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TA4	TA3	TA2	TA1	TA0	T/R	SA4	SA3	SA2	SA1	SA0	WC4	WC3	WC2	WC1	WC0

MSB LSB

Figure 10. The Last Command Register

3.7 Write Only Register

The RTMP has one register that is write only. This register is the Stop Self-Test Register (SST). The host can terminate the RTMP's self-test execution by writing to the SST. When the host performs a write to the SST, the RTMP terminates all memory activity. The Self-Test Enable (STEN) bit in the CTL is also reset, and the Self-Test Active (STACT) bit in the OPS is reset. When writing to the SST, the 16-bit data word is a Don't Care.

4.0 Remote Terminal Interface Operation

The RTMP's remote terminal interface is based on a shared memory concept where the shared memory is the link between the MIL-STD-1553 data bus and the host subsystem (figure 11). All 1553 data, whether transmitted or received, must at one time be stored in this defined memory area. The RTMP accesses the shared memory area with a conventional Direct Memory Access (DMA) interface.

Since the RTMP can access data anywhere within the 64K memory space, the host has to specify exactly where in memory the data associated with each valid transmit or receive command word or mode code is located. The host specifies the 1553 data area locations by programming the RTMP's Base Pointer Data Register (BPD) and by initializing the 64-word Pointer Block. The BPD tells the RTMP where in memory the Pointer Block is located. The Pointer Block in turn specifies the location in memory where the data associated with each valid command word or mode code resides.

Therefore, to control the RTMP's operation, the host first programs the BPD to provide the RTMP with three essential pieces of information: (1) the location in memory of the 64-word Pointer Block; (2) the type of data buffer -- single or separate; and (3) the receive data buffer size. The host can update the Base Pointer Data Register if a new 64-word Pointer Block needs to be selected, but *do not* update the BPD while the RTMP is processing a message transaction. Figure 8 shows the BPD.

4.1 Programming the BPD

The host programs the ten most significant bits of the BPD (BPA15 - BPA6) to point to the starting address of the 64-word Pointer Block within the RTMP's 64K address space. The RTMP generates the least significant six address lines to determine which of the words within the 64-word Pointer Block to use for a specific 1553 transmission. The RTMP does this by detecting the T/$\overline{R}$ bit and the subaddress bits of the last 1553 command word (figure 12). Usually the six least significant address lines, BPA5-BPA0, are part of the T/$\overline{R}$ bit and subaddress or mode code bits of the last command word, respectively. In some cases, BPA5-BPA0 are forced to specific values: (1) when the RTMP stores the command word on the data buffer; (2) when the single buffer mode of operation is chosen; and (3) when a mode code is received.

The Data Buffer Mode bit, BUFSL, is the next bit in the BPD that the host programs. The state of BUFSL determines whether the RTMP stores the 1553 receive data in a single data buffer (BUFSL = 1) or in separate data buffers (BUFSL = 0).

Finally, the host programs bits BSIZ3-BSIZ0 in the BPD to tell the RTMP how large to make the separate data buffers. A formula determines the size of the data buffer(s): take the decimal equivalent of the binary number represented by BSIZ3-BSIZ0, where BSIZ3 is the MSB. This number, represented by X, can range in size from three to fifteen. The actual size of the data buffers is equal to 2^X. This means the data buffers can range from 8 to 32K words in length. In the single buffer mode, bits BSIZ3-BSIZ0 determine the size of this single buffer. In the separate buffer mode, *all* data buffers are the *same* size. This means the system designer must program the buffer size so the *largest* possible message the RTMP can receive over the 1553 bus fits within the programmed buffer size.

4.2 RTMP Pointer Block

The RTMP's Pointer Block is a contiguous block of 64, 16-bit words. The RTMP uses this block of data as the actual address pointer locations for the memory accesses associated with each 1553 message transaction. Therefore, the Pointer Block is divided into receive data pointers, of which one location is for the single buffer mode, transmit data pointers, a mode code command pointer location, and a location

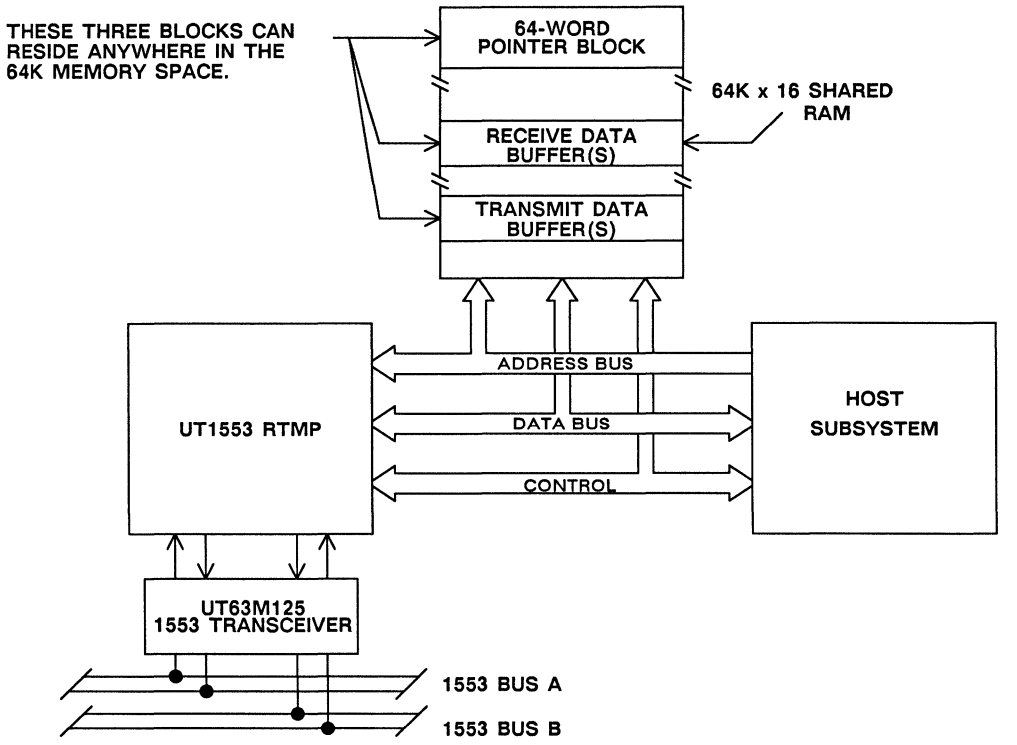


Figure 11. The Memory Link between the RTMP and the Host Subsystem

for the current 1553 command word (figure 13). The host must initialize the Pointer Block *before* enabling the RTMP's 1553 receivers.

The host can program the 16-bit pointer addresses that make up the Pointer Block to point to any memory location in the RTMP's 64K memory space. In this respect, the host has total flexibility to determine where in RAM it stores the actual transmit, receive, and mode code data. The RTMP's data storage flexibility allows the host to buffer 1553 receive messages and maintain data integrity.

The host can update the pointer data within the Pointer Block at any time, but the recommended procedure is for the host *not* to update the pointer data for 1553 receive command data while the RTMP is actively processing a message. To prevent this action, the host can program the RTMP to generate an end-of-activity interrupt for every valid 1553 message with associated data words. In addition, the host can read the Operational Status Register to determine if the RTMP is active.

The RTMP uses the present 1553 command word and the selected mode of operation, single or separate mode, to determine which pointer within the 64-word Pointer Block to use as an address pointer for the memory accesses during 1553 message activity. The 1553 command word T/$\overline{R}$ Bit and the subaddress bits, or the mode code bits for a mode command, specify the exact location of the address pointer in the Pointer Block for transmit, receive, and mode code command words. If the host has selected the single mode of operation, the RTMP forces selection of the address pointer stored in the single mode location for all receive commands. The RTMP stores the present command word in the first location of the Pointer Block.

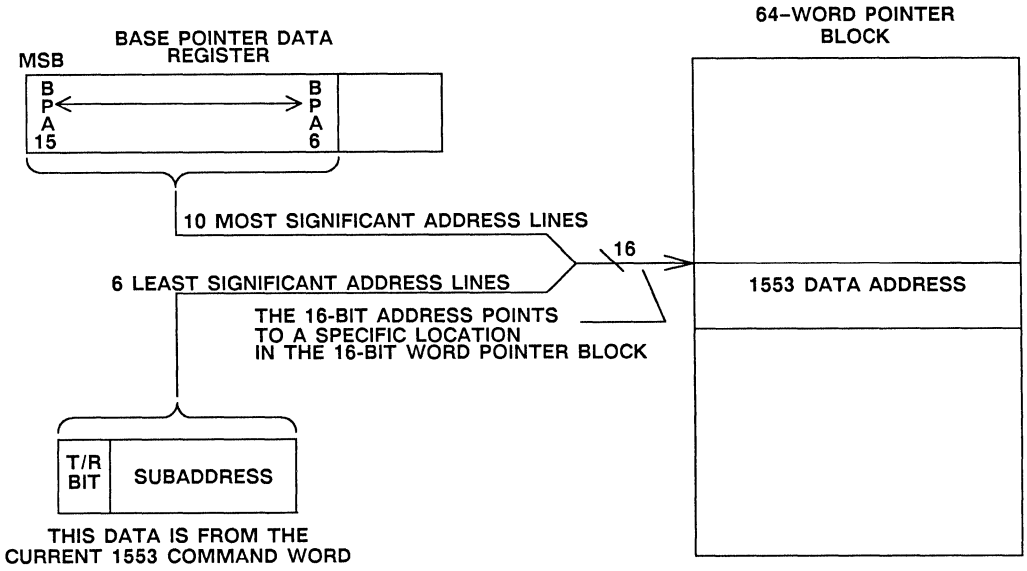


Figure 12. Construction of the Block Pointer Address (BPA) Bits

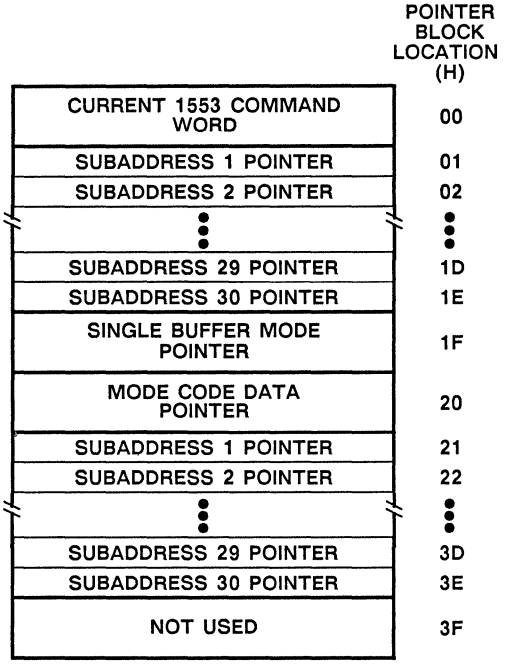


Figure 13. The 64-Word Pointer Block

4.3 Pointer Block Location Definitions
For the following description of the Pointer Block locations, please refer to figure 13.

Command Word Data – Location 00H of the Pointer Block contains the last valid 1553 command word the RTMP received. Bit times 4 through 19 (figure 14) of the 1553 command word are stored in bit positions 15 through 0, respectively. The RTMP updates this location with the most recent command word except when the RTMP is in the 1553B mode and it receives a Transmit Last Command mode code.

Separate Mode, Receive Data Pointers – Pointer Block address locations 1-30 (01H-1EH) contain the pointer values for each receive command word subaddress if the RTMP is operating in the separate mode (Bit 4 of the BPD = 0). The RTMP selects the address pointer data from one of these locations by using the subaddress of the most recent receive command word. The RTMP internally stores this pointer value. This stored pointer value points to the memory location where the RTMP stores the received data associated with this subaddress. After the RTMP has stored all data associated with this subaddress in memory, the RTMP stores the updated pointer value back into the selected location in the Pointer Block. The updated pointer value points to the next available location in memory.

Single Mode, Data Pointer – When the host selects the single mode of operation (bit 4 of the BPD = 1), the pointer value at location 31 (1FH) of the Pointer Block is the address the RTMP uses to store *all* 1553 receive data, regardless of the command word's subaddress. After the RTMP has stored all data associated with a 1553 receive command word, the RTMP stores an updated pointer value back into location 31 of the Pointer Block. The updated pointer value points to the next available location in memory.

Mode Code Pointer – The RTMP uses the pointer value stored in location 32 (20H) of the Pointer Block when it recognizes a valid mode code command with an associated data word. A mode code with data word is only valid when the RTMP is operating in the 1553B mode. When the RTMP is operating in the 1553A mode, it does not recognize or process any mode code with an associated data word.

- 1553A mode: No mode codes with data word allowed.
- 1553A mode: $\overline{MC}$/SA field = 00000 or 11111 is a mode code.
- 1553B mode: $\overline{MC}$/SA field = 00000 or 11111 is a mode code.

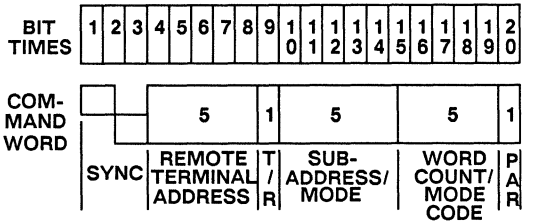
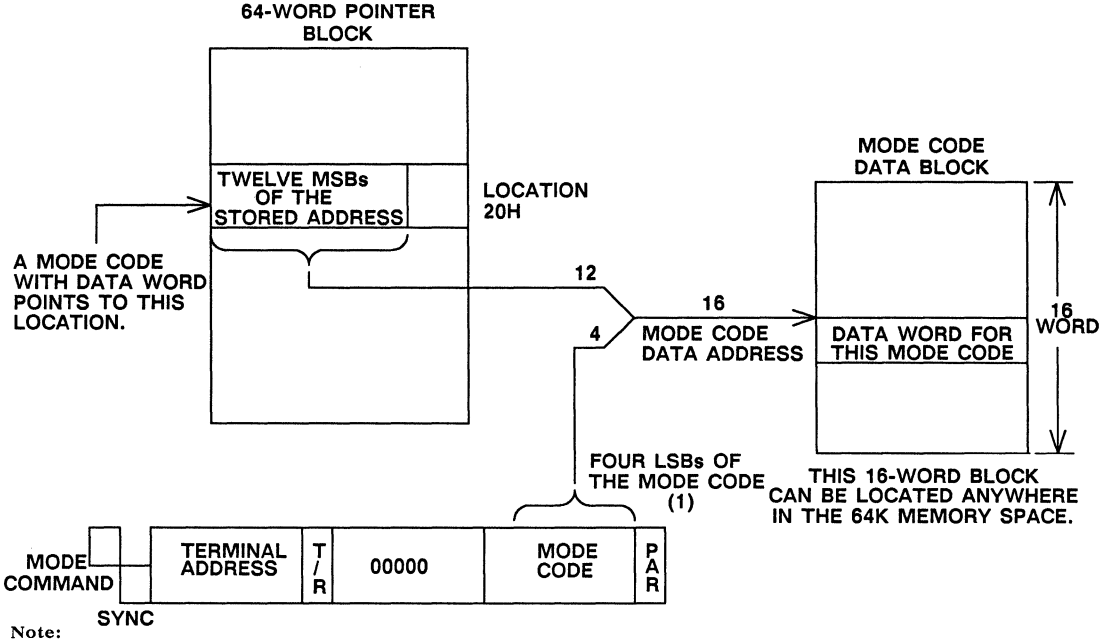


Figure 14. Command Word Bit-Time Definitions

The RTMP stores the pointer value from location 32 internally. The RTMP uses bits 15-4 of this pointer value to point to a memory location of a data block containing the data words associated with each mode code. Bits 3-0 of the pointer address are the four least significant bits of the mode code the RTMP received. These four bits specify the data word within this data block that the RTMP uses for this specific mode code. Figure 15 shows how the RTMP handles mode codes with associated data words.

Transmit Data Pointers – Pointer Block address locations 33 - 62 (21H-3EH) contain the pointer values for each of the 1553 transmit command word subaddresses. The RTMP selects the address pointer



Note:
0000 Transmit Vector Word
0001 Synchronize with data
0010 Transmit Last Command
0011 Transmit BIT Word
0100 Selected Transmitter Shutdown
0101 Override Selected Transmitter Shutdown

Figure 15. Mode Code with Associated Data Word Memory Mapping

data from one of these locations using the subaddress of the most recent valid command word. The RTMP internally stores this pointer value. This stored pointer value points to the memory location where the RTMP accesses the data to transmit with this subaddress. Every RTMP memory access for transmitted data increments the pointer value by one until the RTMP has transmitted all data. *Only* the host can update the pointer values stored in the Pointer Block. Therefore, if the host requires transmit data buffering, the host must control the pointer values stored in the Pointer Block. No identification word or time tag is associated with transmit commands.

Note that the RTMP does not use address location 63 (3FH) of the Pointer Block.

4.4 RTMP Data Storage

The RTMP uses two modes of allocating memory for 1553 receive messages: (1) the single buffer mode, and (2) the separate buffer mode. The user selects the buffer mode by programming bit 4 (BUFSL) of the Base Pointer Data (BPD) Register.

Both modes of operation are based on a ring-buffer type of memory mapping. Ring-buffer memory mapping means the RTMP stores all incoming 1553 data words sequentially in memory starting with an initial address value. The initial address value is one of the address values stored in the 64-word Block Pointer. Note that the initial pointer address must be set up on a boundary consistent with the chosen buffer size. Example: If the buffer size is sixteen (0010H), the initial pointer address must be some multiple of sixteen.

After the RTMP selects an address pointer within the Pointer Block, it loads the selected address pointer into an internal up-counter. Every time the RTMP performs a memory store operation, the up-counter increments by one. Therefore, the address pointer always points to the next sequential memory location. The RTMP continues to increment the address pointer until it reaches the programmed buffer size, which the user programs with bits 3 through 0 of the BPD (BSIZ3-BSIZ0). When the RTMP reaches the programmed buffer size, the internal up-counter ripples over; i.e., it returns to all zeros. At this time, the address pointer once again points to the initial block boundary memory address. To avoid the possibility of corrupting the initial receive data after the up-counter has rippled over, the user must read the data in the block before this event occurs. After the RTMP completes all memory accesses, the RTMP stores the updated address pointer in its initial 64-word Pointer Block location.

When the user chooses the single buffer mode of operation (BUFSL = 1), the RTMP always accesses the same address pointer within the 64-word Pointer Block for every 1553 receive command. Since the RTMP stores all 1553 data words in the same buffer during this mode of operation, the user needs to program the buffer size large enough to allow the RTMP to store several 1553 messages before it overwrites the data at the beginning of the buffer.

When the user chooses the separate buffer mode of operation (BUFSL = 0), the RTMP uses the subaddress of the present 1553 command word to select which of the address pointers within the 64-word Pointer Block it will use to store the received data. Therefore, the user can define up to 30 separate data buffers, one for each receive subaddress, anywhere in memory. The starting memory location of each buffer is stored in the receive section of the Pointer Block. In the separate buffer mode, the user needs to program the buffer size so it is large enough to keep the RTMP from overwriting the current data in any of the separate data buffers if the RTMP receives a new message with the same subaddress before the host can read the data from that data buffer.

Figures 16a and 16b show how each mode operates for a sample receive transmission.

In addition to the data words associated with a receive command, the RTMP also stores two additional words, an identification word, which the RTMP stores immediately before the data words, and a time tag word, which the RTMP stores immediately after the data words. The identification word is the 1553 command word associated with the data in this data block, and the time tag word is the output of the Time Tag Register. Command word bit time four (figure 14) is stored as the MSB of the identification word and command word bit time 19 is stored as the LSB of the identification word. Therefore, each receive message requires two additional memory locations to allow the RTMP to store the message successfully.

For example, a receive message with twelve data words actually requires fourteen memory locations. Therefore, the user needs to program the buffer size to be sixteen (2^4) since buffer sizes defined in the BPD can only be a length of two raised to an integer power from three to fifteen. If, on the other hand, a receive message has fifteen data words, this message actually requires seventeen memory locations. In this case, the user must program a buffer size of 32 (2^5), since this is the next power of two that accommodates seventeen data words.

In the separate buffer mode of operation, the RTMP makes all buffers the same length. Therefore, the host must be sure to program the RTMP so the buffer

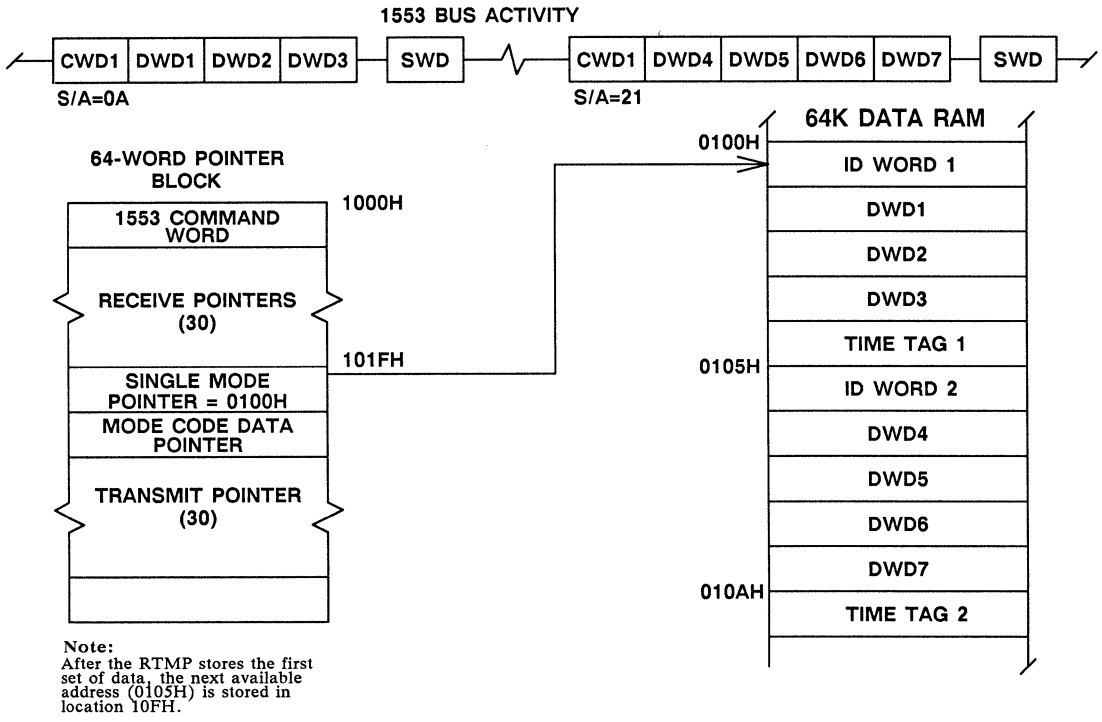


Figure 16a. RTMP Single Buffer Mode of Operation

size is large enough to accommodate the largest message the RTMP can receive for any subaddress.

4.5 RTMP Interrupt Functions

The RTMP has two outputs that provide the host subsystem processor with interrupt control capability: (1) the End of Receive/Transmit Message Activity ($\overline{\text{EORT}}$) interrupt; and (2) the End of Mode Code Activity ($\overline{\text{EOMC}}$) interrupt. The host subsystem can use these two outputs in conjunction with the information the Operational Status Register (OPS) provides to determine the condition of the RTMP after an interrupt condition occurs.

The End of Receive/Transmit Message Activity ($\overline{\text{EORT}}$) interrupt is a maskable interrupt the user can select to occur (1) only when the 1553 receive command activity is complete; (2) only when the 1553 transmit command activity is complete; or (3) when either receive *or* transmit command activity is complete. The host masks the $\overline{\text{EORT}}$ interrupt by resetting the appropriate bits (bit 11-IM1 and bit 10-IM2) in the RTMP's Control Register (CTL). IM1 = 0 keeps $\overline{\text{EORT}}$ from occurring at the end of receive command activity. IM2 = 0 keeps $\overline{\text{EORT}}$ from occurring at the end of transmit command activity. If the host does not mask either IM1 or IM2, the $\overline{\text{EORT}}$ interrupt pulses low. This pulse occurs at the end of either the receive or transmit command activity.

The End of Mode Code Activity ($\overline{\text{EOMC}}$) interrupt is a non-maskable interrupt. The $\overline{\text{EOMC}}$ interrupt, like the $\overline{\text{EORT}}$ interrupt, is also a low pulse, except the $\overline{\text{EOMC}}$ interrupt occurs at the end of all memory accesses associated with any 1553 mode code command. Both $\overline{\text{EORT}}$ and $\overline{\text{EOMC}}$ require an external pull-up resistor and, if necessary, the user can wire-OR the two outputs together to form a composite RTMP interrupt.

If any one of the following conditions occurs during normal RTMP operation, the RTMP does not generate either the $\overline{\text{EORT}}$ or the $\overline{\text{EOMC}}$ interrupt: (1) if a Message Error occurs; (2) if a Framing (Overrun) Error occurs; (3) if the RTMP receives an illegal 1553 command; (4) if the RTMP receives a superseding command word; or (5) if the Busy bit in the Control Register is set (1553B mode of operation only).

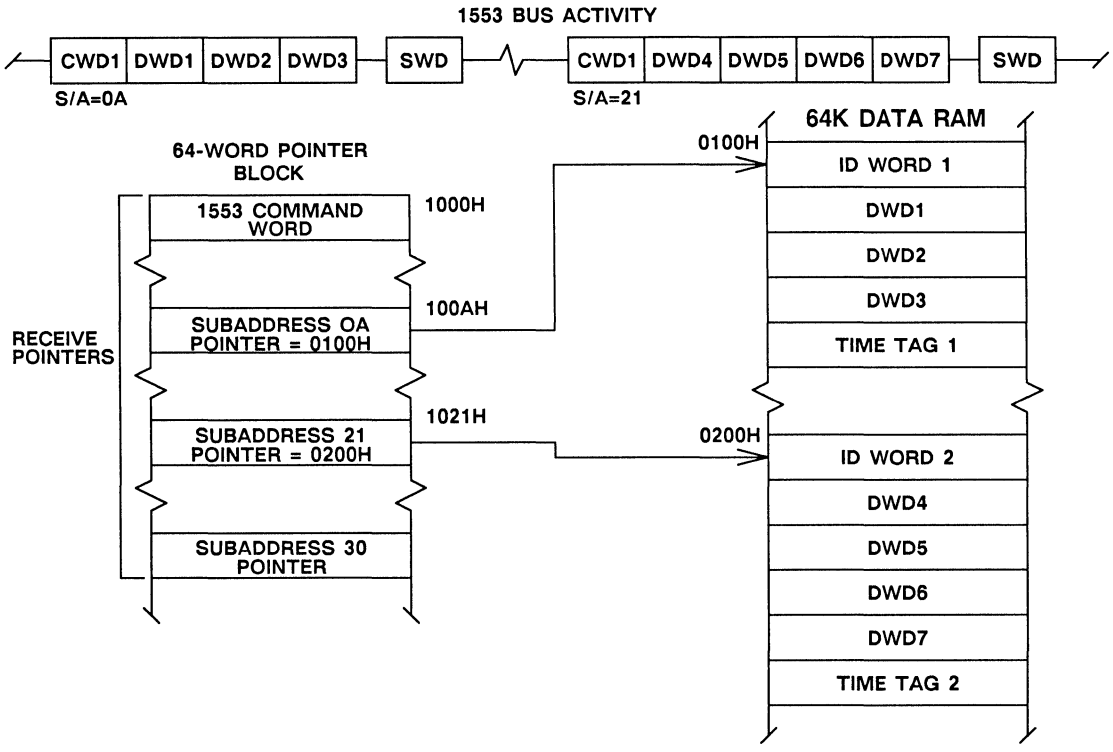


Figure 16b. RTMP Separate Buffer Mode of Operation

4.6 RTMP Error Detection Capabilities

The RTMP provides the host with significant error-detection capabilities. The RTMP can detect the following types of errors:

- Terminal Address Parity Errors
- Framing or Overrun Errors
- 1553 Message Errors

4.6.1 Terminal Address Parity Errors

The RTMP can check the the Terminal Address parity inputs (RTA4-RTA0) when the Terminal Address Parity Enable (TAPEN) input is active high. If TAPEN = 1, then RTA4-RTA0 and the Remote Terminal Parity (RTPTY) input must provide the RTMP with odd parity, or the RTMP flags a Terminal Address Parity Error. For example:

- If the TA = 01000, then RTPTY must equal 0 to prevent a parity error.
- If the TA = 00110, then RTPTY must equal 1 to prevent a parity error.

If the RTMP detects a Terminal Address Parity Error, this error prevents the RTMP from recognizing any valid commands on either channel, preventing the RTMP from responding to a 1553 command word not actually intended for this remote terminal.

4.6.2 Framing or Overrun Errors

A framing error occurs when the RTMP is not permitted to access memory at a sufficient rate to service the requirements of the 1553 data bus. For receive messages, after the RTMP generates a DMA Request ($\overline{\text{DMAR}}$) signal, the host must generate a DMA Grant ($\overline{\text{DMAG}}$) signal before the RTMP receives the next incoming data word to prevent a framing error. For transmit messages, after the RTMP generates $\overline{\text{DMAR}}$, the host must generate a $\overline{\text{DMAG}}$ before the RTMP completes transmitting the previous 1553 data word to prevent a framing error. When a framing error occurs during a receive command, all RTMP memory accesses cease. When a framing error occurs during a transmit command, the RTMP terminates all data transmissions.

The worst-case timing for receive commands requires the RTMP to make four memory accesses within 40 µs. The worst-case timing for transmit commands

depends on whether the RTMP is operating in 1553B or 1553A mode. When the RTMP is operating in the 1553A mode, the worst-case timing requires the RTMP to make three memory accesses within 22 μs; when in the 1553B mode, the worst-case timing requires the RTMP to make three memory accesses within 28 μs. The difference in the timing here is due to the difference in the status word response time between 1553A and 1553B.

The worst-case timing for a transmit command consists of the remote terminal response time, which is mode-dependent, and the time it takes to transmit the 1553 status word (20 μs). During this time, the RTMP must fetch the address pointer from the 64-word Pointer Block, store the 1553 command word in the first location of the Pointer Block, then fetch the first data word from memory before it completes transmitting the status word.

When the RTMP detects a receive command word, it must make four separate memory accesses before it receives the second 1553 data word. The RTMP must (1) fetch the appropriate address pointer from the 64-word Pointer Block; (2) store the 1553 command word in the first location of the Pointer Block; (3) store the identification word at the memory location pointed to by the address pointer; and (4) store the first received data word in the memory location immediately after the identification word.

4.6.3 1553 Message Errors

The RTMP sets the Message Error bit in the 1553 status word and also asserts the MERR output if the RTMP detects a failure in one of the following areas.

1553 Data Word Tests:

- Invalid sync field for any data word
- Incorrect Manchester II format
- Incorrect data word or command word parity
- Too few data bits per word
- Too many data bits per word
- Too few data words per message
- Too many data words per message (1553B mode only)
- Non-contiguous data words

RT-to-RT Transfer Tests:
During an RT-to-RT command sequence, the RTMP monitors the 1553 bus and compares the terminal address of the transmit command word with the terminal address of the status word from the transmitting RT. The RTMP declares the RT-to-RT transfer invalid if no match occurs. The RTMP then sets the Message Error bit. The RTMP also sets the Message Error bit if it detects one of the following errors:

- Data word transmission before the status word transmission
- Excessive time before the transmitting RT sends the status word
- Any deviation from the proper sequence of events for RT-to-RT transfers

Illegal Mode Commands:
When the RTMP is operating in the 1553A mode, it does not automatically declare any received mode code as illegal. To illegalize any mode code, the RTMP outputs the Mode Code/Subaddress outputs (MCSA0-MCSA4) along with the Mode Code/Subaddress status signal ($\overline{MC}$/SA). The host uses these signals to decode when the RTMP receives a mode code and what mode code was received. If the mode code is illegal for this application, the host asserts the RTMP's Illegal Command (ILLCOM) input and the Message Error bit is set in the RTMP's 1553 status word response.

When the RTMP is operating in the 1553B mode, it automatically illegalizes the following mode codes:

- Mode Code 00000 - Dynamic Bus Control
- Reserved Mode Codes 01001 through 01111 (no associated data word)
- Reserved Mode Codes 10110 through 11111 (with associated data word)

In these cases, the RTMP status word response has the Message Error bit set.

4.7 RTMP Self-Test Functions

The RTMP performs a self-test by wrapping the encoder output back into the decoder inputs. Self-test is either internal or external to the RTMP. An internal self-test wraps the RTMP encoder output back into the decoder input via a multiplexer internal to the RTMP. External self-test loops the RTMP encoder back into the decoder via the bus transceiver. In normal operation the transceiver transmitter is connected to the receiver. This connection closes the loop from the encoder to decoder. Self-test has the ability to check the function of Channel A and B, command recognition logic, data transfer logic, and memory address control.

The RTMP's self-test capability is based on the fact that the MIL-STD-1553 status word sync pulse is identical to the command word sync pulse. Thus, if the status from the encoder is fed back to the decoder, the RTMP will recognize the status word as a command and thus cause the RTMP to process the validated command word. After the host invokes self-test, the RTMP self-test logic forces the transmission of a status word even though the RTMP has not received a valid command. By reading the RTMP's Operational Status Register the host can monitor self-test. The host compares self-test results to expected results; data mismatches result in self-test failure. Normal operation is inhibited during self-test.

Anytime during the RTMP's self-test execution, the host can monitor the Operational Status Register's (OPS) Self-Test Active bit (STACT), bit 11. STACT=1 signifies that the RTMP is performing a self-test. STACT is active until the RTMP completes all self-test memory activity. If the host has enabled the activity interrupts ($\overline{EORT}$ and $\overline{EOMC}$), $\overline{EOMC}$ occurs after the memory fetch for the data word that the RTMP wraps around during the self-test, and $\overline{EORT}$ occurs when the self-test is complete. Do not send mode code commands in self-test while operating in the A mode. In B mode the RTMP can verify 3 mode codes (Synchronize with Data, Selected Transmitter Shutdown, Override Selected Transmitter Shutdown). All of these mode codes have the T/$\overline{R}$ bit set to zero.

Note: When monitoring self-test via the Operational Status Register, each OPS read will clear any bits the RTMP set.

Control and invoke self-test by using the TEST input pin, along with Control Register bits 12, 13, 14, and 15 (i.e. STCS, STEN, CHBEN, and CHAEN). Control Register bit 12, Self-test Channel Select (STCS), determines whether internal self-test is performed on Channel A or Channel B. Control external self-test channel select via Control Register bit 12 (STCS) and Control Register bit 14 or bit 15. These three bits determine which channel is active during self-test. STCS identifies which channel, bit 15 or bit 14, enables the hardware. Disable Channels A and B, via Control Register bits 15 and 14, for internal self-test. Control Register bit 13, Self-test Enable, initiates the self-test routine. See Control Register bit descriptions for more information on the function of bits 12 and 13. Input pin TEST determines whether the self-test is external or internal (TEST=1 external, TEST=0 internal).

Note: External self-test will corrupt an operational bus since a remote terminal transmits command word information. Also note that bus activity received by the RTMP decoder (specifically command word validation) will corrupt self-test .

After the host processor enables a self-test, the RTMP's internal self-test logic remains in a "wait" state until the RTMP is not receiving or transmitting any information. Once the RTMP determines that there is no 1553 bus activity, the STEN bit of the Control Register is reset and self-test begins.

Essentially, the self-test makes the RTMP behave as if it just received a Transmit Vector Word mode code. The Transmit Vector Word mode code tells the RTMP to transmit a status word and one associated data word. The RTMP wraps this status word and data word back around into the channel under test. Since a status word and a command word have the same sync pulse, when the RTMP decoder sees this status word, the receiver thinks it has received a valid command from the 1553 data bus.

The status word the RTMP transmits during the self-test, which is wrapped around to the decoder as the 1553 command word, is host-programmable. The RTMP forces bit 11 of this status word to logic zero, hence the status word is recognized as a receive command word. All commands used in self-test are receive commands. The host can program bits 1 through 10 of this status word by writing to bits 0 through 9 of the Control Register. When the RTMP's decoder sees these ten bits in the wrapped-around command word, these bits are decoded as the command word's subaddress and word-count fields. Only one data word is transmitted with the status word, therefore setting the word count field not equal to 1 results in a message error.

The RTMP accesses the data word that it wraps around during the self-test from memory just as it would any other data word. The RTMP reads the data word for the wrap-around test from the memory location to which the address in the Mode Code Pointer (location 20H) points. The twelve most significant bits of this address come from the data programmed in the Mode Code Pointer location. The RTMP always the four least significant address bits to zero (Transmit Vector Word Mode Code).

The RTMP's decoder on the selected test channel recognizes the status word that is wrapped around during the self-test as a valid 1553 receive command word. The RTMP's internal sequencer and error detection logic begin processing the received command word and its associated data in a normal sequence. The host programs the outgoing status/command word to receive one data word at a specific subaddress. Then the RTMP goes to the location in the 64-word Pointer Block corresponding to the actual memory location subaddress where the RTMP stores the data word wrapped around during the self-test, if the host has chosen the separate buffer mode of operation. If the host has selected the single buffer mode of operation, the RTMP stores the wrapped-around data word at the memory location to which the Single Mode Data Pointer in the 64-word Pointer Block points. The RTMP suppresses transmitting a status word after receiving the wrapped-around command word and data word during self-test execution. At this time, the self-test terminates and the RTMP resets the Self-Test Active (STACT) bit in the Operational Status Register.

The host has complete control over the RTMP's self-test processing and can terminate a self-test at any time by performing a write to the Stop Self-test Register (SST). When the host writes to the SST, the

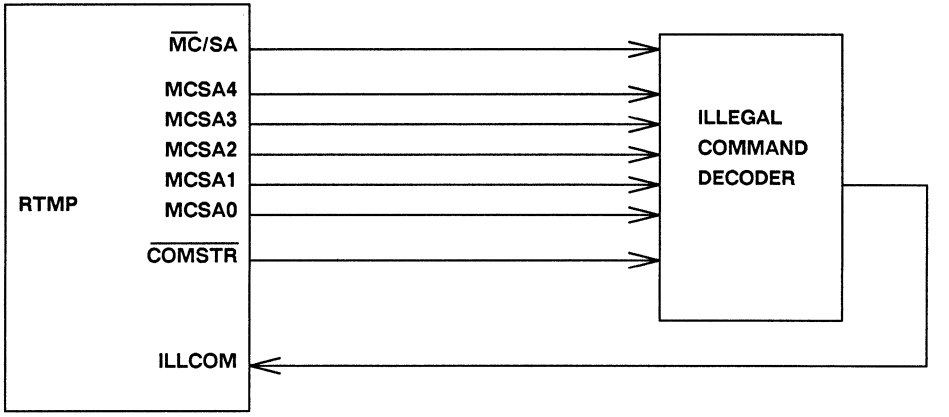


Figure 17. Mode Code/Subaddress Illegalization Circuit

RTMP terminates all memory activity, resets STEN, and resets the Self-Test Active (STACT) bit in the OPS.

5.0 1553A And 1553B Modes Of Operation

The RTMP provides two modes of operation -- one to meet the requirements of MIL-STD-1553A and another to meet the requirements of MIL-STD-1553B. The user selects the mode of operation for the specific application by programming the 1553 mode select input (PRA/$\overline{B}$). When the host sets PRA/$\overline{B}$ = 1, the RTMP is in the 1553A mode of operation. When PRA/$\overline{B}$ = 0, the RTMP is in the 1553B mode of operation.

In either the 1553A or 1553B mode, the RTMP's basic operation remains the same with three major differences among the modes of operation. These differences are: status word bit definitions, mode code responses, and status word response time.

5.1 Status Word Bit Definition

When the RTMP operates in the 1553A mode, the only bits of the status word it defines are the Message Error bit (bit 11) and the Terminal Flag bit (bit 1). The RTMP does not specifically define the rest of the bits in the status word (bits 2 through 10). The user can define these bits for a specific application by programming the corresponding bits in the Control Register (CTL bits 1-9).

In the 1553B mode of operation, the RTMP defines all status word bits in the CTL that correspond to a specific function in the transmitted 1553 status word. The host controls some of the status word bits in the CTL, namely the Instrumentation, Service Request, Broadcast, Busy, Subsystem Flag, and Terminal Flag bits. Finally, if the host sets any undefined status word bits in the CTL, the RTMP masks these bits (i.e., sets to logic zero) before they can be transmitted in the status word.

5.2 Mode Code Responses

When the RTMP operates in the 1553A mode, it does not internally detect any mode codes as being illegal. The RTMP recognizes all other mode codes as being valid, and responds to these mode codes with a status word only. The 1553A mode of operation does not support mode codes with an associated data word.

- Do not send mode codes with data to the RTMP when operating in the 1553A mode.
- No auto-execution of mode codes is performed in the 1553A mode of operation.

The host can illegalize any mode code by decoding the Mode Code/Subaddress outputs (MCSA0-4) and the $\overline{MC}$/SA output with an external device (figure 17). The host can program the external decoder to generate the Illegal Command (ILLCOM) input whenever the RTMP receives a mode code that the system declares illegal. Asserting ILLCOM causes the RTMP to transmit a status word with the Message Error bit set. Illegalization does not stop the auto-execution of mode codes.

In the 1553B mode of operation, the RTMP internally detects the Dynamic Bus Control mode code and all reserved mode codes as illegal. The host can illegalize any other mode code by setting the ILLCOM input, just as described for the 1553A mode of operation.

Table 2. 1553B Mode Code Operation

Mode Code (7)	Number	Legal (L)/ Illegal (I)	Operation (see below)	1553A Mode	Notes
Dynamic Bus Control	00000	I	1	L(2)	
Synchronize	00001	L	2	L(2)	
Transmit Status Word	00010	L	3	L(2)	
Initiate Self-Test	00011	L	2	L(2)	
Transmitter Shutdown	00100	L	3	L(2)	
Override Transmitter Shutdown	00101	L	3	L(2)	
Inhibit Terminal Flag Bit	00110	L	3	L(2)	
Override Inhibit Terminal Flag Bit	00111	L	3	L(2)	
Reset Remote Terminal	01000	L	2	L(2)	
Reserved	01001 01111	I	1	L(2)	
Transmit Vector Word	10000	L	4	L(2)	
Synchronize	10001	L	4	N/A	No mode code with data
Transmit Last Command	10010	L	5	L(2)	Status word only
Transmit Bit Word	10011	L	4	L(2)	
Selected Transmitter Shutdown	10100	L	4	N/A	No mode code with data
Override Selected Transmitter Shutdown (6)	10101	L	4	N/A	No mode code with data
Reserved	10110-11111	I	1	L(2)	

Definition of operations:

1. The RTMP sets the Message Error bit, sends a status word, and stores the 1553 command word, but takes no internal action.
2. The RTMP sends a status word, stores the 1553 command word, but takes no internal action.
3. The RTMP sends a status word, stores the 1553 command word, and takes the appropriate internal action.
4. The RTMP sends a status word, stores the 1553 command word, accesses memory for the associated data word, but takes no internal action.
5. The RTMP sends a status word, updates the 1553 command word in an internal register, accesses memory for the associated data word, but takes no internal action.
6. The RTMP must receive an Override Selected Transmitter Shutdown before the channel that was disabled can be enabled.
7. Undefined mode codes in MIL-STD-1553B are illegalized.

Table 2 shows the action the RTMP takes for each of the mode codes.

5.3 Status Word Response Time

When the RTMP operates in the 1553B mode, it checks to see if too many data words are received while processing a receive command. While operating in the 1553A mode, the RTMP does not make this check. Therefore, the status word response time for the RTMP in the 1553A mode is different from the status word response time in the 1553B mode.

Operating in the 1553A mode, the RTMP's status word response time is from 4.25 to 5.75 μs (reference figure 29). This time is measured from midbit of the command word parity bit to midbit of the status word sync pulse.

Operating in the 1553B mode, the RTMP's status word response time is from 9.25 to 10 μs (reference figure 29). This time is also measured from midbit of the command word parity bit to midbit of the status word sync pulse.

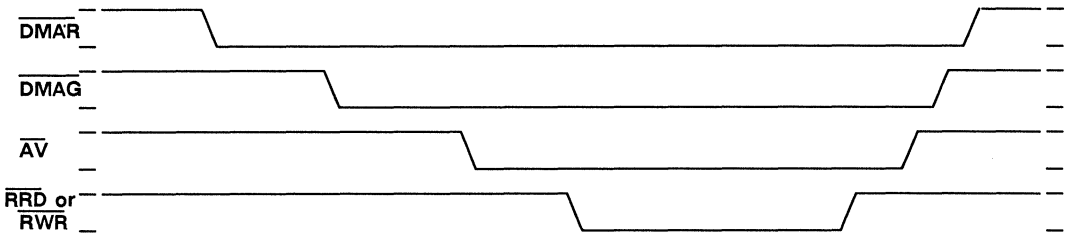


Figure 18. General RTMP DMA Timing Relationships

These midbit-to-midbit response times are measured from the midbit time of the parity bit at the RTMP's inputs to the midbit time of the sync pulse at the RTMP's outputs. These measurements do not include any delays attributable to external devices such as transformers or transceivers.

6.0 RTMP System Interface

The RTMP system interface consists of the major functional interfaces between the host processor and the RTMP. These interfaces (1) allow the host to control the functions of the RTMP and determine its operational status; (2) permit the RTMP and the host to exchange the information from the 1553 data bus; and (3) allow the host to select the RTMP's terminal address.

The system interface provides a description of the following aspects of the RTMP's operation:

- Assigning the RTMP's terminal address
- Controlling the RTMP's DMA interface
- Interfacing with the RTMP's internal registers

6.1 Assigning the Terminal Address

The RTMP's terminal address input pins (RTA0-RTA4) are static inputs. This means the RTMP does not require a latching signal of any sort to assign the RTMP its terminal address. The host simply has to present the correct terminal address on inputs RTA0-RTA4 and the RTMP recognizes this as the terminal address for all 1553 command words.

The RTMP can check the parity of the assigned terminal address by using the Remote Terminal Parity input (RTPTY) and the Terminal Address Parity Enable input (TAPEN) in conjunction with the RTA0-RTA4 inputs. In most applications, it is important that the host enable the terminal address parity checking input to prevent the RTMP from inadvertently responding to a command word not meant for it. If the host requires the RTMP to check the parity of the terminal address, TAPEN must be high and RTPTY must provide the RTMP with odd parity (an odd number of high inputs) for the assigned terminal address.

If for some reason, such as a broken or missing terminal address input or an inadvertent terminal address change, the RTMP detects bad parity, it ignores all incoming command words. The RTMP also sets bit 12 in the Operational Status Register, the Parity Error (PAERR) bit. If the host can re-establish the correct terminal address and parity, the RTMP resumes communication on the 1553 data bus.

6.2 Controlling the DMA Interface

The RTMP has a standard DMA interface that consists of a set of three arbitration signals between the RTMP and the host processor: (1) DMA Request ($\overline{\text{DMAR}}$); (2) DMA Grant ($\overline{\text{DMAG}}$); and (3) DMA Enable (DMAEN). After the bus controller grants the RTMP control of the address and data buses, the RTMP uses three additional signals to control the shared memory: (1) RAM Read ($\overline{\text{RRD}}$); (2) RAM Write ($\overline{\text{RWR}}$); and (3) Address Valid ($\overline{\text{AV}}$). Figure 18 shows the general relationship of these signals during bus arbitration and data acquisition.

When the RTMP requires access to the shared memory, it initiates the bus arbitration sequence by generating $\overline{\text{DMAR}}$. For a transmit message, the RTMP generates $\overline{\text{DMAR}}$ when the internal transmitter buffer is empty. Therefore, the RTMP must be granted control of the data bus before the current data word transmission is finished or an overrun error occurs. The RTMP continues to generate $\overline{\text{DMAR}}$s until it has transmitted the proper number of data words or until an error condition occurs. For a receive message, the RTMP generates $\overline{\text{DMAR}}$ after a received data word is validated. In this situation, the RTMP must receive a bus grant signal before receiving the next data word or an overrun error occurs.

After the RTMP generates $\overline{\text{DMAR}}$, it waits until the bus master generates $\overline{\text{DMAG}}$. After the bus master generates $\overline{\text{DMAG}}$, bus arbitration is complete (provided DMAEN is high) and the RTMP takes

control of the address and data buses by first enabling the address three-state buffers. After the address lines have settled, the RTMP generates $\overline{AV}$ signifying the address is valid.

The next step in the sequence depends on whether the present memory access is for a receive or a transmit message. If the RTMP is processing a receive command, $\overline{RWR}$ goes active allowing the RTMP to write the received 1553 data to the shared memory. If, on the other hand, the RTMP is processing a transmit command, $\overline{RRD}$ goes active allowing the RTMP to access data from the shared memory. In either case, the data is read from or written to shared memory on the rising edge of $\overline{RRD}$ or $\overline{RWR}$, respectively, thus signifying the end of this memory access cycle.

If a memory access bus cycle is pending, i.e., the RTMP has generated $\overline{DMAR}$ but the bus controller has not acknowledged with a $\overline{DMAG}$, four events can terminate the current bus cycle: (1) the RTMP receives a superseding 1553 command word on the same or opposite channel; (2) an overrun error occurs; (3) a message error occurs; or (4) a write to the Stop Self-Test (SST) Register occurs.

6.3 Interfacing with the RTMP's Internal Registers

The host interfaces with the RTMP's six internal registers to control the RTMP's operation and to determine the RTMP's operational status while the RTMP is active. Six signals between the host and the RTMP control this interface: (1) the three least significant address lines (A2-A0); (2) Chip Select ($\overline{CS}$); (3) register read ($\overline{RD}$); and (4) register write ($\overline{WR}$). Figure 19 shows the general timing relationship of these signals. The RTMP's three least significant address bits (A2-A0) are bidirectional. When the host drives these inputs along with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, the RTMP uses this information to select which of its six internal registers the host will access during this operation (table 1).

Before the host attempts to access the RTMP's internal registers, it must make sure the RTMP is not performing a DMA operation. Accessing the RTMP's internal registers during a DMA operation causes data corruption because the $\overline{CS}$ input takes precedence over all other RTMP memory operations and causes the RTMP immediately to place its address and data buffers in a high-impedance state. Therefore, after the bus master has granted the RTMP control of the buses, the host *must not* attempt any internal register reads or writes until the RTMP completes its memory operation.

The interface timing between the host and the RTMP's internal registers follows standard microprocessor interfacing techniques. After the host has determined that the RTMP is not using the address and data buses, it generates the address for the selected RTMP internal register. The host asserts $\overline{CS}$, informing the RTMP that an internal register operation is about to occur. The RTMP responds by placing its address and data bus signals in a high-impedance state and allowing the three least significant address lines to become inputs.

At this point, the host asserts either $\overline{RD}$ or $\overline{WR}$ telling the RTMP the direction of the data flow. The host completes the current register access cycle on the rising edge of $\overline{WR}$ for data input operations and on the rising edge of $\overline{RD}$ for data output operations.

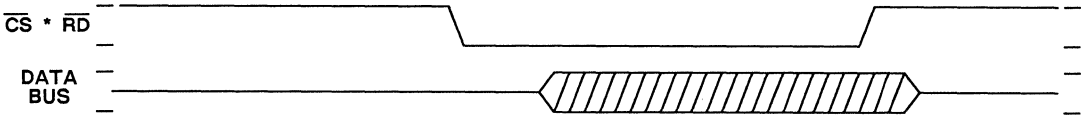


Figure 19a. General RTMP Register Read Timing

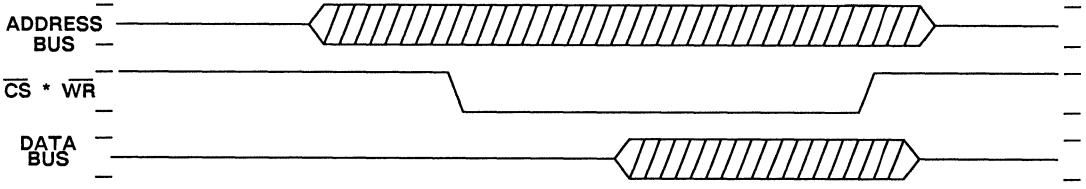


Figure 19b. General RTMP Register Write Timing

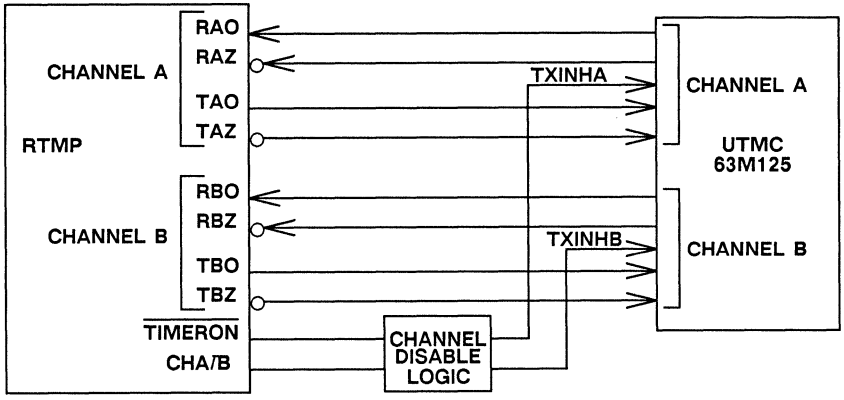


Figure 20. RTMP-to-Transceiver Interface Diagram

6.4 RTMP Hardware Interface

6.4.1 The RTMP - 1553 Transceiver Interface

The RTMP's Manchester II encoder/decoders interface directly with the 1553 bus transceiver as shown in figure 20. The RTMP uses the RAO, RAZ, TAO, and TAZ pins to interface with bus Channel A. The RTMP uses the RBO, RBZ, TBO, and TBZ pins to interface with bus Channel B. The RTMP's encoder outputs (TAO, TAZ, TBO, and TBZ) are low when they are inactive.

In addition to the signals listed above, the RTMP also provides two signals that assist the RTMP in meeting the MIL-STD-1553 fail-safe timer requirements. These signals are the Timer On ($\overline{\text{TIMERON}}$) and the Channel A/B (CHA/$\overline{\text{B}}$) outputs. These signals are also shown in figure 20.

6.4.2 The RTMP DMA Interface

When the RTMP is in its standard DMA configuration, its address, data, and control signals are directly connected to each other as shown in figure 21. The RTMP's signals remain in a high-impedance state until the RTMP is granted control of the buses after DMA arbitration has occurred, or until the host asserts $\overline{\text{CS}}$ signifying that the host is about to access one of the RTMP's internal registers.

The host can disable all DMA transfers by setting the Busy bit (bit 3) of the Control Register (CTL).

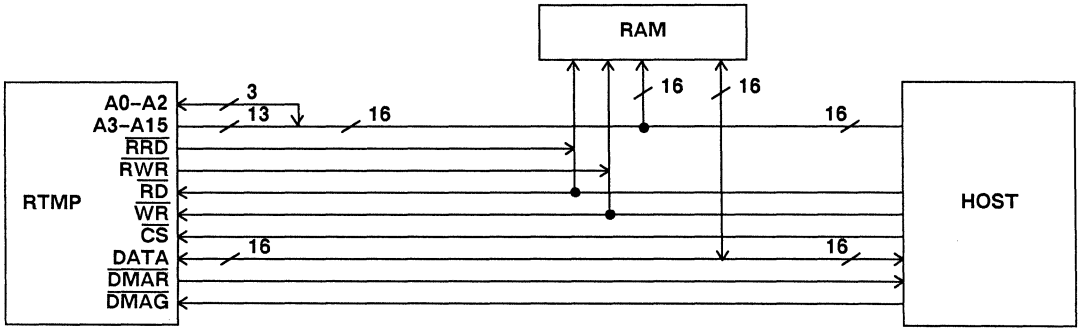


Figure 21. RTMP-to-Host Interface

7.0 Operating Conditions*

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
$V_{I/O}$	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	300	mW
Θ_{JC}	Thermal resistance, junction-to-case	10	°C/W
T_J	Maximum junction temperature	+175	°C

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
T_A	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ±.01%	MHz
V_{IN}	DC input voltage	0 to V_{DD}	V

8.0 DC Electrical Characteristics

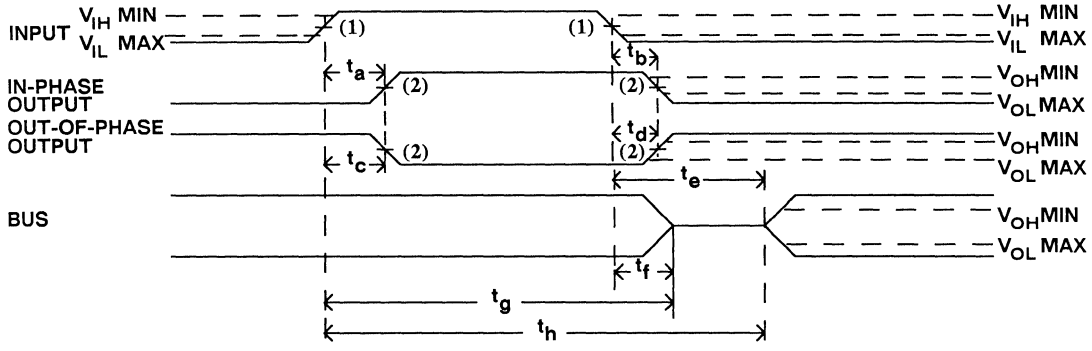
(V_{DD} = 5.0 V ± 10%; -55°C < T_A < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs			0.8	V
V_{IH}	High-level input voltage TTL inputs		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ V_{IN} = 2.4 V $V_{IN} = V_{SS}$	 -1 100 -1000	 1 1000 400 -100	 µA µA µA µA
V_{OL}	Low-level output voltage TTL outputs	I_{OL} = 3.2 mA		0.4	V
V_{OH}	High-level output voltage TTL outputs	I_{OH} = -400 µA	2.4		V
I_{OZ}	Three-state output leakage current TTL outputs	$V_O = V_{DD}$ or V_{SS}	-10	+10	µA
I_{OS}	Short-circuit output current (2, 5)	V_{DD} = 5.5 V, $V_O = V_{DD}$ V_{DD} = 5.5 V, V_O = 0 V	 -100	100	mA mA
C_{IN}	Input capacitance (1)	F = 1 MHz @ 0 V		10	pF
C_{OUT}	Output capacitance (1)	F = 1 MHz @ 0 V		15	pF
C_{IO}	Bidirect I/O capacitance (1)	F = 1 MHz @ 0 V		20	pF
I_{DD}	Average operating current (3, 5)	F = 12 MHz, C_L = 50 pF		50	mA
QI_{DD}	Quiescent current	See Note 4		1	mA

Notes:

1. Measured only for initial qualification and after process or design changes which may affect input/output capacitance.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 amp can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large current surge.
4. All inputs with internal pull-ups and pull-downs should be left floating. All other inputs should be tied high or low.
5. Guaranteed by design or characterization.

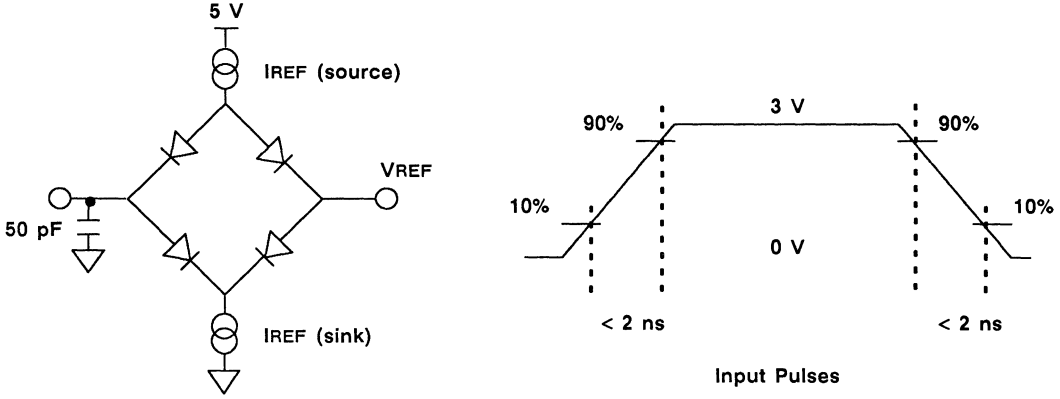
9.0 AC Electrical Characteristics



SYMBOL	PARAMETER
t_a	INPUT ↑ to response ↑
t_b	INPUT ↓ to response ↓
t_c	INPUT ↑ to response ↓
t_d	INPUT ↓ to response ↑
t_e	INPUT ↓ to data valid
t_f	INPUT ↓ to high Z
t_g	INPUT ↑ to high Z
t_h	INPUT ↑ to data valid

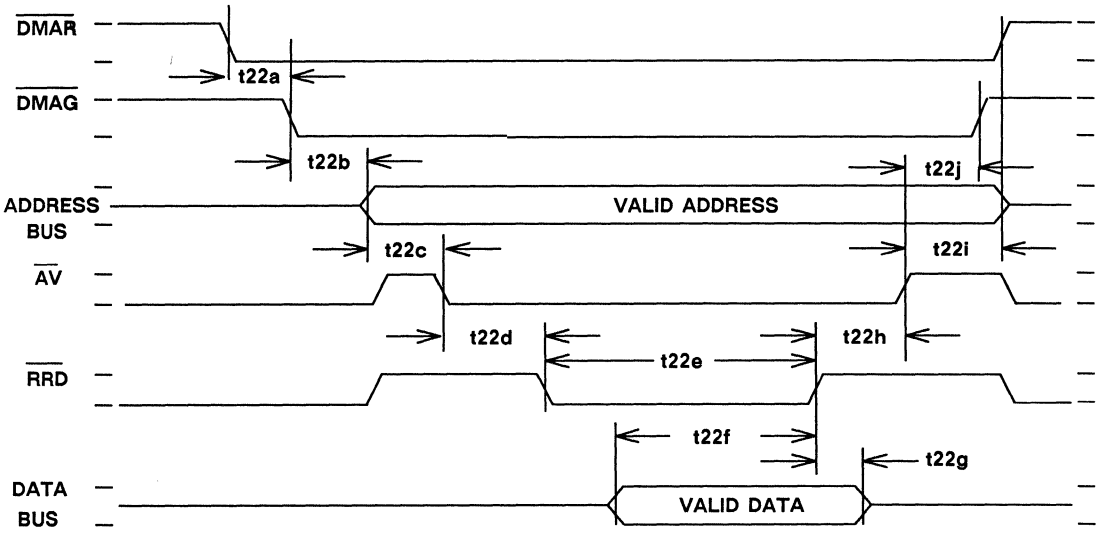
Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50 pF load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 22. Typical Timing Measurements



Note:
50 pF including scope probe and test socket

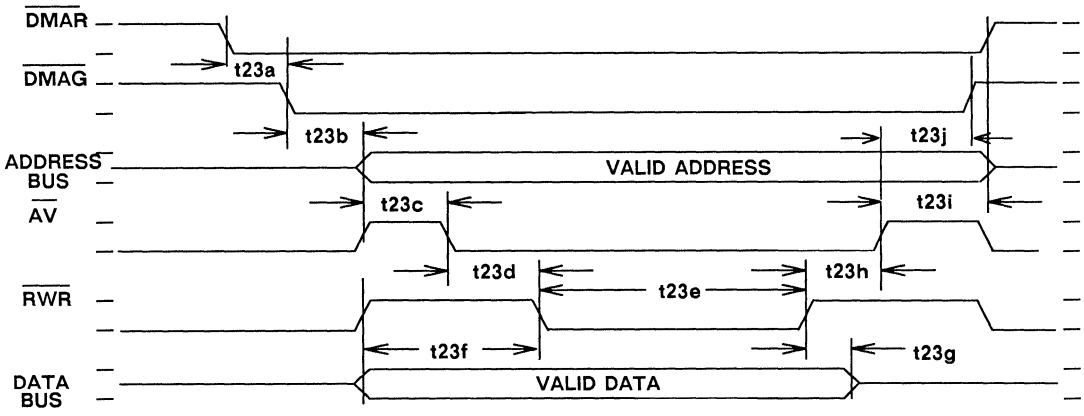
Figure 23. AC Test Loads and Input Waveforms



SYMBOL	PARAMETER	MIN	MAX	UNITS
t22a	$\overline{DMAR}$ ↓ to $\overline{DMAG}$ ↓	0	7.3	µs
t22b (1)	$\overline{DMAG}$ ↓ to Address Bus Valid	0	134	ns
t22c	Address Bus Valid to $\overline{AV}$ ↓	40	176	ns
t22d	$\overline{AV}$ ↓ to $\overline{RRD}$ ↓	80	90	ns
t22e	$\overline{RRD}$ Pulsewidth	95	140	ns
t22f	Data Setup Time to $\overline{RRD}$ ↑	50	—	ns
t22g	Data Hold Time from $\overline{RRD}$ ↑	0	—	ns
t22h	$\overline{RRD}$ ↑ to $\overline{AV}$ ↑	32	70	ns
t22i	$\overline{AV}$ ↑ to Address High-Impedance (Hold) and $\overline{DMAR}$ ↑	0	62	ns
t22j	$\overline{AV}$ ↑ to $\overline{DMAG}$ ↑	0	—	ns

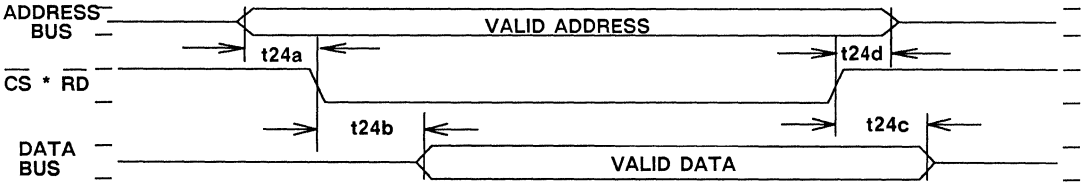
Note:
1. Guaranteed by test.

Figure 24. Detailed Timing - RTMP DMA Read Cycle



SYMBOL	PARAMETER	MIN	MAX	UNITS
t23a	$\overline{DMAR}$ ↓ to $\overline{DMAG}$ ↓	0	7.3	µs
t23b (1)	$\overline{DMAG}$ ↓ to Address Bus Valid	0	134	ns
t23c	Address Bus Valid to $\overline{AV}$ ↓	40	176	ns
t23d	$\overline{AV}$ ↓ to $\overline{RWR}$ ↓	80	90	ns
t23e	$\overline{RWR}$ Pulsewidth	95	140	ns
t23f	Data Bus Valid to $\overline{RWR}$ ↓	145	311	ns
t23g	$\overline{RWR}$ ↑ to Data Bus High-Impedance	20	90	ns
t23h	$\overline{RWR}$ ↑ to $\overline{AV}$ ↑	32	70	ns
t23i	$\overline{AV}$ ↑ to Address High-Impedance and $\overline{DMAR}$ ↑	0	62	ns
t23j	$\overline{AV}$ ↑ to $\overline{DMAG}$ ↑	0	—	ns

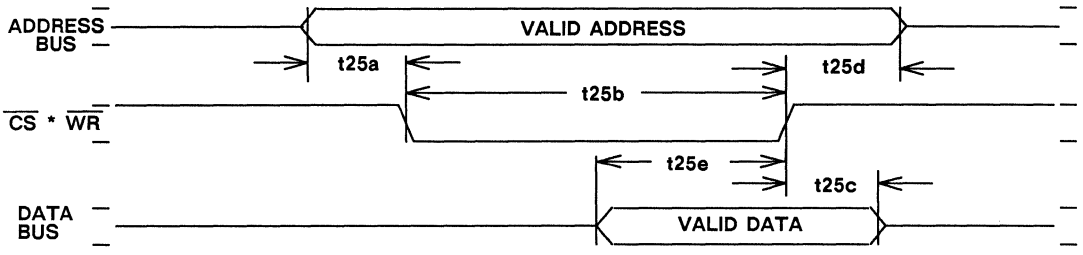
Figure 25. Detailed Timing - RTMP DMA Write Cycle



SYMBOL	PARAMETER	MIN	MAX	UNITS
t24a	Address Bus Valid to ($\overline{CS}$*$\overline{RD}$) ↓	20	—	ns
t24b (1)	($\overline{CS}$*$\overline{RD}$) ↓ to Data Bus Valid	0	93	ns
t24c	($\overline{CS}$*$\overline{RD}$) ↑ to Data Bus High-Impedance	10	100	ns
t24d	($\overline{CS}$*$\overline{RD}$) ↑ to Address Bus High-Impedance	20	—	ns

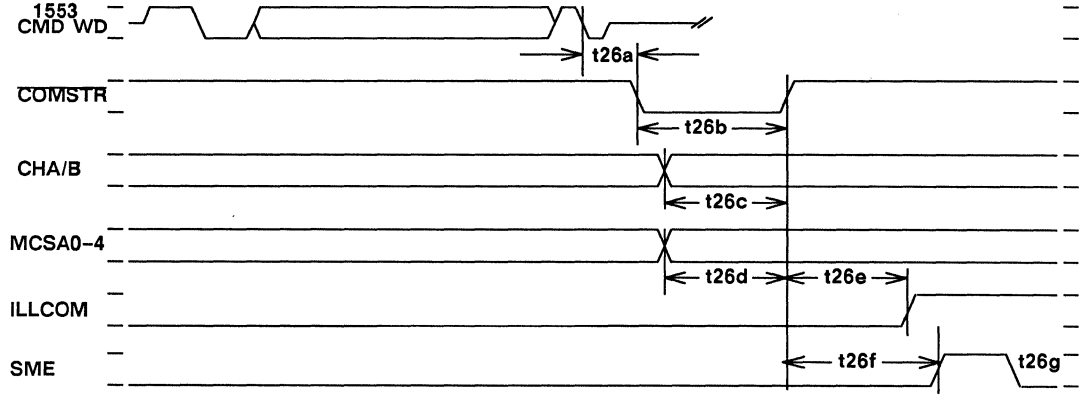
Note:
1. Guaranteed by test.

Figure 26. Detailed Timing - RTMP Register Reads



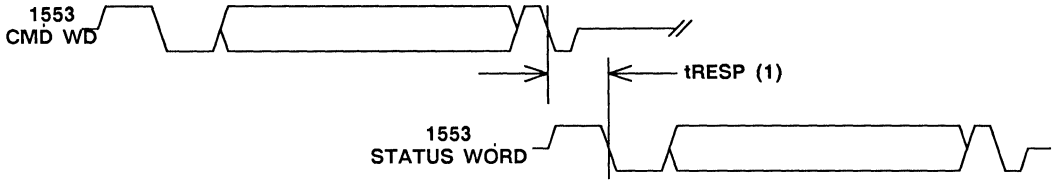
SYMBOL	PARAMETER	MIN	MAX	UNITS
t25a	Address Bus Valid to ($\overline{CS}$ * $\overline{WR}$) ↓	80	—	ns
t25b	$\overline{WR}$ Pulsewidth	50	—	ns
t25c	$\overline{WR}$↑ to Data Bus High-Impedance (Hold time)	70	—	ns
t25d	($\overline{CS}$ * $\overline{WR}$) ↑to Address Bus High-Impedance	50	—	ns
t25e	Data Valid to ($\overline{CS}$ * $\overline{WR}$)↑ (Set-up Time)	20	—	ns

Figure 27. Detailed Timing - RTMP Register Writes



SYMBOL	PARAMETER	MIN	MAX	UNITS
t26a	Mid-bit of Command Word Parity to $\overline{COMSTR}$ ↓	—	3.7	µs
t26b	$\overline{COMSTR}$ Pulsewidth	240	—	ns
t26c	CHA/$\overline{B}$ Valid to $\overline{COMSTR}$ ↑	230	—	ns
t26d	MCSA0-4 Valid to $\overline{COMSTR}$ ↑	240	—	ns
t26e	$\overline{COMSTR}$ ↑to ILLCOM ↑(Active)	—	100	ns
t26f	$\overline{COMSTR}$ ↑to SME ↑ (Active)	—	500	ns
t26g	SME Pulsewidth	.100	1.0	µs

Figure 28. 1553 Command strobe and Channel Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
tRESP (PRA/B=1)	1553A Mode Status Word Response Time	4.25	5.75	µs
tRESP (PRA/B=0)	1553B Mode Status Word Response Time	9.25	10.0	µs

Note:
1. This timing is for RTMP signals only and does not include delays from other sources.

Figure 29. 1553 Status Word Response Times

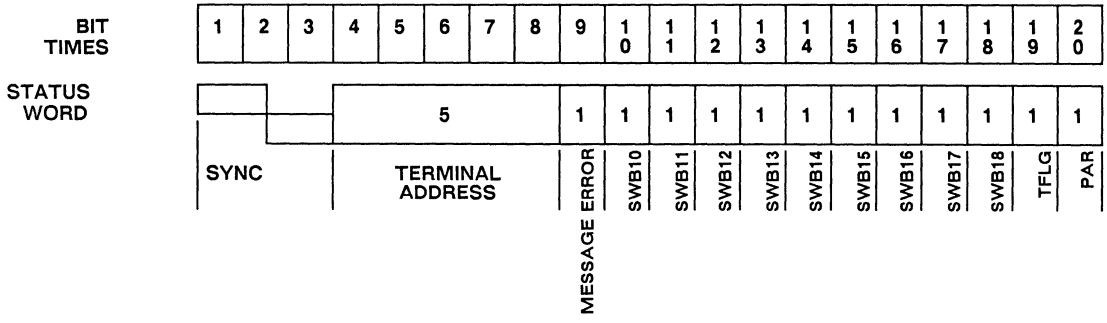


Figure 30. Status Word Bit-Time Definitions for 1553A Mode

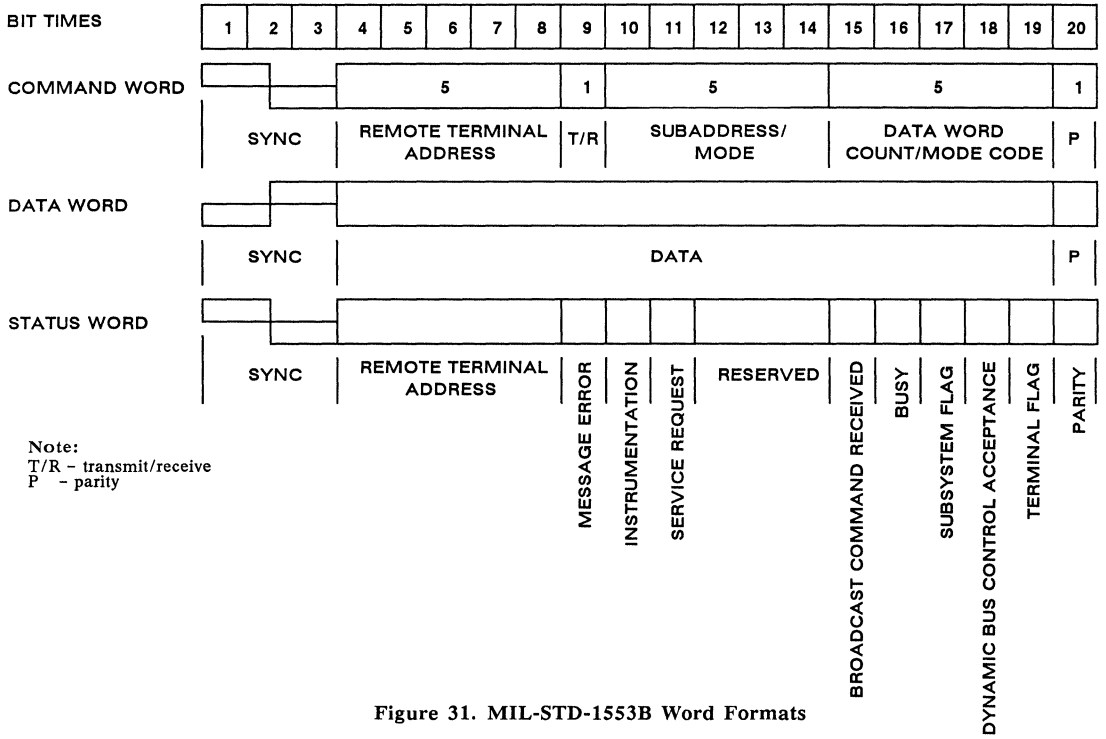


Figure 31. MIL-STD-1553B Word Formats

10.0 Package Outline Drawings

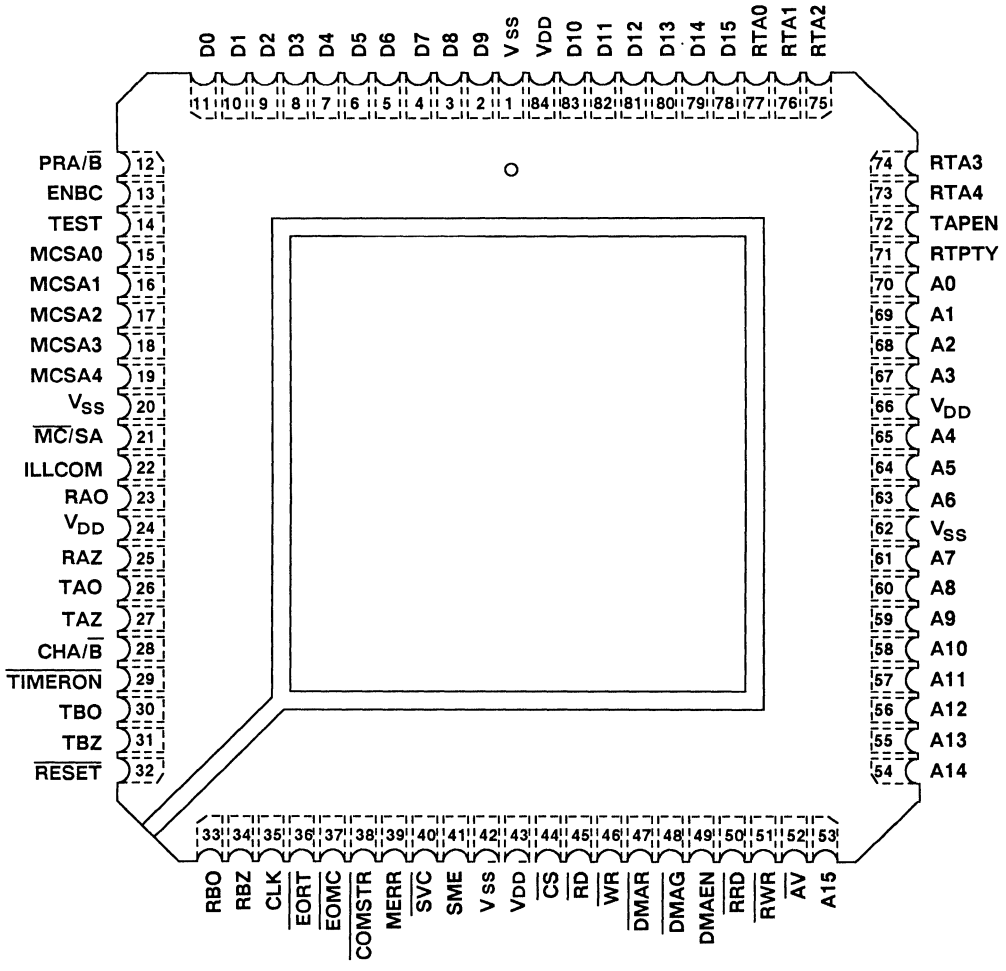


Figure 32a. Leadless Chip Carrier Functional Pin Identification (Top View)

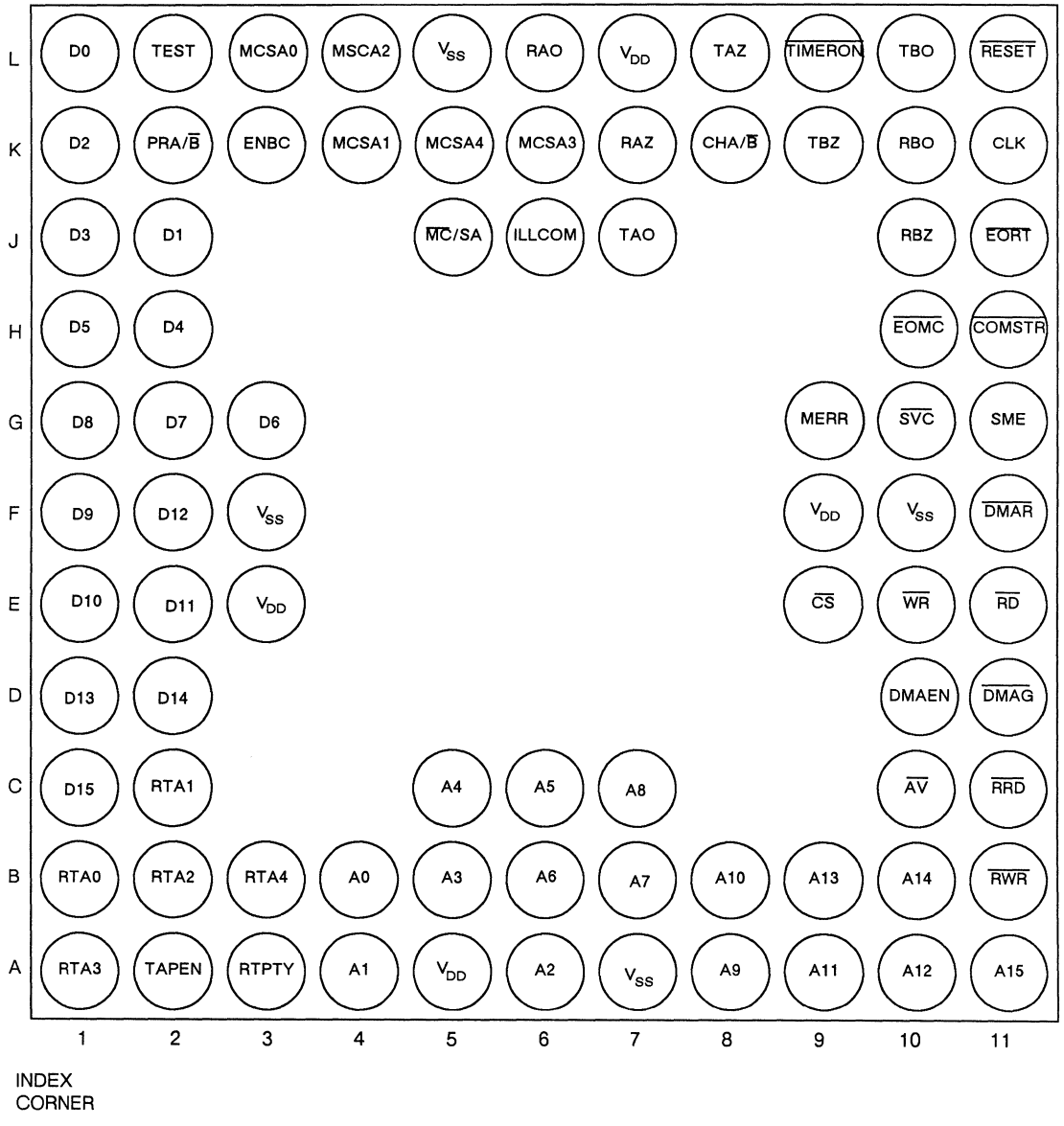


Figure 32b. Pingrid Array Functional Pin Identification (Bottom View)

UT63M1XX 1553A/B Bus Transceiver

Features

- ☐ Full conformance to MIL-STD-1553A and 1553B
- ☐ Completely monolithic bipolar technology
- ☐ Low power consumption
- ☐ Fit and functionally compatible to industry standard 631XX series
- ☐ Idle low and idle high encoding versions
- ☐ Dual-channel .050-center small outline package
- ☐ Flexible power supply voltages: V_{CC} = +5 V, V_{EE} = -12 V or -15 V, and V_{CCA} = +5 V to +12 V or +5 V to +15 V
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ☐ Standard Military Drawing available

Introduction

The monolithic UT63M1XX Transceivers are complete transmitter and receiver pairs conforming fully to MIL-STD-1553A and 1553B. Encoder and decoder interfaces are either idle low or idle high. UTMC's advanced bipolar technology allows the positive analog power to range from +5 V to +12 V or +5 V to +15 V, providing more flexibility in system power supply design.

The receiver section of the UT63M1XX series accepts biphase-modulated Manchester II bipolar data from a MIL-STD-1553 data bus and produces TTL-level signal data at its RXOUT and $\overline{\text{RXOUT}}$ outputs. An external RXEN input enables or disables the receiver outputs.

The transmitter section accepts biphase TTL-level signal data at its TXIN and $\overline{\text{TXIN}}$ and produces MIL-STD-1553 data signals. The transmitter's output voltage is typically 42 V_{PP}, L-L. Activating the TXIHB input or setting both data inputs to the same logic level disables the transmitter.

The UT63M1XX series offers complete transmitter and receiver pairs packaged in either single channel (24-pin) or dual-channel (36-pin) configurations designed for use in any MIL-STD-1553 application.

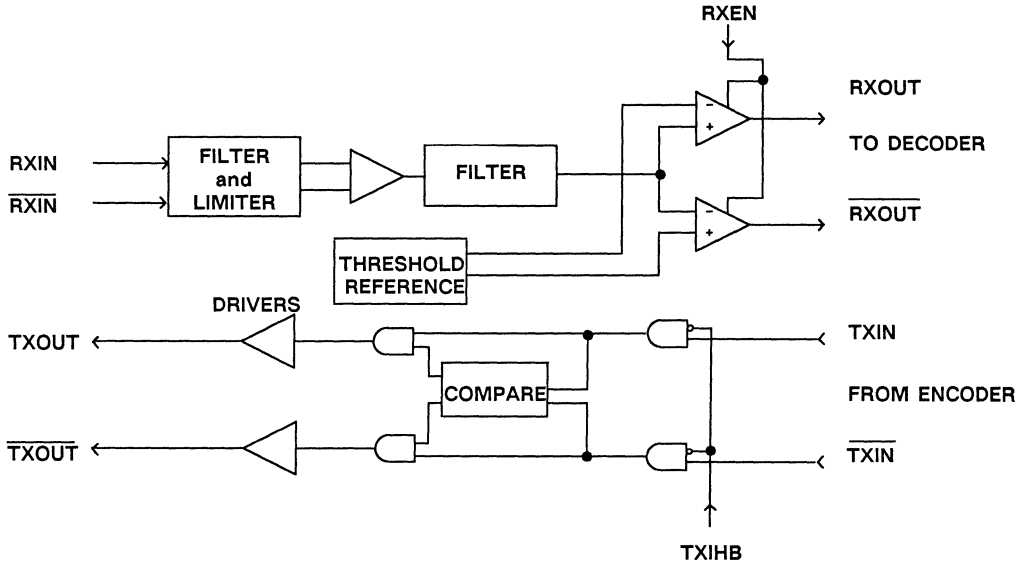


Figure 1. Functional Block Diagram

2.0 Pin Identification

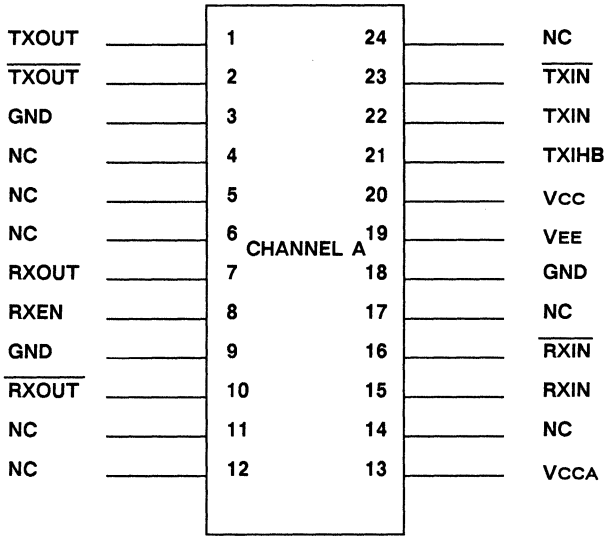


Figure 2a. Functional Pin Diagram--Single Channel

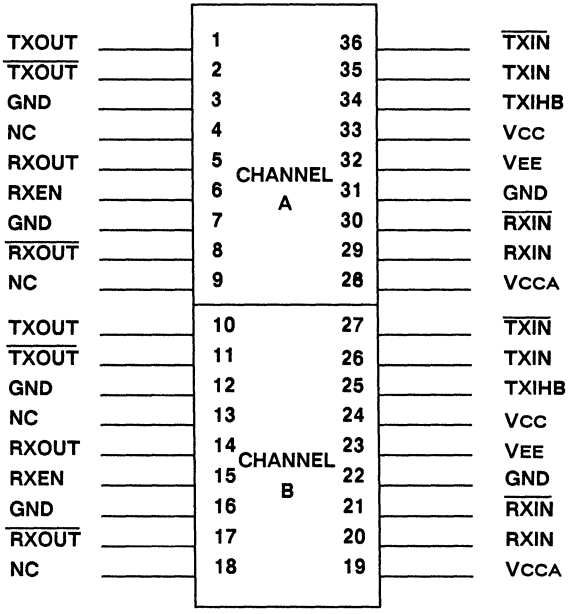


Figure 2b. Functional Pin Diagram--Dual Channel

Legend for TYPE field:

TI = TTL input
TO = TTL output
DO = Differential output
DI = Differential input
( ) = Channel designator

TRANSMITTER

NAME	PACKAGE SINGLE	PACKAGE DUAL	TYPE	DESCRIPTION
TXOUT (A)	1	1	DO	Transmitter outputs: TXOUT and $\overline{\text{TXOUT}}$ are differential data signals.
TXOUT (B)	N/A	10	DO	
$\overline{\text{TXOUT}}$ (A)	2	2	DO	$\overline{\text{TXOUT}}$ is the complement of TXOUT.
$\overline{\text{TXOUT}}$ (B)	N/A	11	DO	
TXIHB (A)	21	34	TI	Transmitter inhibit: This is an active high input signal.
TXIHB (B)	N/A	25	TI	
TXIN (A)	22	35	TI	Transmitter inputs: TXIN and $\overline{\text{TXIN}}$ are complementary TTL-level Manchester II encoder inputs.
TXIN (B)	N/A	26	TI	
$\overline{\text{TXIN}}$ (A)	23	36	TI	$\overline{\text{TXIN}}$ is the complement of TXIN input.
$\overline{\text{TXIN}}$ (B)	N/A	27	TI	

RECEIVER

NAME	PACKAGE		TYPE	DESCRIPTION
	SINGLE	DUAL		
RXOUT (A)	7	5	TO	Receiver outputs: RXOUT and $\overline{\text{RXOUT}}$ are complementary Manchester II decoder outputs.
RXOUT (B)	N/A	14	TO	
$\overline{\text{RXOUT}}$ (A)	10	8	TO	$\overline{\text{RXOUT}}$ is the complement of RXOUT output.
$\overline{\text{RXOUT}}$ (B)	N/A	17	TO	
RXEN (A)	8	6	TI	Receiver enable/disable: This is an active high input signal.
RXEN (B)	N/A	15	TI	
RXIN (A)	15	29	DI	Receiver inputs: RXIN and $\overline{\text{RXIN}}$ are biphase-modulated Manchester II bipolar inputs from MIL-STD-1553 data bus.
RXIN (B)	N/A	20	DI	
$\overline{\text{RXIN}}$ (A)	16	30	DI	$\overline{\text{RXIN}}$ is the complement of RXIN input.
$\overline{\text{RXIN}}$ (B)	N/A	21	DI	

POWER AND GROUND

NAME	PACKAGE		TYPE	DESCRIPTION
	SINGLE	DUAL		
VCC (A)	20	33	PWR	+5 VDC power (+/−10%)
VCC (B)	N/A	24	PWR	
VCCA (A)	13	28	PWR	+5 to +12 VDC power or +5 to +15 VDC power (+/−5%)
VCCA (B)	N/A	19	PWR	
VEE (A)	19	32	PWR	−12 or −15 VDC power (+/−5%) Recommended de-coupling capacitors -4.7 μF and .1 μF
VEE (B)	N/A	23	PWR	
GND (A)	3, 9, 18	3, 7, 31	GND	Ground reference
GND (B)	N/A	12, 16, 22	GND	

Transmitter

The transmitter section accepts Manchester II biphase TTL data and converts this data into differential phase-modulated current drive. Transmitter current drivers are coupled to a MIL-STD-1553 data bus via a transformer driven from the TXOUT and $\overline{\text{TXOUT}}$ terminals. Transmitter output terminals' non-transmitting state is enabled by asserting TXIHB (logic 1), or by placing both TXIN and $\overline{\text{TXIN}}$ at the same logic level. Table 1, Transmit Operating Mode, lists the functions for the output data in reference to the state of TXIHB. Figure 3 shows typical transmitter waveforms.

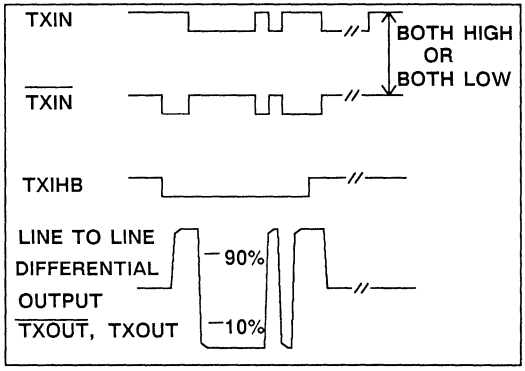
Receiver

The receiver section accepts biphase differential data from a MIL-STD-1553 data bus at its RXIN and $\overline{\text{RXIN}}$ inputs. The receiver converts input data to biphase Manchester II TTL format and is available for decoding at the RXOUT and $\overline{\text{RXOUT}}$ terminals. The outputs RXOUT and $\overline{\text{RXOUT}}$ represent positive and negative excursions (respectively) of the inputs RXIN and $\overline{\text{RXIN}}$. Figure 4 shows typical receiver output waveforms.

Depending on the transceiver version selected, the outputs RXOUT and $\overline{\text{RXOUT}}$ will idle in either the logic 0 or 1 state. The following flexibility in idle states allows compatibility to either the "Harris" or "Smith"-type encoder/decoder. Models UT63M105, UT63M107, UT63M125, and UT63M127 idle in the "0" state when disabled or receiving no signal. Models UT63M115, UT63M117, UT63M135, and UT63M137 idle in the "1" state when they are disabled or receiving no signal.

Power Supply Voltages

The UT63M1XX series meets device requirements over a wide range of power supply voltages. Table 2 shows the overall capabilities of all available devices. Each channel of the dual transceiver is electrically and physically separate from the other and fully independent, including all power and signal lines. Thus there will be no interaction between the channels.



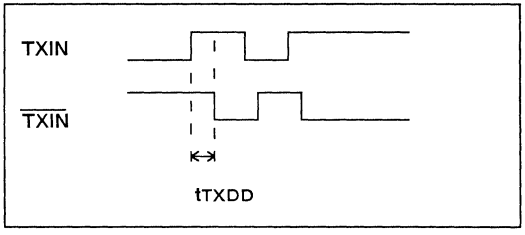


Figure 3. Typical Transmitter Waveforms

Table 1. Transmit Operating Mode

TXIN	$\overline{\text{TXIN}}$	TXIHB	TXOUT
x (1)	x	1	Off (2)
0	0	x	Off (3)
0	1	0	On
1	0	0	On
1	1	x	Off (3)

Notes:
1. x = Don't care.
2. Transmitter output terminals are in the non-transmitting mode during Off time.
3. Transmitter output terminals are in the non-transmitting mode during Off time, independent of TXIHB status.

Data Bus Interface

The designer can connect the UT63M1XX to the data bus via a short-stub (direct-coupling) connection or a long-stub (transformer-coupling) connection. Use a short-stub connection when the distance from the isolation transformer to the data bus does not exceed a one-foot maximum. Use a long-stub connection when the distance from the isolation transformer exceeds the one-foot maximum and is less than twenty-five feet. Figure 5 shows various examples of bus coupling configurations. The UT63M1XX series transceivers are designed to function with MIL-STD-1553A and 1553B compatible transformers.

Recommended Thermal Protection

All packages, single and dual, should mount to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally conductive material between the package and the heat removal rail. Use a material such as Mereco XLN-589 or equivalent to insure heat transfer between the package and heat removal rail.

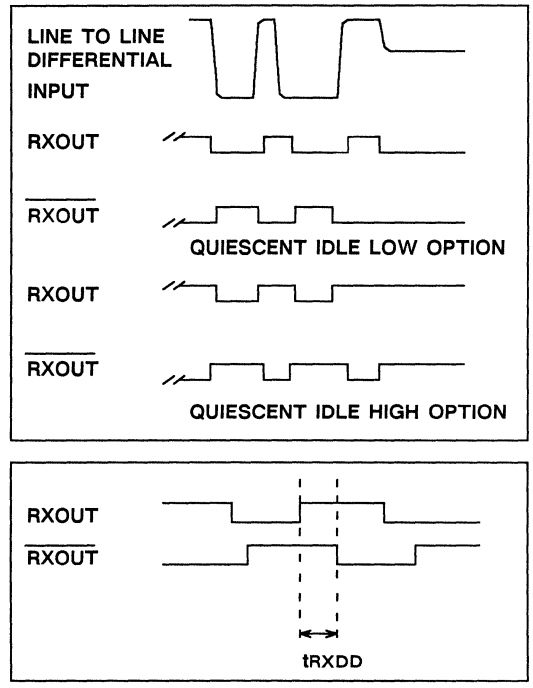
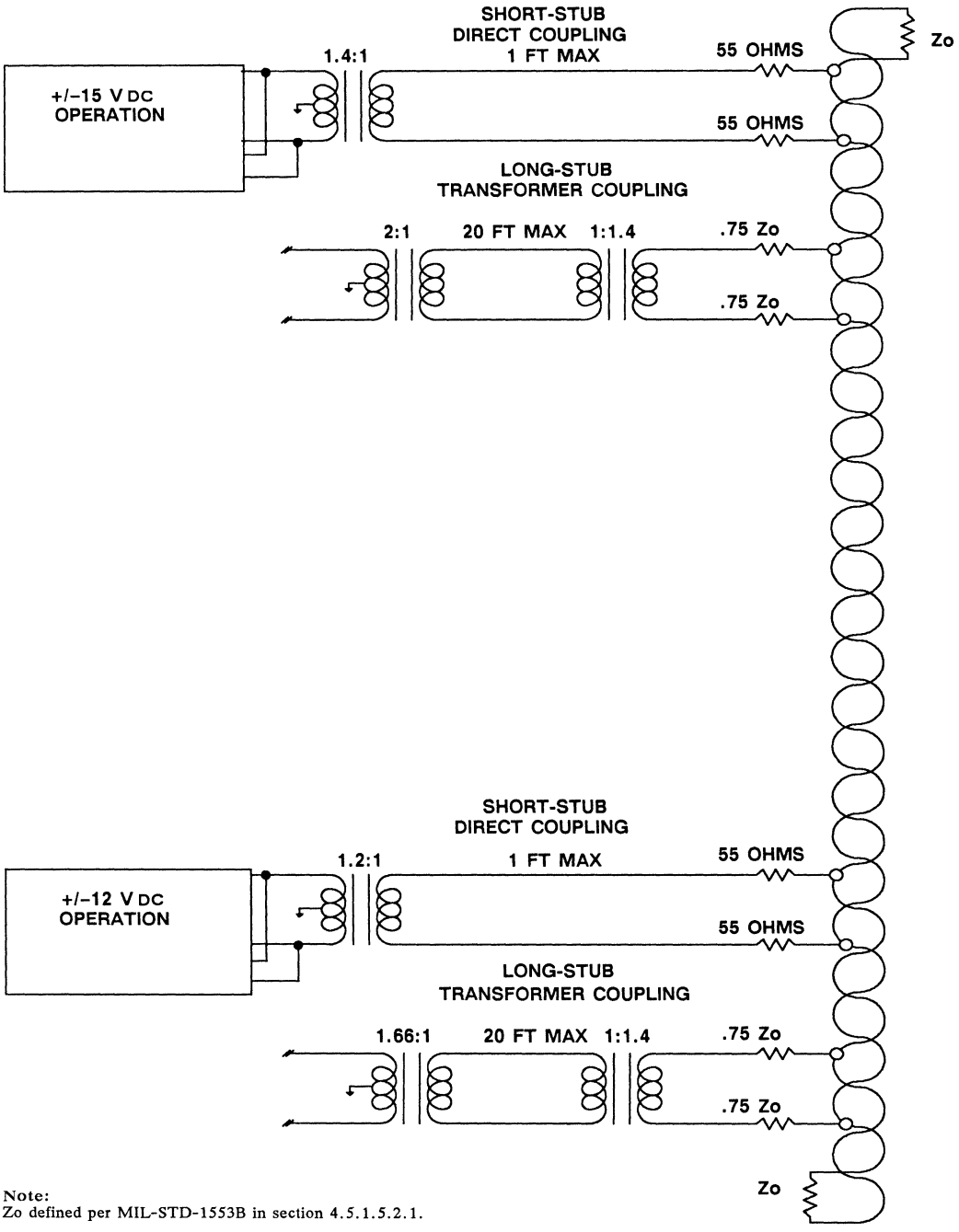


Figure 4. Typical Receiver Waveforms

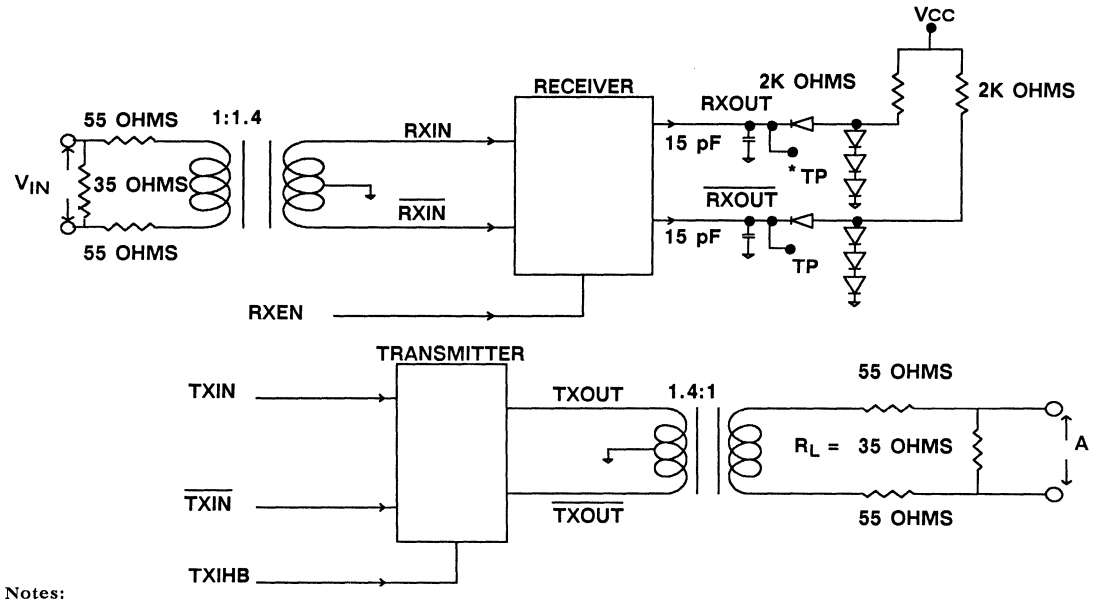
Table 2. Transceiver Model Capabilities

MODEL	VCC	VEE	VCCA	IDLE
UT63M105	+5 V	-15 V	+5 to +15 V	Low
UT63M107	+5 V	-12 V	+5 to +12 V	Low
UT63M115	+5 V	-15 V	+5 to +15 V	High
UT63M117	+5 V	-12 V	+5 to +12 V	High
UT63M125	+5 V	-15 V	+5 to +15 V	Low
UT63M127	+5 V	-12 V	+5 to +12 V	Low
UT63M135	+5 V	-15 V	+5 to +15 V	High
UT63M137	+5 V	-12 V	+5 to +12 V	High



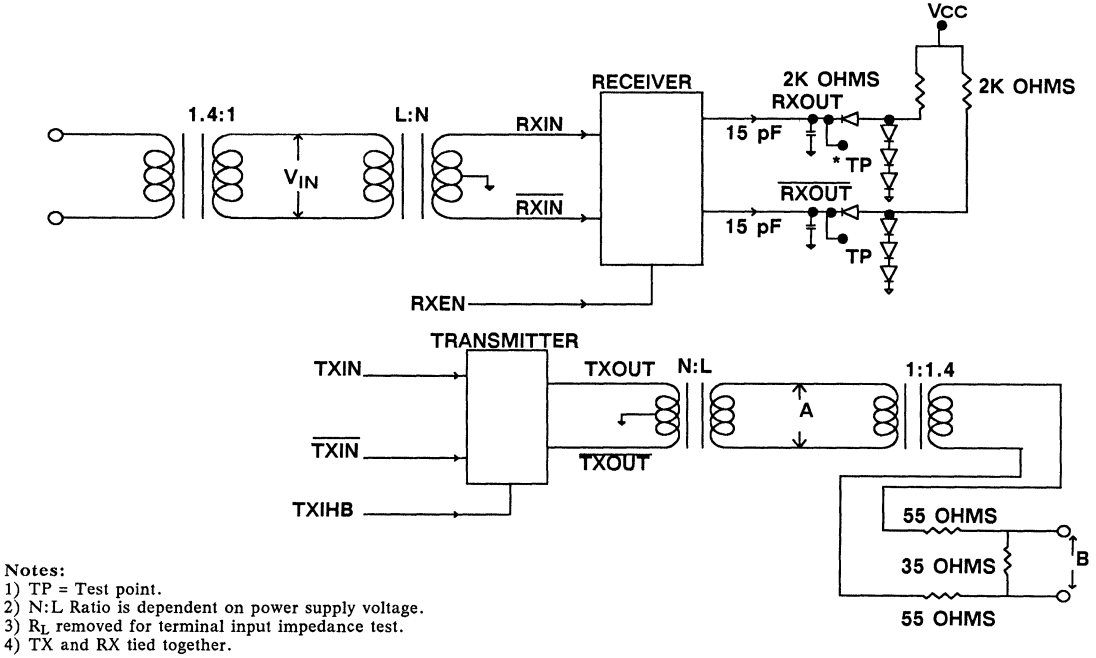
Note:
Zo defined per MIL-STD-1553B in section 4.5.1.5.2.1.

Figure 5. Bus Coupling Configuration



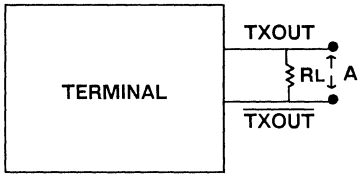
Notes:
1) TP = Test point.
2) R_L removed for terminal input impedance test.
3) TX and RX tied together.

Figure 6. Direct-Coupled Transceiver with Load



Notes:
1) TP = Test point.
2) N:L Ratio is dependent on power supply voltage.
3) R_L removed for terminal input impedance test.
4) TX and RX tied together.

Figure 7. Transformer-Coupled Transceiver with Load



Notes:
Transformer-Coupled Stub:
Terminal is defined as transceiver plus isolation transformer. Point A defined in figure 7.
Direct-Coupled Stub:
Terminal is defined as transceiver plus isolation transformer and fault resistors. Point A defined in figure 6.

Figure 8. Transceiver Test Circuit MIL-STD-1553B

ABSOLUTE MAXIMUM RATINGS (1)

(Reference to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{EE}	Supply voltage	-22	V
V_{CCA}	Supply voltage	+22	V
V_{IN}	Input voltage range (receiver)	42	$V_{PP,\ L\text{-}L}$
V_{IN}	Logic input voltage	-0.3 to +5.5	V
I_O	Output current (transmitter)	190	mA
P_D	Power dissipation (per channel)	4	W
Q_{JC}	Thermal impedance, junction-to-case	6 (2)	°C/W
T_J	Operating temperature junction	-55 to +150	°C
T_C	Operating temperature case	-55 to +125	°C
T_{STG}	Storage temperature	-65 to +150	°C

Notes:
1. Stress outside the listed absolute maximum rating may cause permanent damage to the devices. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Mounting per MIL-STD-883, Method 1012.

DC ELECTRICAL CHARACTERISTICS

VCC = +5 V (+/-10%)
VCCA = +5 V to +12 V (+/-5%) or +5 V to +15 V (+/-5%)
VEE = -12 V or -15 V (+/-5%)
-55°C < TC < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
VIL	Input low voltage		0.8	V	RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$
VIH	Input high voltage	2.0		V	RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$
IIL	Input low current	-1.6		mA	VIL = 0.4 V; RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$
IIH	Input high current		40	uA	VIH = 2.4 V; RXEN, TXIHB TXIN, $\overline{\text{TXIN}}$
VOL	Output low voltage		0.55	V	IOL = 4.0 mA; RXOUT, $\overline{\text{RXOUT}}$
VOH	Output high voltage	2.4		V	IOH = 0.4 mA; RXOUT, $\overline{\text{RXOUT}}$

DC ELECTRICAL CHARACTERISTICS (1)
V_{CC} = +5 V
V_{CCA} = (2)
V_{EE} = (2)
-55°C < Tc < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
ICC	V_{CC} supply current		60	mA	VEE = −12 V VCC = 5 V VCCA = +5 V to +12 V 0% duty cycle (non-transmitting)
			60	mA	50% duty cycle (f = 1 MHz)
			60	mA	100% duty cycle (f = 1 MHz)
					VEE = −15 V VCC = 5 V VCCA = +5 V to +15 V
			60	mA	0% duty cycle (non-transmitting)
			60	mA	50% duty cycle (f = 1 MHz)
			60	mA	100% duty cycle (f = 1 MHz)
ICCA	V_{CCA} supply current		10	mA	VEE = −12 V VCC = 5 V VCCA = +5 V to +12 V
			10	mA	0% duty cycle (non-transmitting)
			10	mA	50% duty cycle (f = 1 MHz)
					100% duty cycle (f = 1 MHz)
					VEE = −15 V VCC = 5 V VCCA = +5 V to +15 V
			10	mA	0% duty cycle (non-transmitting)
			10	mA	50% duty cycle (f = 1 MHz)
			10	mA	100% duty cycle (f = 1 MHz)
IEE	V_{EE} supply current		40	mA	VEE = −12 V VCC = 5 V VCCA = +5 V to +12 V
			140	mA	0% duty cycle (non-transmitting)
			230	mA	50% duty cycle (f = 1 MHz)
					100% duty cycle (f = 1 MHz)
					VEE = −15 V VCC = 5 V VCCA = +5 V to +15 V
			40	mA	0% duty cycle (non-transmitting)
			140	mA	50% duty cycle (f = 1 MHz)
			230	mA	100% duty cycle (f = 1 MHz)
PCD	Power dissipation		0.9	W	VEE = −12 V VCC = 5 V VCCA = +5 V to +12 V
			2.1	W	0% duty cycle (non-transmitting)
			3.3	W	50% duty cycle (f = 1 MHz)
					100% duty cycle (f = 1 MHz)
					VEE = −15 V VCC = 5 V VCCA = +5 V to +15 V
			1.0	W	0% duty cycle (non-transmitting)
			2.5	W	50% duty cycle (f = 1 MHz)
			3.8	W	100% duty cycle (f = 1 MHz)

Notes:
1. All tests guaranteed per test figure 6.
2. As specified in test conditions.

RECEIVER ELECTRICAL CHARACTERISTICS (1)
V_{CC} = +5 V (+/-10%)
V_{CCA} = +5 V to +12 V (+/-5%) or +5 V to +15 V (+/-5%)
V_{EE} = -12 V or -15 V (+/-5%)
-55°C < Tc < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
RIZ (2)	Differential (receiver) input impedance	15		K ohms	Input f = 1 MHz (no transformer in circuit)
CIN (2)	Input capacitance		10	pF	RXEN; input f = 1 MHz @ 0 V
VIC (2)	Common mode input voltage	-10	+10	V	Direct-coupled stub: input 1.2 VPP, 200 ns rise/fall time +/-25 ns, f = 1 MHz.
VTH (2)	Input threshold voltage (no response)		0.20	VPP, L-L	Transformer-coupled stub: input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0-->1 transition).
	Input threshold voltage (no response)		0.28	VPP, L-L	Direct-coupled stub: input at f = 1 MHz, rise/fall time 200 ns at (Receiver output 0-->1 transition).
(2)	Input threshold voltage (response)	.86	14.0	VPP, L-L	Transformer-coupled stub: input at f = 1 MHz, rise/fall time 200 ns output at (Receiver output 0-->1 transition).
	Input threshold voltage (response)	1.20	20.0 (2)	VPP, L-L	Direct-coupled stub: input at f = 1 MHz, rise/fall time 200 ns output at (Receiver output 0-->1 transition).
CMRR (2)	Common mode rejection ratio	Pass/Fail (3)		N/A	

Notes:
1. All tests guaranteed per test figure 6.
2. Guaranteed by device characterization.
3. Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation Test Plan, Section 5.1.2.2, Common Mode Rejection.

TRANSMITTER ELECTRICAL CHARACTERISTICS (1)
V_{CC} = +5 V (+/-10%)
V_{CCA} = +5 V to +12 V (+/-5%) or +5 V to +15 V (+/-5%)
V_{EE} = -12 V or -15 V (+/-5%)
-55°C < Tc < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
V_O	Output voltage swing per MIL-STD-1553B (2) (see figure 9)	18	27	V_{PP}, L-L	Transformer-coupled stub, Figure 8, Point A: input f = 1 MHz, R_L = 70 ohms.
	per MIL-STD-1553B (see figure 9)	6	9	V_{PP}, L-L	Direct-coupled stub, Figure 8, Point A: input f = 1 MHz, R_L = 35 ohms.
	per MIL-STD-1553A (2) (see figure 9)	6	20	V_{PP}, L-L	Figure 7, Point A: input f = 1 MHz, R_L = 35 ohms.
V_{NS} (2)	Output noise voltage differential (see figure 9)		14	mV-RMS L-L	Transformer-coupled stub, Figure 8, Point A: input f = DC to 10 MHz, R_L = 70 ohms.
			5	mV-RMS L-L	Direct-coupled stub, Figure 8, Point A: input f = DC to 10 MHz, R_L = 35 ohms.
V_{OS} (2)	Output symmetry (see figure 9)	-250	+250	mV_{PP}, L-L	Transformer-coupled stub, Figure 8, Point A: R_L = 70 ohms, measurement taken 2.5 µs after end of transmission.
		-90	+90	mV_{PP}, L-L	Direct-coupled stub, Figure 8, Point A: R_L = 35 ohms, measurement taken 2.5 µs after end of transmission.
V_{DIS} (2)	Output voltage distortion (overshoot or ring) (see figure 9)	-900	+900	mV_{peak} L-L	Transformer-coupled stub, Figure 8, Point A: R_L = 70 ohms.
		-300	+300	mV_{peak} L-L	Direct-coupled stub, Figure 8, Point A: R_L = 35 ohms.
C_{IN} (2)	Input capacitance		10	pF	TXIHB, TXIN, $\overline{TXIN}$; input f = 1 MHz @ 0 V
T_{IZ} (2)	Terminal input impedance	1		K ohm	Transformer-coupled stub, Figure 7, Point A: input f = 75 KHz to 1 MHz (power on or power off: non-transmitting, R_L removed from circuit).
		2		K ohm	Direct-coupled stub, Figure 6, Point A: input f = 75 KHz to 1 MHz (power on or power off: non-transmitting, R_L removed from circuit).

Notes:
1. All tests guaranteed per test figure 6.
2. Guaranteed by device characterization.

AC ELECTRICAL CHARACTERISTICS (1)
V_{CC} = +5 V (+/-10%)
V_{CCA} = +5 V to +12 V (+/-5%) or +5 V to +15 V (+/-5%)
V_{EE} = -12 V or -15 V (+/-5%)
-55°C < Tc < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
tR, tF	Transmitter output rise/fall time (see figure 10)	100	300	ns	Input f = 1 MHz 50% duty cycle: direct-coupled R_L = 35 ohms output at 10% through 90% points TXOUT, $\overline{TXOUT}$. Figure 3.
tRXDD	RXOUT delay	-200	+200	ns	RXOUT to $\overline{RXOUT}$; Figure 4.
tTXDD (3)	TXIN skew	-25	+25	ns	TXIN to $\overline{TXIN}$; Figure 3.
tRZCD	Zero crossing distortion (see figure 11)	-150	150	ns	Direct-coupled stub; input f = 1 MHz, 3 V_{PP} (skew INPUT +/-150 ns), rise/fall time 200 ns.
tTZCS	Zero crossing stability (see figure 10)	-25	25	ns	Input TXIN and $\overline{TXIN}$ should create transmitter output zero crossings at 500 ns, 1000 ns, 1500 ns, and 2000 ns. These zero crossings should not deviate more than +/-25 ns.
tDXOFF (3) (4)	Transmitter off; delay from inhibit active		400	ns	TXIN and $\overline{TXIN}$ toggling @ 1 MHz; TXIHB transitions from logic zero to one.
tDXON (3) (5)	Transmitter on; delay from inhibit inactive		250	ns	TXIN and $\overline{TXIN}$ toggling @ 1 MHz; TXIHB transitions from logic one to zero.

Notes:
1. All tests guaranteed per test figure 6.
2. Guaranteed by device characterization.
3. Supplied as a design limit but not guaranteed or tested.
4. Delay time from transmit inhibit (1.5 V) to transmit off (280 mV).
5. Delay time from not transmit inhibit (1.5 V) to transmit on (1.2 V).

Table 3. Transformer Requirements Versus Power Supplies

COUPLING TECHNIQUE	+/-12 VDC	+/-15 VDC
DIRECT-COUPLED: Isolation Transformer Ratio	1.2:1	1.4:1
TRANSFORMER-COUPLED: Isolation Transformer Ratio	1.66:1	2:1
Coupling Transformer Ratio	1:1.4	1:1.4

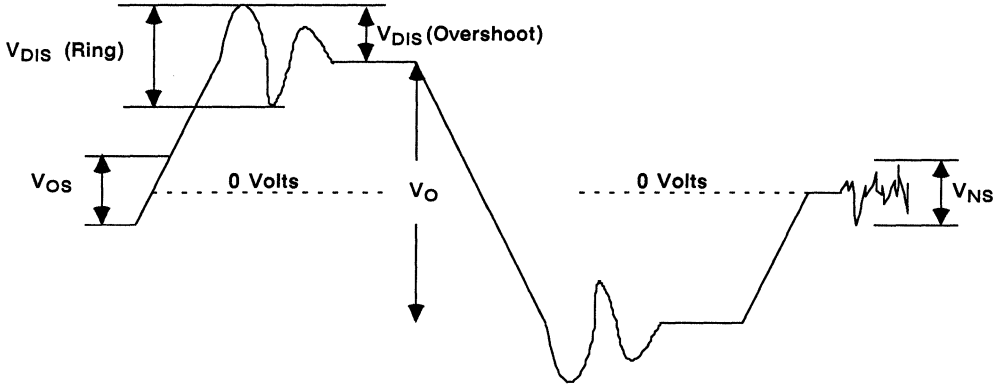


Figure 9. Transmitter Output Characteristics (VDIS, VOS, VNS, VO)

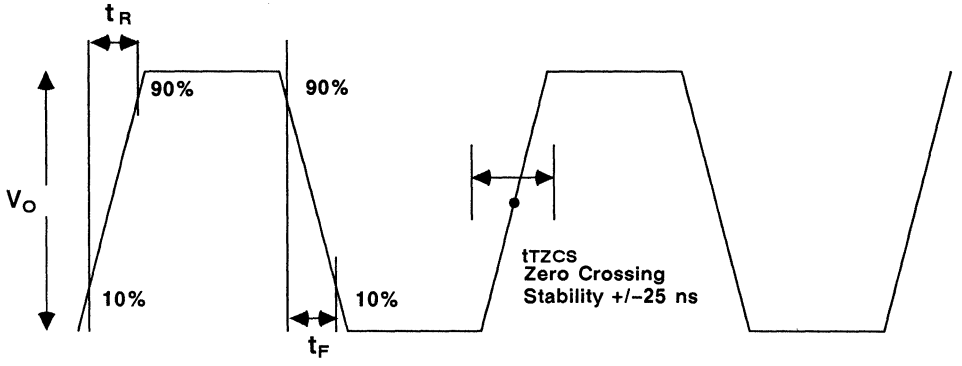


Figure 10. Transmitter Output Zero Crossing Stability (tTZCS, tR, tF)

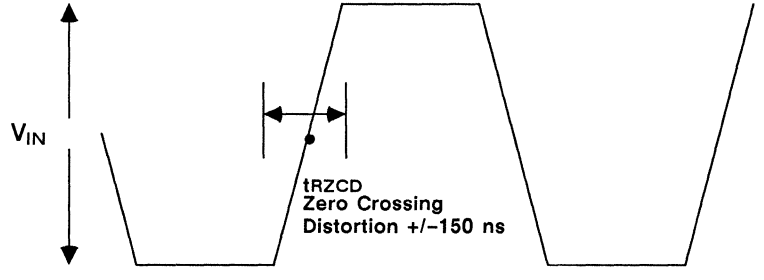


Figure 11. Receiver Input Zero Crossing Distortion (tRZCD)

Table of Contents

RTI Internal Self-Test Routine

INTRODUCTION

The self-test capability of the UT1553B RTI is based upon the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the output encoder is fed back to the input decoder, the decoder will recognize the incoming status word as a command word (wrap-around test). The RTI will interpret the command word and react accordingly (e.g., transmit a status word); status word transmission results in continuation of the wrap-around test. The host microprocessor monitors the System Register, status outputs, and last command data to determine if the RTI is functioning properly. Pass/fail criteria is based on a comparison, performed by the host, of expected data versus data extracted from RTI. The RTI does not contain any internal hardware designed to test functionality.

The host controls the self-test by changing bit patterns in the status word being transmitted. The host alters the status word by periodically writing to the RTI Control Register. Writing to Control Register bits that correspond to MIL-STD-1553B status word bits allows the host to control the incoming command word the RTI receives.

The host controls the Service Request, Subsystem Flag, System Busy, and Terminal Flag by writing to the Control Register. For more information, refer to the current UT1553B RTI Data Sheet.

SELF-TEST CONFIGURATION

The first step is initialization of the RTI. Always initialize the RTI into a known state by using the master reset or software reset before performing self-test. To begin self-test the host writes to the Control Register, setting the Self-Test Enable bit (bit 6) to a logic one. Disable output encoder Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The status word is sent to decoder A or B depending on the channel the host selected for self-test (Control Register bit 5). The status word wraps back into the RTI via the input decoder channel. Figure 1 shows an example of wrap-around test scheme.

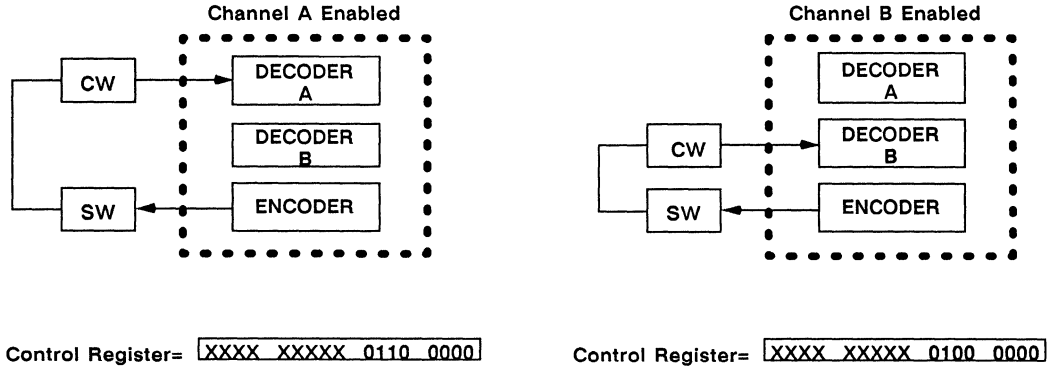


Figure 1. Wrap-around Test

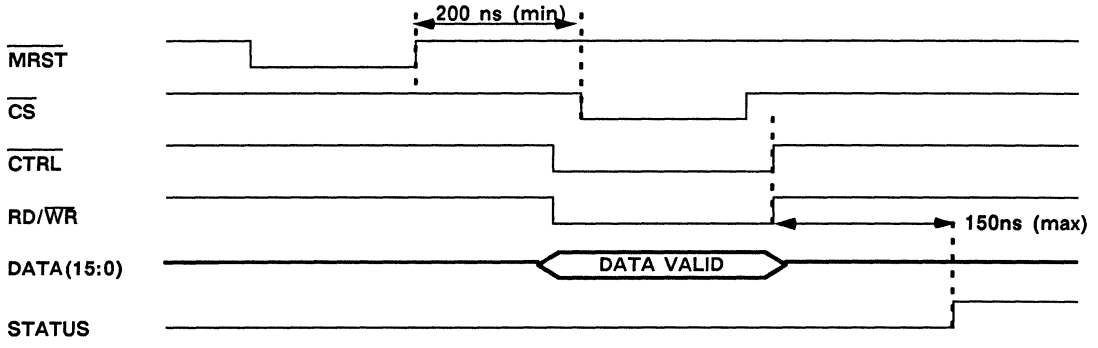
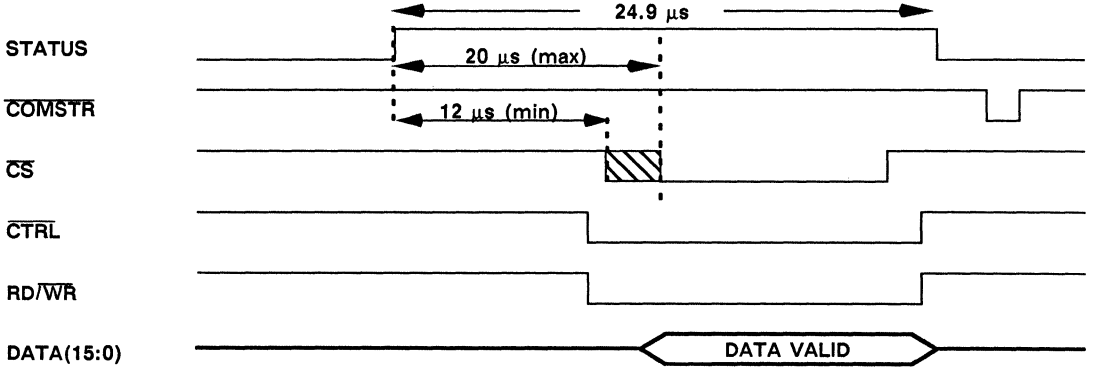


Figure 2a. Reset Control Register Write to STATUS Active



Notes:
1. The host can write to the Control Register during a window defined by the assertion of STATUS. The window opens 12 µs after the assertion of STATUS and closes 20 µs later.
2. ADDR IN(0)=1.

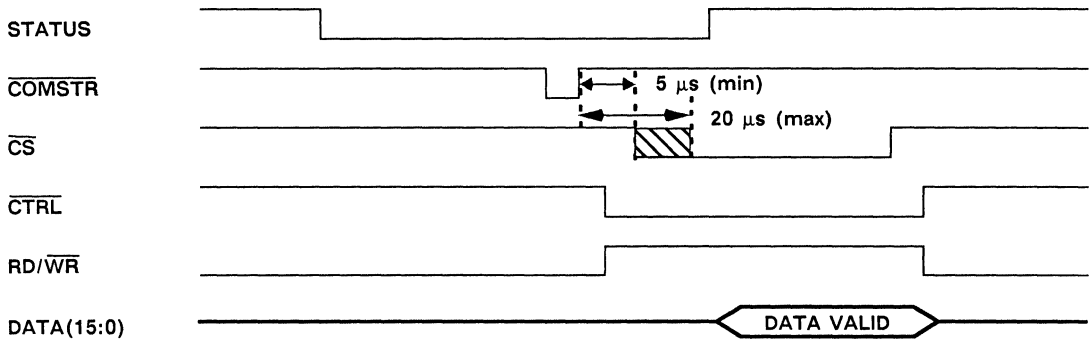
Figure 2b. Control Register Write Window

Control Register Write

Writing to the Control Register bits 2, 3, 4, and 7 changes the status word. Write to the Control Register 12 µs (minimum) after the STATUS pin is asserted; this does not change the contents of the status word being transmitted. Upon receiving the next command word, the transmitted status word reflects the updated Control Register contents. Figure 2 shows an example of the timing for a Control Register write with respect to the assertion of signal STATUS; refer to the RTI data sheet for Control Register write timing specifications.

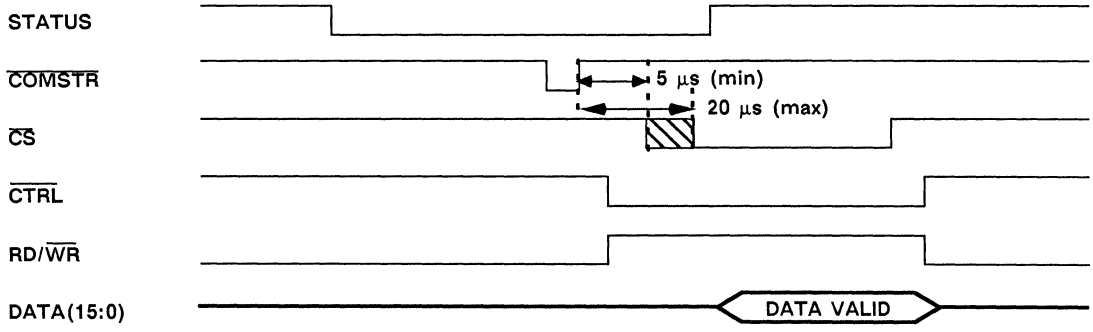
Monitoring Self-Test

Read the Status Register and Last Command Register to monitor how the self-test is performing. The output status pins also supply information regarding the state of the self-test routine. The host reads the Status Register by performing a Status Register read after every command strobe ($\overline{\text{COMSTR}}$) negation. The Status Register is read 5 µs (minimum) after the rising edge of $\overline{\text{COMSTR}}$. The last command word the RTI receives is stored in the Last Command Register. Figures 3 and 4 show examples of the Status Register read and the last Command Register read.



Notes:
1. The host can read the Status Register during a window defined by the negation of $\overline{\text{COMSTR}}$. The window opens 5 µs after the negation of $\overline{\text{COMSTR}}$ and closes 15 µs later.
2. ADDR IN(0)=0.

Figure 3. Status Register Read



Notes:
1. The host can read the last command register during a window defined by the negation of $\overline{\text{COMSTR}}$. The window opens 5 µs after the negation of $\overline{\text{COMSTR}}$ and closes 15 µs later.
2. ADDR IN(0)=1.

Figure 4. Last Command Register Read

Self-Test Start-Up

After the host enables self-test the RTI behaves as if it had just received and validated a command word (CW). The contents of the Command Word Latch (CWL) are decoded and the RTI will respond accordingly. After Master Reset the RTI Command Word Latch contains binary 0 00000 00000. The Command Word Latch contains bits 9 through 19 of the command word. Sync Field Data, Remote Terminal Address, and Parity bit are removed before storage in the Command Word Latch.

The RTI decodes the Command Word Latch contents as illegal and asserts the two message error signals, the Message Error bit in the Status Register and the Message Error pin. The RTI then asserts the STATUS signal indicating transmission of the status word (SW) is about to begin. 12 µs after the assertion of STATUS, a Control Register write is performed to modify the status word. Set the Terminal Flag bit to a logic one in the Control Register. The status word transmitted following the assertion of signal STATUS does not have the

Terminal Flag bit set; however, transmission of the status word (BUSY = 0, TF = 0, ME = 1) results in the Command Word Latch being loaded. The RTI decodes the contents of the Command Word Latch as illegal. STATUS signal is asserted and a status word with TF = 1 and ME = 1 is transmitted. 12 μs after the STATUS signal is asserted the Control Register is again updated. Figure 5 shows an example flow chart of a self-test sequence. Status Register and Last Command Register reads are omitted.

Setting the Terminal Flag (TF), Subsystem Busy (SUBS), and System Busy (BUSY) bits exercises various mode codes. The example flow chart illustrates the setting of one bit at a time; by setting more than one bit the RTI receives the following mode codes.

BUSY	SUBS	TF	
0	0	0	Dynamic Bus Control
0	0	1	Synchronize
0	1	0	Transmitter Shutdown
0	1	1	Override Transmitter Shutdown
1	0	0	Reset Remote Terminal

The RTI decodes these command words as valid (ME = 0) or illegal (ME = 1) depending on the logic state of the T/$\overline{R}$ bit in the command word.

Setting the Service Request (SRQ) bits in the Control Register results in the RTI interpreting the command word as a subaddress receive or transmit. Reception of a transmit command requires the RTI to first transmit a status word followed by the defined number of data words. The BUSY, SUBS, and TF bits control the number of data words. However, once the RTI transmits a status word, a command word is received and is treated as a superseding command, cancelling the transmit command. The RTI decodes the superseding command and responds accordingly.

The receive command is transmitted last in a self-test routine since it results in a bus time-out. After decoding the receive command the RTI waits for forthcoming data words. Following the time-out period, the RTI asserts the Message Error signal and does not transmit a status word. After the receive command is decoded a Control Register write is performed to disable self-test, enable Channel A, and enable Channel B. The Control Register write is performed following the rising edge of $\overline{COMSTR}$. Configure the RTI to begin normal operation following the assertion of the Message Error signal.

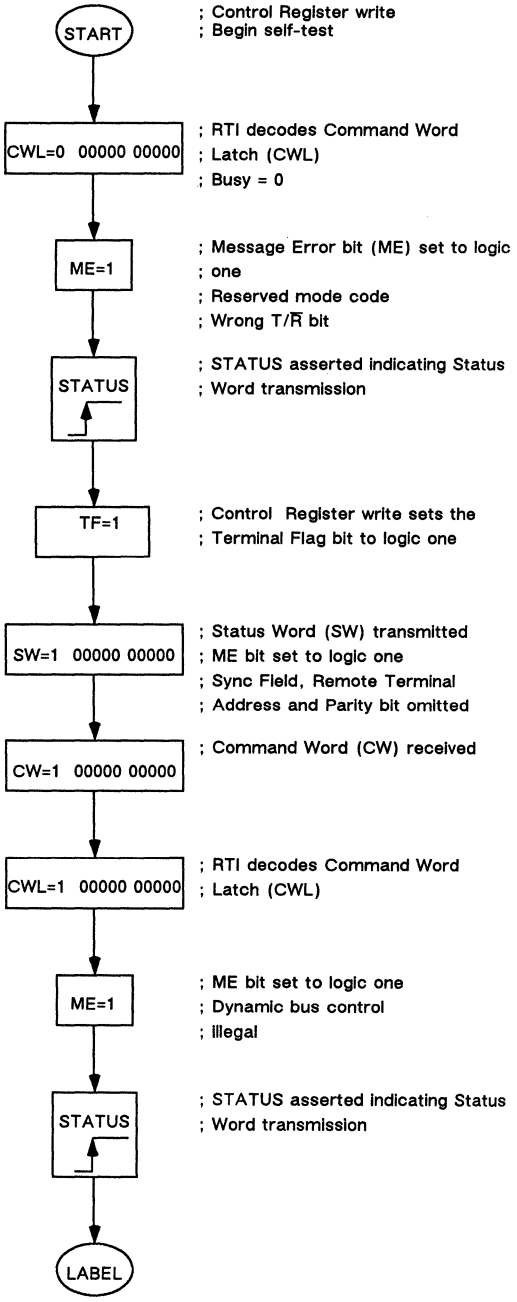


Figure 5a. Self-Test Flow Chart

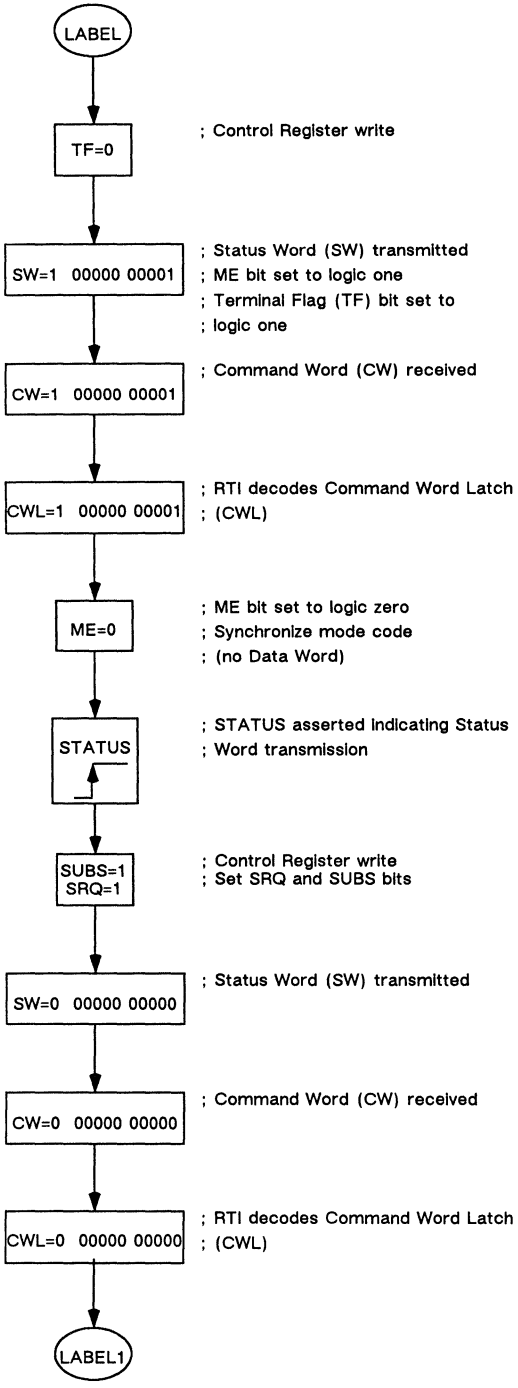


Figure 5b. Self-Test Flow Chart

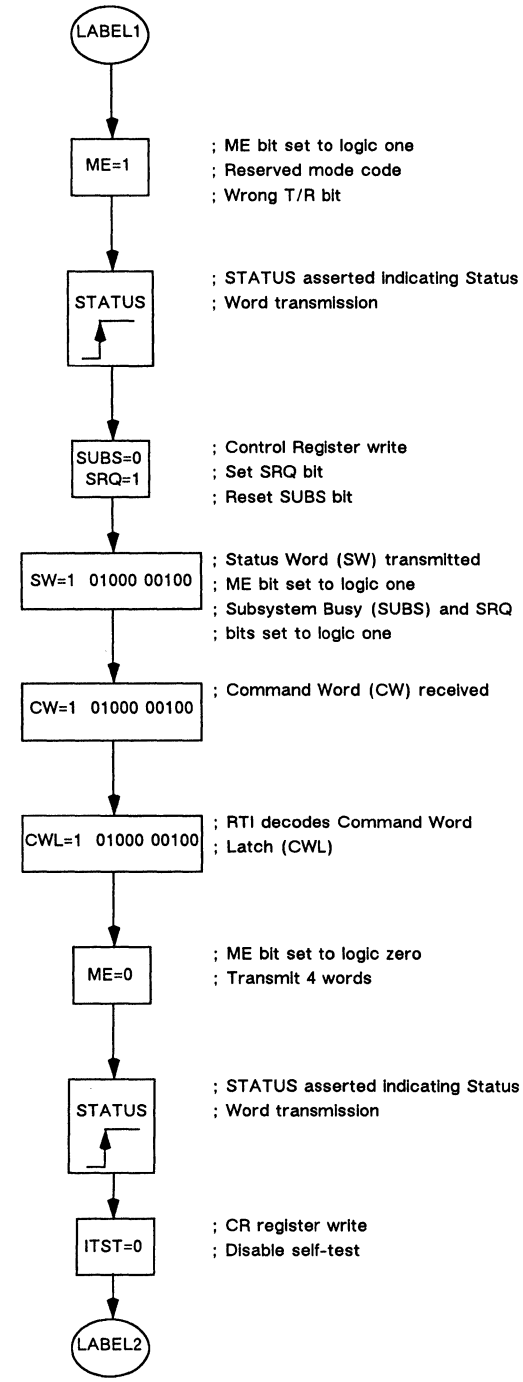


Figure 5c. Self-Test Flow Chart

4

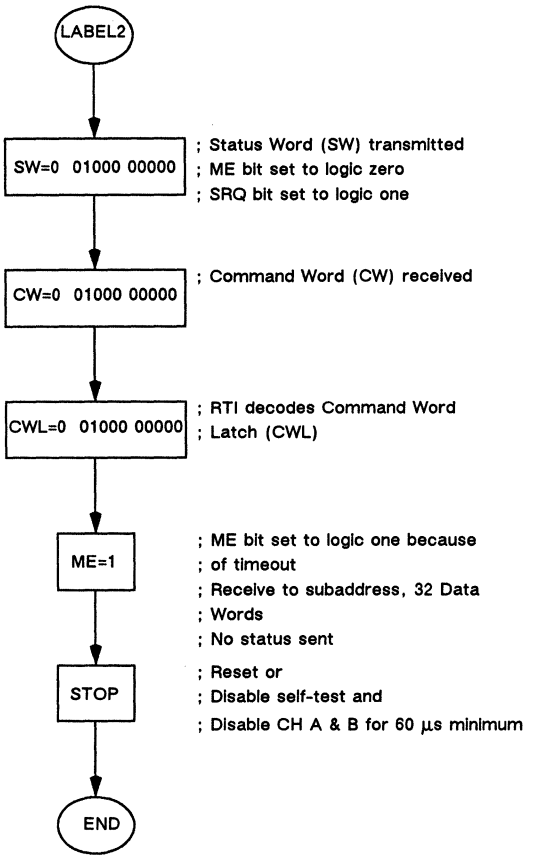


Figure 5d. Self-Test Flow Chart

CONCLUSION

The wrap-around self-test allows the host to perform a rudimentary functionality test of the RTI. The logic blocks that the test controls and observes include input decoders, output encoders, Control Register (bits 2, 3, 4, and 7), Status Register (bits 9, 10, 11, 13, and 14), and Last Command Register. The Last Command Register contents are corrupted as a result of the self-test routine. The RTI and the host accomplish the self-test routine in about 350 µs.

UT1750AR: Bus Arbitration with the UT1553B RTMP

The following design example explores the development of a bus arbitration circuit which prioritizes and controls bus accesses for a system containing DMA devices (i.e., RTMP and UT1750AR). The bus arbitration circuit consists of a sequential state machine interfaced to the DMA signals of the UT1750AR and RTMP. The state machine accepts bus request information from a DMA device and asserts a signal granting access to the bus. If the DMA devices generate coincident requests, the state machine will grant the bus to the device with the highest priority. Figure 1 shows a general system diagram.

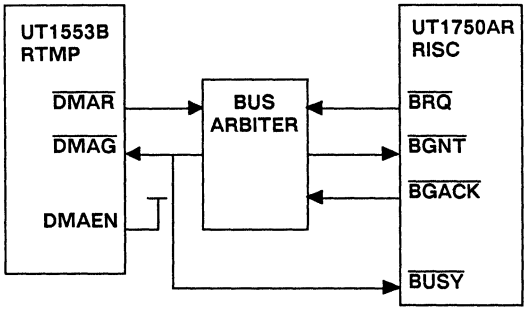
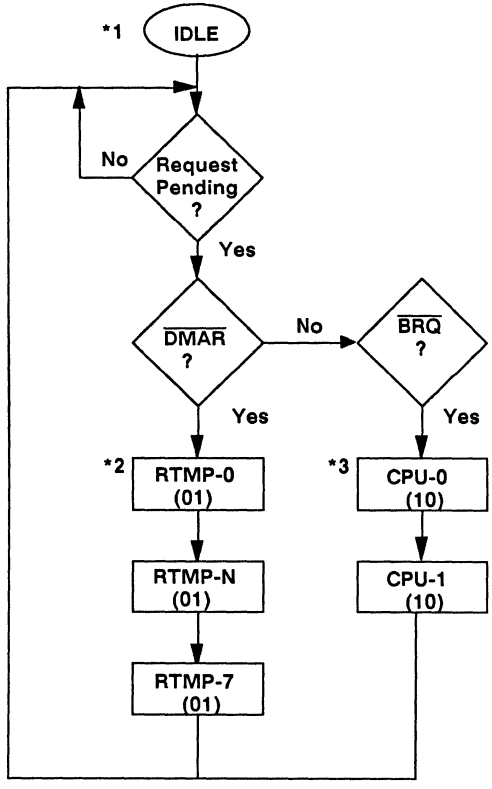


Figure 1. General System Diagram

UT1750AR bus arbitration is controlled by four signals: $\overline{BRQ}$, $\overline{BGNT}$, $\overline{BGACK}$, and $\overline{BUSY}$. Use these signals to handshake with the bus arbiter. The UT1750AR asserts bus request ($\overline{BRQ}$) to gain access to the bus. Bus grant ($\overline{BGNT}$) is returned to the UT1750AR by the bus arbiter; assertion of the $\overline{BGNT}$ input grants the UT1750AR access to the bus. Assert bus grant ($\overline{BGNT}$) until the UT1750AR acknowledges control of the bus. The UT1750AR acknowledges control of the bus by asserting bus grant acknowledge ($\overline{BGACK}$). The busy input pin ($\overline{BUSY}$) informs the UT1750AR that the bus is under control of another bus master.

UT1553B RTMP bus arbitration is controlled by these three signals: $\overline{DMAR}$, $\overline{DMAG}$, and DMAEN. Similar to the UT1750AR control signal $\overline{BRQ}$, the RTMP asserts $\overline{DMAR}$ to request access to the bus. The bus arbiter asserts the $\overline{DMAG}$ signal to inform the RTMP that the bus is available. The bus arbiter asserts the $\overline{DMAG}$ signal until the RTMP completes the bus access. RTMP memory accesses are enabled by the assertion of the DMA enable (DMAEN).

Figure 2 shows a flow chart for the decision-making circuitry contained in the arbiter. Similar to a state diagram, the flow chart identifies the states required in the arbitration circuit. Each state has a corresponding output. The state transition table shown in table 1 defines inputs required to reach each state. For systems that require multiple DMA devices, the flow chart is expanded to incorporate the additional devices.



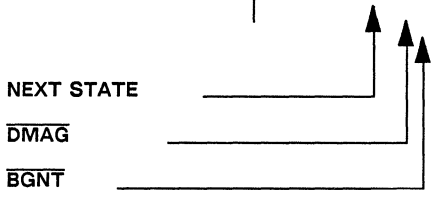
Notes:
1. Idle state: no pending interrupts - $\overline{DMAG} = 1$ and $\overline{BGNT} = 1$
2. RTMP0 to RTMP7 = 8 clocks for RTMP DMA access; $\overline{DMAG} = 0$ and $\overline{BGNT} = 1$
3. CPU0 to CPU1 = 2 clocks for $\overline{BGNT}$ pulse width; $\overline{DMAG} = 1$ and $\overline{BGNT} = 0$

Figure 2. DMA Arbitration Flow chart

Table 1 is the state transition table for the flow chart shown in figure 2; it incorporates outputs as a function of state, along with the inputs required to reach each state as a function of the present state. The RTMP is given priority over the UT1750AR, if bus request inputs $\overline{BRQ}$ and $\overline{DMAR}$ are asserted during the same clock period. Use a D-type flip-flop to sample the state machines outputs; clock the D-type flip-flop on the complementary phase of the clock. Sampling the outputs eliminates instability due to asynchronous inputs.

Table 1. State Transition Tables

PRESENT STATE \ $\overline{DMAR}$ $\overline{BRQ}$ $\overline{BGACK}$	000	001	011	010	110	111	101	100
IDLE (A)	A/11	D/01	D/01	A/11	A/11	A/11	B/10	A/11
CPU0 (B)	C/10	C/10	C/10	C/10	C/10	C/10	C/10	C/10
CPU1 (C)	A/11	D/01	D/01	A/11	A/11	A/11	B/10	A/11
RTMP0 (D)	E/01	E/01	E/01	E/01	E/01	E/01	E/01	E/01
RTMP1 (E)	F/01	F/01	F/01	F/01	F/01	F/01	F/01	F/01
RTMP2 (F)	G01	G/01	G/01	G/01	G/01	G/01	G/01	G/01
RTMP3 (G)	H/01	H/01	H/01	H/01	H/01	H/01	H/01	H01
RTMP4 (H)	I/01	I/01	I/01	II/01	I/01	I/01	I/01	I/01
RTMP5 (I)	J/01	J/01	J/01	J/01	J/01	J/01	J/01	J/01
RTMP6 (J)	K/01	K/01	K/01	K/01	K/01	K/01	K/01	K/01
RTMP7 (K)	A/11	D/01	D/01	A/11	A/11	A/11	B/10	A/11



*** Notes:**
1) RTMP priority 1, UT1750AR priority 2.
2) If $\overline{BGACK} = 0$, return to or stay in Idle State (A).

Simplified state transition is shown in table 2.

Table 2. State Transition Tables

INPUT	P.S.	N. S.	OUTPUT
XX0	0000	0000	11
111	0000	0000	11
101	0000	0001	10
001	0000	0011	01
011	0000	0011	01
XXX	0001	0010	10
XX0	0010	0000	11
111	0010	0000	11
101	0010	0001	10
001	0010	0011	01
011	0010	0011	01
XXX	0011	0100	01
XXX	0100	0101	01
XXX	0101	0110	01
XXX	0110	0111	01
XXX	0111	1000	01
XXX	1000	1001	01
XXX	1001	1010	01
XX0	1010	0000	11
111	1010	0000	11
101	1010	0001	10
001	1010	0011	01
011	1010	0011	01

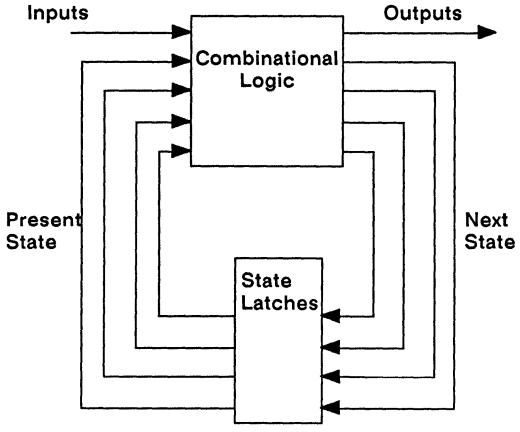


Figure 3. Circuit Representation for Synchronous Sequential Machine

A logic synthesis tool was used to simplify table 2 into the following equations:

```
MODULE NONAME

INPUT  IN1 IN2 IN3 IN4 IN5 IN6 IN7
OUTPUT OUT1 OUT2 OUT3 OUT4 OUT5 OUT6

NETWORK

* input buffering *
I1 INV1 IN1 : BIN1
I2 INV1 IN2 : BIN2
I3 INV1 IN3 : BIN3
I4 INV1 IN4 : BIN4
I5 BUF11 IN5 : BIN6 BIN5
I6 INV1 IN6 : BIN7
I7 INV1 IN7 : BIN8

* sub min term generation *
I8 NOR2 BIN3 IN7 : SN1
I9 NOR2 BIN7 BIN8 : SN2

* output bit 1 *
I10 NAND2 BIN5 SN2 : N1
I11 NAND2 BIN7 IN4 : N2
I12 NAND2 N2 N1 : OUT1

* output bit 2 *
I13 NAND2 BIN6 SN2 : N3
I14 NAND2 BIN8 BIN5 : N4
I15 NAND2 BIN7 BIN5 : N5
I16 NAND3 N5 N4 N3 : OUT2

* output bit 3 *
I17 NAND4 BIN6 BIN4 BIN1 SN1 : N6
I18 NAND2 IN7 BIN7 : N7
I19 NAND3 BIN8 IN6 BIN5 : N8
I20 NAND3 IN6 BIN1 SN1 : N9
I21 NAND4 N9 N8 N7 N6 : OUT3

* output bit 4 *
I22 NAND2 BIN2 SN1 : N10
I23 NAND2 BIN1 SN1 : N11
I24 NAND3 BIN8 BIN7 IN4 : N12
I25 NAND4 N12 N4 N11 N10 : OUT4

* output bit 5 *
I26 INV1 SN2 : N13
I27 NAND4 N2 BIN6 N13 N11 : N14
I28 INV1 N14 : OUT5

* output bit 6 *
I29 NAND2 BIN8 BIN3 : N15
I30 NAND2 BIN8 IN2 : N16
I31 NAND6 N2 BIN6 N13 N11 N16 N15 : OUT6

ENDMODULE
```

Interfacing the RTR to the 80C51 8-Bit Microcomputer

INTRODUCTION

The UTMC UT1553B RTR is a monolithic CMOS integrated circuit that meets the requirements of a MIL-STD-1553B remote terminal interface. The RTR integrates the remote terminal logic with a user-configured 1K x 16 static RAM. The RTR provides protocol, message handling, error checking, and memory control functions for a MIL-STD-1553B remote terminal.

A basic remote terminal using the RTR consists of the following: UT1553B RTR, UT63M125 Transceiver, discrete interface logic, bus interface transformers, optional system memory, and a host microprocessor.

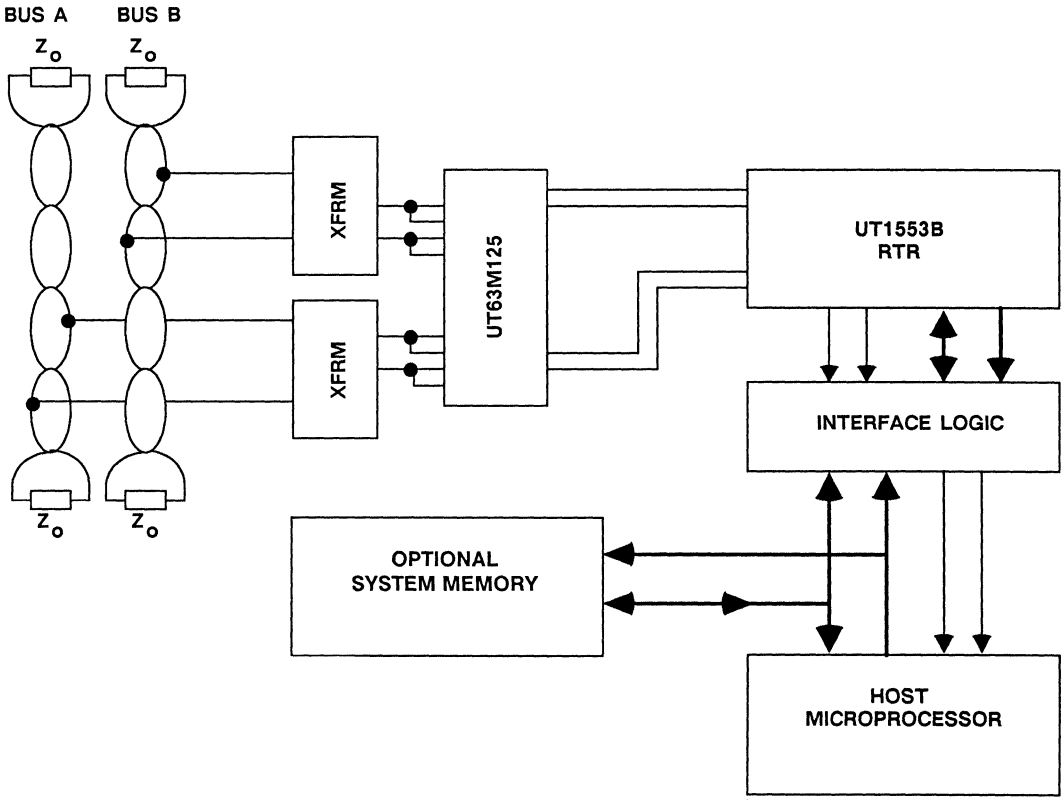


Figure 1. Remote Terminal Interface

The function of the host microprocessor is to define the memory mapping for message handling, configure the RTR for operation, supply (write) information to the RTR for message transmission, and retrieve (read) information stored as a result of message reception. To define the memory map the host microprocessor must write to 64 memory locations within the RTR's 1K of memory. Reading and writing information to the RTR is accomplished via microprocessor input/output (I/O) functions; the RTR interprets these functions as either register read/write or memory read/write.

Optional system memory is added to support specific remote terminal requirements. Interface logic supplies buffering, signal conditioning, and isolation between the microprocessor and RTR. The transceiver and transformers provide coupling to the MIL-STD-1553 bus.

This application note will discuss the configuration of a remote terminal consisting of an RTR and 80C51 microcontroller. The interface logic will specifically address the design problems associated with interfacing an 8-bit (byte-oriented) microcomputer with a 16-bit (word-oriented) peripheral. Due to the flexibility of the 80C51 controller, certain design problems are addressed only conceptually, allowing system designers to tailor design solutions to their systems. The reader should reference the UTMC UT1553B RTR data sheet when using this application note.

General System Description

Using an 8-bit microcomputer to control a 16-bit peripheral presents a problem that is easily solved using data latches and software. The basic problem is that the microcomputer reads and writes in a 8-bit-wide format and the RTR in a 16-bit-wide format. Since the RTR accepts only 16-bit-wide data, external hardware is necessary for data conversion.

Write cycle data conversion is accomplished using an 8-bit-wide three-state latch to store the lower 8 bits of write data while the microcomputer prepares the upper 8 bits for transfer. Once the upper 8 bits are transferred to the Data bus, the three-state latch containing the lower 8 bits is enabled; the two 8-bit sections are merged into a 16-bit word and transferred to the RTR.

For read cycles one 8-bit-wide three-state latch is used to store the low-byte data transferred from the RTR; the high-byte is transferred and latched directly into the microcomputer during the read cycle. The microcomputer reads the low-byte of data, transferred into the latch from the RTR, during a second read cycle.

The RTR has five input signals used to interface a microcomputer to itself ($\overline{CS}$, RD/$\overline{WR}$, $\overline{CTRL}$, $\overline{OE}$, RBUSY). With the exception of RBUSY, the microcomputer uses the interface signals ($\overline{CS}$, RD/$\overline{WR}$, $\overline{CTRL}$, $\overline{OE}$) to read and write to the RTR's internal memory and registers. The RBUSY signal is used to notify the host microcomputer (i.e. 80C51) that the RTR is going to take control of the internal RAM. The delay between the RBUSY signal assertion and the RTR taking control of the RAM is user programmable (i.e. 2.7 μs or 5.7 μs). The UT1553B RTR data sheet defines the timing requirements for accessing the RAM and internal RTR resisters along with the setup of RBUSY. The interpretation of RBUSY by the microcomputer is system specific depending on data transfer rates, software requirements, hardware overhead, etc.

From a system standpoint the RTR can map directly into the 64K data space of the 80C51. Address decode and location of the RTR in system memory is system dependent and is not discussed in this application note.

Data Port Interface

As described in the general system interface, data is read and written to the RTR in 8-bit sections. To perform this task, transceivers, data latches, and software-controlled signals are incorporated into the data port interface. Software-generated signals control the flow of information between the 80C51 and RTR. Figures 3a and 3b show a data port interface schematic.

The following discussion breaks the data port interface into two sections -- the software interface and the hardware interface.

RAM Write Software Interface

To access external memory the 80C51 is first configured to generate read and write signals ($\overline{RD}$ and $\overline{WR}$). $\overline{RD}$ and $\overline{WR}$ are alternate functions of Port 3 in the 80C51 that enable external memory for read or write functions. Setting Port 3 bit-latches 6 and 7 to a logic one invokes alternate functions $\overline{WR}$ and $\overline{RD}$. The SETB (set bit) command is used to write to Port 3 bit-latches 6 and 7.

After the external memory functions are enabled, the address of the RTR RAM location is written into the Data Pointer Register (DPTR) within the 80C51. Writing to the 16-bit DPTR requires two move (MOV) commands to load high-byte and low-byte data.

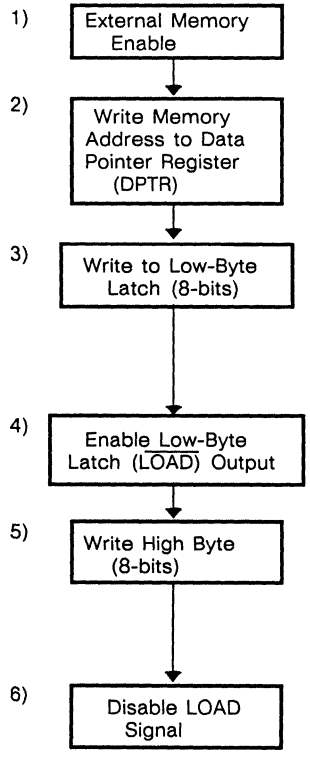
An external indirect move command (MOVX @Ri, A) loads the low-byte data latch; the contents of the accumulator are moved to the low-byte latch via Port 0. Signals A0 (low), $\overline{WR}$ (low), and $\overline{LOAD}$ (high) control the low-byte data latch enable. Once the low-byte data latch is loaded, the $\overline{LOAD}$ signal is asserted (logic 0). The high-byte is written to Port 0 via an external indirect move command (MOVX @DPTR, A). During execution of the move command, the assertion of signal $\overline{LOAD}$ in conjunction with $\overline{WR}$ enables the output buffers of the low-byte latch. Enabling the low-byte data latch during the write cycle supplies both the low-byte and high-byte of data simultaneously to the RTR. Data is written into the RTR during the external move command (MOVX

@DPTR, A). The $\overline{LOAD}$ signal is negated upon completion of the write cycle. Figure 2 shows a sample flow chart and assembly language code. Figure 5a shows an example of write cycle timing.

Control Register Write

The software to perform a Control Register write is similar to that used to write to RTR RAM. A Control Register write is performed using the same software; however, the $\overline{CTRL}$ signal (i.e., Port 3 bit 1) is set to a logic zero. The address information the DPTR supplies is "do not care" during Control Register write cycles since address information is not needed. To set the $\overline{CTRL}$ signal to a logic zero, make the following changes to the code.

```
Replace  MOV B0, #FEh      ;Port 3 bit 1 = 1
With     MOV B0, #FCh      ;Port 3 bit 1 = 0
```




```
1)  SETB P3.6          ;enable alternate function WR
    SETB P3.7          ;enable alternate function RD

2)  MOV 82h, #LB       ; move the lower byte of the
                       ; memory location into the Data
                       ; Pointer Register low byte
    MOV 83h, #HB       ; move the high byte of the
                       ; memory location into the Data
                       ; Pointer Register high byte

3)  MOV R0, #00        ; move 00 into register R0 (low-byte
                       ; indirect addressing)
    MOV A , #DLB       ; move low-byte data into
                       ; accumulator
    MOVX @R0, A        ; move external the contents of
                       ; the accumulator to the low-
                       ; byte latch (A0=0)

4)  MOV B0, #FEh       ; assert (active low) LOAD
                       ; signal Port 3 bit 0=0
                       ; Port 3 bit 1=1 (i.e. CTRL)

5)  MOV A, #DHB        ; move high-byte data into
                       ; accumulator
    MOVX @DPTR, A      ; move external the contents of
                       ; the accumulator to the memory
                       ; location pointed to by the
                       ; contents of the Data Pointer
                       ; Register (DPTR)

6)  MOV B0, #FFh       ; move FF (hex) into Port 3
                       ; disables the LOAD signal P3.1
```

Figure 2. Example Data Port Interface Software (Memory Write)

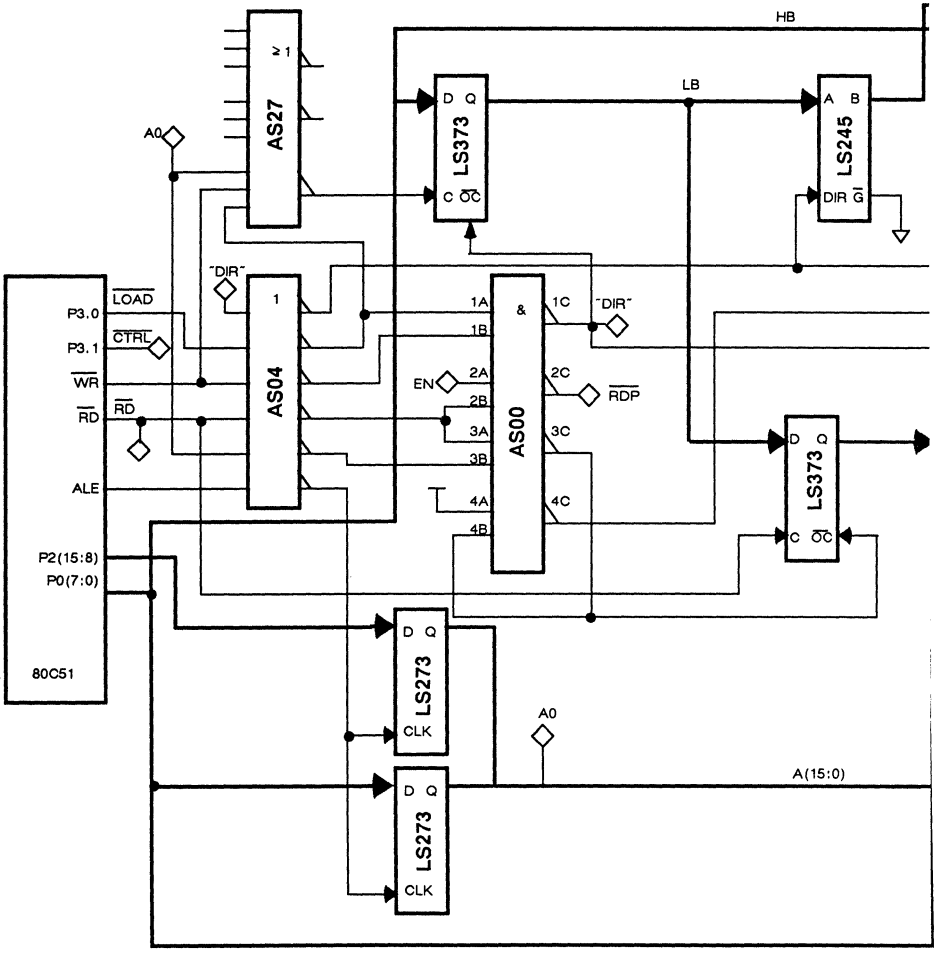
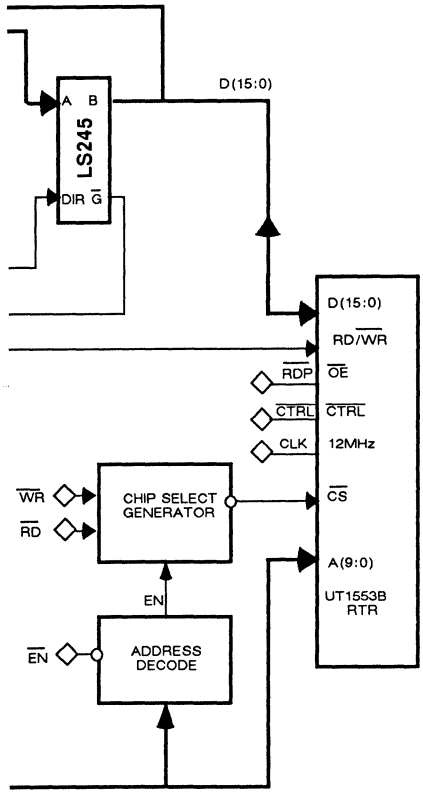


Figure 3a. 80C51 Data Port Interface



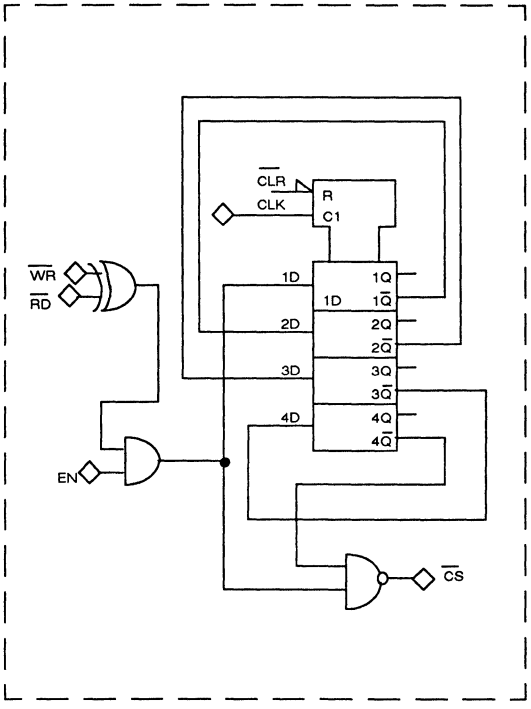


Figure 3b. Chip Select Generator

RAM Read Software Interface

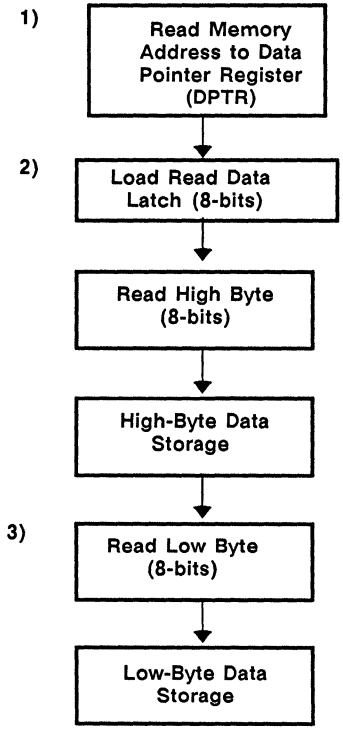
The address of the RTR RAM location is written into the Data Register Pointer (DPTR) within the 80C51. Writing to the 16-bit DPTR requires two move (MOV) commands to load high-byte and low-byte data.

The low and high bytes of read data are latched using an external indirect move command (MOVX A, @DPTR). The low-byte data is stored in an 8-bit-wide data latch (read data latch). The high byte is read during the execution of the indirect external move command (MOVX A, @DPTR). Once loaded into the accumulator, the data is then moved to a storage location to prevent an overwrite during the low-byte read. The low byte is read from the read data latch using an indirect external move command (MOVX A, @R0). Read data is latched on the falling edge of the $\overline{RD}$ signal; the output buffers are enabled on the low-byte read cycle $\overline{RD}$ (low) and A0 (low). To prevent the overwrite of data written into the read data latch during the low-byte read, the output enable ($\overline{OE}$) of the RTR is negated. Figure 4 shows a sample flow chart and assembly language code. Figure 5b shows an example of read cycle timing.

Status Register Read

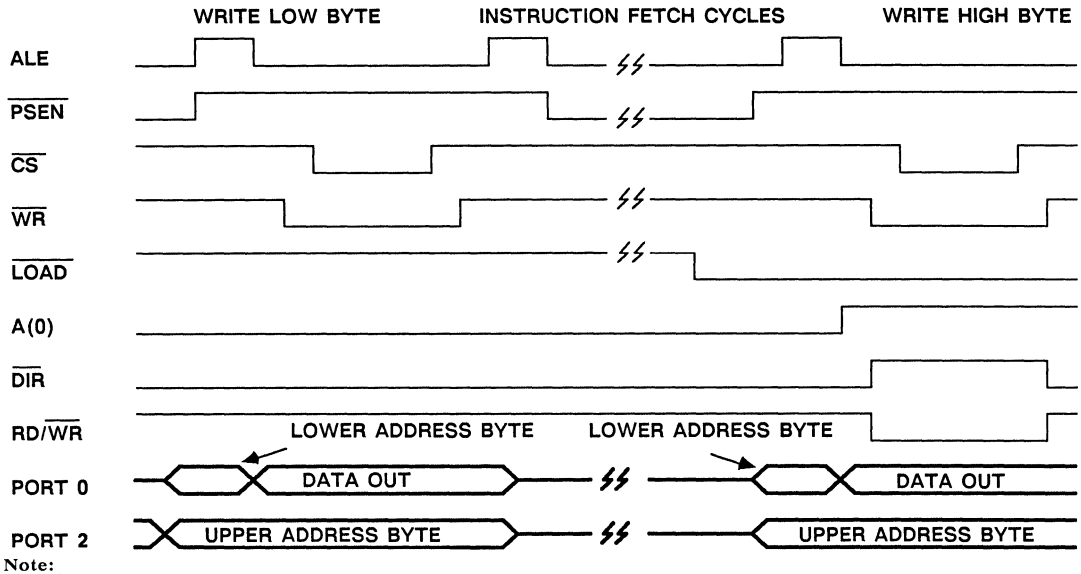
The software to perform a Status Register read is similar to that used to read RTR RAM. A Status Register read is performed using the same software; however, the $\overline{CTRL}$ signal (i.e., Port 3 bit 1) is set to a logic zero. The address information the DPTR supplies must generate an address enable ($\overline{EN}$) during Status Register read cycles. To set the $\overline{CTRL}$ signal to a logic zero, make the following changes to the code.

```
Replace  MOV B0, #FEh      ;Port 3 bit 1 = 1
With     MOV B0, #FCh      ;Port 3 bit 1 = 0
```



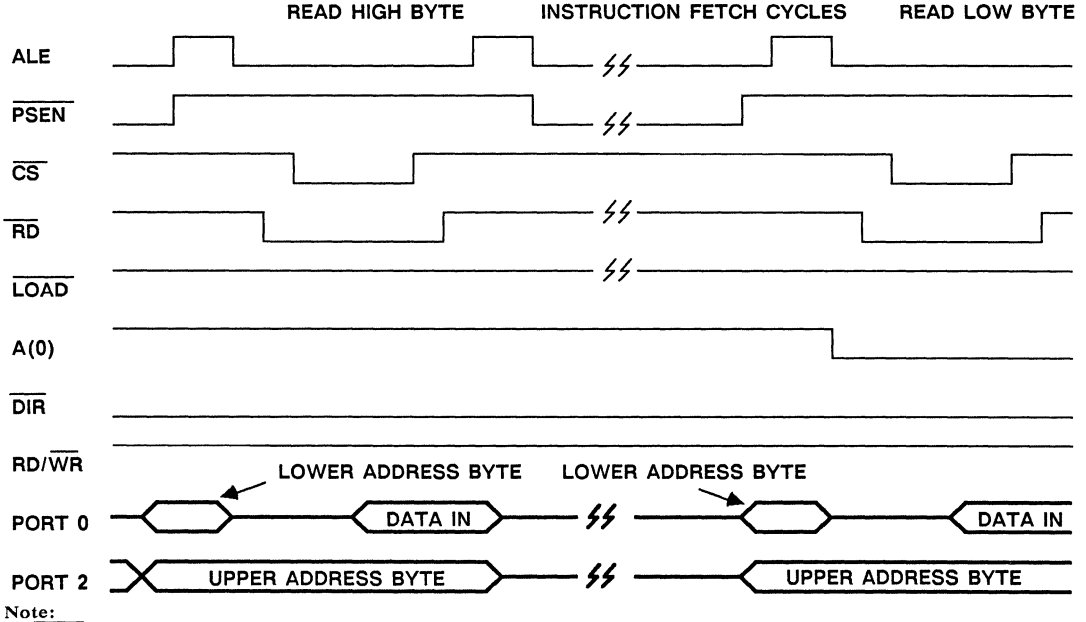

```
1)  MOV 82h, #LB    ; move the lower byte of the
                    ; memory location into the Data
                    ; Pointer Register low-byte
                    ; DPTR
    MOV 83h, #HB    ; move the high byte of the
                    ; memory location into the Data
                    ; Pointer Register high byte
2)  MOV A, @DPTR    ; move the contents of the RTR
                    ; RAM location pointed to by the
                    ; DPTR register into the read
                    ; data latch and accumulator
    MOV R0, #00     ; move 00 into register R0
                    ;(low-byte indirect addressing)
    MOV @temph, A   ; move accumulator to
                    ; temporary storage

3)  MOV A, @R0      ; move the low-byte contents of
                    ; read data latch into the
                    ; accumulator
    MOV @templ, A   ; move accumulator to
                    ; temporary storage
```

Figure 4. Example Data Port Interface Software (Memory Read)



Note:
1. CTRL defined as a logic one for RTR RAM write, and a logic zero for RTR register write.

Figure 5a. RTR Write Cycle Timing



Note:
1. CTRL defined as a logic one for RTR RAM read, and a logic zero for RTR register read.

Figure 5b. RTR Read Cycle Timing

Hardware Interface

Figures 3a and 3b show an example of a data port interface. Figures 5a and 5b respectively show the timing diagrams for a write cycle and read cycle.

A write to the RTR requires two machine cycles of the 80C51. During the first machine cycle the low-byte of the 16-bit word is written to the data latch. The second machine cycle is used to transfer the high-byte of the data word along with the low-byte to the RTR. The machine cycles shown between the low and high-byte write cycles are required for fetches and executes of program code. Software instructions enable the $\overline{RD}$ and $\overline{WR}$ signals to generate read and write strobe signals. These signals latch data and control the direction of data moving between the 80C51 and the RTR. Control signal $\overline{LOAD}$ (Port 3 bit 0) is generated via software and serves as an output enable for the three-state write data latch. Address bit zero differentiates between low-byte (A(0) = 0) and high-byte (A(0) = 1). Signals $\overline{LOAD}$ and $\overline{WR}$ are logically combined to generate the RD/$\overline{WR}$ signal for the RTR.

Inverted signal $\overline{DIR}$ controls the direction of data via the bus transceiver (LS245). During the write cycle, $\overline{DIR}$ is logic zero; the inverted $\overline{DIR}$ signal is then used as the direction input to the bus transceiver. For read cycles $\overline{DIR}$ is logic one, allowing information to move from the RTR into the read data latch. During the low-byte read cycle the high-byte transceiver is high impedance to allow information passage from the read data latch into the 80C51.

Control signal $\overline{CTRL}$ specifies whether the RTR access is RAM or register oriented. For simplicity Port 3 bit 1 is programmed to implement the $\overline{CTRL}$ signal. If the designer is constrained such that Port 3 is not available for such a function, the RTR internal registers can be mapped into memory and the address decoded to generate $\overline{CTRL}$.

The logical OR of the 80C51 read strobe ($\overline{RD}$) and address enable ($\overline{EN}$) asserts the output enable ($\overline{OE}$) of the RTR during read cycles. Address enable is used to three-state the RTR outputs during subsequent read cycles when the RTR is not selected for read access.

RTR RAM and registers are defined as chip select ($\overline{CS}$)-controlled memory accesses. The $\overline{CS}$ signal is generated whenever a read or write cycle occurs and the address A(15:0) corresponds to a location where the RTR is memory mapped. A schematic to generate a $\overline{CS}$ signal is shown in figure 3b; for the circuit shown the $\overline{CS}$ signal is asserted for four clock cycles (approximately 330 ns). The $\overline{CS}$ signal is generated by address decode and the falling edge of $\overline{RD}$ or $\overline{WR}$. The minimum $\overline{RD}$ or $\overline{WR}$ pulse the 80C51 generates is 400 ns, therefore the hold time requirements of the RTR are met.

CONCLUSION

The data port interface between the 80C51 and the UT1553B RTR is easily implemented to solve the 8-bit to 16-bit conversion. The task requires a small amount of software and hardware overhead.

RTR/RTS Internal Self-Test Routine

Introduction

The self-test capability of the UT1553B RTR and UT1760A RTS is based upon the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the output encoder is fed back to the input decoder, the decoder will recognize the incoming status word as a command word (wrap-around test). The RTR/RTS will interpret the command word and react accordingly (e.g. transmit a status word); status word transmission results in continuation of the wrap-around test. The host microprocessor monitors the System Register, status outputs, and last command data to determine if the RTR/RTS is functioning properly. Pass/fail criteria is based on a comparison, performed by the host, of expected data versus data extracted from RTR/RTS. The RTR/RTS does not contain any internal hardware designed to test functionality.

The host controls the self-test by changing bit patterns in the status word being transmitted. The host alters the status word by periodically writing to the RTR/RTS Control Register. Writing to Control Register bits that correspond to MIL-STD-1553B status word bits allows the host to control the incoming command word the RTR/RTS receives. The host controls the Service Request, Subsystem Flag, System Busy, Instrumentation, and Terminal Flag by writing to the Control Register. The reader should reference one of two additional UTMC publications when using this application note: the current UT1553B RTR or UT1760A RTS data sheets.

Self-Test Configuration

The first step is initialization of the RTR/RTS. Always initialize the RTR/RTS into a known state by using the master reset before performing self-test. Define the last command data pointer and subaddress/mode code data pointers by performing RAM writes to the appropriate locations. To begin self-test the host writes to the Control Register, setting the Self-Test Enable bit (bit 6) to a logic one. Disable output encoder Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The status word is sent to decoder A or B depending on the channel the host selected for self-test (Control Register bit 5). The status word wraps back into the RTR/RTS via the input decoder channel. Figure 1 shows an example of wrap-around test scheme.

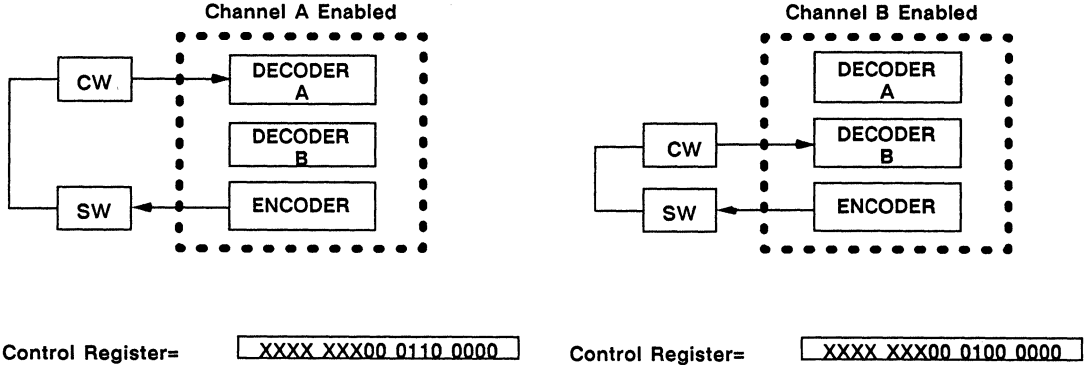


Figure 1. Wrap-around Test

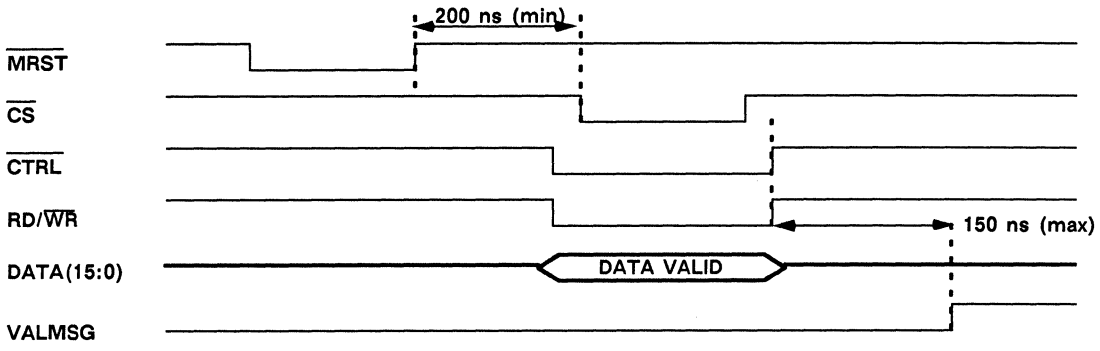
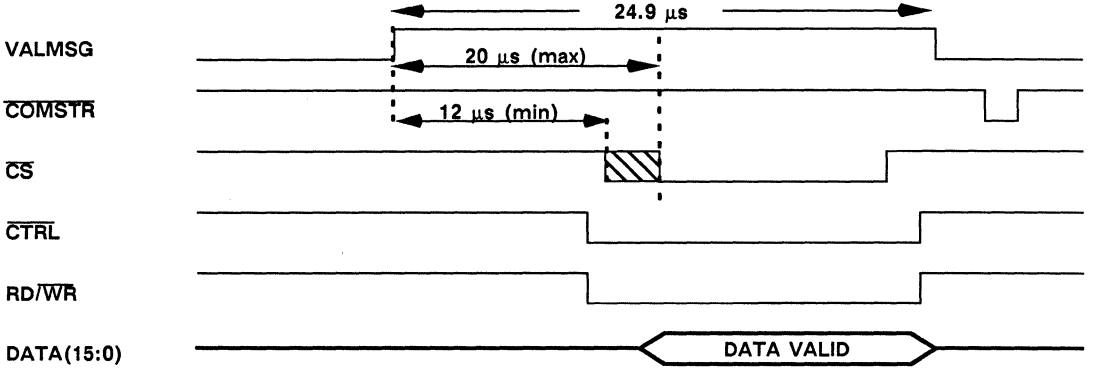


Figure 2a. Reset Control Register Write to VALMSG Active

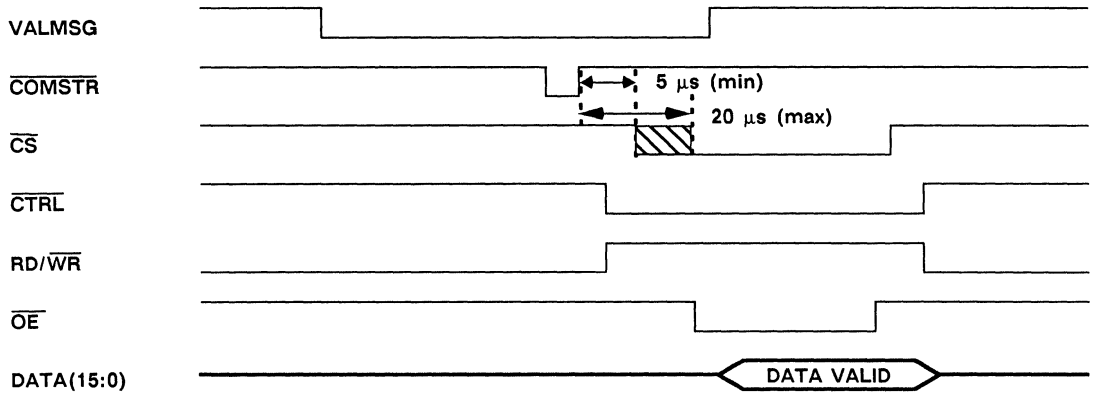


Note:
1. The host can write to the Control Register during a window defined by the assertion of VALMSG. The window opens 12 µs after the assertion of VALMSG and closes 20 µs later.

Figure 2b. Control Register Write Window

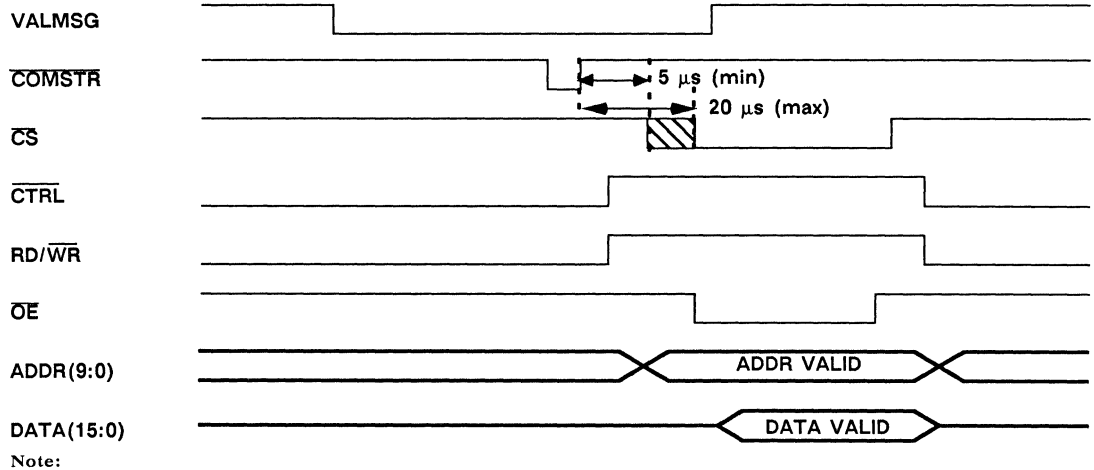
Control Register Write
Writing to the Control Register bits 2, 3, 4, 7, and 8 changes the status word. Write to the Control Register 12 µs (minimum) after the VALMSG pin is asserted; this does not change the contents of the status word being transmitted. Upon receiving the next command word, the transmitted status word reflects the updated Control Register contents. Figure 2 shows an example of the timing for a Control Register write with respect to the assertion of signal VALMSG; refer to the RTS or RTR data sheet for Control Register write timing specifications.

Monitoring Self-Test
Read the Status Register and retrieve last command word information to monitor how the self-test is performing. The output status pins also supply information regarding the state of the self-test routine. The host reads the Status Register by performing a Status Register read after every command strobe ($\overline{\text{COMSTR}}$) negation. The status register is read 5 µs (minimum) after the rising edge of $\overline{\text{COMSTR}}$. The last command word the RTR/RTS receives is stored at the memory location contained at internal RAM location 3E0 (hex) after the first RBUSY assertion. During the configuration of the device for self-test the host initializes location 3E0 (hex); it is recommended that the host set the index field of the data pointer (i.e., location 3E0 (hex)) to zero. This action results in the RTR/RTS storing the last command received at one memory location, which is then treated as a last command register and is read immediately following the Status Register. Figures 3 and 4 show examples of the Status Register read and the last Command Register read.



Note:
1. The host can read the Status Register during a window defined by the negation of $\overline{\text{COMSTR}}$. The window opens 5 µs after the negation of $\overline{\text{COMSTR}}$ and closes 15 µs later.

Figure 3. Status Register Read



Note:
1. The host can read the last command register during a window defined by the negation of $\overline{\text{COMSTR}}$. The window opens 5 µs after the negation of $\overline{\text{COMSTR}}$ and closes 15 µs later.

Figure 4. Last Command Memory Location Read Window

Self-Test Start-Up

After the host enables self-test the RTR/RTS behaves as if it had just received and validated a command word (CW). The contents of the Command Word Latch (CWL) are decoded and the RTR/RTS will respond accordingly. After Master Reset the RTR/RTS Command Word Latch contains binary 0 00000 01000. The Command Word Latch contains bits 9 through 19 of the command word. Sync Field Data, Remote Terminal Address, and Parity bit are removed before storage in the Command Word Latch.

The RTR/RTS decodes the Command Word Latch contents as illegal and asserts the two message error signals, the Message Error bit in the Status Register and the Message Error pin. The RTR/RTS then asserts the VALMSG signal indicating transmission of the status word (SW) is about to begin. 12 µs after the assertion of VALMSG, a Control Register write is

performed to modify the status word. Clear the Busy bit and set the Terminal Flag bit to a logic one in the Control Register. The Status Word transmitted following the assertion of signal VALMSG does not have the Terminal Flag bit set; however, the Busy bit is set to logic one. Transmission of the status word (BUSY = 1, TF = 0, ME = 1) results in the Command Word Latch being loaded. The RTR/RTS decodes the contents of the Command Word Latch as legal. VALMSG signal is asserted and a status word with TF = 1 and ME = 0 is transmitted. 12 μs after the VALMSG signal is asserted the Control Register is again updated. Figure 5 shows an example flow chart of a self-test sequence. Status Register and last command register reads are omitted.

Setting the Terminal Flag (TF), Subsystem Busy (SUBS), and System Busy (BUSY) bits exercises various mode codes. The example flow chart illustrates the setting of one bit at a time; by setting more than one bit the RTR/RTS receives the following mode codes.

BUSY	SUBS	TF	
0	0	0	Dynamic Bus Control
0	0	1	Synchronize
0	1	0	Transmitter Shutdown
0	1	1	Override Transmitter Shutdown
1	0	0	Reset Remote Terminal

The RTR/RTS decodes these command words as valid (ME = 0) or illegal (ME = 1) depending on the logic state of the T/$\overline{R}$ bit in the command word.

Setting either the Instrumentation (INS) or Service Request (SRQ) bits in the Control Register results in the RTR/RTS interpreting the command word as a subaddress receive or transmit. Reception of a transmit command requires the RTR/RTS to first transmit a status word followed by the defined number of data words. The BUSY, SUBS, and TF bits control the number of data words. However, once the RTR/RTS transmits a status word, a command word is received and is treated as a superseding command, cancelling the transmit command. The RTR/RTS decodes the superseding command and responds accordingly. The RBUSY signal is asserted while the RTR/RTS tries to read the data for transmission.

The receive command is transmitted last in a self-test routine since it results in a bus time-out. After decoding the receive command the RTR/RTS waits for forthcoming data words. Following the time-out period, the RTR/RTS asserts the message error signal and does not transmit a status word. After the receive command is decoded a Control Register write is performed to disable self-test, enable Channel A, and enable Channel B. The Control Register write is performed following the rising edge of $\overline{\text{COMSTR}}$. Configure the RTR/RTS to begin normal operation following the assertion of the message error signal.

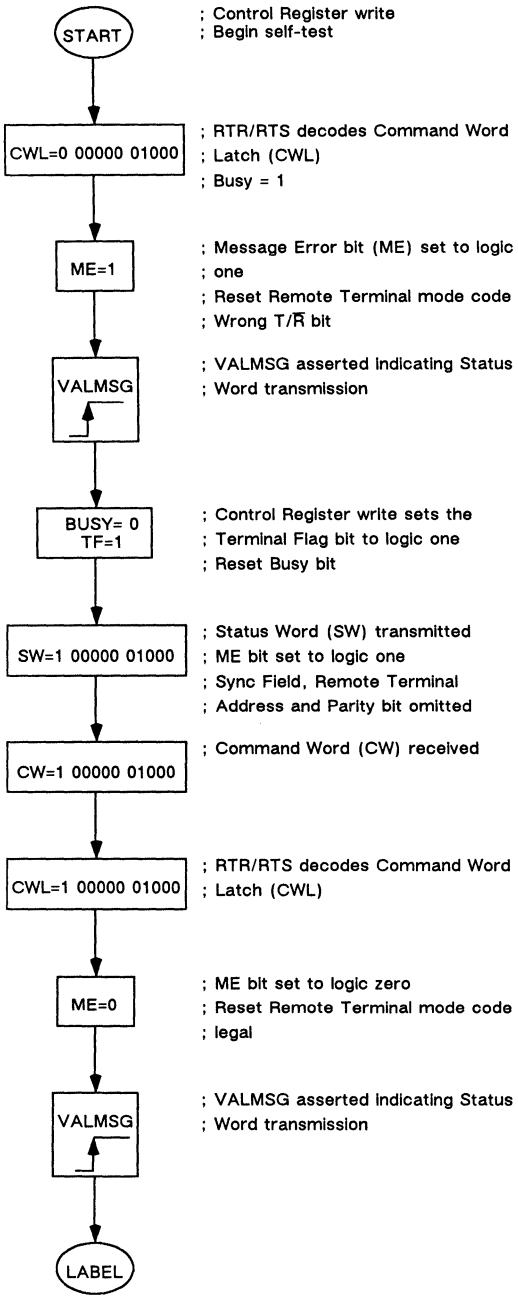


Figure 5a. Self-Test Flow Chart

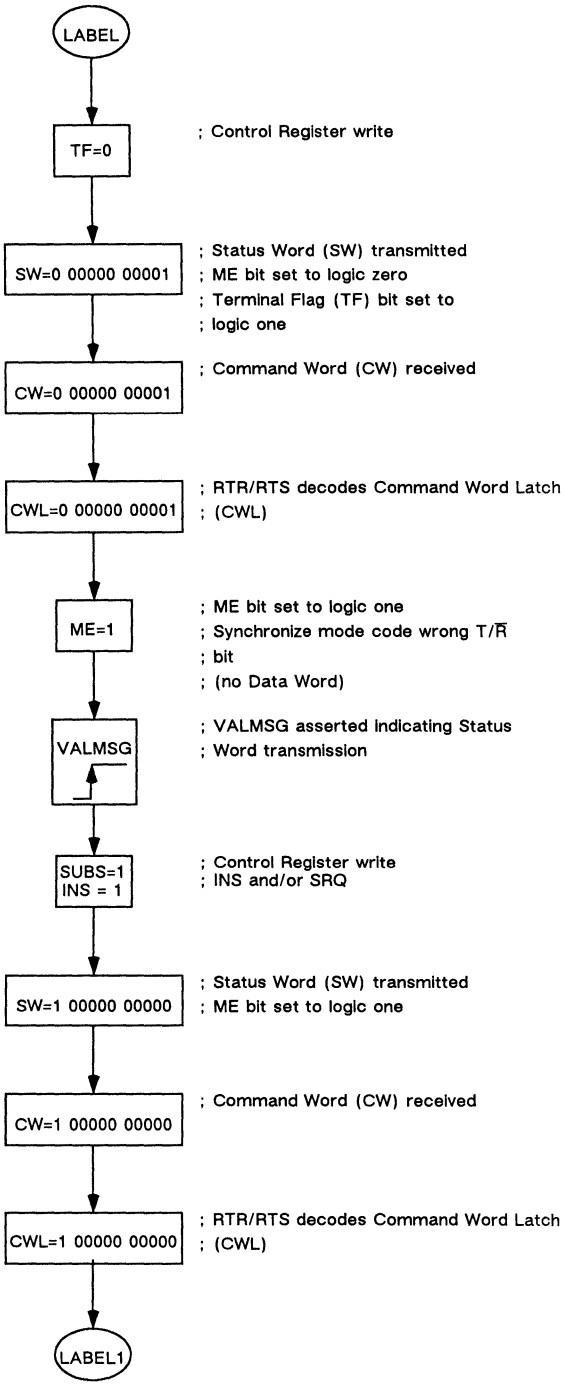


Figure 5b. Self-Test Flow Chart

4

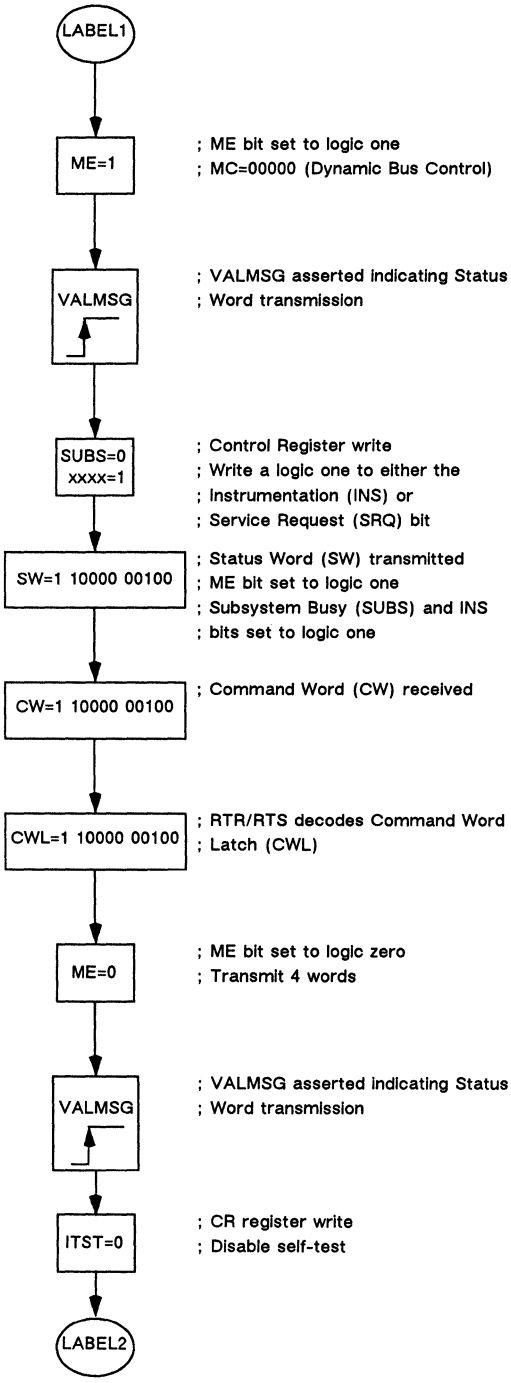


Figure 5c. Self-Test Flow Chart

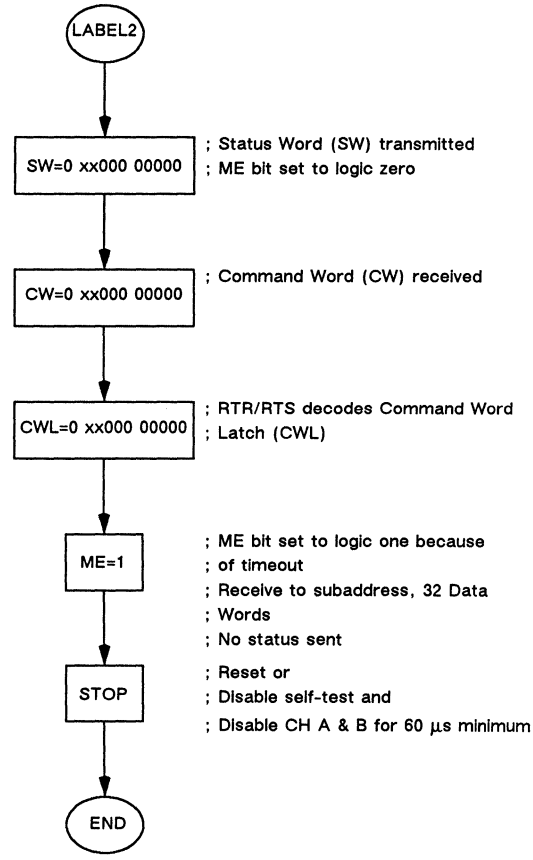


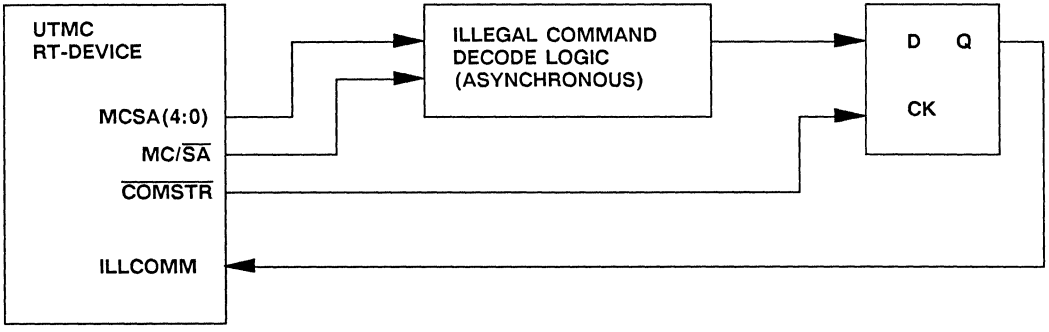
Figure 5d. Self-Test Flow Chart

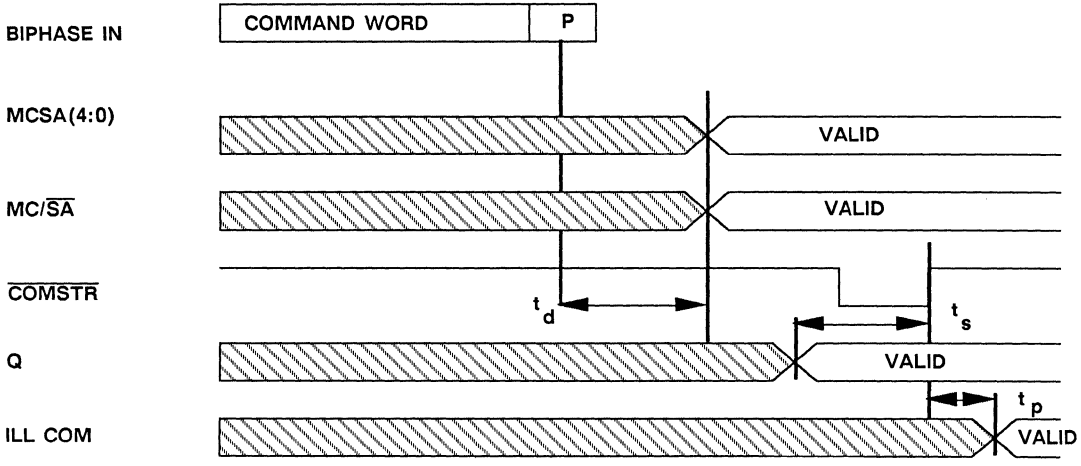
CONCLUSION

The wrap-around self-test allows the host to perform a rudimentary functionality test of the RTR/RTS. The logic blocks that the test controls and observes include input decoders, output encoders, Control Register (bits 2, 3, 4, 7, and 8), Status Register (bits 9, 10, 11, 13, and 14), and last command register. The last command register contents are corrupted as a result of the self-test routine. The RTR/RTS and the host accomplish the self-test routine in about 350 µs.

Simple Command Illegalization for the RT Family

A simple illegal command decoder for the MIL-STD-1553 Remote Terminal interface family consists of asynchronous decode logic and a D flip-flop. The output of the D flip-flop drives the illegal command input to the Remote Terminal interface (i.e., RTI, RTR, RTMP). The D flip-flop is clocked by the the rising edge of the command strobe pin ($\overline{\text{COMSTR}}$). The decode logic supplies the input stimulus to the D flip-flop. The decode logic propagation delay must be short enough to allow an acceptable set-up time for the D flip-flop. Refer to the specific remote terminal





Interfacing the BCRT to the 68000 16-Bit MPU

INTRODUCTION

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive MIL-STD-1553B Bus Controller and Remote Terminal functions. The BCRT design reduces the host computer's overhead requirements by automatically executing message transfers, providing interrupts, and generating status information. The BCRT accomplishes much of this off-loading with built-in memory management functions designed specifically for MIL-STD-1553B applications. This means the host need only establish the necessary data and/or control parameters in memory for the BCRT to access the information as required, thus providing the requisite MIL-STD-1553B bus functions.

Back to Basics

Several terms and concepts are involved in describing a multimaster microprocessor-based system. A bus master is a device capable of controlling the Address, Data, and Control buses. A multimaster system contains two or more master devices. Only one bus master can control the bus at any given time.

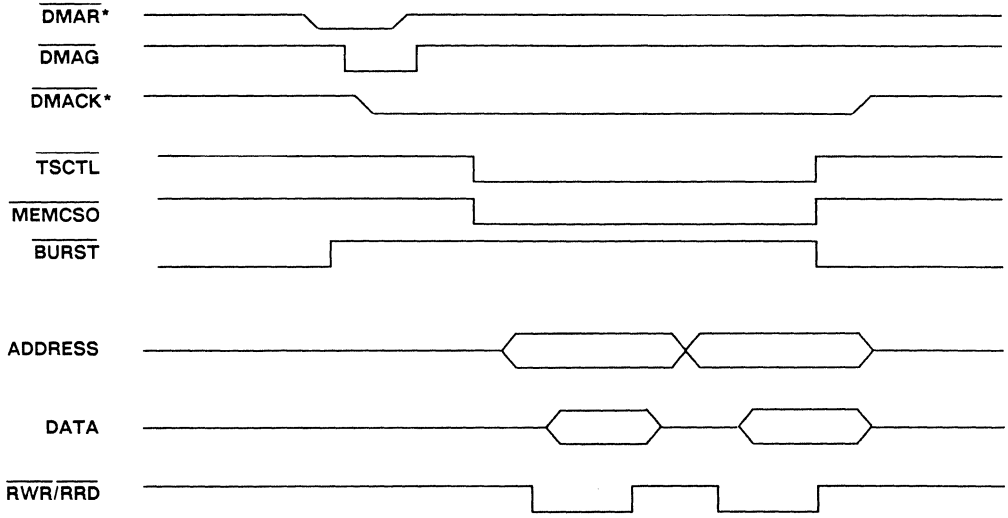
DMA Configuration

The BCRT interfaces easily into a 68000-based system. Except for the 68000 processor, the DMA configuration assigns the BCRT as the highest priority bus master in a multimaster system. This configuration requires using one or more 68000 processors, one or more BCRTs, and could also contain other bus masters. The following sections define the architecture of a system containing only two bus masters: a BCRT and a 68000.

DMA Arbitration

The process of the BCRT assuming control of the bus while another master relinquishes control is called DMA arbitration. Figure 1 depicts a DMA arbitration sequence. Three signals are involved in the arbitration process: $\overline{\text{DMAR}}$ (DMA Request), $\overline{\text{DMAG}}$ (DMA Grant), and $\overline{\text{DMACK}}$ (DMA Acknowledge). The requesting device asserts $\overline{\text{DMAR}}$ when it needs to control the bus. The controlling device recognizes the $\overline{\text{DMAR}}$ assertion and generates $\overline{\text{DMAG}}$ when it is finished with the bus. The requesting device deasserts $\overline{\text{DMAR}}$ and asserts $\overline{\text{DMACK}}$. The arbitration is now complete and the requesting device has become the controlling bus master.

The other signals associated with DMA are $\overline{\text{DMAGO}}$, BURST, and $\overline{\text{TSCTL}}$. The $\overline{\text{DMAGO}}$ signal is for serially chaining multiple bus masters. The $\overline{\text{DMAGO}}$ signal passes the $\overline{\text{DMAG}}$ signal if the BCRT is not requesting the bus when $\overline{\text{DMAG}}$ is asserted. The BURST signal is an active high signal that indicates the current DMA cycle will transfer at least two words (worst case is five words). The $\overline{\text{TSCTL}}$ (Three-State Control) signal indicates when the BCRT is actually accessing memory. The host system's address and data lines must be in the high-impedance state when this signal is active.



*These signals transition from a high-impedance state to active low

Figure 1. DMA Timing (Refer to BCRT Data Sheet for Detailed Timing Information)

BCRT Memory Bus Signals

The BCRT bus signals are split into three groups: Address, Data, and Control. Four bidirectional signals (A0-A3) and 12 three-state signals (A4-A15) comprise the Address bus. The word size for the BCRT is always sixteen bits. The 68000 processor address references must be divided by two when compared to the BCRT. The Data bus consists of 16 bidirectional signals numbered D0 through D15. The memory control signals consist of $\overline{RRD}$ (RAM Read) and $\overline{RWR}$ (RAM Write). $\overline{RRD}$ pulses low during a DMA read operation, and $\overline{RWR}$ pulses low during a write operation. Figure 1 represents DMA read and write operations. Consult the UT1553B BCRT data sheet for actual timing relationships.

DMA Hardware Configuration

Figure 2 illustrates the DMA interface signal connections for a two-master system containing a 68000 and a BCRT. Four signals are involved: $\overline{DMAR}$ is connected to $\overline{BR}$ (Bus Request), $\overline{DMAG}$ is connected to $\overline{BG}$ (Bus Grant), $\overline{DMACK}$ is connected to $\overline{BGACK}$ (Bus Grant Acknowledge), and AEN is tied high.

Figure 3 is a block diagram illustrating the DMA and memory signals. Figure 4 shows a simplified circuit diagram containing the BCRT and 68000, along with a bank of static memory devices.

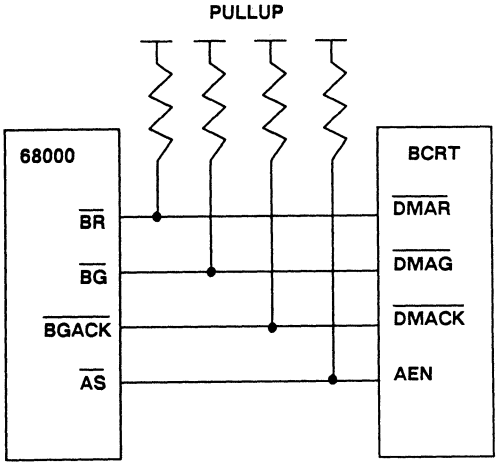


Figure 2. DMA Interface Signal Connections

CONCLUSION

This application note presents a system configuration example of the UT1553B BCRT'S interface to a typical 16-bit microprocessor using the 68000 as the processor. This information also applies to a wide variety of other microprocessors. For more detailed information on the UT1553B BCRT or other UTMC products.

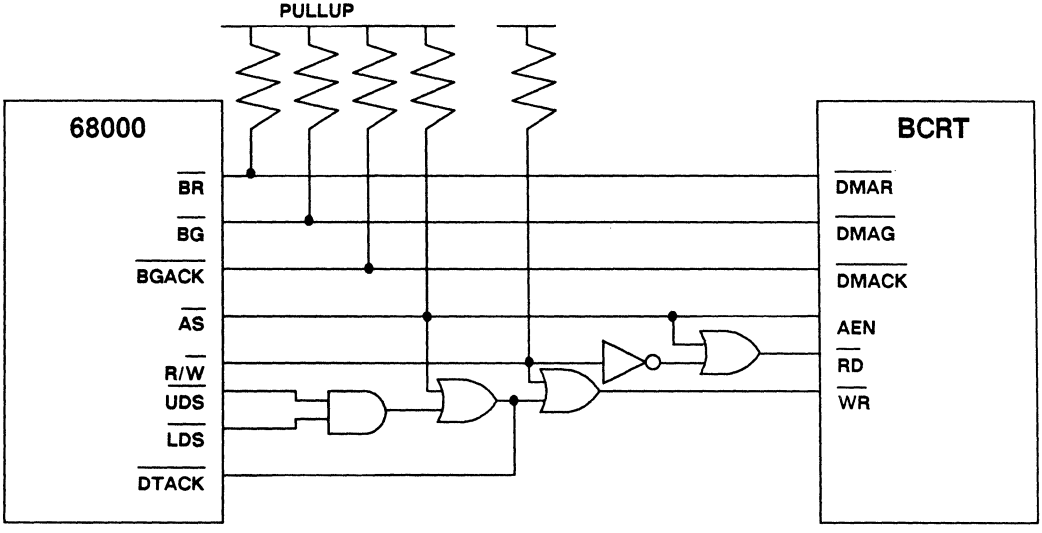


Figure 3. DMA and Memory Interface Signal Connections

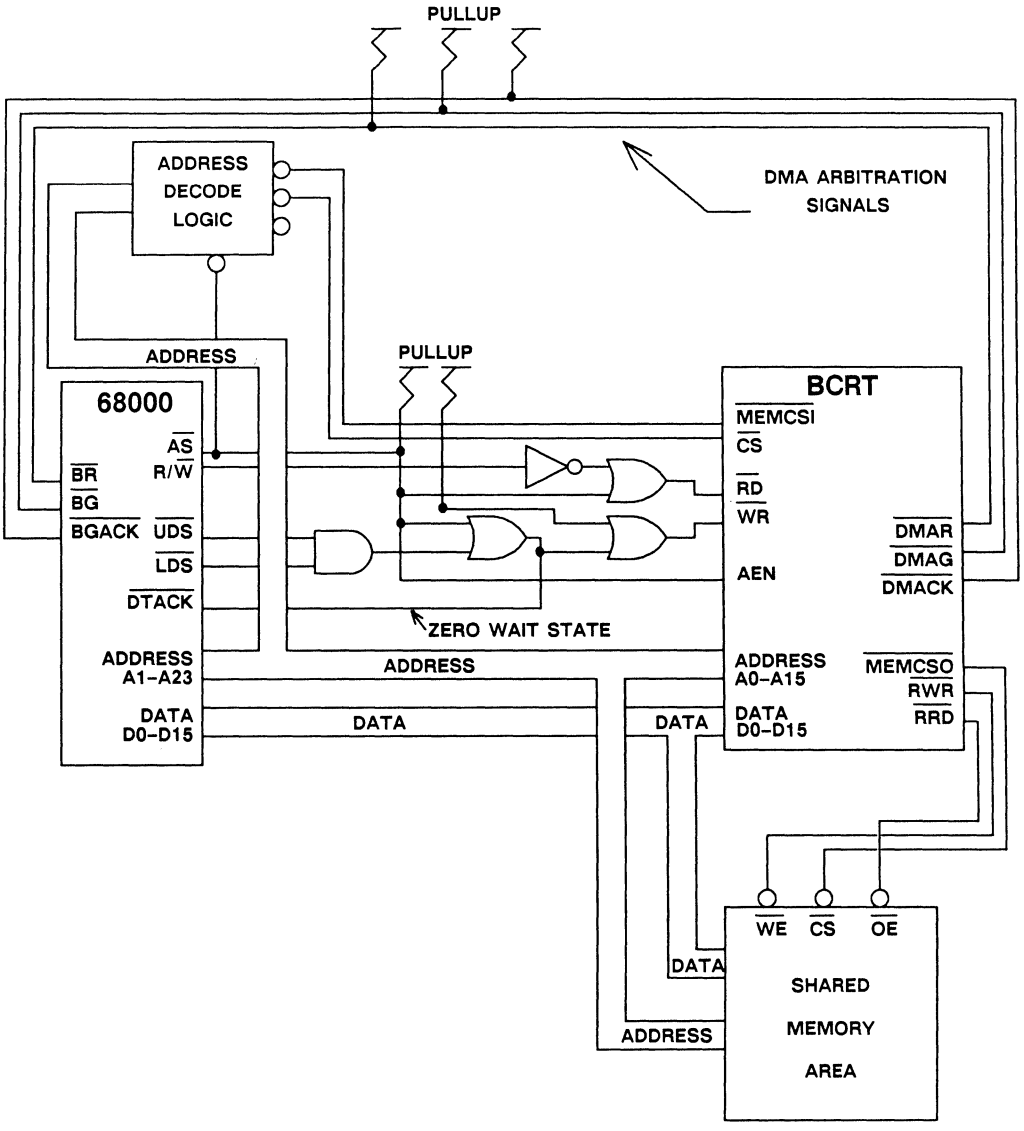


Figure 4. DMA Configuration

Cycle Stealing Interface for the UT1553B BCRT

Introduction

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive MIL-STD-1553B Bus Controller and Remote Terminal functions. The BCRT design reduces the overhead requirements placed on the host computer by automatically executing message transfers, providing interrupts, and generating status information. The host processor accomplishes much of its off-loading with built-in memory management functions designed specifically for MIL-STD-1553B applications. This means that the host need only establish the necessary data and/or control parameters in memory so the BCRT can access the information as required and, therefore, provide the requisite MIL-STD-1553B bus functions.

This application note provides a single-chip solution for interfacing the BCRT to a host processor or controller that does not have built-in DMA capability. The Cycle Stealing state machine, described in this application note, provides all the interface control for the BCRT/Host Processor interface.

The interface between the BCRT and the host processor generally takes one of two forms, either a standard DMA-type configuration or a Pseudo-Dual-Port RAM configuration. In either case, the host controls when the BCRT has access to RAM by controlling the Memory Request, Memory Grant, and Memory Acknowledge signals.

For some applications, the BCRT must interface with a processor or controller that does not have built-in DMA capability. In these applications, an alternate method for preventing bus contention is necessary. This Application Note discusses a method of preventing bus contention called Cycle Stealing.

Cycle Stealing prevents bus contention between the BCRT and the host processor by allowing the BCRT to take control of the address and data busses between the times when the processor is accessing memory. The BCRT performs cycle stealing by placing the host processor in a WAIT or HOLD state while the BCRT accesses shared memory.

The reader should reference two additional UTMC publications when using this application note. They are: (1) The UTMC UT1553B BCRT Data Sheet; and (2) Interfacing the BCRT to the 68000 16-Bit MPU application note.

General System Description

The BCRT is usually configured in either a DMA configuration or a Pseudo-Dual-Port RAM configuration. In either of these configurations the BCRT uses a set of memory bus signals to interface with the system RAM. The memory bus signals fall into three categories: Address signals, Bidirectional Data signals, and Control signals.

Of the 16 Address signals, 12 lines are three-statable and four lines are bidirectional. The four bidirectional Address lines are the four least significant bits of the Address. These four Address lines are bidirectional so the host processor can address the internal registers of the BCRT. The data bus consists of 16 bidirectional data lines; bit D15 is the most significant bit. Finally, the BCRT has three memory control signals. They are: RAM Read ($\overline{RRD}$), RAM Write ($\overline{RWR}$), and Memory Chip Select Out ($\overline{MEMCSO}$). The $\overline{MEMCSO}$ output selects external memory during memory accesses. The $\overline{RRD}$ and the $\overline{RWR}$ signals pulse low during a read operation or a write operation, respectively.

4

DMA Configuration

The block diagram of the BCRT/Host Processor interface in a DMA configuration is shown in figure 1. In a standard DMA configuration, the BCRT's and the host processor's data, address, and control signals are directly connected together. These signals remain in a high-impedance state until the host processor tries to access the BCRT's internal registers or until the BCRT accesses the system RAM.

Although the BCRT ignores any host processor attempt to access the BCRT's internal registers while the BCRT is accessing memory, the designer must use care to prevent the host processor from attempting an internal register access while the BCRT is performing a DMA operation. (Refer to Interfacing the BCRT to the 68000 16-bit MPU Application Note.)

Three signals are associated with the DMA arbitration process. The signals are: DMA request ($\overline{DMAR}$), DMA grant ($\overline{DMAG}$), and DMA acknowledge ($\overline{DMACK}$). The BCRT asserts $\overline{DMAR}$ when it requires the bus. The current bus controller asserts $\overline{DMAG}$ to signal the BCRT that the bus is available. When the BCRT assumes control of the bus, the BCRT removes $\overline{DMAR}$ and asserts $\overline{DMACK}$.

In addition to the $\overline{DMAR}$, $\overline{DMAG}$, and $\overline{DMACK}$ arbitration signals, three other signals are available from the BCRT to assist with DMA memory accesses. They

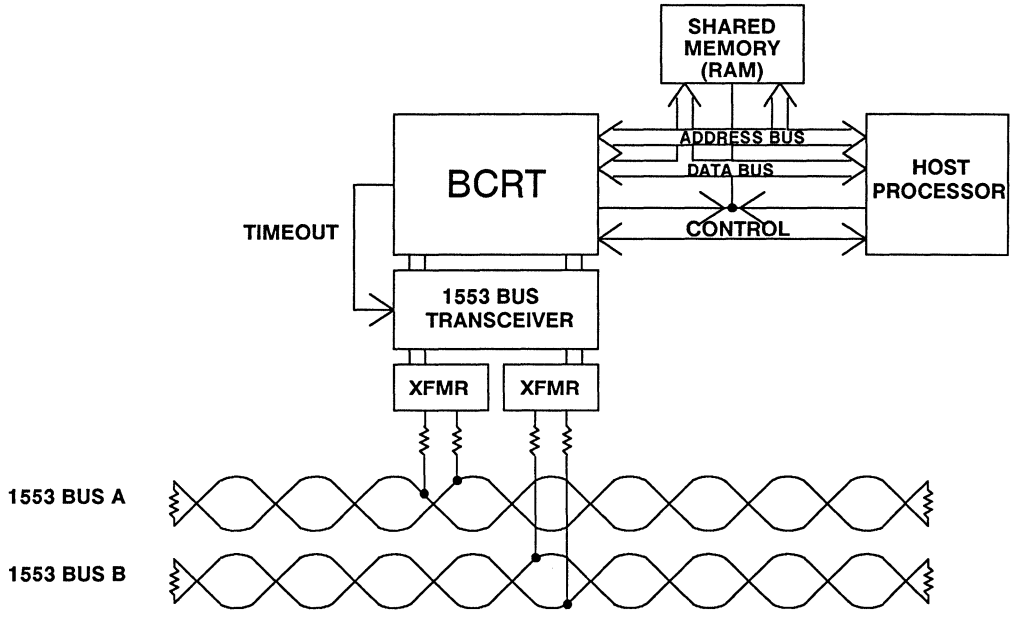


Figure 1. Host Processor/BCRT Interface -- DMA Configuration

are: DMA Grant Out ($\overline{\text{DMAGO}}$), DMA Burst (BURST), and Three-State Control ($\overline{\text{TSCTL}}$). The $\overline{\text{DMAGO}}$ output allows the $\overline{\text{DMAG}}$ input to propagate through the BCRT when $\overline{\text{DMAG}}$ is asserted and the BCRT is not requesting the bus. $\overline{\text{DMAGO}}$ is used when serially chaining multiple bus masters. The BURST signal indicates that the current DMA cycle transfers at least two words to memory but no more than five words. $\overline{\text{TSCTL}}$ indicates when the BCRT is actually accessing memory. When $\overline{\text{TSCTL}}$ is active, the host processor's data bus should be in a high-impedance state.

Pseudo-Dual-Port RAM Configuration

The block diagram of the BCRT/CPU interface in a Pseudo-Dual-Port RAM configuration is shown in figure 2. In the Pseudo-Dual-Port RAM mode, the BCRT and the host processor communicate through a shared memory area referred to as the Dual-Port RAM. The BCRT's address and data busses connect directly to RAM. Octal buffers isolate the BCRT's address and data busses from the host processor's. The host processor's memory control signals, Read ($\overline{\text{RD}}$), Write ($\overline{\text{WR}}$), and Memory Chip Select ($\overline{\text{MEMCSI}}$) connect directly to the BCRT and pass through BCRT as $\overline{\text{RRD}}$, $\overline{\text{RWR}}$, and $\overline{\text{MEMCSO}}$. $\overline{\text{RRD}}$, $\overline{\text{RWR}}$, and $\overline{\text{MEMCSO}}$ are then connected to the Output Enable ($\overline{\text{OE}}$), Write Enable ($\overline{\text{WE}}$), and Chip Select ($\overline{\text{CS}}$) inputs of the RAM chips. This configuration only requires using conventional static RAM.

For more information on interfacing the BCRT in either the DMA configuration or the Pseudo-Dual-Port RAM configuration, please refer to Interfacing the BCRT to the 68000 16-bit MPU Application Note.

The Cycle Stealing Configuration

The block diagram of the BCRT/CPU interface in a Cycle Stealing configuration is shown in figure 3. The Cycle Stealing configuration is similar to the Pseudo-Dual-Port RAM configuration except for adding the Cycle Stealing state machine (sequential logic). This state machine allows the BCRT to control when the host processor may access the shared memory area by placing the host in a HOLD or WAIT state while the BCRT is accessing memory. This is the main difference between the Cycle Stealing configuration and the DMA or Pseudo-Dual-Port RAM configurations. In the DMA or Pseudo-Dual-Port RAM configurations, the host processor controls memory access.

The Cycle Stealing state machine simplifies the interface between the BCRT and the host processor because the state machine performs all the bus arbitration functions. Since the BCRT places the host in a WAIT state during the BCRT's RAM accesses, from the host processor's point of view, the address and data busses are available for use at any time. Therefore, in the Cycle Stealing configuration the host processor need only be concerned about the BCRT when the BCRT reaches a predetermined interrupt point which is signaled to the host processor.

A detailed diagram of the BCRT in a Cycle Stealing configuration is shown in figure 4. The functional interconnections between the BCRT, the host processor, and the Cycle Stealing state machine are given. If the host processor has address, data, and control lines that enter a high-impedance state when a WAIT or HOLD state is entered, the designer can omit the buffers marked with (*).

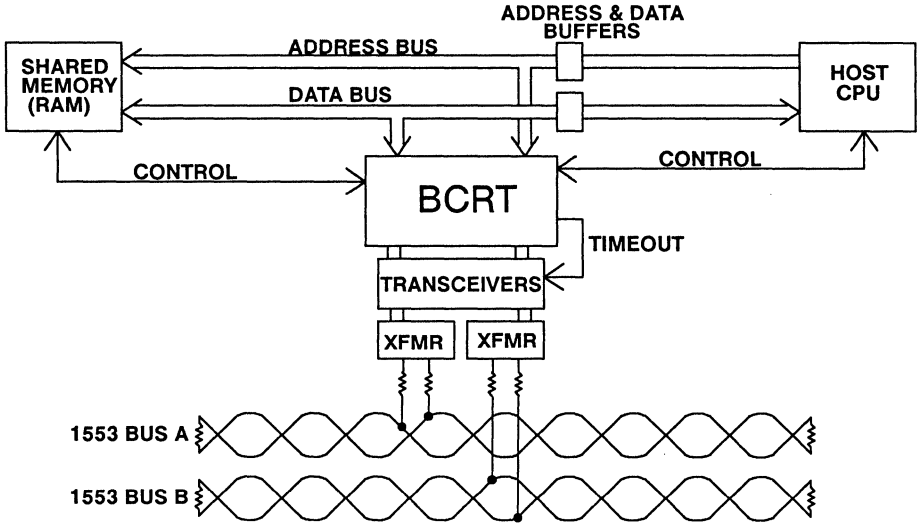


Figure 2. Host Processor/BCRT Interface -- Pseudo-Dual-Port RAM Configuration

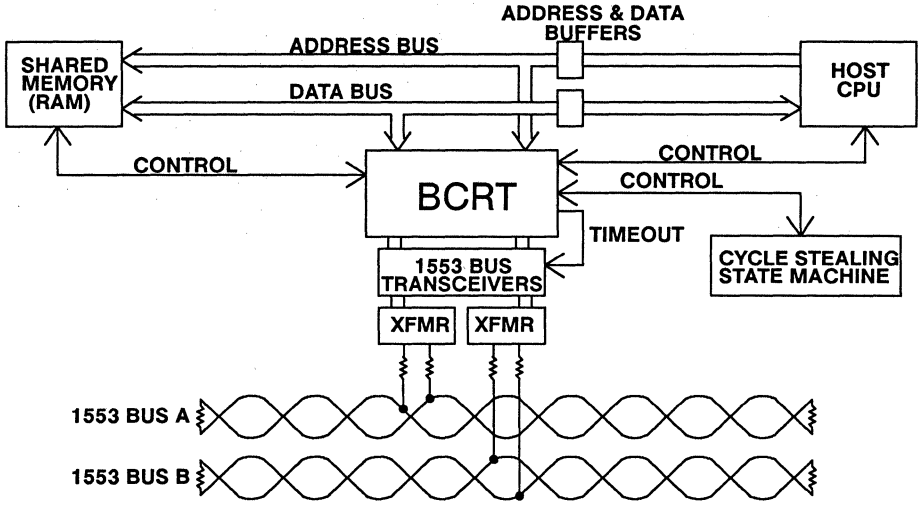


Figure 3. Host Processor/BCRT Interface -- Cycle Stealing Configuration

Cycle Stealing State Machine Design

State Machine ASM Chart

The first step in designing any state machine is to describe fully a specific sequence of events. This sequence of events defines the operations the state machine must accomplish to complete a given task. An ASM (Algorithmic State Machine) chart that describes the sequence of events for the Cycle Stealing state machine is shown in figure 5. Each of the rectangles in figure 5 represents one state, or clock cycle, of the state machine. Any text within a rectangle is an output for that state. The text within a decision diamond represents state machine inputs that must be acted on to alter state machine flow. Finally, the text within the ellipse is a conditional output.

The sequence of events in the ASM chart of figure 5 is explained below. This description assumes the state machine operates with a 12 MHz clock:

1. The state machine waits in state 000 until the $\overline{\text{DMAR}}$ input signal from the BCRT becomes active (low), indicating that the BCRT is requesting access to the shared memory. As soon as $\overline{\text{DMAR}}$ is active, the WAIT (or HOLD) output becomes active.

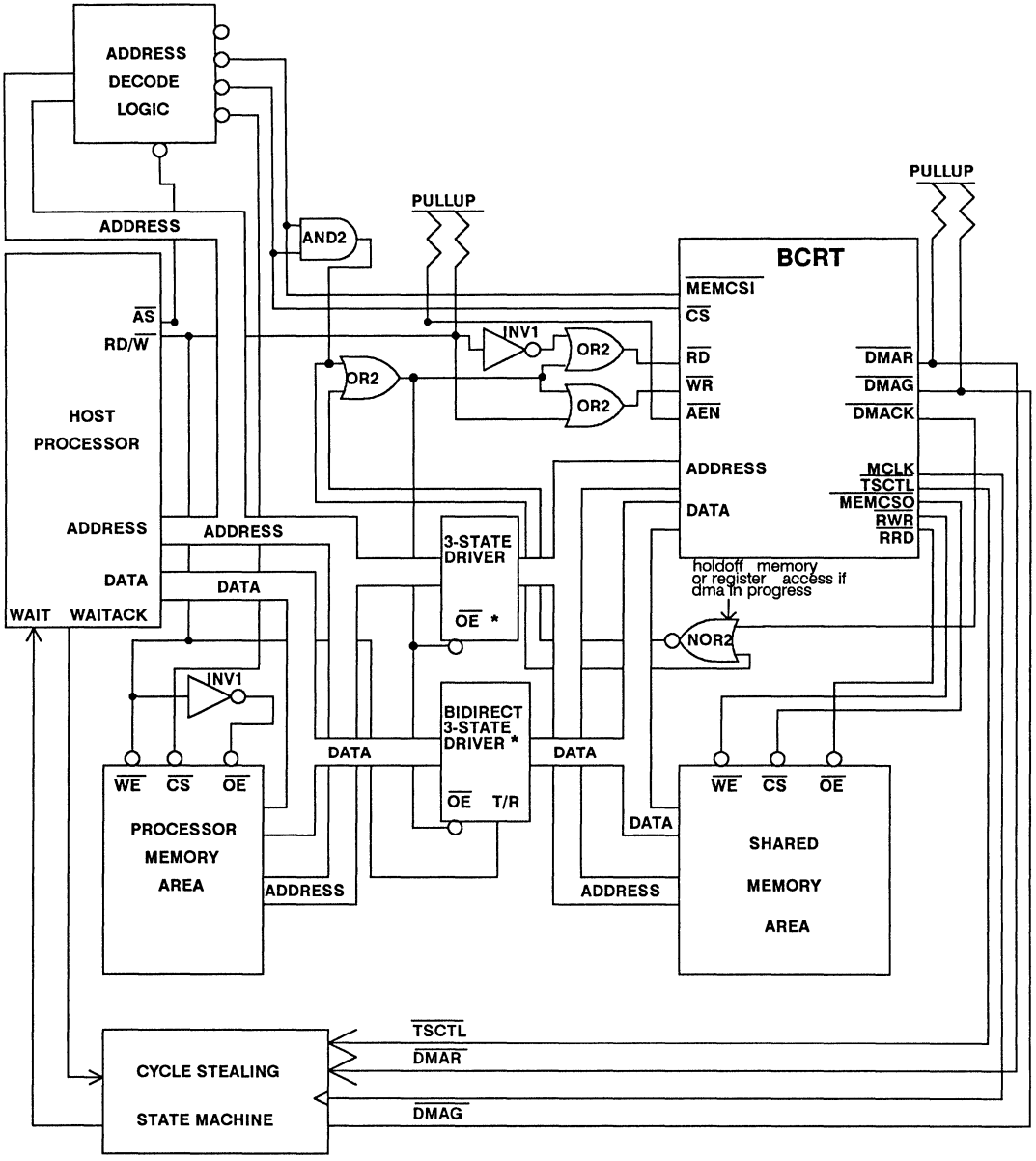
2. The state machine remains in state 001 until the Wait Acknowledge (WAITACK) input becomes active, indicating the host processor has actually entered a WAIT state.

3. States 010, 011, and 100 are identical and serve two purposes. First, they generate a sufficiently long $\overline{\text{DMAG}}$ for the BCRT to recognize, and second, they keep the WAIT output active. The timing requirement for $\overline{\text{DMAG}}$ is defined as tPW2 in figure 22 of the BCRT data sheet and has a minimum time of one MCLK period and a maximum period of six MCLK periods.

   There is a maximum amount of time that can elapse between state 001 and 010. This time period is given as tPHL4 in figure 22 of the BCRT data sheet and it is the time between $\overline{\text{DMAR}}$ going low and $\overline{\text{DMAG}}$ going low. This time depends on the frequency of the Memory Clock (MCLK) input. Therefore, the system designer should verify that the host processor does not violate this timing constraint when entering a WAIT state.

4. The state machine remains in state 101 until the BCRT's $\overline{\text{TSCTL}}$ output becomes active (low).

5. After $\overline{\text{TSCTL}}$ is active, the state machine advances to state 110 where it remains until $\overline{\text{TSCTL}}$ becomes inactive, indicating the BCRT has finished using the shared memory area. After the state machine has left state 110, WAIT is deasserted and the state machine returns to state 000 where the sequence repeats the next time the BCRT requires access to the shared memory area.



* If the Host Processor can three-state its buses, the designer can eliminate these buffers.

Figure 4. Detailed Block Diagram of the Cycle Stealing Configuration

The sequence of events described above is for a generalized host processor. Some processors require the WAIT or HOLD signal to be asserted only during a particular phase of the processor clock. If this is the case for your processor, then synchronize the WAIT output of the state machine with the host processor by using the processor clock, or other processor output, as an additional input to the state machine.

The maximum number of words the BCRT transfers to/from RAM in one burst is five. Given this, the maximum time the Cycle Stealing state machine holds the processor in a WAIT state is approximately 1.5 μs when using a MCLK of 12 MHz.

To determine the maximum WAIT time for a MCLK other than 12 MHz, use the following equation:

$$WAIT(max) = [(12 \times 1/MCLK) + tPHL2 + tPHL3]\ \mu s$$

The values for tPHL2 and tPHL3 are found in the BCRT data sheet.

State Machine Truth Table

When the Cycle Stealing ASM chart is complete, the designer can develop a truth table. This truth table is shown in table 1.

Table 1 assumes both WAIT and WAITACK are active HI signals. This table was developed by looking at each state in the ASM chart of figure 5. For each Present State and input combination, a Next State and state machine output is listed.

Table 1. Cycle Stealing State Machine Truth Table

INPUTS						OUTPUTS				
			PRESENT STATE			NEXT STATE				
$\overline{DMAR}$	WAITACK	$\overline{TSCTL}$	PS2	PS1	PS0	NS2	NS1	NS0	WAIT	$\overline{DMAG}$
H	X	X	L	L	L	L	L	L	L	H
L	X	X	L	L	L	L	L	H	H	H
X	L	X	L	L	H	L	L	H	H	H
X	H	X	L	L	H	L	H	L	H	H
X	X	X	L	H	L	L	H	H	H	L
X	X	X	L	H	H	H	L	L	H	L
X	X	X	H	L	L	H	L	H	H	L
X	X	H	H	L	H	H	L	H	H	H
X	X	L	H	L	H	H	H	L	H	H
X	X	L	H	H	L	H	H	L	H	H
X	X	H	H	H	L	L	L	L	H	H

Legend

L = TTL Lo
H = TTL Hi
X = Don't Care

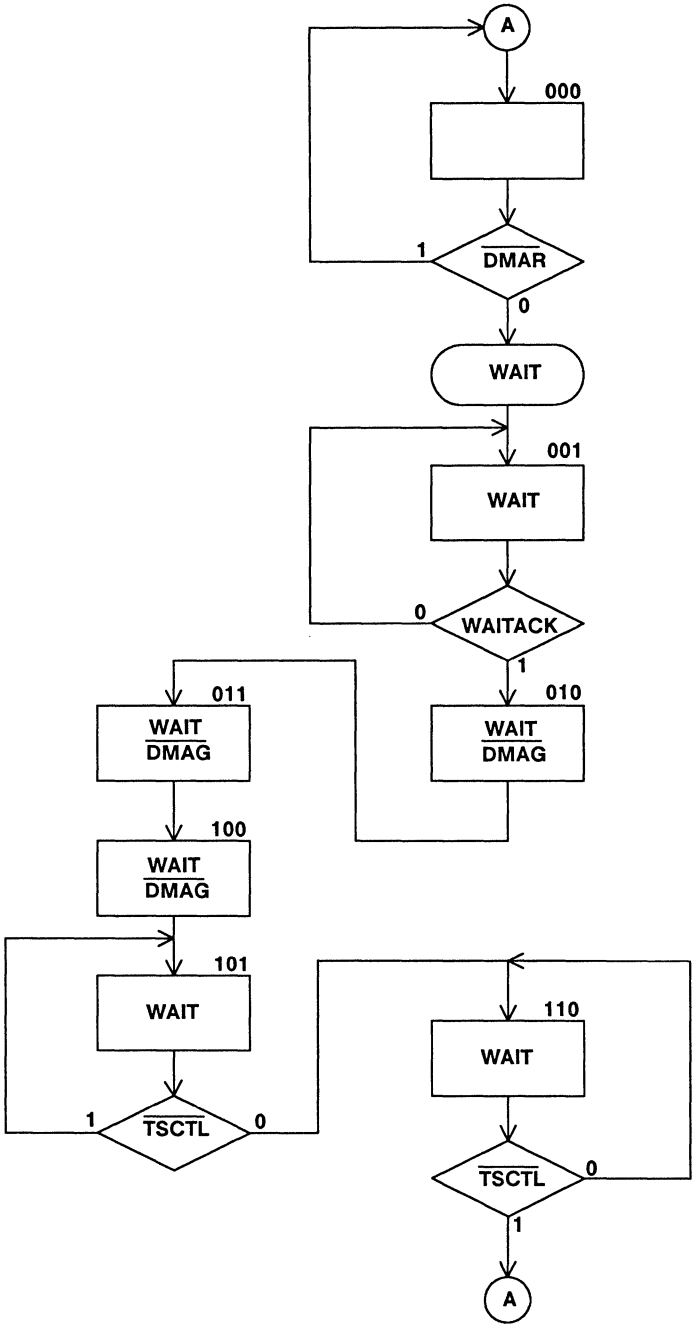


Figure 5. ASM Chart for the Cycle Stealing State Machine

Cycle Stealing Logic Equations

The final step in designing the Cycle Stealing state machine is translating the data in the truth table into a set of logic equations. The logic equations are given in table 2.

The WAIT output is active in every state except 000; the logic equation for WAIT is the inverse of WAIT for state 000. The state machine has a Clear input to set it to a known state when Clear is asserted. Finally, to increase the potential for "glitchless" operation of the WAIT output, route the WAIT signal through another register stage, as shown in equation 5 of table 2, for the WAITDG (Wait De-Glitch) signal.

Table 2. Cycle Stealing State Machine Logic Equations

1.	NS2	:= /PS2 * PS1 * PS0 * /CLR + PS2 * /PS1 * /PS0 * /CLR + PS2 * /PS1 * PS0 * /CLR + /TSCTL * PS2 * PS1 * /PS0 * /CLR
2.	NS1	:= WAITACK * /PS2 * /PS1 * PS0 * /CLR + /PS2 * PS1 * /PS0 * /CLR + /TSCTL * PS2 * /PS1 * PS0 * /CLR + /TSCTL * PS2 * PS1 * /PS0 * /CLR
3.	NS0	:= /DMAR * /PS2 * /PS1 * /PS0 * /CLR + /WAITACK * /PS2 * /PS1 * PS0 * /CLR + /PS2 * PS1 * /PS0 * /CLR + PS2 * /PS1 * /PS0 * /CLR + TSCTL * PS2 * /PS1 * PS0 * /CLR
4.	WAIT	:= /(DRAM * /PS2 * /PS2 * /PS0) * /CLR
5.	WAITDG	:= WAIT
6.	DMAG	:= /PS2 * PS1 * /PS0 * /CLR + /PS2 * PS1 * PS0 * /CLR + PS2 * /PS1 * /PS0 * /CLR

Legend

/ = Invert signal
* = Logical AND
\+ = Logical OR
:= = Registered output

CONCLUSION

Implementing the logic equations for the Cycle Stealing state machine easily fits into a 20-pin registered programmable logic device, such as a 16R8, 16RP8, 16V8, EP310, or any other equivalent device.

UT1553B BCRT True Dual-port Memory Interface

Introduction

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive MIL-STD-1553B Bus Controller and Remote Terminal functions. The BCRT design reduces the overhead placed on the host computer by automatically executing message transfers, providing interrupts, and generating status information. The BCRT off-loads the host processor with built-in memory management functions designed specifically for MIL-STD-1553B applications. This means that the host need only establish the necessary data and/or control parameters in memory so the BCRT can access the information as required and, therefore, provide the requisite MIL-STD-1553B bus functions. UTMC variants of the BCRT are the BCRTM, a BCRT with monitor functions, and the BCRTMP, a BCRT which operates in a wide variety of 1553 protocols.

This note will discuss a true dual-port (TDP) interface configuration. The design uses a 2K x 16 dual-port memory device available from several manufacturers. If additional memory is needed, the designer can incorporate more than one memory chip. Some manufacturers also offer single package dual-port RAM assemblies in configurations up to 8K x 16. This interface is applicable to the BCRT, the BCRTM, and the BCRTMP.

True Dual-port Configuration

The TDP configuration's main advantage over both the DMA (direct memory access) and PDP (pseudo dual-port) configurations is that it generates minimal impact on the host processor's operations. In the DMA configuration, the processor must be put on "hold" during any BCRT memory access. Using the PDP method, the processor must wait for the BCRT whenever the BCRT is accessing common memory. The only time the processor must wait in the TDP configuration is when the processor tries to access the exact same memory location to which the BCRT already has access, or when the host processor needs to access one of the BCRT's internal registers and the BCRT is in a memory cycle.

The TDP configuration's main disadvantage is cost. The price of dual-port devices is significantly higher than that of standard memory, and the density of the memory devices is lower. Of course, in a system where throughput is the driving issue, the TDP method is the most effective solution.

Circuit Operation - Memory Arbitration

Figure 1 shows the circuit's basic configuration. Figure 2 details operation of the PLD. The PLD is designed as a Mealy machine to improve response time and simplify state transitions. The dual-port RAM contains two signals: $\overline{\text{BUSYL}}$ and $\overline{\text{BUSYR}}$. When both the host and BCRT access the same memory locations at the same time, one of these signals will assert. Generally, the rules outlined in table 1 are followed.

Table 1. Simultaneous Memory Arbitration

CONDITION	"WINNING" SIDE	NOTES
left X ns before right	left	1
right X ns before left	right	1
left/right within X ns of each other	arbitration	1,2

1. X = detection limit; this value is between 2 and 10 ns depending upon the device used.
2. Arbitration algorithm depends on device. Examples: always give to left, give to side which didn't have it last, random, etc.

The TDP configuration outlined in this note uses $\overline{\text{BUSYL}}$, $\overline{\text{BUSYR}}$, $\overline{\text{DMAR}}$, $\overline{\text{DMAG}}$, $\overline{\text{MEMCSI}}$, $\overline{\text{BCRTCS}}$, and $\overline{\text{READY}}$ to properly arbitrate RAM use.

When the BCRT needs to read or write to dual-port memory, it asserts $\overline{\text{DMAR}}$. If (or when) the host access to memory is inactive (i.e., $\overline{\text{MEMCSI}}$ is deasserted), $\overline{\text{DMAG}}$ will be asserted and the BCRT will begin its memory cycle. Note that in this case, the memory location being accessed does not affect the arbitration decision. This would seem to defeat the purpose of the dual-port. However, the BCRT- side arbitration must work this way for the following combination of reasons:

1. In order to determine a "busy" condition in the dual-port RAM, all addresses must be known.

2. Once the BCRT receives $\overline{\text{DMAG}}$, there is no way to delay completion of its memory cycle.

Thus, if we try to give the BCRT a grant and use $\overline{\text{BUSYR}}$ for a collision, there is no way to use $\overline{\text{BUSYR}}$ to delay the BCRT when an address match occurs. This is really not a problem; since the BCRT's "throughput" is not very high, it can afford to wait for a host memory

cycle to complete. Figure 3 shows BCRT-memory access timing.

Note: Most host access times are small (1/10) compared to the BCRT request-to-grant requirement of 1.9 µs at 12 MHz. However, when designing a system, this requirement should not be overlooked.

When the host accesses memory, it is only delayed if a collision occurs, thus realizing the advantage of the dual-port RAM. If and only if an address match occurs, $\overline{\text{BUSYL}}$ will assert and the host will have to wait for the BCRT to complete its cycle. If the host accesses a memory location other than the one the BCRT is using, both the BCRT and host will complete their memory cycles normally. Figure 5 shows the timing diagrams for host-memory accesses both with and without arbitration.

A special arbitration case may also occur in this design. After the BCRT receives a $\overline{\text{DMAG}}$, the host may access memory. The BCRT may take up to four MCLK periods before it actually begins the memory access, thus it is possible the host may begin a cycle after $\overline{\text{DMAG}}$ has asserted but before $\overline{\text{MEMCSO}}$ on the BCRT asserts. Since the BCRT has already started a cycle, it is too late to stop this access. If the host and BCRT address the same memory location in this situation, $\overline{\text{BUSYR}}$ will assert. As was already stated, there is no way to stop the BCRT in this situation. To correct this problem, the host will be delayed if $\overline{\text{BUSYR}}$ asserts. The $\overline{\text{READY}}$ signal will deassert and the chip select to the host side of memory will be blocked. This clears the $\overline{\text{BUSYR}}$ condition. The BCRT will complete its cycle. After completion, the host chip select will be reasserted and the host cycle will complete.

The PLD device controls all of the arbitration. It consists of a state machine to control access to the "BCRT bus" and some random logic to generate the $\overline{\text{READY}}$ signal.

Special Cautions
Since this document is written for a "generic" processor, some cautions are necessary for direct use of this design:

1. To prevent multiple BCRT read/write operations, the $\overline{\text{BCSI}}$ (BCRT chip select in) signal must be asserted low for no more than one cycle after the falling edge of $\overline{\text{READY}}$.

2. The $\overline{\text{READY}}$ signal stays in an asserted state to facilitate faster memory access times. Thus during a host-to-BCRT cycle, the $\overline{\text{READY}}$ signal must deassert high first. This deassertion may take as long as two clock cycles.

3. During a host-to-BCRT register read, the data from the BCRT is only valid for one clock cycle after the $\overline{\text{READY}}$ signal is asserted low.

4. During a host-to-memory cycle, the $\overline{\text{READY}}$ signal is asynchronous; it may change to a deasserted state at any time during the cycle. As long as the host cycle does not complete while $\overline{\text{READY}}$ is deasserted, no problems will occur.

Register Arbitration

The same Address/Data bus is used for both BCRT register access by the host and memory access by the BCRT. Thus, when the host accesses a BCRT internal register, it must wait for the BCRT to complete a current memory cycle. This is accomplished using the host's $\overline{\text{READY}}$ signal and the BCRT's $\overline{\text{DMACK}}$ signal. When the BCRT is given a grant, $\overline{\text{DMACK}}$ is asserted until the BCRT is finished. The assertion of $\overline{\text{DMACK}}$ will prevent the address/data buffers and the $\overline{\text{READY}}$ line from being enabled. When the BCRT completes, the buffers are enabled. One clock cycle later, the $\overline{\text{READY}}$ signal will assert. Figure 4 shows the timing diagrams for host-BCRT accesses with and without arbitration.

Further Assistance

Due to the variety of processors to which the BCRT can be connected, this document cannot address all the possibilities. Contact UTMC applications support for additional assistance.

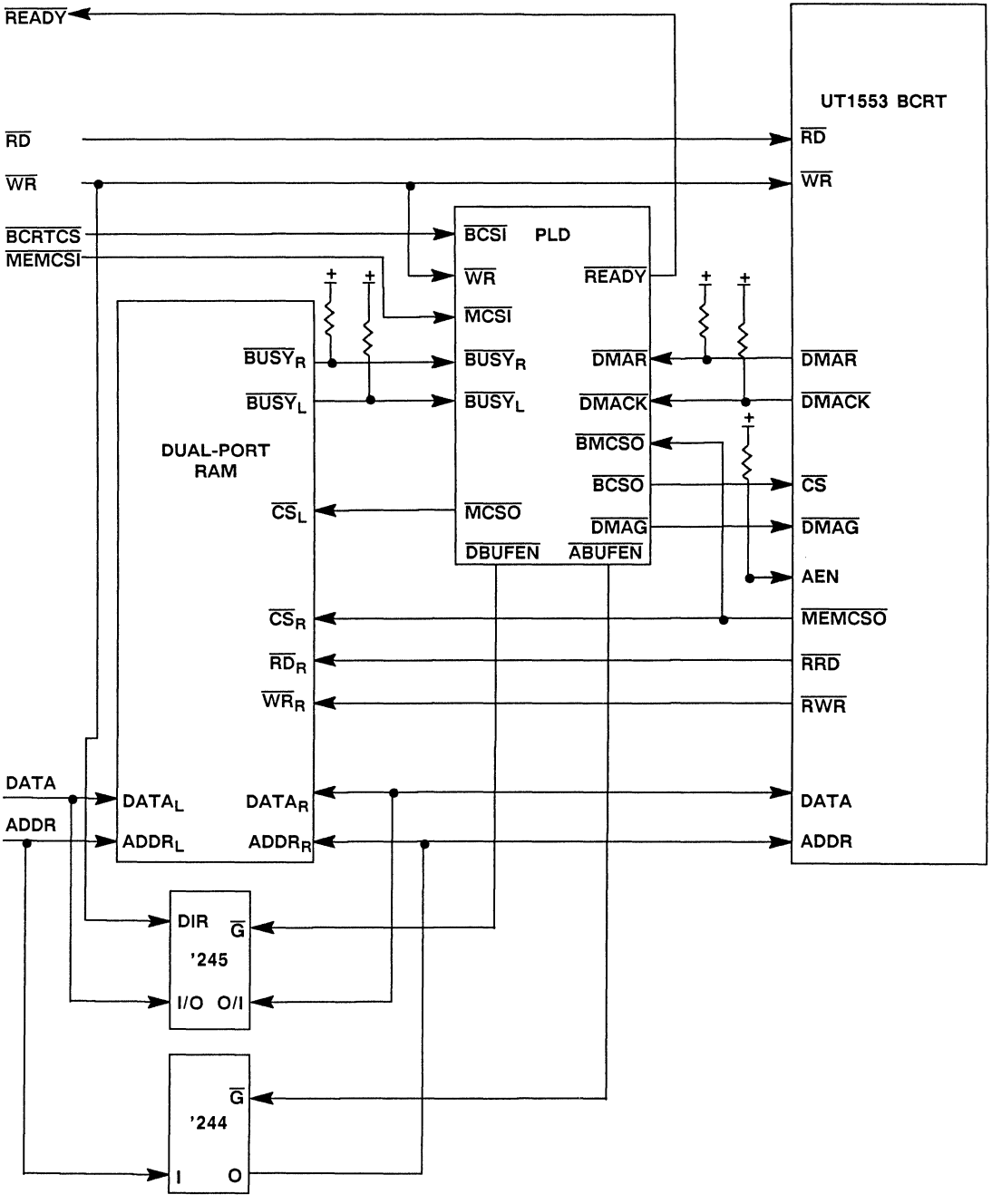
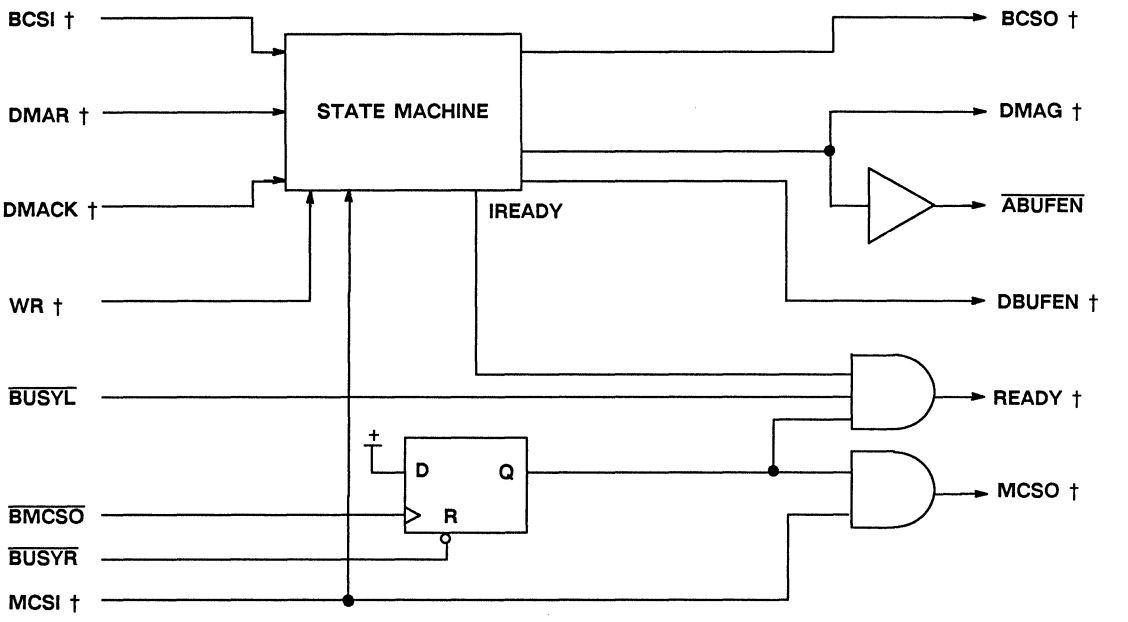


Figure 1. Basic Block Diagram



† To avoid confusion, the PLD design is implemented in positive (active high) logic. It will be necessary to add inverters to the design where negative (active low) logic signals are required.

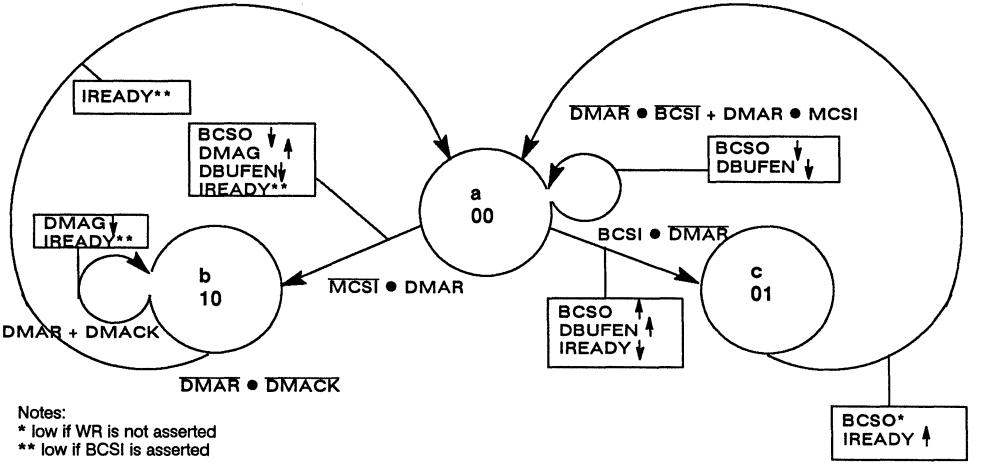


Figure 2. PLD Description

INPUT VARIABLES					CURRENT STATE			NEXT STATE		OUTPUT VARIABLES			
WR	MCSI	DMAR	BCSI	DMACK	S_0	S_1		NS_0	NS_1	BCSO	DMAG	DBUFEN	IREADY
X	X	L	L	X	0	0	a → a	0	0	L	L	L	H
X	H	H	X	X	0	0	a → a	0	0	L	L	L	H
X	L	H	L	X	0	0	a → b	1	0	L	H	L	H
X	L	H	H	X	0	0	a → b	1	0	L	H	L	L
X	X	L	H	X	0	0	a → c	0	1	H	L	H	L
X	X	H	L	X	1	0	b → b	1	0	L	L	L	H
X	X	H	H	X	1	0	b → b	1	0	L	L	L	L
X	X	X	L	H	1	0	b → b	1	0	L	L	L	H
X	X	X	H	H	1	0	b → b	1	0	L	L	L	L
X	X	L	L	L	1	0	b → a	0	0	L	L	L	H
X	X	L	H	L	1	0	b → a	0	0	L	L	L	L
H	X	X	X	X	0	1	c → a	0	0	L	L	H	H
L	X	X	X	X	0	1	c → a	0	0	H	L	H	H

PLD state machine equations:

†BCSO: = $\overline{DMAR} \bullet BCSI \bullet \overline{S0} \bullet \overline{S1} + \overline{S0} \bullet SI \bullet \overline{WR}$

†DMAG: = $\overline{MCSI} \bullet DMAR \bullet \overline{S0} \bullet \overline{S1}$

†DBUFEN: = $\overline{DMAR} \bullet BCSI \bullet \overline{S0} \bullet \overline{SI} + \overline{S0} \bullet S1$

IREADY: = $\overline{\overline{DMAR} \bullet BCSI \bullet \overline{S0} \bullet \overline{S1} + DMAR \bullet \overline{MCSI} \bullet \overline{S0} \bullet \overline{SI} \bullet BCSI + S0 \bullet \overline{S1} \bullet BCSI}$

NS0: = $DMAR \bullet S0 \bullet \overline{S1} + DMACK \bullet S0 \bullet \overline{S1} + DMAR \bullet \overline{MCSI} \bullet \overline{S0} \bullet \overline{S1}$

NS1: = $\overline{S0} \bullet \overline{S1} \bullet \overline{DMAR} \bullet BCSI$

: = registered output
x = don't care
† = outputs which will probably need inversion

Figure 2. PLD Description (Continued)

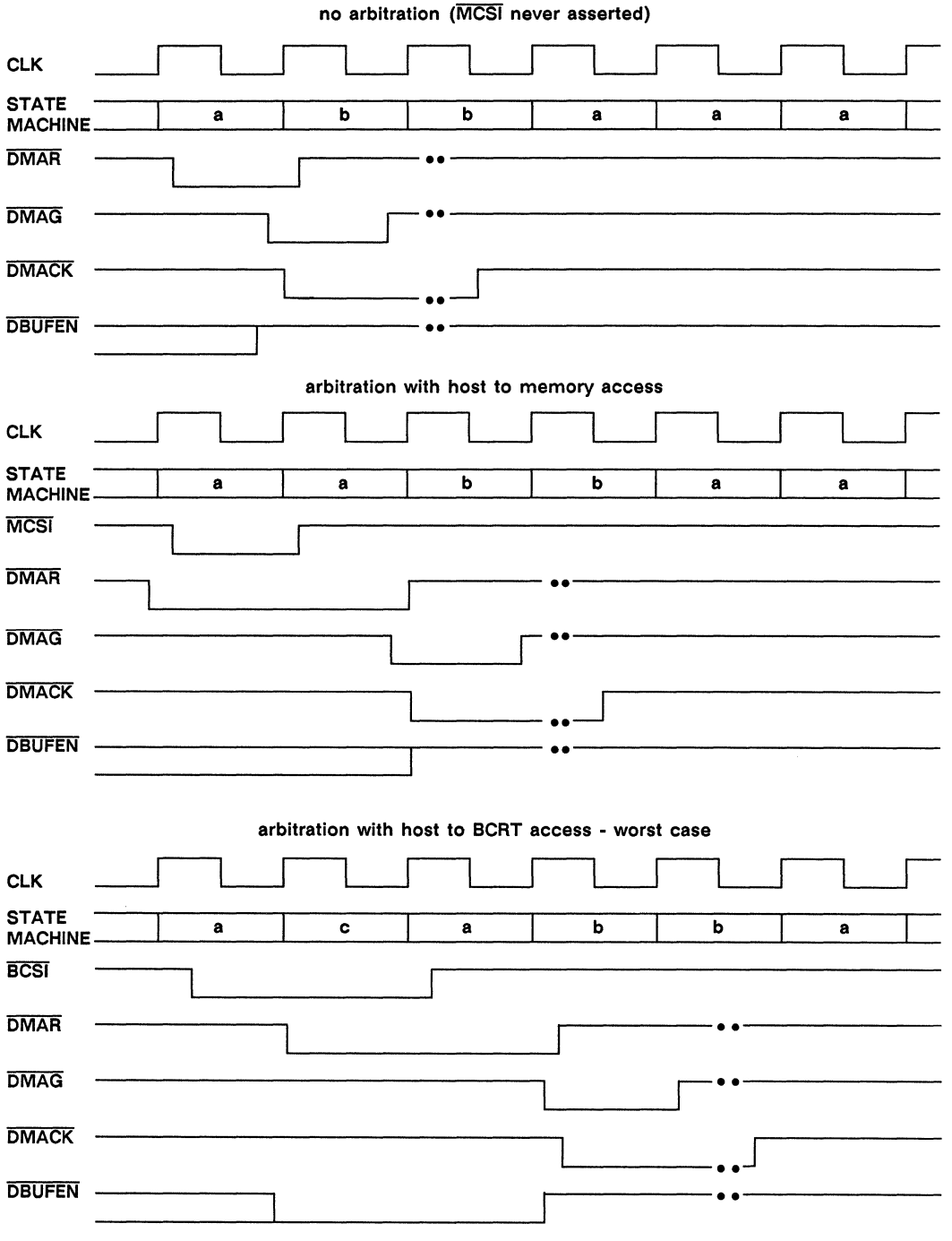


Figure 3. BCRT-Memory Access (Single Word)

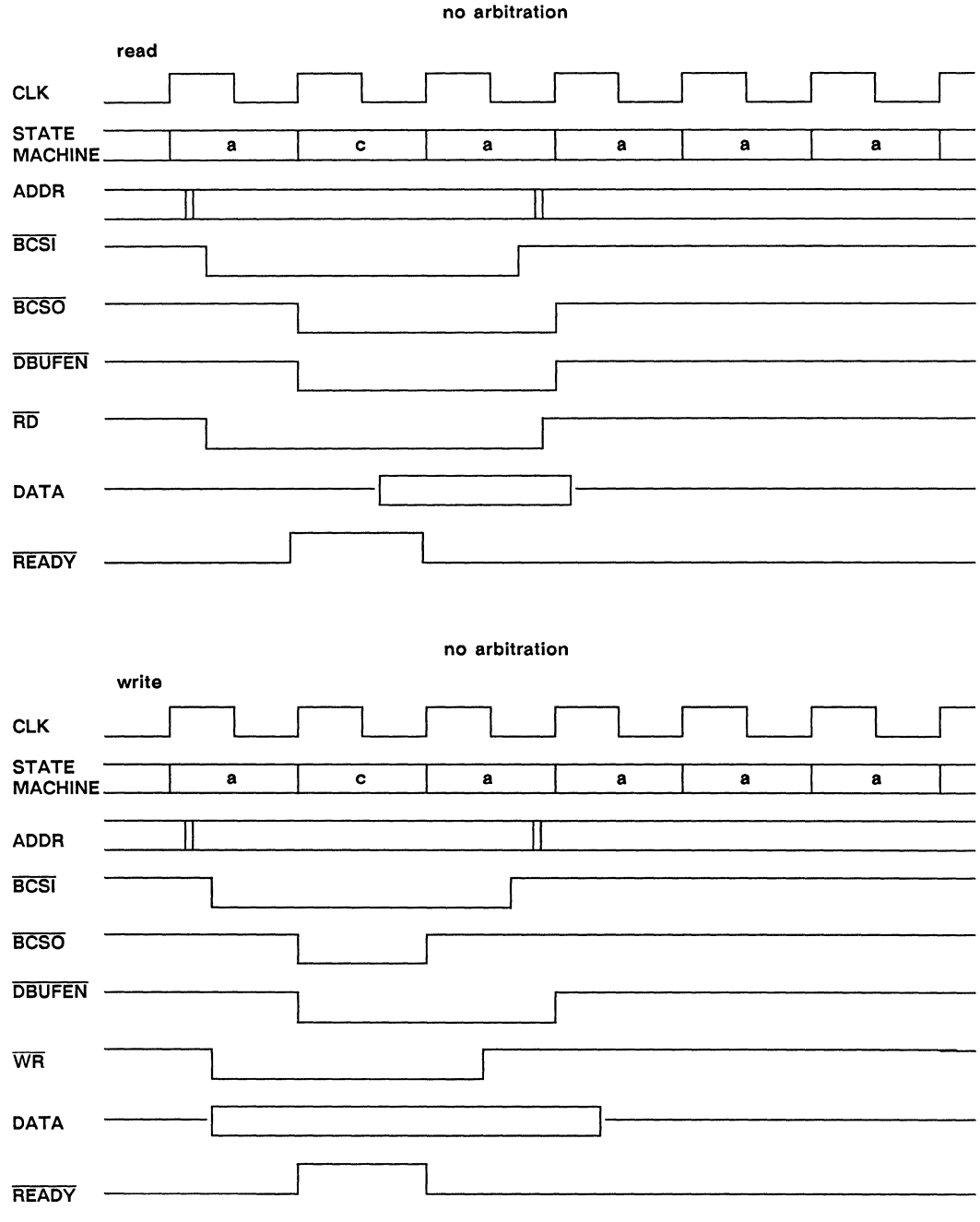


Figure 4. Host-BCRT Access

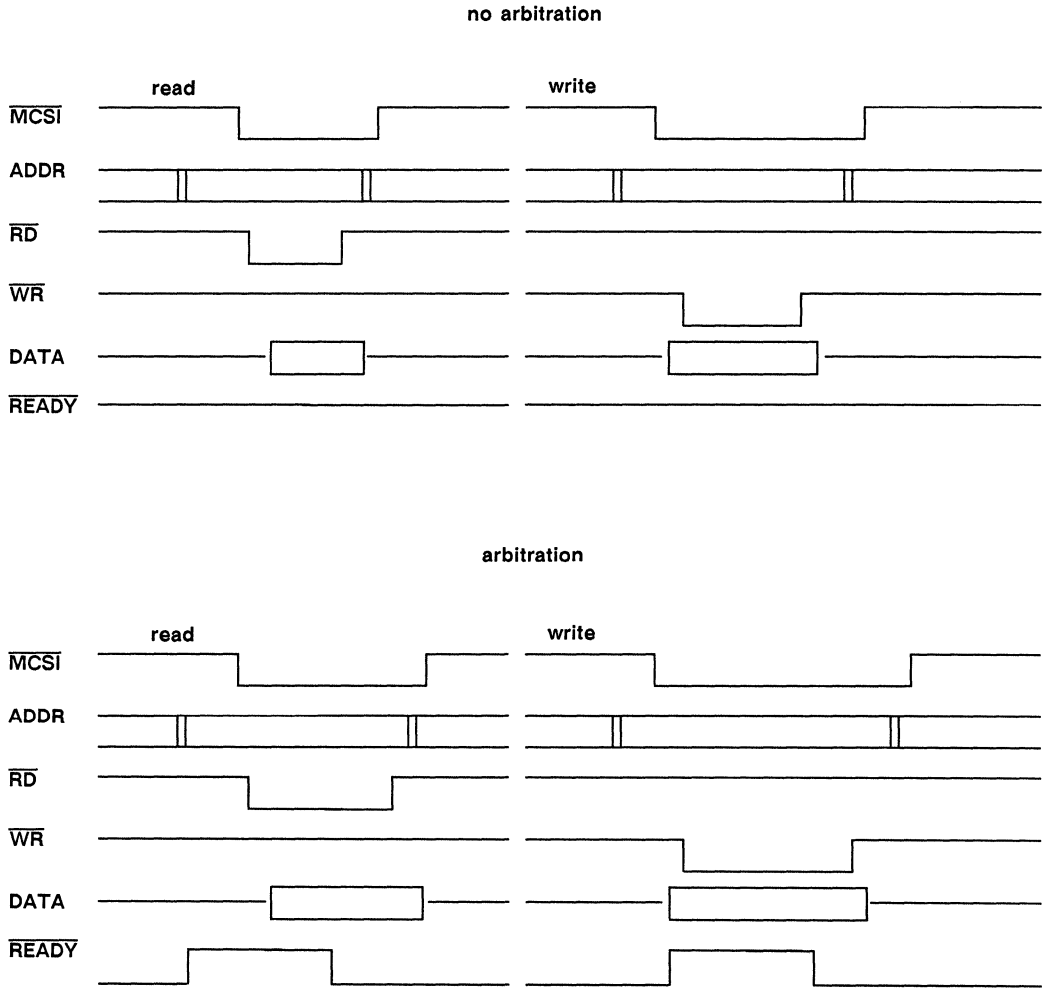


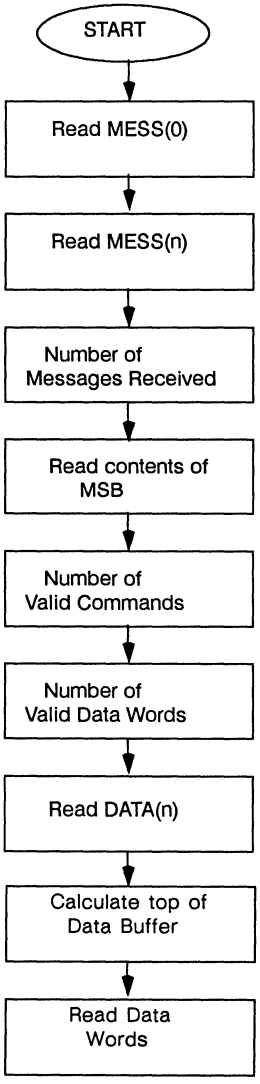
Figure 5. Host-Memory Access

BCRT/M RT-mode Multiple Message Handling Flow Chart

The following section discusses the recovery of individual data packets from a receive subaddress using message indexing. The BCRT stores a message status word for each attempted data transaction. The message status word reflects the number of data words received along with message validity and time-tag data.

To recover multiple data packets from a subaddress data buffer, the host is required to extract data from the buffer and match it with the message status word generated as a result of the message. For more information on the message status word and data buffer architecture refer to the BCRT data sheet. The data recovery routine was designed for execution after the index field of the subaddress control word has decremented to zero.

Assume the host has stored the initial condition of the message status list pointer [MESS(0)]. MESS(0) points to the top of the message buffer (MSB).



; MESS(0) - top of message status buffer;
; stored in local processor memory

; MESS(n) - bottom of message status buffer
; stored in RT Descriptor Space

; Calculate number of messages received
; N= MESS(n) - MESS(0) + 1

; Read N number of message status words
; from message status buffer (MSB)

; Test bit 13 of each message status word
; Bit 13 should equal logic zero
; count only message status words with
; bit 13 =0

; Total the number of data words received (X),
; extract word count from each message
; status word (bits 8 through 12)
; sum all word counts except last entry

; Read bottom of data buffer from RT
; Descriptor Space - DATA(n)

; Calculate top of data buffer
; DATA(0) = DATA(n) - X

; Read associated data words from the buffer
; for each message transacted
; data is removed from the buffer top to bottom

Example:

```
INDEX = 6                    ; Control Word Index field, buffer 7 messages (0 thru 6)
MESS(0) = 100 (hex)          ; stored in local memory
MESS(n) = 106 (hex)          ; read from RT Descriptor Space
N = MESS(n) - MESS(0) +1 = 7
X = 15                       ; sum of word count fields (0, 2, 3, 5)
DATA(n) = 20F (hex)          ; read from RT Descriptor Space
```

Calculate: DATA(0) = DATA(n) - X = 20F - F = 200 (hex)

DATA(0)	data word 0
	data word 1
	data word 2
	data word 3
	data word 0
	data word 0
DATA(n)	data word 0
	data word 1
	data word 2
	data word 3
	data word 4
	data word 5
	data word 6
	data word 7
	data word 8
	next data word

MESS(0)	xx00 0100 xxxx xxxx
	xx1x xxxx xxxx xxxx
	xx00 0001 xxxx xxxx
	xx00 0001 xxxx xxxx
	xx1x xxxx xxxx xxxx
	xx00 1001 xxxx xxxx
MESS(n)	xx1x xxxx xxxx xxxx

Note:
1. Subaddress setup to buffer seven messages (index = 6). Messages 2, 5, and 7 resulted in message errors. Final value of index field is zero.

Message #1, receive 4 data words, MESS(0)
Message #3, receive 1 data word, MESS(2)
Message #4, receive 1 data word, MESS(3)
Message #6, receive 9 data words, MESS(5)

The following paragraphs discuss re-synchronization of the RT after a message error occurs. Re-synchronization of the remote terminal is required when the bus controller observes a message error, and the remote terminal has invoked transmit message buffering (i.e., Control Word Index field not equal to zero). For this scenario, the remote terminal is instructed to transmit "N" data words. The remote terminal responds by transmitting a status word followed by "N" data words. The subaddress data pointer, message status pointer, and control word are updated after the last data word DMA is performed. Since the transaction results in a message error, the bus controller can attempt to re-try the same transmit command. However, the remote terminal descriptor was updated and no longer points to the data from the failed command. To re-transmit the failed data packet, set the remote terminal descriptor to transmit the failed message.

To re-synchronize the remote terminal, the host processor must modify, on command, the transmit subaddress descriptor. Utilize the Sychronize with Data mode code to instruct the remote terminal host to begin modification of the transmit subaddress descriptor for re-try. The data word associated with the mode code designates which subaddress to modify along with the word count of the failed message. Use the failed word count to calculate the re-try data list pointer. As part of the descriptor re-synchronization, the message status list pointer is decremented by one to update the failed message status word. The host increments the Control Word Index field by one to maintain the proper buffered size.

To begin the re-synchronization process, the bus controller transmits a Synchronize with Data mode code. Upon reception of this command word the remote terminal generates an interrupt signaling, to the host, receipt of the re-synchronize command. The host reads the data word associated with the mode code and determines which subaddress descriptor to service. The host proceeds to reset the data list pointer, message status list pointer, and control word. Figure 1a and 1b shows a transmit message sequence and recovery after a message error.


```
MESS(0) = 100 (hex)      ; message status list pointer initial condition
MESS(2) = 102 (hex)      ; message status list pointer after two transmit commands
DATA(0) = 200 (hex)      ; data list pointer initial condition
DATA(7) = 207 (hex)      ; data list pointer after two transmit commands
```

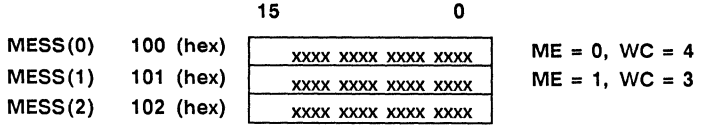


Figure 1a. Transmit Message Sequence

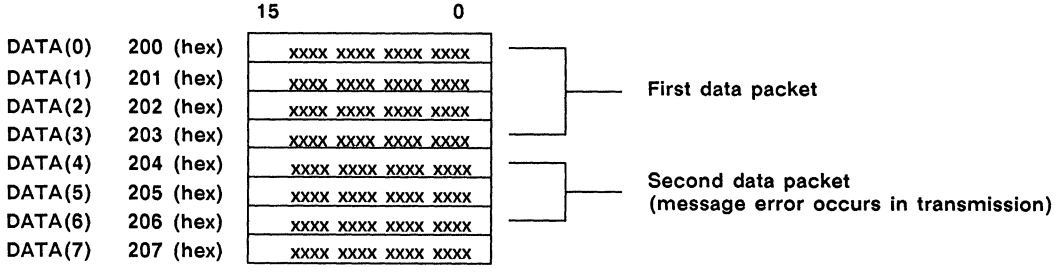


Figure 1b. Recovery Sequence

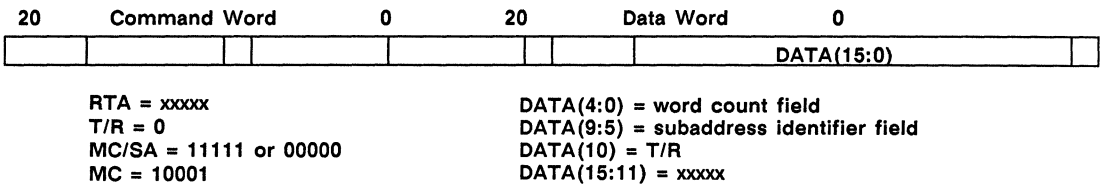


Figure 2. Synchronize with Data Example

To begin the re-synchronization process, the bus controller instructs the host to reset the data list pointer (DATA(n)), message status list pointer (MESS(n)), and control word. The host resets the data list pointer by subtracting the failed transmission word count from the present data list pointer value. Word count information along with a subaddress identifier is contained in the data word associated with the Synchronize with Data mode code. Organization of information contained in the data word is left up to the system designer. The host completes the remote terminal reset by decrementing the message status list by one and incrementing the control word index field by one. For the above example the data list pointer is decremented to 204 (hex), message status list pointer to 101 (hex), and the Control Word Index is incremented by one.

Figure 2 is an example of information organized in the Synchronize with Data mode code data

Converting from the UT1553B BCRT to the BCRTM

According to MIL-STD-1553B, there are three different terminals that may be interfaced to the protocol bus. By definition, these terminals can be a Bus Controller (BC), Remote Terminal (RT), or Monitor Terminal (MT). To support MIL-STD-1553B United Technologies Microelectronics Center (UTMC) has developed a full line of monolithic 1553 products. Two products discussed in this note are the UT1553B BCRT and UT1553B BCRTM.

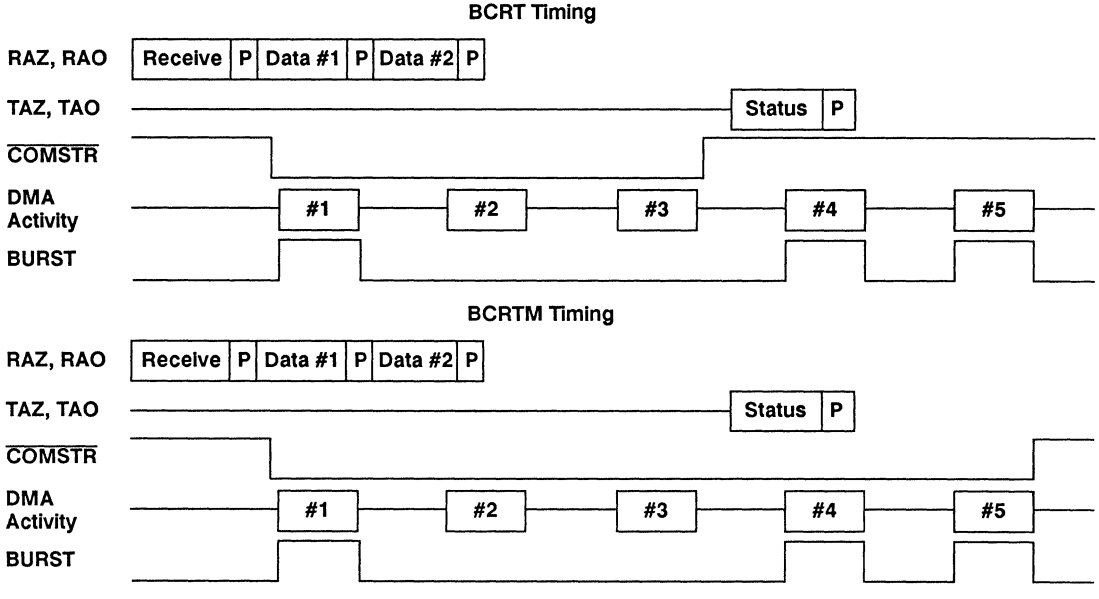
UTMC first introduced the BCRT in March 1986 as it's initial entry into the 1553 Bus Controller market. By design, the user may program the BCRT to function as either a bus controller or as a remote terminal. UTMC added the BCRTM in April 1987; it may function as either a bus controller, remote terminal, or monitor.

Recently several customers have had requirements to support all three terminal types with one design. These customer have asked UTMC how to convert their existing BCRT design to a BCRTM design so they could meet those requirements using one part. The following text describes the changes necessary to convert from a UT1553B BCRT design to a design using the UT1553B BCRTM.

Hardware Differences

The BCRT and BCRTM are pin-for-pin compatible devices. However, to completely support the monitor function, the BCRTM contains three additional accessible registers. One additional address line must be used to access these registers. Therefore, address line (A4) is a bidirectional line on the BCRTM but only an output on the BCRT. If a design uses the BCRTM but wants only BCRT functions, the designer must force low the address line A4 in order to access the lower registers (Register 0 - Register 13). The following software section describes the differences in the three additional registers.

Another hardware difference between the BCRT and BCRTM exists in the definition of the signal called Command Strobe ($\overline{\text{COMSTR}}$). The BCRT asserts COMSTR upon receipt of a valid command and deasserts it after the final 1553 transfer (before updating the interrupt log list). The BCRTM also asserts $\overline{\text{COMSTR}}$ upon the receipt of a valid command but leaves it asserted until all DMA activity is completed. Figure 1 shows the Command Strobe signal similarities and differences between the two devices.



DMA - #1-Descriptor, #2-Data Word #1, #3-Data Word #2, #4-Interrupt (opt.), #5-Descriptor Update

Figure 1. BCRT/BCRTM Command Strobe Timing Comparison

SOFTWARE DIFFERENCES

As previously discussed, the BCRTM contains three more registers than does the BCRT. Also, the BCRTM defines additional bits in register 0 that may be set. In the BCRTM, these registers and additional bits are initialized to logic 0 and the part will function as a BCRT if they are not overwritten as a logic "1". The additional bits and registers are described below: REGISTER #0 -- Control Register - Bit 14 When RT31 = 0 the BCRTM recognizes RT Address 31 as a broadcast command. When RT31 = 1 the BCRTM treats RT Address 31 as a normal terminal address. - Bit 13 When SA31 = 0 the BCRTM recognizes a command word with either subaddress 0 or 31 as being a valid mode code. When SA31 = 1 the BCRTM only recognizes a command word with a subaddress of 0 as a valid mode code. - Bit 12 When the BCRTM is a bus controller, setting bit 12 allows a remote terminal more time to respond with a status word. If BCTO = 0 the RT has up to 16 μs to respond with a status word before the BCRTM declares a bus time-out. If BCTO = 1 the RT has up to 32 μs to respond with a status word before the BCRTM declares a bus time-out.

Register #14	Bus Monitor Control Register - Bit 15 The host sets this bit to enable the BCRTM's monitor mode of operation; the host must also clear Bit 10 of Register #0 to enable the Monitor mode of operation. - Bit 14 When set, the BCRTM monitors all remote terminal bus activity. If Bit 14 is not set, then Bit 13 must be set. This bit should be cleared for RT mode operation. - Bit 13 When set, the BCRTM monitors only the remote terminals selected in Registers #16 and #17. If Bit 13 is not set, then Bit 14 must be set. This bit should be cleared for RT mode operation. - Bits 12-0 Reserved.
Register #16	Monitor Selected Remote Terminal Addresses 15-0 - Bits 15-0 By setting the appropriate bit(s) in this register, the host can determine which of the remote terminals (RT0 through RT15) the BCRTM will monitor. These bits are not mutually exclusive so the host can monitor any number of different RTs by selecting the proper combination of bits.
Register #17	Monitor Selected Remote Terminal Addresses 31-16 - Bits 15-0 By setting the appropriate bit(s) in this register, the host can determine which of the remote terminals (RT16 through RT31) the BCRTM will monitor. These bits are not mutually exclusive so the host can monitor any number of different RTs by selecting the proper combination of bits.

Simply stated, the BCRT may be replaced with the BCRTM with the above changes. The existing software will operate the BCRTM as a BCRT. To use the BCRTM monitor, the BCRT software requires the above alterations to incorporate the additional monitor registers.

Using the BCRTMP with Multiple Protocols

Introduction

The UTMC UT1553 BCRTMP is a single CMOS chip solution to a multitude of 1553 protocols. This device will implement the Remote Terminal (RT) or Bus Controller (BC) functions for 1553 protocols such as McDonnell Douglas A3818, 5232, 5690, Grumman SPG-151, MIL-STD-1553A, and MIL-STD-1553B. The user need only select the right combination of mode select options via input pins or programmable registers.

This application note discusses and compares these various 1553 protocols. These specifications can vary in several areas, including status word response time, 1553 status word bit definitions, mode codes, and error handling. By understanding these variables, it is simple to configure the BCRTMP to handle any of these protocol. The designer can implement various features to match system-specific requirements.

Several manufacturers have created their own proprietary 1553 specifications. Some of these specifications are based on the MIL-STD-1553A specification, while others are based on MIL-STD-1553B. As a result of the variety of specifications, particularly those based on 1553A, a number of incompatible 1553 implementations exist. The BCRTMP can be easily configured to handle any of these protocols using programmable mode select pins or register bits.

The Basic Differences Among The 1553 Protocols

The basic differences among the 1553 protocols fall into the following categories: status word definition, mode codes, use of broadcast, message error handling, and RT response time.

Status Word Definition

MIL-STD-1553B is quite formal in defining status bits, while the other specifications define or leave bits open to varying degrees for procurement-specific options. All of the 1553 protocols considered in this paper define the Terminal Address, ME (Message Error), and TF (Terminal Flag) status word bits in the same way. The remaining bits are defined in a variety of ways, not only dependent upon the 1553 protocol, but also on the individual procurement specification. Figure 1 illustrates status words for each protocol considered in this paper.

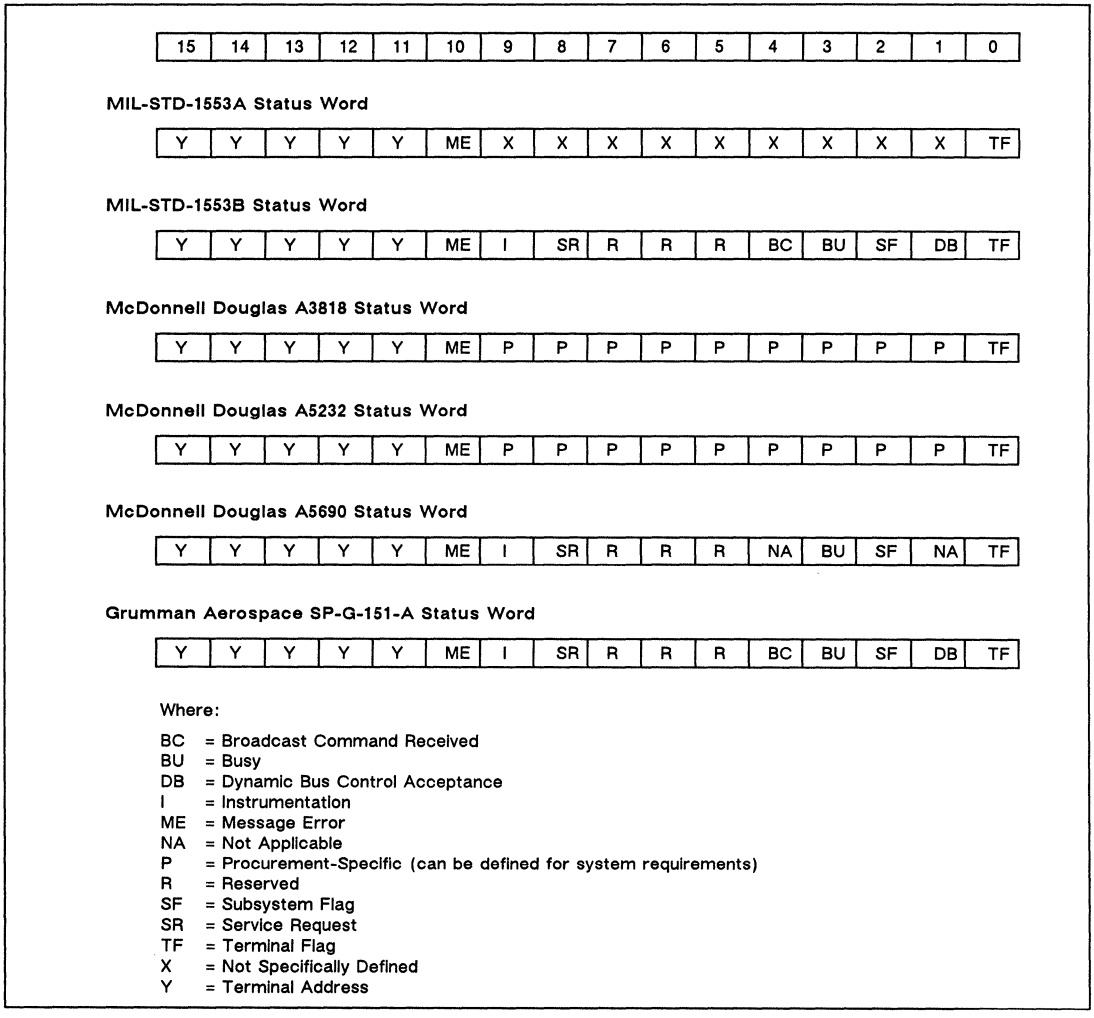


Figure 1. The Various 1553 Status Word Definitions

The BCRTMP contains a user-programmable Status Word Register (Register 15). The user can program any value desired into the status word bit field to conform to selected protocol requirements. Configuring Operational Mode 4, accessed via the input pin (MD4) or the corresponding register bit in the Operational Mode Register (Register 14, bit 4), selects the method of mode code generation.

Mode Codes

Differences in mode code definitions among the 1553 protocols center around the number of defined mode codes and whether mode codes with data are defined. MIL-STD-1553B's definition is quite formal, but the other specifications define to varying degrees the possible mode codes, and may not use mode codes with data. Table 1 illustrates the mode code possibilities for all 1553 protocols considered in this paper.

Table 1. Mode Code Assignments

MIL-STD-1553A Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	Dynamic bus control	No	No
1 or 0	00001	Undefined	No	No
.	.	.	.	.
1 or 0	11111	Undefined	No	No

MIL-STD-1553B Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
.	.	.	.	.
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
.	.	.	.	.
1 or 0	11111	Reserved	Yes	TBD

McDonnell Douglas A3818 Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	Dynamic bus control	No	No
1 or 0	00001	Procurement-Definable	No	No
.	.	.	.	.
1 or 0	11111	Procurement-Definable	No	No

McDonnell Douglas A5232 Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	Dynamic bus control	No	No
1 or 0	00001	Procurement-Definable	No	No
.	.	.	.	.
1 or 0	11111	Procurement-Definable	No	No

McDonnell Douglas A5690 Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	N/A	No	No
1	00001	Synchronize	No	No
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	No
1	00100	Transmitter shutdown	No	No
1	00101	Override transmitter shutdown	No	No
1	00110	N/A	No	No
1	00111	N/A	No	No
1	01000	Reset remote terminal	No	No
1	01001	Reserved	No	No
.	.	.	.	.
1	01111	Reserved	No	No
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	No
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	N/A	Yes	No
0	10101	N/A	Yes	No
1 or 0	10110	Reserved	Yes	No
.	.	.	.	.
1 or 0	11111	Reserved	Yes	No

Grumman SP-G-151A Assigned Mode Codes

Trans-Rcv Bit	Mode Code	Function	Assoc Data Word	Broadcast Command Allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
.	.	.	.	.
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
.	.	.	.	.
1 or 0	11111	Reserved	Yes	TBD

The BCRTMP allows flexible mode code implementation. This flexibility includes the selection of only mode codes with data or only mode codes without data. The user can also select automatic execution of modes codes, as defined in MIL-STD-1553B, or configure the BCRTMP to respond with status and allow the host to execute a mode code. Finally, the user can configure the BCRTMP to determine the reception of a mode code command with either all ones AND all zeros in the subaddress field, or all zeros only. This flexibility allows the device to be configured for mode code operation for any of the 1553 protocols discussed. The source selection for the status word is accomplished via the Operational Mode 3, accessed either through the input pin (MD3) or bit 3 of the Operational Mode Register (Register 14). The selection of mode codes with data versus without data is accomplished with Operational Mode 6. This is accessed via the input pin (MD6) or the corresponding register bit in the Operational Mode Register (Register 14, bit 6).

Use Of Broadcast

The 1553 protocol differences include the broadcast option. For protocols that support the broadcast option, the RT address 11111 is reserved to indicate a broadcast command. When a broadcast command is transmitted, all RTs must receive the message. No RT is to respond with a status word.

Protocols that do support the broadcast option treat RT address 11111 as a normal RT address.

The BCRTMP allows the use or disabling of broadcast commands. When broadcast is disabled, then RT address 11111 is treated as a normal RT address via the Operational Mode 1, accessed either through the input pin (MD1) or bit 1 of the Operational Mode Register (Register 14).

Message Error Handling

Some 1553 protocols (MIL-STD-1553B, McDonnell Douglas A5690, and Grumman SP-G-151A) consider any message error reason to discard the entire message and suppress the status word, while others (MIL-STD-1553A, and McDonnell Douglas A3818 and A5232) react according to message error severity. In the latter three protocols, if a Manchester error or parity error occurs in a data word, the defective data word is discarded but the remainder of the message can be used. The RT then responds with the status word with the Message Error bit set.

Status Word Suppression For Erroneous Transactions (MIL-STD-1553B, McDonnell Douglas A5690, Grumman SP-G-151A)

The criteria for suppressing a status word for message error condition for an RT that conforms to these protocols is defined as follows:

- Any data word that contains a parity error.
- Any data word that contains a Manchester error.
- Any data word that contains an invalid sync.
- The remote terminal received an incorrect number of data words.

If any of the above conditions occur, the RT suppresses status and sets the Message Error bit.

Note: If the command word is in error, or is going to another RT address, then the RT does not consider the message.

Status Word Suppression For Erroneous Transactions (MIL-STD-1553A, McDonnell Douglas A3818 and A5232)
The criteria for suppressing a status word for an RT message error condition that conforms to these protocols is defined as follows:

- Any data word that contains an invalid sync.
- The remote terminal received an incorrect number of data words.

If any of the above conditions occur, the RT suppresses status and sets the Message Error bit.

Note: If the command word is in error or is going to another RT address, the RT does not consider the message.

If the above-listed conditions did not occur for a message, but one of the following conditions occurs, the RT sends status with the Message Error bit set.

- Any data word that contains a parity error.
- Any data word that contains a Manchester error.

The user can configure the BCRTMP to handle errors in accordance with either of the methods discussed above via the Operational Mode 5, accessed either through the input pin (MD5) or bit 5 of the Operational Mode Register (Register 14). Note: The BCRTMP validates each data word on sync and two bits.

RT Response Time
The RT response time differs among the 1553 protocols. RT response time measurement is from the parity bit's zero crossing of the receive command's last data word, or the command word's zero crossing for a transmit command to the status word sync's zero crossing.

The maximum response time allowed for an RT in a MIL-STD-1553A or McDonnell Douglas A3818 or A5232 system is 7.0 microseconds; for an RT in a MIL-STD-1553B, McDonnell Douglas A5690, or Grumman SP-G-151G system it is 12.0 μs.

The BCRTMP can be configured for a response time in accordance with the above requirements via Operational Mode 2. It is accessed via the input pin (MD2), or the corresponding register bit in the Operational Mode Register (Register 14, bit 2).

Protocol Comparisons

1553 Protocol Features

1553 Protocol	Message Error Method	Broadcast Allowed	Status Bits	Maximum Response Time
1553A	A3818	No	Definable	7 μs
1553B	1553B	Yes	Defined	12 μs
MDC A3818	A3818	No	Definable	7 μs
MDC A5232	A3818	No	Definable	7 μs
MDC A5690	1553B	Yes	Definable	12 μs
Grumman SPG151A	1553B	No	Definable	12 μs

Where:

1553A Response Time = 4.0 to 12.0 μs, as measured from parity zero cross to sync zero cross.
1553B Response Time = 4.0 to 12.0 μs, as measured from parity zero cross to sync zero cross.

BCRTMP Response Time is 5.5 μs (using Legalization bus).
BCRTMP Response Time is 10 μs (using DMA).

A3818 Message Error Handling Method: The status word is transmitted with Message Error bit set if a data word parity or Manchester error occurs.

1553B Message Error Handling Method: The status word is suppressed and the Message Error bit is set if any message error occurs.

Design Considerations For Implementing 1553 Protocols

Substantial differences among 1553 protocols create challenging obstacles for creating a BCRT that conforms to all 1553 protocols. Design considerations fall into the following categories: status word definition, mode codes, use of broadcast, message error handling, and RT response time.

Designing For Status Word Flexibility

The status word must be flexible in order to conform to a variety of 1553 protocols. The BCRTMP can operate in a mode where the status word is defined in strict correspondence with the MIL-STD-1553B specification or it can operate in a more flexible mode. In the flexible status word mode, the user can program the individual status word bits via read/write registers.

Designing For All Mode Code Possibilities

Two of the BCRTMP's mode options address the need for mode code flexibility. The designer can place the BCRTMP in an operational mode so the device performs in strict correspondence with the mode code definitions for MIL-STD-1553B. Illegalization of any unsupported mode code can occur in one of two ways: (1) The designer can illegalize the mode code via the Legalization bus (figure 2), or (2) the device can perform illegalization via DMA Descriptor Block fetches (figure 3).

The BCRTMP can also accommodate a flexible mode code definition by employing two operational mode options. One option allows the device to employ mode codes with or without data. If it employs mode codes with data, it allows only single data word transfers using the data word rules established in MIL-STD-1553B. Alternatively, an operational mode completely disallows mode codes with data.

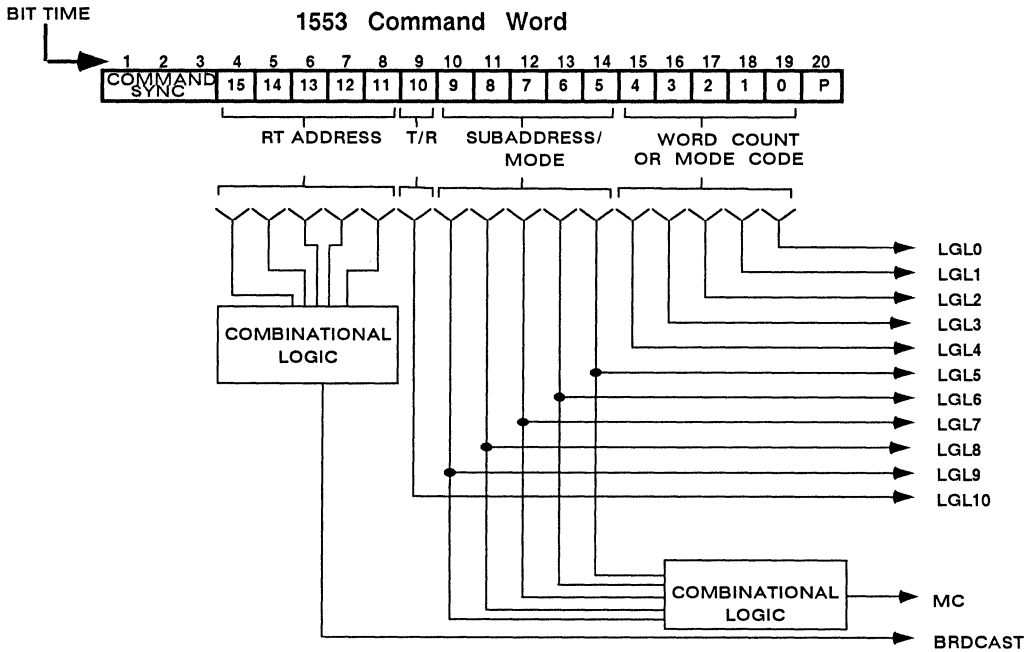


Figure 2. BCRTMP Legalization Bus

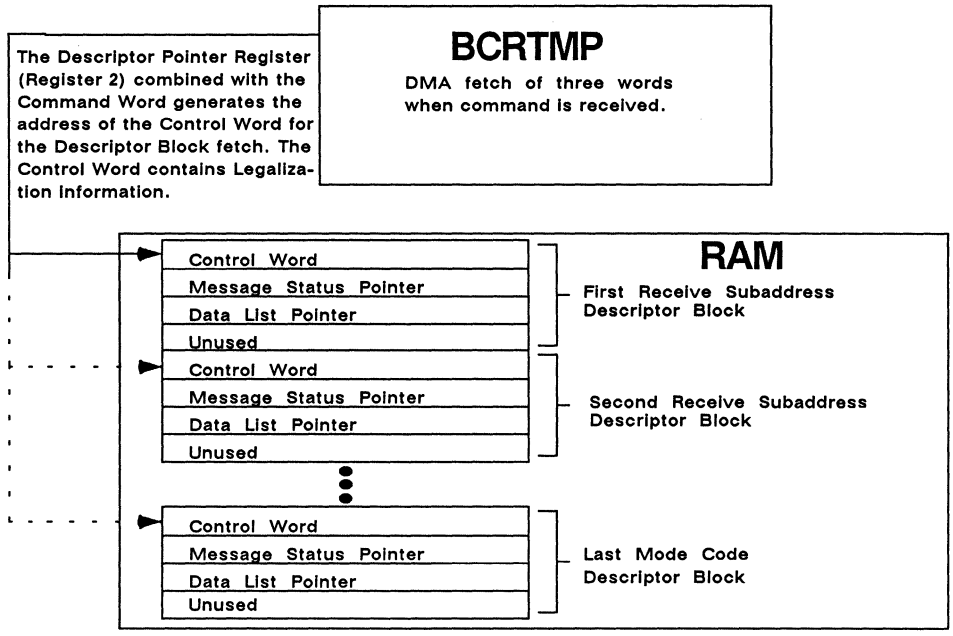


Figure 3. BCRTMP Descriptor Block Legalization

Designing For Broadcast

The broadcast option may or may not be included in a particular 1553 protocol. The BCRTMP has a programmable mode option that allows the user to determine whether to allow broadcast commands in a system. If broadcast commands are allowed, then any command to RT address 11111 is considered a broadcast command. If broadcast commands are not allowed, then a command to RT address 11111 is considered a normal command.

Designing For Both Message Error Handling Techniques

The two message error handling techniques in 1553 protocols require a flexible design. The message error handling technique described above, the A3818 method, is a particularly difficult design to use. The remote terminal must be able to distinguish the severity of message errors. A less severe error, either a Manchester error or a parity error in a data word, requires special attention. The RT must mark the individual defective data word and respond with the Message Error bit set in the status word.

The BCRTMP accomplishes this challenging task. When a Manchester or parity error occurs in a data word, the BCRTMP asserts the ERRB signal and places the word count for the defective data word in bits 0-4 of the Legalization bus. In a typical system, the ERRB signal can control a TTL FIFO (first-in/first-out) device, and can strobe the word count into the device. The system can examine the FIFO at the end of the message to determine if the message contains defective data. If the message has defective data, the data can be identified by reading the FIFO (figure 4).

The alternative and much simpler message error handling technique treats all message errors the same way. If a message error occurs in this operational mode, the system discards the entire message. The RT sets the Message Error bit in the status bit, but suppresses transmitting the status word.

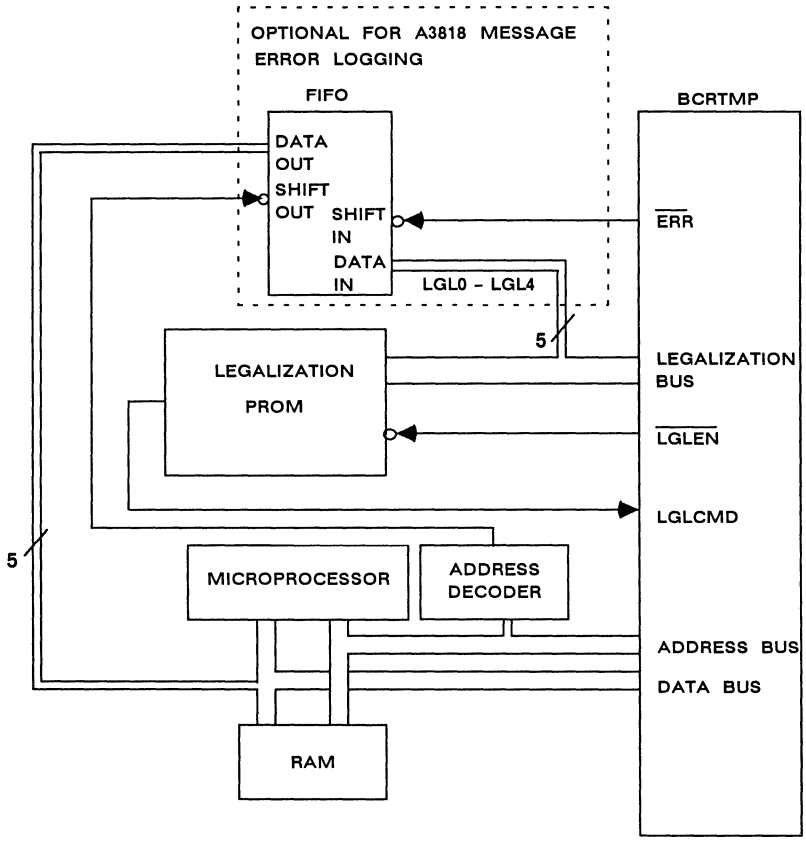


Figure 4. BCRTMP Bus Legalization Example

Designing For Flexible RT Response Time

The two 1553 response times require a flexible design. The minimums are either 7 μs or 12 μs. The BCRTMP can accommodate either response time by selecting the appropriate mode options. Either response time can be accommodated while using the Legalization bus for command illegalization. The faster response time requires use of the Legalization bus. The slower response time can be met using the DMA Descriptor Block fetch method.

Figure 5 illustrates the system timing for the Legalization bus and figure 6 shows RT response time for both modes of operation.

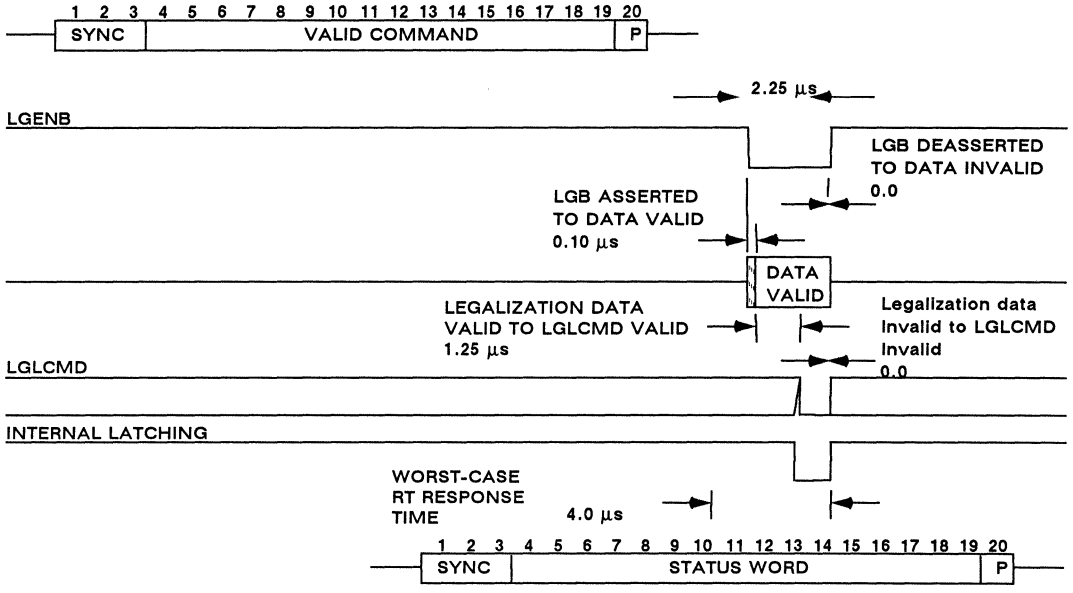


Figure 5. Illegalization Bus Timing

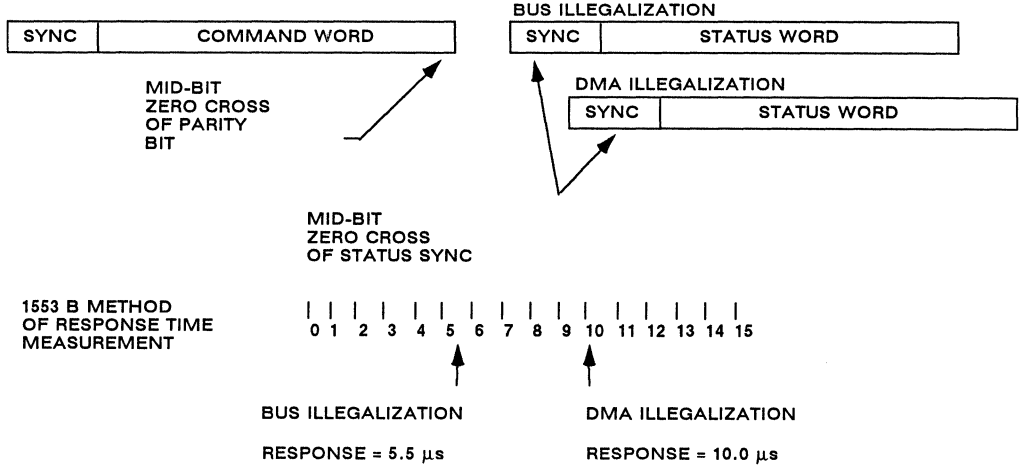


Figure 6. BCRTMP Worst-Case Response Time

Programmable Mode Options

Six programmable mode options provide flexibility and address the characteristics that vary among the 1553 protocols. The designer can configure the BCRTMP to operate in a wide variety of modes by using the device's mode select pins. Each mode select is accessible via an internal register as well.

MODE0 Illegalization Select

MODE0 illegalization select chooses either DMA or bus illegalization. A high on this signal selects DMA illegalization, while a low on this signal selects bus illegalization. When the BCRTMP operates as an RT with the 1553A response time, MODEO bit must be low because it is impossible to meet the 1553A response time and use DMA illegalization.

Bus illegalization is a method by which the 1553 command word, minus the RT address, is routed to the Legalization bus. The BCRTMP uses this information, for example, as a PROM address. The single-bit output from the PROM then feeds to the LEGAL input signal of the BCRTMP. If a command is considered legal, the PROM output is high; if a command is considered illegal, the PROM output is low.

DMA illegalization allows the BCRTMP to access a specific Descriptor Block when it receives a given command. The Descriptor Block contains information the BCRTMP uses to determine if the command is considered legal or illegal.

In both illegalization methods, if the command is illegal, the BCRTMP sends a status word with the Message Error bit set (bit 10); it does not transmit data when it receives an illegal message. When the illegal command is a broadcast command, and broadcast is enabled, the BCRT suppresses the status word.

MODE1 Broadcast Enable
The MODE1 broadcast enable signal determines whether the selected protocol contains broadcast commands. When this signal is high, the selected 1553 protocol contains the broadcast option. When the RT address is 11111 (binary), the command is considered a broadcast command.

When this signal is low, the selected 1553 protocol selected does not contain the broadcast option. When the RT address is 11111 (binary), the command goes to a normal unique RT address.

MODE2 Response Time Select
The MODE2 response time select signal determines the response time for the status word. When this signal is high, the response time is nominally 10 μs as measured from the parity bit's zero crossing to the status word sync zero crossing.

When this signal is low, the response time is nominally 5.0 μs as measured from the parity bit's zero crossing to the status word sync zero crossing. When the 5.0 μs response time is selected, the BCRTMP performs illegalization via the bus.

MODE3 Protocol Selection
MODE3 protocol selection selects between two sets of protocol options. When this signal is high, the device uses the 1553B protocol options. When this signal is low, the device uses the 1553A protocol options. The functions these protocol options affect include mode code execution and status word bit definition.

When in the 1553B mode, all ones or all zeros in the subaddress field determine a mode code command. When in the 1553B mode, the mode codes are rigidly defined according to MIL-STD-1553B.

When in the 1553A mode, all ones in the subaddress field indicate a mode code command.

When in the 1553A mode, the mode codes are more flexible since the MIL-STD-1553A and derivative specifications can treat the mode code definitions flexibly. Likewise, the status word is programmable to accommodate the loose definition in the MIL-STD-1553A specification.

MODE4 Message Error Handling Method
The MODE4 message error handling method select signal selects between two message error handling methods. When this signal is high, the BCRTMP handles message errors as defined in MIL-STD-1553B. When this signal is low, the BCRTMP handles message errors as defined in McDonnell Douglas A3818. The differences in standards deal with Manchester and parity errors when they occur in a data word. With MIL-STD-1553B, when a Manchester or parity error occurs in any data word for a given message, the correct RT response is to suppress the status word and set the Message Error bit.

With A3818, when a Manchester or parity error occurs in a data word, the RT does not use the erroneous data, but the status word must be sent with the Message Error bit set. To provide the means for the RT system to discard only the erroneous data word, the BCRTMP strobes the ERRB signal and places the word count for the erroneous word on the least significant five bits of the Legalization bus. If only Manchester or parity errors occur in data words, the BCRTMP transmits the status word with the Message Error bit set.

MODE5 Mode Code With Data Select
The MODE5 mode code with data select signal selects between two 1553A protocol mode code options. When this signal is internally pulled high, mode codes with data are not allowed. As such, no mode code has an associated data word.

When this signal is pulled low, mode codes with data are allowed; the data rules follow MIL-STD-1553B. mode codes 00000 - 01111 do not have data. mode codes 10000 - 11111 do have an associated data word. The data is sent from the RT if the Transmit/Receive bit is 1. The data is sent to the RT if the Transmit/Receive bit is 0.

In the 1553A mode (i.e., MD3 is low), the BCRTMP handles the data word as a single data word transmit or receive command.

In the 1553B mode (i.e., MD3 is high), mode codes correspond strictly with MIL-STD-1553B.

Summary

The BCRTMP was designed with thorough consideration of all characteristics that might vary among a group of commonly used 1553 protocols. Carefully characterization of all variable criteria led to creation of a set of programmable mode options that address all 1553 protocols.

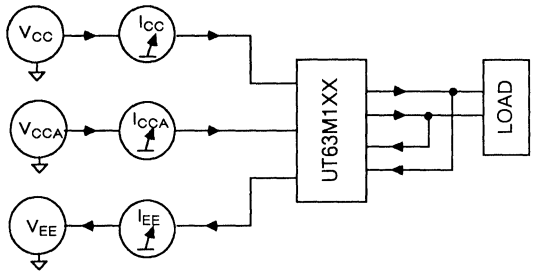
UT63M1XX: Power Consumption vs. Dissipation

INTRODUCTION

The monolithic UT63M1XX Series Bus Transceivers are complete transmitter and receiver pairs conforming fully to MIL-STD-1553A and B. Transceivers provide the electrical bus interface for subsystems to the MIL-STD-1553 bus. MIL-STD-1553 specifies the data bus signal's wave shape, amplitude, frequency, and power.

This application note will discuss the power consumption and dissipation of the bus transceiver as it transmits signals on the MIL-STD-1553 data bus. Specifically it will differentiate between power consumed by the bus interface (i.e., system power) versus power dissipated within the transceiver. For system designers addressing system power consumption and the sizing of power supplies, the power consumption of the bus interface (transceiver plus load) is important. Transceiver power dissipation is important for evaluating the reliability and thermal characteristics of the transceiver. This document will present examples of calculating the power dissipation and consumption for a direct-coupled transceiver transmitting onto the MIL-STD-1553 data bus.

System Power Consumption
System power consumption is defined as the power consumed by the device plus load. UTMC's UT63M1XX Bus Transceiver data sheet specifies the maximum current per voltage supply including load. To obtain the system power consumption the voltage is multiplied by the AC current. Figure 1 shows an example of the power the transceiver consumes while driving the bus.



$P_{SYS} = V_{EE}\ I_{EE} + V_{CC}\ I_{CC} + V_{CCA}\ I_{CCA}$

Figure 1. System Power Consumption

For sizing power supplies and characterizing system current requirements, no differentiation between power consumption and dissipation is necessary.

Transceiver Power Dissipation
Transceiver power dissipation defines the power dissipated in the device while the transceiver drives the bus load. Power supplies V_{CC} and V_{CCA} dissipate essentially all of their supplied power within the transceiver device. A small amount of the V_{CC} power is dissipated at the receiver output load but is negligible compared to the transmitter output. Therefore the power dissipated by these supplies (V_{CC}, V_{CCA}) is equal to the power consumed by these supplies.

$P_D(V_{CC}) = I_{CC} \times V_{CC} = 60\ mA \times 5\ V = 300\ mW$
$P_D(V_{CCA}) = I_{CCA} \times V_{CCA} = 10\ mA \times 15\ V = 150\ mW$
$*P_D(V_{CCA}) = I_{CCA} \times V_{CCA} = 10\ mA \times 5\ V = 50\ mW$

*Note : +5 and -15 volt operation (i.e., $V_{CCA} = V_{CC}$)

The power supplied by the negative source (V_{EE}) is consumed by both the load and the transceiver output stage. To calculate the power dissipated within the transceiver, perform a best- and worst-case analysis. MIL-STD-1553 specifies the output voltage level (V_O) and load impedance (Z_O) for the direct-coupled transceiver (+/-15 volt version) shown in figure 2.

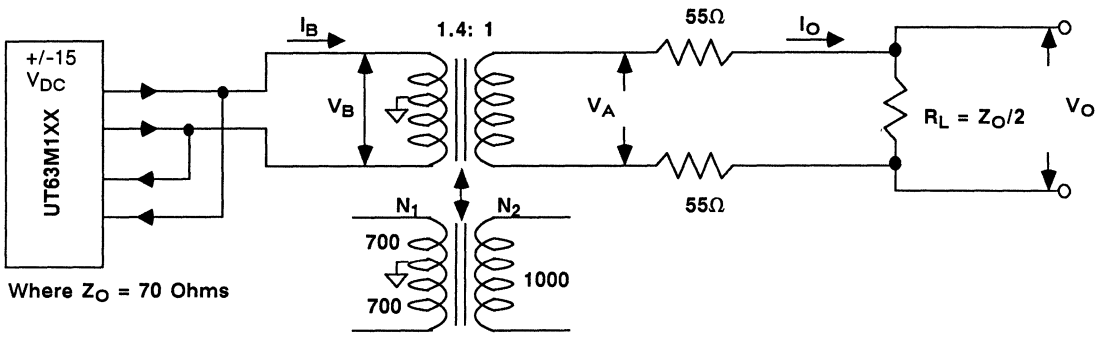


Figure 2. Transceiver Power Dissipation

The following calculations are performed on the circuit using these MIL-STD-1553B specification limits:

V_O	6 V_{P-P} (min)	9 V_{P-P} (max)
Z_O	70 ohms	70 ohms

For an ideal transformer the following equations are written for voltage and current:

$V_B = (N1/N2)V_A/2$ where N1/N2 = .70

$I_B = (N2/N1)I_O/2$ where N2/N1 = 1.43

Using the above limits the voltage and current supplied by the transceiver are calculated for a single-ended 1 megahertz cycle.

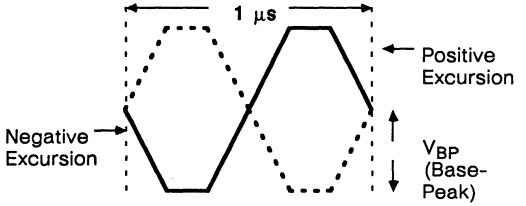


Figure 3. Single-Ended Waveform (V_B= 4 V_{BP})

Negative Excursion:

V_O = 6 V_{P-P}, L-L ($_{P-P}$, Peak-Peak)	V_O = 9 V_{P-P}, L-L ($_{P-P}$, Peak-Peak)
Z_O = 70 ohms	Z_O = 70 ohms
I_O = 171 mA/2 = 85 mA	I_O = 257 mA/2 = 128 mA
$V_A = 4 \times V_O$ = 24 V_{P-P}, L-L	$V_A = 4 \times V_O$ = 36 V_{P-P}, L-L
$V_{BP} = (N_1/N_2)V_A/2$ = 8.4	$V_{BP} = (N_1/N_2)V_A/2$ = 12.6
$I_B = I_O \times 1.43$ = 122 mA	$I_B = I_O \times 1.43$ = 184 mA
$\Delta V_{BP} = \{V_{EE} - V_{BP}\}$ = {6.6 V}	$\Delta V_{BP} = \{V_{EE} - V_{BP}\}$ = {2.4 V}
$P_D = \Delta V_{BP} \times I_B$ = 805 mW	$P_D = \Delta V_{BP} \times I_B$ = 441 mW

Where: V_{BP} = the voltage V_B measured base to peak
ΔV_{BP} = the voltage imposed across the transceiver
P_D = power dissipated in the transceiver due to the loading of the output (negative excursion)

Positive Excursion:

V_{BP} = 8.4 V	V_{BP} = 12.6 V
R_{IL} = 14K ohms (internal resistor)	R_{IL} = 14K ohms (internal resistor)
I_L = 600 µA	I_L = 900 µA
P_R = 5 mW	P_R = 11.3 mW

Where: P_R = power dissipated in the transceiver (positive excursion)

Single-Ended Power Dissipation:

$P_T = P_D + 2P_R$
$P_T = 805\ mW + 10\ mW = 815\ mW$

$P_T = P_D + 2P_R$
$P_T = 441\ mW + 22.6\ mW = 463.6\ mW$

Blocking Diode:

$P_D (V_D) = V_D \times I_O = .9 \times 122\ mA = 109\ mW$

The minus supply (V_{EE}) also supplies power that is dissipated within bias circuitry and is not included with the output power dissipation. That power is defined as:

$P_D(bias) = 40\ mA \times 15\ V = 600\ mW$

Therefore:

$P_D(V_{EE}) = P_D(total) + P_D(bias)$

The total power dissipated in transceiver (worst case) for a complete cycle is as follows:

$$P_{CD} = P_D(V_{EE}) + P_D(V_{CC}) + P_D(V_{CCA}) + P_D(V_D)$$
$$= (.815\ W + .60\ W) + .30\ W + .15\ W + .109\ W$$
$$= 1.974\ W$$

$$*P_{CD} = P_D(V_{EE}) + P_D(V_{CC}) + P_D(V_{CCA}) + P_D(V_D)$$
$$= (.815\ W + .60\ W) + .30\ W + .05\ W + .109\ W$$
$$= 1.874\ W$$

*Note : +5 and -15 volt operation (i.e., $V_{CCA} = V_{CC}$)

Duty Cycle

Figure 4 shows transceiver power dissipation during various duty cycles. While receiving information from the bus the power dissipation is low (i.e., idle state); the receiver section of the device is active and the transmitter is inactive. When transmitting information onto the data bus the transceiver power dissipation increase is proportional to the transmission time. Table 1 shows a breakdown of duty cycle vs. message length.

Message	Word Count	Idle	Transmitting
Receive	32	97%	3%
Receive	1	97%	3%
Transmit	32	3%	97%
Transmit	1	94%	6%

* The above calculations are based on time period $t = 680\ \mu s$

Conclusion

Calculation of the worst-case power dissipation for the transceiver while it transmits information onto the MIL-STD-1553 data bus is straightforward. Use the same analysis method to determine power dissipation for a transformer-coupled stub and for the various voltage versions of the UT63M1XX Transceiver.

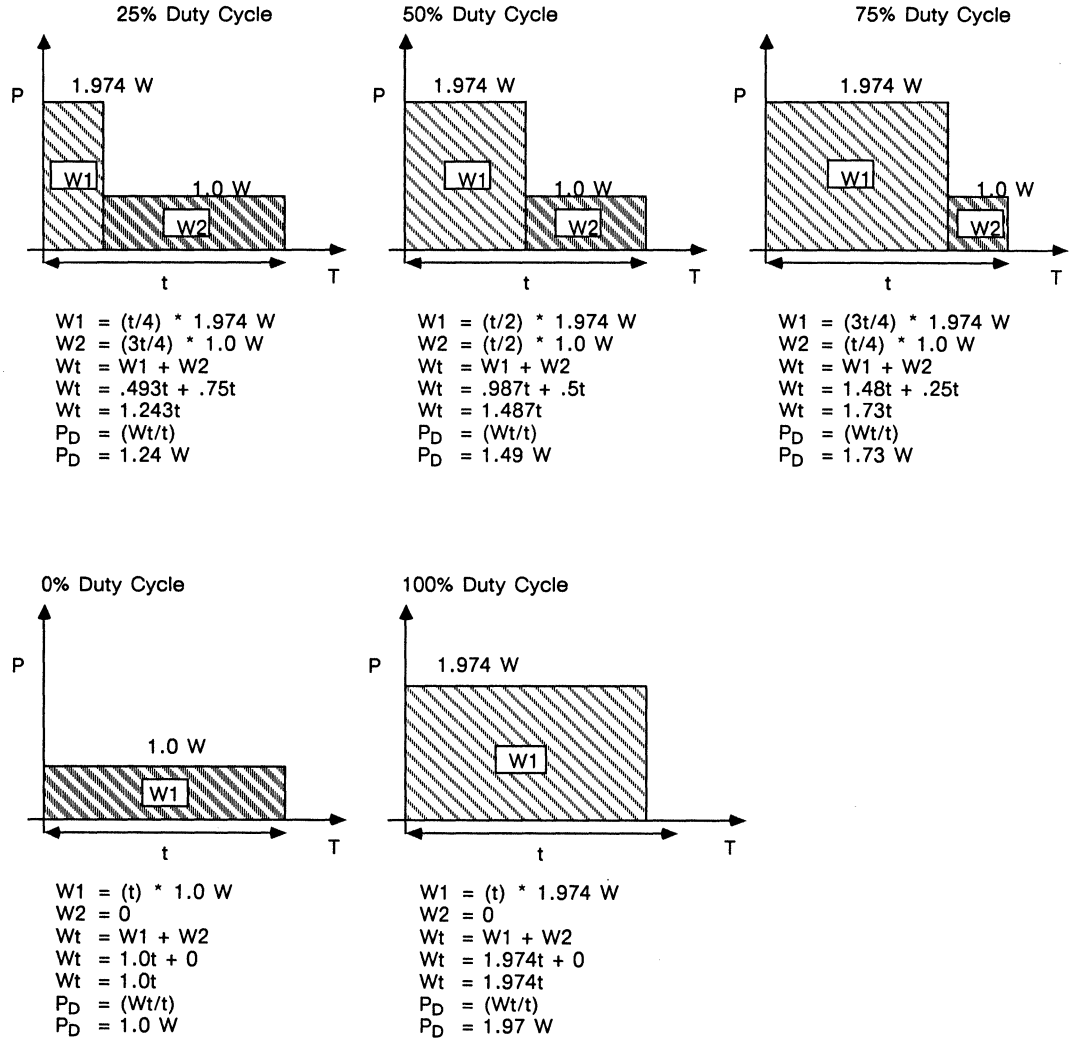


Figure 4. Duty Cycle Calculation

UT63M1XX Series Transceiver: Thermal Considerations

INTRODUCTION

To operate UT63M1XX Series Transceivers over the upper end of the data sheet temperature range, thermal protection is recommended. The following discussion will define an electrical analog model used to analyze thermal systems consisting of a packaged integrated circuit, thermally conductive mounting material, and heat sink.

Thermal Resistance

The heat generated within a packaged integrated circuit will conduct away from its sources (transistor junctions and resistors) to the case. Heat conduction results in a temperature gradient between the case and junction proportional to the power dissipated by the device. The proportionality factor is a term that represents the resistance to heat transfer and is defined as thermal resistance, Θ_{JC}.

Eq. 1 $\Theta_{JC} = (T_J - T_C)/P_D$ (°C/W)

Where:
T_J = device maximum junction temperature (°C)
T_C = maximum case temperature (°C)
P_D = device power dissipation (W)

The thermal resistance of the heat sink and mounting material also represents heat transfer resistance in degrees Celsius per watt. Thermal conductivity or K-factor for the heat sink or mounting material is specified, by the manufacturer, in watts per centimeter-Celsius or (W)/(cm-°C). Thermal resistance of a material is defined as:

Eq. 2 $\Theta_M = W/(A \times K)$ (°C/W)

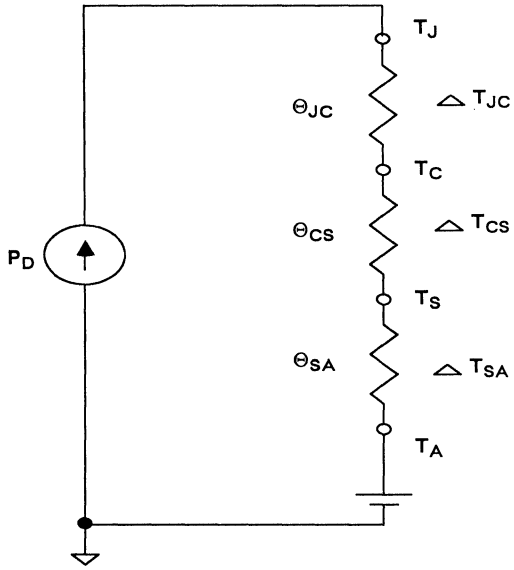
Where:
W = material thickness (cm)
A = heat transfer area (normal to heat flow)
K = thermal conductivity (K-factor)

Electrical Analog

Since thermal resistance is defined as a temperature gradient proportional to power dissipation (i.e. °C/W), it is useful to say:

Eq. 3 $\Delta T_{JC} = P_D \times \Theta_{JC}$

The electrical analog is derived from the above equation since the heat generated at the junction flows through the package, the mounting material and into the heat sink. Each material's thermal resistance results in a temperature rise starting at ambient temperature (T_A). Figure 1 shows the electrical analog of a thermal system consisting of a packaged device, mounting material, and heat sink.



Where: **Θ_{JC} is the thermal resistance junction to case**
Θ_{CS} is the thermal resistance case to heat sink
Θ_{SA} is the thermal resistance of heat sink to ambient

Figure 1. Electrical Analog of Thermal System

From the electrical model an equation is written as follows:

Eq. 4 $T_J = \Delta T_{JC} + \Delta T_{CS} + \Delta T_{SA} + T_A$

4

Where:
$\Delta T_{JC} = P_D \times \Theta_{JC}$
$\Delta T_{CS} = P_D \times \Theta_{CS}$
$\Delta T_{SA} = P_D \times \Theta_{SA}$

Eq. 5 $T_J = P_D(\Theta_{JC} + \Theta_{CS} + \Theta_{SA}) + T_A$

To perform a worst-case analysis of this system, enter the transceiver's maximum junction temperature along with the maximum system ambient temperature, Θ_{JC}, and the maximum power dissipation (P_D).

CONCLUSION

The thermal impedance of the mounting compound and heat sink is calculated from equation 2. Size the mounting material and heat sink (i.e., thickness and surface area) to solve equation 5 for T_J. Refer to UTMC's UT63M1XX Bus Transceiver data sheet for the maximum limits used in equation 5.

A Processor-less Interface for UT1553B BCRTM/BCRT

Overview

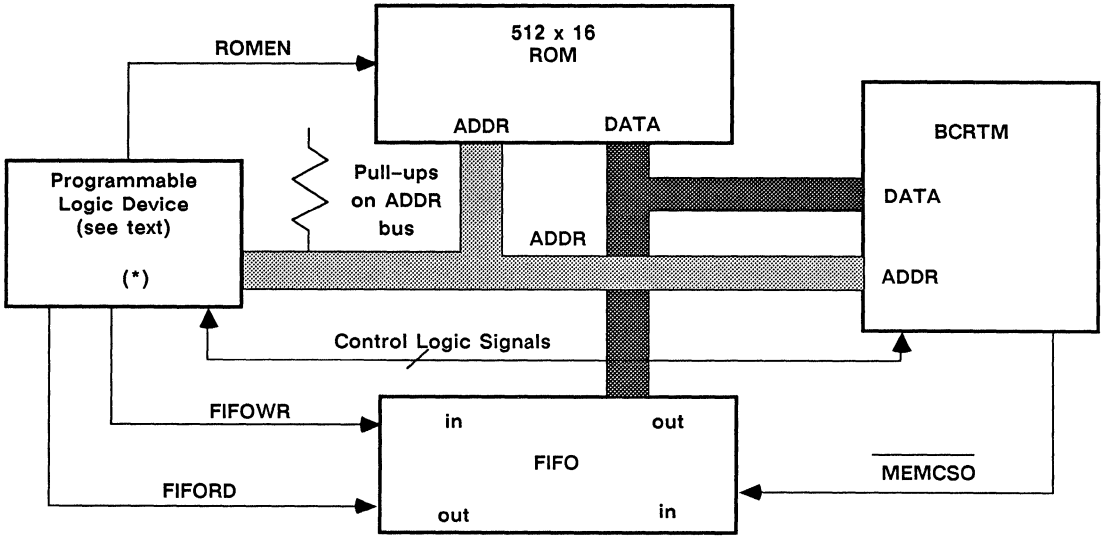
MIL-STD-1553B specifies a time-division multiplex communications bus designed for use in avionics applications. Many times, the 1553B interface is located in a relatively simple device such as a velocity or altitude sensor. In these instances, a processor is not required and the 1553B protocol device must operate stand-alone.

The UT1553B BCRTM is an extremely flexible 1553B protocol device. An inherent quality of its flexibility is that it has several registers to control its operation. As this application note will demonstrate, the BCRTM is a simple device to initialize in spite of its various registers. In can easily be used with a state machine. This solution is ideal for the applications where a processor is not available.

In applications where a processor is available for control, UTMC recommends it be used. Having a processor increases the BCRTM's flexibility and capabilities. However, the design outlined in this note provides for complete RT and Monitor functions from a simple state machine.

The design described requires the BCRTM, a PLD such as the 22V10, a 512 x 16 ROM, and a bidirectional FIFO. The FIFO stores incoming and outgoing data to the host "system." The size of the FIFO is system dependent; it varies according to the largest subsystem and system throughput. The ROM contains the control information for the BCRTM. The PLD controls the sequencing of the BCRTM and FIFOs.

To initialize the BCRTM, the PLD addresses the ROM. The ROM provides the data to the BCRTM. After the data is enabled, the PLD pulses the BCRTM. The BCRTM configuration data is stored at ROM addresses whose lower five bits match the BCRTM register to which the data is going. This feature eliminates the need for multiple address buses or temporary data storage. The address bus should be pulled up to allow the PLD to access the proper ROM addressees with only five address bits. Since the control words are stored in high memory locations, the upper four bits will default to a logic 1. When the BCRTM addresses the ROM to read the control words for incoming 1553 command words, all address lines will be driven, allowing access to the lower memory locations. Figure 1 shows a block diagram of the design.



(*) The PLD also includes the REQUEST-GRANT circuit

Figure 1. Processor-less BCRTM Interface

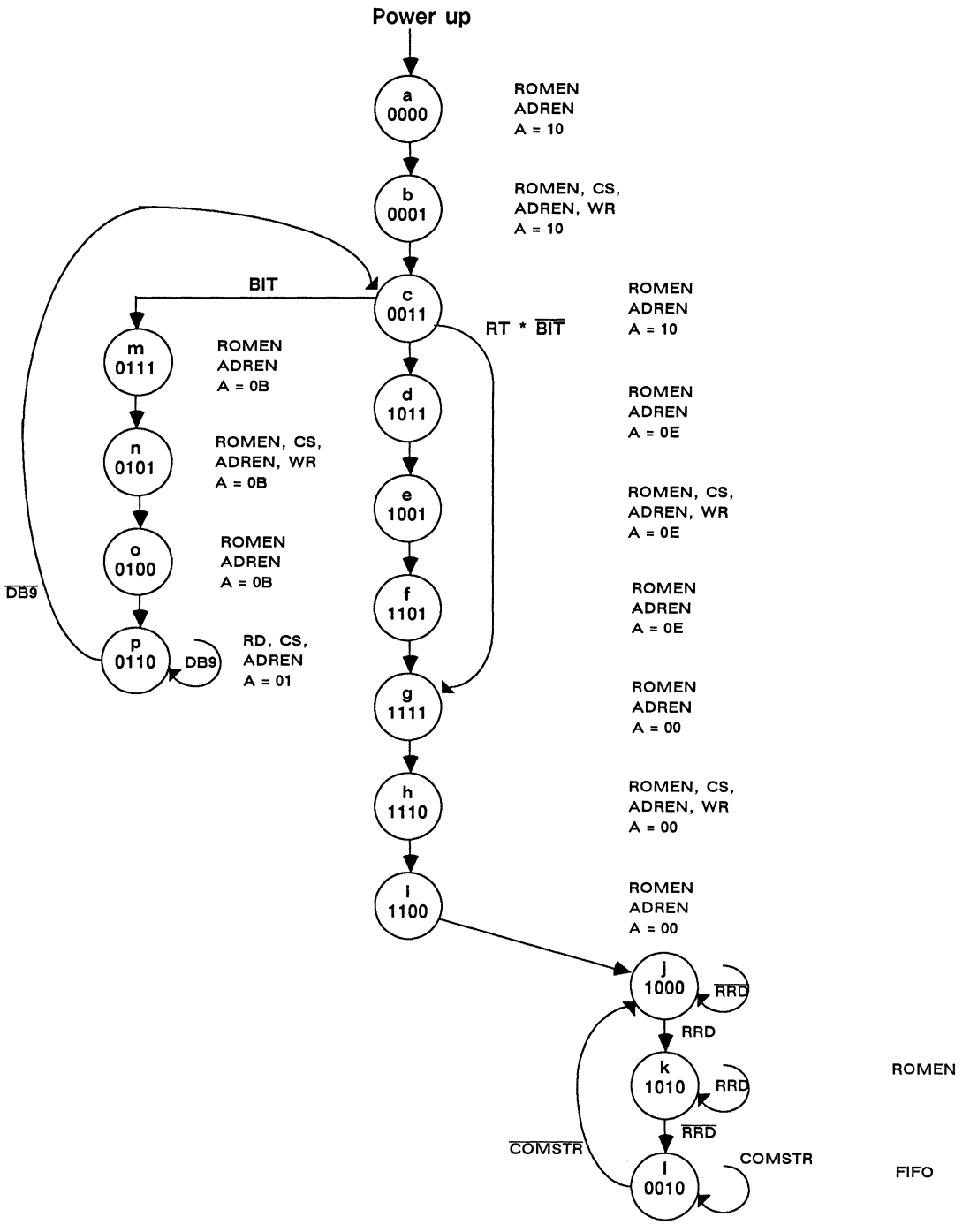


Figure 2. State Diagram

OPERATION

This section will describe the operation of the state machine shown in figure 2. States #a, #b, and #c immediately set up Monitor mode to monitor one terminal. In the example, terminal address 01 is used. If the BIT (Built-In Self-Test) input is asserted, states #m, #n, and #o cause the BCRTM to execute self-test. In state #p, register 1 is continuously examined for end of self-test, indicated by the deassertion of data bit 9 (DB9). BIT is repeated until the BIT input is deasserted. If BIT is not asserted and RT/MON is in the MON state, states #d, #e, and #f set up Monitor mode. If BIT is not asserted and RT/MON is in the RT state, states #d, #e, and #f are skipped.

Execution continues at state #g. This state, along with #h and #i, enables the BCRTM. The state machine then waits at state #j for assertion of the RRD signal. This signal indicates that the BCRTM has received a valid command and is attempting to read the control word. Operation advances to state #k where the BCRTM is allowed to address the ROM to fetch its control word.

If the BCRTM is in RT mode, it will read the corresponding control word out of the ROM as shown in the memory map to allow for command word illegalization. Bits 15, 14, and 12 in the ROM are always ignored and can be used to send flags to the host system if desired.

If the BCRTM is in MON mode, the ROM address accessed is unpredictable. However, the only bit which can affect operation is bit 13. This bit is unused in RT mode; so as long as all bit 13s in the ROM are set to zero, nothing will go wrong.

After the control word access, the state machine advances to state #l where FIFO mode is enabled. All future BCRTM reads will get data from the outgoing FIFO. All future writes will go into the incoming FIFO. FIFO mode is disabled at the end of the message, indicated by $\overline{\text{COMSTR}}$ deasserting. At this time, the state machine returns to state #j. The state machine remains in the state #j/#k/#l loop until the RESET signal is asserted.

In RT mode, two null reads always occur after the control word read. Data will be taken from the outgoing FIFO during these reads. In RT mode for incoming messages, WORD COUNT + 1 words will be stored. The data words are stored in the order they are received. The last word in the FIFO will be the message status word, described in the BCRTM data sheet. In RT mode, for outgoing messages, a status word indicating successful or unsuccessful completion will be stored in the incoming FIFO at the end of the transmission.

In MON mode, the first word stored in the incoming FIFO will be the 1553 command word. This will be followed by a null read from the outgoing FIFO. After this, data words will be stored in the incoming FIFO.

SUMMARY

The techniques described in this note may be extended to the UT1553B BCRT device. In this case, all references to Monitor mode do not apply, and the PLD need only control four address lines.

Table 1. ROM (512 x 16) Memory Map (Addresses not indicated are unused)

000	RX subaddress 01 control word
004	RX subaddress 02 control word
008	RX subaddress 03 control word
078	RX subaddress 31 control word
080	TX subaddress 01 control word
084	TX subaddress 02 control word
0F8	TX subaddress 31 control word
100	Mode Codes 0 & 16 control word
104	Mode Codes 1 & 17 control word
13C	Mode Codes 15 & 31 control word
1E0	Data used to put in BCRTM reg 0 - must be 0181 hex
1EE	Data used to put in BCRTM reg 14 - must be 2000 hex
1F0	Data used to put in BCRTM reg 16 - determined by terminal address value

Table 2a. PLD Description

8 inputs, 4 binary outputs, 5 three-state outputs

Inputs: RESET, CLK (12 MHz), BIT, RT/MON, DB9, $\overline{RRD}$, $\overline{RWR}$, $\overline{COMSTR}$

Binary Outputs: $\overline{CS}$, $\overline{WR}$, FIFORD, FIFOWR

Three-State Outputs: A(4:0)

State Machine State Table:

Current ABCD	Inputs	Next ABCD	Output ROMEN	CS	WR	RD	A(4:0)	ADREN	FIFO
0000 a		0001 b	1	0	0	0	10	1	0
0001 b		0011 c	1	1	1	0	10	1	0
0011 c	/BIT * MON	1011 d	1	0	0	0	10	1	0
	BIT	0111 m							
	* /BIT * RT	1111 g							
1011 d		1001 e	1	0	0	0	0E	1	0
1001 e		1101 f	1	1	1	0	0E	1	0
1101 f		1111 g	1	0	0	0	0E	1	0
1111 g		1110 h	1	0	0	0	00	1	0
1110 h		1100 i	1	1	1	0	00	1	0
1100 i		1000 j	1	0	0	0	00	1	0
1000 j	$\overline{RD}$	1000 j	0	0	0	0	xx	0	0
	RD	1010 k							
1010 k	RD	1010 k	1	0	0	0	xx	0	0
	$\overline{RD}$	0010 l							
0010 l	COMSTR	0010 l	0	0	0	0	xx	0	1
	$\overline{COMSTR}$	1000 j							
0111 m		0101 n	1	0	0	0	0B	1	0 *
0101 n		0100 o	1	1	1	0	0B	1	0 *
0100 o		0110 p	1	0	0	0	0B	1	0 *
0110 p	DB9	0110 p	0	1	0	1	01	1	0 *
	$\overline{DB9}$	0011 c *							

Notes:

1. Lines indicated by an asterisk may be eliminated if a host-controlled self-test is not required.
2. ADREN is an internal signal which controls three-state outputs A(4:0). When ADREN = 0, A(4:0) must be high impedance. The internal values of A(4:0) will be unimportant in this situation. All other outputs are binary.
3. FIFO is an internal signal used in equations shown in table 2b.

Table 2b. PLD Description continued

PLD equations:

Equations are shown using positive logic for all signals; for instance: X = Y * Z indicates that X is HIGH when Y is HIGH and Z is HIGH. Z is high when the input $\overline{Z}$ is LOW. ":-" indicates a registered output; "-" indicates a combinatorial output.

FIFOWR = FIFO * RWR

FIFORD = FIFO * RRD

ROMEN = $\overline{((A * \overline{B} * \overline{C} * \overline{D}) + (\overline{A} * C * \overline{D}))}$

CS = $(B * C * \overline{D}) + (\overline{A} * \overline{C} * D) + (\overline{B} * \overline{C} * D)$

RD = $\overline{A} * B * C * \overline{D}$

WR = $(A * B * C * \overline{D}) + (\overline{A} * \overline{C} * D) + (\overline{B} * \overline{C} * D)$

A0 = $\overline{A} * B$

A1 = $(A * \overline{B}) + (\overline{A} * B * \overline{C}) + (B * \overline{C} * D) + (\overline{A} * B * D)$

A2 = $(A * \overline{B}) + (A * \overline{C} * D)$

A3 = $(A * \overline{B}) + (\overline{A} * B * \overline{C}) + (B * \overline{C} * D) + (\overline{A} * B * D)$

A4 = $(\overline{A} * \overline{B})$

ADREN = $\overline{((A * \overline{B} * \overline{D}) + (\overline{B} * C * \overline{D}))}$

FIFO = $\overline{A} * \overline{B} * C * \overline{D}$

A = $(A * \overline{C}) + (A * D) + (A * C * RD) + (A * B) + (\overline{A} * \overline{B} * C * \overline{D} * \overline{COMSTR}) + (\overline{B} * C * D * \overline{BIT})$

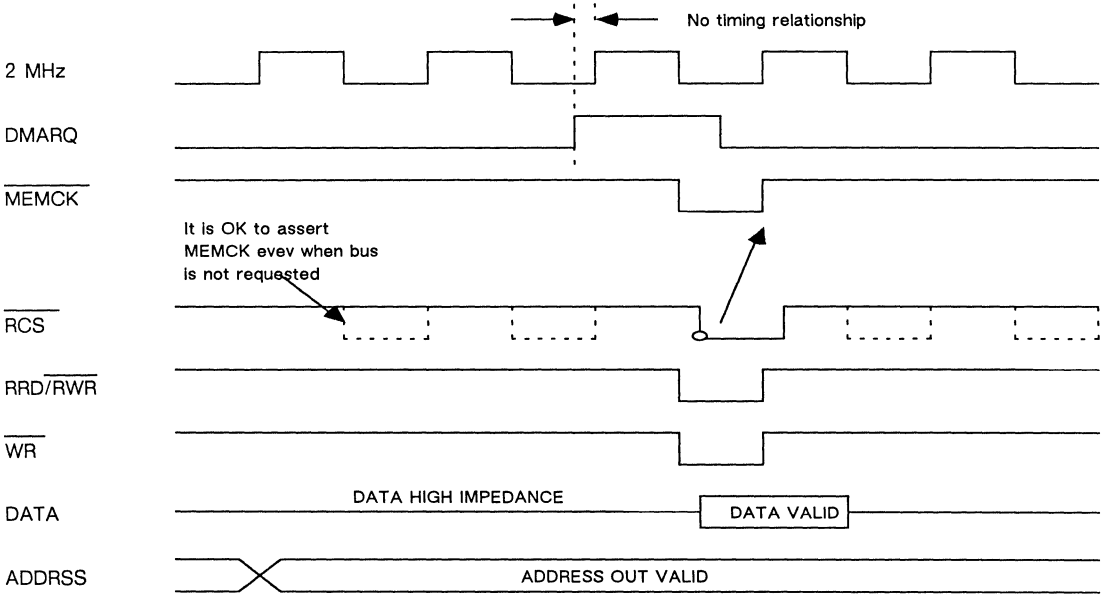
B = $(C * D * \overline{BIT} * RT) + (C * D * BIT) + (A * D) + (B * D) + (\overline{A} * B * \overline{C} * \overline{D}) + (\overline{A} * B * DB9)$

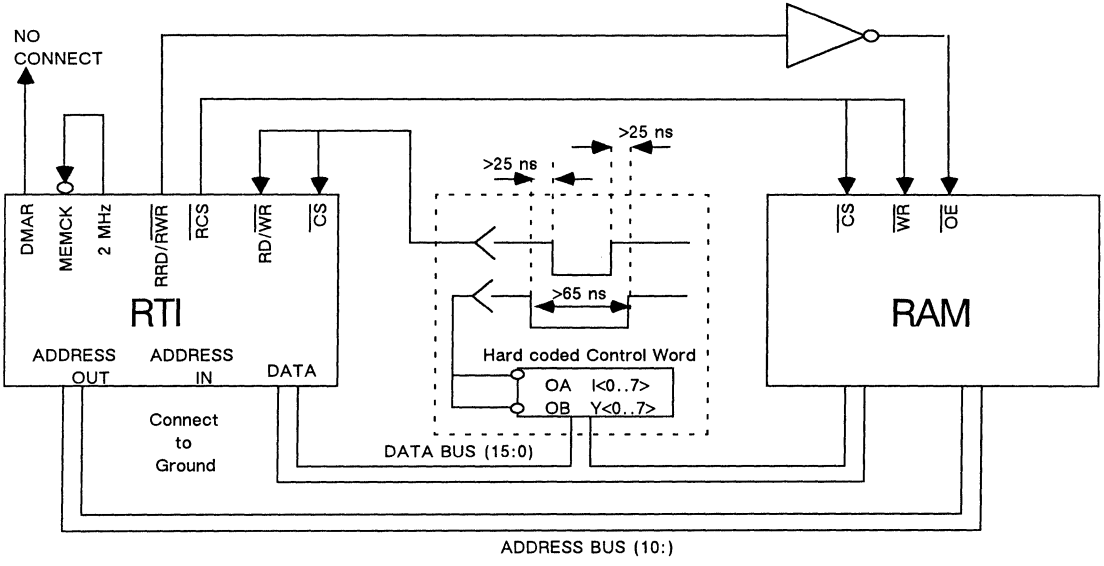
C = $(\overline{A} * \overline{B} * D) + (\overline{A} * B * \overline{D}) + (A * B * D) + (A * \overline{B} * C * \overline{D}) + (A * \overline{B} * \overline{D} * RD)$

D = $(\overline{A} * \overline{B} * \overline{C}) + (\overline{B} * D) + (\overline{A} * C * D) + (A * \overline{C} * D) + (A * \overline{B} * C * \overline{DB9})$

4

It is possible to design the UT1553B RTI into applications not requiring a microprocessor. Start-up requires only assigning an RT Address (refer to RTI data sheet for assigning an Address RT) and an initialization write to the Control Register. The figure below shows the timing for the Control Register write.





UT1553B BCRT to 80186 Interface

Introduction

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive Bus Controller and Remote Terminal functions for MIL-STD-1553B. The BCRT design reduces the overhead placed on the host computer by automatically executing message transfers, providing interrupts, and generating status information. The BCRT offloads the host processor with built-in memory management functions designed specifically for MIL-STD-1553B applications. Thus the host need only establish the necessary data and/or control parameters in memory so that the BCRT can access the information as required and therefore provide the requisite bus functions.

This application note outlines a simple pseudo-dual-port RAM memory interface for the BCRT to be used in conjunction with a 80186 microprocessor. A DMA interface will also be discussed.

The information supplied in this note is entirely applicable to other members of the UTMC BCRT family. This family includes the BCRTM (a BCRT with Monitor functions) and the BCRTMP (a BCRT which operates with a wide variety of avionics serial bus protocols).

Design Selections

The 80186 processor provides the designer with a number of convenient signals for selecting memory and I/O ports. In this application note, the BCRT's registers are in peripheral space. 8K x 16 of static RAM is in the 80186's software programmable "mid-range" memory space. 8K of memory is sufficient for most 1553 applications, but any amount of memory can be used without affecting this design.

Pseudo-dual-port RAM Architecture

The BCRT is equipped with signals for implementing a pseudo-dual-port design with ease. The input signals are: $\overline{RD}$, $\overline{WR}$, and $\overline{MEMCSI}$. The output signals are $\overline{RRD}$, $\overline{RWR}$, and $\overline{MEMCSO}$. When the BCRT is not accessing memory, indicated by $\overline{DMACK}$ high, the inputs are passed through to the outputs. When $\overline{DMACK}$ is low, the inputs are blocked. To generate wait states, an arbitration device controls the 80186's SRDY signal. The same device controls access to the BCRT by the 80186, and to the memory by the BCRT. Figure 1 shows the input and output signals to this device.

Arbitration Details

The arbitration algorithm can be accomplished in a small programmable logic device such as a 22V10. Figure 2 shows a description of the state machine necessary through the use of a state diagram and state table. The state machine is designed to change states on the rising edges of CLKOUT.

A request by the 80186 is defined as the assertion of either $\overline{MCS0}$ in the case of a memory access or $\overline{PCS0}$ in the case of a BCRT access. Since either access requires use of the shared address and data buses, they are treated identically. A request by the BCRT is defined as the assertion of its $\overline{DMAR}$ signal.

Upon reset, the arbitration state machine (ASM) goes to state *a*. It remains in this state until one of three possible conditions:

1. The BCRT requests
2. The 80186 requests
3. Both 1 & 2

In case 1, the ASM goes to state *c*. Here, $\overline{DMAG}$ is asserted. Upon receiving $\overline{DMAG}$, the BCRT asserts $\overline{DMACK}$. The ASM remains in state *c* until one of three events occur:

1.1. The BCRT deasserts $\overline{DMACK}$
1.2. The 80186 requests
1.3. Both 1 & 2.

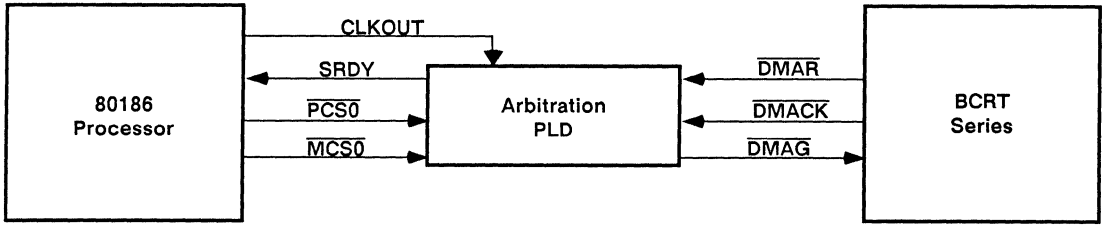
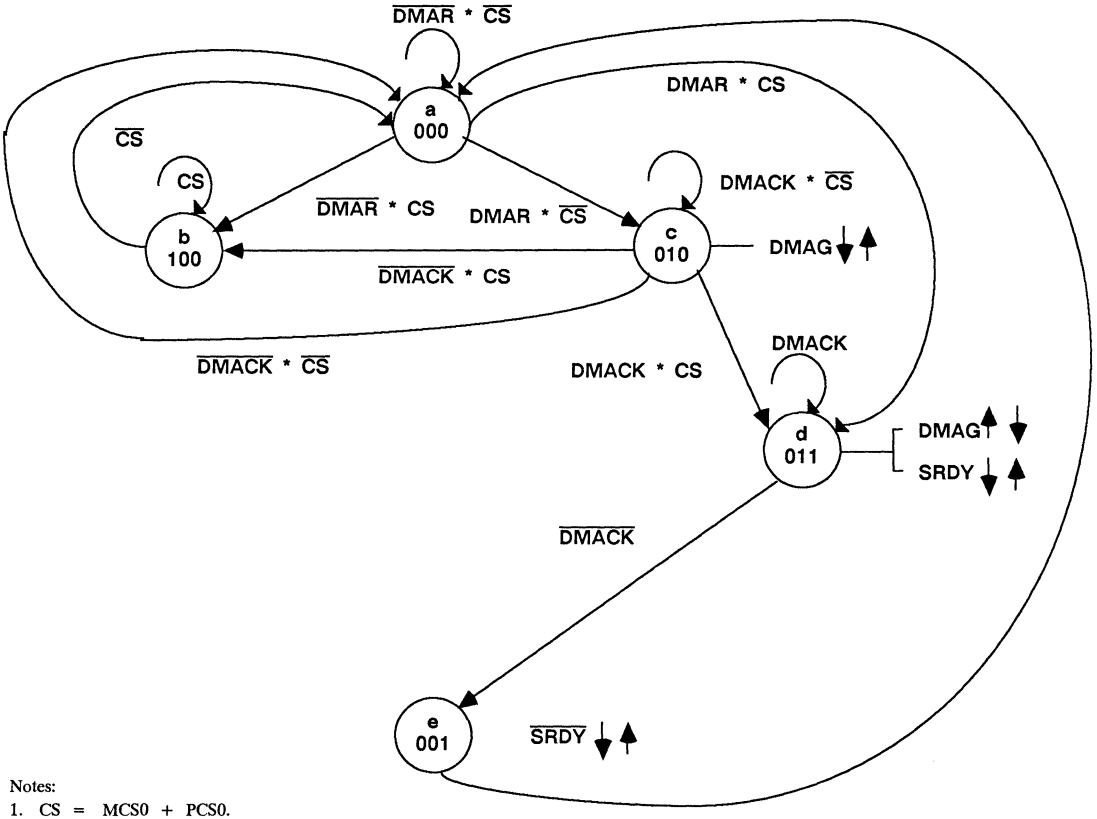


Figure 1. Arbitration PLD Inputs and Outputs



Notes:
1. CS = MCS0 + PCS0.
2. All signals in this diagram have been converted to positive logic; thus DMAR indicates the asserted (low) state and $\overline{\text{DMAR}}$ indicates the de-asserted (high) state of the actual signal.
3. SRDY must be sychronized to CLKOUT.

Figure 2. Arbitration PLD Description

CURRENT STATE				INPUTS			NEXT STATE				OUTPUTS	
	S_0	S_1	S_2	DMAR	CS	DMACK		S_0	S_1	S_2	DMAG	SRDY
a	0	0	0	0	0	X	a	0	0	0	0	0
a	0	0	0	0	1	X	b	1	0	0	0	0
a	0	0	0	1	0	X	c	0	1	0	0	0
a	0	0	0	1	1	X	d	0	1	1	0	0
b	1	0	0	X	1	X	b	1	0	0	0	0
b	1	0	0	X	0	X	a	0	0	0	0	0
c	0	1	0	X	0	0	a	0	0	0	1	0
c	0	1	0	X	1	0	b	1	0	0	1	0
c	0	1	0	X	0	1	c	0	1	0	1	0
c	0	1	0	X	1	1	d	0	1	1	1	0
d	0	1	1	X	X	0	e	0	0	1	1	1
d	0	1	1	X	X	1	d	0	1	1	1	1
e	0	0	1	X	X	X	a	0	0	0	0	1

In case 1.1, the BCRT returns to idle state *a*. In case 1.2, the ASM advances to state *d*, where SRDY is deasserted causing the 80186 to wait until the BCRT is finished. The ASM stays in state *d* until $\overline{\text{DMACK}}$ is deasserted, at which time it advances to state *e*. In this state, the address buffers switch back to 80186 control. The data the processor is trying to read or write is passed. The

ASM then returns to state *a*, where the SRDY is asserted and the 80186 completes its cycle.

In case 1.3, the 80186 requests access in the same cycle that the BCRT has completed. In this case, state *b* is entered and the processor performs a cycle as if the ASM had started from an idle state.

In case 2 from above, the 80186 requests from an ASM idle state. In this case, the ASM goes to state *b*. State *b* prevents the BCRT from receiving a $\overline{\text{DMAG}}$. On the next cycle, the 80186 cycle is complete and the ASM returns to idle state. For slower memories, wait states may be added (with SRDY deasserted) between *a* and *b*. However, care must be taken not to exceed the maximum $\overline{\text{DMAR}}$ to $\overline{\text{DMAG}}$ times given in the BCRT data sheet.

In case 3 from above, the BCRT and 80186 request at the same time. In this case, the BCRT wins and the 80186 must wait (entering state *d*).

Figures 4 and 5 show timing diagrams for each of the possible arbitration scenarios. These diagrams show the transitions on a cycle-by-cycle basis of CLKOUT. For exact timing delays for the 80186 or BCRT, consult the appropriate data sheet.

Memory Control/Access Logic

Figure 3 shows the connection of the remaining control signals required in this interface. Note the use of bus transceivers and latches to demultiplex the 80186 address/data bus. Also note the use of the $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MEMCSI}}$, $\overline{\text{RRD}}$, $\overline{\text{RWR}}$, and $\overline{\text{MEMCSO}}$ signals. If additional memory devices or other peripherals are to be placed in the 80186 system, they should have separate bus transceivers and latches.

DMA Configuration

If additional memory devices and other peripherals are put on the shared address/data bus shown in the diagram, the pseudo-dual-port design is essentially converted to DMA configuration. The arbitration algorithm must now be used for all 80186 accesses. In this configuration, the BCRT lacks a "local" data bus, eliminating several bus buffers and latches. The disadvantage to this approach is that the BCRT data transfers now compete with non-1553-related activity on the host bus. In systems with low bus throughput, this alternative may be an acceptable.

Summary

This note has shown a simple pseudo-dual-port RAM implementation for a BCRT to 80186 interface. A separate application note is available discussing a true dual-port configuration.

For further information on UTMC products and literature, please contact UTMC applications support.

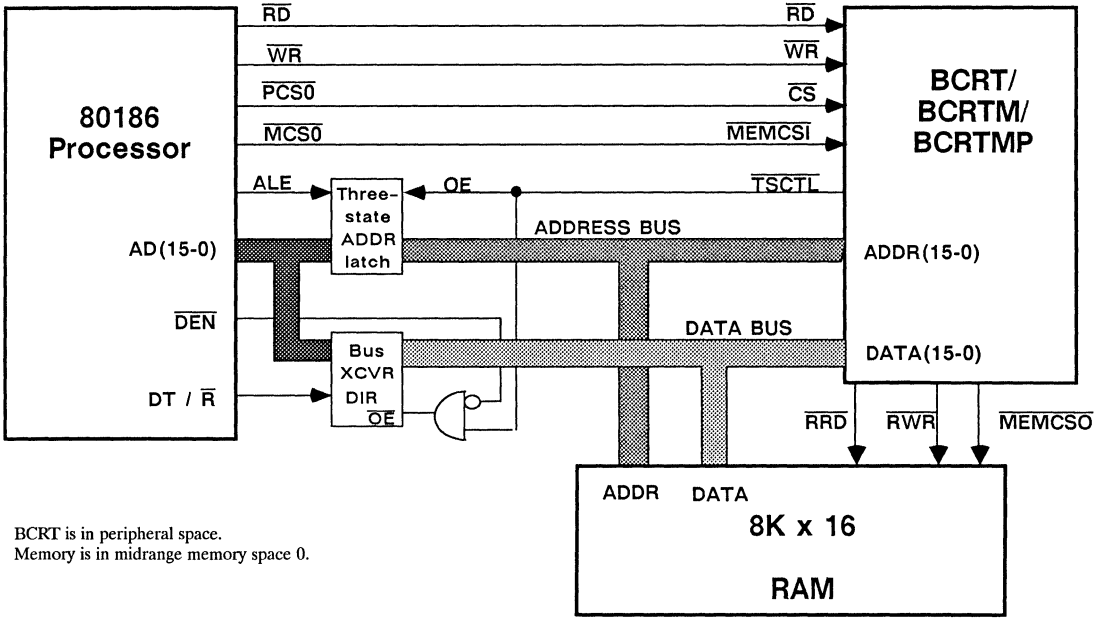
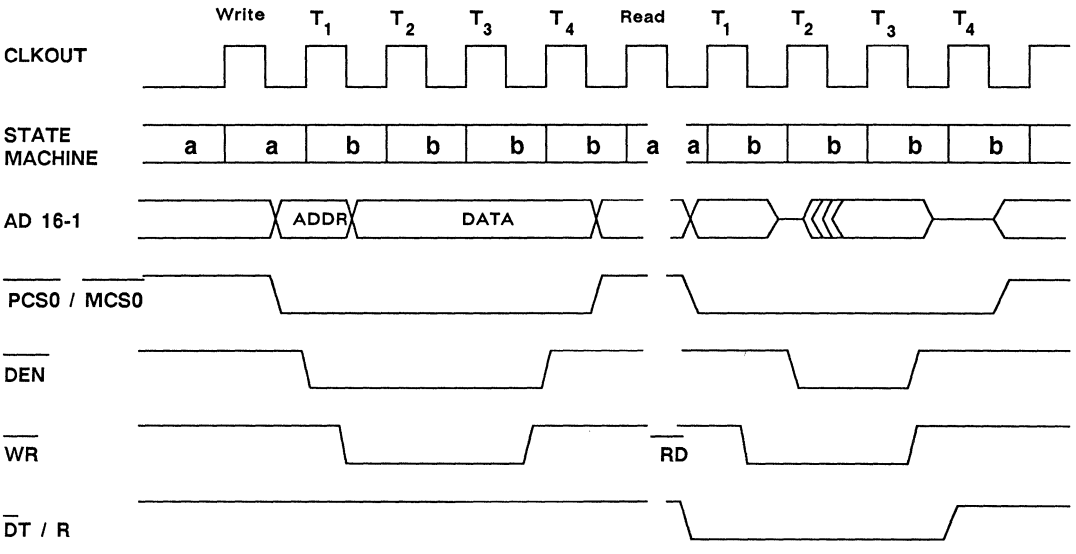


Figure 3. System-Level Control Signals

80186 Access with no Arbitration



Note:
If the BCRTM asserts $\overline{\text{DMAR}}$ while the state machine is in state b, it will have to wait until the state machine returns to state a before its request will be processed (processing then continues as shown below.)

BCRTM Access with no Arbitration

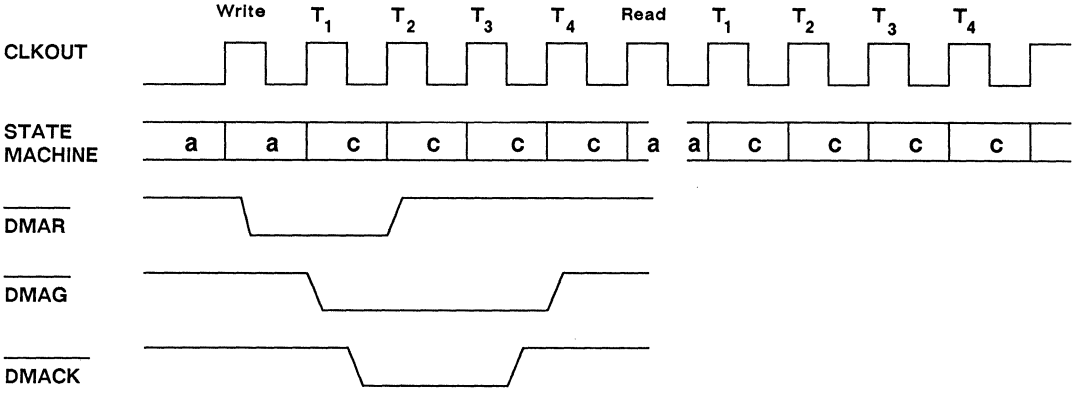
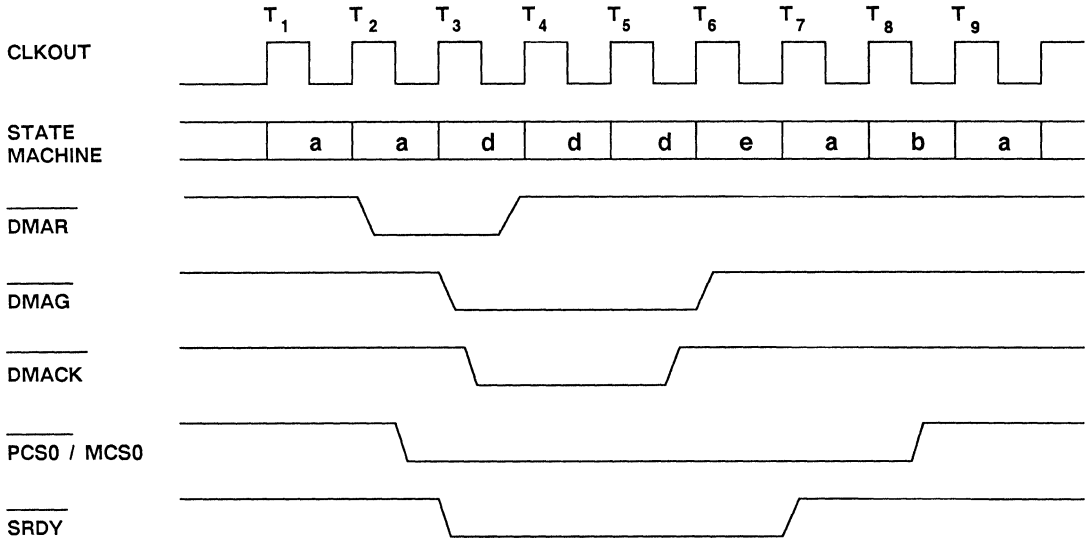


Figure 4. Arbitration Timing Diagram

80186/BCRTM Request at Same Time



80186 Requests While BCRTM is using the Bus (BCRTM is on Last Cycle)

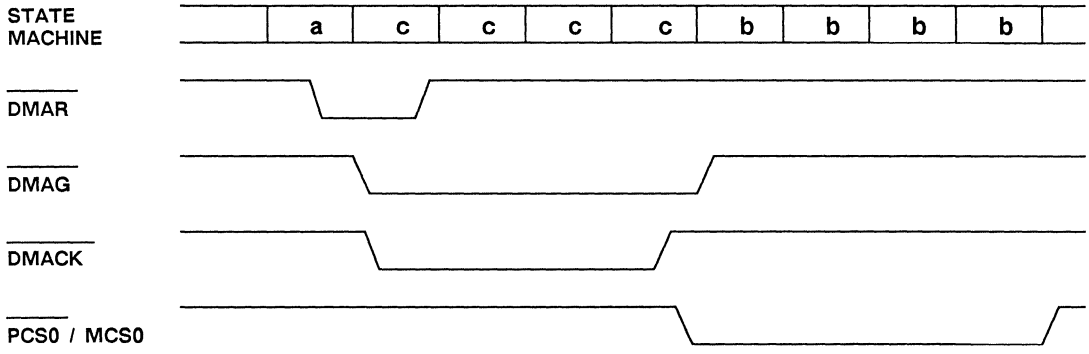


Figure 5. Arbitration Timing Diagram

80186 Requests While BCRT is using the Bus (BCRTM is not on Last Cycle)

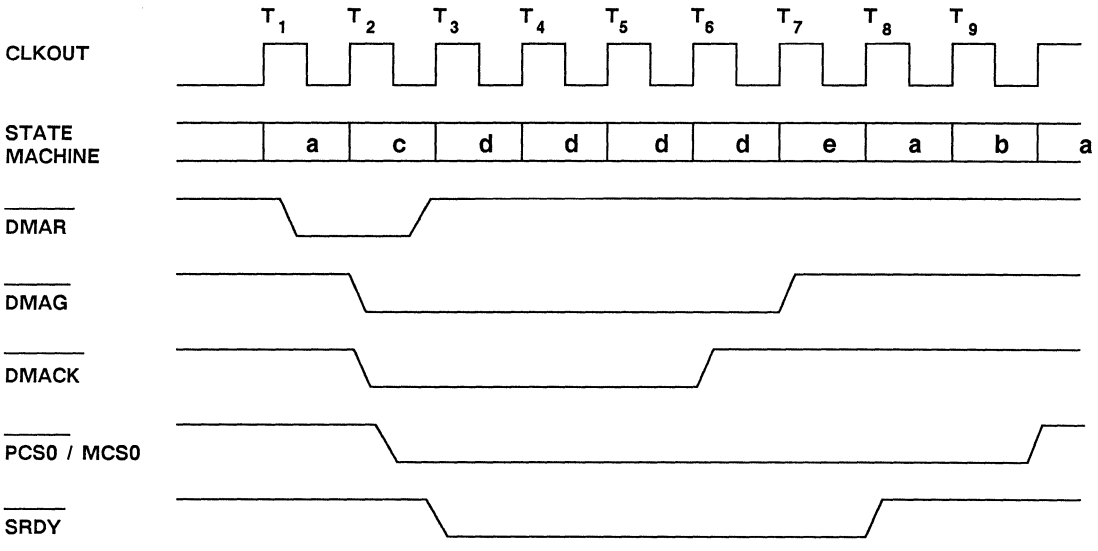


Figure 5. Arbitration Timing Diagram (cont.)

Table of Contents

1.0 Overview

UTMC's quality assurance programs, reliability programs, and military product programs are integrated into the entire manufacturing process.

Our assurance programs support customer needs for nearly every system requirement, regardless of how stringent the application. We welcome the opportunity to discuss how we may support your specific requirements. This section is organized into three major parts: Quality Assurance Programs, including general information about UTMC's typical flow for Level B product and other significant quality activities and capabilities; Reliability Programs and Capabilities; and Military Product Assurance Programs and Capabilities.

2.0 Introduction To UTMC's Quality Assurance Program

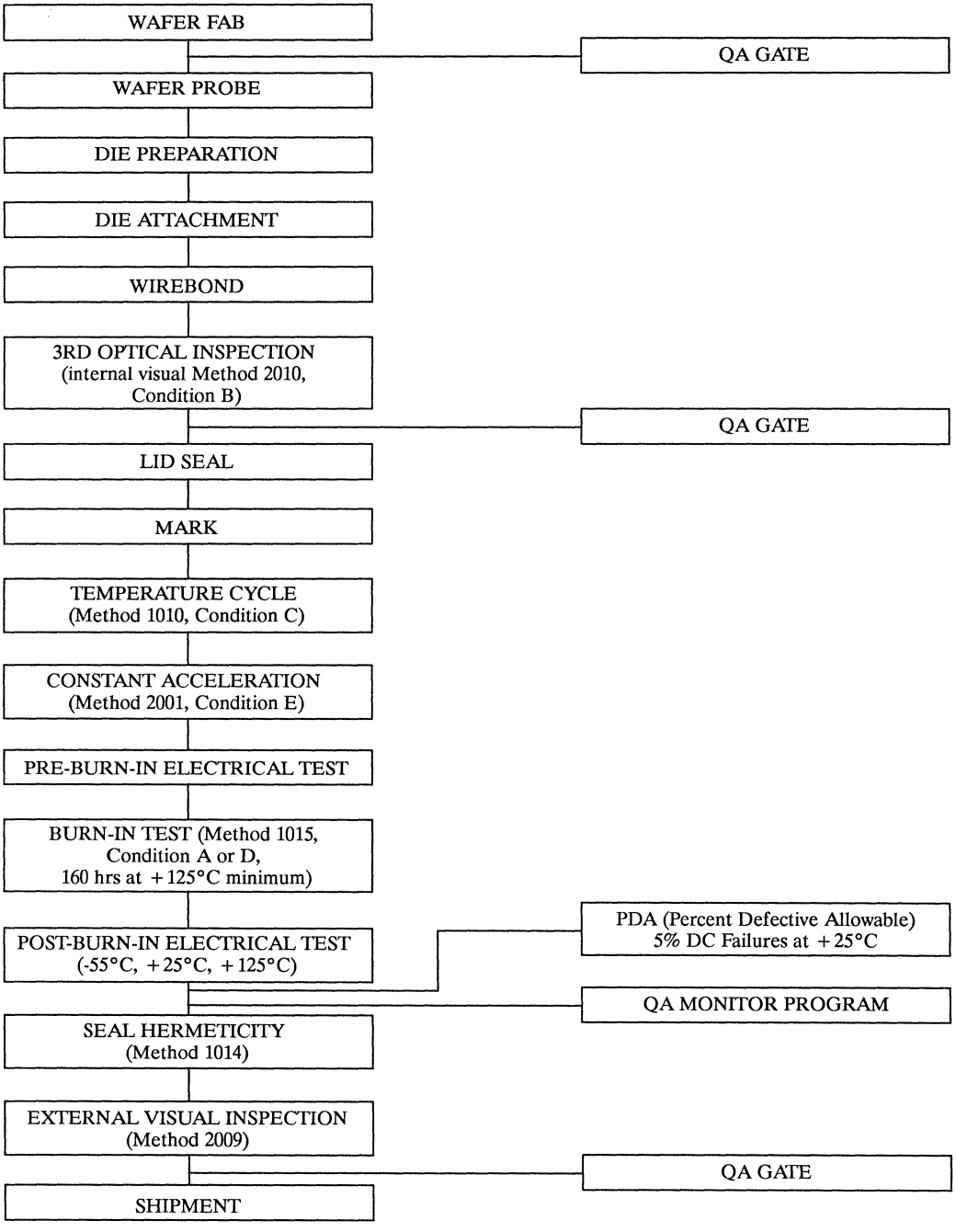
Since 1980, UTMC has delivered advanced high-reliability products to its customers. UTMC's quality assurance activity covers all phases of the manufacturing process, including wafer fabrication, assembly, test, screening, quality conformance procedures, statistical process control, and documentation. UTMC routinely passes on-site quality assurance audits from the country's most demanding military and aerospace companies. UTMC has been approved to MIL-STD-45662, MIL-I-45208, MIL-Q-9858, MIL-STD-883, as well as MIL-M-38510.

The following section describes UTMC's flow for Level B screened product and describes the various capabilities of the quality organization. Additional flows are described in the Military Product Assurance capability section.

2.1 General Information About Level B Flow For UTMC Product

UTMC has established a Level B screening program for those customers whose application simply requires the assurance of a high-reliability screen. One-hundred percent of the devices receive all tests in the production and screening flow, as the flowchart shows. A brief description of each step follows the flowchart (on page 4) and describes the UTMC quality organization's activities and involvement during the manufacturing process. The specific MIL-STD-883 test method is identified in parentheses.

2.1.1 Flowchart



2.1.2 Flowchart Explanation
Class 10 Wafer Fabrication
UTMC fabricates wafers in its Class 10 cleanroom. Reticles and masks are verified before exposing the lot. Scanning electron microscope (SEM) inspection monitors each metal level for step coverage. Electrical parametric process monitors are a routine part of the process for every wafer lot. There are monitors on oxide integrity and phosphorus content, and thickness controls on deposited layers. C-V monitors assure the absence of contamination.

2.1.3 Wafer Probe
The wafer contains many complete circuits (die). During wafer probe, UTMC electrically tests each die on the wafer. Circuits that fail the electrical test are marked with an ink dot so they can easily be distinguished from electrically good die.

2.1.4 Die Preparation
Once probed and inked, the wafers are sawn into separate individual circuits (die). The circuits with ink dots are discarded, and the electrically good die are inspected at high magnification to ensure compliance to visual criteria of MIL-STD-883, Method 2010. Visual rejects, due to physical damage and wafer fabrication defects, are also discarded.

2.1.5 Die Attachment
Using only electrically and visually good circuits, certified operators mount the die in packages using qualified die-attach processes. Die shear or studpull tests monitor the integrity of the die attach.

2.1.6 Wirebond
UTMC uses semiautomatic ultrasonic wirebond machines. This is a critical operation performed by certified operators, who attach aluminum wires from the die surface (bond pads) to posts that lead to external pins on the device, thereby establishing electrical connections. Destructive wirepull SPC (statistical process control) monitors verify bond strength and compliance to military specifications.

2.1.7 3rd Optical Inspection
Certified manufacturing operators inspect all devices assembled using inspection criteria in MIL-STD-883, Method 2010, which consists of a low power microscope inspection from 30-60X, followed by a high power inspection of 75-150X. At low power, the package cavity and the wirebond condition are inspected, and at high power, the die is inspected. Quality assurance then performs a sample inspection to the same visual criteria. Any lot rejected in the quality assurance inspection is reinspected by manufacturing and resubmitted to quality assurance.

2.1.8 Lid Seal
Devices are hermetically sealed with metal lids in a belt furnace that has a controlled temperature ramp from room temperature up to the solder seal temperature. The seal furnace is monitored to assure that the water vapor content is less than 5,000 ppm. Sealing is performed in a nitrogen atmosphere and package moisture is periodically monitored.

2.1.9 Mark
UTMC marks all devices with unique manufacturing part numbers, lot identification, and date codes for traceability as well as ESD markings and customer-specific information, if required. The marking is periodically tested for permanency and inspected 100% for legibility.

2.1.10 Temperature Cycling
One-hundred percent of the devices are tested to Method 1010 (Condition C) of MIL-STD-883, which determines the resistance of devices to high and low temperature extremes as well as to the effects of exposure to extreme temperature gradients. For Condition C, the temperature range is -65°C to +150°C.

2.1.11 Constant Acceleration
UTMC performs the constant acceleration test to a stress level of 30,000 G (20,000 G for packages with inner seals greater than 2 inches or mass greater than 2 grams) per Method 2001 of MIL-STD-883 to cull devices that have internal structural or mechanical weaknesses.

2.1.12 Pre-burn-in Electrical Test
Pre-burn-in electrical test is performed at UTMC's option. This test is designed to detect any electrical defects caused during assembly or environmental tests.

2.1.13 Burn-in Test
The burn-in test eliminates marginal devices, those with inherent defects or defects resulting from manufacturing aberrations that cause early lifetime and stress-dependent failures. UTMC performs this test per MIL-STD-883, Method 1015.

2.1.14 Post-burn-in Electrical Test
Post-burn-in electrical tests verify the effects of burn-in. A 5% PDA (percent defective allowed) is imposed on post-burn-in DC electrical tests at +25°C. UTMC also tests all parts at -55°C and +125°C to ensure that the circuits will operate over the full military temperature range. All devices receive DC, functional, and propagation delay tests at all three temperatures (-55°C, +25°C, +125°C). Quality assurance witnesses the tests or performs a monitor of the setup and reviews the results (see section 2.3.4).

2.1.15 Seal Hermeticity
The purpose of seal hermeticity is to determine the integrity (hermeticity) of the seal on the devices. The fine leak and gross leak testing conforms to MIL-STD-883, Method 1014.

2.1.16 External Visual Inspection
An external visual inspection verifies that the device materials, design, construction, markings, and workmanship meet the specification. Manufacturing operators perform the external visual inspection to Method 2009 of MIL-STD-883, at a magnification of 3-10X. Quality assurance performs a gate inspection

(sample) after manufacturing's 100% inspection. Manufacturing rescreens 100% of the lots rejected in the quality assurance inspection and resubmits them to quality assurance. Quality assurance also checks the travelers for completeness, for necessary data, and to ensure traceability requirements.

2.2 Other Significant Quality Activities And Capabilities At UTMC

UTMC provides complete quality assurance capabilities and services to internal customers as well as purchasers of UTMC components. Fully qualified and trained personnel, knowledgeable in supporting customers' requirements, staff our departments.

2.3 Process Control

2.3.1 Statistical Process Control

UTMC has embarked on a company-wide Statistical Process Control (SPC) effort to support the intent of and letter of JEDEC Standard 19, General Standard for Statistical Process Control. With the support and involvement of management from the president to the operators on the production floor, UTMC is placing all critical nodes under SPC. On-line real-time methods such as control charts support SPC efforts at critical points in the fabrication process. UTMC's goals through these efforts are continual improvement of all product and the development of products that are more reliable, have less variation in their performance parameters, and are thus made more efficiently. All of these efforts result in the customer seeing a superior product at a reduced cost.

2.3.2 Quality Assurance Inspections And Monitors

Work-in-process inspection gates and monitors enhance the production process by ensuring process consistency and component conformance from operation to operation, and by providing information for tracking the quality and yields of a given process. The quality assurance staff performs the required inspections and ensures that the proper departments generate and retain required records in accordance with MIL-M-38510. Quality assurance controls and assigns quality assurance stamps.

2.3.3 Wafer Fabrication Process Monitors

UTMC quality assurance personnel visually inspect all wafer lots at completion of the manufacturing process. Quality assurance personnel also conduct a complete traveler review on every lot. In addition to the gate inspection, quality assurance also performs process monitors at strategically placed locations throughout the wafer fab process. Quality assurance also performs environmental monitors, and conducts particle counts, humidity checks, temperature checks, and production log book audits on a periodic basis.

2.3.4 Monitor Program At Test

Quality assurance inspectors verify test hardware, software, and test conditions to ensure that UTMC tests devices in accordance with specifications requirements, in lieu of performing a separate Group A electrical test, when not specifically required. As with all specification requirements, quality engineering reviews test programs against customer requirements before use.

2.3.5 Off-line Monitors

For semiconductor manufacturing, process monitors are important tools for process control. UTMC conducts many of the off-line monitors such as boron and phosphorous doping in oxides using Fourier-transform infrared wavelength spectrophotometer (FTIR) and wet chemistry methods, process gas monitoring using mass spectral analysis, step coverage using cross-sectioning and SEM analysis, die attach and bonding characteristics using SEM and x-ray analysis. In addition, finished device cross-sectioning (structural analysis) and spreading resistance probing (SRP) are used to analyze doping profiles and to evaluate the integrated process flow.

2.3.6 Outgoing Inspection

Prior to shipment, all lot documentation is verified against the customer purchase order to ensure that the product meets customer requirements. A certificate of compliance, signed by a quality engineer, accompanies each production shipment.

2.3.7 Nonconforming Material Handling

UTMC segregates any rejected material and then submits it to a Material Review Board for disposition. Representatives of quality assurance, engineering, planning, and manufacturing comprise the Material Review Board (MRB). All voting members approve disposition of the material. The material must meet the customer specification unless the customer has provided written approval to waive the requirements.

2.4 Program Support

2.4.1 Incoming Quality Assurance (IQA)

UTMC ensures that all supplies and services from external vendors conform to contract requirements. Trained quality assurance personnel perform all incoming inspection procedures. The sources and controls UTMC exercises depend on the material's use and the supplier's demonstrated performance capability. Package pieceparts are evaluated using MIL-STD-883 test methods. Quality assurance engineers review purchase orders before they are placed with vendors, and also conduct periodic vendor surveys. UTMC quality assurance maintains an approved vendor list. Statistical process control is used wherever possible to maintain critical parameters. UTMC uses SEMI standard methods for routine incoming chemical analysis prior to acceptance. The equipment available in support of these evaluations includes gas chromatograph (GC), atomic absorption spectrophotometer (AA), ultraviolet/visible wavelength spectrophotometer, Fourier-transform infrared wavelength spectrophotometer (FTIR), and liquid ion chromatograph (IC), as well as complete wet-lab chemistry capability.

2.4.2 Metrology

UTMC's metrology section maintains the calibration of test and measuring equipment in accordance with MIL-STD-45662. A computerized recall and record-keeping system assures that UTMC uses only

calibrated test and measuring equipment for device acceptance testing, process monitoring, and equipment setup.

2.4.3 Quality Audit Program
UTMC's quality audit program consists of roving process checks, product inspections, and evaluations in all UTMC manufacturing operations and support groups that can affect quality, reliability, or yield. These audits determine compliance of operators and inspectors to procedures and specifications, evaluate the product status and quality, and assess the effectivity of manufacturing and quality assurance systems. UTMC maintains a self-audit program in accordance with MIL-M-38510. This program assures that UTMC's Product Assurance Programs maintain compliance to the applicable military specifications. This program also assures that UTMC maintains its quality system procedures and controls in accordance with UTMC policies.

2.4.4 Major Change Notification
UTMC notifies all customers of any major change as defined by MIL-M-38510. Major change notifications include a thorough description of the proposed change and, if requested, a test plan that demonstrates that the change will not adversely affect performance, quality, reliability, or interchangeability, and that the changed product will continue to meet the customers' specifications and expectations.

2.4.5 Quality Assurance Engineering Customer Support
Quality assurance engineers are assigned to specific customers and review their customer's specifications at all stages of the customer-supplier relationship. Quality assurance engineers are the liaisons for all customer surveys and audits. UTMC makes every effort to accommodate the customer's needs for understanding our capability to manufacture a device meeting his requirements. We are also fully prepared to support customer or government source inspections.

2.4 6 Quality Assurance Manual
UTMC maintains a comprehensive quality assurance policy manual, which is available to customers at all times. The manual describes UTMC's quality and reliability practices, references controlled procedures and specifications, and is updated periodically.

2.4.7 Document Control
Document control ensures the adequacy, uniformity, and currentness of all documentation used or referenced during the design or manufacture of UTMC's IC devices. Controlled documentation is an integral part of the quality assurance program that satisfies customer quality requirements, and is concerned with traceability of product, effective change control, and the documentation that describes product configuration. Documentation practices are based on the requirements of DOD-D-1000 and DOD-STD-100. Changes in product description, materials, or procedures used to assemble product cannot be implemented until the change assessment is made and proper documentation is in place. UTMC's documentation meets the requirements of MIL-M-38510 and MIL-STD-976 for process change control, including record retention and archive. Any changes to process or product become part of the historical record in our documentation, thus providing full traceability of how a product was fabricated.

Document control makes a record of the document change and stores the records for approved document changes in accordance with MIL-M-38510. This information is essential to building UTMC's statistical data files and for test or screening analysis.

2.4.8 Document Change Control
Document change control provides a record of approved changes to process, procedure, raw material, or other controlled documents. Document change control provides the means for initiating new documents or updating existing documents as necessary to assure that manufacturing uses only approved documents to produce product. Quality assurance engineers are required to approve changes for all manufacturing documentation.

UTMC's document control has full word processing capabilities and computerized document tracking, which contribute to providing prompt document updates. Document control also assures that documents are well organized and grammatically correct so that readers easily understand instructions and information. Document control distributes controlled documents to manufacturing and engineering areas and removes expired or withdrawn documents from the controlled document stations. Having this responsibility centralized provides assurance that product is built to the correct revisions of all processes.

2.4.9 Materials Analysis Services
Materials analysis services are contained in a well-equipped laboratory with chemical services, drainage, and ventilation. Within the laboratory, advanced analytical equipment is available for routine evaluations as well as developmental requests. In addition to incoming materials evaluations and off-line process monitors, the laboratory performs process evaluations and failure analysis. These services enable UTMC to satisfy customer concerns with respect to technology evaluation.

UTMC conducts process and equipment evaluations, defect identification, as well as failure analysis inspections, using optical microscopes and two scanning electron microscopes (SEMs) capable of in situ elemental identification using WDX (wavelength dispersive x-ray) and EDS (energy dispersive spectroscopy) methods. For these evaluations, UTMC uses metallurgical sectioning and polishing methods in sample preparation. Evaluations may include top view and cross-section photomicrographs, structural analysis, and Spreading Resistance Probe (SRP) junction profiles. The laboratory performs SEM step-coverage analysis and destructive physical analysis (DPA) in conformance with MIL-STD requirements.

For product that requires failure analysis, Materials Analysis performs the evaluation. The failure analysis support extends from electrical test rejects, to failures to

MIL-STD tests, to customer returns. In addition to full electrical characterization available on the electrical test systems, bench test techniques such as microprobing, laser isolation, and liquid crystal mapping are used in diagnosis. Deprocessing may include acid and plasma etching, with inspections conducted on the SEM. Failure analysis reports are available to the customer on all return material authorization requests (RMAs).

3.0 UTMC Reliability Capabilities

The UTMC reliability department's charter is to verify product reliability performance using accelerated methods and to conduct product testing to satisfy conformance requirements established internally as well as those the military or the customer may specify.

The reliability department uses procedures that comply with recognized industry test methodologies as well as MIL-M-38510 and MIL-STD-883 requirements. Certified personnel conduct testing on calibrated equipment using fully documented test methods. UTMC uses industry-recognized statistical methods in selecting sample sizes and evaluating test results.

Equipment to conduct most reliability test methods is located on-site. For tests that require externally contracted service, we use only recognized laboratories that have satisfied UTMC audits of their compliance to our requirements.

Reliability tests product under numerous conditions for a complete understanding of product reliability throughout the manufacturing cycle. Testing begins during the process development cycle, continues through qualification, and extends into monitors of the manufacturing process. Test methods include wafer-level testing for quick-turn monitoring of the fabrication process, steady-state life testing as the formal method of accelerating use conditions, and mechanical and environmental tests to determine tolerance under exposure to harsh environments. Because of the numerous product variations permitted with customer specific designs, UTMC performs much of the testing using a Standard Evaluation Circuit (SEC). Thus, UTMC can assure high reliability prior to delivery of product to the customer.

3.1 Wafer-level Reliability Testing

UTMC recognizes that product performance requires that technology development decisions be undertaken with reliability as a key consideration. In support of this belief, the reliability department conducts wafer-level evaluations of product and test circuits during the decision-making phases of process development. These evaluations include transistor lifetime (hot-carrier injection), oxide lifetime (time-dependent dielectric breakdown), metalization lifetime under electromigration, and thermal and physical stresses directed at evaluation of void formation in aluminum. Process development selects the manufacturing technology only after achieving established performance targets on these wafer-level tests.

3.2 Steady-state Life Test

Reliability conducts steady-state life testing of product using temperature and voltage acceleration from operating conditions on all manufacturing technologies using package configurations that include DIP, LCC, PGA, and Cerquad. Reliability determines potential product failure mechanisms and projects failure rates using data from these tests. These tests conform to MIL-STD-883, Method 1005.

3.3 Mechanical Tests

Reliability conducts various mechanical tests to qualify the materials and manufacturing technology at mechanical fatigue levels above projected use. These tests include constant acceleration, lead integrity, severe shock (mechanical shock), and product tolerance to vibration. These tests conform to MIL-STD-883, Methods 2001, 2002, 2004, and 2007.

3.4 Environmental Tests

Reliability conducts environmental tests to ensure package integrity under harsh environments such as exposure to humidity, salt, temperature cycling, and thermal shock. All package outlines complete these tests as part of qualification. These tests conform to MIL-STD-883, Methods 1004, 1009, 1010, and 1011.

3.5 Circuit Performance Evaluation

Reliability evaluates circuit performance with respect to electrostatic discharge sensitivity (ESDS) and latchup susceptibility. Our ESD testing conforms to MIL-STD-883, Method 3015.

3.6 Radiation Testing

UTMC produces integrated circuits that satisfy the highest levels of radiation tolerance specified for military and space applications. To assure acceptable performance and radiation tolerance, UTMC qualifies manufacturing processes and tests each radiation-hardened fabrication lot on-site. This testing includes wafer-level transistor performance and radiation tolerance monitoring using an Aracor x-ray irradiation system. Radiation tolerance testing also includes the functional testing of packaged devices after exposure to gamma rays from an on-site cobalt 60 source. This packaged device testing conforms to MIL-STD-883, Method 1019.

4.0 Military Product Assurance Capabilities

UTMC has several ongoing Product Assurance Programs to satisfy the demanding requirements of aerospace and defense systems. UTMC is capable of manufacturing product compliant to MIL-STD-883, Level S and Level B, Standard Military Drawing (SMD) devices, JAN MIL-M-38510 qualified standard product, and JAN MIL-M-38510 gate array qualified product. These programs, described in the following pages, allow customers to select the Product Assurance Program that best meets their system requirements. For the various programs, UTMC maintains critical design and traceability documentation, including process

travelers/flowcharts, design baselines, design files, current density calculations, and major change control. These services fully support customers' product assurance program requirements.

4.1 UTMC Level S Program

UTMC's Level S Program satisfies customers' requirements for space application systems. These applications include rocket launch vehicles, manned spacecraft, satellites, and strategic weapons. The program ensures the highest level of reliability. This reliability is essential where a single failure could be catastrophic to system performance. UTMC achieves the highest level of reliability by processing, monitoring, and inspecting product to the strict Level S requirements of MIL-STD-883. This includes meeting the Level S process control requirements of MIL-M-38510 and MIL-STD-976.

UTMC verifies the integrity of the wafer lot by performing wafer lot acceptance to MIL-STD-883, Method 5007, which verifies film thicknesses, gate oxide integrity, and metalization interconnect quality. Die attach and wirebond assembly operations quality is tightly controlled in accordance with the Level S requirements of MIL-STD-976. UTMC uses the Level S lot formation and rework controls of MIL-M-38510 to assure lot uniformity and removal of defective product. Where non-destructive bondpull testing is not feasible to verify the integrity of wirebonds, such as for high pincount packages, UTMC uses statistical process control techniques. Product screening flows can accommodate both static and dynamic burn-ins as defined by system requirements to eliminate infant mortality or ionic contamination failures devices. Automated delta calculation capability assures accurate results for critical system parameters. UTMC can also perform total dose irradiation testing internally to verify product radiation hardness. Data summaries for wafer lot acceptance, screening results, quality conformance inspections, and other process information is available to customers upon request. See UTMC's Level S Program brochure for more details on the Level S process flow and inspection requirements.

4.2 JAN MIL-M-38510 Gate Arrays

UTMC has established JAN certifications and qualifications to build CMOS gate arrays to the generic family qualification requirements in military detail specifications MIL-M-38510/605, 606, 607. These generic family qualifications allow UTMC to supply its customers JAN gate arrays without having to go through the added time and expense of qualifying each design personalization. The design system and process controls assure that the entire product family meets the quality and reliability requirements for military and defense applications. Once a customer's circuit design is ready for production, UTMC manufactures the product and performs lot-specific quality conformance inspections, and delivers the product as JAN-qualified. This enables customers to receive CMOS gate arrays to the JAN quality/reliability level established for defense applications.

Each design receives a standard set of Design Rule Checks (DRC), Electrical Rule Checks (ERC), and Layout versus Schematic (LVS) checks to verify the integrity of the customer's design.

UTMC has developed standard evaluation circuits (SEC) for assessing product reliability. These evaluation circuits exercise the design process by maximizing use of the cell family, and exercise the layout and fabrication processes by maximizing routing and silicon use. The standard evaluation circuits flow through the entire manufacturing process (design, layout, simulation, fabrication, assembly, inspection, and testing) using specified UTMC procedures. With these worst-case designs, the technology receives full-scale evaluation prior to customer product delivery. The SEC establishes the initial qualification of each process family and serves as an ongoing reliability monitor. This eliminates the need for costly qualifications on individual customer designs from the same product family and reduces the lead time for delivering gate array products to customers.

This program also generically qualifies packages with the same case outline style (e.g. pingrid arrays). The worst-case package (usually the package with the highest pincount) within a given case outline style receives the quality and reliability tests the JAN detail specification defines. This testing establishes the qualification of the given package family and eliminates the added cost and time to qualify.

4.3 JAN MIL-M-38510 Standard Product

UTMC has the capability to establish JAN qualification of its standard products for those customers whose systems demand the JAN quality level. The Defense Electronics Supply Center (DESC), Dayton, Ohio, certified UTMC's wafer fabrication, assembly, screening, and test capabilities to build JAN Level B CMOS product. The qualification and quality conformance procedures meet the Groups A, B, C, and D inspection requirements of MIL-M-38510. The successful completion of the qualification tests results in a listing on the Qualified Products List (QPL-38510). DESC periodically audits the JAN-certified line to assure that UTMC maintains MIL-M-38510 requirements. The U.S. Government Defense Contracts Administrative Service (DCAS) monitors qualification and production lots to assure that we build product to military specifications.

4.4 Standard Military Drawings (SMD)

UTMC establishes Standard Military Drawings (SMDs) on many of its standard products upon their initial release. SMDs help minimize the number of source control drawings (SCDs) generated for a given standard product. The ease in generating SMDs permits immediate standardization in the military systems parts procurement programs. Such standardization helps minimize part number tracking, allows the use of the same part number for multiple systems, and reduces inventory costs. Also, SMD devices are built in compliance with MIL-STD-883, Level B, requirements specified for many military and defense systems.

The SMD program eliminates added time and cost for UTMC and its customers in generating and reviewing customers' source control drawings (SCDs). UTMC generates the drawings quickly by being on-line with DESC's telecommunication SMD system. This system allows immediate transmission and review of SMD drawings as they are generated, which significantly reduces the lead times for releasing drawings for customers' use. SMDs receive recognition and approval by program offices when compliance to MIL-STD-883, Level B, is imposed on system requirements.

4.5 MIL-STD-883 Class B Program

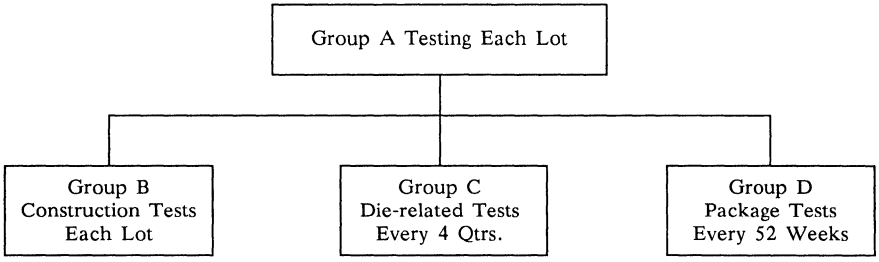
UTMC maintains a compliancy program for those products not JAN qualified nor listed on an SMD. This program supports Class B products with radiation hardness requirements of 1.0×10^5 or 1.0×10^6 total dose, and also supports customers' SCDs that require Class B product compliant to MIL-STD-883. UTMC has implemented the requirements of MIL-STD-883, paragraph 1.2.1, which includes meeting the screening requirements of Method 5004 and the qualification and conformance requirements of Method 5005, Groups A, B, C, and D. UTMC also has the internal capability to perform Group E total dose irradiation testing for products requiring radiation hardness testing. The following flow diagrams further describe the Class B screening and quality inspection flows.

UTMC has implemented Method 5010 to support small lot quantities for complex devices. This program provides several time and cost advantages for customers. Incoming package evaluations allow reduction of end-of-line quality conformance inspections, and generic process qualifications eliminate individual design qualifications. Method 5010 allows an alternate procedure for QA verification of production electrical test setup in lieu of a separate Group A electrical test. Sample sizes are smaller for Groups C and D, die and package, reliability tests. See the following inspection flows.

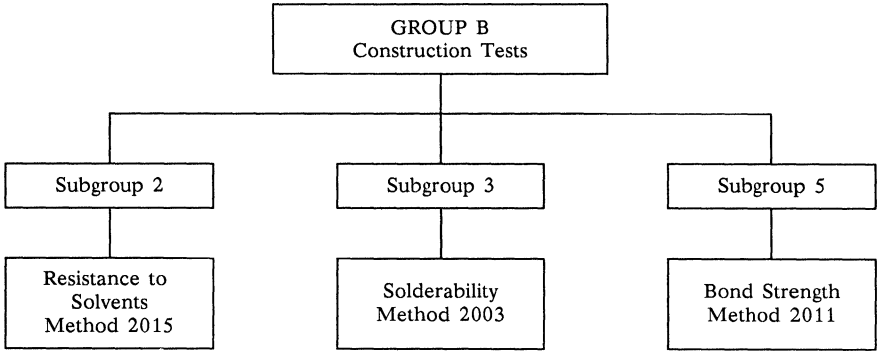
5.0 MIL-STD-883, Class B, Quality Conformance Inspection (QCI)

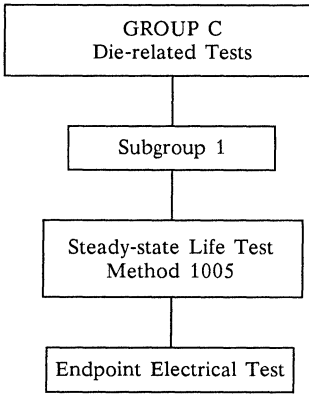
5.1 MIL-STD-883, Class B, M5005, Quality Conformance Inspection

UTMC performs Group A, B, C and D tests as military specifications require or as the customer specifies. All tests are in compliance with the required methods detailed in MIL-STD-883.

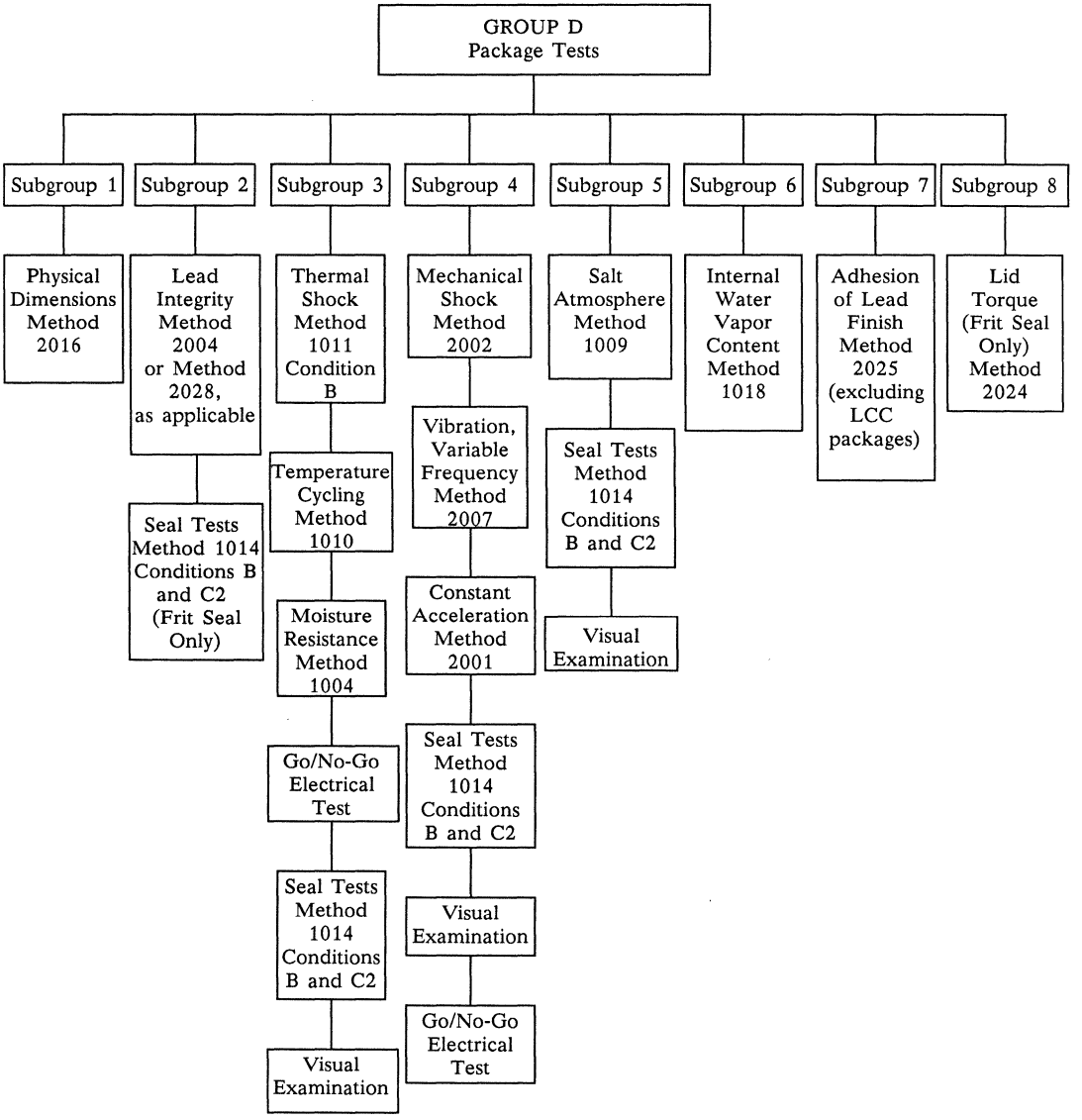


MIL-STD-883, Class B, M5005, Quality Conformance Inspection - Groups B & C



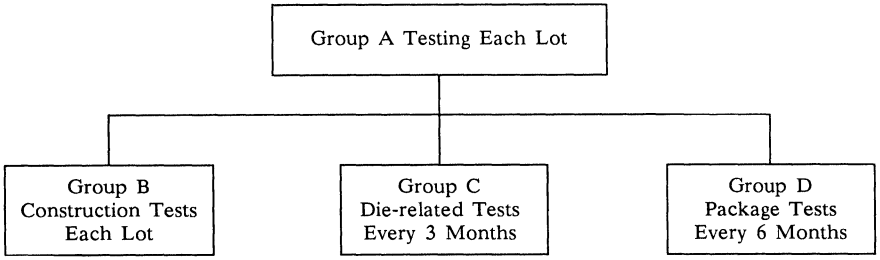


MIL-STD-883, Class B, M5005, Quality Conformance Inspection - Group D

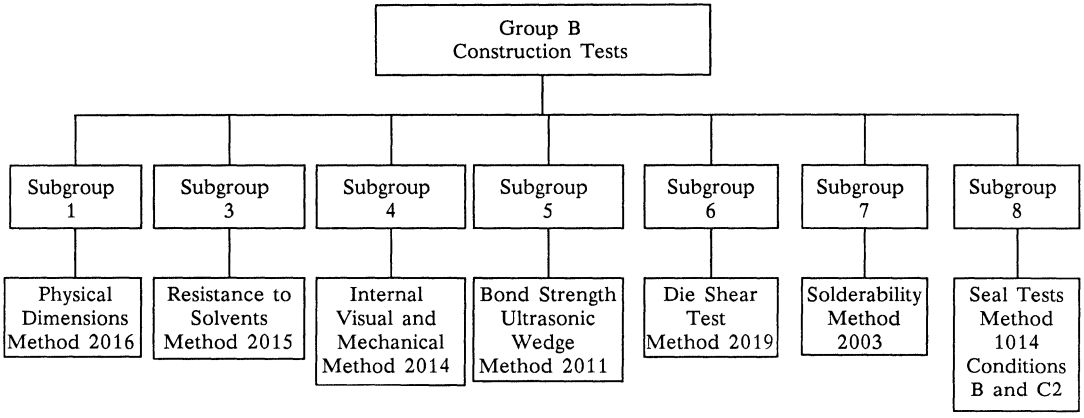


5.2 MIL-STD-883, Class B, M5010 Quality Conformance Inspection

UTMC performs Group A, B, C and D tests as military specifications require or as the customer specifies. All tests are in compliance with the required methods detailed in MIL-STD-883.

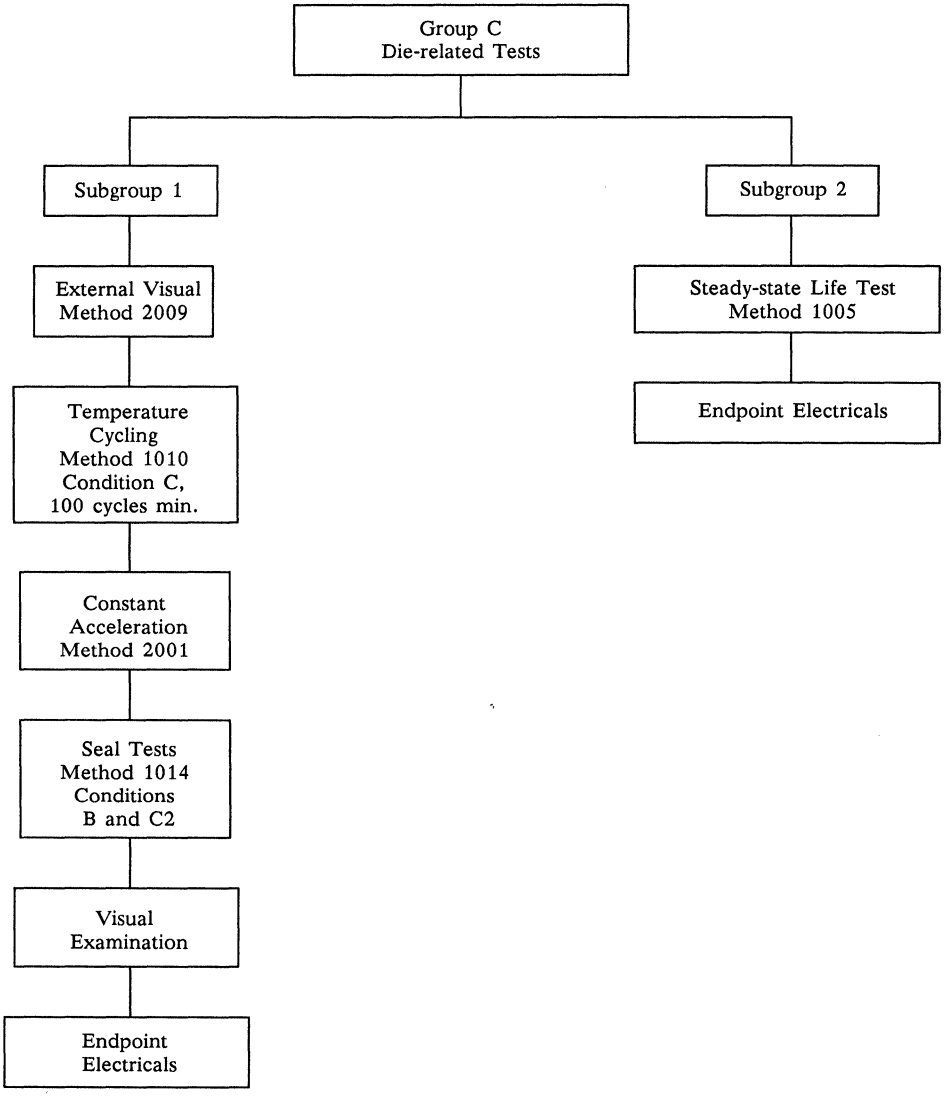


MIL-STD-883, Class B, M5010, Quality Conformance Inspection - Group B

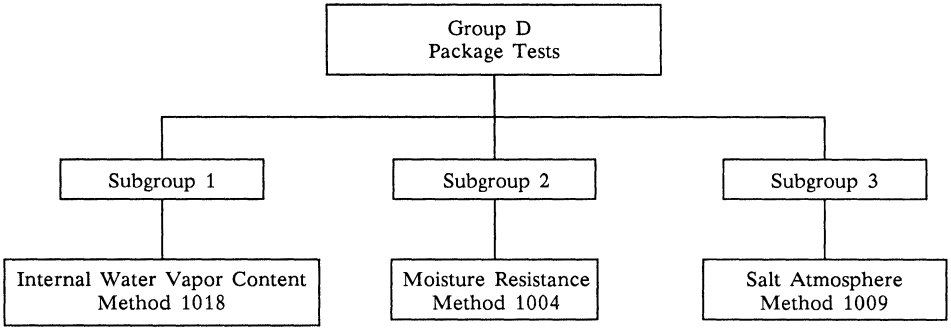


5

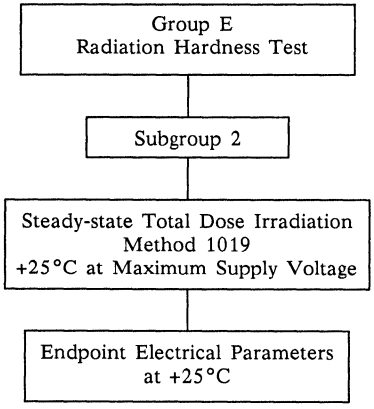
MIL-STD-883, Class B, M5010, Quality Conformance Inspection - Group C



MIL-STD-883, Class B, M5010, Quality Conformance Inspection - Group D

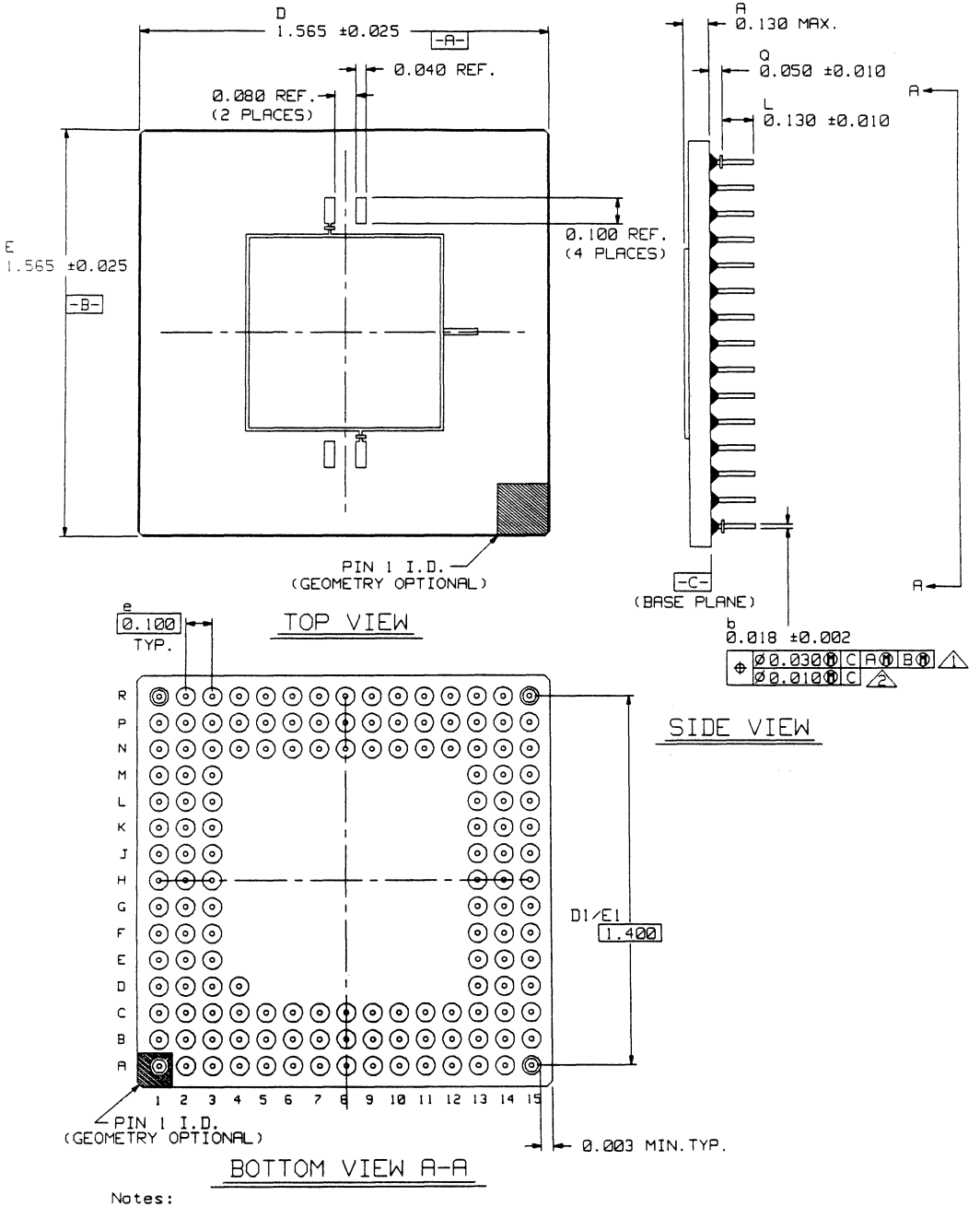


MIL-STD-883, Class B, M5005 and M5010, Quality Conformance Inspection - Group E



Package Selection Guide

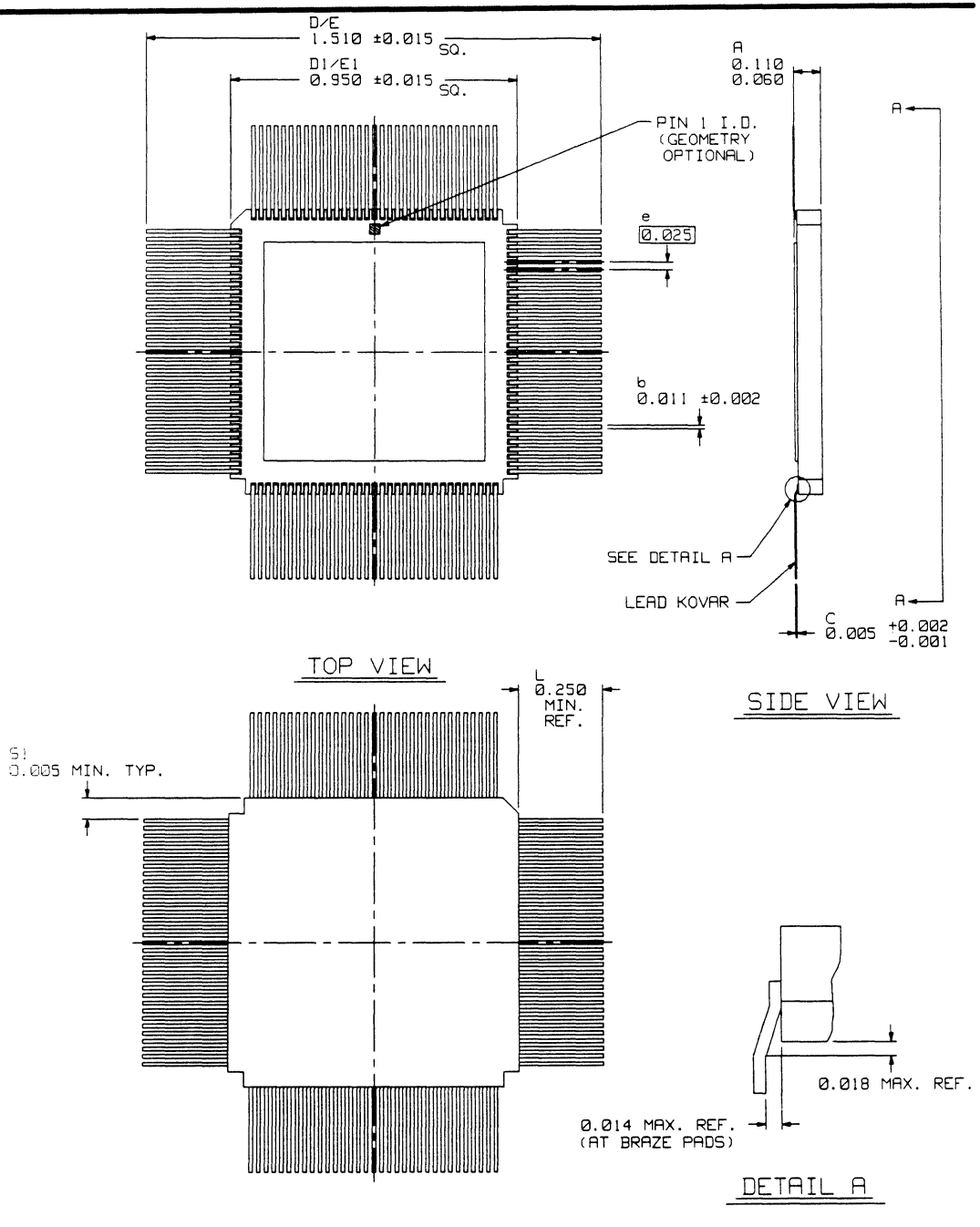
Package	Product							
	RTI	**RTMP**	**RTR**	**BCRT**	**BCRTM**	**BCRTMP**	**RTS**	**XCVR**
24-pin DIP (single cavity)								X
36-pin DIP (dual cavity)								X
68-pin PGA			X				X	
84-pin PGA	X	X		X	X			
144-pin PGA						X		
68-lead LCC			X					
84-lead LCC	X	X		X	X		X	
36-lead FP (dual cavity) (50-mil ctr)								X
84-lead FP	X			X	X			
84-lead FP		X						
132-lead FP						X		



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

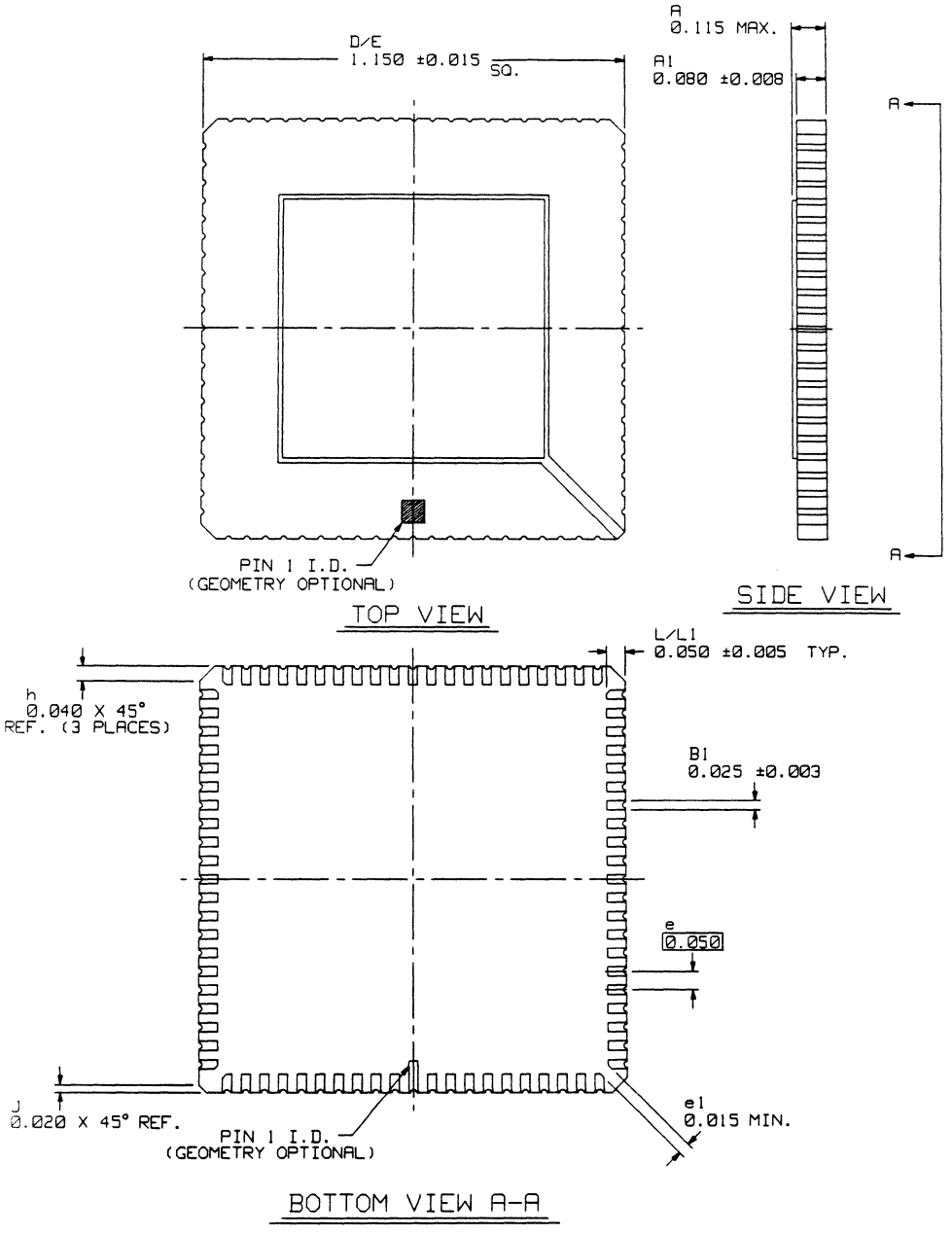
144-pin Pingrid Array



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

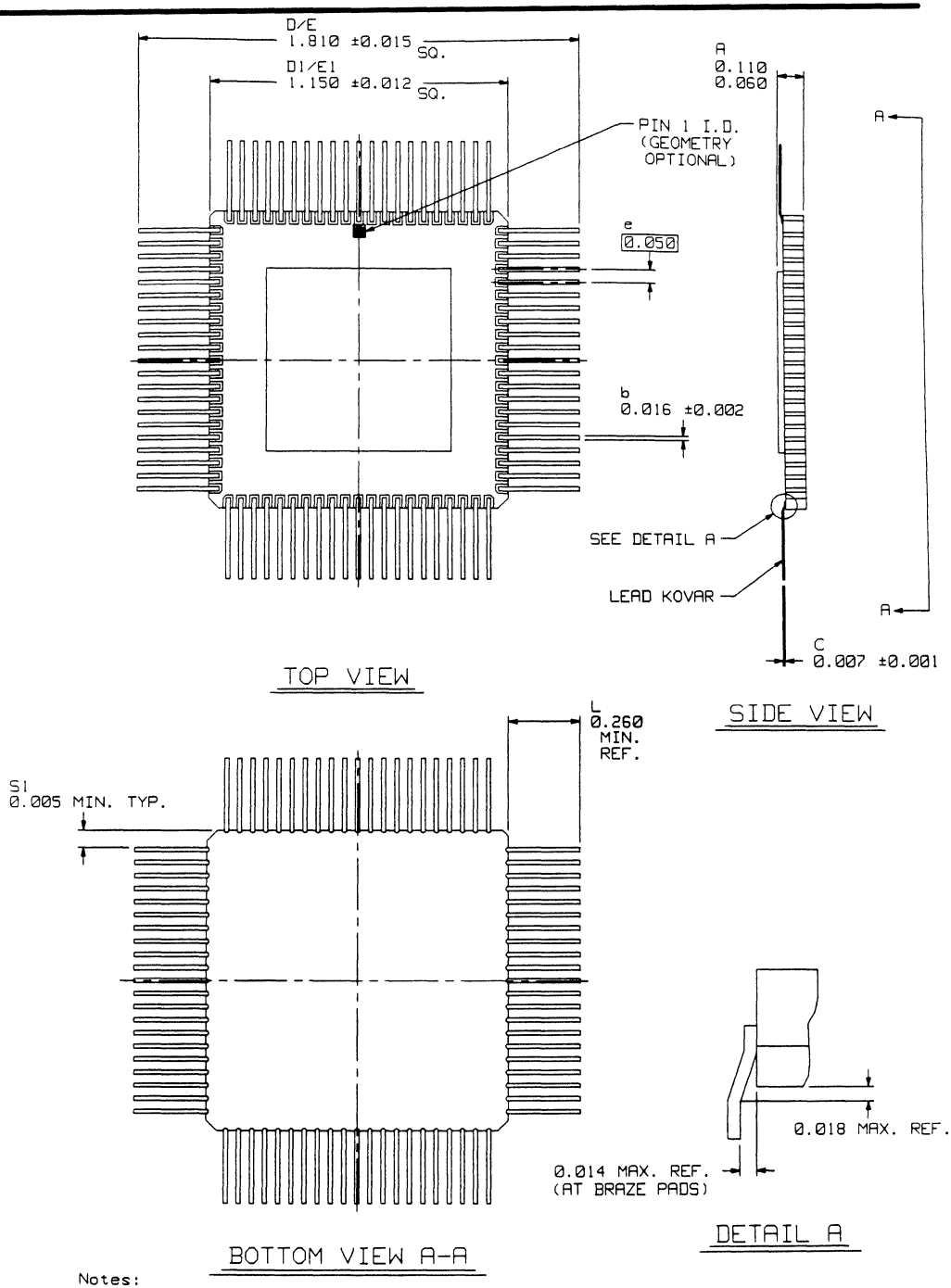
132-lead Flatpack
(25-MIL lead spacing)



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

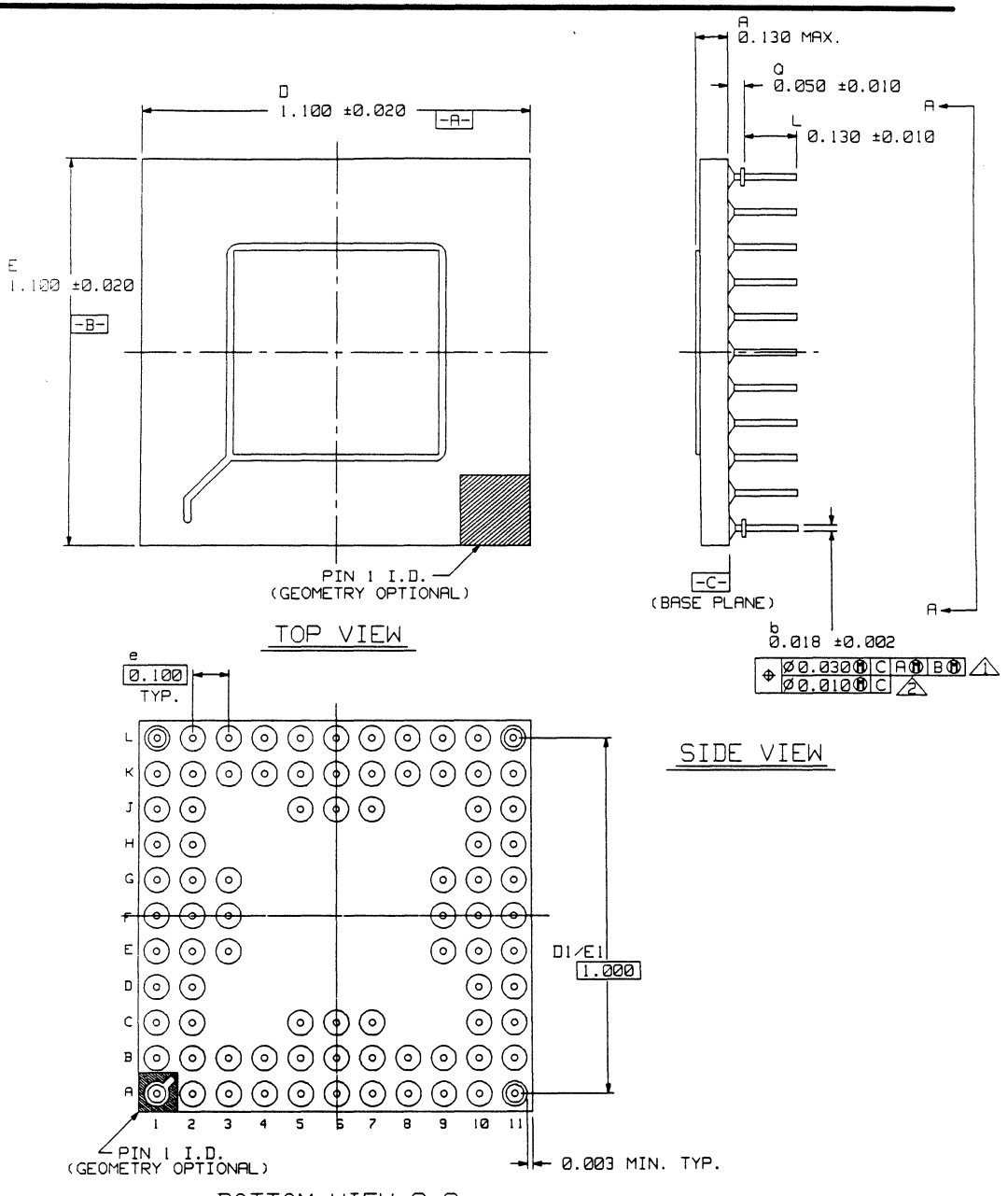
84-LCC



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

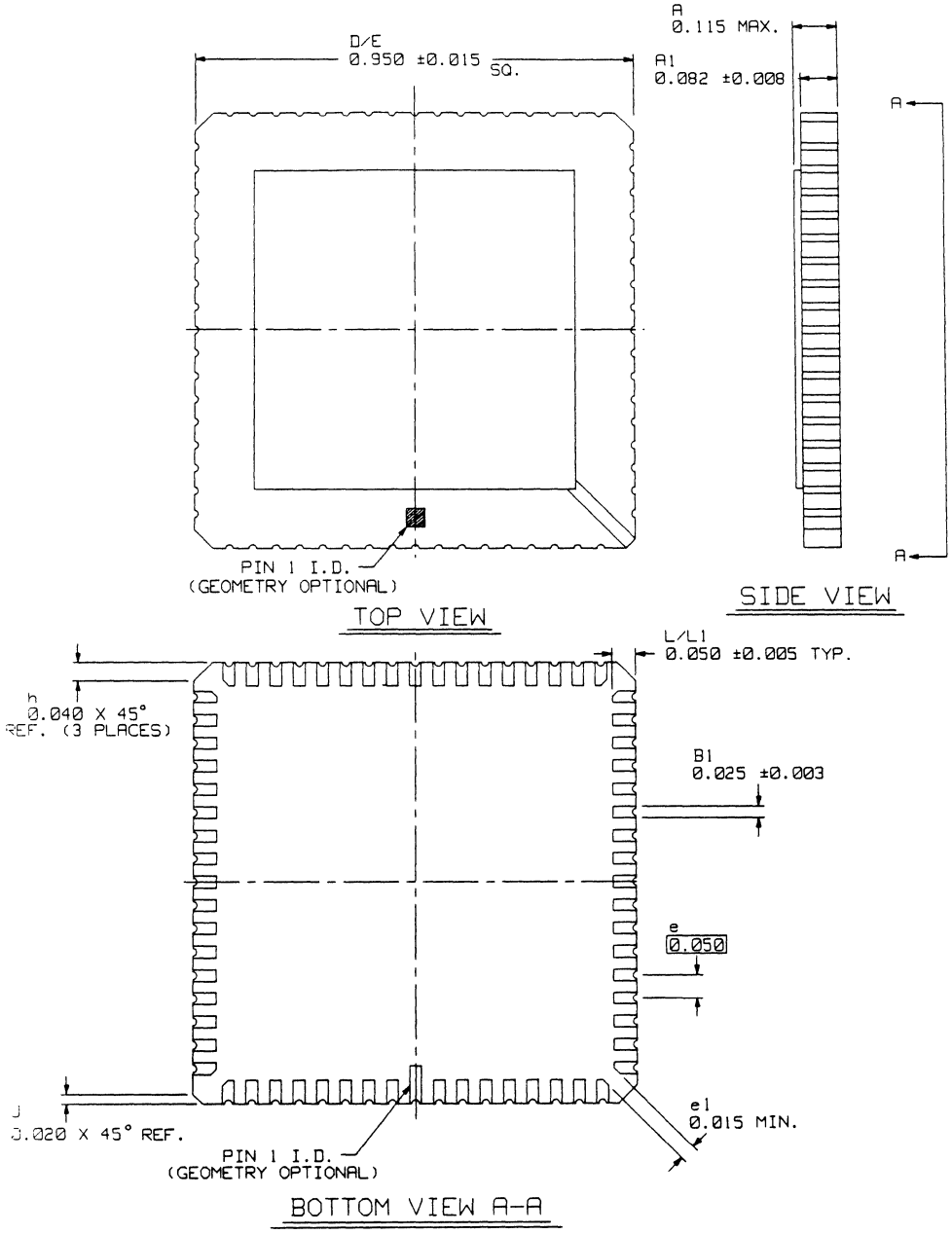
84-lead Flatpack
(50-MIL lead spacing)



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

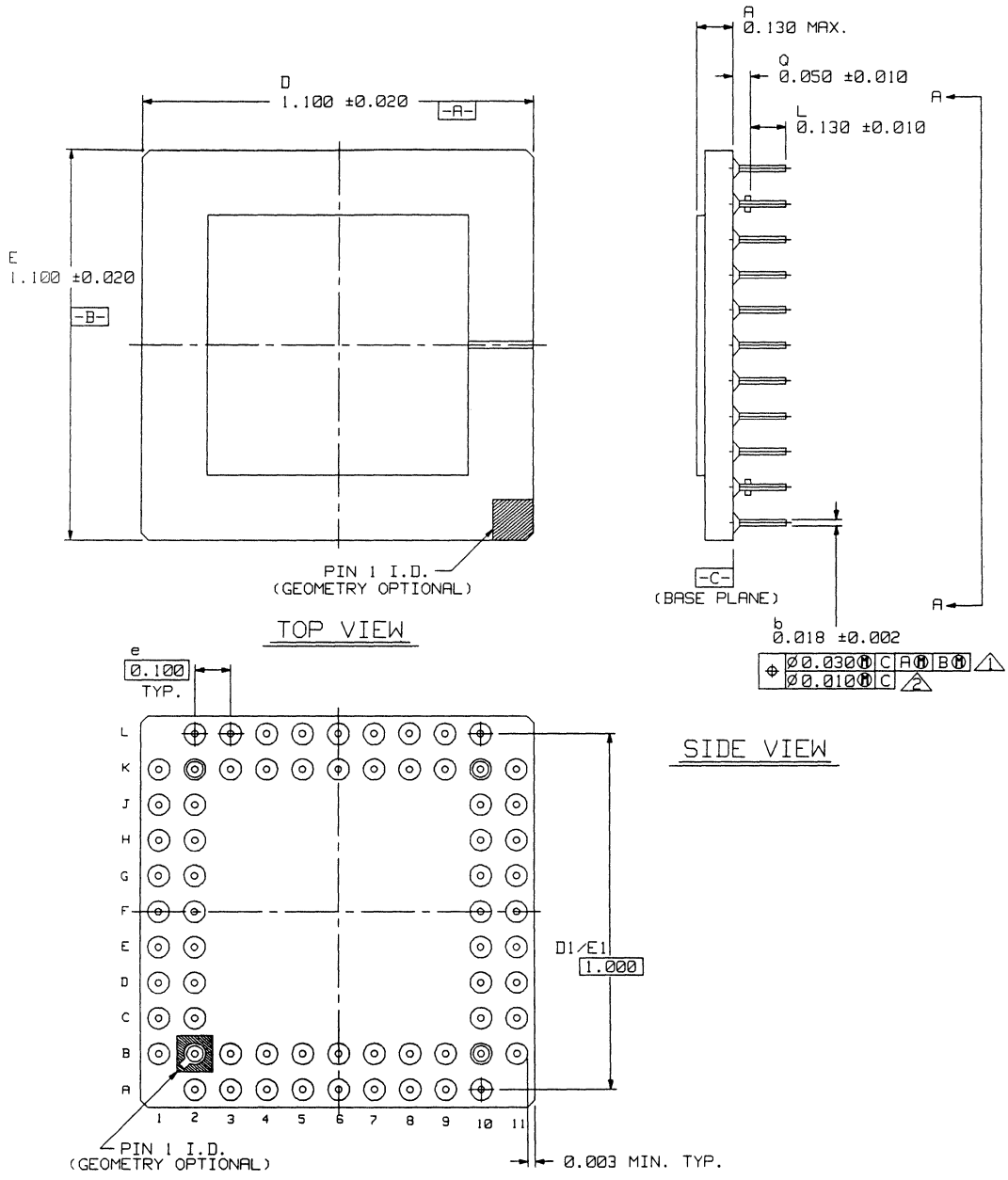
84-pin Pingrid Array



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

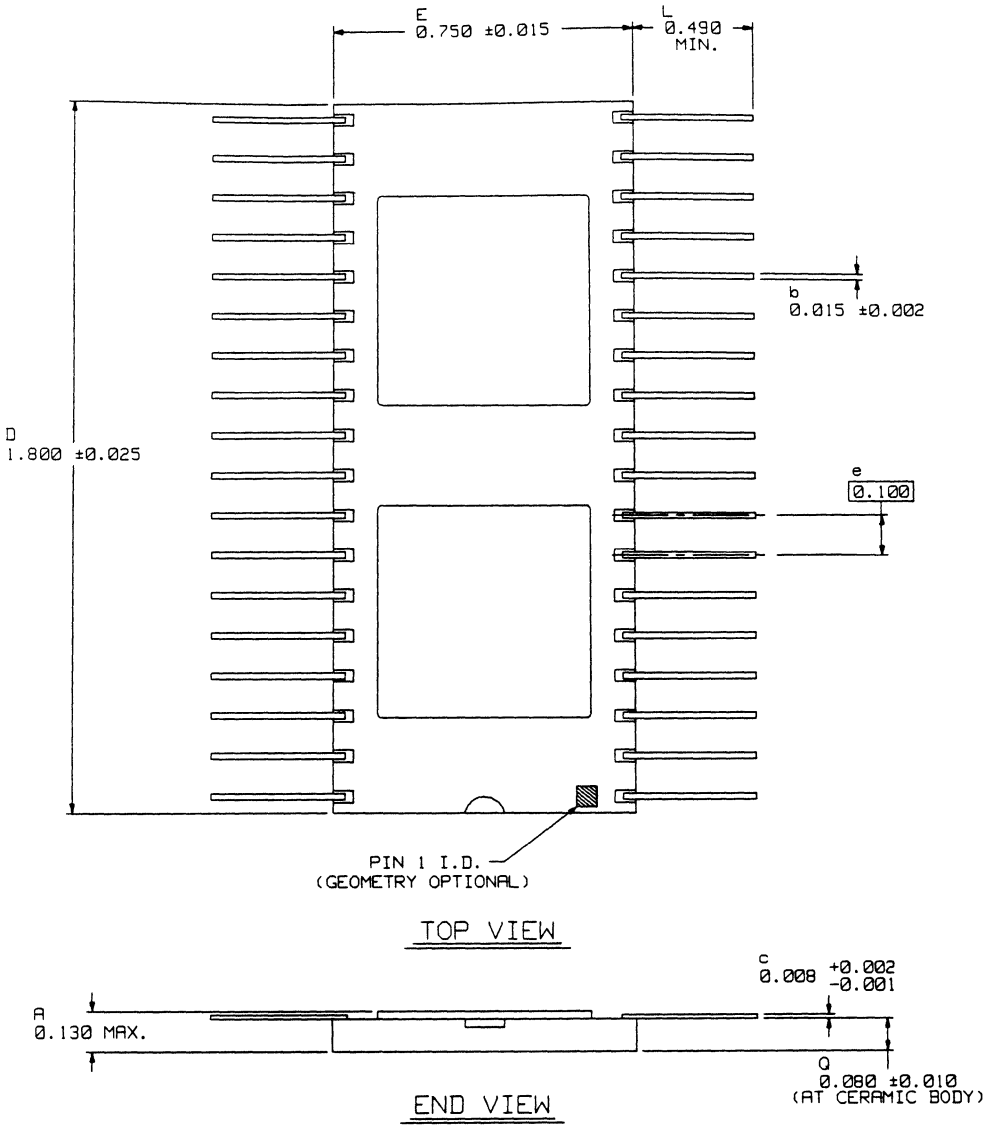
68-LCC



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

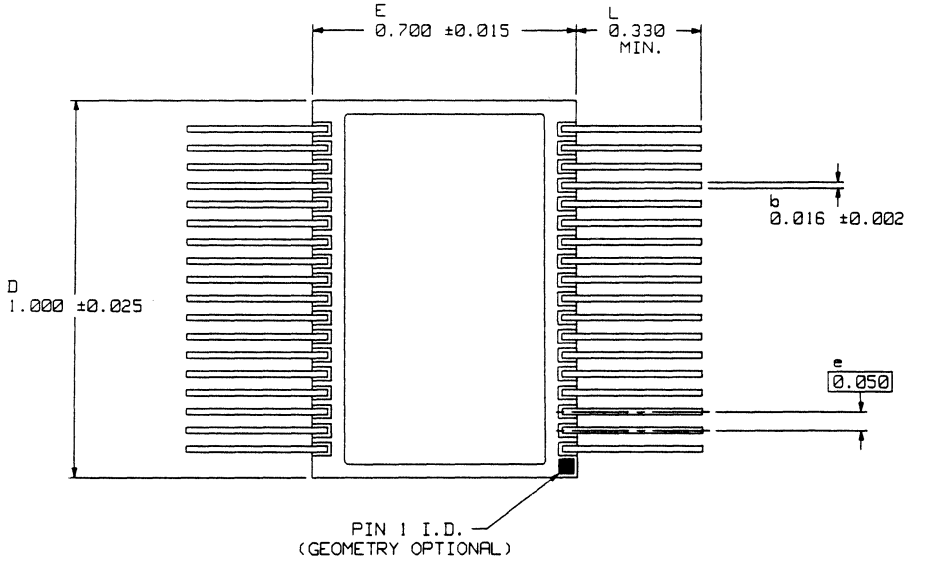
68-pin Pingrid Array



Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

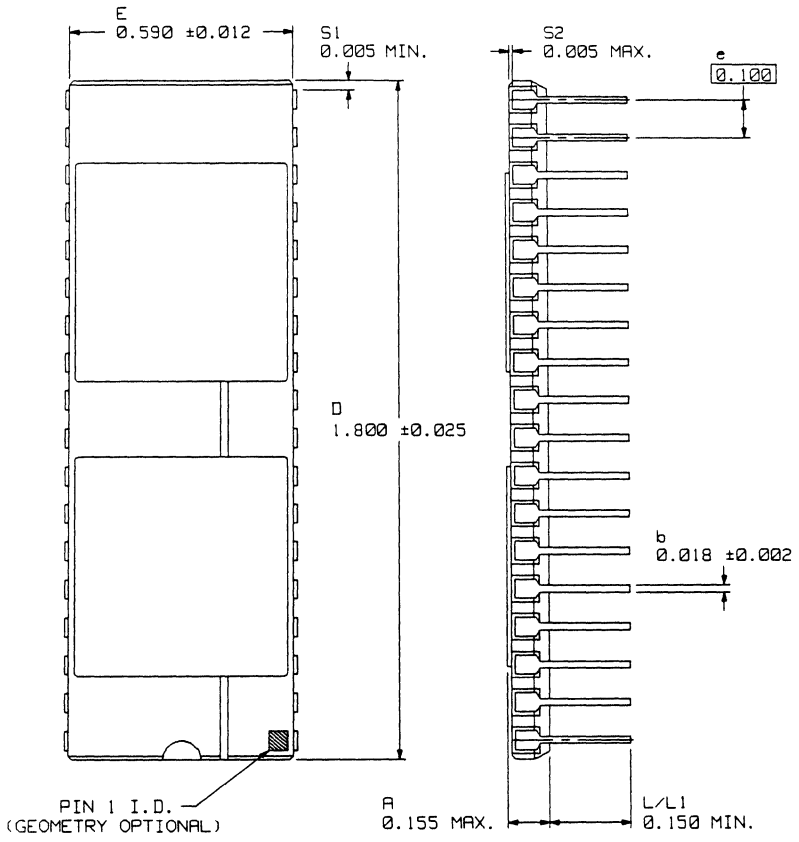
36-lead Flatpack, Dual Cavity
(100-MIL lead spacing)



Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

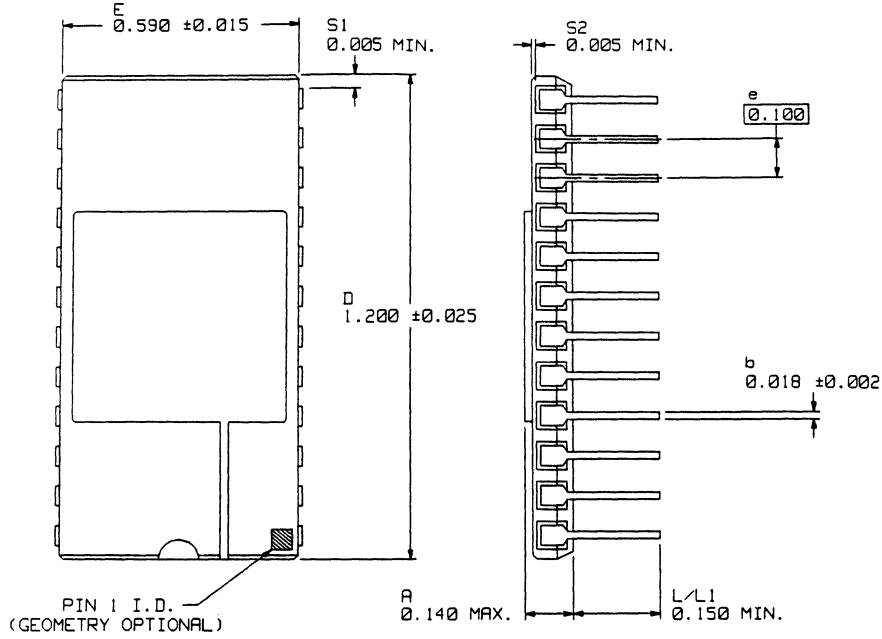
36-lead Flatpack, Dual Cavity
(50-MIL lead spacing)

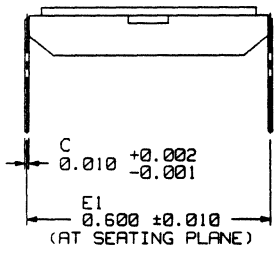


Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

36-lead size-brazed DIP, Dual Cavity





Notes:

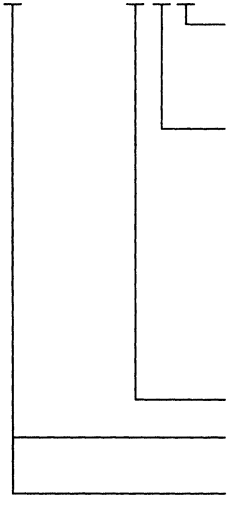
1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

24-lead size-brazed DIP, Dual Cavity

JAN/SMD Product Ordering Information

To order a UTMC JAN or SMD product, please refer to the following information.

DRAWING NUMBER ** * *



LEAD FINISH:
X=Any
A=Solder
C=Gold

CASE OUTLINE:
JAN:
Z=PGA
X=LCC
Y=FP

SMD (refer to specification):
X=PGA, 36 DIP
Z=LCC, 36 FP (50 mil)
Y=FP, 36 FP (100 mil)
U=24 DIP

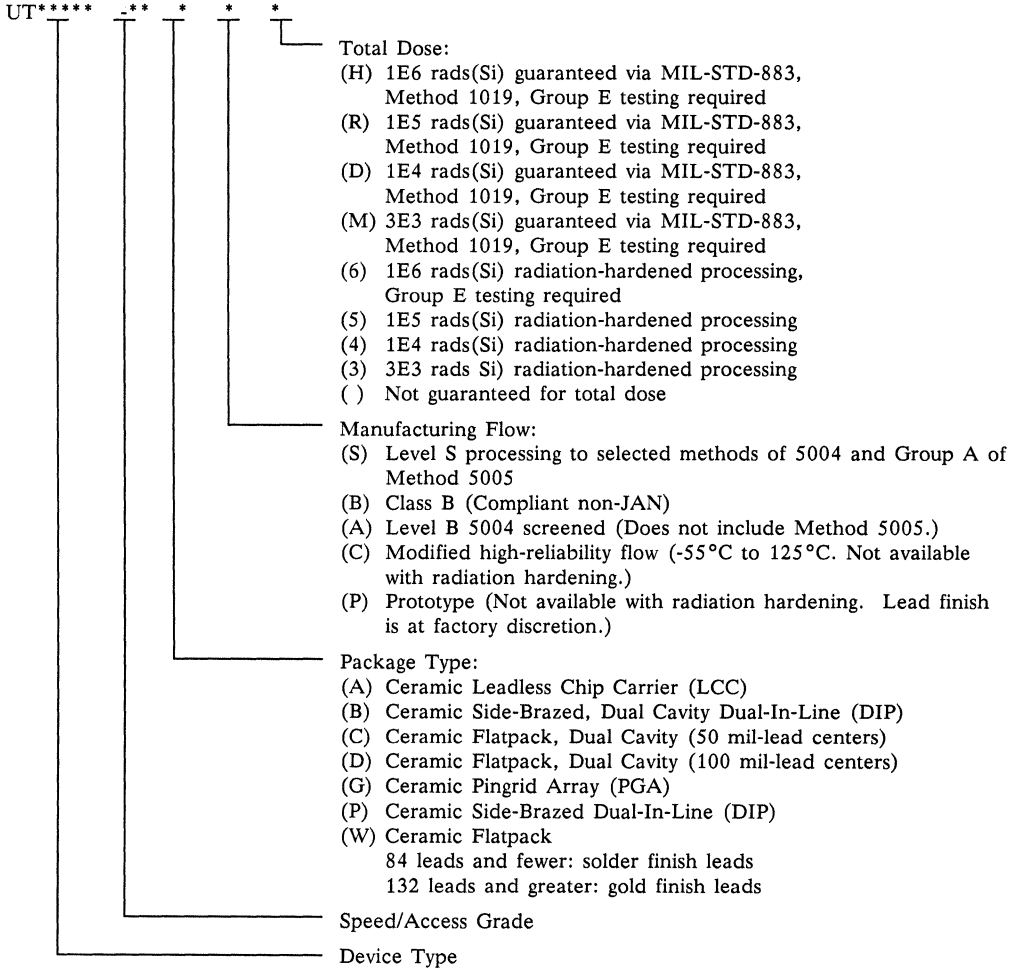
DEVICE TYPE--refer to specification

JAN:
38510/555 = UT1553B RTI

SMD:
5962-88645 =UT1553 RTMP
5962-89576 =UT1553B RTR
5962-89575 =UT1760A RTS
5962-88628 =UT1553B BCRT
5962-89577 =UT1553B BCRTM
5962-89501 =UT1553 BCRTMP
5962-88644 =UT63M1xx XCVR

UTMC Standard Product Ordering Information

To order a UTMC standard product, please refer to the following information.



UTMC Sales Offices

Colorado Springs Sales Office
1575 Garden of the Gods Road
Colorado Springs, CO 80907-3486
719-594-8060
FAX 719-594-8486

Annapolis Sales Office
932 Barracuda Cove Ct.
Annapolis, MD 21401
301-626-8690
FAX 301-626-8692

Orlando Sales Office
One Harbor Place
1901 S. Harbor City Blvd., Suite 636
Melbourne, FL 32901
407-951-4164
FAX 407-951-4254

South LA Sales Office
23422 Mill Creek Drive, Suite 215
Laguna Hills, CA 92653
714-830-1177
FAX 714-830-0880

North LA Sales Office
20750 Ventura Blvd., Suite 300
Woodland Hills, CA 91264
818-992-5399
FAX 818-992-1422

Boston Sales Office
1000 Winter Street, Suite 4550
Waltham, MA 02154
617-890-8862
FAX 617-890-7865

Dallas Sales Office
2350 Lakeside Blvd., Suite 850
Richardson, TX 75082
214-480-9949
FAX 214-480-8234

In addition to our Sales Offices, UTMC has a field sales representative force that you may contact for product or ordering information. Please contact your nearest sales office or the factory directly at 1-800-722-1575.

A

MIL-STD-1553B
21 September 1978
SUPERSEDING
MIL-STD-1553A
30 April 1975

MILITARY STANDARD

AIRCRAFT INTERNAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS

A

FSC MISC

DEPARTMENT OF DEFENSE
Washington D.C. 20360

Aircraft Internal Time Division Command/Response Multiplex Data Bus

MIL-STD-1553B

1. This Military Standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Aeronautical Systems Division, Attn: ENA1, Wright-Patterson Air Force Base 45433, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

This standard contains requirements for aircraft internal time division command/response multiplex data bus techniques which will be utilized in systems integration of aircraft subsystems. Even with the use of this standard, subtle differences will exist between multiplex data buses used on different aircraft due to particular aircraft mission requirements and the designer options allowed in this standard. The system designer must recognize this fact and design the multiplex bus controller hardware and software to accommodate such differences. These designer-selected options must exist, so as to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architecture redundancy, degradation concept and traffic patterns peculiar to the specific aircraft mission requirements.

CONTENTS

CONTENTS (Cont'd)

CONTENTS (Cont'd)

CONTENTS (Cont'd)

A

1. SCOPE

1.1 Scope. This standard establishes requirements for digital, command/response, time division multiplexing (Data Bus) techniques on aircraft. It encompasses the data bus line and its interface electronics illustrated on figure 1, and also defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed.

1.2 Application. When invoked in a specification or statement of work, these requirements shall apply to the multiplex data bus and associated equipment which is developed either alone or as a portion of an aircraft weapon system or subsystem development. The contractor is responsible for invoking all the applicable requirements of this Military Standard on any and all subcontractors he may employ.

2. REFERENCED DOCUMENTS

2.1 Issue of document. The following document, of the issue in effect on date of invitation for bid or request for proposal, forms a part of the standard to the extent specified herein.

SPECIFICATION

MILITARY

MIL-E-6051 Electromagnetic Compatibility Requirements, Systems

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. DEFINITIONS

3.1 Bit. Contraction of binary digit: may be either zero or one. In information theory a binary digit is equal to one binary decision or the designation of one of two possible values or states of anything used to store or convey information.

3.2 Bit rate. The number of bits transmitted per second.

3.3 Pulse code modulation (PCM). The form of modulation in which the modulation signal is sampled, quantized, and coded so that each element of information consists of different types or numbers of pulses and spaces.

3.4 Time division multiplexing (TDM). The transmission of information from several signal sources through one communication system with different signal samples staggered in time to form a composite pulse train.

3.5 Half duplex. Operation of a data transfer system in either direction over a single line, but not in both directions on that line simultaneously.

3.6 Word. In this document a word is a sequence of 16 bits plus sync and parity. There are three types of words: command, status and data.

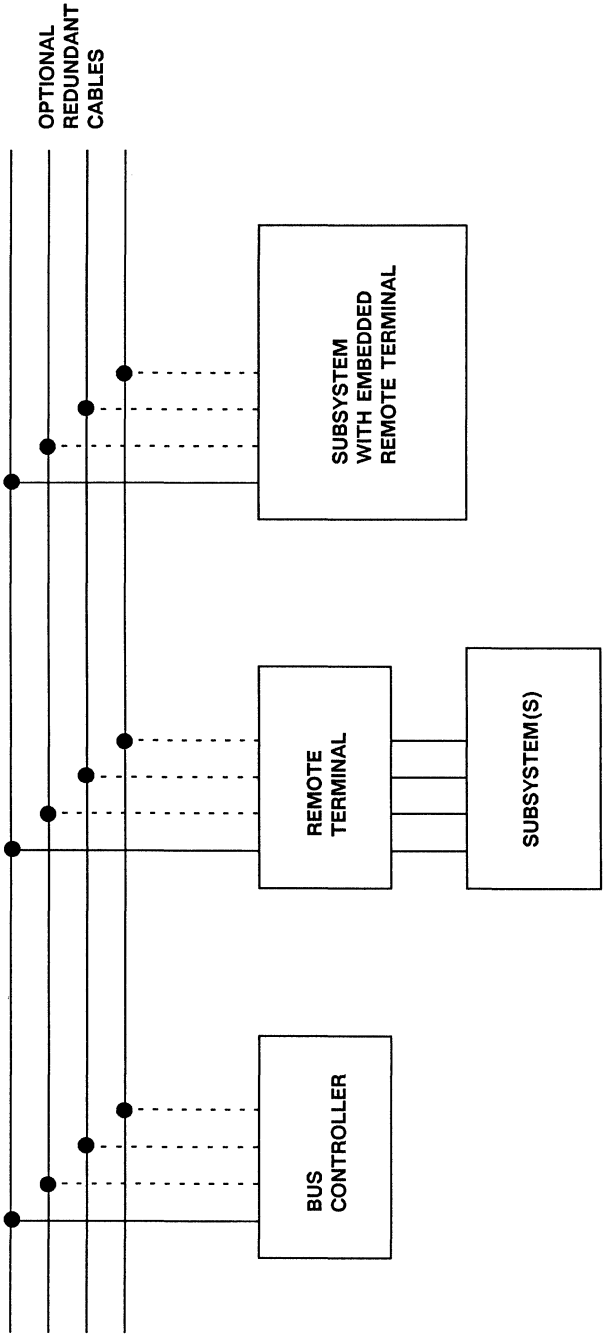


Figure 1. Sample multiplex data bus architecture.

3.7 Message. A single message is the transmission of a command word, status word, and data words if they are specified. For the case of a remote terminal to remote terminal (RT to RT) transmission, the message shall include the two command words, the two status words, and data words.

3.8 Subsystem. The device or functional unit receiving data transfer service from the data bus.

3.9 Data bus. Whenever a data bus or bus is referred to in this document it shall imply all the hardware including twisted shielded pair cables, isolation resistors, transformers, etc., required to provide a single data path between the bus controller and all the associated remote terminals.

3.10 Terminal. The electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate line replaceable units (LRU's) or be contained within the elements of the subsystem.

3.11 Bus controller. The terminal assigned the task of initiating information transfers on the data bus.

3.12 Bus monitor. The terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time.

3.13 Remote terminal (RT). All terminals not operating as the bus controller or as a bus monitor.

3.14 Asynchronous operation. For the purpose of this standard, asynchronous operation is the use of an independent clock source in each terminal for message transmission. Decoding is achieved in receiving terminals using clock information derived from the message.

3.15 Dynamic bus control. The operation of a data bus system in which designated terminals are offered control of the data bus.

3.16 Command/Response. Operation of a data bus system such that remote terminals receive and transmit data only when commanded to do so by the bus controller.

3.17 Redundant data bus. The use of more than one data bus to provide more than one data path between the subsystems, i.e., dual redundant data bus, tri-redundant data bus, etc.

3.18 Broadcast. Operation of a data bus system such that information transmitted by the bus controller or a remote terminal is addressed to more than one of the remote terminals connected to the data bus.

3.19 Mode code. A means by which the bus controller can communicate with the multiplex bus-related hardware, in order to assist in the management of information flow.

A

4. GENERAL REQUIREMENTS

4.1 Test and operating requirements. All requirements as specified herein shall be valid over the environmental conditions which the multiplex data bus system shall be required to operate.

4.2 Data bus operation. The multiplex data bus system in its most elemental configuration shall be as shown on figure 1. The multiplex data bus system shall function asynchronously in a command/response mode, and transmission shall occur in a half-duplex manner. Sole control of information transmission on the bus shall reside with the bus controller, which shall initiate all transmissions. The information flow on the data bus shall be comprised of messages which are, in turn, formed by three types of words (command, data, and status) as defined in 4.3.3.5.

4.3 Characteristics.

4.3.1 Data form. Digital data may be transmitted in any desired form, provided that the chosen form shall be compatible with the message and word formats defined in this standard. Any unused bit positions in a word shall be transmitted as logic zeros.

4.3.2 Bit priority. The most significant bit shall be transmitted first with the less significant bits following in descending order of value in the data word. The number of bits required to define a quantity shall be consistent with the resolution or accuracy required. In the event that multiple precision quantities (information accuracy or resolution requiring more than 16 bits) are transmitted, the most significant bits shall be transmitted first, followed by the word(s) containing the lesser significant bits in numerical descending order. Bit packing of multiple quantities in a single data word is permitted.

4.3.3 Transmission method.

4.3.3.1 Modulation. The signal shall be transferred over the data bus in serial digital pulse code modulation form.

4.3.3.2 Data code. The data code shall be Manchester II bi-phase level. A logic one shall be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero shall be a bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time (see figure 2).

4.3.3.3 Transmission bit rate. The transmission bit rate on the bus shall be 1.0 megabit per second with a combined accuracy and long-term stability of +/- 0.1 percent (i.e., +/- 1000 Hertz (Hz)). The short-term stability (i.e., stability over 1.0 second interval) shall be at least 0.01 percent (i.e., +/- 100 Hz).

4.3.3.4 Word size. The word size shall be 16 bits plus the sync waveform and the parity bit for a total of 20 bits times as shown on figure 3.

4.3.3.5 Word formats. The word formats shall be as shown on figure 3 for the command, data, and status words.

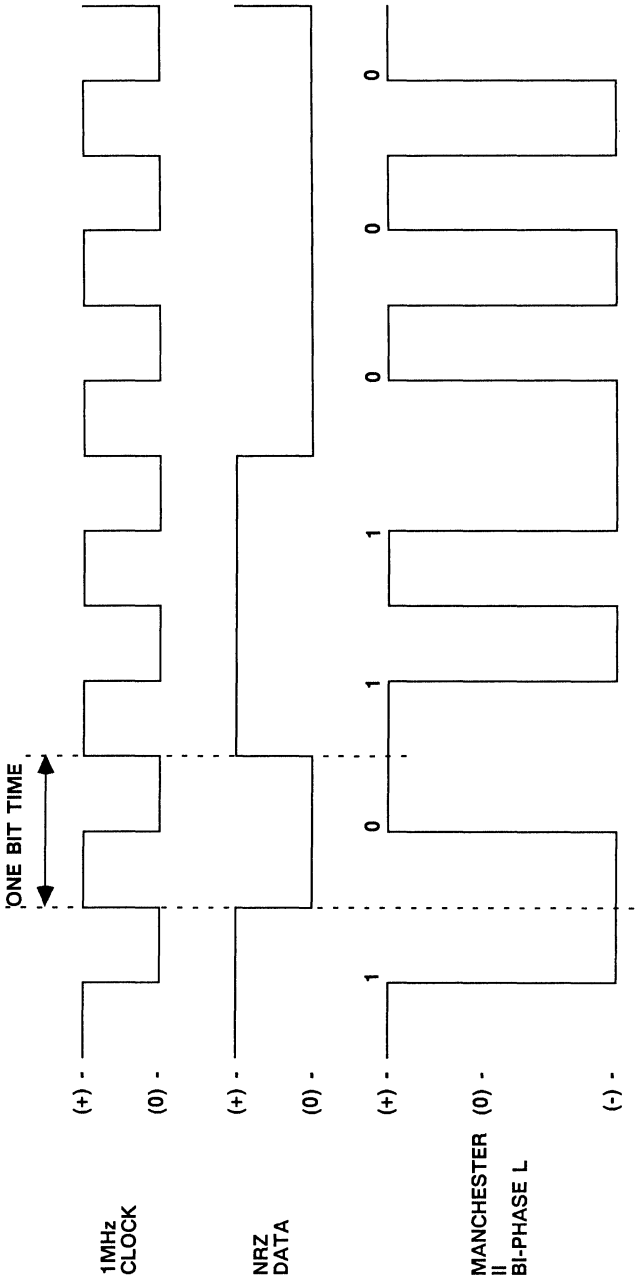
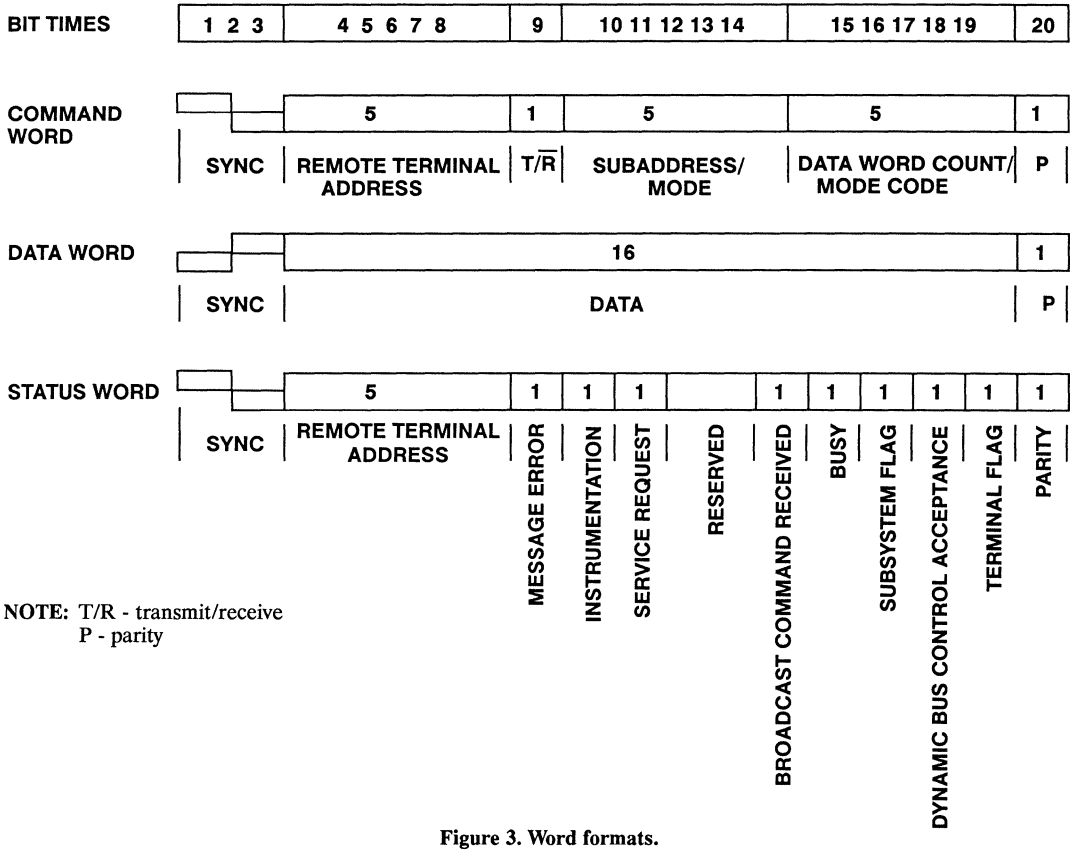


Figure 2. Data encoding.



NOTE: T/R - transmit/receive
P - parity

Figure 3. Word formats.

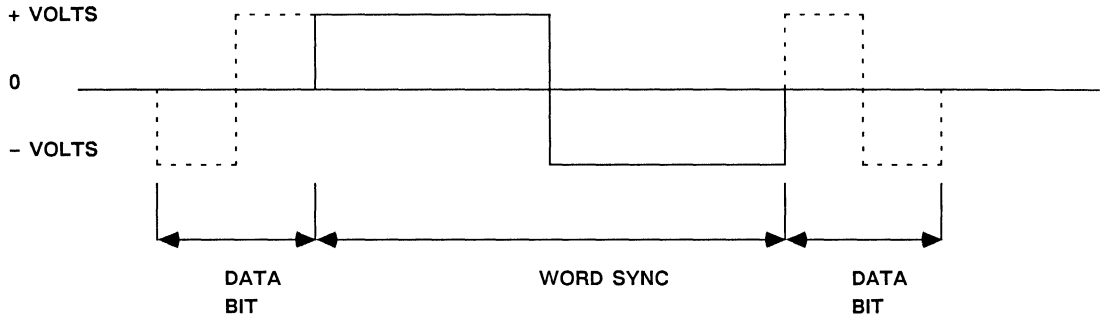


Figure 4. Command and status word sync.

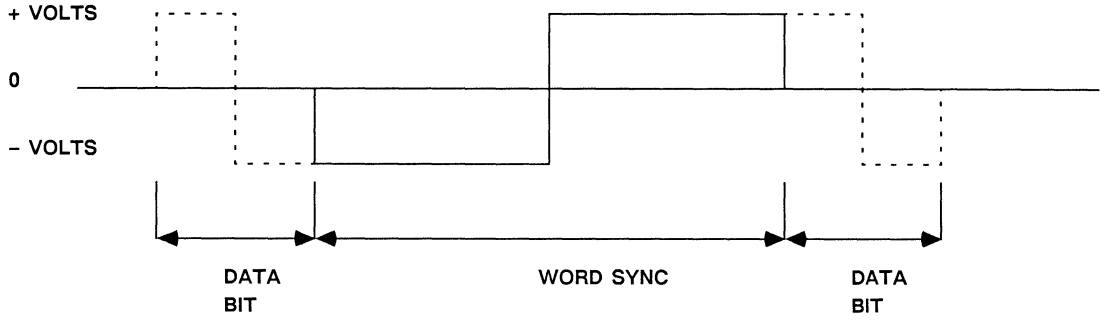


Figure 5. Data word sync.

4.3.3.5.1 Command word. A command word shall be comprised of a sync waveform, remote terminal address field, transmit/receive (T/R) bit, subaddress/mode field, word count/mode code field, and a parity (P) bit (see figure 3).

4.3.3.5.1.1 Sync. The command sync waveform shall be an invalid Manchester waveform as shown on figure 4. The width shall be three bit times, with the sync waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half bit times. If the next bit following the sync waveform is a logic zero, then the last half of the sync waveform will have an apparent width of two clock periods due to the Manchester encoding.

4.3.3.5.1.2 Remote terminal address. The next five bits following the sync shall be the RT address. Each RT shall be assigned a unique address. Decimal address 31 (11111) shall not be assigned as a unique address. In addition to its unique address, a RT shall be assigned decimal address 31 (11111) as the common address, if the broadcast option is used.

4.3.3.5.1.3 Transmit/receive. The next bit following the remote terminal address shall be the T/R bit, which shall indicate the action required of the RT. A logic zero shall indicate the RT is to receive, and a logic one shall indicate the RT is to transmit.

4.3.3.5.1.4 Subaddress/mode. The next five bits following the R/T bit shall be utilized to indicate an RT subaddress or use of mode control, as is dictated by the individual terminal requirements. The subaddress/mode values of 00000 and 11111 are reserved for special purposes, as specified in 4.3.3.5.1.7, and shall not be utilized for any other function.

4.3.3.5.1.5 Data word count/mode code. The next five bits following the subaddress/mode field shall be the quantity of data words to be either sent out or received by the RT or the optional mode code as specified in 4.3.3.5.1.7. A maximum of 32 data words may be transmitted or received in any one message block. All 1's shall indicate a decimal count of 31, and all 0's shall indicate a decimal count of 32.

4.3.3.5.1.6 Parity. The last bit in the word shall be used for parity over the preceding 16 bits. Odd parity shall be utilized.

4.3.3.5.1.7 Optional mode control. For RT's exercising this option a subaddress/mode code of 00000 or 11111 shall imply that the contents of the data word count/mode code field are to be decoded as a five bit mode command. The mode code shall only be used to communicate with the multiplex bus related hardware, and to assist in the management of information flow, and not to extract data from or feed data to a functional subsystem. Codes 00000 through 01111 shall only be used for mode codes which do not require transfer of a data word. For these codes, the T/R bit shall be set to 1. Codes 10000 through 11111 shall only be used for mode codes which require transfer of a single data word. For these mode codes, the T/R bit shall indicate the direction of data word flow as specified in 4.3.3.5.1.3. No multiple data word transfer shall be implemented with any mode code. The mode codes are reserved for the specific functions as specified in table I and shall not be used for any other purpose. If the designer chooses to implement any of these functions, the specific codes, T/R bit assignments, and use of a data word, shall be used as indicated. The use of the broadcast command option shall only be applied to particular mode codes as specified in table I.

4.3.3.5.1.7.1 Dynamic bus control. The controller shall issue a transmit command to an RT capable of performing the bus control function. This RT shall respond with a status word as specified in 4.3.3.5.3. Control of the data bus passes from the offering bus controller to the accepting RT upon completion of the transmission of the status word by the RT. If the RT rejects control of the data bus, the offering bus controller retains control of the data bus.

4.3.3.5.1.7.2 Synchronize (without data word). This command shall cause the RT to synchronize (e.g., to reset the internal timer, to start a sequence, etc.). The RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.3 Transmit status word. This command shall cause the RT to transmit the status word associated with the last valid command word preceding this command. This mode command shall not alter the state of the status word.

4.3.3.5.1.7.4 Initiate self-test. This command shall be used to initiate self-test within the RT. The RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.5 Transmitter shutdown. This command (to only be used with dual redundant bus systems) shall cause the RT to disable the transmitter associated with the redundant bus. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3 after this command.

4.3.3.5.1.7.6 Override transmitter shutdown. This command (to only be used with dual redundant bus system) shall cause the RT to enable a transmitter which was previously disabled. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3 after this command.

4.3.3.5.1.7.7 Inhibit terminal flag (T/F) bit. This command shall cause the RT to set the T/F bit in the status word specified in 4.3.3.5.3 to logic zero until otherwise commanded. The RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.8 Override inhibit T/F bit. This command shall cause the RT to override the inhibit T/F bit specified in 4.3.3.5.1.7.7. The RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.9 Reset remote terminal. This command shall be used to reset the RT to a power up initialized state. The RT shall first transmit its status word, and then reset.

4.3.3.5.1.7.10 Reserved mode codes (01001 to 01111). These mode codes are reserved for future use and shall not be used.

A

TABLE I. Assigned mode codes

T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	Override Inhibit Terminal Flag Bit	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	Transmit BIT Word	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

NOTE: To be determined (TBD)

4.3.3.5.1.7.11 Transmit vector word. This command shall cause the RT to transmit a status word as specified in 4.3.3.5.3 and a data word containing service request information.

4.3.3.5.1.7.12 Synchronize (with data word). The RT shall receive a command word followed by a data word as specified in 4.3.3.5.2. The data word shall contain synchronization information for the RT. After receiving the command and data word, the RT shall transmit the status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.13 Transmit last command word. This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word which contains bits 4-19 of the last command word, excluding a transmit last command word mode code received by the RT. This mode command shall not alter the state of the RT's status word.

4.3.3.5.1.7.14 Transmit built-in-test (BIT) word. This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word containing the RT BIT data. This function is intended to supplement the available bits in the status word when the RT hardware is sufficiently complex to warrant its use. The data word, containing the RT BIT data, shall not be altered by the reception of a transmit last command or a transmit status word mode code. This function shall not be used to convey BIT data from the associated subsystem(s).

4.3.3.5.1.7.15 Selected transmitter shutdown. This command shall cause the RT to disable the transmitter associated with a specified redundant data bus. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be disabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.16 Override selected transmitter shutdown. This command shall cause the RT to enable a transmitter which was previously disabled. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be enabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3.

4.3.3.5.1.7.17 Reserved mode codes (10110 to 11111). These mode codes are reserved for future use and shall not be used.

4.3.3.5.2 Data word. A data word shall be comprised of a sync waveform, data bits, and a parity bit (see figure 3).

4.3.3.5.2.1 Sync. The data sync waveform shall be invalid Manchester waveform as shown on figure 5. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit times.

A

4.3.3.5.2.2 Data. The sixteen bits following the sync shall be utilized for data transmission as specified in 4.3.2.

4.3.3.5.2.3 Parity. The last bit shall be utilized for parity as specified in 4.3.3.5.1.6.

4.3.3.5.3 Status word. A status word shall be comprised of a sync waveform, RT address, message error bit, instrumentation bit, service request bit, three reserved bits, broadcast command received bit, busy bit, subsystem flag bit, dynamic bus control acceptance bit, terminal flag bit, and a parity bit. For optional broadcast operation, transmission of the status word shall be suppressed as specified in 4.3.3.6.7.

4.3.3.5.3.1 Sync. The status sync waveform shall be as specified in 4.3.3.5.1.1.

4.3.3.5.3.2 RT address. The next five bits following the sync shall contain the address of the RT which is transmitting the status word as defined in 4.3.3.5.1.2.

4.3.3.5.3.3 Message error bit. The status word bit at bit time nine (see figure 3) shall be utilized to indicate that one or more of the data words associated with the preceding receive command word from the bus controller has failed to pass the RT's validity tests as specified in 4.4.1.1. This bit shall also be set under the conditions specified in 4.4.1.2, 4.4.3.4 and 4.4.3.6. A logic one shall indicate the presence of a message error, and a logic zero shall show its absence. All RT's shall implement the message error bit.

4.3.3.5.3.4 Instrumentation bit. The status word at bit time ten (see figure 3) shall be reserved for the instrumentation bit and shall always be a logic zero. This bit is intended to be used in conjunction with a logic one in bit time ten of the command word to distinguish between a command word and a status word. The use of the instrumentation bit is optional.

4.3.3.5.3.5 Service request bit. The status word bit at bit time eleven (see figure 3) shall be reserved for the service request bit. The use of this bit is optional. This bit, when used, shall indicate the need for the bus controller to take specific predefined actions relative to either the RT or associated subsystem. Multiple subsystems, interfaced to a single RT, which individually require a service request signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific requesting subsystem. The service request bit is intended to be used only to trigger data transfer operations which take place on an exception rather than periodic basis. A logic one shall indicate the presence of a service request, and a logic zero its absence. If this function is not implemented, the bit shall be set to zero.

4.3.3.5.3.6 Reserved status bits. The status word bits at bit times twelve through fourteen are reserved for future use and shall not be used. These bits shall be set to a logic zero.

4.3.3.5.3.7 Broadcast command received bit. The status word at bit time fifteen shall be set to a logic one to indicate that the preceding valid command word was a broadcast command and a logic zero shall show it was not a broadcast command. If the broadcast command option is not used, this bit shall be set to a logic zero.

4.3.3.5.3.8 Busy bit. The status word bit at bit time sixteen (see figure 3) shall be reserved for the busy bit. The use of this bit is optional. This bit, when used, shall indicate that the RT or subsystem is unable to move data to or from the subsystem in compliance with the bus controller's command. A logic one shall indicate the presence of a busy condition, and a logic zero its absence. In the event the busy bit is set in response to a transmit command, then the RT shall transmit its status word only. If this function is not implemented, the bit shall be set to logic zero.

4.3.3.5.3.9 Subsystem flag bit. The status word bit at bit time seventeen (see figure 3) shall be reserved for the subsystem flag bit. The use of this bit is optional. This bit, when used, shall flag a subsystem fault condition, and alert the bus controller to potentially invalid data. Multiple subsystems, interfaced to a single RT, which individually require a subsystem flag bit signal, shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific reporting subsystem. A logic one shall indicate the presence of the flag, and a logic zero its absence. If not used, this bit shall be set to logic zero.

4.3.3.5.3.10 Dynamic bus control acceptance bit. The status word bit at bit time eighteen (see figure 3) shall be reserved for the acceptance of dynamic bus control. This bit shall be used if the RT implements the optional dynamic bus control function. This bit, when used, shall indicate acceptance or rejection of a dynamic bus control offer as specified in 4.3.3.5.1.7.1. A logic one shall indicate acceptance of control, and a logic zero shall indicate rejection of control. If this function is not used, this bit shall be set to logic zero.

4.3.3.5.3.11 Terminal flag bit. The status word bit at bit time nineteen (see figure 3) shall be reserved for the terminal flag function. The use of this bit is optional. This bit, when used, shall flag a RT fault condition. A logic one shall indicate the presence of the flag, and a logic zero, its absence. If not used, this bit shall be set to logic zero.

4.3.3.5.3.12 Parity bit. The least significant bit in the status word shall be utilized for parity as specified in 4.3.3.5.1.6.

4.3.3.5.4 Status word reset. The status word bit, with the exception of the address, shall be set to logic zero after a valid command word is received by the RT with the exception as specified in 4.3.3.5.1.7. If the conditions which caused bits in the status word to be set (e.g., terminal flag) continue after the bits are reset to logic zero, then the affected status word bit shall be again set, and then transmitted on the bus as required.

4.3.3.6 Message formats. The messages transmitted on the data bus shall be in accordance with the formats on figure 6 and figure 7. The maximum and minimum response times shall be as stated in 4.3.3.7 and 4.3.3.8. No message formats, other than those defined herein, shall be used on the bus.

A

4.3.3.6.1 Bus controller to remote terminal transfers. The bus controller shall issue a receive command followed by the specified number of data words. The RT shall, after message validation, transmit a status word back to the controller. The command and data words shall be transmitted in a contiguous fashion with no interword gaps.

4.3.3.6.2 Remote terminal to bus controller transfers. The bus controller shall issue a transmit command to the RT. The RT shall, after command word validation, transmit a status word back to the bus controller, followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no interword gaps.

4.3.3.6.3 Remote terminal to remote terminal transfers. The bus controller shall issue a receive command to RT A followed contiguously by a transmit command to RT B. RT B shall, after command validation, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. At the conclusion of the data transmission by RT B, RT A shall transmit a status word within the specified time period.

4.3.3.6.4 Mode command without data word. The bus controller shall issue a transmit command to the RT using a mode code specified in table I. The RT shall, after command word validation, transmit a status word.

4.3.3.6.5 Mode command with data word (transmit). The bus controller shall issue a transmit command to the RT using a mode code specified in table I. The RT shall, after command word validation, transmit a status word followed by one data word. The status word and data word shall be transmitted in a contiguous fashion with no gap.

4.3.3.6.6 Mode command with data word (receive). The bus controller shall issue a receive command to the RT using a mode code specified in table I, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT shall, after command and data word validation, transmit a status word back to the controller.

4.3.3.6.7 Optional broadcast command. See 10.6 for additional information on the use of the broadcast command.

4.3.3.6.7.1 Bus controller to remote terminal(s) transfer (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field followed by the specified number of data words. The command word and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall, after message validation, set the broadcast command received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

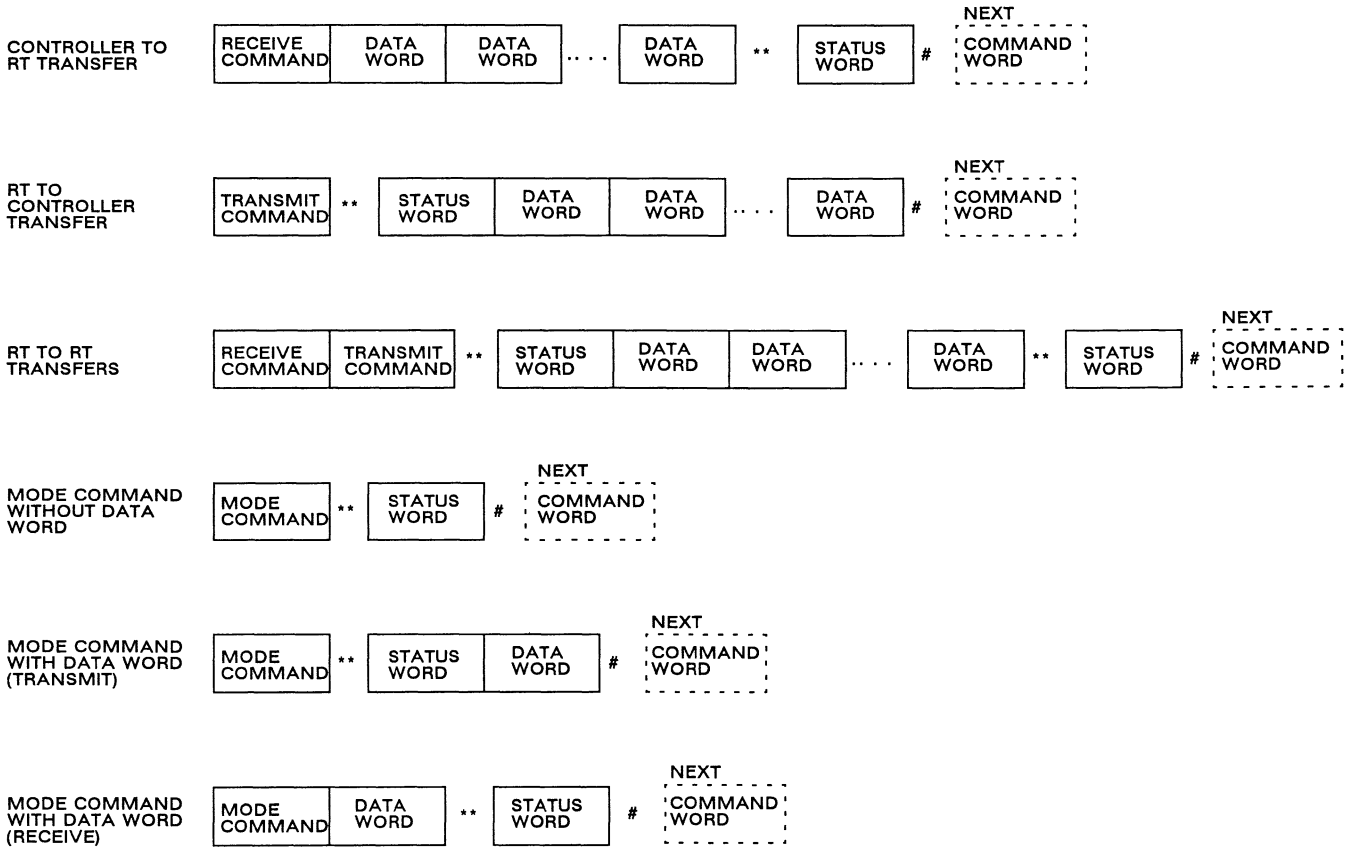


Figure 6. Information transfer formats

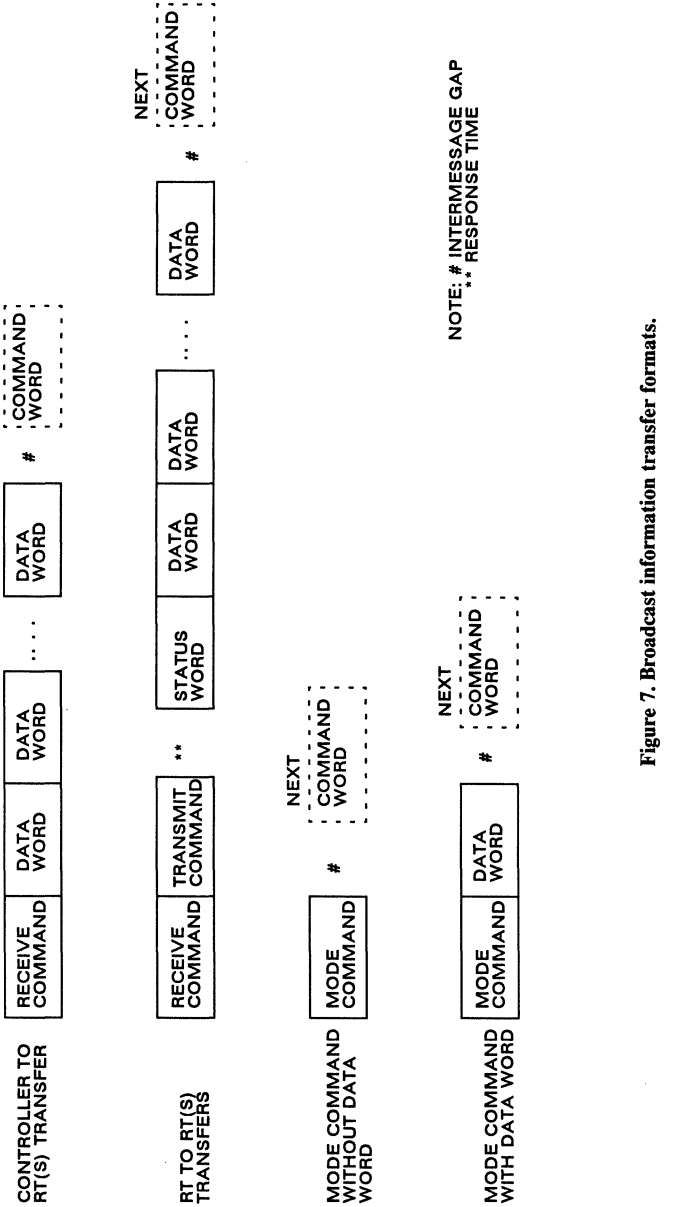


Figure 7. Broadcast information transfer formats.

4.3.3.6.7.2 Remote terminal to remote terminal(s) transfers (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field followed by a transmit command to RT A using the RT's address. RT A shall, after command word validation, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option, excluding RT A, shall, after message validation, set the broadcast received bit in the status word specified in 4.3.3.5.3.7 and shall not transmit the status word.

4.3.3.6.7.3 Mode command without data word (broadcast). The bus controller shall issue a transmit command word with 11111 in the RT address field, and a mode code specified in table I. The RT(s) with the broadcast option shall, after command word validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

4.3.3.6.7.4 Mode command with data word (broadcast). The bus controller shall issue a receive command word with 11111 in the RT address field and a mode code specified in table I, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall, after message validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

4.3.3.7 Intermessage gap. The bus controller shall provide a minimum gap time of 4.0 microseconds (μs) between messages as shown on figure 6 and figure 7. This time period, shown as T on figure 8, is measured at point A of the bus controller as shown on figure 9 or figure 10. The time is measured from the mid-bit zero crossing of the last bit of the preceding message to mid-zero crossing of the next command word sync.

4.3.3.8 Response time. The RT shall respond, in accordance with 4.3.3.6, to a valid command word within the time period of 4.0 to 12.0 μs. This time period, shown as T on figure 8, is measured at point A of the RT as shown on figure 9 or figure 10. The time is measured from the mid-bit zero crossing of the last word as specified in 4.3.3.6 and as shown on figure 6 and figure 7 to the mid-zero crossing of the status word sync.

4.3.3.9 Minimum no-response time-out. The minimum time that a terminal shall wait before considering that a response as specified in 4.3.3.8 has not occurred shall be 14.0 μs. The time is measured from the mid-bit zero crossing of the last bit of the last word to the mid-zero crossing of the expected status word sync at point A of the terminal as shown on figure 9 or figure 10.

4.4 Terminal operation.

4.4.1 Common operation. Terminals shall have common operating capabilities as specified in the following paragraphs.

A

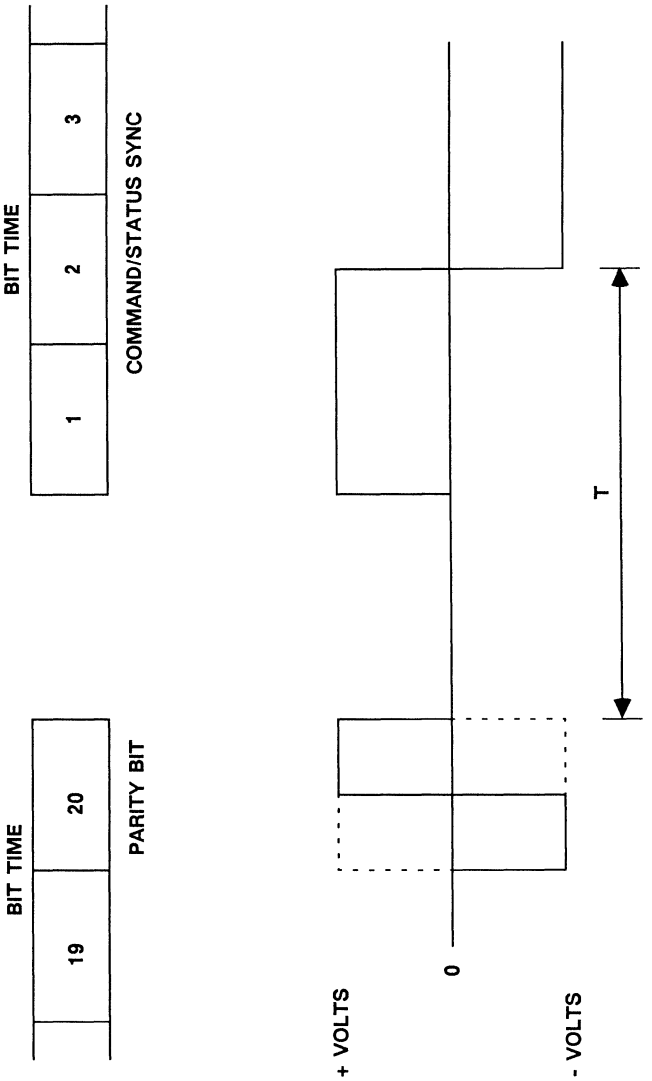


Figure 8. Intermessage gap and response time.

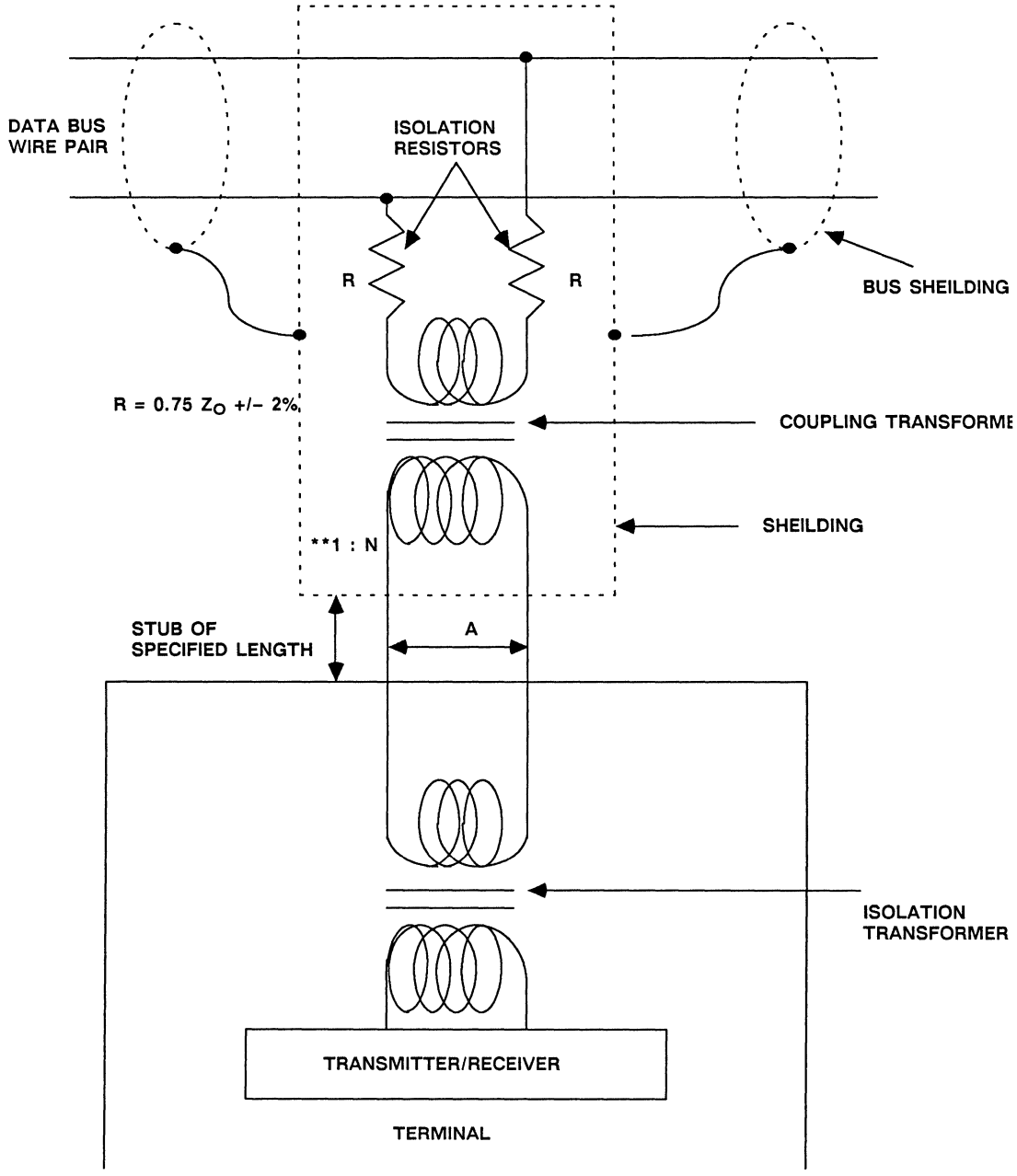


Figure 9. Data bus interface using transformer coupling.

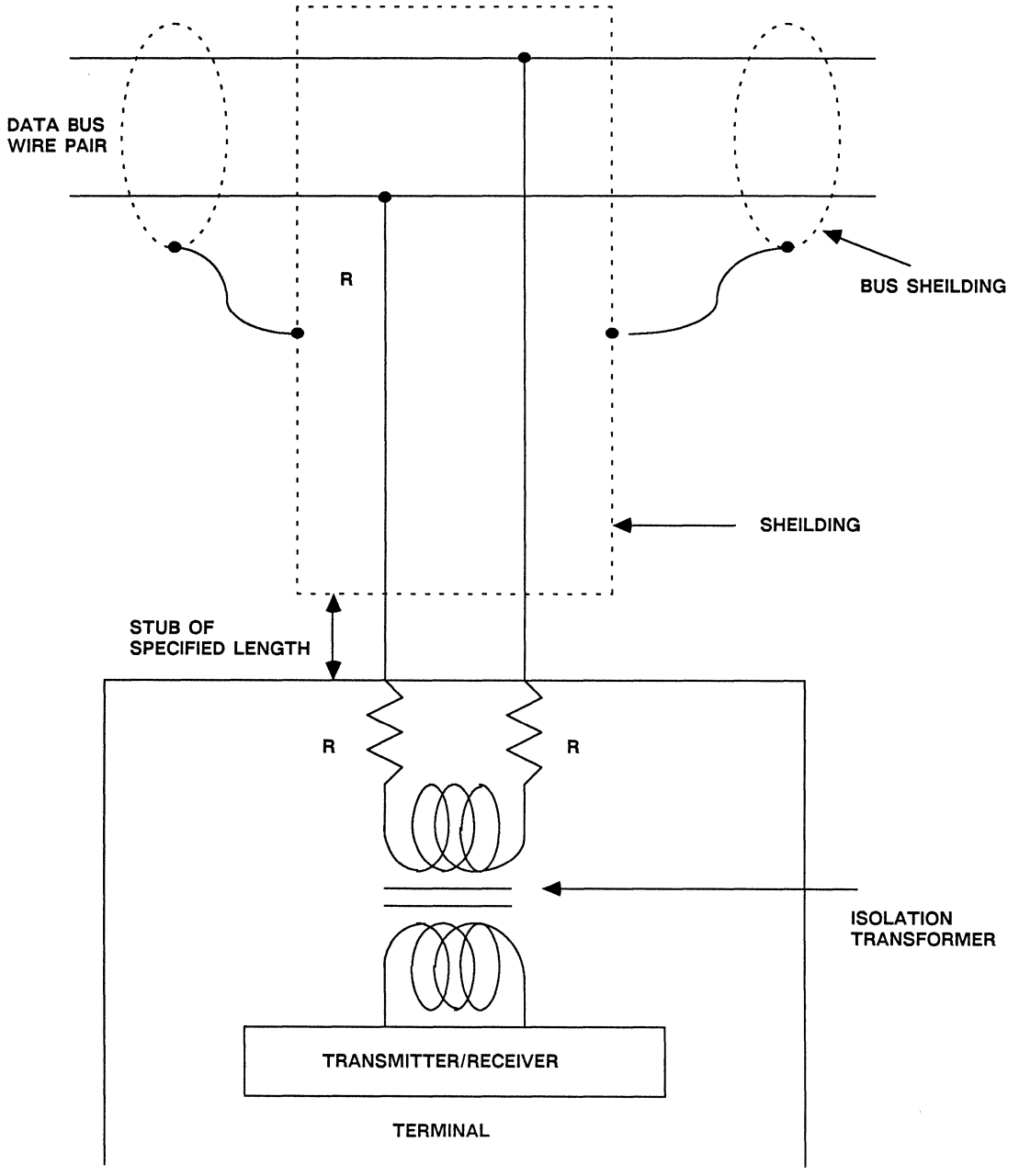


Figure 10. Data bus interface using direct coupling.

4.4.1.1 Word validation. The terminal shall insure that each word conforms to the following minimum criteria:

a. The word begins with a valid sync field.
b. The bits are in a valid Manchester II code.
c. The information field has 16 bits plus parity.
d. The word parity is odd.

When a word fails to conform to the preceding criteria, the word shall be considered invalid.

4.4.1.2 Transmission continuity. The terminal shall verify that the message is contiguous as defined in 4.3.3.6. Improperly timed data syncs shall be considered a message error.

4.4.1.3 Terminal fail-safe. The terminal shall contain a hardware implemented time-out to preclude a signal transmission of greater than 800.0 μs. This hardware shall not preclude a correct transmission in response to a command. Reset of this time-out function shall be performed by the reception of a valid command on the bus on which the time-out has occurred.

4.4.2 Bus controller operation. A terminal operating as a bus controller shall be responsible for sending data bus commands, participating in data transfers, receiving status responses, and monitoring system status as defined in this standard. The bus controller function may be embodied as either a stand-alone terminal, whose sole function is to control the data bus(s), or contained within a subsystem. Only one terminal shall be in active control of a data bus at any one time.

4.4.3. Remote terminal.

4.4.3.1 Operation. A remote terminal (RT) shall operate in response to valid commands received from the bus controller. The RT shall accept a command word as valid when the command word meets the criteria of 4.4.1.1, and the command word contains a terminal address which matches the RT address or an address of 11111, if the RT has the broadcast option.

4.4.3.2 Superseding valid commands. The RT shall be capable of receiving a command word on the data bus after the minimum intermessage gap time as specified in 4.3.3.7 has been exceeded, when the RT is not in the time period T as specified in 4.3.3.8 prior to the transmission of a status word, and when it is not transmitting on that data bus. A second valid command word sent to an RT shall take precedence over the previous command. The RT shall respond to the second valid command as specified in 4.3.3.8.

4.4.3.3 Invalid commands. A remote terminal shall not respond to a command word which fails to meet the criteria specified in 4.4.3.1.

4.4.3.4 Illegal command. An illegal command is a valid command as specified in 4.4.3.1 where the bits in the subaddress/mode field, data word count/mode code field, and the T/R bit indicate a mode command, subaddress, or word count that has not been implemented in the RT. It is the responsibility of the bus controller to assure that no illegal commands are sent out. The RT designer has the option of monitoring for illegal commands. If an RT that is designed with this option detects an illegal command and the proper number of contiguous valid data words as specified by the illegal command word, it shall respond with a status word only, setting the message error bit, and not use the information received.

4.4.3.5 Valid data reception. The remote terminal shall respond with a status word when a valid command word and the proper number of contiguous valid data words are received, or a single valid word associated with a mode code is received. Each data word shall meet the criteria specified in 4.4.1.1.

4.4.3.6 Invalid data reception. Any data word(s) associated with a valid receive command that does not meet the criteria specified in 4.4.1.1 and 4.4.1.2 or an error in the data word count shall cause the remote terminal to set the message error bit in the status word to a logic one and suppress the transmission of the status word. If a message error has occurred, then the entire message shall be considered invalid.

4.4.4 Bus monitor operation. A terminal operating as a bus monitor shall receive bus traffic and extract selected information. While operating as a bus monitor, the terminal shall not respond to any message except one containing its own unique address if one is assigned. All information obtained while acting as a bus monitor shall be strictly used for off-line applications (e.g., flight test recording, maintenance recording or mission analysis) or to provide the back-up bus controller sufficient information to take over as the bus controller.

4.5 Hardware characteristics.

4.5.1 Data bus characteristics.

4.5.1.1 Cable. The cable used for the main bus and all stubs shall be a two conductor, twisted, shielded, jacketed cable. The wire-to-wire distributed capacitance shall not exceed 30.0 picofarads per foot. The cables shall be formed with not less than four twists per foot where a twist is defined as a 360 degree rotation of the wire pairs; and, the cable shield shall provide a minimum of 75.0 percent coverage.

4.5.1.2 Characteristic impedance. The nominal characteristic impedance of the cable (Z_O) shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz (MHz).

4.5.1.3 Cable attenuation. At the frequency of 4.5.1.2, the cable power loss shall not exceed 1.5 decibels (dB)/100 feet (ft).

4.5.1.4 Cable termination. The two ends of the cable shall be terminated with a resistance, equal to the selected cable nominal characteristic impedance (Z_O) +/- 2.0 percent.

4.5.1.5 Cable stub requirements. The cable shall be coupled to the terminal as shown on figure 9 or figure 10. The use of long stubs is discouraged, and the length of a stub should be minimized. However, if installation requirements dictate, stub lengths exceeding those lengths specified in 4.5.1.5.1 and 4.5.1.5.2 are permissible.

4.5.1.5.1 Transformer coupled stubs. The length of a transformer coupled stub should not exceed 20 feet. If a transformer coupled stub is used, then the following shall apply.

4.5.1.5.1.1 Coupling transformer. A coupling transformer, as shown on figure 9, shall be required. This transformer shall have a turns ratio of 1:1.41 +/- 3.0 percent, with the higher turns on the isolation resistor side of the stub.

4.5.1.5.1.1.1 Transformer input impedance. The open circuit impedance as seen at point B on figure 11 shall be greater than 3000 ohms over the frequency range of 75.0 kilohertz (kHz) to 1.0 megahertz (MHz), when measured with a 1.0 V root-mean-square (RMS) sine wave.

4.5.1.5.1.1.2 Transformer waveform integrity. The droop of the transformer using the test configuration shown on figure 11 at point B shall not exceed 20.0 percent. Overshoot and ringing as measured at point B shall be less than +/- 1.0 V peak. For this test, R shall equal 360.0 ohms +/- 5.0 percent and the input A of figure 11 shall be a 250.0 kHz square wave. 27.0 V peak-to-peak, with a rise and fall time no greater than 100 nanoseconds (ns).

4.5.1.5.1.1.3 Transformer common mode rejection. The coupling transformer shall have a common mode rejection ratio greater than 45.0 dB at 1.0 MHz.

4.5.1.5.1.2 Fault isolation. As isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 0.75 Z_O ohms plus or minus 2.0 percent, where Z_O is the selected cable nominal characteristic impedance. The impedance placed across the data bus cable shall be no less than 1.5 Z_O ohms for any failure of the coupling transformer, cable stub, or terminal transmitter/receiver.

4.5.1.5.1.3 Cable coupling. All coupling transformers and isolation resistors, as specified in 4.5.1.5.1.1 and 4.5.1.5.1.2, shall have continuous shielding which will provide a minimum of 75 percent coverage. The isolation resistors and coupling transformers shall be placed at minimum possible distance from the junction of the stub to the main bus.

4.5.1.5.1.4 Stub voltage requirements. Every data bus shall be designed such that all stubs at point A of figure 9 shall have a peak-to-peak amplitude, line-to-line within the range of 1.0 and 14.0 V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance specified in 4.5.1.5.1.2 on the data bus. This shall also include the worse case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

4.5.1.5.2 Direct coupled stubs. The length of a direct coupled stub should not exceed 1 foot. Refer to 10.5 for comments concerning direct coupled stubs. If a direct coupled stub is used, then the following shall apply.

4.5.1.5.2.1 Fault isolation. An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 55.0 ohms plus or minus 2.0 percent. The isolation resistors shall be placed within the RT as shown on figure 10.

A

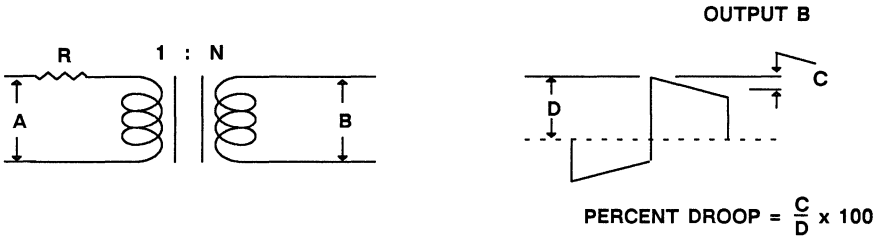


Figure 11. Coupling transformer.

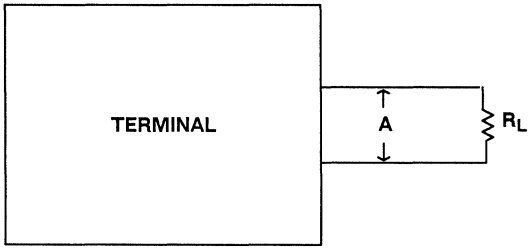


Figure 12. Terminal I/O characteristics for transformer coupled and direct coupled stubs.

4.5.1.5.2.2 Cable coupling. All bus-stub junctions shall have continuous shielding which will provide a minimum of 75 percent coverage.

4.5.1.5.2.3 Stub voltage requirements. Every data bus shall be designed such that all stubs at point A of figure 10 shall have a peak-to-peak amplitude, line-to-line within the range of 1.4 and 20.0 V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance of 110 ohms on the data bus. This shall also include the worst case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

4.5.1.5.3 Wiring and cabling for EMC. For purposes of electromagnetic capability (EMC), the wiring and cabling provisions of MIL-E-6051 shall apply.

4.5.2 Terminal characteristics.

4.5.2.1 Terminals with transformer coupled stubs.

4.5.2.1.1 Terminal output characteristics. The following characteristics shall be measured with R_L, as shown on figure 12, equal to 70.0 ohms +/- 2.0 percent.

4.5.2.1.1.1 Output levels. The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 18.0 to 27.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

4.5.2.1.1.2 Output waveform. The waveform, when measured at point A on figure 12, shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point, measured with respect to the previous zero crossing (i.e., .5 +/- .025 μs, 1.0 +/- .025 μs, 1.5 +/- .025 μs, and 2.0 +/- .025 μs). The rise and fall time of this waveform shall be from 100.0 to 300.0 ns when measured from levels of 10 to 90 percent of full waveform peak-to-peak, line-to-line, voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed +/- 900.0 millivolts (mV) peak, line-to-line, as measured at point A, figure 12.

4.5.2.1.1.3 Output noise. Any noise transmitted when the terminal is receiving or has power removed shall not exceed a value of 14.0 mV, RMS, line-to-line, as measured at point A, figure 12.

4.5.2.1.1.4 Output symmetry. From the time beginning 2.5 μs after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A of figure 12 shall be no greater than +/- 250.0 mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words it is designed to transmit, up to 33. This test shall be run six times with each word in a contiguous block of words having the same bit pattern. The six word contents that shall be used are 8000_{16}, $7FFF_{16}$, 0000_{16}, $FFFF_{16}$, 5555_{16}, and $AAAA_{16}$. The output of the terminal shall be as specified in 4.5.2.1.1.1 and 4.5.2.1.1.2.

4.5.2.1.2 Terminal input characteristics. The following characteristics shall be measured independently.

A

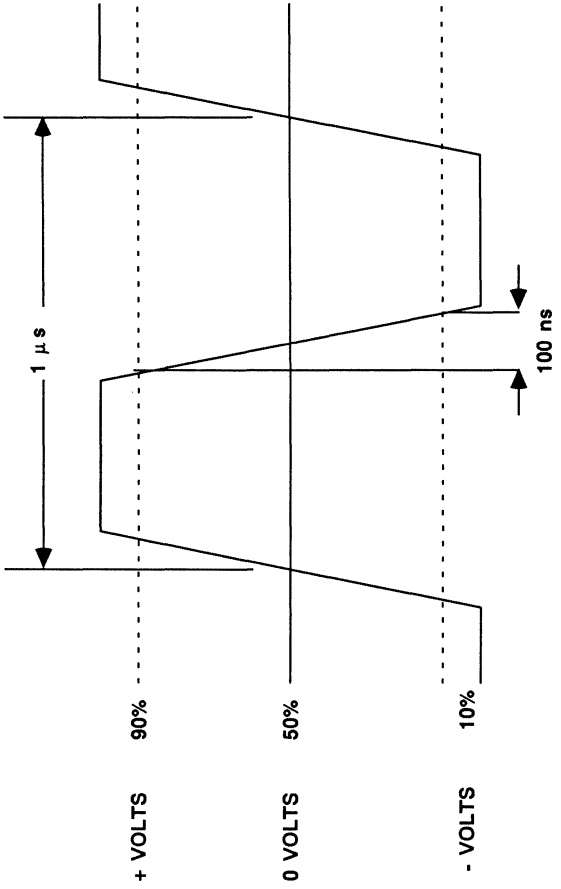


Figure 13. Output waveform.

4.5.2.1.2.1 Input waveform compatibility. The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with a maximum zero crossing deviation from the ideal with respect to the previous zero crossing of +/- 150 ns, (i.e., 2.0 +/- .15 μs, 1.5 +/- .15 μs, 1.0 +/- .15 μs, .5 +/- .15 μs). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of .86 to 14.0 V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .20 V. The voltages are measured at point A on figure 9.

4.5.2.1.2.2 Common mode rejections. Any signals from direct current (DC) to 2.0 MHz, with amplitudes equal to or less than +/- 10.0 V peak, line-to-ground, measured at point A on figure 9, shall not degrade the performance of the receiver.

4.5.2.1.2.3 Input impedance. The magnitude of the terminal input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 1000.0 ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A figure 9.

4.5.2.1.2.4 Noise rejection. The terminal shall exhibit a maximum word error rate of one part in 10^7, on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 140 mV. A word error shall include any fault which causes the message error bit to be set in the terminal's status word, or one which causes a terminal to not respond to a valid command. The word error rate shall be measured with a 2.1 V peak-to-peak, line-to-line, input to the terminal as measured at point A on figure 9. The noise tests shall be run continuously until, for a particular number of failures, the number of words received by the terminal, including both command and data words, exceeds the required number for acceptance of the terminal, or is less than the required number for rejection of the terminal, as specified in table II. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

4.5.2.2 Terminals with direct coupled stubs.

4.5.2.2.1 Terminal output characteristics. The following characteristics shall be measured with R_L, as shown on figure 12, equal to 35.0 ohms +/- 2.0 percent.

4.5.2.2.1.1 Output levels. The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 6.0 to 9.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

A

Table II. Criteria for acceptance or rejection of a terminal for the noise rejection test

No. of Errors	TOTAL WORDS RECEIVED BY THE TERMINAL (in multiples of 107) Reject (Equal or Less)	Accept (Equal or more)
0	N/A	4.40
1	N/A	5.21
2	N/A	6.02
3	N/A	6.83
4	N/A	7.64
5	N/A	8.45
6	.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	N/A

4.5.2.2.1.2 Output waveform. The waveform, when measured at point A on figure 12, shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point, measured with respect to the previous zero crossing (i.e., .5 +/- .025 μs, 1.0 +/- .025 μs, 1.5 +/- .025 μs and 2.0 +/- .025 μs). The rise and fall time of this waveform shall be from 100.0 to 300.0 ns when measured from levels of 10 to 90 percent of full waveform peak-to-peak, line-to-line, voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed +/- 300.0 mV peak, line-to-line, as measured at point A on figure 12.

4.5.2.2.1.3 Output noise. Any noise transmitted when the terminal is receiving or has power removed, shall not exceed a value of 5.0 mV, RMS, line-to-line, as measured at point A on figure 12.

4.5.2.2.1.4 Output symmetry. From the time beginning 2.5 μs after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A on figure 12 shall be no greater than + 90.0 mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words it is designed to transmit, up to 33. This test shall be run six times with each word in a contiguous block of words having the same bit pattern. The six word contents that shall be used are 8000_{16}, $7FFF_{16}$, 0000_{16}, $FFFF_{16}$, 5555_{16}, and $AAAA_{16}$. The output of the terminal shall be as specified in 4.5.2.2.1.1 and 4.5.2.2.1.2.

4.5.2.2.2 Terminal input characteristics. The following characteristics shall be measured independently.

4.5.2.2.2.1 Input waveform compatibility. The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with a maximum zero crossing deviation from the ideal with respect to the previous zero crossing of plus or minus 150 ns, (i.e., 2.0 +/- .15 μs 1.5 +/- .15 μs 1.0 +/- .15 μs .5 +/- .15 μs). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 1.2 to 20.0 V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .28 V. The voltages are measured at point A on figure 10.

4.5.2.2.2.2 Common mode rejections. Any signals from DC to 2.0 MHz, with amplitudes equal to or less than +/- 10.0 V peak, line-to-ground, measured at point A on figure 10, shall not degrade the performance of the receiver.

4.5.2.2.2.3 Input impedance. The magnitude of the terminal input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 2000.0 ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A on figure 10.

4.5.2.2.2.4 Noise rejection. The terminal shall exhibit a maximum word error rate of one part in 10^7, on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 200 mV. A word error shall include any fault which causes the message error bit to be set in the terminal's status word, or one which causes a terminal to not respond to a valid command. The word error rate shall be measured with a 3.0 V peak-to-peak, line-to-line, input to the terminal as measured at point A on figure 10. The noise tests shall be run continuously until, for a particular number of failures, the number of words received by the terminal, including both command and data words, exceeds the required number for acceptance of the terminal, or is less than the required number for rejection of the terminal, as specified in table II. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

A

4.6 Redundant data bus requirements. If redundant data buses are used, the requirements as specified in the following shall apply to those data buses.

4.6.1 Electrical isolation. All terminals shall have a minimum of 45 db isolation between data buses. Isolation here means the ratio in db between the output voltage on the active data bus and the output voltage on the inactive data bus. This shall be measured using the test configuration specified in 4.5.2.1.1 or 4.5.2.2.1 for each data bus. Each data bus shall be alternately activated with all measurements being taken at point A on figure 12 for each data bus.

4.6.2 Single event failures. All data buses shall be routed to minimize the possibility that a single event failure to a data bus shall cause the loss of more than that particular data bus.

4.6.3 Dual standby redundant data bus. If a dual redundant data bus is used, then it shall be a dual standby redundant data bus as specified in the following paragraphs.

4.6.3.1 Data bus activity. Only one data bus can be active at any given time except as specified in 4.6.3.2.

4.6.3.2 Reset data bus transmitter. If while operating on a command, a terminal receives another valid command, from either data bus, it shall reset and respond to the new command on the data bus on which the new command is received. The terminal shall respond to the new command as specified in 4.3.3.8.

5. DETAIL REQUIREMENTS (Not Applicable)

Custodian:
Army - EL
Navy - AS
Air Force - 11

Preparing Activity:
Air Force - 11

Project MISC-0D03

APPENDIX

10. General. The following paragraphs in this appendix are presented in order to discuss certain aspects of the standard in a general sense. They are intended to provide a user of the standard more insight into the aspects discussed.

10.1 Redundancy. It is intended that this standard be used to support rather than to supplant the system design process. However, it has been found, through application experience in various aircraft, that the use of a dual standby redundancy technique is very desirable for use in integrating mission avionics. For this reason, this redundancy scheme is defined in 4.6 of this standard. Nonetheless, the system designer should utilize this standard as the needs of a particular application dictate. The use of redundancy, the degree to which it is implemented, and the form which it takes must be determined on an individual application basis. Figures 10.1 and 10.2 illustrate some possible approaches to dual redundancy. These illustrations are not intended to be inclusive, but rather representative. It should be noted that analogous approaches exist for the triple and quad redundant cases.

10.2 Bus controller. The bus controller is a key part of the data bus system. The functions of the bus controller, in addition to the issuance of command, must include the constant monitoring of the data bus and traffic on the bus. It is envisioned that most of the routine minute details of bus monitoring (e.g., parity checking, terminal non-response time-out, etc.) will be embodied in hardware, while the algorithms for bus control and decision making will reside in software. It is also envisioned that, in general, the bus controller will be a general purpose airborne computer with a special input/output (I/O) to interface with the data bus. It is of extreme importance in bus controller design that the bus controller be readily able to accommodate terminals of differing protocols and status word bits used. Equipment designed to MIL-STD-1553A will be in use for a considerable period of time; thus, bus controllers must be capable of adjusting to their differing needs. It is also important to remember that the bus controller will be the focal point for modification and growth within the multiplex system, and thus the software must be written in such a manner as to permit modification with relative ease.

A

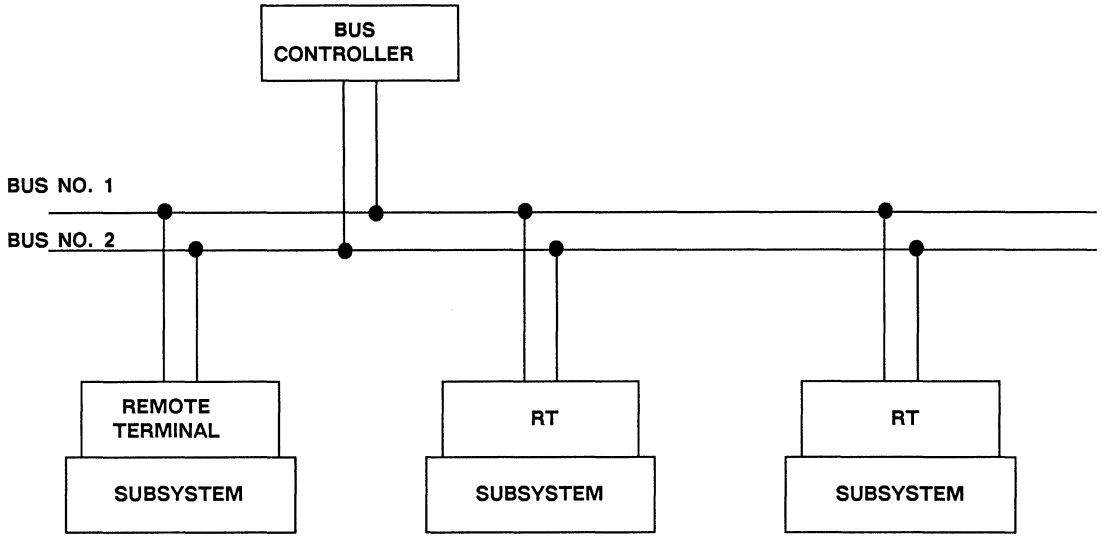
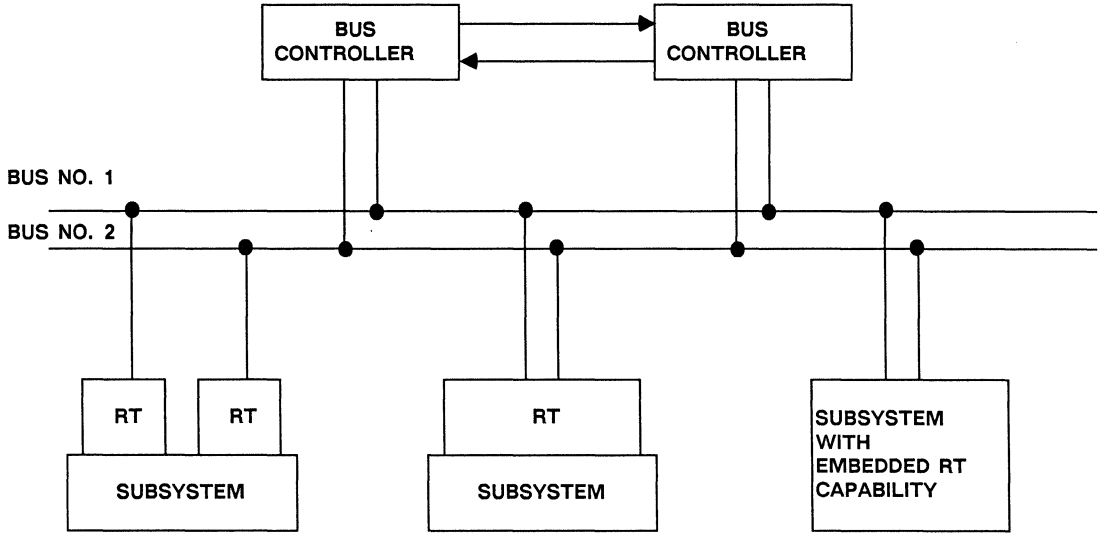


Figure 10.1. Illustration of possible redundancy.



NOTE: RT - Remote Terminal

Figure 10.2. Illustration of possible redundancy.

10.3 Multiplex selection criteria. The selection of candidate signals for multiplexing is a function of the particular application involved, and criteria will in general vary from system to system. Obviously, those signals which have bandwidths of 400 Hz or less are prime candidates for inclusion on the bus. It is also obvious that video, audio, and high speed parallel digital signals should be excluded. The area of questionable application is usually between 400 Hz and 3 kHz bandwidth. The transfer of these signals on the data bus will depend heavily upon the loading of the bus in a particular application. The decision must be based on projected future bus needs as well as the current loading. Another class of signals which in general are not suitable for multiplexing are those which can be typified by a low rate (over a mission) but possessing a high priority or urgency. Examples of such signals might be a nuclear event detector output or a missile launch alarm from a warning receiver. Such signals are usually better left hardwired, but they may be accommodated by the multiplex system if a direct connection to the bus controller's interrupt hardware is used to trigger a software action in response to the signal.

10.4 High reliability requirements. The use of simple parity for error detection within the multiplex bus system was dictated by a compromise between the need for reliable data transmission, system overhead, and remote terminal simplicity. Theoretical and empirical evidence indicates that an undetected bit error rate of 10^{-12} can be expected from a practical multiplex system built to this standard. If a particular signal requires a bit error rate which is better than that provided by the parity checking, then it is incumbent upon the system designer to provide the reliability within the constraints of the standard or to not include this signal within the multiplex bus system. A possible approach in this case would be to have the signal source and sink provide appropriate error detection and correction encoding/decoding and employ extra data words to transfer the information. Another approach would be to partition the message, transmit a portion at a time, and then verify (by interrogation) the proper transfer of each segment.

10.5 Stubbing. Stubbing is the method wherein a separate line is connected between the primary data bus line and a terminal. The direct connection of a stub line causes a mismatch which appears on the waveforms. This mismatch can be reduced by filtering at the receiver and by using bi-phase modulation. Stubs are often employed not only as a convenience in bus layout but as a means of coupling a unit to the line in such a manner that a fault on the stub or terminal will not greatly affect the transmission line operation. In this case, a network is employed in the stub line to provide isolation from the fault. These networks are also used for stubs that are of such length that the mismatch and reflection degrades bus operation. The preferred method of stubbing is to use transformer coupled stubs, as defined in 4.5.1.5.1. This method provides the benefits of DC isolation, increased common mode protection, a doubling of effective stub impedance, and fault isolation for the entire stub and terminal. Direct coupled stubs, as defined in 4.5.1.5.2 of this standard, should be avoided if at all possible. Direct coupled stubs provide no DC isolation or common mode rejection for the terminal external to its subsystem. Further, any shorting fault between the subsystem's internal isolation resistors (usually on a circuit board) and the main bus junction will cause failure of that entire bus. It can be expected that when the direct coupled stub length exceeds 1.6 feet, it will begin to distort the main bus waveforms. Note that this length includes the cable runs internal to a given subsystem.

10.6 Use of broadcast option. The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

NOTICE 1

A

MIL-STD-1553B
NOTICE 1(USAF)
12 February 1980

MILITARY STANDARD

AIRCRAFT INTERNAL TIME DIVISION
COMMAND/RESPONSE MULTIPLEX DATA BUS

TO ALL HOLDERS OF MIL-STD-1553B.

1. THE FOLLOWING PAGES OF MIL-STD-1553B HAVE BEEN REVISED AND SUPERSEDE PAGES LISTED:

NEW PAGE	SUPERSEDED PAGE	DATE
iii	iii	21 September 1978
viii	viii	21 September 1978
34	34	21 September 1978

2. THE FOLLOWING NEW PAGES ARE TO BE INSERTED AS LISTED:

NEW PAGE

viiia
35

3. RETAIN THIS NOTICE PAGE AND INSERT BEFORE THE TABLE OF CONTENTS.

4. Holders of MIL-STD-1553B will verify that page changes indicated above have been entered. The notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the Military Standard is completely revised or cancelled.

5. This notice is applicable to all U.S. Air Force internal avionics activities.

A

Custodian:
Air Force - 11

Preparing activity
Air Force - 11

Project MISC-FD32

*U.S. GOVERNMENT PRINTING OFFICE: 1980-603-121/1244

FSC MISC

FOREWARD

This standard contains requirements for aircraft internal time division command/response multiplex data bus techniques which will be utilized in systems integration of aircraft subsystems. Even with the use of this standard, subtle differences will exist between multiplex data buses used on different aircraft due to particular aircraft mission requirements and the designer options allowed in this standard. The system designer must recognize this fact, and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist, so as to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architecture redundancy, degradation concept and traffic patterns peculiar to the specific aircraft mission requirements. * Appendix Section 20 selects those options which shall be required and further restricts certain portions of the standard for use in Air Force aircraft internal avionics applications.

FIGURES

TABLES

APPENDIX

Paragraph Page

APPENDIX FIGURES

10.6 Use of broadcast option. The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

*20. General. This appendix is applicable to all U.S. Air Force aircraft internal avionics activities. The intent of the appendix is to select those options which shall be required and to further restrict certain portions of the standard for use in Air Force avionics. References in parenthesis are to the paragraphs in the standard that are affected.

*20.1 Mode codes. (4.3.3.5.1.7) The mode codes for dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown and override selected transmitter shutdown shall not be transmitted on the data bus by bus controllers in Air Force avionics applications. However, these mode codes may be implemented in a remote terminal for Air Force avionics applications.

*20.2 Broadcast command. (4.3.3.6.7) The broadcast command shall not be transmitted on the data bus by bus controllers in Air Force avionics applications. However, this message format may be implemented in remote terminals. If the broadcast message format is implemented in a remote terminal, then that terminal shall also implement the transmit status word mode code as specified in 4.3.3.5.1.7.3. Note that the remote terminal address of 11111 is still reserved for broadcast, and shall not be used for any other purpose in Air Force Avionics applications.

*20.3 Mode code indicators.

*20.3.1 Bus controller. (4.4.2) In Air Force avionics applications, the bus controller shall be able to utilize both 00000 and 11111 in the subaddress/mode field as defined in 4.3.3.5.1.7. In addition, if a bus controller is required to utilize any mode code in its operation, then it shall be required to implement the capacity to utilize all mode codes.

*20.3.2 Remote terminals. (4.4.3.1) All RT's which are designed for Air Force avionics applications, and which implement mode codes, shall respond properly to a mode code command, as defined in 4.3.3.5.1.7, with 00000 in the subaddress/mode field. In addition, such RT's may also respond to 11111 in the subaddress/mode field as a designer option. See section 20.8.1 for design consideration relating to the 11111 mode code indicator.

Supersedes page 34 of 21 September 1978

A

*20.4 Data bus cable.

*20.4.1 Shielding. (4.5.1.1) The cable shield shall provide a minimum of 90.0 percent coverage.

*20.4.2 Characteristic impedance. (4.5.1.2) The actual (not nominal) characteristic impedance shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz (MHz).

*20.5 Cable coupling. (4.5.1.5.1.3) For Air Force avionics applications, the continuous shielding shall provide a minimum of 90.0 percent coverage.

*20.6 Direct coupled stubs. (4.5.1.5.2) Direct coupled studs shall not be utilized in Air Force avionics applications.

*20.7 Redundant data bus requirements. (4.6) Dual standby redundant data buses as defined in 4.6.3 shall be utilized. There may be more than two data buses utilized but the buses must operate in dual redundant data bus pairs. 4.6.1 add 4.6.2 shall also apply.

*20.8 Design considerations. Avionics designed for Air Forces applications may be required to interface to existing avionics systems which were designed to preceding versions of the standard (e.g., the F-16 avionics suite). In this case, downward compatibility problems between the new avionics and the existing system can be minimized through the consideration of three key items:

*20.8.1. Mode code indicator. In some existing systems, such as the F-16, the bus controller uses 11111 to indicate a mode code command. The designer may wish to implement the capability in the new avionics to respond to 11111 mode code commands, in addition to the required capability for 00000 mode code commands.

*20.8.2 Clock stability. Since this version of the standard relaxed the transmission bit rate stability requirements (4.3.3.3), the avionics designer may wish to return to the stability requirements of the preceding version of the standard. The previous requirements were + /-0.01 percent long term and + /-0.001 percent short term stability.

*20.8.3 Response time. This version of the standard also expanded the maximum response time to 12.0 microseconds (4.3.3.8). The designer may also wish to return to the previous maximum response time of 7.0 microseconds as defined in 4.3.3.8 of this version of the standard.

NOTICE 2

A

MIL-STD-1553B
NOTICE 2
8 September 1986
SUPERSEDING
NOTICE 1
12 February 1980

MILITARY STANDARD

DIGITAL TIME DIVISION

COMMAND/RESPONSE MULTIPLEX DATA BUS

TO ALL HOLDERS OF MIL-STD-1553B:

1. MAKE THE FOLLOWING PEN AND INK CHANGES:

Page i

Delete title and substitute: "DIGITAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS".

Page ii

Delete title and substitute: "DIGITAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS".

Page 1

Paragraph 1.1, second line: Delete "on aircraft".
Paragraph 1.2, third line: Delete "an aircraft" and substitute "a".

Page 3

Paragraph 3.11, first line, after "Bus controller": Insert "(BC)".
Paragraph 3.12, first line, after "Bus monitor": Insert "(BM)".

Page 21

Paragraph 4.4.3.1, add: "No combination of RT address bits, T/R bit, subaddress/mode bits, and data word count/mode code bits of a command word shall result in invalid transmissions by the RT. Subsequent valid commands shall be properly responded to by the RT."

Page 30

Paragraph 4.6.3.2, first line: Delete "Reset data bus transmitter" and substitute "Superseding valid commands".
Paragraph 4.6.3.2, second line: Delete "from either data bus" and substitute "from the other data bus".

Page 31

Paragraph 10.2, eighth line: Delete "airborne".

A

FSC MCCR

2. THE FOLLOWING PAGES OF MIL-STD-1553B HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGES	DATE	SUPERSEDED PAGE	DATE
iii	8 September 1986	iii	12 February 1980
iv	8 September 1986	iv	21 September 1978
vii	8 September 1986	vii	21 September 1978
viii	8 September 1986	viii	12 February 1980
viiia	8 September 1986	viiia	12 February 1980
33	21 September 1978	33	Reprinted Without Change
34	8 September 1986	34	12 February 1980
35	8 September 1986	35	12 February 1980
36	8 September 1986	INITIAL PUBLICATION	
37	8 September 1986	INITIAL PUBLICATION	
38	8 September 1986	INITIAL PUBLICATION	

3. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

4. Holders of MIL-STD-1553B will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or cancelled.

Custodians
Army - ER
Navy - AS
Air Force - 11

Preparing activity:
Air Force - 11

Project No. MCCR-0008

FOREWORD

This standard contains requirements for a digital time division command/response multiplex data bus for use in systems integration. Even with the use of this standard, differences may exist between multiplex data buses in different system applications due to particular application requirements and the designer options allowed in this standard. The system designer must recognize this fact and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architectural redundancy, degradation concept and traffic patterns peculiar to the specific application requirements. Appendix, Section 30 selects those options which shall be required and further restricts certain portions of the standard for the use in all dual standby redundant applications for the Army, Navy, and Air Force.

Supersedes page iii dated 12 February 1980.

CONTENTS

Supersedes page iv dated 21 September 1978.

CONTENTS (Cont'd)

A

CONTENTS (Cont'd)

CONTENTS (Cont'd)

A

Supersedes page vii dated 21 September 1978.

CONTENTS (Cont'd)

Supersedes page viii dated 12 February 1980.

CONTENTS (Cont'd)

APPENDIX FIGURES

A

Supersedes page viiia dated 12 February 1980.

10.3 Multiplex selection criteria. The selection of candidate signals for multiplexing is a function of the particular application involved, and criteria will in general vary from system to system. Obviously, those signals which have bandwidths of 400 Hz or less are prime candidates for inclusion on the bus. It is also obvious that video, audio, and high speed parallel digital signals should be excluded. The area of questionable application is usually between 400 Hz and 3 kHz bandwidth. The transfer of these signals on the data bus will depend heavily upon the loading of the bus in a particular application. The decision must be based on projected future bus needs as well as the current loading. Another class of signals which in general are not suitable for multiplexing are those which can be typified by a low rate (over a mission) but possessing a high priority or urgency. Examples of such signal might be a nuclear event detector output or a missile launch alarm from a warning receiver. Such signals are usually better left hardwired, but they may be accommodated by the multiplex system if a direct connection to the bus controller's interrupt hardware is used to trigger a software action in response to the signal.

10.4 High reliability requirements. The use of simple parity for error detection within the multiplex bus system was dictated by a compromise between the need for reliable data transmission, system overhead, and remote terminal simplicity. Theoretical and empirical evidence indicates that an undetected bit error rate of 10^{-12} can be expected from a practical multiplex system built to this standard. If a particular signal requires a bit error rate which is better than that provided by the parity checking, then it is incumbent upon the system designer to provide the reliability within the constraints of the standard or to not include this signal within the multiplex bus system. A possible approach in this case would be to have the signal source and sink provide appropriate error detection and correction encoding/decoding and employ extra data words to transfer the information. Another approach would be to partition the message, transmit a portion at a time, and then verify (by interrogation) the proper transfer of each segment.

10.5 Stubbing. Stubbing is the method wherein a separate line is connected between the primary data bus line and a terminal. The direct connection of a stub line causes a mismatch which appears on the waveforms. This mismatch can be reduced by filtering at the receiver and by using bi-phase modulation. Stubs are often employed not only as a convenience in bus layout but as a means of coupling a unit to the line in such a manner that a fault on the stub or terminal will not greatly affect the transmission line operation. In this case, a network is employed in the stub line to provide isolation from the fault. These networks are also used for stubs that are of such length that the mismatch and reflection degrades bus operation. The preferred method of stubbing is to use transformer coupled stubs, as defined in 4.5.1.5.1. This method provides the benefits of DC isolation, increased common mode protection, a doubling of effective stub impedance, and fault isolation for the entire stub and terminal. Direct coupled stubs, as defined in 4.5.1.5.2 of this standard, should be avoided if at all possible. Direct coupled stubs provide no DC isolation or common mode rejection for the terminal external to its subsystem. Further, any shorting fault between the subsystem's internal isolation resistors (usually on a circuit board) and the main bus junction will cause failure of that entire bus. It can be expected that when the direct coupled stub length exceeds 1.6 feet, that it will begin to distort the main bus waveforms. Note that this length includes the cable runs internal to a given subsystem.

* 10.6 Use of broadcast option. The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast option. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

* 10.7 Other related documents. Several documents exist which are related to this standard. MIL-HDBK-1553 describes implementation practices for this standard and other related data. This standard is embodied in or referenced by the following international documents: NATO STANAG 3838, ASCC Air Standard 50/2, and UK DEF STAN 00-18 (Part 2)/Issue 1.

* 20. REFERENCED DOCUMENTS

Not applicable.

* 30. GENERAL REQUIREMENTS

* 30.1 Option selection. This section of the appendix shall select those options required to further define portions of the standard to enhance tri-service interoperability. References in parentheses are to paragraphs in this standard which are affected.

* 30.2 Application. Section 30 of this appendix shall apply to all dual standby redundant applications for the Army, Navy, and Air Force. All Air Force aircraft internal avionics applications shall be dual standby redundant, except where safety critical or flight critical requirements dictate a higher level of redundancy.

* 30.3 Unique address (4.3.3.5.1.2). All remote terminals shall be capable of being assigned any unique address from decimal address 0 (00000) through decimal address 30 (11110). The address shall be established through an external connector, which is part of the system wiring and connects to the remote terminal. Changing the unique address of a remote terminal shall not require the physical modification or manipulation of any part of the remote terminal. The remote terminal shall, as a minimum, determine and validate its address during power-up conditions. No single point failure shall cause a terminal to validate a false address. The remote terminal shall not respond to any messages if it has determined its unique address is not valid.

A

Supersedes page 34 dated 12 February 1980.

* 30.4 Mode codes (4.3.3.5.1.7)

* 30.4.1 Subaddress/mode (4.3.3.5.1.4). An RT shall have the capability to respond to mode codes with both subaddress/mode of 00000 and 11111. Bus controllers shall have the capability to issue mode commands with both subaddress/mode of 00000 and 11111. The subaddress/mode of 00000 and 11111 shall not convey different information.

* 30.4.2 Required mode codes (4.3.3.5.1.7)

* 30.4.2.1 Remote terminal required mode codes. An RT shall implement the following mode codes as a minimum:

Mode Code	Function
00010	Transmit status word
00100	Transmitter shutdown
00101	Override transmitter shutdown
01000	Reset remote terminal

* 30.4.2.2 Bus controller required mode codes. The bus controller shall have the capability to implement all of the mode codes as defined in 4.3.3.5.1.7. For Air Force applications, the dynamic bus control mode command shall never be issued by the bus controller.

* 30.4.3 Reset remote terminal (4.3.3.5.1.7.9). An RT receiving the reset remote terminal mode code shall respond with a status word as specified in 4.3.3.5.1.7.9 and then reset. While the RT is being reset, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is being reset, the information content of the data shall be valid. An RT receiving this mode code shall complete the reset function within 5.0 milliseconds following transmission of the status word specified in 4.3.3.5.1.7.9. The time shall be measured from the mid-bit zero crossing of the parity bit of the status word to the mid-sync zero crossing of the command word at point A on figures 9 and 10.

* 30.4.4 Initiate RT self test (4.3.3.5.1.7.4). If the initiate self test mode command is implemented in the RT, then the RT receiving the initiate self test mode code shall respond with a status word as specified in 4.3.3.5.1.7.4 and then initiate the RT self test function. Subsequent valid commands may terminate the self test function. While the RT self test is in progress, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is in self test, the information content of the data shall be valid. An RT receiving this mode code shall complete the self test function and have the results of the self test available within 100.0 milliseconds following transmission of the status word specified in 4.3.3.5.1.7.4. The time shall be measured from the mid-bit zero crossing of the parity bit of the status word to the mid-sync zero crossing of the command word at point A on figures 9 and 10.

* 30.5 Status word bits (4.3.3.5.3)

30.5.1 Information content. The status word transmitted by an RT shall contain valid information at all times, e.g., following RT power up, during initialization, and during normal operation.

* 30.5.2 Status bit requirements (4.3.3.5.3). An RT shall implement the status bits as follows:

Message error bit (4.3.3.5.3.3) - Required

Instrumentation bit (4.3.3.5.3.4) - Always logic zero

Service request bit (4.3.3.5.3.5) - Optional

Reserved status bits (4.3.3.5.3.6) - Always logic zero

Broadcast command received bit (4.3.3.5.3.7) - If the RT implements the broadcast option, then this bit shall be required.

Busy bit (4.3.3.5.3.8) - As required by 30.5.3

Subsystem flag bit (4.3.3.5.3.9) - If an associated subsystem has the capability for self test, then this bit shall be required.

Dynamic bus control acceptance bit (4.3.3.5.3.10) - If the RT implements the dynamic bus control function, then this bit shall be required.

Terminal flag bit (4.3.3.5.3.11) - If an RT has the capability for self test, then this bit shall be required.

* 30.5.3 Busy bit (4.3.3.5.3.8). The existence of busy conditions is discouraged. However, any busy condition in the RT or the subsystem interface that would affect communication over the bus shall be conveyed via the busy bit. Busy conditions, and thus the setting of the busy bit, shall occur only as a result of particular commands/messages sent to an RT. Thus for a non-failed RT, the bus controller can, with prior knowledge of the remote terminal characteristics, determine when the remote terminal can become busy and when it will not be busy. However, the RT may also set the busy bit (in addition to setting the terminal flag bit or subsystem flag bit) as a result of failure/fault conditions within the RT/subsystem.

* 30.6 Broadcast (4.3.3.6.7). The only broadcast commands allowed to be transmitted on the data bus by the bus controller shall be the broadcast mode commands identified in table 1. The broadcast option may be implemented in remote terminals. However, if implemented, the RT shall be capable of distinguishing between a broadcast and a non-broadcast message to the same subaddress for non-mode command messages. The RT address of 11111 is still reserved for broadcast and shall not be used for any other purpose.

A

* 30.7 Data wrap-around (4.3.3.5.1.4). Remote terminals shall provide a receive subaddress to which one to N data words of any bit pattern can be received. Remote terminals shall provide a transmit subaddress from which a minimum of N data words can be transmitted. N is equal to the maximum word count from the set of all messages defined for the RT. A valid receive message to the data wrap-around receive subaddress followed by a valid transmit command to the data wrap-around transmit subaddress, with the same word count and without any intervening valid commands to that RT, shall cause the RT to respond with each data word having the same bit pattern as the corresponding received data word. A data wrap-around receive and transmit subaddress of 30 (11110) is desired.

* 30.8 Message formats (4.3.3.6). Remote terminals shall, as a minimum, implement the following non-broadcast message formats as defined in 4.3.3.6: RT to BC transfers, BC to RT transfers, RT to RT transfers (receive and transmit), and mode command without data word transfers. For non-broadcast messages, the RT shall not distinguish between data received during a BC to RT transfer or data received during a RT to RT transfer (receive) to the same subaddress. The RT shall not distinguish between data to be transmitted during an RT to BC transfer or data to be transmitted during an RT to RT transfer (transmit) from the same subaddress. Bus controllers shall have the capability to issue all message formats defined in 4.3.3.6.

* 30.9 RT to RT validation (4.3.3.9). For RT to RT transfers, in addition to the validation criteria specified in 4.4.3.6, if a valid receive command is received by the RT and the first data word is received after 57.0 plus or minus 3.0 microseconds, the RT shall consider the message invalid and respond as specified in 4.4.3.6. The time shall be measured from the mid-bit zero crossing of the parity bit of the receive command to the mid-sync zero crossing of the first expected data word at point A as shown on figures 9 and 10. It is recommended that the receiving RT of an RT to RT transfer verify the proper occurrence of the transmit command word and status word as specified in 4.3.3.6.3.

* 30.10 Electrical characteristics (4.5)

* 30.10.1 Cable shielding (4.5.1.1). The cable shield shall provide a minimum of 90.0 percent coverage.

* 30.10.2 Shielding (4.5.1). All cable to connector junctions, cable terminations, and bus-stub junctions shall have continuous 360 degree shielding which shall provide a minimum of 75.0 percent coverage.

* 30.10.3 Connector polarity. For applications that use concentric connectors or inserts for each bus, the center pin of the connector or insert shall be used for the high (positive) Manchester bi-phase signal. The inner ring shall be used for the low (negative) Manchester bi-phase signal.

* 30.10.4 Characteristic impedance (4.5.1.2). The actual (not nominal) characteristic impedance of the data bus cable shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz.

* 30.10.5 Stub coupling (4.5.1.5). For Navy applications, each terminal shall have both transformer and direct coupled stub connections externally available. For Navy systems using these terminals, either transformer or direct coupled connections may be used. For Army and Air Force applications, each terminal shall have transformer coupled stub connections, but may also have direct coupled stub connections. For Army and Air Force systems, only transformer coupled stub connections shall be used. Unused terminal connections shall have a minimum of 75 percent shielding coverage.

* 30.10.6 Power on/off noise. A terminal shall limit any spurious output during a power-up or power-down sequence. The maximum allowable output noise amplitude shall be +/- 250 mV peak, line-to-line for transformer coupled stubs and +/- 90 mV peak, line-to-line for direct coupled stubs, measured at point A of figure 12.

Notes

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

1575 Garden of the Gods Road
Colorado Springs, Colorado 80907-3486 USA
719-594-8081 or 800-722-1575

Printed in USA. UTMC publication 1553-PH-1-7-91